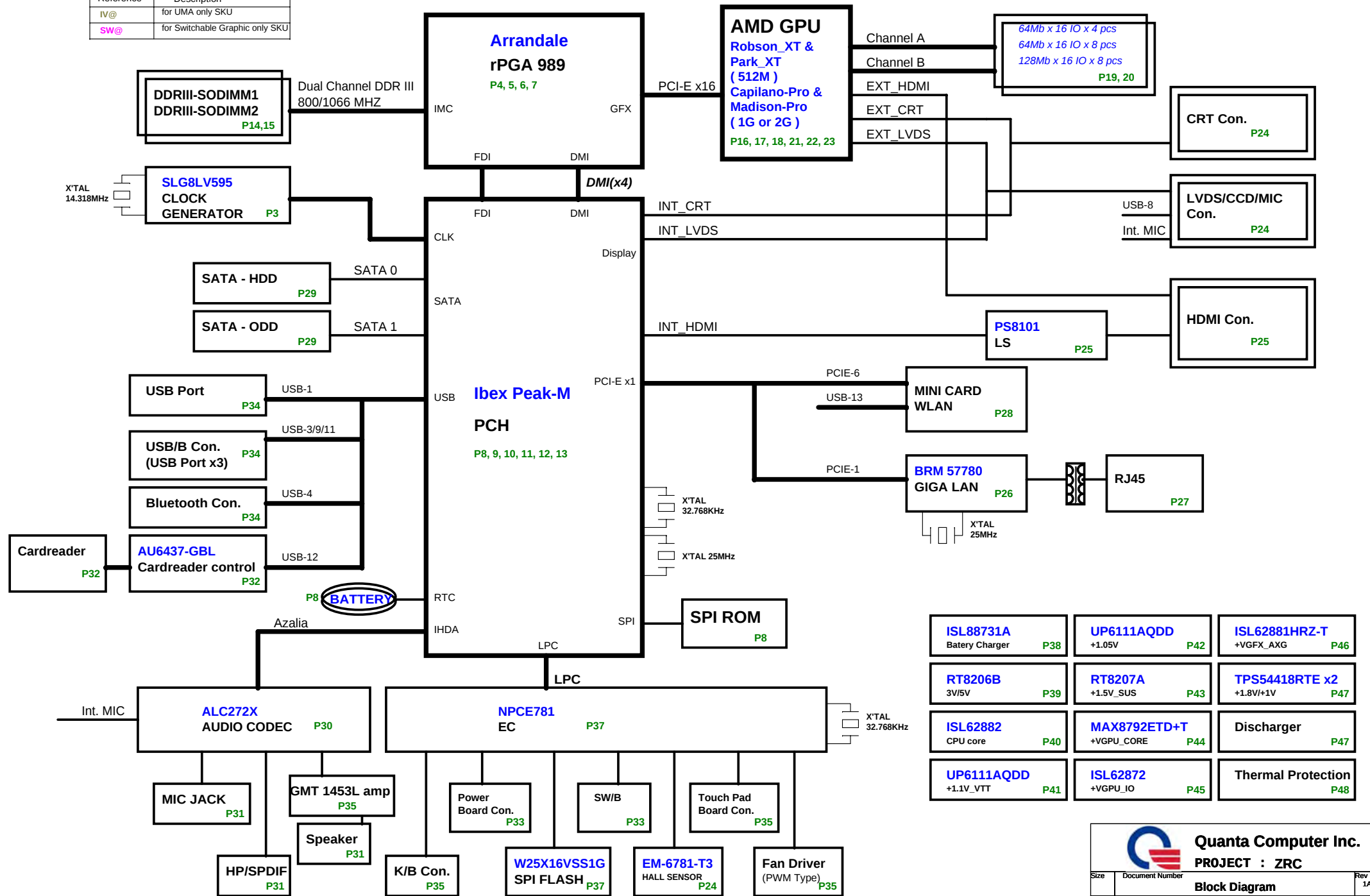


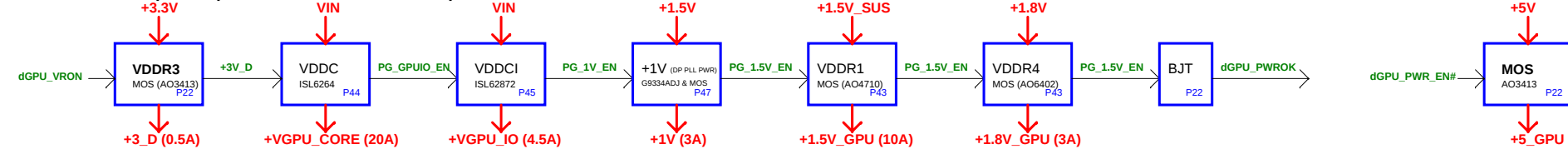
ZRC SYSTEM BLOCK DIAGRAM

BOM Option Table

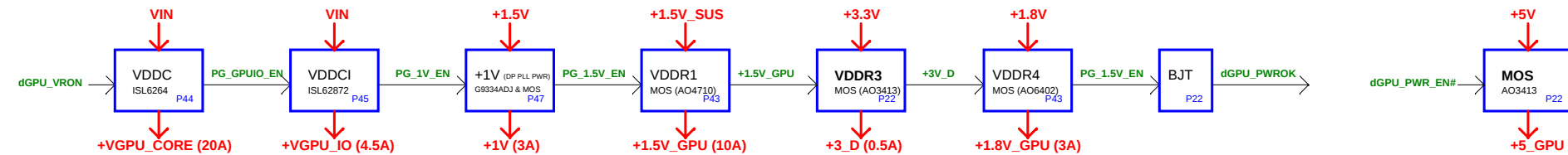
Reference	Description
IV@	for UMA only SKU
SW@	for Switchable Graphic only SKU



GPU PWR CTRL Option 1 (Default: VDDR3 before VDDC)



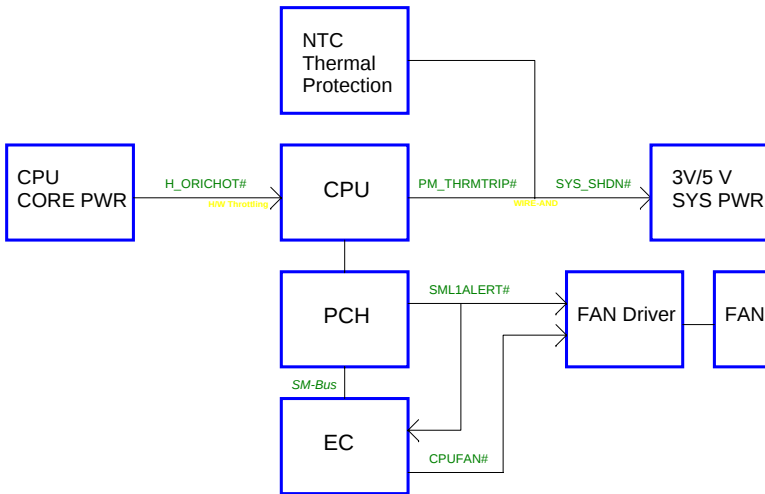
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)

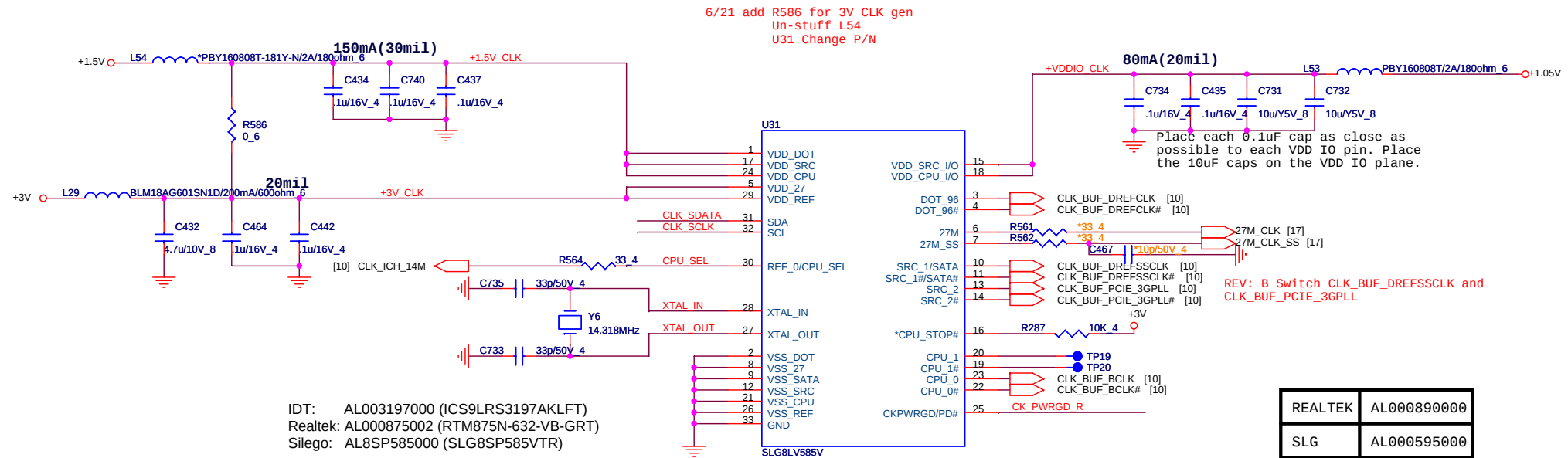


Power States

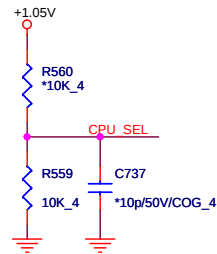
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



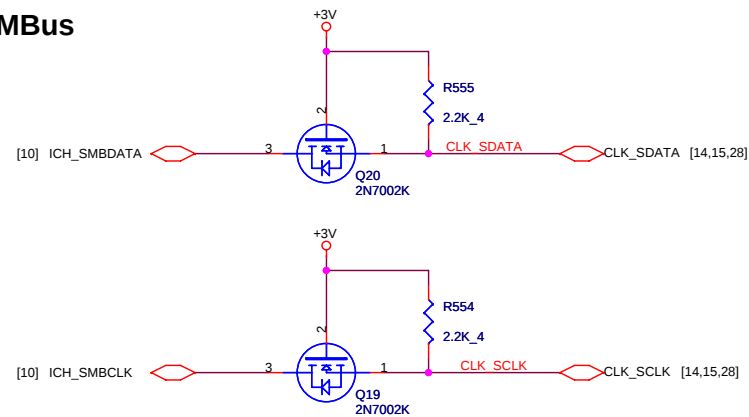


CPU_CLK select

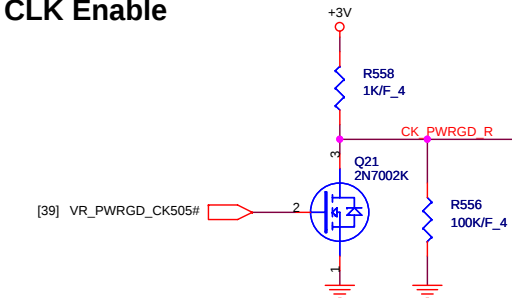


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable

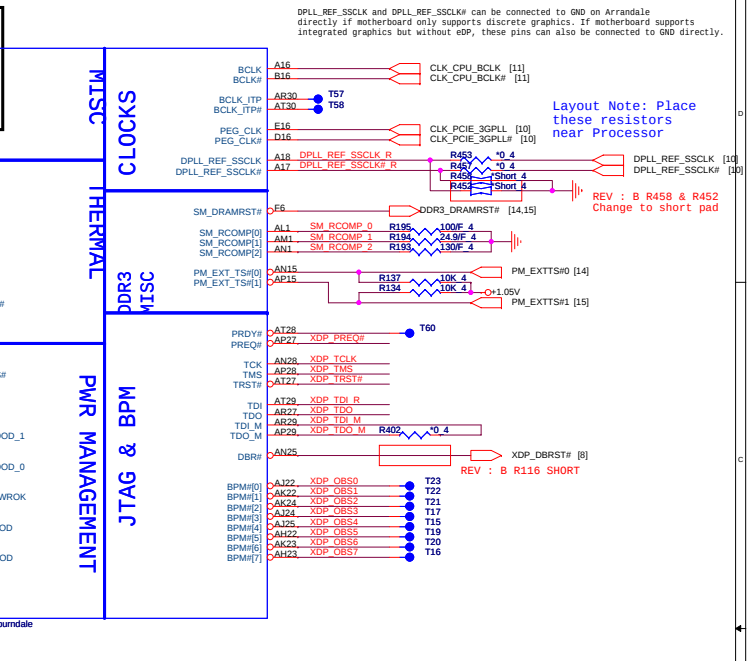
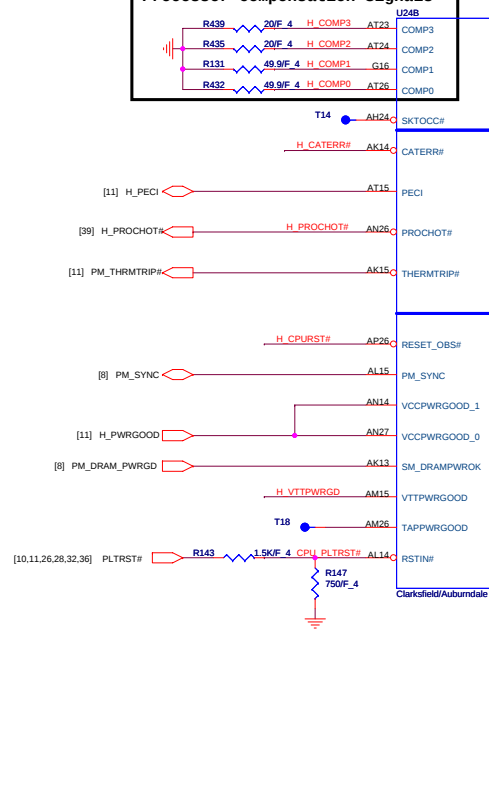


Quanta Computer Inc.
PROJECT : ZRC

Size	Document Number	Rev
	Clock Generator	1A
Date:	Wednesday, July 21, 2010	Sheet 3 of 46

Qual, Motherboard Schematic

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466
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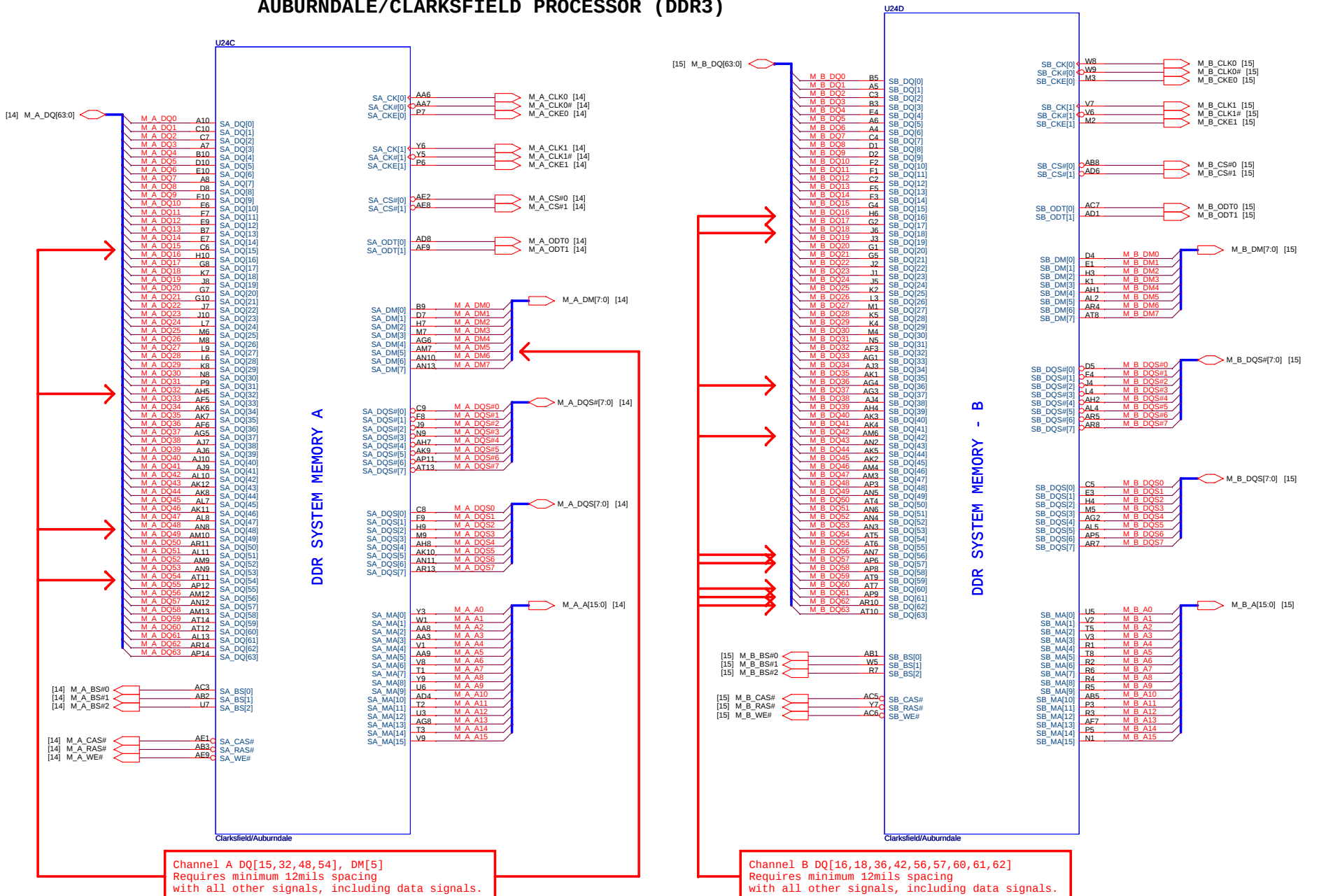
8

A



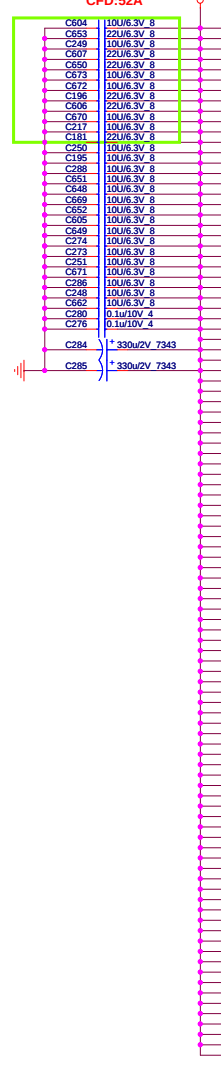
100

A	



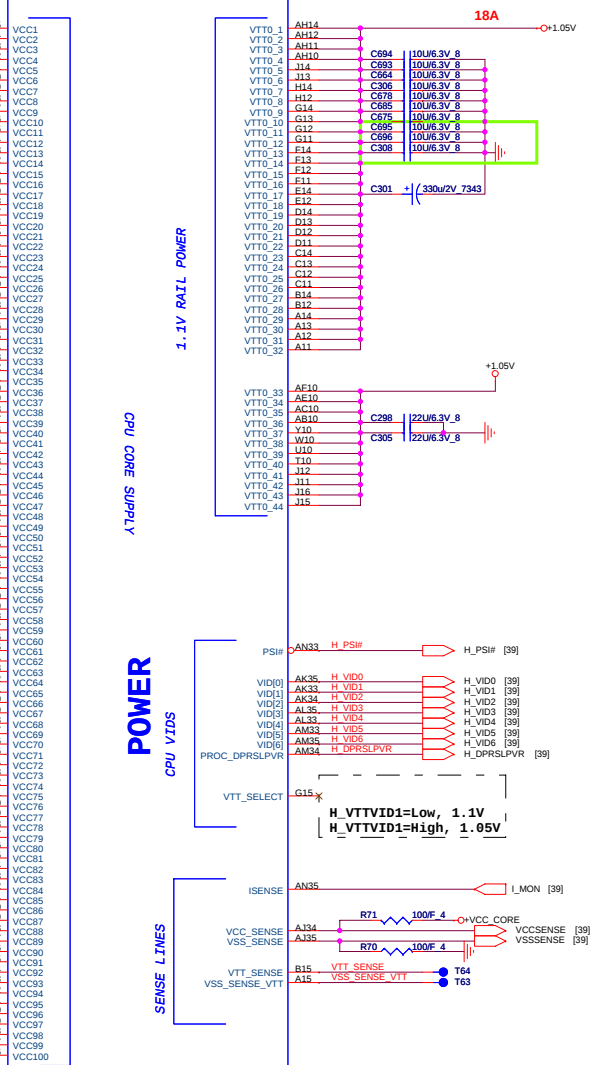
CPU Core Power

ARD:48A
CFD:52A



U24F

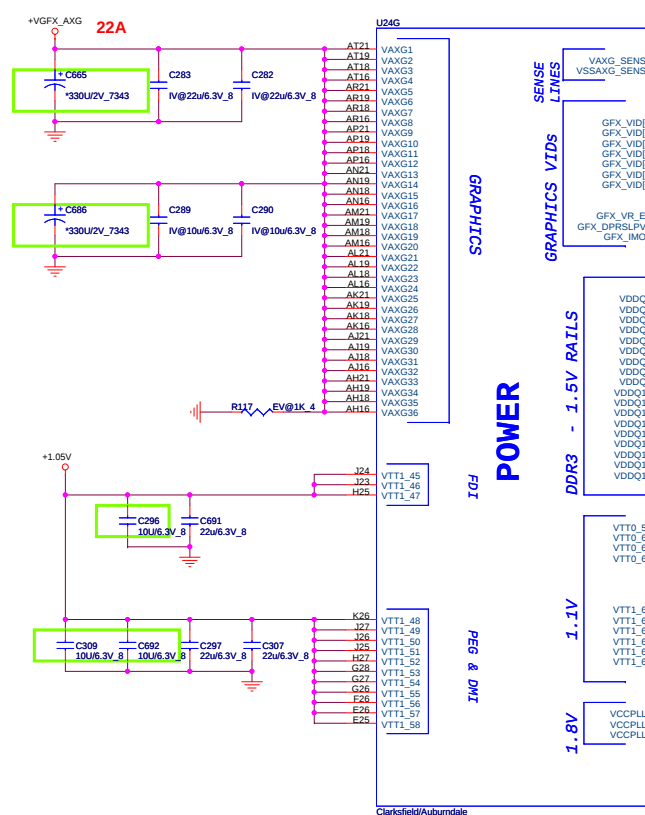
VTT Rail Values are
Auburndale VTT=1.05V
Clarksfield VTT=1.1V



Clarksfield/Auburndale

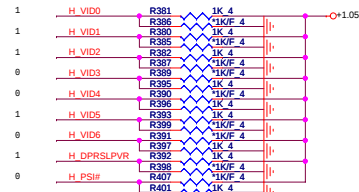
AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



NOTE:
For Validating IMP VR R6451 should be STUFF
and R2N1 NO_STUFF

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V



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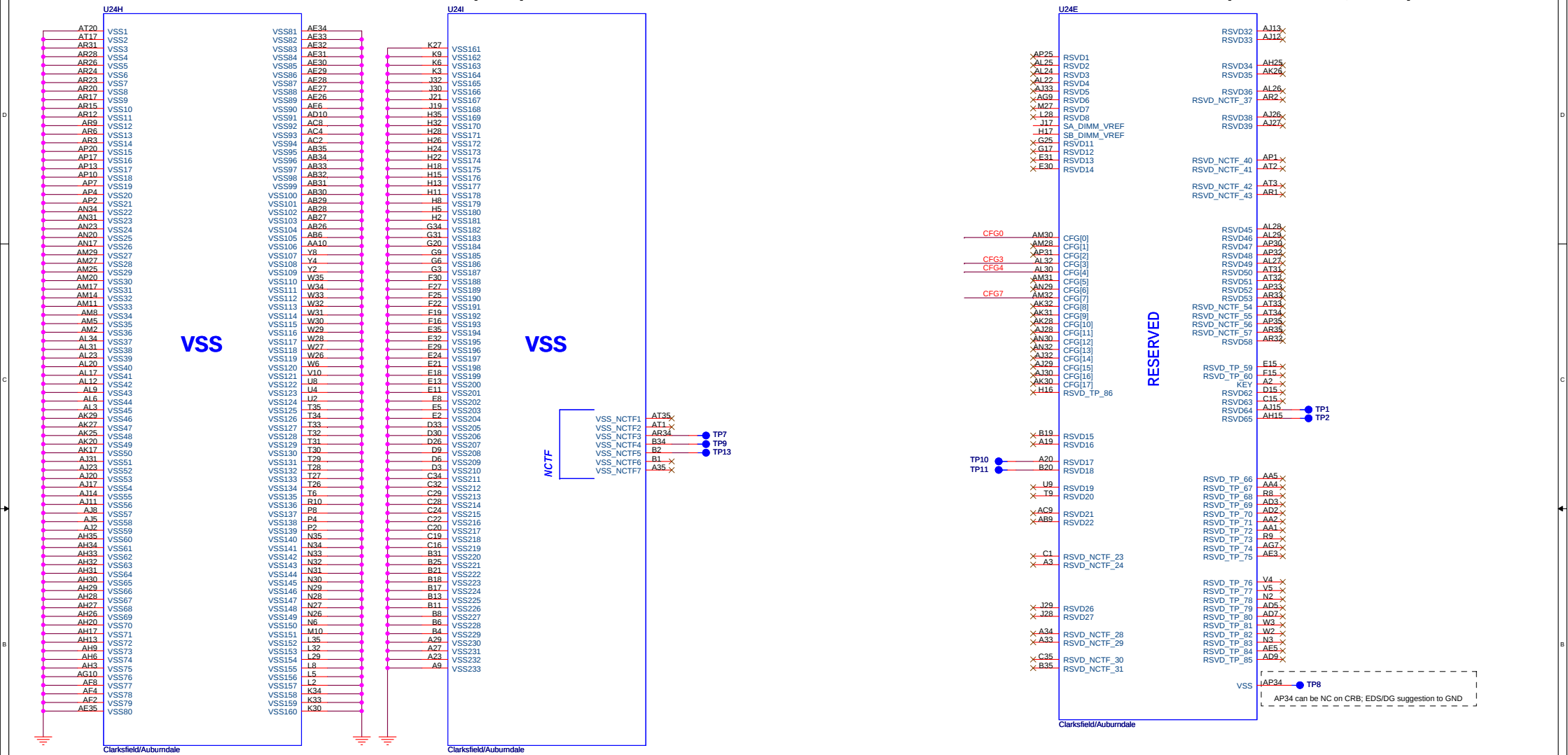
Size: **AUBURND 3/4 (PWR)**

Date: Thursday, July 22, 2010

Rev: 1A

Sheet: 6 of 46

AUBURNDALE/CLARKSFIELD PROCESSOR (GND), Service Manual, Motherboard Schematic, Processor (RESERVED, CFG)

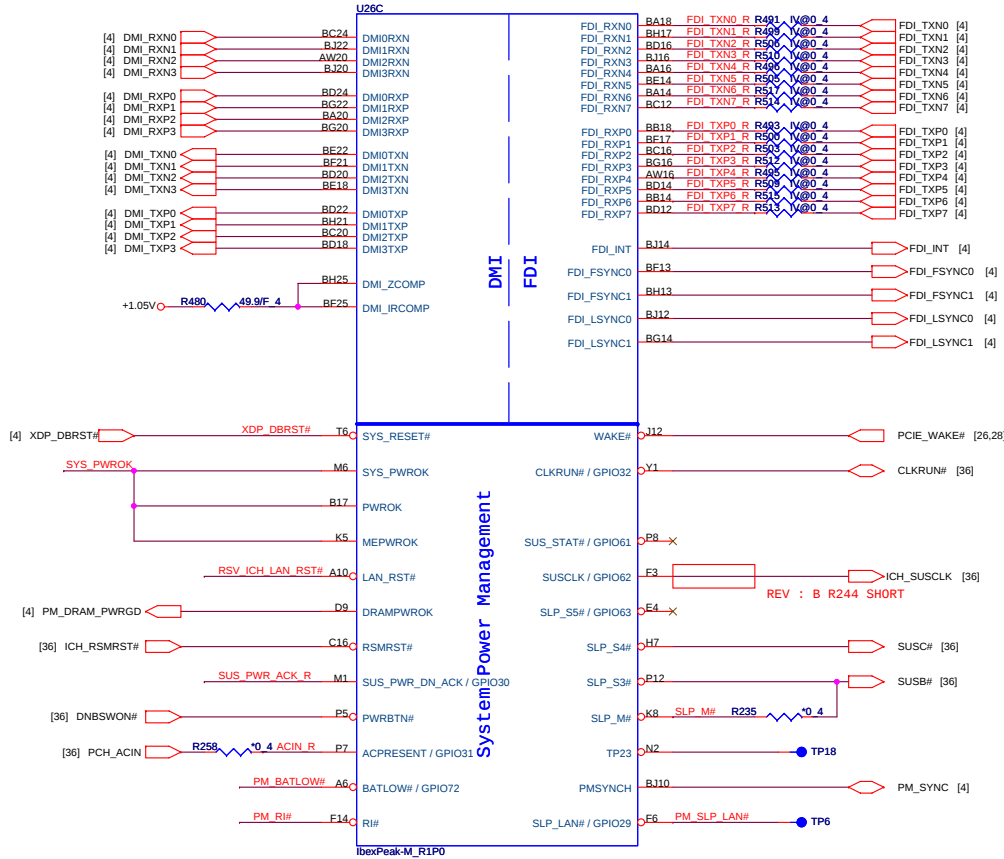


Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1	
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.				

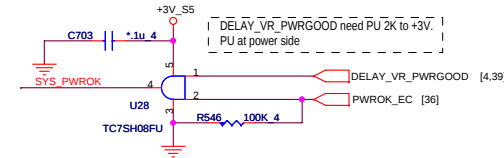
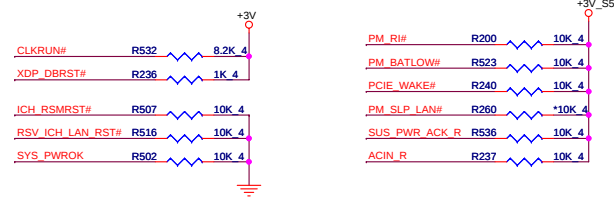
0-ohm resistor place close to PCH

IBEX PEAK-M (LVDS, DDI)

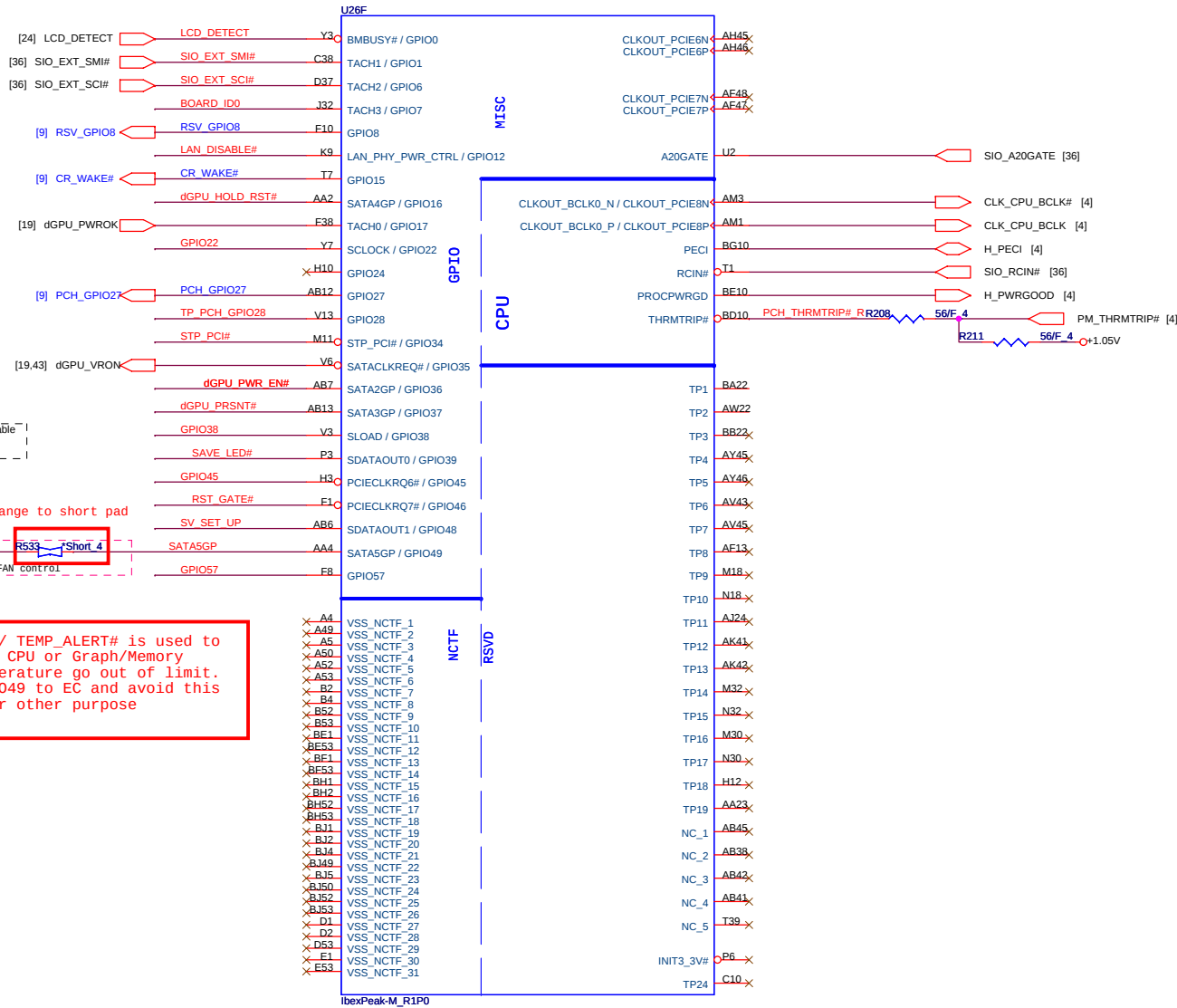


System PWR_OK

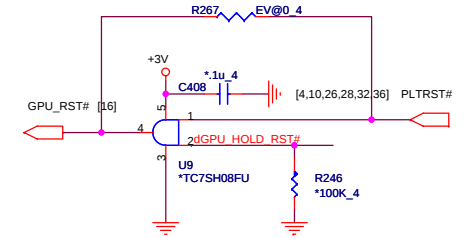
PCH Pull-high/low



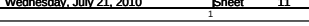
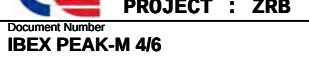
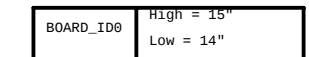
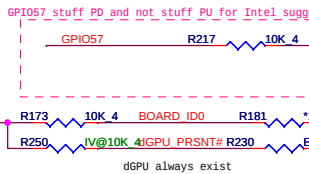
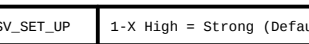
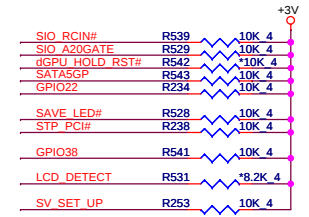
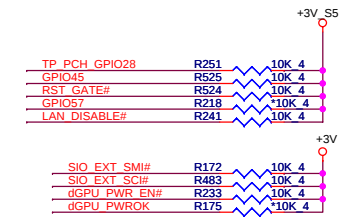
IBEX PEAK-M (GPIO, VSS_NCTF, RSVD)

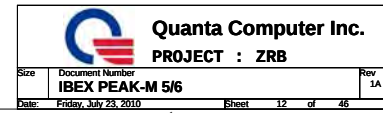


GPU_RST#

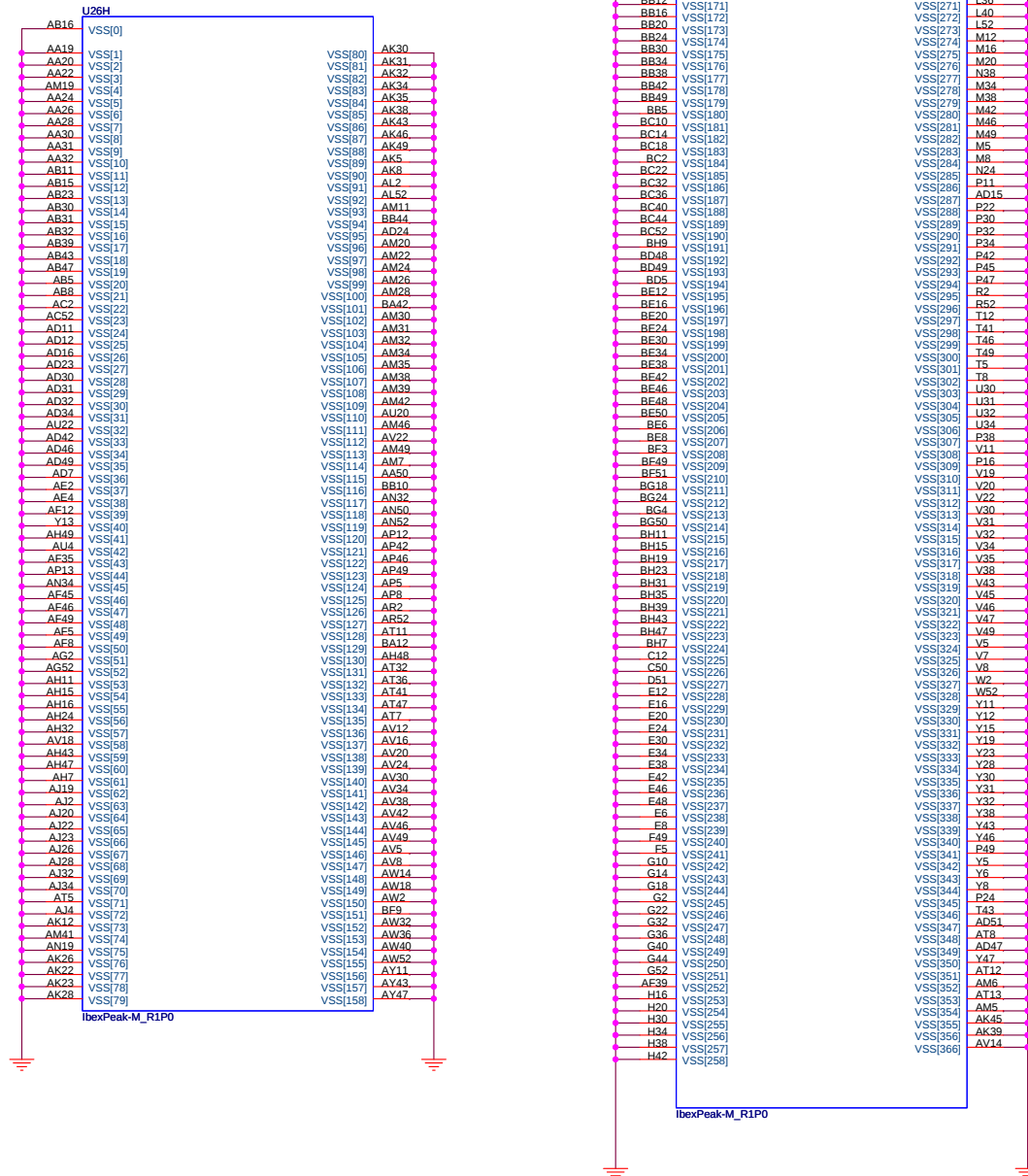


GPIO Pull-up/Pull-down

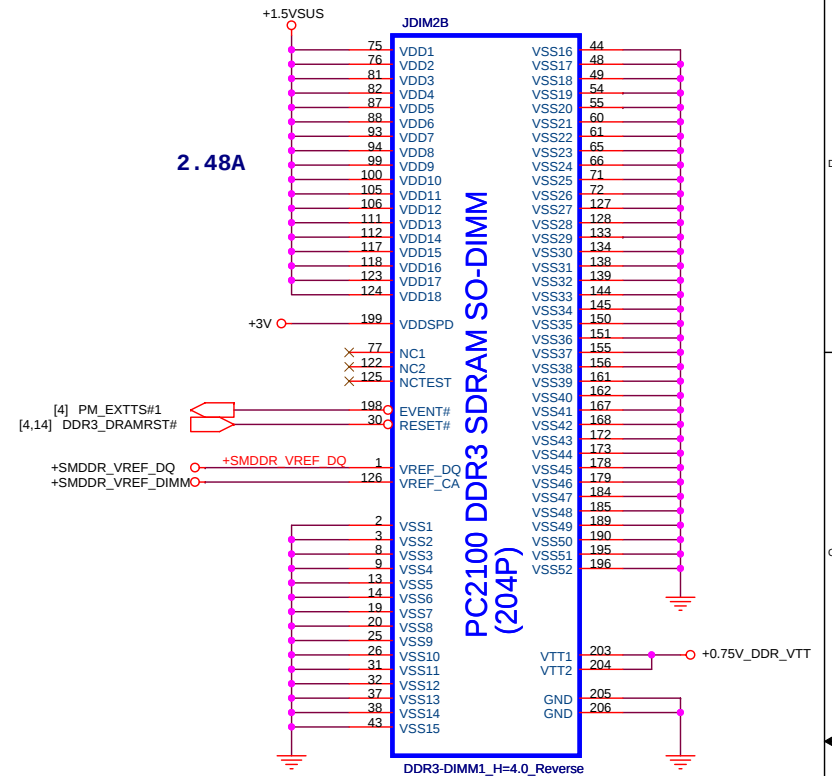
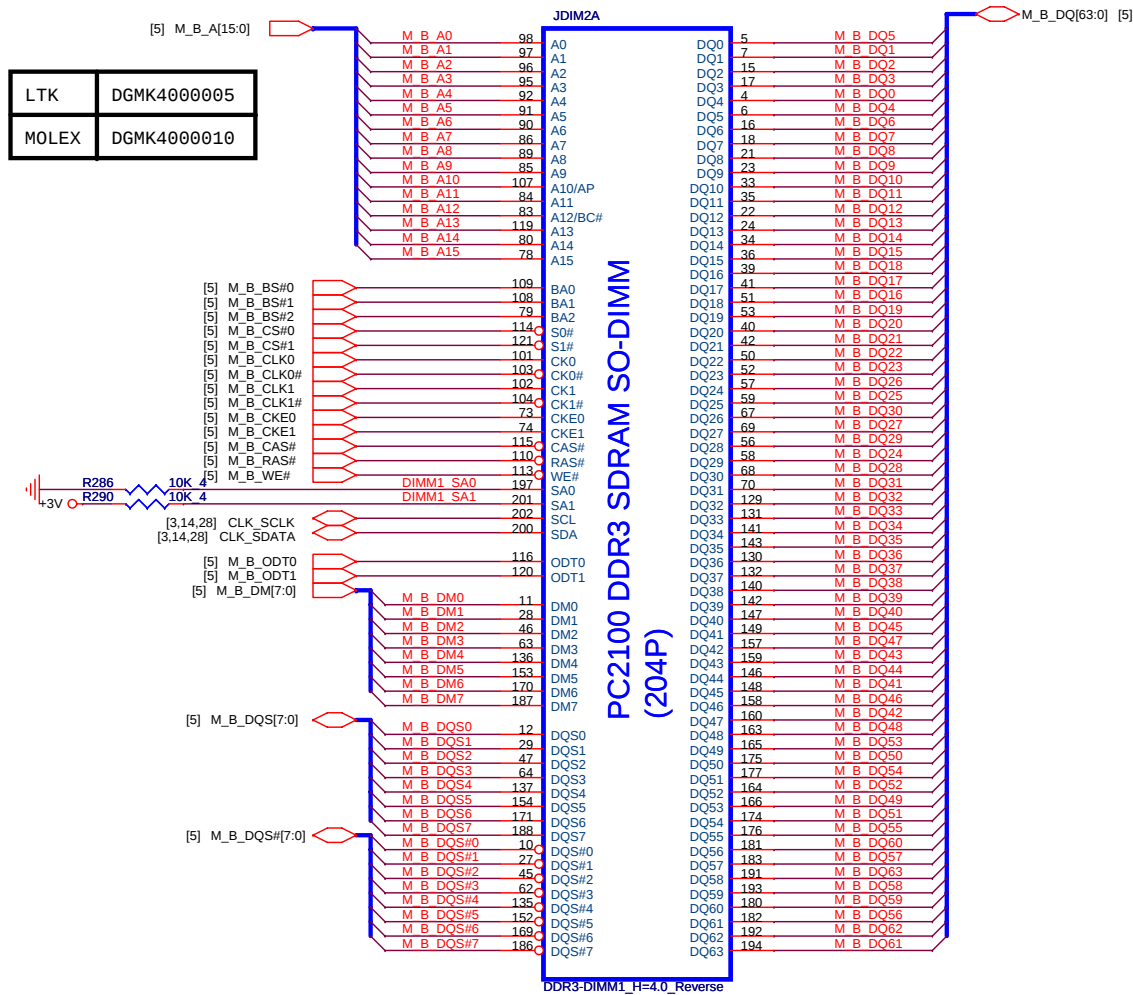




IBEX PEAK-M (GND)

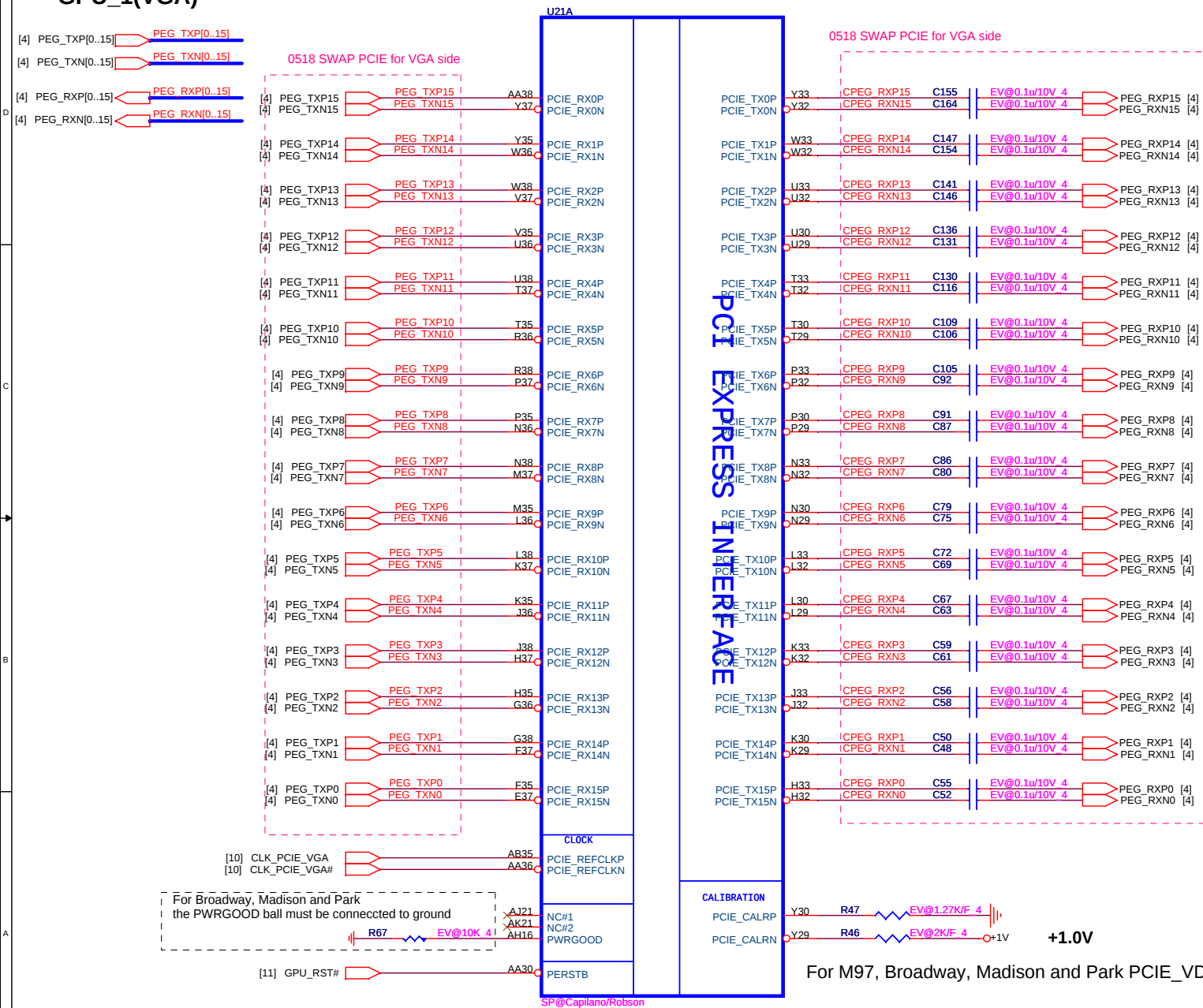


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GPU_1(VGA)



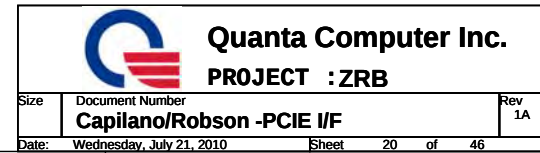
Madison	AJ007720T02
Park	AJ077400T08

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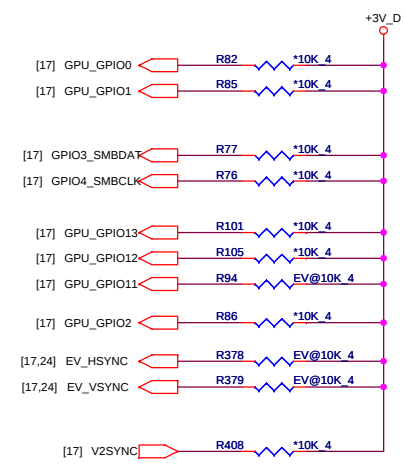
Size	Document Number	Rev
	Capilano/Robson -PCIE I/F	1A
Date:	Wednesday, July 21, 2010	Sheet 16 of 46

For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

SP@Capilano/Robson



PIN STRAPS(VGA)



Size of the primary memory apertures	GPIO[13:11]
128 MB	000
256MB	001
64 MB	010
32 MB	011
More than 512 MB	Not Supported

CONFIGURATION STRAPS

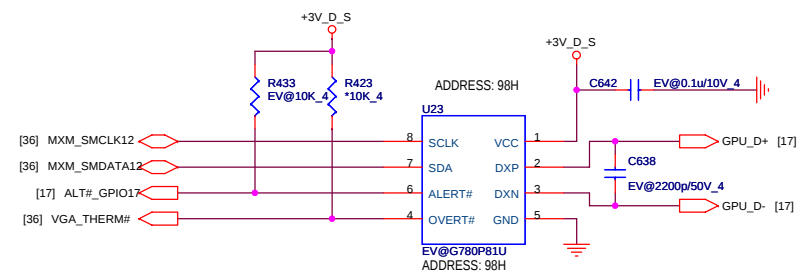
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0	
ROMIDCFG[2:0]	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

Thermal Sensor(VGA)

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

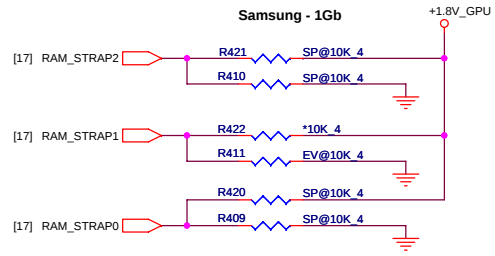
USD0.16



DDR3 Memory Aperture size(GPU)

DDR3 Memory size

Vendor	Vendor P/N	STN B/S P/N	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1	0	0
	H5TQ2G63BFR-12C	AKD5MGGTW03 (128M*16)	1	0	1
Samsung					
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500 (128m*16)	0	0	1
AMD					
	23EY2387MA12-SZ	AKD5LGGT700	0	1	0



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

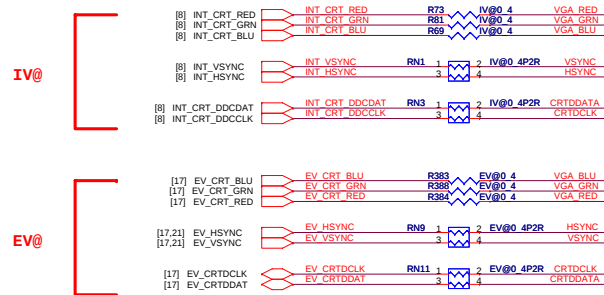


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PROJECT :ZRB

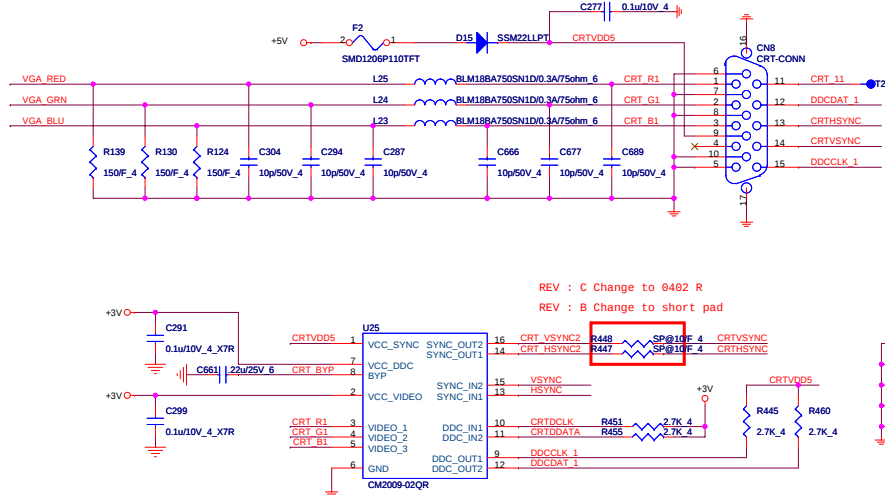
Size	Document Number	Rev
	Strip/Thermal	1A
Date:	Wednesday, July 21, 2010	Sheet 21 of 46

CRT Switch

0_ohm Resistor place close to Joint-Point

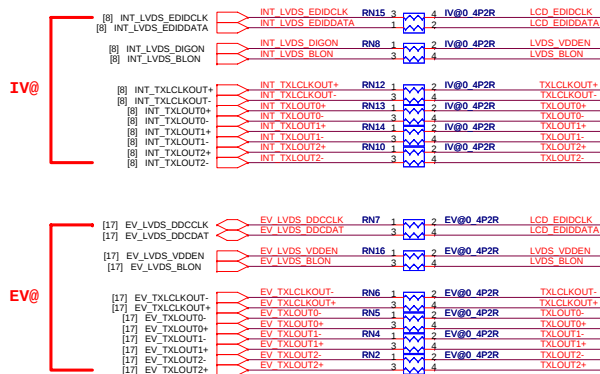


CRT

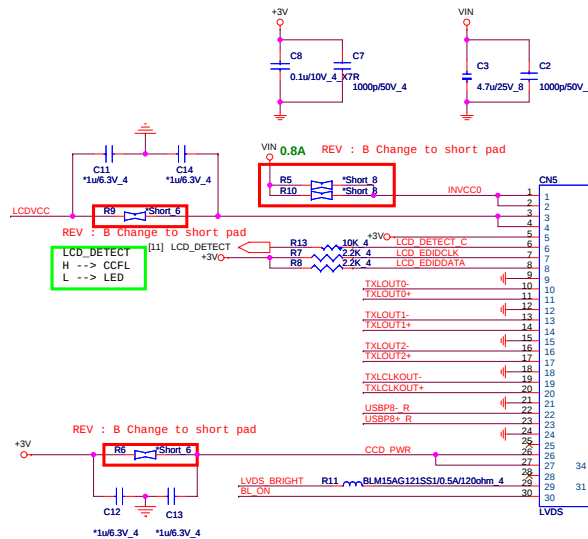


LVDS

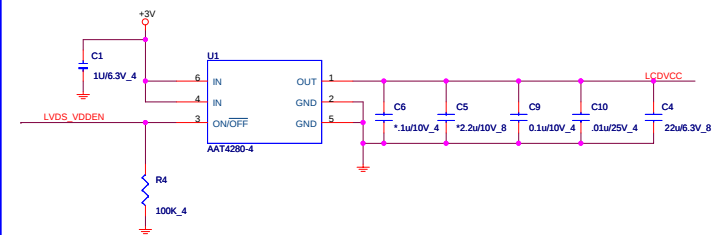
0_ohm Resistor place close to Joint-Point



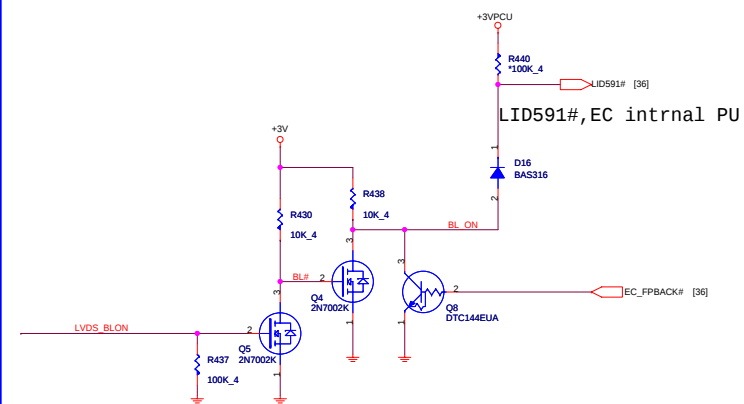
LVDS



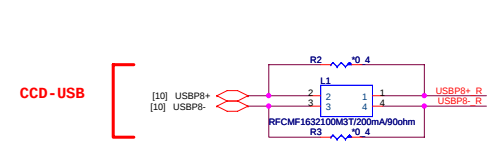
LCD Power



Backlight Control



LVDS_BRIGHT

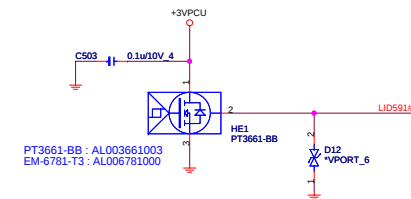


CCD-USB

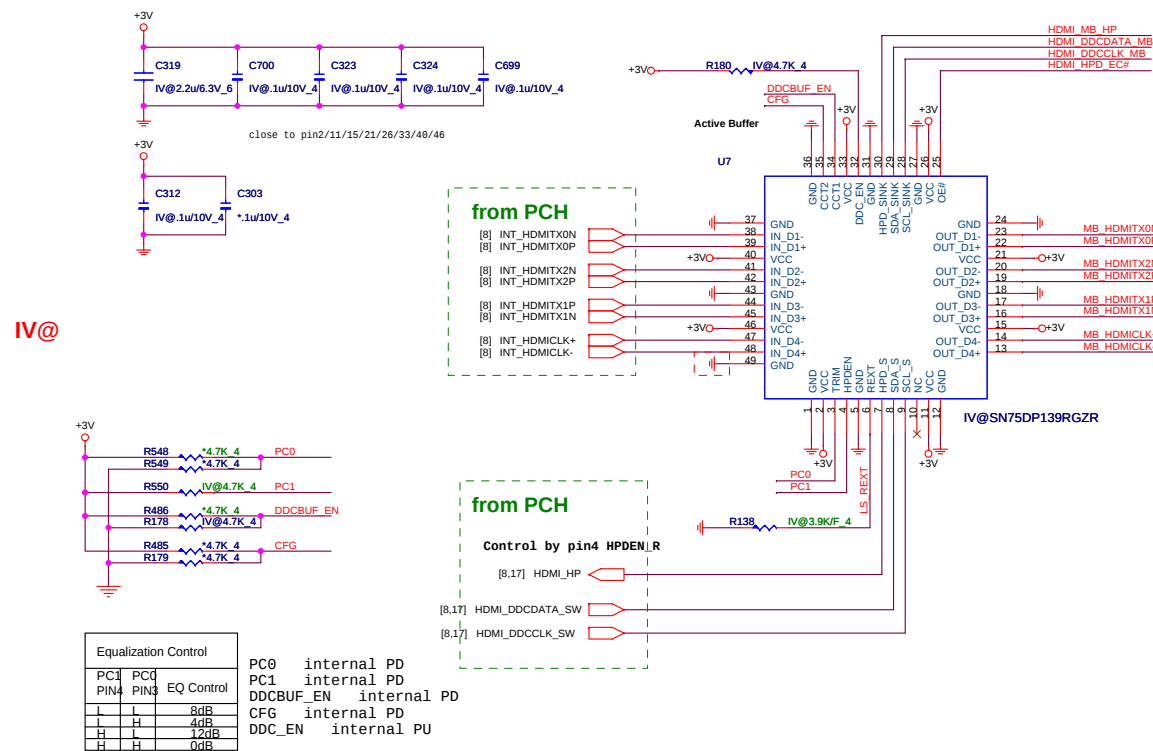


CCD +3V-current budget 0.2A

Lid Switch (Hall sensor)

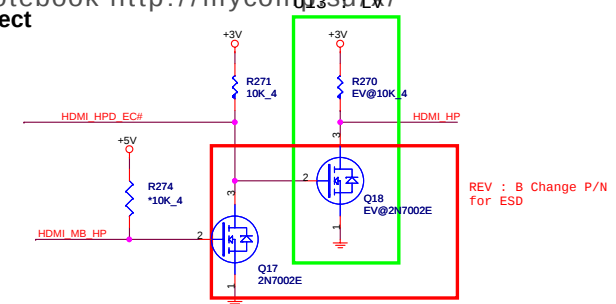


HDMI LEVEL SHIFTER



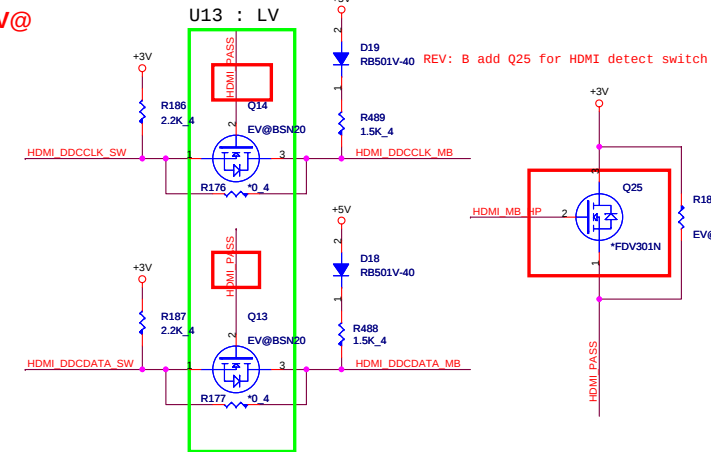
HDMI-detect

EV@



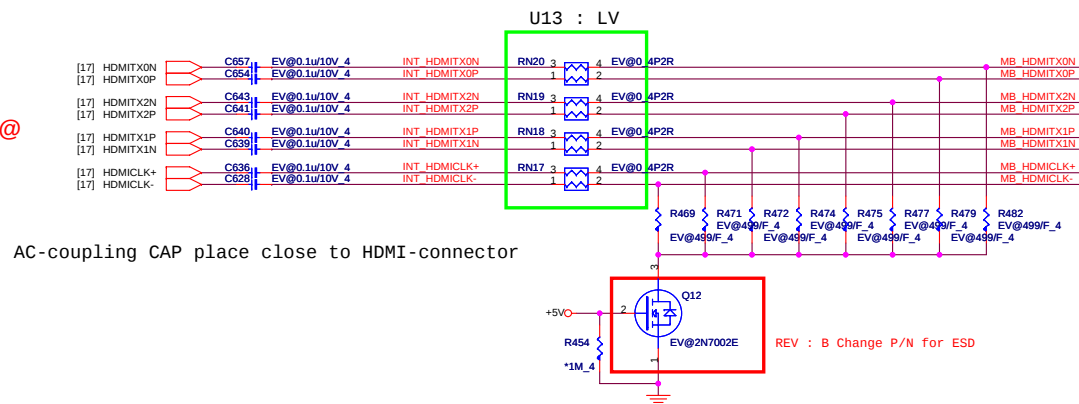
I2C

EV@

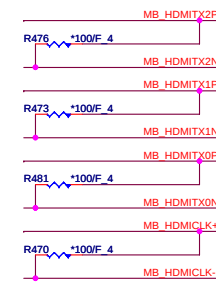


Switchable Graphic HDMI source

EV@

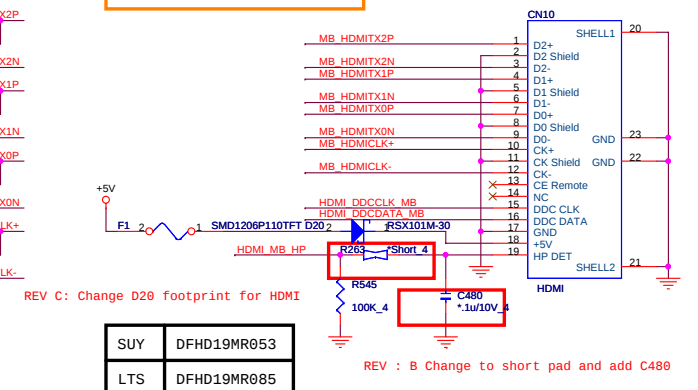


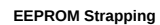
EMI



HDMI connector

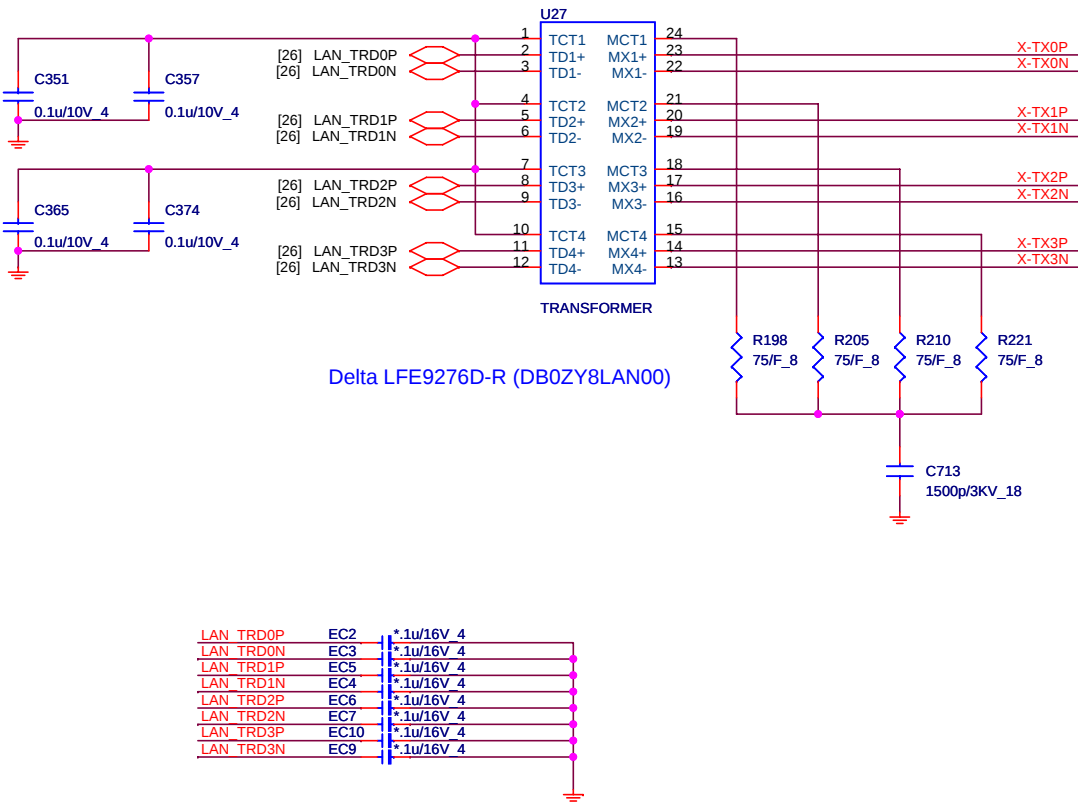
REV : C Location : D20 Change Footprint & P/N



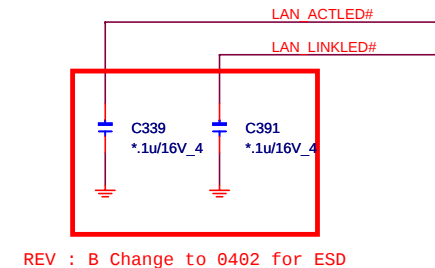
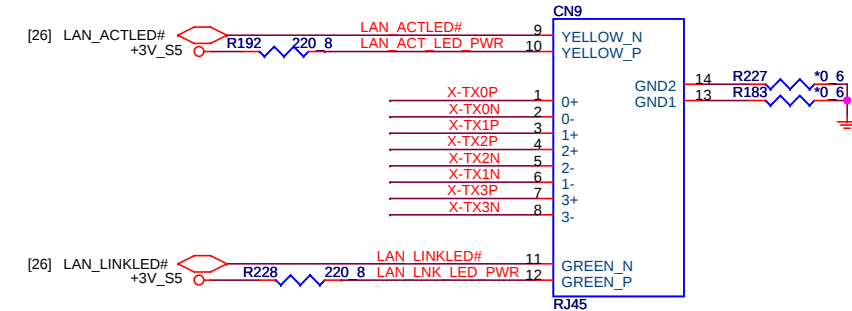


EEPROM Type	EECLK	EEDAT
24LC02	1	1
Internal	1	0

TRANSFORMER



SUY	DFTJ12FR109
AEC	DFTJ12FR135

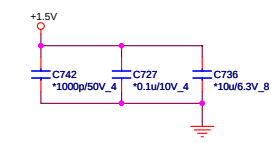
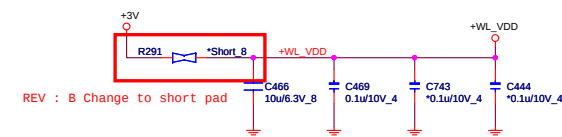
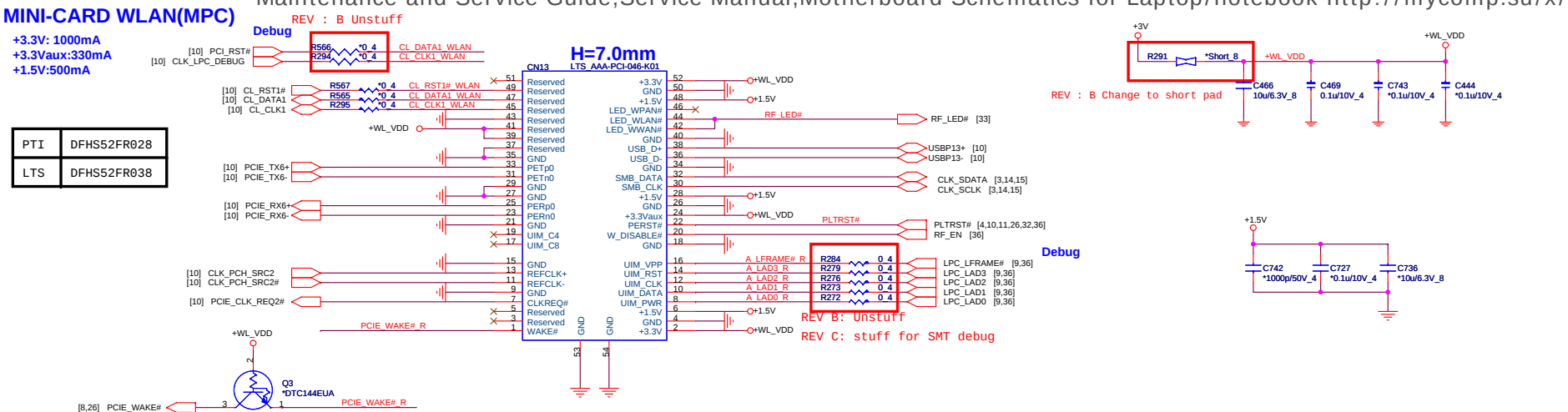


REV : B Change to 0402 for ESD

MINI-CARD WLAN(MPC)

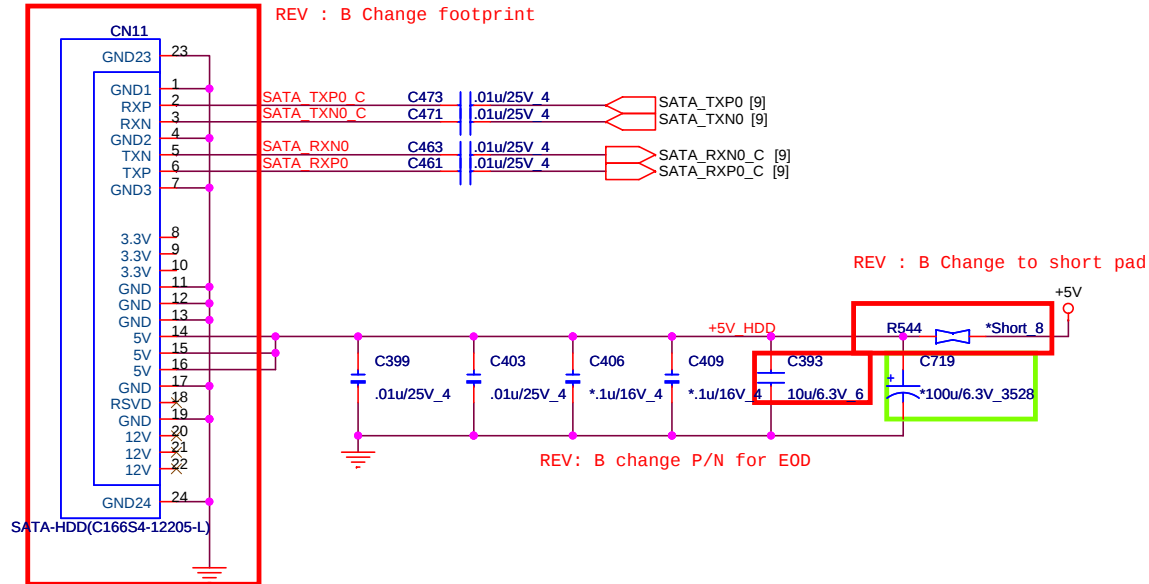
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

PTI	DFHS52FR028
LTS	DFHS52FR038

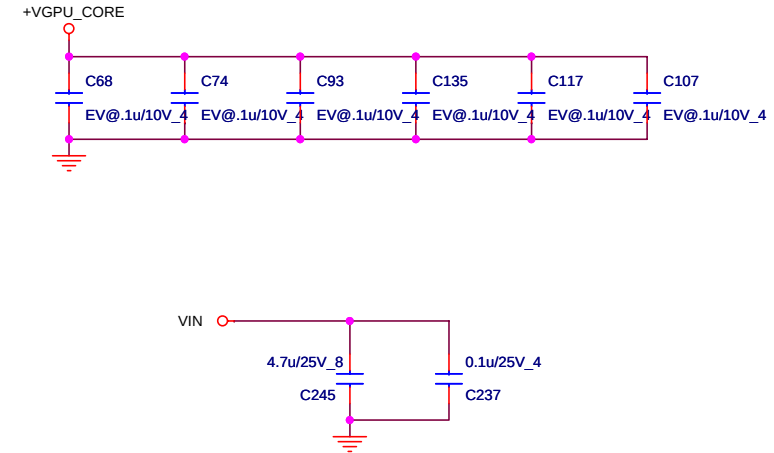


MAIN SATA HDD

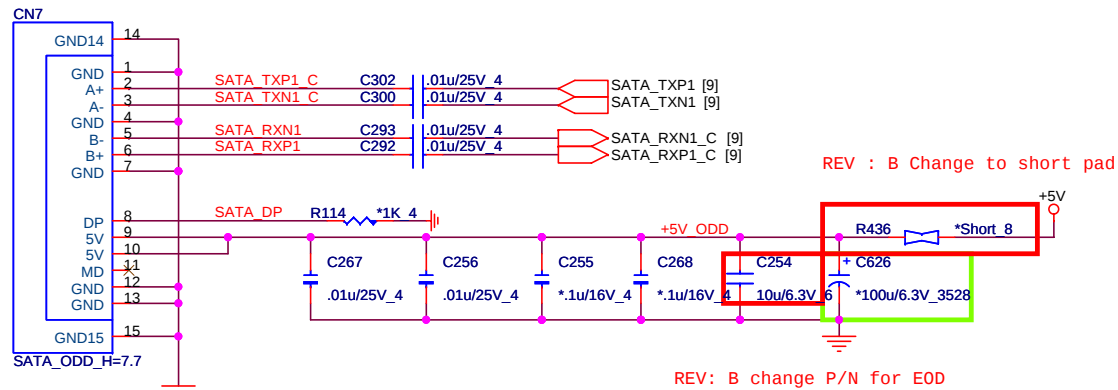
REV : B Change footprint



EE RETURN-PATH CAPACITORS



ODD (SATA)



REV: B change P/N for EOD

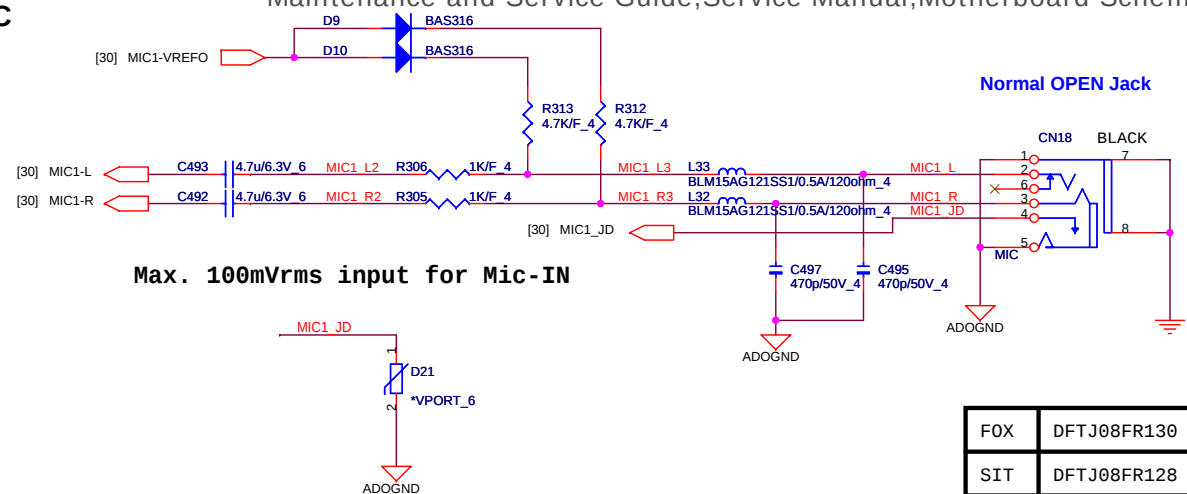
SUY	DFHS22FR214
AOP	DFHS22FR232
AEC	DFHS22FR216

AOP	DFHS13FR011
OTK	DFHS13FR010

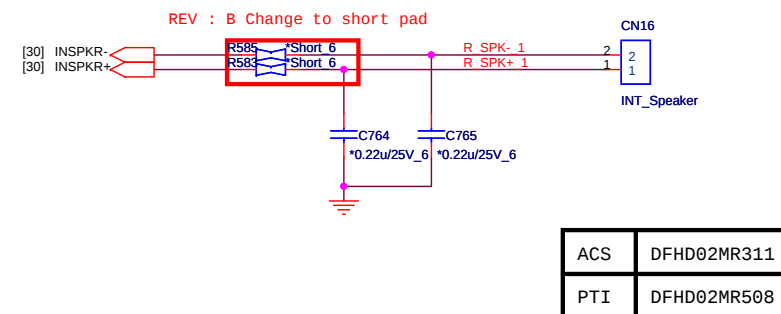
**Quanta Computer Inc.**
PROJECT : ZRB

Size	Document Number	Rev
	SATA-HDD/ODD/RETURN-PATH	1A
Date:	Wednesday, July 21, 2010	Sheet 29 of 46

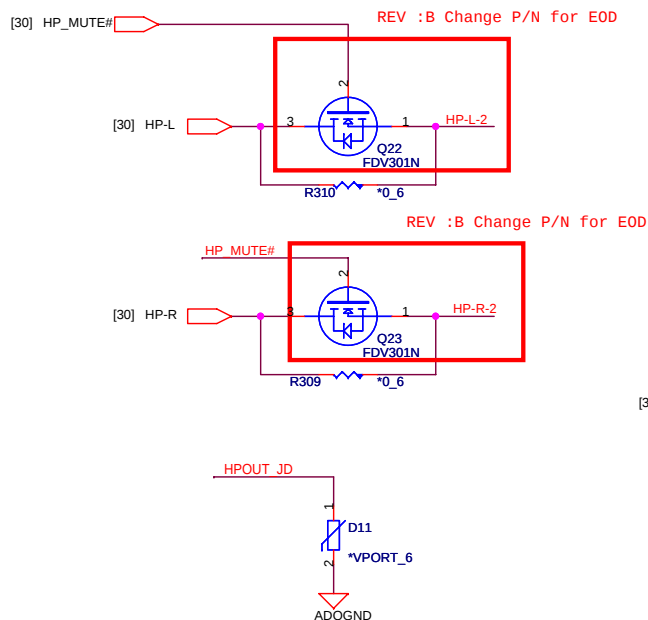
MIC



Internal Speaker

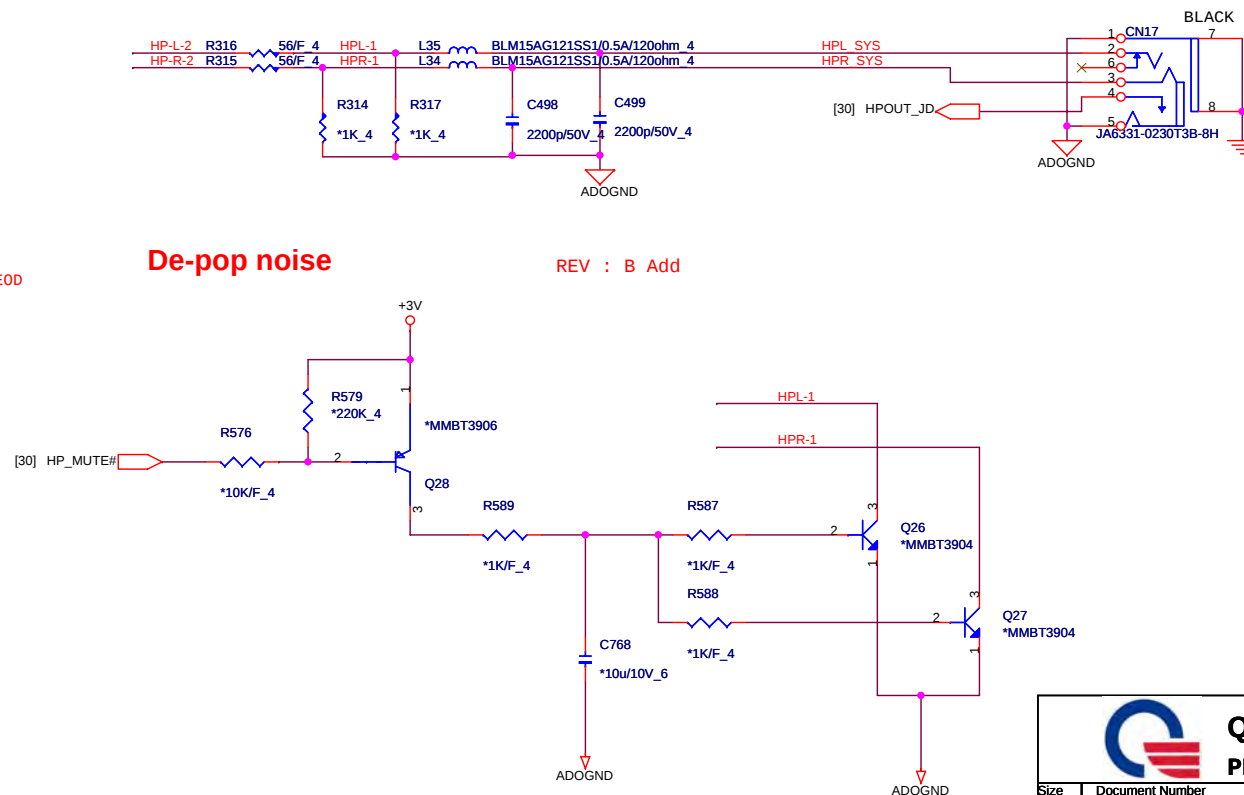


HP/SPDIF



De-pop noise

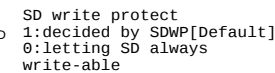
REV : B Add



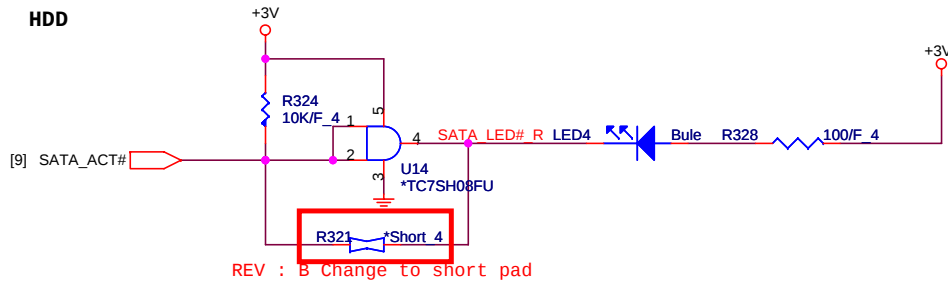
Quanta Computer Inc.
PROJECT : ZRB

Size	Document Number	Rev
		1A
AMP /AUDIO JACK CONN		
Date:	Wednesday, July 21, 2010	Sheet 31 of 46

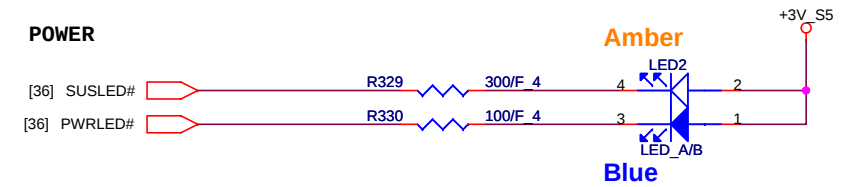
2 IN 1 CARD READER (SD/MMC)



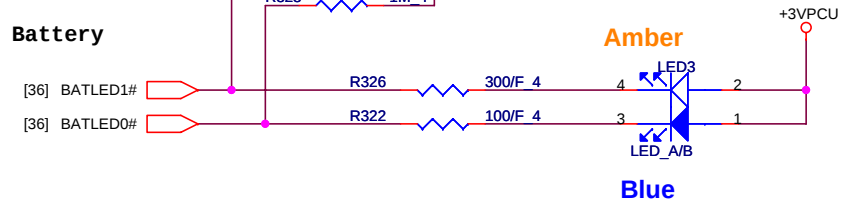
LED



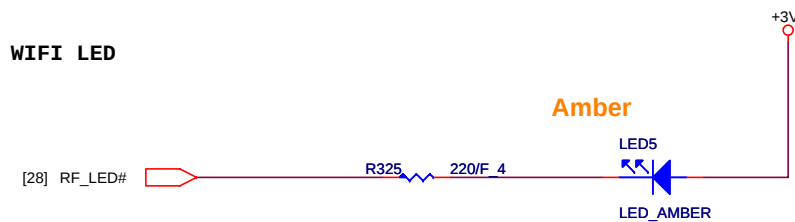
POWER



Battery



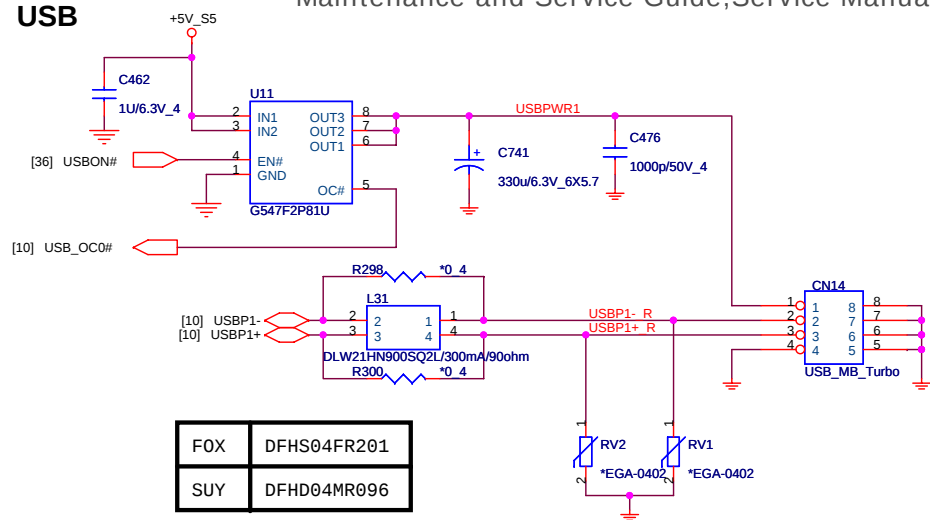
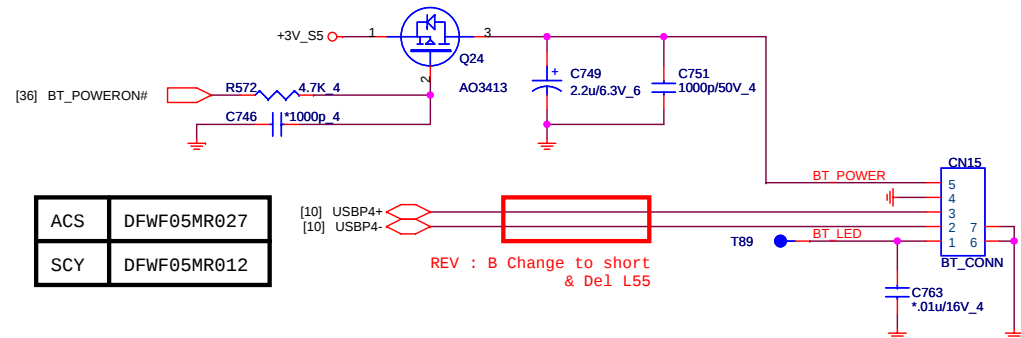
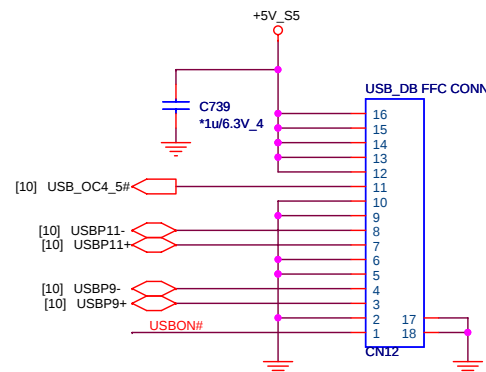
WIFI LED



Quanta Computer Inc.
PROJECT : ZRB

Size	Document Number	Rev 1A
Date: Monday, July 26, 2010	Sheet 33 of 46	

POWER/MMB/LAUNCH/LED

USB**BLUETOOTH CONNECTOR****USB/B**

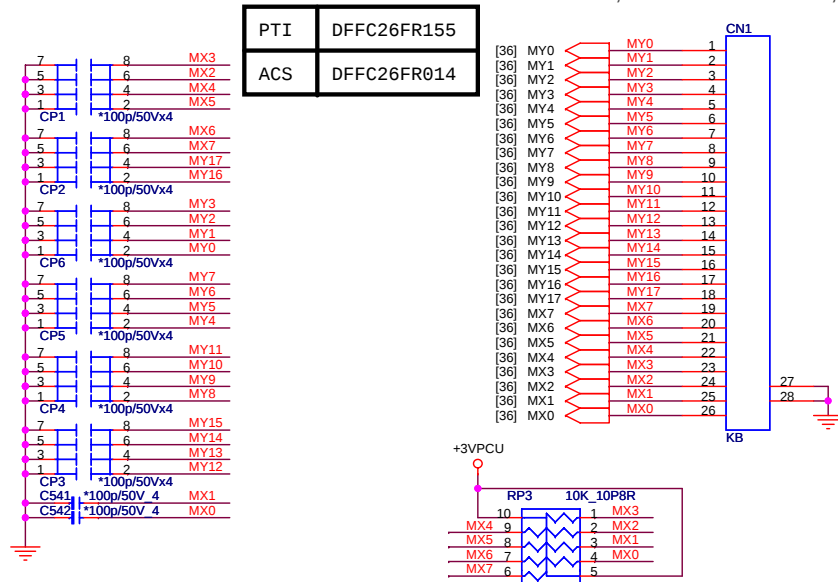
Quanta Computer Inc.
PROJECT : ZRC

Size	Document Number	Rev
		1A

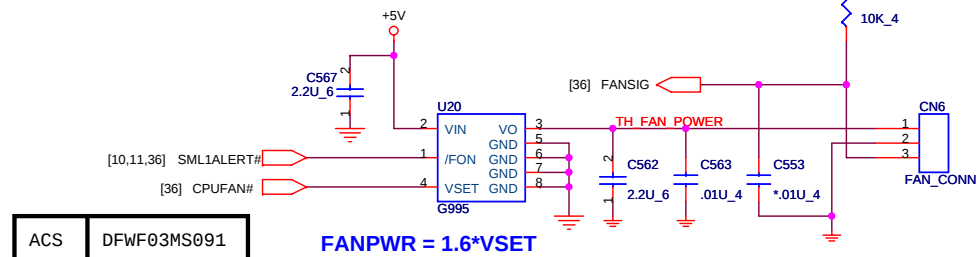
USB/ BT

Date: Friday, July 23, 2010 Sheet 34 of 46

K/B

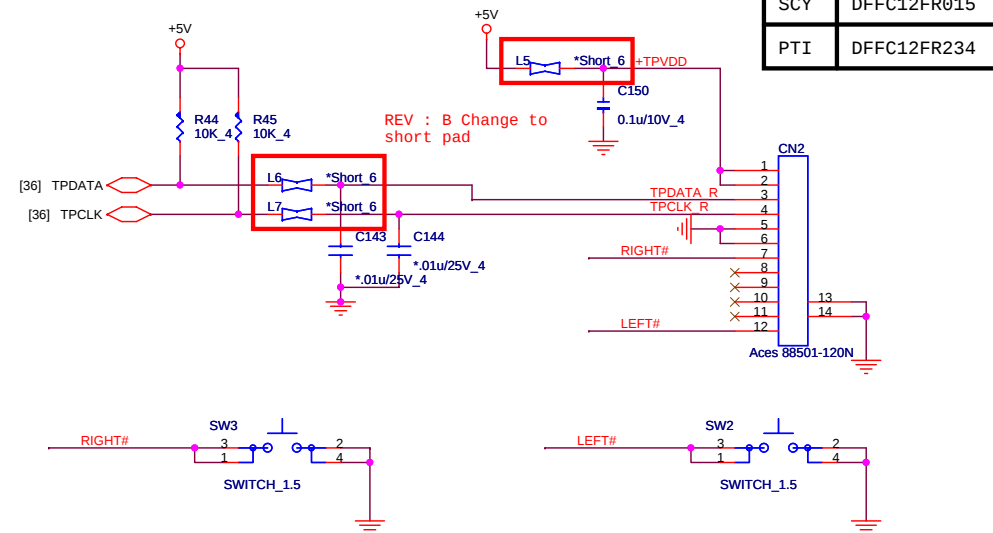


CPU FAN

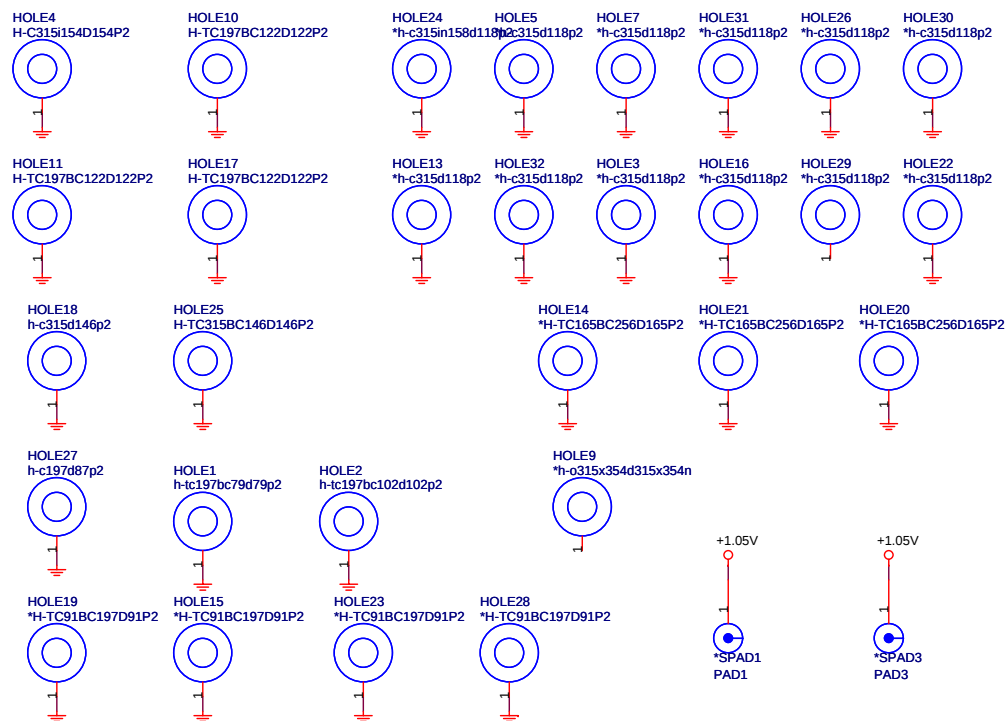


ACS	DFWF03MS091
SCY	DFWF03MS000

TOUCHPAD & Switch CONN.



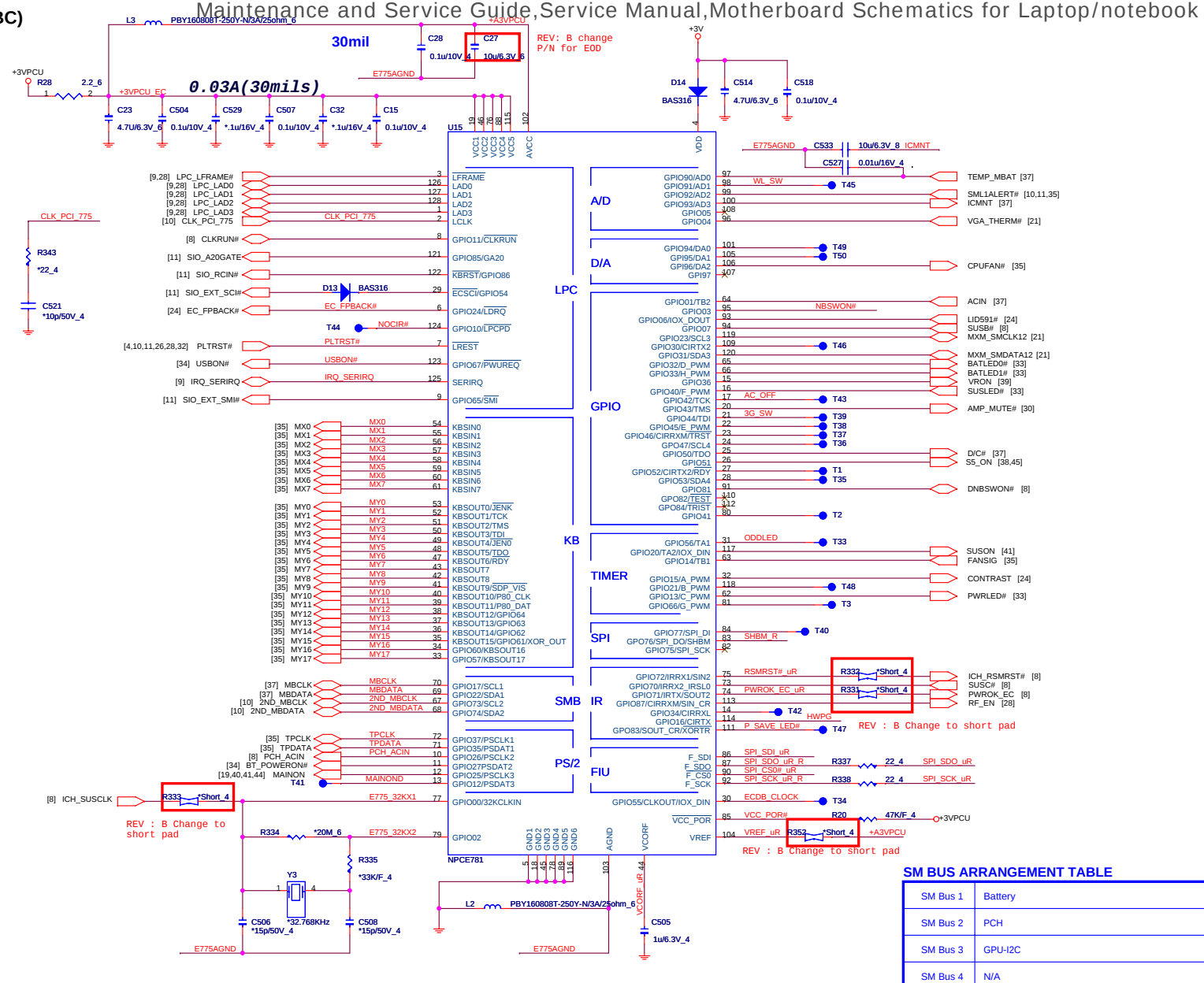
ACS	DFFC12FR017
SCY	DFFC12FR015
PTI	DFFC12FR234



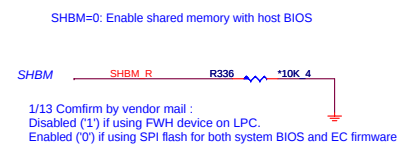
Quanta Computer Inc.
PROJECT : ZRB

Size	Document Number	Rev 1A
Date	Friday, July 23, 2010	Sheet 35 of 46

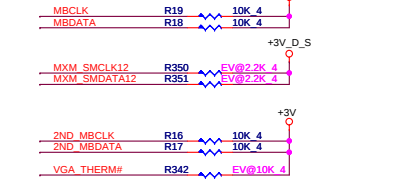
EC(KBC)



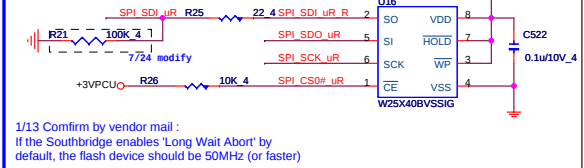
IO ADDRESS SETTING(KBC)



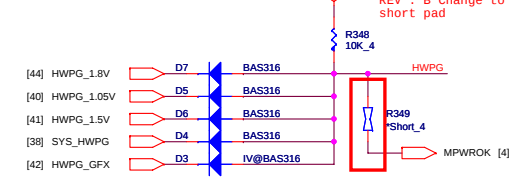
SM BUS PU(KBC)



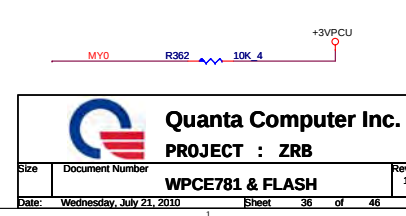
SPI FLASH(KBC)



HWPG(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)



200mil
OCP:6.5A
5A

OCP:6.5A

$$L(\text{ripple current}) = (9-5) * 5 / (2.2u * 0.4m * 9) = 2.525A$$

$$I_{ocp} = 6.5 - (2.525 / 2) = 5.24A$$

$$V_{th} = 5.24A * 14.2m\Omega = 0.074V$$

$$R(I_{lim}) = (0.07437V * 10) / 5uA = 148.74K$$

$$I_{peak}(\text{choke}) = 10.687A$$

OCP:9A

$$L(\text{ripple current}) = (9-3.3) * 3.3 / (2.2u * 0.5m * 9) = 1.9A$$

$$I_{ocp} = 9 - (1.9 / 2) = 8.05A$$

$$V_{th} = 8.05A * 14.2m\Omega = 114.31mV$$

$$R(I_{lim}) = (114.31mV * 10) / 5uA = 228.62K$$

$$I_{peak}(\text{choke}) = 11.479A$$

10mil
0.23A

2.85A
114mil

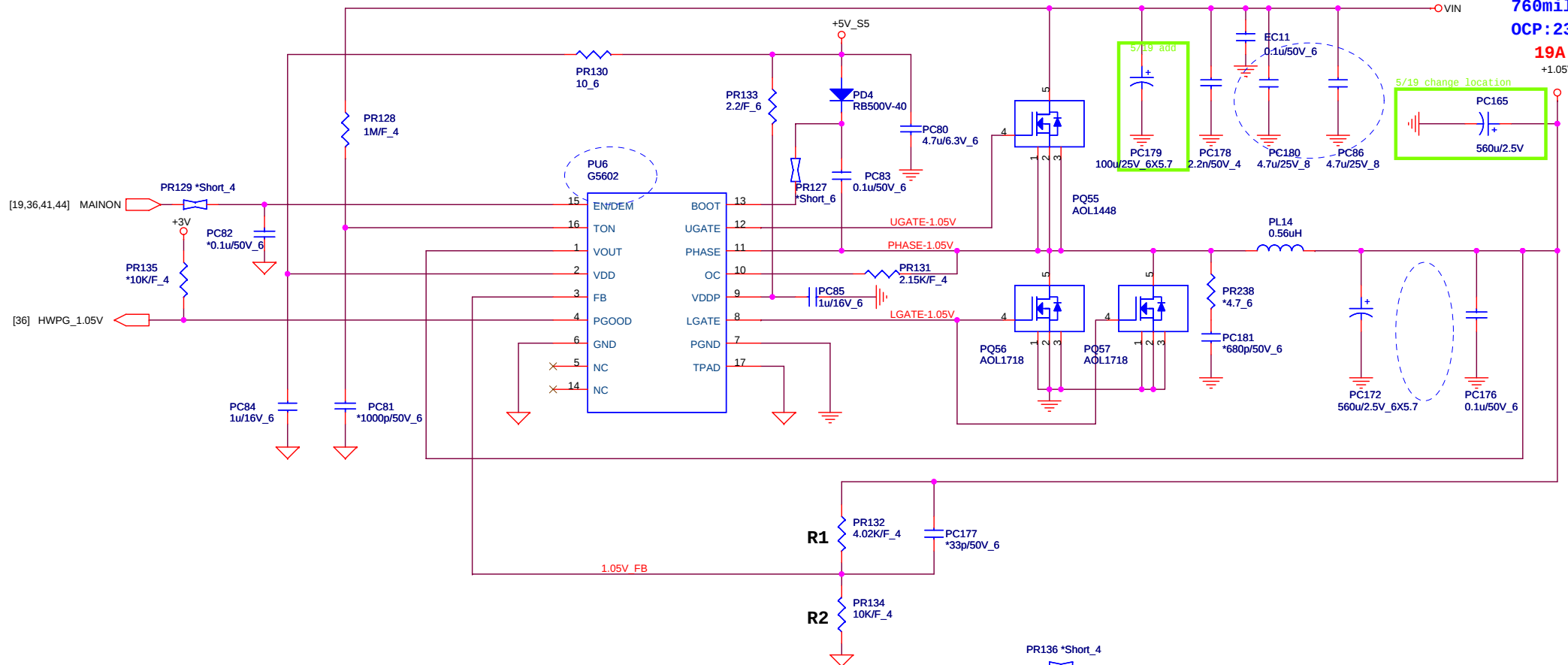
2.171A
87mil

3A
107mil

280mil
OCP:9A
7A

[PWM]

760m11
OCP: 23A
19A
+1.05V



$$T_{ON} = 3.85p \cdot R_{TON} \cdot V_{out} / (V_{in} - 0.5)$$

$$\text{Frequency} = V_{out} / (V_{in} \cdot T_{ON})$$

$$T_{ON} = 3.85p \cdot 1M \cdot 1 / (V_{in} - 0.5)$$

$$\text{Frequency} = 1 / (0.0036767) = 272K$$

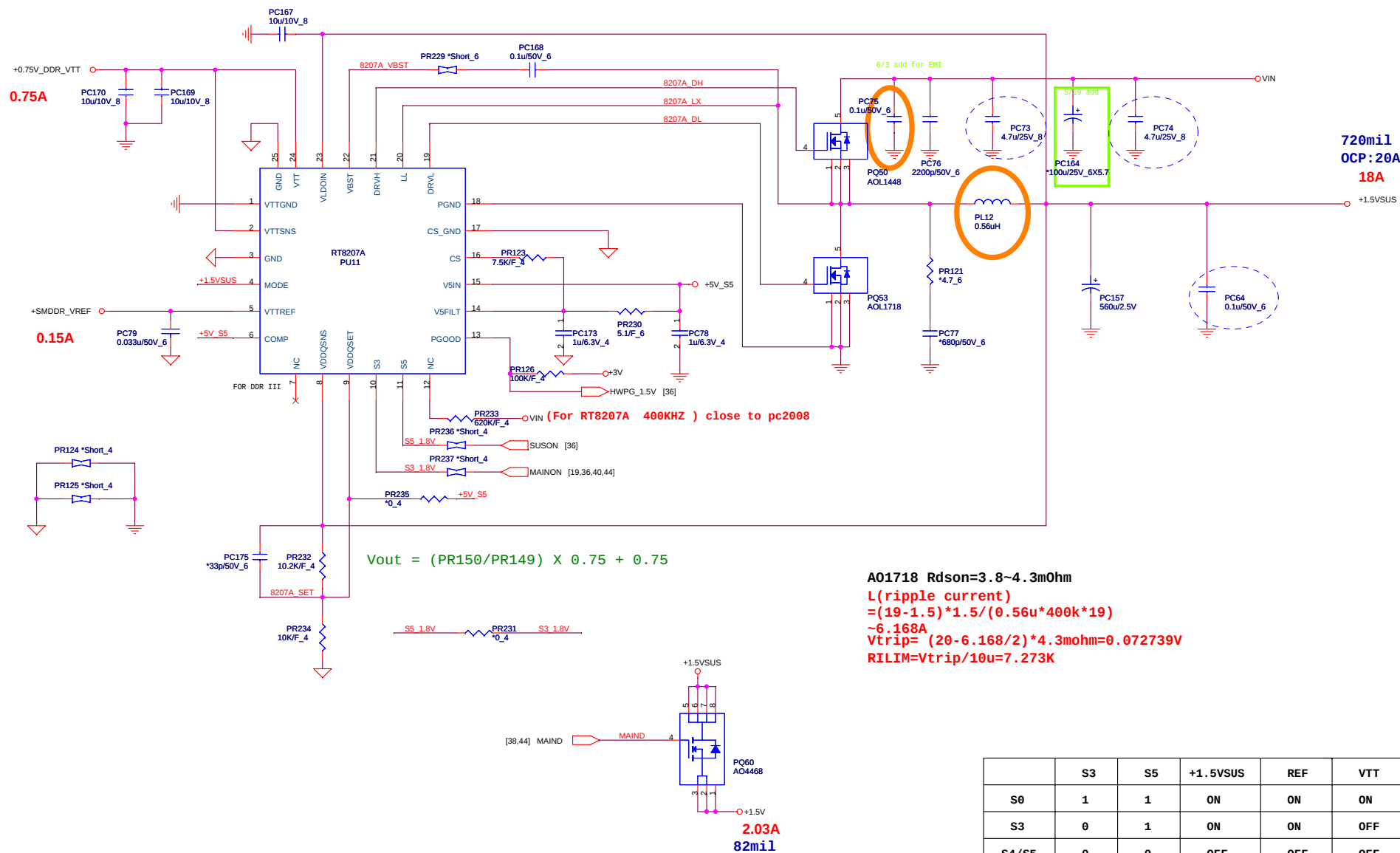
A01718 $R_{dson} = 3 \sim 4.3m\Omega$

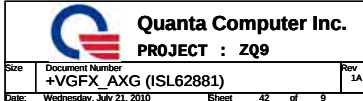
$$L(\text{ripple current}) = (19 - 1.05) \cdot 1.05 / (0.56u \cdot 272k \cdot 19) \sim 6.512A$$

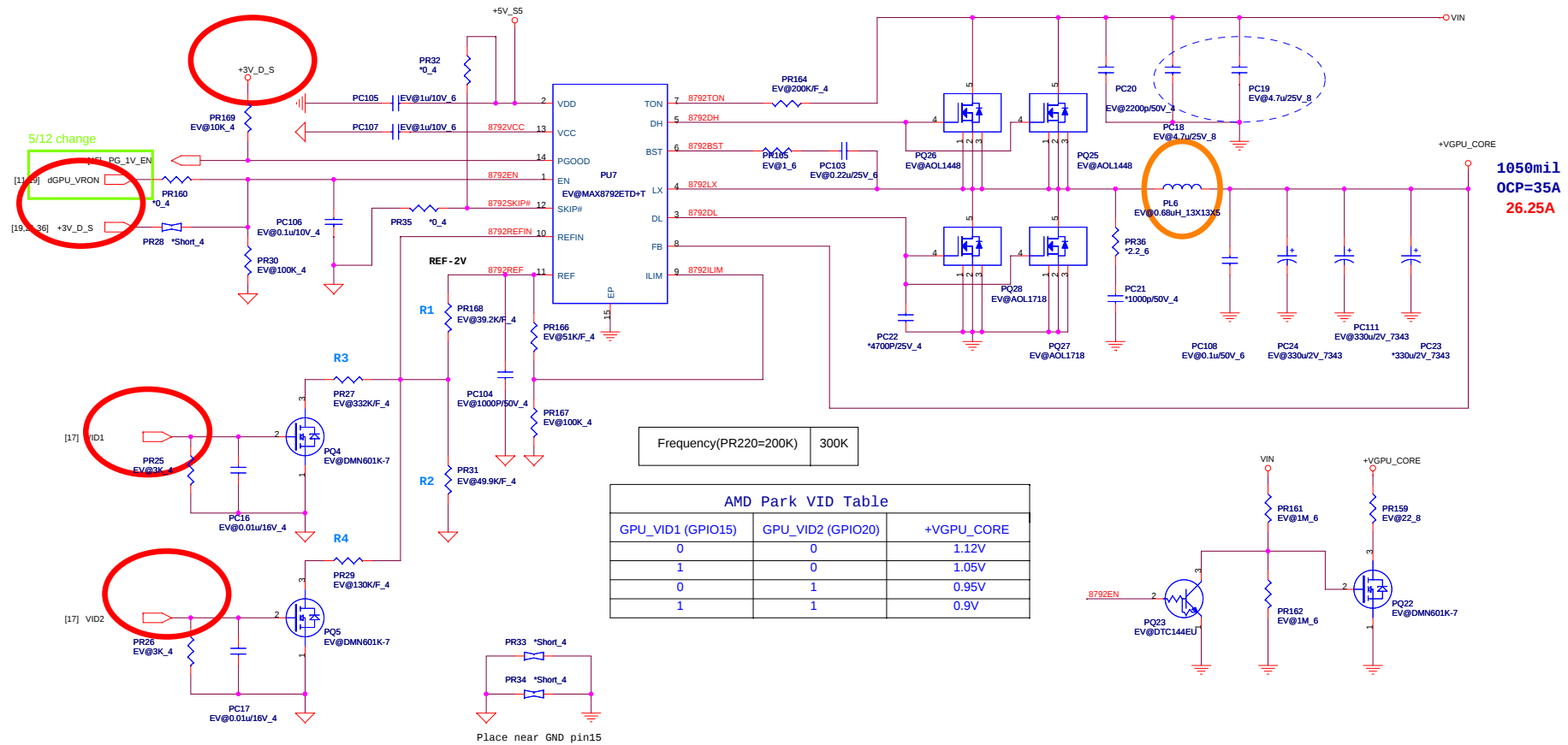
$$R_{ILIM} = 2.15m\Omega \cdot 23 - 3.256 / 20uA = 2.122K\Omega$$

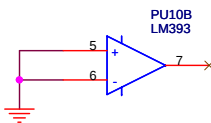
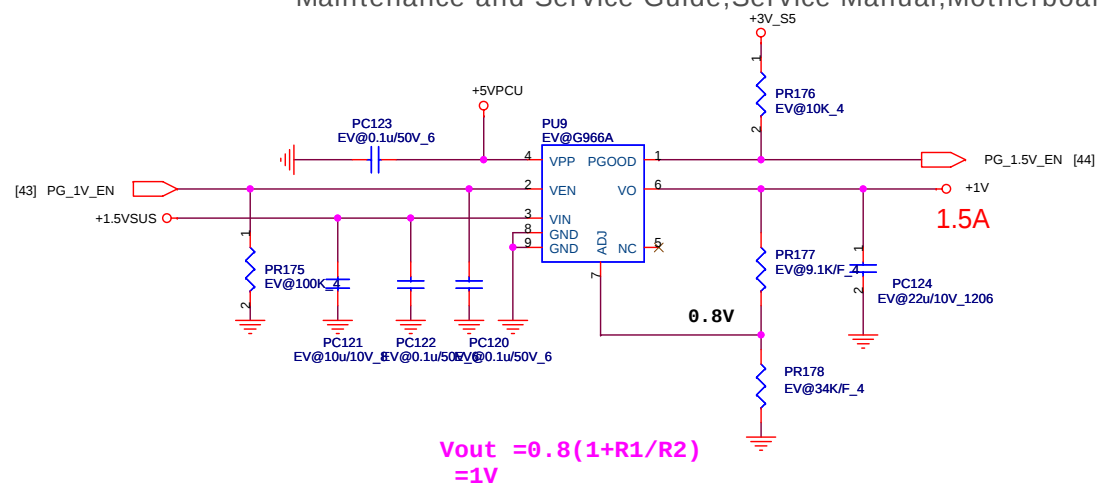
$$I(\text{choke})_{\text{peak}} = 29.512A$$

[PWM]





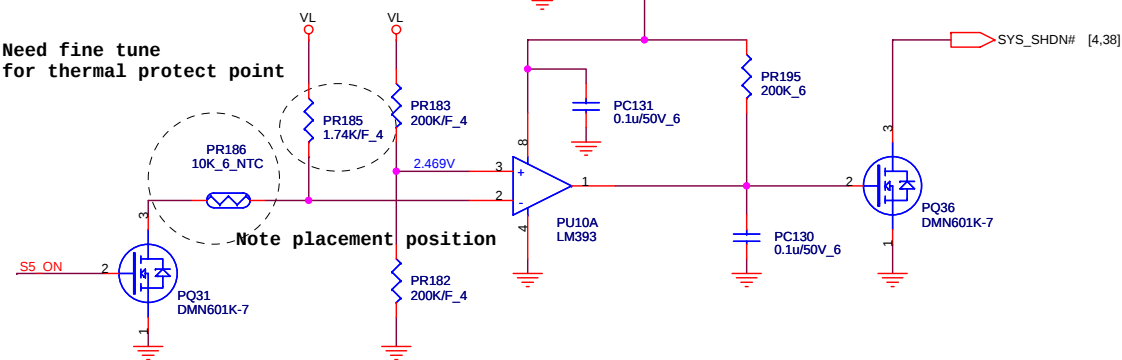




For EC control thermal protection (output 3.3V)

Thermal protection

Need fine tune
for thermal protect point



Model		REV	CHANGE LIST	MODEL	ZY9B
ZY9B MB	1A	FIRST RELEASED		FROM	To
	2A		Page 3 : Unstuff L54 & stuff R586 & change U31 P/N for 3V CLK gen and Switch CLK_BUF.DREFSSCLK and CLK_BUF.PCIE_36PLL	X	1A
			Page 4 : Q18 Change P/N for E00 part & short R116 (Del.) for 0 ohm	X	1A
	3A		Page 8 : Short R224 (Del.) for 0 ohm	1A	2A
Page 10 : Short R242 (Del.) for 0 ohm			1A	2A	
		Page 12 : Short R189 , R199 & R543 (Del.) for 0 ohm & C655 change P/N for E00 part	1A	2A	
		Page 14 : R248 & R247 for RS solution & stuff R269 , R229 , R225 & R226 for M1 solution, Stuff C372 for +1.5VSUS leakage	1A	2A	
		Page 15 : Stuff C459 for +1.5VSUS leakage	1A	2A	
		Page 25 : Q12 , Q17 & Q19 Change P/N for ESD , CN10 Change P/N , Q14.2 & Q13.2 Change from +5V to +3V	1A	2A	
		Page 27 : C339 & C281 footprint change from 0805 to 0402 for ESD	1A	2A	
		Page 28 : Unstuff R460 , R234 , R233 , R219 , R276 , R272 for disable debug card function	1A	2A	
		Page 29 : C383 & C254 change P/N for E00 , CN11 Change footprint for ME design request.	1A	2A	
		Page 30 : R193 change amp circuit	1A	2A	
		Page 31 : Q22 & Q33 change P/N for E00 part.	1A	2A	
		Page 32 : R51 , L35 , CN12 Change P/N	1A	2A	
		Page 36 : C27 change P/N for E00 part	1A	2A	
		Page 41 : Change to short pad : Location : R458 , R452 , R537 , R533 , R144 , R155 , R191 , R140 , R201 , R224 , R461 , R136 , R197 , R206 , R219 , R212 , R166 , R174 , R188 , R202 , R209 , R184 , R168 , R185 , R448 , R447 , R5 , R10 , R9 , R6 , R263 , R288 , R544 , R436 , R563 , R570 , R569 , R584 , R299 , C738 , R311 , R585 , R583 , R571 , R582 , R575 , R576 , R579 , R333 , R352 , R331 , R332 & R349	1A	2A	
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