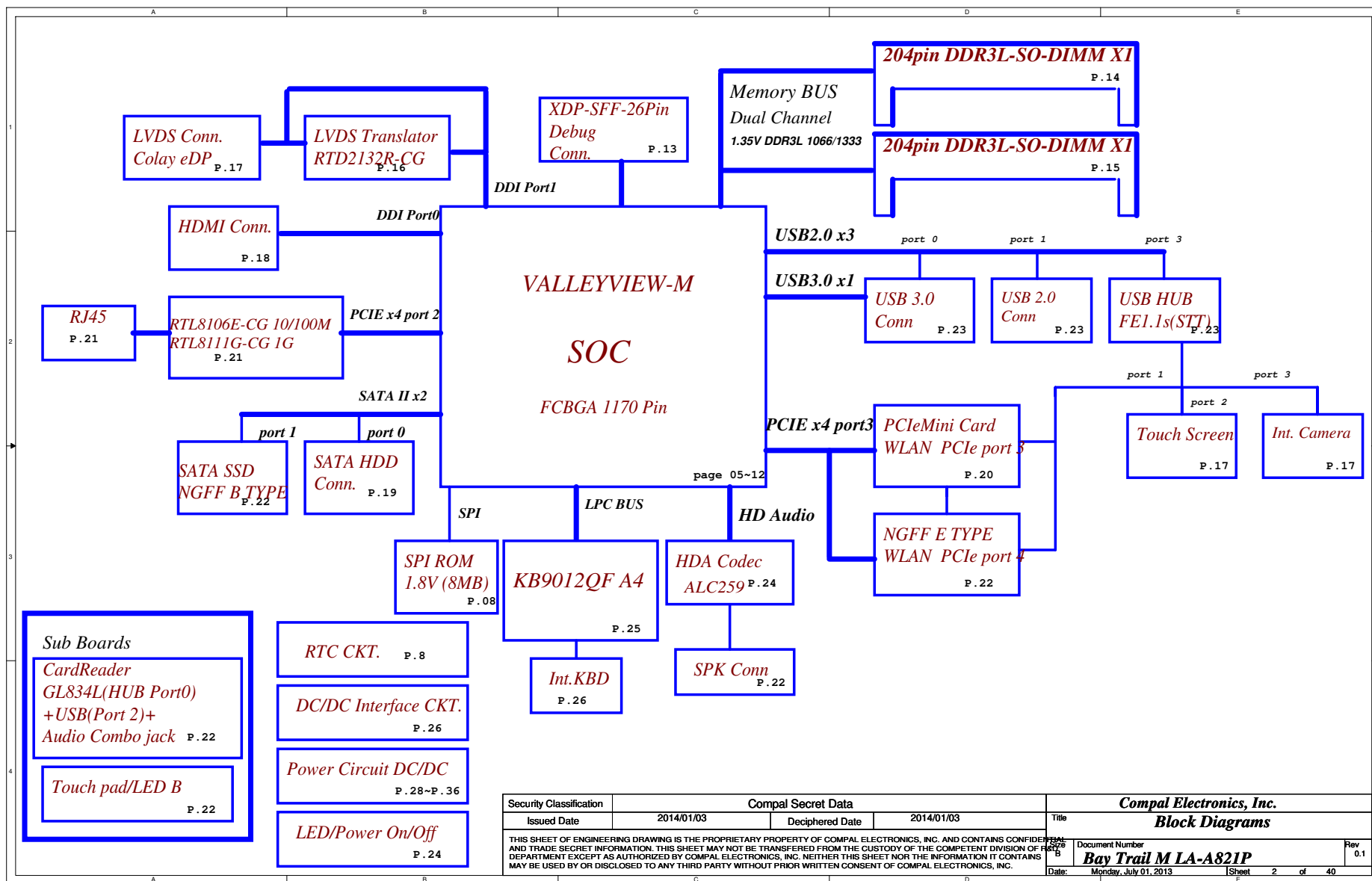


Intel BayTrail-M Platform

Date : 2013/05/22
Version 0.1

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/01/03	Deciphered Date	2014/01/03	Title	
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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
--------	---------

SOC SM Bus address

Device	Address
SO-DIMM A (JDIMM1)	A0h
SO-DIMM B (JDIMM2)	A2h

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
XDP (Debug Port)	XDP@
EMC requirement	EMC@
EMC requirement unpop	@EMC@
TPM	TPM@
Touch Screen	TS@
R short	RS@
Test Point	TEST@

BOM config

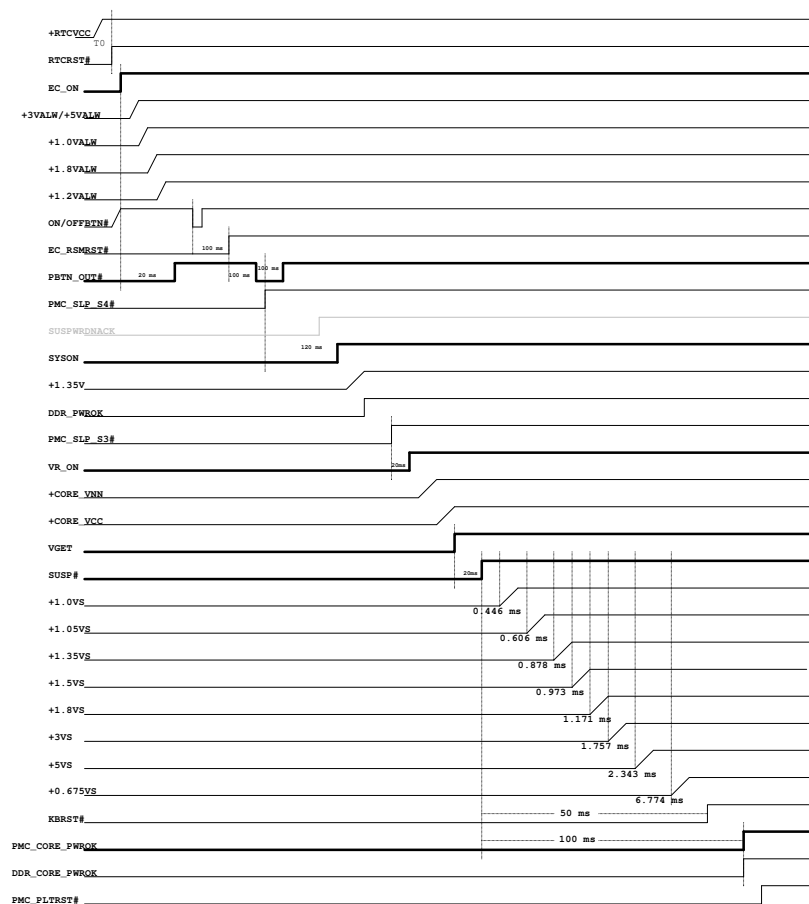
PCB P/N
EVT BOM config

43 level BOM table

43 Level	Description	BOM Structure
----------	-------------	---------------

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				Bay Trail M LA-A821P
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Power ON

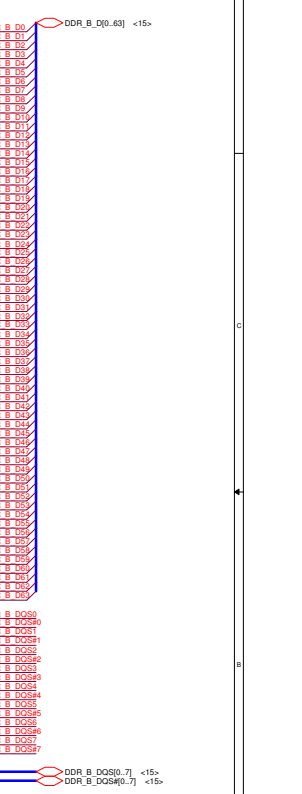
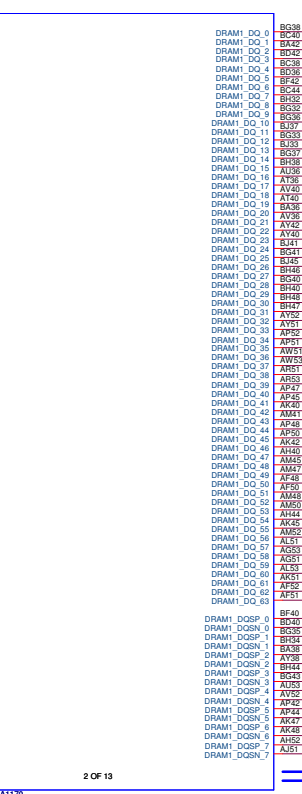
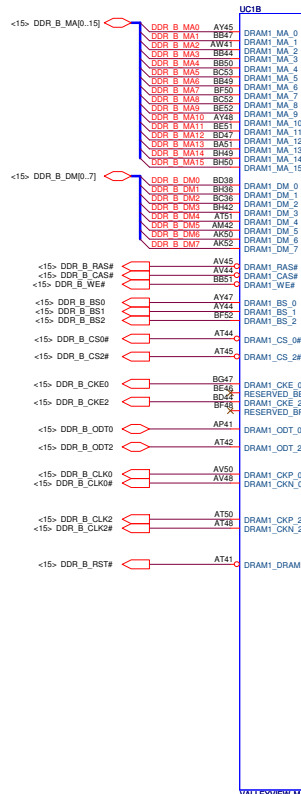
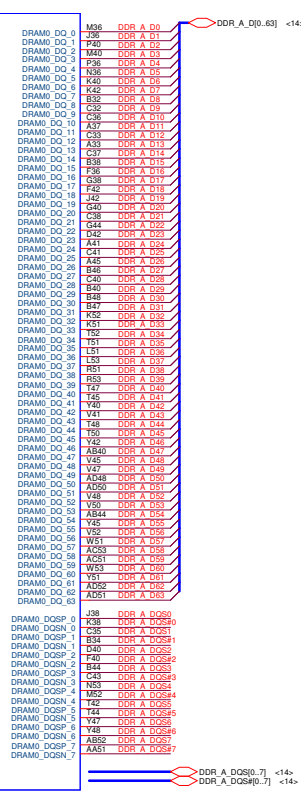
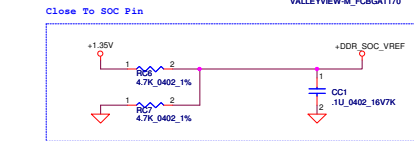
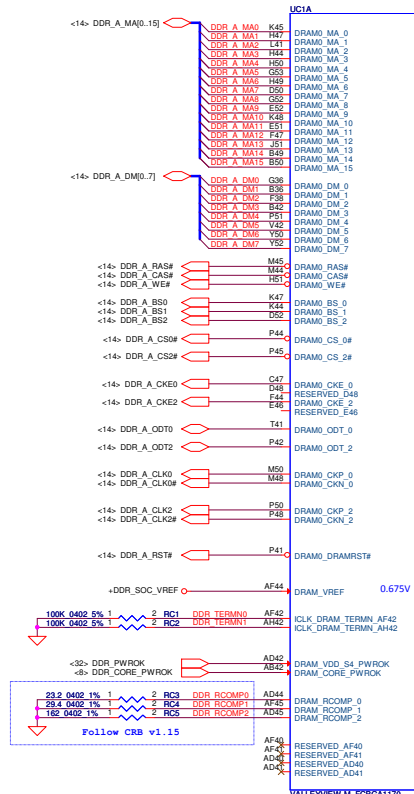


T0: +RTCVCC stable to RTCRST# high > 9ms
T1: VR ramp up time from 10% to 90% voltage level < 2ms
T2 :Rail to subsequent rail turn on delay < 2ms
T3 :+VALWAS stable to EC_RSMRST# high > 10ms
T4 :+VS rails stable to PMC_CORE_PWROK > TBD

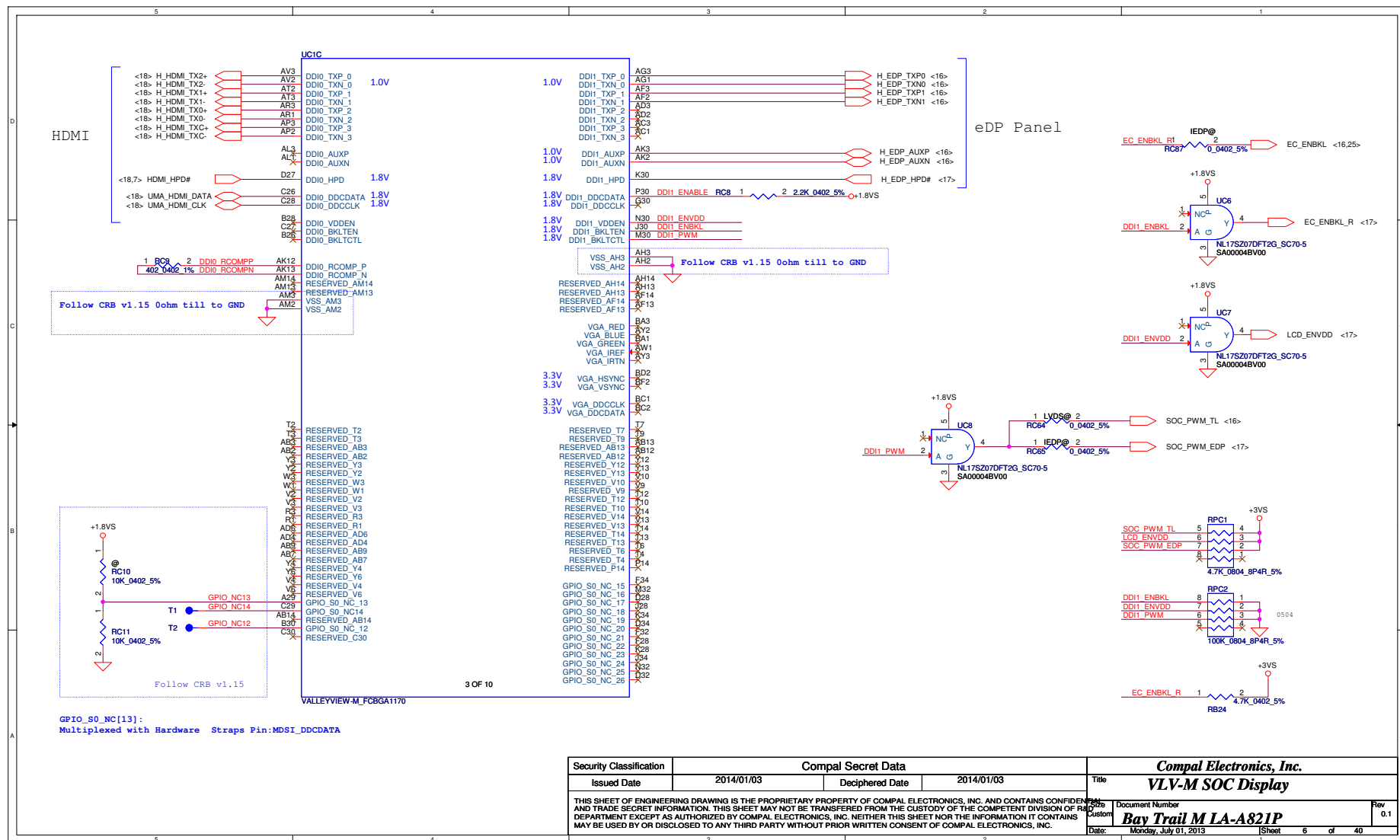
NOTE:
1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.

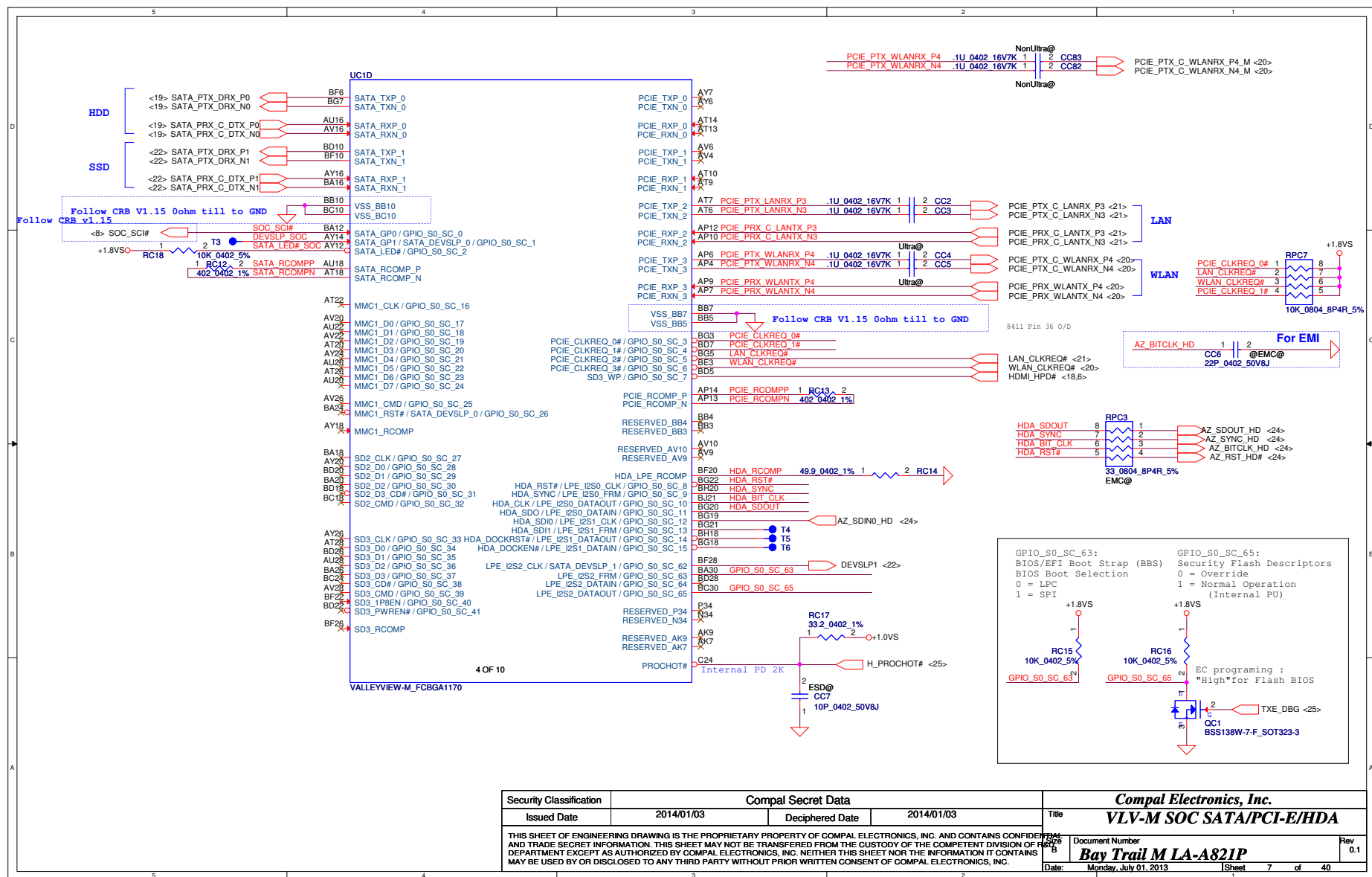
2. Platform devices other than SOC sequencing are not explicitly shown as they are not limited by the SOC sequencing requirement.

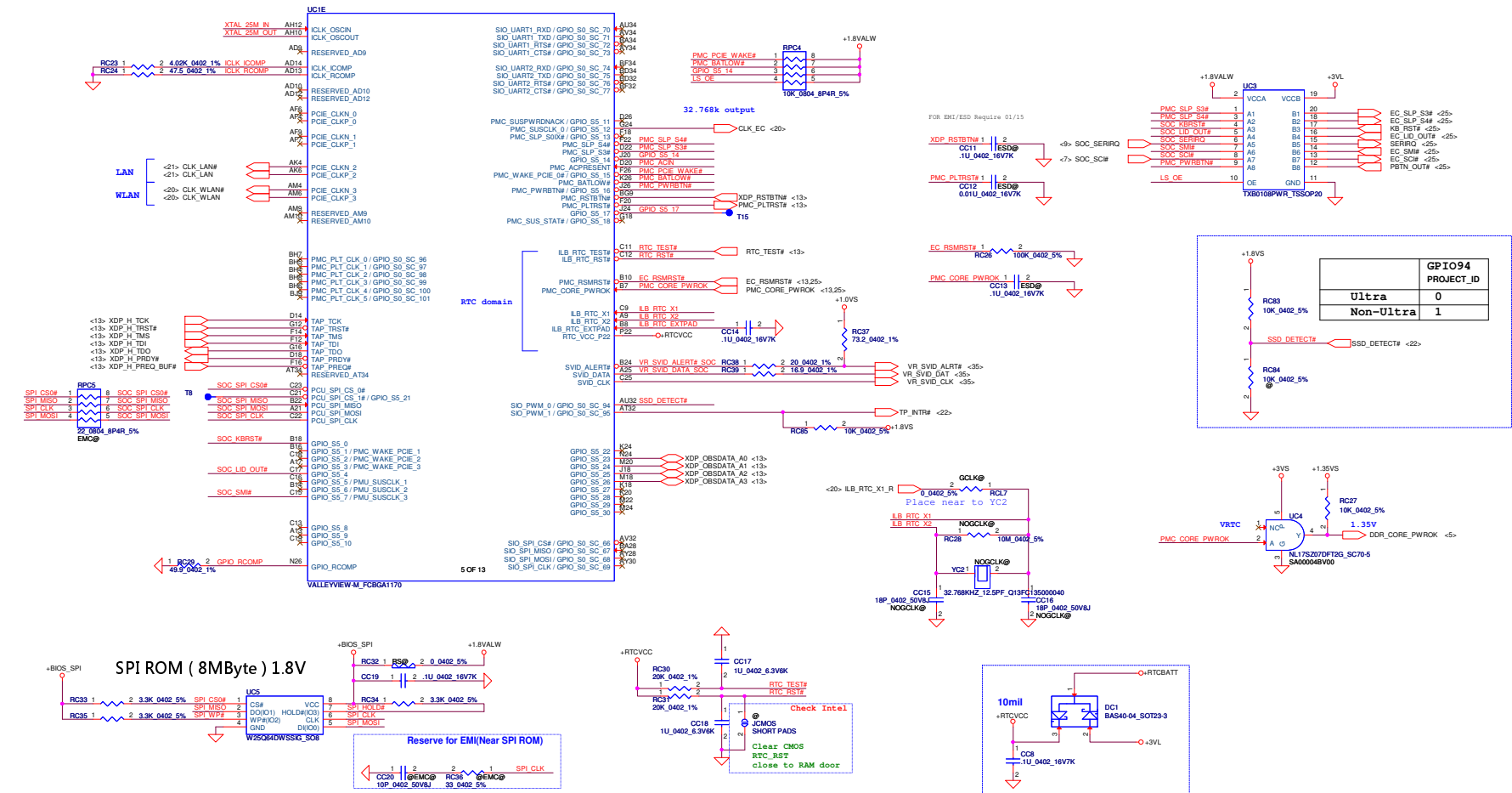
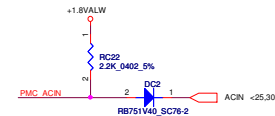
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/01/03	Deciphered Date	2014/01/03	Title
				Power Sequence
				Document Number
				Bay Trail M LA-A821P
				Date
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				Sheet 4 of 40

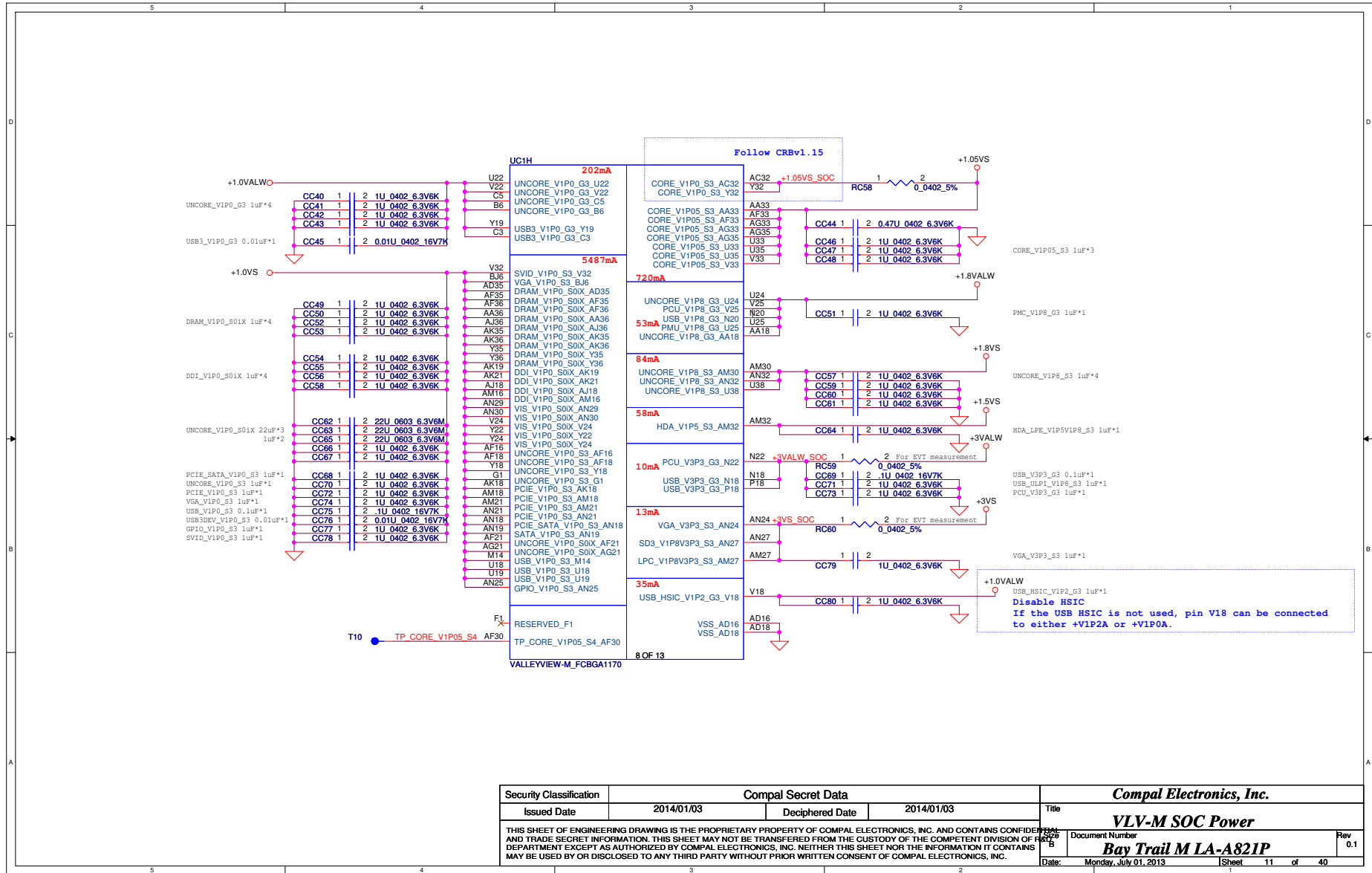


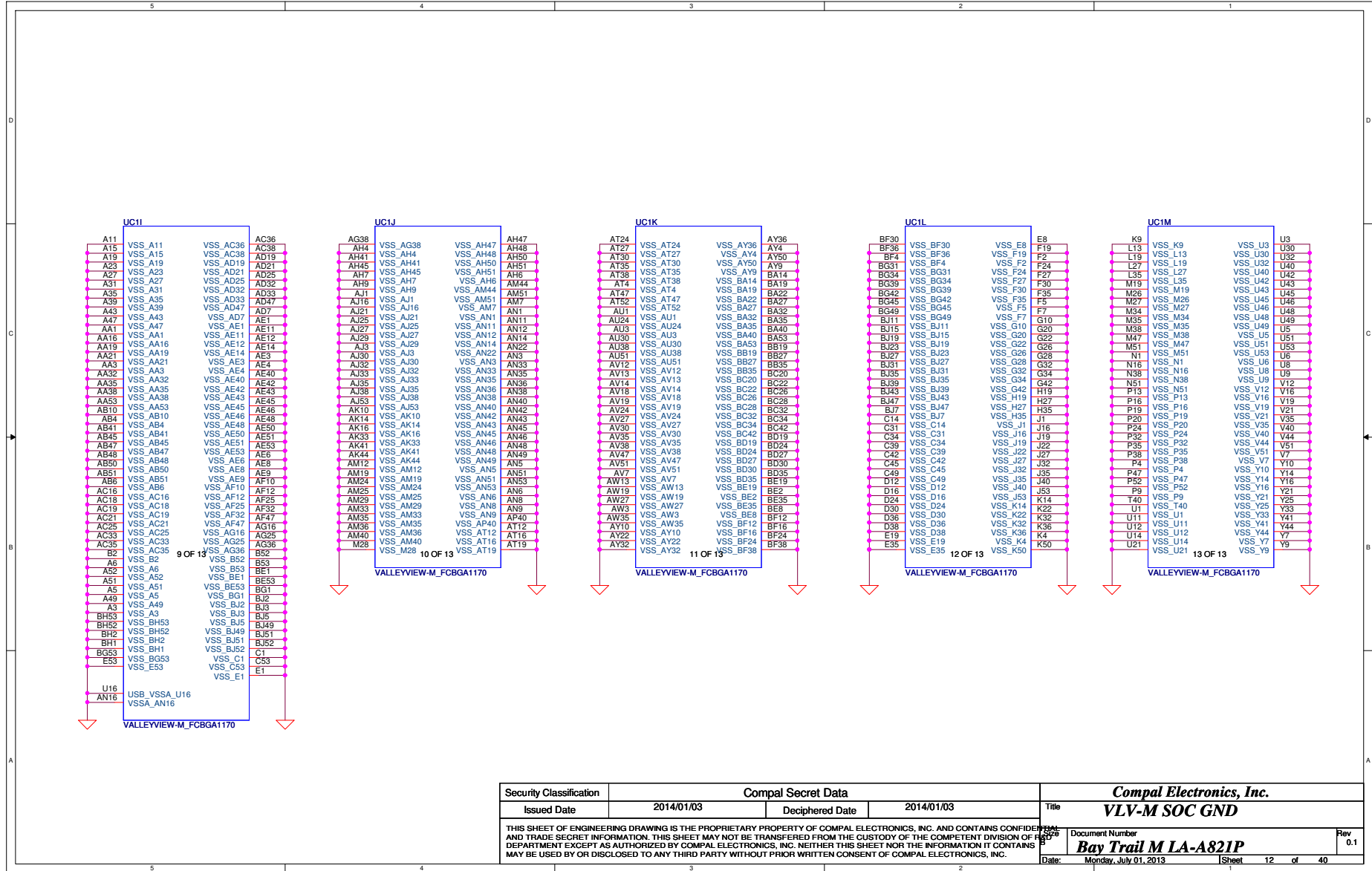
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/01/03	Deciphered Date	2014/01/03	Title	VLV-M SOC Memory DDR3L
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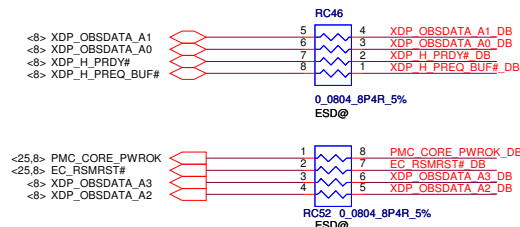
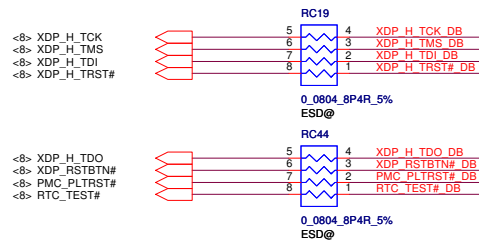
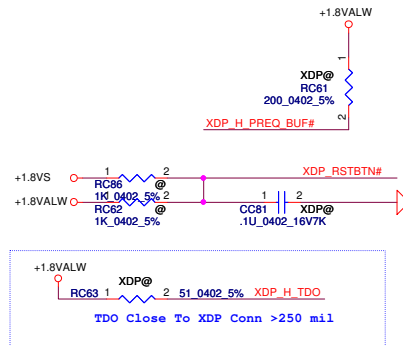




CONN@
JDB1

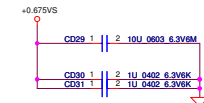
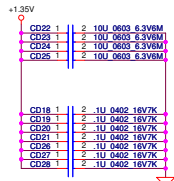
Signal	Pin
XDP_H_PREQ_BUF#_DB	1
XDP_H_PRDY#_DB	2
XDP_OBSDATA_A0_DB	3
XDP_OBSDATA_A1_DB	4
XDP_OBSDATA_A2_DB	5
XDP_OBSDATA_A3_DB	6
EC_RSMRST#_DB	7
PMC_CORE_PWROK_DB	8
RTC_TEST#_DB	9
PMC_PLTRST#_DB	10
XDP_RSTBTN#_DB	11
XDP_H_TDO_DB	12
XDP_H_TRST#_DB	13
XDP_H_TDI_DB	14
XDP_H_TMS_DB	15
XDP_H_TCK_DB	16
G1 G2	17
GND	18
GND	19
GND	20
GND	21
GND	22
GND	23
GND	24
GND	25
GND	26

MOLEX 52435-2671 26P P0.5
PCB Footprint = MOLEX_52435-2671_26P_



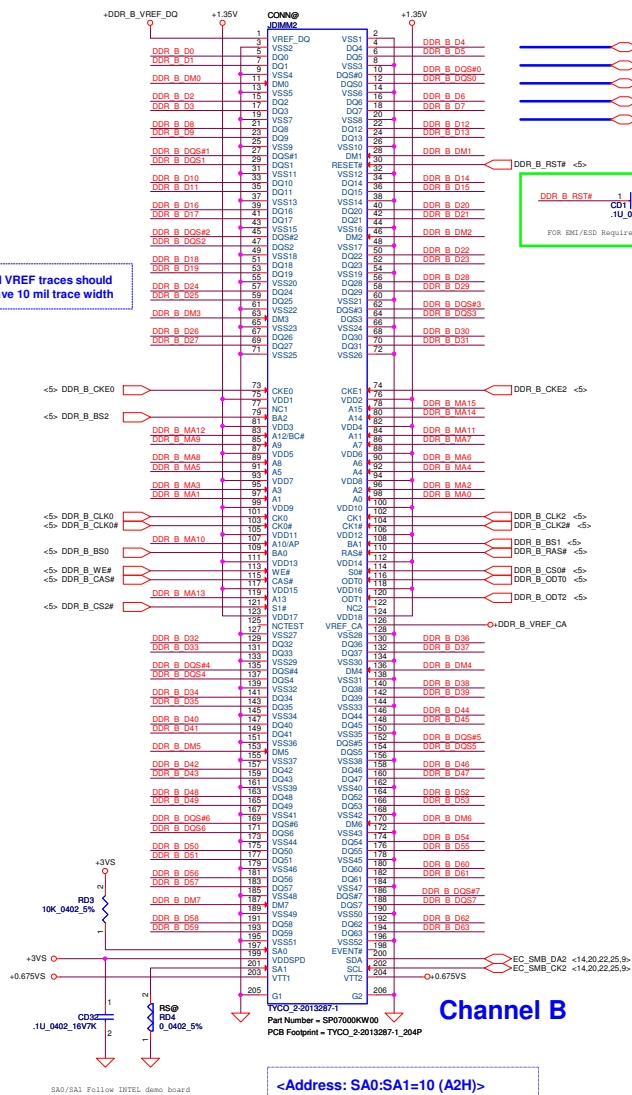
Security Classification		Compal Secret Data		Compal Electronics, Inc. VLV-M SOC Debug	
Issued Date	2014/01/03	Deciphered Date	2014/01/03	Title	
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Layout Note:
Place near JDIMM2



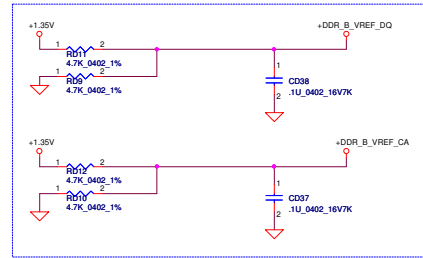
Layout Note:
Place near JDIMM2.203,204

All VREF traces should
have 10 mil trace width

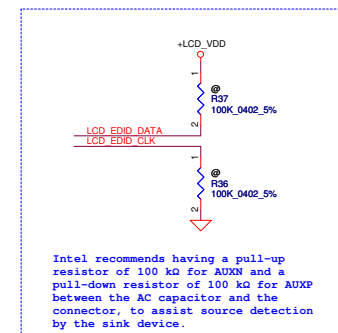
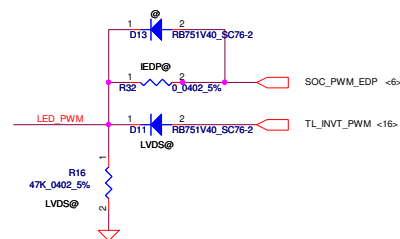
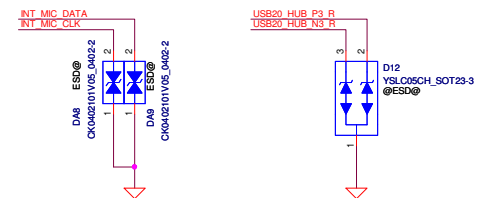


Channel B

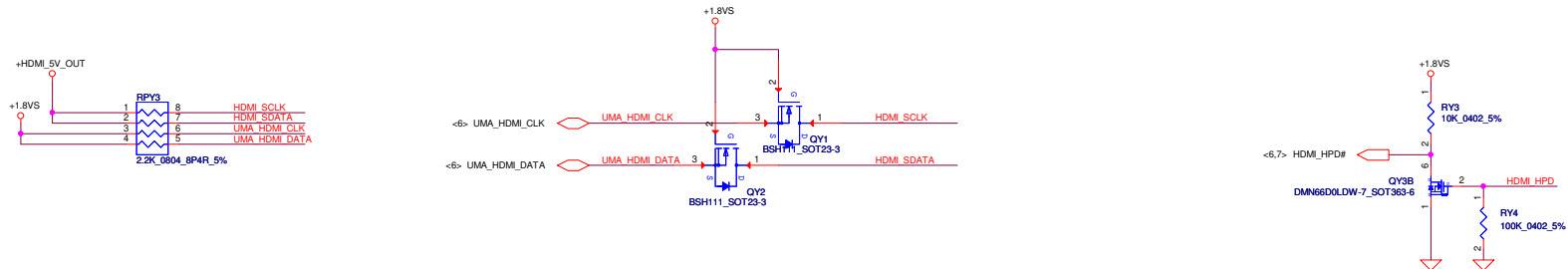
<Address: SA0:SA1=10 (A2H)>
DIMM_2 REV H:4mm



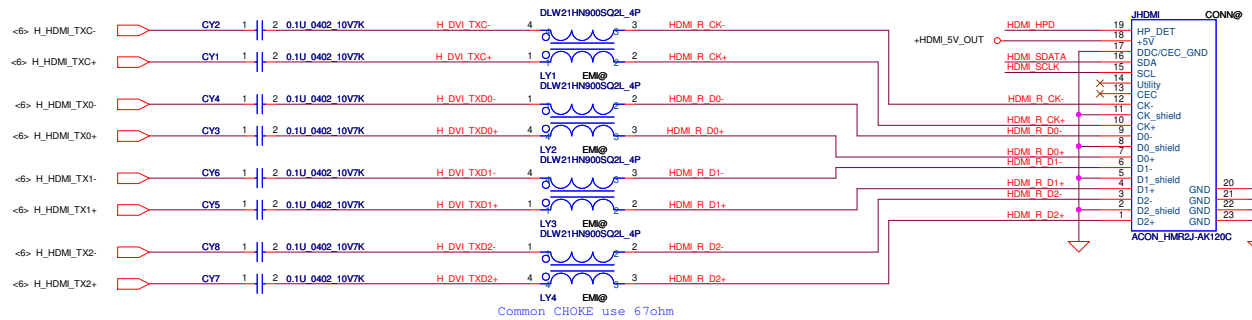
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Issued Date		Deciphered Date		Title	
2014/01/03		2014/01/03		DDR3L DIMMB	
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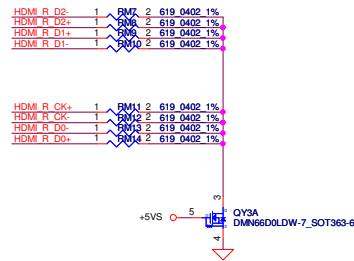
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Issued Date	2014/01/03	Deciphered Date	2014/01/03	Title	LVDS	
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HDMI Connector

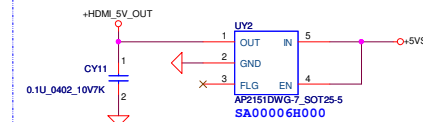


HDMI Royalty
 ZZZ1 HDMH5@
 RO0000003HM
 HDMI W/Logo + HDCP
 HDMI W/O Logo: RO0000001HM
 HDMI W/Logo: RO0000002HM
 HDMI W/Logo + HDCP: RO0000003HM
 please manually load
 this virtual material to 45@ BOM



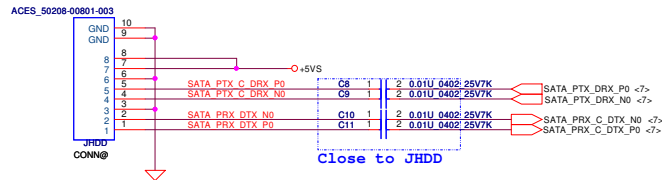
HDMI POWER CIRCUIT

VIN = 5V, IOUT = 0.5A, RDS(ON) TYP=95m ; MAX=115m
 Current Limit: TYP=0.8A ; MAX=1A

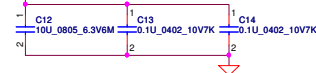


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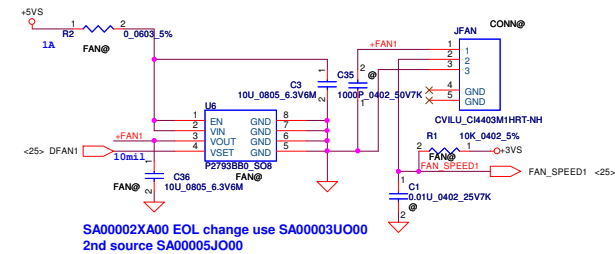
SATA HDD Conn.



Place closely JHDD SATA CONN.



FAN Control Circuit



Slot 1 Half PCIe Mini Card-WLAN

WLAN6BT Combo module circuits

WLAN6BT Combo module circuits	BT on module	BT on module Disable
BT_ON	H	L

Mini PCIe type for Non-Ultra

WLAN/WiFi

WIMax/ BT

NGFF E TYPE for Ultra

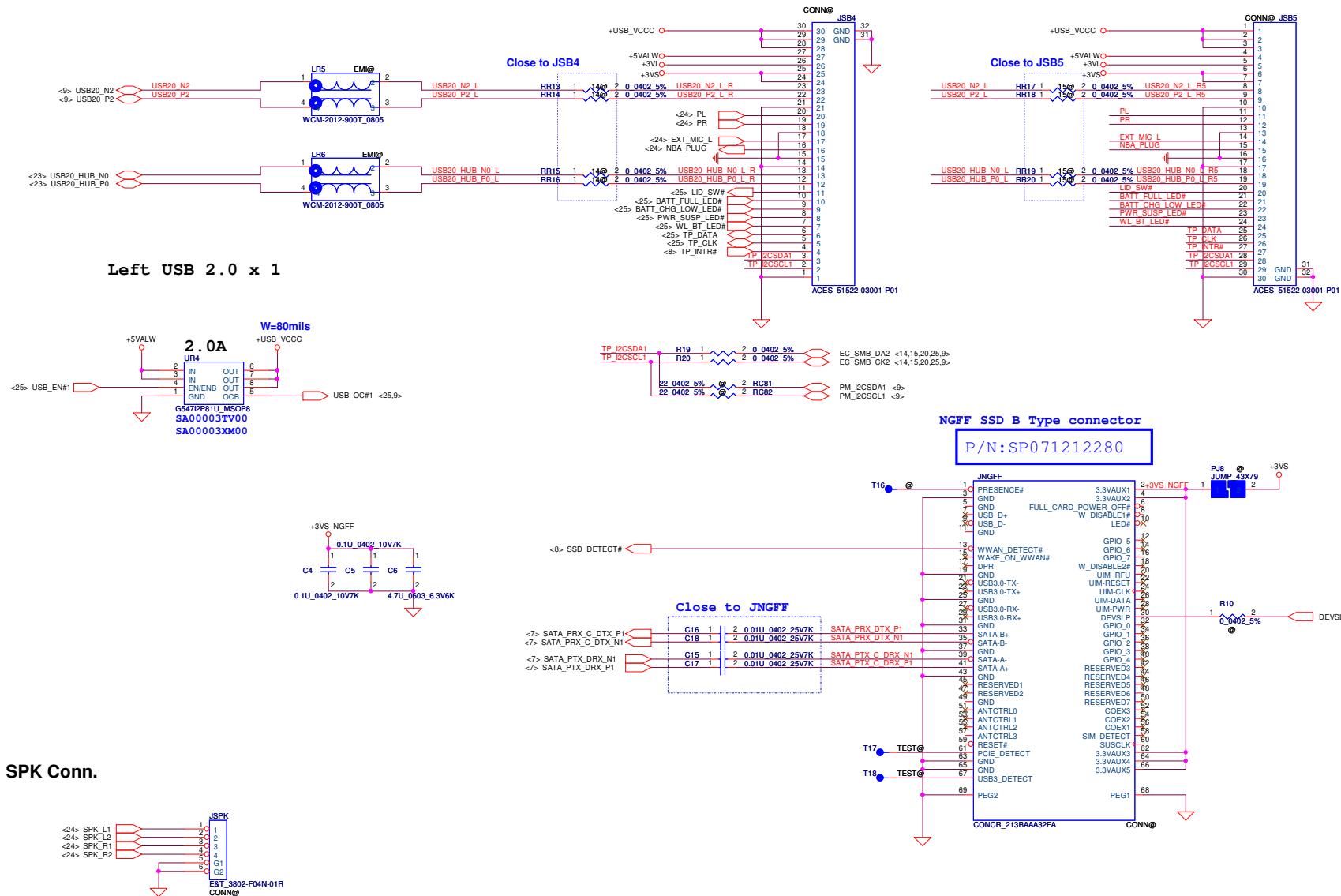
Green Clock

For safety request

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			PCle-WLAN/mSATA/GCLK Bay Trail M LA-821P		0.1
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Small board Conn



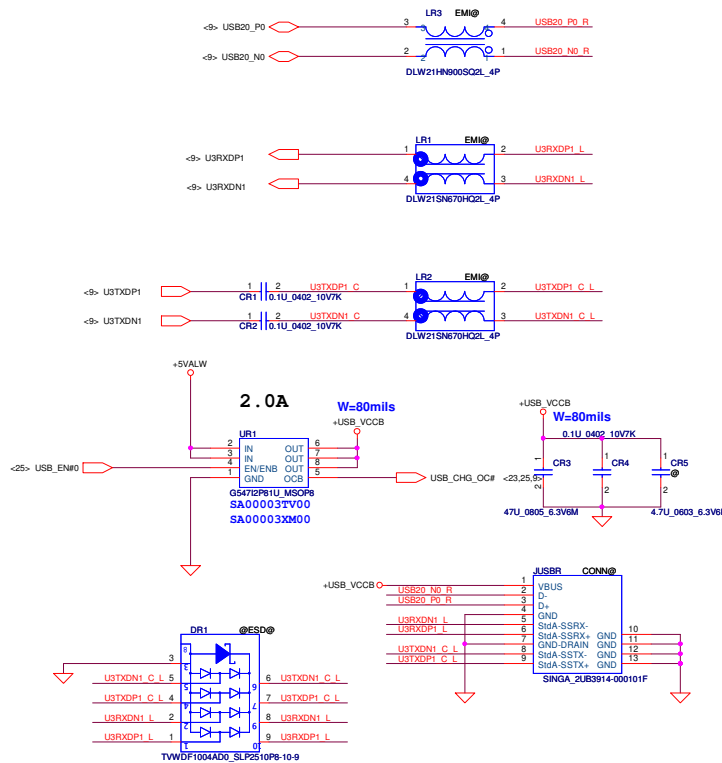
Security Classification		Compal Secret Data		Compal Electronics, Inc. NGFF SATA/S_B conn/SPK	
Issued Date	2014/01/03	Deciphered Date	2014/01/03	Title	
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				Date: Monday, July 01, 2013	Sheet 22 of 40

USB Sleep & Charge

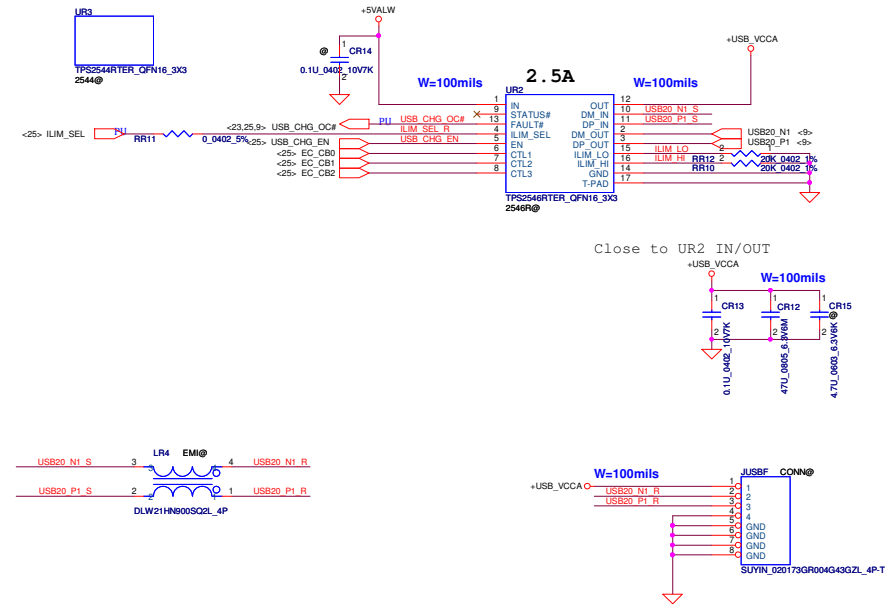
State table for TPS2546RTER

CB0	CB1	CB2	ILIM_SEL	Mode	STATUS
0	1	1	1	Auto	Auto-detection charger mode for Apple device(2A,1A). Resistor dividers are connected to DP/DM. Including DCP
1	0	1	1	Alternate	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	1	1	0	SDP	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	1	1	CDP	USB pass-through mode with CDP emulation. DP/DM are connected to TDP/TDM

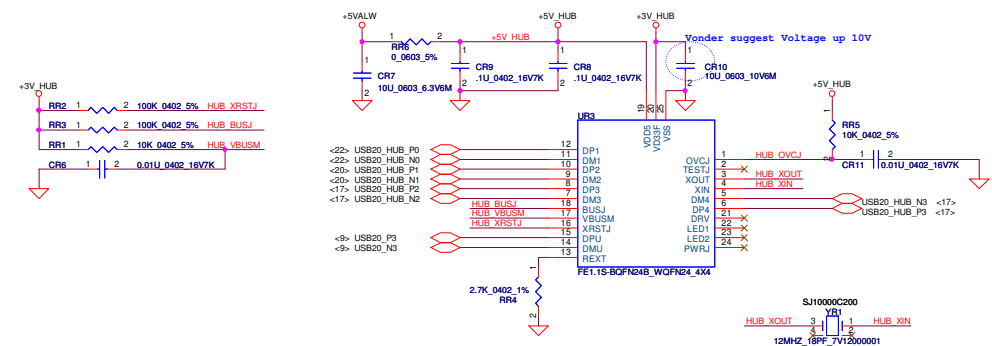
RIGHT REAR USB3.0 CONN.



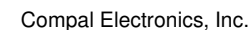
RIGHT FRONT USB 2.0 W/S&C



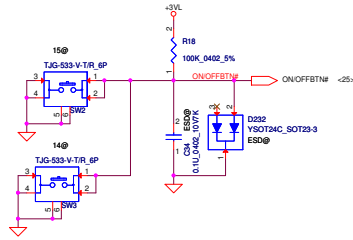
USB 2.0 HUB



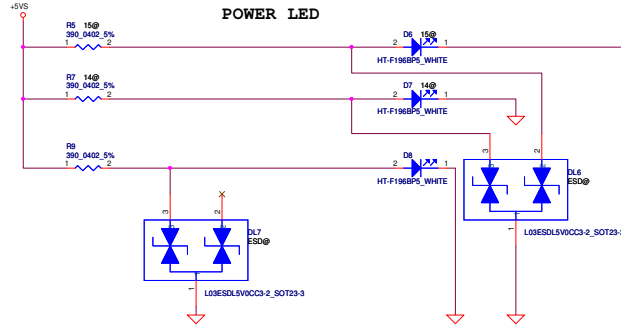
Security Classification	Compal Secret Data			Title	
Issued Date	2014/01/03	Deciphered Date	2014/01/03	Compal Electronics, Inc.	
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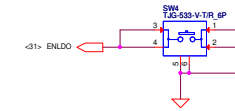
Power Button



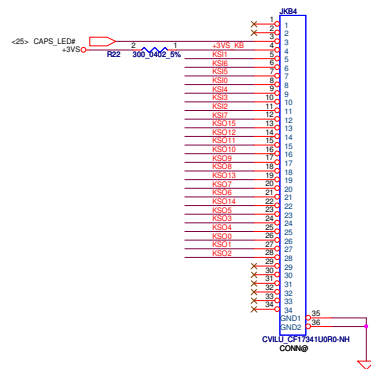
POWER LED



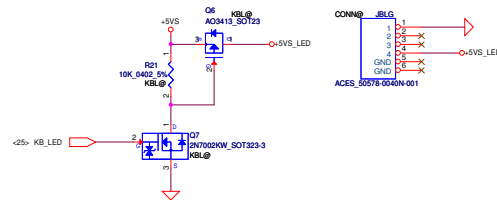
Battery Reset



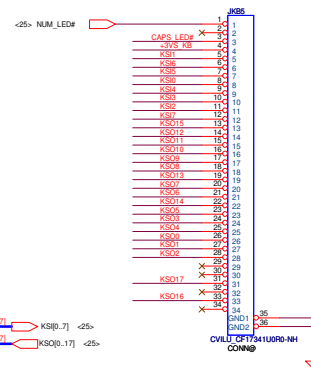
14 " KEYBOARD CONN.



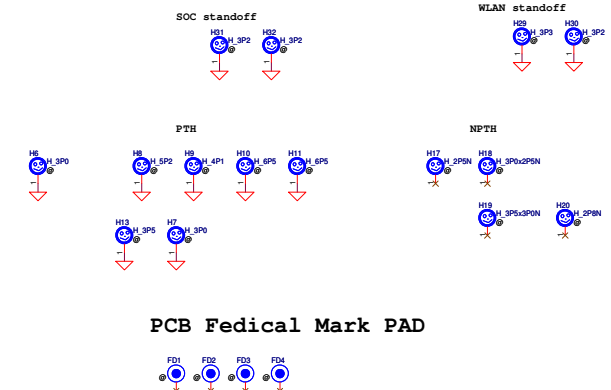
Keyboard LED



15" KEYBOARD CONN.



Screw Hole

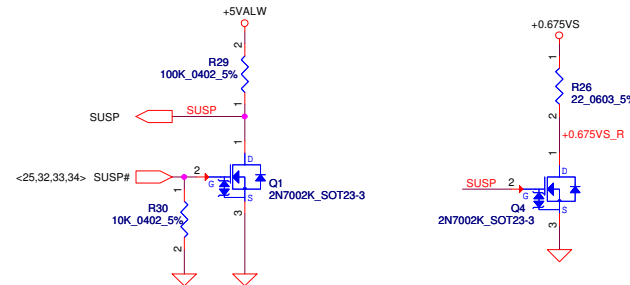
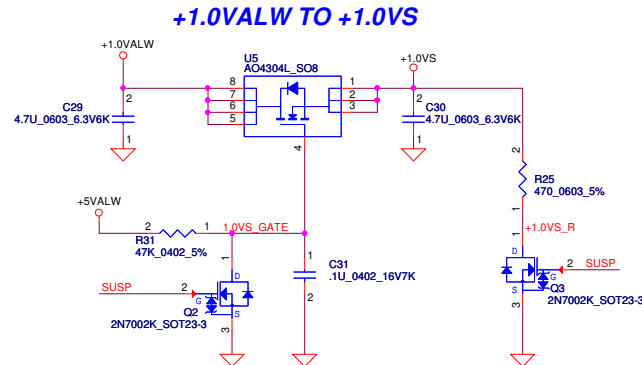
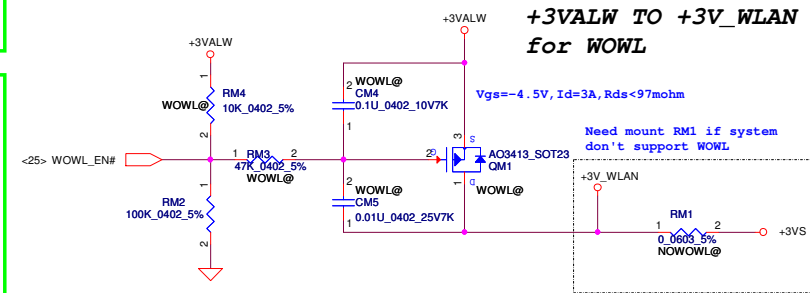
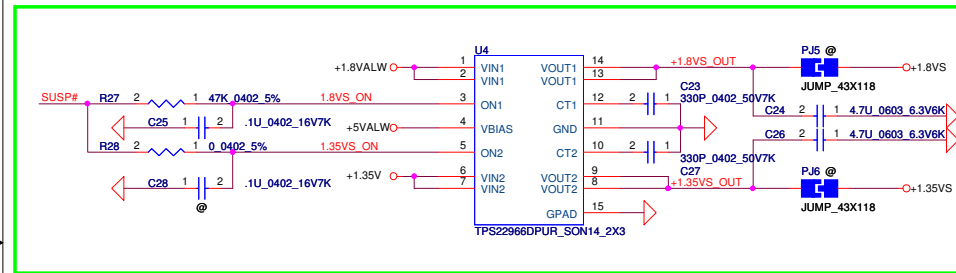
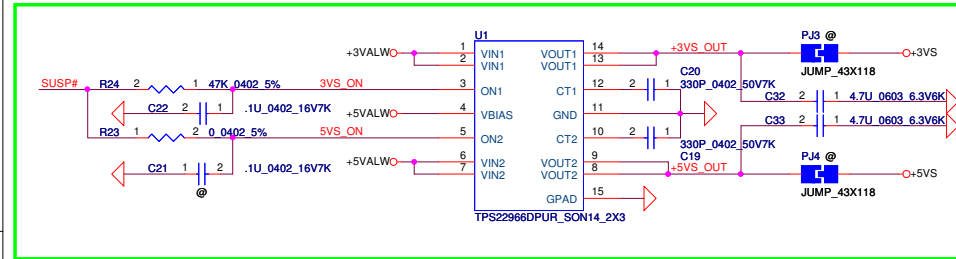


ISPD

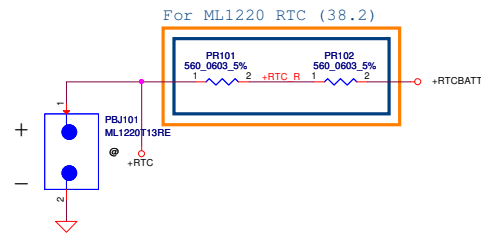
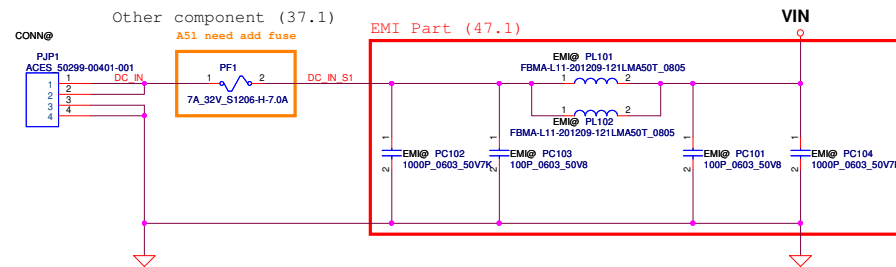


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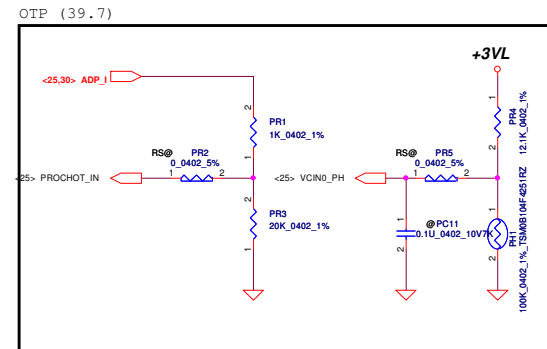
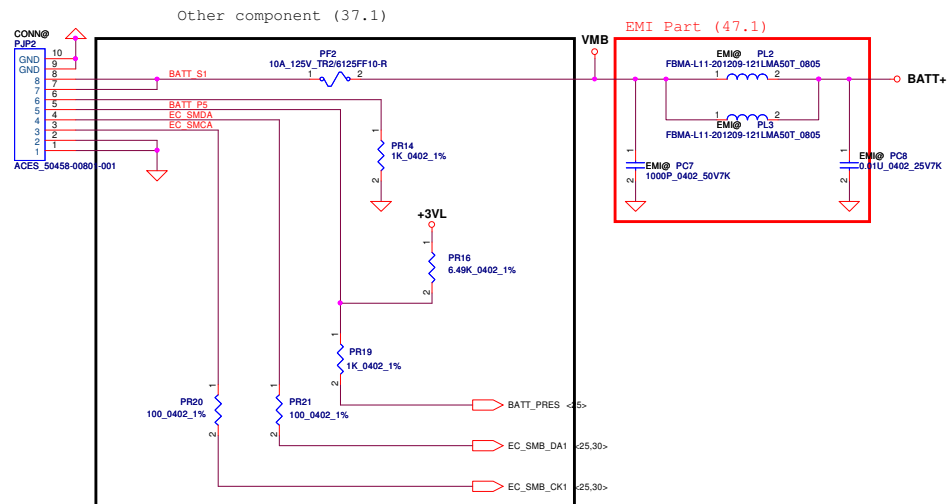
Normall Platform (Not support M-STATE and Deep Sleep)



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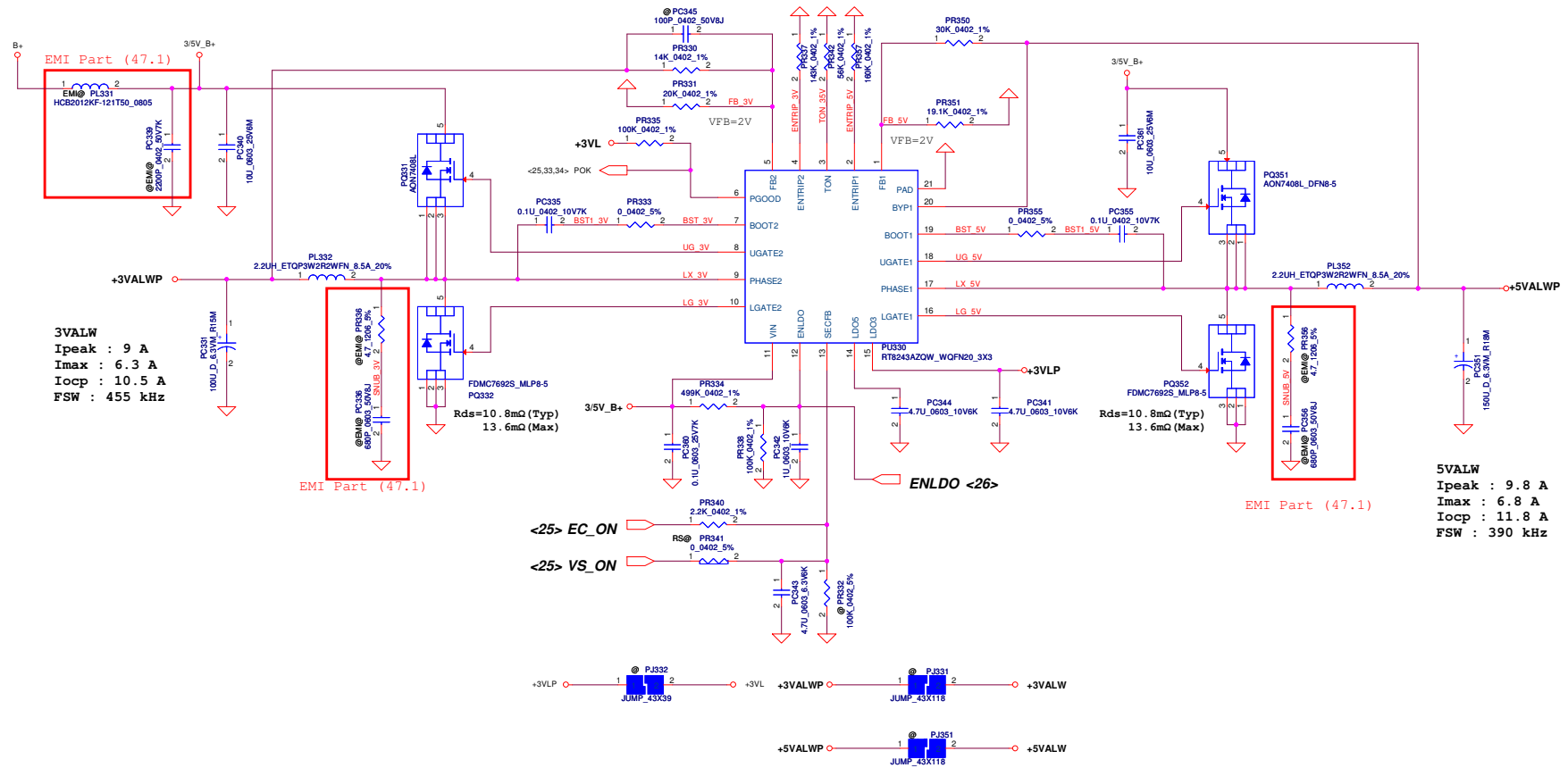


	Initial	Recovery
45W UMA	0.55V	0.43V
75W N14P-GV2	0.90V	0.72V

	Initial	Recovery
CPU OTP	90 C	70 C

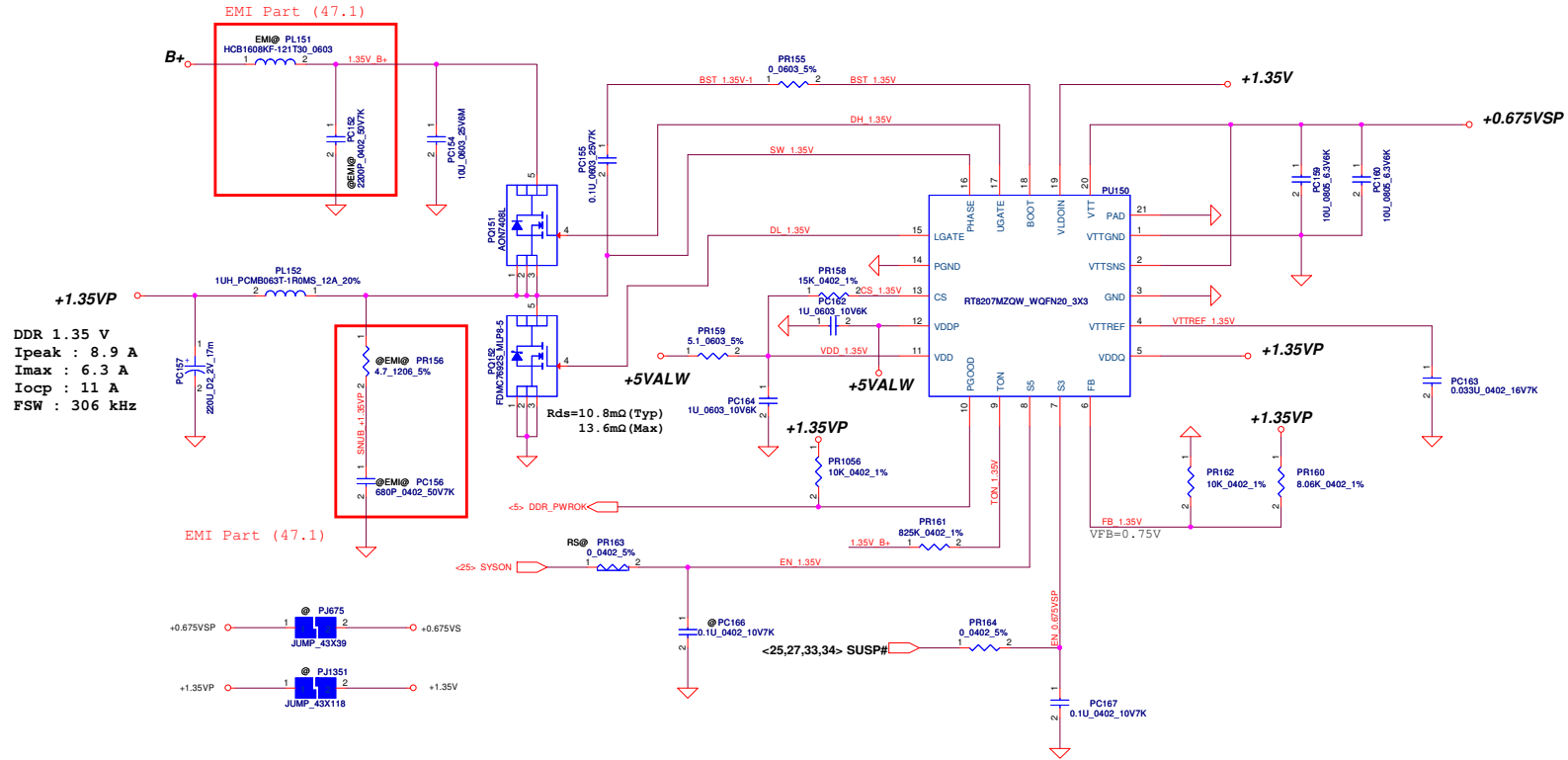
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3/5VALW controller (35.1), Support component (35.2)



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					ZRMAA
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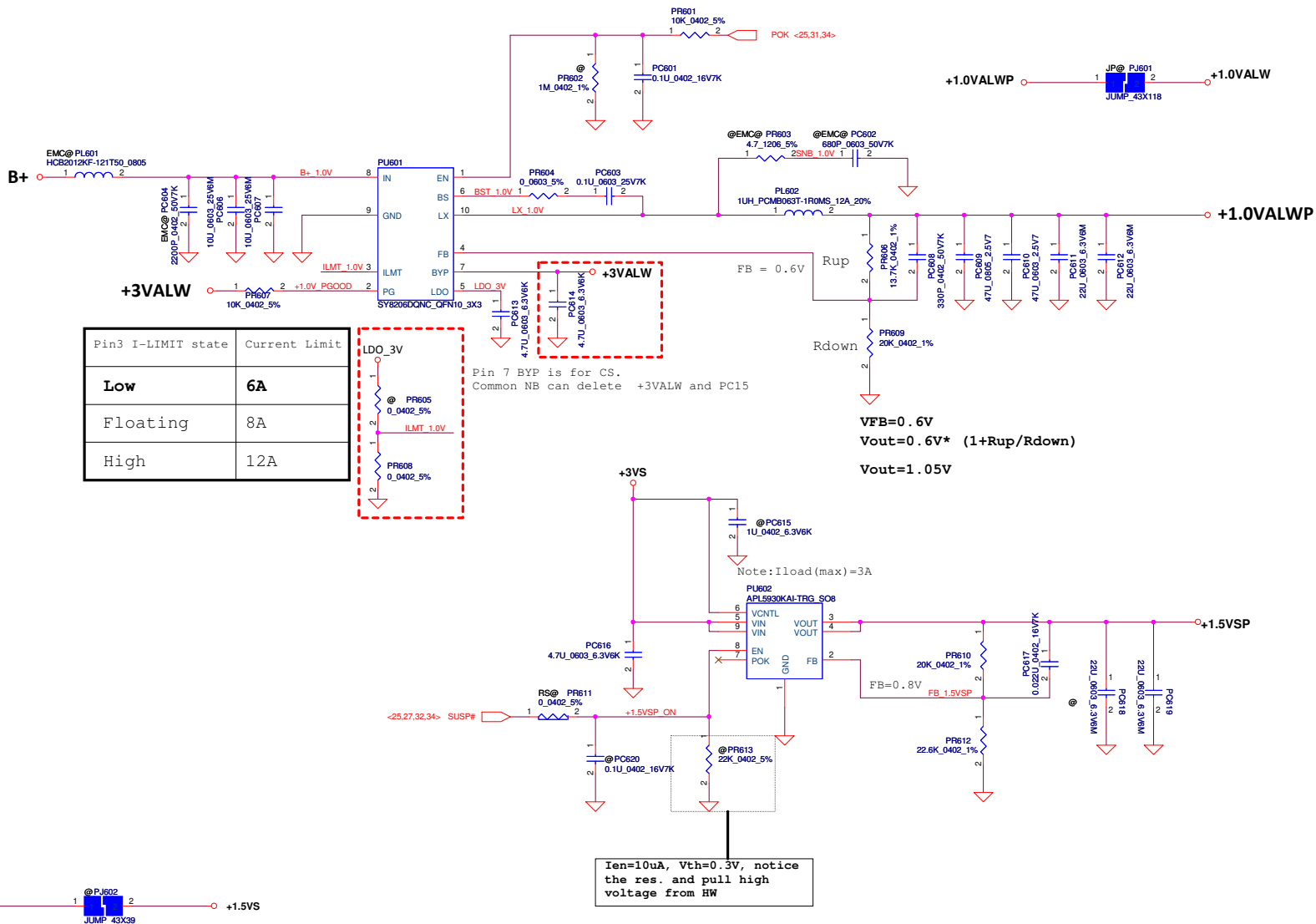
DDR controller (35.3), Support component (35.4)



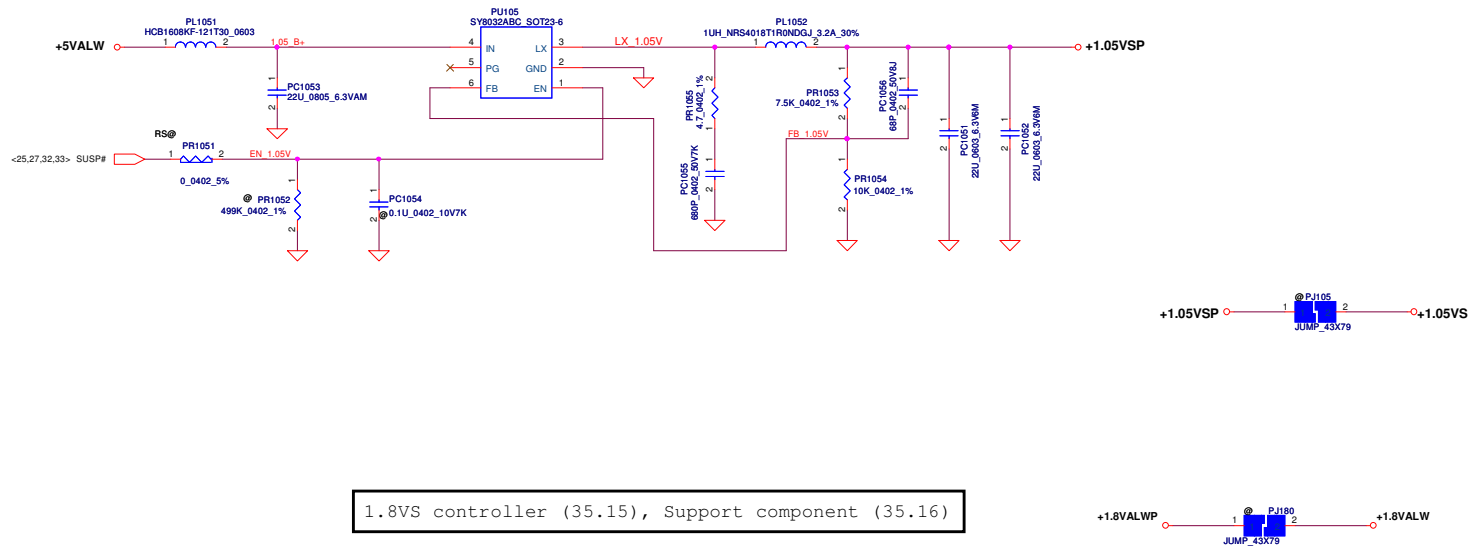
STATE	S3	S5	1.5VP	VIT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

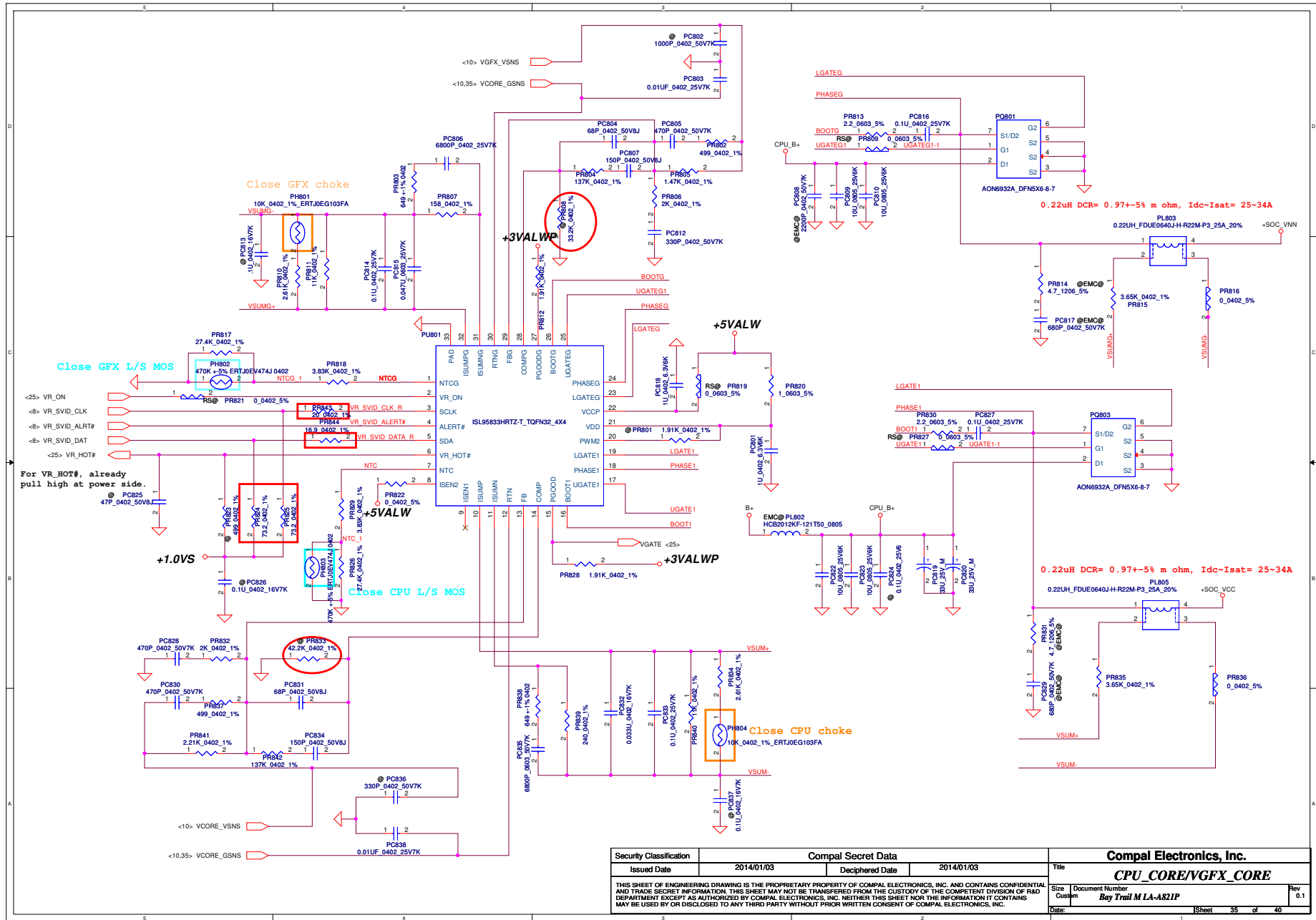
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				Document Number
				V5WE2 M/B LA-9531P Schematic
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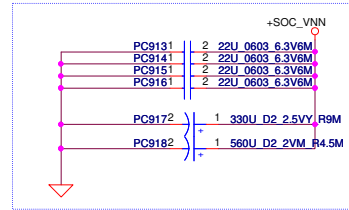
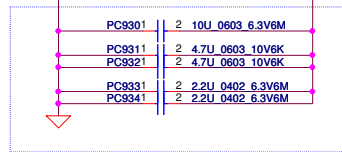
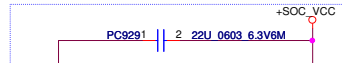
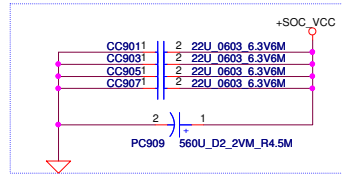
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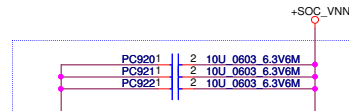
Output Cap

Package Edge Cap

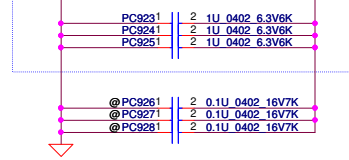
Back Side Cap



Output Cap



Package Edge Cap



Back Side Cap

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Notes
POSCAP 330 μ F	2	6 m Ω	1.8 nH	Output	1, 2
22 μ F 0805 X5R	4	3 m Ω	0.6 nH	Output	

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Notes
POSCAP 330 μ F	3	6 m Ω	1.8 nH	Output	1, 2
22 μ F 0805 X5R	4	3 m Ω	0.6 nH	Output	

Package Pin Name	Back Side Cap	Package Edge Cap	Comments
CORE_VCC_S0IX	1X0603 10 μ F 2X0402 4.7 μ F 2X0402 2.2 μ F	3X0805 22 μ F	
UNCORE_VNN_S3	3X0402 1 μ F	3X0805 10 μ F	

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HW PIR (Product Improve Record)

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HW PIR (Product Improve Record)

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