

	1	2	3	4	5	6	7	8	
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B									B
C									C
D									D
E									E
F									F

ROCKY AMD-Sabine 15"

DB

2010/08/09

DATE	CHANGE NO.	REV
1	2	

	EE	DATE	POWER	DATE
DRAWER	ALAN W		ALBERT	
DESIGN	VENS HUANG		ALBERT	
CHECK				
RESPONSIBLE				
SIZE = 3				
FILE NAME : XXXX-XXXXXX-XX				
P/N	XXXXXXXXXXXX			
VER :				

INVENTEC			
TITLE ROCKY-AMD Project Name			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
SHEET		1	OF 60

	1	2	3	4	5	6	7	8

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01- Project Name
 02- Index
 03- Power Sequence
 04- Power Procedure
 05- Block Diagram
 06- DC & BATTERY CHARGER
 07- BATTERY CONN
 08- +V5A & +V3A & +V2.5S
 09- +V1.1A & +VDDA
 10- +VCC_CORE & +VDDIO_SUS&+V0.75S
 11- +APU_VDD&+VDDNB
 12- +VDDP&+V1.8S
 13- +V5S&+V3S&+V1.5S
 14- +GPU_VDDC&+VPCIE
 15- BLANK
 16- Reserve
 17- BLANK
 18- CPU-1
 19- CPU-2
 20- CPU-3
 21- CPU-4
 22- DDR3 DIMM0
 23- DDR3 DIMM1
 24- FAN & THERMAL IC
 25- FCH-1
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 28- FCH-4
 29- FCH-5
 30- FCH-6

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 35- GPU-5
 36- GPU-6
 37- VRAM-1
 38- VRAM-2
 39- KBC
 40- HDMI
 41- BLANK
 42- CRT
 43- LCM
 44- Keyboard CONN & Indicate LED
 45- Card reader-RTS5219
 46- SATA HDD & SATA ODD CONN
 47- NA
 48- USB CONN
 49- LAN
 50- RJ45 CONN
 51- AUDIO CODEC & SPEAKER CONN
 52- HP JACK & MIC JACK
 53- LED BOARD ON MB
 54- SCREW
 55- WLAN&BT

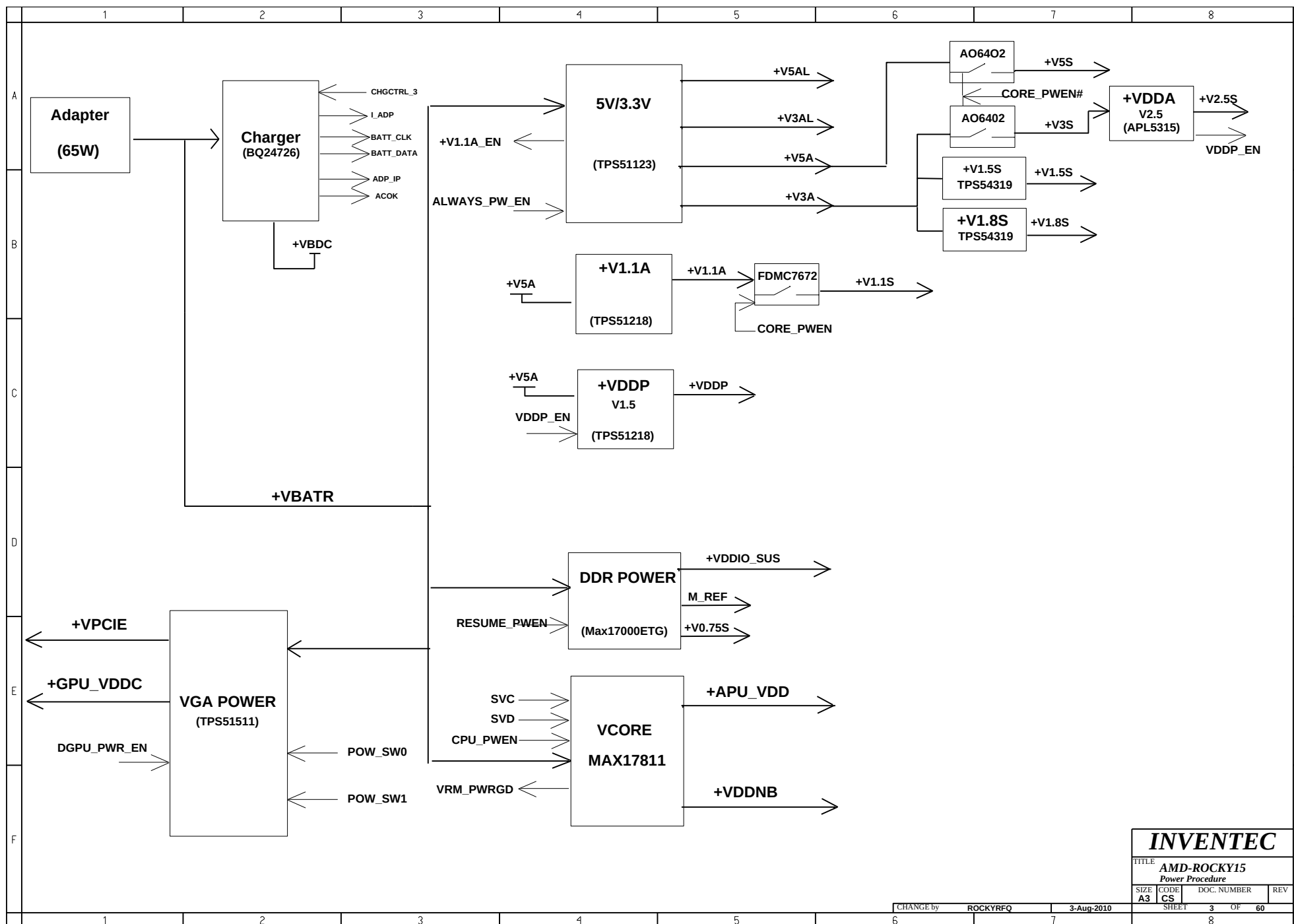
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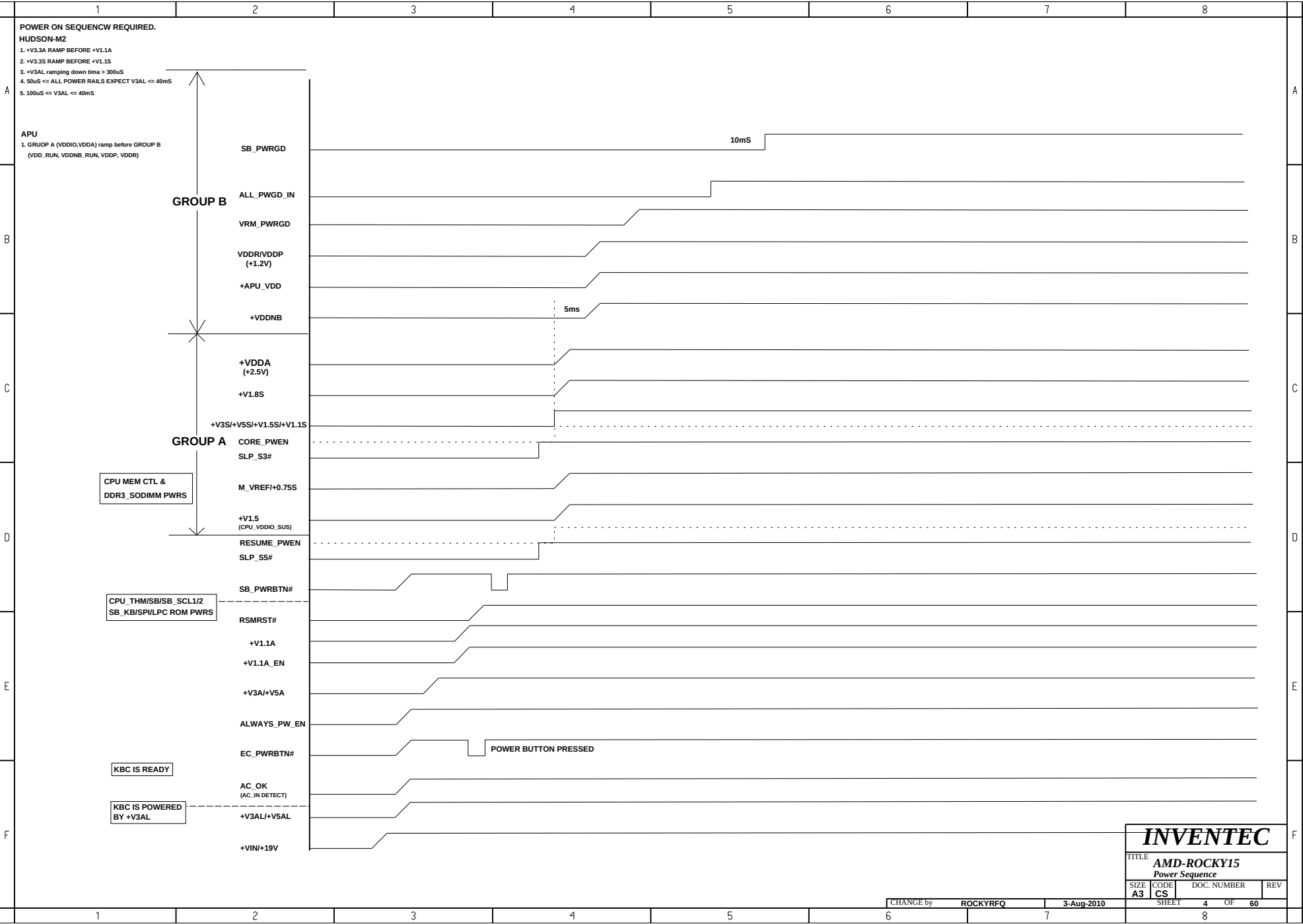
56- PICK BUTTON BOARD & LED BOARD
 57- USB BOARD & BUTTON BOARD
 58- SATA HDD BOARD
 59- TRAVIS
 60- STRAP

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TITLE ROCKY-AMD Index			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
SHEET		2	OF 60

CHANGE by *Ken, Chiang* 6-Aug-2010





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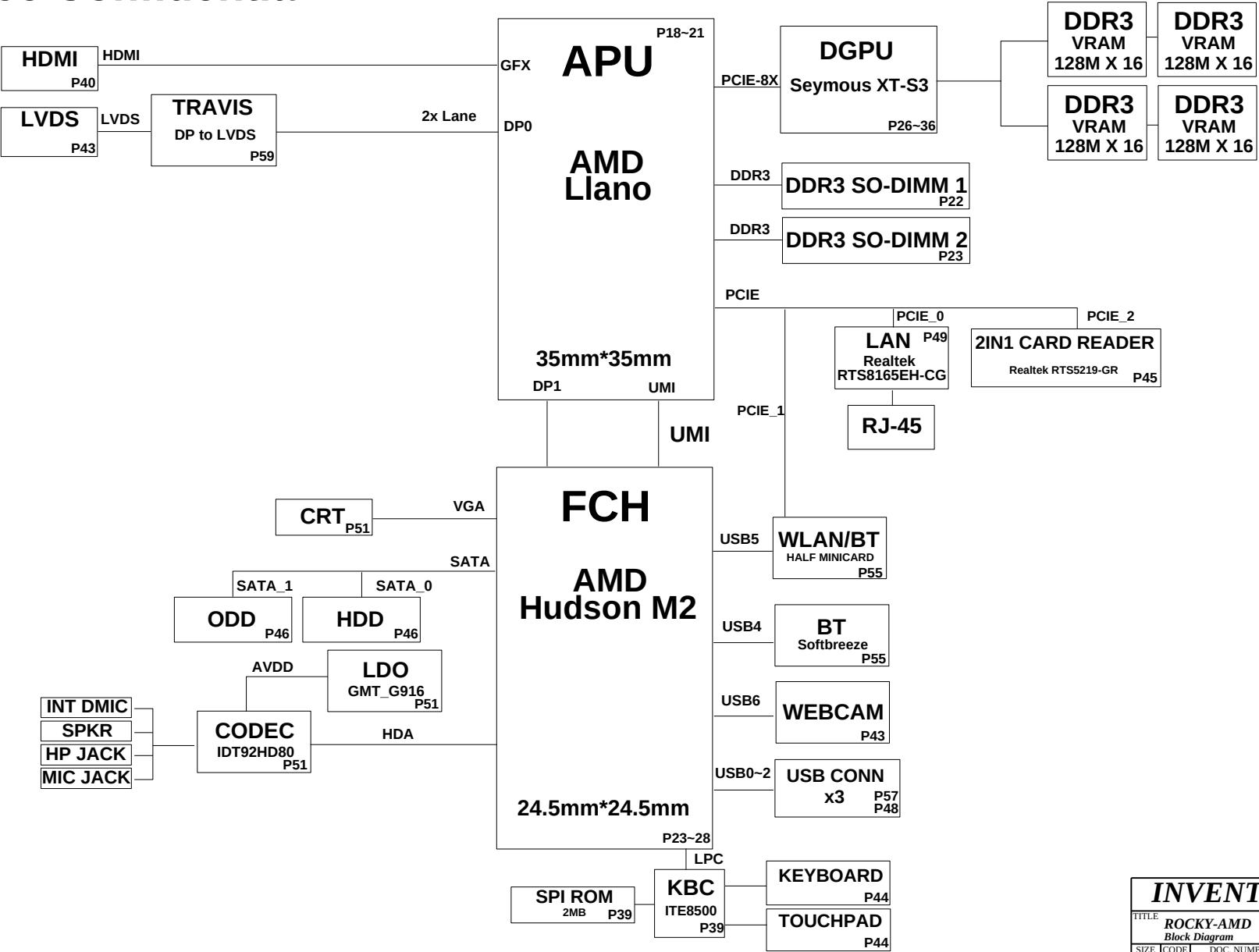
TITLE
AMD-ROCKY15
Power Sequence

SIZE A3	CODE CS	DOC. NUMBER	REV
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SHEET	4	OF	60
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Inventec Confidential

Sabine - DIS

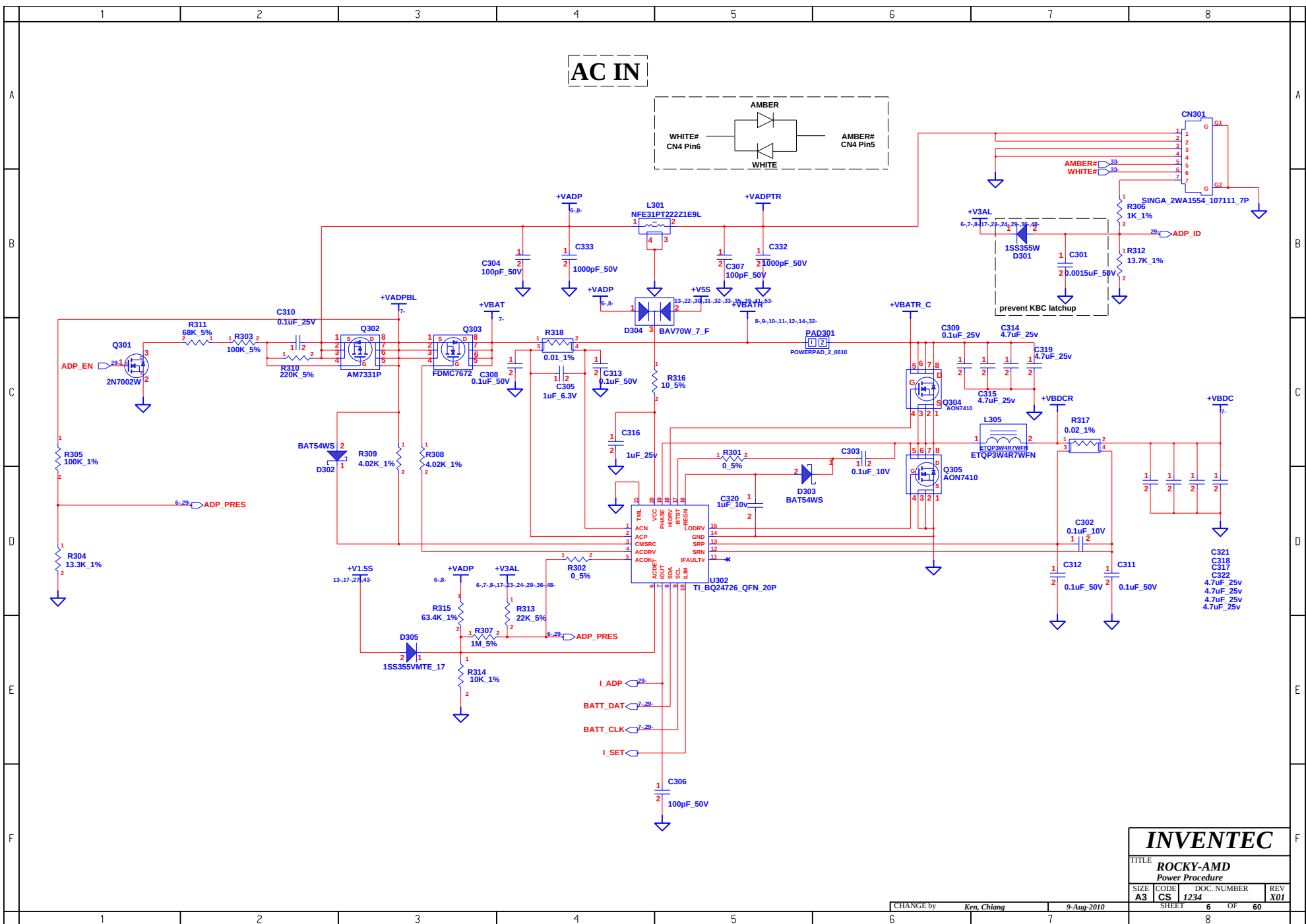


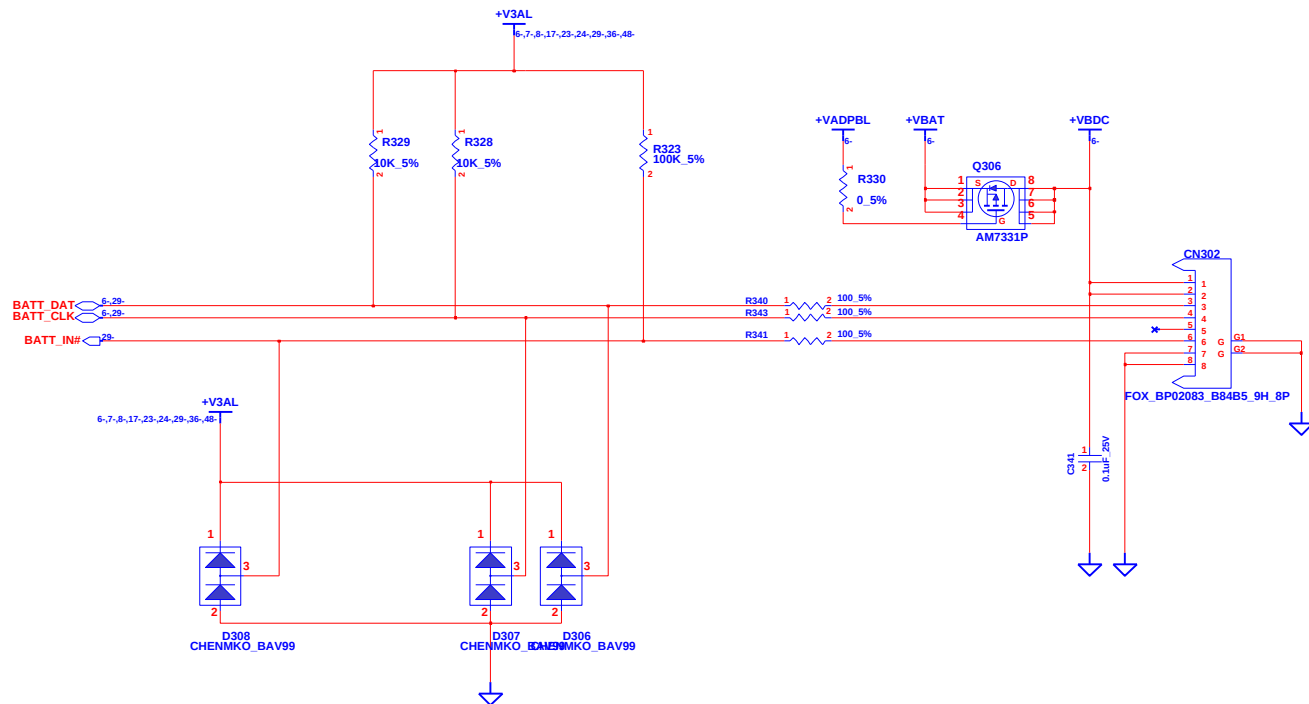
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TITLE			
ROCKY-AMD			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01

CHANGE by Ken, Chiang 3-Aug-2010

SHEET 5 OF 60



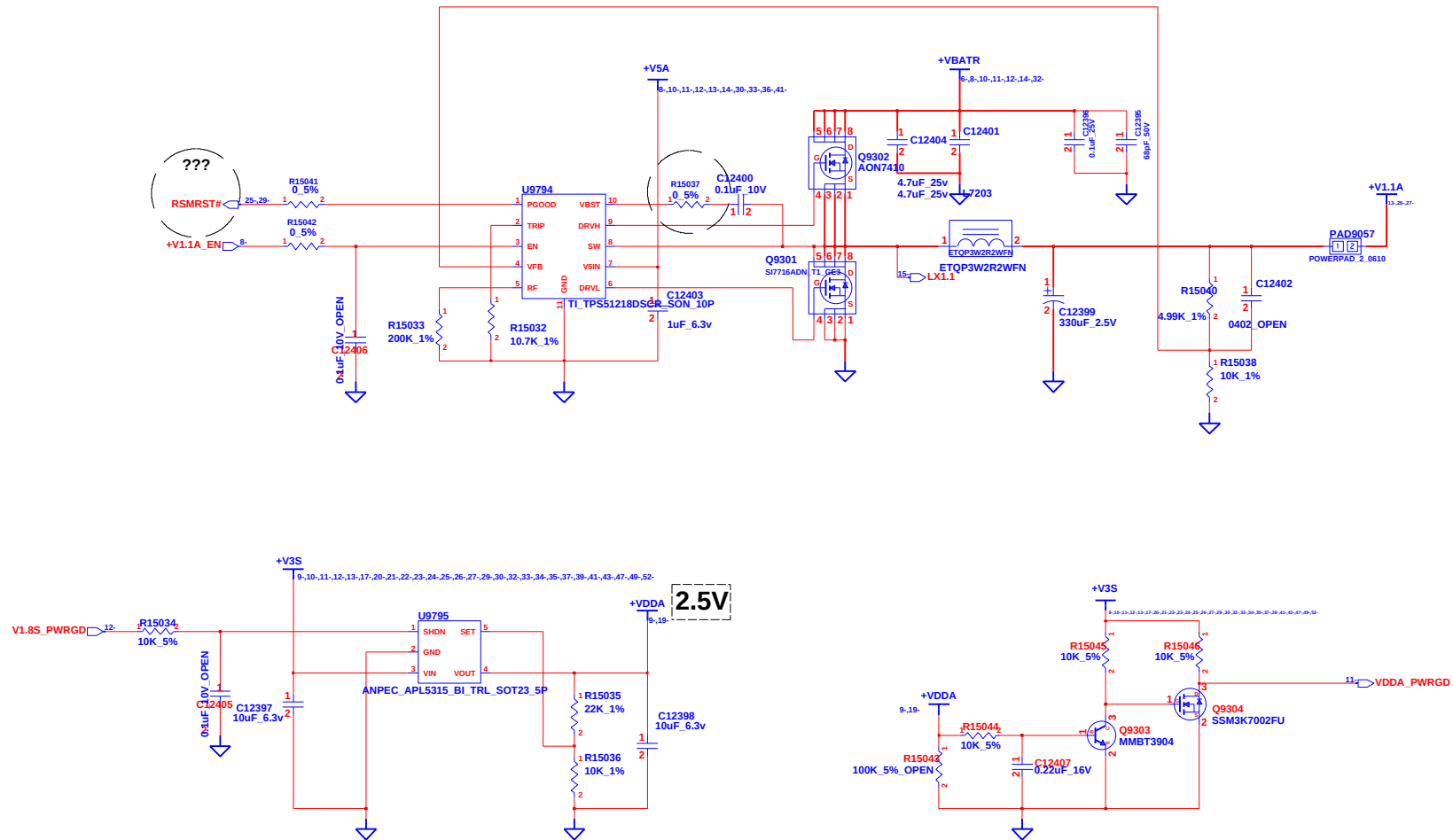


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TITLE ROCKY-AMD Power Sequence			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01

CHANGE by **Ken, Chiang** 9-Aug-2010

SHEET 7 OF 60

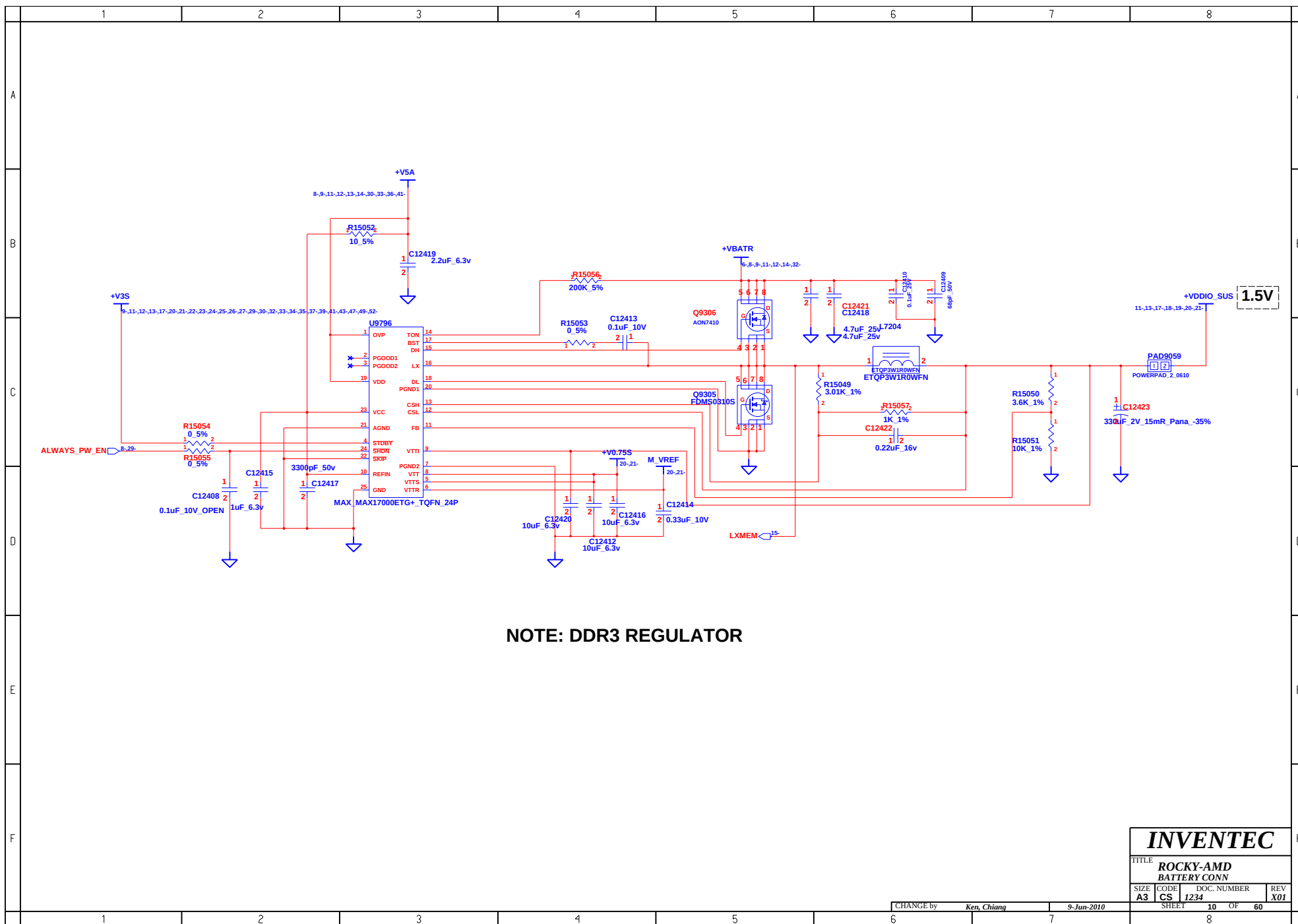


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TITLE			
ROCKY-AMD DC & BATTERY CHARGER			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01

CHANGE by Ken, Chiang 9-Jun-2010

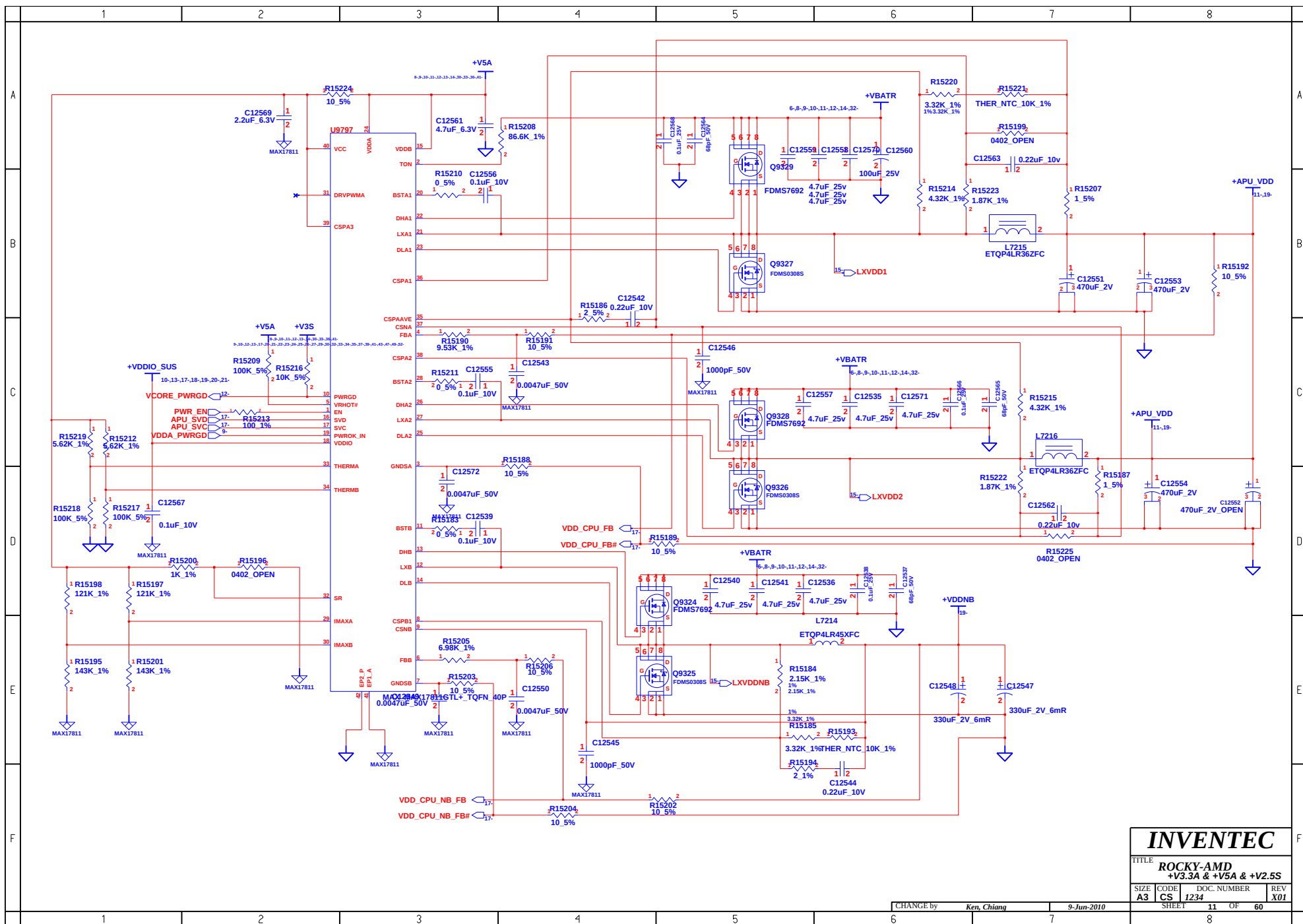
SHEET 9 OF 60

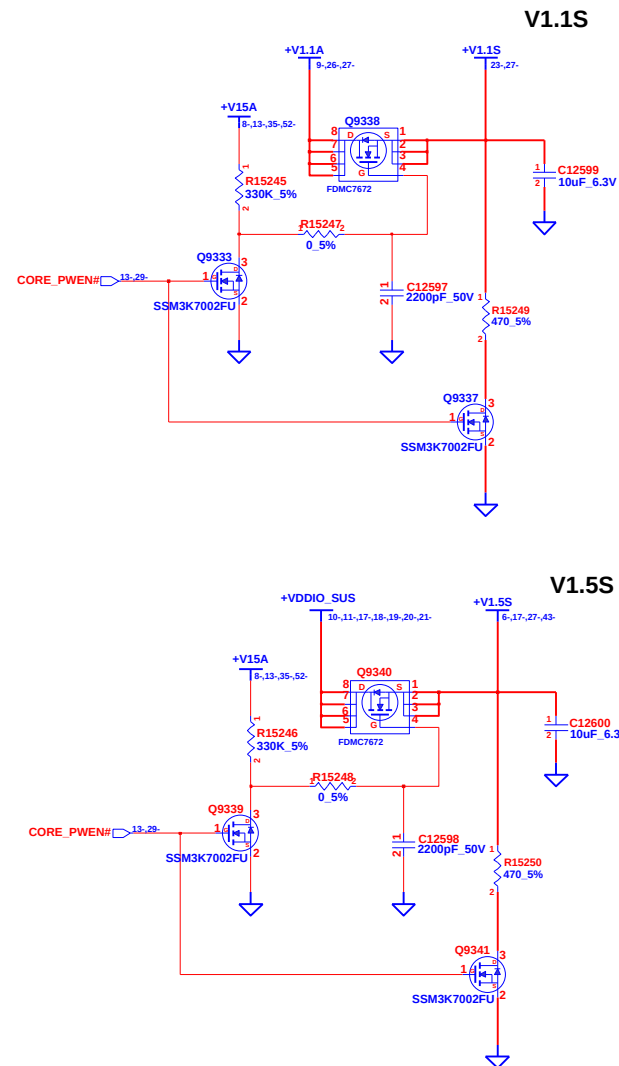
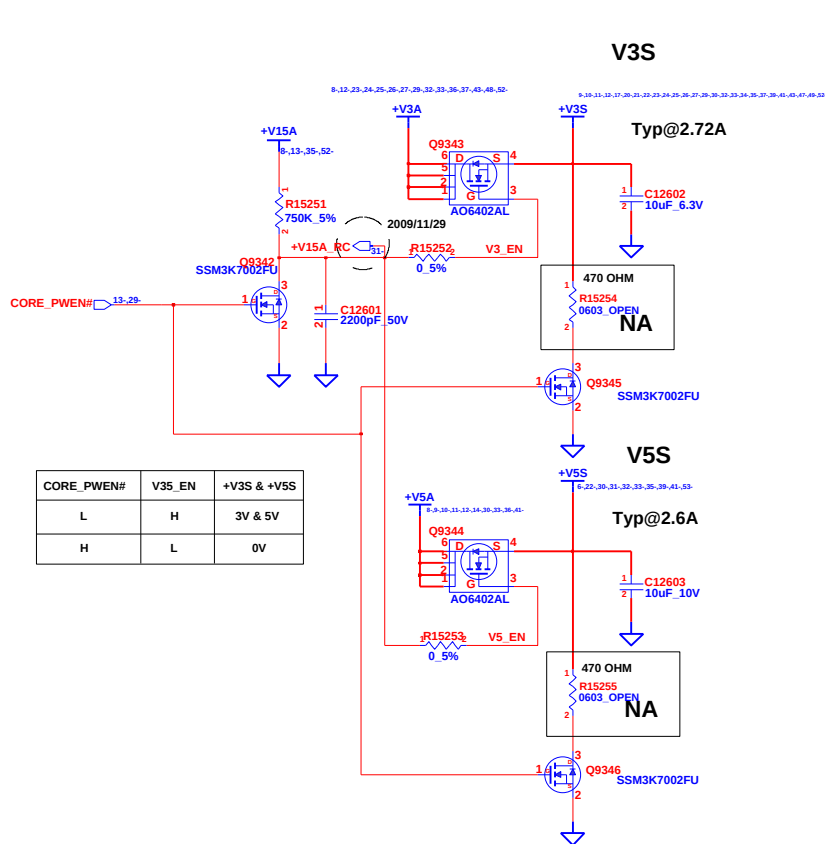


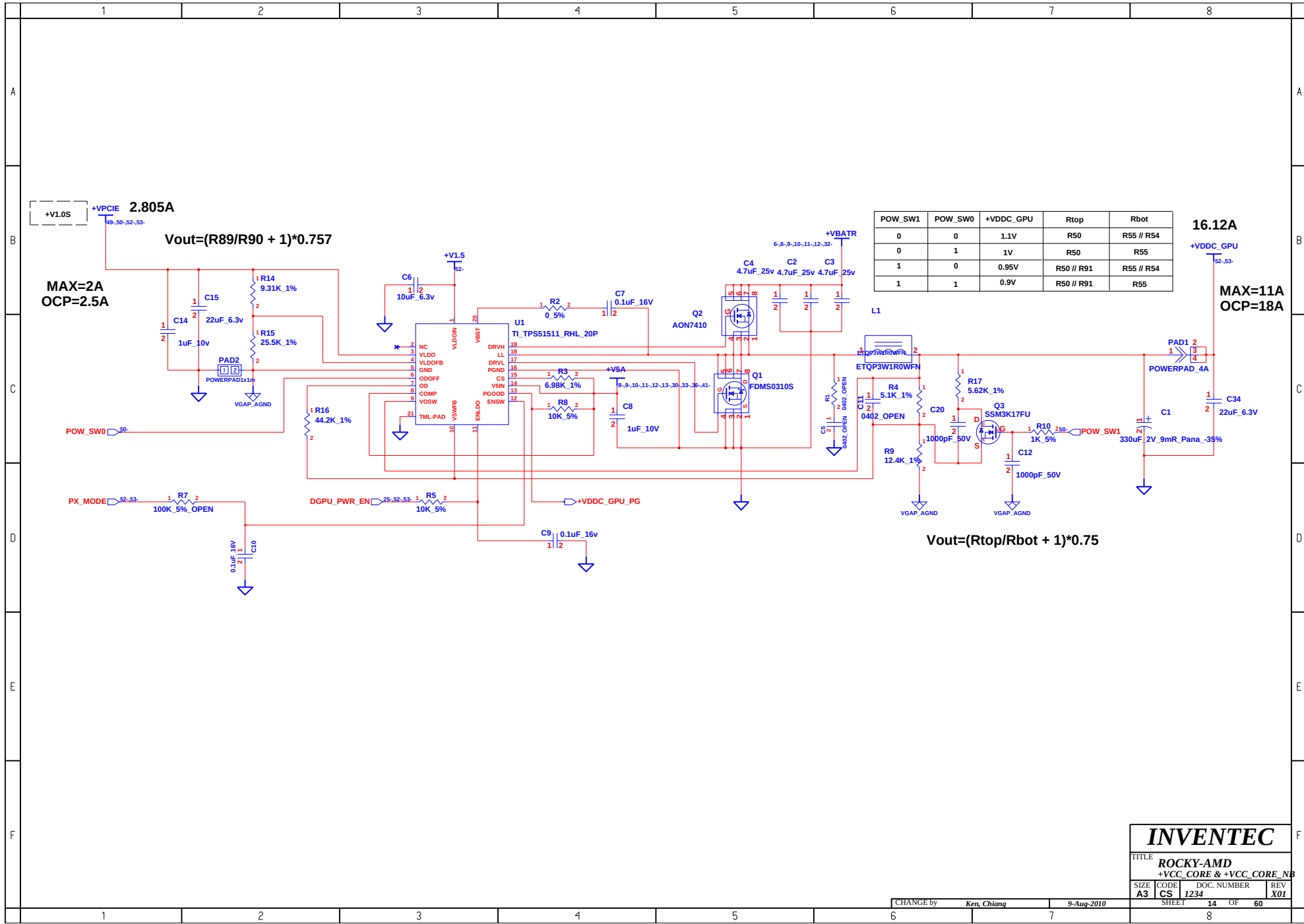
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TITLE			
ROCKY-AMD BATTERY CONN			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01

CHANGE by	Ken, Chiang	9-Jun-2010	SHEET	10	OF	60
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POW_SW1	POW_SW0	+VDDC_GPU	Rtop	Rbot
0	0	1.1V	R50	R55 // R54
0	1	1V	R50	R55
1	0	0.95V	R50 // R91	R55 // R54
1	1	0.9V	R50 // R91	R55

16.12A

+VDDC_GPU

MAX=11A
OCP=18A

$V_{out} = (R_{top}/R_{bot} + 1) \cdot 0.75$

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TITLE ROCKY-AMD +VCC_CORE & +VCC_CORE_NB			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01

CHANGE by *Ken, Chiang* 9-Aug-2010

SHEET 14 OF 60

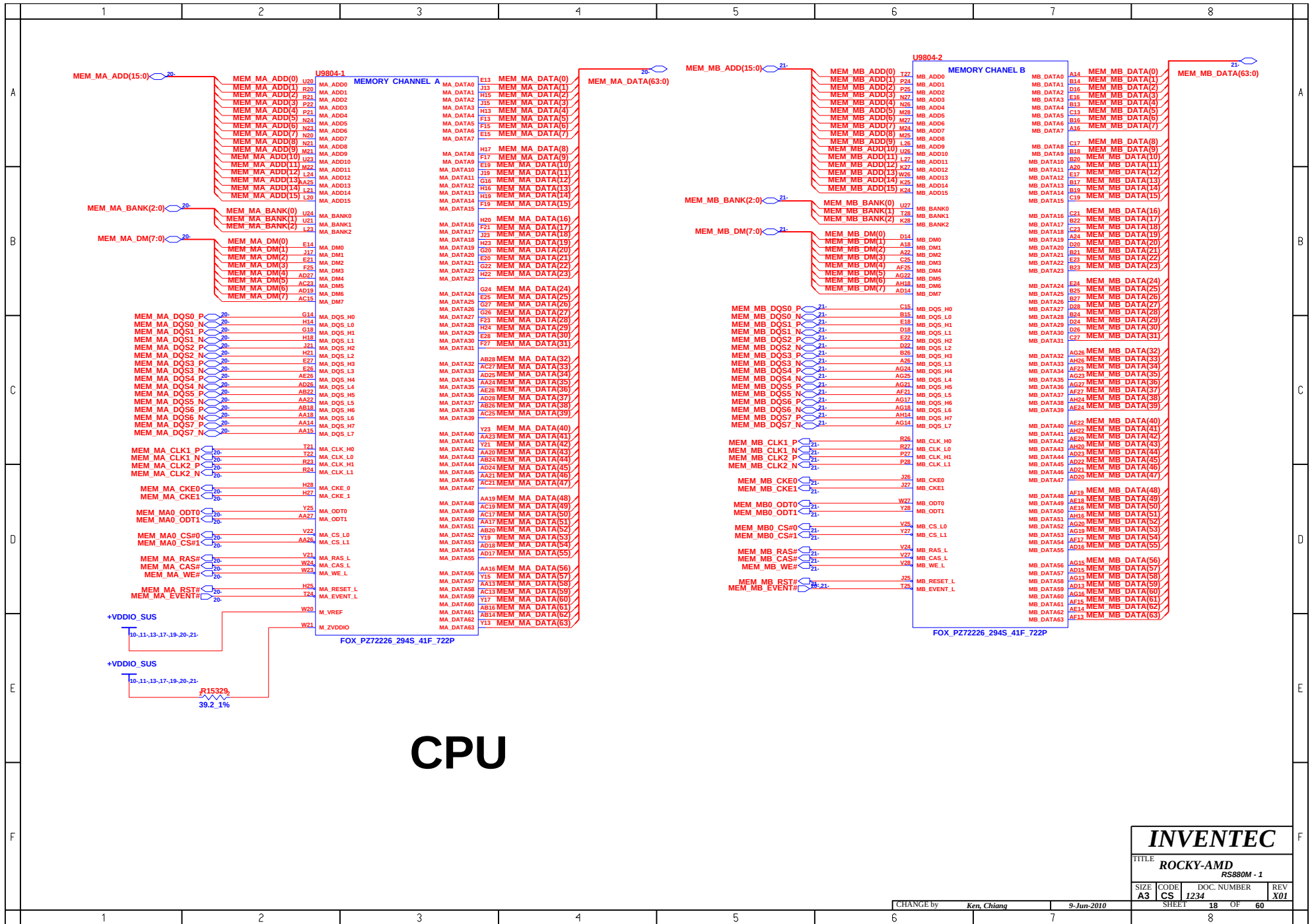
[illegible]

**LAN
WLAN
CardReader**

INVENTEC			
TITLE ROCKY-AMD +V5S & +V3.3S & +V1.5S & +V1.2S			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
SHEET 16		OF 60	

[illegible]

TITLE			
ROCKY-AMD CLK GEN			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01



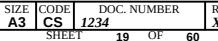
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TITLE
ROCKY-AMD
RS880M - 1

SIZE CODE DOC. NUMBER REV
A3 CS 1234 18 OF 60 X01

CHANGE by Ken, Chiang 9-Jun-2010

SHEET 18 OF 60



SO-DIMM0

Layout NOTE: Place these Caps near SO-DIMM0 power pin

Layout NOTE: Place C4100 on common path for both DIMM's

Place these caps close to VTT1 and VTT2

NOTE:
IF SA0_DIM0=0, SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0xA0
SO-DIMMA TS ADDRESS IS 0x30

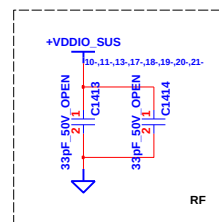
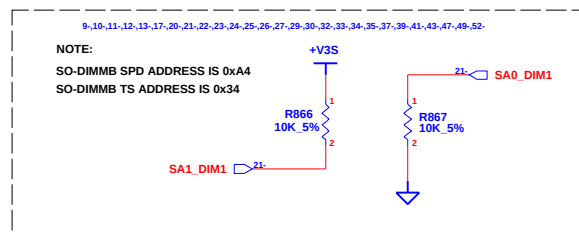
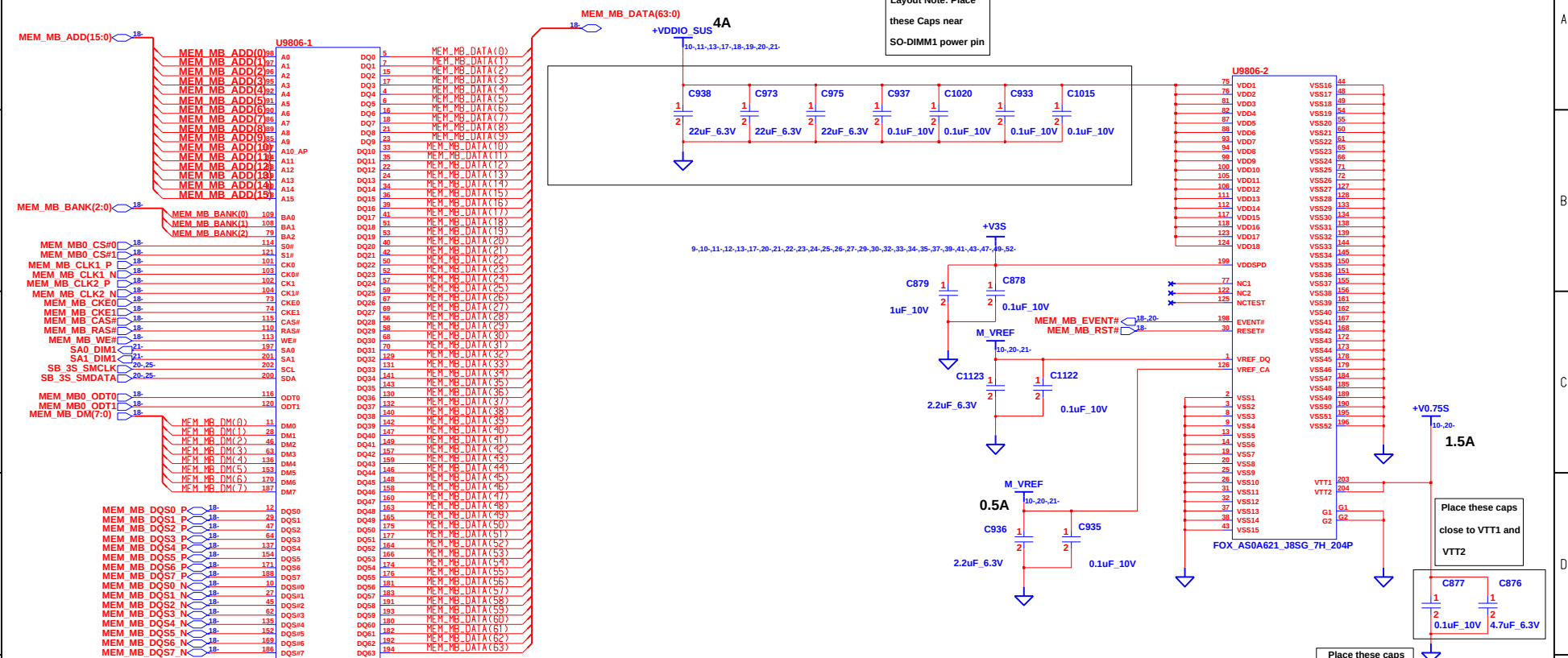
IF SA0_DIM0=1, SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0xA2
SO-DIMMA TS ADDRESS IS 0x32

INVENTEC
TITLE: ROCKY-AMD CPU-1
SIZE: A3 CODE: CS DOC. NUMBER: 1234 REV: X01
SHEET: 20 OF 60

CHANGE by: Ken, Chiang 30-Jul-2010

TITLE			
ROCKY-AMD CPU-1			
SIZE	CODE	DOC. NUMBER	REV.
A3	CS	1234	X0
SHEET		20	OF 60

SO-DIMM1



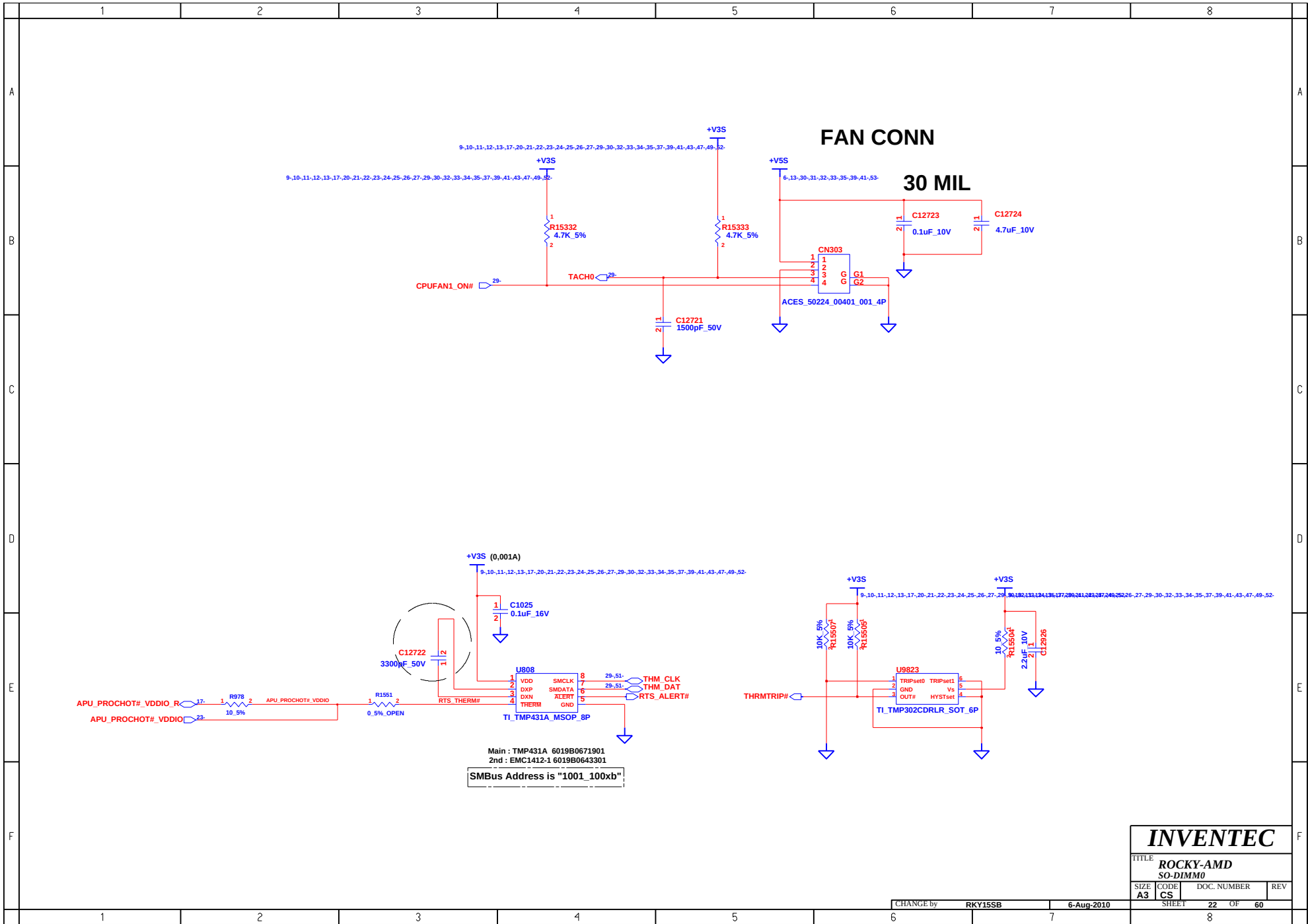
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TITLE	ROCKY-AMD
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SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
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AS	CS	1234	AS1
SHEET		21	OF 60
		Q	

CHANGE by	<i>Ken, Chiang</i>	9-Jun-2010
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FCH

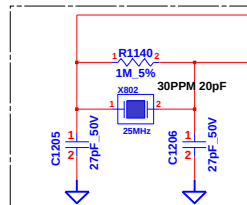
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UMI_FCH_APU_RX0N
UMI_FCH_APU_RX1P
UMI_FCH_APU_RX1N
UMI_FCH_APU_RX2P
UMI_FCH_APU_RX2N
UMI_FCH_APU_RX3P
UMI_FCH_APU_RX3N

PLACE THESE PCIE AC
COUPLING CAPS CLOSE TO U9770-1

EXTERNAL CLOCK GEN??

NB_REF - 100MHZ NB_R_REFCLKP NB_R_REFCLKN
NB_HT - 100MHZ TRAVIS_REFCLKP TRAVIS_REFCLKN
CPU - 200 MHZ CPU_R_CLKP CPU_R_CLKN
NB_GFX - 100MHZ GPU_PCIE_CLK GPU_PCIE_CLK#
LAN - 100MHZ PCIE_LAN_CLKP PCIE_LAN_CLKN
WLAN - 100MHZ PCIE_R_WLAN_CLKP PCIE_R_WLAN_CLKN
CARDREADER - 100MHZ CLK_PCIE_CARD CLK_PCIE_CARD#

LPC_AD(0) 23-29-43 R1138 8.2K 5% OPEN
LPC_AD(1) 23-29-43 R1162 8.2K 5%
LPC_AD(2) 23-29-43 R1137 8.2K 5%
LPC_AD(3) 23-29-43 R1139 8.2K 5%



HUDSON-2

A_RX0P_C
A_RX0N_C
A_RX1P_C
A_RX1N_C
A_RX2P_C
A_RX2N_C
A_RX3P_C
A_RX3N_C

GPP_TX0P
GPP_TX0N
GPP_TX1P
GPP_TX1N
GPP_TX2P
GPP_TX2N
GPP_TX3P
GPP_TX3N

CLK_CALRN

PCIE_RCLKP
PCIE_RCLKN

DISP_CLKP
DISP_CLKN

APU_CLKP
APU_CLKN

SLT_GFX_CLKP
SLT_GFX_CLKN

GPP_CLK0P
GPP_CLK0N

GPP_CLK1P
GPP_CLK1N

GPP_CLK2P
GPP_CLK2N

GPP_CLK3P
GPP_CLK3N

GPP_CLK4P
GPP_CLK4N

GPP_CLK5P
GPP_CLK5N

GPP_CLK6P
GPP_CLK6N

GPP_CLK7P
GPP_CLK7N

GPP_CLK8P
GPP_CLK8N

14M_25M_28M_OSC

25M_X1

25M_X2

AMD 218_0755002_FCBGA_656P

Connect to c602. pdf p51 mictor

PCICLK0
PCICLK1-GP037
PCICLK3-GP038
PCICLK4-14M_OSC-GP039

AD0-GPIO0
AD1-GPIO1
AD2-GPIO2
AD3-GPIO3
AD4-GPIO4
AD5-GPIO5
AD6-GPIO6
AD7-GPIO7
AD8-GPIO8
AD9-GPIO9
AD10-GPIO10
AD11-GPIO11
AD12-GPIO12
AD13-GPIO13
AD14-GPIO14
AD15-GPIO15
AD16-GPIO16
AD17-GPIO17
AD18-GPIO18
AD19-GPIO19
AD20-GPIO20
AD21-GPIO21
AD22-GPIO22
AD23-GPIO23
AD24-GPIO24
AD25-GPIO25
AD26-GPIO26
AD27-GPIO27
AD28-GPIO28
AD29-GPIO29
AD30-GPIO30
AD31-GPIO31

PCIE_SERR#

PE_GPIO0
PE_GPIO1

ALLOW_STOP
APU_PROCHOT#_VDDIO
APU_PWRGD

CPU_LDT_RST#

RTC_CLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

Connect to kbc pciclk

PCI_CLK1
PCI_CLK3
PCI_CLK4

PCI_RST#

APU_PCIE_RST#

PCI_RST#_TRAVIS

GPU_PCIE_RST#

PE_GPIO0

CPU_LDT_RST#

RTC_CLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

Connect to c602. pdf p51 mictor

PCICLK0
PCICLK1-GP037
PCICLK3-GP038
PCICLK4-14M_OSC-GP039

AD0-GPIO0
AD1-GPIO1
AD2-GPIO2
AD3-GPIO3
AD4-GPIO4
AD5-GPIO5
AD6-GPIO6
AD7-GPIO7
AD8-GPIO8
AD9-GPIO9
AD10-GPIO10
AD11-GPIO11
AD12-GPIO12
AD13-GPIO13
AD14-GPIO14
AD15-GPIO15
AD16-GPIO16
AD17-GPIO17
AD18-GPIO18
AD19-GPIO19
AD20-GPIO20
AD21-GPIO21
AD22-GPIO22
AD23-GPIO23
AD24-GPIO24
AD25-GPIO25
AD26-GPIO26
AD27-GPIO27
AD28-GPIO28
AD29-GPIO29
AD30-GPIO30
AD31-GPIO31

PCIE_SERR#

PE_GPIO0
PE_GPIO1

ALLOW_STOP
APU_PROCHOT#_VDDIO
APU_PWRGD

CPU_LDT_RST#

RTC_CLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

Connect to kbc pciclk

PCI_CLK1
PCI_CLK3
PCI_CLK4

PCI_RST#

APU_PCIE_RST#

PCI_RST#_TRAVIS

GPU_PCIE_RST#

PE_GPIO0

CPU_LDT_RST#

RTC_CLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

Connect to c602. pdf p51 mictor

PCICLK0
PCICLK1-GP037
PCICLK3-GP038
PCICLK4-14M_OSC-GP039

AD0-GPIO0
AD1-GPIO1
AD2-GPIO2
AD3-GPIO3
AD4-GPIO4
AD5-GPIO5
AD6-GPIO6
AD7-GPIO7
AD8-GPIO8
AD9-GPIO9
AD10-GPIO10
AD11-GPIO11
AD12-GPIO12
AD13-GPIO13
AD14-GPIO14
AD15-GPIO15
AD16-GPIO16
AD17-GPIO17
AD18-GPIO18
AD19-GPIO19
AD20-GPIO20
AD21-GPIO21
AD22-GPIO22
AD23-GPIO23
AD24-GPIO24
AD25-GPIO25
AD26-GPIO26
AD27-GPIO27
AD28-GPIO28
AD29-GPIO29
AD30-GPIO30
AD31-GPIO31

PCIE_SERR#

PE_GPIO0
PE_GPIO1

ALLOW_STOP
APU_PROCHOT#_VDDIO
APU_PWRGD

CPU_LDT_RST#

RTC_CLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

Connect to kbc pciclk

PCI_CLK1
PCI_CLK3
PCI_CLK4

PCI_RST#

APU_PCIE_RST#

PCI_RST#_TRAVIS

GPU_PCIE_RST#

PE_GPIO0

CPU_LDT_RST#

RTC_CLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

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VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

Connect to c602. pdf p51 mictor

PCICLK0
PCICLK1-GP037
PCICLK3-GP038
PCICLK4-14M_OSC-GP039

AD0-GPIO0
AD1-GPIO1
AD2-GPIO2
AD3-GPIO3
AD4-GPIO4
AD5-GPIO5
AD6-GPIO6
AD7-GPIO7
AD8-GPIO8
AD9-GPIO9
AD10-GPIO10
AD11-GPIO11
AD12-GPIO12
AD13-GPIO13
AD14-GPIO14
AD15-GPIO15
AD16-GPIO16
AD17-GPIO17
AD18-GPIO18
AD19-GPIO19
AD20-GPIO20
AD21-GPIO21
AD22-GPIO22
AD23-GPIO23
AD24-GPIO24
AD25-GPIO25
AD26-GPIO26
AD27-GPIO27
AD28-GPIO28
AD29-GPIO29
AD30-GPIO30
AD31-GPIO31

PCIE_SERR#

PE_GPIO0
PE_GPIO1

ALLOW_STOP
APU_PROCHOT#_VDDIO
APU_PWRGD

CPU_LDT_RST#

RTC_CLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

Connect to kbc pciclk

PCI_CLK1
PCI_CLK3
PCI_CLK4

PCI_RST#

APU_PCIE_RST#

PCI_RST#_TRAVIS

GPU_PCIE_RST#

PE_GPIO0

CPU_LDT_RST#

RTC_CLK

INTRUDER_ALERT#

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VDDBT_RTC_C

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RTCCLK

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VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

Connect to c602. pdf p51 mictor

PCICLK0
PCICLK1-GP037
PCICLK3-GP038
PCICLK4-14M_OSC-GP039

AD0-GPIO0
AD1-GPIO1
AD2-GPIO2
AD3-GPIO3
AD4-GPIO4
AD5-GPIO5
AD6-GPIO6
AD7-GPIO7
AD8-GPIO8
AD9-GPIO9
AD10-GPIO10
AD11-GPIO11
AD12-GPIO12
AD13-GPIO13
AD14-GPIO14
AD15-GPIO15
AD16-GPIO16
AD17-GPIO17
AD18-GPIO18
AD19-GPIO19
AD20-GPIO20
AD21-GPIO21
AD22-GPIO22
AD23-GPIO23
AD24-GPIO24
AD25-GPIO25
AD26-GPIO26
AD27-GPIO27
AD28-GPIO28
AD29-GPIO29
AD30-GPIO30
AD31-GPIO31

PCIE_SERR#

PE_GPIO0
PE_GPIO1

ALLOW_STOP
APU_PROCHOT#_VDDIO
APU_PWRGD

CPU_LDT_RST#

RTC_CLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

SS_CORE_EN

RTCCLK

INTRUDER_ALERT#

VDDBT_RTC_C

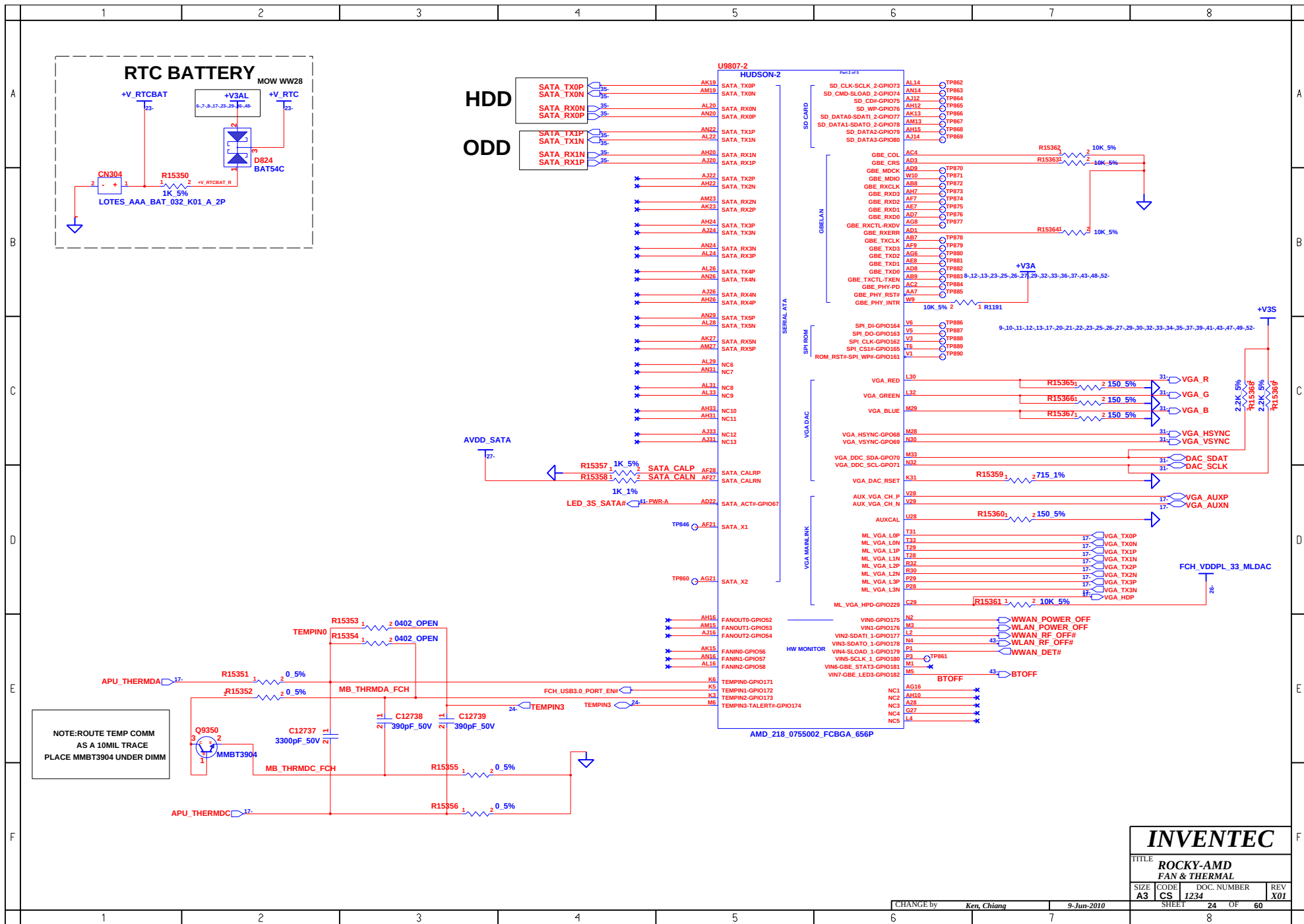
SS_CORE_EN

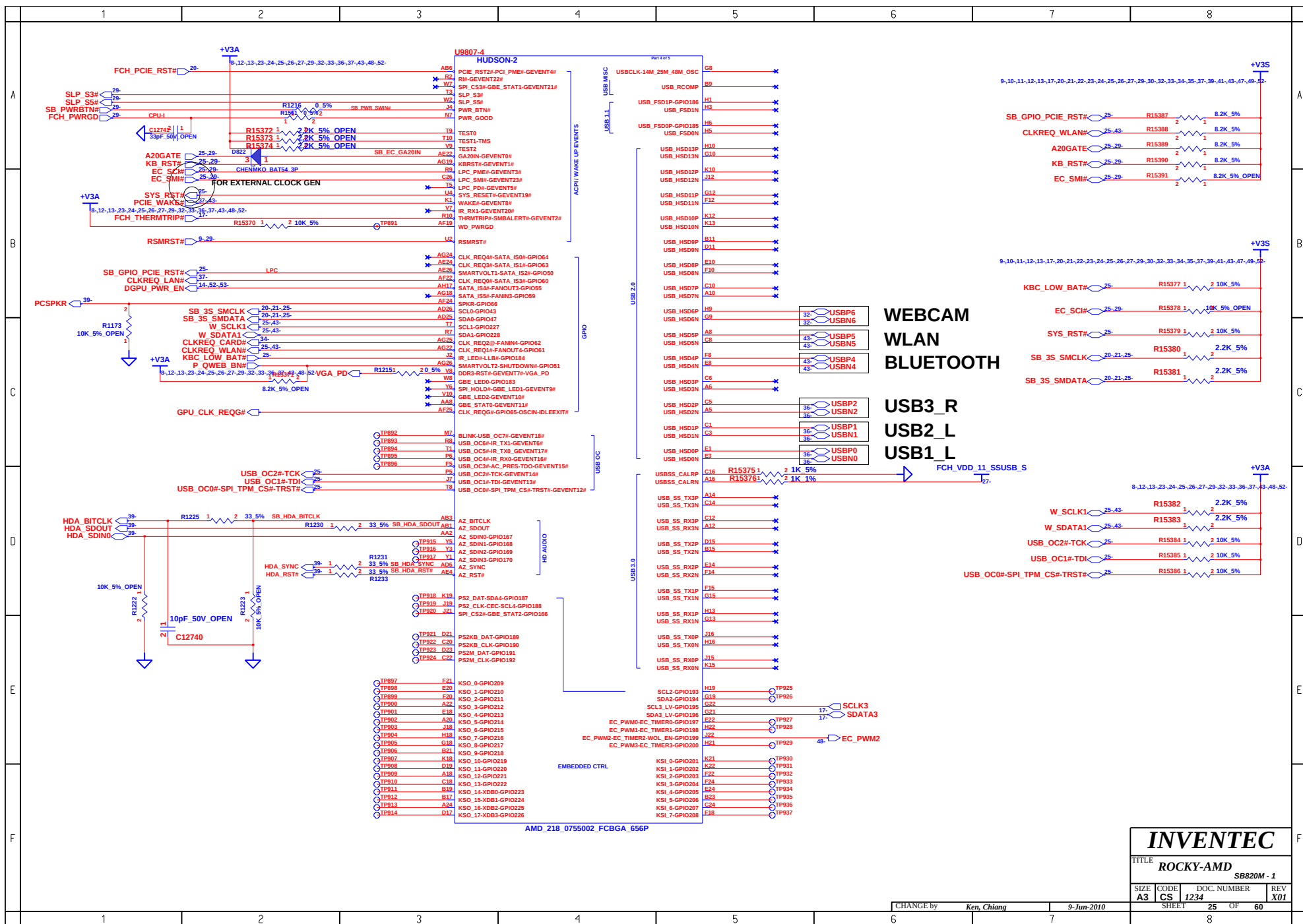
RTCCLK

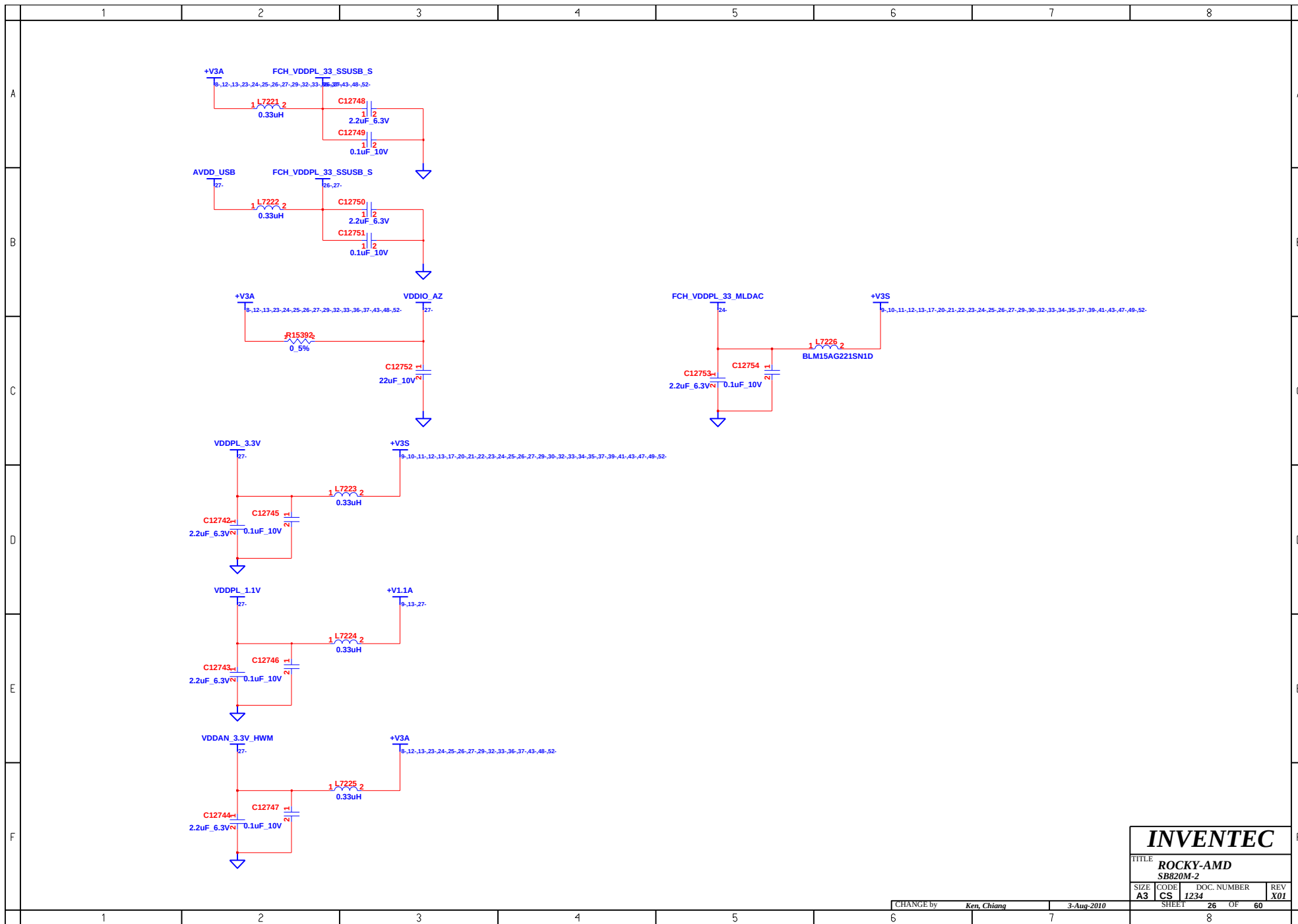
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VDDBT_RTC_C

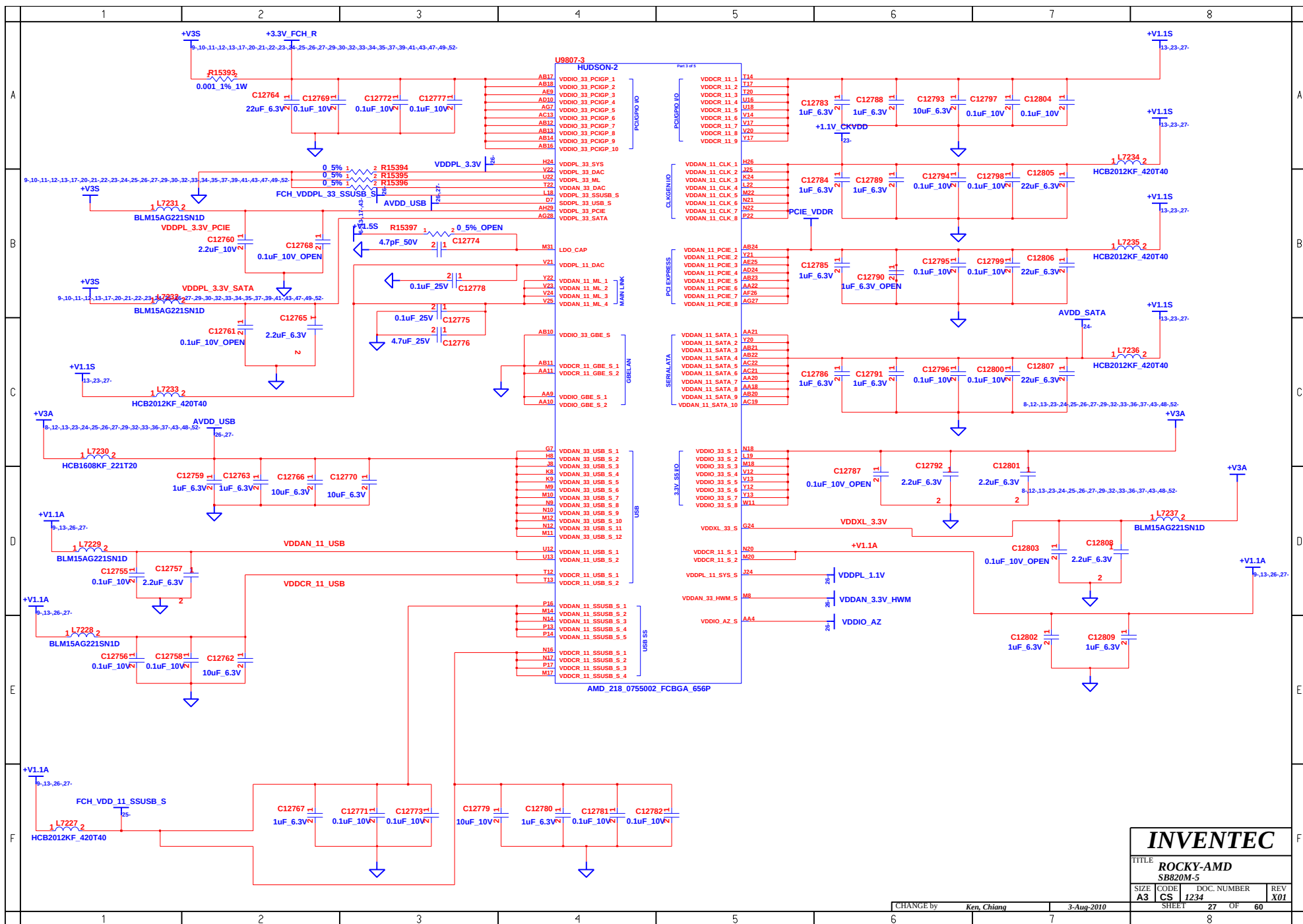
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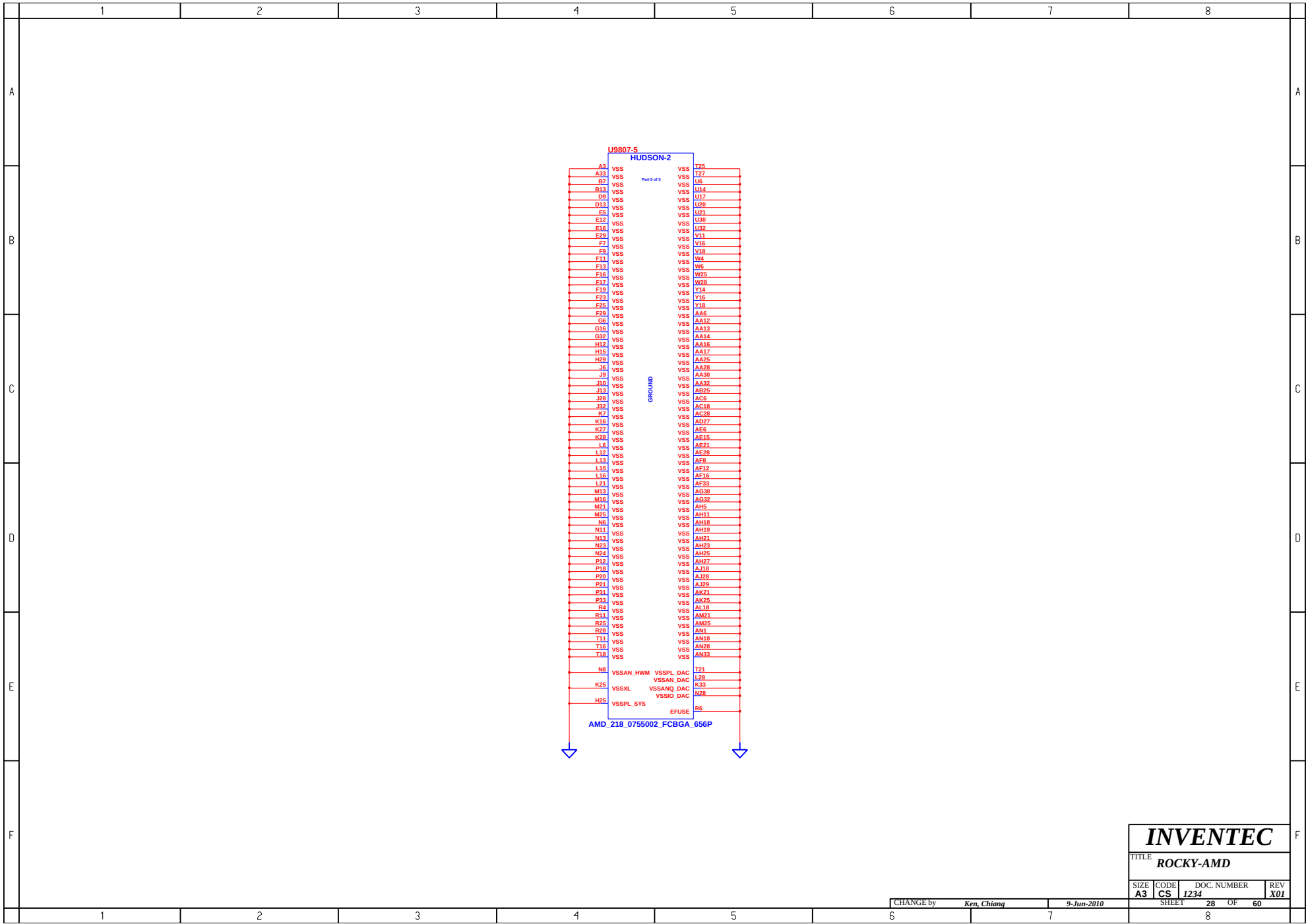






INVENTEC			
TITLE ROCKY-AMD SB820M-2			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
CHANGE by Ken, Chiang		3-Aug-2010	
SHEET		26	OF 60
		8	





INVENTEC

TITLE
ROCKY-AMD

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01

CHANGE by Ken, Chiang 9-Jun-2010

SHEET 28 OF 60

U805_ 6019B0724201

U805
ITE_IT8502E-KX_L_LQFP_128P

BOARD ID

INVENTEC

TITLE	ROCKY-AMD SB820M - 3
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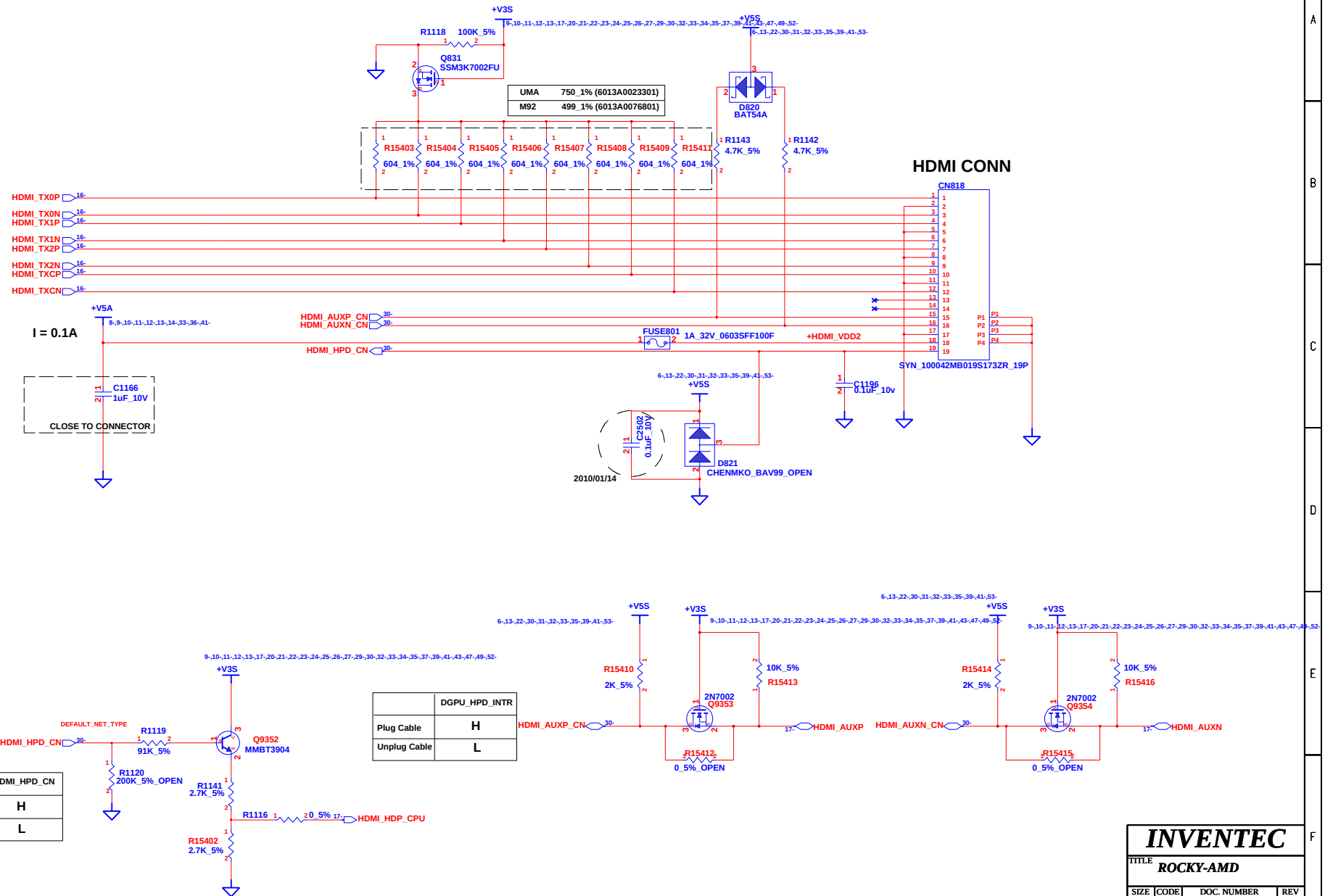
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
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CHANGE by	<i>Ken, Chiang</i>
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	9-Jun-2010
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29 OF 60

HDMI



INVENTEC

TITLE
ROCKY-AMD

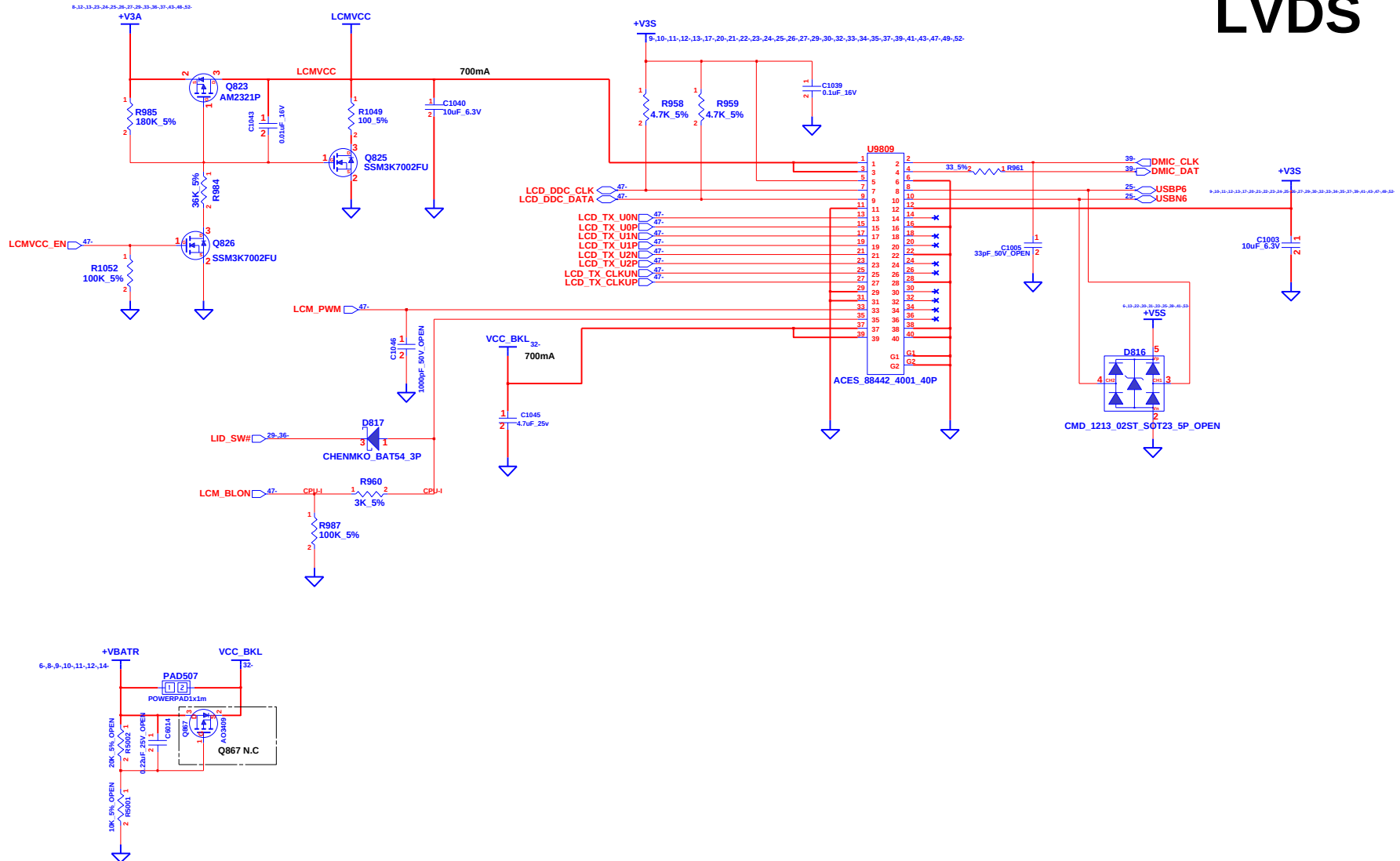
SIZE CODE DOC. NUMBER REV
A3 CS 1234 X01

CHANGE by **Ken Chiang**

9-Jun-2010

SHEET 30 OF 60

LVDS



INVENTEC

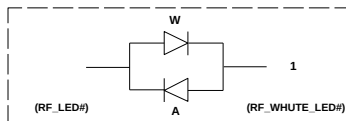
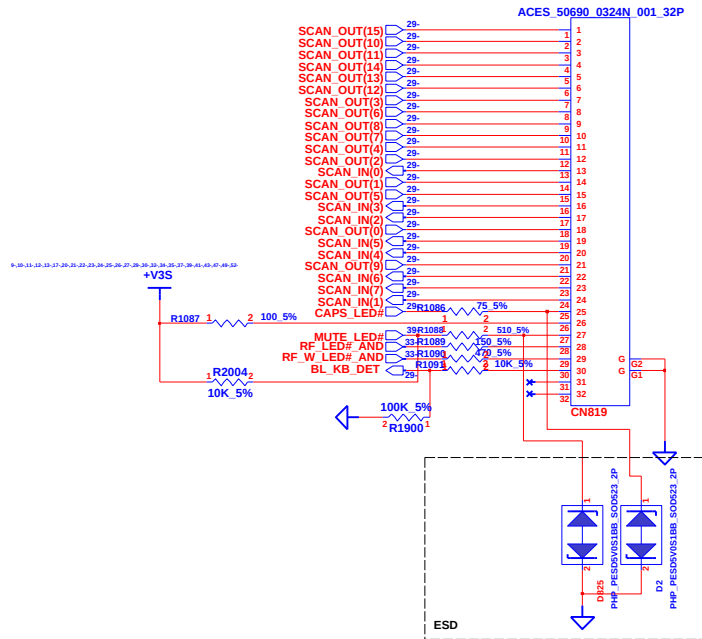
TITLE
ROCKY-AMD

SIZE CODE DOC. NUMBER REV
A3 CS

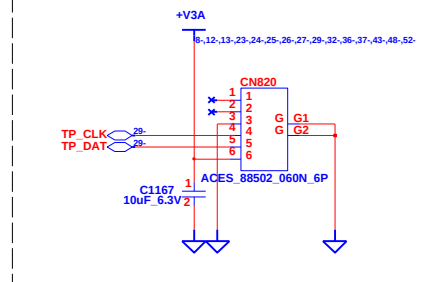
CHANGE by **RKY15SB** 9-Aug-2010

SHEET 32 OF 60

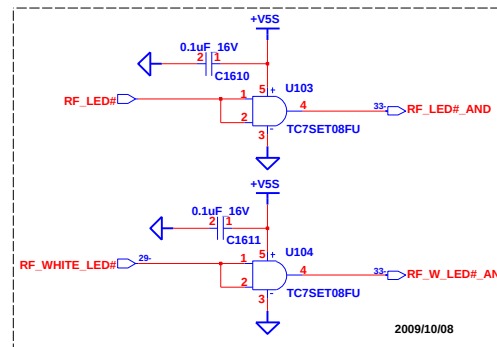
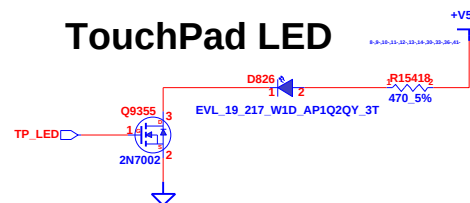
KeyBoard CONN (30 pin)



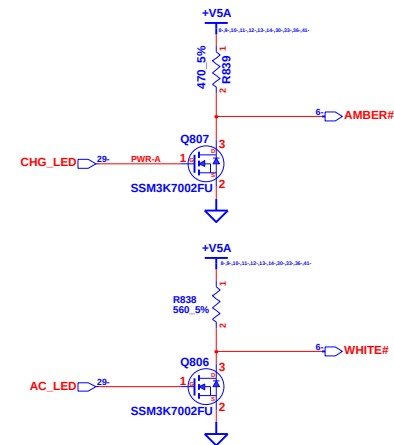
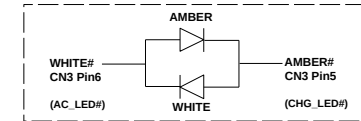
TouchPad on MB



TouchPad LED



DC-JACK LED



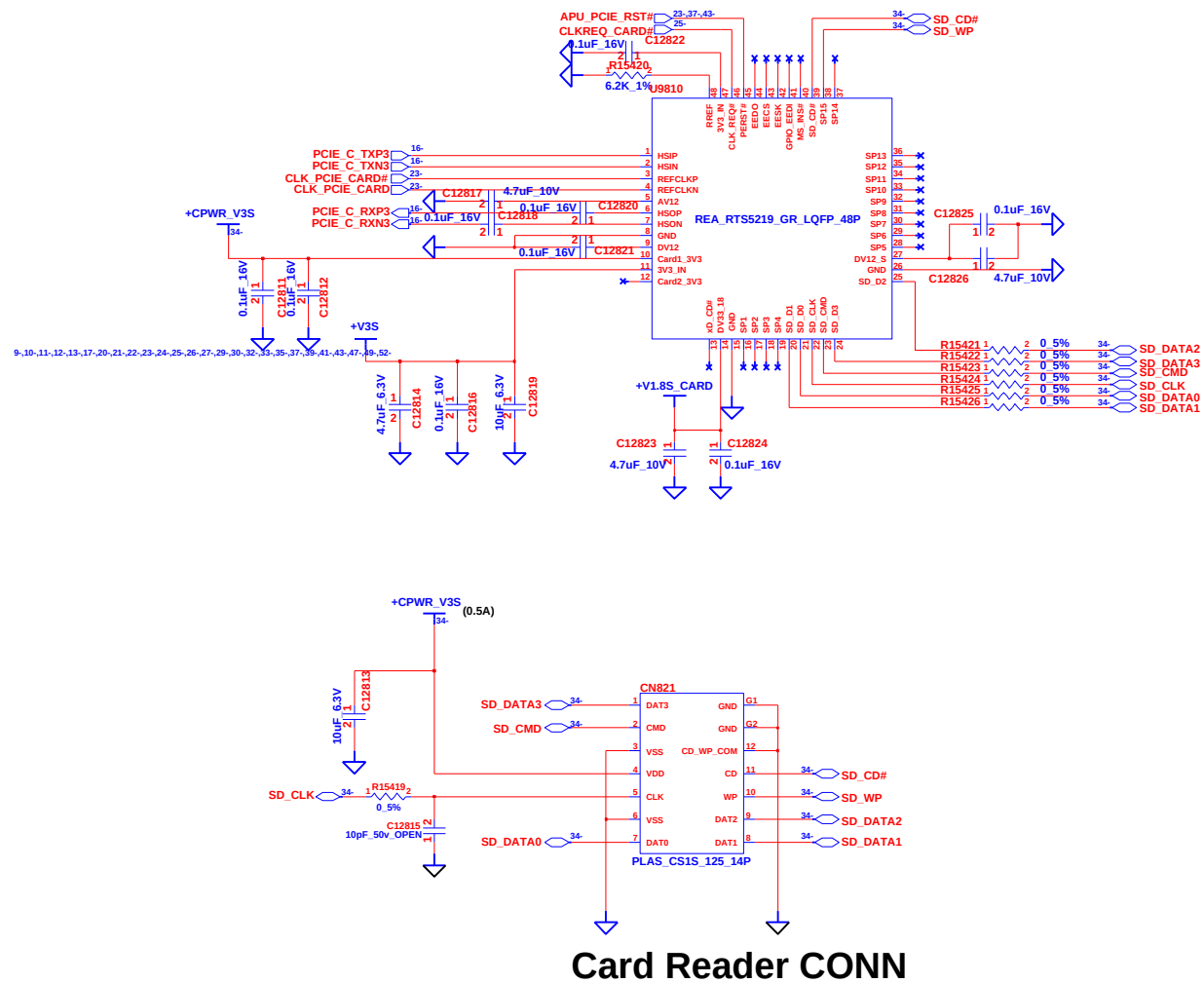
INVENTEC

TITLE
ROCKY-AMD

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01

CHANGE by *Ken, Chiang* 5-Aug-2010

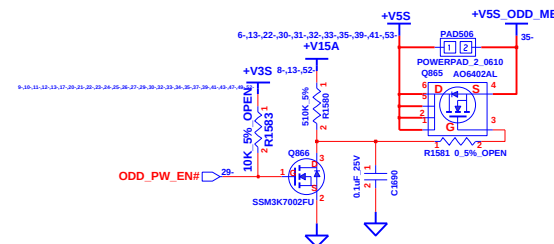
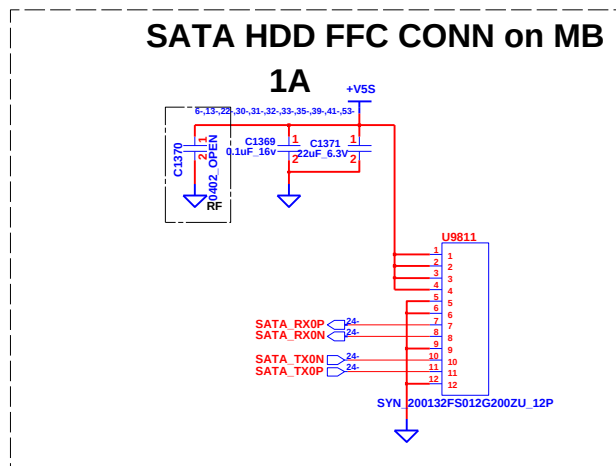
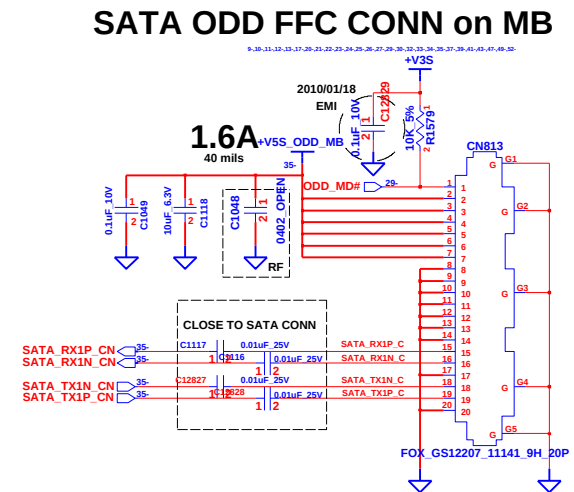
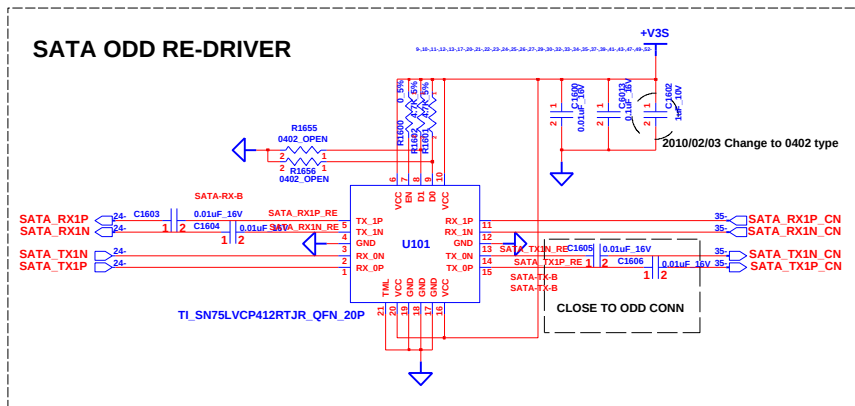
SHEET 33 OF 60



INVENTEC			
TITLE			
ROCKY-AMD			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01

CHANGE by Ken, Chiang 5-Aug-2010

SHEET 34 OF 60



INVENTEC

TITLE
ROCKY-AMD

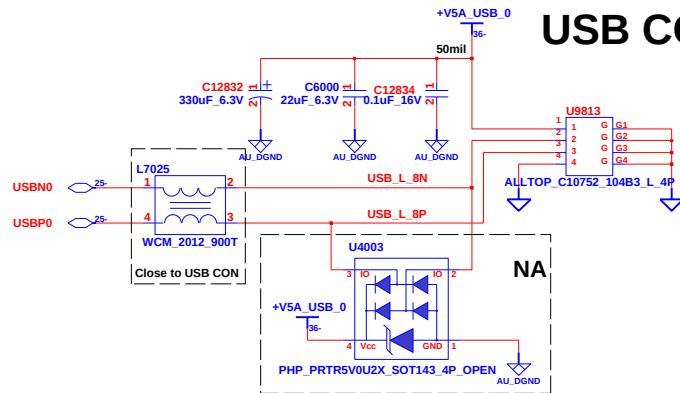
SIZE CODE DOC. NUMBER REV
A3 CS 1234

CHANGE by **Ken Chiang** 5-Aug-2010

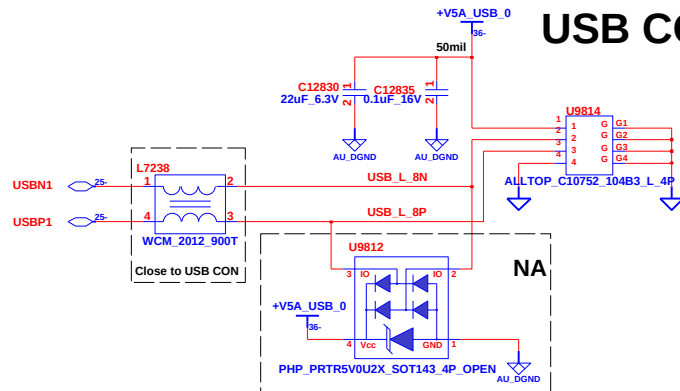
SHEET 35 OF 60

USB

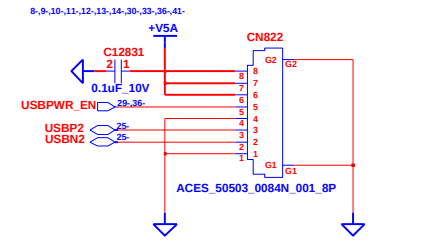
USB CONN01



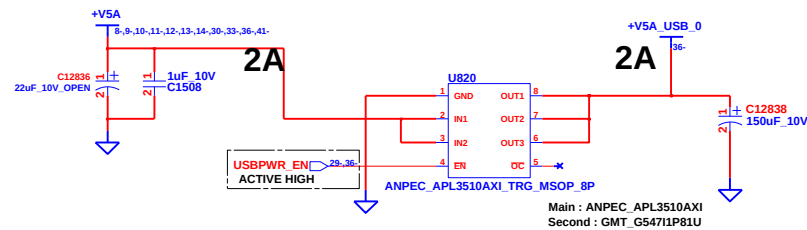
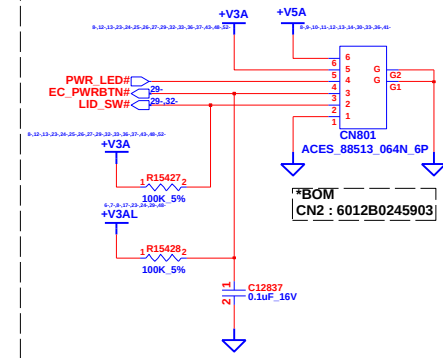
USB CONN02



USB BOARD Cable on MB



PBN Cable CN on MB



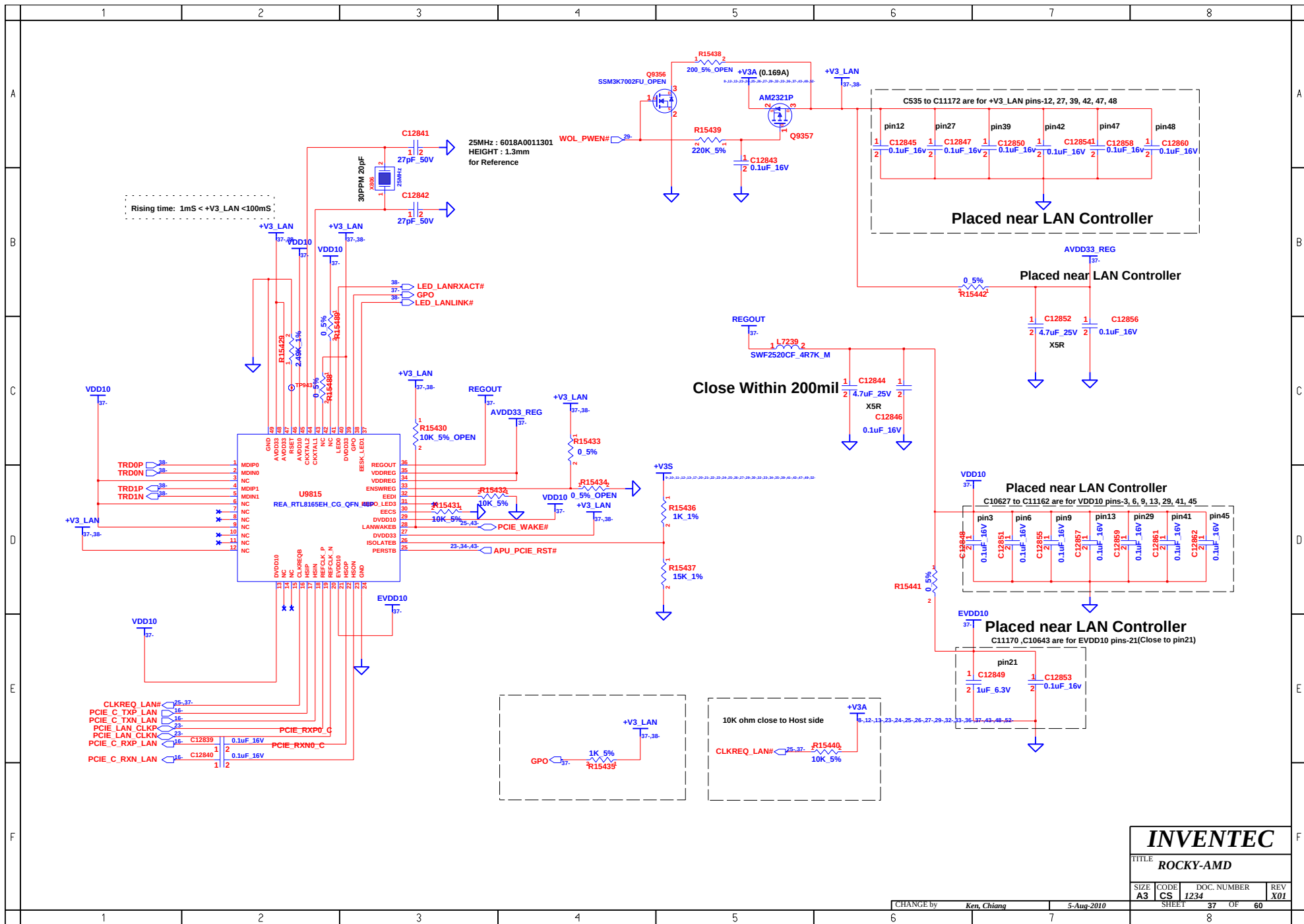
INVENTEC

TITLE
ROCKY-AMD

SIZE CODE DOC. NUMBER REV
A3 CS 1234 36 OF 60 X01

CHANGE by Ken Chiang 5-Aug-2010

8



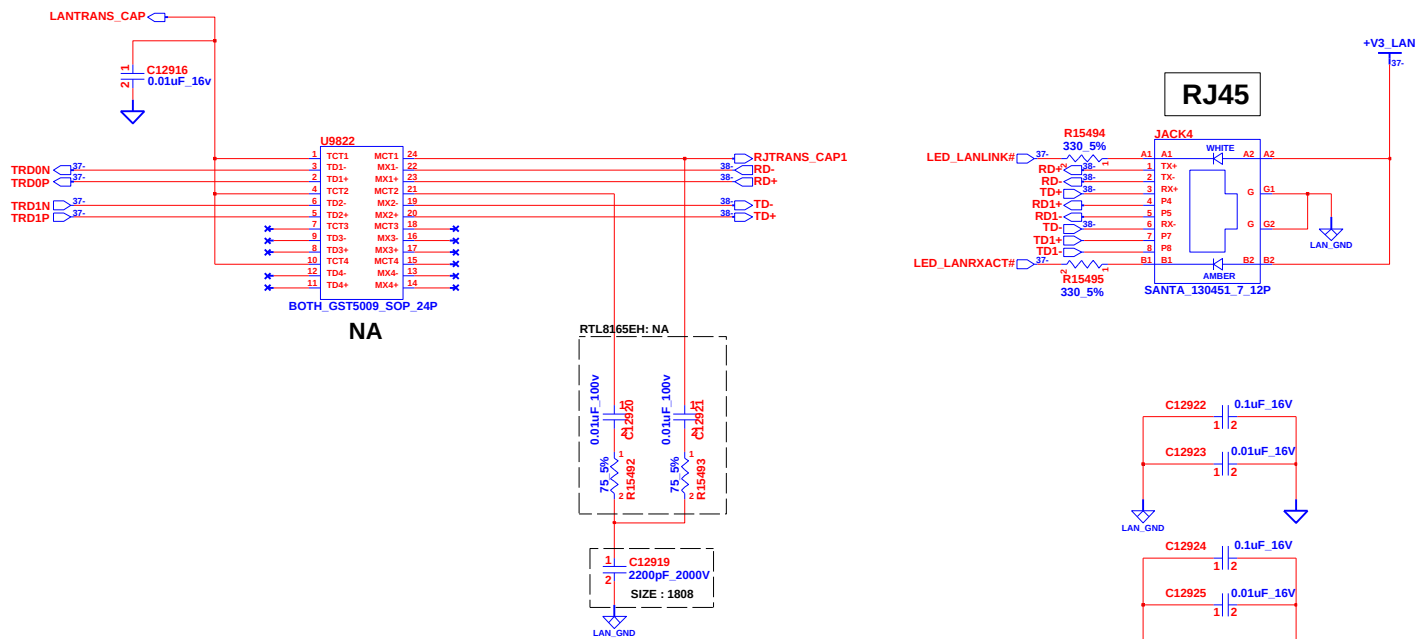
INVENTEC

TITLE
ROCKY-AMD

SIZE CODE DOC. NUMBER REV
A3 CS 1234

SHEET 37 OF 60
REV **X01**

CHANGE by **Ken, Chiang** 5-Aug-2010



LAYOUT NOTE : Place termination resistors and caps as close to LAN controller as possible

INVENTEC

TITLE
ROCKY-AMD

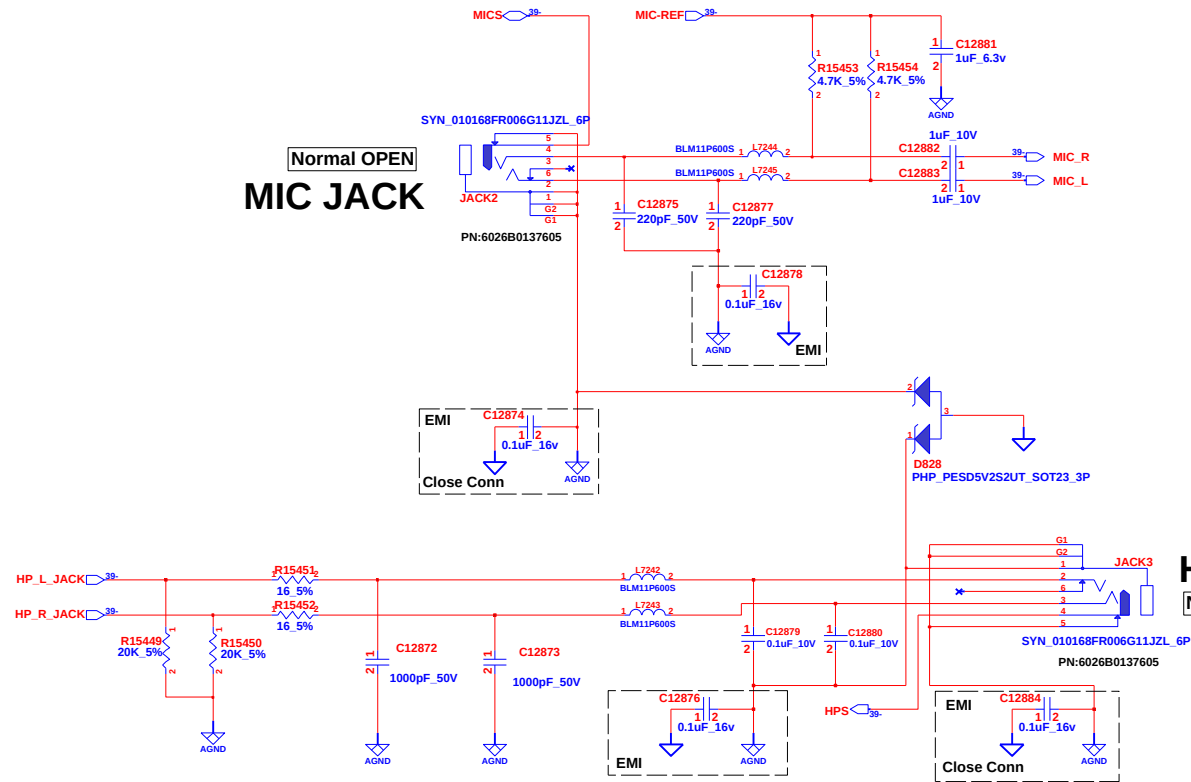
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
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CHANGE by <i>Ken, Chiang</i>	5-Aug-2010
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SHEET 38	OF 60
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Normal OPEN
MIC JACK

HP JACK
Normal OPEN



INVENTEC

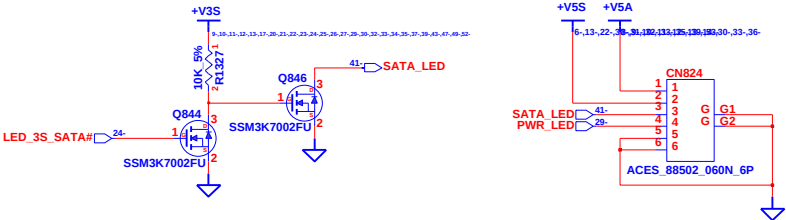
TITLE
**ROCKY-AMD
HDMI**

SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
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CHANGE by *Ken, Chiang* 9-Jun-2010

SHEET 40 OF 60

LED BOARD on MB



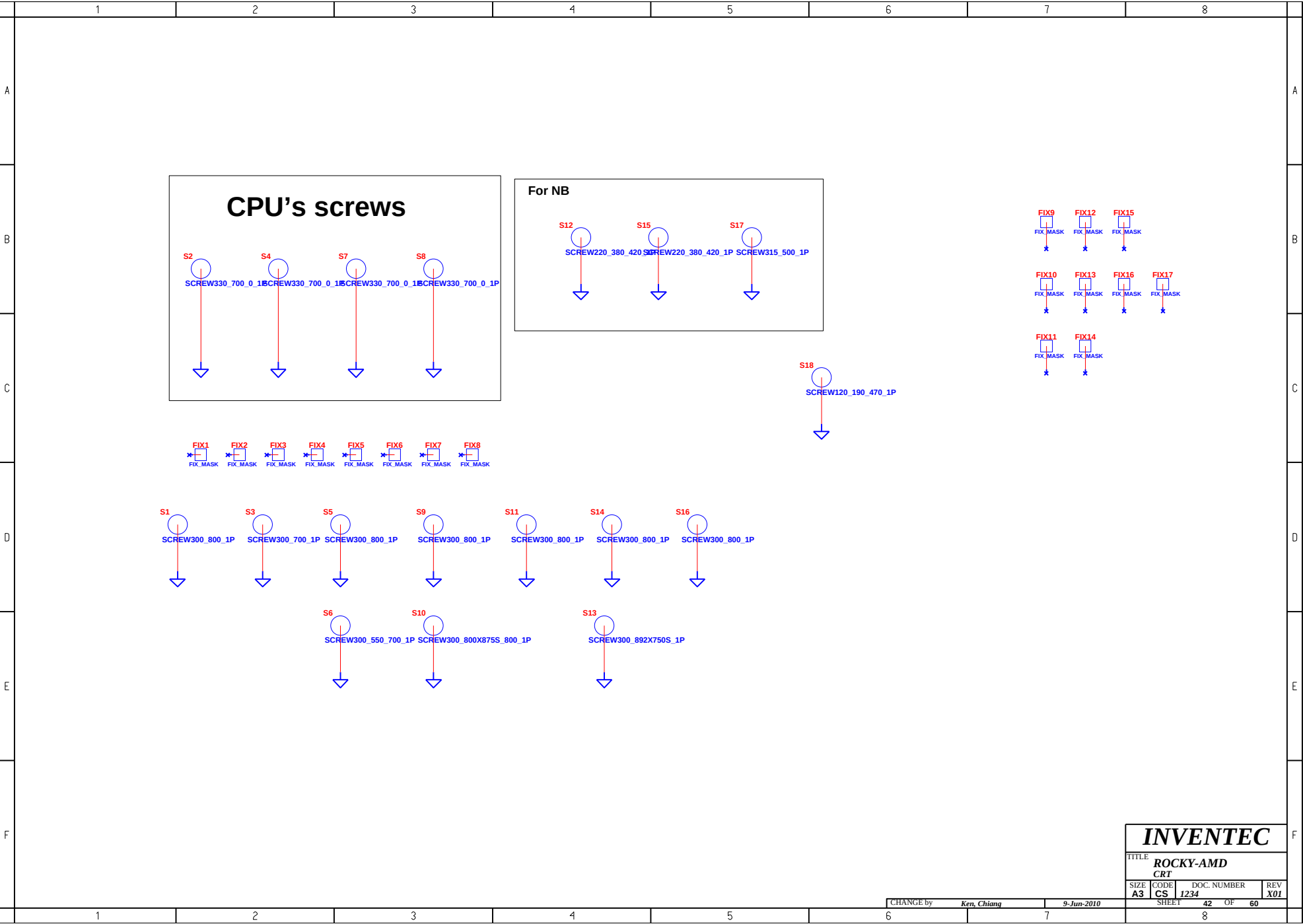
INVENTEC

TITLE
**ROCKY-AMD
DDR3 DAMPING**

SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
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CHANGE by *Ken, Chiang* 4-Aug-2010

SHEET 41 OF 60



A



D

3



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A

B

1

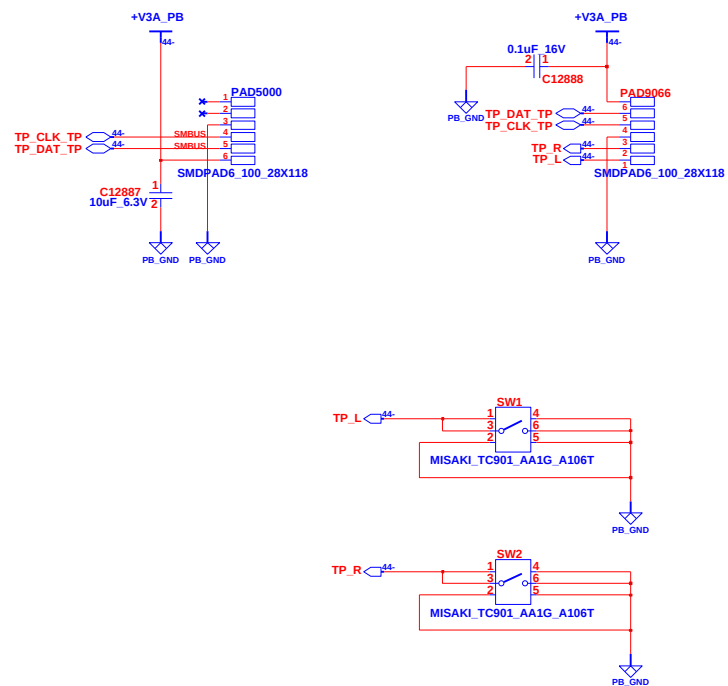
D

F

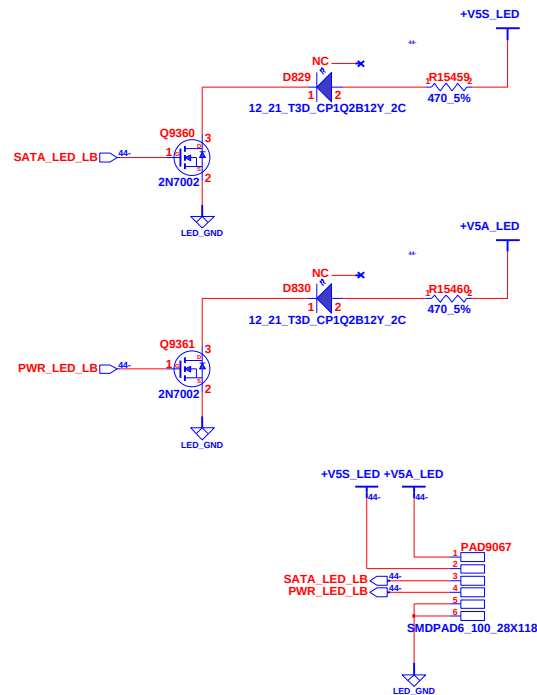
3

--	--

PICK BUTTON BOARD



LED BOARD



INVENTEC

TITLE			
ROCKY-AMD KEYBOARD CONN			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01

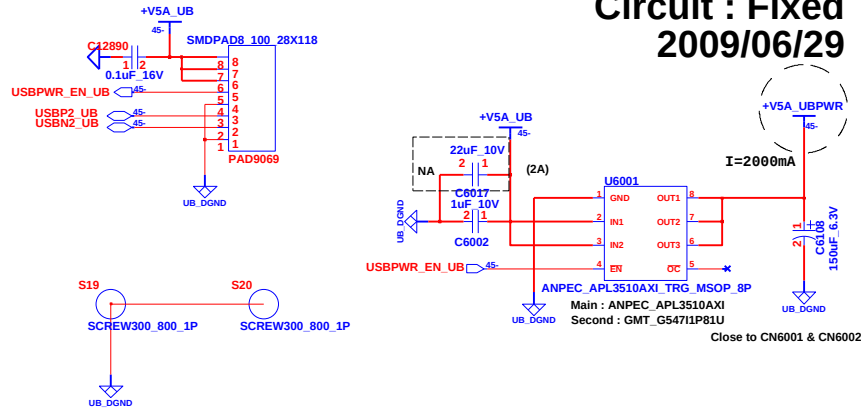
CHANGE by Ken, Chiang 9-Jun-2010

SHEET 44 OF 60

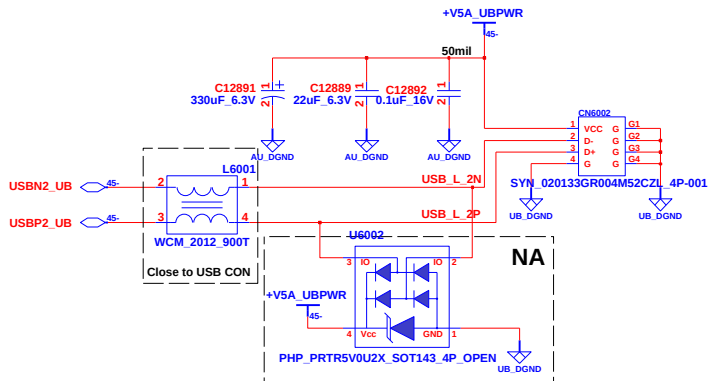
USB BOARD

USB BOARD Cable ON UB

Circuit : Fixed
2009/06/29

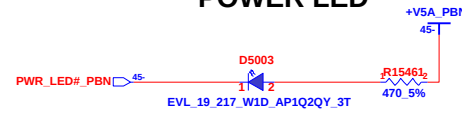


USB CONN03

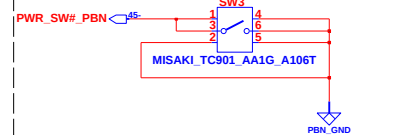


POWER BOTTON BOARD

POWER LED

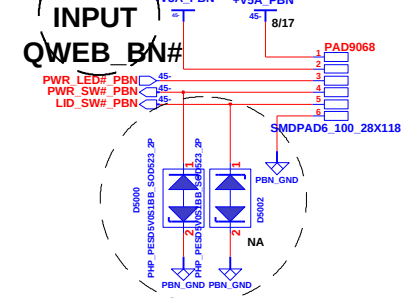


POWER BUTTON

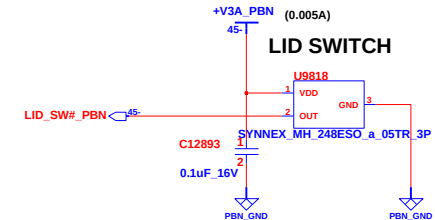


Circuit : Fixed
2009/06/29

PBN Cable CN on PBN



LID SWITCH



INVENTEC

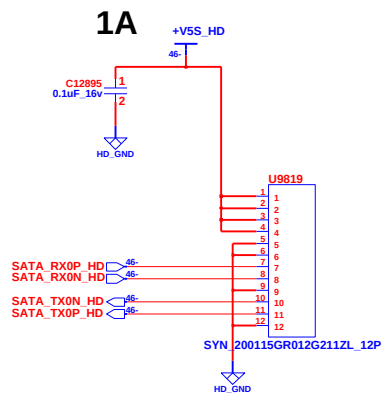
TITLE
ROCKY-AMD
AU6433 & CARDREADER CONN
SIZE CODE DOC. NUMBER REV
A3 CS 1234 45 OF 60 X01

CHANGE by Ken, Chiang 9-Jun-2010

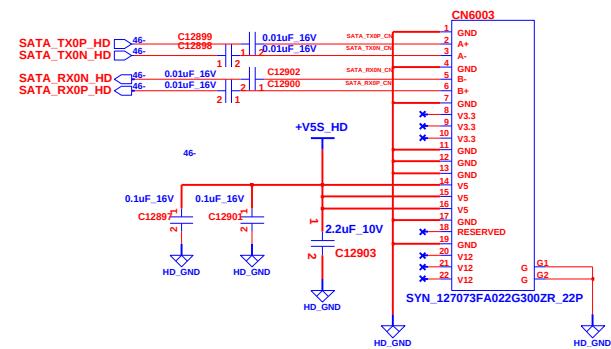
SHEET 45 OF 60

SATA HDD BOARD

SATA HDD FFC CONN on HDD/B



HDD CONN

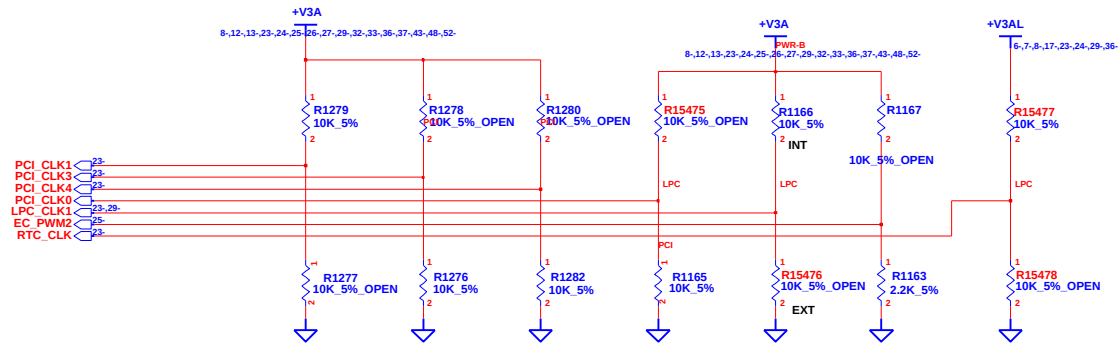


INVENTEC

TITLE			
ROCKY-AMD			
SATA HDD & SATA ODD			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01

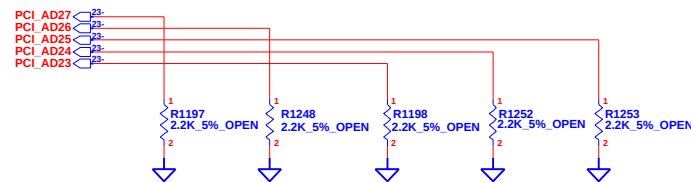
CHANGE by Ken Chiang 9-Jun-2010

SHEET 46 OF 60



Required Straps:

RTCCCLK		PCI_CLK1	PCI_CLK3	PCI_CLK4	PCI_CLK0	PCI_CLK1	EC_PWM2
S5 PLUS MODE DISABLE (DEFAULT)	PULL HIGH	ALLOW PCIE Gen2 DEFAULT	USE DEBUG STRAP	non Fusion CLOCK MODE APU_CLK AND DISP_CLK NO CLOCK OUTPUT	EC ENABLED	INTEGRATED CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT
S5 PLUS MODE ENABLE	PULL LOW	FORCE PCIE Gen1	IGNORE DEBUG STRAPE DEFAULT	Fusion CLOCK MODE DEFAULT APU_CLK AND DISP_CLK CLOCK OUTPUT FROM INT CLOCK GEN	EC DISABLED DEFAULT	INTEGRATED CLKGEN DISABLED	SPI ROM



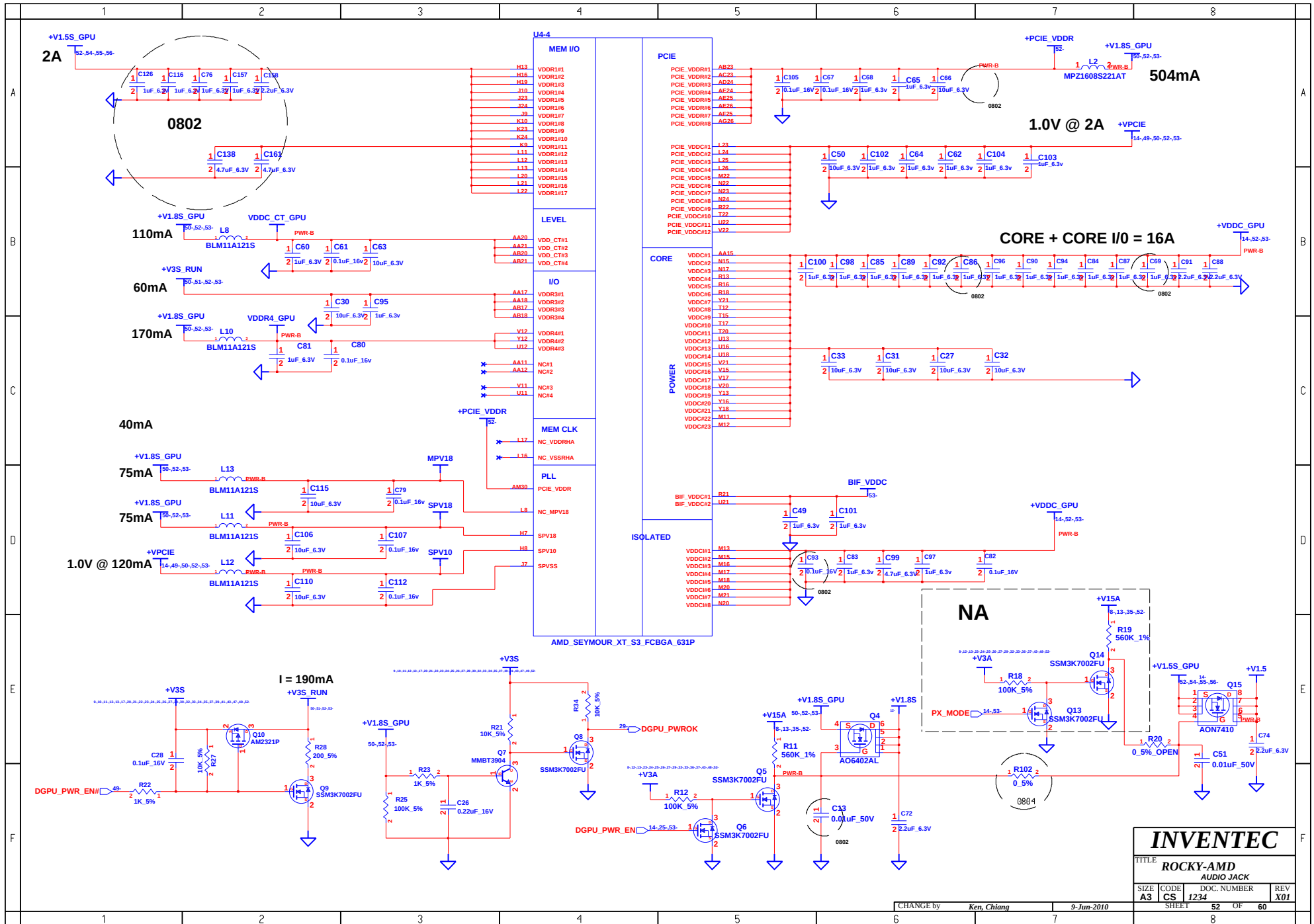
Debug Straps

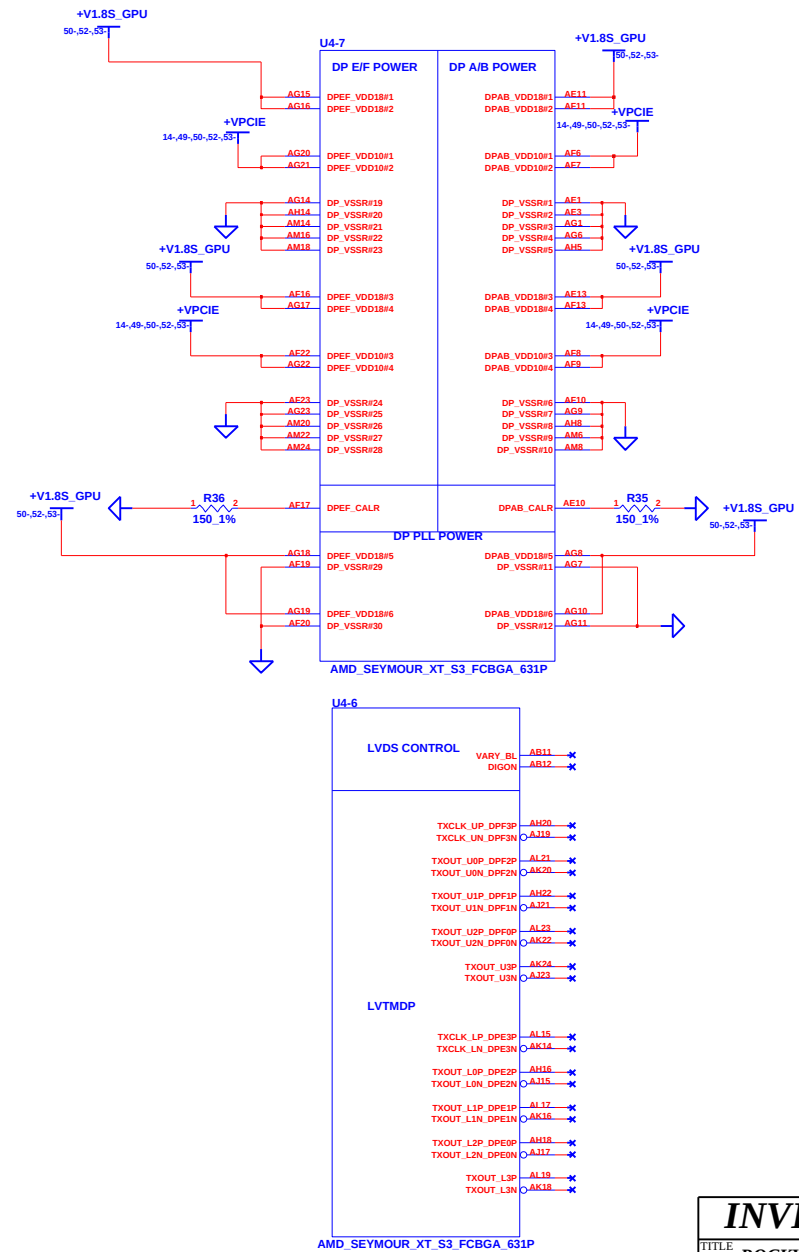
SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_3S_AD27	PCI_3S_AD24	PCI_3S_AD23
PULL HIGH	USE PCI PLL (default)	GETTING I2C ROM ENABLE	DISABLE PCI MEM BOOT (default)
PULL LOW	BYPASS PCI PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

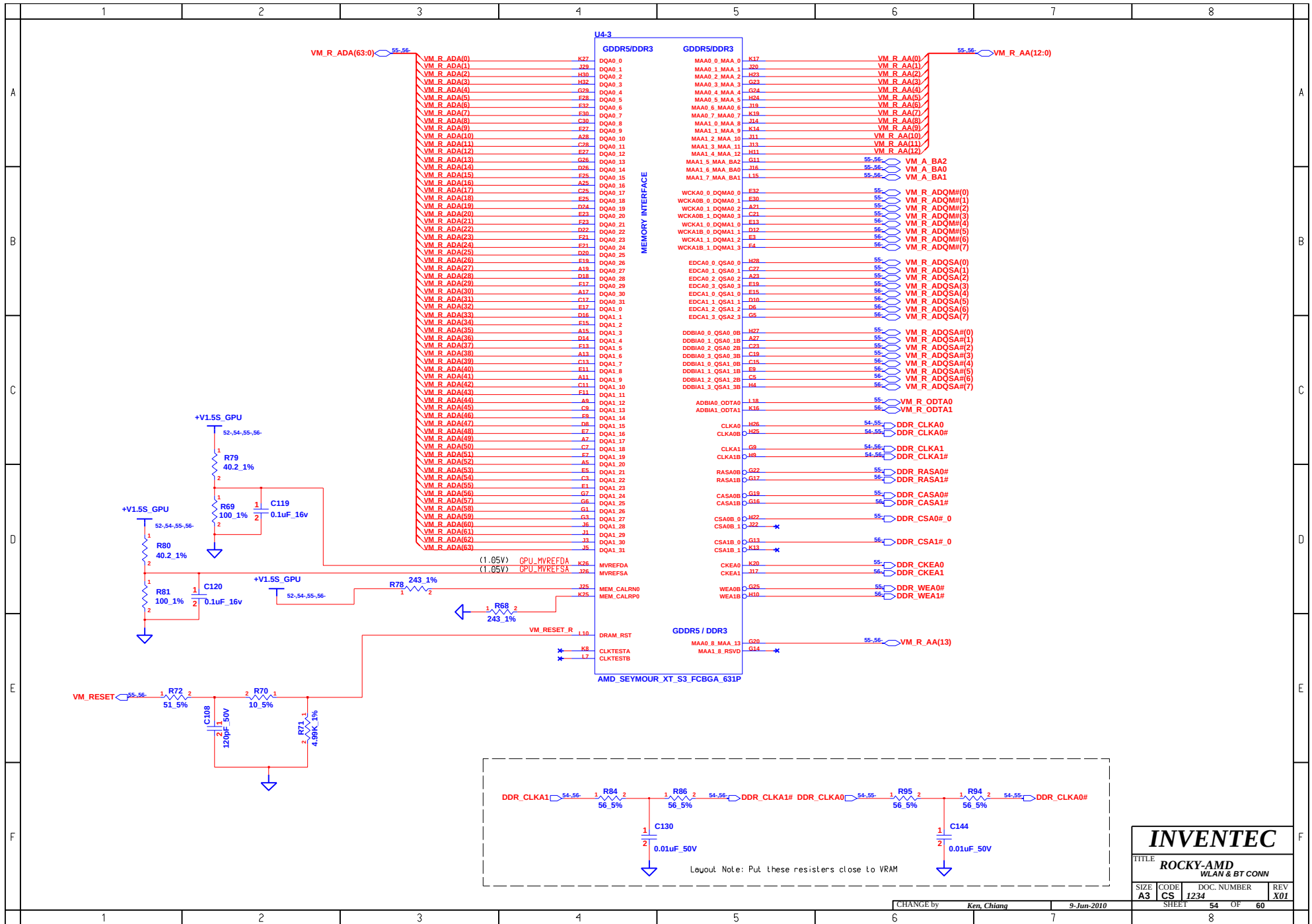
INVENTEC			
TITLE ROCKY-AMD ESATA & USB BOARD CABLE			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
SHEET 48 OF 60			

CHANGE by Ken Chiang 9-Jun-2010





CHANGE by	<i>Ken, Chiang</i>	<i>4-Aug-2010</i>
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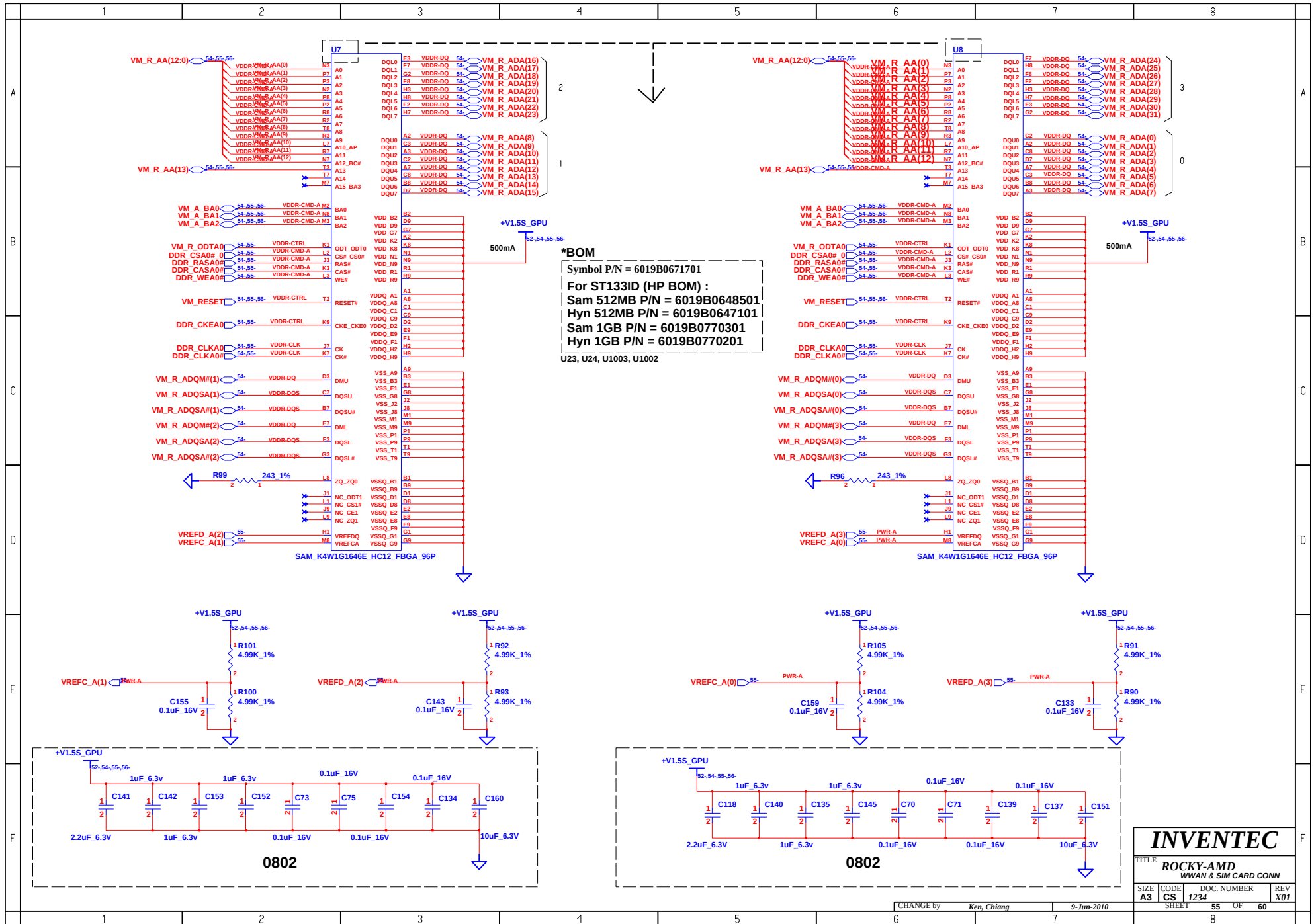
INVENTEC

TITLE
ROCKY-AMD
WLAN & BT CONN

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01

CHANGE by **Ken, Chiang** 9-Jun-2010

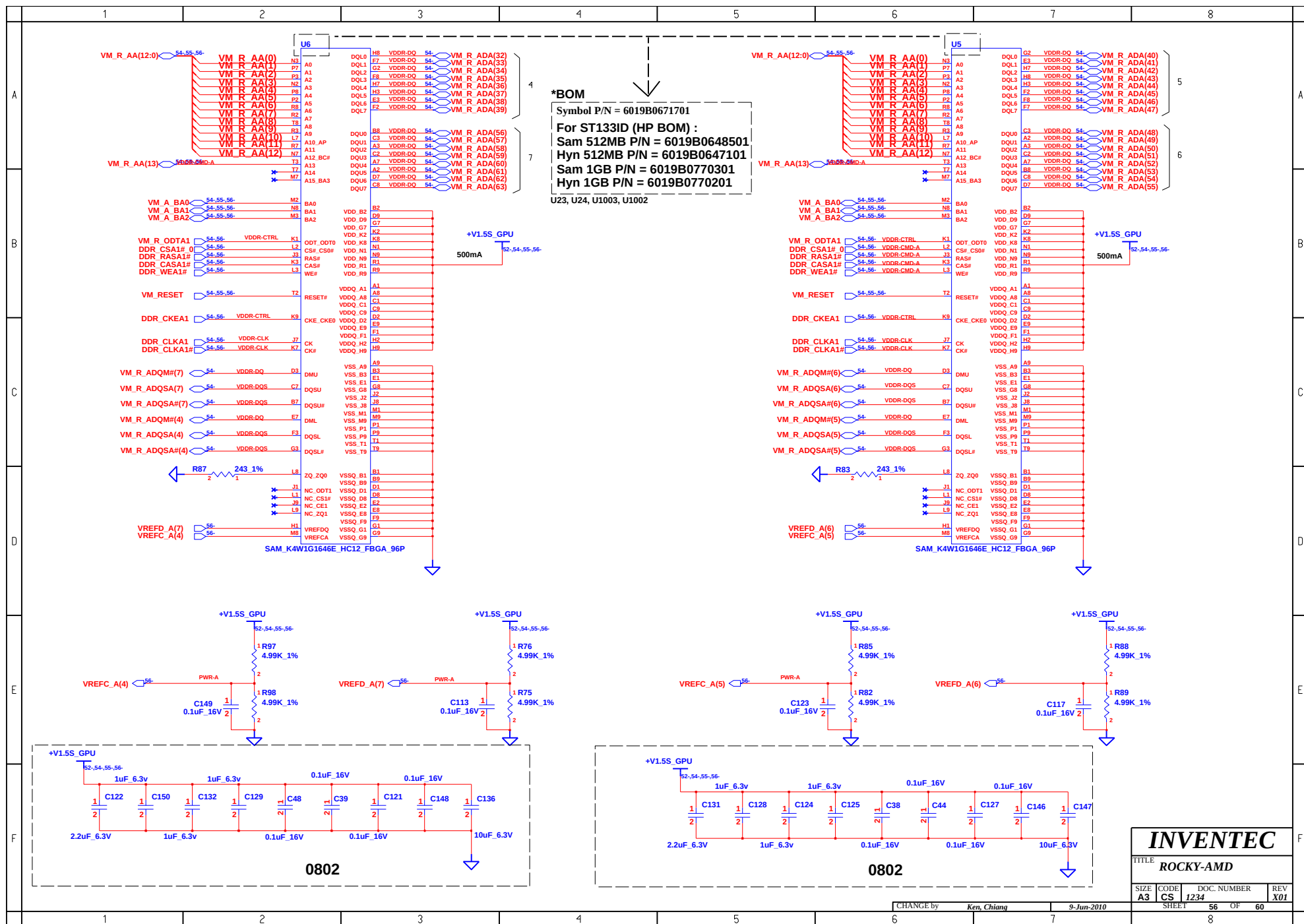
SHEET 54 OF 60



INVENTEC

TITLE				
ROCKY-AMD				
WWAN & SIM CARD CONN				
SIZE	CODE	DOC. NUMBER	REV	
A3	CS	1234	X01	
SHEET		55	OF	60

CHANGE by Ken, Chiang 9-Jun-2010



	1	2	3	4	5	6	7	8	
A									A
B									B
C									C
D									D
E									E
F									F
						CHANGE by <i>Ken, Chiang</i>		9-Aug-2010	
1	2	3	4	5	6	7	8		

INVENTEC			
TITLE ROCKY-AMD EXT USB CONN			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
SHEET		57	OF 60

	1	2	3	4	5	6	7	8	
A									A
B									B
C									C
D									D
E									E
F									F
						CHANGE by <i>Ken, Chiang</i>		9-Aug-2010	
1	2	3	4	5	6	7	8		

INVENTEC			
TITLE ROCKY-AMD			
SIZE A3	CODE CS	DOC. NUMBER <i>1234</i>	REV X01
SHEET		58	OF 60

	1	2	3	4	5	6	7	8	
A									A
B									B
C									C
D									D
E									E
F									F
						CHANGE by <i>Ken, Chiang</i>		9-Aug-2010	
1	2	3	4	5	6	7	8		

INVENTEC			
TITLE ROCKY-AMD			
SIZE A3	CODE CS	DOC. NUMBER <i>1234</i>	REV X01
SHEET		59	OF 60

	1	2	3	4	5	6	7	8	
A									A
B									B
C									C
D									D
E									E
F									F
						CHANGE by <i>Ken, Chiang</i>		9-Aug-2010	
1	2	3	4	5	6	7	8		

INVENTEC			
TITLE ROCKY-AMD			
SIZE A3	CODE CS	DOC. NUMBER <i>1234</i>	REV X01
SHEET		60	OF 60