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LUXOR10FG															
2011.08.02															
INVENTEC															
DRAWN: ES DATE: POWER: DATE: TITLE: MODEL PROJECT FUNCTION Everest Main Board															
DESIGN: CHECK: RESPONSIBLE: SIZE: CODE: DOC NUMBER: REV: X01															
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NVIDIA
W/ OPTIMUS

N13P-GL
29X 29 MM

IVY BRIDGE
DC 35W
SOCKET-RPGA989
37.5 X 37.5 X 5 mm

DDR3@1.5/0.75V
(1333/1600 MHZ)
204-PIN SODIMMO

DDR3@1.5/0.75V
(1333/1600 MHZ)
204-PIN SODIMM1

HDMI

CRT

LCM

RJ45

PCIE_1:LAN
ATHEROS_AR8161/8162

PCIE_2:WLAN

PCIE_3:USB3.0

PCH
PANTHER POINT
25 X 25 X 2.3 mm

AUDIO CODEC
REA_ALC269Q_VB6

INTERNAL MIC IN

EXT MIC IN

HEADPHONE

USB_0: USB CONN
USB_2: USB CONN
USB_5: MINICARD WLAN
USB_8: CARD READER
USB_10:WEBCAM

SLEEP & CHARGE

USB_1: USB3.0 CONN

USB_8: CARD READER
REA_RTS5129

SATA0:ESATA
SATA1: HDD
SATA6: ODD

EC WINDBOND
NPCE885LA0DX

SPI FLASH 8MB
MXIC_MX25L3206EM21

KEYBOARD

TOUCH PAD

ENE-P2809A
THERMAL SENSOR

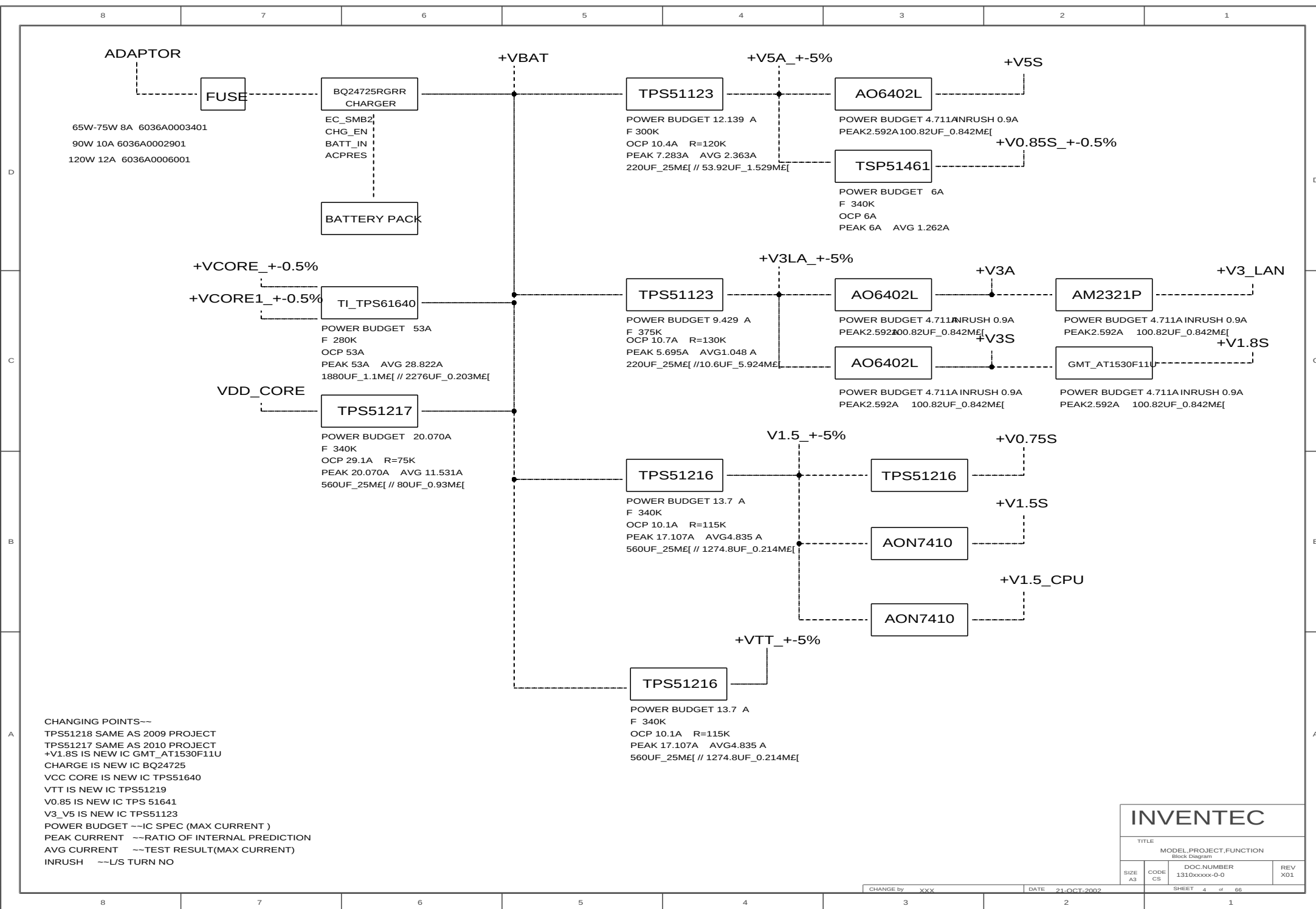
BATTERY CHARGER &
DC/DC & IMVP 7

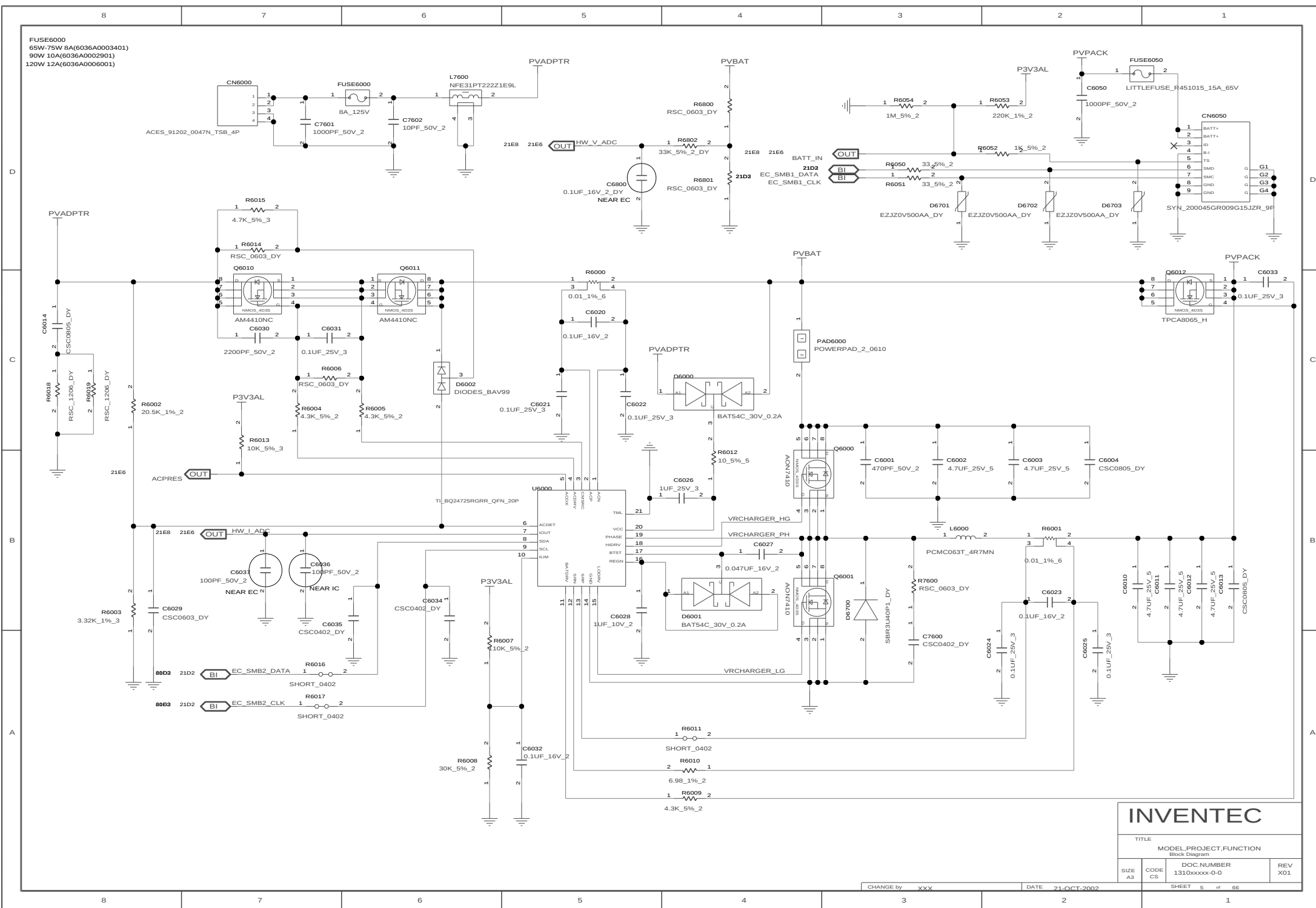
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6-Cell

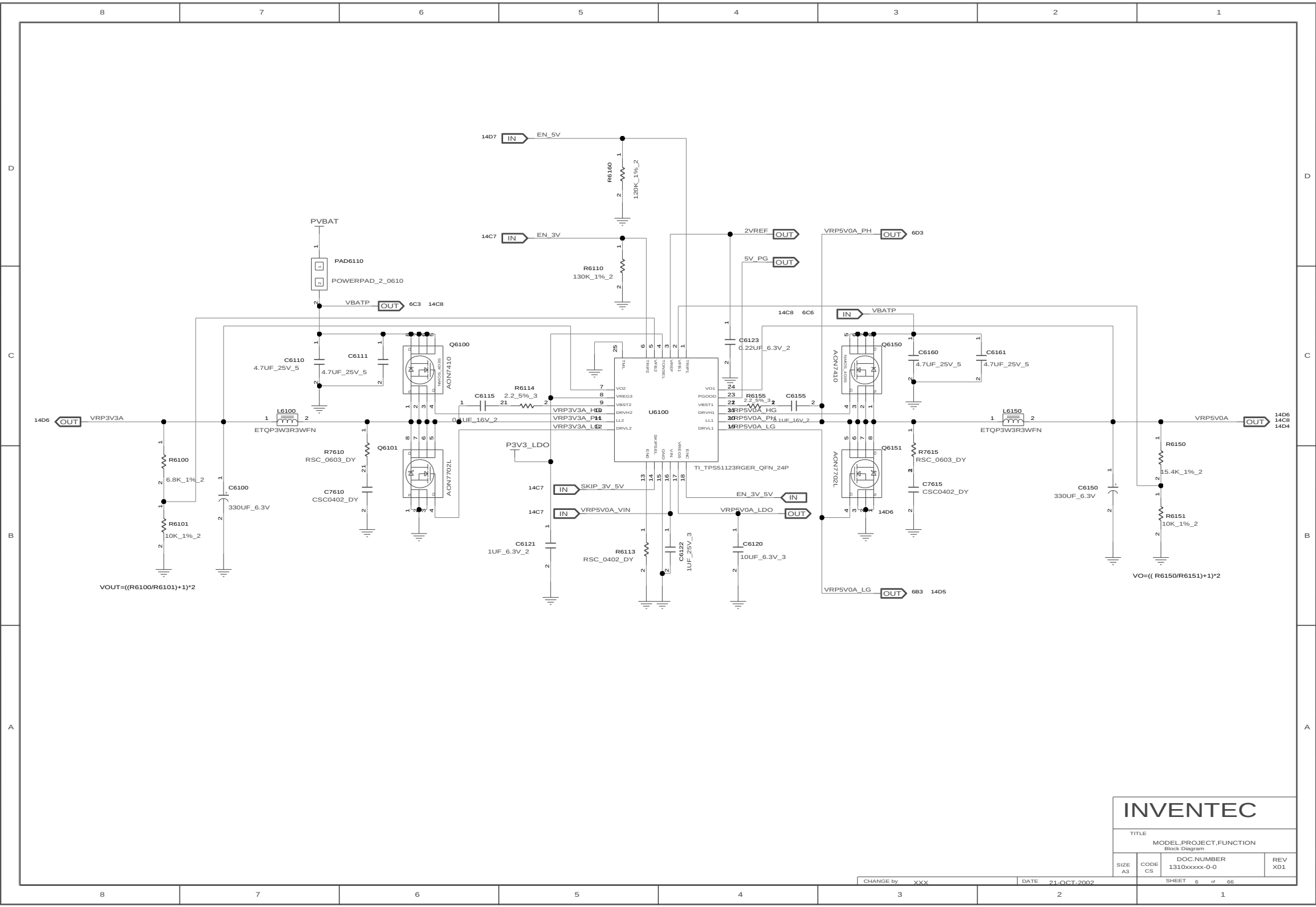
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INVENTEC

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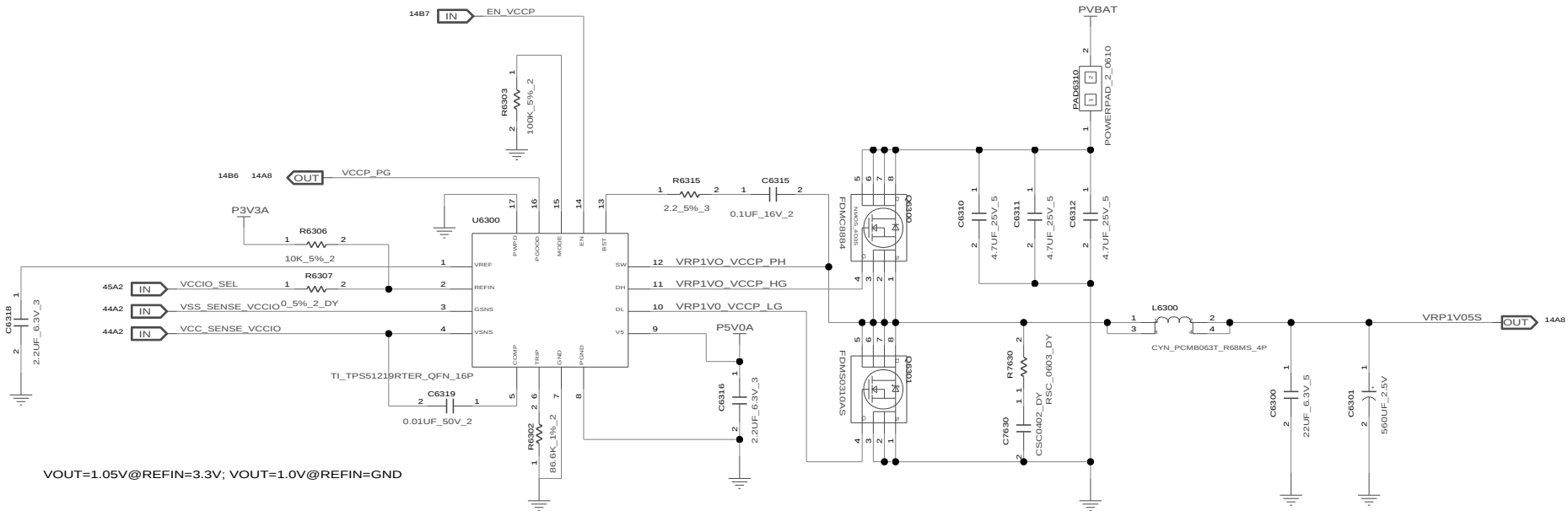
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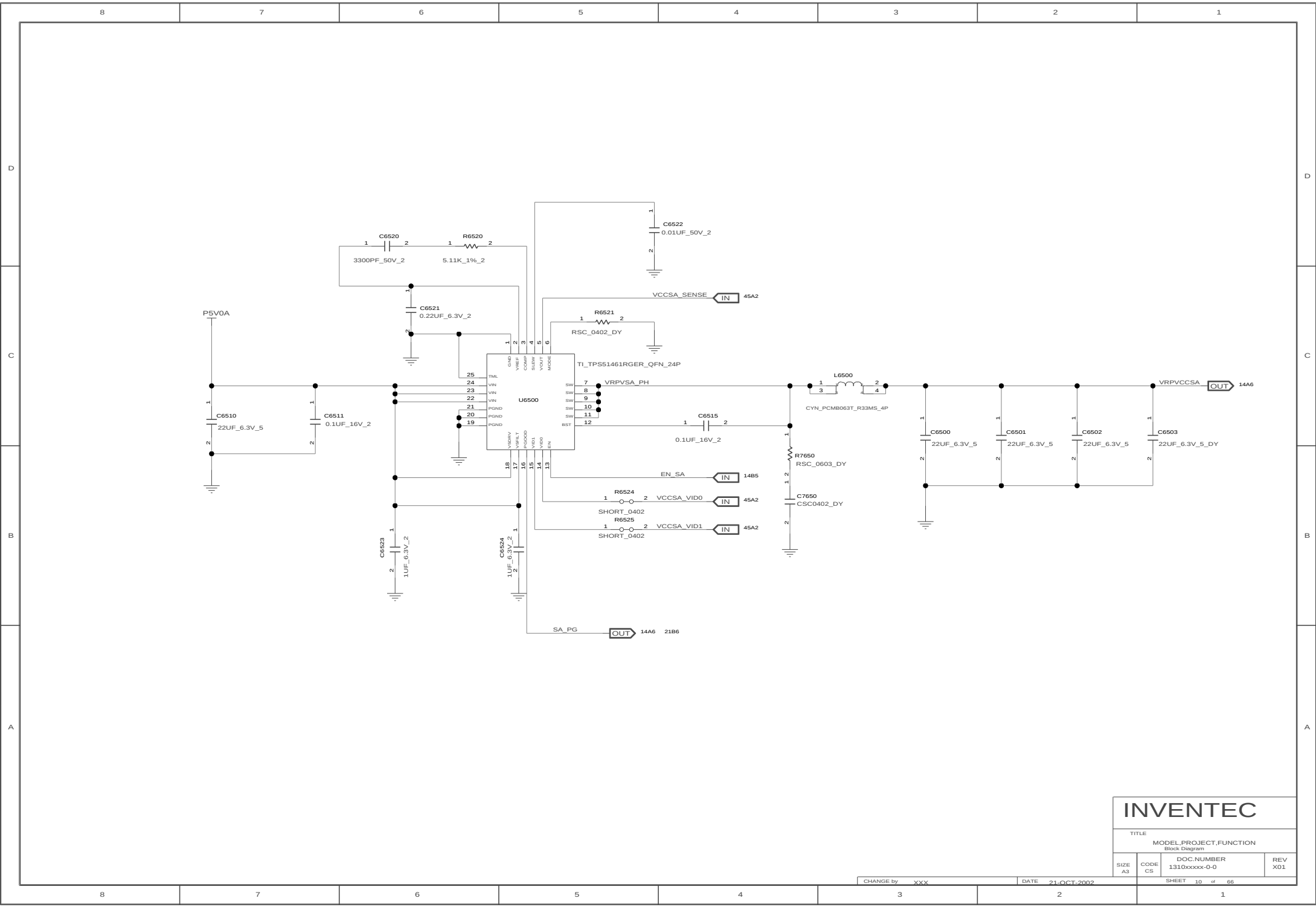
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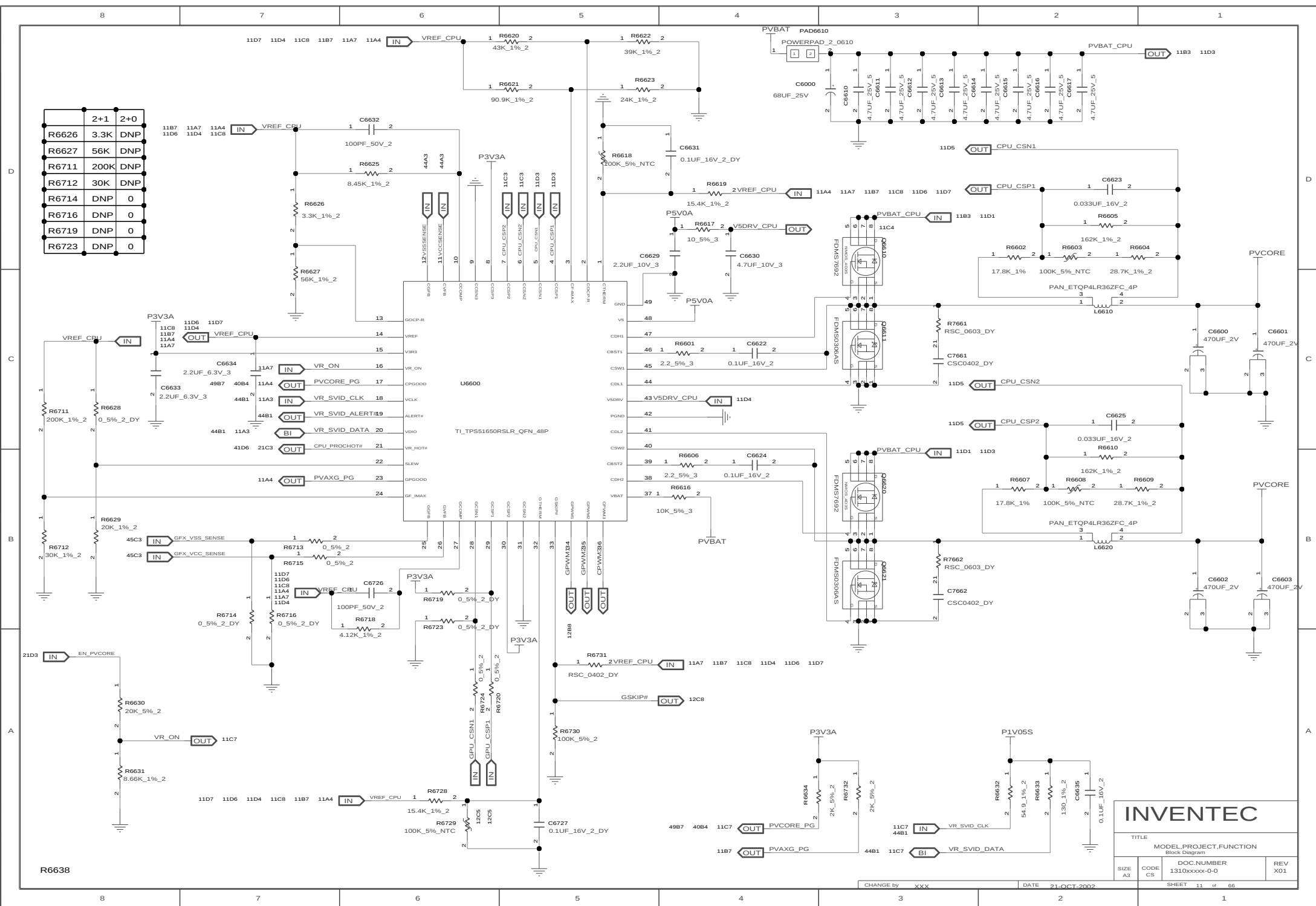


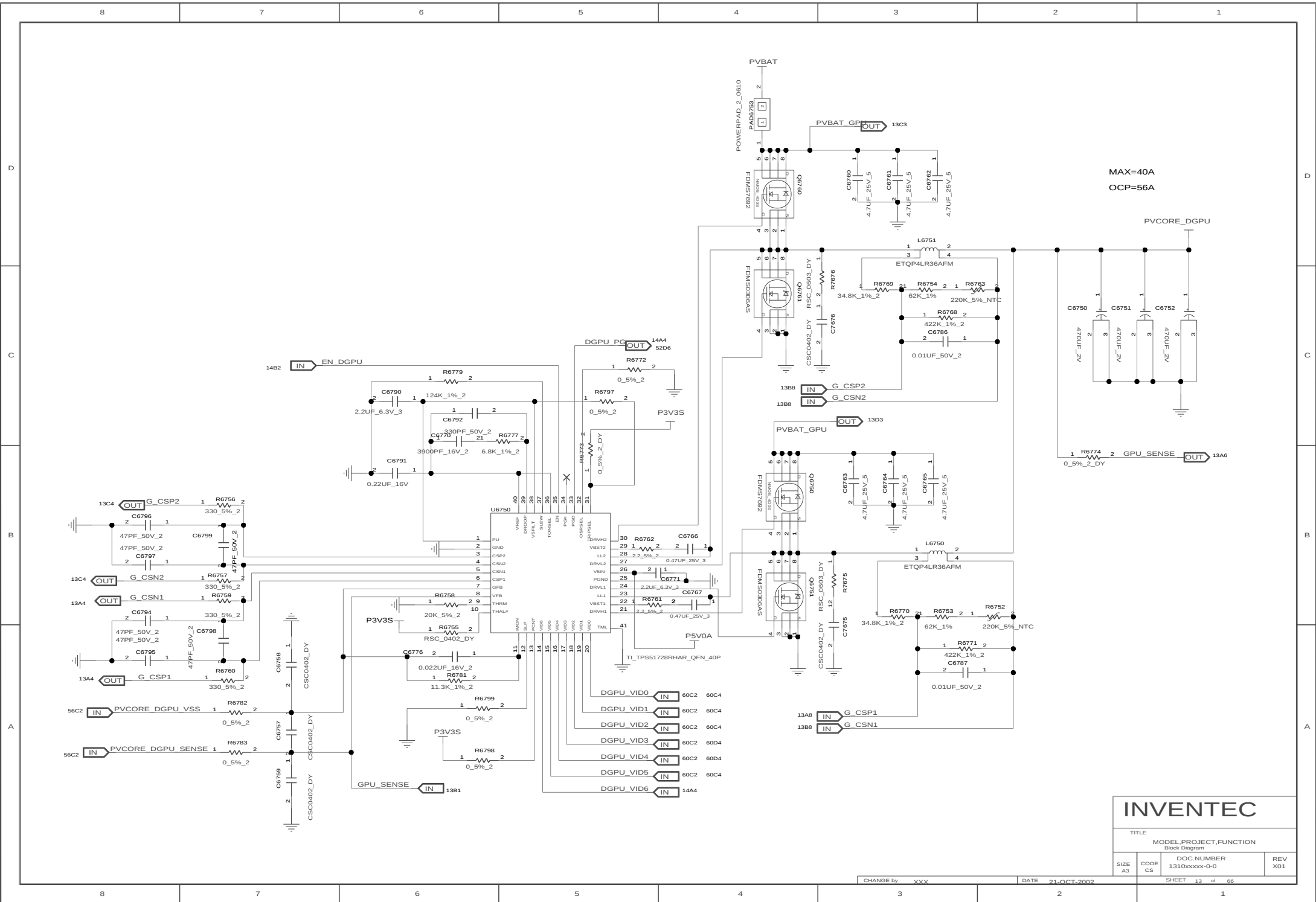
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3V & 5V

VCCIO

VCCSA

DGPU

DDR_P1V5

P1V8S

INVENTEC

TITLE

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DOC.NUMBER

1310xxxx-0-0

REV

X01

SIZE

A3

CODE

CS

CHANGE by

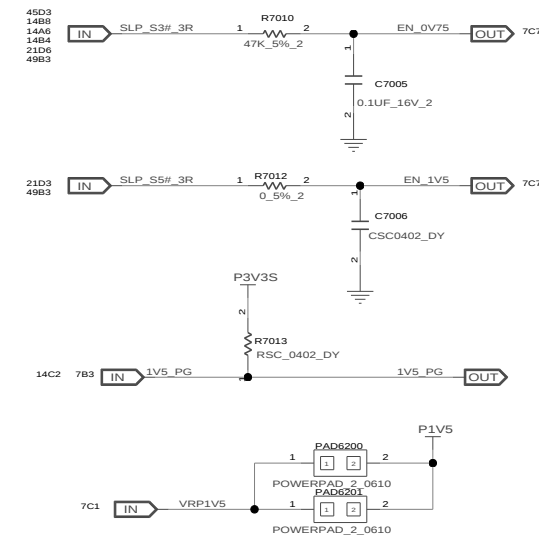
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3V & 5V

VCCIO

VCCSA

DGPU

DDR_P1V5

P1V8S

INVENTEC

TITLE

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1310xxxx-0-0

REV

X01

SIZE

A3

CODE

CS

CHANGE by

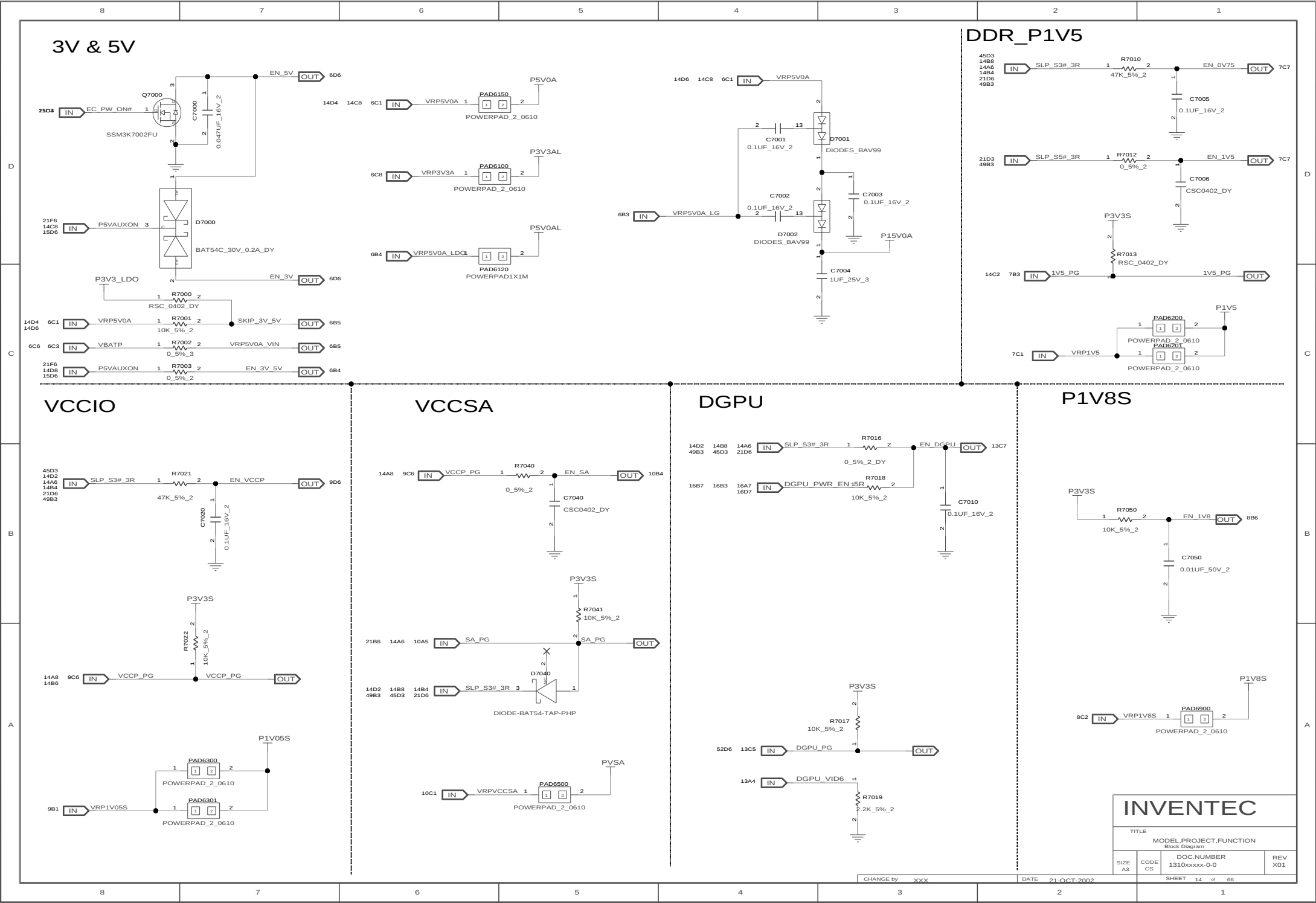
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3V & 5V

VCCIO

VCCSA

DGPU

DDR_P1V5

P1V8S

INVENTEC

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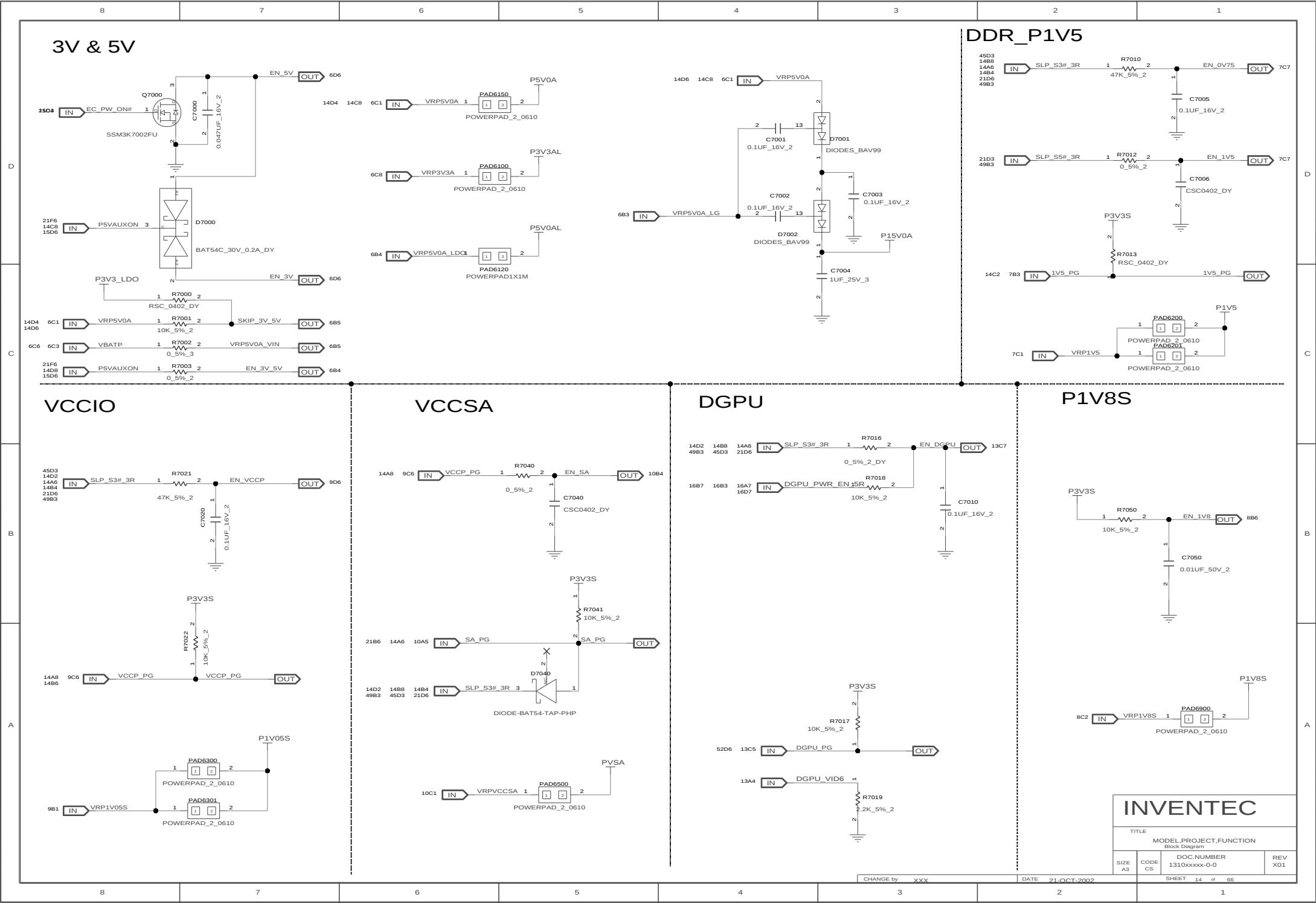
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3V & 5V

VCCIO

VCCSA

DGPU

DDR_P1V5

P1V8S

INVENTEC

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CHANGE by

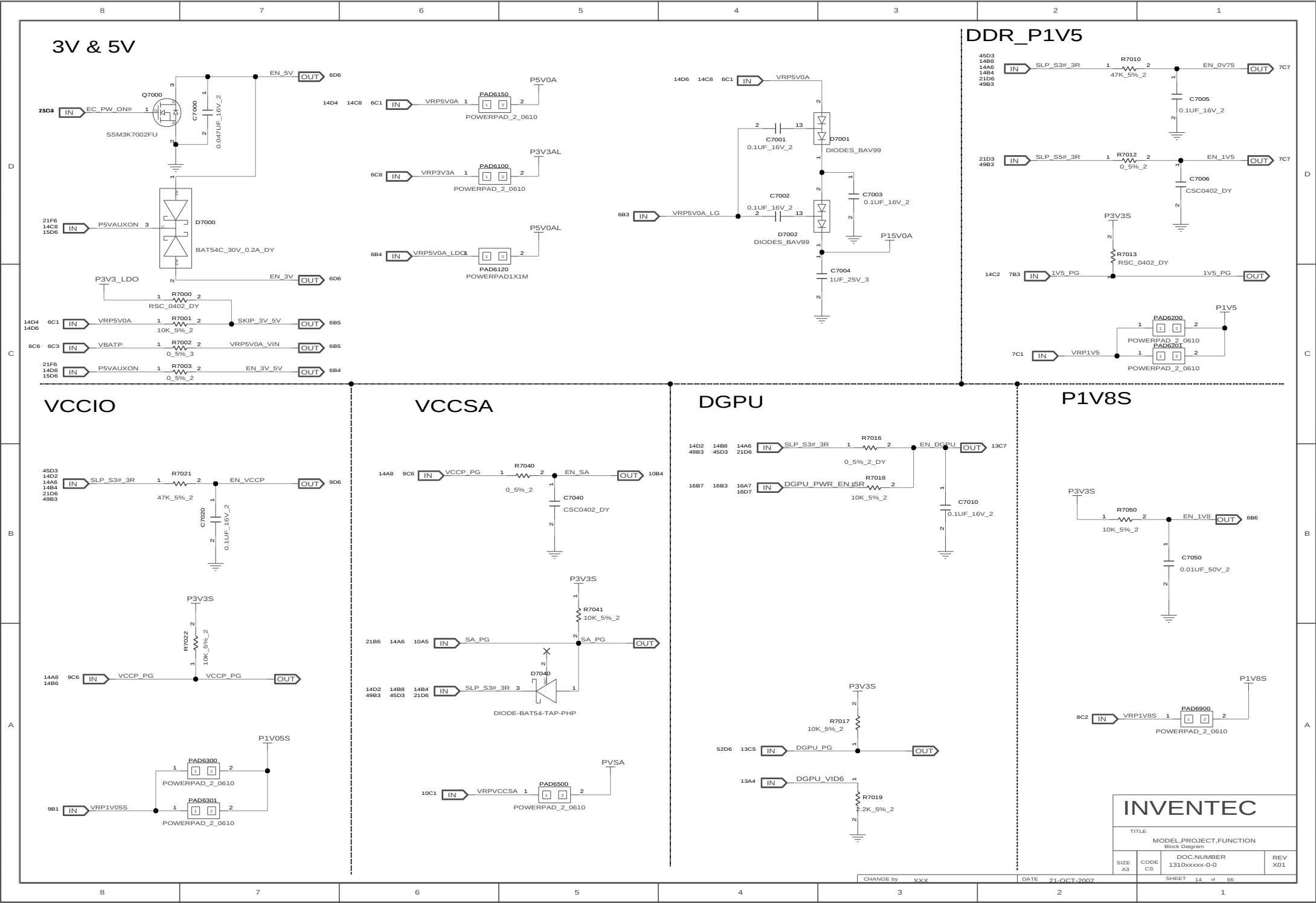
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3V & 5V

VCCIO

VCCSA

DGPU

DDR_P1V5

P1V8S

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CHANGE by

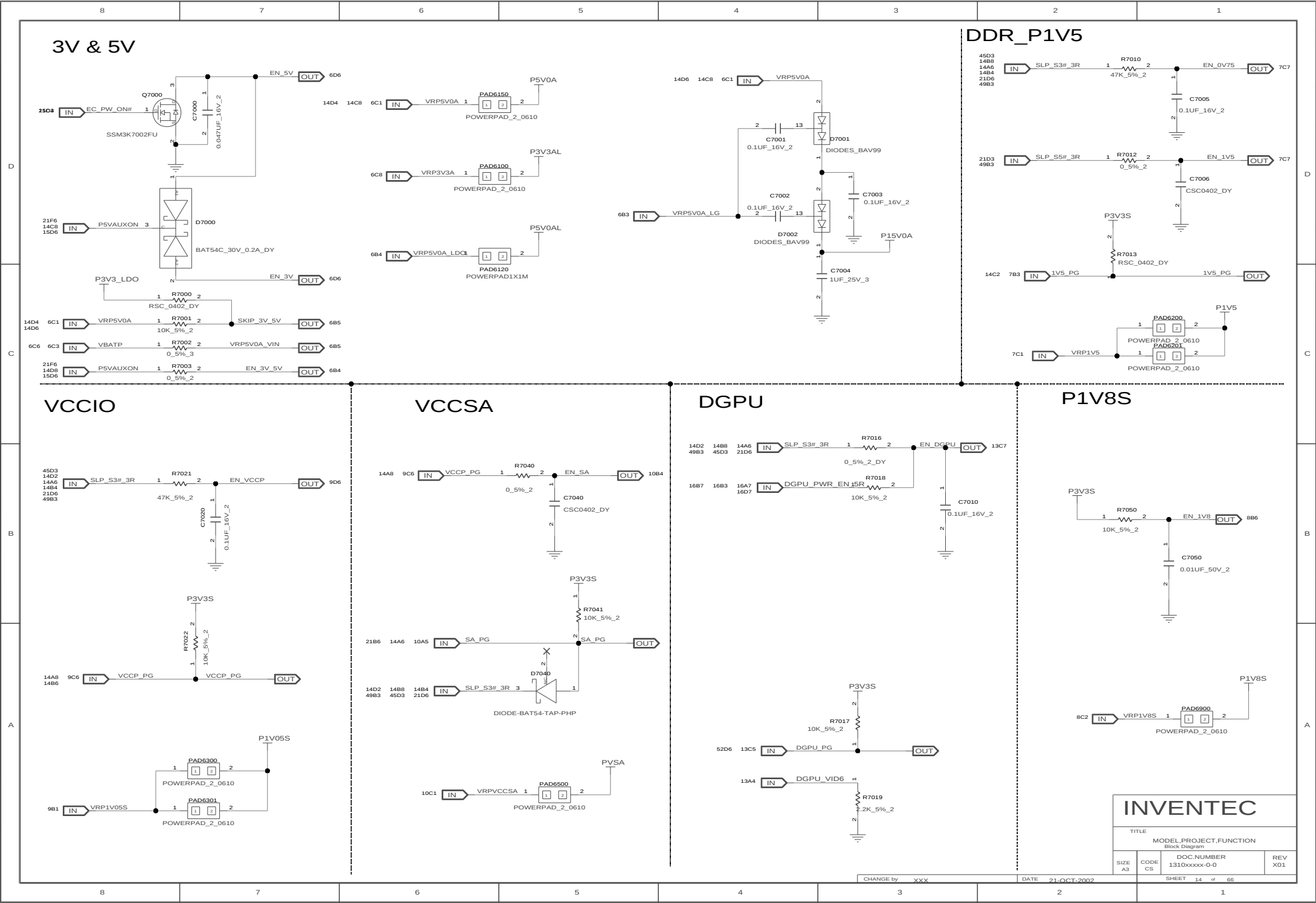
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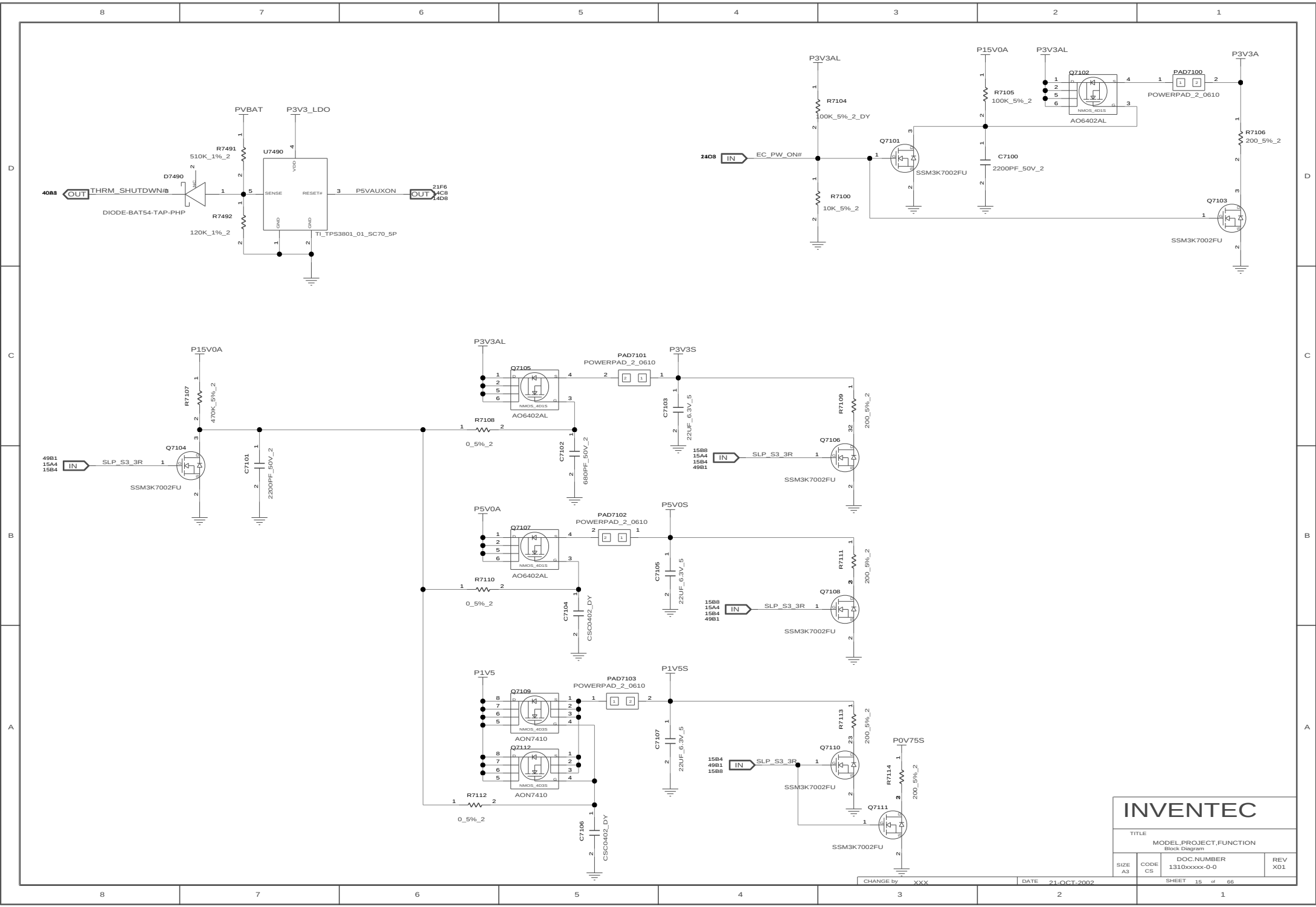
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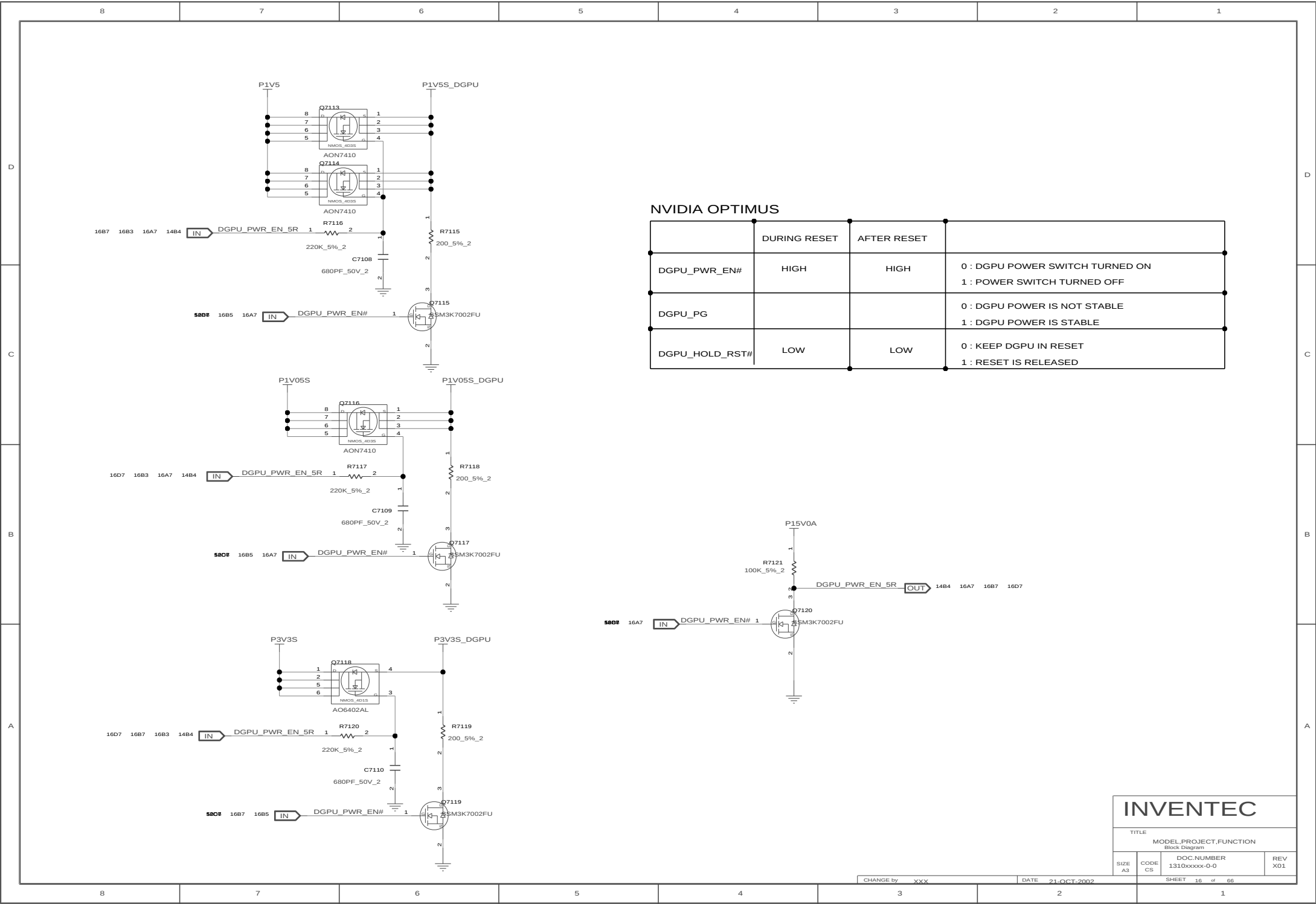
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NVIDIA OPTIMUS

	DURING RESET	AFTER RESET	
DGPU_PWR_EN#	HIGH	HIGH	0 : DGPU POWER SWITCH TURNED ON 1 : POWER SWITCH TURNED OFF
DGPU_PG			0 : DGPU POWER IS NOT STABLE 1 : DGPU POWER IS STABLE
DGPU_HOLD_RST#	LOW	LOW	0 : KEEP DGPU IN RESET 1 : RESET IS RELEASED

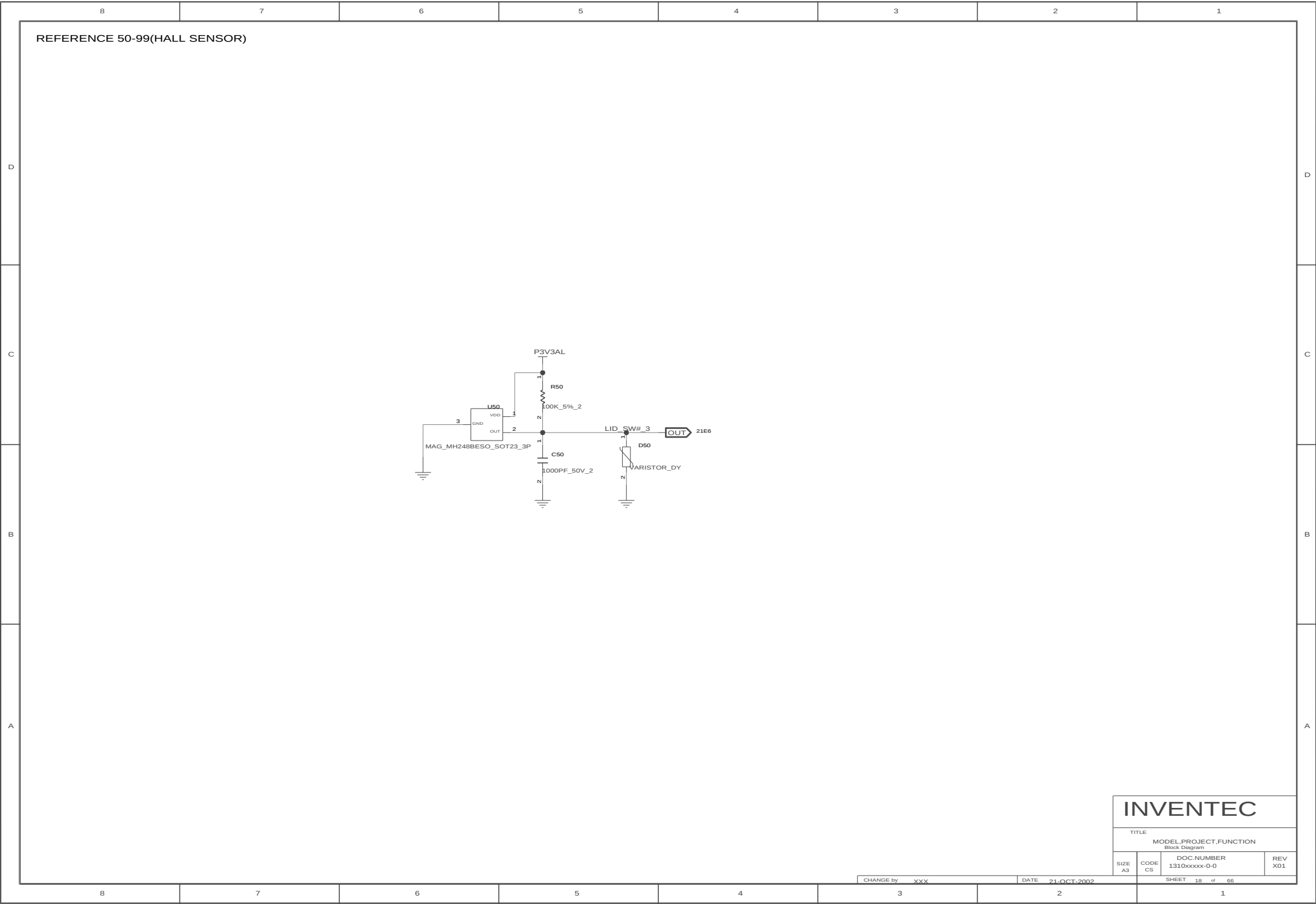
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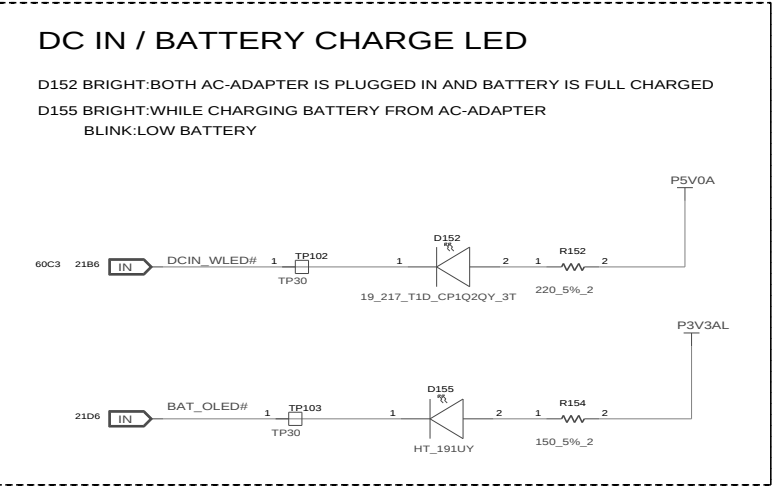
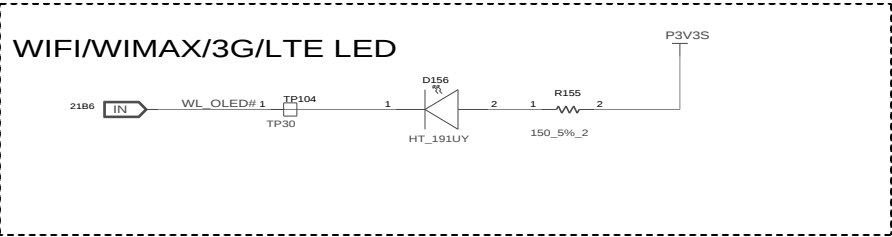
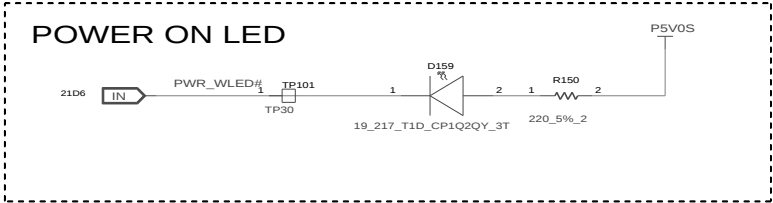
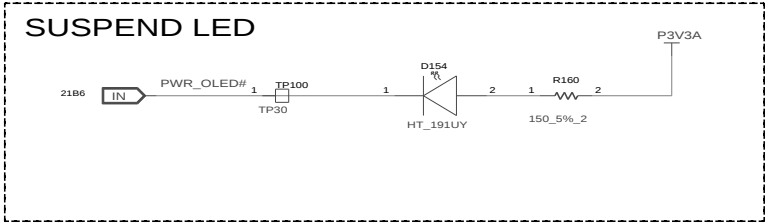
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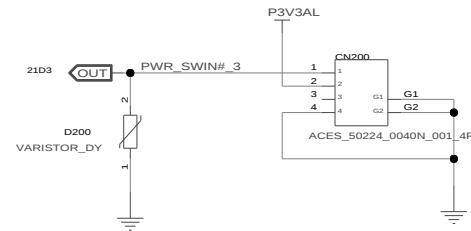
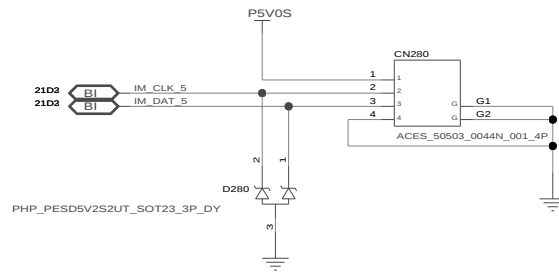
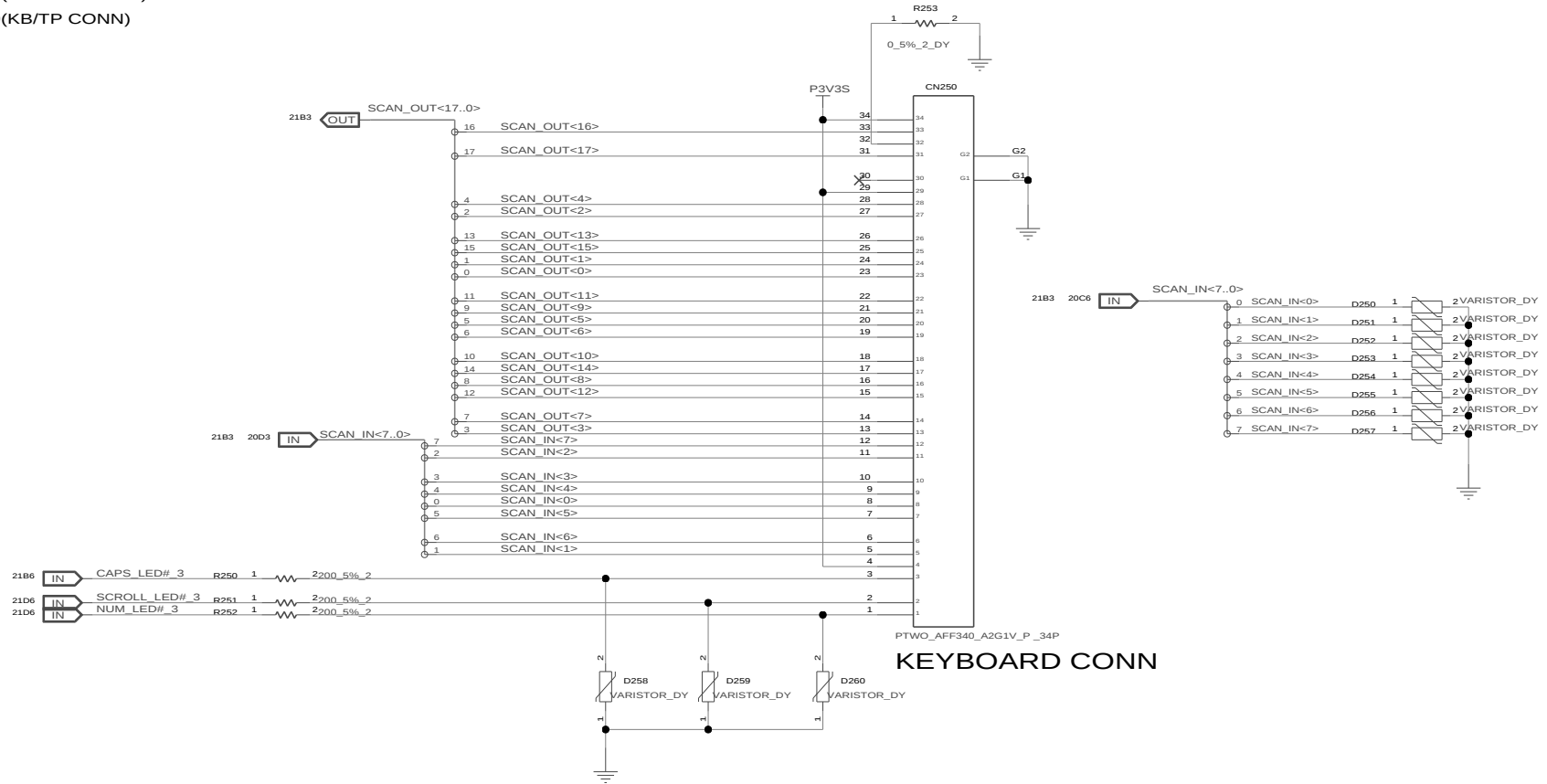
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REFERENCE 200~249(POWER CONN)
REFERENCE 250~299(KB/TP CONN)



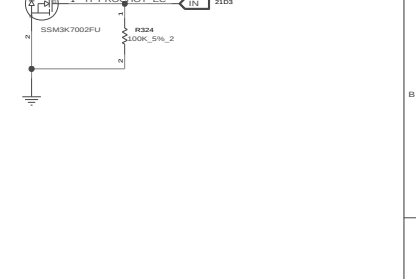
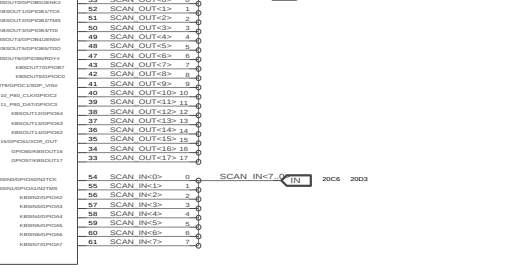
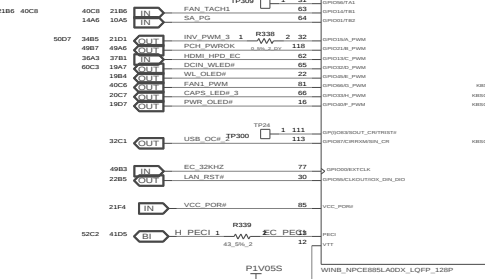
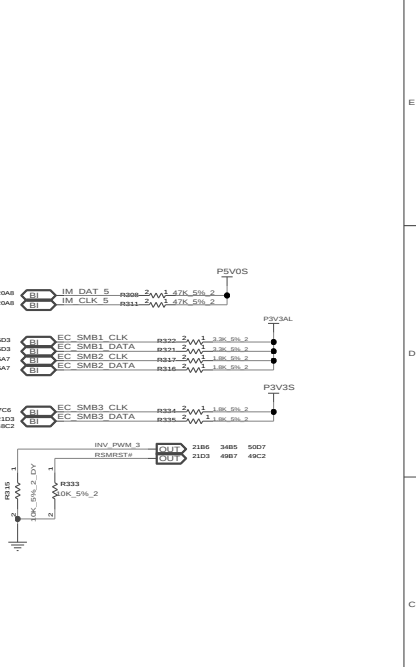
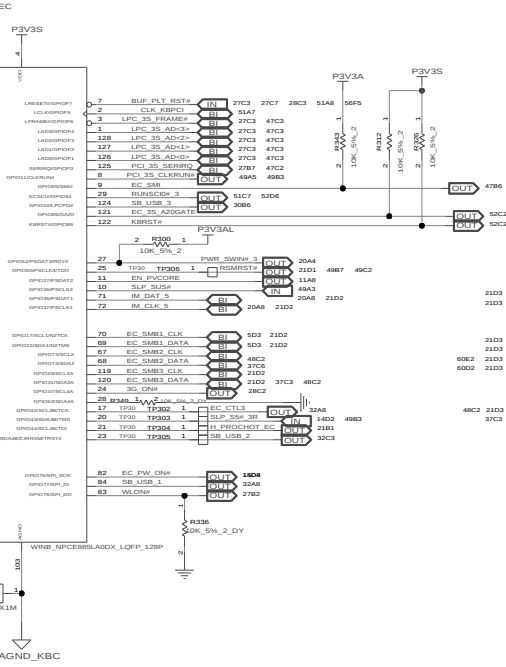
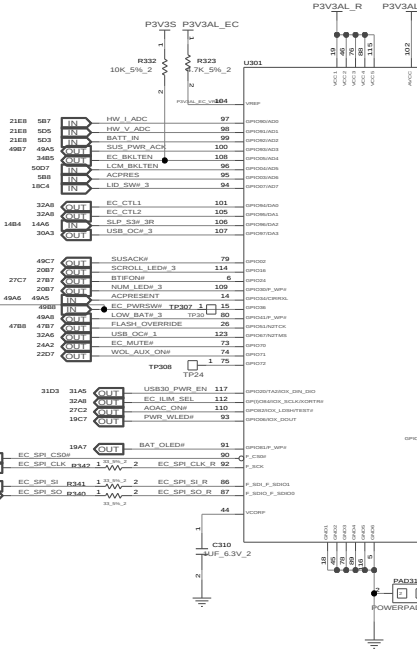
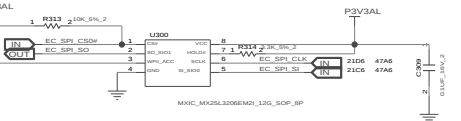
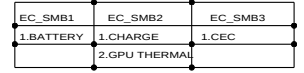
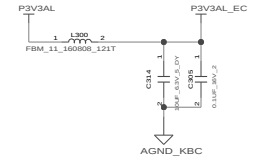
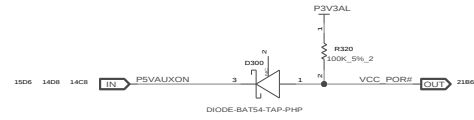
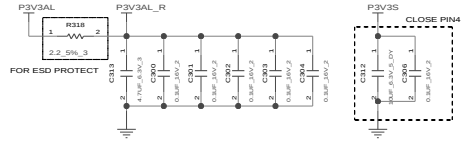
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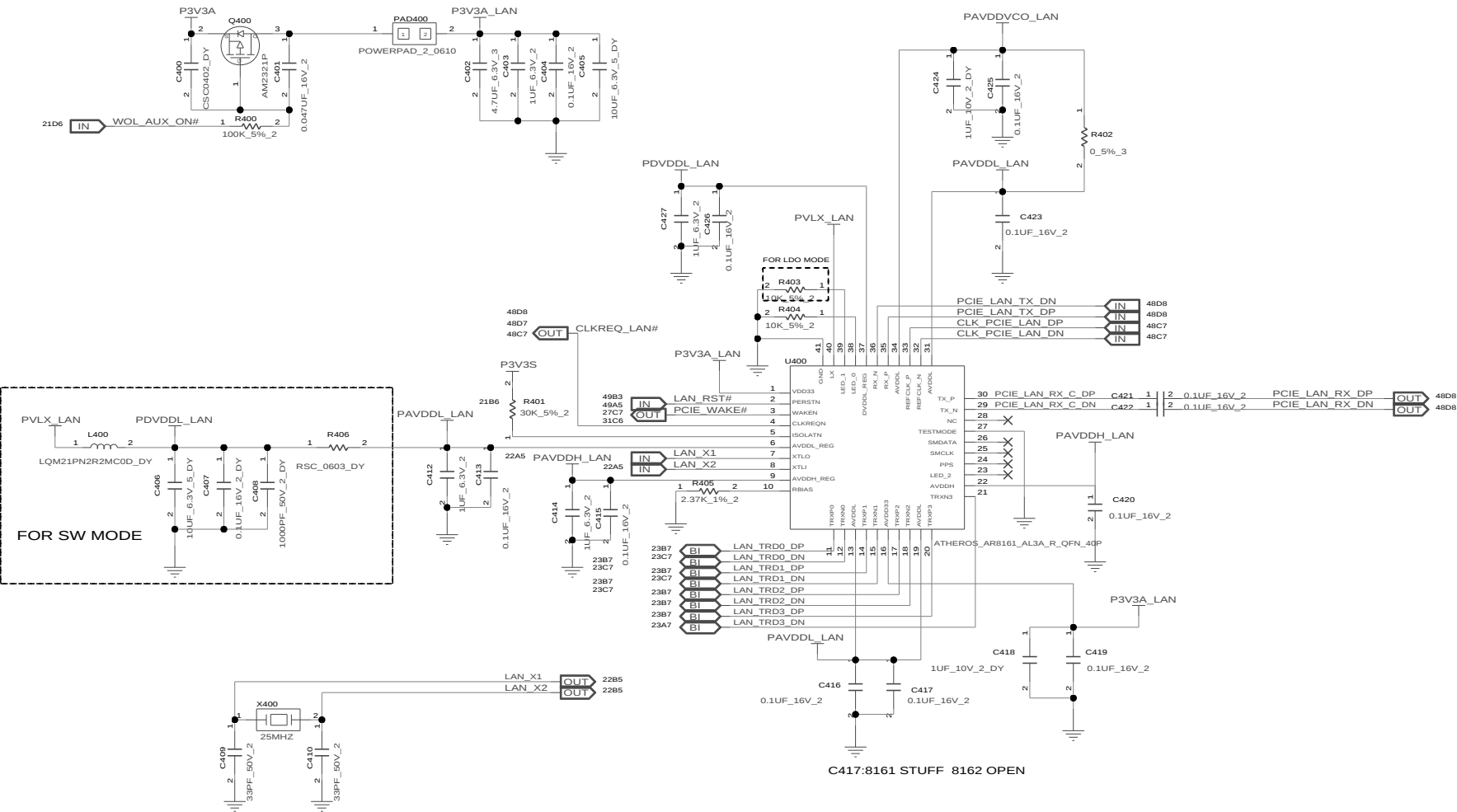
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REFERENCE 300-389(KBC)





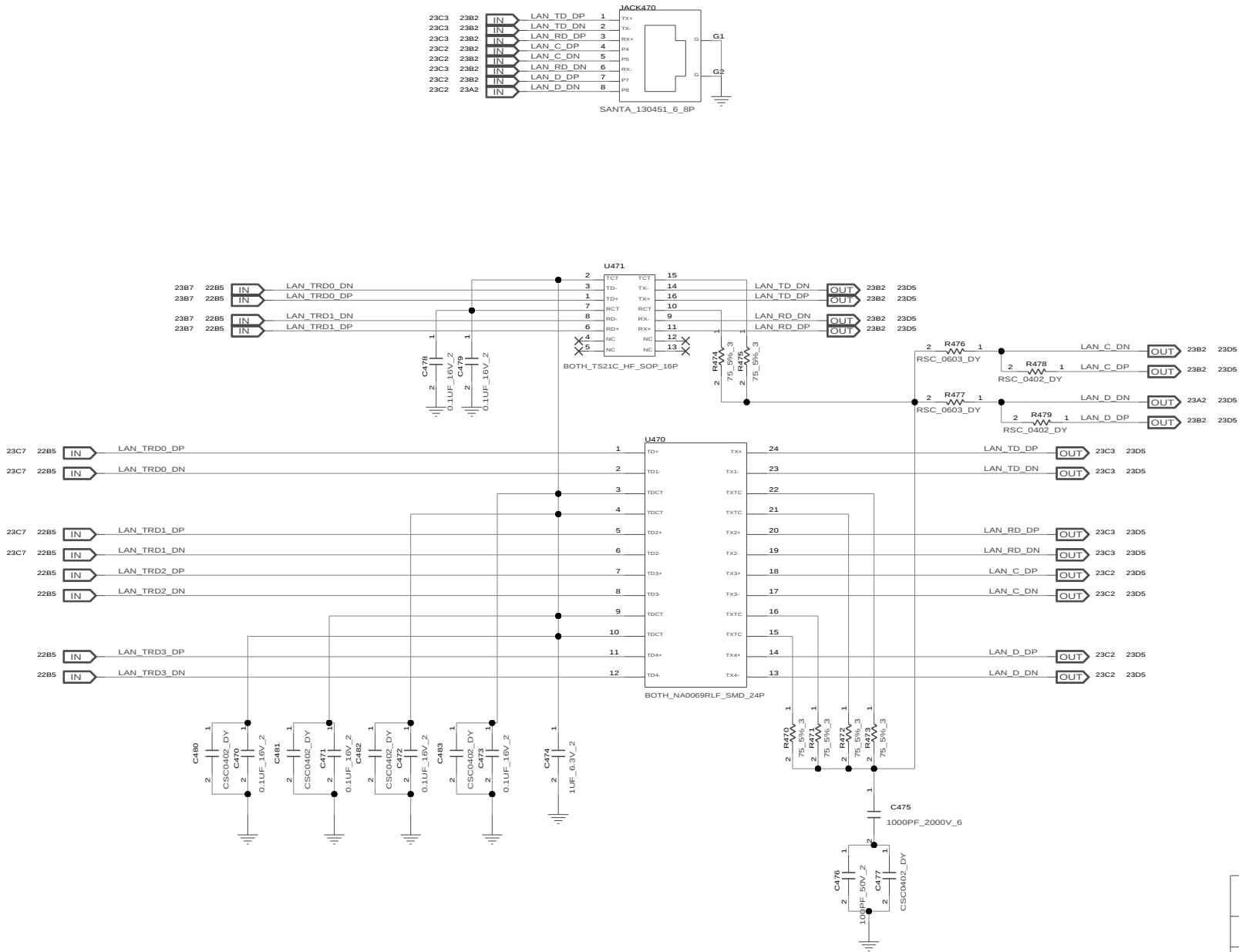
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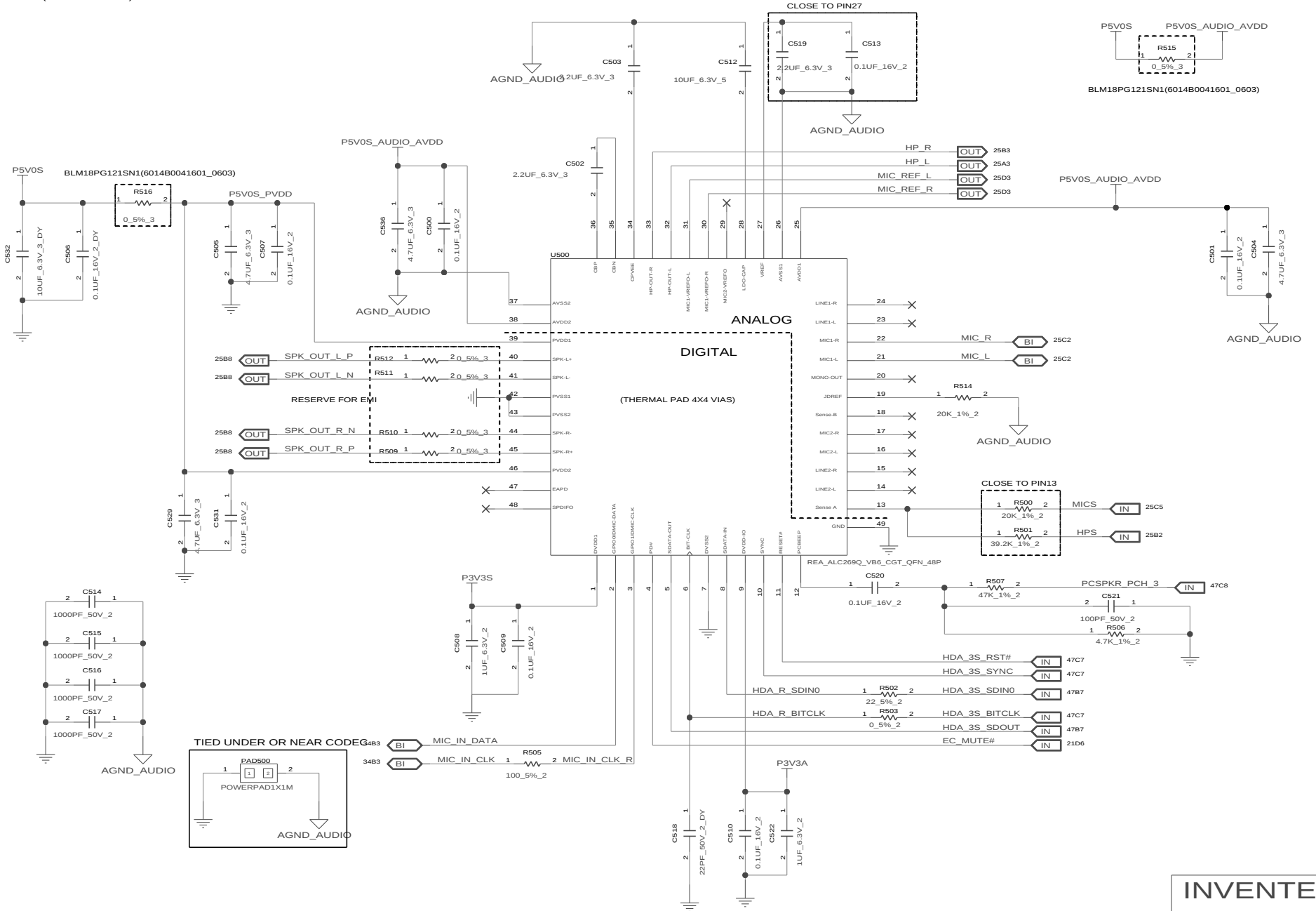
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REFERENCE 400~499(LAN)



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REFERENCE 500-549(AUDIO CODEC)



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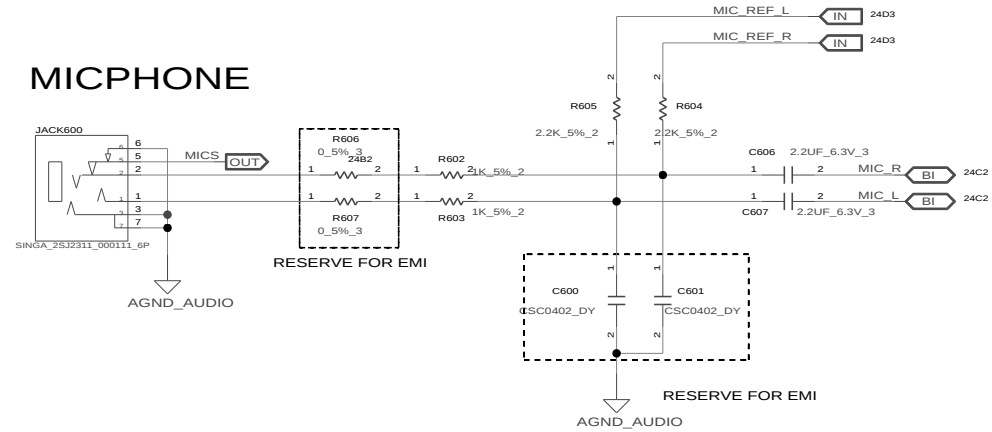
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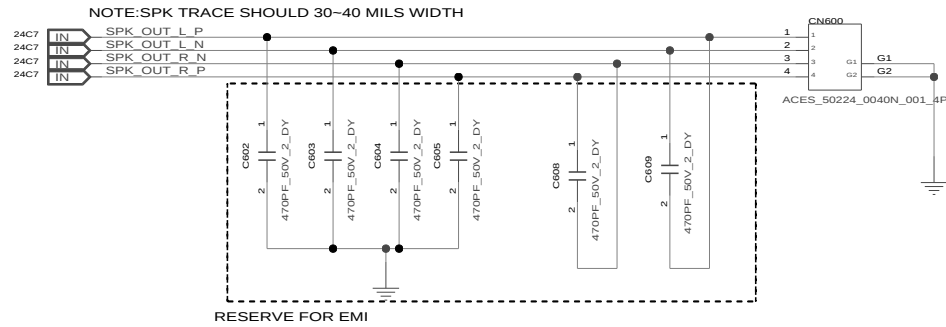
REFERCE 600~649(JACK/MIC/SPEAKER)

AUDIO JACKS

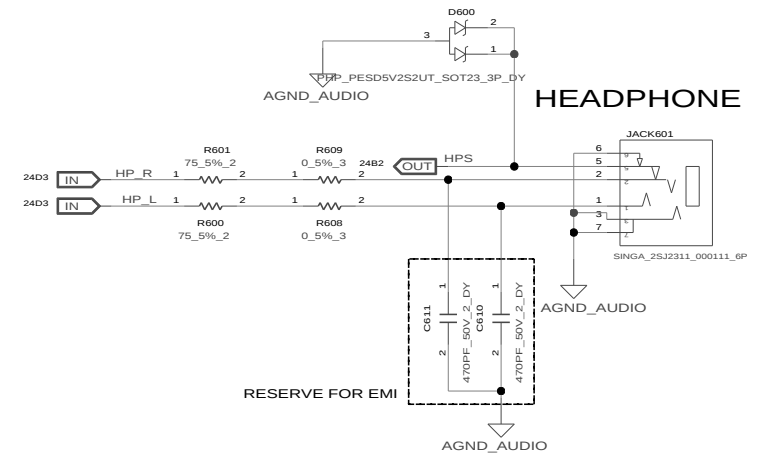
MICPHONE



INTERNAL SPEAKERS



HEADPHONE



INVENTEC

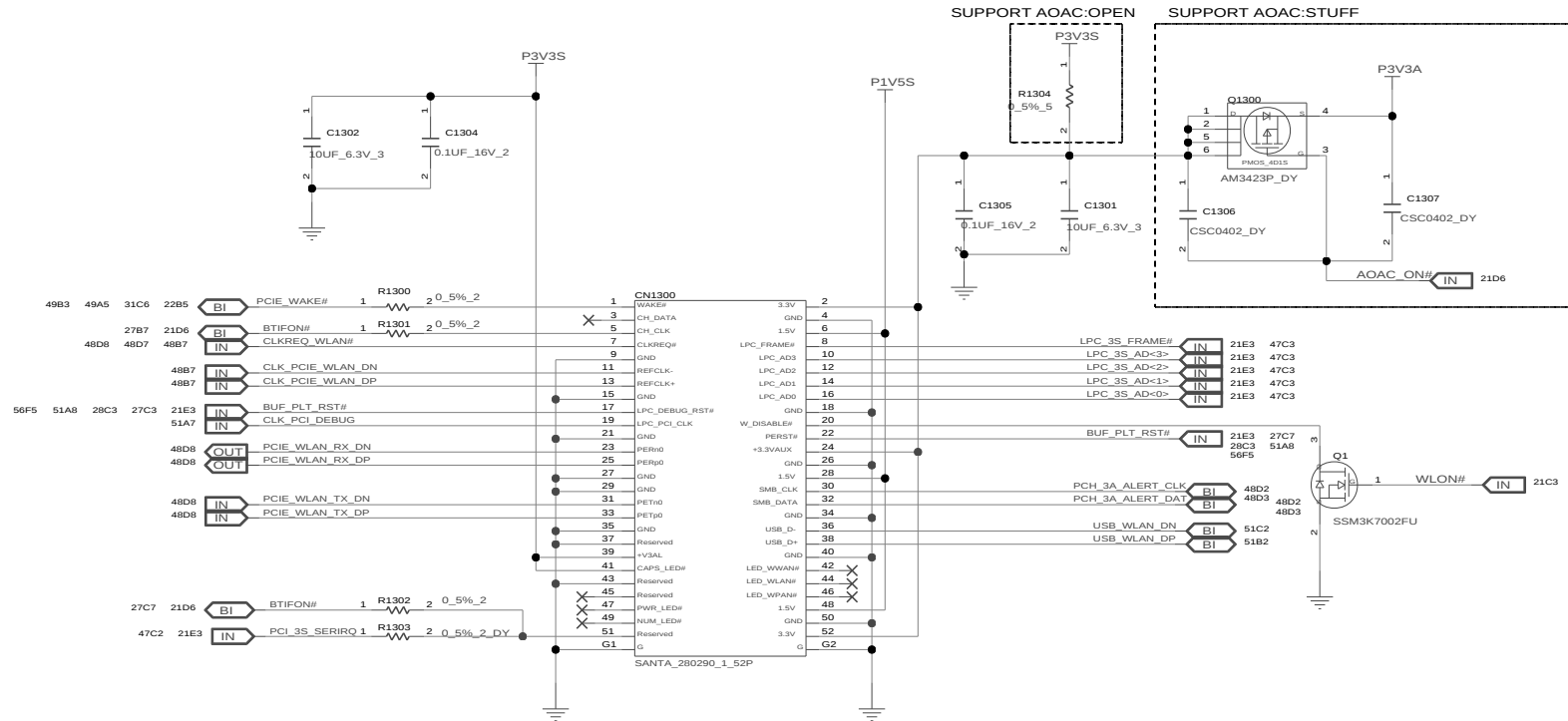
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REFERENCE 1300~1349(WLAN)



MINI CARD 1(WLAN)

INVENTEC

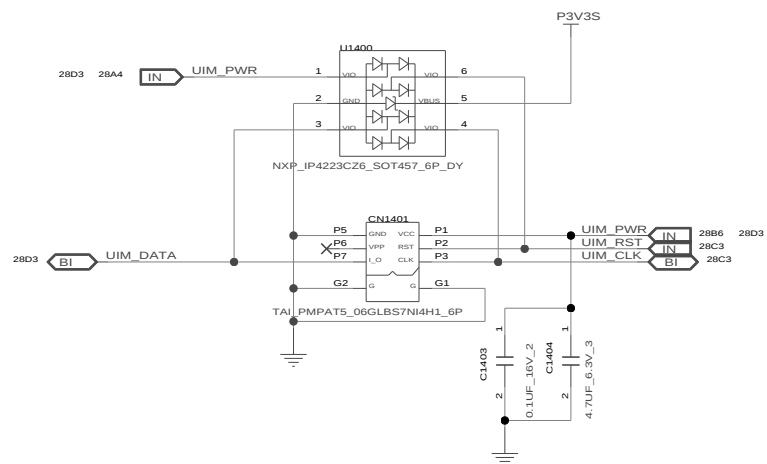
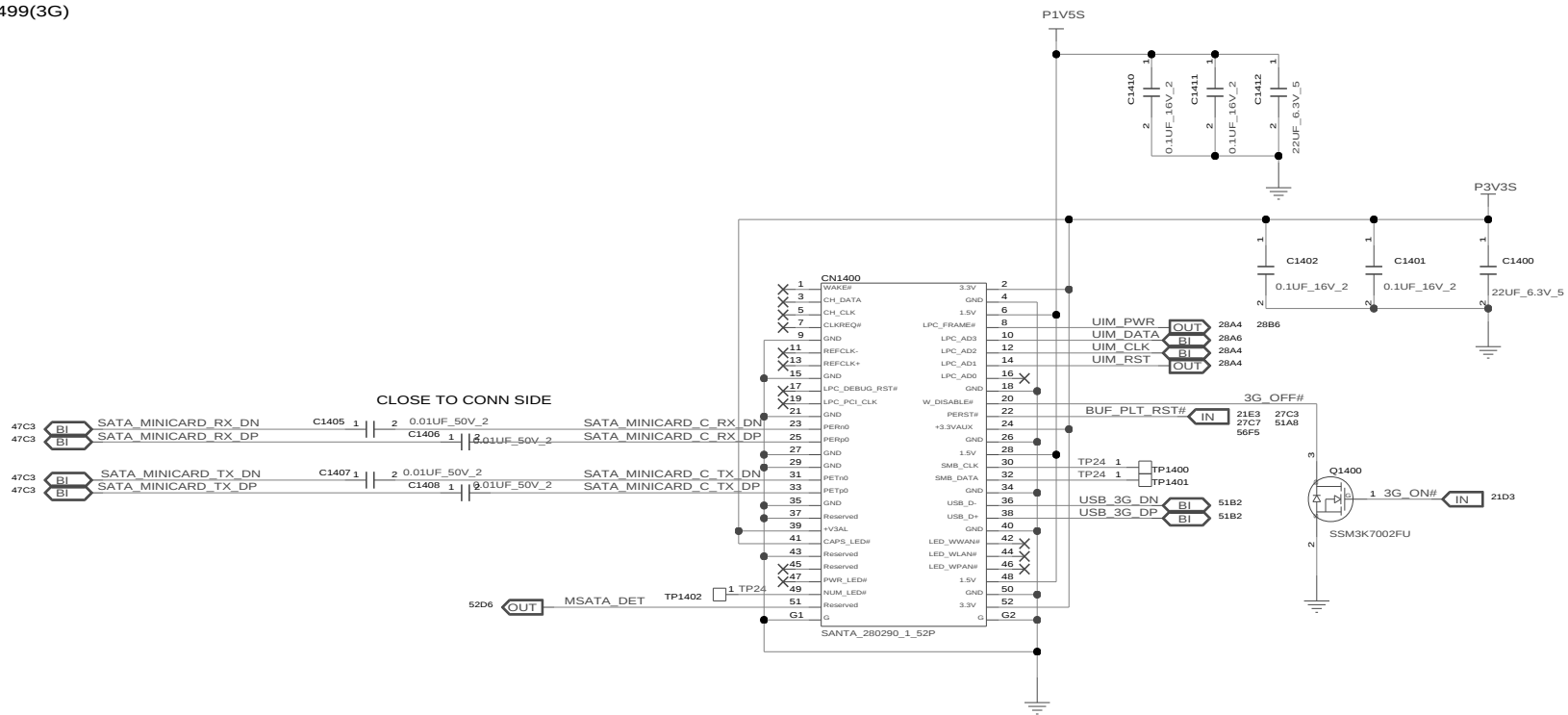
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REFERENCE 1400~1499(3G)



INVENTEC

TITLE
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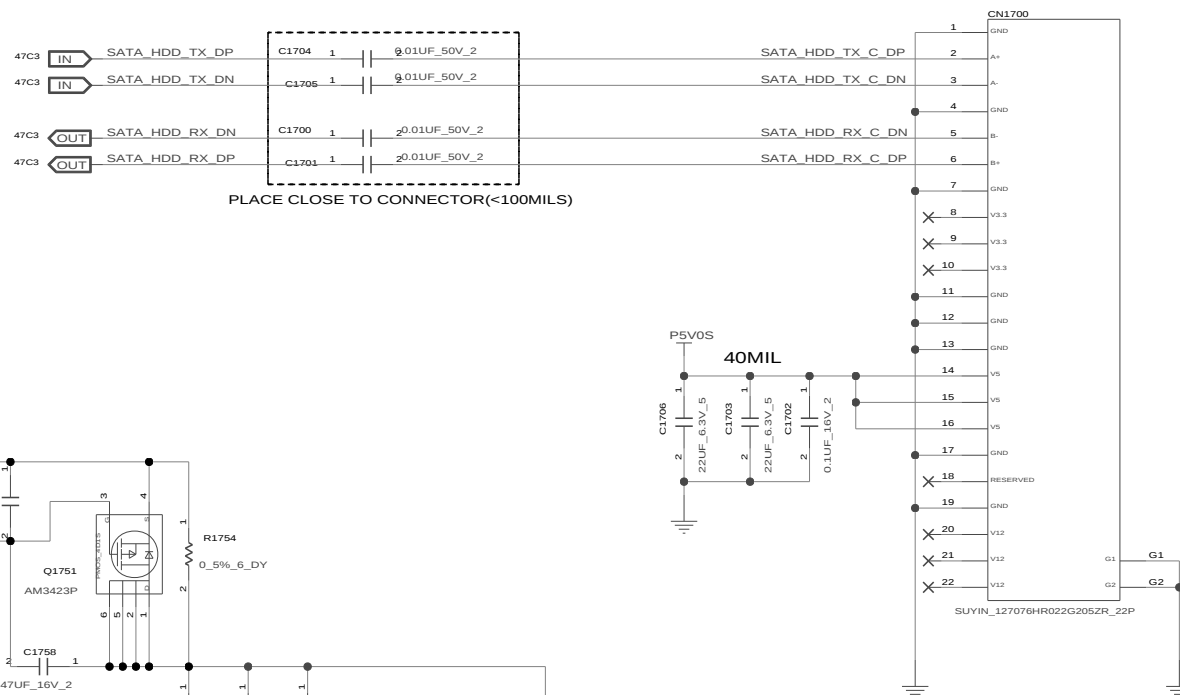
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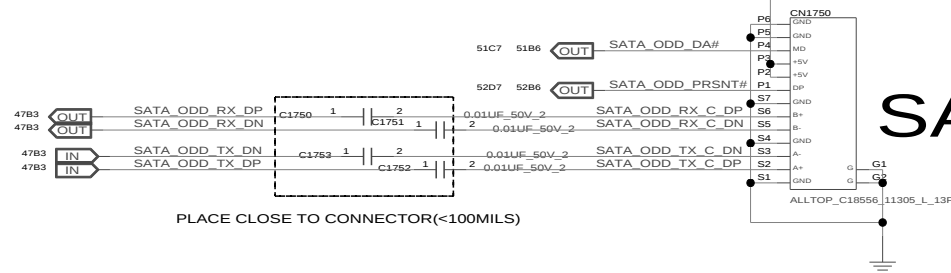
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REFERENCE 1700~1749(HDD)
REFERENCE 1750~1799(ODD)

SATA HDD



SATA ODD



INVENTEC

TITLE
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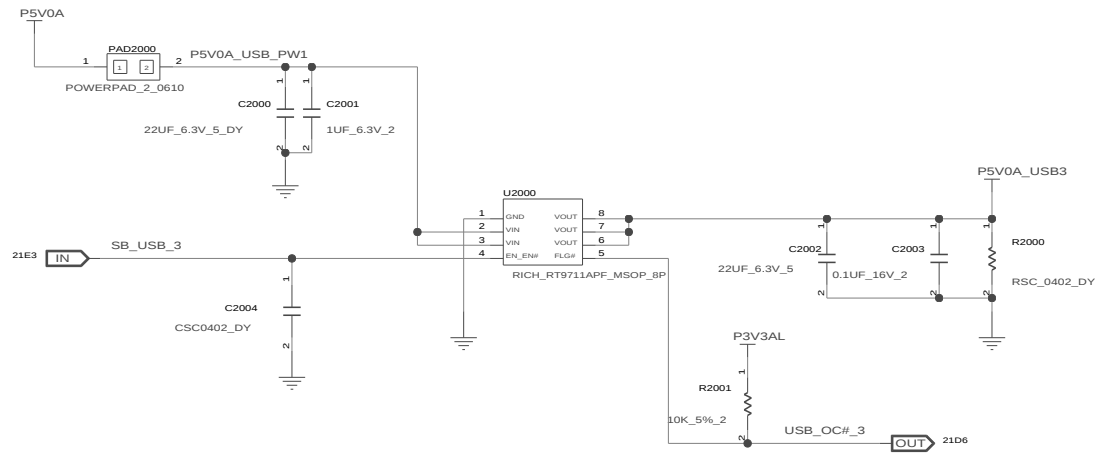
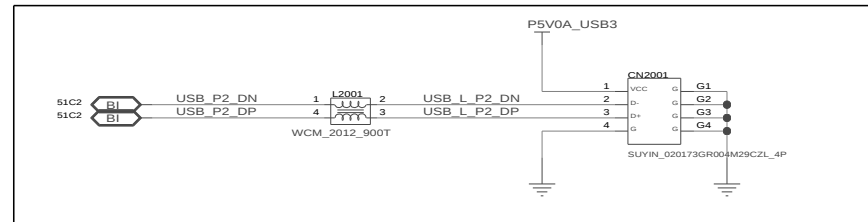
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REFERENCE 2000-2099(USB)

PLACEMENT @LEFT SIDE



INVENTEC

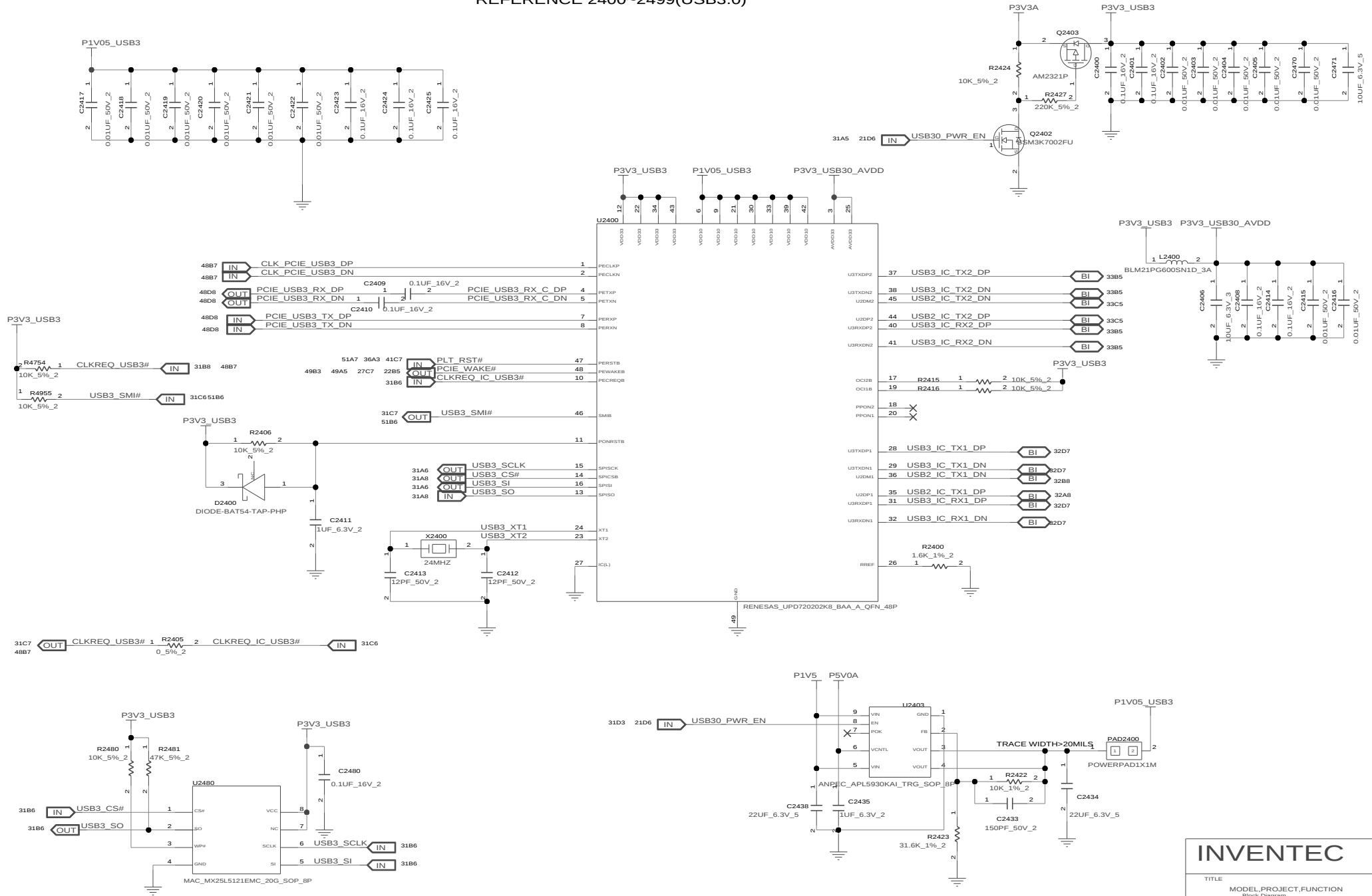
TITLE
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REFERENCE 2400-2499(USB3.0)



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REFERENCE 2400~2499(USB3.0)

USB3.0

USB 3.0 CONNECTOR

CTL1	CTL2	CTL3	Mode
0	0	X	Dedicated Charging Port, Auto-detect
0	1	X	Dedicated Charging Port, BC Specification 1.1 Only
1	0	X	Dedicated Charging Port, Apple Only
1	1	0	Standard Downstream Port, USB 2.0 Mode
1	1	1	Charging Downstream Port, BC Specification 1.1

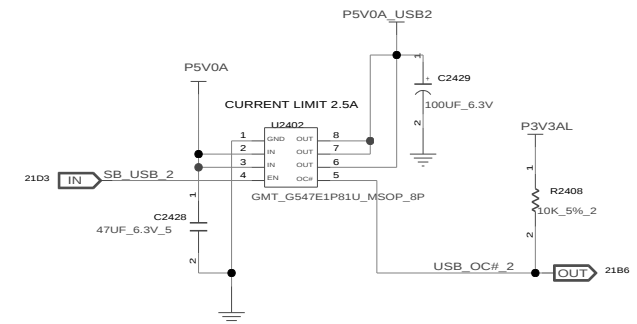
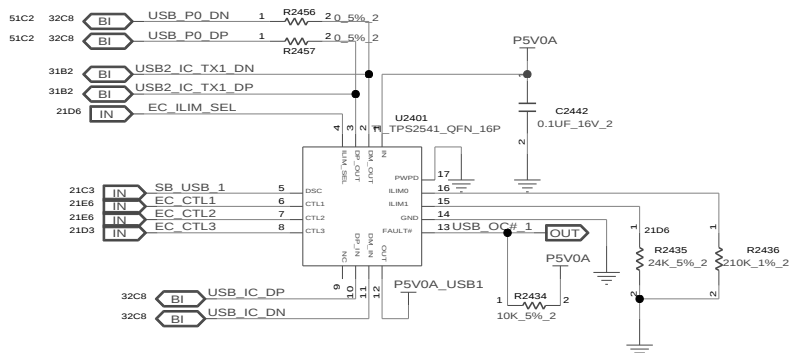
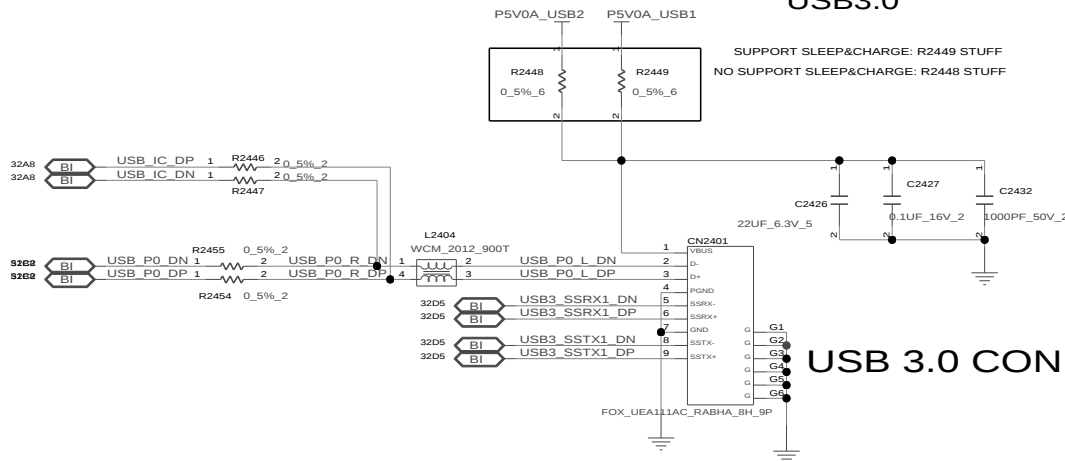
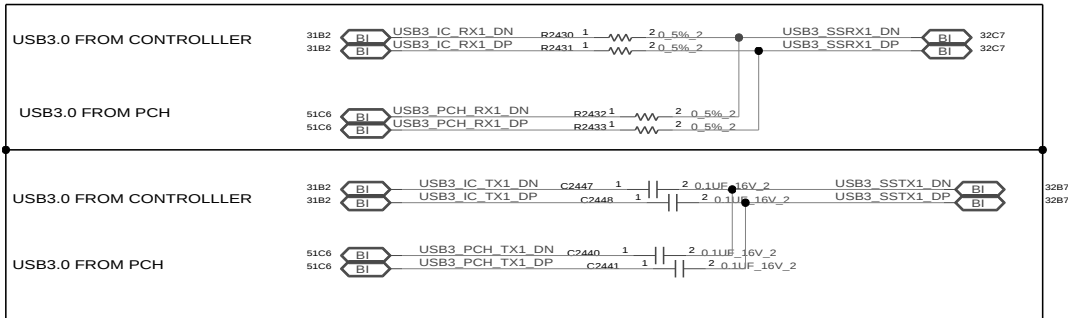
Table 3 – TPS2541 Control Truth Table

INVENTEC

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D



B

A

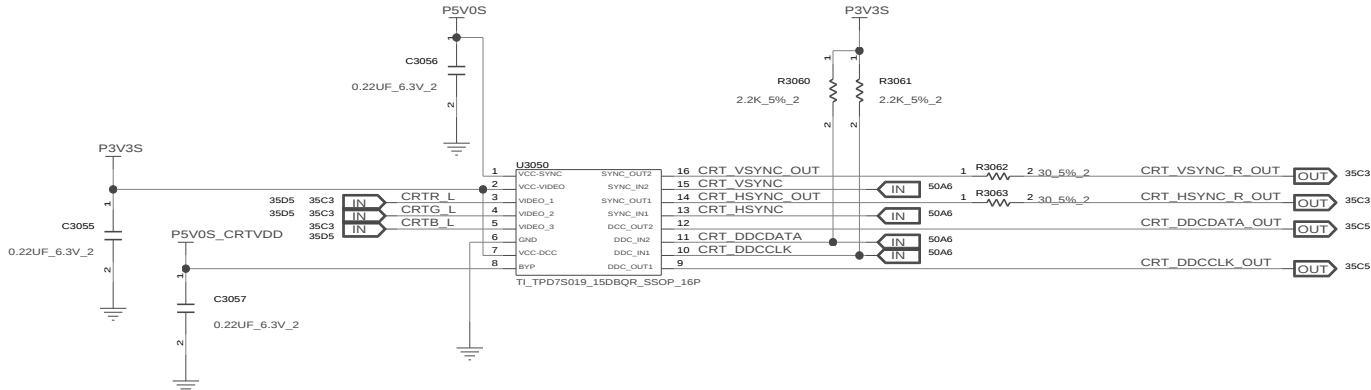
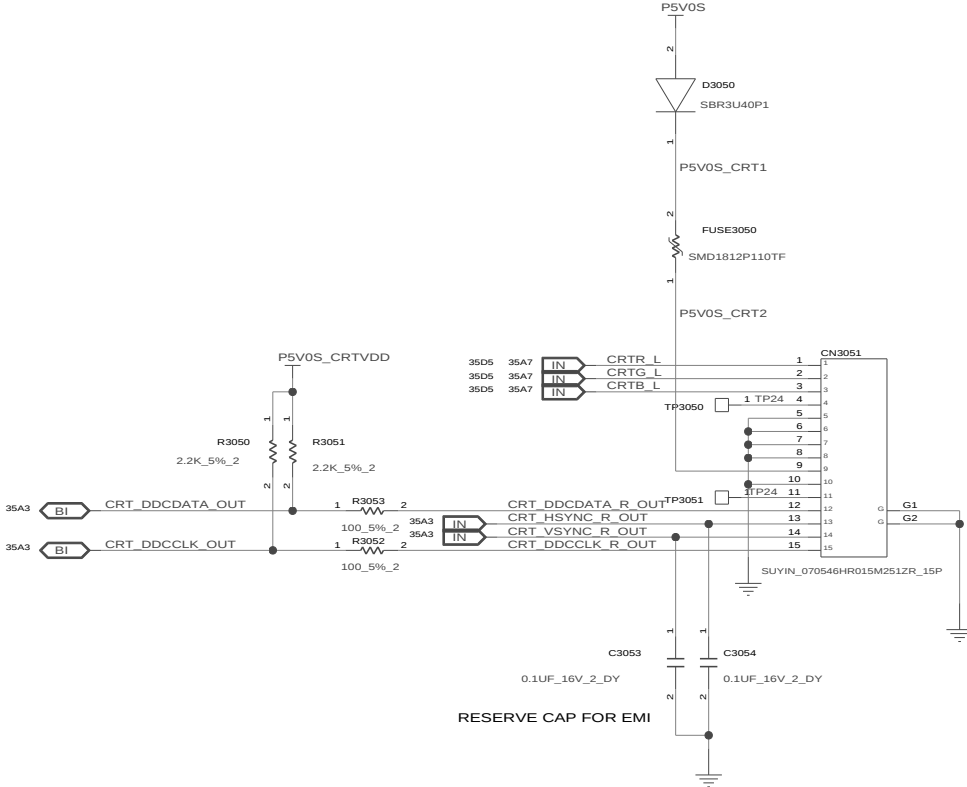
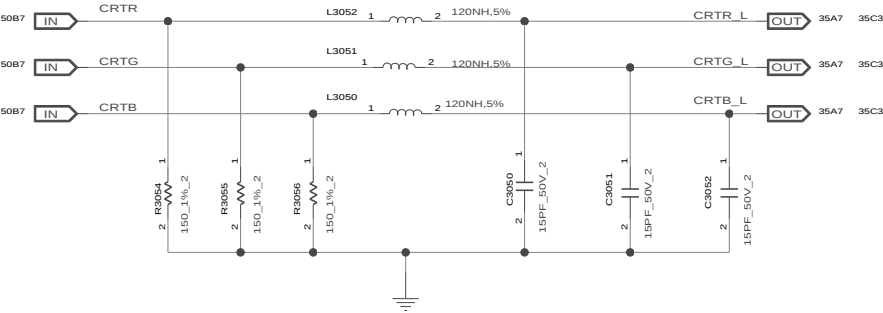
CHANGE by	xxx	DATE	31 OCT 2003	SHEET	33	of	66
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△



SHEET 34 of 66

REFERENCE 3050-3099(CRT)



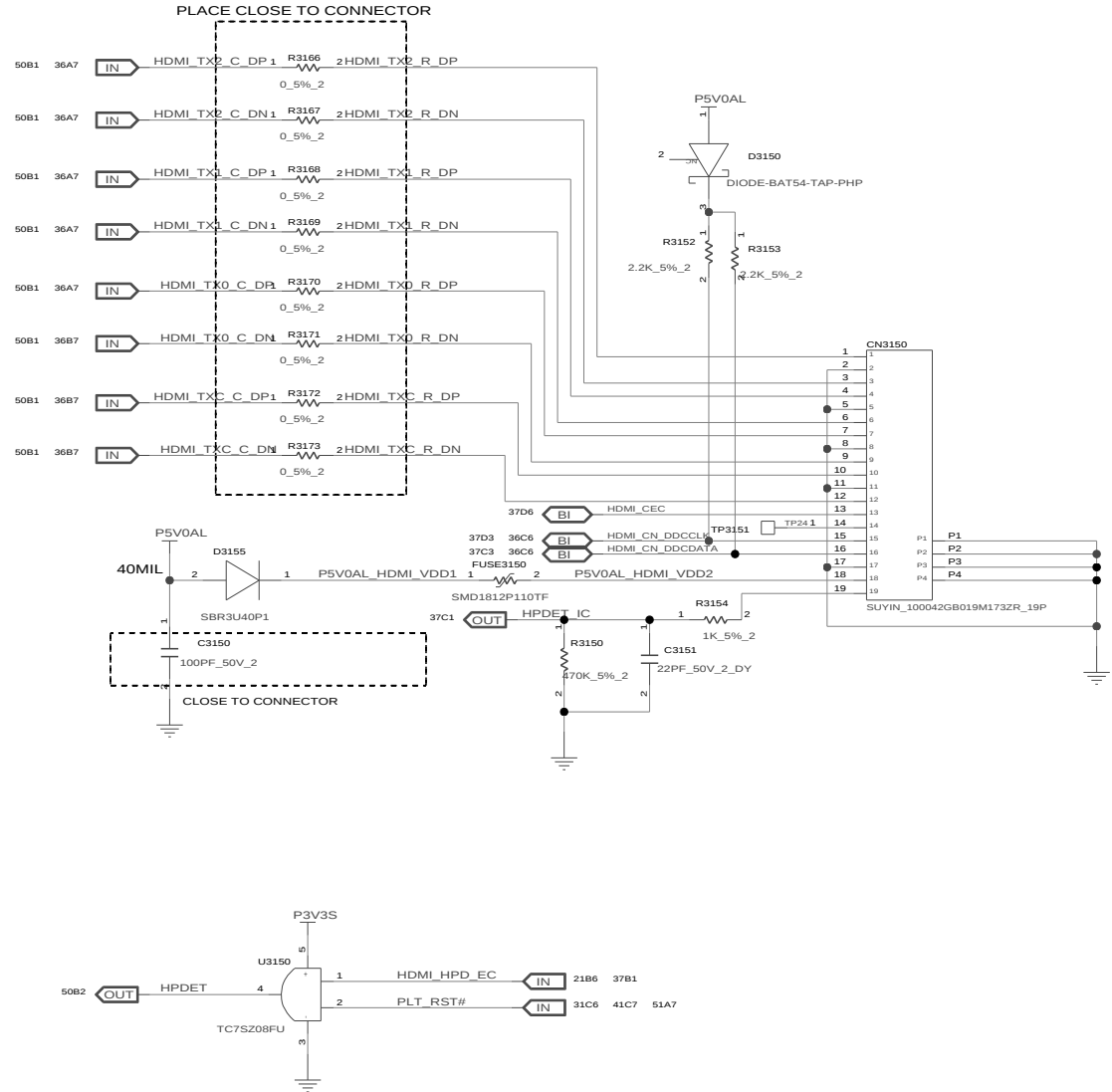
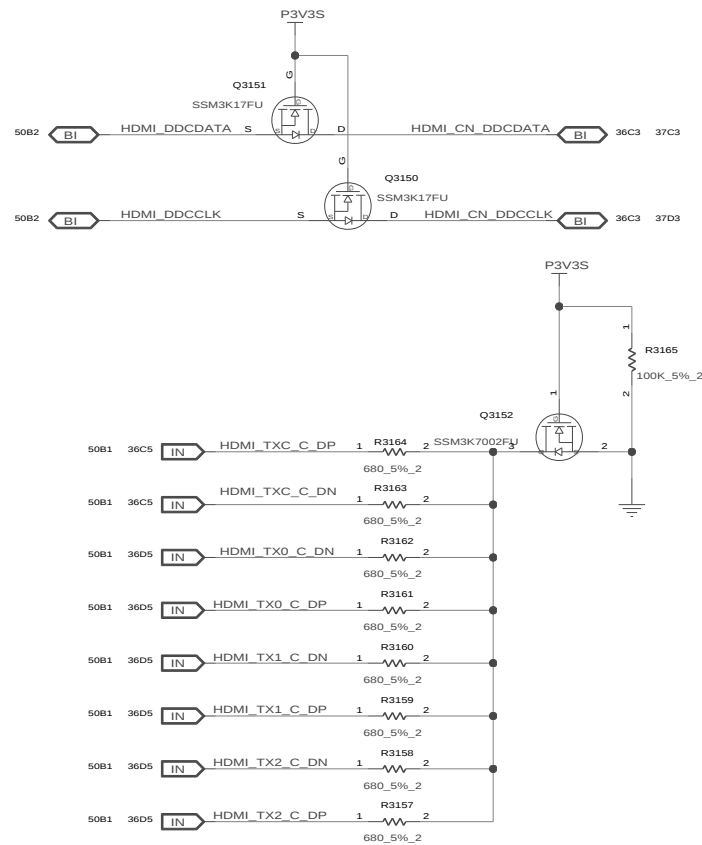
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 35 of 66

REFERENCE 3150~3199(HDMI)



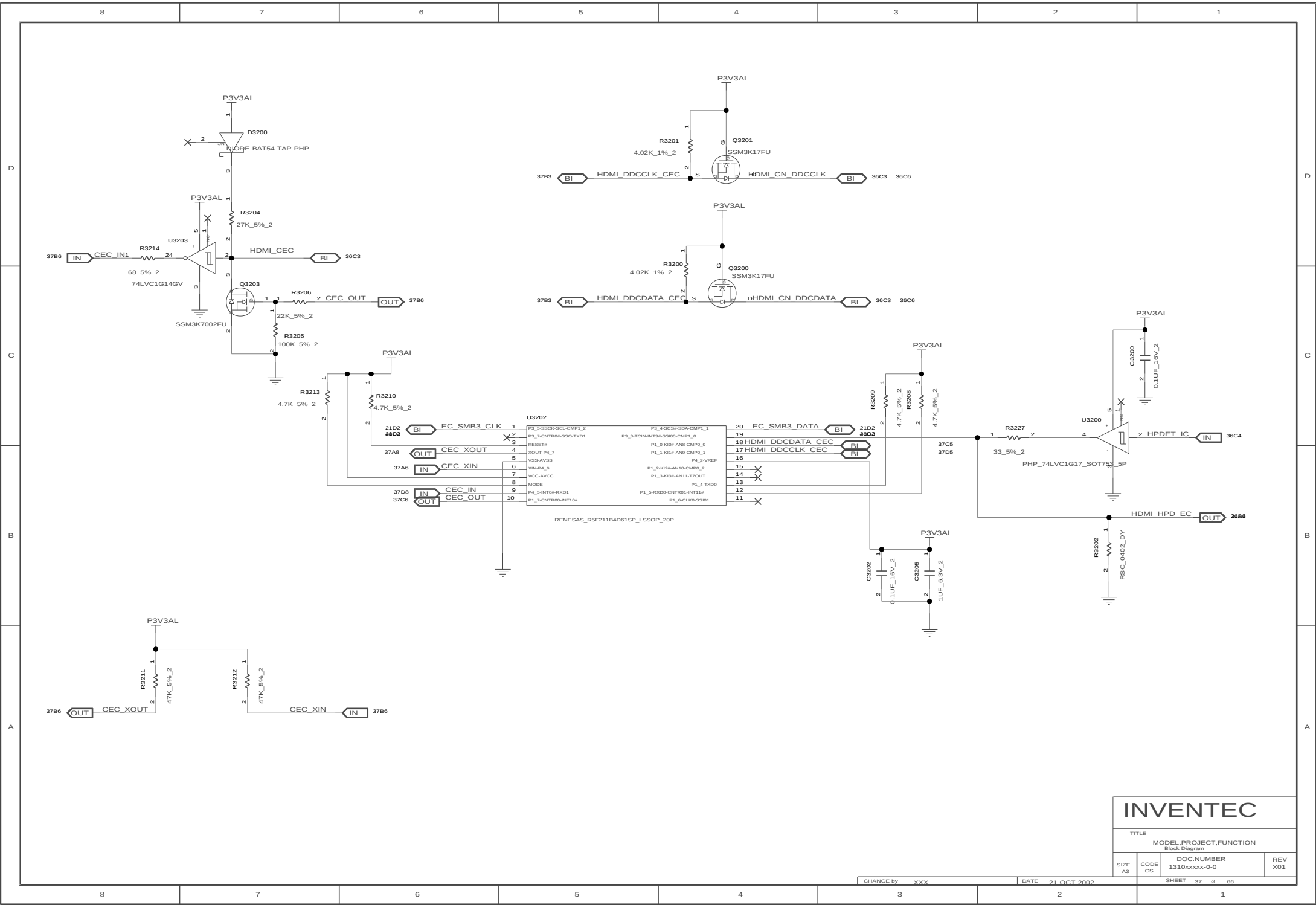
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3 CODE CS DOC.NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002

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INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3 CODE CS DOC.NUMBER 1310xxxx-0-0 REV X01

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SHEET 37 of 66

REFERENCE 4100~4299(DDR)

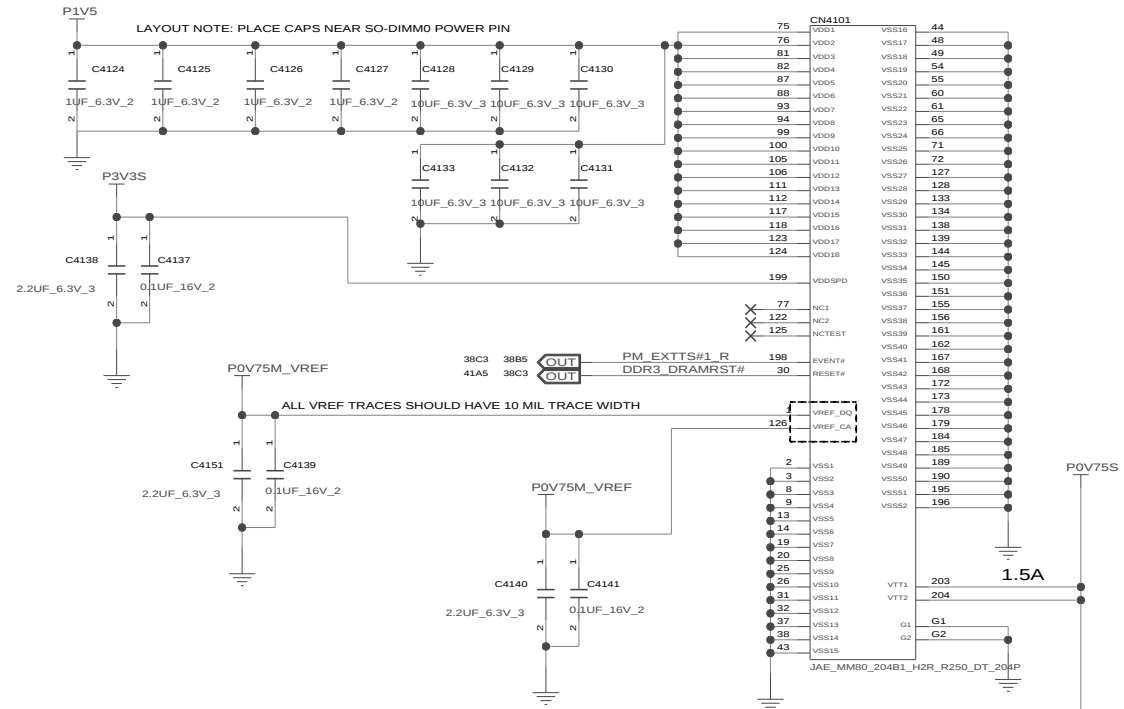


IF SA0_DIM0=0 , SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0XA0
SO-DIMMA TS ADDRESS IS 0X30 ¹



SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
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CHB

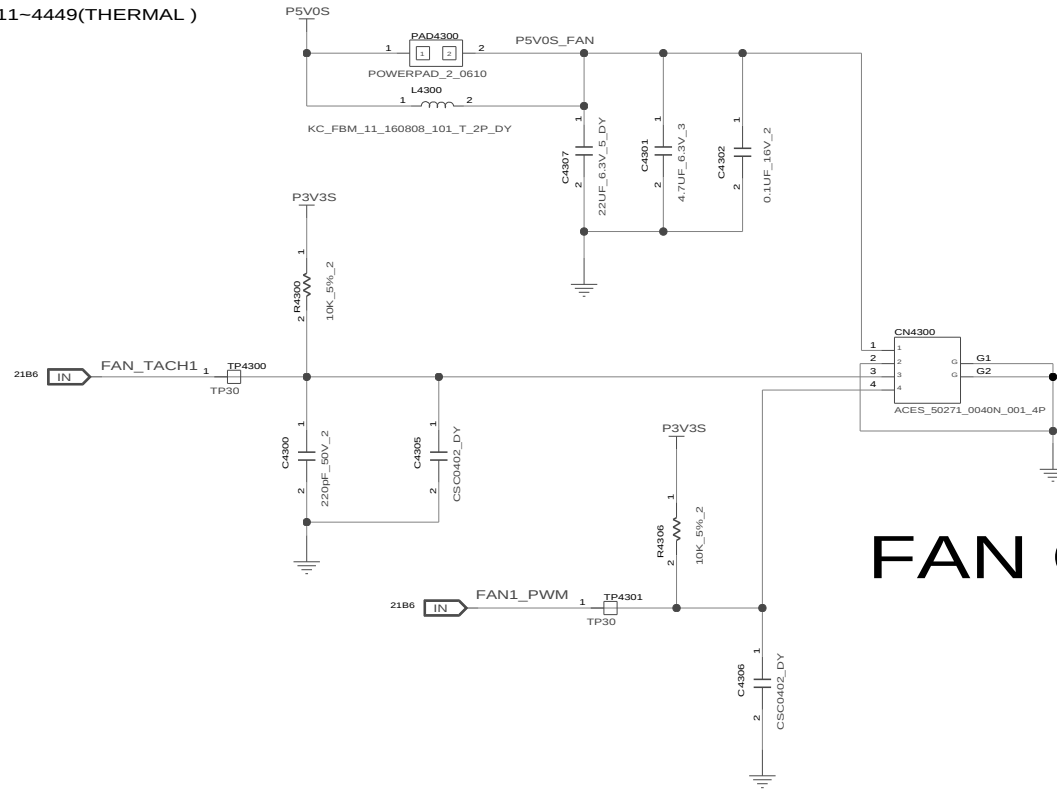


The diagram shows a parallel circuit with four branches. Each branch contains a capacitor labeled C4142, C4143, C4144, and C4145 respectively. Below each capacitor is the value $1\mu\text{F}_6.3\text{V}_2$. The circuit is enclosed in a dashed rectangular box.

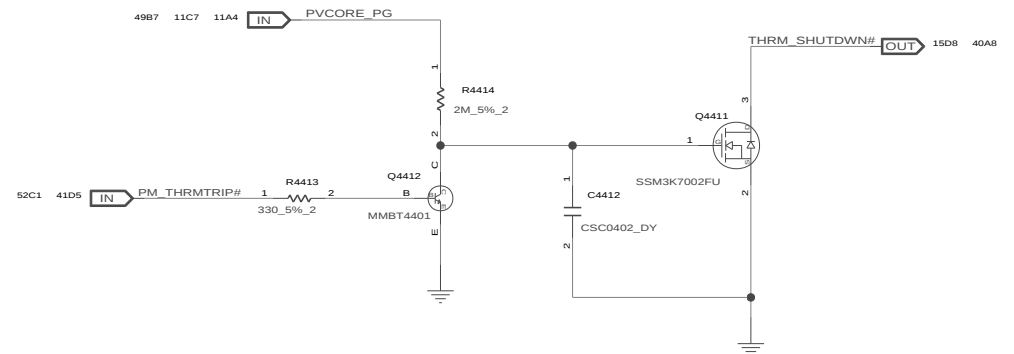
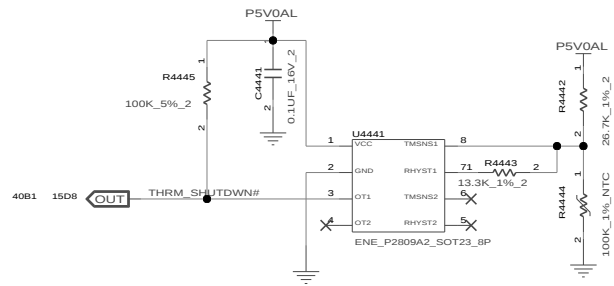
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 29 of 66			

REFERENCE 4300~4349(FAN)

REFERENCE 4411~4449(THERMAL)



FAN CN



INVENTEC

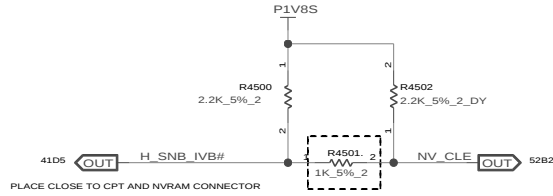
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01

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SHEET 40 of 66

REFERENCE 4500-4699(CPU)

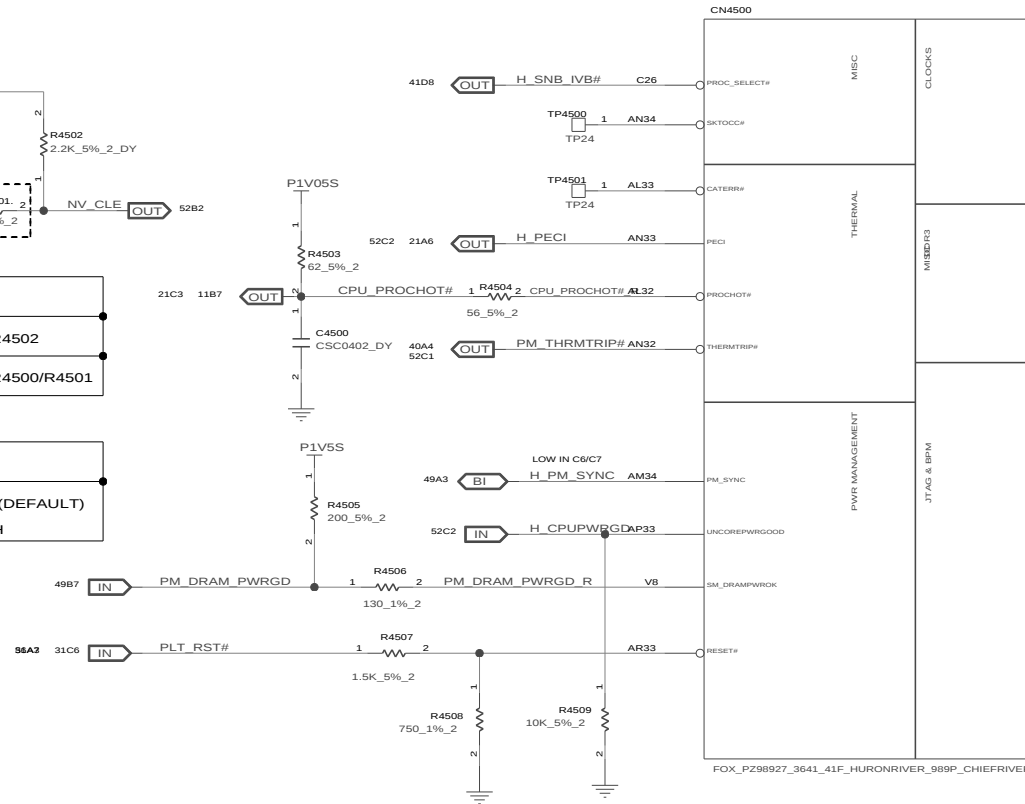


PROCESS STRAP SETTING

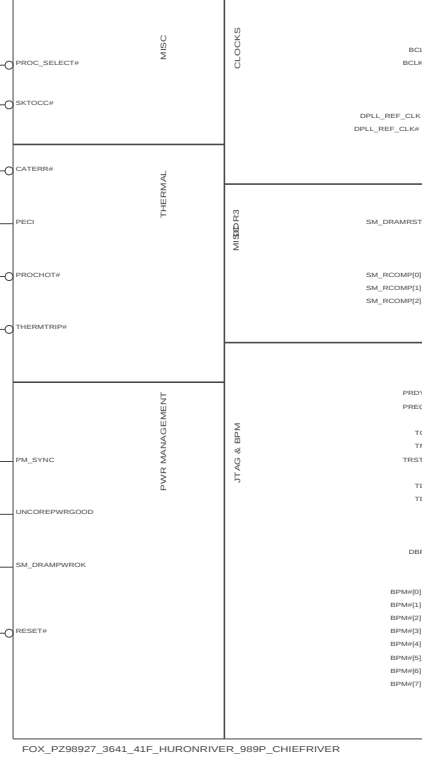
SANDY BRIDGE ONLY	STUFF R4502
SANDY BRIDGE/IVY BRIDGE	STUFF R4500/R4501

DMI&FDI TERMINATIONVOLTAGE

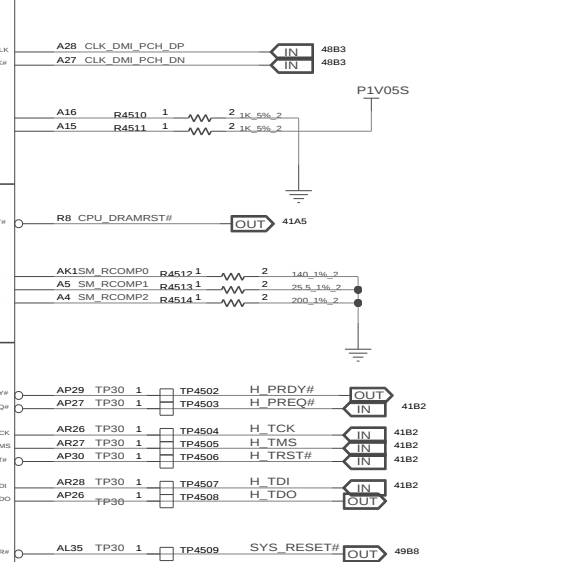
NV_CLE	SET TOVSS WHEN LOW(DEFAULT)
	SET TOVCC WHEN HIGH



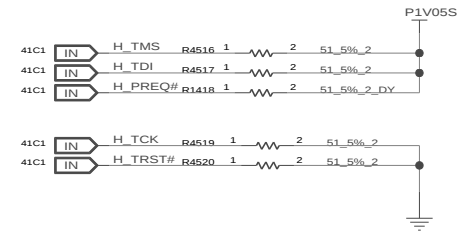
CN4500



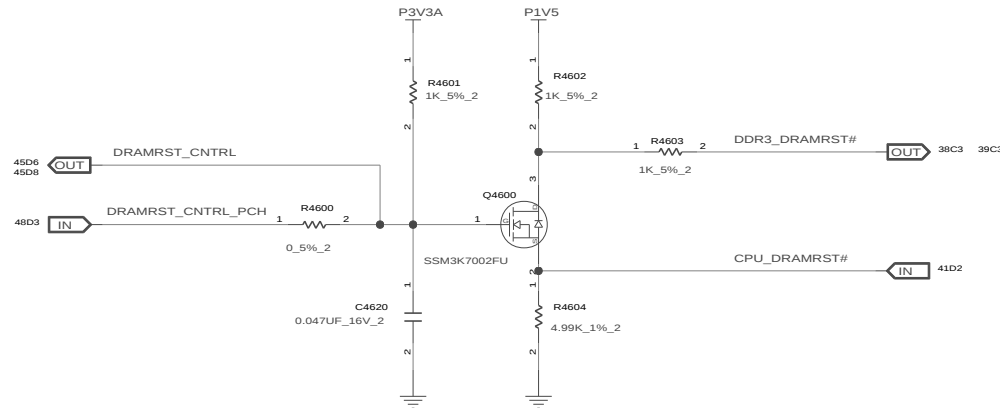
FOX_PZ98927_3641_41F_HURONRIVER_989P_CHIEFRIVER



CAD NOTE: ALL DDR_COMP SIGNALS SHOULD BE ROUTED SUCH TAHT
- MAX LENGTH = 500 MILS
- TRACE WIDTH = 15MILS AND
- MB TRACE IMPEDANCE < 68 MOHMS
(WORST CASE RESISTANCE)



S3 CIRCUIT: DRAM_RST# TO MEMORY SHOULD BE HIGH DURING S3



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002

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D



B

A



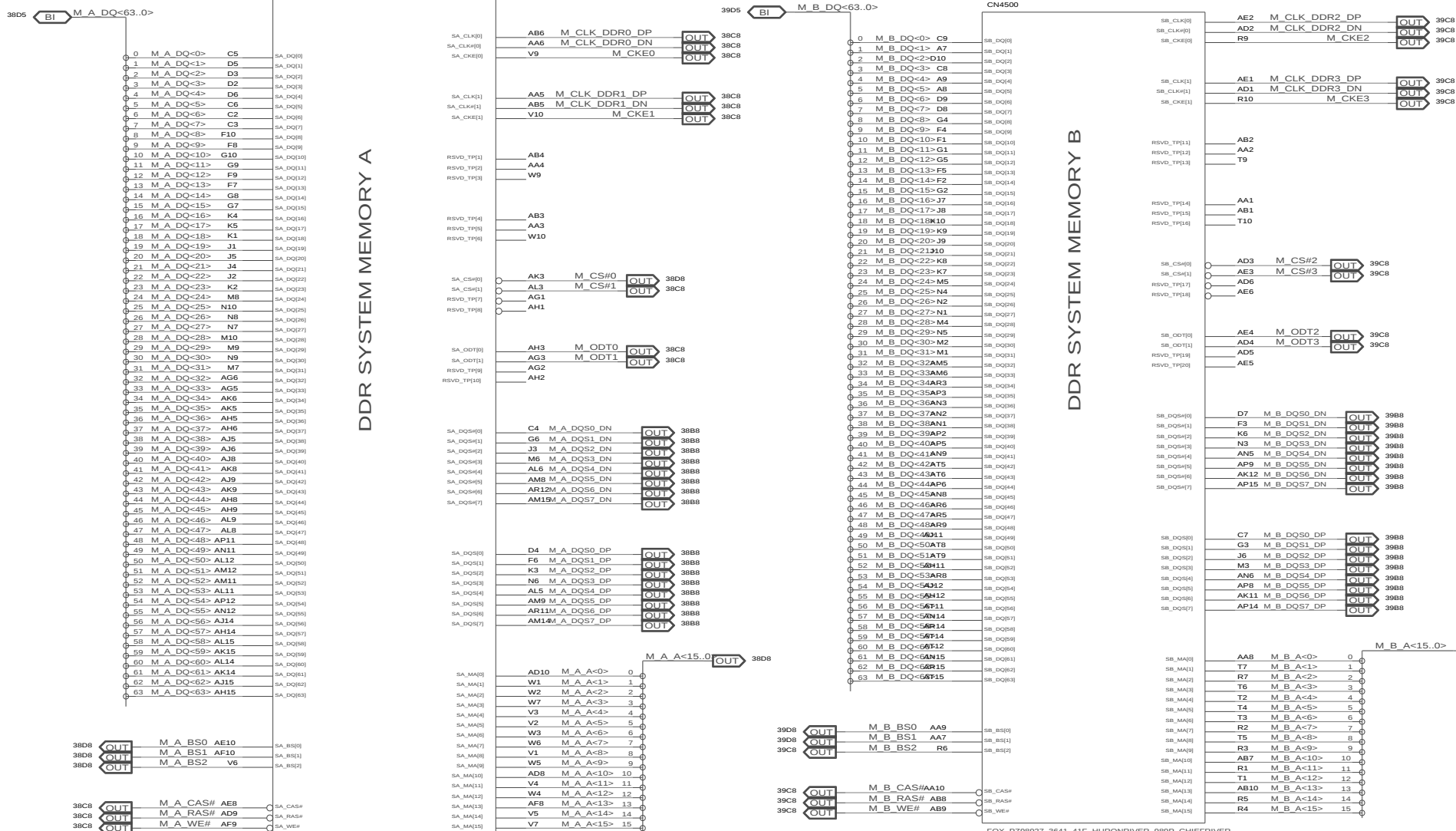
C

B

A

SOCKET.CPU.989P.TIN.3.0MM.STB.SMD.TR

CN4500



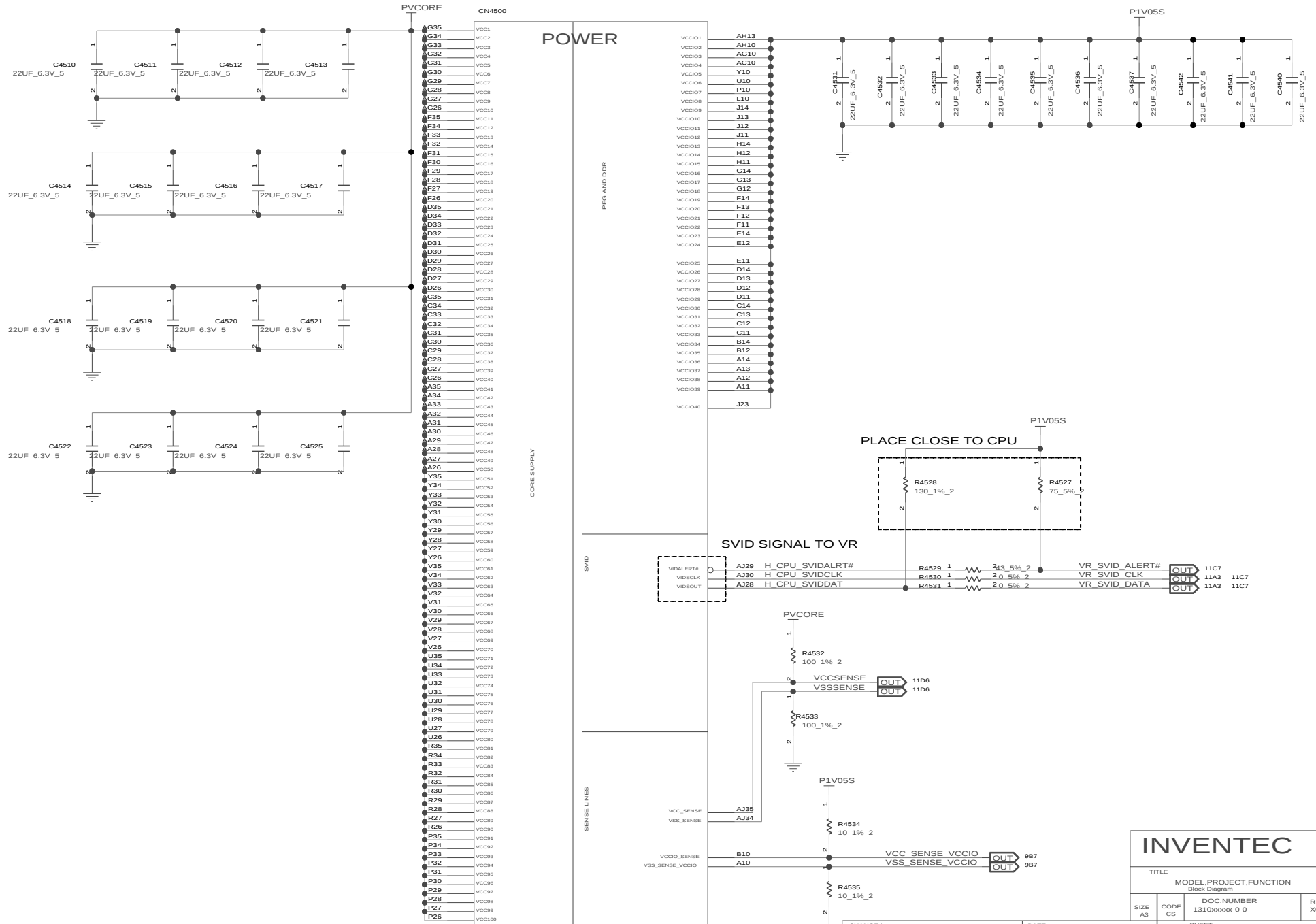
FOX PZ98927 3641 41F HURONRIVER 989P CHIEFRIVER

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION
	Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 43 of 66			

REFERENCE 4500~4699(CPU)



INVENTEC

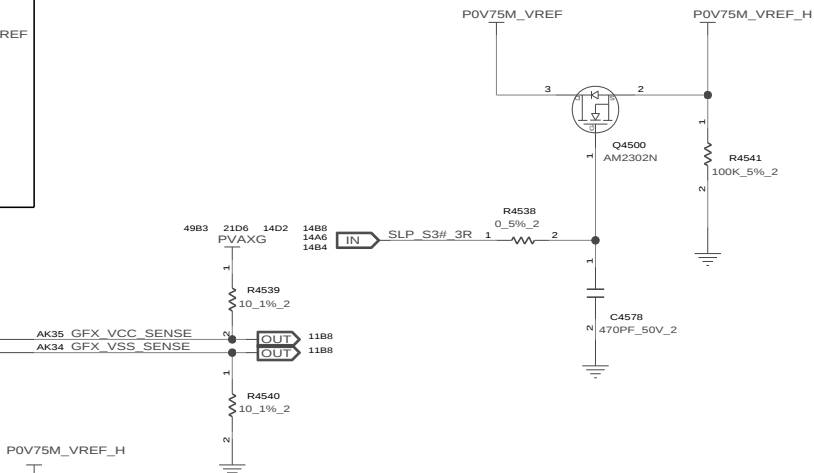
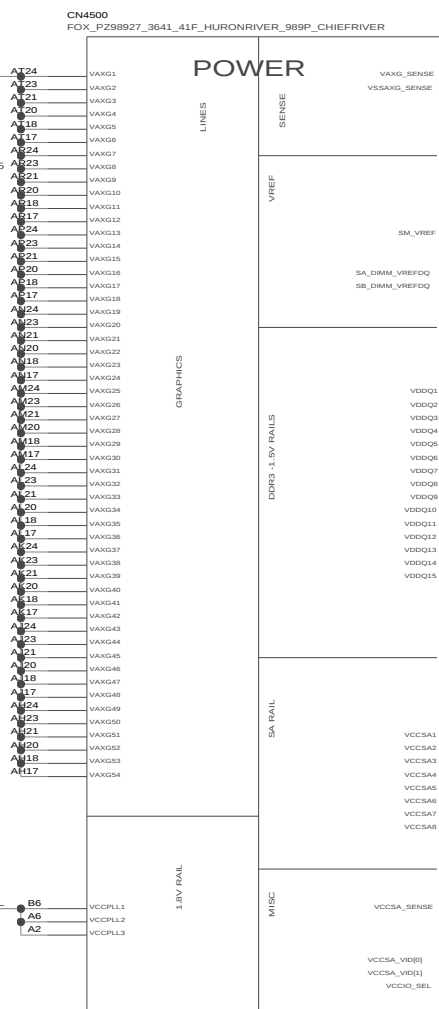
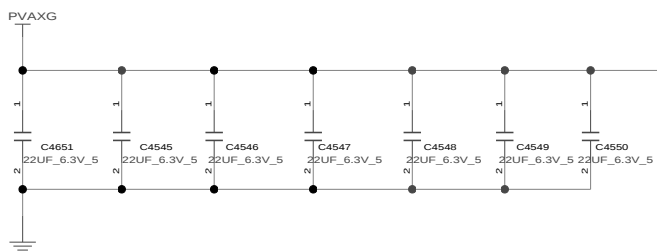
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE 00	CODE 00	DOC.NUMBER 1310xxxxx-0-0
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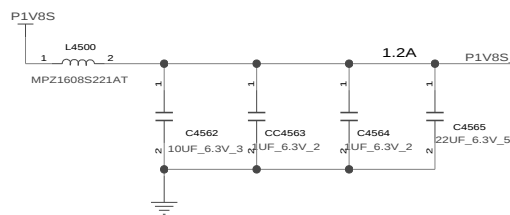
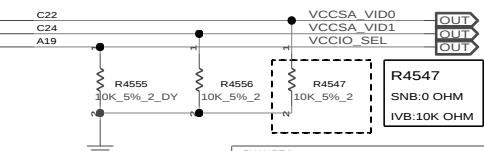
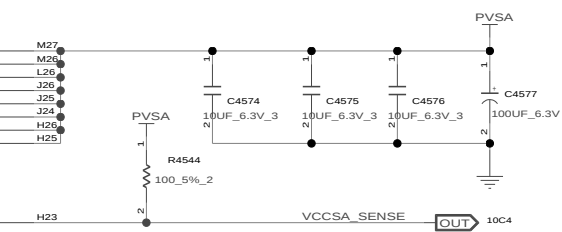
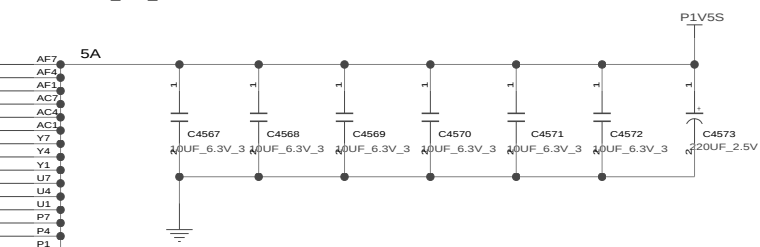
A3	C5	
SHEET 44 of 66		

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PROCESSOR DRIVEN VREF PATH WAS STUFFED BY DEFAULT:
ROUTE WITH MIN. TRACE WIDTH OF 10 MILS

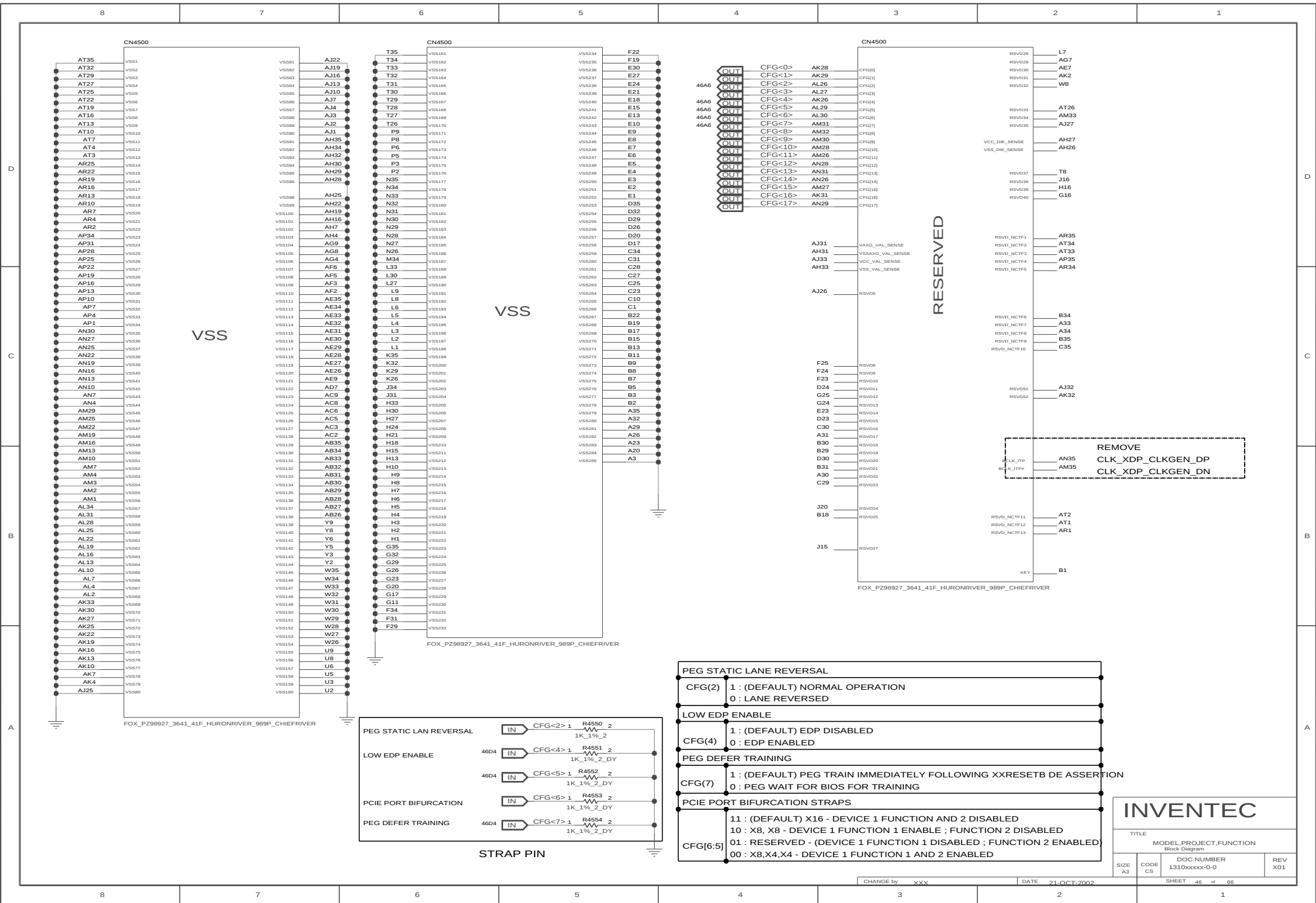


NOTE : DDR_WR_VREF SHOULD HAVE 20/20 MIL WHEREVER POSSIBLE



INVENTEC		
TITLE MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0
SHEET 45 of 66		

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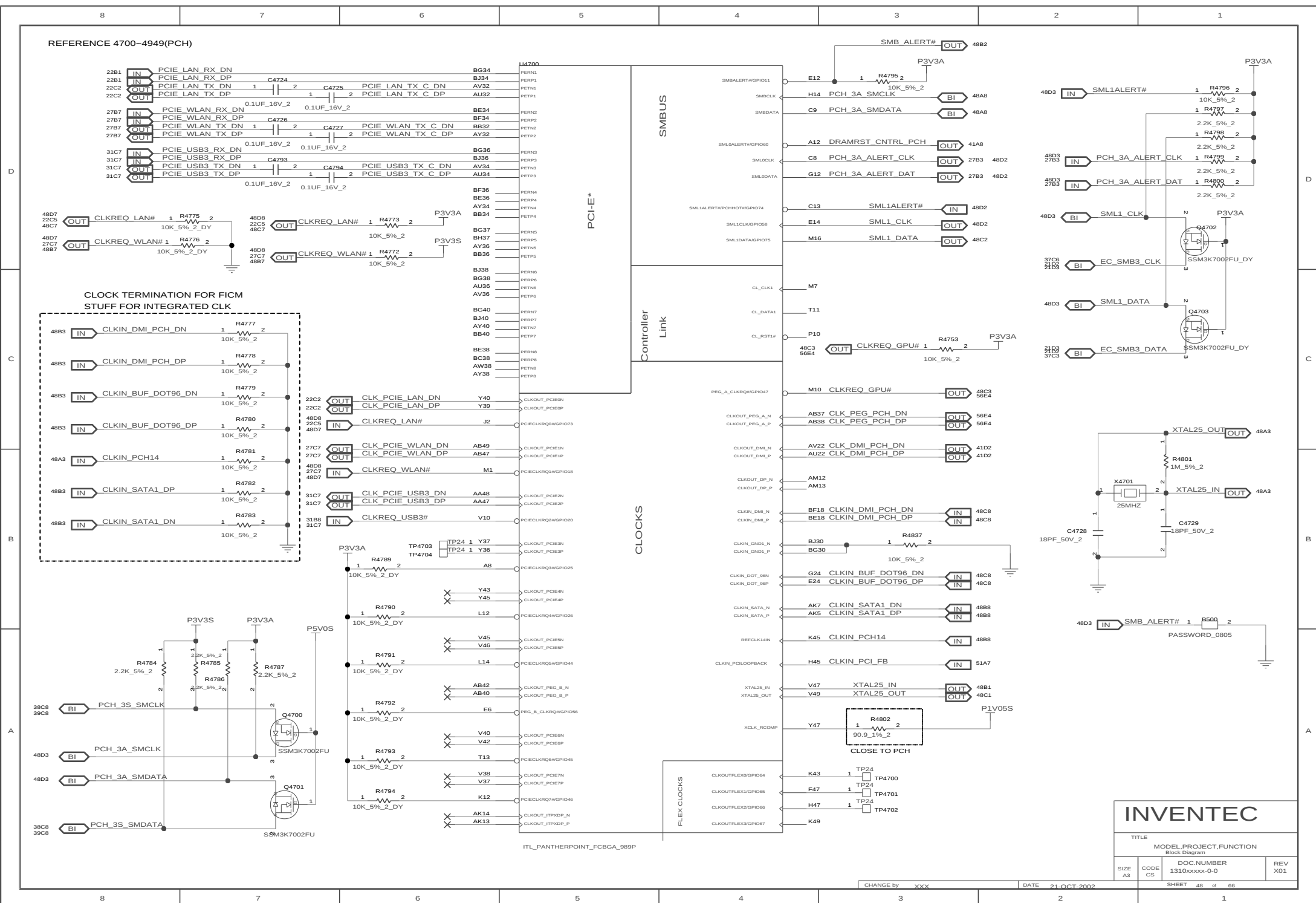


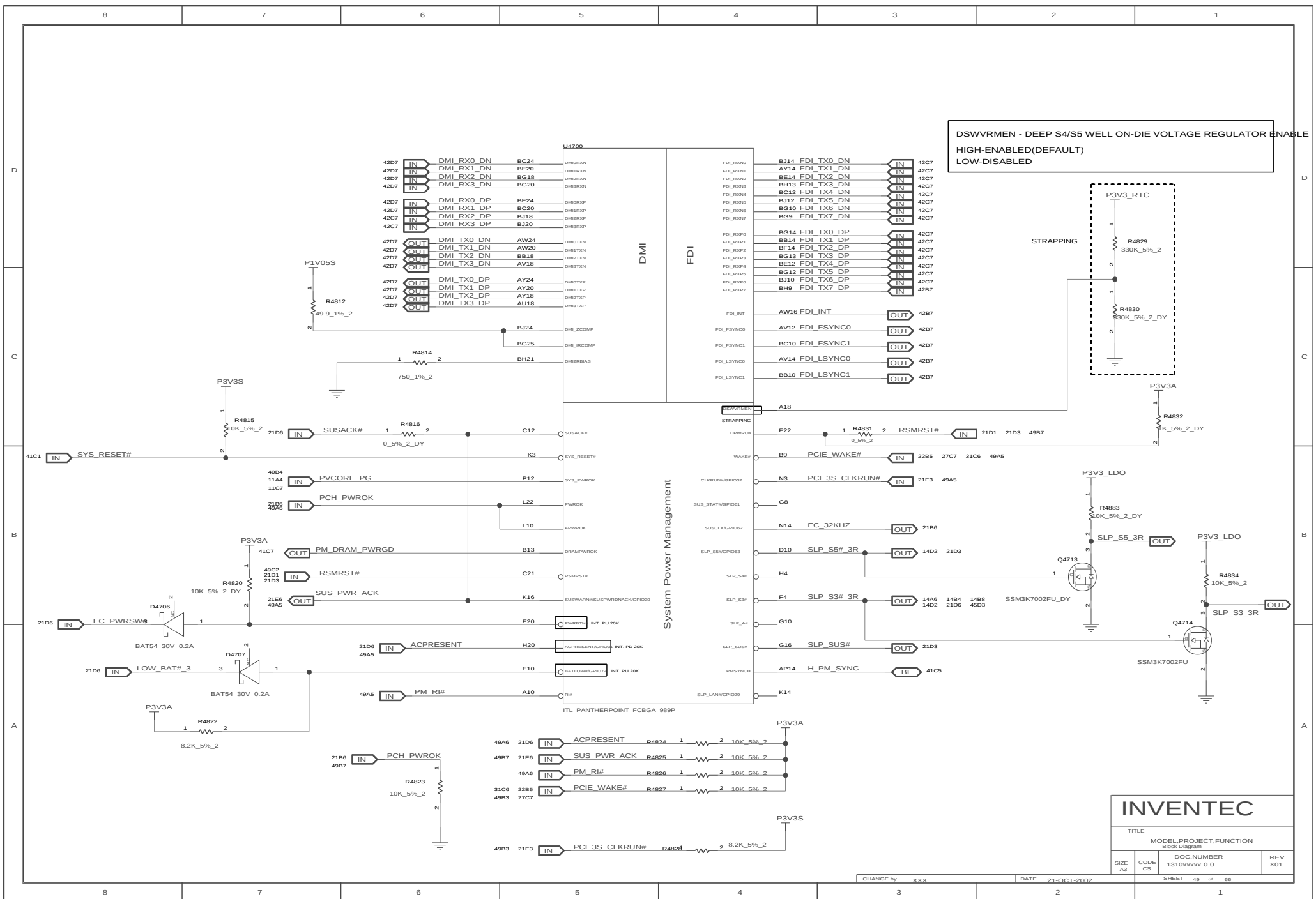
The schematic diagram illustrates the internal circuitry of the Intel Pantherpoint FCBGA 989P board. Key components and their connections include:

- Power Management:**
 - P3V3AL:** Input for the 3.3V ALM (Always Low Mode) supply.
 - P3V3_RTC:** Input for the 3.3V RTC supply.
 - P3V3S:** Input for the 3.3V SDRAM supply.
 - Resistors:** R4700 (1K_1%_2), R4703 (20K_1%_2), R4704 (20K_1%_2), R4707 (30K_5%_3), R4708 (10M_5%_2), R4709 (33_5%_2), R4710 (33_5%_2), R4711 (33_5%_2), R4712 (33_5%_2), R4713 (33_5%_2), R4714 (1K_5%_2), R4715 (1K_5%_2), R4716 (33_5%_2), R4717 (1K_5%_2), R4718 (1K_5%_2), R4719 (1K_5%_2), R4720 (10K_5%_2), R4721 (37_4_1%_2), R4722 (49_9_1%_2), R4723 (10K_5%_2), R4724 (10K_5%_2), R4725 (10K_5%_2), R4726 (10K_5%_2), R4727 (10K_5%_2), R4728 (10K_5%_2), R4729 (10K_5%_2), R4730 (10K_5%_2), R4731 (10K_5%_2), R4732 (10K_5%_2), R4733 (10K_5%_2), R4734 (10K_5%_2), R4735 (10K_5%_2), R4736 (10K_5%_2), R4737 (10K_5%_2), R4738 (10K_5%_2), R4739 (10K_5%_2), R4740 (10K_5%_2), R4741 (10K_5%_2), R4742 (10K_5%_2), R4743 (10K_5%_2), R4744 (10K_5%_2), R4745 (10K_5%_2), R4746 (10K_5%_2), R4747 (10K_5%_2), R4748 (10K_5%_2), R4749 (10K_5%_2), R4750 (10K_5%_2), R4751 (10K_5%_2), R4752 (10K_5%_2), R4753 (10K_5%_2), R4754 (10K_5%_2), R4755 (10K_5%_2), R4756 (10K_5%_2), R4757 (10K_5%_2), R4758 (10K_5%_2), R4759 (10K_5%_2), R4760 (10K_5%_2), R4761 (10K_5%_2), R4762 (10K_5%_2), R4763 (10K_5%_2), R4764 (10K_5%_2), R4765 (10K_5%_2), R4766 (10K_5%_2), R4767 (10K_5%_2), R4768 (10K_5%_2), R4769 (10K_5%_2), R4770 (10K_5%_2), R4771 (10K_5%_2), R4772 (10K_5%_2), R4773 (10K_5%_2), R4774 (10K_5%_2), R4775 (10K_5%_2), R4776 (10K_5%_2), R4777 (10K_5%_2), R4778 (10K_5%_2), R4779 (10K_5%_2), R4780 (10K_5%_2), R4781 (10K_5%_2), R4782 (10K_5%_2), R4783 (10K_5%_2), R4784 (10K_5%_2), R4785 (10K_5%_2), R4786 (10K_5%_2), R4787 (10K_5%_2), R4788 (10K_5%_2), R4789 (10K_5%_2), R4790 (10K_5%_2), R4791 (10K_5%_2), R4792 (10K_5%_2), R4793 (10K_5%_2), R4794 (10K_5%_2), R4795 (10K_5%_2), R4796 (10K_5%_2), R4797 (10K_5%_2), R4798 (10K_5%_2), R4799 (10K_5%_2), R4800 (10K_5%_2), R4801 (10K_5%_2), R4802 (10K_5%_2), R4803 (10K_5%_2), R4804 (10K_5%_2), R4805 (10K_5%_2), R4806 (10K_5%_2), R4807 (10K_5%_2), R4808 (10K_5%_2), R4809 (10K_5%_2), R4810 (10K_5%_2), R4811 (10K_5%_2), R4812 (10K_5%_2), R4813 (10K_5%_2), R4814 (10K_5%_2), R4815 (10K_5%_2), R4816 (10K_5%_2), R4817 (10K_5%_2), R4818 (10K_5%_2), R4819 (10K_5%_2), R4820 (10K_5%_2), R4821 (10K_5%_2), R4822 (10K_5%_2), R4823 (10K_5%_2), R4824 (10K_5%_2), R4825 (10K_5%_2), R4826 (10K_5%_2), R4827 (10K_5%_2), R4828 (10K_5%_2), R4829 (10K_5%_2), R4830 (10K_5%_2), R4831 (10K_5%_2), R4832 (10K_5%_2), R4833 (10K_5%_2), R4834 (10K_5%_2), R4835 (10K_5%_2), R4836 (10K_5%_2), R4837 (10K_5%_2), R4838 (10K_5%_2), R4839 (10K_5%_2), R4840 (10K_5%_2), R4841 (10K_5%_2), R4842 (10K_5%_2), R4843 (10K_5%_2), R4844 (10K_5%_2), R4845 (10K_5%_2), R4846 (10K_5%_2), R4847 (10K_5%_2), R4848 (10K_5%_2), R4849 (10K_5%_2), R4850 (10K_5%_2), R4851 (10K_5%_2), R4852 (10K_5%_2), R4853 (10K_5%_2), R4854 (10K_5%_2), R4855 (10K_5%_2), R4856 (10K_5%_2), R4857 (10K_5%_2), R4858 (10K_5%_2), R4859 (10K_5%_2), R4860 (10K_5%_2), R4861 (10K_5%_2), R4862 (10K_5%_2), R4863 (10K_5%_2), R4864 (10K_5%_2), R4865 (10K_5%_2), R4866 (10K_5%_2), R4867 (10K_5%_2), R4868 (10K_5%_2), R4869 (10K_5%_2), R4870 (10K_5%_2), R4871 (10K_5%_2), R4872 (10K_5%_2), R4873 (10K_5%_2), R4874 (10K_5%_2), R4875 (10K_5%_2), R4876 (10K_5%_2), R4877 (10K_5%_2), R4878 (10K_5%_2), R4879 (10K_5%_2), R4880 (10K_5%_2), R4881 (10K_5%_2), R4882 (10K_5%_2), R4883 (10K_5%_2), R4884 (10K_5%_2), R4885 (10K_5%_2), R4886 (10K_5%_2), R4887 (10K_5%_2), R4888 (10K_5%_2), R4889 (10K_5%_2), R4890 (10K_5%_2), R4891 (10K_5%_2), R4892 (10K_5%_2), R4893 (10K_5%_2), R4894 (10K_5%_2), R4895 (10K_5%_2), R4896 (10K_5%_2), R4897 (10K_5%_2), R4898 (10K_5%_2), R4899 (10K_5%_2), R4900 (10K_5%_2), R4901 (10K_5%_2), R4902 (10K_5%_2), R4903 (10K_5%_2), R4904 (10K_5%_2), R4905 (10K_5%_2), R4906 (10K_5%_2), R4907 (10K_5%_2), R4908 (10K_5%_2), R4909 (10K_5%_2), R4910 (10K_5%_2), R4911 (10K_5%_2), R4912 (10K_5%_2), R4913 (10K_5%_2), R4914 (10K_5%_2), R4915 (10K_5%_2), R4916 (10K_5%_2), R4917 (10K_5%_2), R4918 (10K_5%_2), R4919 (10K_5%_2), R4920 (10K_5%_2), R4921 (10K_5%_2), R4922 (10K_5%_2), R4923 (10K_5%_2), R4924 (10K_5%_2), R4925 (10K_5%_2), R4926 (10K_5%_2), R4927 (10K_5%_2), R4928 (10K_5%_2), R4929 (10K_5%_2), R4930 (10K_5%_2), R4931 (10K_5%_2), R4932 (10K_5%_2), R4933 (10K_5%_2), R4934 (10K_5%_2), R4935 (10K_5%_2), R4936 (10K_5%_2), R4937 (10K_5%_2), R4938 (10K_5%_2), R4939 (10K_5%_2), R4940 (10K_5%_2), R4941 (10K_5%_2), R4942 (10K_5%_2), R4943 (10K_5%_2), R4944 (10K_5%_2), R4945 (10K_5%_2), R4946 (10K_5%_2), R4947 (10K_5%_2), R4948 (10K_5%_2), R4949 (10K_5%_2), R4950 (10K_5%_2), R4951 (10K_5%_2), R4952 (10K_5%_2), R4953 (10K_5%_2), R4954 (10K_5%_2), R4955 (10K_5%_2), R4

SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by	XXX	DATE	21-OCT-2002
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A

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A



A

A

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	xxx	DATE	31 OCT 2002
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SHEET 52 of 66

REFERENCE 4700~4949(PCH)

The schematic illustrates the power and signal connections for the U4700 processor. It is divided into several functional blocks:

- POWER:** Includes connections for VCCADAC, VSSADAC, VCCALVDS, VSSALVDS, VCCCTX_LVDS[1-4], VCCCTX_LVDS[5-8], VCC3_3[6-7], VCCVRM[1], VCCDM[1], VCCCLADM, VCCDIFRM[1-4], and VCCSN. It shows the distribution of power from P1V05S and P3V3S sources through various capacitors (C4772, C4773, C4774, C4775, C4776, C4777, C4778, C4779, C4780, C4781, C4782, C4783, C4784, C4785, C4786, C4787, C4788, C4789, C4790, C4791, C4792) and inductors (L4700, L4701).
- LVDS:** Shows connections for VCCCTX_LVDS[1-4] and VCCCTX_LVDS[5-8] to the LVDS block.
- HVCMOS:** Shows connections for VCC3_3[6-7] to the HVCMOS block.
- DMI:** Shows connections for VCCVRM[1], VCCDM[1], and VCCCLADM to the DMI block.
- FDI:** Shows connections for VCCDIFRM[1-4] and VCCSN to the FDI block.
- NAND / SPI:** Shows connections for VCCDIFRM[1-4] and VCCSN to the NAND / SPI block.

The processor is labeled U4700 and includes various pins such as AA23, AC23, AD21, AD23, AF21, AF23, AG23, AG24, AG26, AG27, AG29, AJ23, AJ26, AJ27, AJ29, AJ31, AN19, AN16, AN17, AN21, AN26, AN27, AP21, AP23, AP24, AP26, AT24, AN33, AN34, BH29, AP16, AP17, AU20, and VCCIO[1-17].

ITL_PANTHERPOINT_FCBGA_989P

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

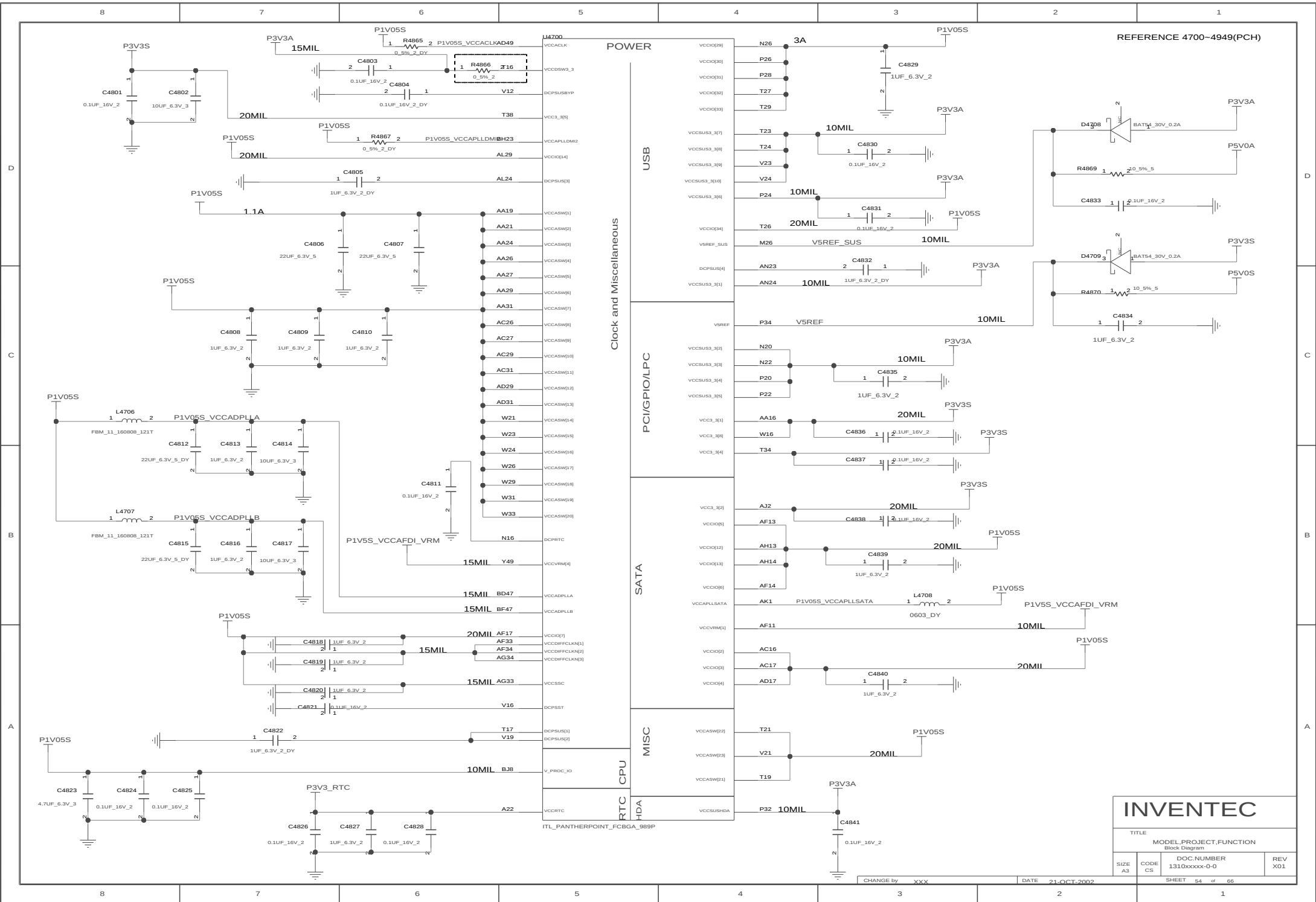
SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

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TITLE	MODEL,PROJECT,FUNCTION
	Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 53 of 66			

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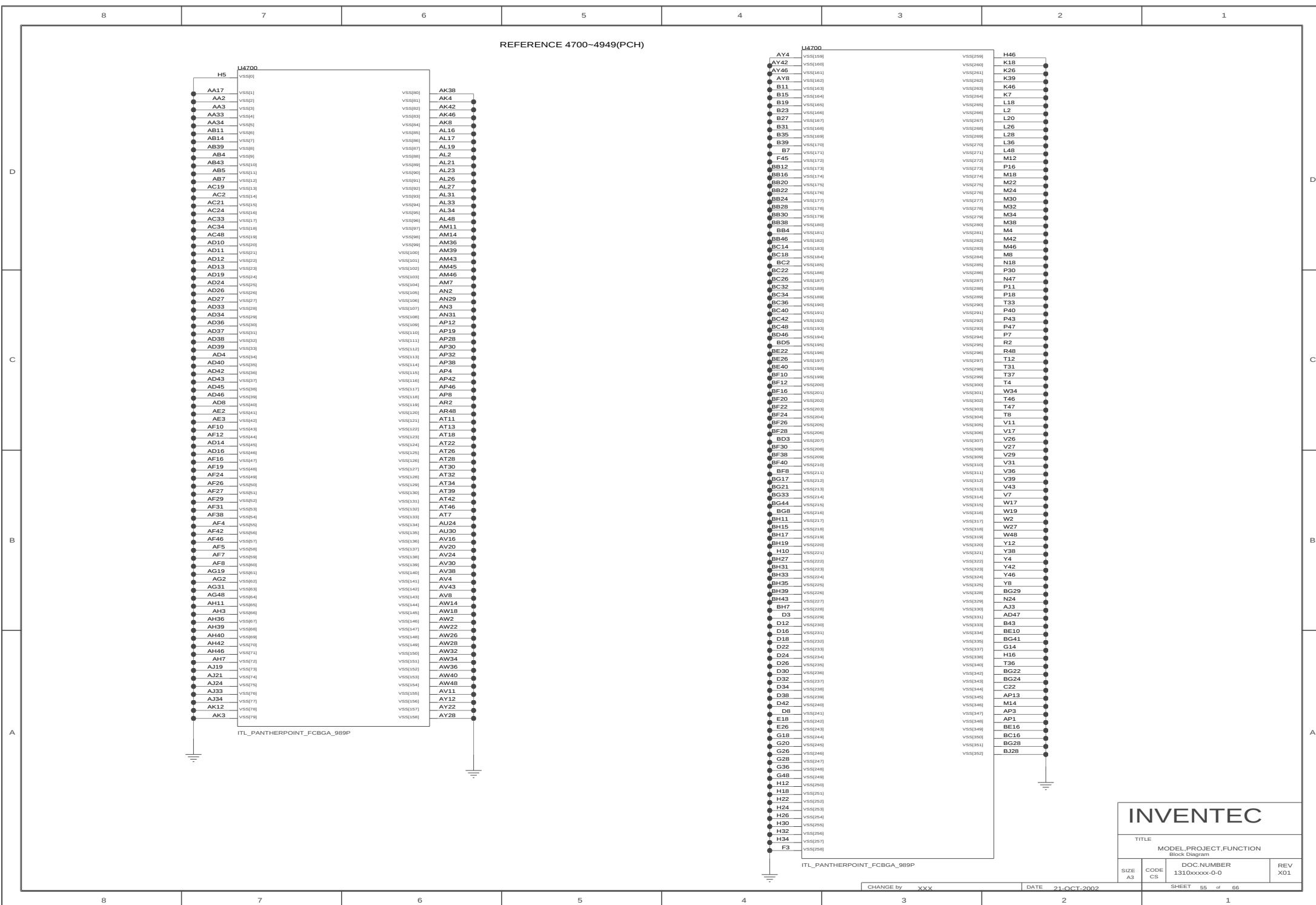


INVENTEC

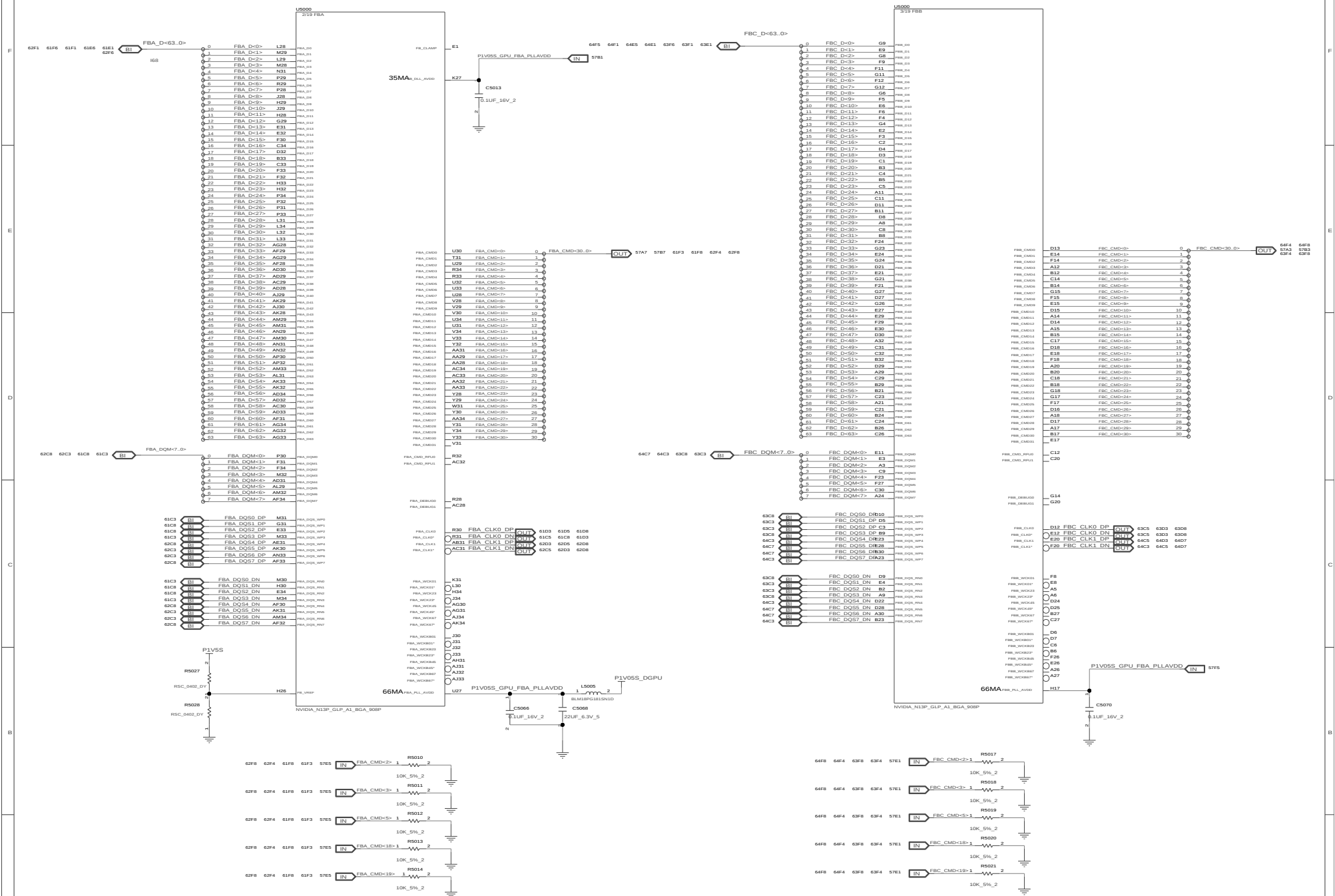
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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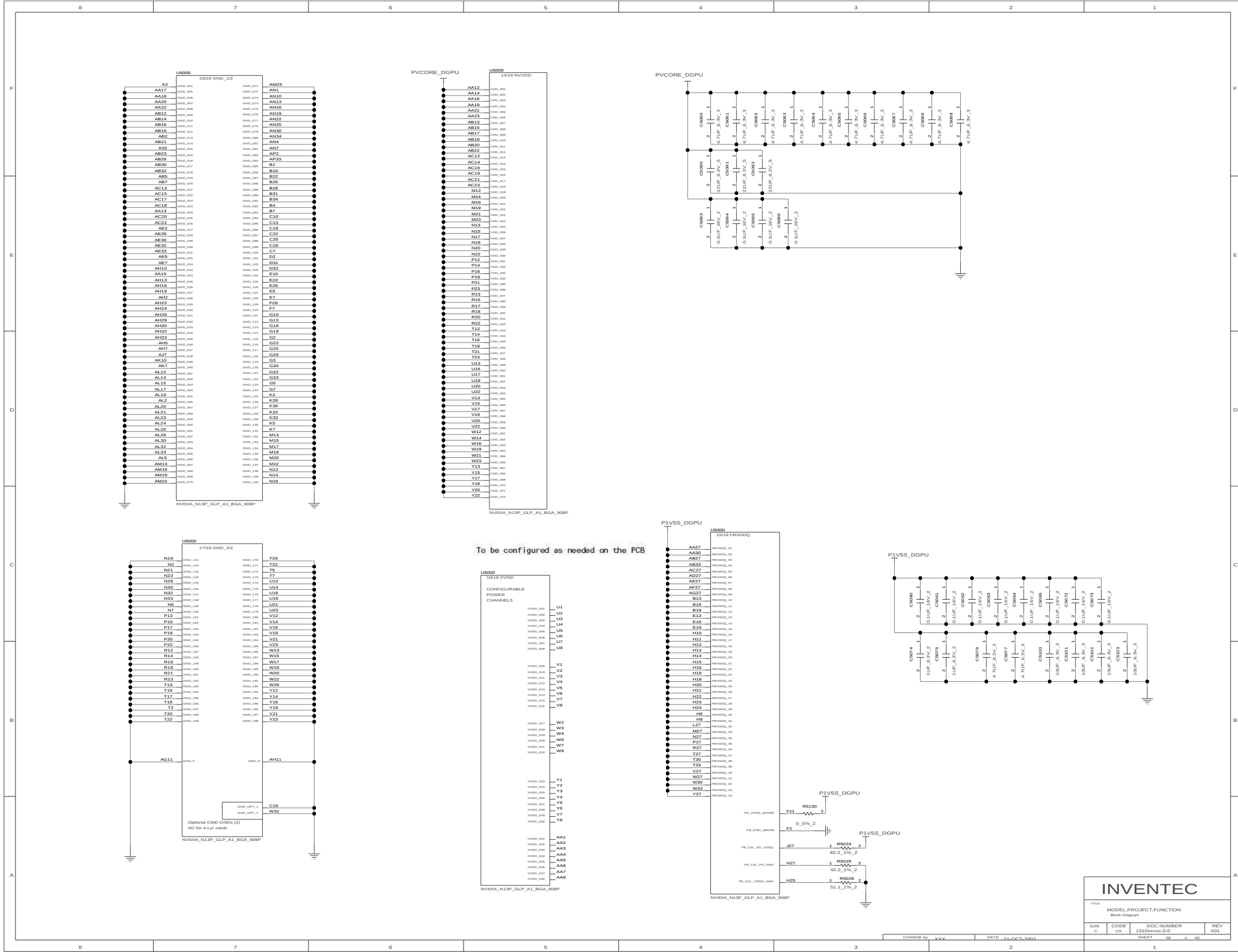
FB_CLAMP
N13P-PES/GLGLP : NC
N13P-GV,N13M-GS:N13P-GT-GLP: PL10K

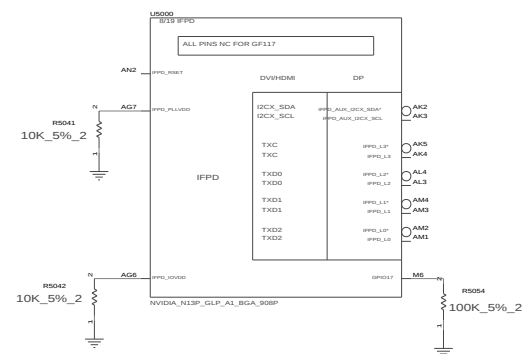
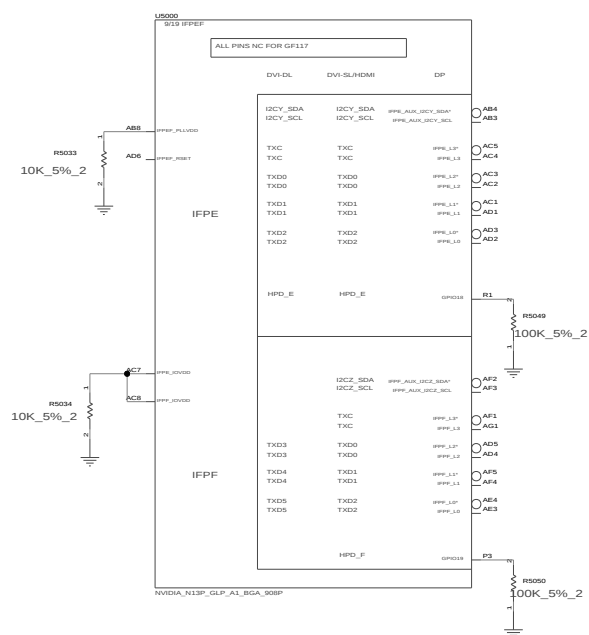
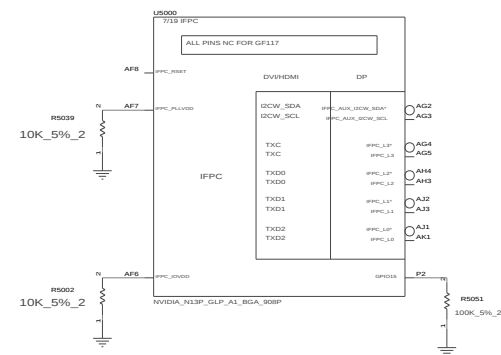
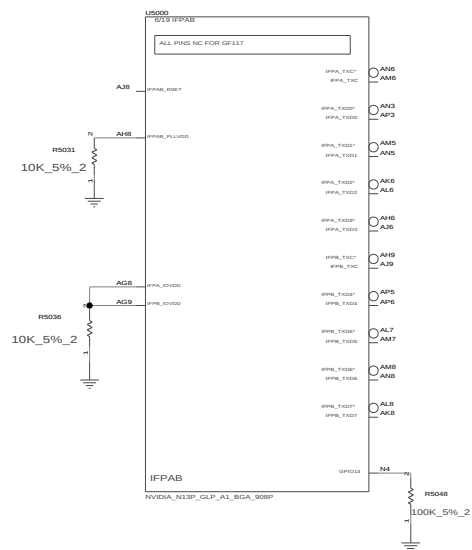


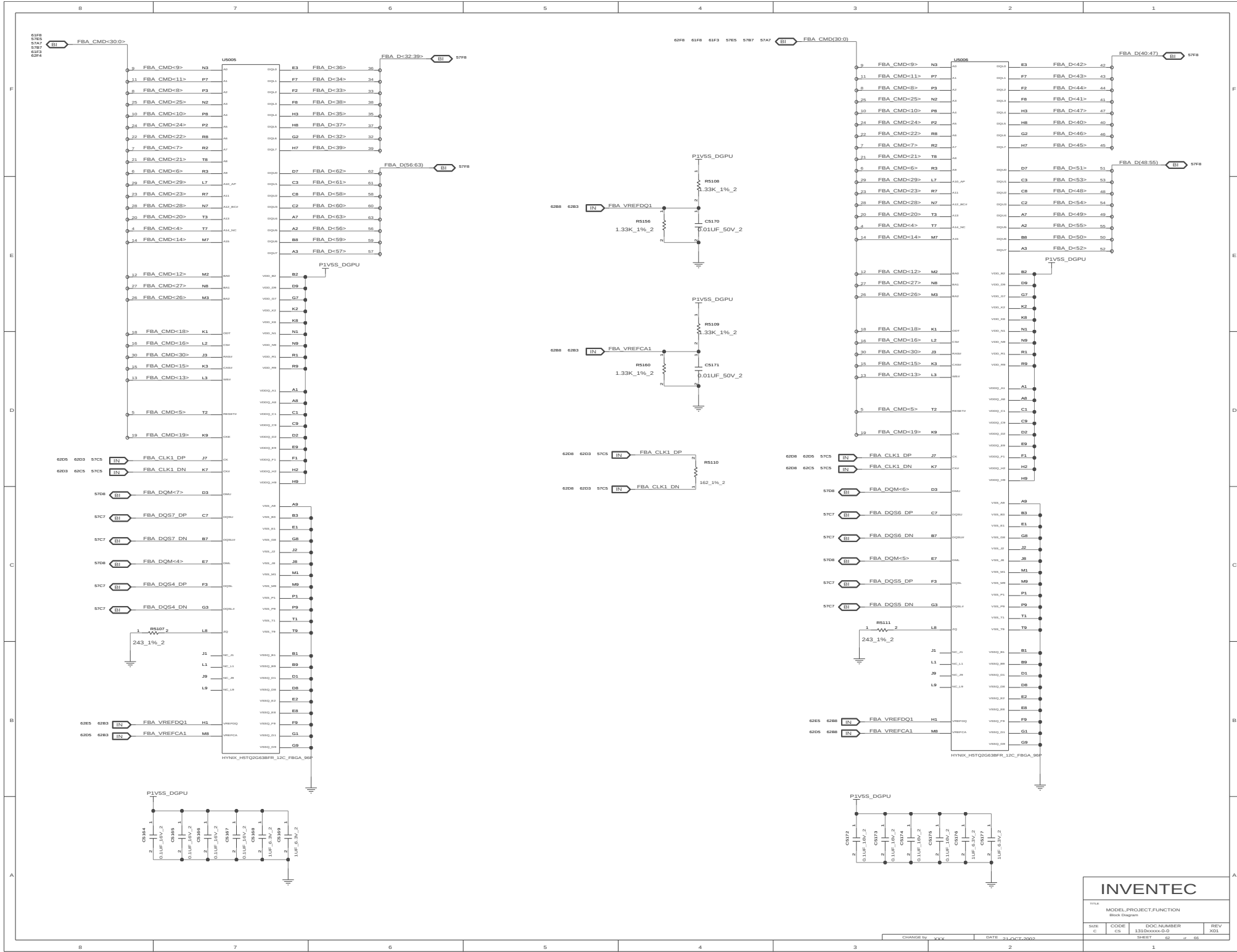
INVENTEC

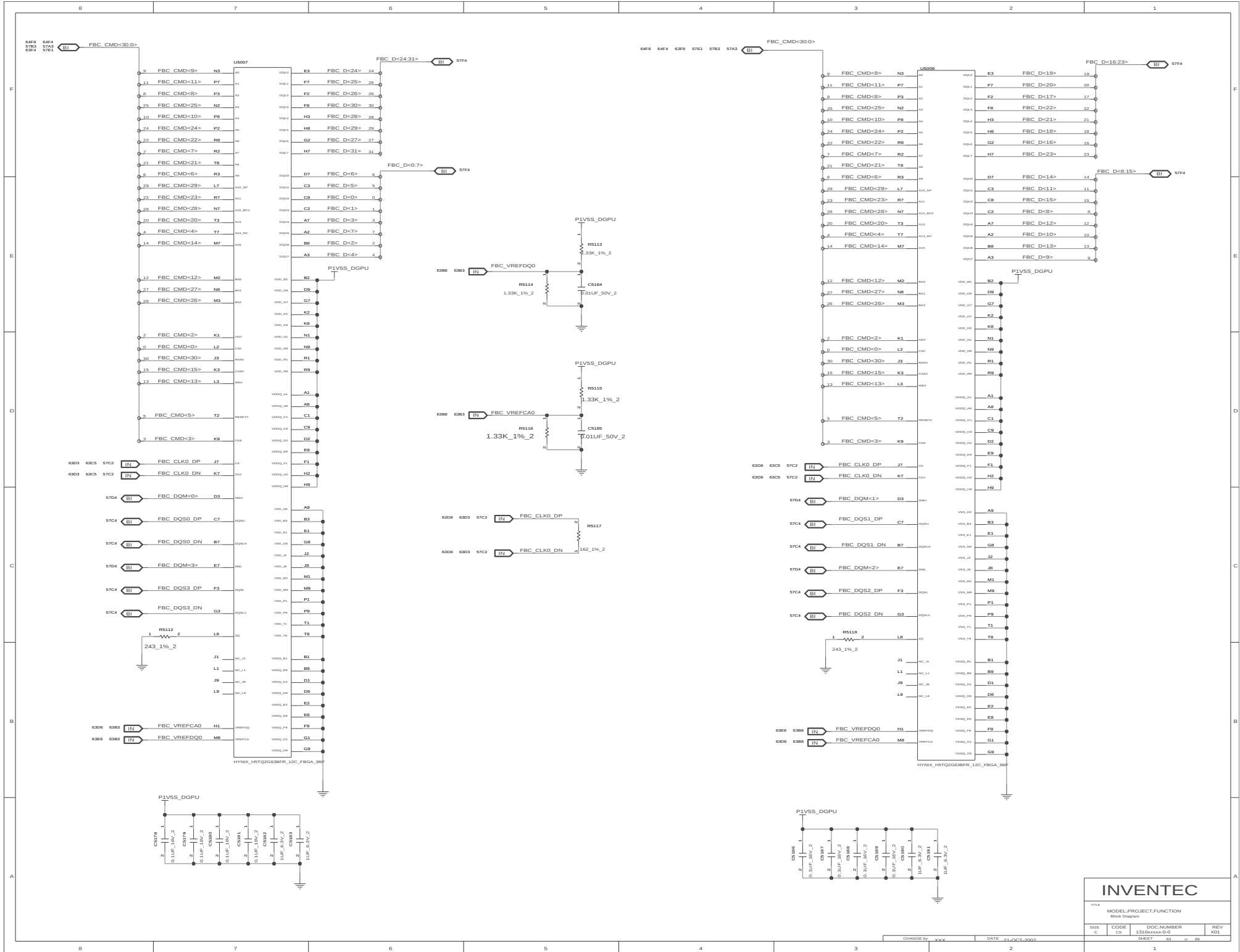
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Blank Diagram			
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CHANGE BY: Y.Y.V. DATE: 21-DEC-2002





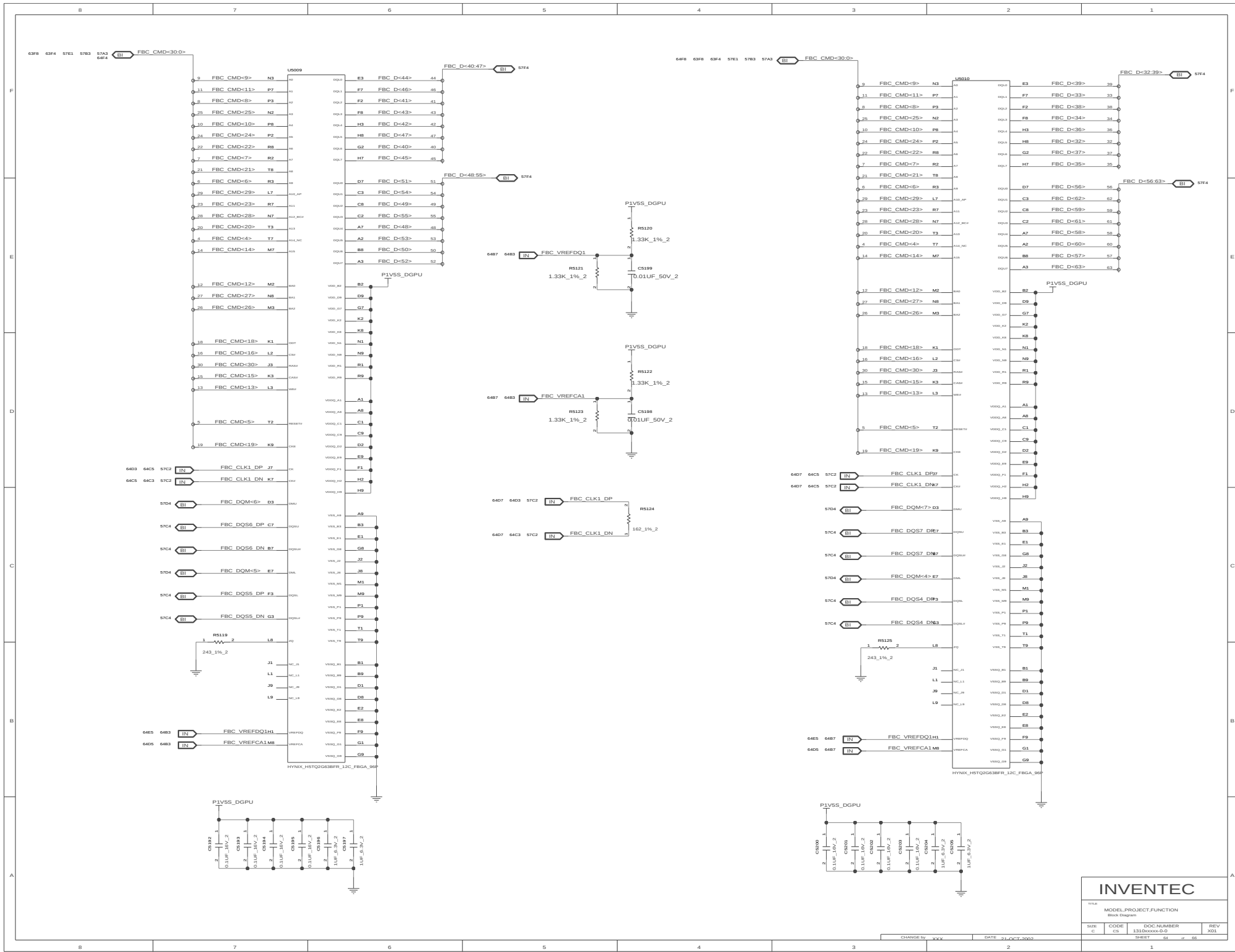




INVENTEC

TITLE			
MODEL PROJECT.FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
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CHANGE BY		DATE		SHEET	
XXX		21/01/2002		1 of 65	



INVENTEC

MODEL PROJECT FUNCTION
Block Diagram

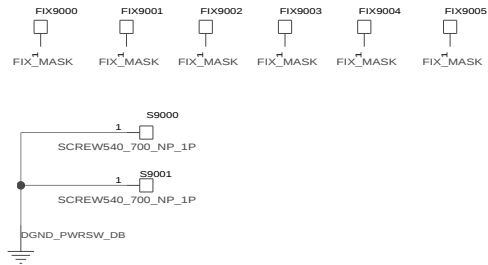
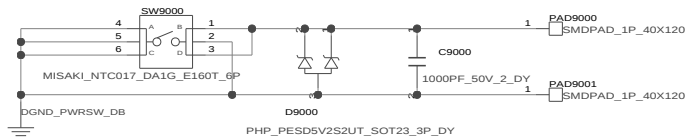
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CHANGE BY: YYY DATE: 21-JULY-2002

SHEET 55 OF 55

REFERENCE 9000~9999(SMALL BOARD)

POWER BUTTON



INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 65 of 66

	8	7	6	5	4	3	2	1
D								
C								
B								
A								
	8	7	6	5	4	3	2	1

INVENTEC			
TITLE MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
SHEET 66 of 66			

CHANGE by XXX DATE 21-OCT-2002