Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM+ICH9-M SFF core logic

ULV core logic HDI board DISCRETE VGA M92

2009-06-19 V.03

Security Classification	Compal Secret Data		
Issued Date	2009/04/20	Deciphered Date	2010/04/30

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Title: *Cover Sheet*

Size	Document Number	Rev
Custom	*LS-5588*	0.3

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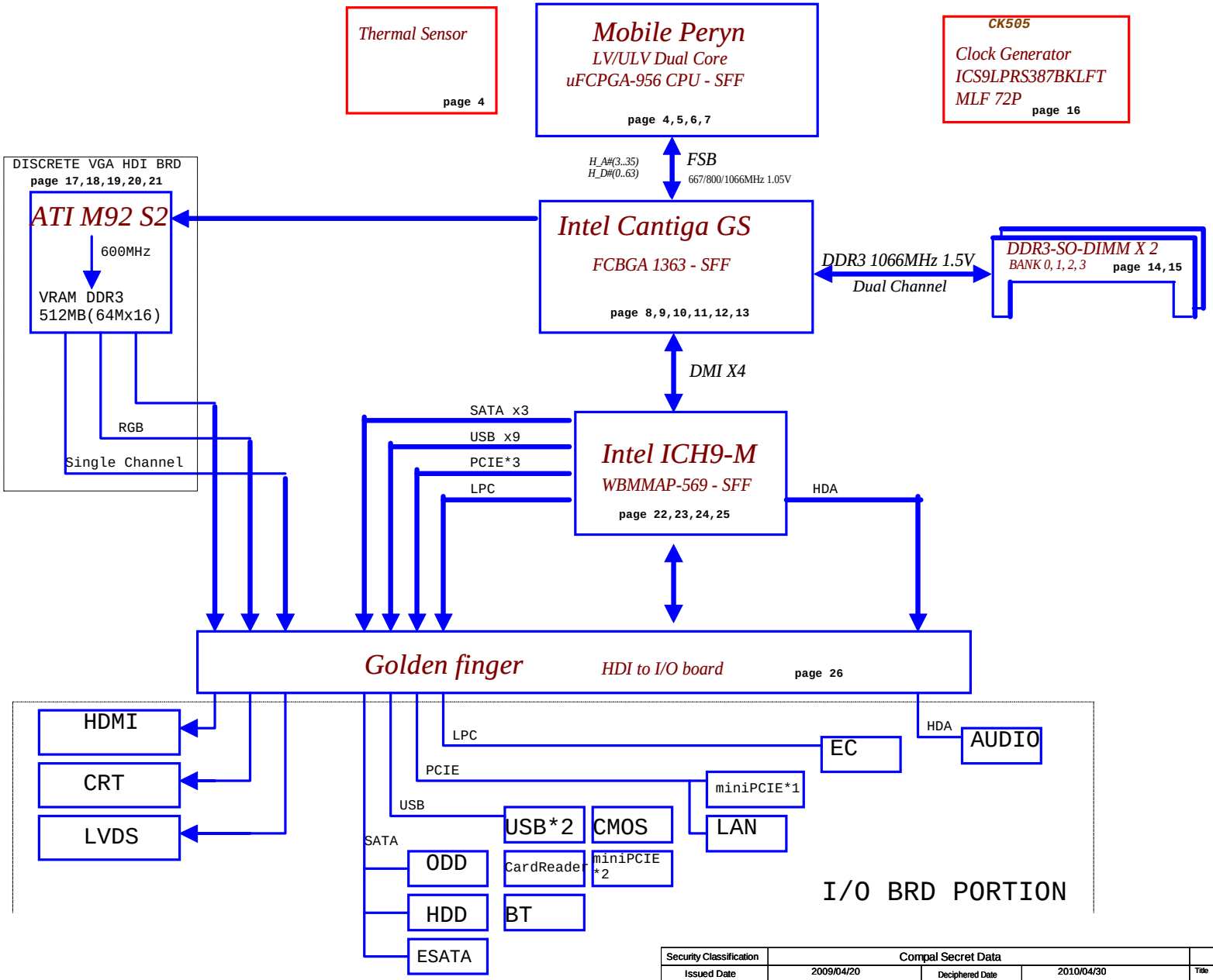
Compal confidential
Model Name : NAW20
File Name : LS-5588P

ULV



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Title: Block Diagram

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+B +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75VS +VCCP +CPU_CORE +VGA_CORE +1.1VS +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
ME@ : means ME part.
45@ : means install after SMT.

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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Title: Notes List

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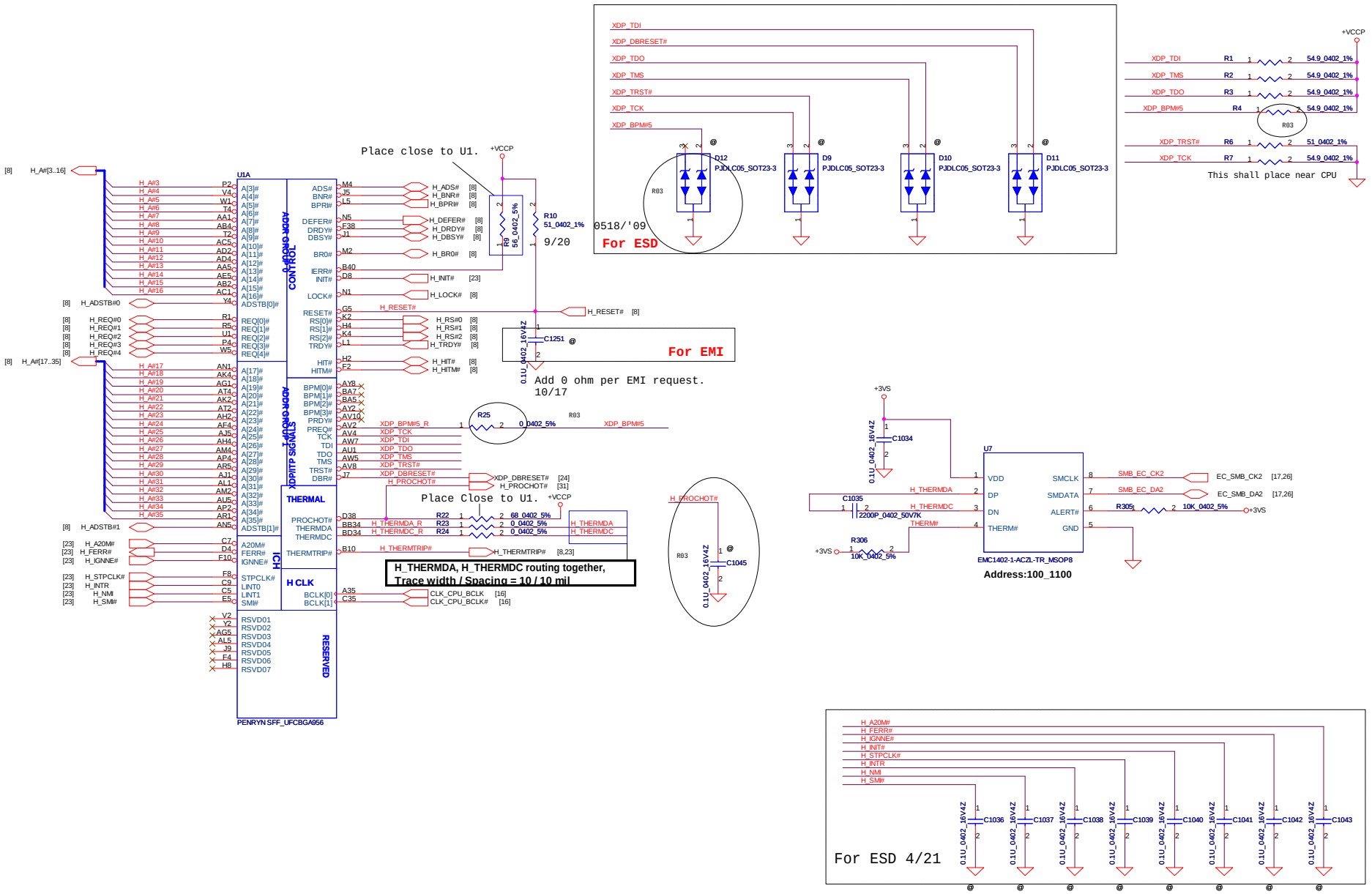

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Compal Electronics, Inc.

Title: **Penryn(1/3)-AGTL+/ITP-XDP**

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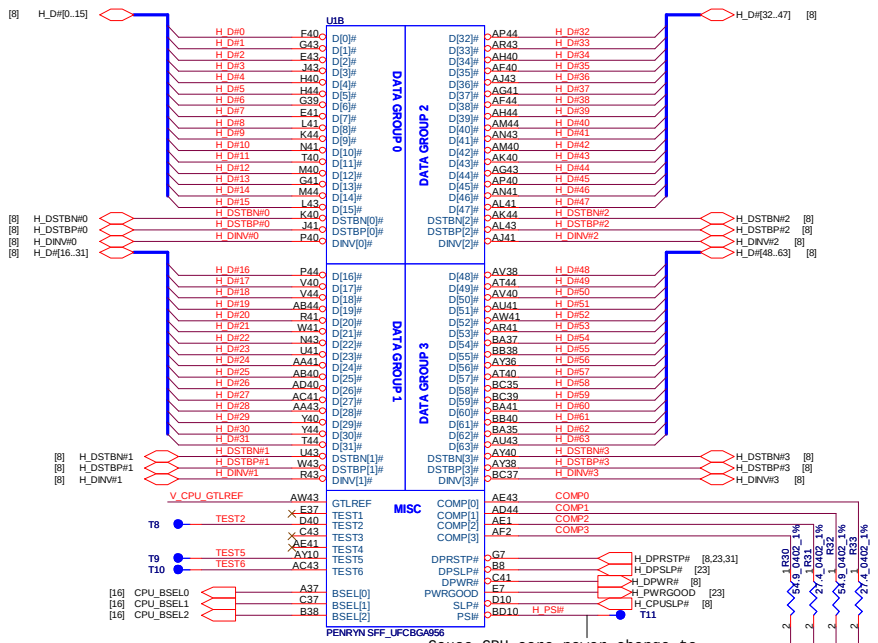
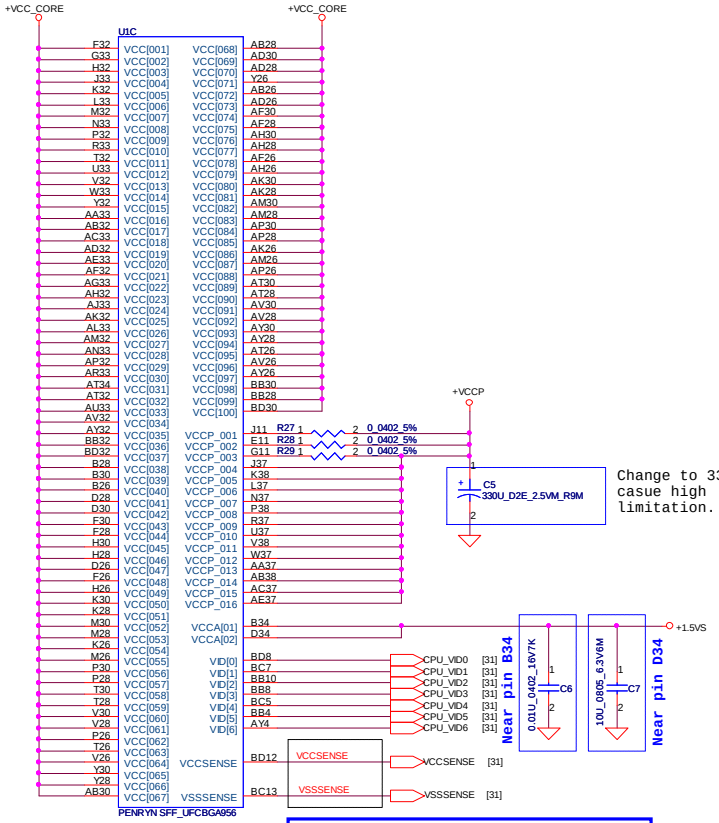


Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

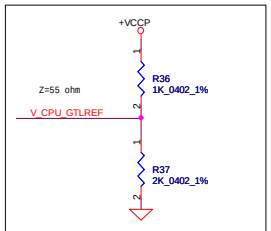
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

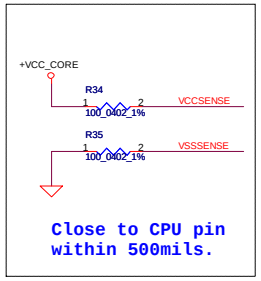


Change to 330u_R9, casue high limitation. 12/14

Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin AW43 within 500mils.



Close to CPU pin within 500mils.

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Compal Electronics, Inc.

Title: **Penryn(2/3)-AGTL+/ITP-XDP**

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Custom	LS-5588	0.3

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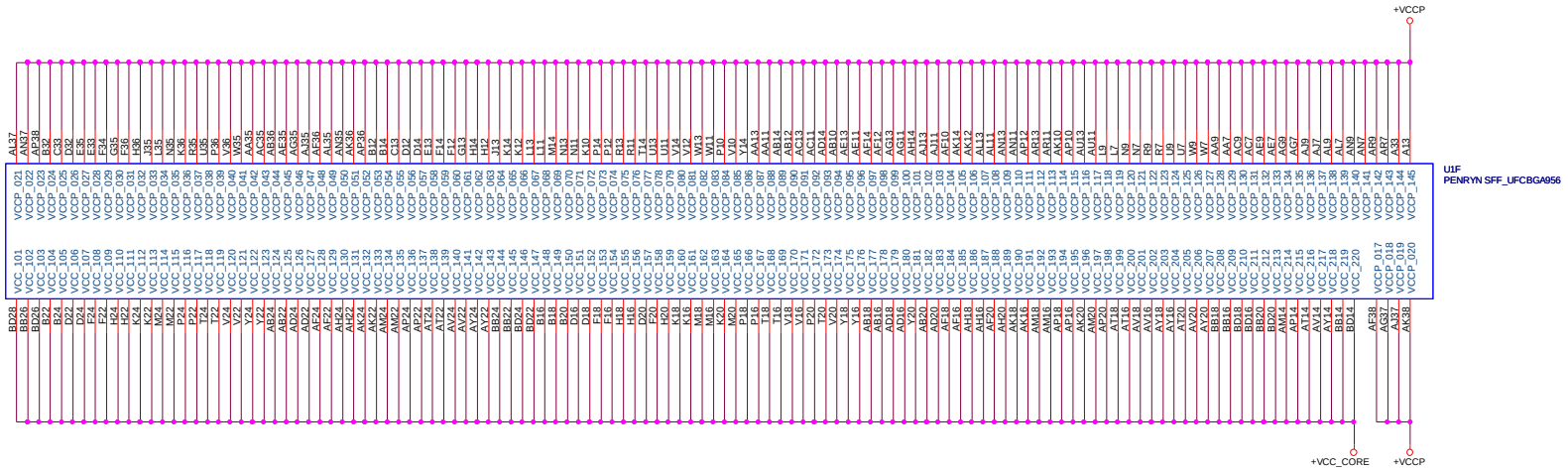

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Title: **Penryn(3/3)-Power**

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Custom	LS-5588	0.3

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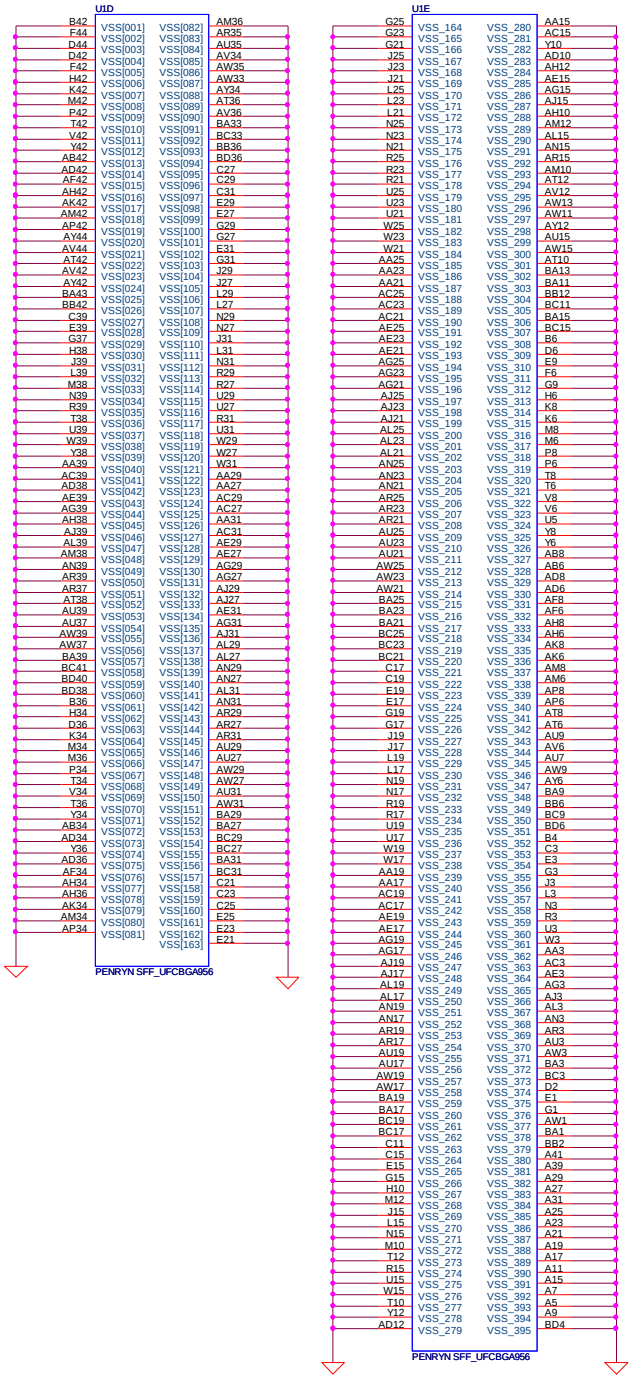

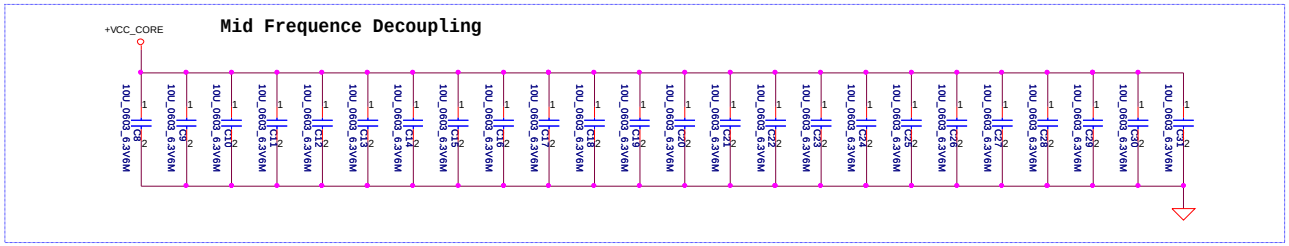

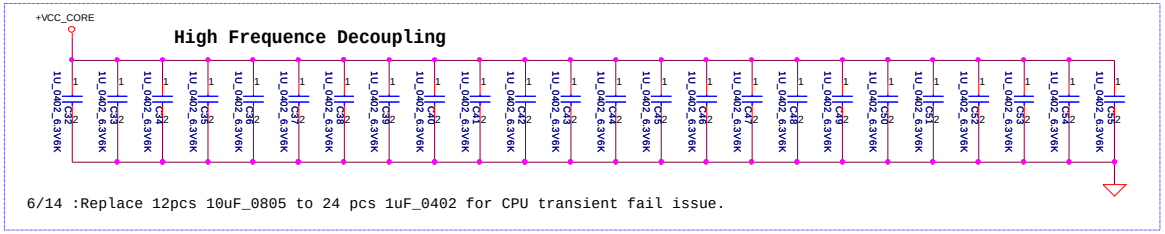

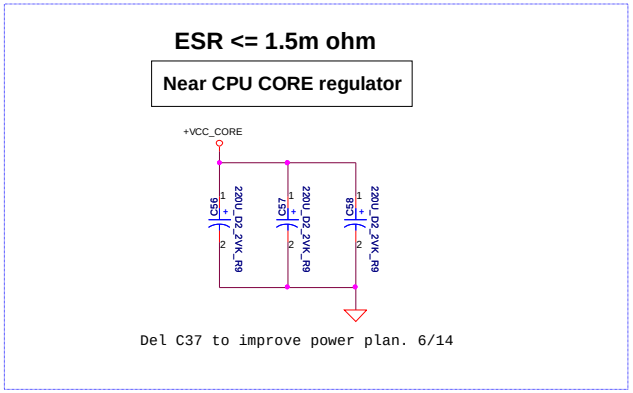

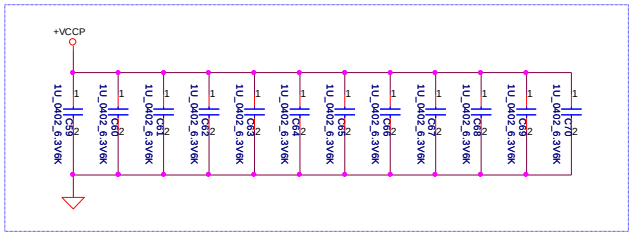

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Title: **Penryn(3/3)-GND/Bypass**

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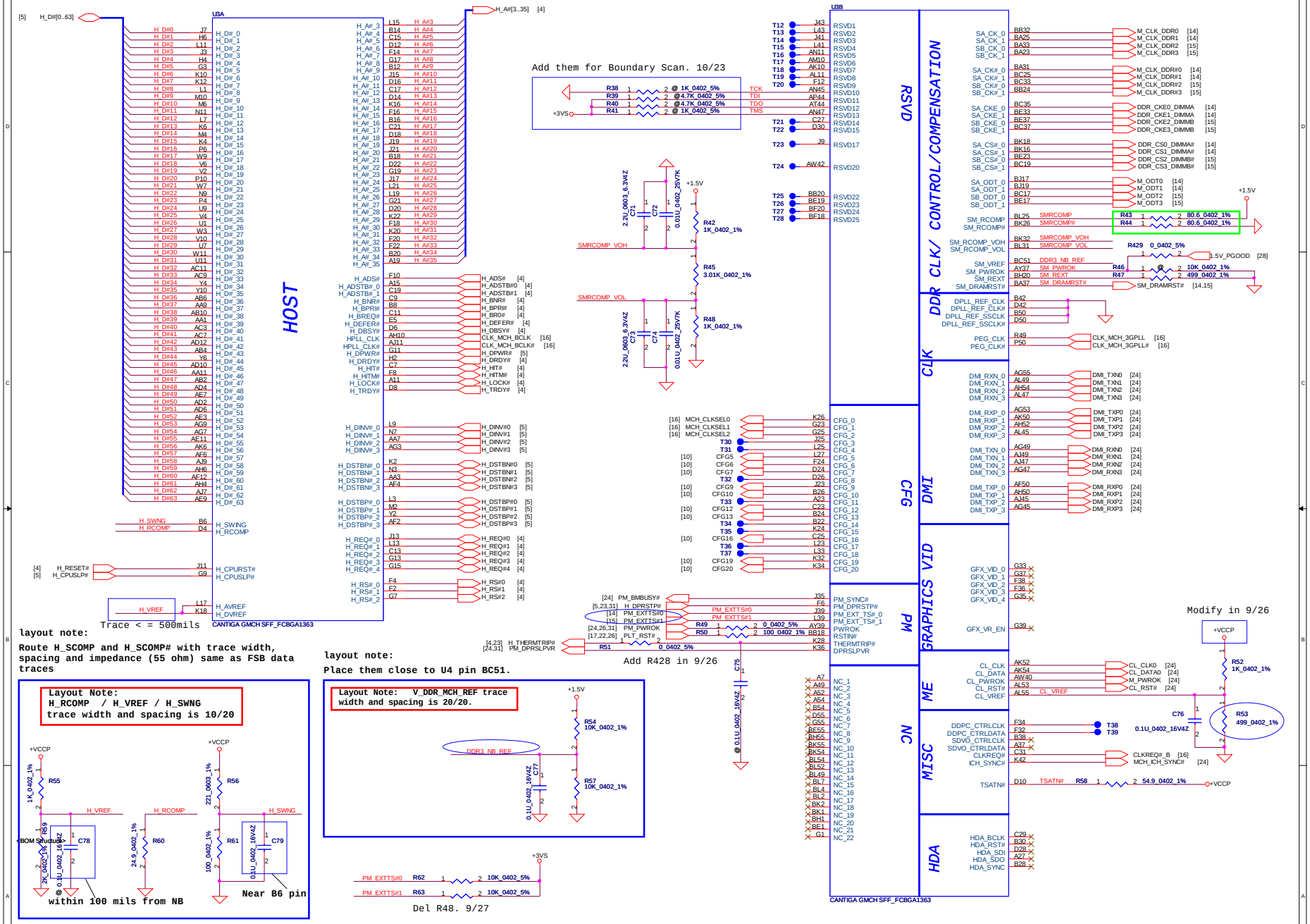

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Title: **Cantiga(1/6)-AGTL/DMI/DDR**

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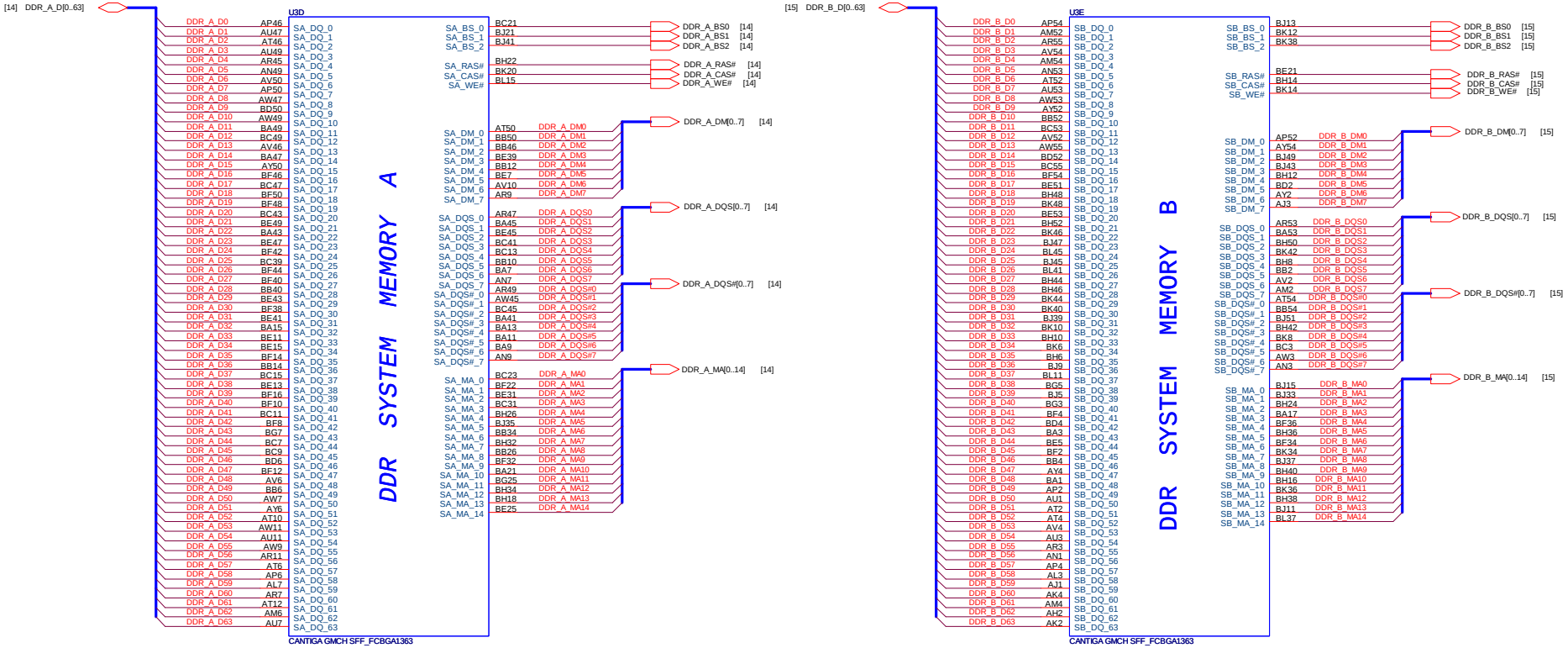

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Compal Electronics, Inc.

Title: **Cantiga(2/6)-DDR2 A/B CH**

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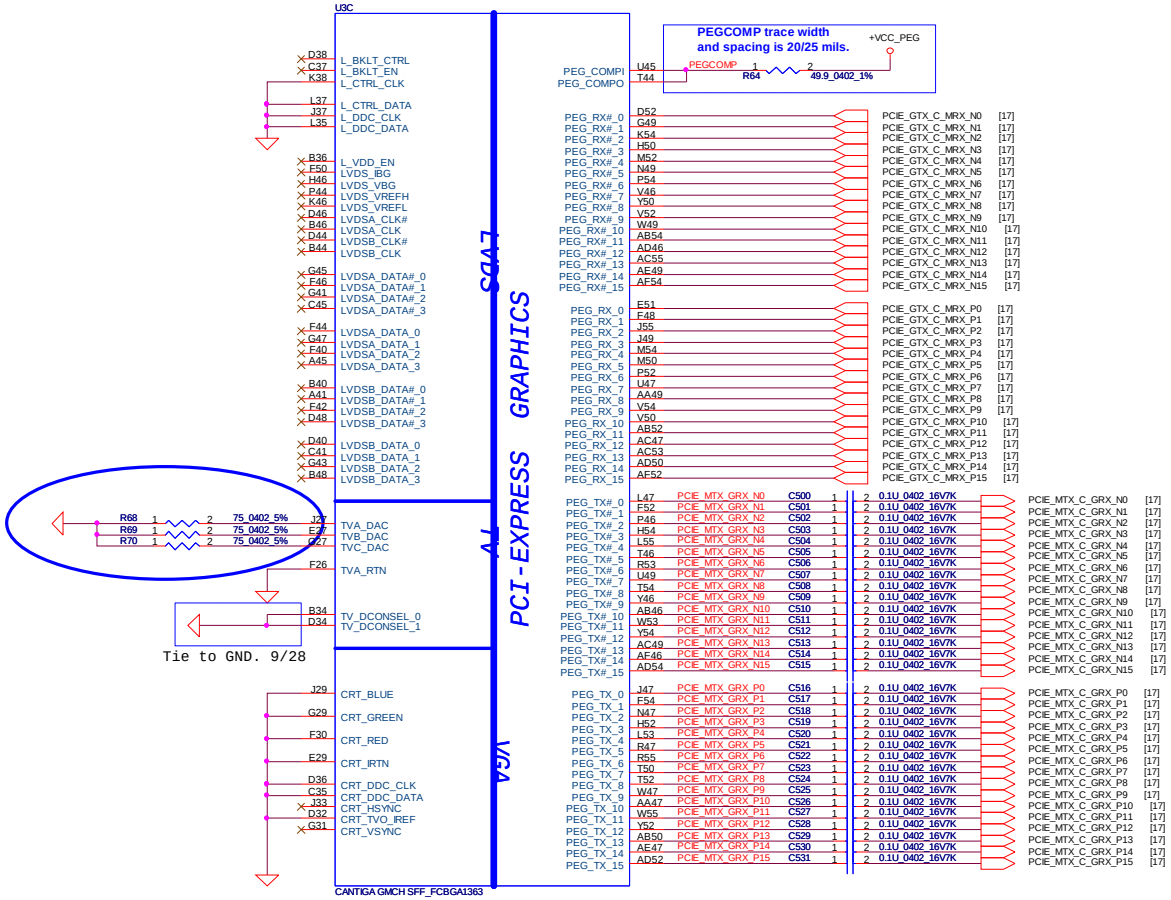

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

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Title: Cantiga(3/6)-VGA/LVDS/TV

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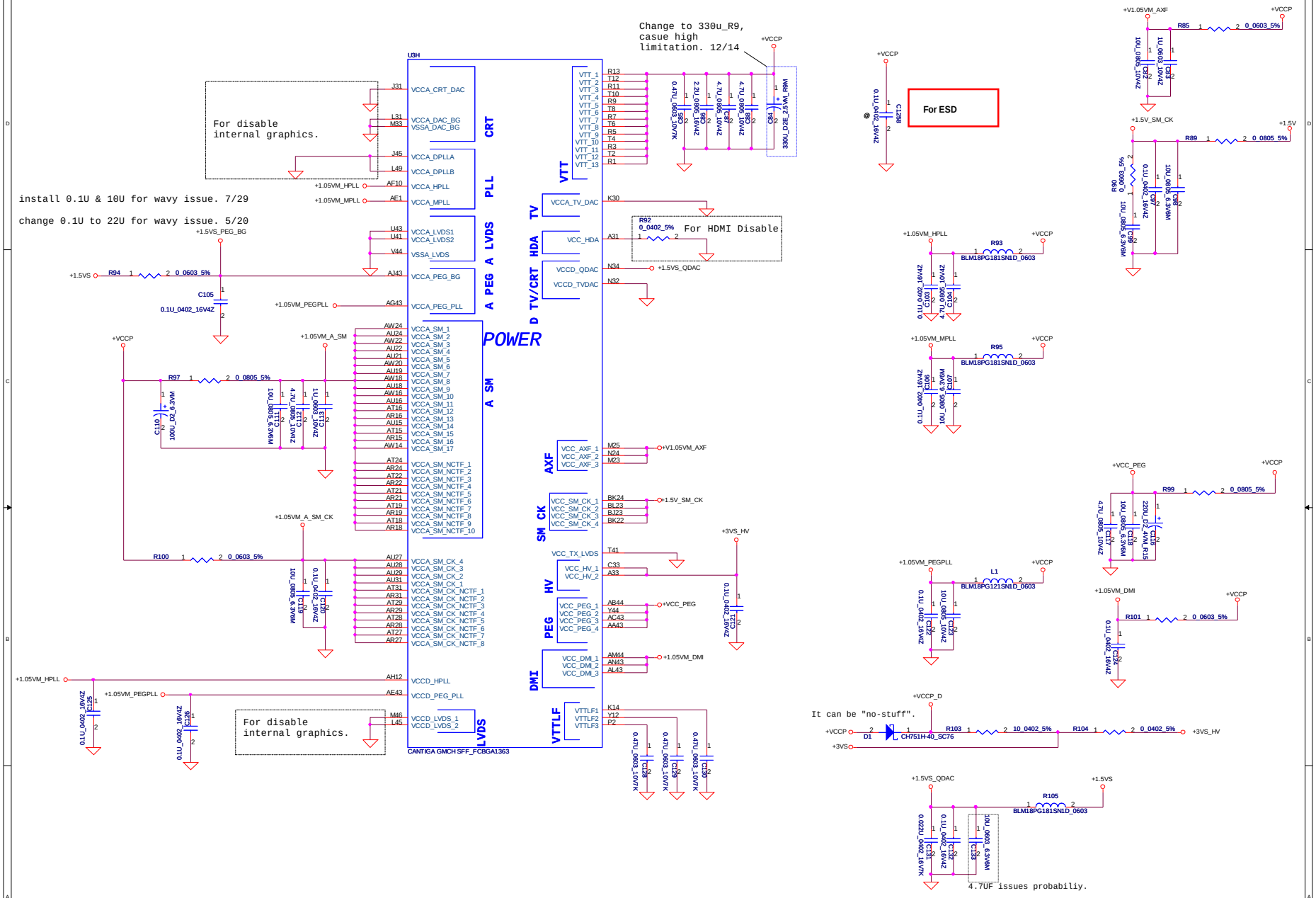

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Title: **Cantiga(4/6)-PWR**

Size: Custom | Document Number: **LS-5588** | Rev: 0.3

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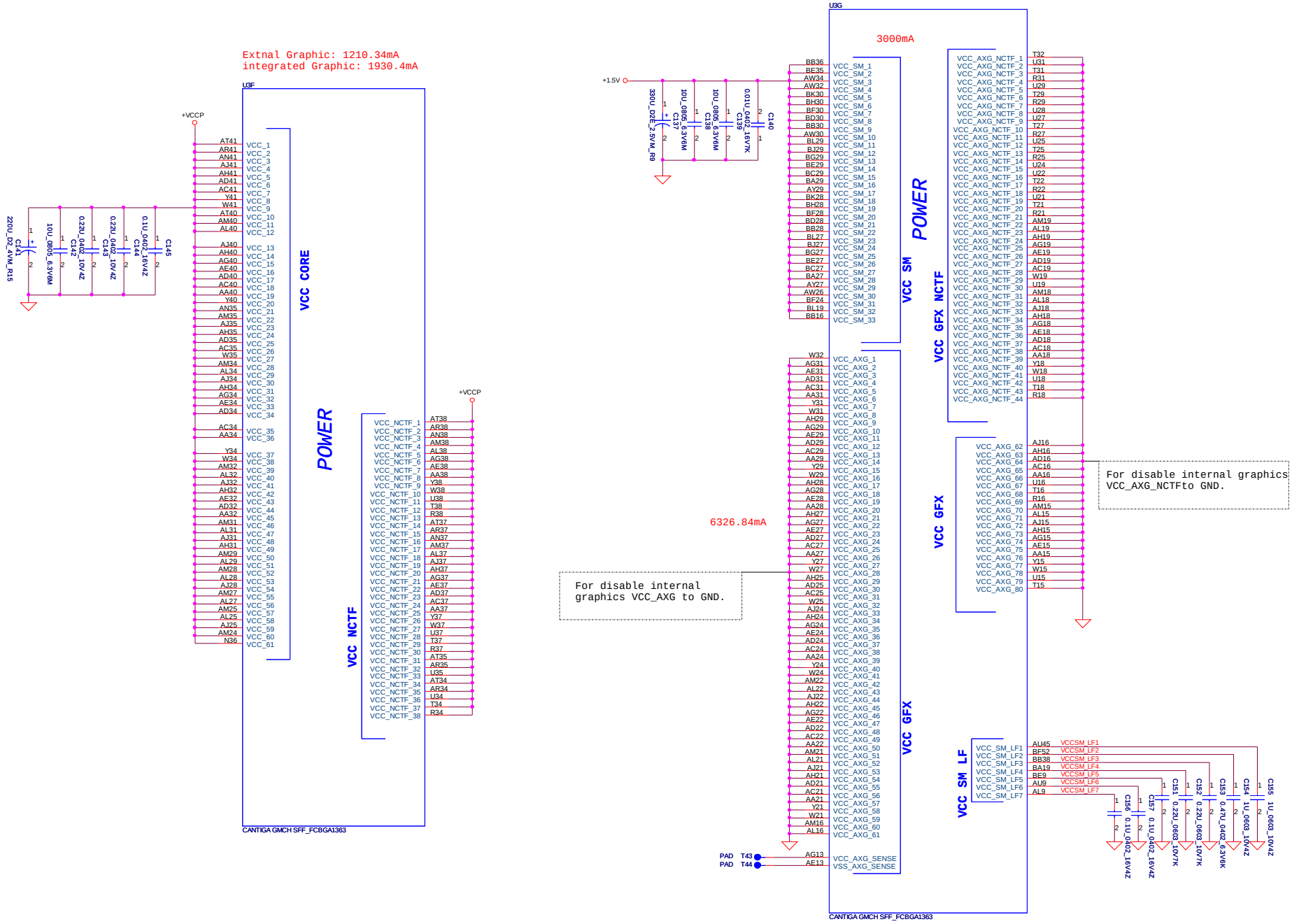

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Title: **Cantiga(5/6)-PWR/GND**

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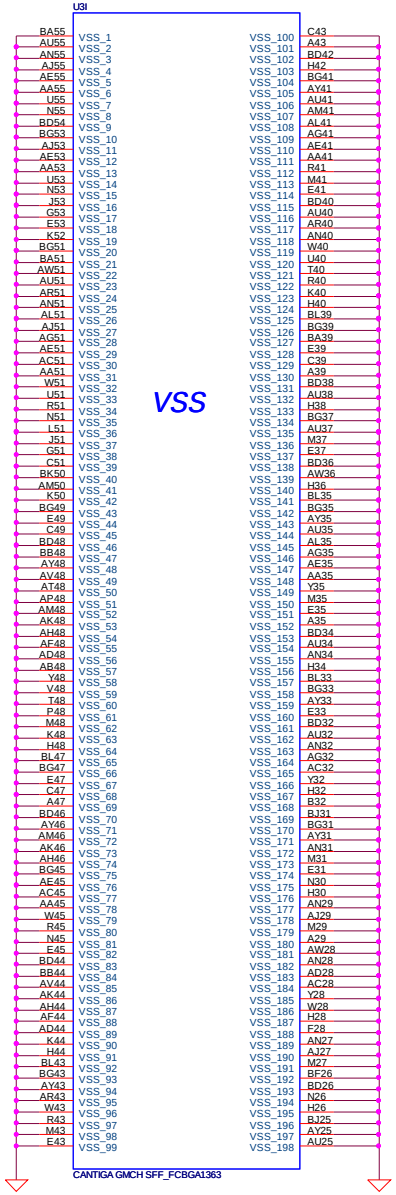

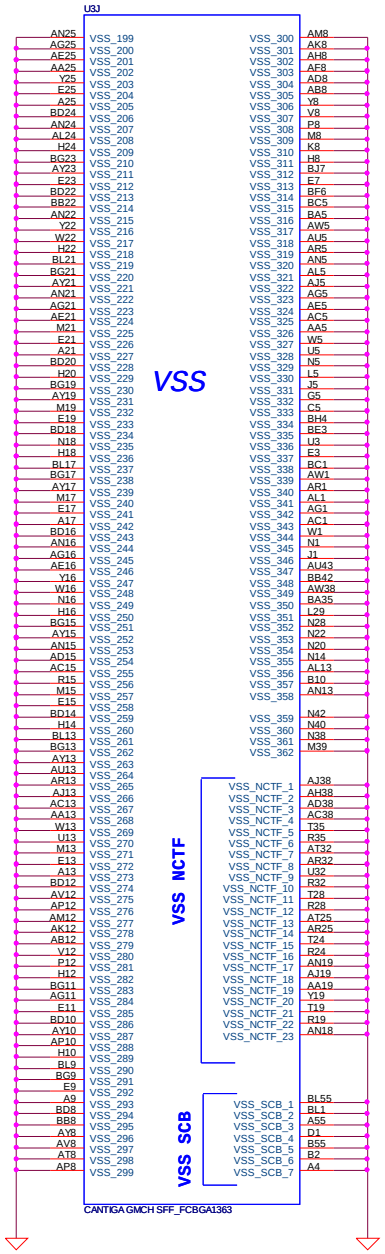

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Compal Electronics, Inc.

Title: **Cantiga(6/6)-PWR/GND**

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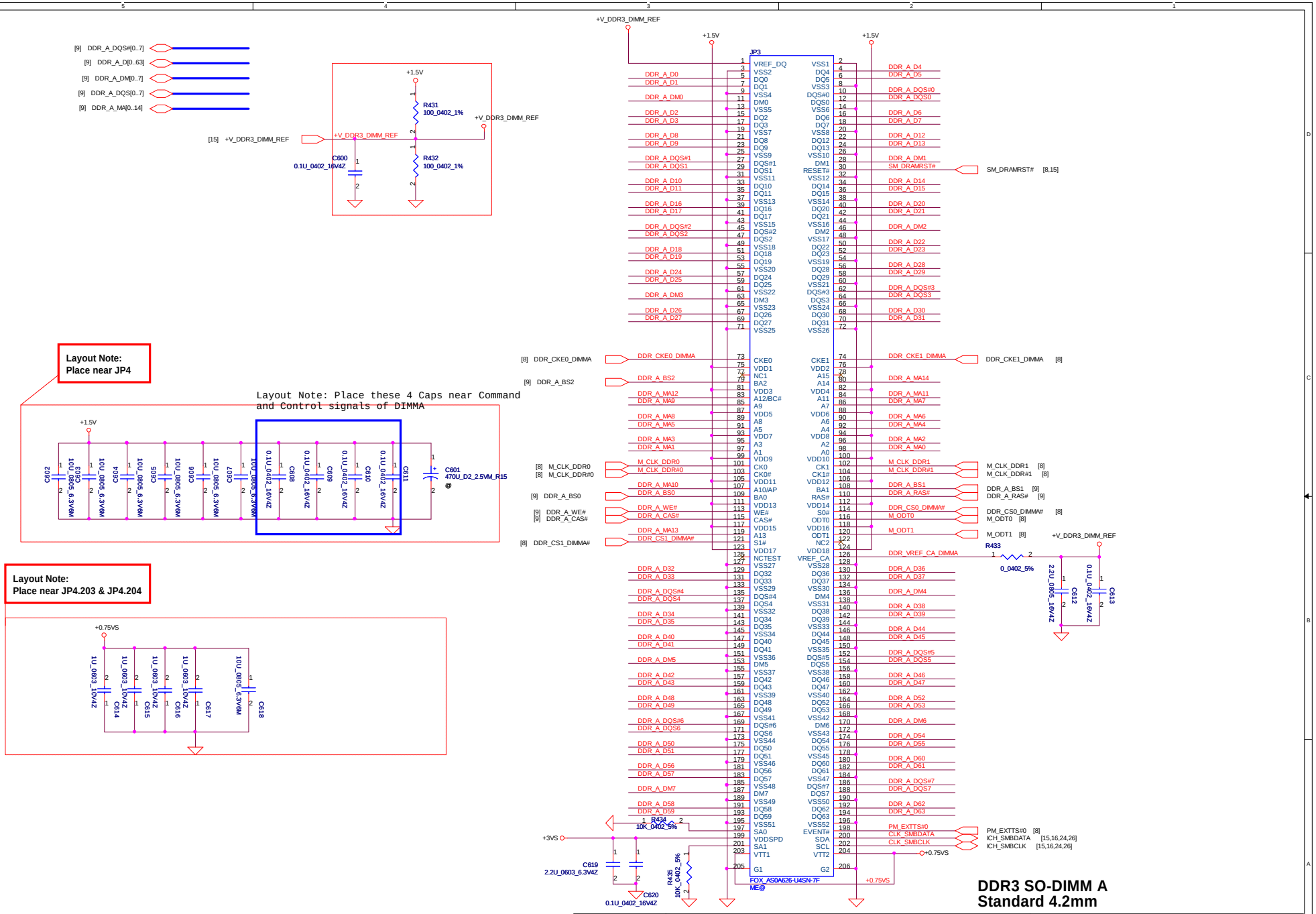

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Title: **DDR3-SODIMM SLOT1**

Size	Document Number	Rev
Custom	LS-5588	0.3

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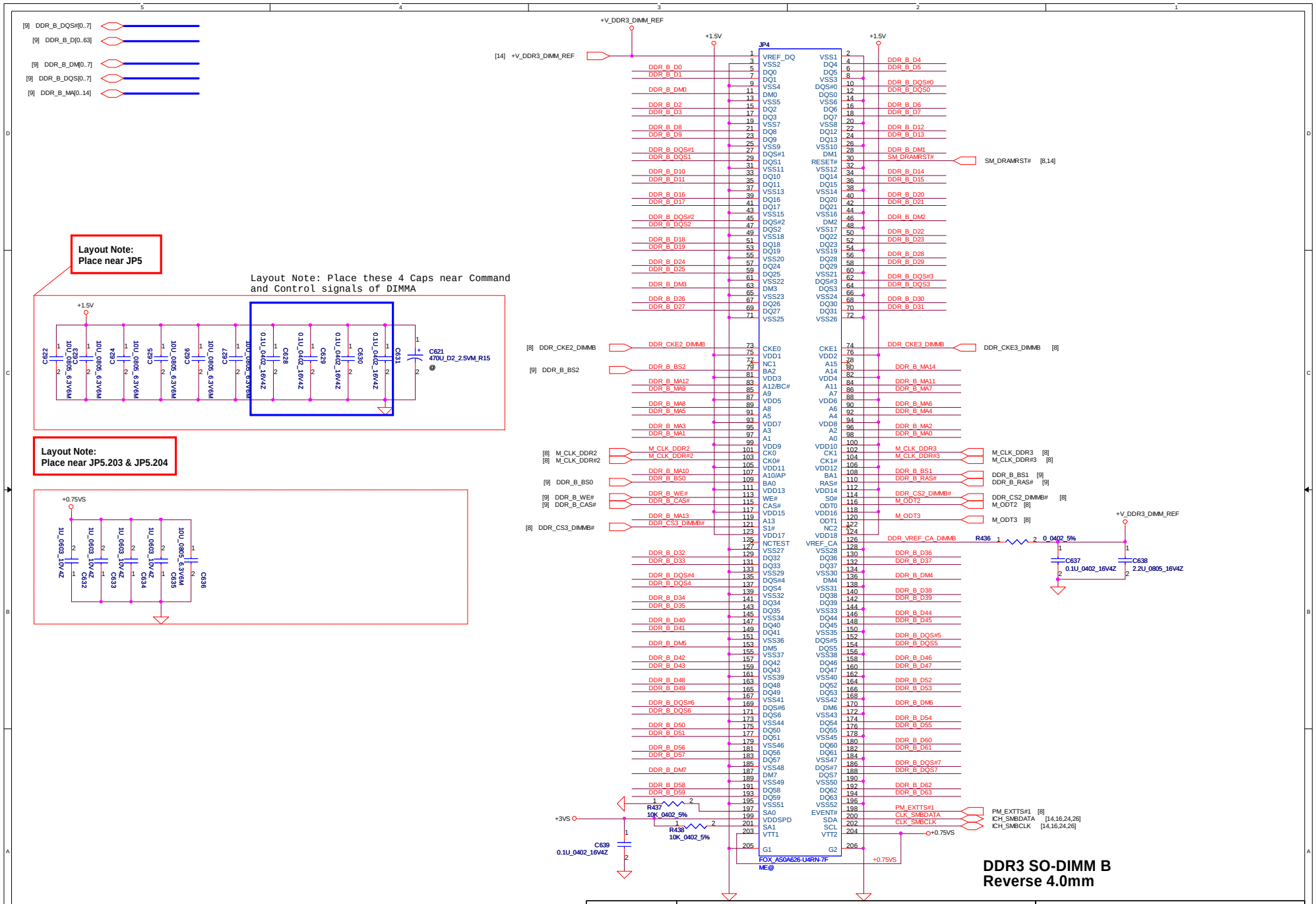

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Title: **DDR3-SODIMM SLOT2**

Size	Document Number	Rev
	LS-5588	0.3

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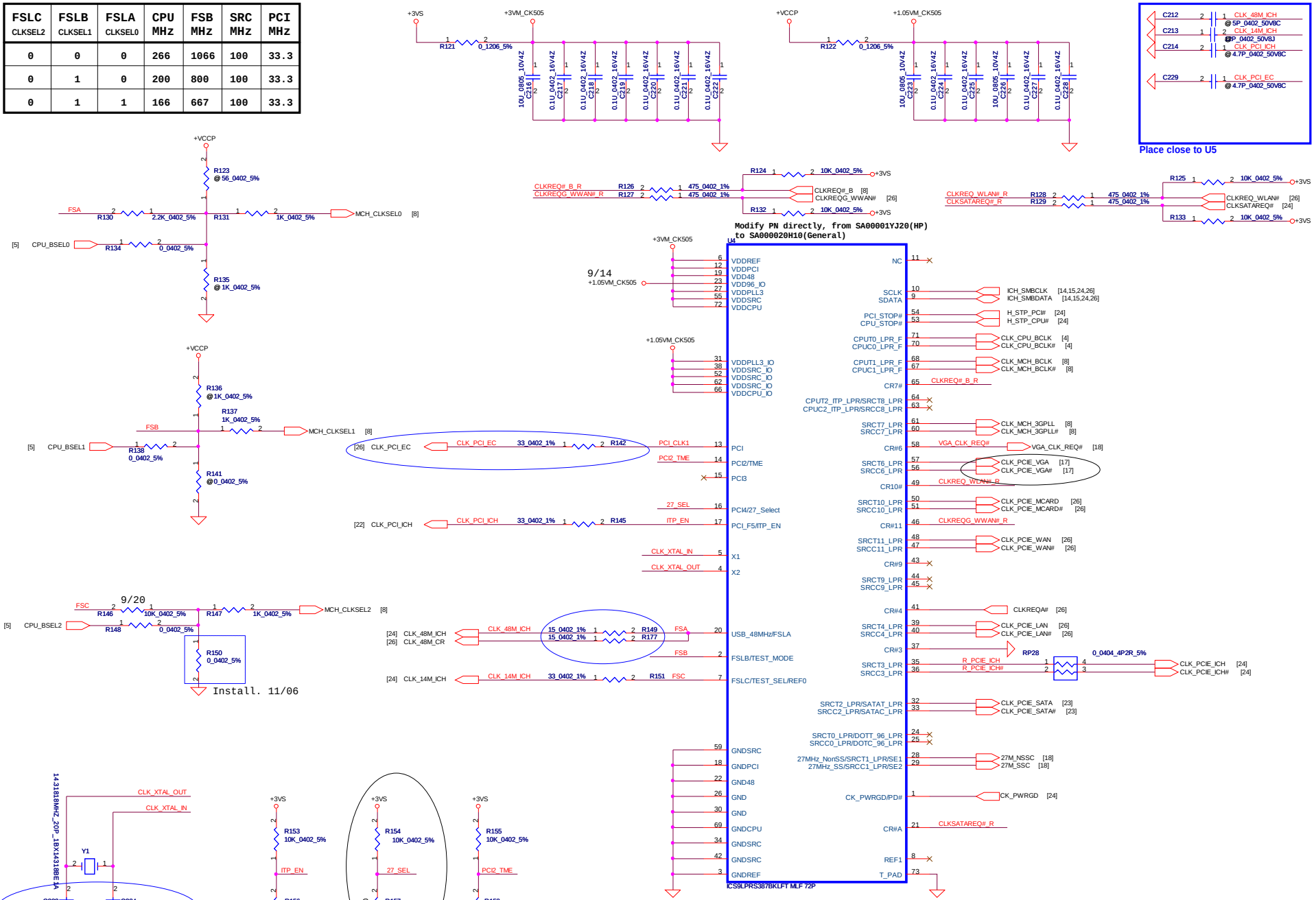
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	FSB MHz	SRC MHz	PCI MHz
0	0	0	266	1066	100	33.3
0	1	0	200	800	100	33.3
0	1	1	166	667	100	33.3



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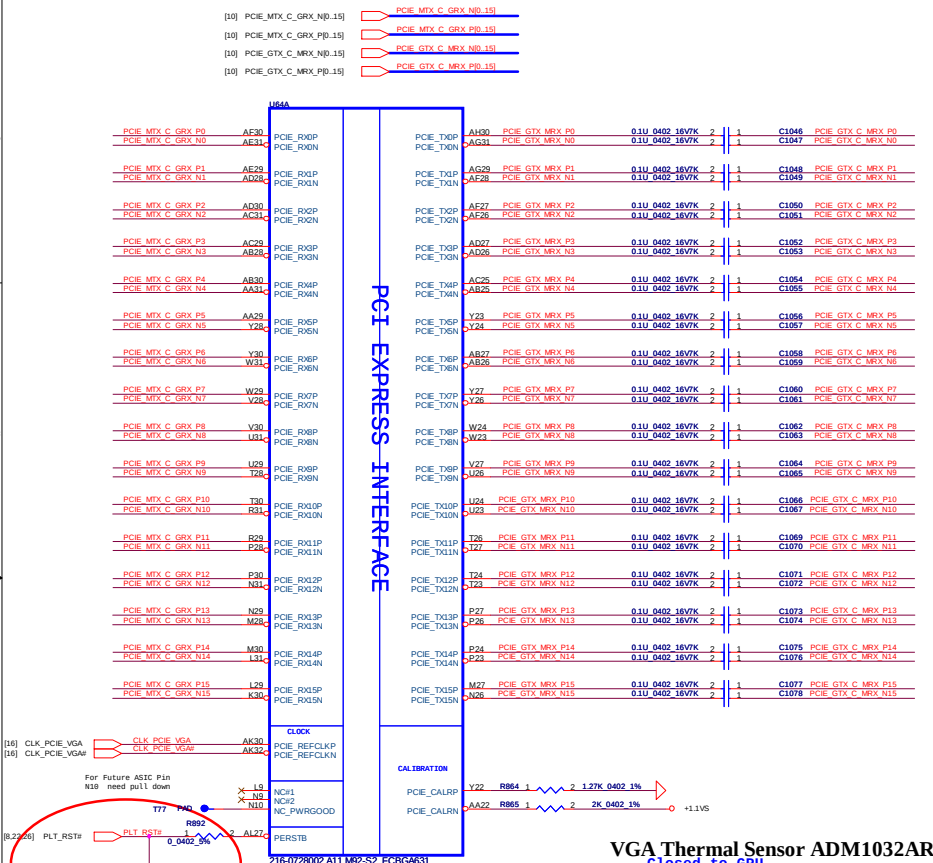
Compal Electronics, Inc.

Title: **CLOCK GENERATOR**

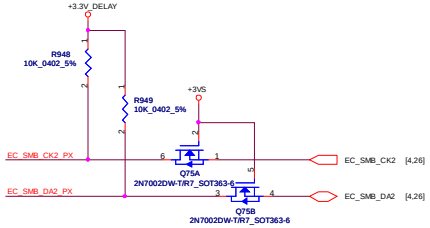
Size	Document Number	Rev
	LS-5588	0.3

Date: Wednesday, July 01, 2009 | Sheet 16 of 35

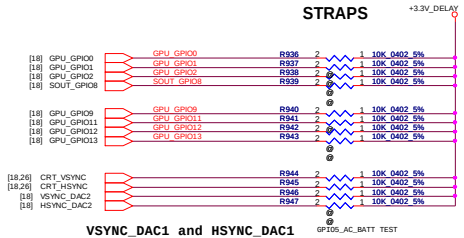


216-0728002 A11 M92-S2_FCBGA631

NOTE:
Change part number directly,
from SA00002ZM10 to SA000030020
M92XT -> LP, 2009/05/20



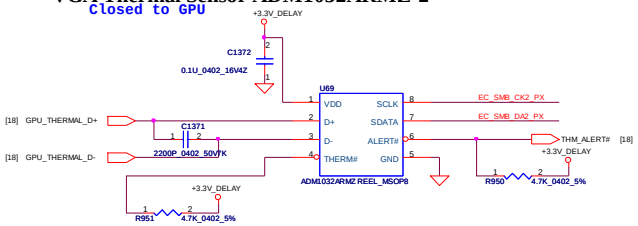
STRAPS



VSYNC_DAC1 and HSYNC_DAC1
pull up to HDMI & DISPLAYPORT
AUDIO funciton

VGA Thermal Sensor ADM1032ARMZ-2

Closed to GPU



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB		1
ROMIDCFG(2:0)	GPIO[13:11]	BIF_RX_PLL_CALIB_BP	0 0
VIP_DEVICE_STRAP_ENA	V2SYNC	ENABLE EXTERNAL BIOS ROM	0
SMS_EN_HARD	H2SYNC	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0
CCBYPASS	GENERICC	IGNORE VIP DEVICE STRAPS	0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO	GPIO21_BB_EN

STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 2,1,0
VRAM_ID[2:0]	DVIDATA 3,2,1	M92 S2-XT	JM51_PU	512MB(x4)	Samsung 64Mx16x4 DDR3	SA000035700	1 0 0
			JM51_PU	256MB(X2)	Samsung 64Mx16x2 DDR3		1 0 1
			JM51_PU	512MB(x4)	Hynix 64Mx16x4 DDR3	SA000032400	0 0 0
			JM51_PU	256MB(X2)	Hynix 64Mx16x2 DDR3		0 1 0

Security Classification	Compal Secret Data		
Issued Date	2009/04/20	Deciphered Date	2010/04/30

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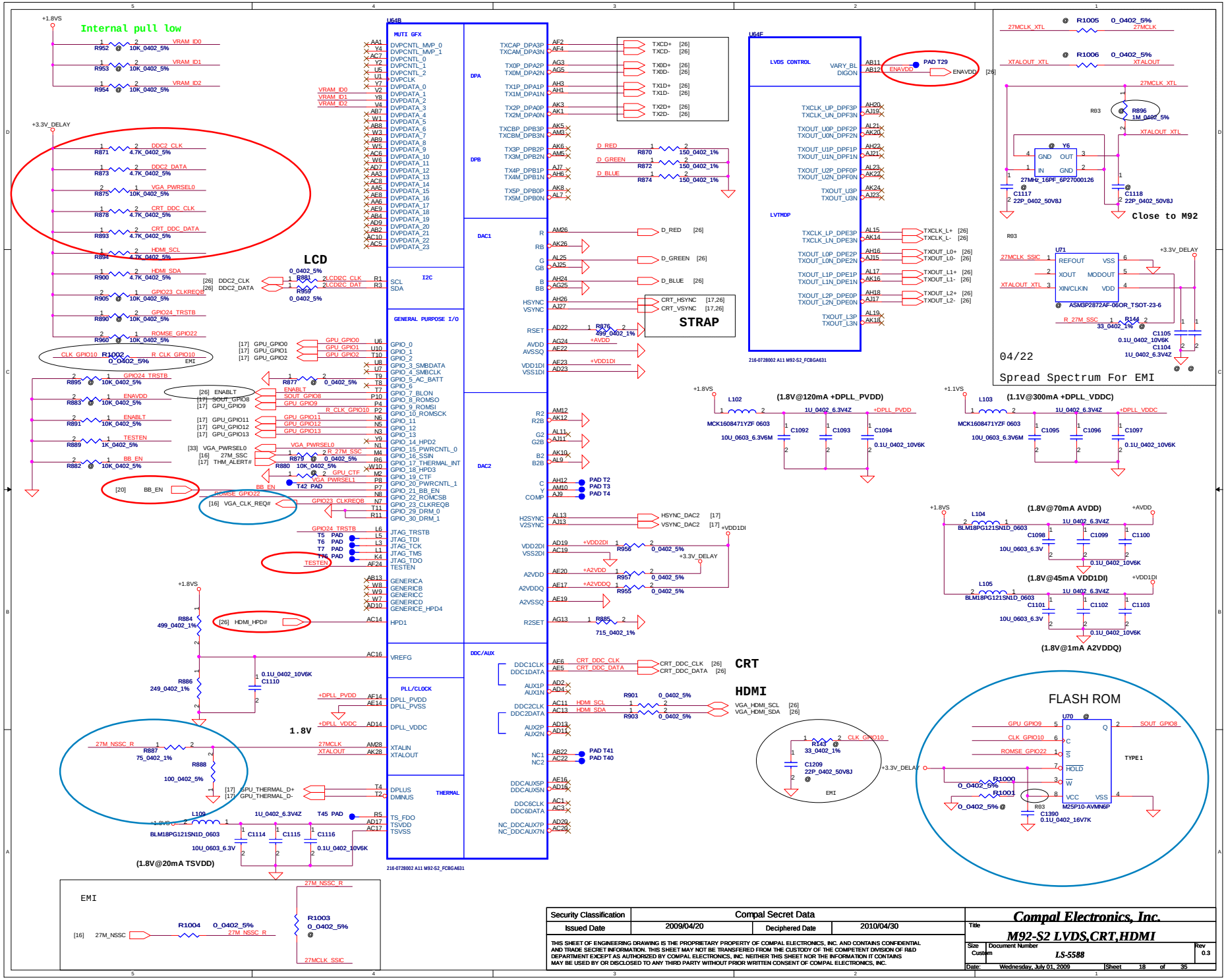
Compal Electronics, Inc.

Title: M92-S2 PCIE,STRAP

Size: Custom | Document Number: LS-5588 | Rev: 0.3

Date: Wednesday, July 01, 2009 | Sheet 17 of 35



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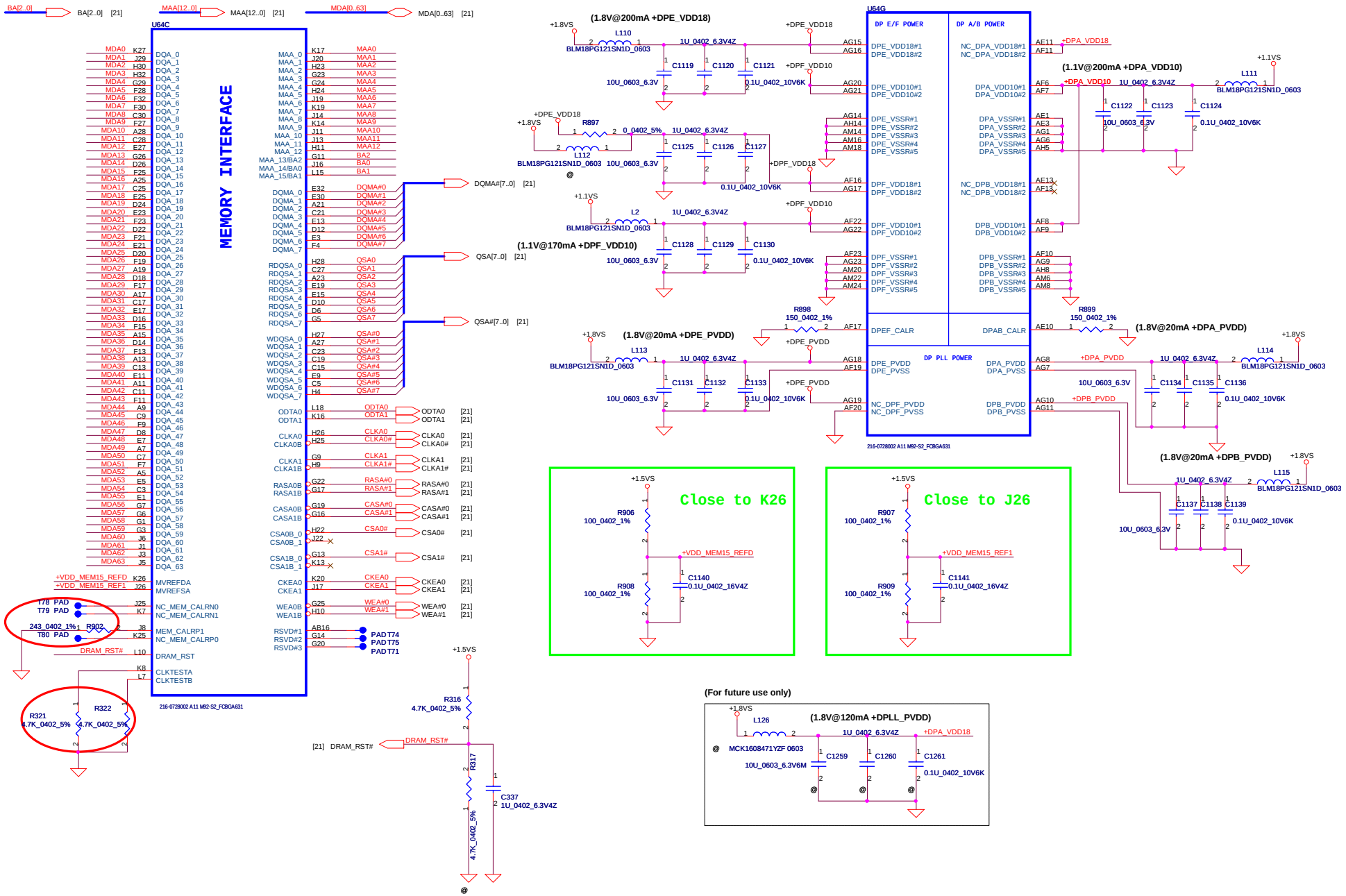
Compal Electronics, Inc.

Title: **M92-S2 LVDS,CRT,HDMI**

Size	Document Number	Rev
Custom	LS-5588	0.3

Date: Wednesday, July 01, 2009 | Sheet 18 of 35



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Issued Date	2009/04/20	Deciphered Date	2010/04/30

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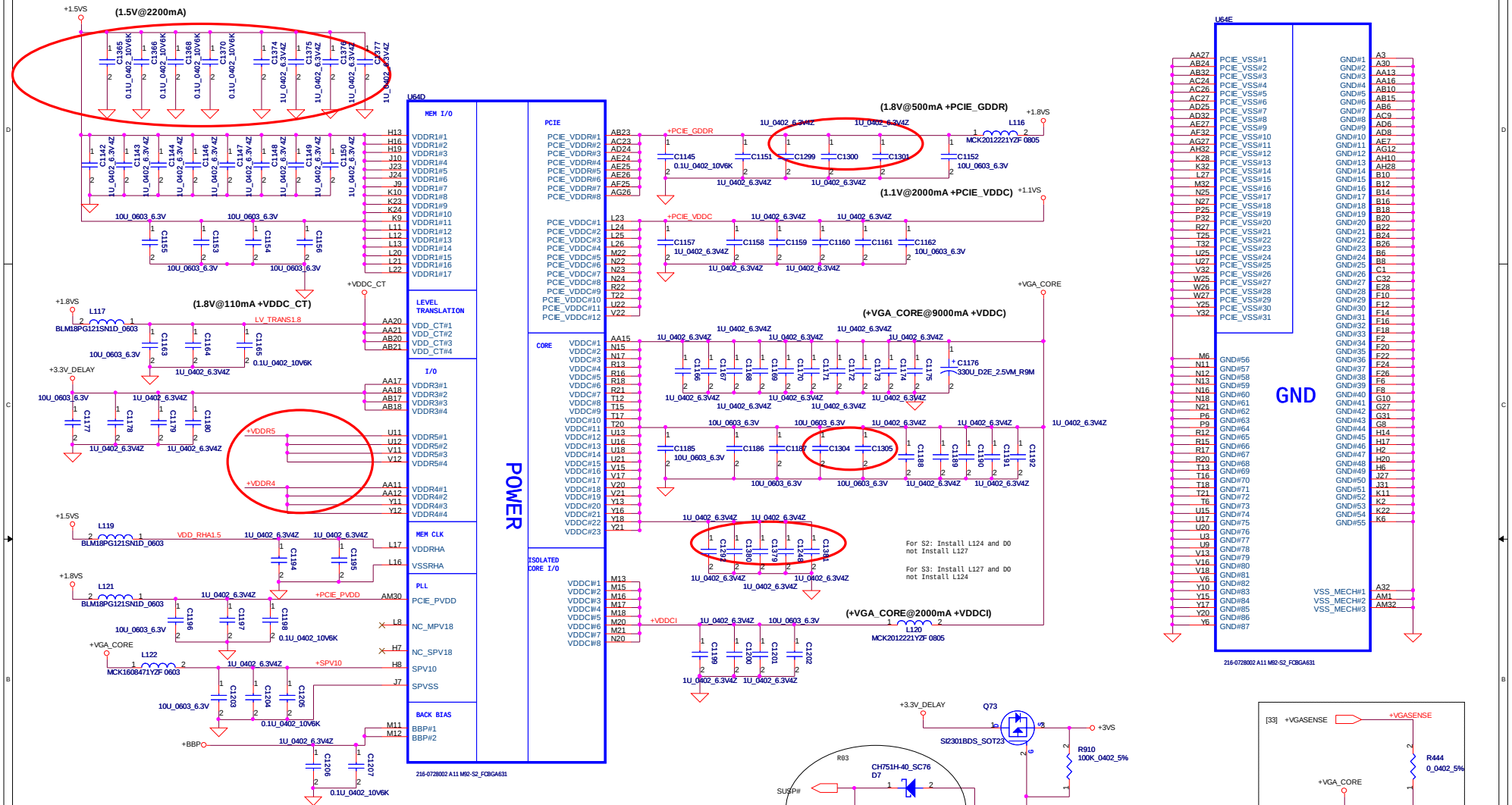
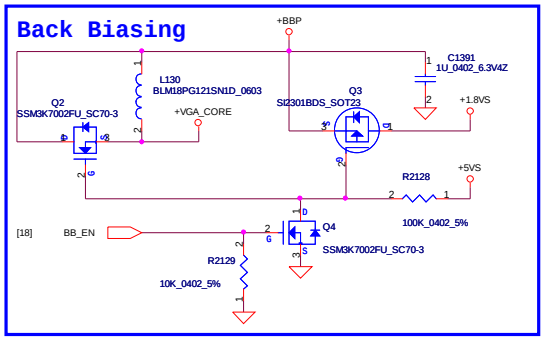
Compal Electronics, Inc.

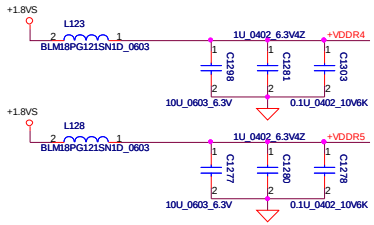
Title: **M92-S2 MEMORY**

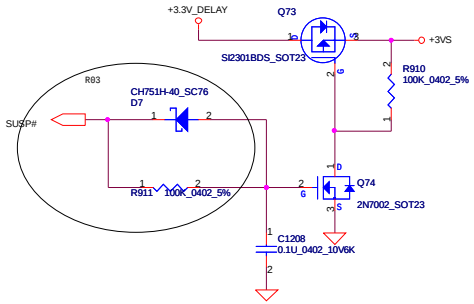
Size: Custom | Document Number: LS-5588 | Rev: 0.3

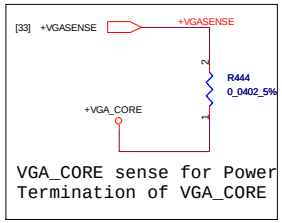
Date: Wednesday, July 01, 2009 | Sheet 19 of 35











BB_EN=0V, for Back Biasing Disabled, Q2004=OFF, Q2005=OFF and Q2006=ON, +BBP=+GPU_CORE
BB_EN=+3.3V, for Back Biasing Enabled, Q2004=ON, Q2005=ON and Q2006=OFF, +BBP=+1.8VSDGPU

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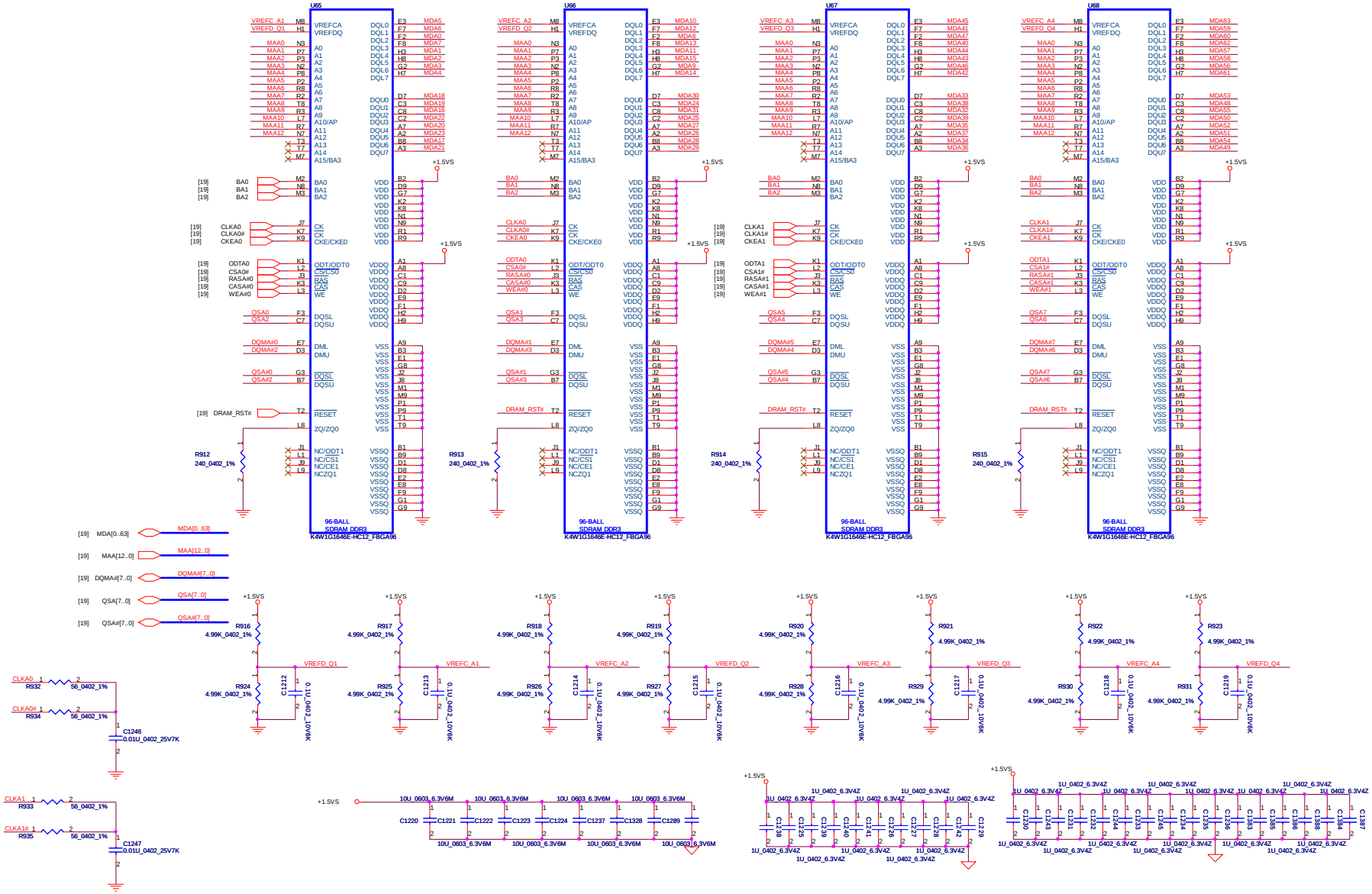
Compal Electronics, Inc.

Title: **M92-S2 PWR,GND**

Size	Document Number	Rev
B	LS-5588	0.3

Date: Wednesday, July 01, 2009 | Sheet 20 of 35



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Issued Date	2009/04/20	Deciphered Date	2010/04/30

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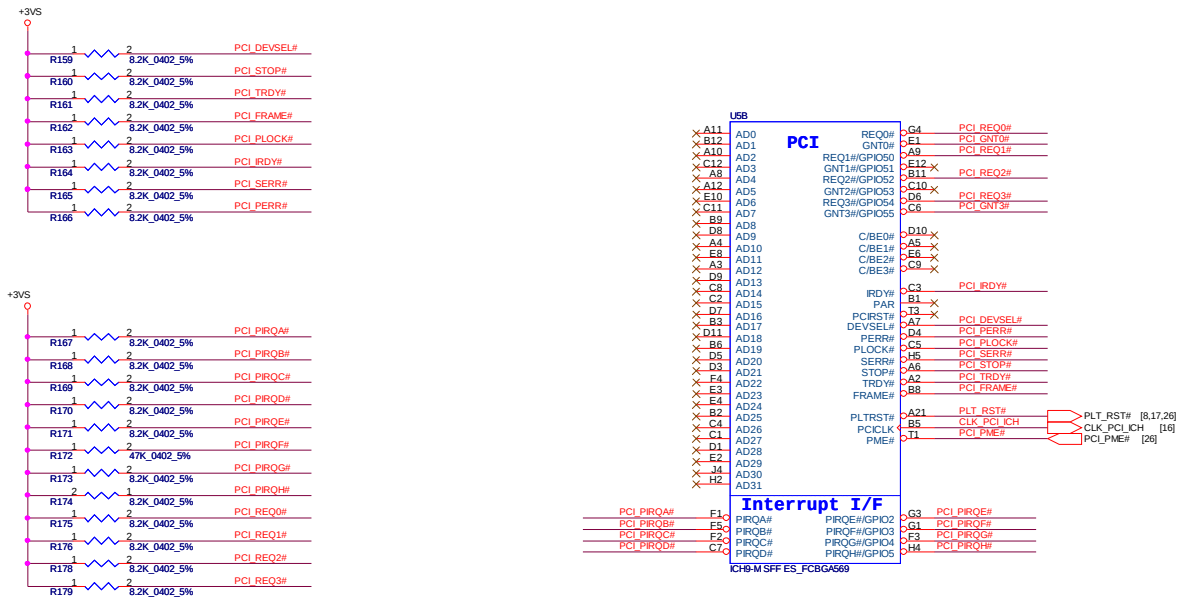
Compal Electronics, Inc.

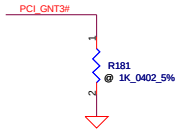
Title: **VRAM DDR3**

Size	Document Number	Rev
C	LS-5588	0.3

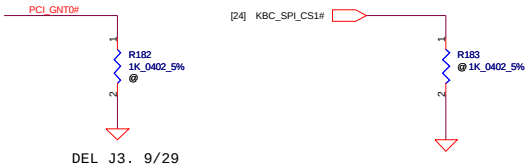
Date: Wednesday, July 01, 2009 Sheet 21 of 35



A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *

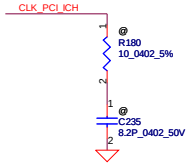


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



DEL J3. 9/29

Place closely pin B10



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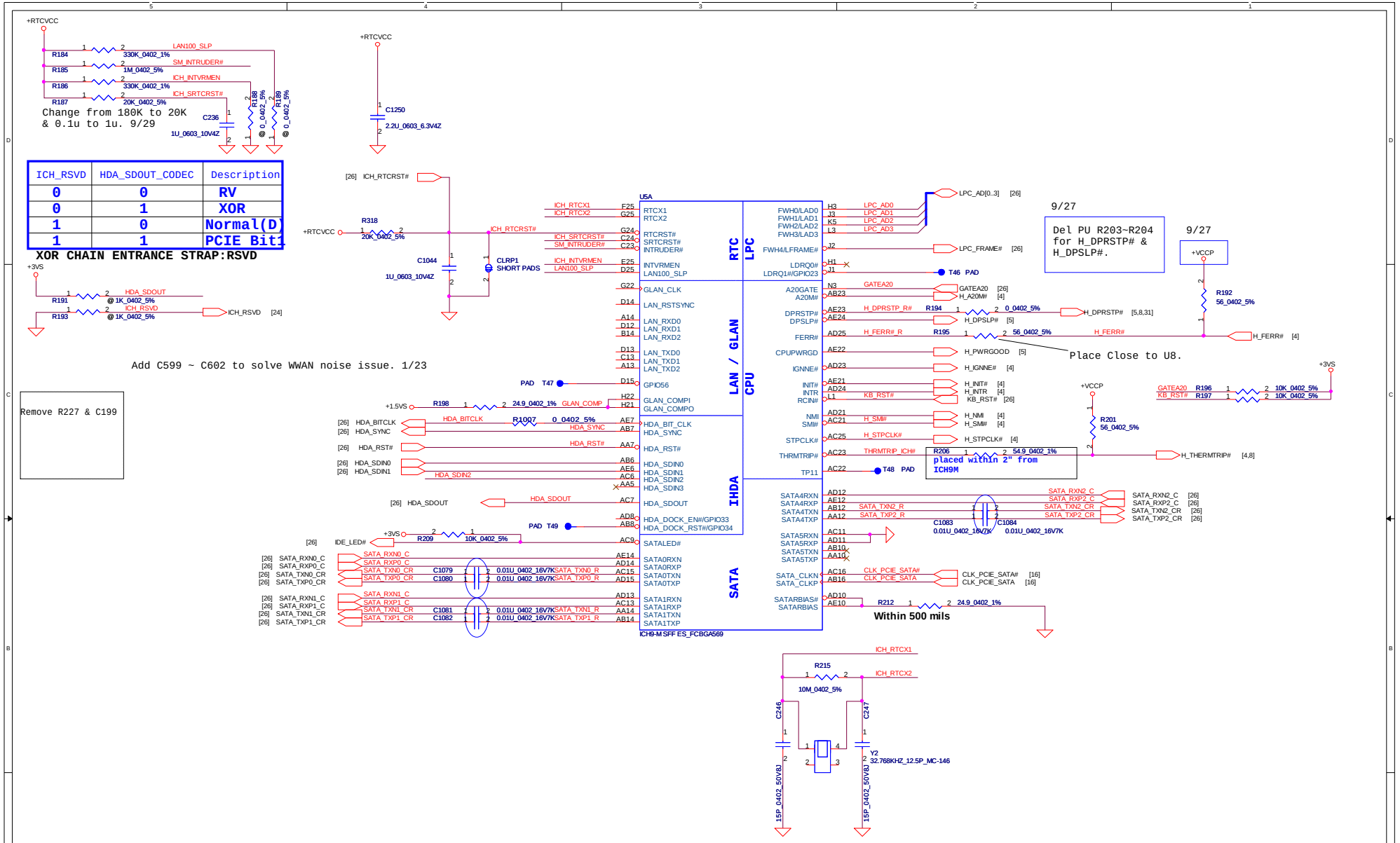
Compal Electronics, Inc.

Title: ICH9(1/4)-PCI/INT

Size | Document Number: LS-5588 | Rev: 0.3

Date: Wednesday, July 01, 2009 | Sheet 22 of 35



Security Classification	Compal Secret Data		
Issued Date	2009/04/20	Deciphered Date	2010/04/30

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Compal Electronics, Inc.

Title: ICH9(2/4)_LAN,HD,IDE,LPC

Size	Document Number	Rev
Custom	LS-5588	0.3

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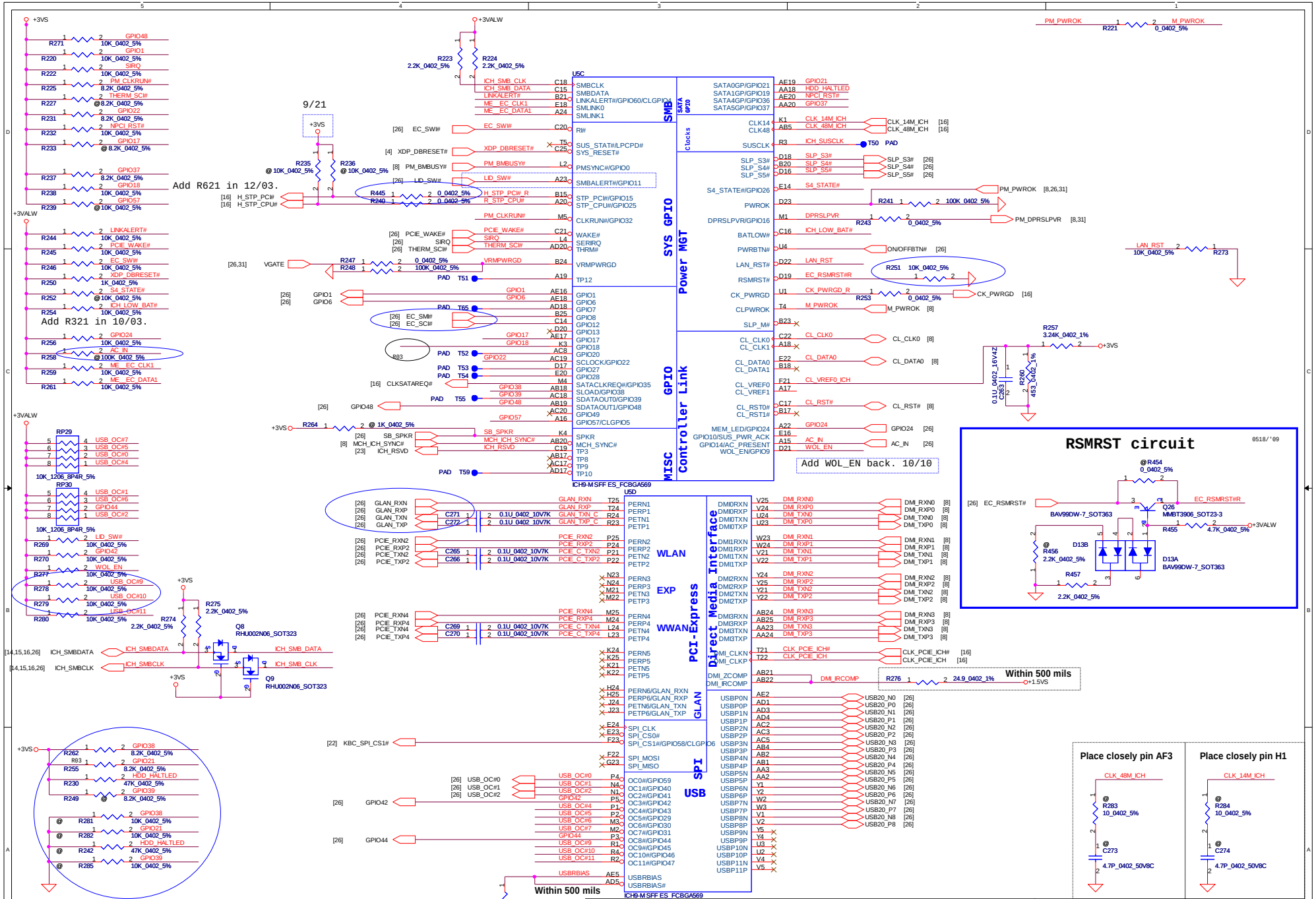
U5C
ICH9-M SFF ES_FCBGA569
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
Clocks
SATA GPIO
U5D
WLAN
EXP
WWAN
PCI-Express
Direct Media Interface
GLAN
SPI
USB
Add R621 in 12/03.
Add R321 in 10/03.
Add WOL_EN back. 10/10
9/21
RSMRST circuit
Q26 MMBT3906_SOT23-3
BAV99DW-7_SOT363
Q8 RHU002N06_SOT323
Q9 RHU002N06_SOT323
Within 500 mils
Place closely pin AF3
Place closely pin H1
CLK_48M_ICH
CLK_14M_ICH
Compal Secret Data
Issued Date 2009/04/20
Deciphered Date 2010/04/30
Compal Electronics, Inc.
ICH9(3/4)_DMI,USB,GPIO,PCIE
LS-5588
Wednesday, July 01, 2009
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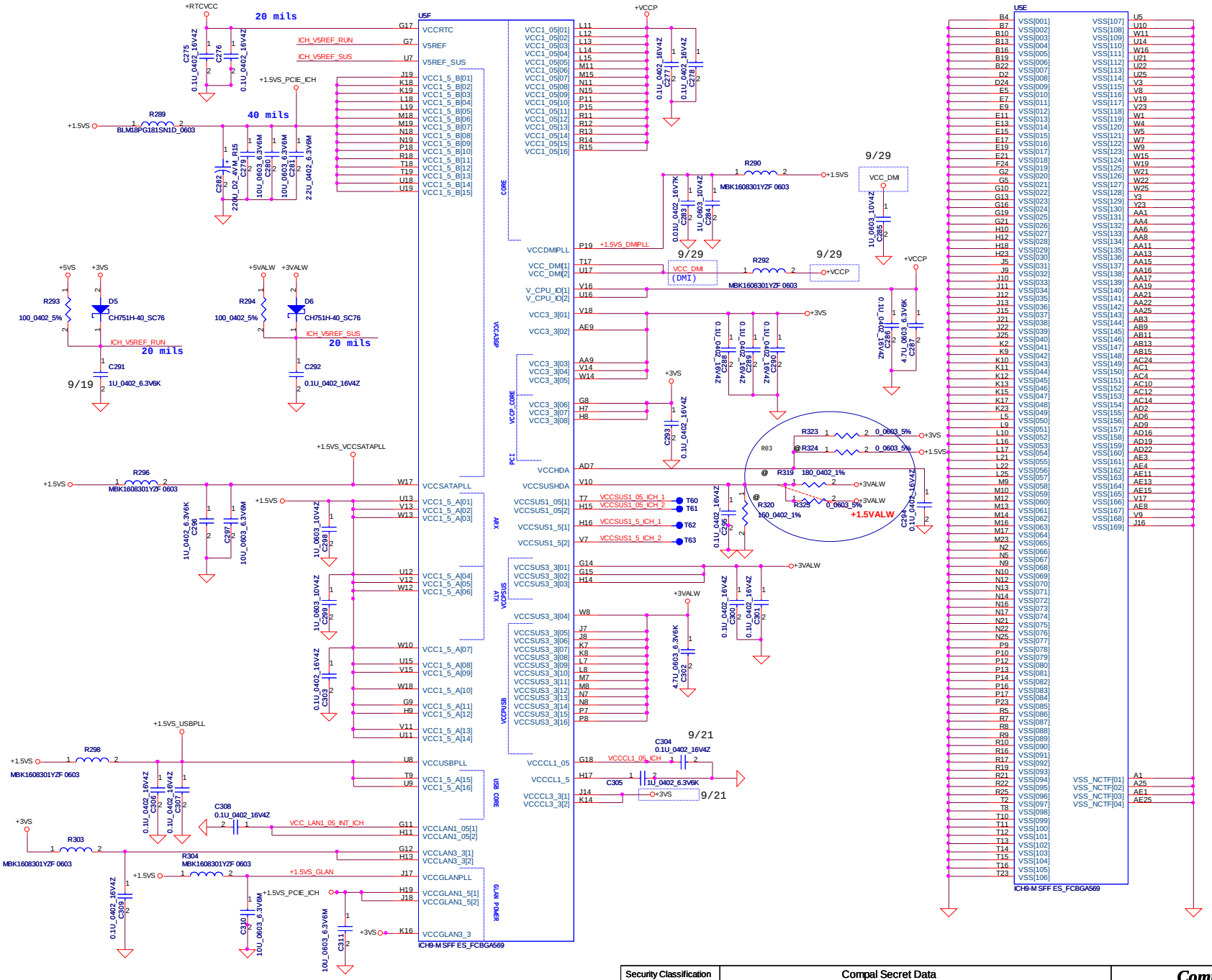

Security Classification	Compal Secret Data		
Issued Date	2009/04/20	Deciphered Date	2010/04/30

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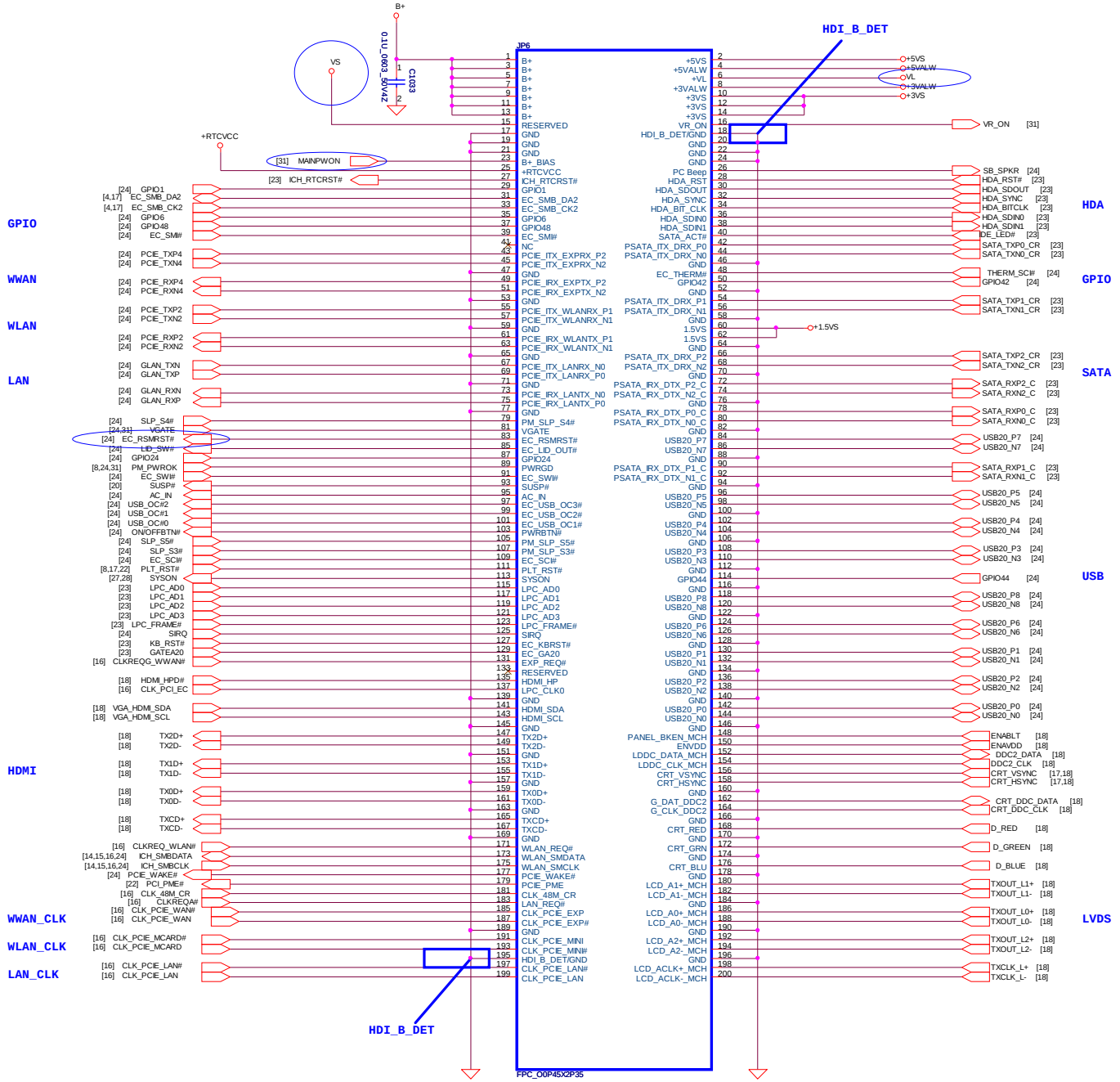
Compal Electronics, Inc.

Title: **ICH9(4/4)_POWER&GND**

Size	Document Number	Rev
Custom	LS-5588	0.3

Date: Wednesday, July 01, 2009 | Sheet 25 of 35



Security Classification	Compal Secret Data		
Issued Date	2009/04/20	Deciphered Date	2010/04/30

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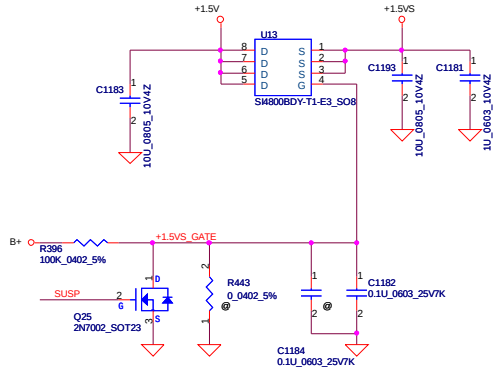
Compal Electronics, Inc.

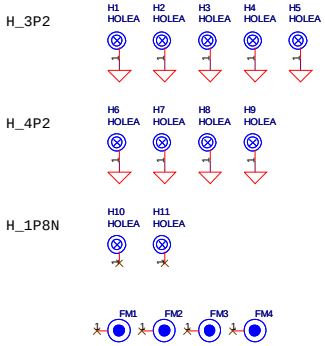
Title: **Golden finger**

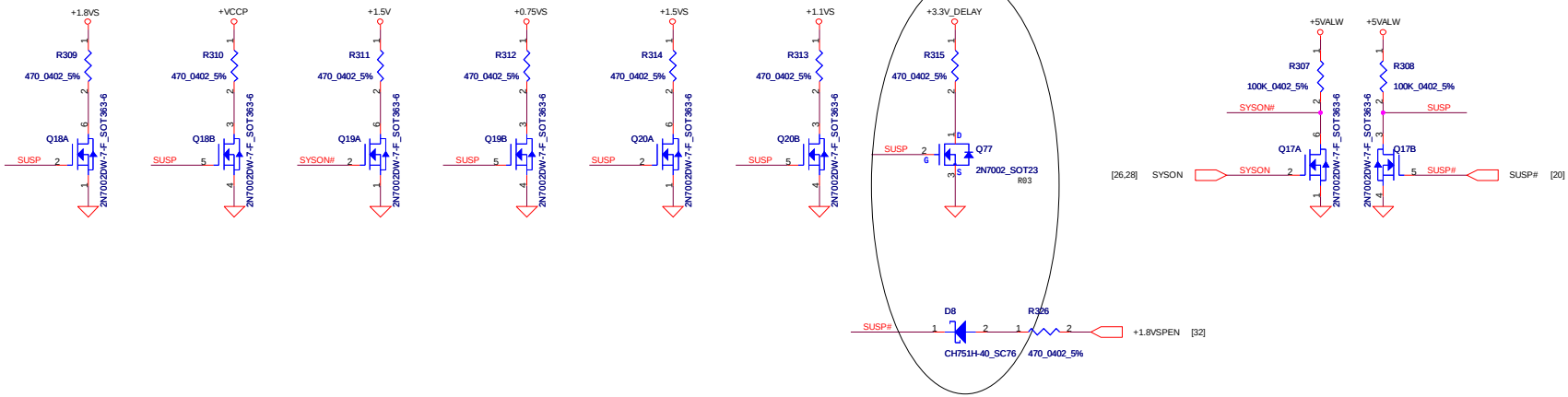
Size	Document Number	Rev
	LS-5588	0.3

Date: Wednesday, July 01, 2009 | Sheet 26 of 35

+1.5V to +1.5VS







Security Classification	Compal Secret Data		
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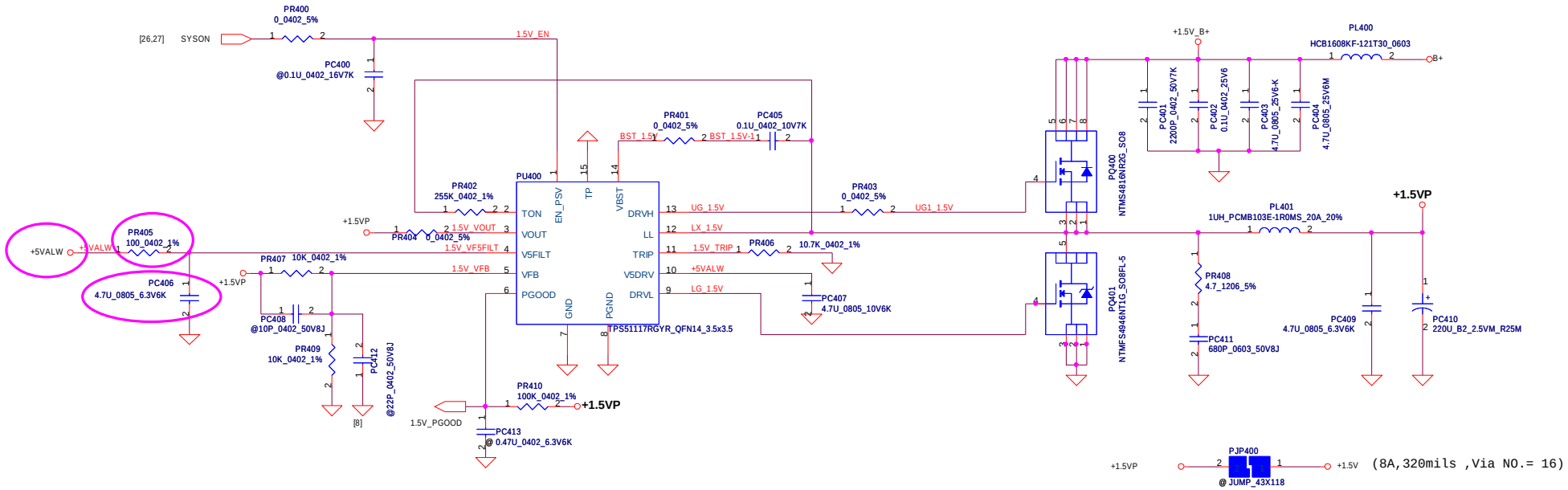
Compal Electronics, Inc.

Title: **DC/DC Interface**

Size	Document Number	Rev
Custom	LS-5588	0.3

Date: Wednesday, July 01, 2009 | Sheet 27 of 35



Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

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Compal Electronics, Inc.

Title: **1.5VP**

Size | Document Number: *LS5588P* | Rev: 0.3

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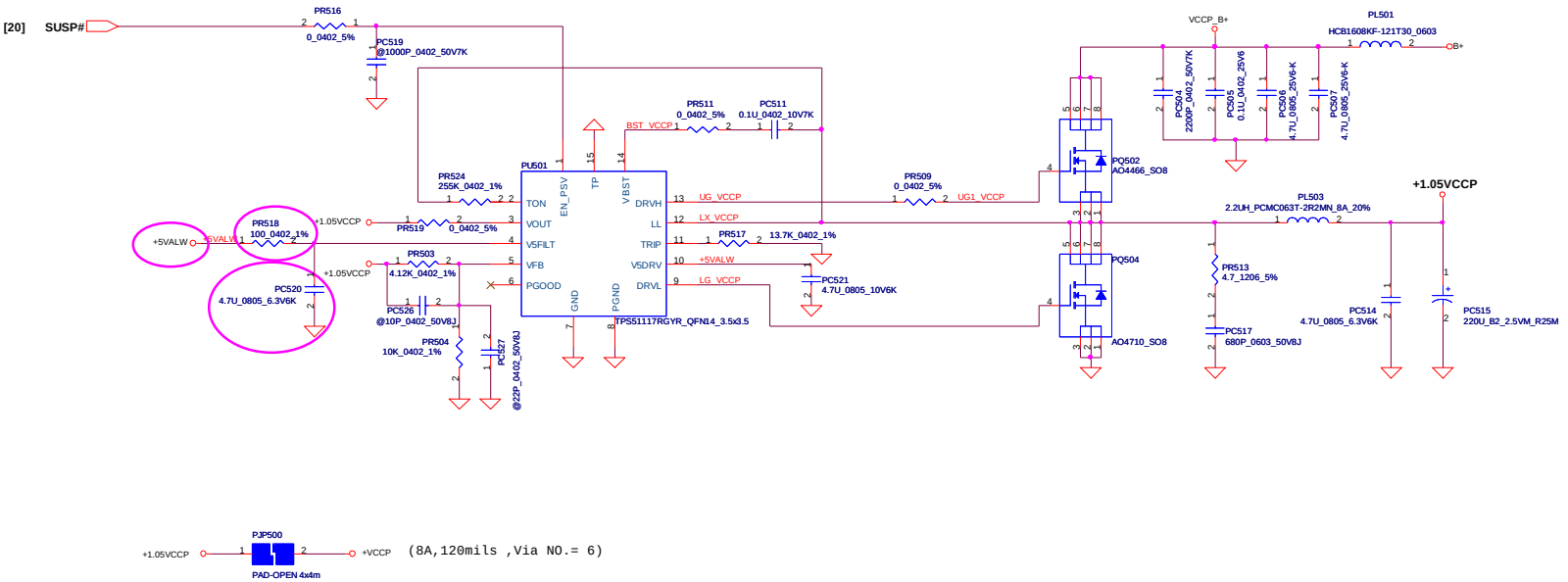

(8A,120mils ,Via NO.= 6)

Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

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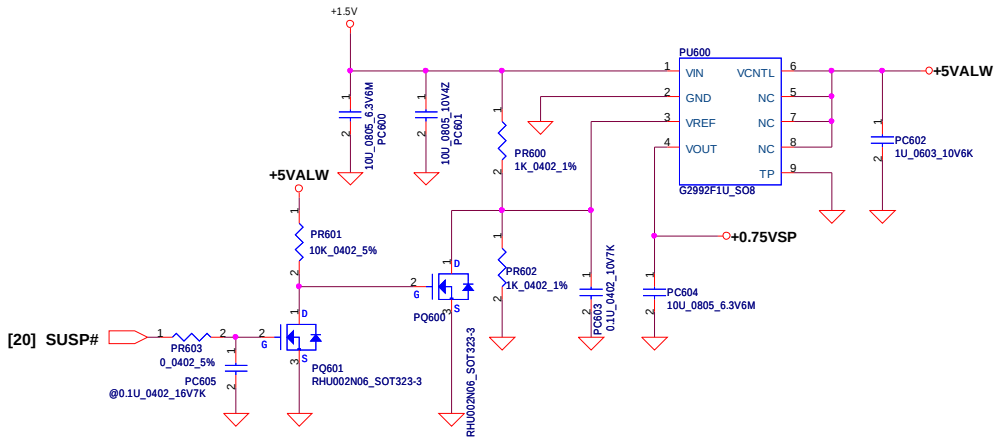
Compal Electronics, Inc.

Title: **1.05VCCP**

Size | Document Number: *LS5588P* | Rev: 0.3

Date: Wednesday, July 01, 2009 | Sheet 29 of 35



(2A,80mils ,Via NO.= 4)

Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

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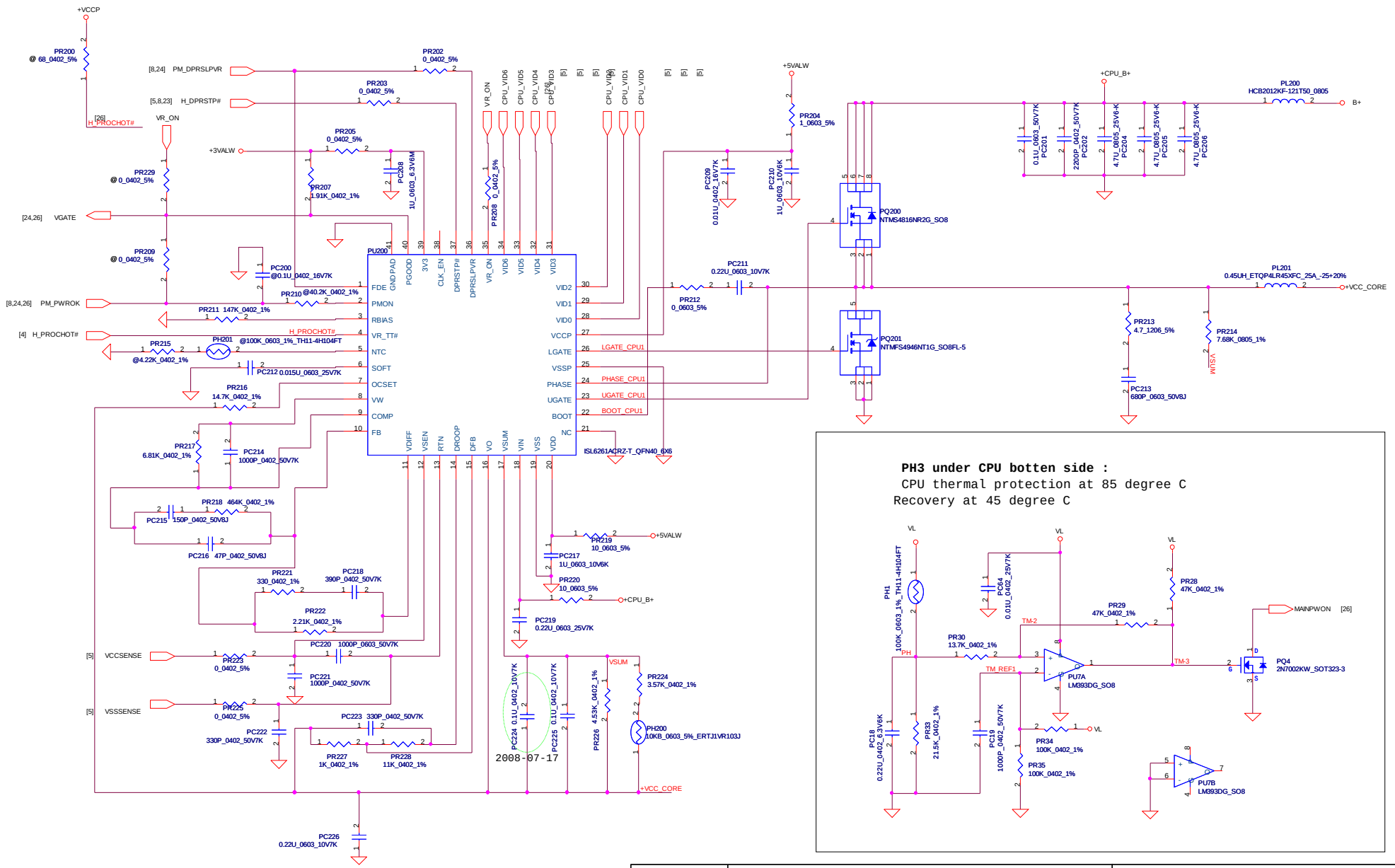
Compal Electronics, Inc.

Title: **0.75VSP**

Size | Document Number: *LS5588P* | Rev: 0.3

Date: Wednesday, July 01, 2009 | Sheet 30 of 35



Security Classification	Compal Secret Data		
Issued Date	2005/06/23	Deciphered Date	2006/10/22

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Title: CPU_CORE

Size: Custom | Document Number: IAX00 | Rev: 0.3

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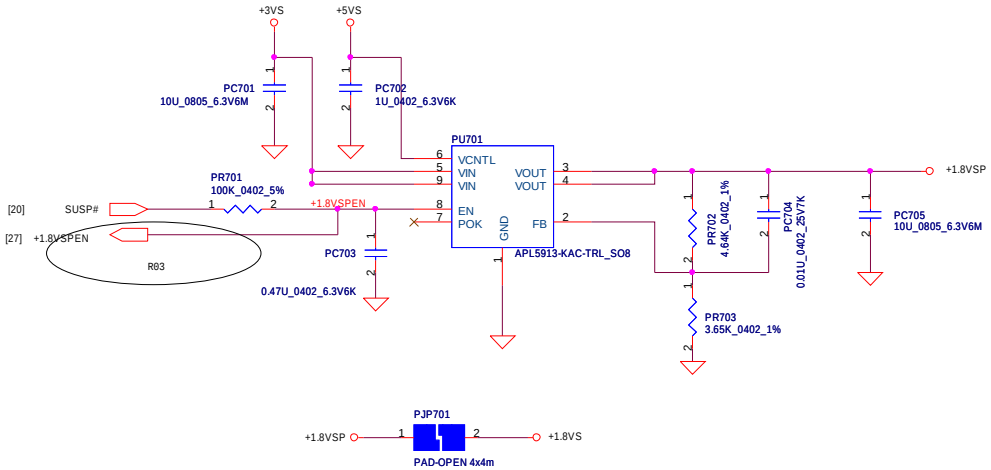

Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

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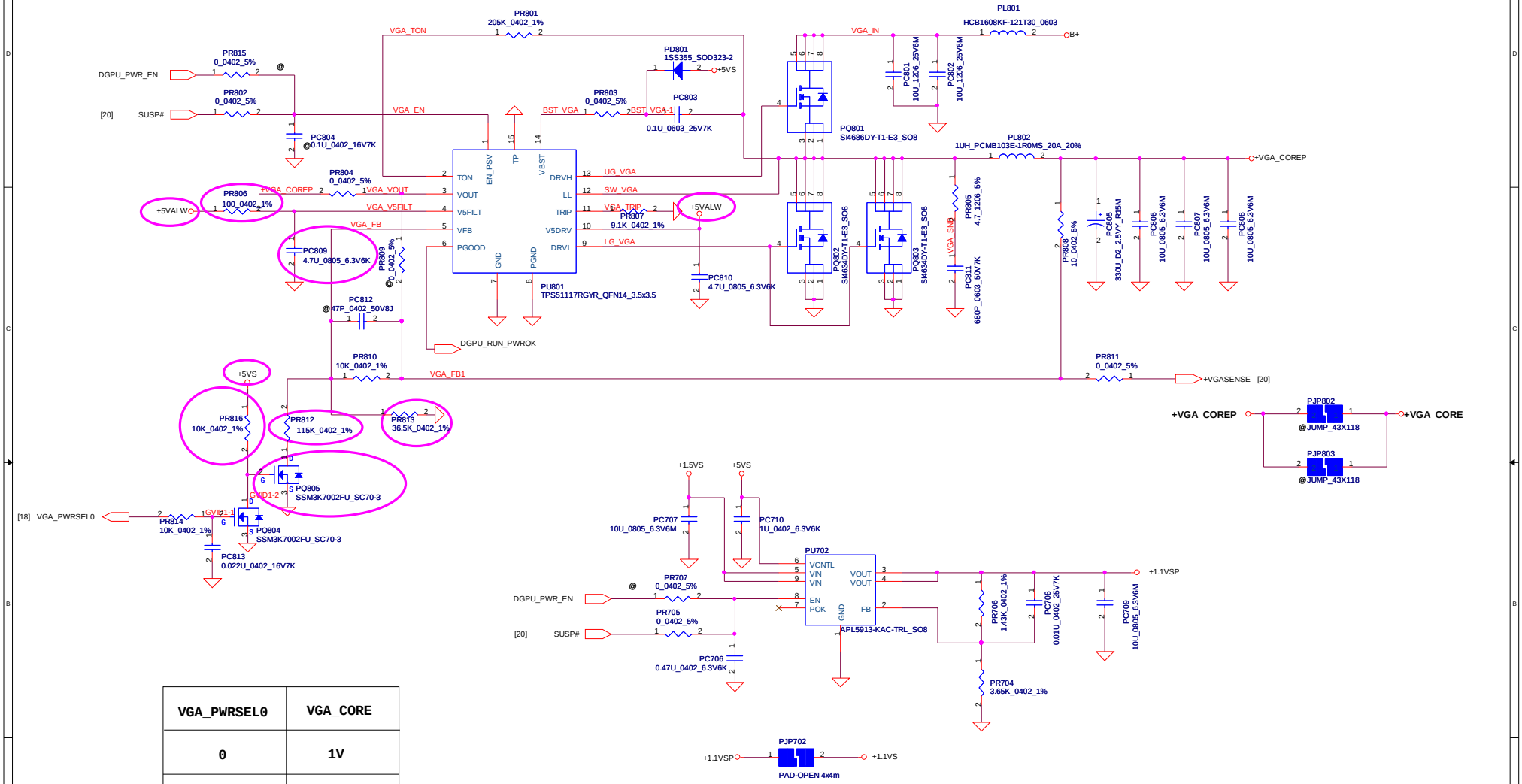
Compal Electronics, Inc.

Title: **1.8VSP**

Size | Document Number: *LS5588P* | Rev: 0.3

Date: Wednesday, July 01, 2009 | Sheet 32 of 35



VGA_PWRSEL0	VGA_CORE
0	1V
1	0.95V

Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

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Compal Electronics, Inc.

Title: VGA_CORE/1.1V

Size | Document Number | Rev 0.3

Date: Wednesday, July 01, 2009 | Sheet 33 of 35

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
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21							
22							

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

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Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: <Doc> | Rev: 0.3

Date: Wednesday, July 01, 2009 | Sheet 34 of 35

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change OVT Circuit		1.0		add PU7,PH1,PC18,PC19,PC64,PR33,PR30,PR34,PR35,PR29,PR28,PQ4		
2							
3							
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22							

Security Classification	Compal Secret Data		
Issued Date	2009/04/20	Deciphered Date	2010/04/30

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Title: **HW Changed-List History-1**

Size | Document Number: *LS-5588* | Rev: 0.3

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