

Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M SFF core logic

ULV core logic HDI board

DISCRETE VGA M92

2009-06-19 V.03

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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				Size Custom	Document Number LS-5588	Rev 0.3
				Date: Wednesday, July 01, 2009	Sheet 1	of 35

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Model Name : NAW20

File Name : LS-5588P

ULV

Thermal Sensor

page 4

Mobile Peryn

LV/ULV Dual Core
uFCPGA-956 CPU - SFF

page 4, 5, 6, 7

CK505

Clock Generator
ICS9LPRS387BKLFT
MLF 72P

page 16



H_{A#}(3..35)
H_{D#}(0..63)

FSB

667/800/1066MHz 1.05V

Intel Cantiga GS

FCBGA 1363 - SFF

page 8, 9, 10, 11, 12, 13

DDR3 1066MHz 1.5V

Dual Channel

DDR3-SO-DIMM X 2

BANK 0, 1, 2, 3

page 14, 15

DMI X4

Intel ICH9-M

WBMMAP-569 - SFF

page 22, 23, 24, 25

HDA

Golden finger

HDI to I/O board

page 26

HDMI

CRT

LVDS

LPC

PCIE

USB

SATA

ODD

HDD

ESATA

CardReader

USB*2

BT

CMOS

minIPCE*2

LAN

minIPCE*1

I/O BRD PORTION

EC

HDA

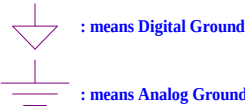
AUDIO

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Voltage Rails (0 MEANS ON X MEANS OFF)

power plane State	+B +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75VS +VCCP +CPU_CORE +VGA_CORE +1.1VS +1.8VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



@ : means just reserve , no build
ME@ : means ME part.
45@ : means install after SMT.

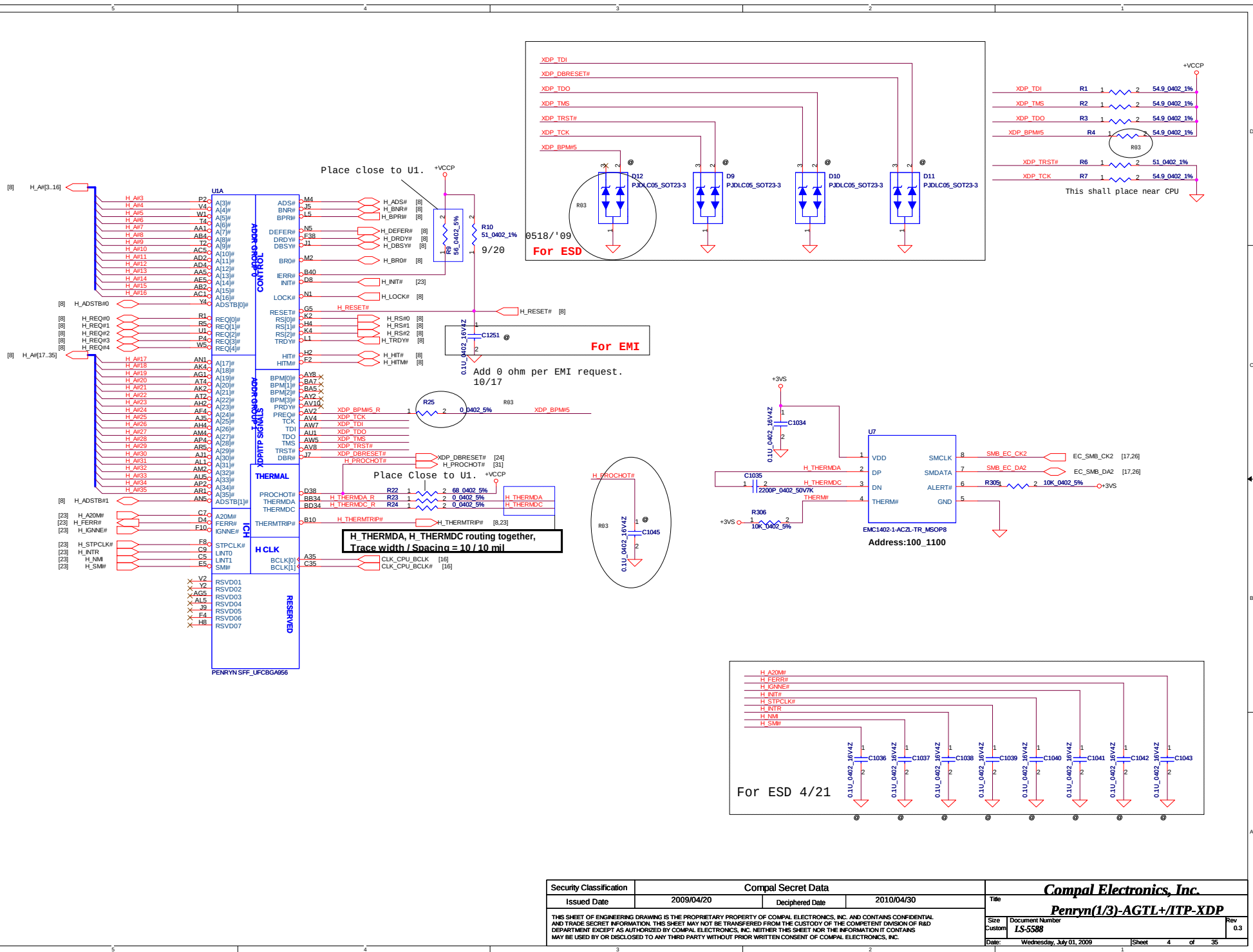
SMBUS Control Table

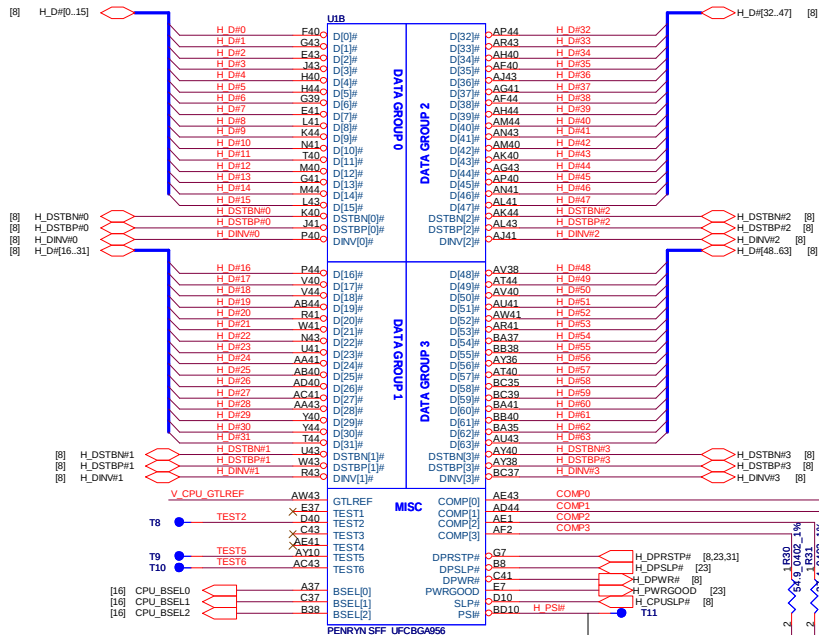
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CLK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CLK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CLK_CLK1 SMB_CLK_DAY1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAY	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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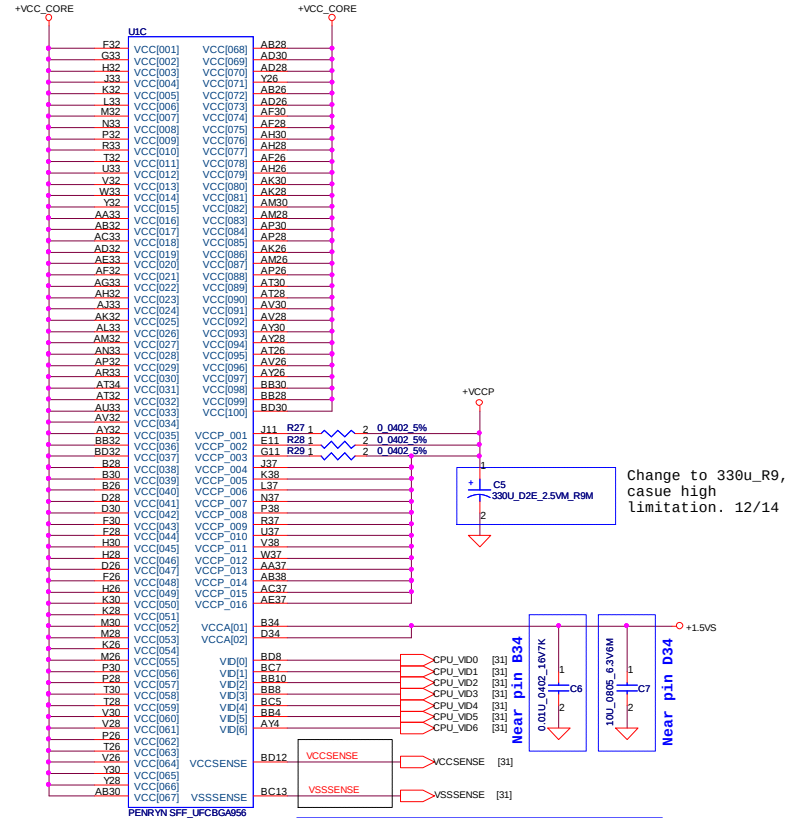


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

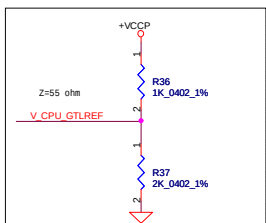
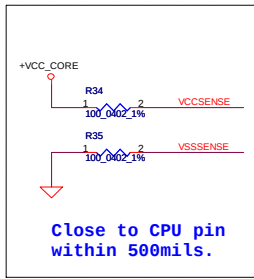
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02

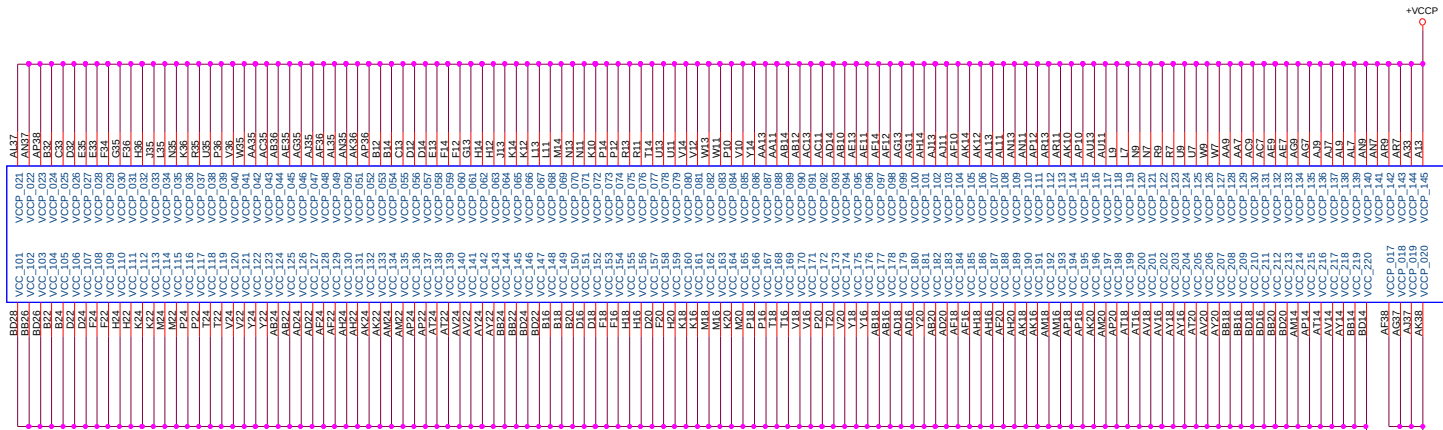
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.



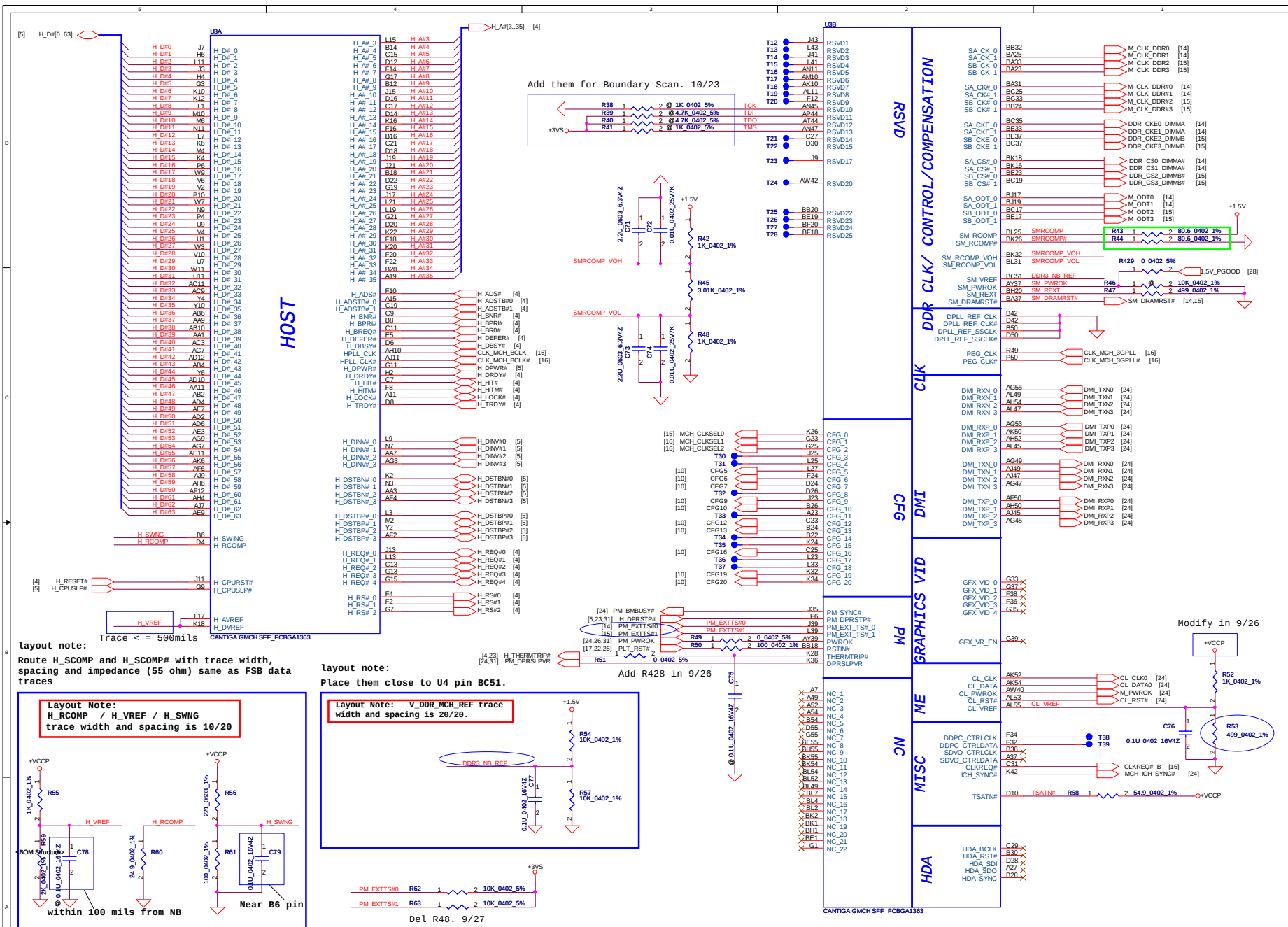
Close to CPU pin AW43 within 500mils.



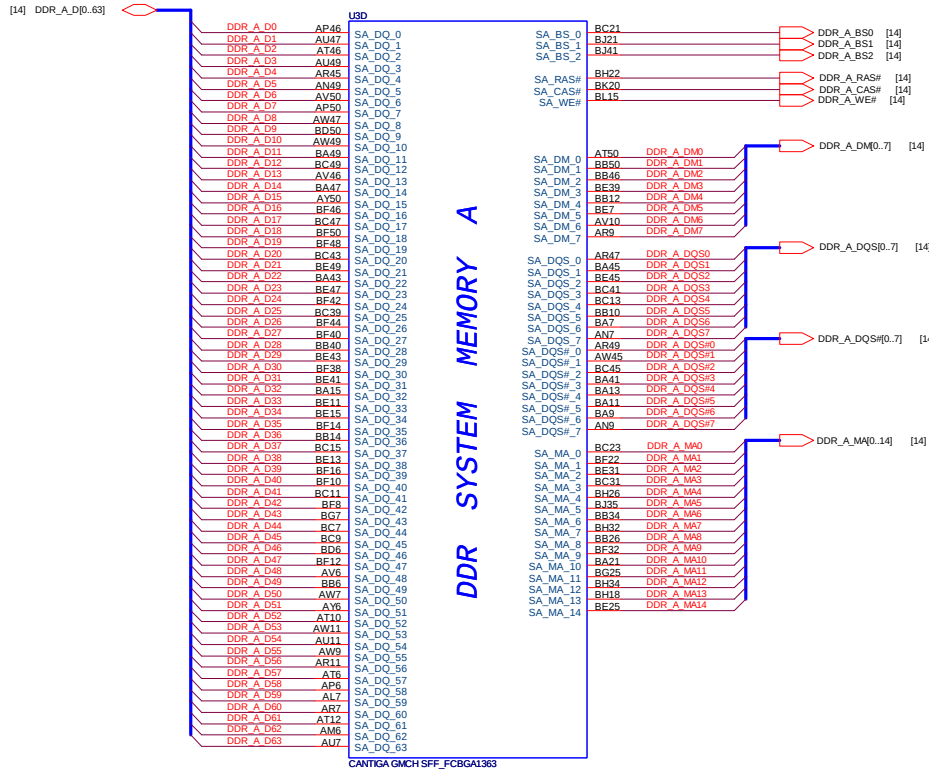
U1F
PENRYN SFF_UFCBG956

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				Penryn(3/3)-Power	
				Size	Document Number
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UID	UIDE	UIDE
B42	VSS[001]	AM36
F44	VSS[002]	AR35
D44	VSS[003]	AU35
D42	VSS[004]	AV34
F42	VSS[005]	AW35
H42	VSS[006]	AX34
K42	VSS[007]	AY34
M42	VSS[008]	AZ34
T42	VSS[009]	BA33
V42	VSS[010]	BB33
Y42	VSS[011]	BC33
AB42	VSS[012]	BD33
AC42	VSS[013]	BE33
AD42	VSS[014]	BF33
AE42	VSS[015]	BG33
AF42	VSS[016]	BH33
AG42	VSS[017]	BI33
AH42	VSS[018]	BJ33
AI42	VSS[019]	BK33
AM42	VSS[020]	BL33
AN42	VSS[021]	BM33
AO42	VSS[022]	BN33
AP42	VSS[023]	BO33
AV44	VSS[024]	BP33
AW44	VSS[025]	BQ33
AX44	VSS[026]	BR33
AY44	VSS[027]	BS33
AZ44	VSS[028]	BT33
BA44	VSS[029]	BU33
BB44	VSS[030]	BV33
BC44	VSS[031]	BW33
BD44	VSS[032]	BX33
BE44	VSS[033]	BY33
BF44	VSS[034]	BZ33
BG44	VSS[035]	CA32
BH44	VSS[036]	CB32
BI44	VSS[037]	CC32
BJ44	VSS[038]	CD32
BK44	VSS[039]	CE32
BL44	VSS[040]	CF32
BM44	VSS[041]	CG32
BN44	VSS[042]	CH32
BO44	VSS[043]	CI32
BP44	VSS[044]	CJ32
BQ44	VSS[045]	CK32
BR44	VSS[046]	CL32
BS44	VSS[047]	CM32
BT44	VSS[048]	CN32
BU44	VSS[049]	CO32
BV44	VSS[050]	CP32
BW44	VSS[051]	CQ32
BX44	VSS[052]	CR32
BY44	VSS[053]	CS32
BZ44	VSS[054]	CT32
CA44	VSS[055]	CU32
CB44	VSS[056]	CV32
CC44	VSS[057]	CW32
CD44	VSS[058]	CX32
CE44	VSS[059]	CY32
CF44	VSS[060]	CZ32
CG44	VSS[061]	DA31
CH44	VSS[062]	DB31
CI44	VSS[063]	DC31
CJ44	VSS[064]	DD31
CK44	VSS[065]	DE31
CL44	VSS[066]	DF31
CM44	VSS[067]	DG31
CN44	VSS[068]	DH31
CO44	VSS[069]	DI31
CP44	VSS[070]	DJ31
CQ44	VSS[071]	DK31
CR44	VSS[072]	DL31
CS44	VSS[073]	DM31
CT44	VSS[074]	DN31
CU44	VSS[075]	DO31
CV44	VSS[076]	DP31
CW44	VSS[077]	DQ31
CX44	VSS[078]	DR31
CY44	VSS[079]	DS31
CZ44	VSS[080]	DT31
DA44	VSS[081]	DU31
DB44	VSS[082]	DV31
DC44	VSS[083]	DW31
DD44	VSS[084]	DX31
DE44	VSS[085]	DY31
DF44	VSS[086]	DZ31
DG44	VSS[087]	EA30
DH44	VSS[088]	EB30
DI44	VSS[089]	EC30
DJ44	VSS[090]	ED30
DK44	VSS[091]	EE30
DL44	VSS[092]	EF30
DM44	VSS[093]	EG30
DN44	VSS[094]	EH30
DO44	VSS[095]	EI30
DP44	VSS[096]	EJ30
DQ44	VSS[097]	EK30
DR44	VSS[098]	EL30
DS44	VSS[099]	EM30
DT44	VSS[100]	EN30
DU44	VSS[101]	EO30
DV44	VSS[102]	EP30
DW44	VSS[103]	EQ30
DX44	VSS[104]	ER30
DY44	VSS[105]	ES30
DZ44	VSS[106]	ET30
EA44	VSS[107]	EU30
EB44	VSS[108]	EV30
EC44	VSS[109]	EW30
ED44	VSS[110]	EX30
EE44	VSS[111]	EY30
EF44	VSS[112]	EZ30
EG44	VSS[113]	FA29
EH44	VSS[114]	FB29
EI44	VSS[115]	FC29
EJ44	VSS[116]	FD29
EK44	VSS[117]	FE29
EL44	VSS[118]	FF29
EM44	VSS[119]	FG29
EN44	VSS[120]	FH29
EO44	VSS[121]	FI29
EP44	VSS[122]	FJ29
EQ44	VSS[123]	FK29
ER44	VSS[124]	FL29
ES44	VSS[125]	FM29
ET44	VSS[126]	FN29
EU44	VSS[127]	FO29
EV44	VSS[128]	FP29
EW44	VSS[129]	FQ29
EX44	VSS[130]	FR29
EY44	VSS[131]	FS29
EZ44	VSS[132]	FT29
FA44	VSS[133]	FU29
FB44	VSS[134]	FV29
FC44	VSS[135]	FW29
FD44	VSS[136]	FX29
FE44	VSS[137]	FY29
FF44	VSS[138]	FZ29
FG44	VSS[139]	GA28
GH44	VSS[140]	GB28
GI44	VSS[141]	GC28
GO44	VSS[142]	GD28
GP44	VSS[143]	GE28
GQ44	VSS[144]	GF28
GR44	VSS[145]	GG28
GS44	VSS[146]	GH28
GT44	VSS[147]	GI28
GU44	VSS[148]	GJ28
GV44	VSS[149]	GK28
GW44	VSS[150]	GL28
GX44	VSS[151]	GM28
GY44	VSS[152]	GN28
GZ44	VSS[153]	GO28
HA28	VSS[154]	HP28
HB28	VSS[155]	HQ28
HC28	VSS[156]	HR28
HD28	VSS[157]	HS28
HE28	VSS[158]	HT28
HF28	VSS[159]	HU28
HG28	VSS[160]	HV28
HH28	VSS[161]	HW28
HI28	VSS[162]	HX28
HJ28	VSS[163]	HY28
HK28	VSS[164]	HZ28
HL28	VSS[165]	IA27
HM28	VSS[166]	IB27
HN28	VSS[167]	IC27
HO28	VSS[168]	ID27
HP28	VSS[169]	IE27
HQ28	VSS[170]	IF27
HR28	VSS[171]	IG27
HS28	VSS[172]	IH27
HT28	VSS[173]	II27
HU28	VSS[174]	IJ27
HV28	VSS[175]	IK27
HW28	VSS[176]	IL27
HX28	VSS[177]	IM27
HY28	VSS[178]	IN27
HZ28	VSS[179]	IO27
IA27	VSS[180]	IP27
IB27	VSS[181]	IQ27
IC27	VSS[182]	IR27
ID27	VSS[183]	IS27
IE27	VSS[184]	IT27
IF27	VSS[185]	IU27
IG27	VSS[186]	IV27
IH27	VSS[187]	IW27
II27	VSS[188]	IX27
IJ27	VSS[189]	IY27
IK27	VSS[190]	IZ27
IL27	VSS[191]	JA26
IM27	VSS[192]	KB26
IN27	VSS[193]	KC26
IO27	VSS[194]	KD26
IP27	VSS[195]	KE26
IQ27	VSS[196]	KF26
IR27	VSS[197]	KG26
IS27	VSS[198]	KH26
IT27	VSS[199]	KI26
IU27	VSS[200]	KJ26
IV27	VSS[201]	KK26
IW27	VSS[202]	KL26
IX27	VSS[203]	KM26
IY27	VSS[204]	KN26
IZ27	VSS[205]	KO26
JA26	VSS[206]	KP26
KB26	VSS[207]	KQ26
KC26	VSS[208]	KR26
KD26	VSS[209]	KS26
KE26	VSS[210]	KT26
KF26	VSS[211]	KU26
KG26	VSS[212]	KV26
KH26	VSS[213]	KW26
KI26	VSS[214]	KX26
KJ26	VSS[215]	KY26
KK26	VSS[216]	KZ26
KL26	VSS[217]	LA25
KM26	VSS[218]	LB25
KN26	VSS[219]	LC25
KO26	VSS[220]	LD25
KP26	VSS[221]	LE25
KQ26	VSS[222]	LF25
KR26	VSS[223]	LG25
KS26	VSS[224]	LH25
KT26	VSS[225]	LI25
KU26	VSS[226]	LJ25
KV26	VSS[227]	LK25
KW26	VSS[228]	LM25
KX26	VSS[229]	LN25
KY26	VSS[230]	LO25
KZ26	VSS[231]	LP25
LA25	VSS[232]	LQ25
LB25	VSS[233]	LR25
LC25	VSS[234]	LS25
LD25	VSS[235]	LT25
LE25	VSS[236]	LU25
LF25	VSS[237]	LV25
LG25	VSS[238]	LW25
LH25	VSS[239]	LX25
LI25	VSS[240]	LY25
LJ25	VSS[241]	LZ25
LK25	VSS[242]	MA24
LM25	VSS[243]	MB24
LN25	VSS[244]	MC24
LO25	VSS[245]	MD24
LP25	VSS[246]	ME24
LQ25	VSS[247]	MF24
LR25	VSS[248]	MG24
LS25	VSS[249]	MH24
LT25	VSS[250]	MI24
LU25	VSS[251]	MJ24
LV25	VSS[252]	MK24
LW25	VSS[253]	ML24
LX25	VSS[254]	MM24
LY25	VSS[255]	MN24
LZ25	VSS[256]	MO24
MA24	VSS[257]	MP24
MB24	VSS[258]	MQ24
MC24	VSS[259]	MR24
MD24	VSS[260]	MS24
ME24	VSS[261]	MT24
MF24	VSS[262]	MU24
MG24	VSS[263]	MV24
MH24	VSS[264]	MW24
MI24	VSS[265]	MX24
MJ24	VSS[266]	MY24
MK24	VSS[267]	MZ24
ML24	VSS[268]	NA23
MM24	VSS[269]	NB23
MN24	VSS[270]	NC23
MO24	VSS[271]	ND23
MP24	VSS[272]	NE23
MQ24	VSS[273]	NF23
MR24	VSS[274]	NG23
MS24	VSS[275]	NH23
MT24	VSS[276]	NI23
MU24	VSS[277]	NJ23
MV24	VSS[278]	NK23
MW24	VSS[279]	NL23
MX24	VSS[280]	NO23
MY24	VSS[281]	NP23
MZ24	VSS[282]	NQ23
NA23	VSS[283]	NR23
NB23	VSS[284]	NS23
NC23	VSS[285]	NT23
ND23	VSS[286]	NU23
NE23	VSS[287]	NV23
NF23	VSS[288]	NW23
NG23	VSS[289]	NX23
NH23	VSS[290]	NY23
NI23	VSS[291]	NZ23
NJ23	VSS[292]	OA22
NK23	VSS[293]	OB22
NL23	VSS[294]	OC22
NO23	VSS[295]	OD22
NP23	VSS[296]	OE22
NQ23	VSS[297]	OF22
NR23	VSS[298]	OG22
NS23	VSS[299]	OH22
NT23	VSS[300]	OI22
NU23	VSS[301]	OJ22
NV23	VSS[302]	OK22
NW23	VSS[303]	OL22
OX23	VSS[304]	OM22
NY23	VSS[305]	ON22
NZ23	VSS[306]	OO22
OA22	VSS[307]	OP22
OB22	VSS[308]	OQ22
OC22	VSS[309]	OR22
OD22	VSS[310]	OS22
OE22	VSS[311]	OT22
OF22	VSS[312]	OU22
OG22	VSS[313]	OV22
OH22	VSS[314]	OW22
OI22	VSS[315]	OX22
OJ22	VSS[316]	OY22
OK22	VSS[317]	OZ22
OL22	VSS[318]	PA21
OM22	VSS[319]	PB21
ON22	VSS[320]	PC21
OO22	VSS[321]	PD21
OP22	VSS[322]	PE21
OQ22	VSS[323]	PF21
OR22	VSS[324]	PG21
OS22	VSS[325]	PH21
OT22	VSS[326]	PI21
OU22	VSS[327]	PJ21
OV22	VSS[328]	PK21
OW22	VSS[329]	PL21
OX22	VSS[330]	PM21
OY22	VSS[331]	PN21
OZ22	VSS[332]	PO21
PA21	VSS[333]	PP21
PB21	VSS[334]	PQ21
PC21	VSS[335]	PR21
PD21	VSS[336]	PS21
PE21	VSS[337]	PT21
PF21	VSS[338]	PU21
PG21	VSS[339]	PV21
PH21	VSS[340]	PW21
PI21	VSS[341]	PX21
PJ21	VSS[342]	PY21
PK21	VSS[343]	PZ21
PL21	VSS[344]	QA20
PM21	VSS[345]	QB20
PN21	VSS[346]	QC20
PO21	VSS[347]	QD20
PP21	VSS[348]	QE20
PQ21	VSS[349]	QF20
PR21	VSS[350]	QG20
PS21	VSS[351]	QH20
PT21	VSS[352]	QI20
PU21	VSS[353]	QJ20
PV21	VSS[354]	QK20
PW21	VSS[355]	QL20
PX21	VSS[356]	QM20
PY21	VSS[357]	QN20
PZ21	VSS[358]	QO20
QA20	VSS[359]	QP20
QB20	VSS[360]	QR20
QC20	VSS[361]	QS20
QD20	VSS[362]	QT20
QE20	VSS[363]	QU20
QF20	VSS[364]	QV20
QG20	VSS[365]	QW20
QH20	VSS[366]	QX20
QI20	VSS[367]	QY20
QJ20	VSS[368]	QZ20
QK20	VSS[369]	RA19
QL20	VSS[370]	RB19
QM20	VSS[371]	RC19
QN20	VSS[372]	RD19
QO20	VSS[373]	RE19
QP20	VSS[374]	RF19
QR20	VSS[375]	RG19
QS20	VSS[376]	RH19
QT20	VSS[377]	RI19
QU20	VSS[378]	RJ19
QV20	VSS[379]	RK19
QW20	VSS[380]	RL19
QX20	VSS[381]	RM19
QY20	VSS[382]	RN19
QZ20	VSS[383]	RO19
RA19	VSS[384]	RP19
RB19	VSS[385]	RQ19
RC19	VSS[386]	RS19
RD19	VSS[387]	RT19
RE19	VSS[388]	RU19
RF19	VSS[389]	RV19
RG19	VSS[390]	RW19
RH19	VSS[391]	RX19
RI19	VSS[392]	RY19
RJ19	VSS[393]	RZ19
RK19	VSS[394]	SA18
RL19	VSS[395]	SB18
RM19	VSS[396]	SC18
RN19	VSS[397]	SD18
RO19	VSS	

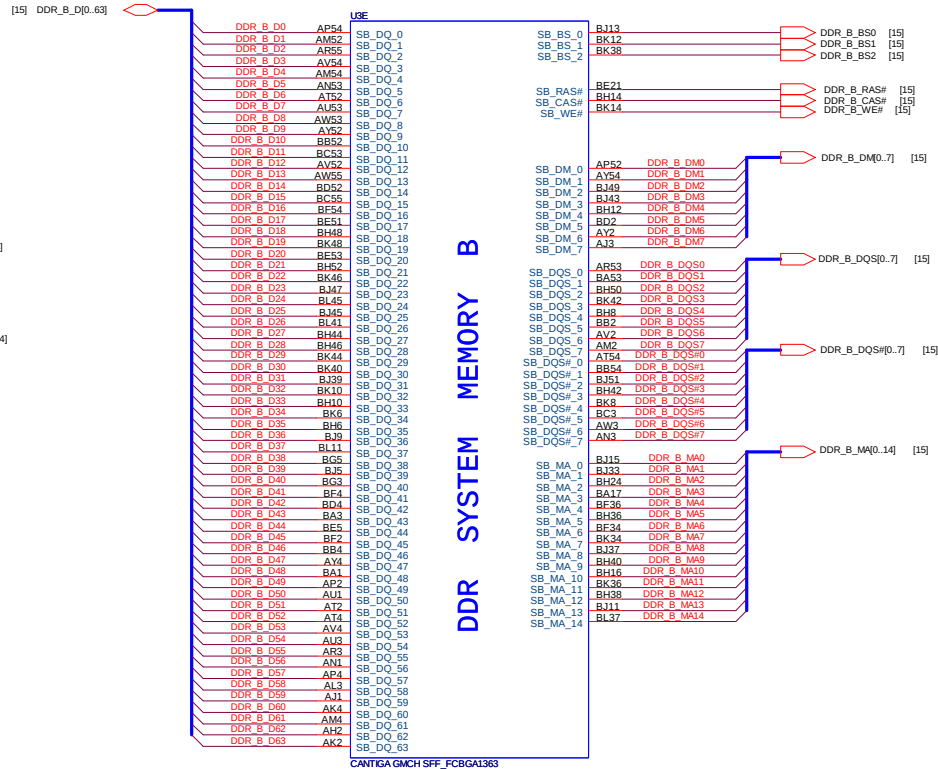


DDR SYSTEM MEMORY A



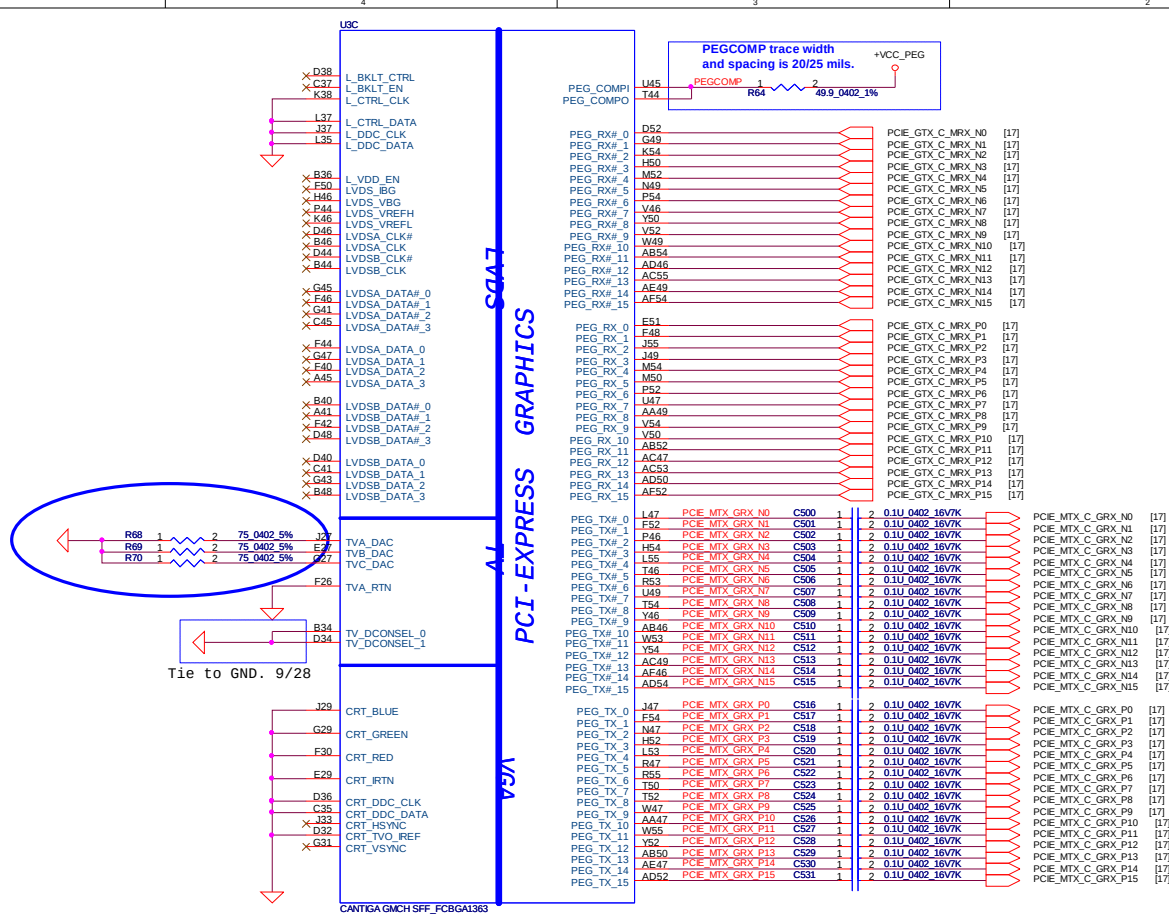
CANTIGA GMCH SFF_FCBGA1363

DDR SYSTEM MEMORY B



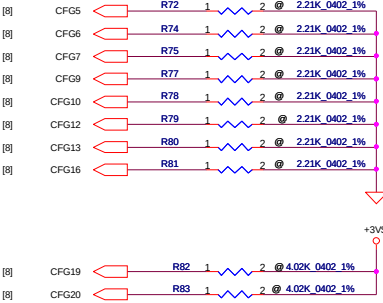
CANTIGA GMCH SFF_FCBGA1363

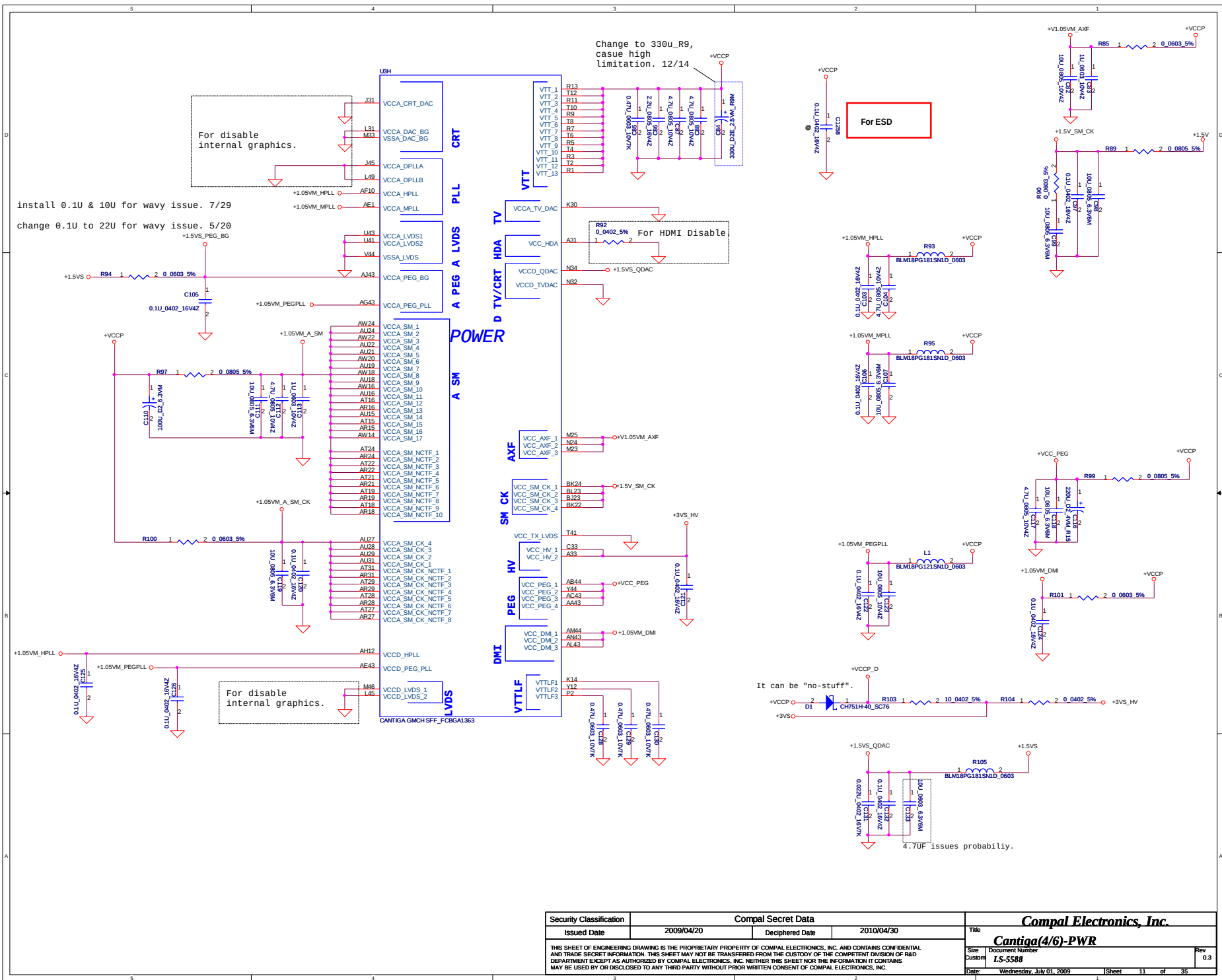
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Issued Date	2009/04/20	Deciphered Date	2010/04/30	Title
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				Size
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				LS-5588
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				Date
				Wednesday, July 01, 2009
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				9
				of
				35



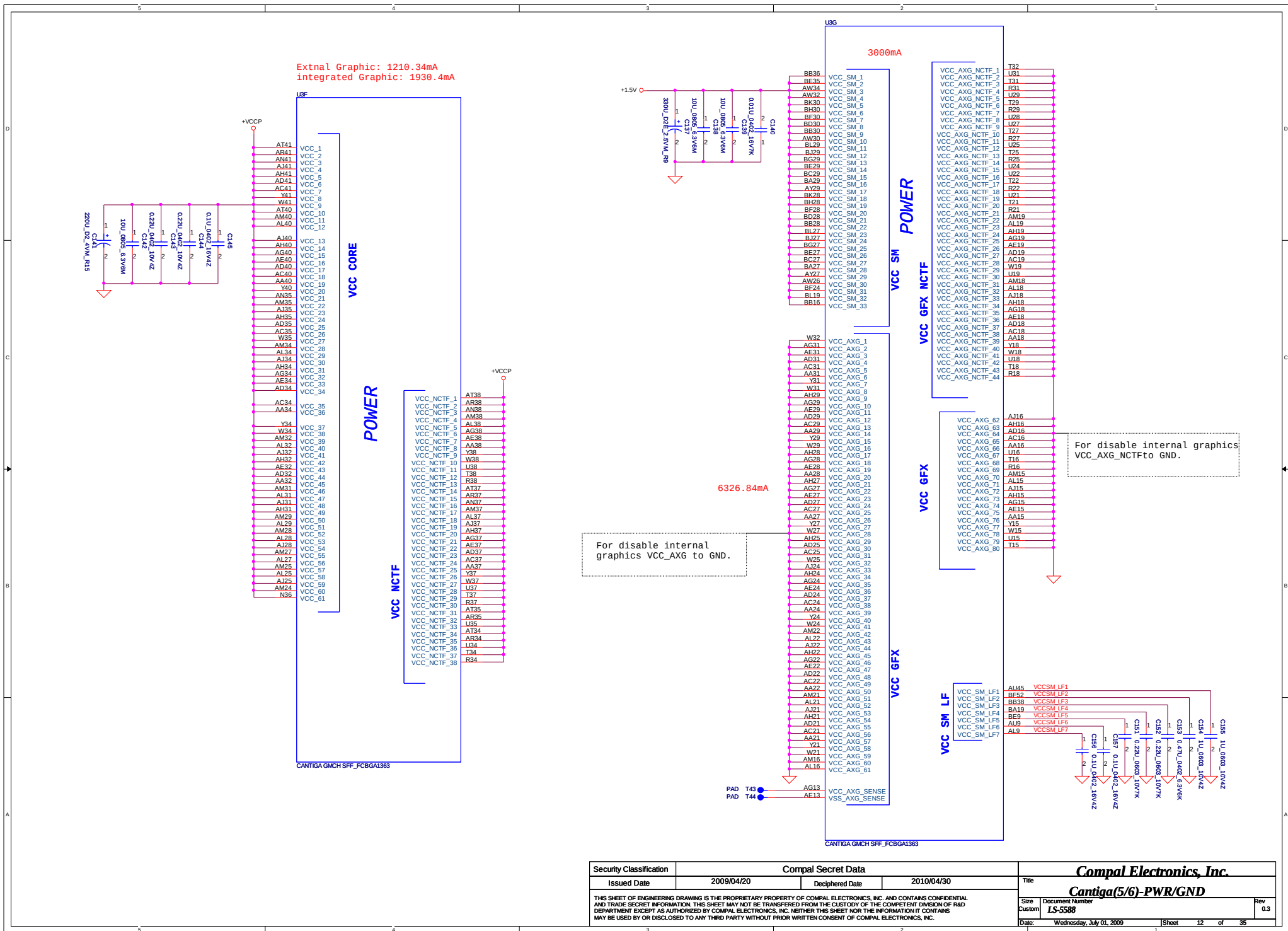
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.





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				Custom	LS-5588
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				Rev	0.3



U3

BA55	VSS_1	C43
AU55	VSS_2	A43
AN55	VSS_3	BD42
AJ55	VSS_4	H42
AE55	VSS_5	BG41
AA55	VSS_6	AY41
VSS_6	VSS_6	AM41
U55	VSS_7	AL41
BD54	VSS_8	AG41
BG53	VSS_9	AE41
AJ53	VSS_10	AA41
AE53	VSS_11	R41
AA53	VSS_12	M41
N53	VSS_13	E41
U53	VSS_14	BD40
N53	VSS_15	AU40
GS3	VSS_16	AR40
ES3	VSS_17	AM40
K32	VSS_18	W40
BG51	VSS_19	U40
BA51	VSS_20	T40
AM51	VSS_21	R40
AU51	VSS_22	K40
AR51	VSS_23	H40
AE51	VSS_24	BL39
AJ51	VSS_25	BG39
AE51	VSS_26	BA39
AC51	VSS_27	E39
AC51	VSS_28	C39
AC51	VSS_29	A39
AA51	VSS_30	BD38
W51	VSS_31	AU38
U51	VSS_32	H38
R51	VSS_33	BG37
N51	VSS_34	M37
L51	VSS_35	E37
J51	VSS_36	BD36
GS1	VSS_37	AM36
C51	VSS_38	H36
BK50	VSS_39	BL35
AM50	VSS_40	BG35
K50	VSS_41	AY35
BG49	VSS_42	AL35
E49	VSS_43	AG35
C49	VSS_44	AE35
BD48	VSS_45	AA35
BB48	VSS_46	Y35
AY48	VSS_47	M35
AV48	VSS_48	E35
AT48	VSS_49	A35
AP48	VSS_50	BD34
AM48	VSS_51	AU34
AK48	VSS_52	AN34
AH48	VSS_53	H34
AF48	VSS_54	BL33
AD48	VSS_55	BG33
AB48	VSS_56	E33
Y48	VSS_57	BD32
V48	VSS_58	AJ32
T48	VSS_59	AG32
P48	VSS_60	AC32
M48	VSS_61	Y32
K48	VSS_62	H32
H48	VSS_63	B32
BL47	VSS_64	BJ31
BG47	VSS_65	BC31
E47	VSS_66	AY31
C47	VSS_67	AN31
BD46	VSS_68	M31
AB46	VSS_69	E31
AM46	VSS_70	N30
AK46	VSS_71	H30
AH46	VSS_72	AN29
BG46	VSS_73	AJ29
AE46	VSS_74	M29
AC46	VSS_75	A29
AA46	VSS_76	AW28
W45	VSS_77	AN28
R45	VSS_78	AD28
N45	VSS_79	AC28
E45	VSS_80	Y28
BD44	VSS_81	W28
BB44	VSS_82	H28
AV44	VSS_83	E28
AK44	VSS_84	AN27
AH44	VSS_85	AJ27
AF44	VSS_86	M27
AD44	VSS_87	BF26
K44	VSS_88	BD26
H44	VSS_89	N26
BL43	VSS_90	H26
BG43	VSS_91	BJ25
AB43	VSS_92	AY25
AM43	VSS_93	AU25
AK43	VSS_94	
AH43	VSS_95	
AF43	VSS_96	
AD43	VSS_97	
K43	VSS_98	
H43	VSS_99	

CANTIGA GMCH SFF_FCBGA1363

U3J

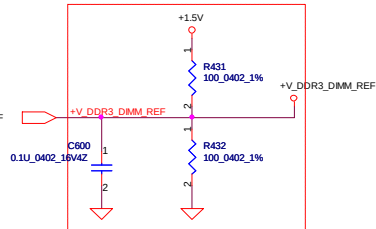
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Y25	VSS_203	VSS_304	AD8
E25	VSS_204	VSS_305	AB8
A25	VSS_205	VSS_306	V8
BD24	VSS_206	VSS_307	V8
AN24	VSS_207	VSS_308	P8
AL24	VSS_208	VSS_309	M8
H24	VSS_209	VSS_310	K8
BG23	VSS_210	VSS_311	H8
AY23	VSS_211	VSS_312	B177
E23	VSS_212	VSS_313	E7
BD22	VSS_213	VSS_314	BF6
BR22	VSS_214	VSS_315	BC5
AN22	VSS_215	VSS_316	BA5
Y22	VSS_216	VSS_317	AW5
W22	VSS_217	VSS_318	AU5
H22	VSS_218	VSS_319	AR5
BL21	VSS_219	VSS_320	AN5
BG21	VSS_220	VSS_321	AL5
AY21	VSS_221	VSS_322	AJ5
AN21	VSS_222	VSS_323	AG5
AE21	VSS_223	VSS_324	AE5
E21	VSS_224	VSS_325	AC5
M21	VSS_225	VSS_326	AA5
C21	VSS_226	VSS_327	W5
A21	VSS_227	VSS_328	U5
BD20	VSS_228	VSS_329	N5
H20	VSS_229	VSS_330	L5
BG19	VSS_230	VSS_331	J5
AY19	VSS_231	VSS_332	G5
AL19	VSS_232	VSS_333	C5
H19	VSS_233	VSS_334	BH4
BD18	VSS_234	VSS_335	BE3
N18	VSS_235	VSS_336	U3
H18	VSS_236	VSS_337	E3
BL17	VSS_237	VSS_338	BC1
BG17	VSS_238	VSS_339	AW1
AY17	VSS_239	VSS_340	AR1
M17	VSS_240	VSS_341	AL1
E17	VSS_241	VSS_342	AG1
AL17	VSS_242	VSS_343	AC1
BD16	VSS_243	VSS_344	W1
AN16	VSS_244	VSS_345	N1
AG16	VSS_245	VSS_346	J1
AE16	VSS_246	VSS_347	AU3
Y16	VSS_247	VSS_348	BB42
W16	VSS_248	VSS_349	AW38
N16	VSS_249	VSS_350	BA35
H16	VSS_250	VSS_351	I29
BG15	VSS_251	VSS_352	N28
AY15	VSS_252	VSS_353	N22
AN15	VSS_253	VSS_354	N20
AD15	VSS_254	VSS_355	N14
AC15	VSS_255	VSS_356	AL13
R15	VSS_256	VSS_357	B10
M15	VSS_257	VSS_358	AN13
E15	VSS_258		
BD14	VSS_259	VSS_359	M42
H14	VSS_260	VSS_360	N40
BL13	VSS_261	VSS_361	N38
BG13	VSS_262	VSS_362	M39
AY13	VSS_263		
AN13	VSS_264		
AE13	VSS_265	VSS_NCTF_1	AJ38
E13	VSS_266	VSS_NCTF_2	AH38
BD12	VSS_267	VSS_NCTF_3	AD38
AN12	VSS_268	VSS_NCTF_4	AC38
AD12	VSS_269	VSS_NCTF_5	T35
AC12	VSS_270	VSS_NCTF_6	R35
R12	VSS_271	VSS_NCTF_7	A132
M12	VSS_272	VSS_NCTF_8	AR32
E12	VSS_273	VSS_NCTF_9	U32
BD11	VSS_274	VSS_NCTF_10	R32
AN11	VSS_275	VSS_NCTF_11	T28
AD11	VSS_276	VSS_NCTF_12	R28
AC11	VSS_277	VSS_NCTF_13	AT25
R11	VSS_278	VSS_NCTF_14	AR25
M11	VSS_279	VSS_NCTF_15	T24
E11	VSS_280	VSS_NCTF_16	R24
BD10	VSS_281	VSS_NCTF_17	AN19
AN10	VSS_282	VSS_NCTF_18	AJ19
AD10	VSS_283	VSS_NCTF_19	AA19
AC10	VSS_284	VSS_NCTF_20	Y19
R10	VSS_285	VSS_NCTF_21	T19
M10	VSS_286	VSS_NCTF_22	R19
E10	VSS_287	VSS_NCTF_23	AN18
BD9	VSS_288		
AN9	VSS_289		
AD9	VSS_290	VSS_SCB_1	BL55
AC9	VSS_291	VSS_SCB_2	BL1
R9	VSS_292	VSS_SCB_3	A55
M9	VSS_293	VSS_SCB_4	D1
E9	VSS_294	VSS_SCB_5	B55
BD8	VSS_295	VSS_SCB_6	B2
AN8	VSS_296	VSS_SCB_7	A4
AD8	VSS_297		
AC8	VSS_298		
R8	VSS_299		

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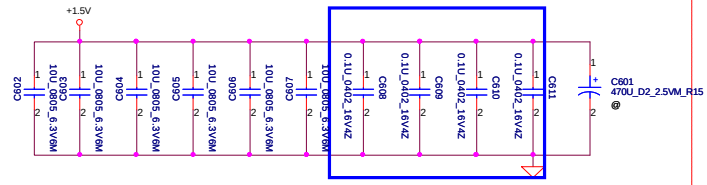
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 [0] DDR_A_D0..63
 [0] DDR_A_DM[0..7]
 [0] DDR_A_DQS#[0..7]
 [0] DDR_A_MA[0..14]

[15] +V_DDR3_DIMM_REF

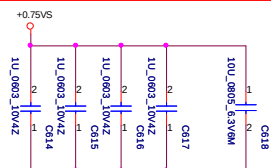


Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:
Place near JP4.203 & JP4.204



[0] DDR_CKE0_DIMMA

[0] DDR_A_BS2

[0] M_CLK_DDR0

[0] M_CLK_DDR#0

[0] DDR_A_BS0

[0] DDR_A_WE#

[0] DDR_A_CAS#

[0] DDR_CS1_DIMMA#

[0] DDR_CKE1_DIMMA

[0] DDR_A_BS1

[0] DDR_A_BS1

[0] DDR_A_BS1

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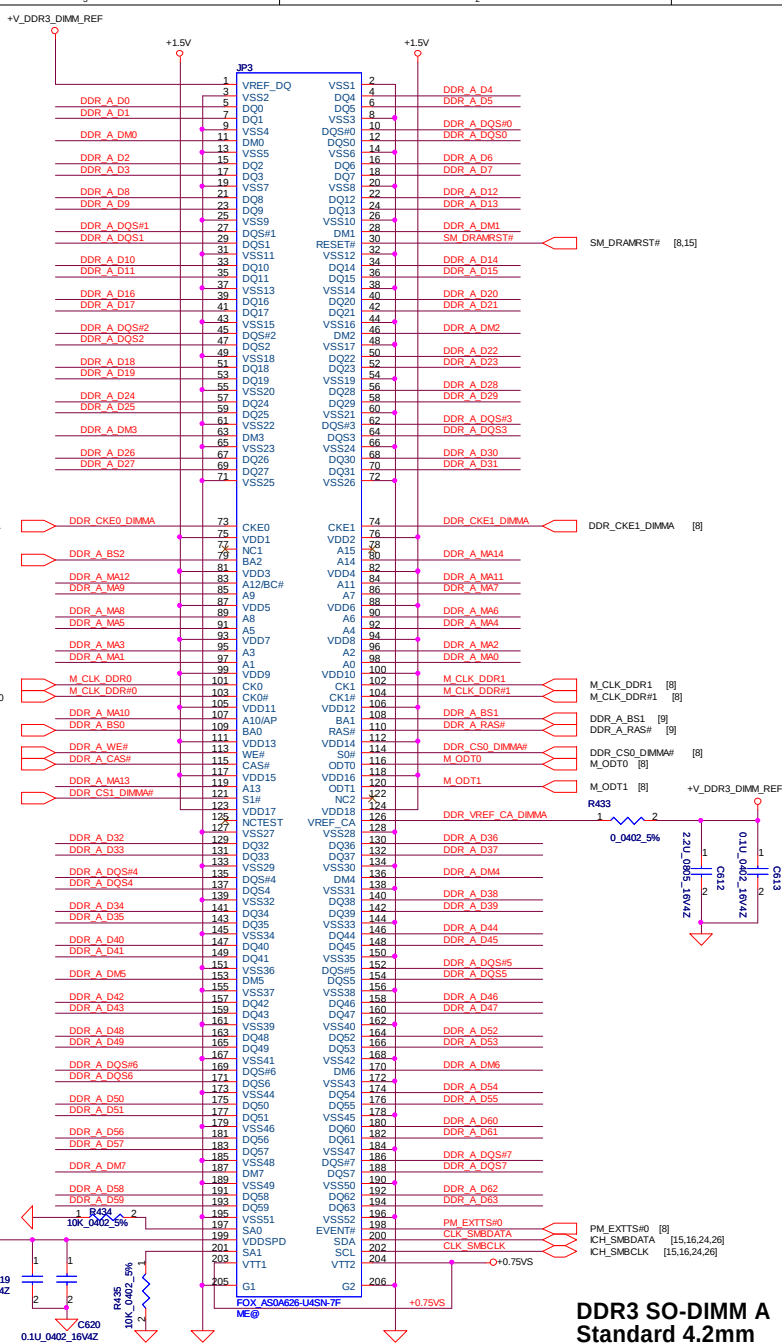
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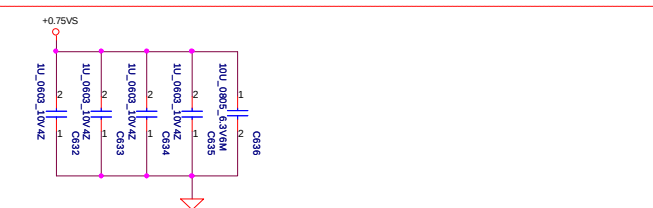
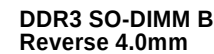
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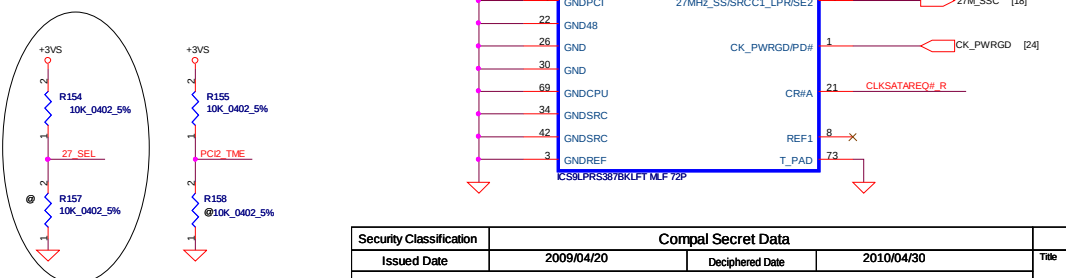
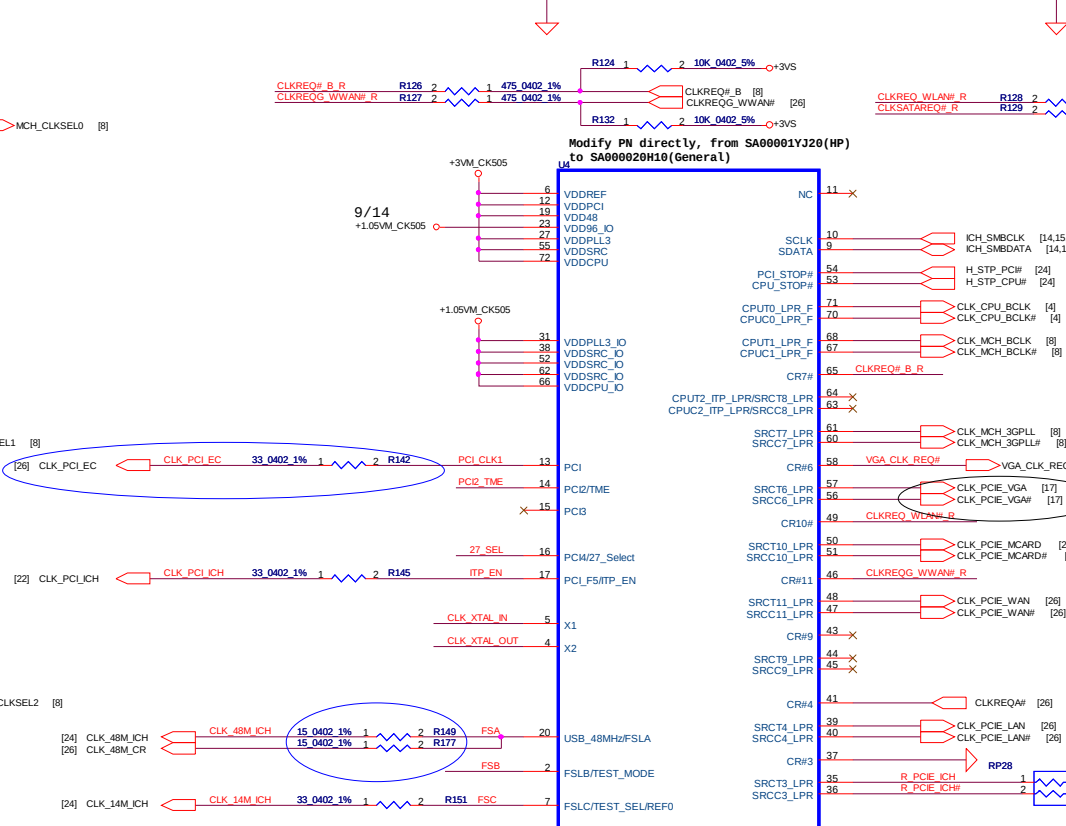
[0] DDR_A_BS1



DDR3 SO-DIMM A
Standard 4.2mm

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				DDR3-SODIMM SLOT1	
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Place close to U5

10K_0402_5% 1 2 +3VS

R125

CLKREQ_WLAN# [26]

CLKSATAREQ# [24]

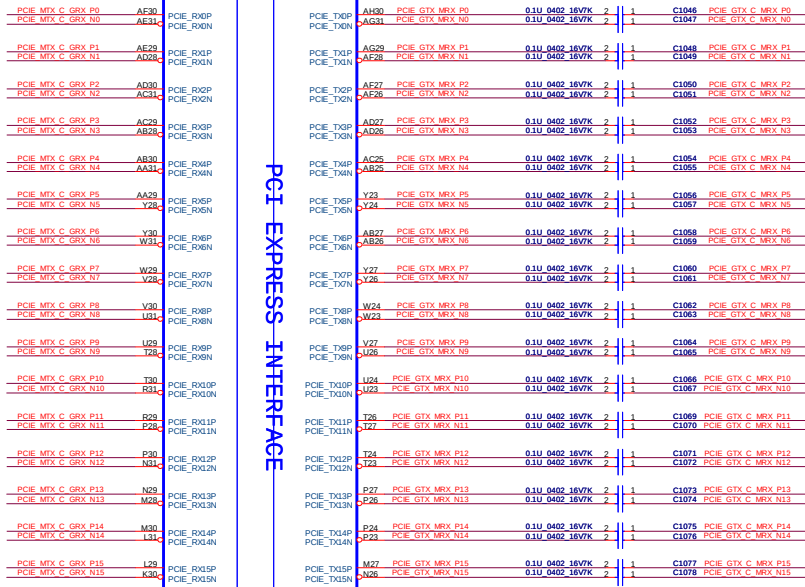
R133

10K_0402_5% 1 2 +3VS

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- [10] PCIE_MTX_C_GRPX_N0_15] PCIE_MTX_C_GRPX_N0_15]
[10] PCIE_MTX_C_GRPX_P0_15] PCIE_MTX_C_GRPX_P0_15]
[10] PCIE_GTX_C_GRPX_N0_15] PCIE_GTX_C_GRPX_N0_15]
[10] PCIE_GTX_C_GRPX_P0_15] PCIE_GTX_C_GRPX_P0_15]

U8AA



PCI EXPRESS INTERFACE

CLOCK

PCIE_REFCLKP

PCIE_REFCLKN

PCIE_CALRPN

PCIE_CALRPN

PCIE_CALRPN

PCIE_CALRPN

PCIE_CALRPN

PCIE_CALRPN

PCIE_CALRPN

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PCIE_CALRPN

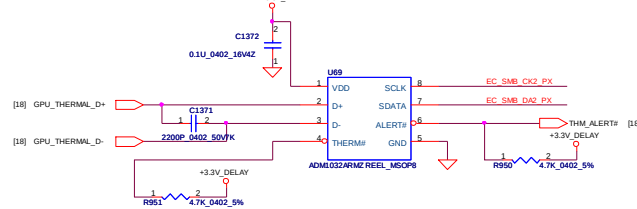
PCIE_CALRPN

PCIE_CALRPN

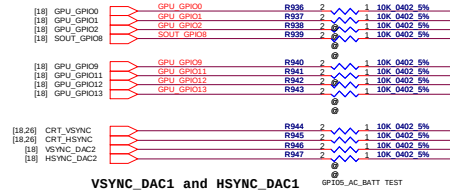
NOTE:
Change part number directly,
from SA000002ZM10 to SA000030020
M92XT -> LP, 2009/05/20

VGA Thermal Sensor ADM1032ARMZ-2

Closed to GPU



STRAPS



VSYN_DAC1 and HSYN_DAC1
pull up to HDMI & DISPLAYPORT
AUDIO function

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED,
THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	1
BF_CLK_PM_EN	GPIO8	BF_CLK_PM_EN	0
BF_VGADIS	GPIO9	VGAENABLED	0
BF_RX_PLL_CALIB_BP	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB		1
ROMDCFSQ20	GPIO[23:11]	BF_RX_PLL_CALIB_BP	0 0
VP_DEVICE_STRAP_ENA	V2SYN	ENABLE EXTERNAL BIOS ROM	0
SMS_EN_HWRD	H2SYN	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0
CCBYPASS	GENERIC	IGNORE VIP DEVICE STRAPS	0
AUD[1]	HSYN	AUD[1] AUD[0]	
AUD[0]	VSYN	0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

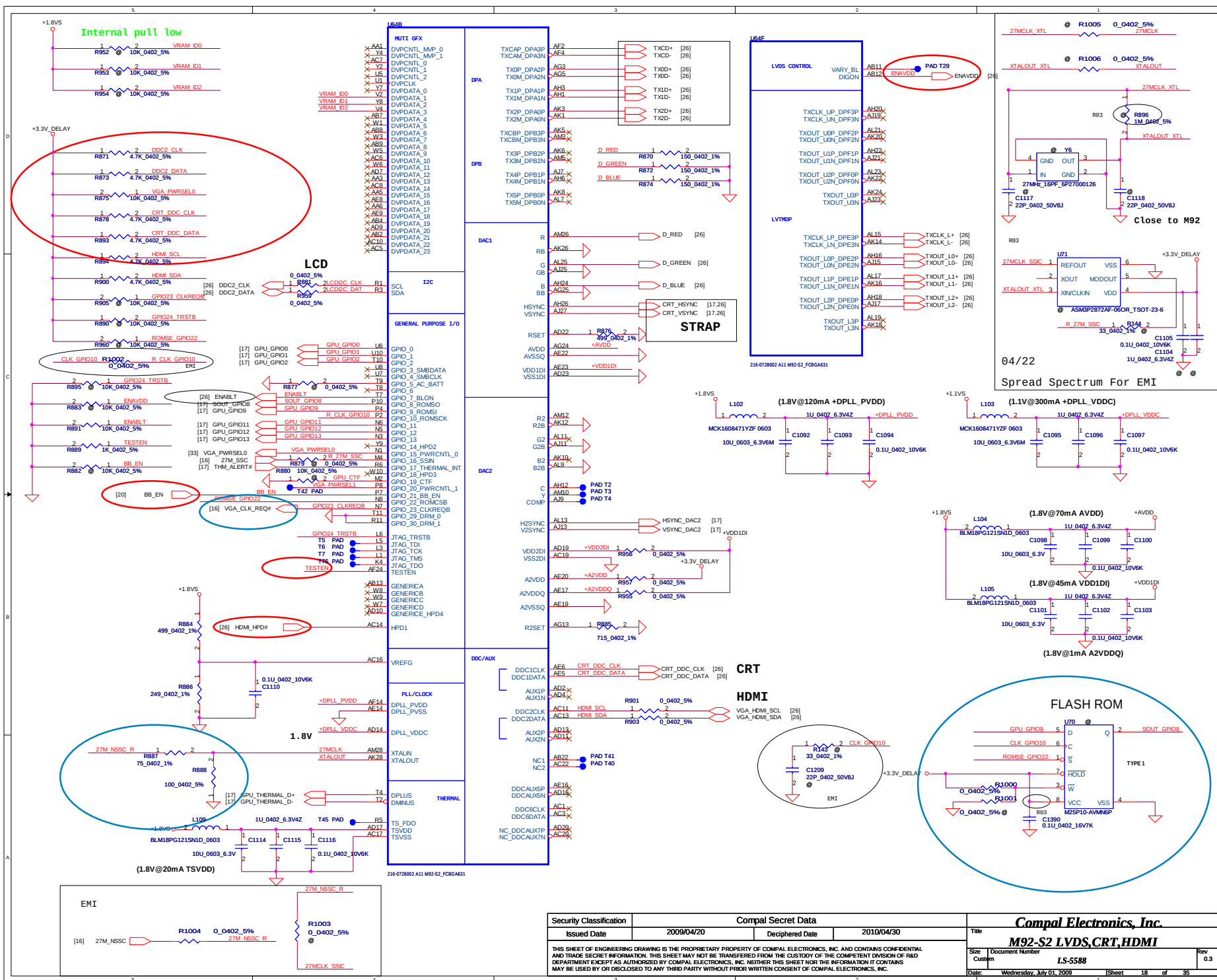
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED,
THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
H2SYN	GENERIC		
GPIO_28_TDO	GPIO21_BB_EN		

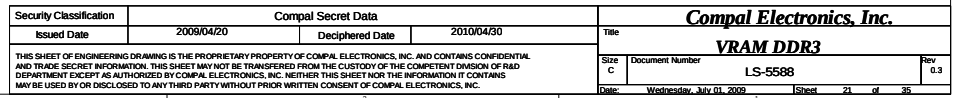
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED,
THEY MUST NOT CONFLICT DURING RESET

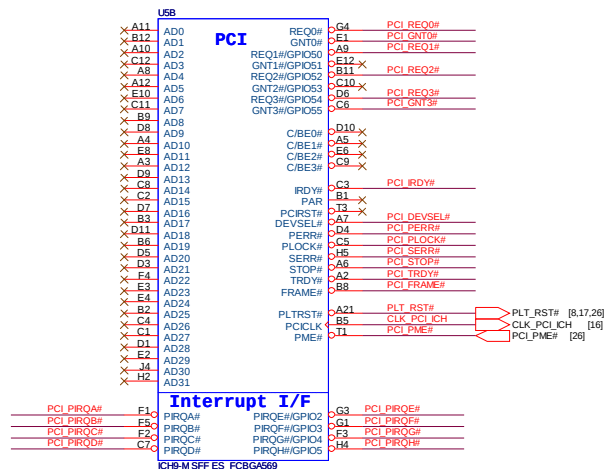
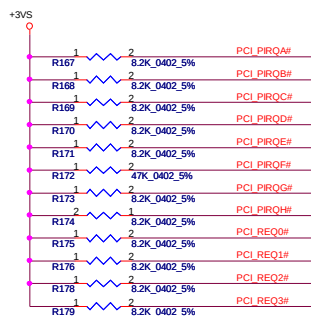
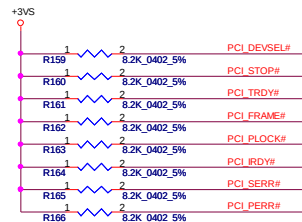
STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 2.1.0
VRAM_ID[2:0]	DVI0DATA 3.2	M92 S2-XT	JM51_PU	512MB(x4)	Samsung 64Mx16x4 DDR3	SA000035700	1 0 0
			JM51_PU	256MB(x2)	Samsung 64Mx16x2 DDR3		1 0 1
			JM51_PU	512MB(x4)	Hynix 64Mx16x4 DDR3	SA000032400	0 0 0
			JM51_PU	256MB(x2)	Hynix 64Mx16x2 DDR3		0 1 0

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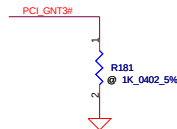


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				Custom	LS-5588	0.3
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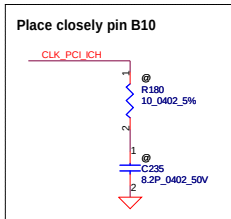
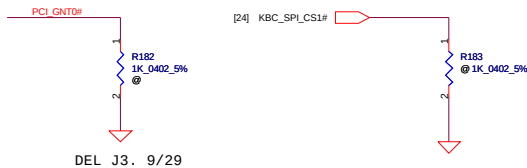




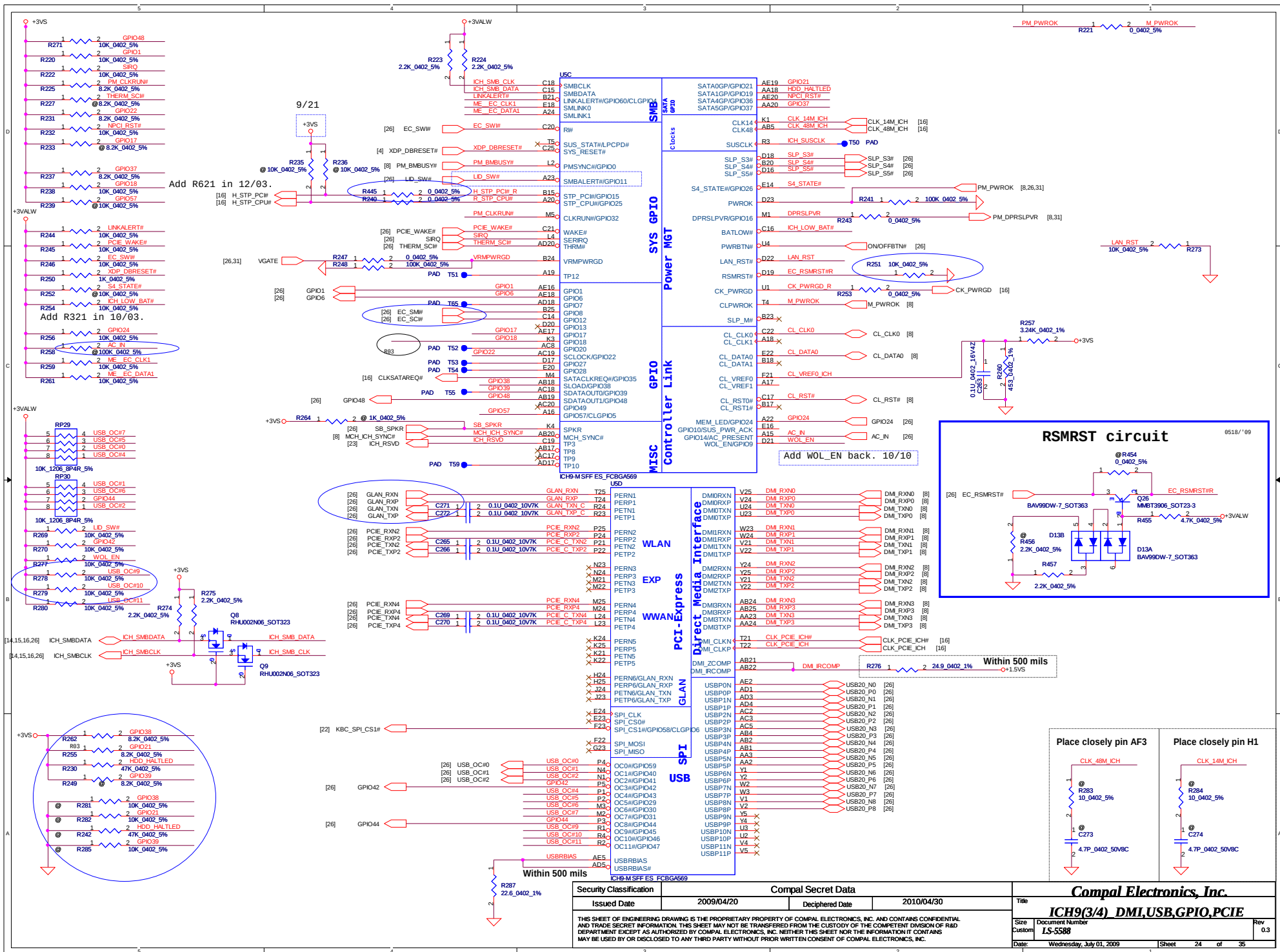
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *

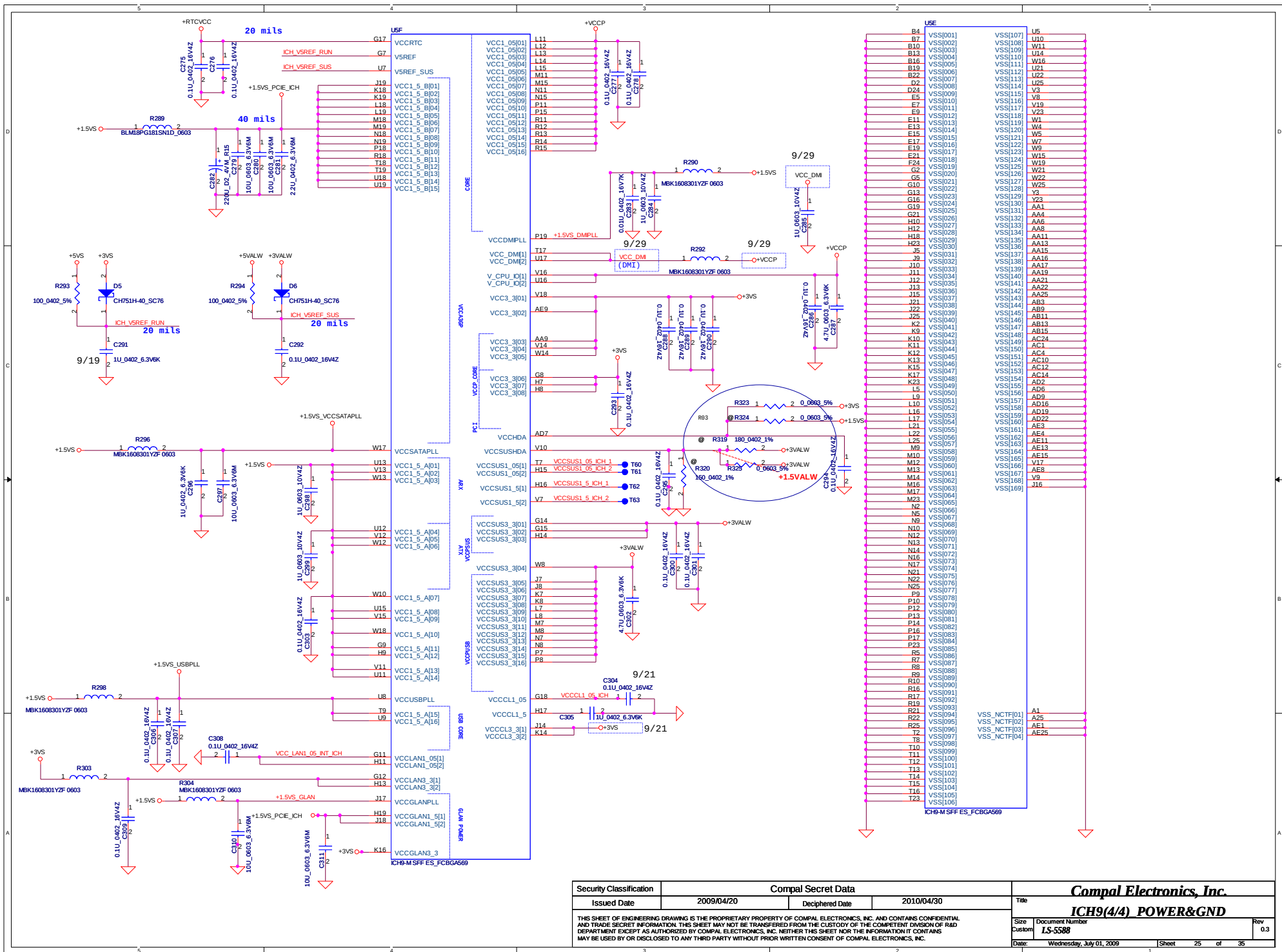


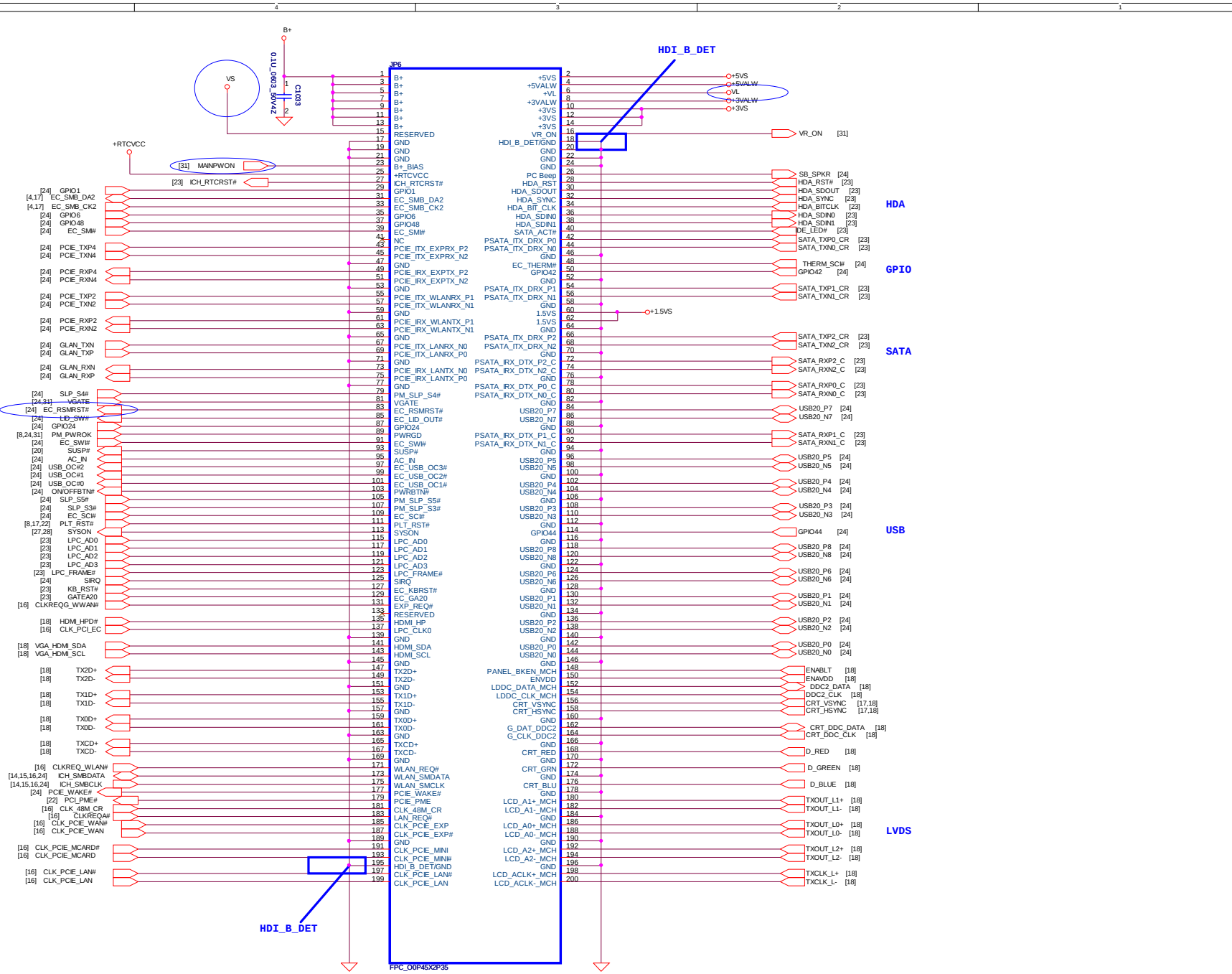
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



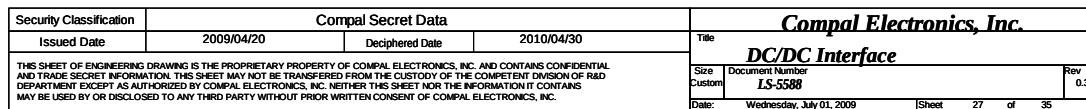
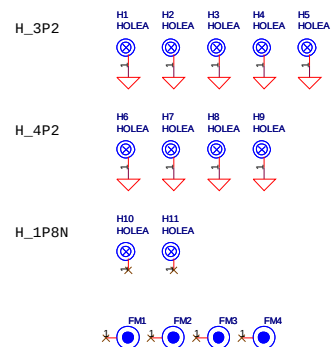
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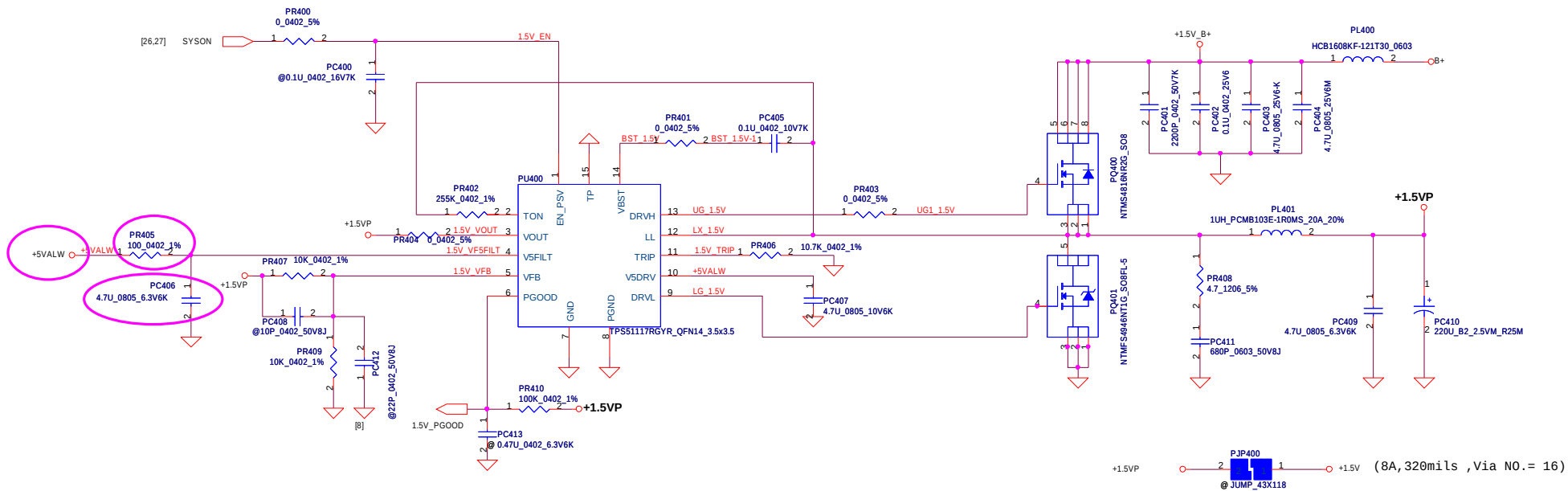




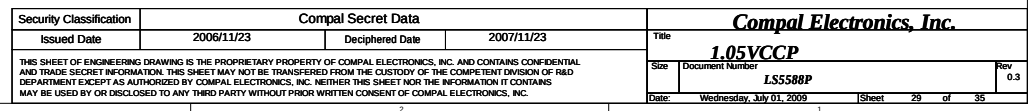


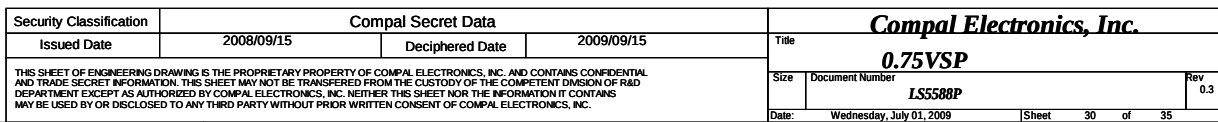
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				Date	
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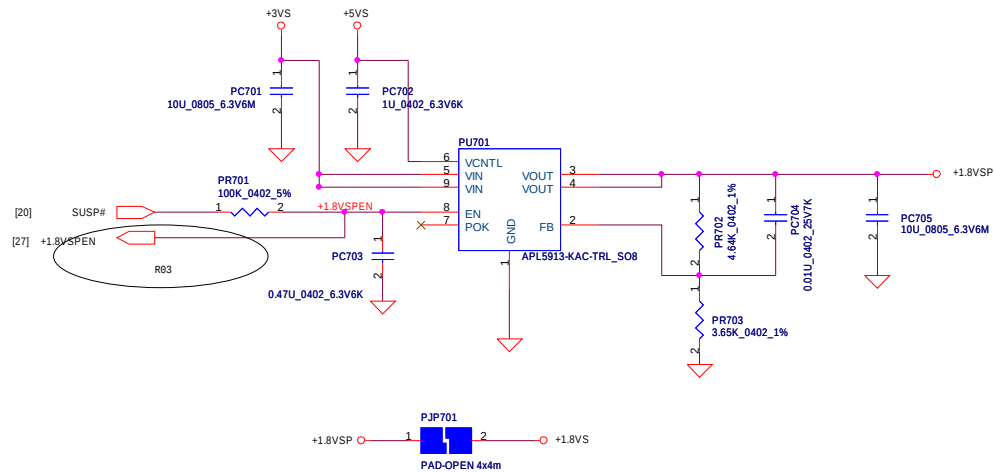




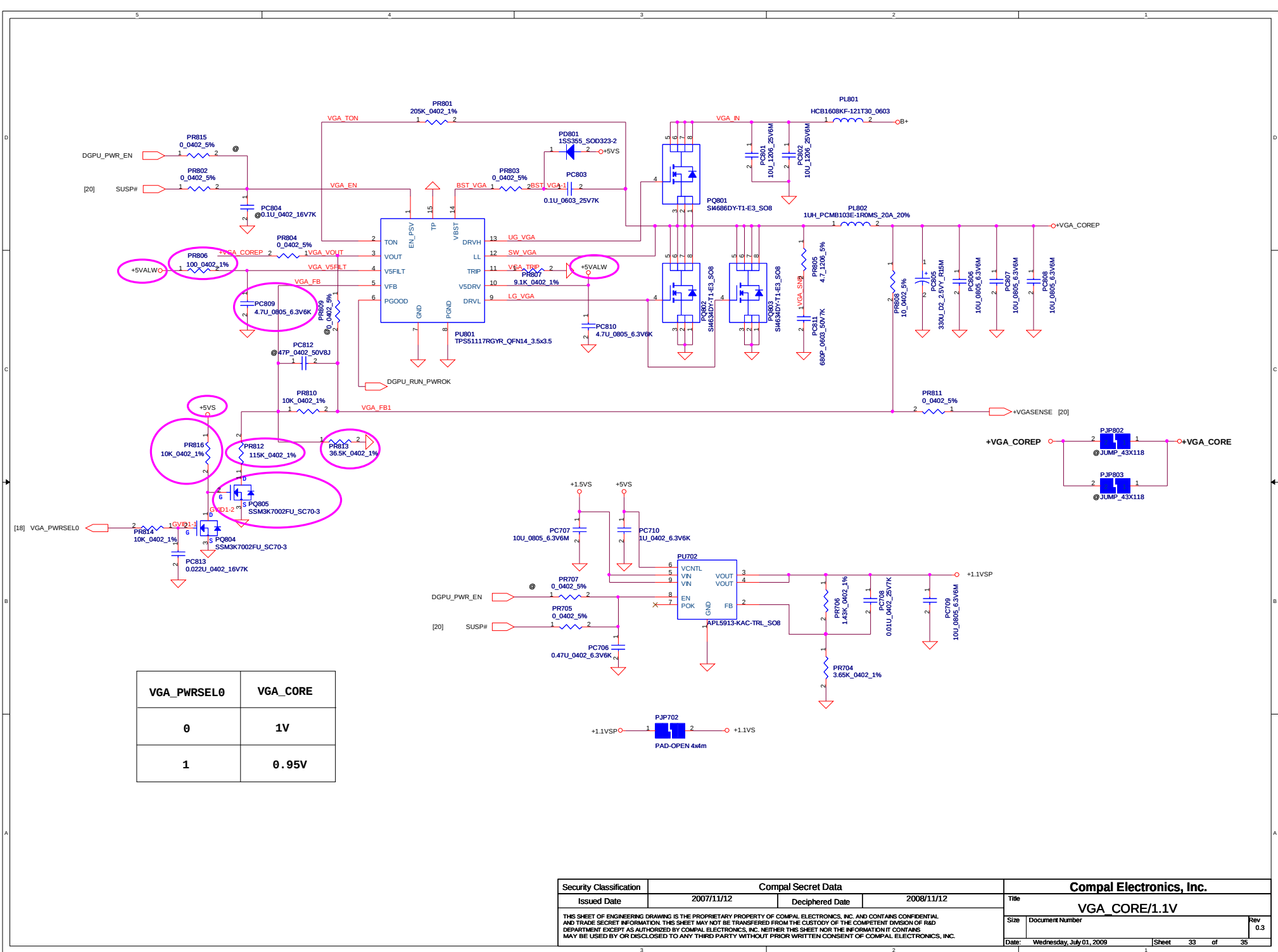
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title PIR (PWR)	
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				Date Wednesday, July 01, 2009	Rev 0.3
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change OVT Circuit		1.0		add PU7, PH1, PC18, PC19, PC64, PR33, PR30, PR34, PR35, PR29, PR28, PQ4		
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				Size	Document Number
				LS-5588	
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