Compal Confidential

PBL80 Project

LA-7441P REV 0.1 Schematic

Intel Sandy Bridge/Cougar Point

N12P-GV/GS-Optimus Only

2011-01-21 Rev. 0.1

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cover Page

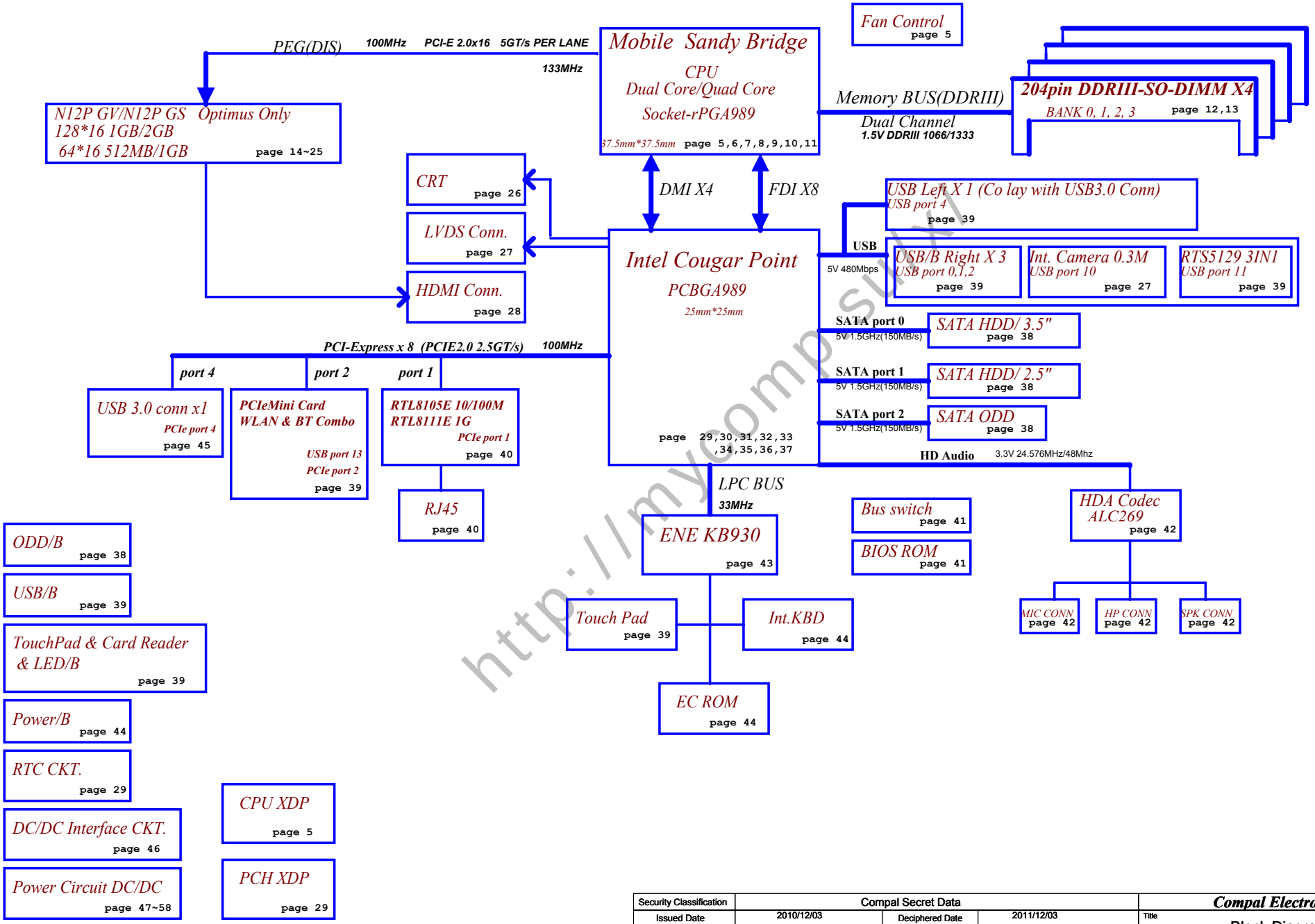
Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 1 of 58

Compal Confidential

Model Name : PBL80

File Name : LA-7441PR01



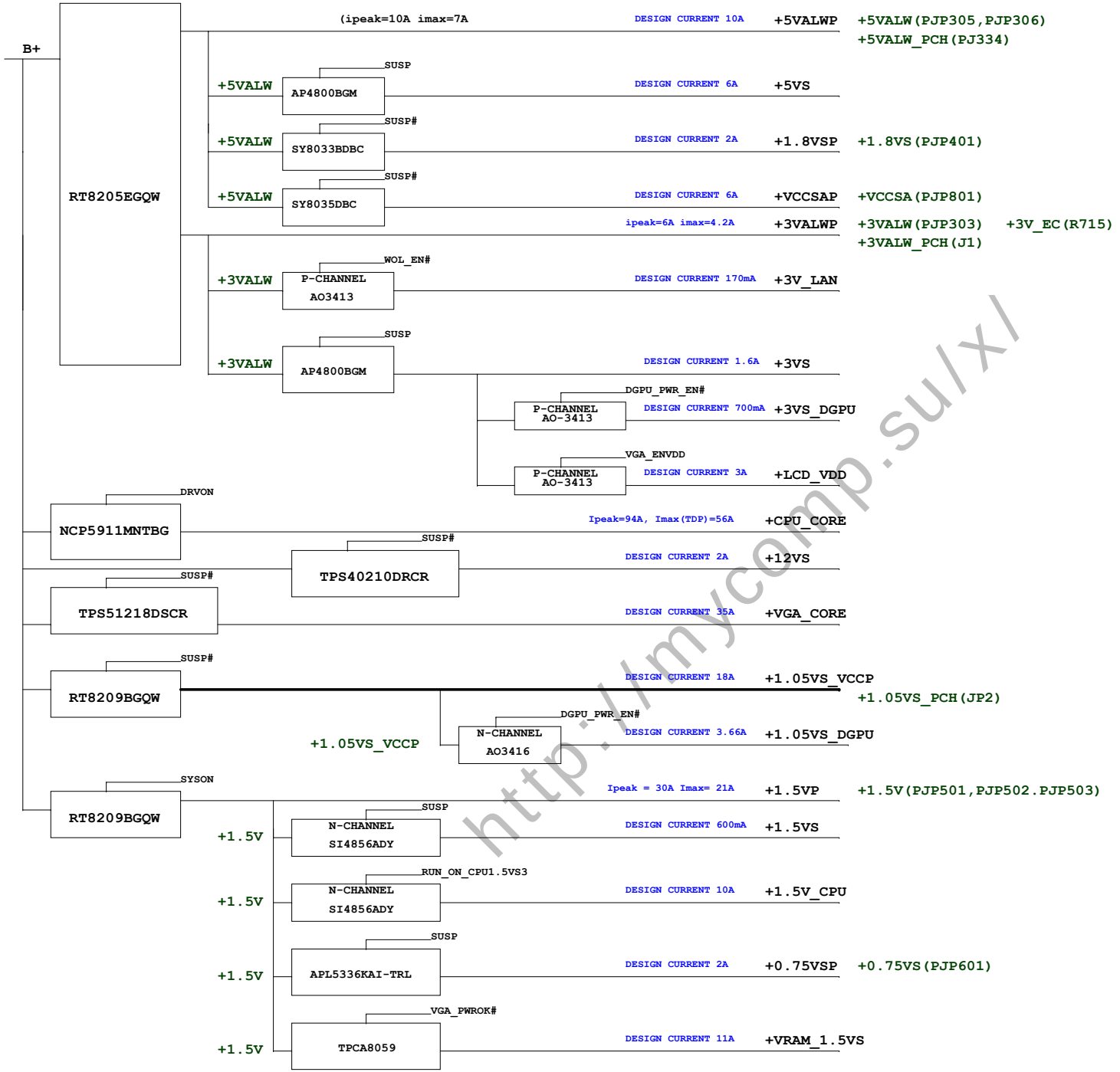
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Block Diagrams

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 2 of 58



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Power Map

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 3 of 58

Voltage Rails

(O MEANS ON X MEANS OFF)

State \ power plane	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +5VALW_PCH +3VALW_PCH +3V_LAN +3V_EC +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS_VCCP +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VCCSA +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU +12VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

Function	VRAM					GPU		Board ID
description	VRAM	Samsung 64bits	Hynix 64bits	Samsung 128bits	Hynix 128bits	N12P-GS	N12P-GV	Adaptor
explain	VRAM	Strap pin	Strap pin	Strap pin	Strap pin	Strap pin	Strap pin	Adaptor
BTO	8PCS@	PD 20K	PD 15K	PD 45.3K	PD 34.8K	N12PGS@	N12PGV@	90W@, 120W@

Function	Crisis recovery	HDMI	WLAN+BT		LAN	
description	BUS SWITCH	HDMI	WLAN+BT(BT pin 51)	WLAN+BT(BT pin 5)	Giga LAN	10/100M LAN
explain	BUS SWITCH	HDMI	WLAN+BT(BT pin 51)	WLAN+BT(BT pin 5)	Strap pin	Strap pin
BTO	Debug@	HDMI@	BT@	COMBO@	8111E@	8105E@

Function	USB3.0/2.0 Colay		SATA3.0 Repeater Chip		SATA Preemphasis		SATA Equalization	
description	USB3.0	USB2.0	MAXIM	TI	Preemphasis		Equalization	
explain	USB3.0	USB2.0	MAX4951	SN75LVCP601	Enable	Disable	Maximum	Normal
BTO	USB3@	USB2@	MAXIM@	TI@	DEN@	NDEN@	EQ@	NEQ@

Function	SATA path	
description	PCH	Repeater
explain	PCH	Repeater
BTO	SATA@	SATARP@

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMMA1	A0 H	1010 0000 b
+3VS	DDR SO-DIMMA2	A0 H	1010 0010 b
+3VS	DDR SO-DIMMB1	A4 H	1010 0100 b
+3VS	DDR SO-DIMMB2	A0 H	1010 0110 b
+3VS	WLAN		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	VGA Thermal Sensor	9A H	1001 1010 b

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

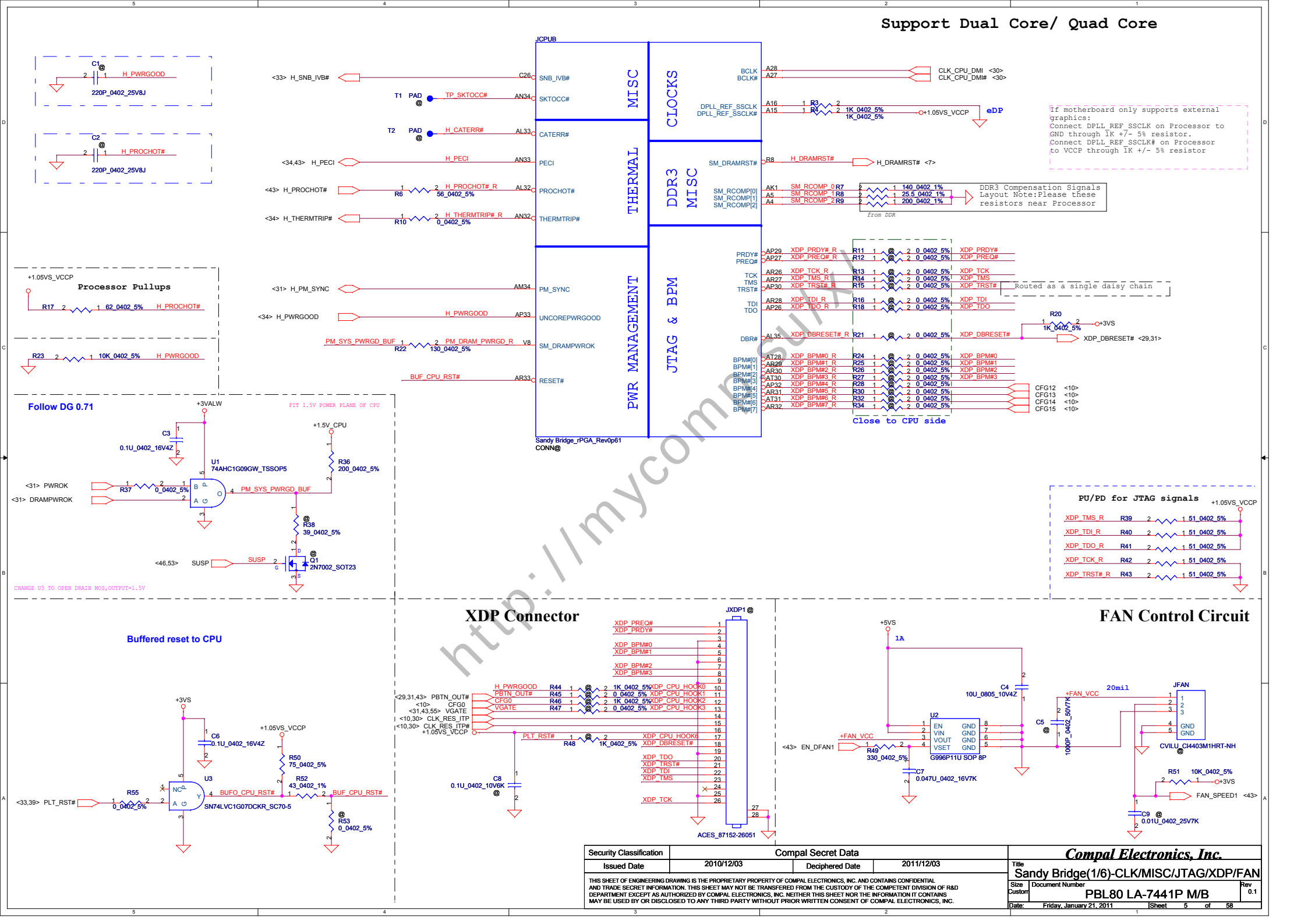
Compal Electronics, Inc.

Title: Notes List

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 4 of 58

Support Dual Core/ Quad Core



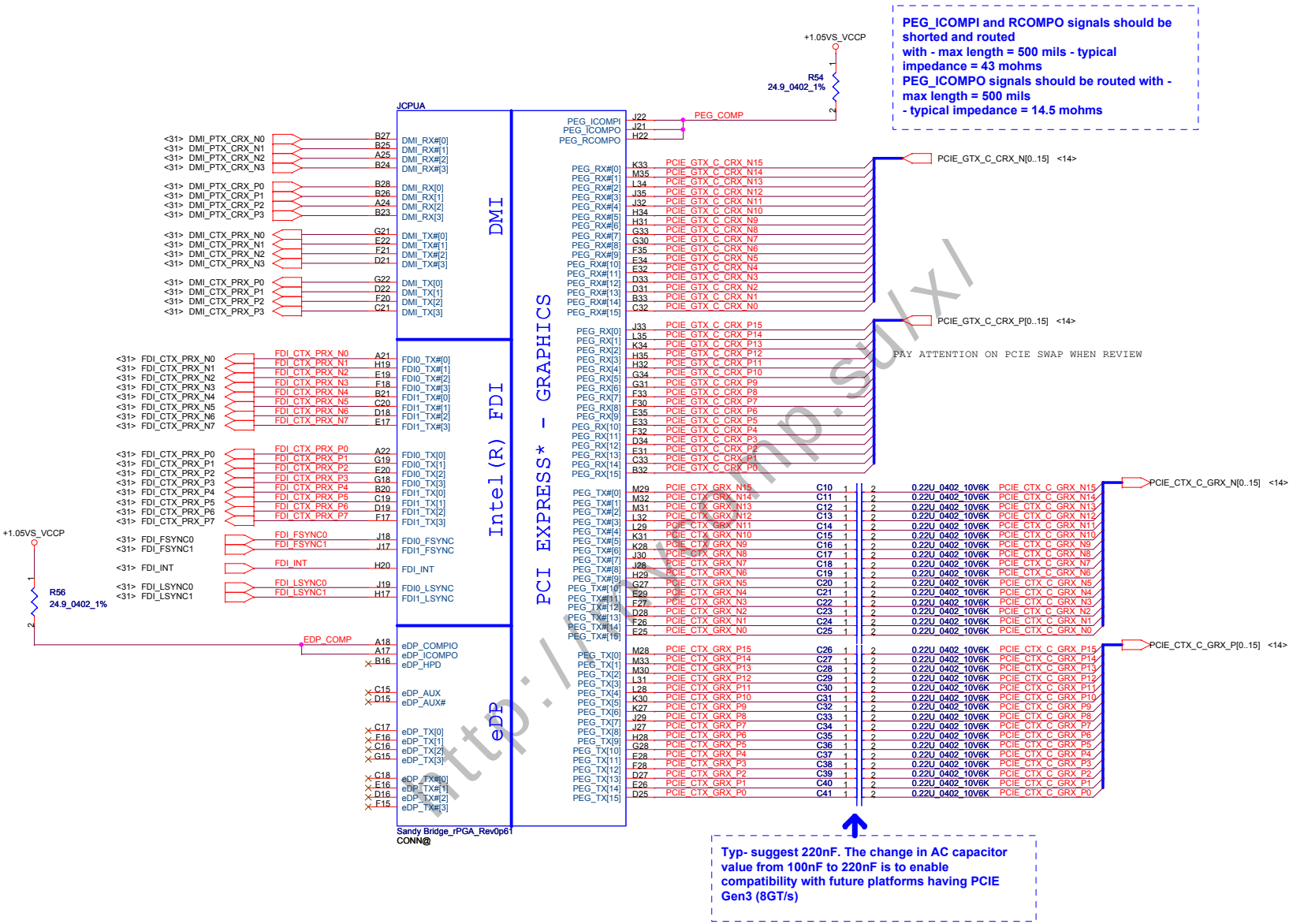
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Sandy Bridge(1/6)-CLK/MISC/JTAG/XDP/FAN

Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.1

Date: Friday, January 21, 2011 Sheet 5 of 58



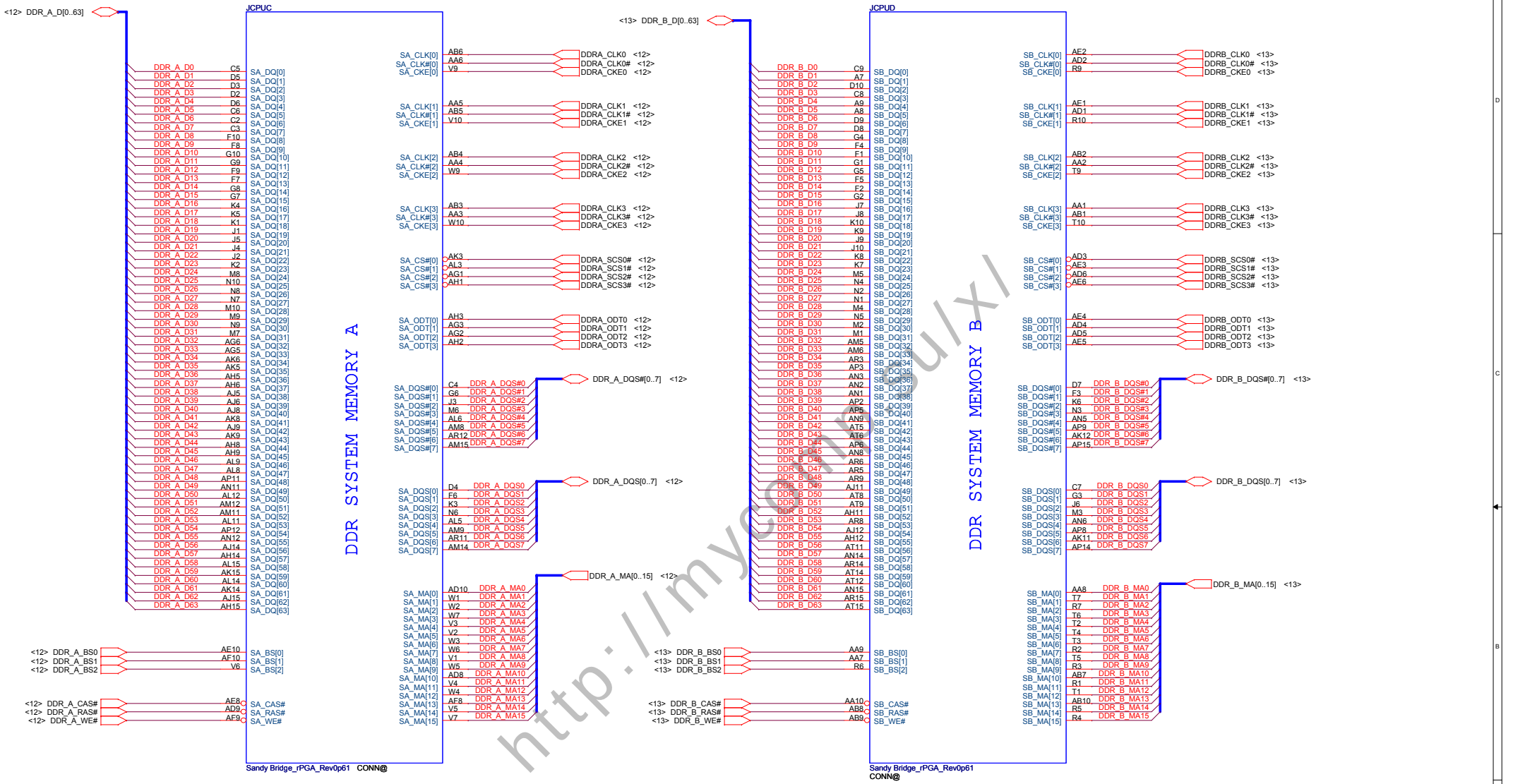
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Sandy Bridge(2/6)-DMI/FDI/PEG/eDP

Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.1

Date: Friday, January 21, 2011 Sheet 6 of 58



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Sandy Bridge(3/6)-DDR III

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 7 of 58

Group1

POWER

+CPU_CORE

JCPUF

94A

18A

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

VCC1 AG35
VCC2 AG34
VCC3 AG33
VCC4 AG32
VCC5 AG31
VCC6 AG30
VCC7 AG29
VCC8 AG28
VCC9 AG27
VCC10 AG26
VCC11 AF35
VCC12 AF34
VCC13 AF33
VCC14 AF32
VCC15 AF31
VCC16 AF30
VCC17 AF29
VCC18 AF28
VCC19 AF27
VCC20 AF26
VCC21 AD35
VCC22 AD34
VCC23 AD33
VCC24 AD32
VCC25 AD31
VCC26 AD30
VCC27 AD29
VCC28 AD28
VCC29 AD27
VCC30 AD26
VCC31 AC35
VCC32 AC34
VCC33 AC33
VCC34 AC32
VCC35 AC31
VCC36 AC30
VCC37 AC29
VCC38 AC28
VCC39 AC27
VCC40 AC26
VCC41 AA35
VCC42 AA34
VCC43 AA33
VCC44 AA32
VCC45 AA31
VCC46 AA30
VCC47 AA29
VCC48 AA28
VCC49 AA27
VCC50 AA26
VCC51 Y35
VCC52 Y34
VCC53 Y33
VCC54 Y32
VCC55 Y31
VCC56 Y30
VCC57 Y29
VCC58 Y28
VCC59 Y27
VCC60 Y26
VCC61 V35
VCC62 V34
VCC63 V33
VCC64 V32
VCC65 V31
VCC66 V30
VCC67 V29
VCC68 V28
VCC69 V27
VCC70 V26
VCC71 U35
VCC72 U34
VCC73 U33
VCC74 U32
VCC75 U31
VCC76 U30
VCC77 U29
VCC78 U28
VCC79 U27
VCC80 U26
VCC81 R35
VCC82 R34
VCC83 R33
VCC84 R32
VCC85 R31
VCC86 R30
VCC87 R29
VCC88 R28
VCC89 R27
VCC90 R26
VCC91 P35
VCC92 P34
VCC93 P33
VCC94 P32
VCC95 P31
VCC96 P30
VCC97 P29
VCC98 P28
VCC99 P27
VCC100 P26

VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AG10
VCCIO4 AC10
VCCIO5 Y10
VCCIO6 U10
VCCIO7 P10
VCCIO8 L10
VCCIO9 J14
VCCIO10 J13
VCCIO11 J12
VCCIO12 J11
VCCIO13 H14
VCCIO14 H12
VCCIO15 H11
VCCIO16 G14
VCCIO17 G13
VCCIO18 G12
VCCIO19 F14
VCCIO20 F13
VCCIO21 F12
VCCIO22 F11
VCCIO23 E14
VCCIO24 E12
VCCIO25 E11
VCCIO26 D14
VCCIO27 D13
VCCIO28 D12
VCCIO29 D11
VCCIO30 C14
VCCIO31 C13
VCCIO32 C12
VCCIO33 C11
VCCIO34 B14
VCCIO35 B12
VCCIO36 A14
VCCIO37 A13
VCCIO38 A12
VCCIO39 A11
VCCIO40 J23

Sandy Bridge_rPGA_Rev0p61
CONN@

Material Note (+1.05VS_VCCP)

2 x 330 µF
(3x 330 µF for 2012 capable designs)
Top Socket Cavity 22U 0805 *7
Bottom Socket Cavity 22U 0805 *5

+1.05VS_VCCP

C43 22U_0805_6.3V6M
C44 22U_0805_6.3V6M
C45 22U_0805_6.3V6M
C46 22U_0805_6.3V6M
C47 22U_0805_6.3V6M
C48 22U_0805_6.3V6M
C49 22U_0805_6.3V6M
C50 22U_0805_6.3V6M
C51 22U_0805_6.3V6M
C52 22U_0805_6.3V6M
C53 22U_0805_6.3V6M
C54 22U_0805_6.3V6M
C62 330U_D2_2V_Y
C63 330U_D2_2V_Y
@C64 330U_D2_2V_Y

Cap quantity follow 439028_HR_PDDG_R1_51

+1.05VS_VCCP

C83 330U_2.5V_M_R17
C73 330U_2.5V_M_R17

reserve for test
please co-layout with C62,C63

+1.05VS_VCCP +1.05VS_VCCP

R65 130_0402_5%
R66 75_0402_5%
R67 43_0402_1%

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

R68 0_0402_5%
R69 0_0402_5%

VR_SVID_ALRT# <55>
VR_SVID_CLK <55>
VR_SVID_DAT <55>

Resistors close to CPU

Close to CPU

+CPU_CORE

VCCSENSE R70 100_0402_1%
VSSSENSE R71 100_0402_1%

VCC_SENSE AJ35 VCCSENSE_R
VSS_SENSE AJ34 VSSSENSE_R

R72 0_0402_5%
R73 0_0402_5%

VCCSENSE <55>
VSSSENSE <55>

VCCIO_SENSE B10
VSSIO_SENSE A10

VCCIO_SENSE <52>
R74 10_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Sandy Bridge(4/6)-PWR

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 8 of 58

POWER Group2

Material Note (GFXCORE)
2 x 330 µF on Bottom socket edge
Bottom Socket Cavity 22U 0805 *2
Bottom Socket Edge 22U 0805 *4
Top Socket Cavity 22U 0805 *2
Top Socket Edge 22U 0805 *4

+GFX_CORE
C217 330U_D2_2V_Y
C225 330U_D2_2V_Y
22U_0805_6.3V6M: C284 C285 C286 C414 C415 C416 C364 C365 C410 C412 C411 C413

JCPUG
26A
AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17
VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

GRAPHICS

SENSE LINES
VAXG_SENSE AK35
VSSAXG_SENSE AK34
R131 100_0402_1% +GFX_CORE
VCC_AXG_SENSE <55>
VSS_AXG_SENSE <55>
R129 100_0402_1%

VREF
SM_VREF AL1
+1.5V_CPU
R76 0_0402_5%
R75 1K_0402_1%
+V_SM_VREF_CNT
+V_SM_VREF
@ Q3 AP2302GN-HF_SOT23-3
RUN_ON_CPU1.5VS3
R77 1K_0402_1%
C65 0.1U_0402_16V4Z

Follow DG V1.5 P.109
+V_SM_VREF should have 20 mil trace width

DDR3 -1.5V RAILS
5A
VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15
AF7 AF4 AE1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1
+1.5V_CPU
@ JP1 JUMP_43X118 +1.5V
10U_0603_6.3V6M: C66 C67 C68 C69 C70 C71
330U_D2_2V_Y C72

Material Note (VDDQ)
Bottom Socket Edge
1 x 330 µF
10U 0805 *6

SA RAIL
6A
VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8
M27 M26 L26 J26 J25 J24 H26 H25
+VCCSA
10U_0805_6.3V6M: C74 C75 C76
R78 0_0402_5%
330U_D2_2V_Y C73
VCCSA_SENSE

Material Note (VCCSA)
1 x 330 µF
Bottom Socket Cavity 10U 0805 *2
Bottom Socket Edge 10U 0805 *1

1.8V RAIL
+1.8VS R124 0_0805_5%
C79 330U_D2_2V_Y @
C80 10U_0603_6.3V6M
C81 1U_0402_6.3V6K
C82 1U_0402_6.3V6K
+1.8VS_VCCPLL
VCCPLL1 VCCPLL2 VCCPLL3
B6 A6 A2

Material Note (+1.8VS_VCCPLL)
1 x 330 µF
Bottom Socket Edge
1U 0402 *1
10U 0805 *1

MISC
VCCSA_SENSE H23
VCCSA_SENSE <54>
FC_C22 C22
VCCSA_VID1 C24
H_FC_C22
VCCSA_SEL <54>
R79 10K_0402_5%
@R80 0_0402_5%

Sandy Bridge_rPGA_Rev0p61
CONN@

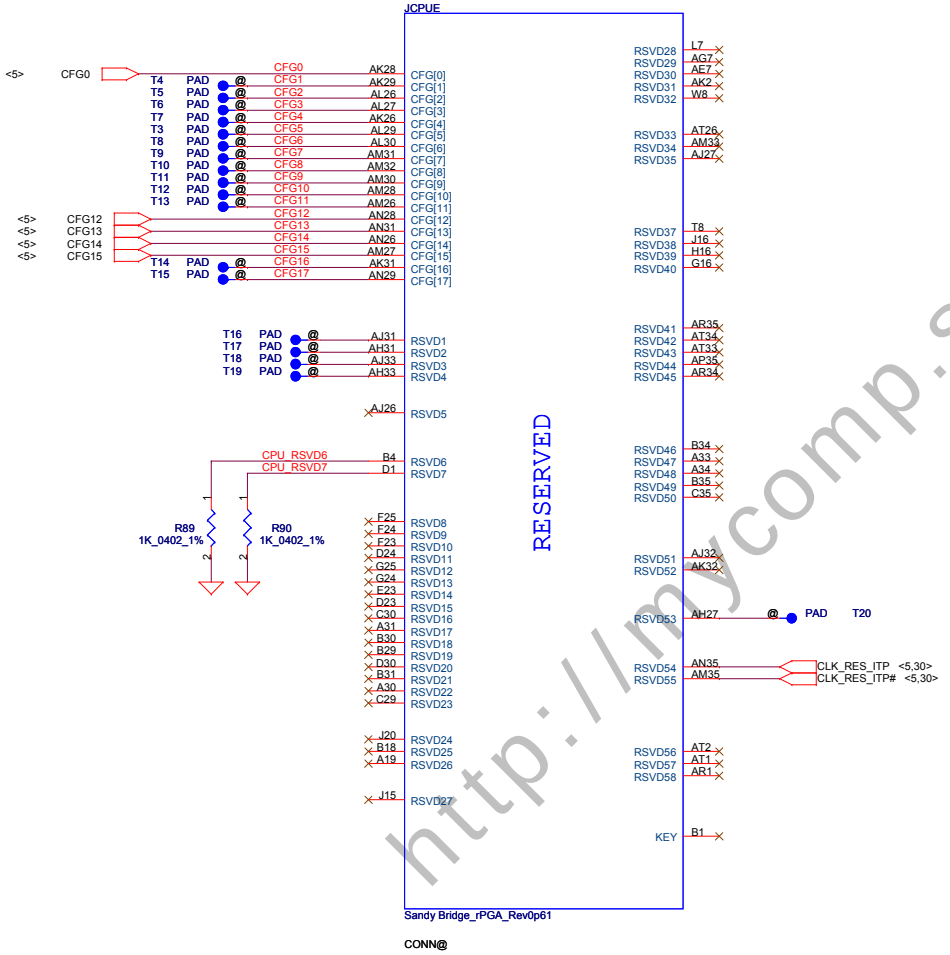
+1.5V_CPU Source

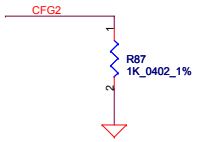
+VSB +1.5V +1.5V_CPU
Q4 SI4634DY-T1-GE3_SO8
+3VALW
R81 100K_0402_5%
R82 470_0603_5%
R83 100K_0402_5%
RUN_ON_CPU1.5VS3
RUN_ON_CPU1.5VS3#
R84 0_0402_5%
<43> CPU1.5V_S3_GATE
@R86 0_0402_5%
<43,46,50,52,54,57,58> SUSP#
Q35B 2N7002DW-T/R7_SOT363-6
Q35A 2N7002DW-T/R7_SOT363-6
R85 330K_0402_5%
C86 0.1U_0402_16V4Z
Q6 2N7002H 1N SOT23-3

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

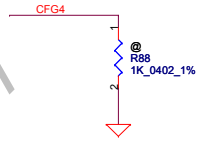
Compal Electronics, Inc.
Title: Sandy Bridge(4/6)-PWR
Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1
Date: Friday, January 21, 2011 | Sheet 9 of 58

CFG Straps for Processor

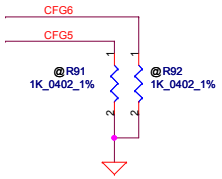




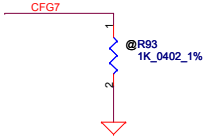
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



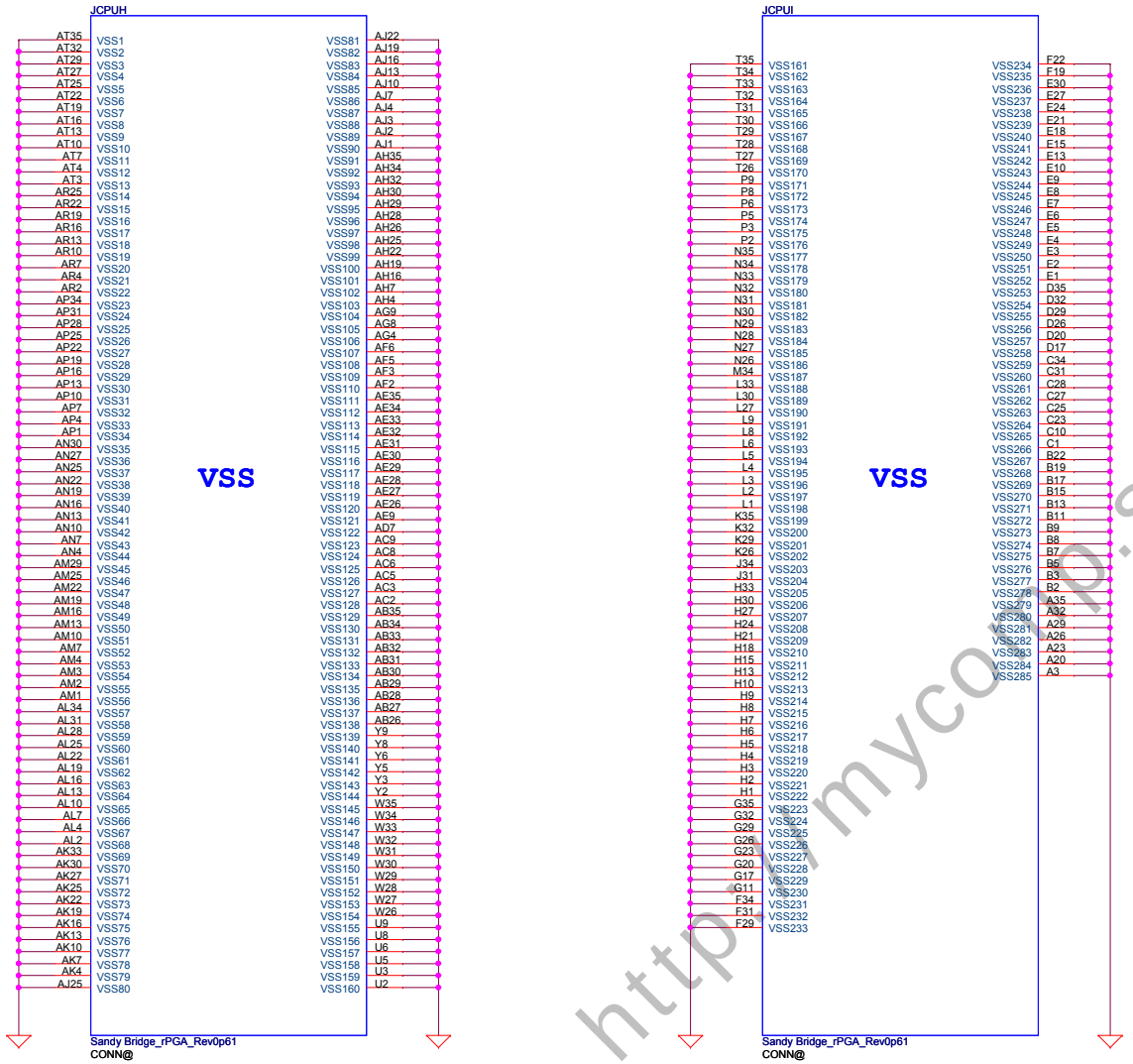
PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

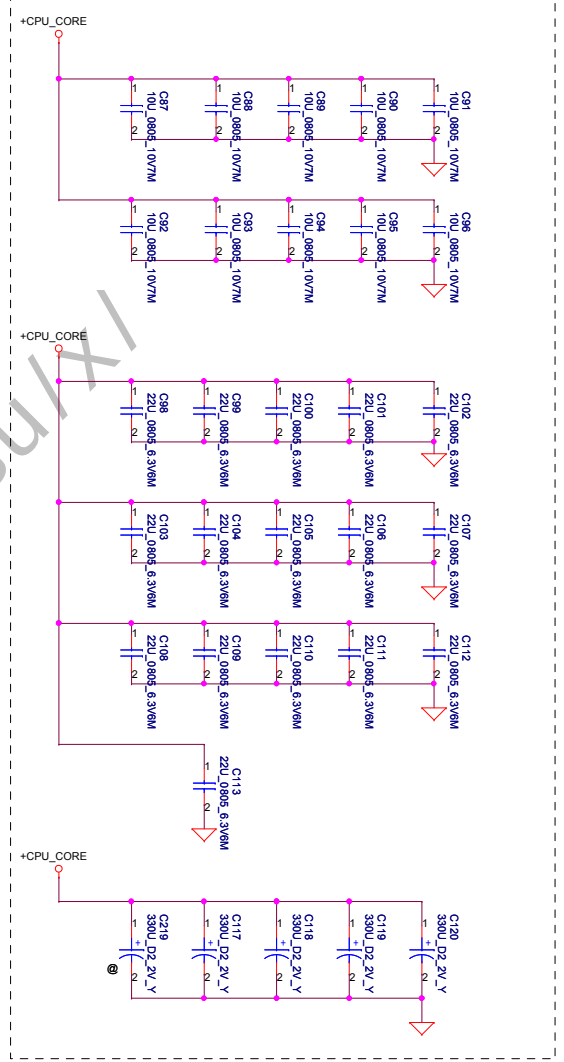
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.			
Title	Sandy Bridge(5/6) Reserve		
Size: Custom	Document Number: PBL80 LA-7441P M/B		Rev: 0.1
Date: Friday, January 21, 2011	Sheet 10 of 58		



Material Note (+CPU_CORE)

4 x 330 µF
Top Socket Cavity 22U 0805 *8
Top Socket Edge 22U 0805 *8
Bottom Socket Cavity 10U 0805 *10



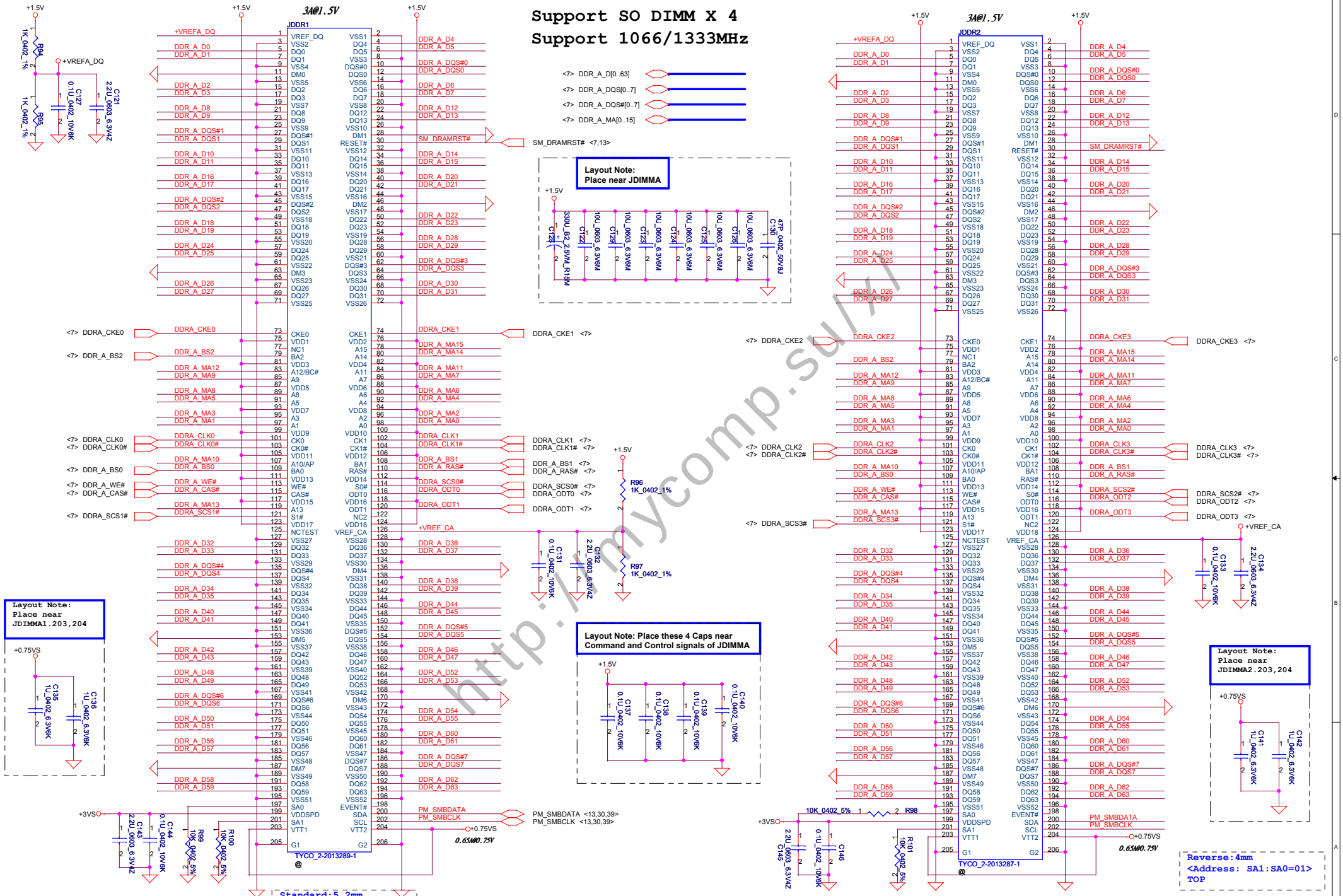
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Sandy Bridge(6/6)-GND

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 11 of 58



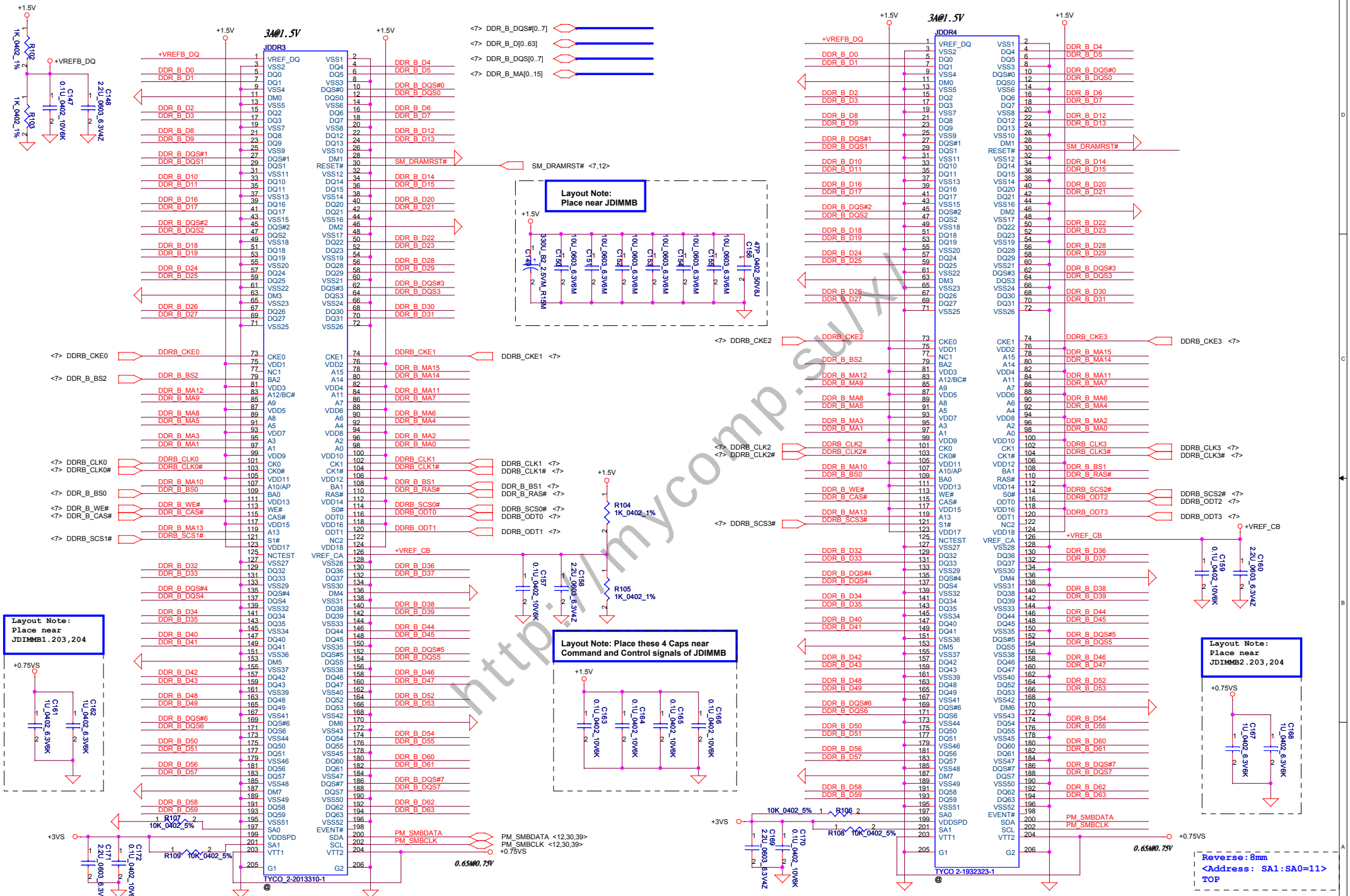
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: DDRIII-DIMMA

Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.1

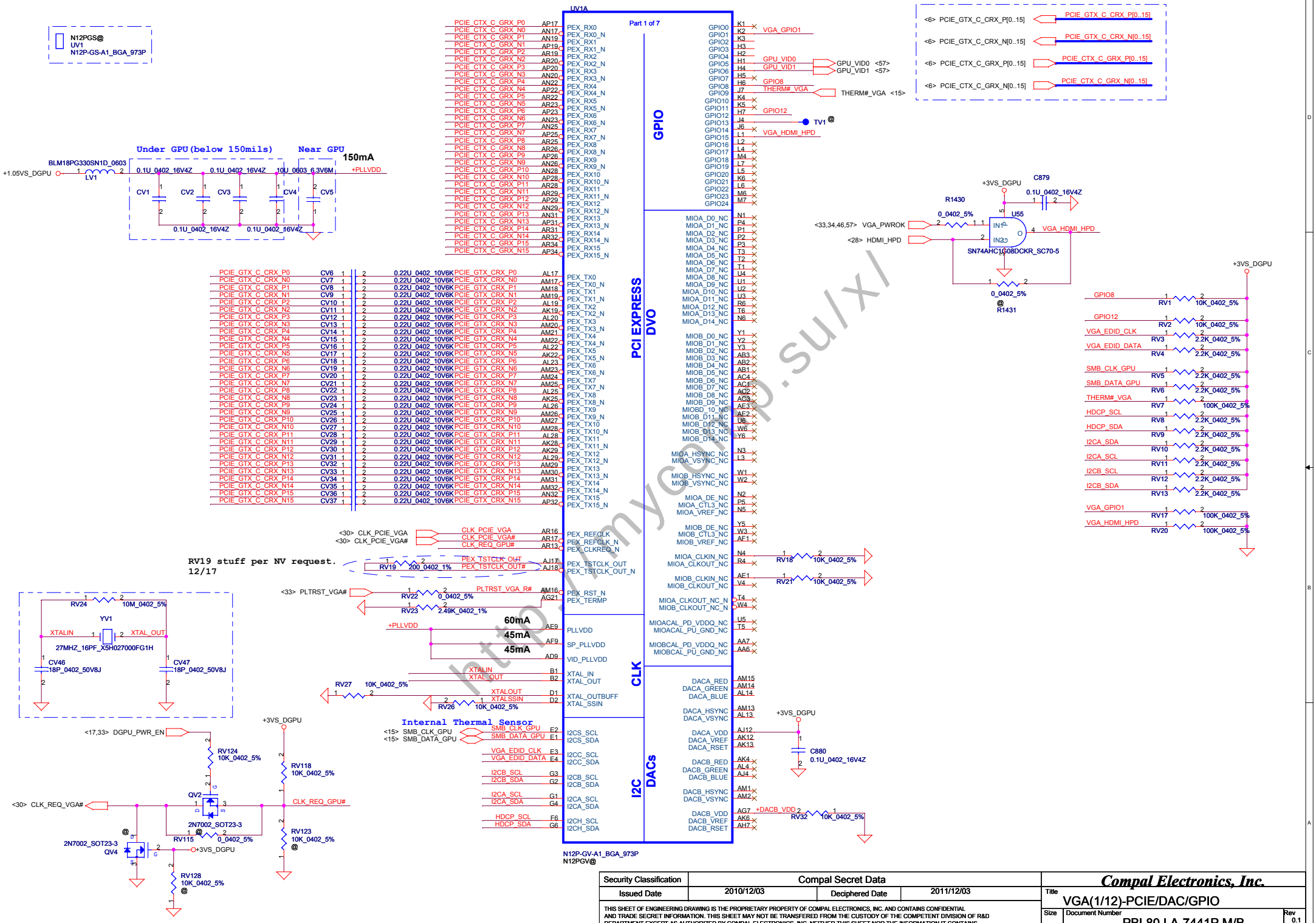
Date: Friday, January 21, 2011 Sheet 12 of 58



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title	DDRIII-DIMMB	
Size	Document Number	Rev
	PBL80 LA-7441P M/B	0.1
Date: Friday, January 21, 2011	Sheet 13 of 58	



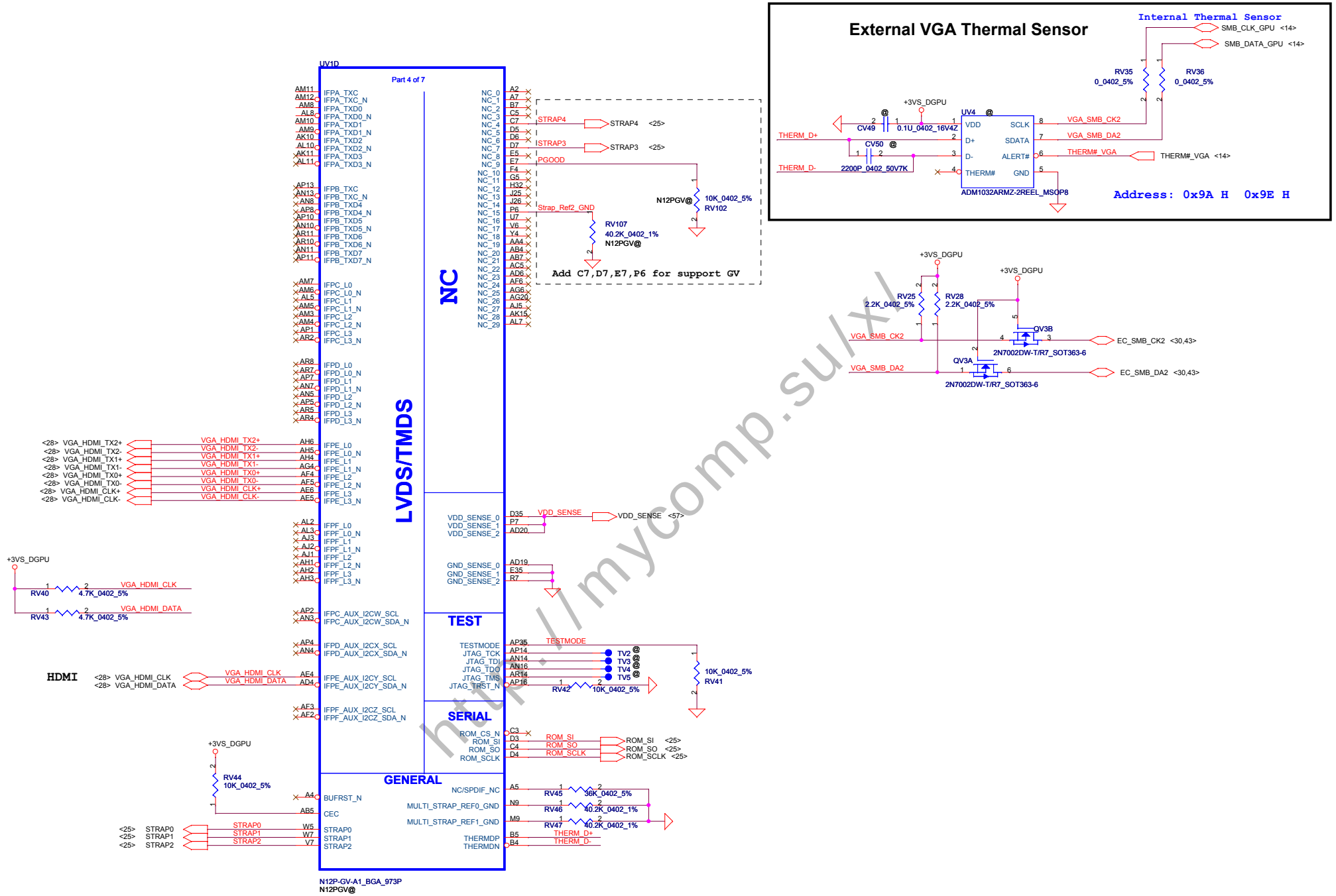
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(1/12)-PCIE/DAC/GPIO

Size: | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

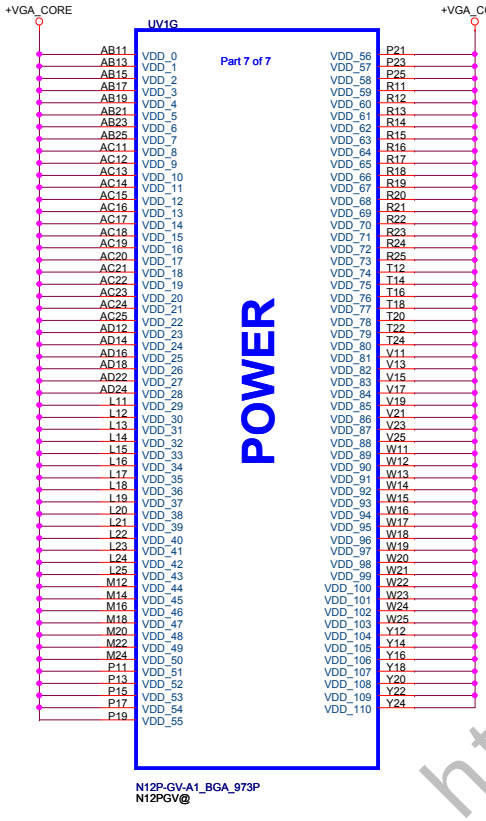
Date: Friday, January 21, 2011 | Sheet 14 of 58



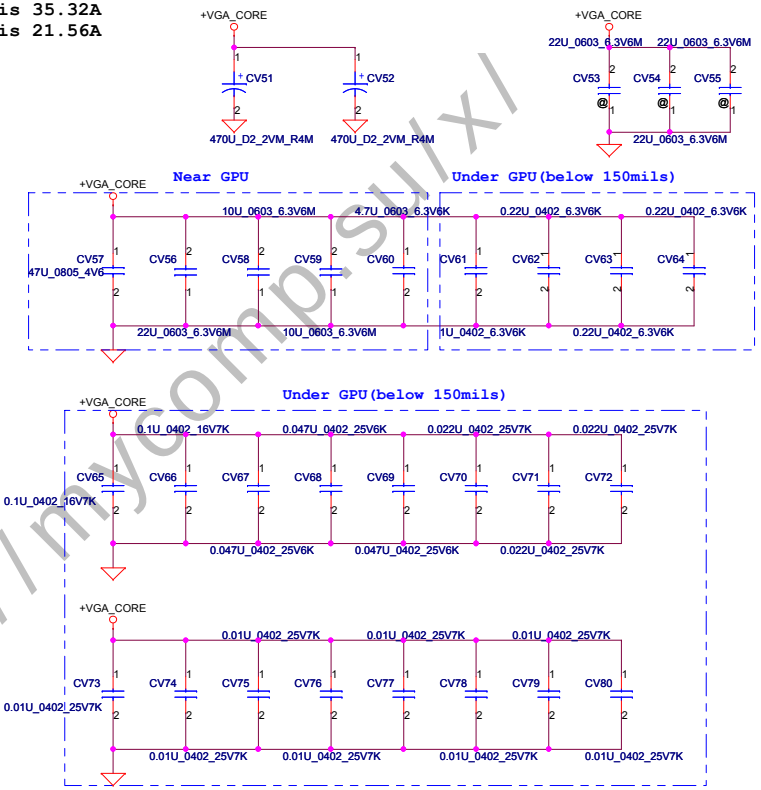
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.	
Title	VGA(2/12)-LVDS/HDMI/DP/THM
Size	Document Number: PBL80 LA-7441P M/B
Rev	0.1
Date: Friday, January 21, 2011	Sheet 15 of 58

Pstate	GPU_VID0	GPU_VID1	N12P-GS	N12P-GV
P8-P12	0	0	0.825V	0.85V
P0(Hot)	1	0	0.975V	1V
	0	1		
P0(cold)	1	1	1V	1.025V



GS EDP Peak is 35.32A
GV EDP Peak is 21.56A



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(3/12)-VGA CORE

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 16 of 58

GS is 5.49A
GV is 2.99A

GS is 2.95A
GV is 3.51A

Near GPU

Under GPU(below 150mils)

UV1E

Part 5 of 7

POWER

120mA

240mA (120mA each)

120mA(12~16mils)

220mA

570mA

+3VS to +3VS_DGPU

N12PGV@ N12P-GV-A1_BGA_973P

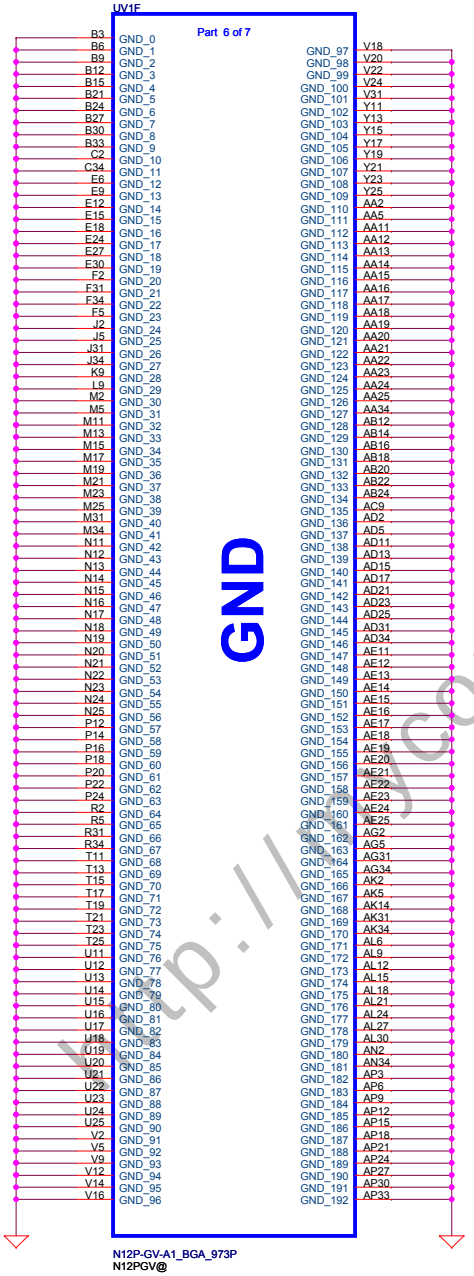
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(4/12)-POWER

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 17 of 58



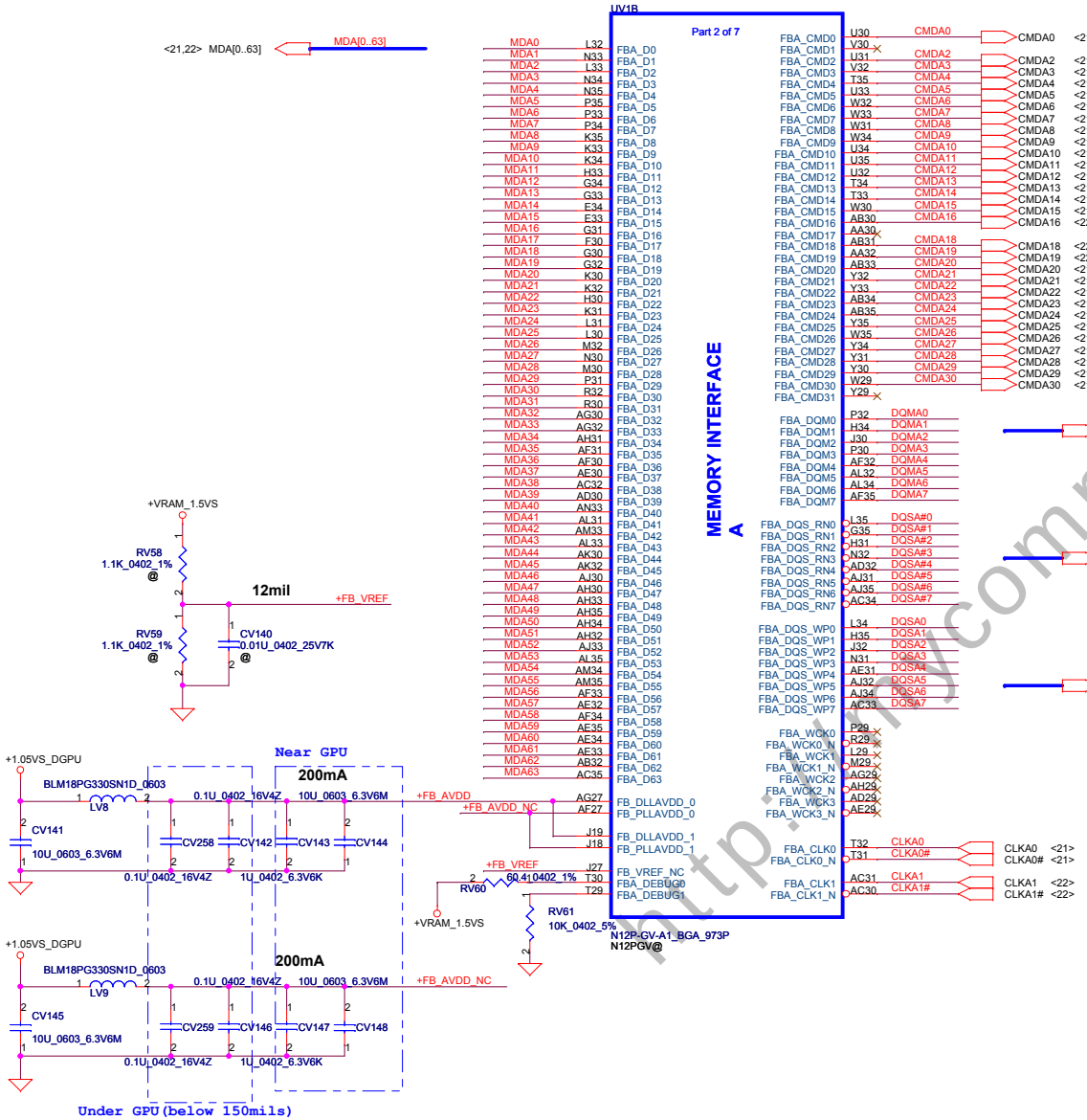
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(5/12)-GND

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 18 of 58



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

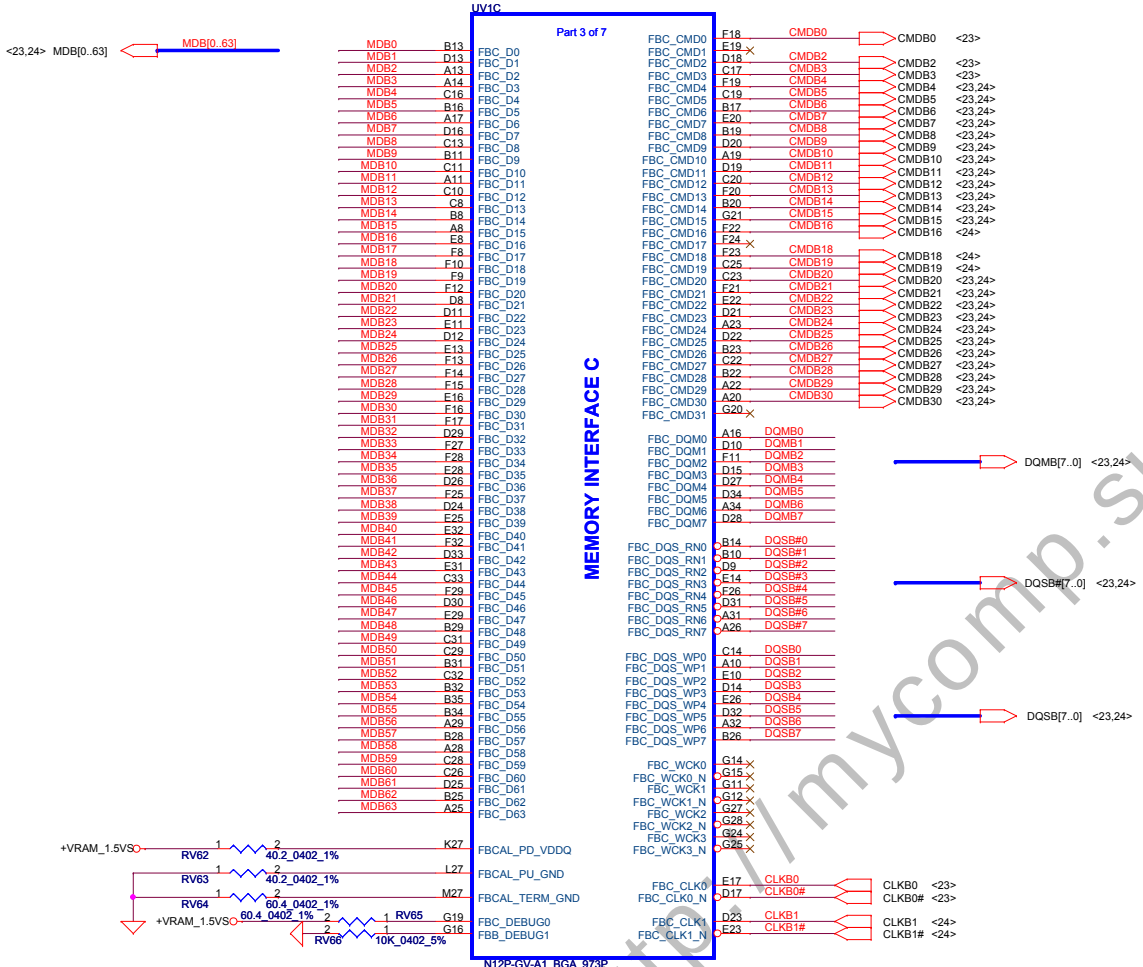
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(6/12)-MEM Interface A

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 19 of 58



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

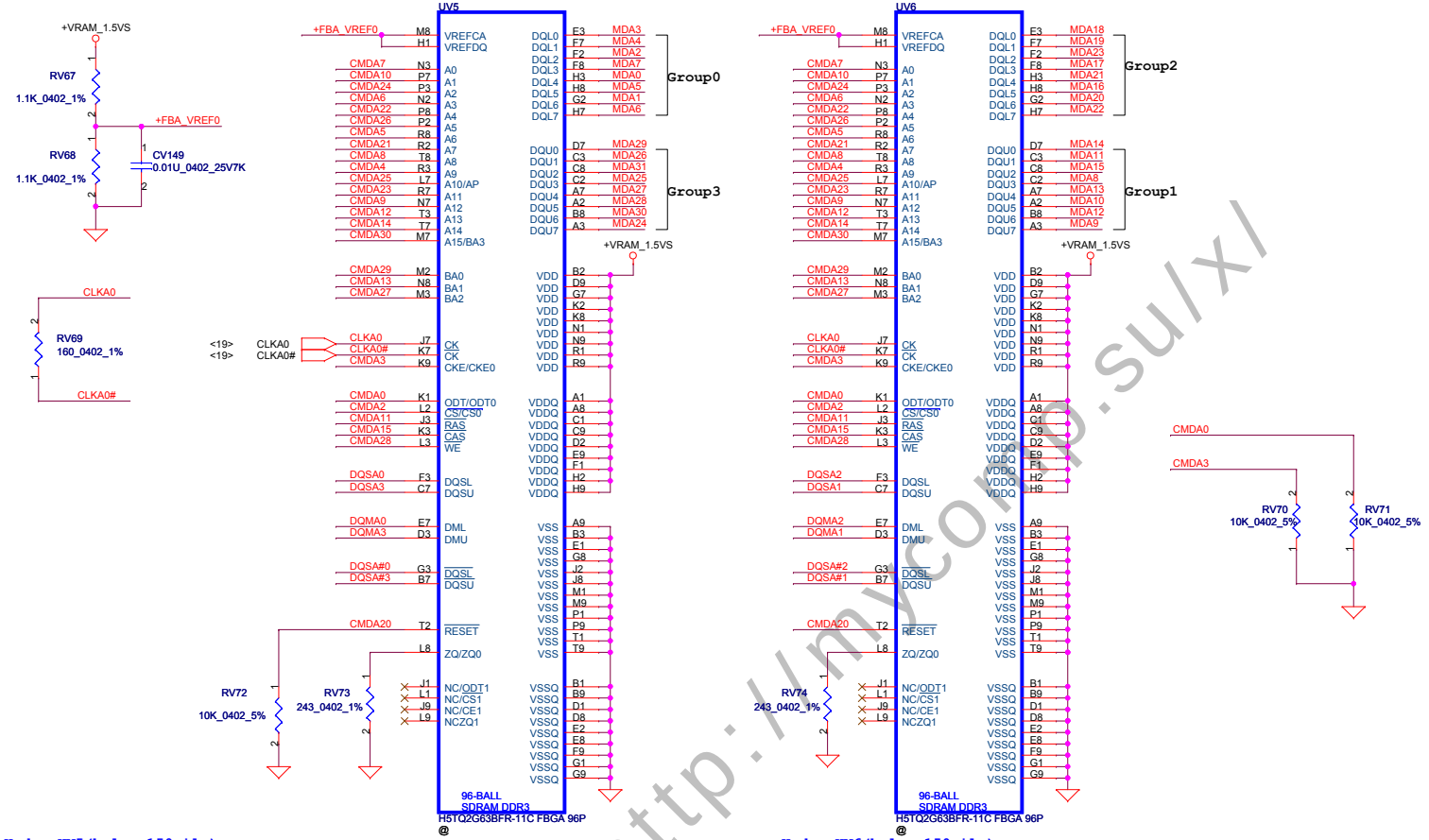
Title: VGA(7/12)-MEM Interface C

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 20 of 58

Memory Partition A - Lower 32 bits

Support N12P-GV/GS
Support Max VRAM 2G

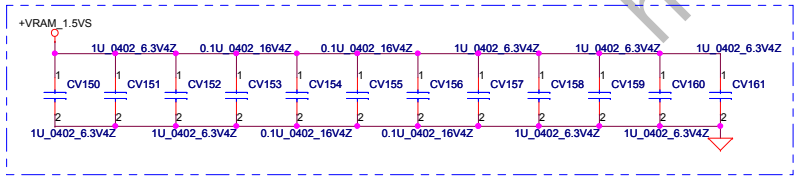


MDA[0..63] <19,22>
CMDA[30..0] <19,22>
DQMA[7..0] <19,22>
DQSA[7..0] <19,22>
DQSA#[7..0] <19,22>

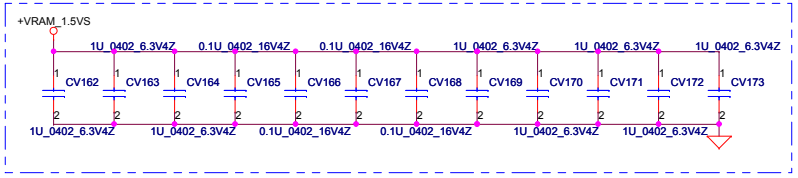
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Under UV5(below 150mils)



Under UV6(below 150mils)



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

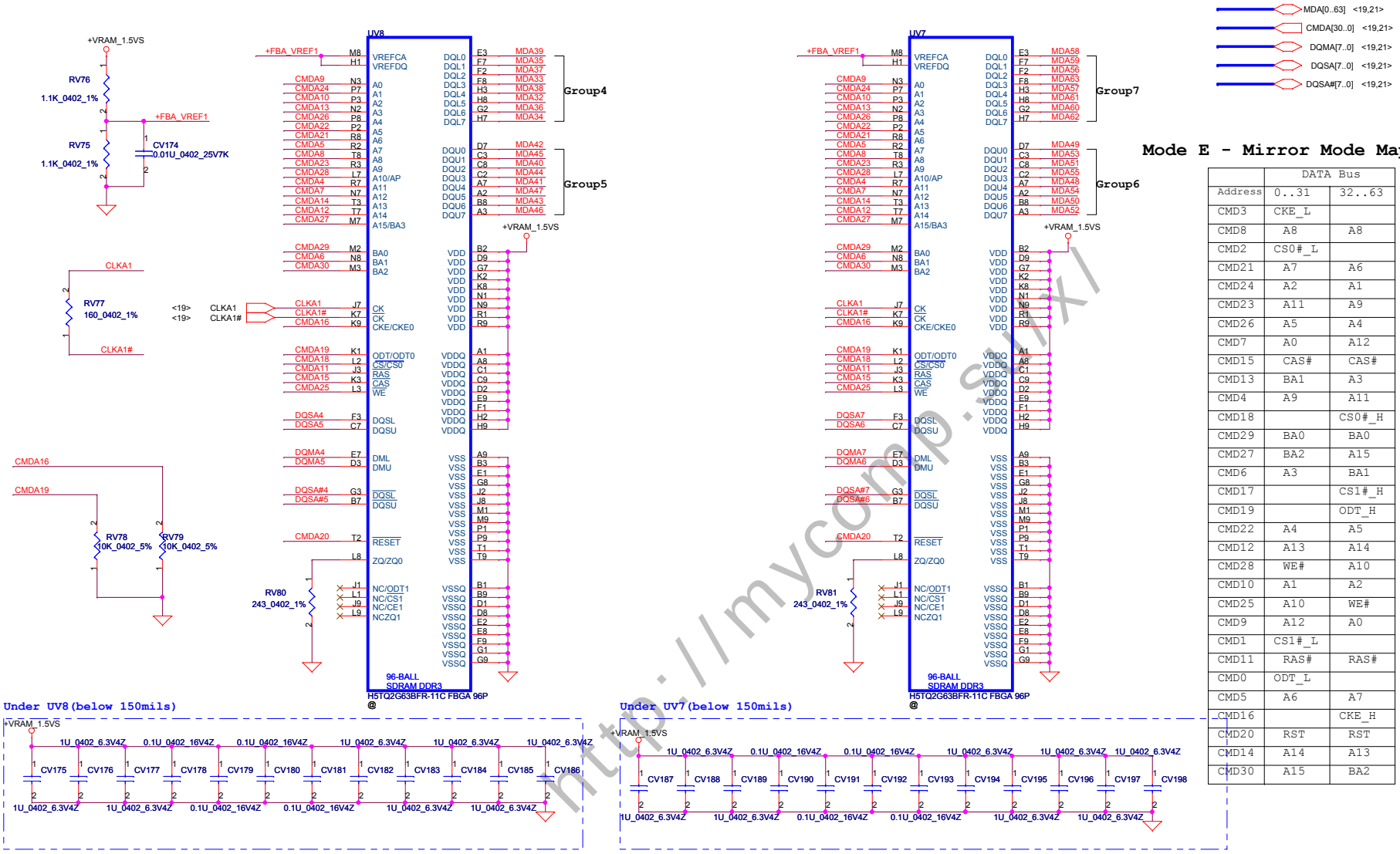
Compal Electronics, Inc.

Title: VGA(8/12)-VRAM A Lower

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 21 of 58

Memory Partition A - Upper 32 bits



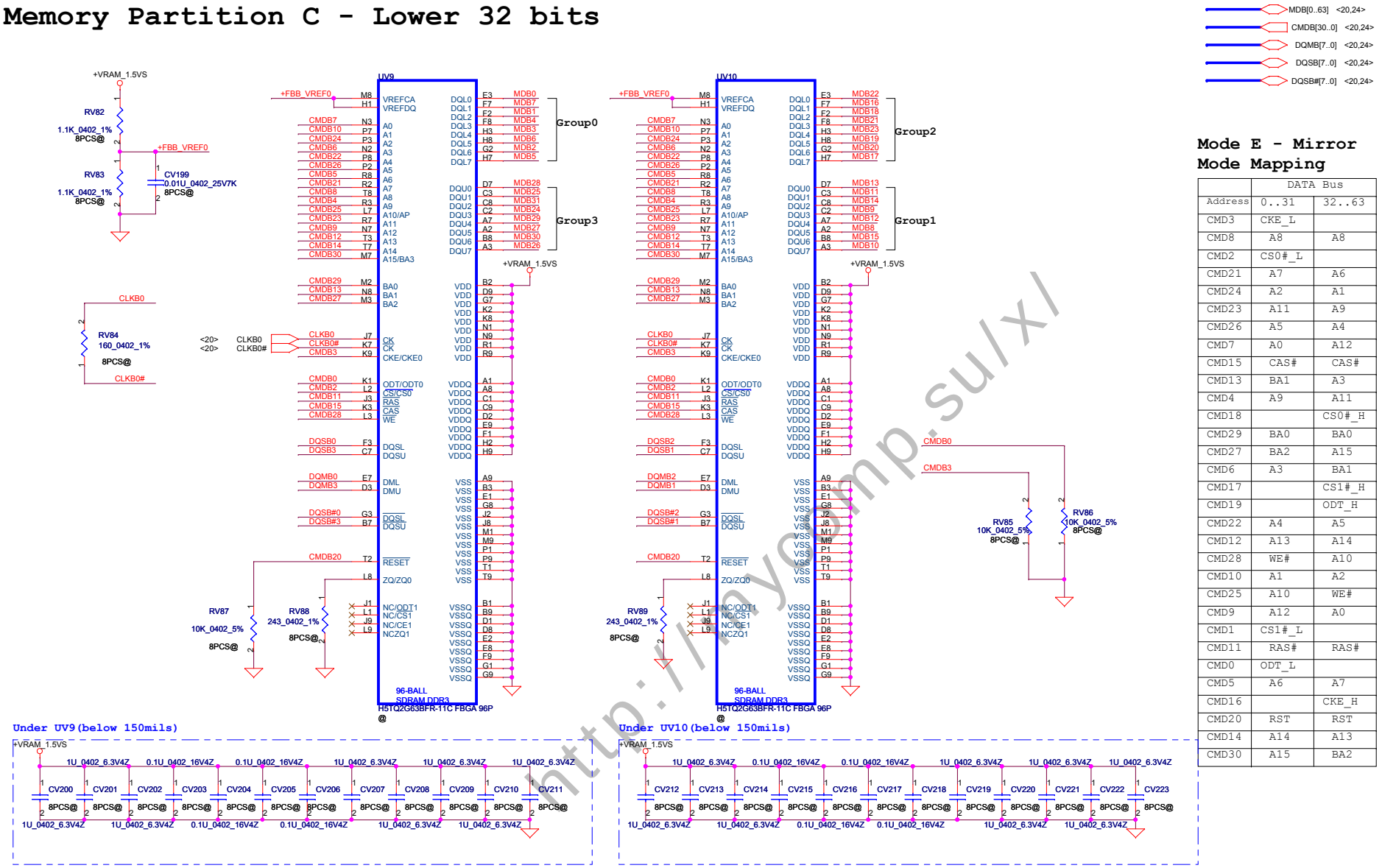
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.		
Title	VGA(9/12)-VRAM A Upper	
Size	Document Number	Rev
	PBL80 LA-7441P M/B	0.1
Date: Friday, January 21, 2011	Sheet 22 of 58	

Memory Partition C - Lower 32 bits



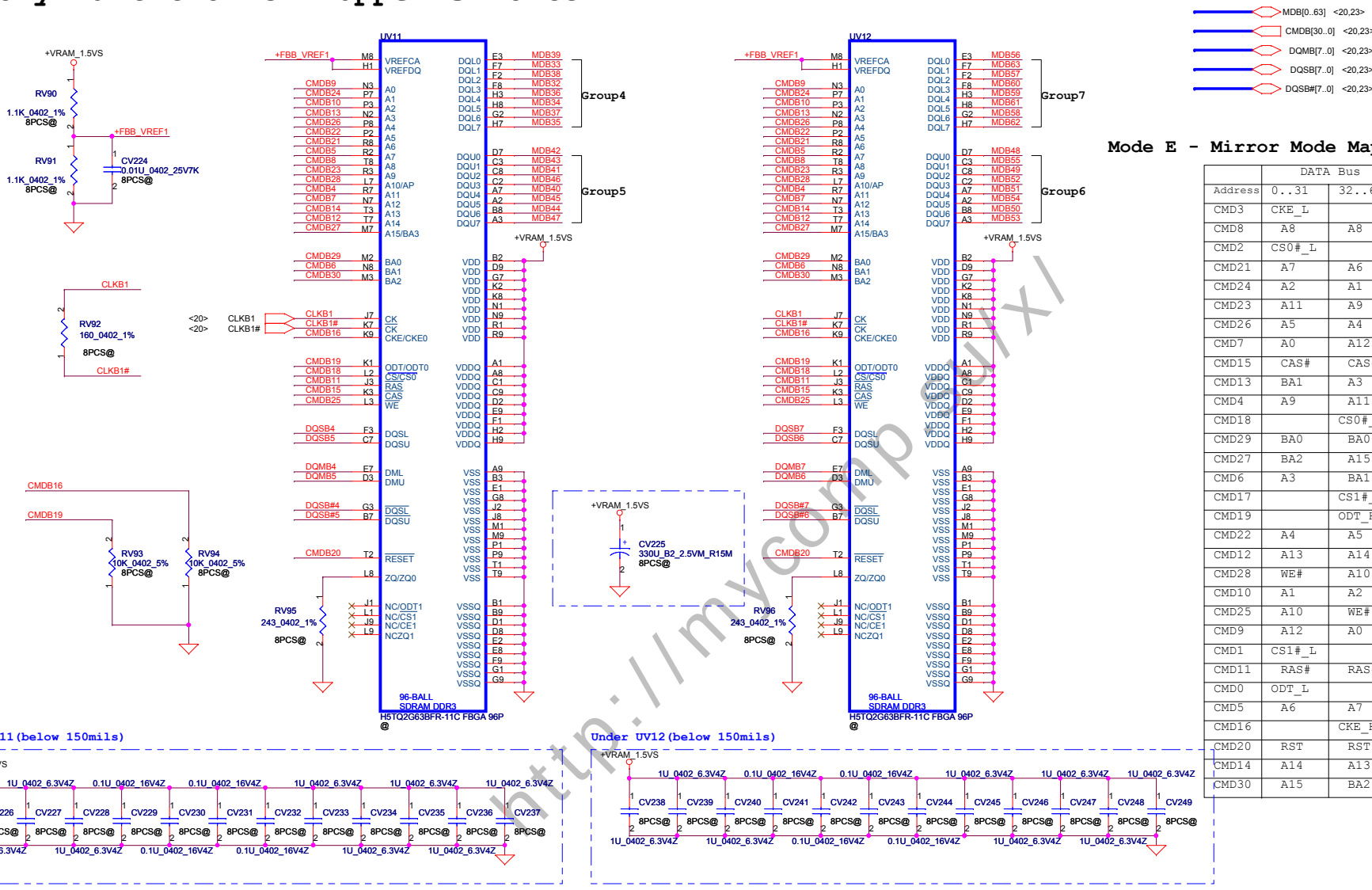
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.		
Title	VGA(10/12)-VRAM C Lower	
Size: Custom	Document Number: PBL80 LA-7441P M/B	Rev: 0.1
Date: Friday, January 21, 2011	Sheet 23 of 58	

Memory Partition C - Upper 32 bits

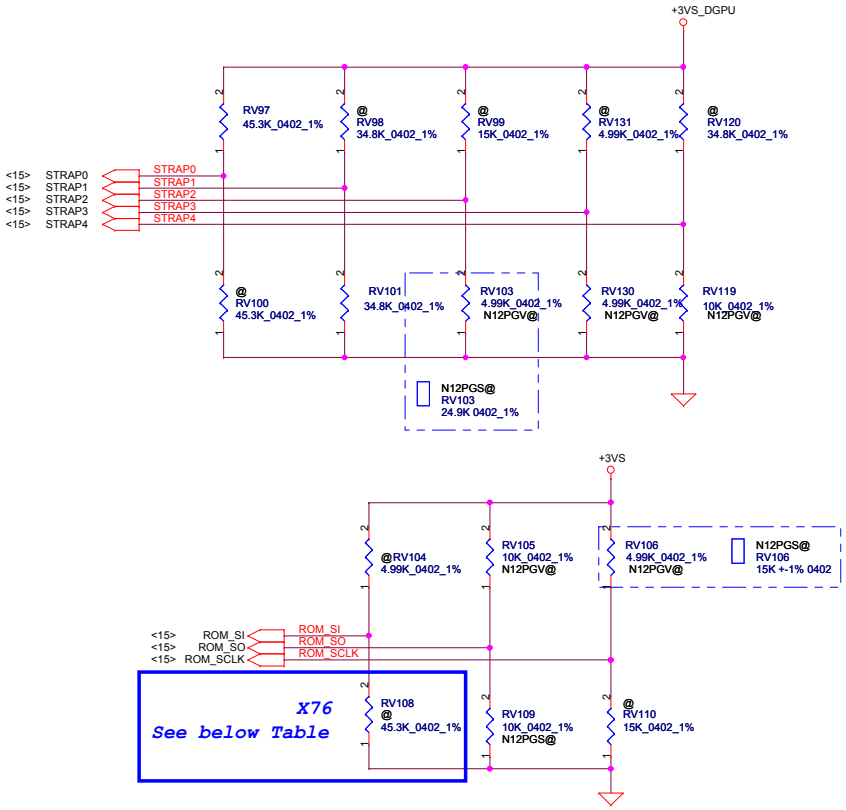


Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.			
Title	VGA(11/12)-VRAM C Upper		
Size: Custom	Document Number: PBL80 LA-7441P M/B		Rev: 0.1
Date: Friday, January 21, 2011	Sheet 24 of 58		



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SI	ROM_SCLK	ROM_SO	STRAP0
N12P-GS	0x0DF4	Below Table	Pull up 15K	Pull down 10K	Pull up 45K
N12P-GV	0x1050	Below Table	Pull up 5K	Pull up 10K	Pull up 45K

GPU	DeviceID	STRAP1	STRAP2	STRAP3	STRAP4
N12P-GS	0x0DF4	Pull down 35K	Pull down 25K		
N12P-GV	0x1050	Pull down 35K	Pull down 5K	Pull down 5K	Pull down 10K

GPU	DDR3 Type	VRAM		RAMCFG[3..0]		RV108
N12P-GS	64M16 900MHz	Hynix H5TQ1G63DFR-11C SA000041S20	512MB 1GB	0010	PD 15K	SD034154280 SD034154280
		Samsung K4W1G1646E-HC11 SA000041T00	512MB 1GB	0011	PD 20K	SD034200280 SD034200280
	128M16 900MHz	Hynix H5TQ2G63BFR-11C SA00003YO00	1GB 2GB	0110	PD 34.8K	SD034348280 SD034348280
		Samsung K4W2G1646C-HC11 SA000047Q00	1GB 2GB	0111	PD 45.3K	SD034453280 SD034453280
N12P-GV	64M16 800MHz	Hynix H5TQ1G63DFR-12C SA0000324C0	512MB	0010	PD 15K	SD034154280
		Samsung K4W1G1646G-BC12 SA00004HS00	512MB	0011	PD 20K	SD034200280
	128M16 800MHz	Hynix H5TQ2G63BFR-12C SA00003VS00	1GB	0110	PD 34.8K	SD034348280
		Samsung K4W2G1646C-HC12 SA00003MQ40	1GB	0111	PD 45.3K	SD034453280

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

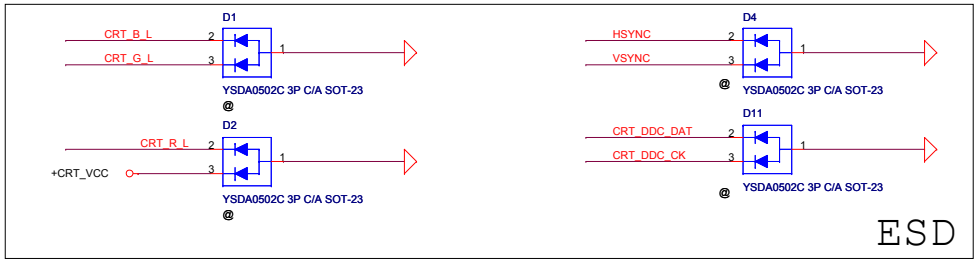
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

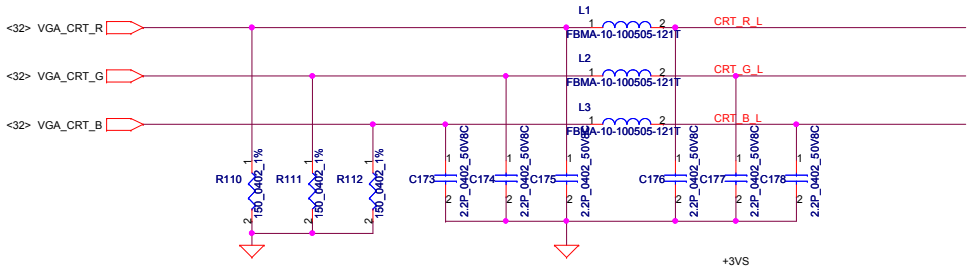
Compal Electronics, Inc.

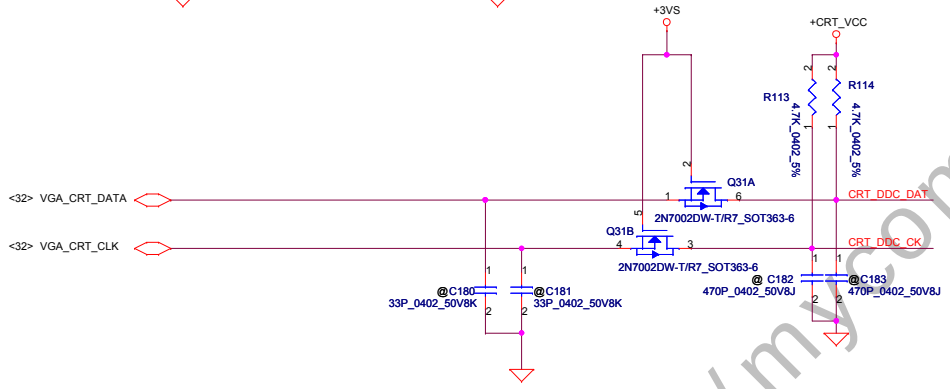
Title: VGA(12/12)-MISC

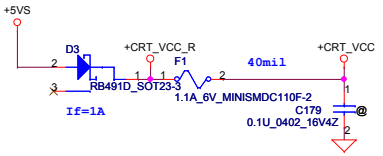
Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

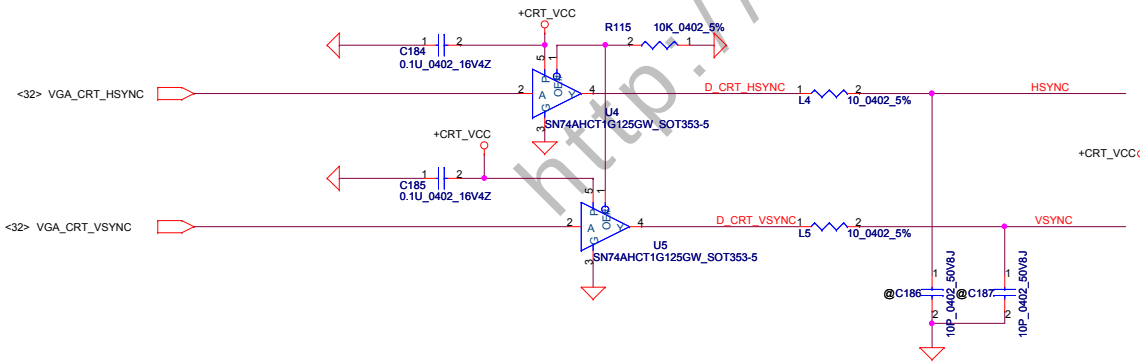
Date: Friday, January 21, 2011 | Sheet 25 of 58



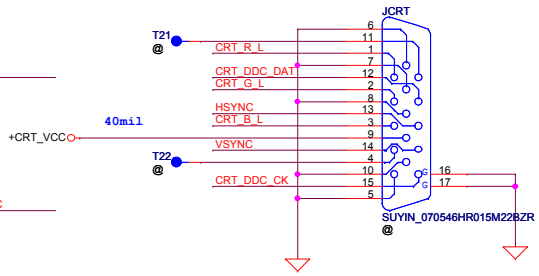






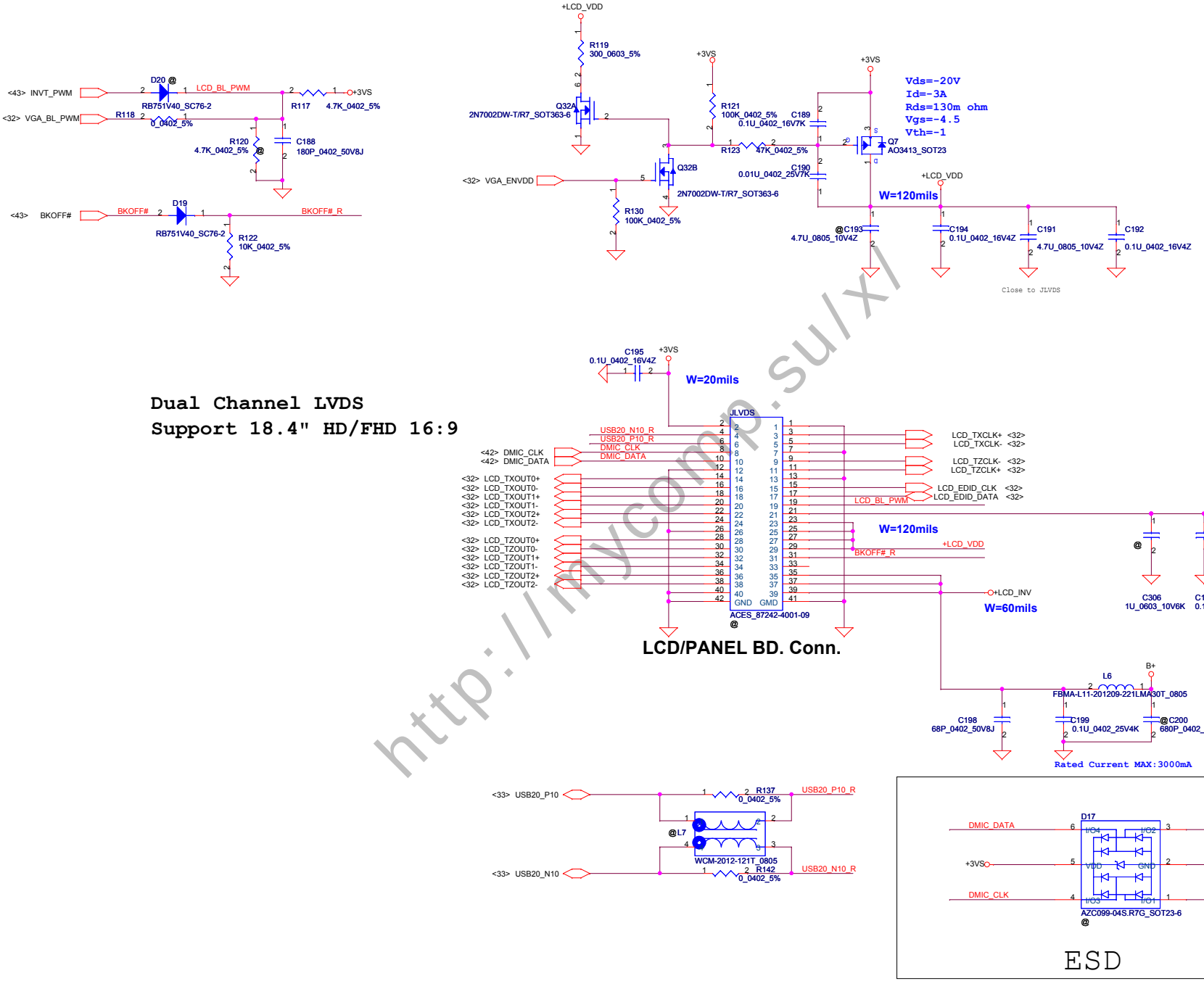


CRT CONNECTOR



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.			
Title	CRT		
Size	Document Number	PBL80 LA-7441P M/B	Rev 0.1
Date: Friday, January 21, 2011	Sheet 26 of 58		



Dual Channel LVDS
Support 18.4" HD/FHD 16:9

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

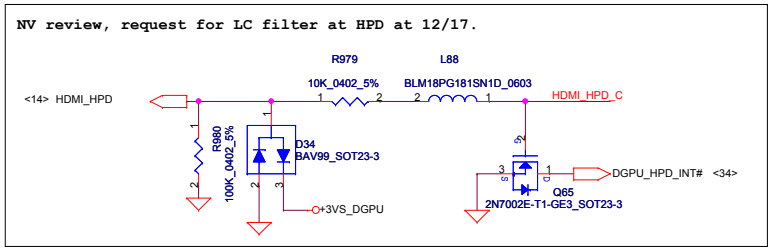
Compal Electronics, Inc.

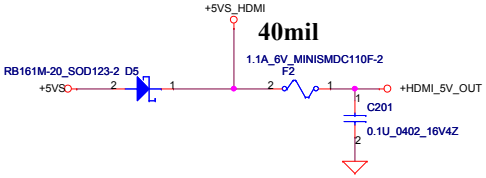
Title: LVDS

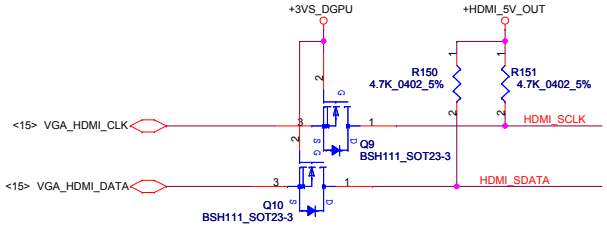
Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

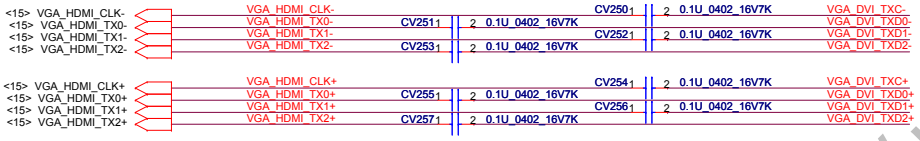
Date: Friday, January 21, 2011 | Sheet 27 of 58

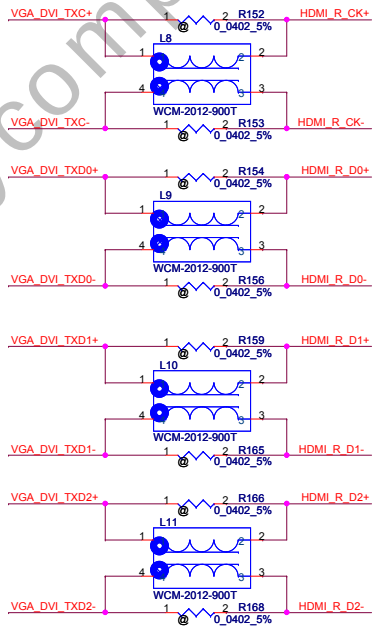
HDMI Connector

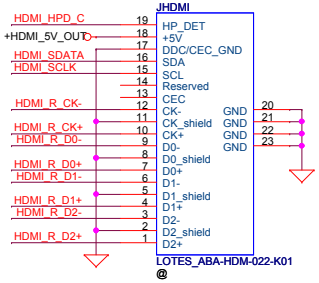


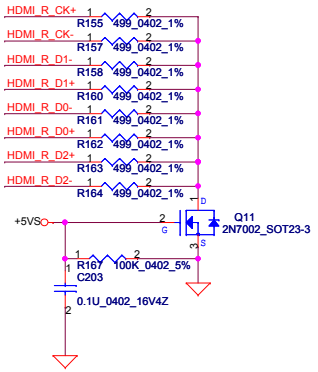


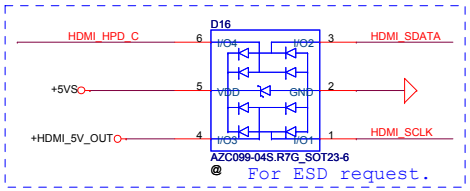


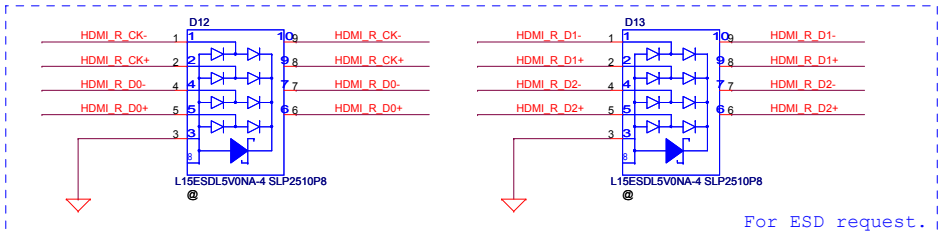












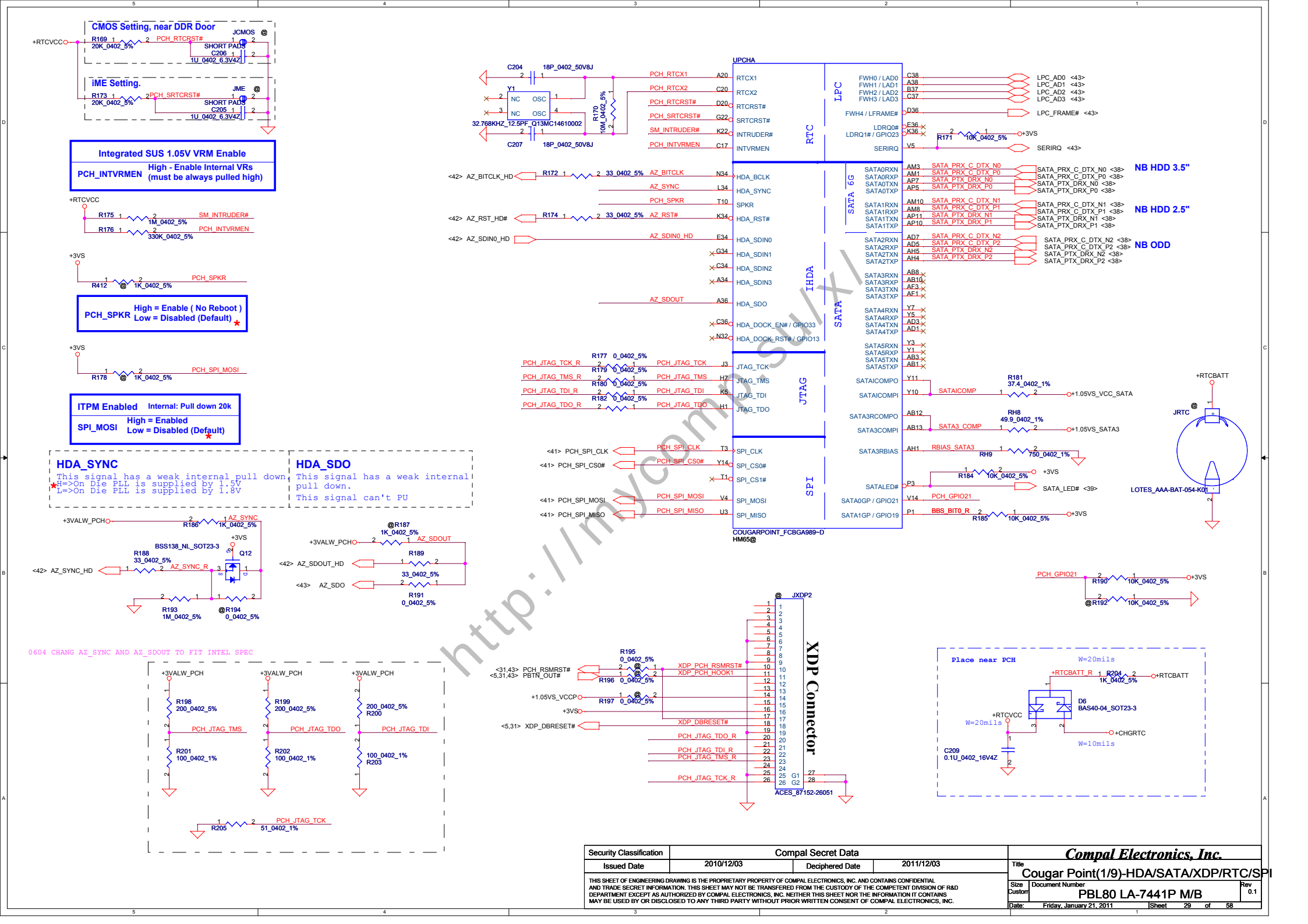
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
	PBL80 LA-7441P M/B	0.1

Date: Friday, January 21, 2011 Sheet 28 of 58



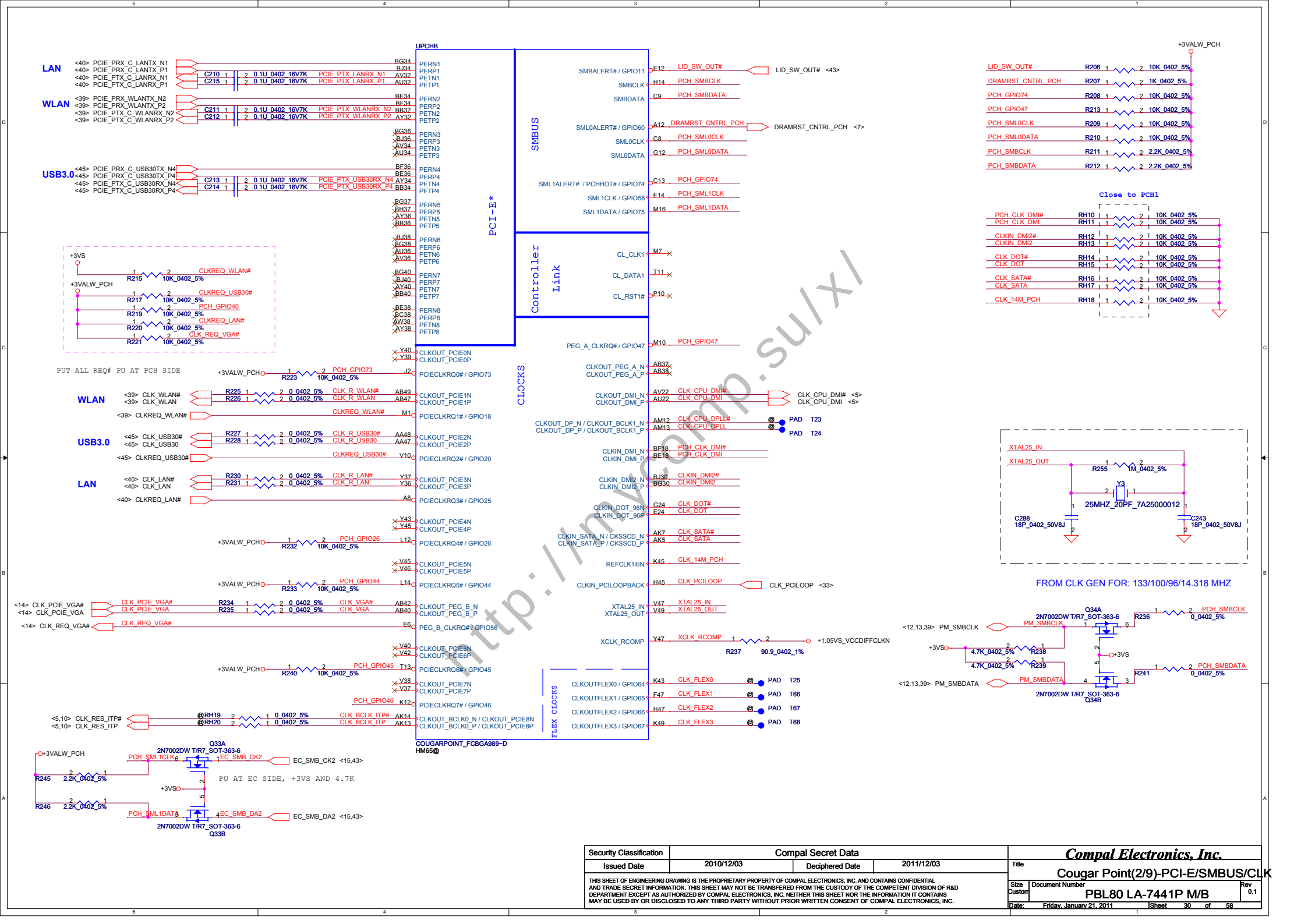
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(1/9)-HDA/SATA/XDP/RTC/SPI

Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.1

Date: Friday, January 21, 2011 Sheet 29 of 58



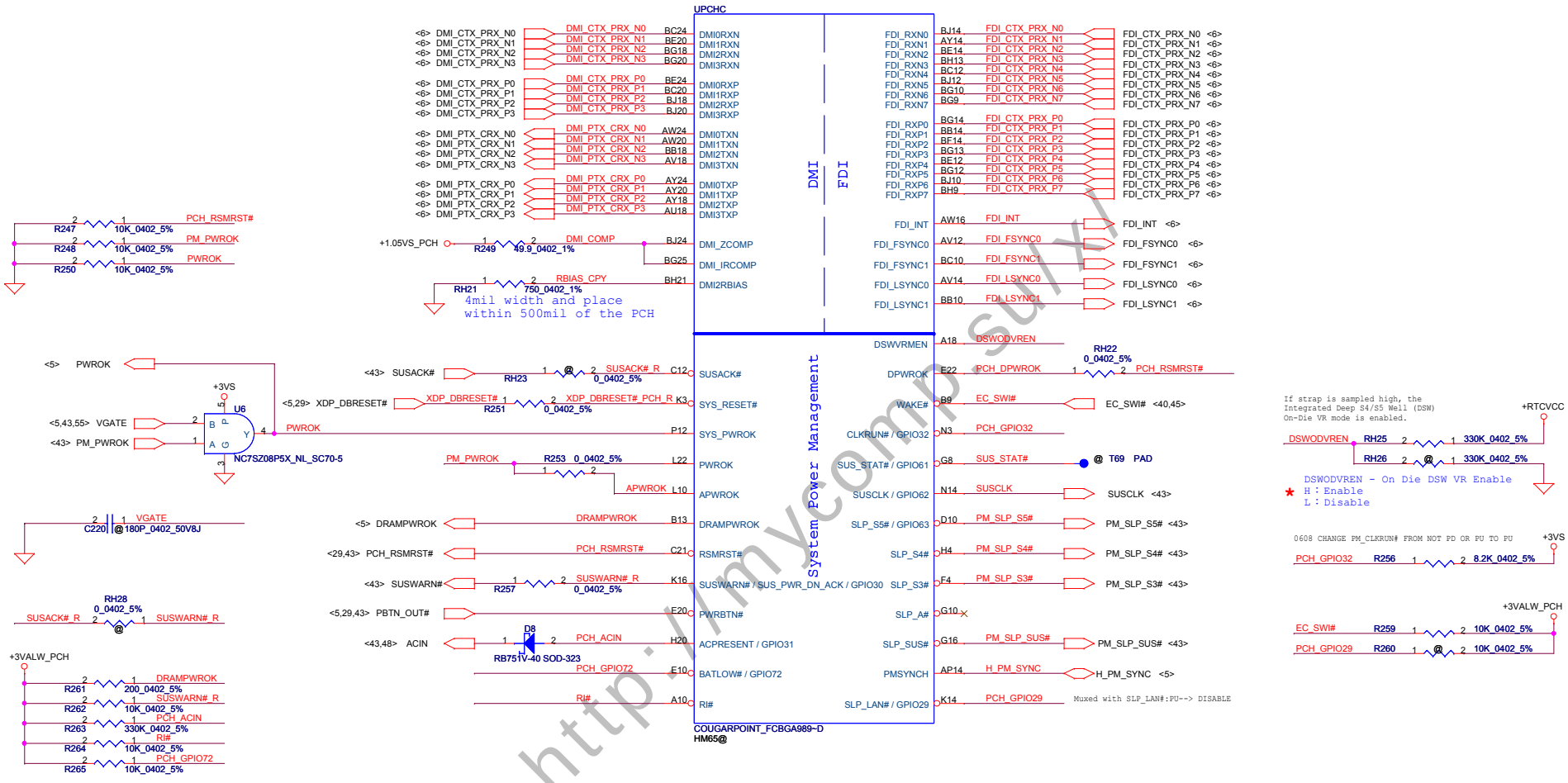
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(2/9)-PCI-E/SMBUS/CLK

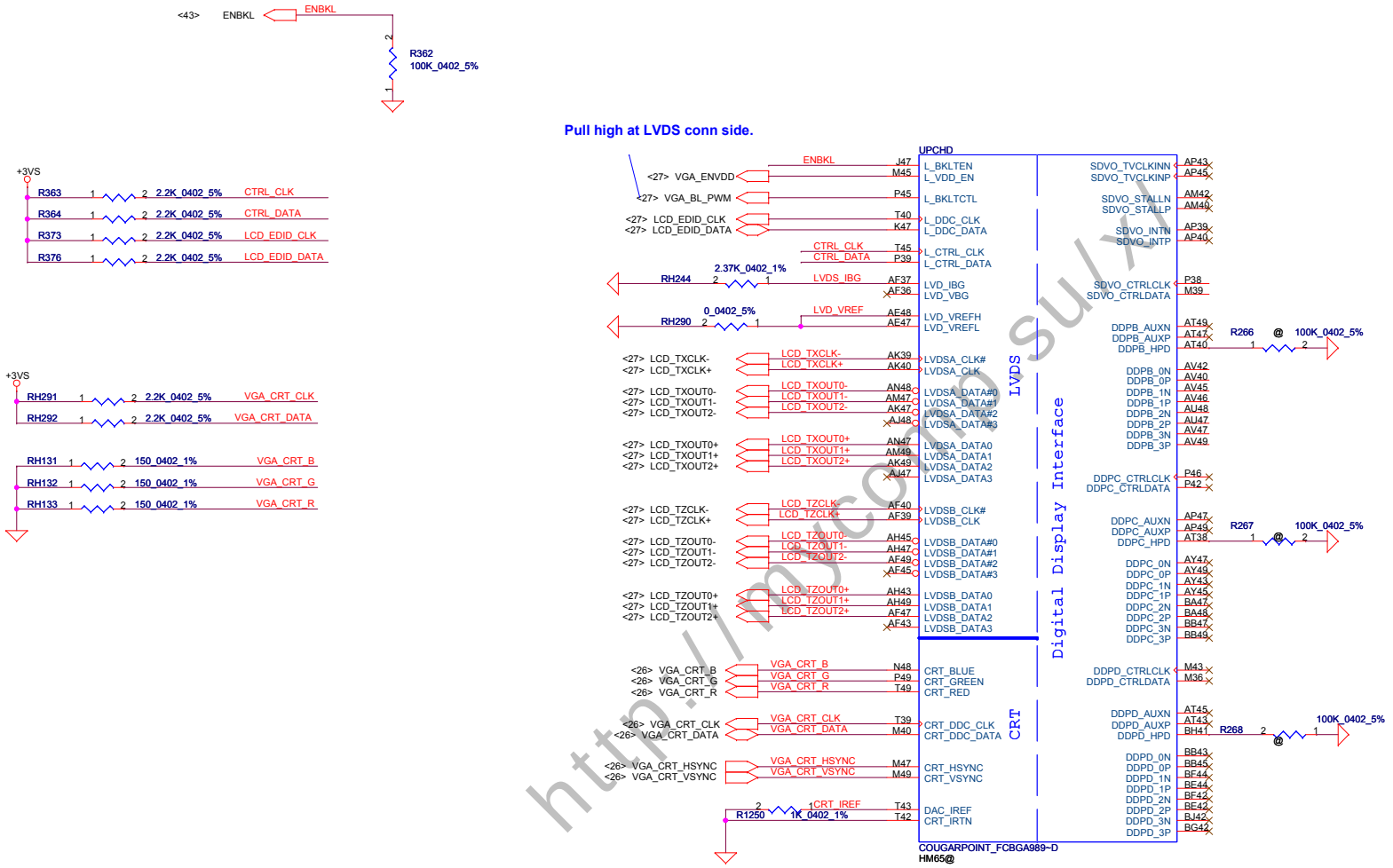
Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.1

Date: Friday, January 21, 2011 Sheet 30 of 58



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.	
Title	Cougar Point(3/9)-DMI/FDI/PWM
Size: Custom	Document Number: PBL80 LA-7441P M/B
Rev	0.1
Date: Friday, January 21, 2011	Sheet 31 of 58



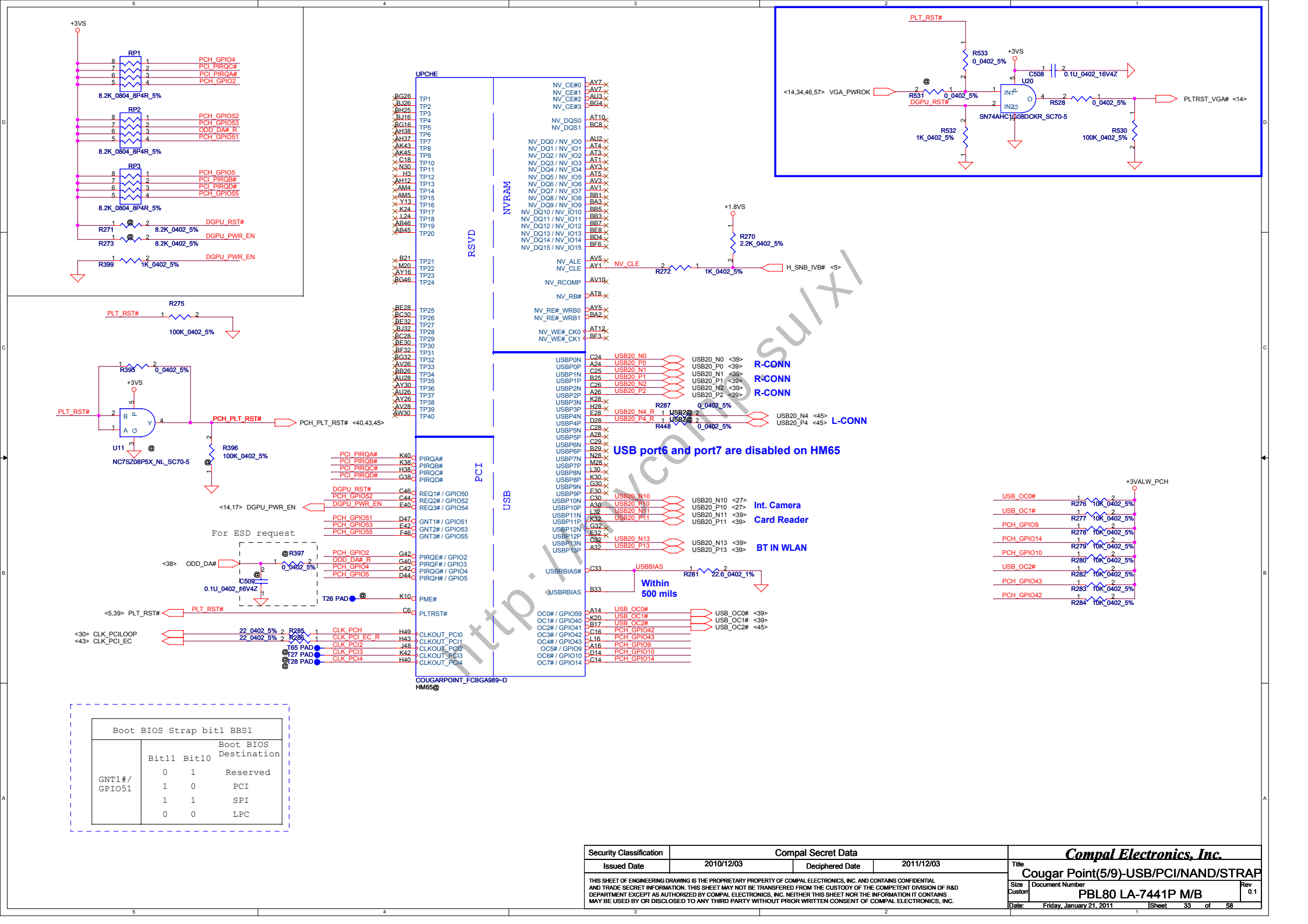
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(4/9)-CRT/LVDS/HDMI/DP

Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.1

Date: Friday, January 21, 2011 Sheet 32 of 58



Boot BIOS Strap bit1 BBS1			
	Bit11	Bit10	Boot BIOS Destination
GNT1#/ GPIO51	0	1	Reserved
	1	0	PCI
	1	1	SPI
	0	0	LPC

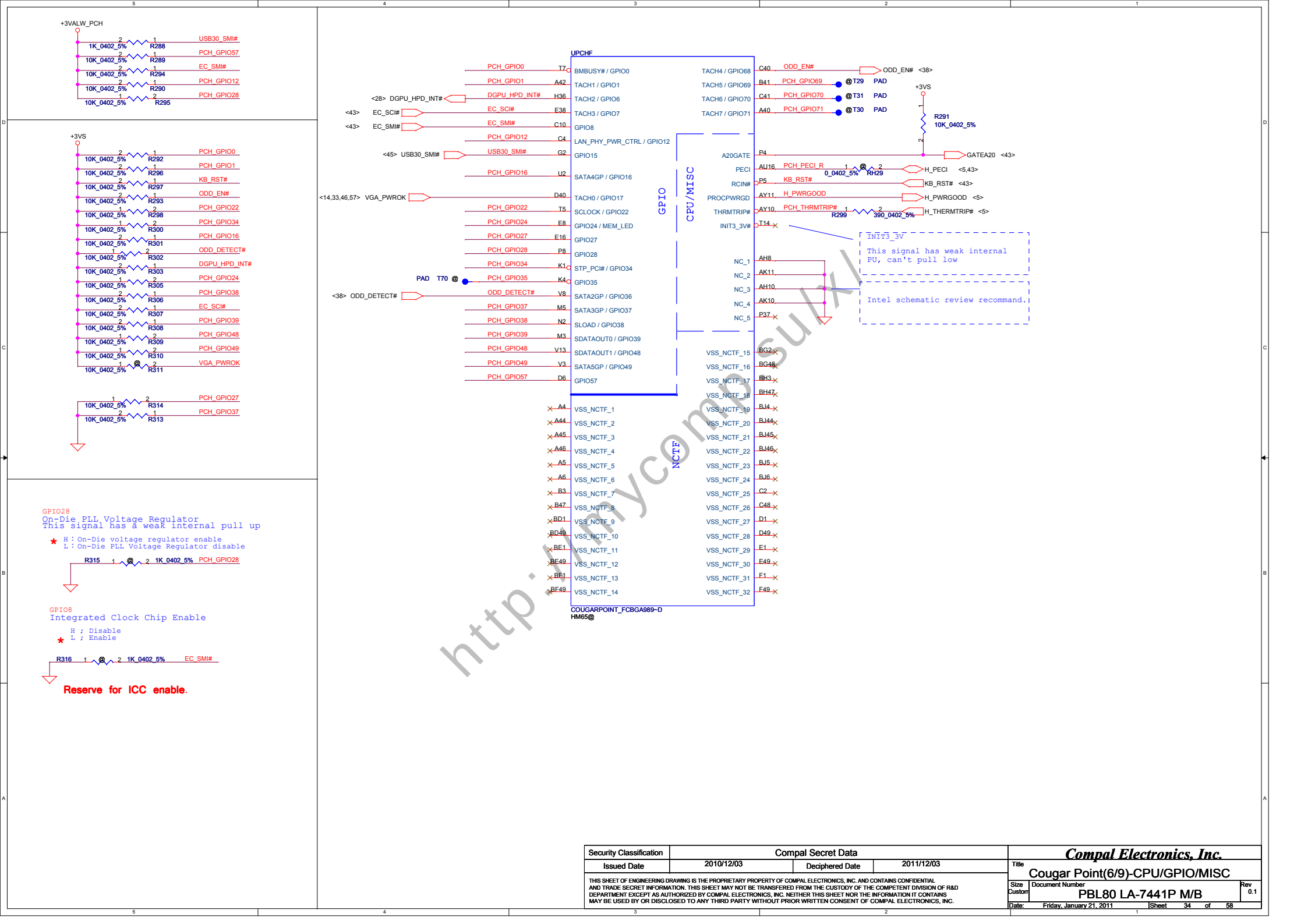
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(5/9)-USB/PCI/NAND/STRAP

Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.1

Date: Friday, January 21, 2011 Sheet 33 of 58



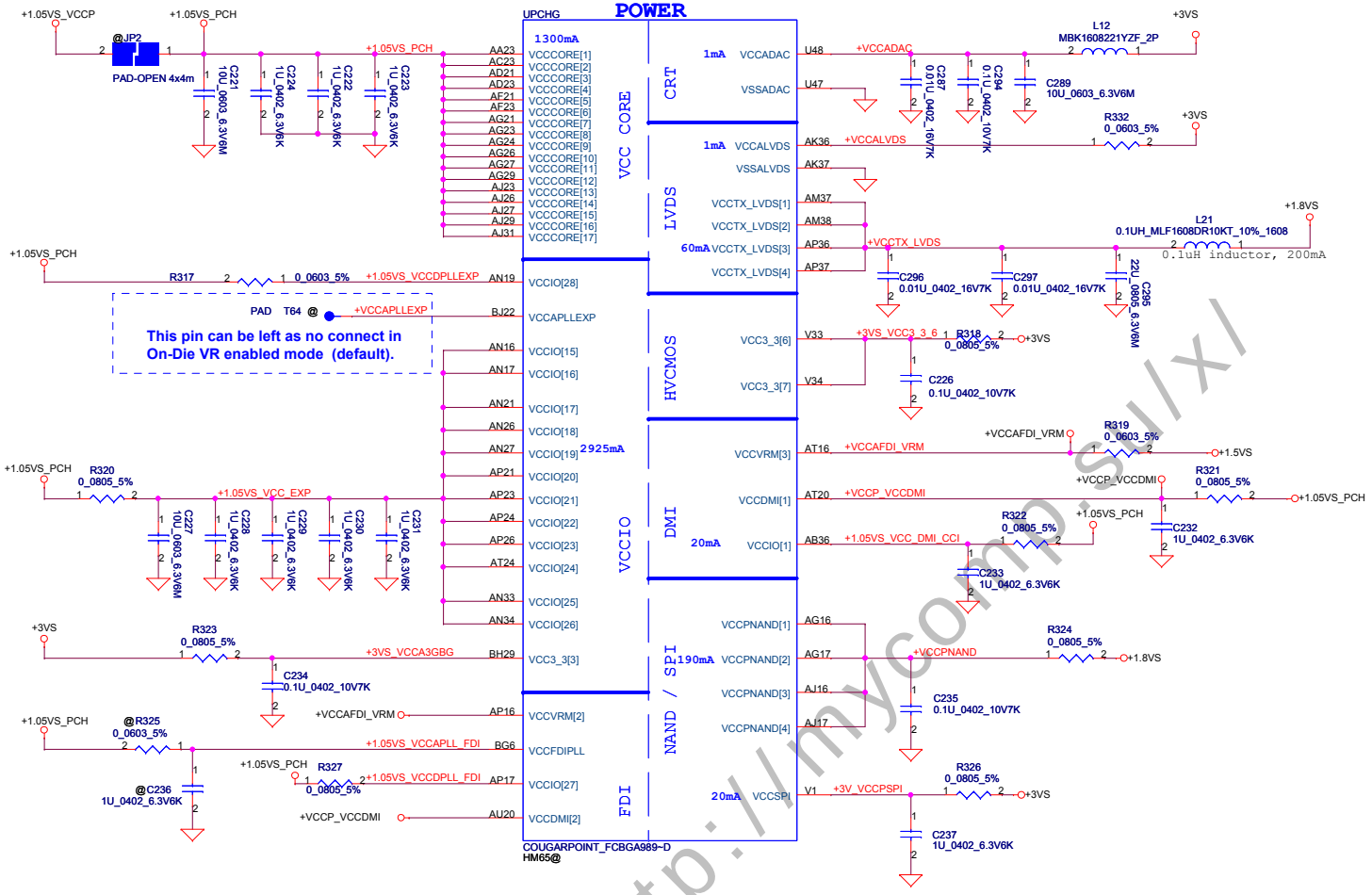
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(6/9)-CPU/GPIO/MISC

Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.1

Date: Friday, January 21, 2011 Sheet 34 of 58



PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(7/9)-PWR1

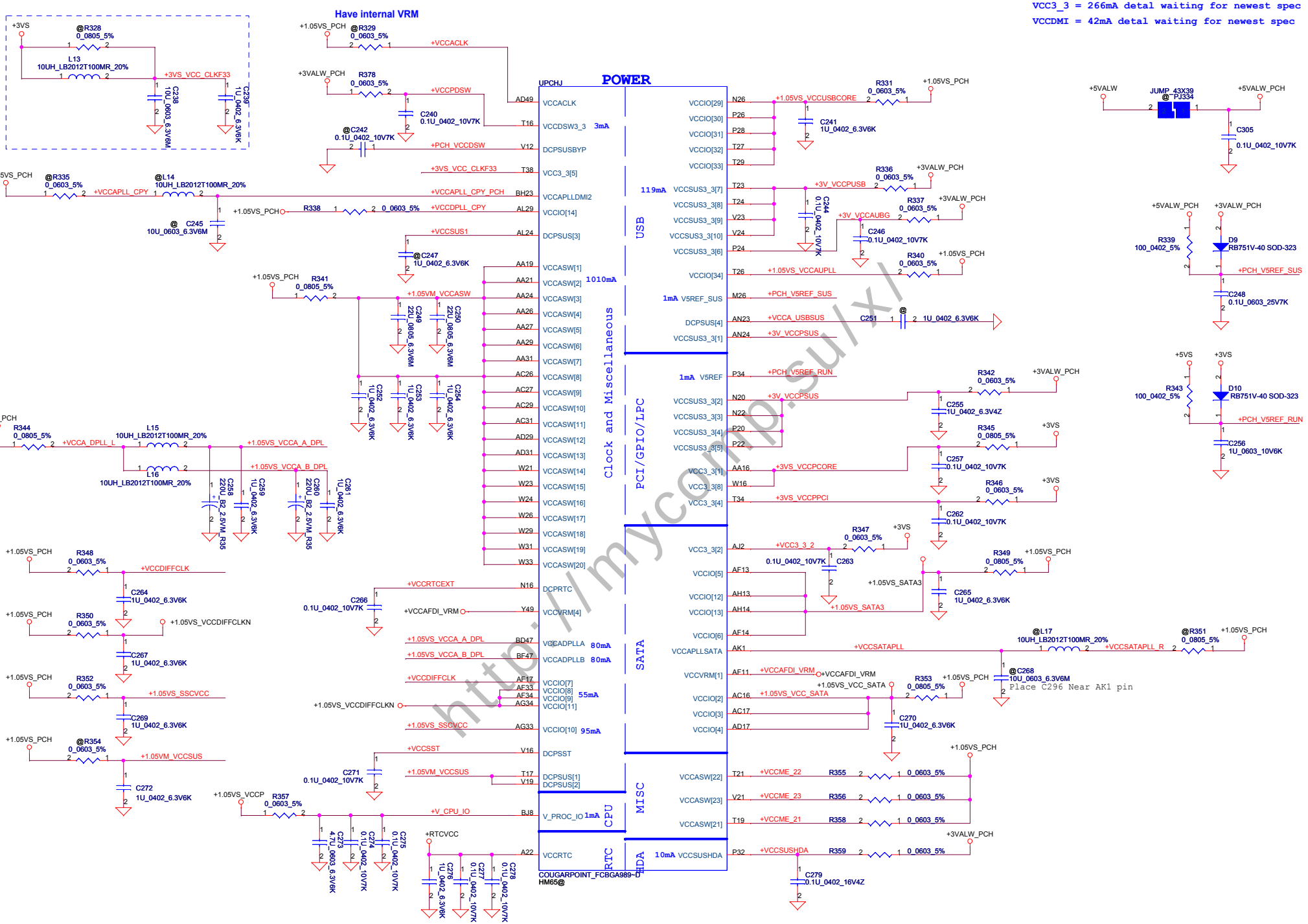
Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 35 of 58

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

Have internal VRM

POWER

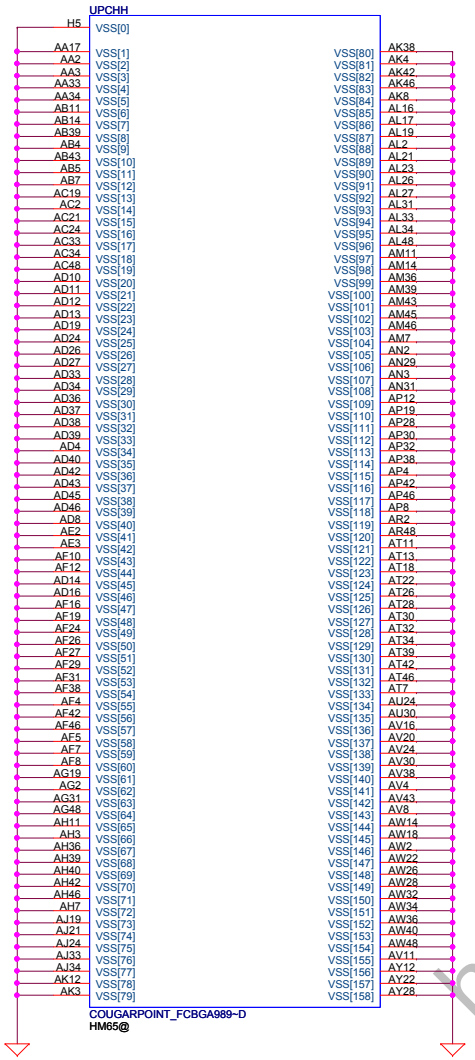


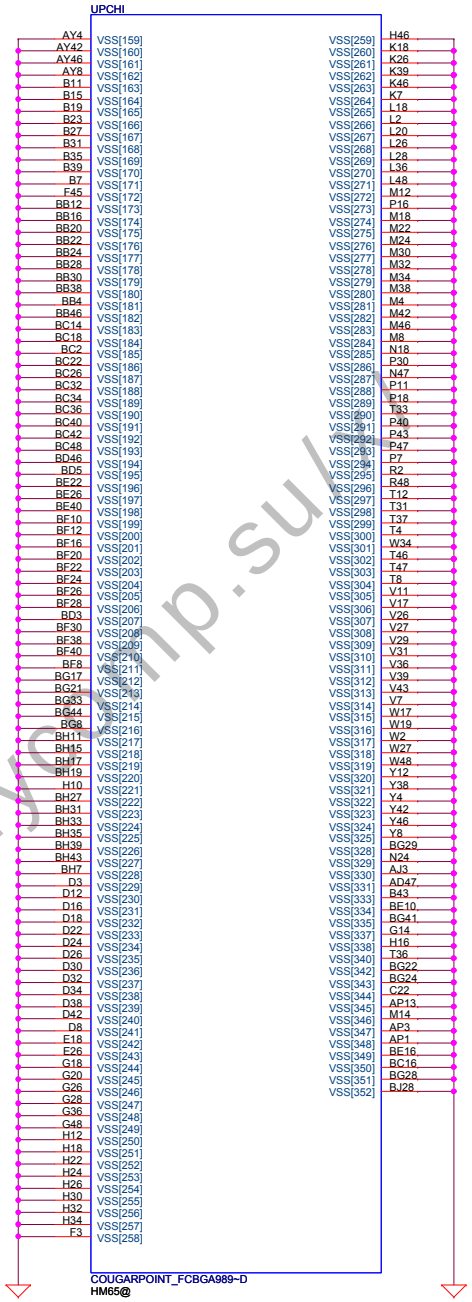
Compal Electronics, Inc.

Title: Cougar Point(8/9)-PWR2

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 36 of 58





Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

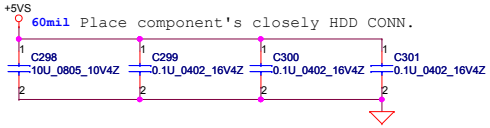
Compal Electronics, Inc.

Title: Cougar Point(9/9)-GND

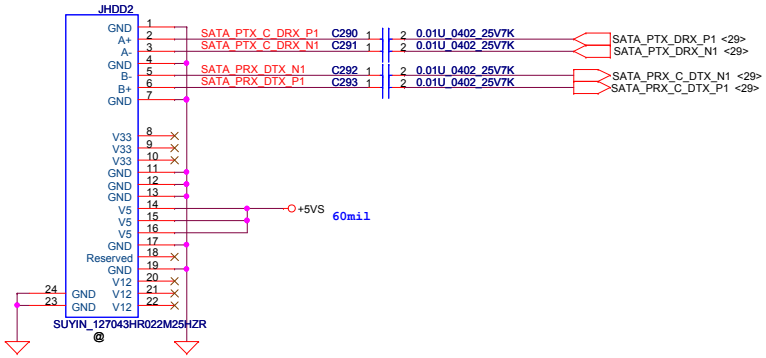
Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 37 of 58

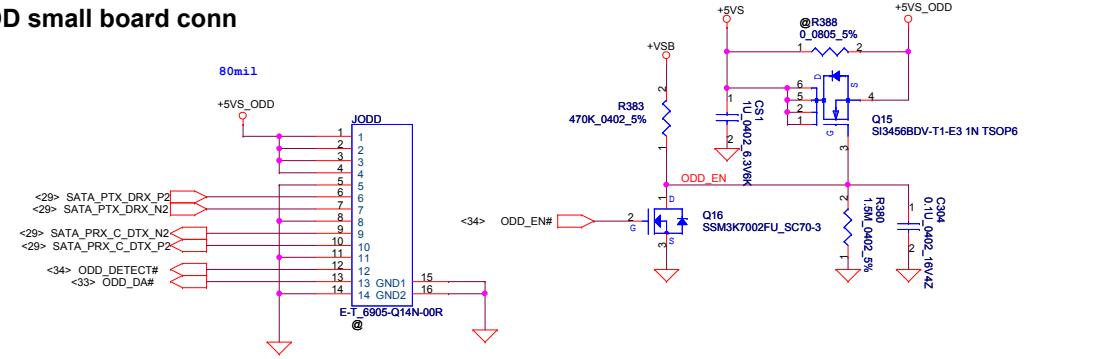
SATA HDD 2.5" Conn.



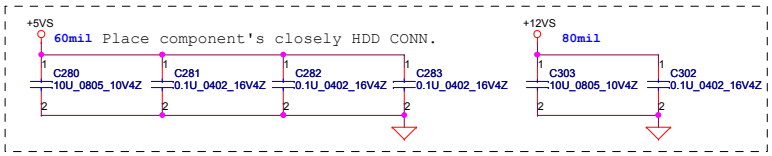
HDD



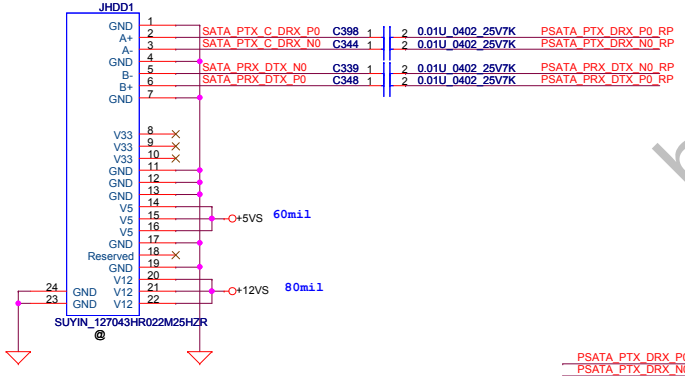
ODD small board conn



SATA HDD 3.5" Conn.

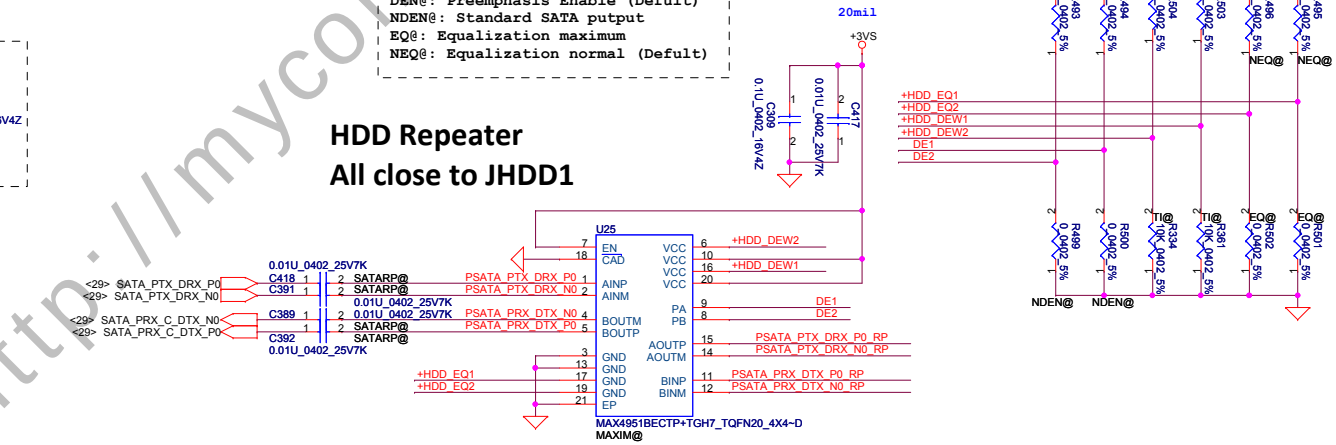


HDD

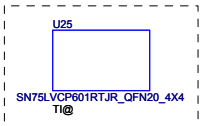


MAXIM@: MAX4951BECTP+TGH7 (Defult)
TI@: SN75LVCP601TJR
DEN@: Preemphasis Enable (Defult)
NDEN@: Standard SATA putput
EQ@: Equalization maximum
NEQ@: Equalization normal (Defult)

HDD Repeater
All close to JHDD1



Note: +HDD_DEW1, +HDD_DEW2, +HDD_EQ1, +HDD_EQ2 need to route 10 mils



PSATA_PTX_DRX_P0_RP — R505 SATA@ 0_0402_5% — SATA_PTX_DRX_P0 <29>
PSATA_PTX_DRX_N0_RP — R506 SATA@ 0_0402_5% — SATA_PTX_DRX_N0 <29>
PSATA_PRX_DTX_N0_RP — R507 SATA@ 0_0402_5% — SATA_PRX_C_DTX_N0 <29>
PSATA_PRX_DTX_P0_RP — R508 SATA@ 0_0402_5% — SATA_PRX_C_DTX_P0 <29>

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

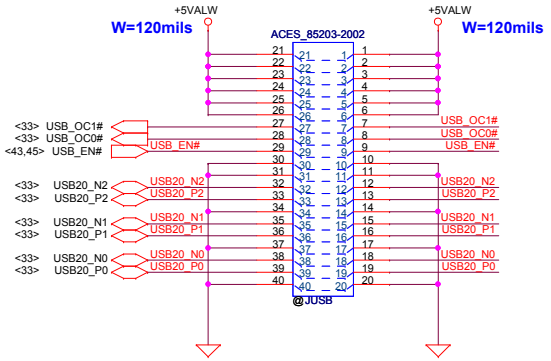
Compal Electronics, Inc.

Title: SATA-HDD&ODD/B

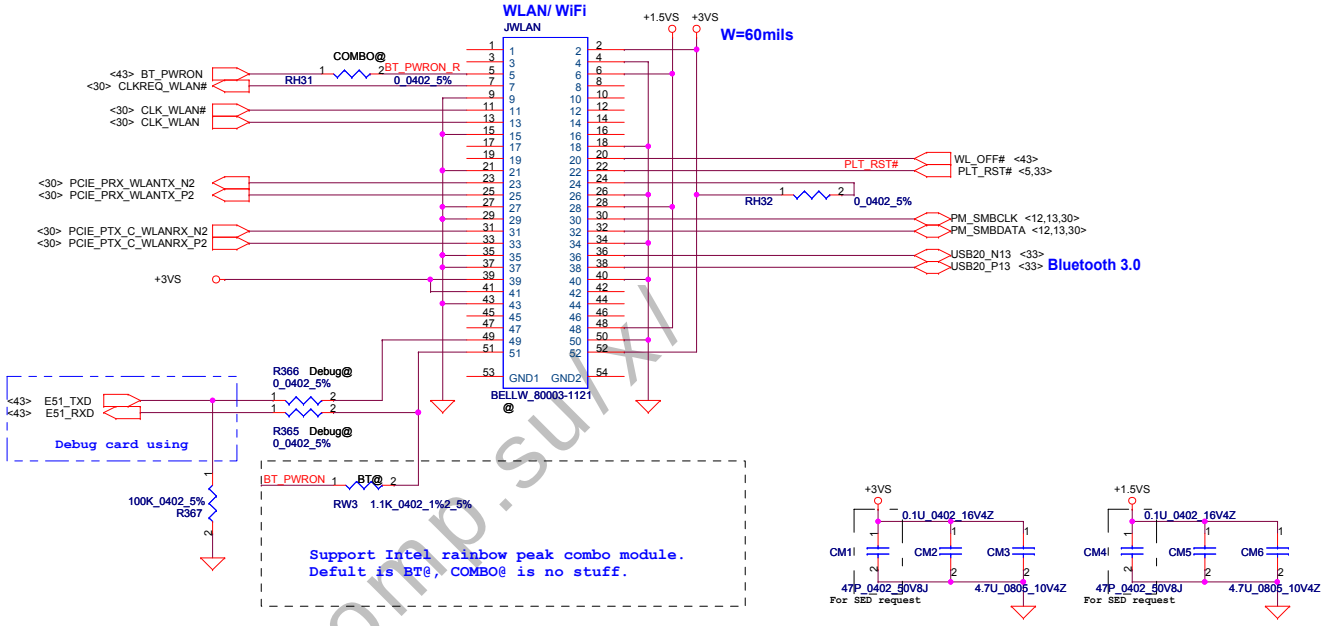
Size	Document Number	Rev
	PBL80 LA-7441P M/B	0.1

Date: Friday, January 21, 2011 Sheet 38 of 58

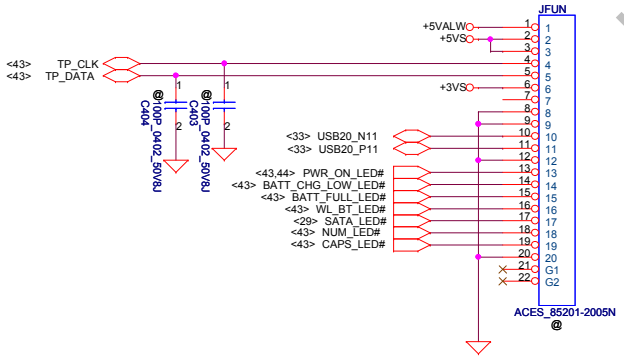
USB/B
Right USB X 3



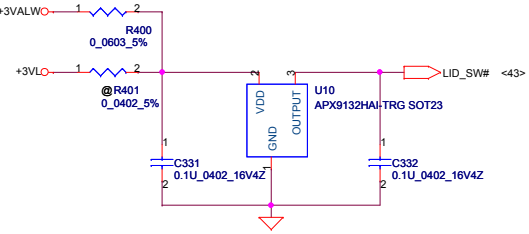
Slot 1 Half PCIe Mini Card-WLAN & BT3.0



Touch pad & LID &
Card Reader & LED small board Connector

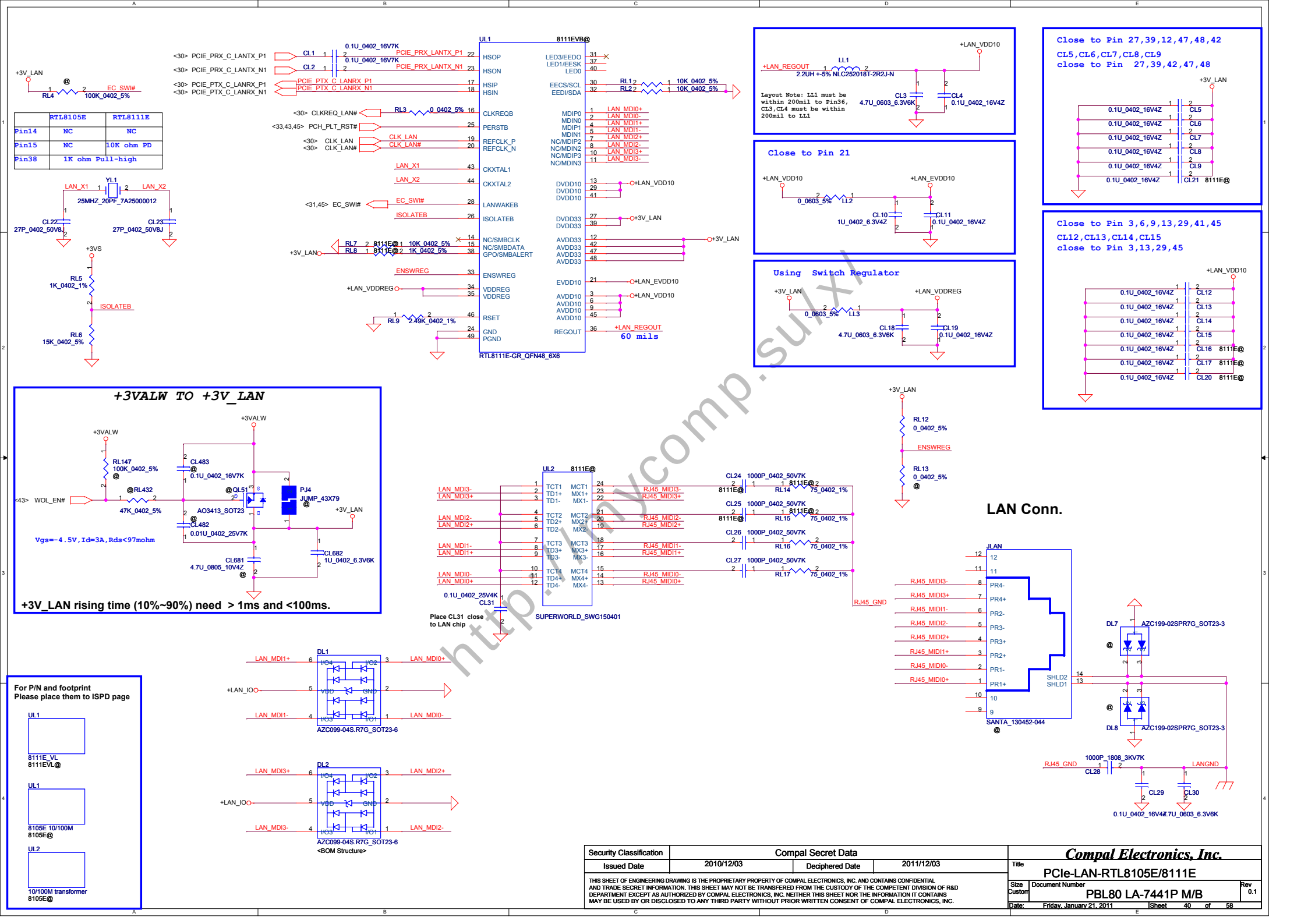


Lid SW



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.			
Title	USB/B&TP/LED/CR/B&LID&PCIe-WLAN		
Size	Document Number		Rev
	PBL80 LA-7441P M/B		0.1
Date: Friday, January 21, 2011		Sheet 39 of 58	



BIOS Bus switch

SPI ROM For Basic ME ROM size 4MByte

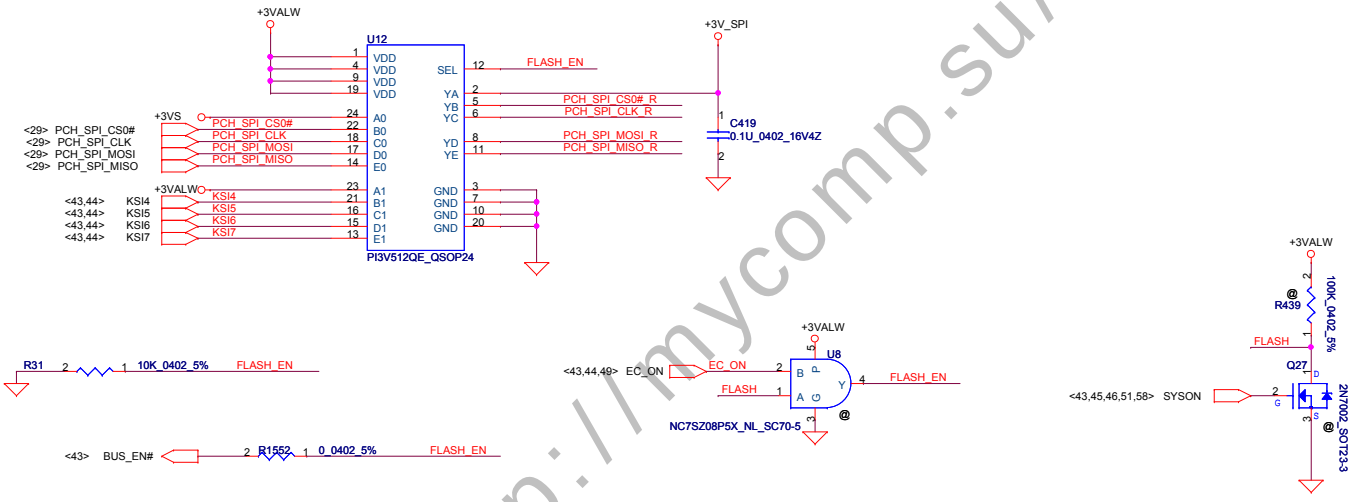
1. When Flash EC ROM.
   KSO2 to Low (Test mode)
   KSO3 to Low (ISP mode)---------FDA mode
   EC_ON->Low, BUS_EN#->Low
   U11 : Y->A0, PCH to BIOS ROM.
   KSI4,5,6,7 direct to EC_SPI

2. When Flash BIOS ROM.
   KSO2 to High
   KSO3 to Low (ISP mode)
   EC_ON->High, BUS_EN#->High.
   U11 : Y->A1, KSI4,5,6,7 to BIOS ROM.
   +3V_SPI from +3VALW
   Set EC pin KSI4,5,6,7 to HiZ.

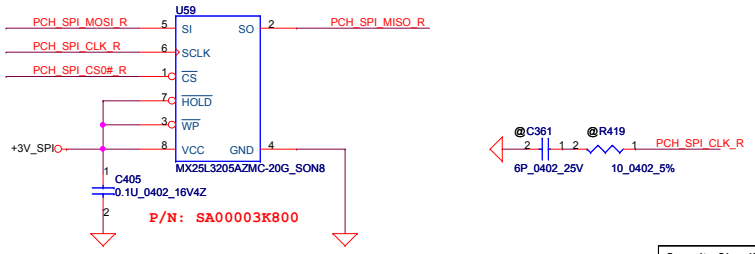
3.When normal operation.
   EC_ON->High , BUS_EN#->Low.
   U11 : Y->A0, PCH direct to BIOS ROM.
   +3V_SPI from +3VS.

4. When enter S3,4
   EC_ON->High, BUS_EN#->Low.
   U11 : Y->A1, PCH direct to BIOS ROM.
   But +3V_SPI from +3VS is no power.

** BUS_EN# only high when test mode.
   And must make sure it's low when FDA mode.
   Or HW use 10K pull down to GND.



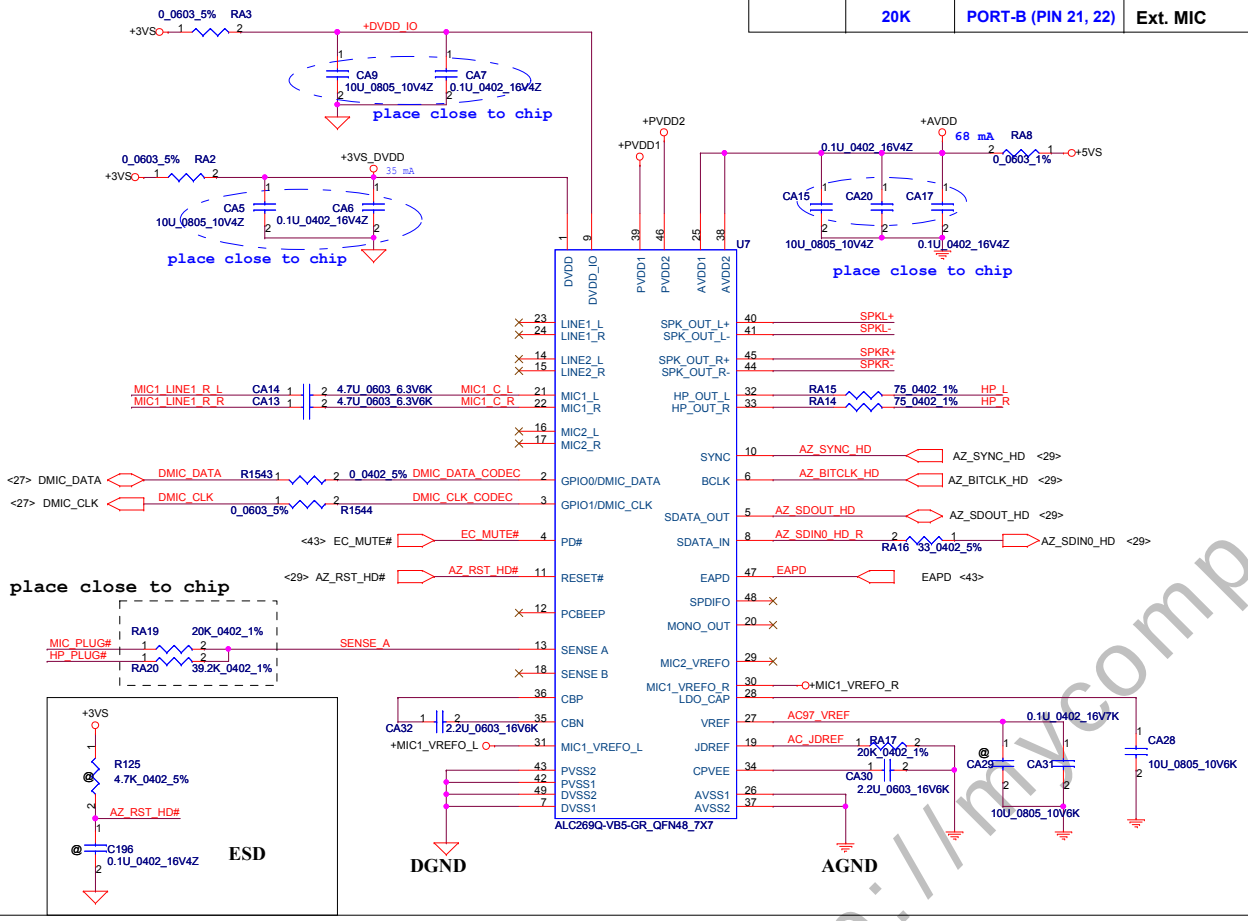
BIOS SPI Flash (4MByte*1)

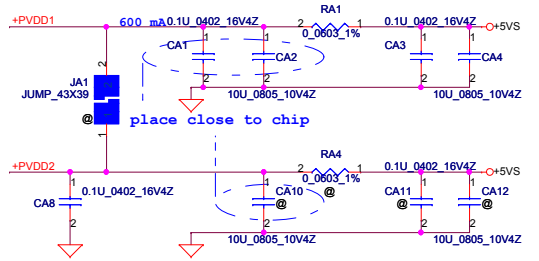


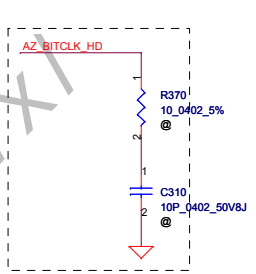
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

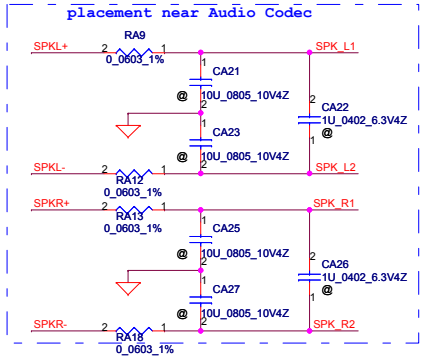
Compal Electronics, Inc.		
Title: Bus switch&BIOSROM		
Size	Document Number: PBL80 LA-7441P M/B	Rev: 0.1
Date: Friday, January 21, 2011	Sheet 41 of 58	

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC

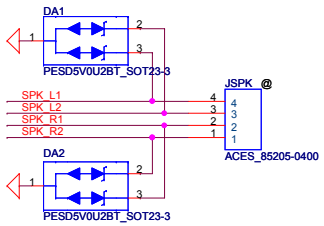


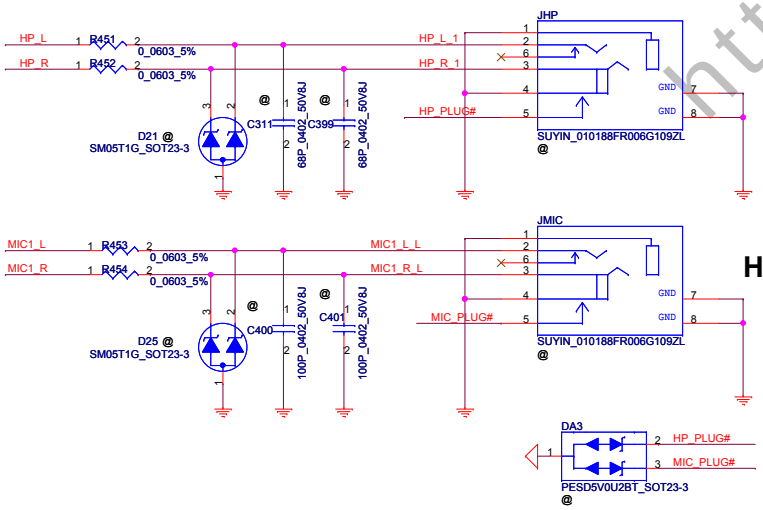




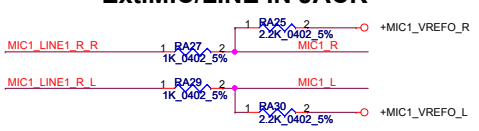


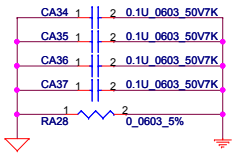
SPEAKER CONN





Ext.MIC/LINE IN JACK





Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

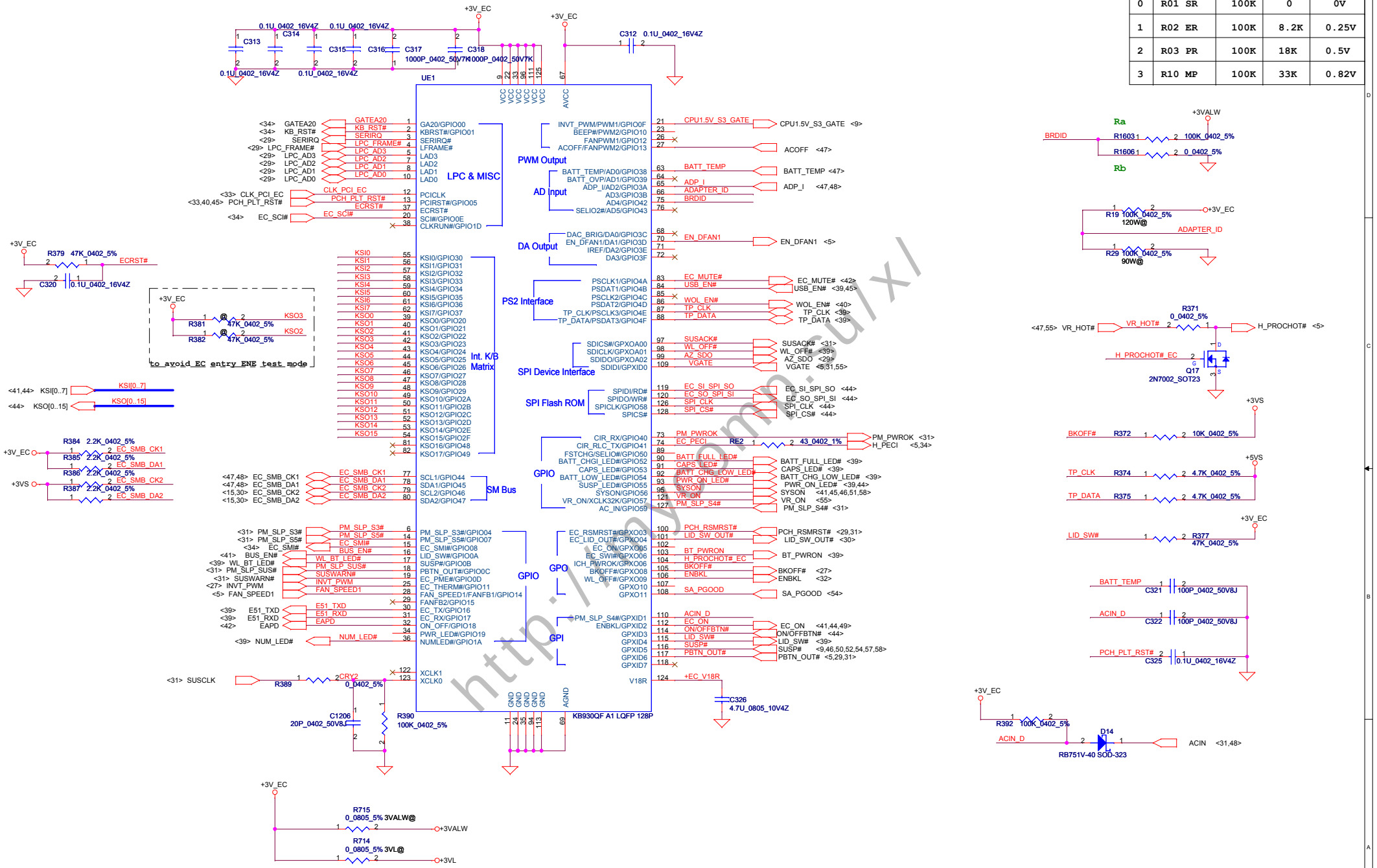
Compal Electronics, Inc.

Title: HD CODEC ALC269

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 42 of 58

ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R03 PR	100K	18K	0.5V
3	R10 MP	100K	33K	0.82V



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

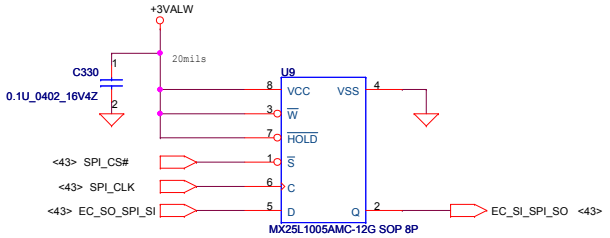
Compal Electronics, Inc.

Title: ENE-KB930

Size: | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

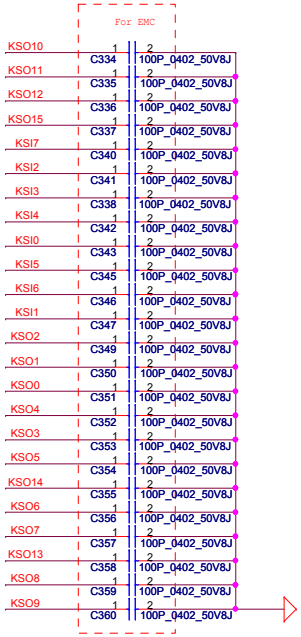
Date: Friday, January 21, 2011 | Sheet 43 of 58

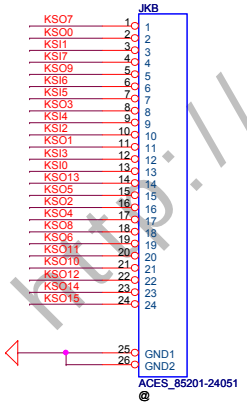
SPI Flash (1MByte*1)



P/N :SA00003GK00 & SA00003GM10

KEYBOARD CONN.

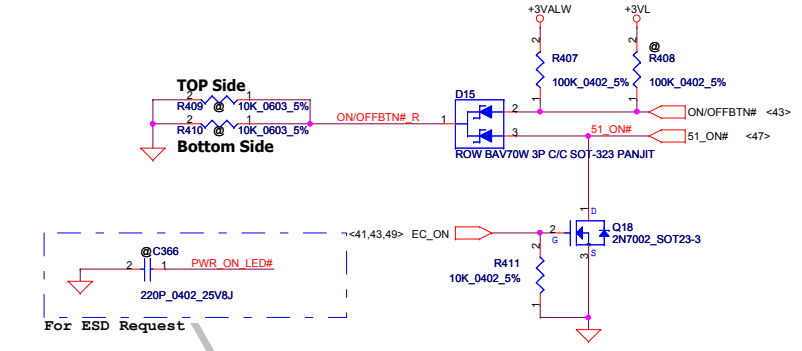


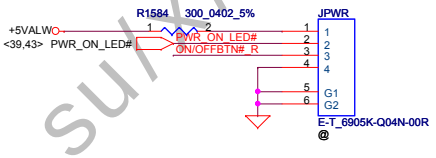


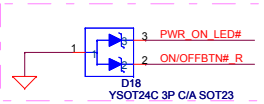
KSI[0..7] KSI[0..7] <41,43>

KSO[0..15] KSO[0..15] <43>

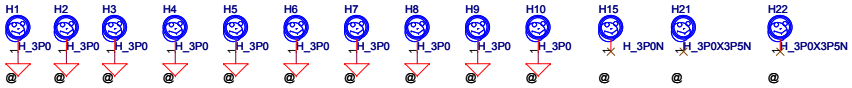
Power Button/ PWR/B



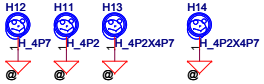




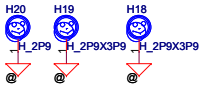
Screw Hole



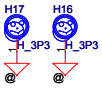
CPU

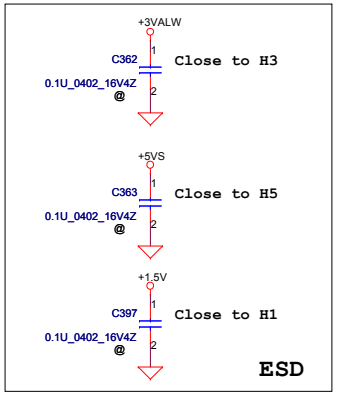


VGA



WLAN

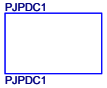




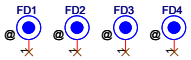
ISPD

PCB

DC-IN



PCB Fedical Mark PAD



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: ECROM/KB/PWR/B/SCREW

Size	Document Number	Rev
	PBL80 LA-7441P M/B	0.1

Date: Friday, January 21, 2011 Sheet 44 of 58

+1.5V to +1.05V Transfer

Vout=0.8*(1+10K/32.4K)
1.042 ~ 1.0469 ~ 1.0519V
Spec: 0.9975 ~ 1.05 ~ 1.1025

+3VALW to +3V Transfer

+3V & +1.05V has power sequence timing:
0.1*VDD(+3V) ~ 0.9*VDD(+1.05V) < 100ms

Close to U102.D7

Close to U102.P13

Follow Vendor recommend.

+3V:200mA
+1.05V:800mA

2.5A

W=80mils

35mA

must to close to JUSB30

CSEL=0 : 24MHz XTAL
CSEL=1 : 48MHz Clock

Place as close as possibile to
UU2.N14 and UU2.M14

UPD720200A:
SMIB Low active

For UPD720200:
SMI high active

2010/09/17 Add Level shift to avoid +3V leakage from +3VALW_PCH

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

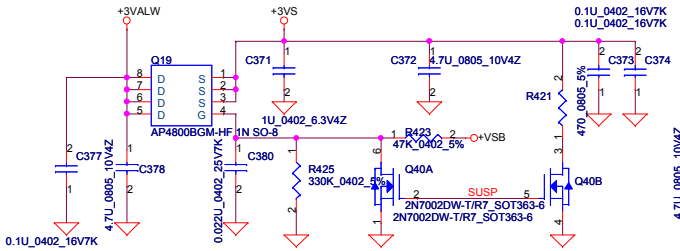
Title: PCIe-USB3.0

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

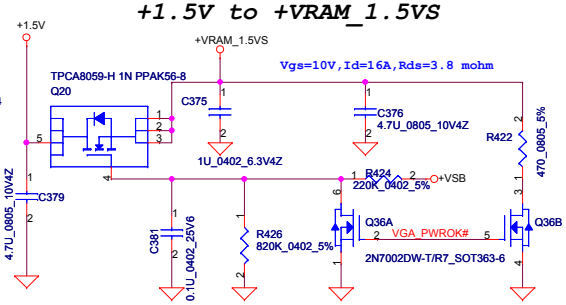
Date: Friday, January 21, 2011 | Sheet 45 of 58

+3VALW TO +3VS

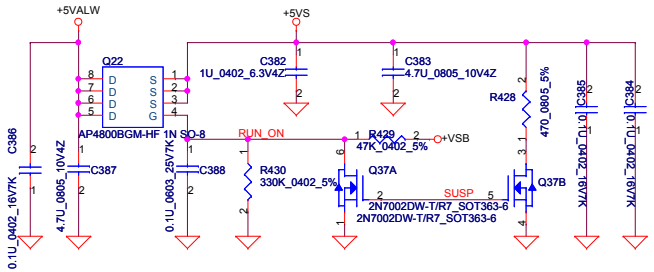
Vgs=-0V,Id=9A,Rds=18.5mohm



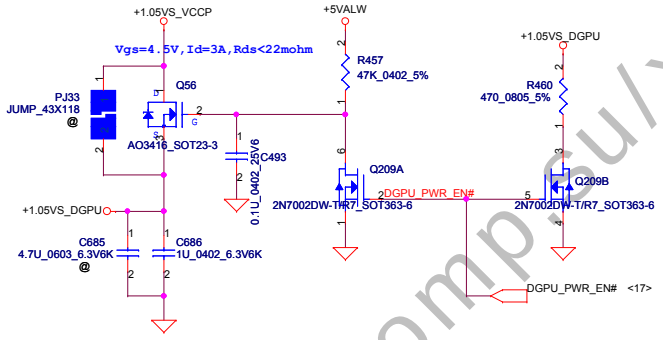
+1.5V to +VRAM_1.5VS



+5VALW TO +5VS

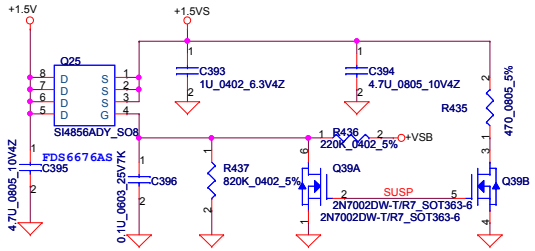


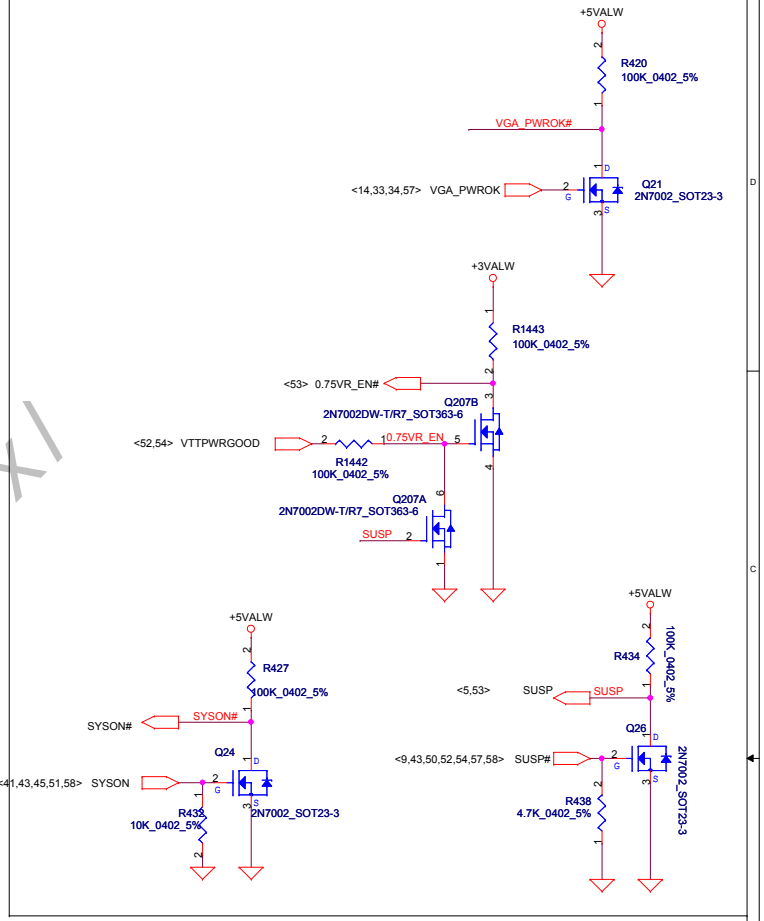
+1.05VS_VCCP to +1.05VS_DGPU



+1.5V to +1.5VS

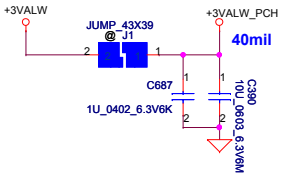
Vgs=10V,Id=14.5A,Rds=6mohm

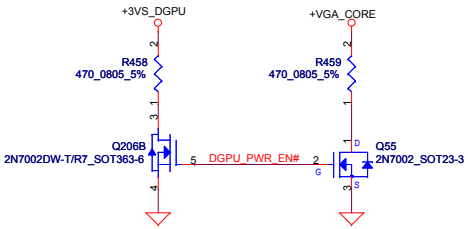


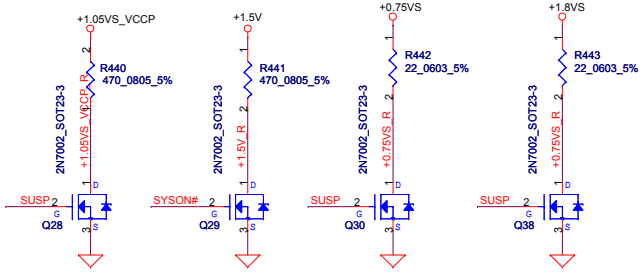


+3VALW TO +3VALW(PCH AUX Power)

Short J1 for PCH VCCSUS3.3







Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 46 of 58

DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME

need confirm: ME give us battery connector P/N is DC040000800

PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

If EC use 3VL and can not detect VGATE, must connect EN0

Reserve when EC use +3VL.
Install when EC use +3VALW.

(120mA,40mils ,Via NO.= 1)

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **DCIN / BATT CONN / OTP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

Date: Friday, January 21, 2011 Sheet 47 of 58

for reverse input protection

PQ106 SI1304BDL-T1-E3_SC70-3
PR103 1M_0402_5%
PR104 3M_0402_5%

VIN
AO4466L_SO8 PQ101
P1
PR105 0_0402_5%
PC110 0.1U_0402_25V6
PC112 2200P_0402_50V7K
BQ24725_ACDRV
AO4466L_SO8 PQ102
P2
0.02_2512_1% PR101
PC113 0.1U_0402_25V6
PC115 0.1U_0402_25V6
PR108 4.12K_0603_1%
PR109 4.12K_0603_1%
B+
@HCB2012KF-121T50_0805 PL103
PL102 0.56UH_1127AS-R56N_3.3A_30%
PC111 10U_0805_25V6K
PC105 10U_0805_25V6K
PC104 10U_0805_25V6K
PC103 10U_0805_25V6K
PC102 @0.1U_0402_25V6
PC101 2200P_0402_50V7K
PD101 BAS40CW_SOT323-3
CHG_B+
AO4466L_SO8 PQ103
PC114 0.01U_0402_50V7K
PR106 @0_0402_5%
BQ24725_BATDRV
PR107 4.12K_0603_1%

VIN
PR112 @3.3_1210_5%
PR113 @3.3_1210_5%
PC120 @2.2U_0805_25V6K

PC117 0.1U_0603_25V7K
BQ24725_ACP
BQ24725_ACN
PC116 0.047U_0402_25V7K
PR110 10_1206_1%
PR111 10_0603_5%
PD102 RB751V-40_SOD323-2
PC118 1U_0603_25V6K
PC119 1U_0603_25V6K
BQ24725_VCC
BQ24725_LX
DH_CHG
BQ24725_BST
BQ24725_REGN

PQ104 AON7408L_DFN8-5
PQ105 AO4468L_SO8
PL101 4.7U_LF919AS-4R7M-P3_5.2A_20%
PR102 0.01_1206_1%
PR114 @4.7_1206_5%
PC123 @680P_0402_50V7K
PC124 2.2U_0603_16V6K
PC121 0.1U_0402_25V6
PC122 0.1U_0402_25V6
PC106 10U_0805_25V6K
PC107 10U_0805_25V6K
PC108 2200P_0402_50V7K
PC109 0.01U_0402_50V7K
BATT+

PU101 BQ24725RGRR_VQFN20_3P5X3P5
PAD VCC PHASE HIDRV BTST REGN
ACN LODRV DL_CHG
ACP GND
CMSRC SRP
ACDRV SRN
ACOK BATDRV
ACDET IOUT SDA SCL ILIM
BQ24725_CMSRC
BQ24725_ACDRV
BQ24725_ACOK
BQ24725_BATDRV
PR115 10_0603_5%
PR116 6.8_0603_5%
SRP1 CSOP1 SRN CSON1

+3VALW
PR117 10K_0402_1%
<31,43> ACIN
PR118 10K_0402_1%
Pre_chg
PD7 RB751V-40_SOD323-2
PR119 316K_0402_1%
BQ24725_ILIM
PR120 255K_0402_1%
PR121 100K_0402_1%
PC125 0.01U_0402_25V7K
PR122 154K_0402_1%
PR123 66.5K_0402_1%
PC126 0.1U_0402_25V6
PC127 100P_0402_50V8J
EC_SMB_CK1 <43,47>
EC_SMB_DA1 <43,47>
ADP_I <43,47>

Vin Dectector		
Min.	Typ	Max.
H-->L	17.23V	
L--> H	17.63V	

ILIM and external DPM
3.97A

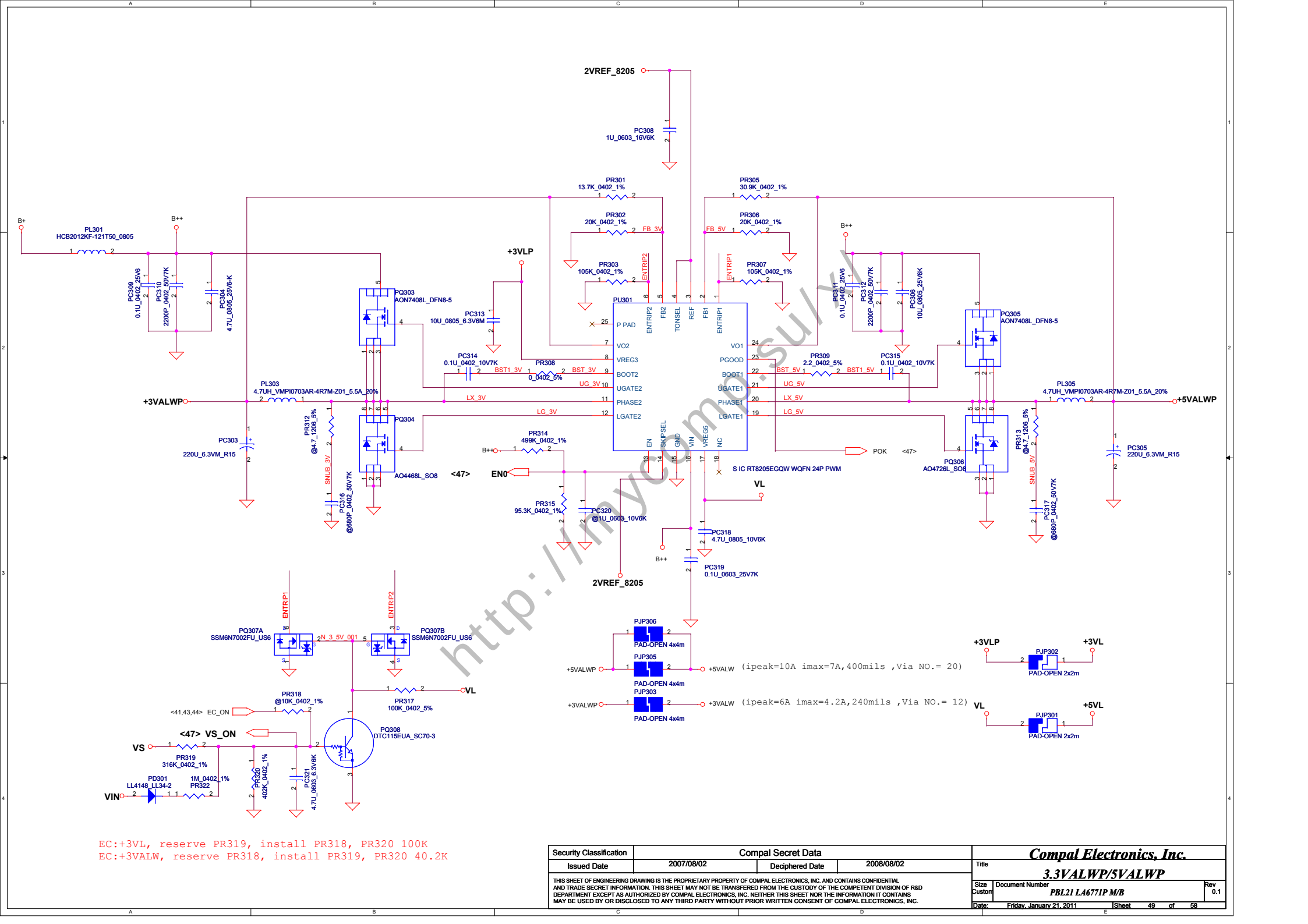
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: LA-7221P | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 48 of 58



EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 40.2K

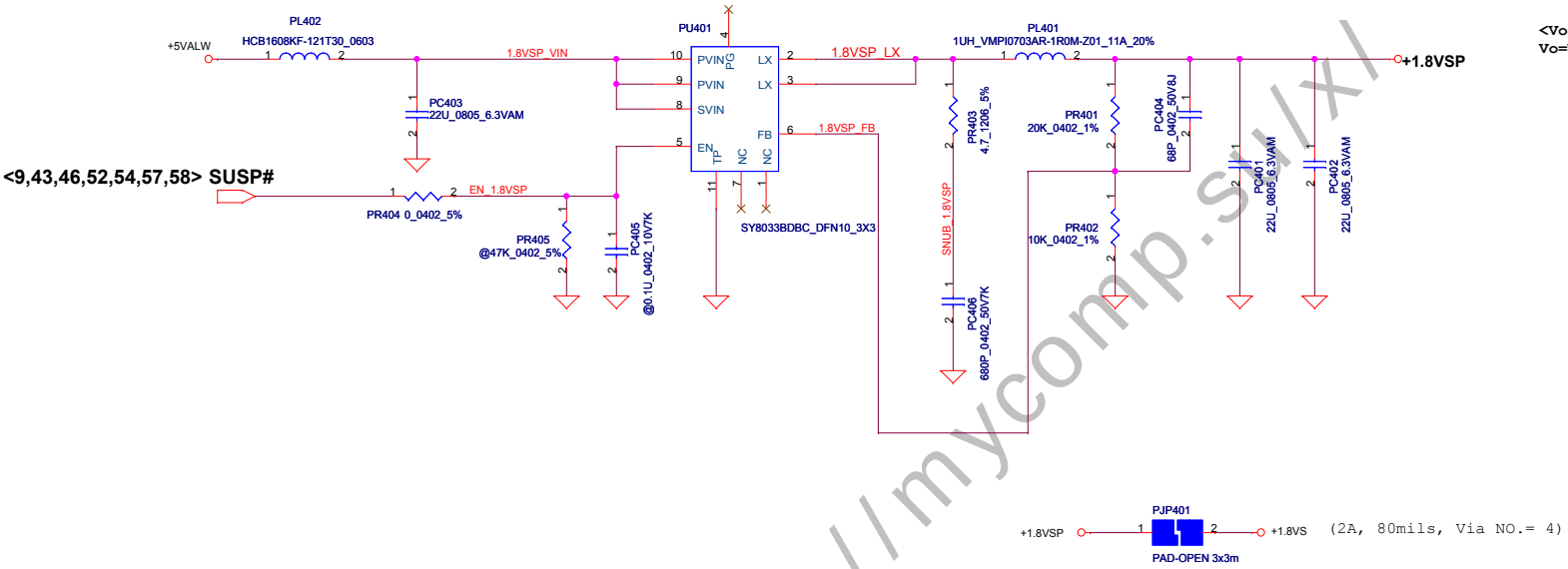
Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

Title: **3.3VALWP/5VALWP**

Size	Document Number	Rev
Custom	PBL21 LA6771P M/B	0.1

Date: Friday, January 21, 2011 Sheet 49 of 58



<Vo=1.8V> VFB=0.6V
Vo=VFB*(1+PR401/PR402)=0.6*(1+20K/10K)=1.8V

(2A, 80mils, Via NO.= 4)

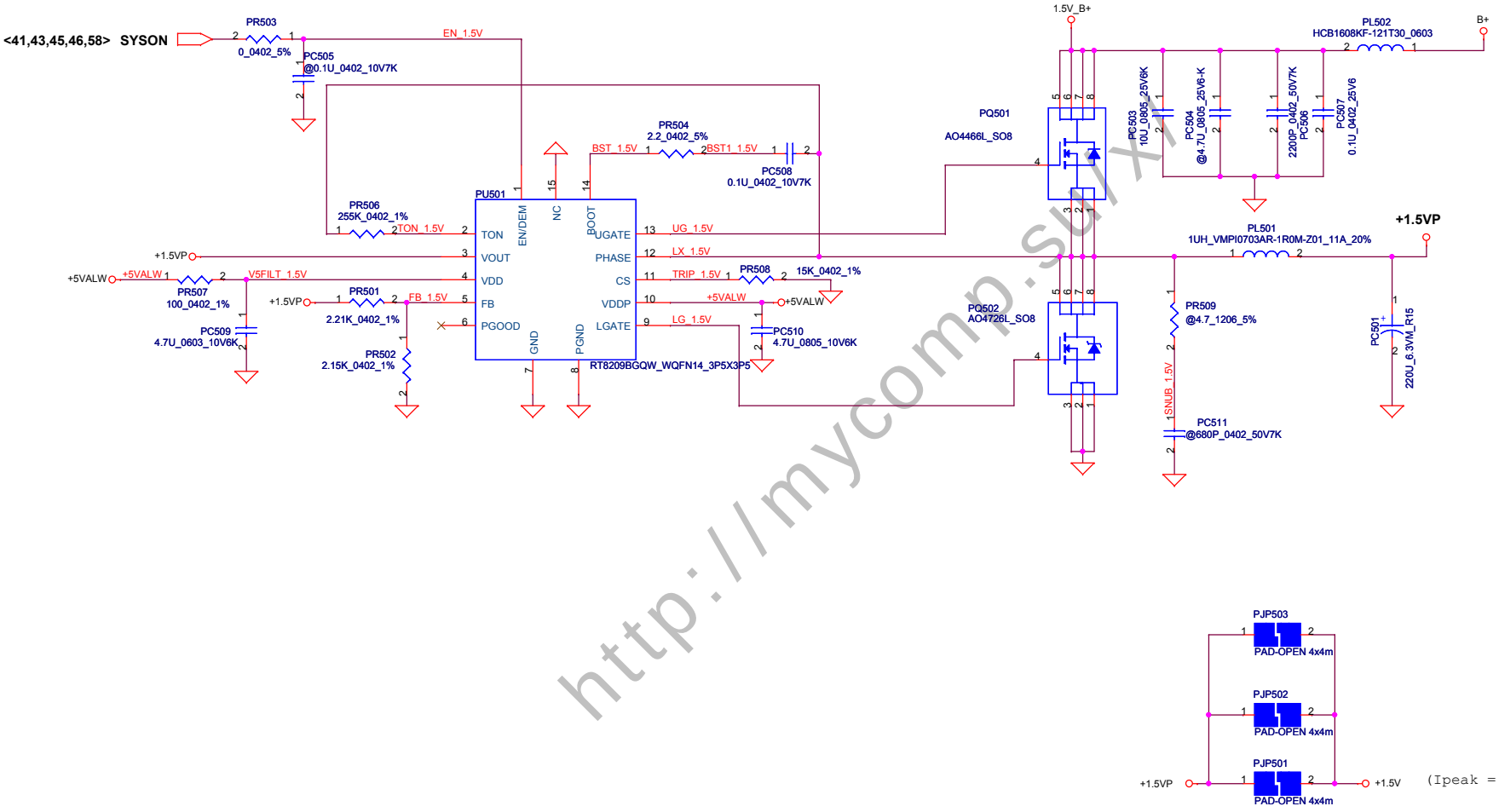
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **+1.8VSP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

Date: Friday, January 21, 2011 | Sheet 50 of 58



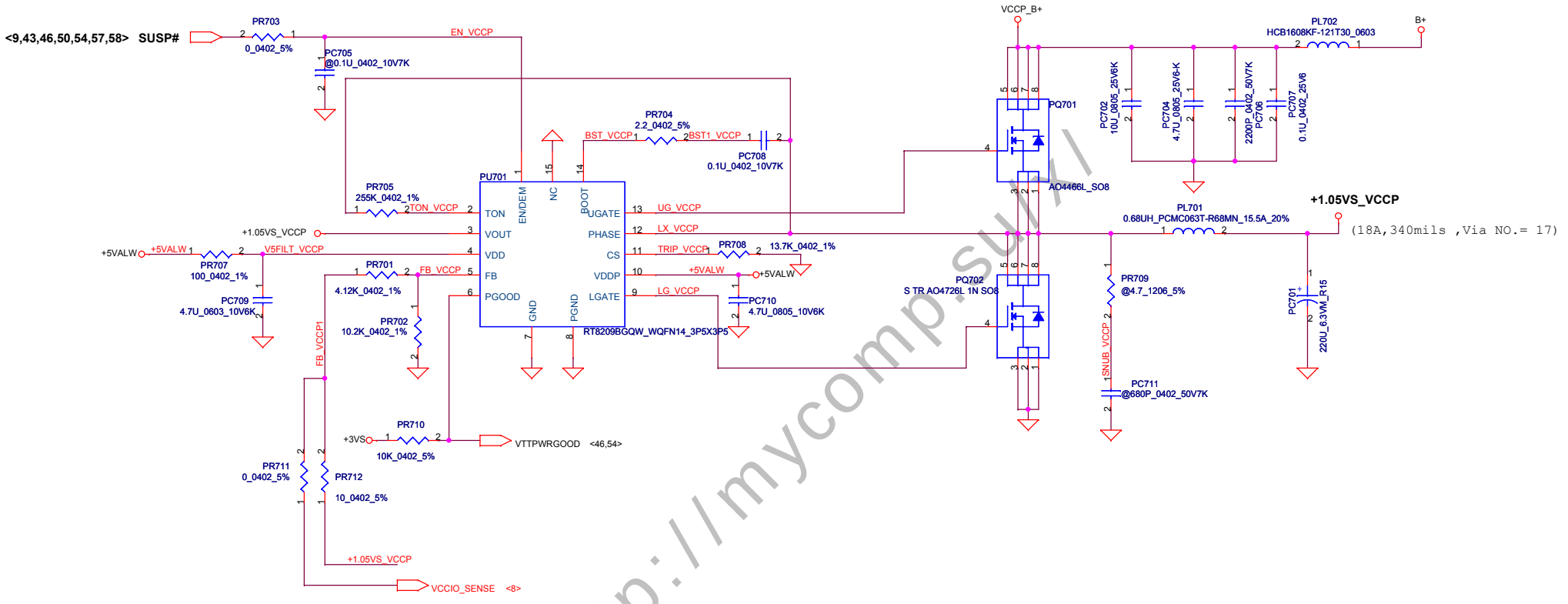
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **+1.5VP**

Size	Document Number	Rev
	PBL21 LA6771P M/B	0.1

Date: Friday, January 21, 2011 | Sheet 51 of 58



VSSIO_SENSE connect to GND directly.

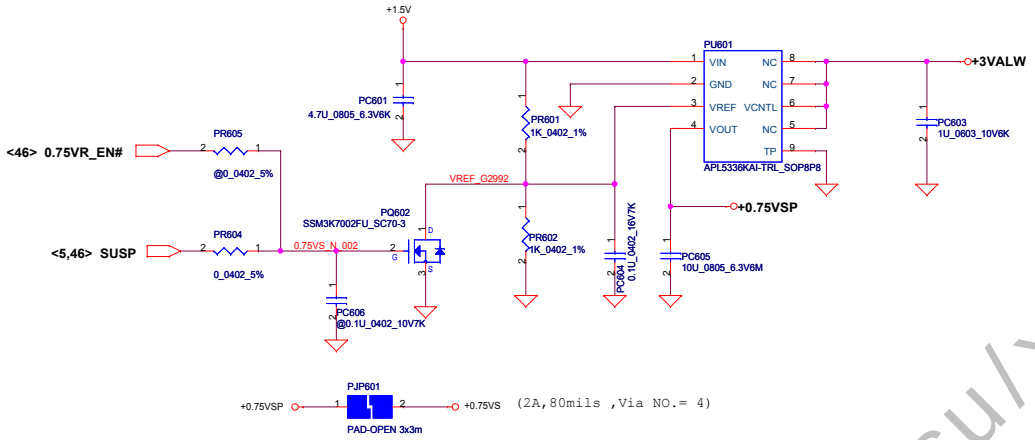
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR+1.05VSP/+VCCPP

Size: Custom | Document Number: PBL21 LA6771P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 52 of 58



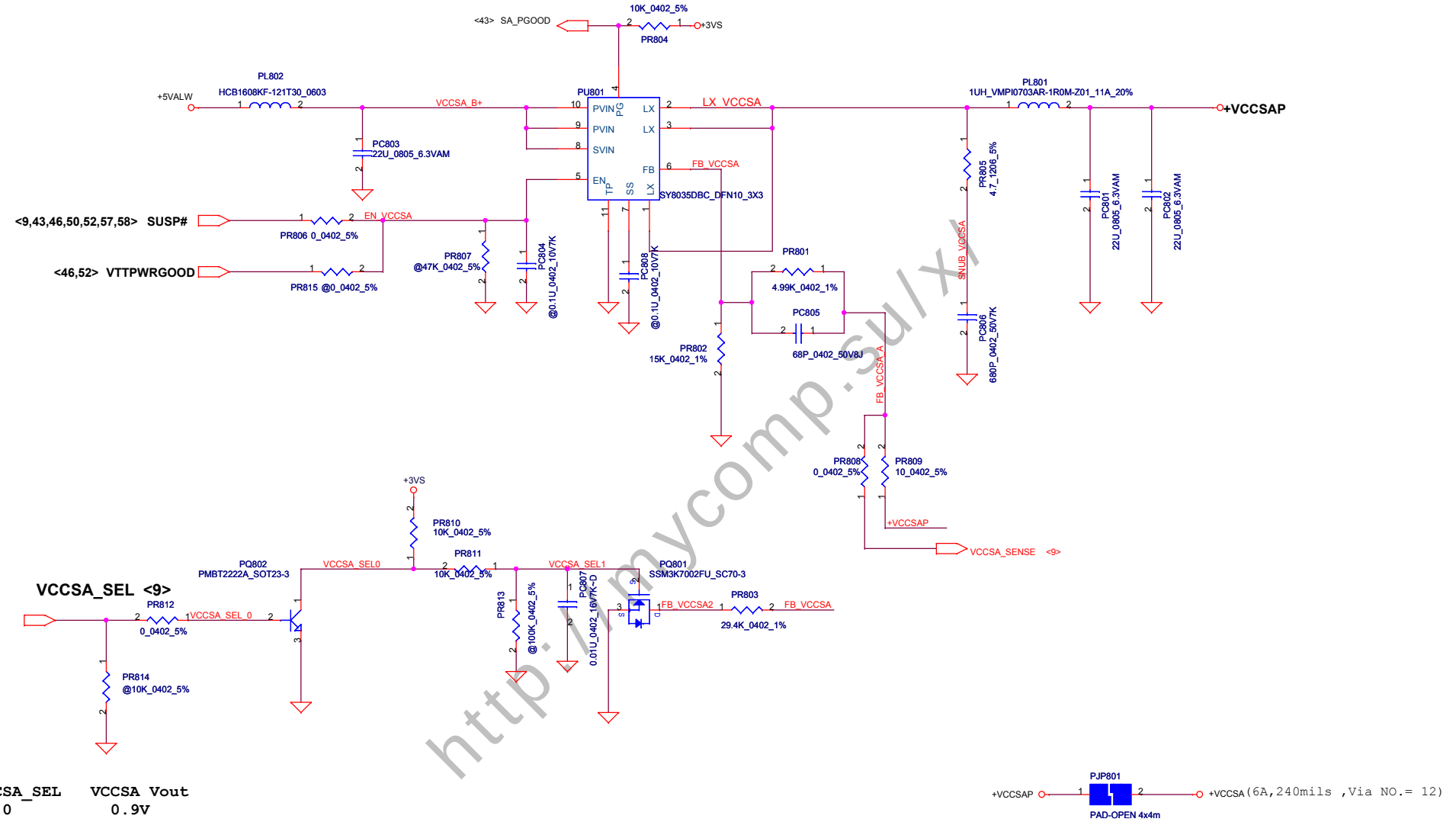
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: 0.75VSP/1.2VSP

Size | Document Number: PBL21 LA6771P M/B | Rev: 0.1

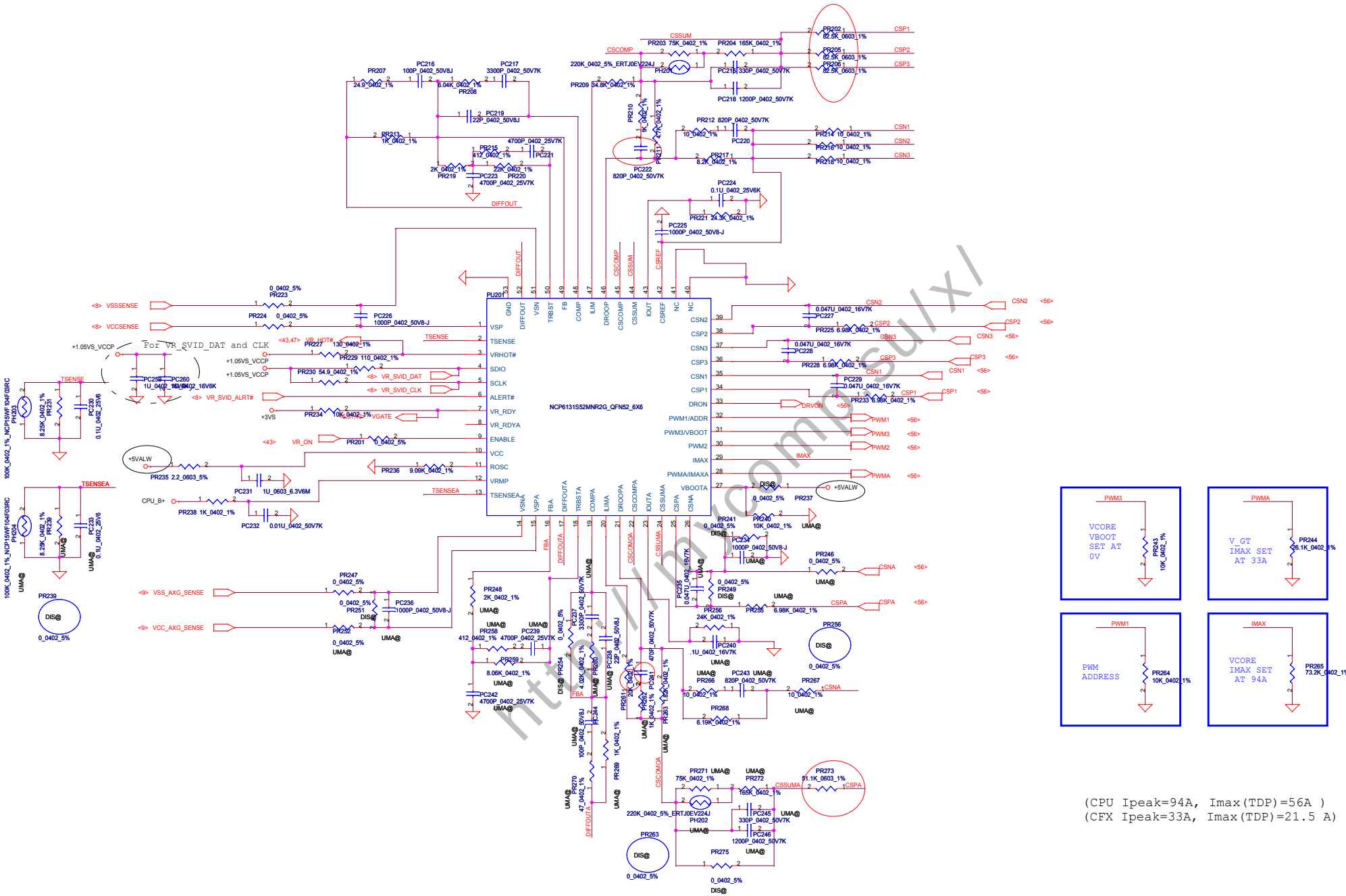
Date: Friday, January 21, 2011 | Sheet 53 of 58



VCCSA_SEL	VCCSA Vout
0	0.9V
1	0.8V

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

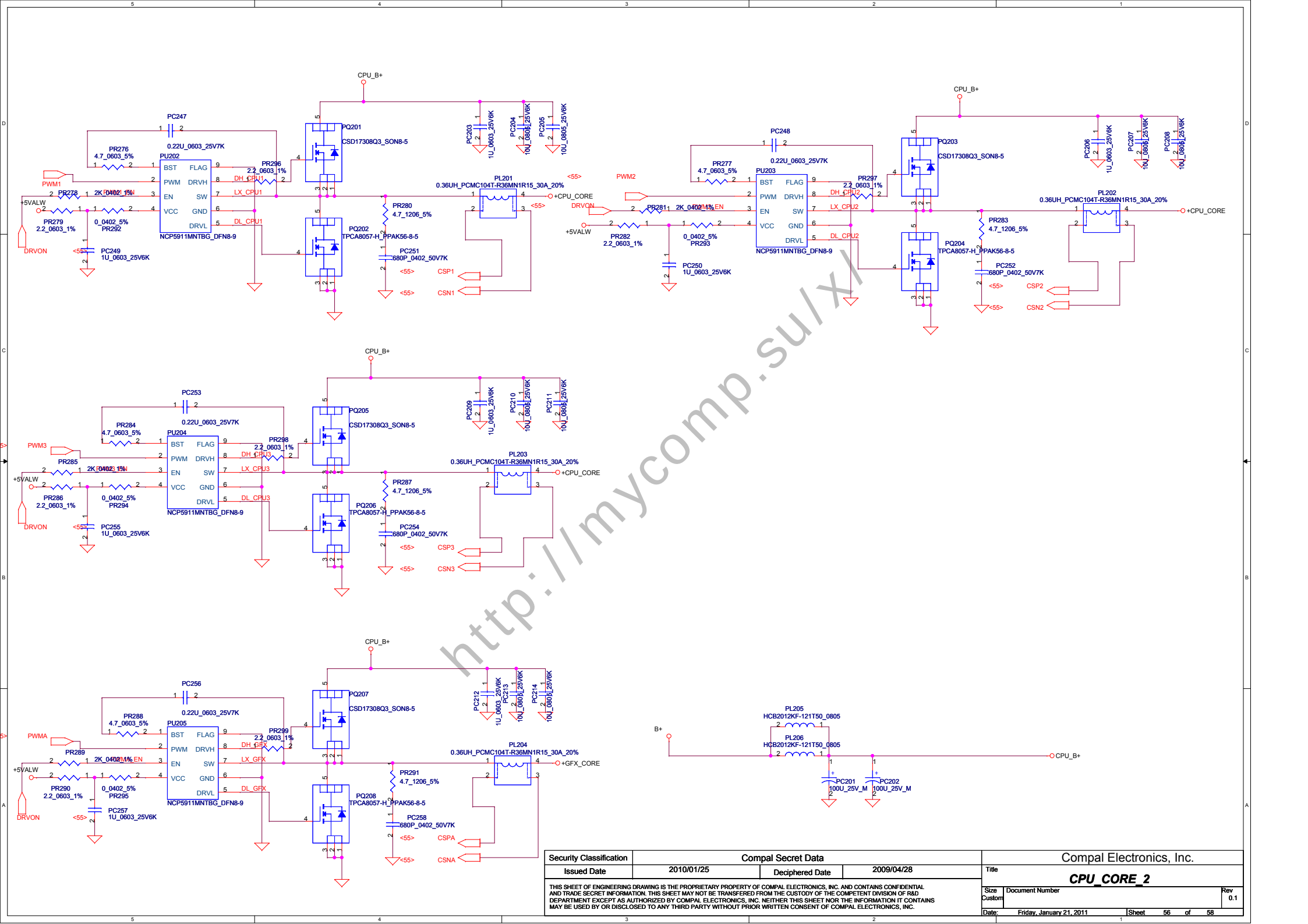
Compal Electronics, Inc.		
Title	PWR+VCCSAP	
Size: Custom	Document Number: PBL21 LA6771P M/B	Rev: 0.1
Date: Friday, January 21, 2011	Sheet 54 of 58	



(CPU Ipeak=94A, Imax(TDP)=56A)
(CFX Ipeak=33A, Imax(TDP)=21.5 A)

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/01/25	Deciphered Date	2009/04/28

Title	CPU_CORE_1		
Size C	Document Number PCA60/70 LA-7001P M/B		Rev 0.1
Date: Friday, January 21, 2011	Sheet 55 of 58		



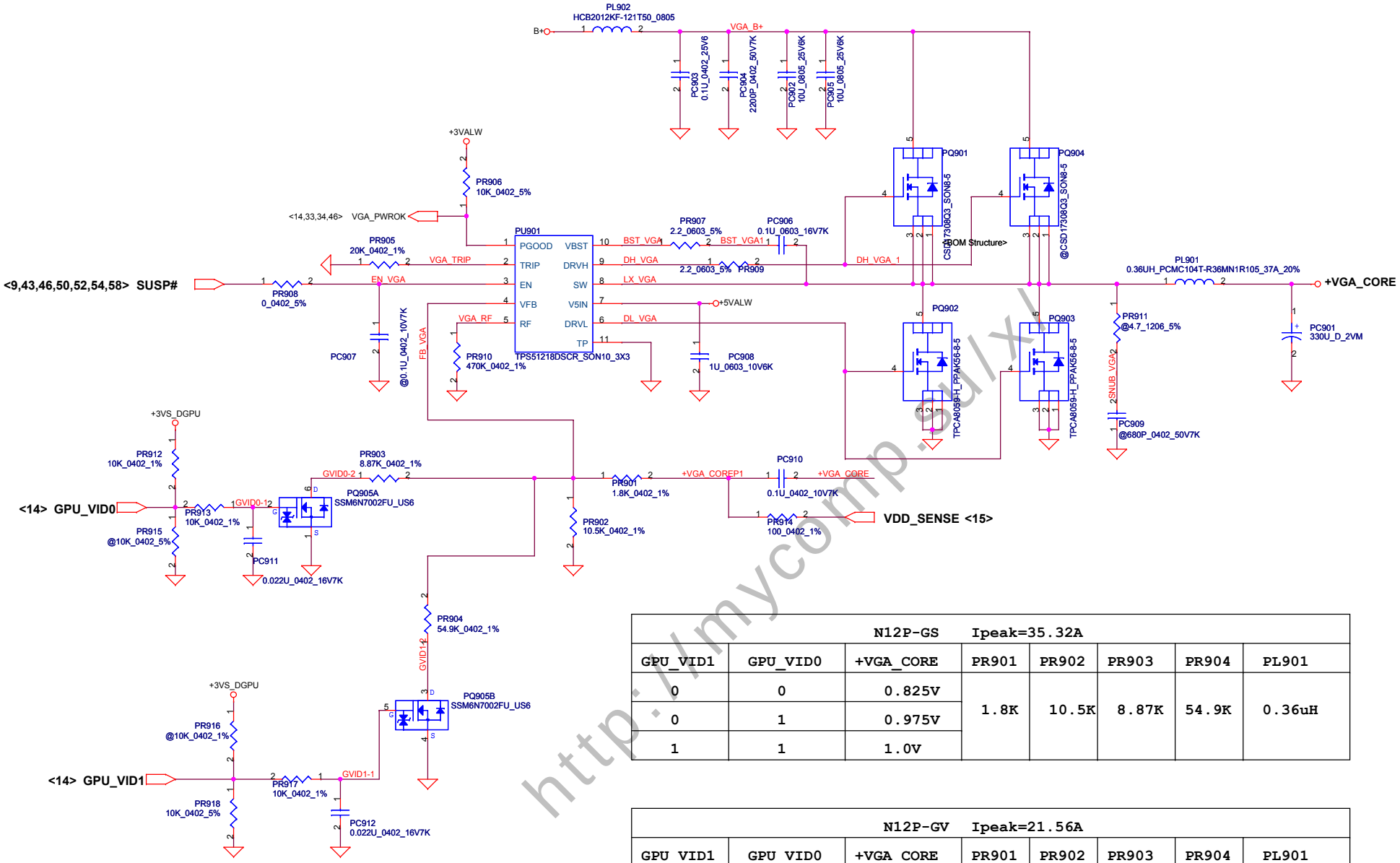
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

Compal Electronics, Inc.

Title: **CPU_CORE_2**

Size	Document Number	Rev
Custom		0.1

Date: Friday, January 21, 2011 | Sheet 56 of 58

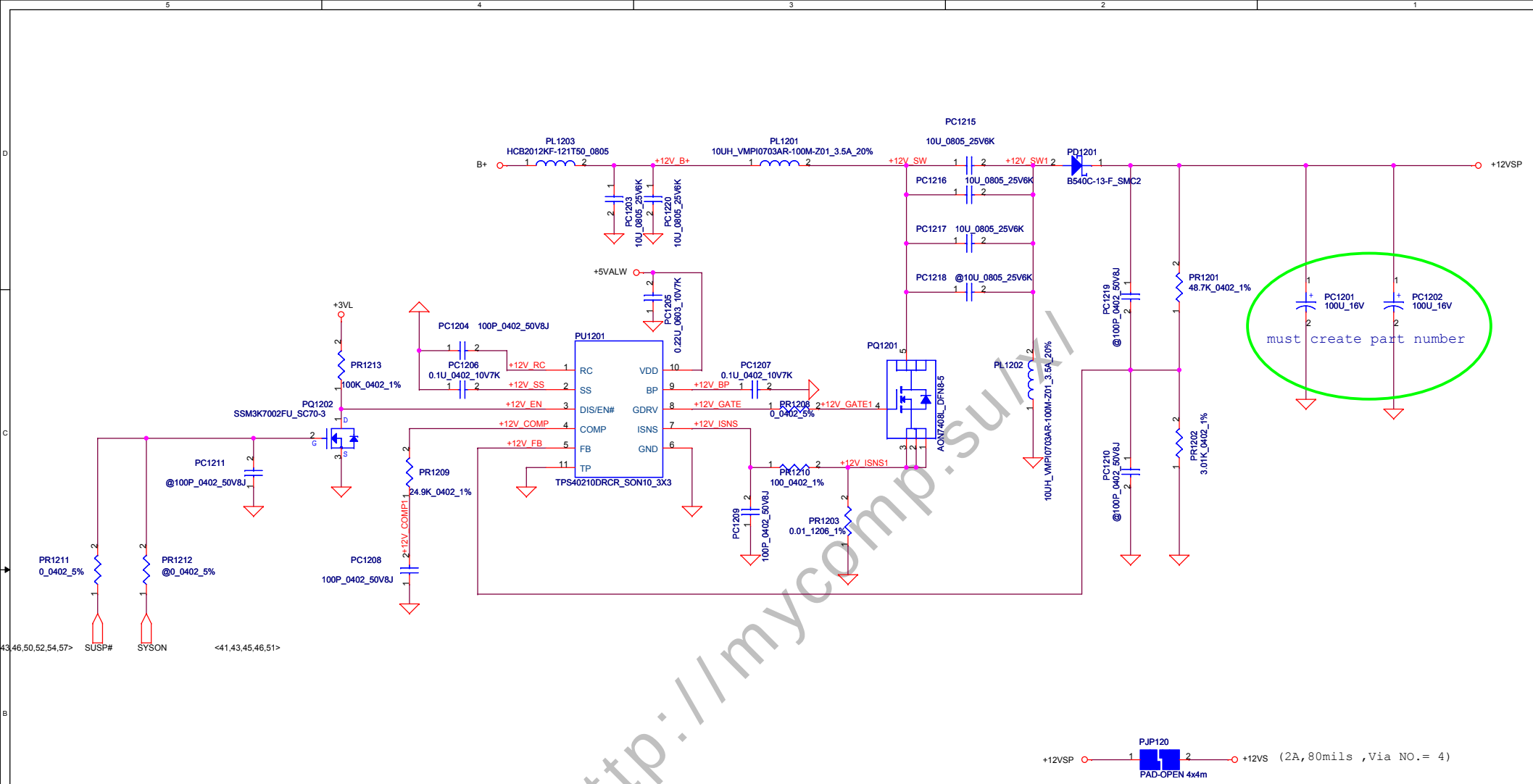


N12P-GS Ipeak=35.32A							
GPU_VID1	GPU_VID0	+VGA_CORE	PR901	PR902	PR903	PR904	PL901
0	0	0.825V	1.8K	10.5K	8.87K	54.9K	0.36uH
0	1	0.975V					
1	1	1.0V					

N12P-GV Ipeak=21.56A							
GPU_VID1	GPU_VID0	+VGA_CORE	PR901	PR902	PR903	PR904	PL901
0	0	0.85V	1.8K	10.5K	8.87K	54.9K	0.36uH
0	1	1.0V					
1	1	1.025V					

Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

Compal Electronics, Inc.			
Title	+VGA_COREP		
Size	Document Number	PBL21 LA6771P M/B	Rev 0.1
Date: Friday, January 21, 2011	Sheet 57 of 58		



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title	PWR+12V_SEPIC		
Size: Custom	Document Number: PBL21 LA6771P M/B		Rev: 0.1
Date: Friday, January 21, 2011	Sheet 58 of 58		