

Compal Confidential

Schematics Document

AUBURNDALE with Intel
IBEX PEAK-M core logic

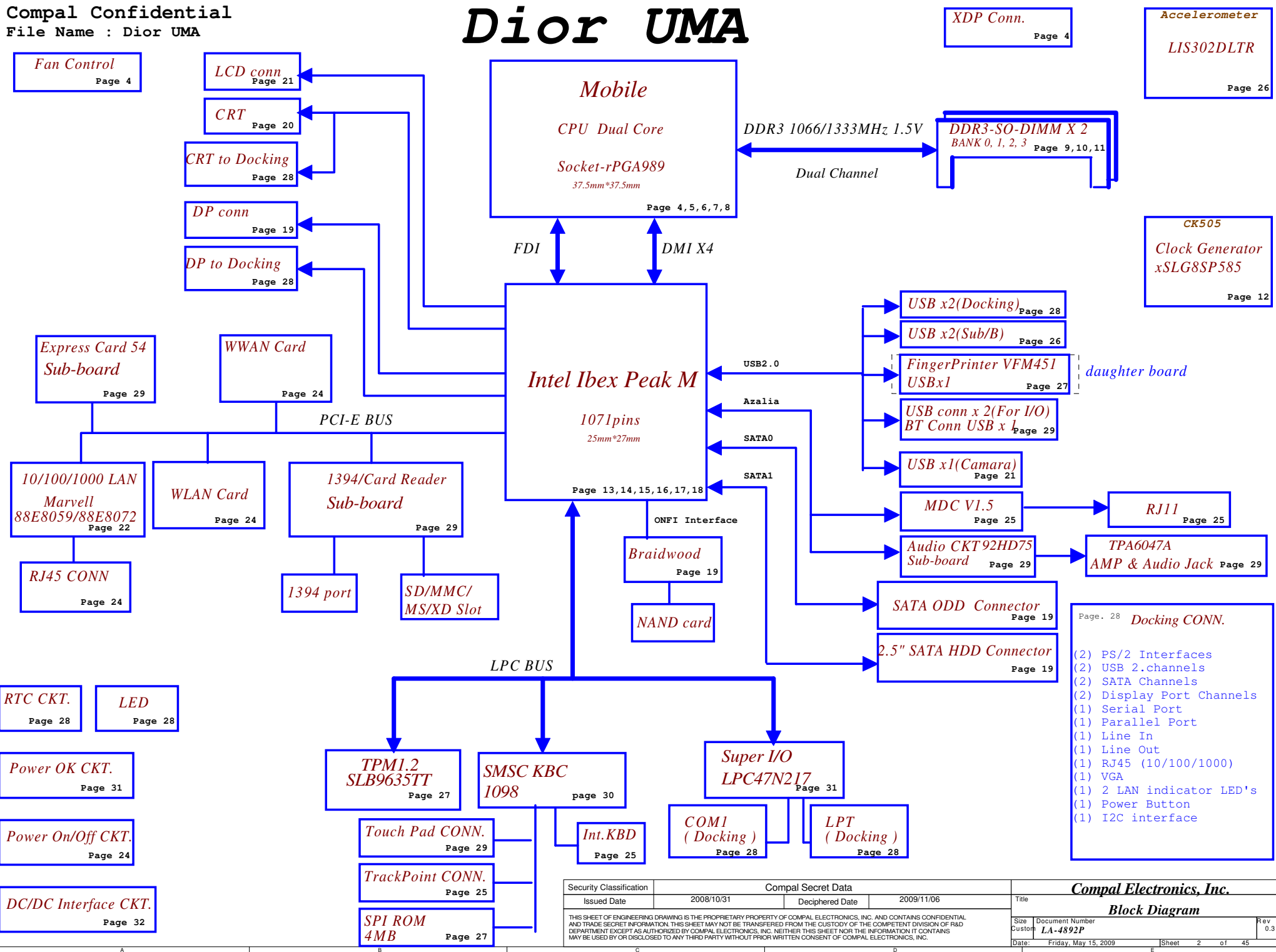
Dior UMA

2009-05-16

REV: 0.3

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				Date: Friday, May 15, 2009	Rev 0.3
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Dior UMA

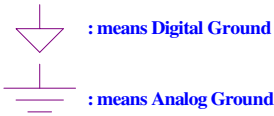


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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B +3VL	+5VALW +3VALW	+1.5V +0.75V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +1.05VS +1.8VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

Symbol Note :



Install below 43 level BOM structure for ver. 0.2

8072@ : Install for 8072 NIC controller

Install below 45 level BOM structure for ver. 0.2

45@ : means just put it in the BOM of 45 level.

Reserve below BOM structure for ver. 0.2

@ : means just reserve , no build

CONN@ : means ME part.

8059@ : Install for 8059 NIC controller

SMBUS Control Table

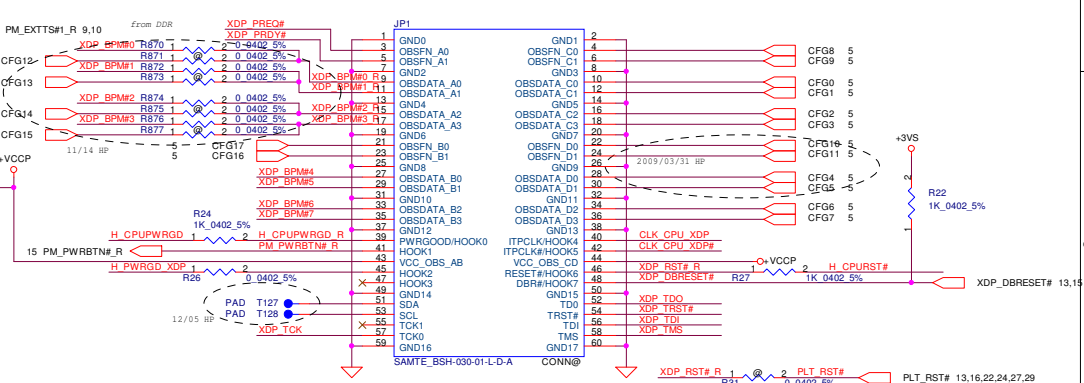
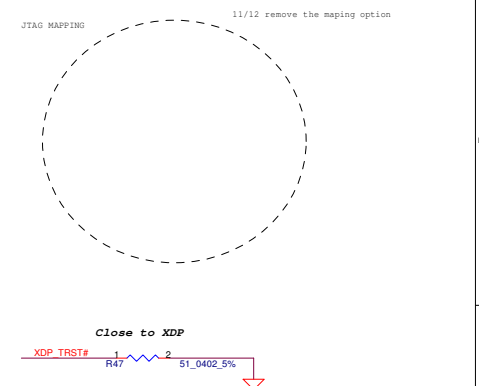
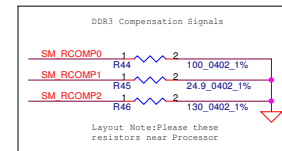
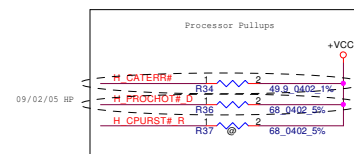
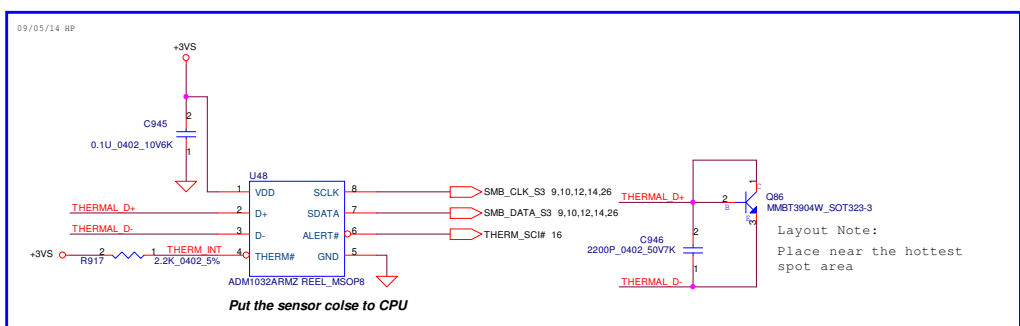
	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	V	X	V
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	X

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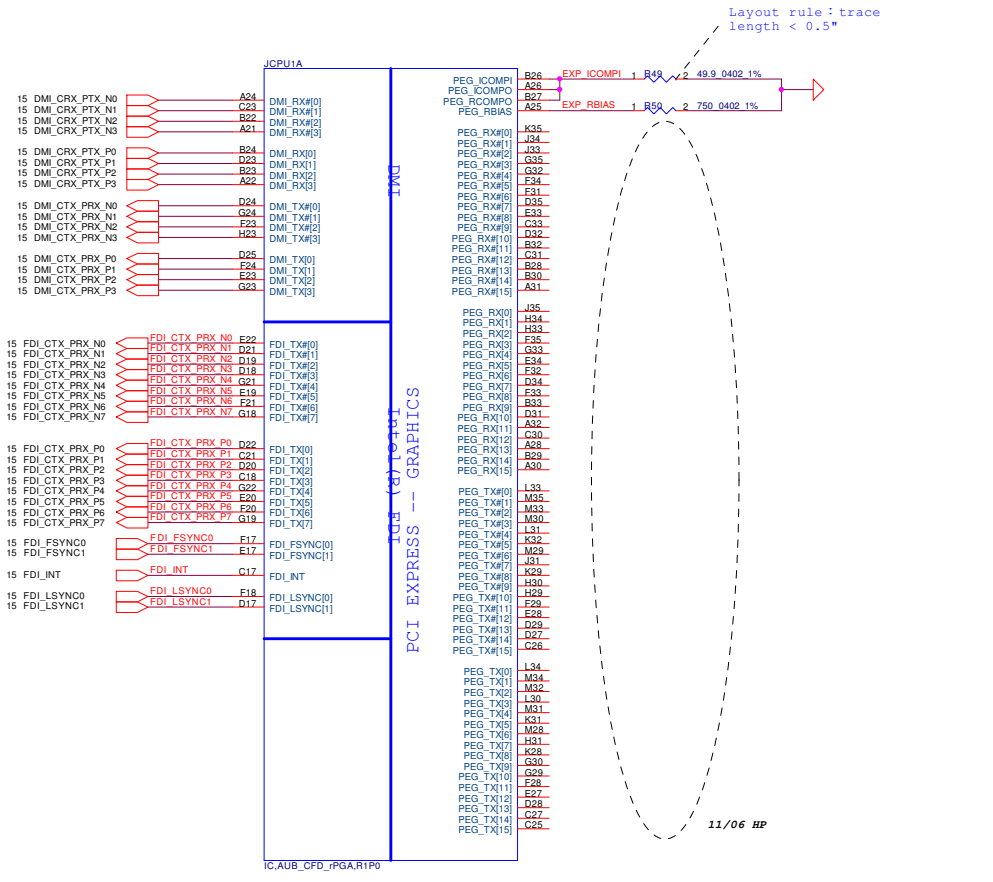
The schematic diagram illustrates the internal wiring of the JCPU1B board, organized into functional blocks:

- JCPU1B**: The central processing unit at the top.
- MISC**: Miscellaneous components including COMP0, COMP1, COMP2, COMP3, SKTOCC#, CATERR#, PECI, PROCHOT#, THERMTRIP#, RESET_OBS#, PM_SYNC, VCCPWRGOOD_1, VCCPWRGOOD_0, SM_DRAMPWROK, TAPPWRGOOD, RSTIN#, and IC.AUB_CFD_PGA,R1P0.
- CLOCKS**: Clock signals including BCLK_BCLK#, BCLK_ITP, BCLK_ITPW, PEG_CLK#, PEG_CLK#, DPLL_REF_SCLK#, DPLL_REF_SSCLK#, CLK_CPU_BCLK_16, CLK_CPU_BCLK#_16, CLK_EXP_14, CLK_EXP#_14, and FES.
- THERMAL**: Thermal management components including H_PECI ISO, H_PROCHOT# D, H_THERMTRIP# R, H_CPURST# R, H_PM_SYNC R, H_CPUVWRGD R, VDDPWRGOOD_0 AK13, H_PVRGD_XDP R, and PLT_RST# R.
- DDR3 MISC**: Memory-related components including SM_DRAMRST#, SM_RCOPMP0, SM_RCOPMP1, SM_RCOPMP2, PM_EXT_TS[0], PM_EXT_TS[1], ATN28_XDP PRDY#, AP27_XDP PREQ#, AN28_XDP TCK, AP28_XDP TMS, AT27_XDP TRST#, TD1, TD0, DBR#, C1, and 0.1uF 0.402_10VK.
- PWR MANAGEMENT**: Power management components including XDP_PWDY#, XDP_FREQ#, XDP_TCK, XDP_TMS, XDP_TRST#, XDP_TD1, XDP_TD0_M, XDP_DBRSETE, XDP_BPMM0, XDP_BPMM1, XDP_BPMM2, XDP_BPMM3, XDP_BPMM4, XDP_BPMM5, XDP_BPMM6, XDP_BPMM7, and XDP_BPMM8.

The diagram shows the physical layout of the board with components represented by rectangles and wires connecting them to the J1 connector pins. Various signal types are indicated by different symbols (e.g., triangles for clocks, circles for power). A date stamp "09/11/22 HP" is visible in the bottom left corner.

[illegible]

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CFG Straps for PROCESSOR

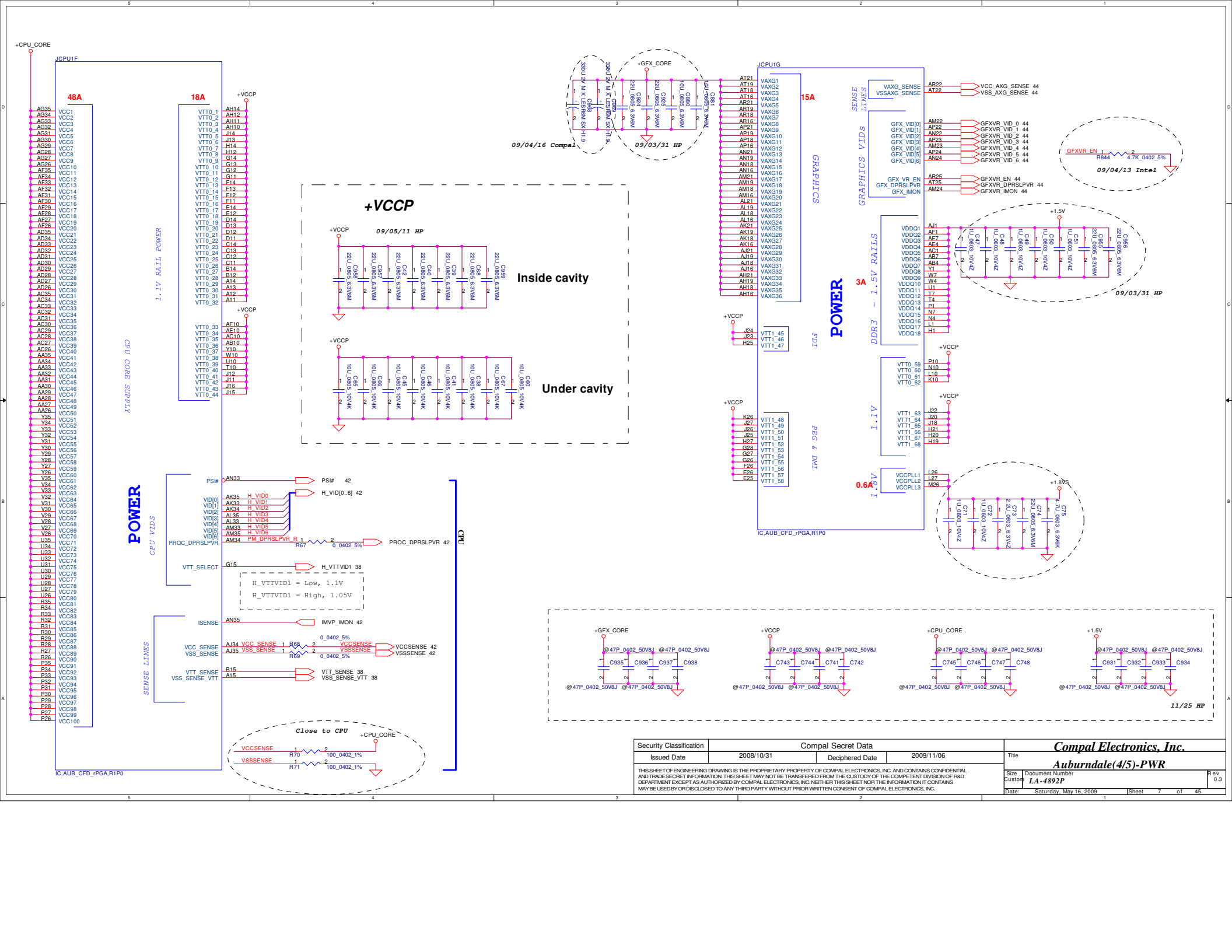
CFG0
R60 @ 5.01K_0402_1%
PCI-Express Configuration Select
CFG0: 1: Single F80
0: Riserfunction enabled
Not applicable for Clocksfield Processor

CFG3
R62 @ 5.01K_0402_1%
CFG01-PCI Express Static Lane Reversal
CFG3: 1: Normal Operation
0: Lane Numbers Reversed
15 -> 0, 14 -> 13,

CFG4
R63 @ 5.01K_0402_1%
CFG04-Display Port Presence
CFG4: 1: Disabled; No Physical Display Port attached to Embedded Display Port
0: Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7
R61 @ 5.01K_0402_1%
Only temporary for early CPD samples (rPGA/BGA)
No needed by MoW41.

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DDR3 SO-DIMM A

TOP SLOT

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DDR3 SO-DIMM A

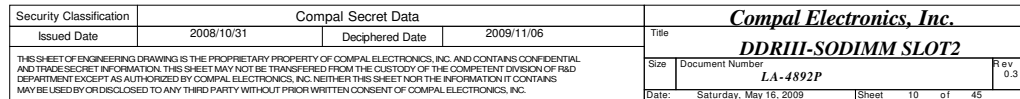
TOP SLOT

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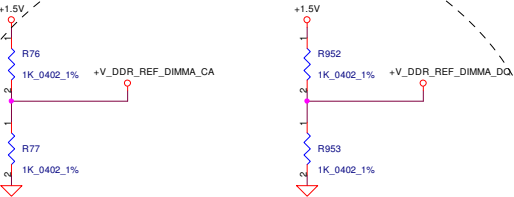
DDR3 SO-DIMM A

TOP SLOT

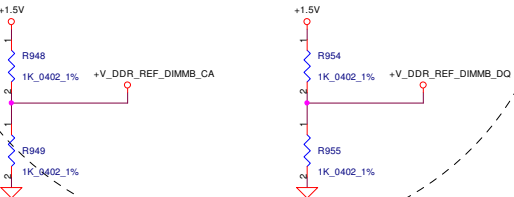
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09/04/03 Auburndale/Arrandale only supports M1 change Vref to +V_DDR_CPU_REF



09/04/23 HP



11/20 Auburndale does not require to support M2 for VrefDQ, HP

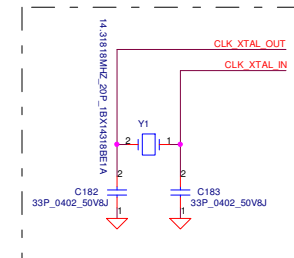
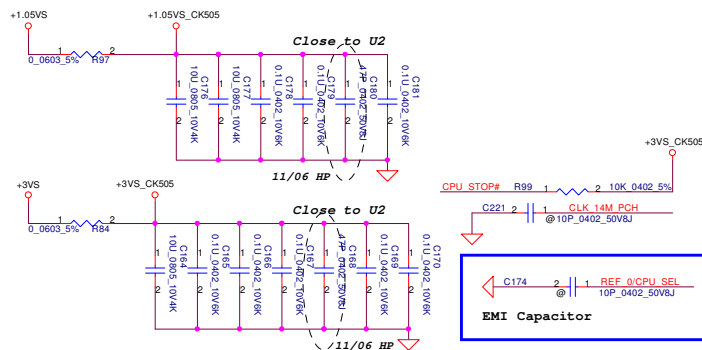
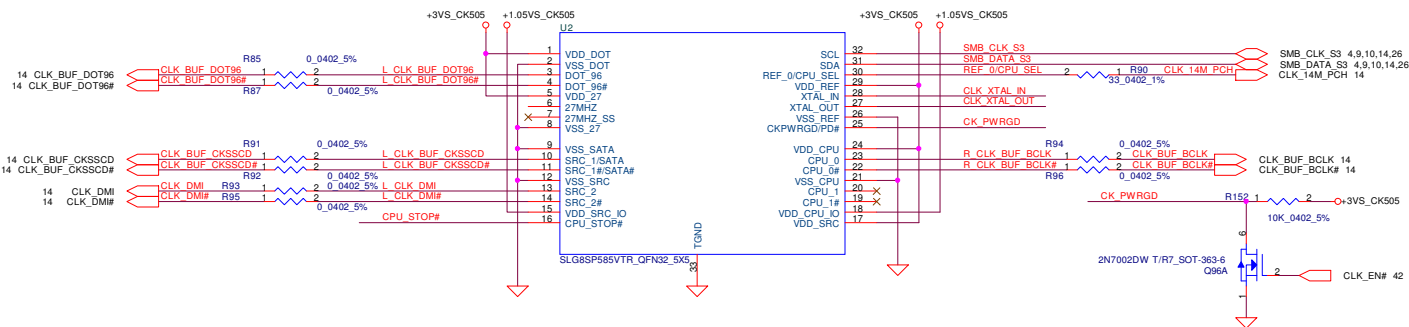
11/20 HP

09/03/31 Auburndale/Arrandale only supports M1, HP

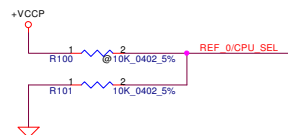
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09/03/31 Auburndale/Arrandale only supports M1, HP

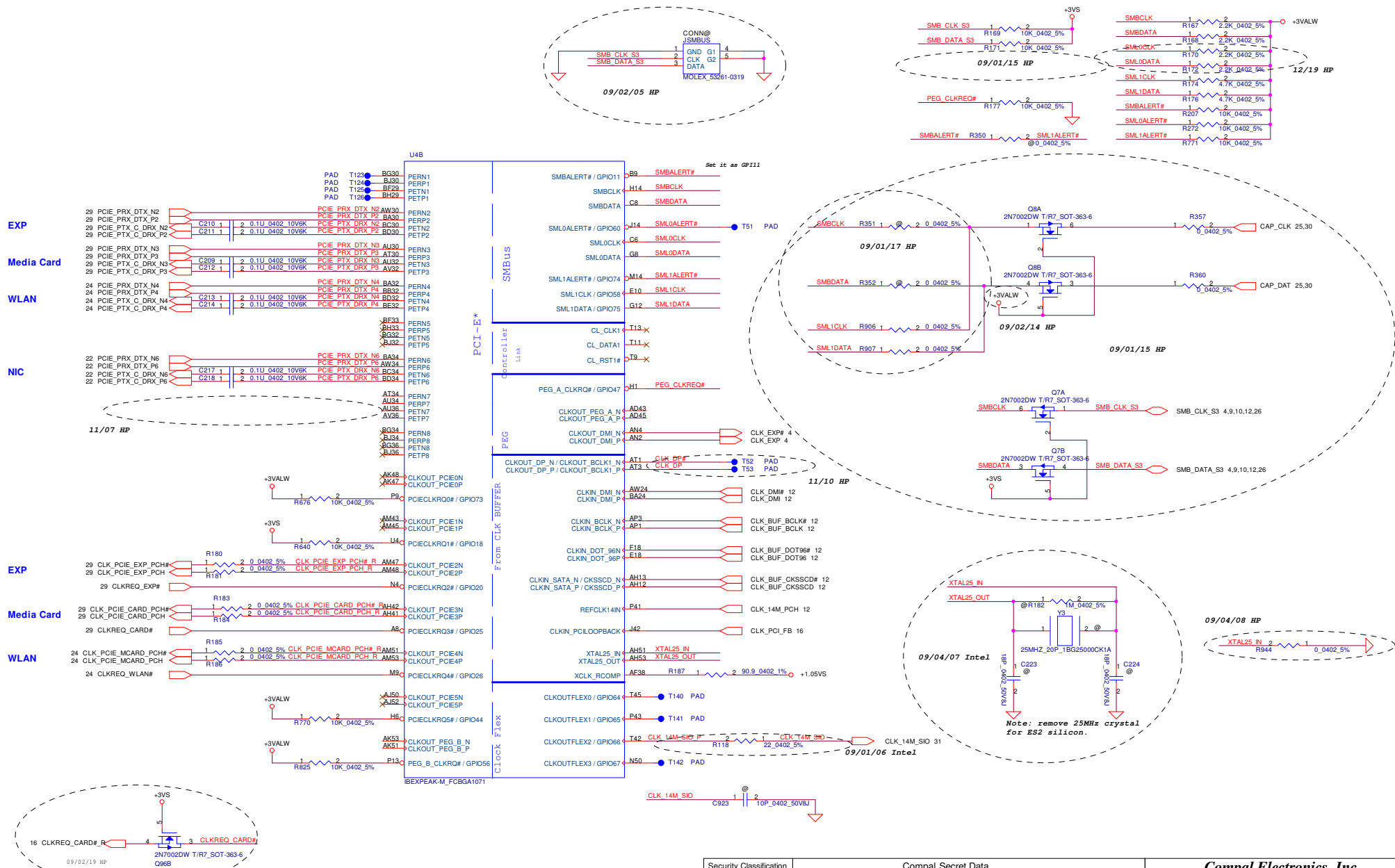
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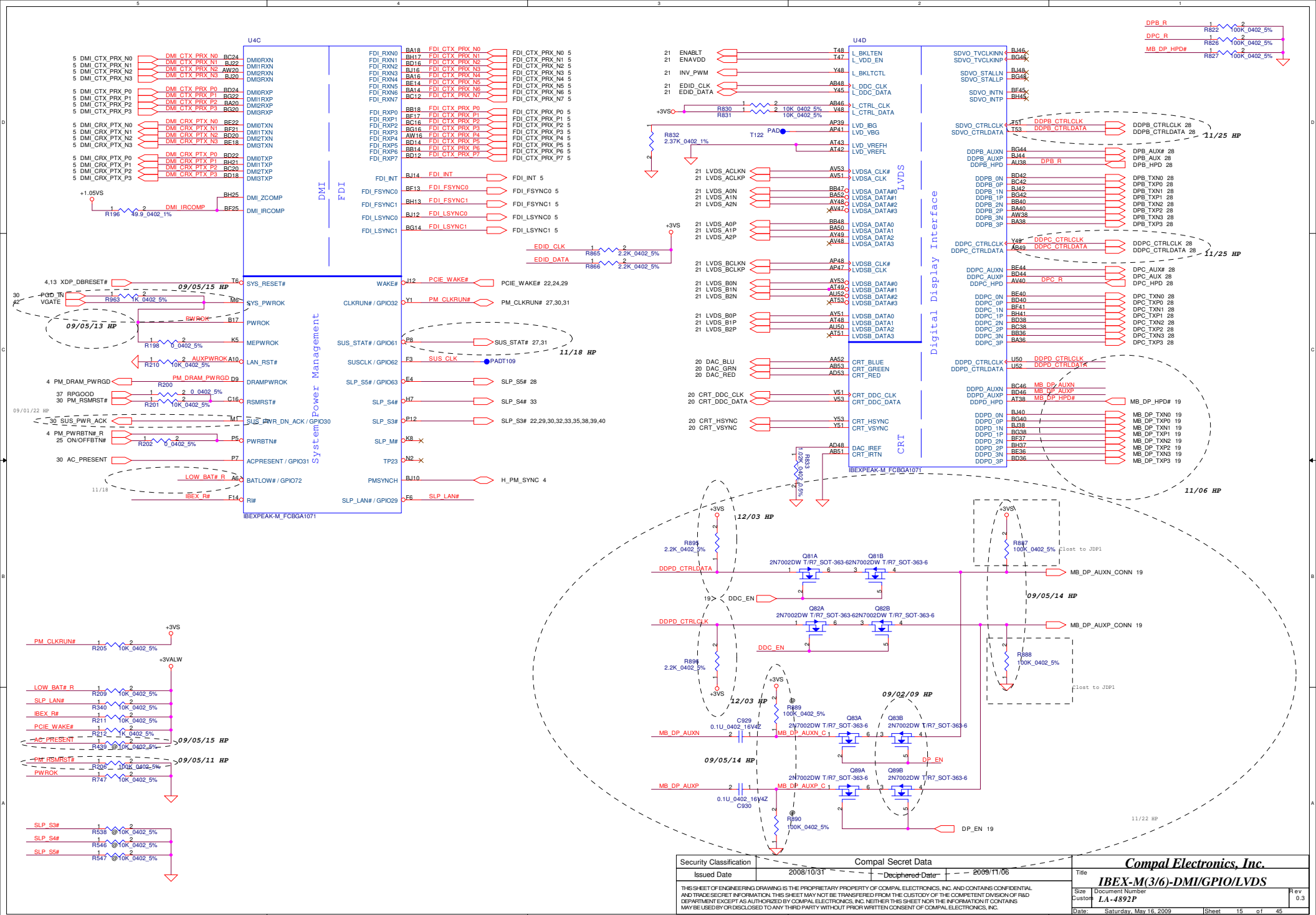
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

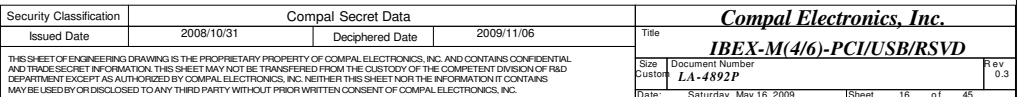


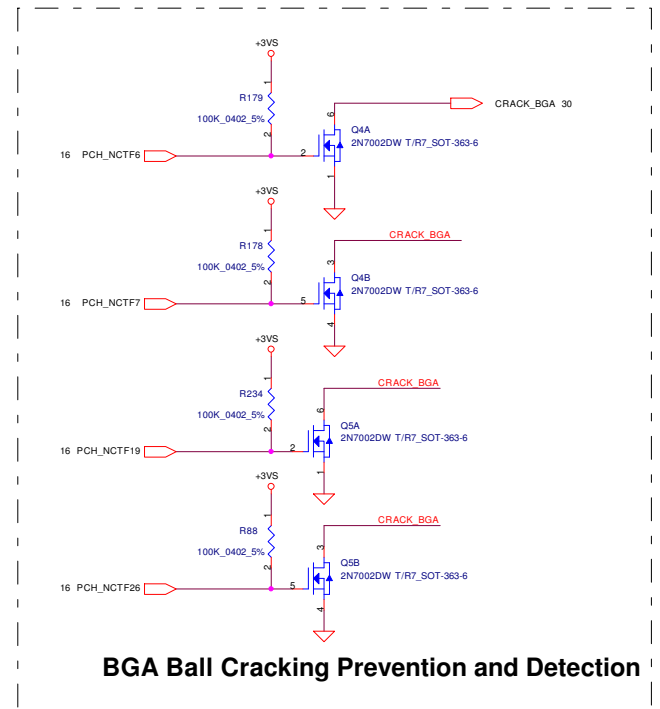
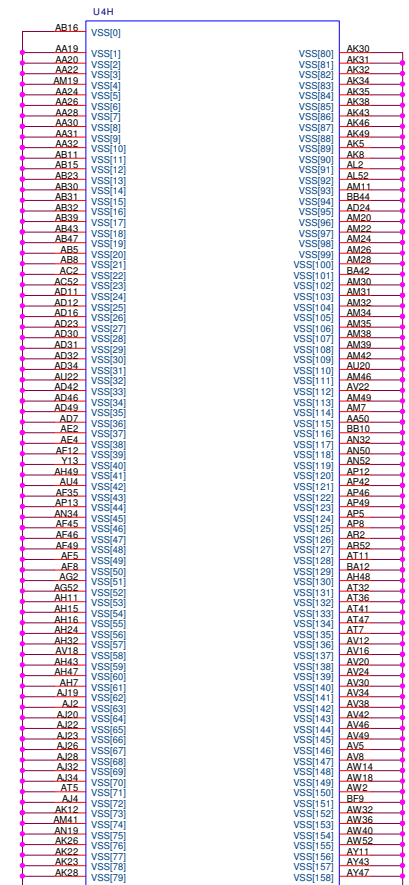
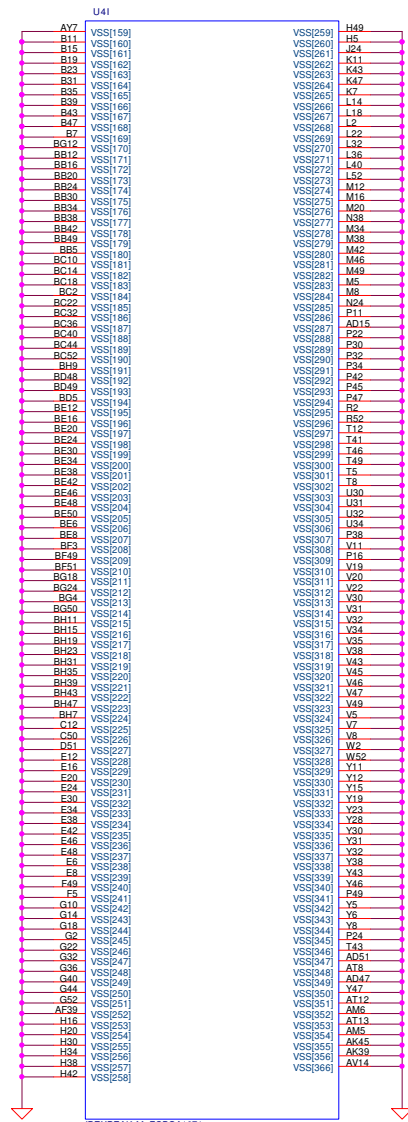
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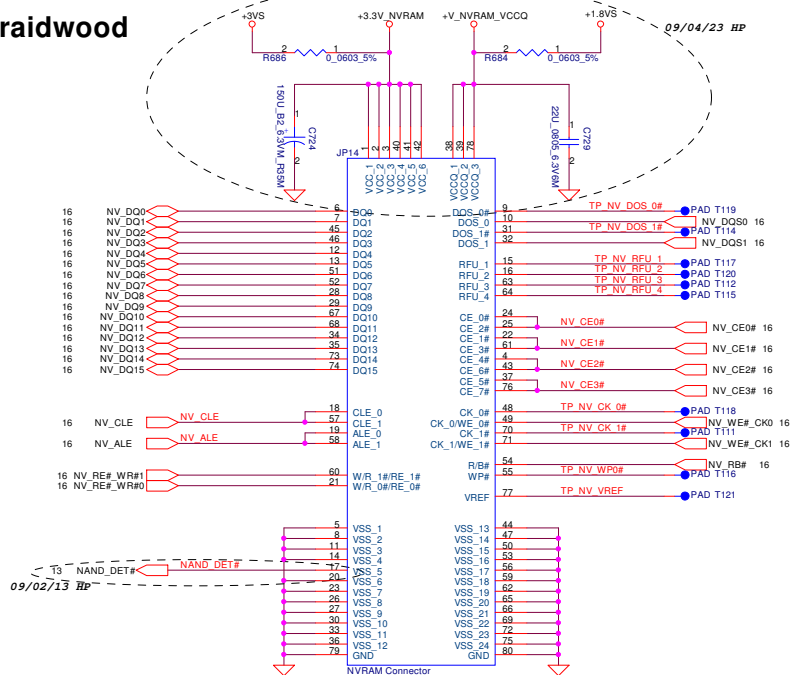




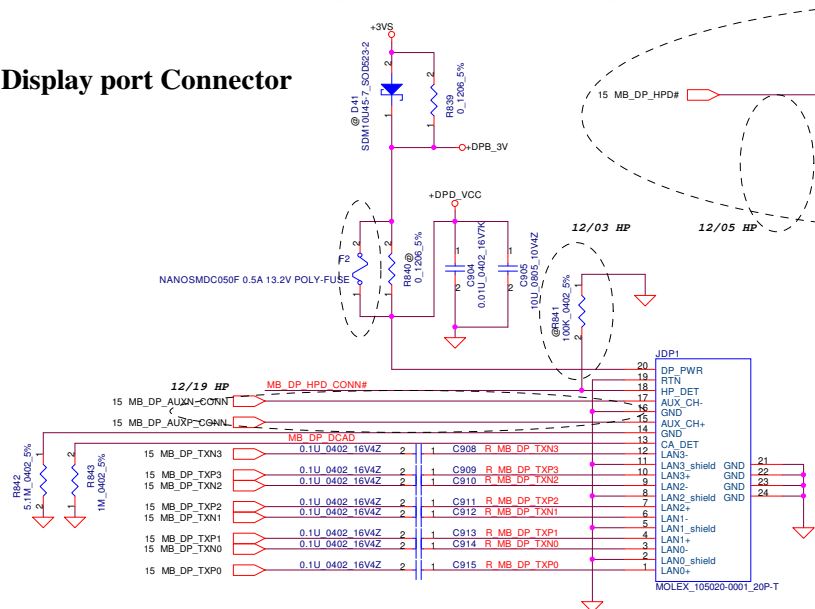
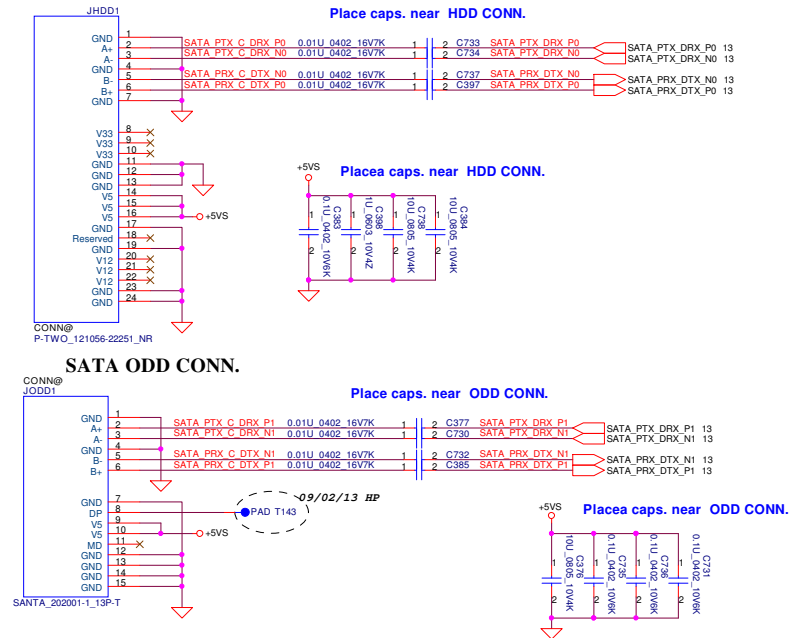


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Braidwood

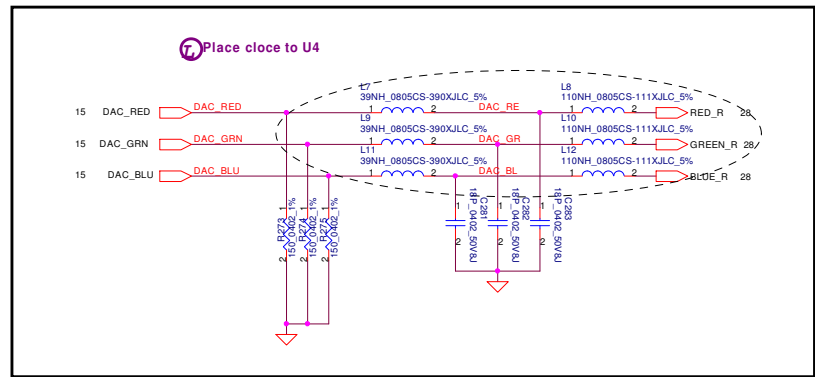
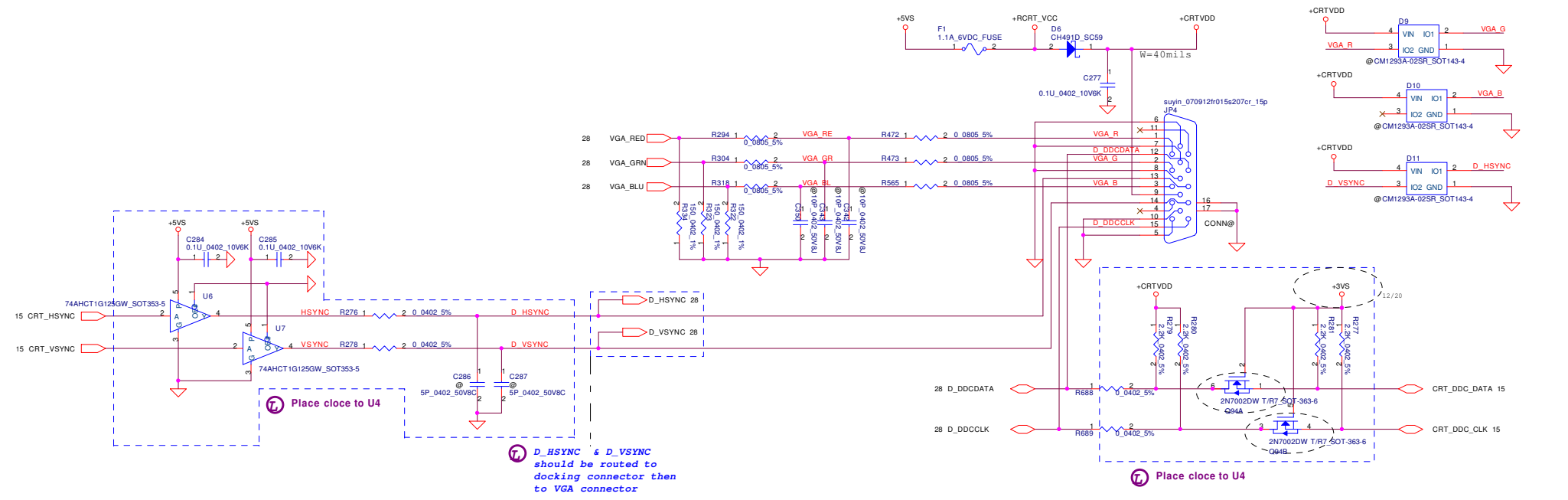


Display port Connector

**SATA HDD CONN.**

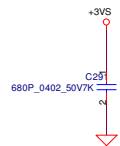
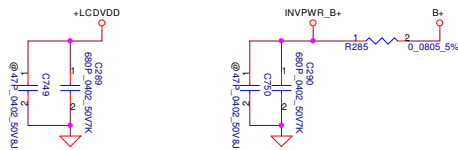
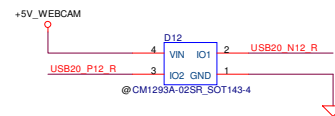
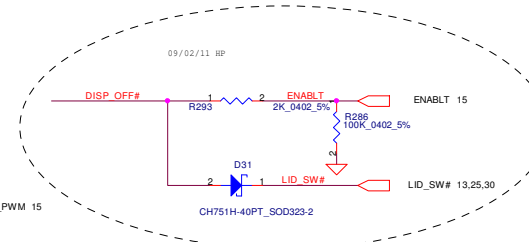
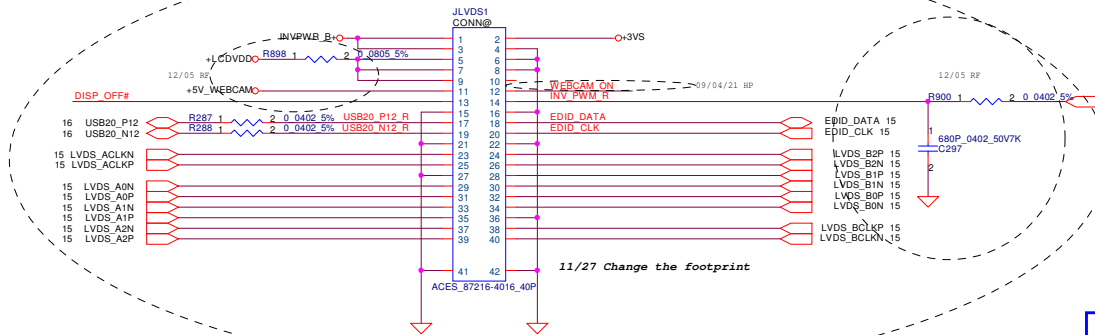
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CRT Connector



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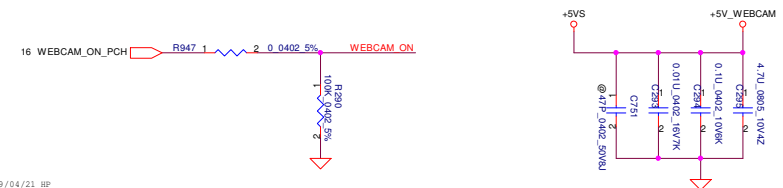
LCD/PANEL BD. CONN.



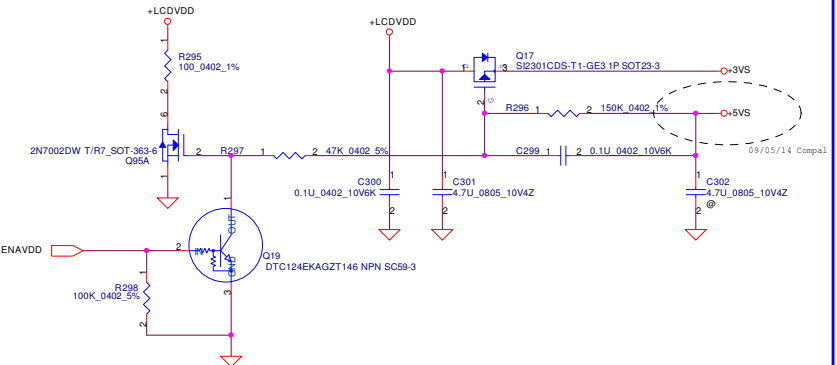
For CCFL only

09/04/13 HP

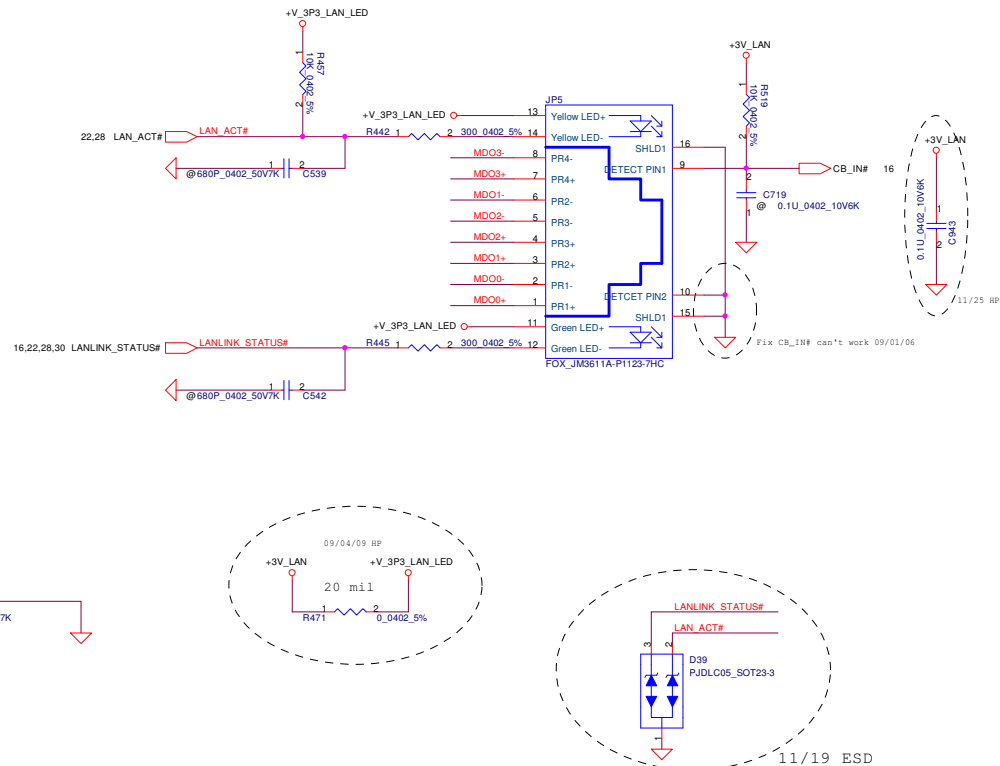
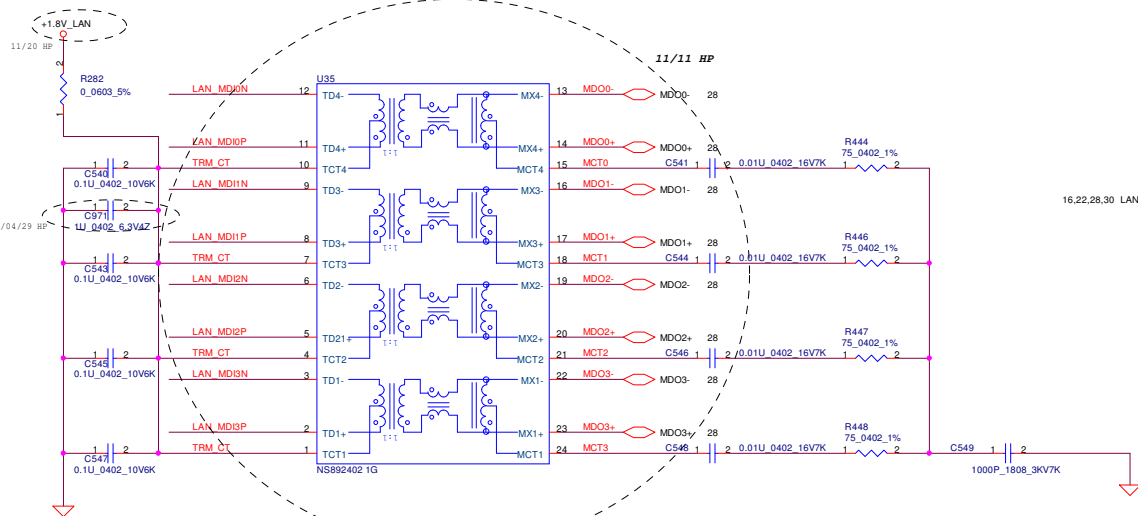
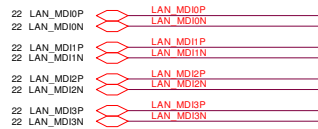
Webcam POWER CIRCUIT



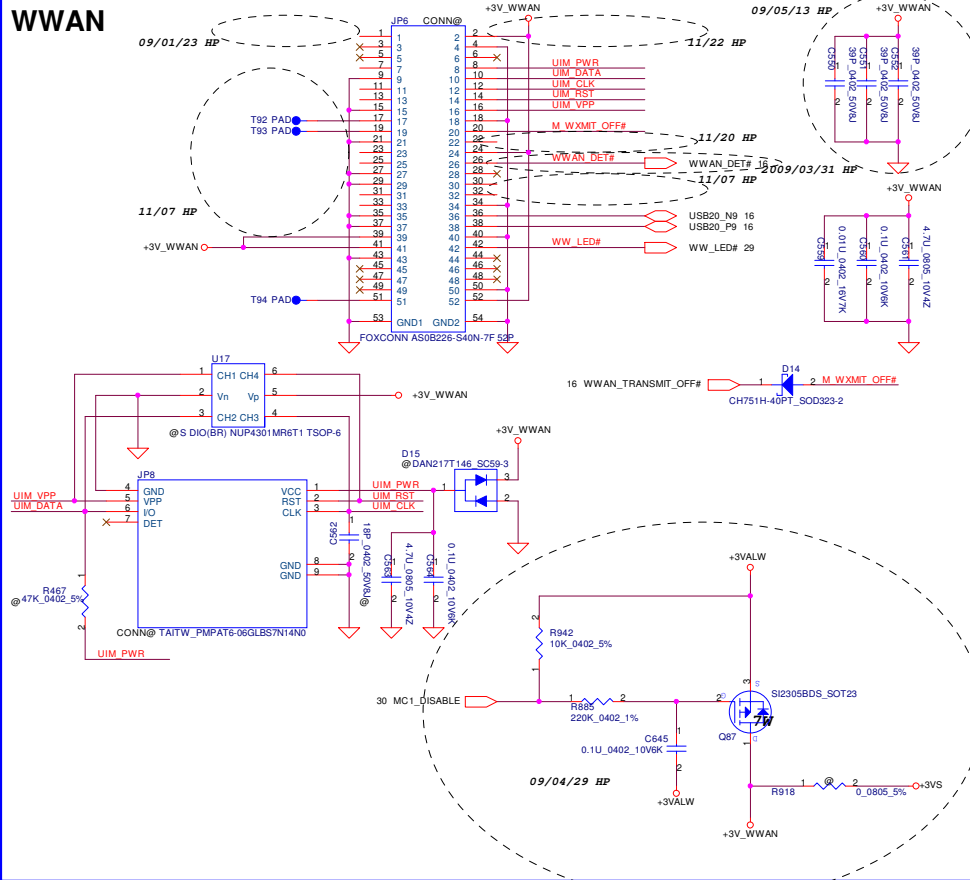
LCD POWER CIRCUIT



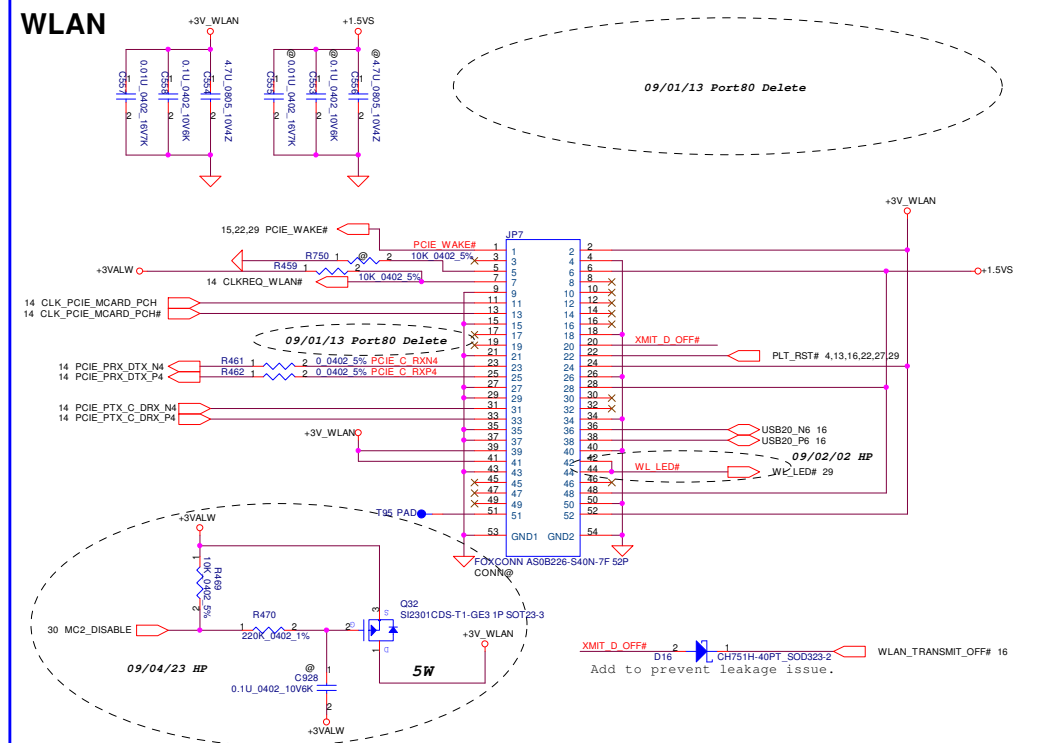
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Issued Date	2008/10/31	Deciphered Date	2009/11/06	Title	LCD CONN & Q-Switch & GPIO Ext.		
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WWAN

WLAN



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power button

The schematic diagram illustrates the power button circuit. It features a 3V_L supply connected to a 100K_0402_5% resistor (R484). The other end of R484 is connected to a node that also receives a signal from ON/OFF# through a 47_0402_5% resistor (R486). This node is also connected to a 1U_0603_10V4Z capacitor (C591) which is grounded. The node is further connected to the anode of a CH751H-40PT_SOD323-2 diode (D25). The cathode of D25 is connected to a 100K_0402_5% resistor (R487), which is then connected to a 3V_ALW supply. The output of the diode is connected to ON/OFFBTN# 15. The ON/OFFBTN_KBC# 30 signal is also connected to the anode of D25.

TrackPoint CONN.

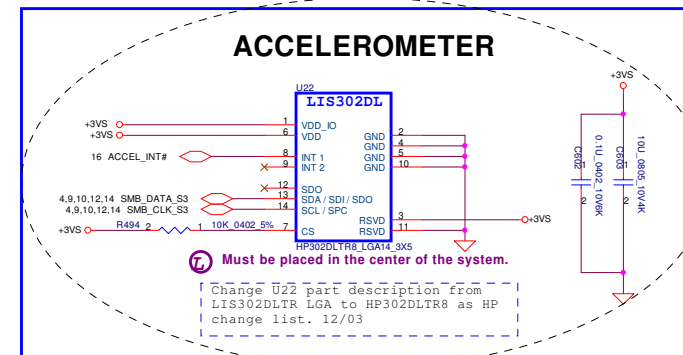
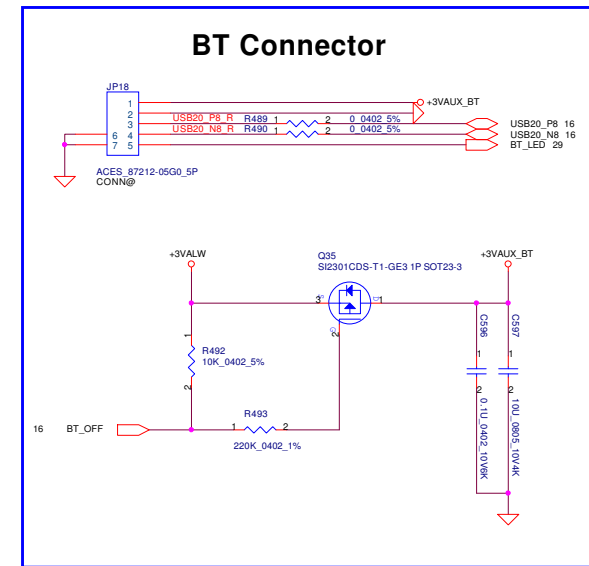
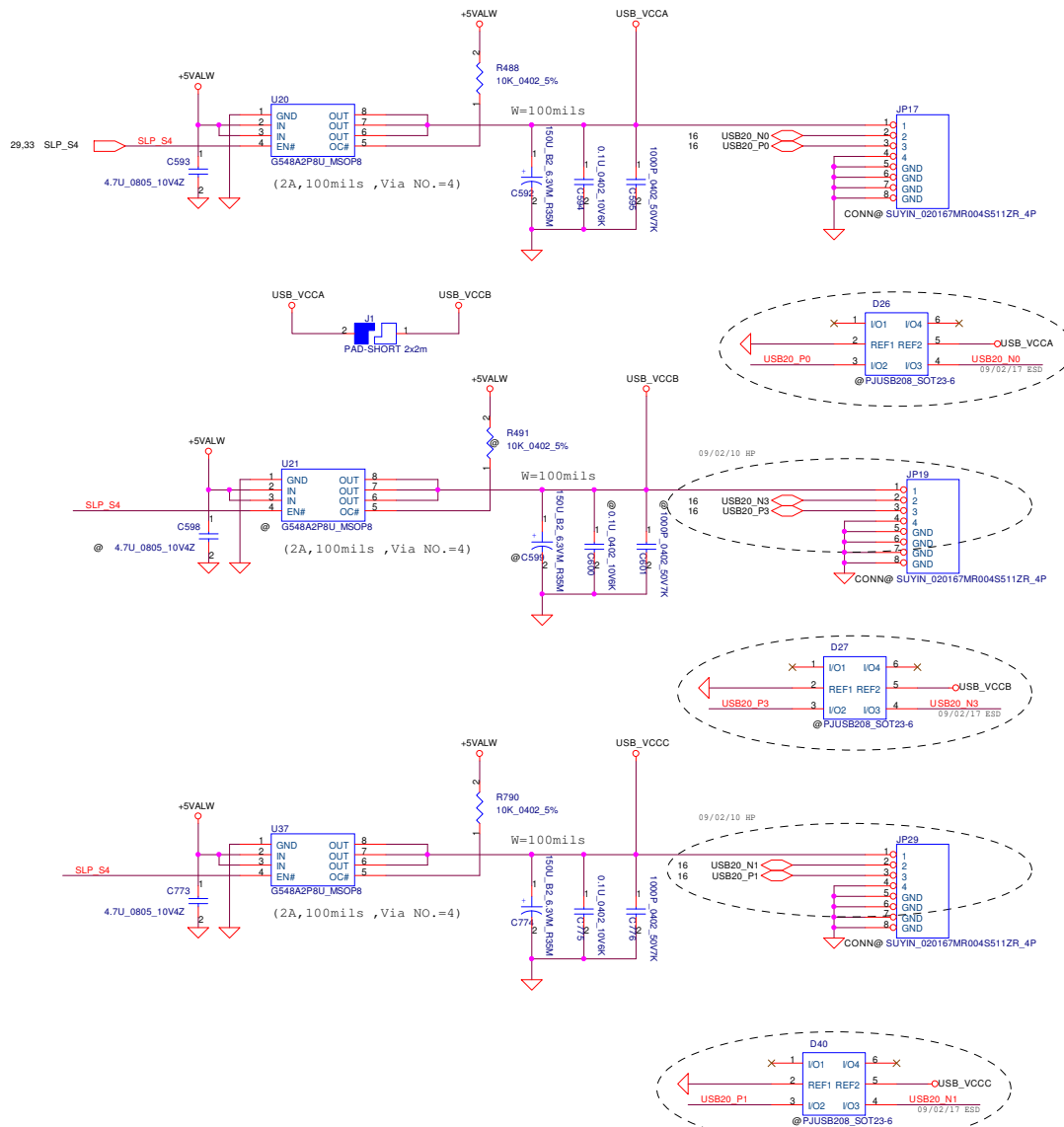
The diagram shows the TrackPoint connector (JP18) with 12 pins. The connections are as follows:

- Pin 1:** +5V
- Pin 2:** SP_DATA
- Pin 3:** SP_CLK
- Pin 4:** SP_DATA
- Pin 5:** SP_CLK
- Pin 6:** SP_DATA
- Pin 7:** SP_CLK
- Pin 8:** SP_DATA
- Pin 9:** G1
- Pin 10:** G2
- Pin 11:** G3
- Pin 12:** G4

The ground pins (9, 10, 11, 12) are connected to a common ground. The SP_CLK and SP_DATA signals are connected to a 0.1μF capacitor, which is then connected to a 5V supply.

09/03/31 Update Pin Out

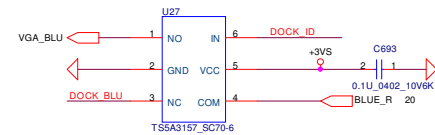
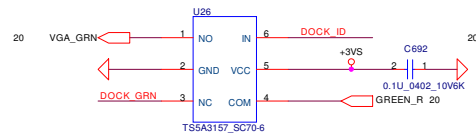
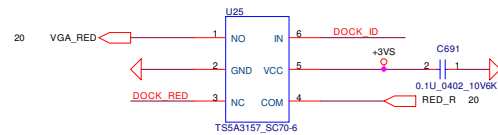
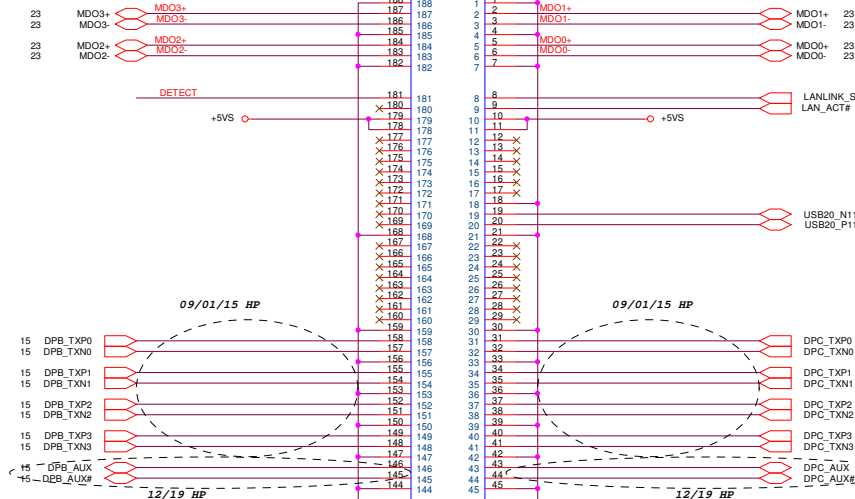
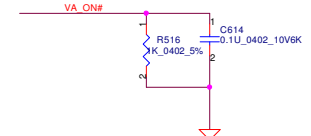
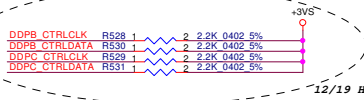
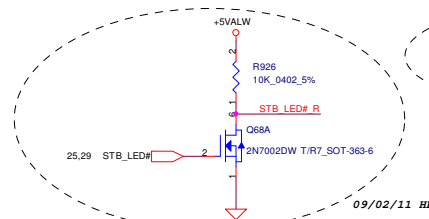
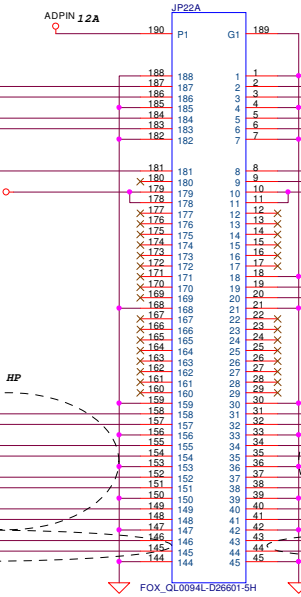
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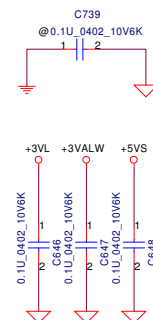
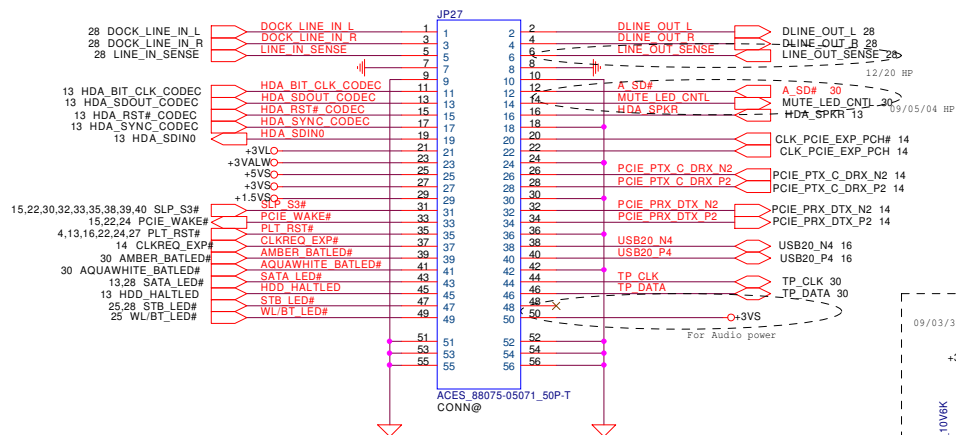
DOCKING CONNECTOR



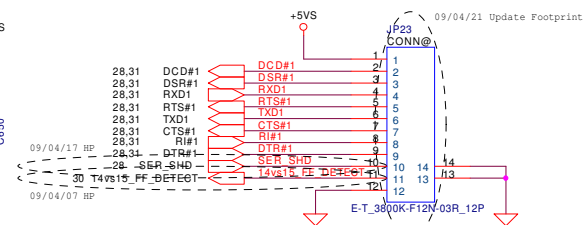
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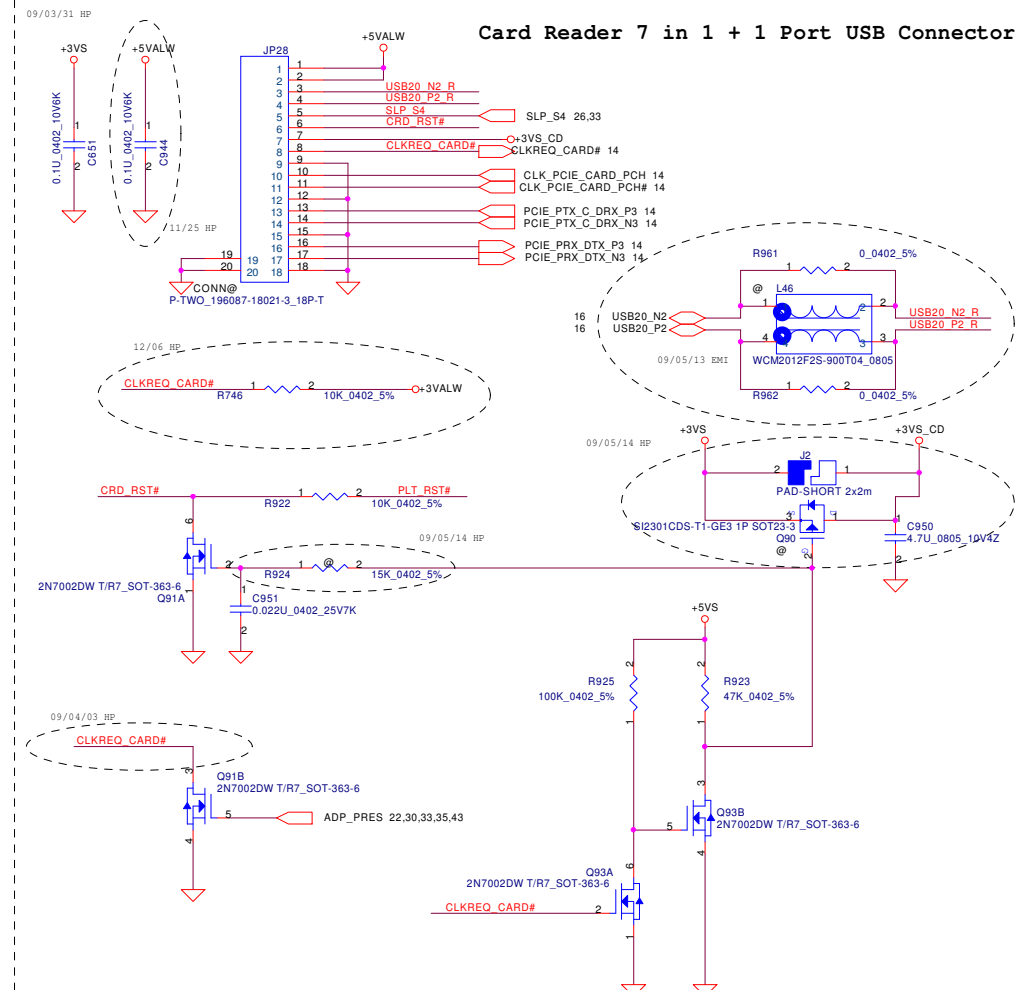
Audio/Express Card/TP/LEDs Connector



Serial Port CONN



Card Reader 7 in 1 + 1 Port USB Connector



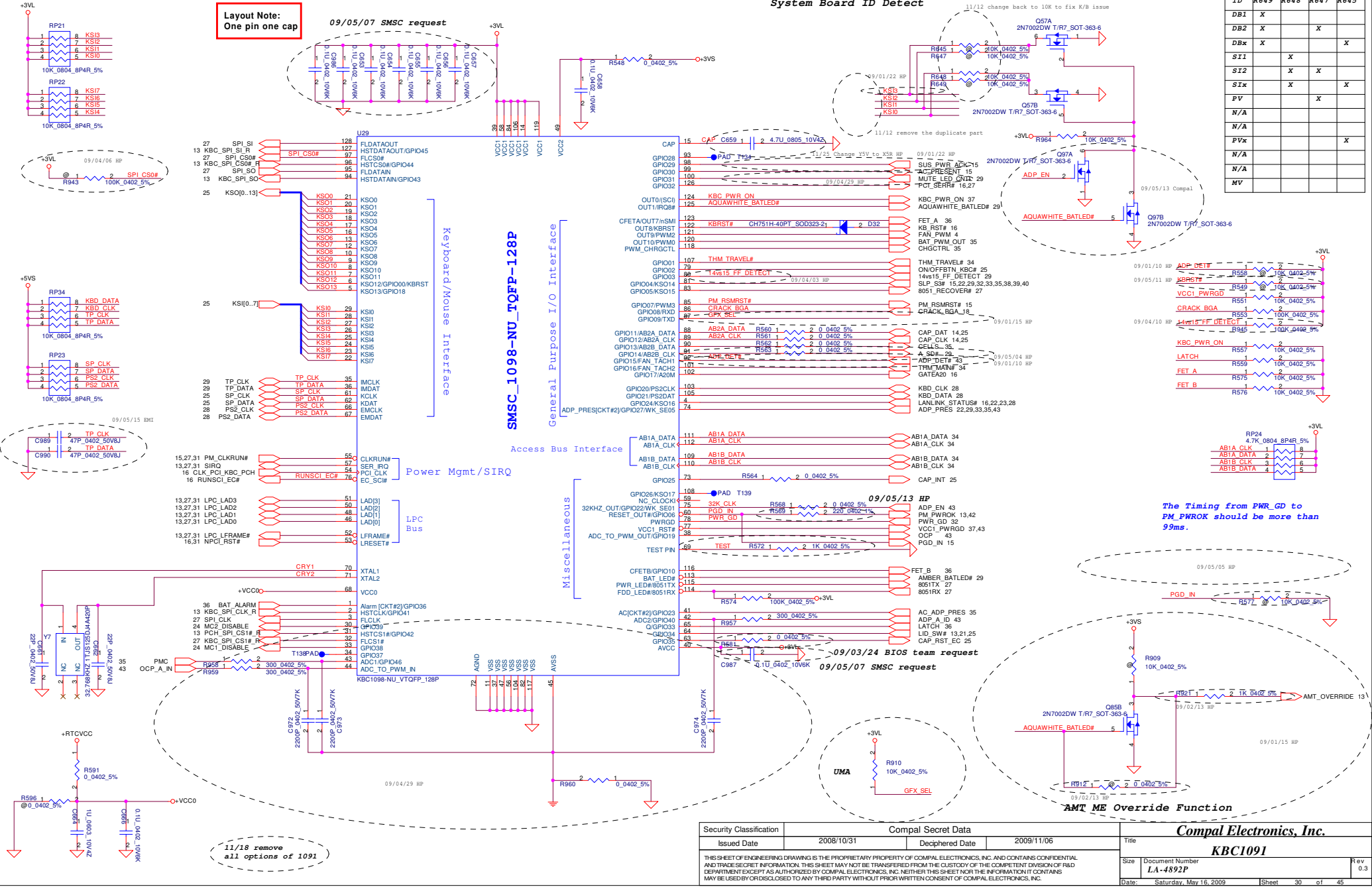
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Layout Note:
One pin one cap

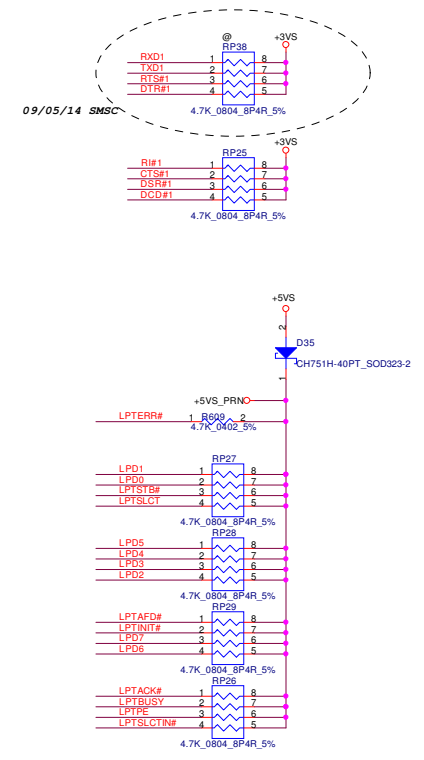
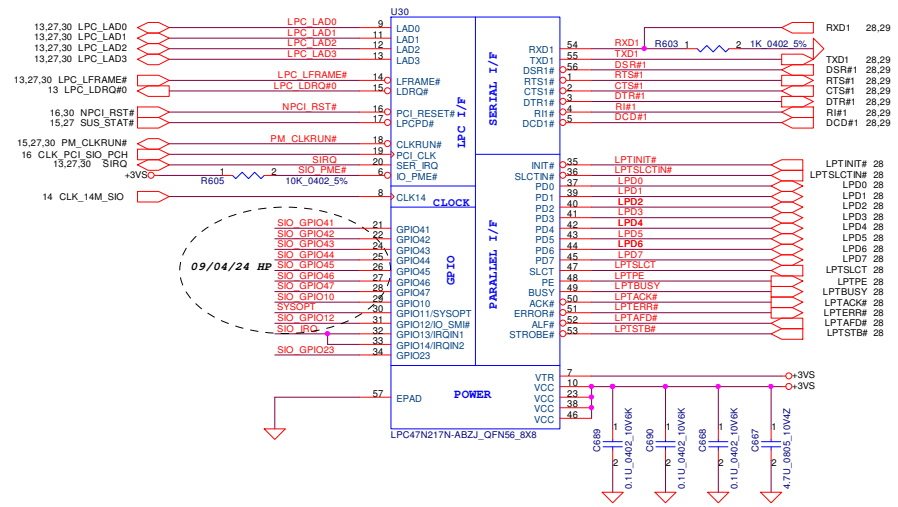
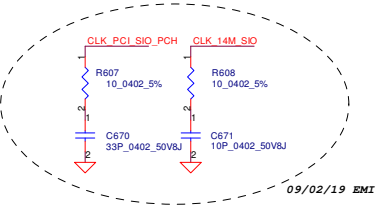
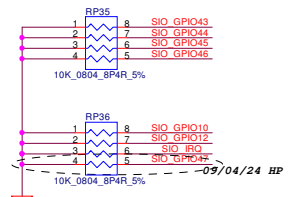
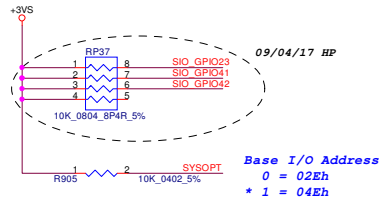
09/05/07 SMSC request

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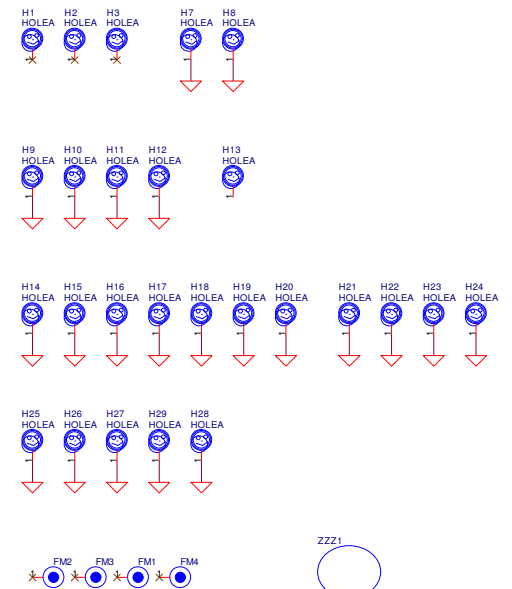
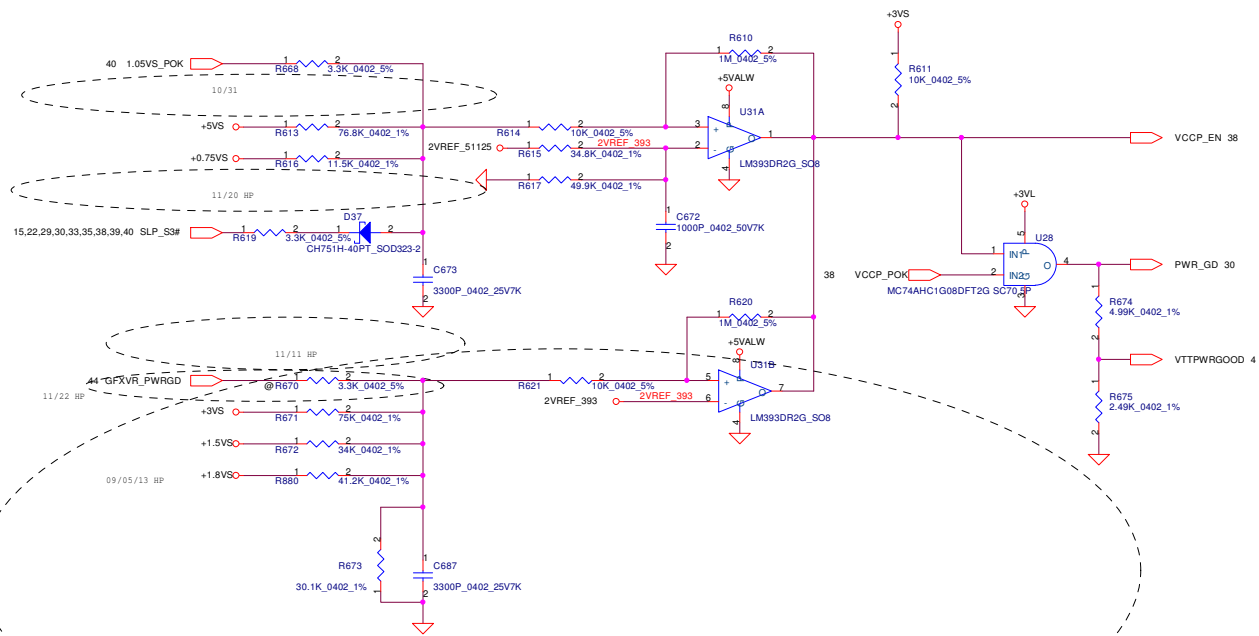
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DB2	X		X	
DBx	X			X
SI1		X		
SI2			X	X
SIx		X		X
PV			X	
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N/A				
PVx				X
N/A				
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MV				



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ZZZ1
PCB-LA-4982P

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[illegible]

+5VALW to +5VS Transfer

The diagram shows a MOSFET (SI7326DN-T1-GE3 1N 1212-8 U34) used for signal transfer. The gate is connected to +5VALW via a 10uF capacitor (C678). The drain is connected to +5VS via a 10uF capacitor (C681). The source is connected to ground through a 10k resistor (R1000). A label 'RUNON' is placed near the source connection.

+1.5VALV to +1.5V Transfer

The schematic diagram illustrates the transfer of a signal from the +1.5VALV input to the +1.5V output. The circuit includes the following components and connections:

- Inputs:** +1.5VALV and +1.5V.
- Resistors:**
 - R791: 330K_0402_5%
 - R793: 820K_0402_5%
 - R794: 470_0402_5%
- Capacitors:**
 - C785: 0.1U_0402_100MK
 - C786: 10U_0805_100MK
- MOSFETs:**
 - Q69A: 2N7002DW T/R7_SOT-363-6
 - Q69B: 2N7002DW T/R7_SOT-363-6
- Signal Path:**
 - The +1.5VALV input is connected to the gate of Q69A through R791 and C786.
 - The gate of Q69A is connected to the gate of Q69B through R793 and C785.
 - The gate of Q69B is connected to the +1.5V output through R794 and C786.
 - The source of Q69A is connected to the source of Q69B through R793 and C785.
 - The source of Q69B is connected to the +1.5V output through R794 and C786.
- Control Signal:**
 - A dashed oval labeled **ADP PRES** is connected to the gates of Q69A and Q69B.
 - The ADP PRES signal is also connected to the gates of Q69A and Q69B through R793 and C785.

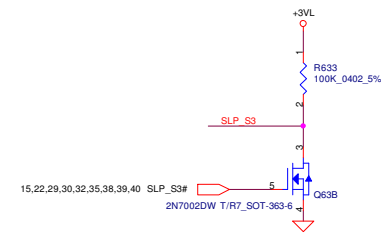
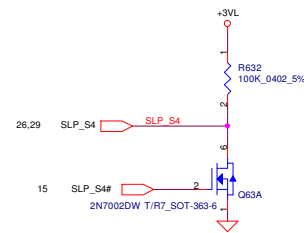
+1.5VALW to +1.5VS Transfer

The diagram shows a MOSFET circuit for transferring power from +1.5VALW to +1.5VS. The MOSFET (U38) has its gate connected to +1.5VALW via capacitor C777. Its drain is connected to +1.5VS via capacitor C779. The source is connected to ground via resistor R792 and capacitor C784. A RUNON signal is connected to the drain via a 0.01U_0402_16V7K capacitor.

+1.8V_LAN to +1.8VS Transfer

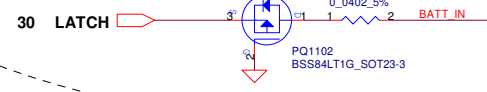
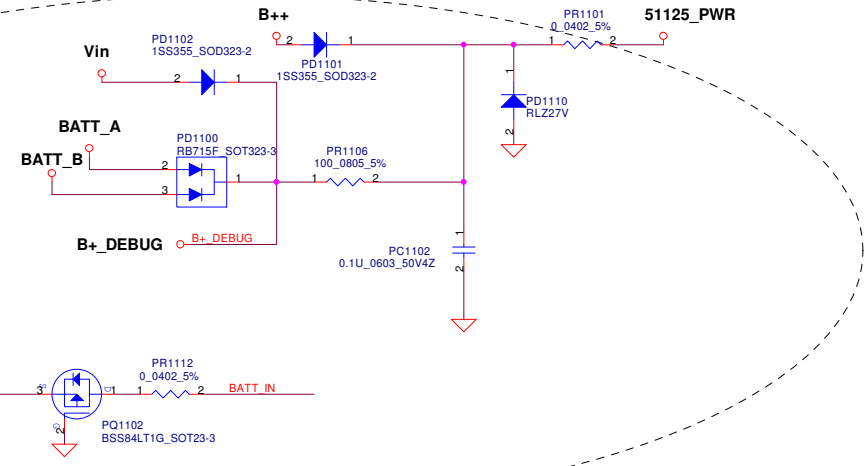
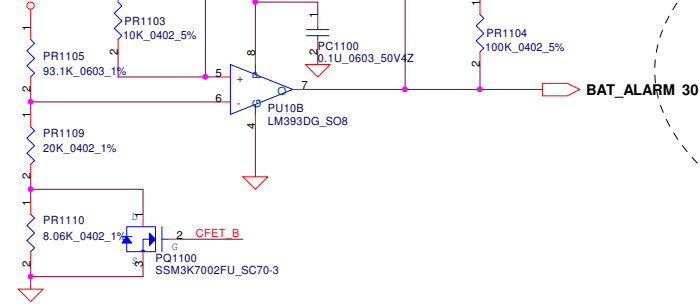
The circuit diagram shows a MOSFET (U39, Si7326DN-T1-GE3 1N1212-8) used for signal transfer. The input is +1.8V_LAN, connected to the gate of the MOSFET through capacitor C786 (100u_0805_10V4K). The drain of the MOSFET is connected to the output +1.8VS through capacitor C788 (100u_0805_10V4K). The source of the MOSFET is connected to ground through capacitor C789 (0.010U_0402_16V7K). A resistor R795 (0.0402 5%) is connected between the drain and the source. The output is labeled RUNON.

Discharge circuit-1

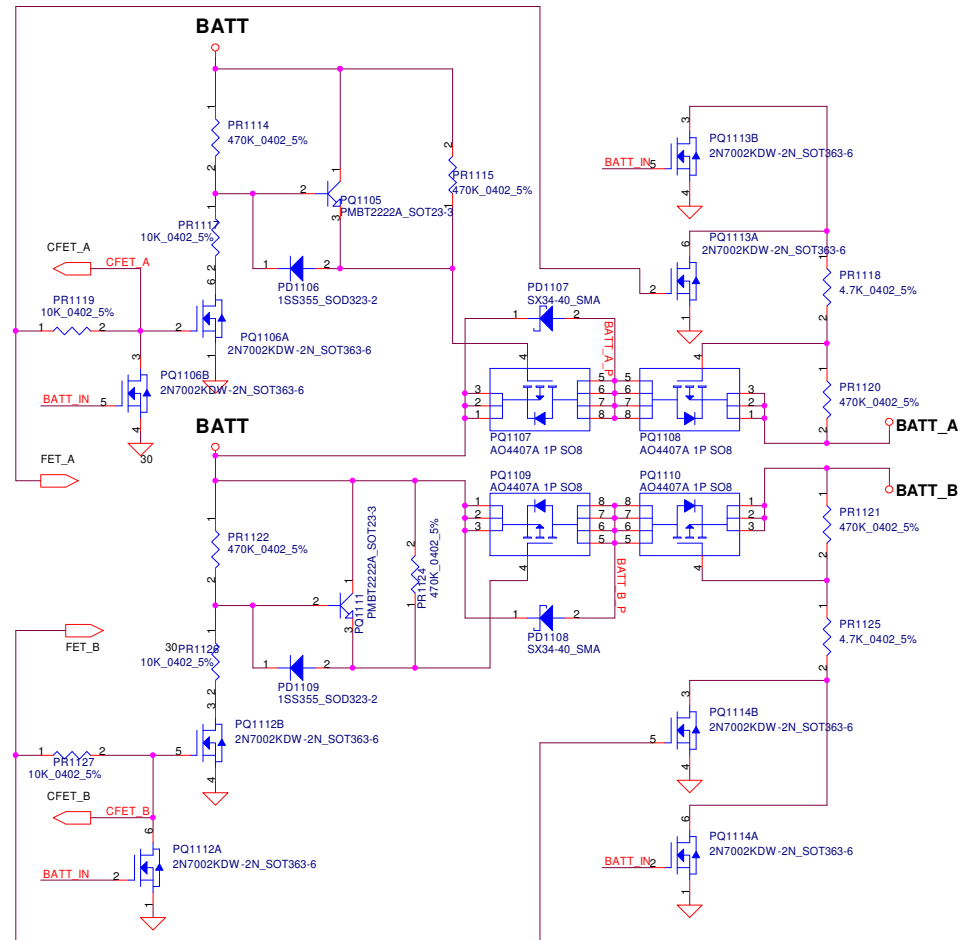


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BATT



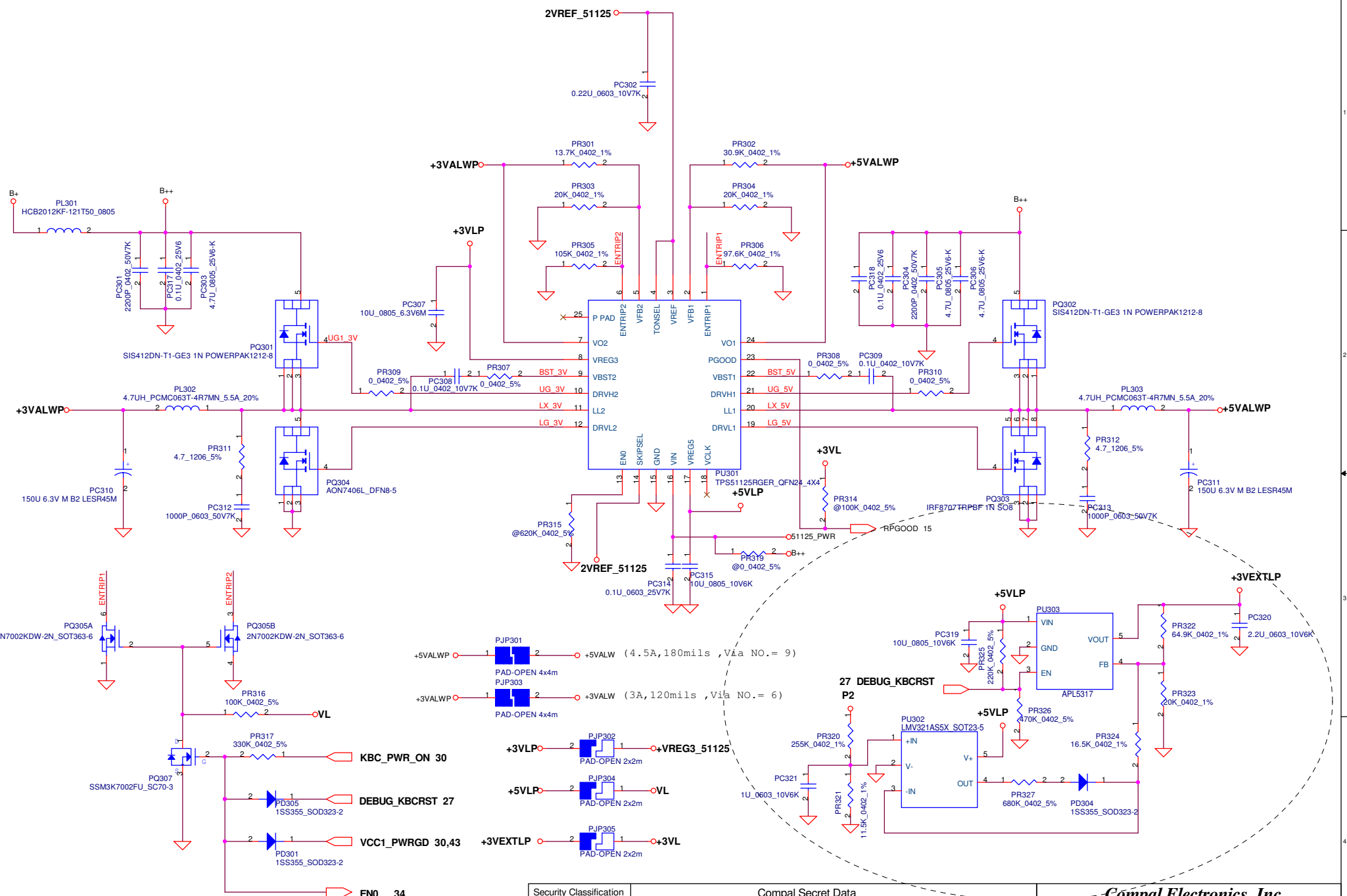
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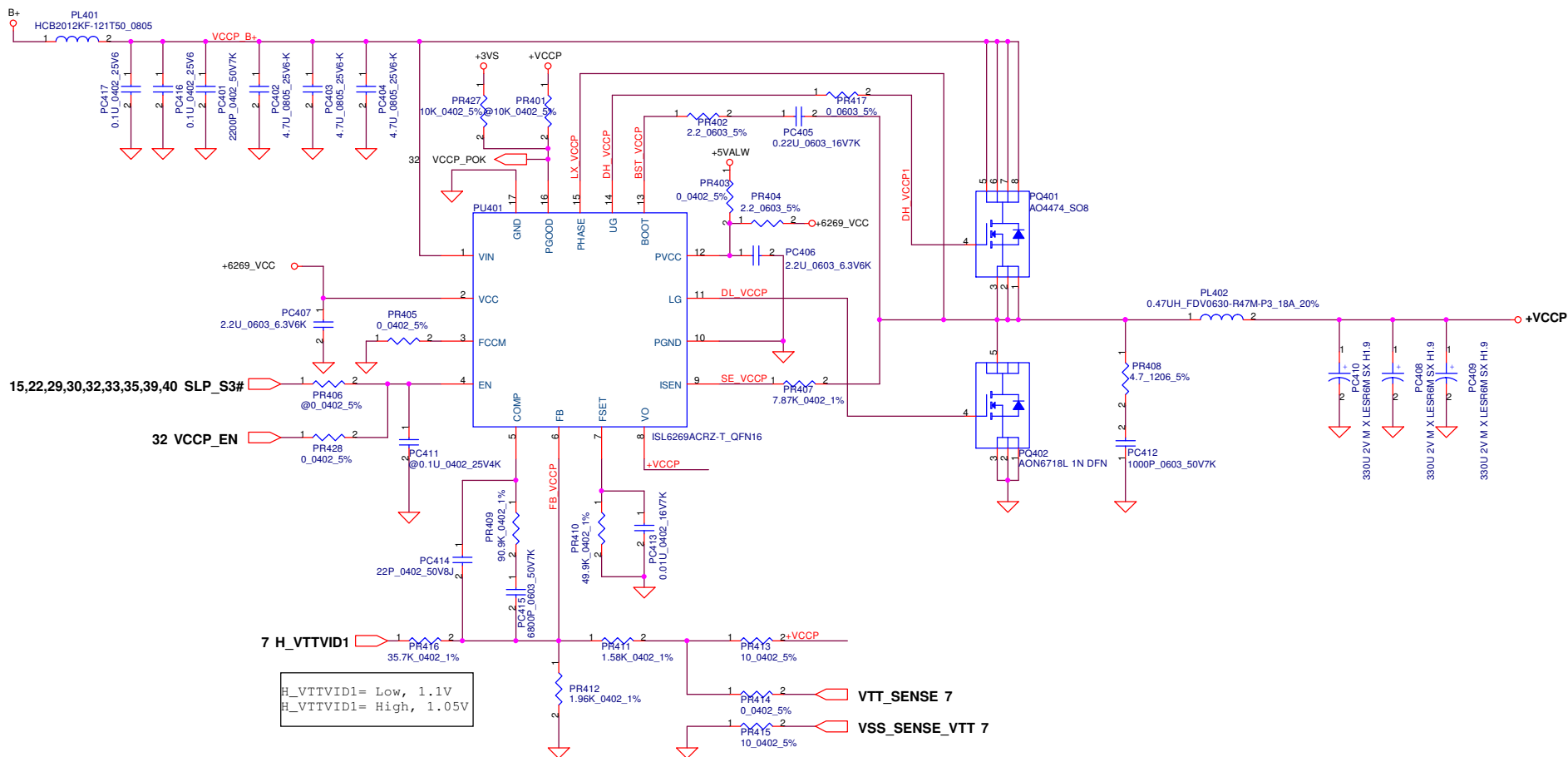
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Battery selector

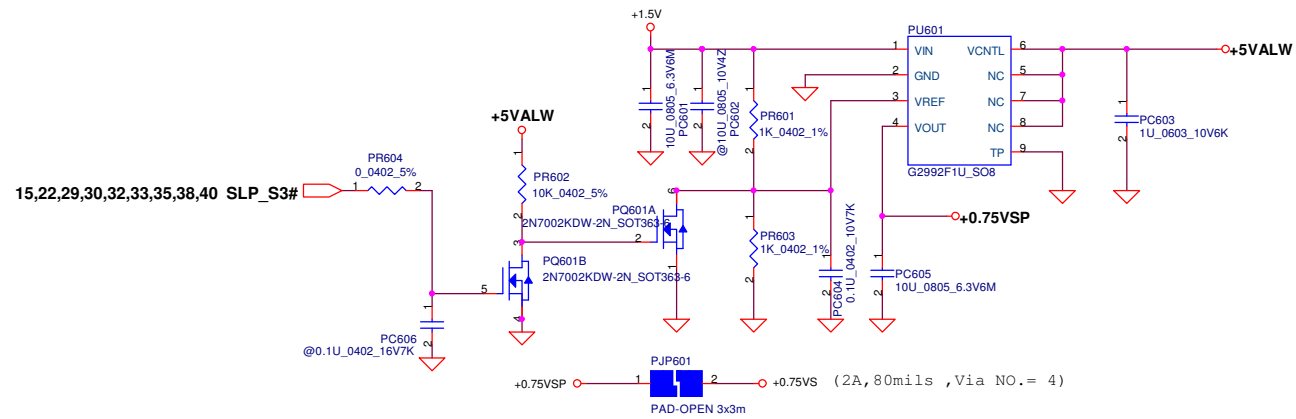


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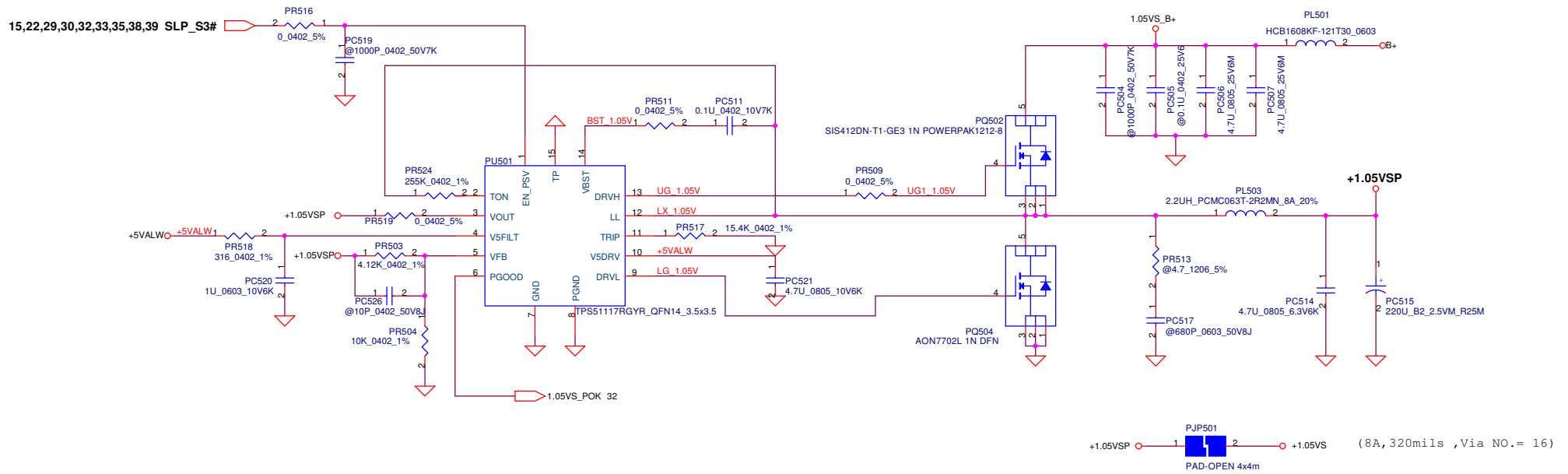
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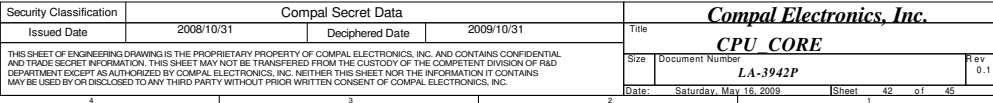
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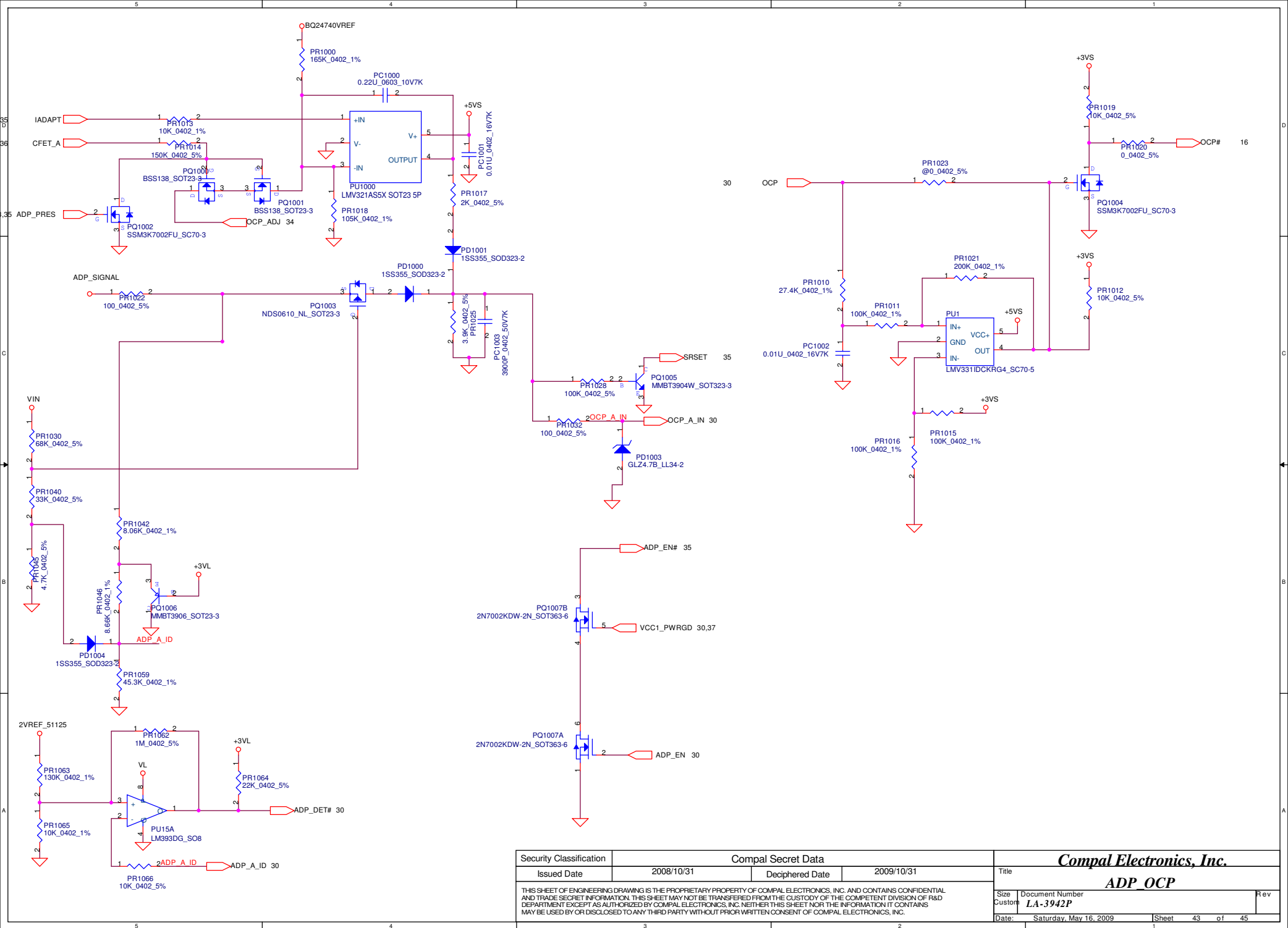


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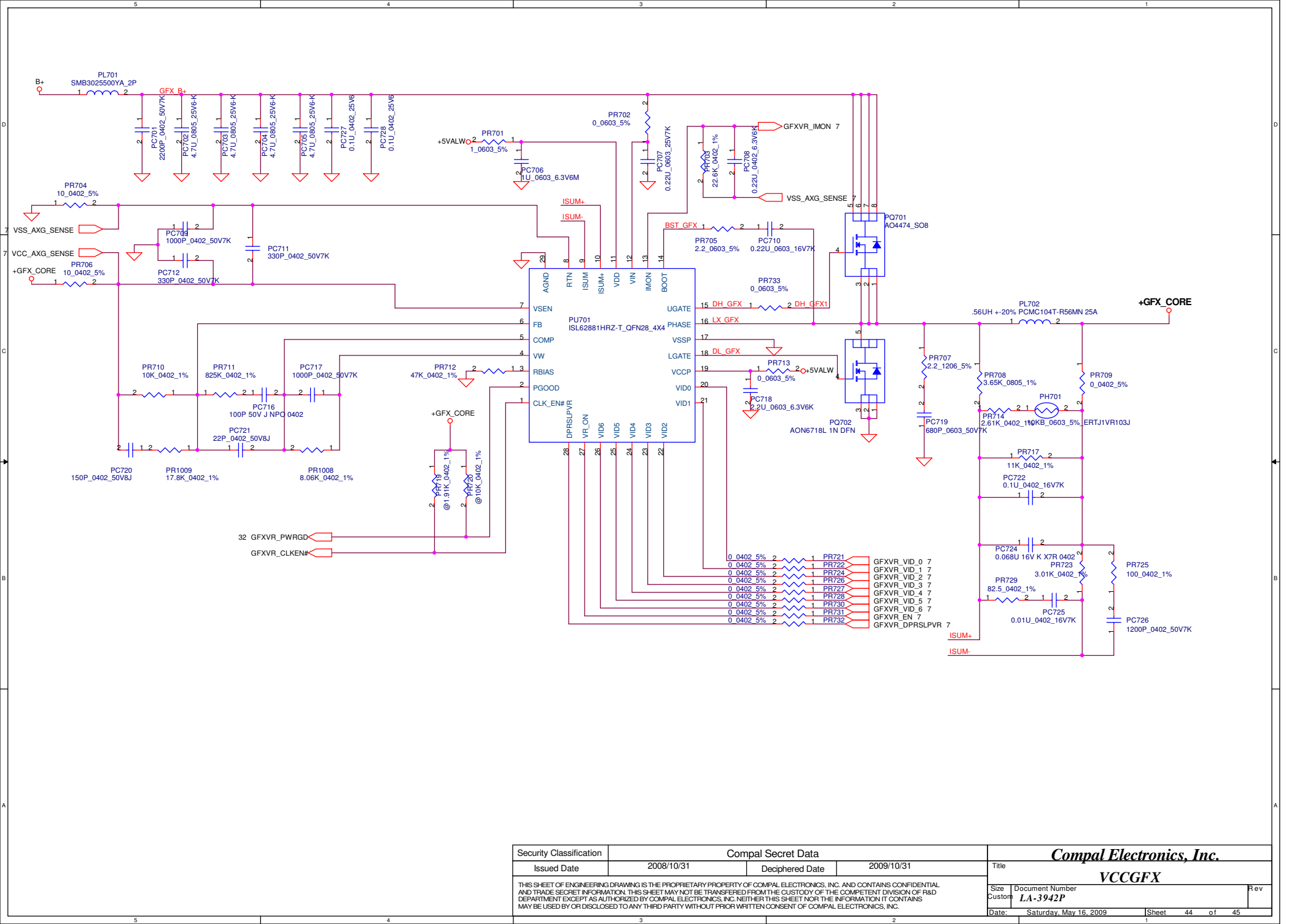


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