PCB STACK UP 8L

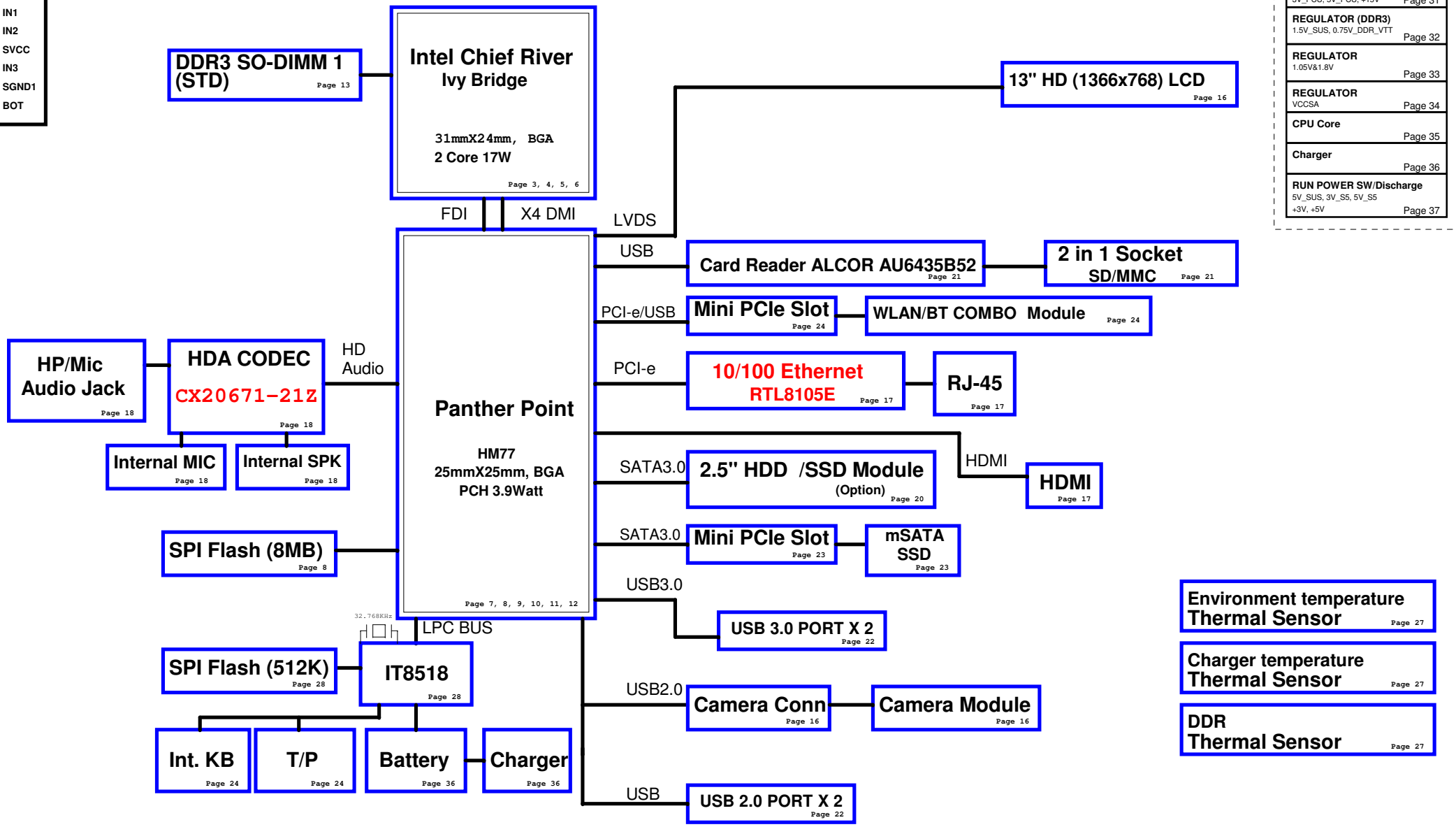
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT

LZ7 13" Block Diagram -- Intel Chief River UMA

01

POWER

DC/DC 3V_PCU, 5V_PCU, +15V	Page 31
REGULATOR (DDR3) 1.5V_SUS, 0.75V_DDR_VTT	Page 32
REGULATOR 1.05V&1.8V	Page 33
REGULATOR VCCSA	Page 34
CPU Core	Page 35
Charger	Page 36
RUN POWER SW/Discharge 5V_SUS, 3V_S5, 5V_S5 +3V, +5V	Page 37



PROJECT : LZ7
Quanta Computer Inc.
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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	16,32,34,35,36,37,39	MAIN POWER		S0~S5
+3V_RTC	+3.0V~+3.3V	7,8,11,28	RTC		S0~S5
3VPCU	+3.3V	8,16,19,25,28,29,32,33,34,38	IT8518/19 POWER	3V5V_EN	S0~S5
5VPCU	+5V	16,32,33,35,36,37,38,39	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
15V	15V	16,32,33,35	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	19,33	LAN POWER	LAN_ON	
5V_S5	+5V	11,22,33	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	3,7,8,9,10,11,24,33	Sys Management,PCH Resume Well, USB,WLAN,WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V		SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V		SLP_S4# CTRLD POWER	SUSON	S0~S3
1.5V_SUS	+1.5V	3,11,13,33,35	DDR3 SODIMM POWER	SUSON	S0~S3
+0.75V_DDR_VTT	+0.75V	7,11,16,17,18,20,27,33,34	DDR3 SODIMM REFERENCE POWER	MAINON	S0
+5V	+5V	16,32,34,35,36,37,39	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	3,7,8,9,10,11,13,15,16,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39	SLP_S3# CTRLD POWER	MAINON	S0
+VCC_GFX		5,39	VGA CORE POWER	MAINON	S0
VCCSA	+0.8V~+0.9V	**5,33,37**	Sandy Bridge Power	MAINON	S0
+1.8V	+1.8V	5,8,11,33,38	LVDS,NVM POWER	MAINON	S0
+1.05V	+1.05V	3,5,7,8,9,11,15,33,36	Sandy Bridge VTT POWER/PCH CORE POWER	MAINON	S0
+VCC_CORE		5,6,39	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	16	LCD Power	ENVDD	S0
+3V_HDD	+3V	20	ODD Power	ODD_5V_ON	S0
+5V_HDD	+5V	20	HDD Power	MAINON#	S0
BAT-V	+10V~+17V	34	MAIN BATTERY	CHG_PBATT	S0~S5
+1.5V_CPU	+1.5V	3,5,35	DDR3 1.5V Rails	PS_S3CNTRL	S0

PROJECT : LZ7

Quanta Computer Inc.

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Ivy Bridge Processor (DMI,PEG,FDI)

Ivy Bridge Processor (CLK,MISC,JTAG)

03

U22A

DMI_TXN0 7 → M2 DMI_RX#[0]
DMI_TXN1 7 → P6 DMI_RX#[1]
DMI_TXN2 7 → P1 DMI_RX#[2]
DMI_TXN3 7 → P10 DMI_RX#[3]
DMI_TXP0 7 → N3 DMI_RX[0]
DMI_TXP1 7 → P7 DMI_RX[1]
DMI_TXP2 7 → P3 DMI_RX[2]
DMI_TXP3 7 → P11 DMI_RX[3]
DMI_RXN0 7 → K1 DMI_TX#[0]
DMI_RXN1 7 → M8 DMI_TX#[1]
DMI_RXN2 7 → N4 DMI_TX#[2]
DMI_RXN3 7 → R2 DMI_TX#[3]
DMI_RXP0 7 → K3 DMI_TX[0]
DMI_RXP1 7 → M7 DMI_TX[1]
DMI_RXP2 7 → P4 DMI_TX[2]
DMI_RXP3 7 → T3 DMI_TX[3]

DMI

FDI_TXN0 7 → U7 FDI0_TX#[0]
FDI_TXN1 7 → W11 FDI0_TX#[1]
FDI_TXN2 7 → W1 FDI0_TX#[2]
FDI_TXN3 7 → AA6 FDI0_TX#[3]
FDI_TXN4 7 → W6 FDI1_TX#[0]
FDI_TXN5 7 → Y4 FDI1_TX#[1]
FDI_TXN6 7 → AC9 FDI1_TX#[2]
FDI_TXN7 7 → FDI1_TX#[3]
FDI_TXP0 7 → U6 FDI0_TX[0]
FDI_TXP1 7 → W10 FDI0_TX[1]
FDI_TXP2 7 → W3 FDI0_TX[2]
FDI_TXP3 7 → AA7 FDI0_TX[3]
FDI_TXP4 7 → W7 FDI1_TX[0]
FDI_TXP5 7 → T4 FDI1_TX[1]
FDI_TXP6 7 → AA3 FDI1_TX[2]
FDI_TXP7 7 → AC8 FDI1_TX[3]
FDI_FSYNC0 7 → AA11 FDI0_FSYNC
FDI_FSYNC1 7 → AC12 FDI1_FSYNC
FDI_INT 7 → U11 FDI_INT
FDI_LSYNC0 7 → AA10 FDI0_LSYNC
FDI_LSYNC1 7 → AG8 FDI1_LSYNC

Intel(R) FDI

eDP_COMP → AF3 eDP_COMPIO
eDP_HPD# → AD2 eDP_ICOMPO
AG11 eDP_HPD
AG4 eDP_AUX#
AF4 eDP_AUX
AC1 eDP_TX[0]
AA4 eDP_TX[1]
AE10 eDP_TX[2]
AE6 eDP_TX[3]
AC3 eDP_TX#[0]
AC4 eDP_TX#[1]
AE11 eDP_TX#[2]
AE7 eDP_TX#[3]

DP

IC,SNB_2CBGA,1P0

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI G3 → PEG_COMP
PEG_ICOMPO G1
PEG_RCOMPO G4

PEG_COMP connect to PIN G3&G4 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN G1 W:12mils/S:15mils/L: 500mils.

PEG_RX[0] H22
PEG_RX#[1] J21
PEG_RX#[2] B22
PEG_RX#[3] D21
PEG_RX#[4] A19
PEG_RX#[5] D17
PEG_RX#[6] B14
PEG_RX#[7] D13
PEG_RX#[8] A11
PEG_RX#[9] B10
PEG_RX#[10] G8
PEG_RX#[11] A8
PEG_RX#[12] B6
PEG_RX#[13] H8
PEG_RX#[14] E5
PEG_RX#[15] K7

PEG_RX[0] K22
PEG_RX[1] K19
PEG_RX[2] C21
PEG_RX[3] D19
PEG_RX[4] C19
PEG_RX[5] D16
PEG_RX[6] C13
PEG_RX[7] D12
PEG_RX[8] C11
PEG_RX[9] C9
PEG_RX[10] F8
PEG_RX[11] C8
PEG_RX[12] C5
PEG_RX[13] H6
PEG_RX[14] F6
PEG_RX[15] K6

PEG_TX#[0] G22
PEG_TX#[1] C23
PEG_TX#[2] D23
PEG_TX#[3] F21
PEG_TX#[4] H19
PEG_TX#[5] C17
PEG_TX#[6] K15
PEG_TX#[7] F17
PEG_TX#[8] F14
PEG_TX#[9] A15
PEG_TX#[10] J14
PEG_TX#[11] H13
PEG_TX#[12] M10
PEG_TX#[13] F10
PEG_TX#[14] D9
PEG_TX#[15] J4

PEG_TX[0] F22
PEG_TX[1] A23
PEG_TX[2] D24
PEG_TX[3] E21
PEG_TX[4] G19
PEG_TX[5] B18
PEG_TX[6] K17
PEG_TX[7] G17
PEG_TX[8] E14
PEG_TX[9] C15
PEG_TX[10] K13
PEG_TX[11] G13
PEG_TX[12] K10
PEG_TX[13] G10
PEG_TX[14] D8
PEG_TX[15] K4

eDP_COMP connect to PIN AF3 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN AD2 W:12mils/S:15mils/L: 500mils.

EC-A-23

U22B

MISC

8 PROC_SELECT# → F49 PROC_SELECT#
SNB_IVB# N.A at SNB EDS #27637 0.7v1
TP48 SKTOCC# → C57 PROC_DETECT#

THERMAL

TP45 TP_CATERR# → C49 CATERR#
10,28 EC_PECI → A48 PECI
28,39 H_PROCHOT# R459 56.2/F_4 H_PROCHOT#_R → C45 PROCHOT#
10 PM_THRMTRIP# R457 *0_4@SHORT PM_THRMTRIP#_R → D45 THERMTRIP#

PWR MANAGEMENT

7 PM_SYNC R462 *0_4@SHORT PM_SYNC_R → C48 PM_SYNC
10 H_PWRGOOD R460 *0_4@SHORT H_PWRGOOD_R → B46 UNCOREPWRGOOD
R461 10K/F_4
PM_DRAM_PWRGD_R BE45 SM_DRAMPWROK
CPU_PLTRST#_R D44 RESET#

IC,SNB_2CBGA,1P0

CPU RESET#

9,19,21,24 PLTRST#
U13 74LVC1G07GW: GND OUT 3, IN 2, NC 1, VCC 5
+1.05V
R456 *75_4
CPU_PLTRST# 4 → R455 *43_4 → CPU_PLTRST#_R
3V_S5 → C468 *0.1U/10V/X7R_4
R454 750/F_4
R453 1.5K/F_4

CLOCKS

BCLK J3 / BCLK# H2 → CLK_CPU_BCLKP 9 / CLK_CPU_BCLKN 9
R447 1K_4
*0_4P2R_04 RP7
DPLL_REF_CLK AG3 / DPLL_REF_CLK# AG1 → CLK_DPLL_SSCLKP_R / CLK_DPLL_SSCLKN_R
CLK_DPLL_SSCLKP 9 / CLK_DPLL_SSCLKN 9
BCLK_ITP N59 / BCLK_ITP# N58 → BCLK_ITP TP57 / BCLK_ITP# TP56
R448 1K_4 +1.05V

EC-A-23

DDR3 MISC

SM_DRAMRST# AT30 → CPU_DRAMRST#
SM_RCOMP[0] BF44 → SM_RCOMP_0 R237 140/F_4
SM_RCOMP[1] BE43 → SM_RCOMP_1 R229 26.1/F_4
SM_RCOMP[2] BG43 → SM_RCOMP_2 R234 200/F_4

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

JTAG & BPM

PRDY# N53 → XDP_PRDY# TP53
PREQ# N55 → XDP_PREQ# TP52
CPU XDP
TCK L56 → XDP_TCLK TP51
TMS L55 → XDP_TMS TP50
TRST# J58 → XDP_TRST# TP62
TDI M60 → XDP_TDI TP60
TDO L59 → XDP_TDO TP54
R472 *1K/F_4 +3V
DBR# K58 → XDP_DBRST# TP49 / XDP_DBRST# 7
BPM[0] G58 → XDP_BPM0 TP49
BPM[1] E55 → XDP_BPM1 TP46
BPM[2] E59 → XDP_BPM2 TP63
BPM[3] G55 → XDP_BPM3 TP47
BPM[4] G59 → XDP_BPM4 TP61
BPM[5] H60 → XDP_BPM5 TP58
BPM[6] J59 → XDP_BPM6 TP55
BPM[7] J61 → XDP_BPM7 TP59

SM_DRAMPWROK Processor Input.

3V_S5
C470 *0.1U/10V/X7R_4
+1.5V_CPU
R481 200/F_4
7 SYS_PWROK
7 PM_DRAM_PWRGD
R477 *0_4
U23 74AHC1G09
PM_DRAM_PWRGD_Q
R480 130/F_4 → PM_DRAM_PWRGD_R
R478 0_4
R482 39_4
Q38 ME2N7002E
PM_DRAM_PWRGD_Q
R479 *3K/F_4
MAINON# 33

EC-A-24

DDR3 DRAM RESET

1.5V_SUS
R445 1K/F_4
R440 *0_4
13 DDR3_DRAMRST#
R444 1K/F_4
CPU_DRAMRST#
FOR DEEP S3
28 DRAMRST_CNTRL_EC
R446 *0_4
Q30 2N7002
9 DRAMRST_CNTRL_PCH
R443 0_4
R442 4.99K/F_4
13 DRAMRST_CNTRL_DDR
C440 0.047U/10V/X7R_4
EC-B-01

1.5V_SUS 11,13,33,35
+1.05V 5,7,8,9,11,33,36
+1.5V_CPU 5,35
3V_S5 7,8,9,10,11,18,24,29,33
+3V 7,8,9,10,11,13,16,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39

DP & PEG Compensation

+1.05V R206 *10K_4 eDP_HPD#
+1.05V R449 24.9/F_4 eDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

+1.05V R450 24.9/F_4 PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)

+1.05V

H_PROCHOT#	R458	62_4
XDP_TDO	R473	51/F_4
XDP_TMS	R239	51/F_4
XDP_TDI	R471	51/F_4
XDP_PREQ#	R242	*51/F_4
XDP_TCLK	R240	51/F_4
XDP_TRST#	R474	51/F_4

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Quanta Computer Inc.

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	Custom SNB 1/4 (PCIE&DMI&FDI)	1A
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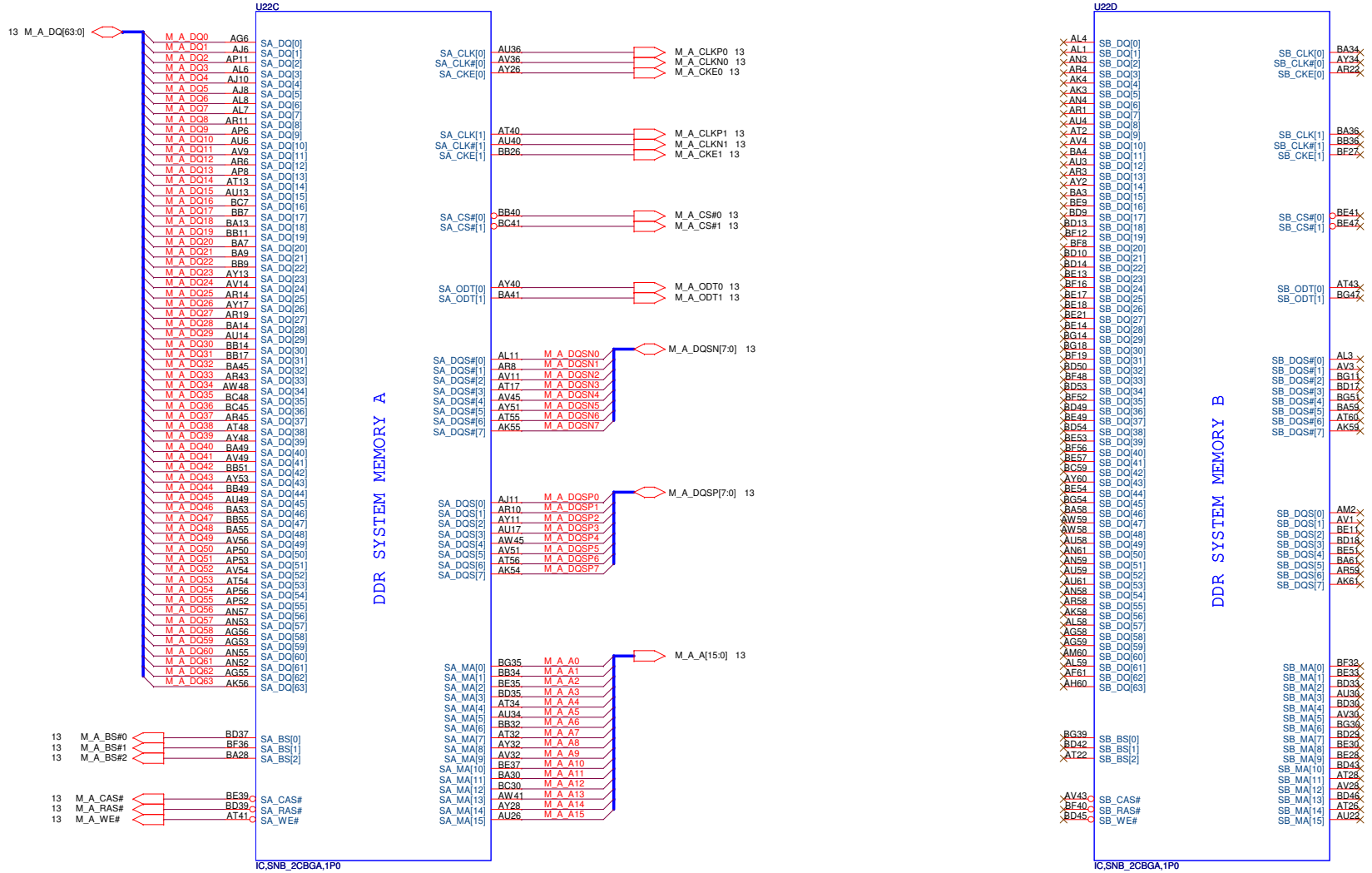
Ivy Bridge Processor (DDR3)



PROJECT : LZ7

Quanta Computer Inc.

Size	Document Number	Rev
	Custom SNB 2/4 (DDR3 I/F)	1A
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Ivy Bridge Processor (POWER)

330uF locate power side

8.5A

CPU Core Power

SNB-21.5A, IVY-33A@ VCC_CORE

+VCC_CORE

U22F

POWER

CORE SUPPLY

PEG AND DDR

3.3V_SUS?(PDDG p127)

QUIET RAILS

SVID

SENSE LINES

IC,SNB_2CBGA,1P0

Ivy Bridge Processor (GRAPHIC POWER)

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

05

SNB-21.5A, IVY-33A@ VCC GFX

+VCC_GFX

U22G

POWER

GRAPHICS

DDR3 - 1.5V RAILS

SENSE LINES

1.8V RAIL

QUIET RAILS

1.2A

SNB:6A

SA RAIL

EC-A-18

5A

SNB_IVB# N.A at SNB EDS #27637 0.7v1

If +1.5V_CPU will be implemented, have to change the two divided resistor as 100-ohm 1%

IC,SNB_2CBGA,1P0

SVID CLK

Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to VR

SVID DATA

Place PU resistor close to CPU

Place PU resistor close to VR

SVID ALERT

Place PU resistor close to CPU

PROJECT : LZ7

Quanta Computer Inc.

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	Custom SNB 3/4 (POWER)	1A
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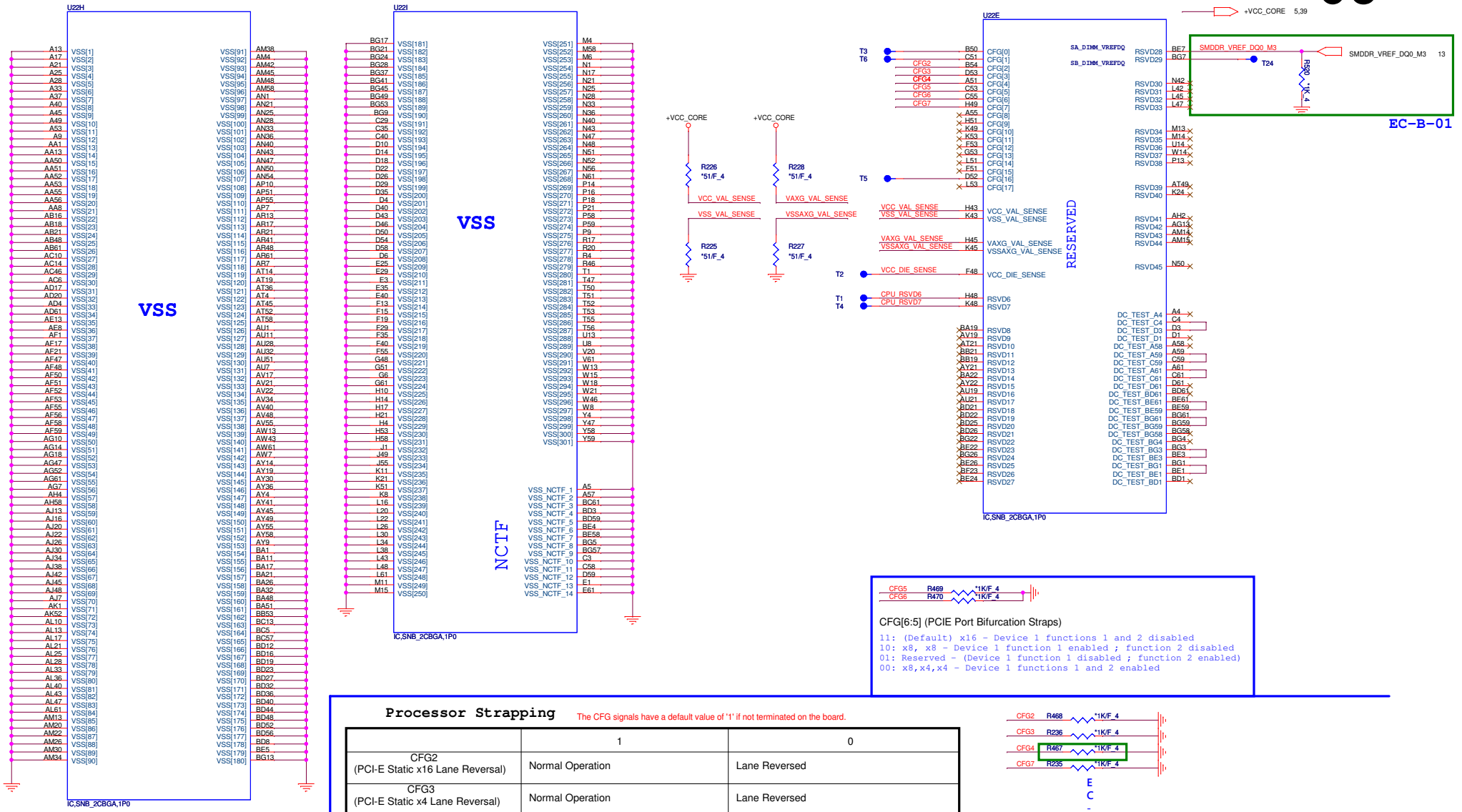
Ivy Bridge Processor (GND)

Ivy Bridge Processor (RESERVED, CFG)

06



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

EC-A-24

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Quanta Computer Inc.

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Cougar Point/Panther Point (DMI,FDI,PM)

Cougar Point/Panther Pointt (LVDS,DDI)

07

U19C

U19D

Layout note:
AC coupling capacitors of DP are placed on near connector

FOR DEEP S3

CougarPoint_R1P0

PCH Pull-high/low(CLG)

System PWR_OK(CLG)

INT HDMI DETECT

DPWROK FOR DSW (DEEP S3)

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

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Quanta Computer Inc.
PCH 1/6 (DMI/FDI/VIDEO)
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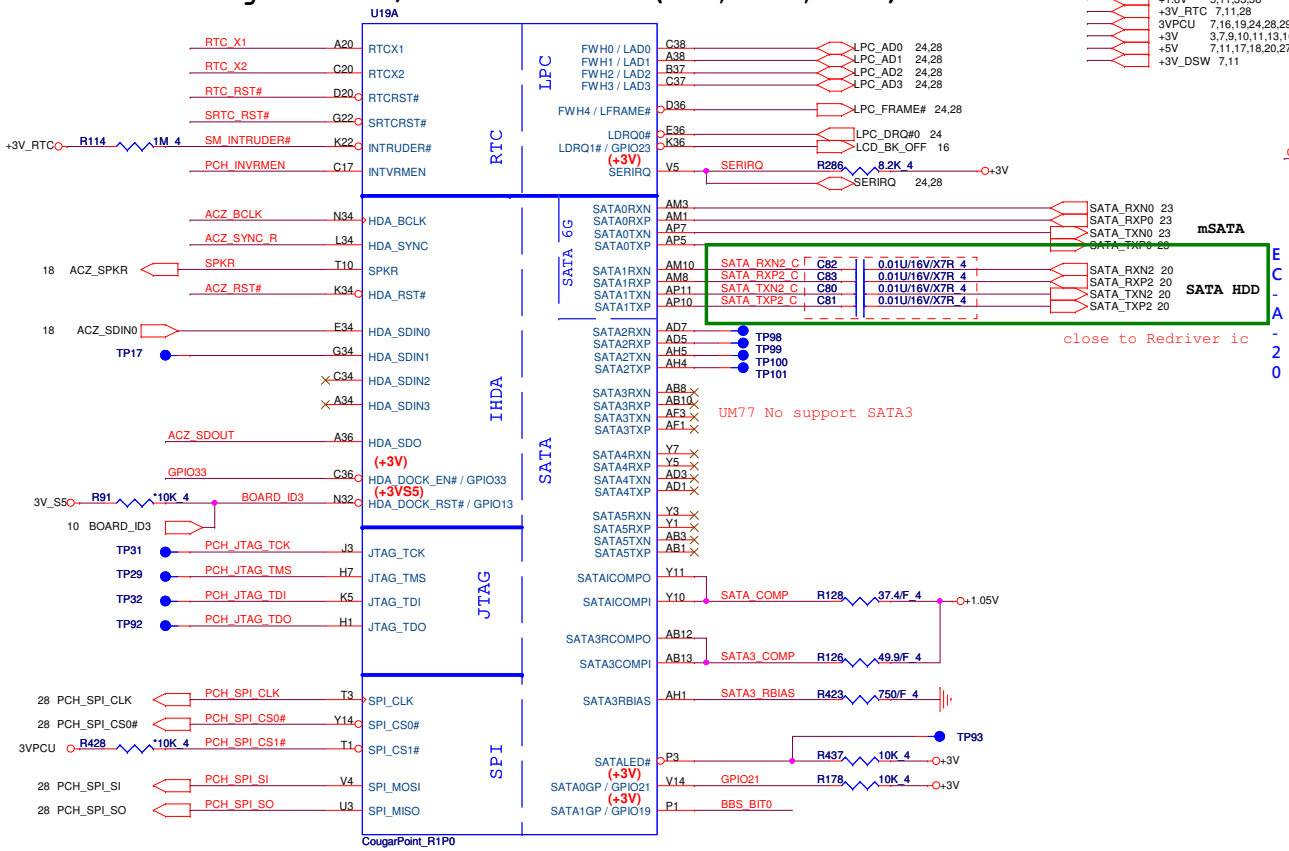
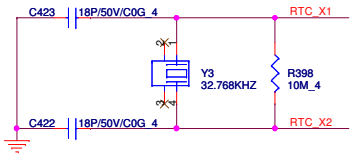
Cougar Point/Panther Point (HDA,JTAG,SATA)



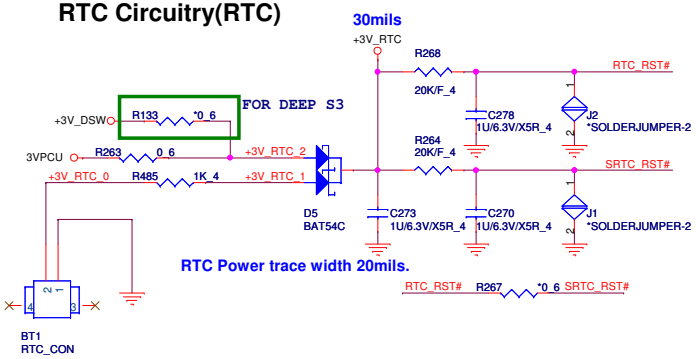
+1.05V 3,5,7,9,11,33,36
+1.8V 5,11,33,38
+3V_RTC 7,11,28
3VPCU 7,16,19,24,28,29,32,33,34,38
+3V 3,7,9,10,11,13,16,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39
+5V 7,11,17,18,20,27,33,34
+3V_DSW 7,11

RTC Clock 32.768KHz



08

RTC Circuitry(RTC)

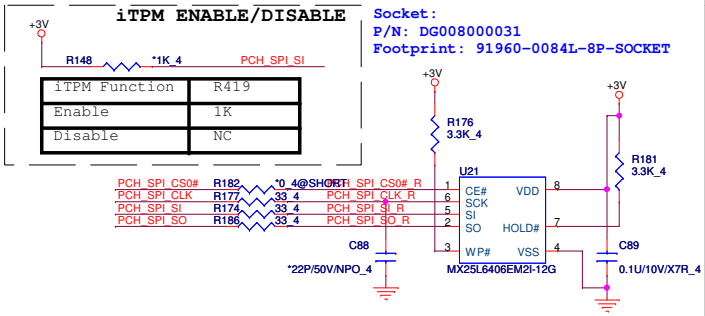


W25Q64CVSSIG: AKE3EFP0N04
MX25L6406EM2I-12G: AKE3NFP0Z00
EN25Q64-104HIP: AKE3EFN0Q00

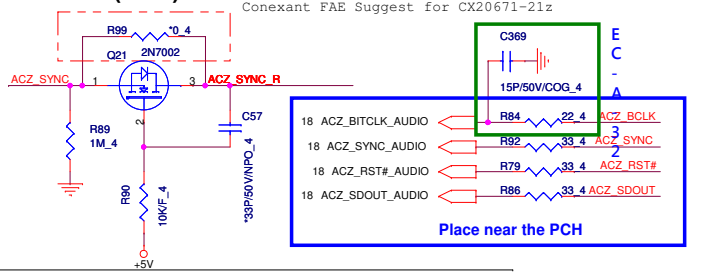
PCH Dual SPI

64Mbit (8M Byte), SPI

Socket:
P/N: DG008000031
Footprint: 91960-0084L-8P-SOCKET



HDA Bus(CLG)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R168 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V R26 *1K_4 R23 *10K_4 PCI_GNT3# 9
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R399 330K_4 +3V_RTC
HDA_SDO	Flash Descriptor Security Only for Interposer	PWROK	0 = effective(Default: weak pull down) 1 = Override	ACZ_SDOUT R87 *1K_4 3V_S5
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1 0 / GNT0# 1 0 / Boot Location SPI LPC	[Need external pull-down for LPC BIOS] R429 *1K_4 R28 *1K_4 BBS_BIT0 BBS_BIT1 9
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
DF_TVS	DMI Termination voltage IVY:0 SANDY:1	PWROK	weak pull-down 20kohm	R416 2.2K_4 +1.8V; 3 PROC_SELECT# R415 1K_4 DF_TVS 10
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_S5 R85 1K_4 ACZ_SYNC_R
GPIO15	Intel ME Crypto Transport Layer Security cipher suite		Low = Disable (Default) High = Enable	10 HOST_ALERT#1_R HOST_ALERT#1_R R432 1K_4 3V_S5
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R167 *1K_4 PLL_ODVR_EN 10
DSWVREN	0: disable 1: enable			

if default boot destination is SPI,
no external pull-up/-down resistors on the board are necessary

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Quanta Computer Inc.
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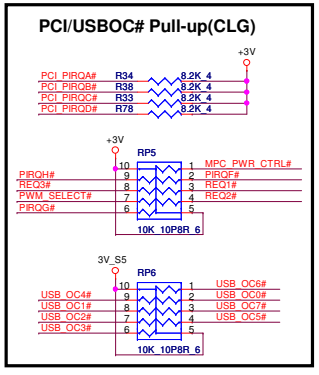
Cougar Point/Panther Point (PCI,USB,NVRAM)

Cougar Point/Panther Point (PCI-E,SMBUS,CLK)

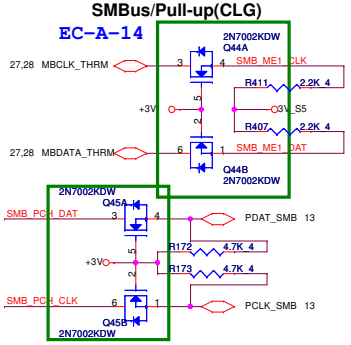
09

PCI/USBOC# Pull-up(CLG)

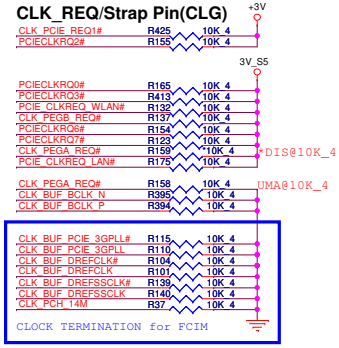


SMBus/Pull-up(CLG)

EC-A-14



CLK_REQ/Strap Pin(CLG)



PCIE Clock

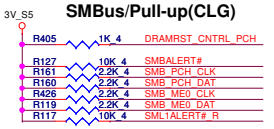
Layout note:
PCIE_CLKREQ_LAN# layout adjacent
to CLK_PEGA_REQ#

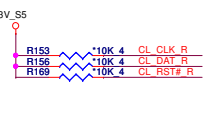
MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R43 *1K_4

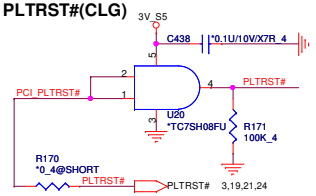
3V_S5 3,7,8,10,11,18,24,29,33
+3V 3,7,8,10,11,13,16,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39

SMBus/Pull-up(CLG)





PLTRST#(CLG)



Size	Document Number	Rev
	PCH 3/6 (PCIE/USB/CLK)	1A
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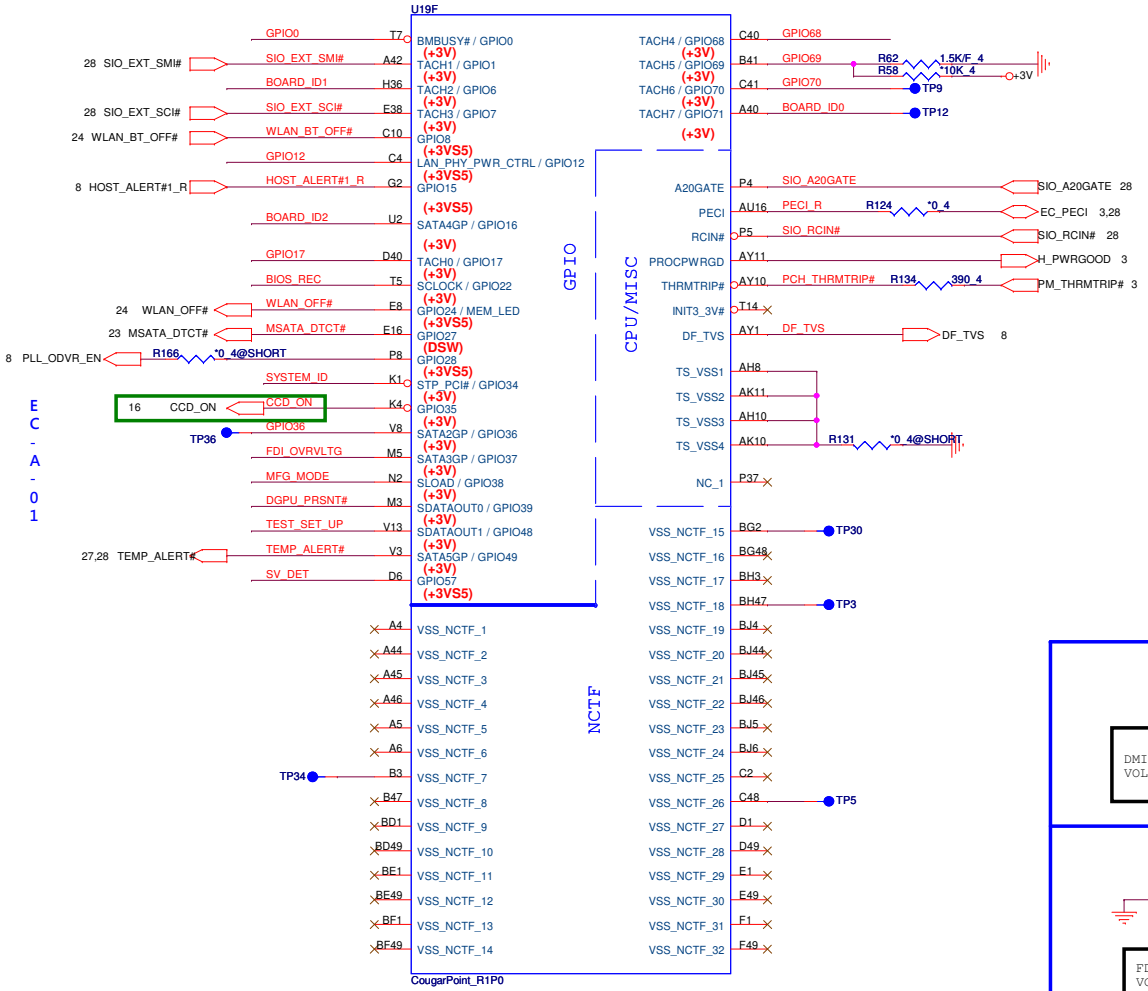
PROJECT:LZ7
Quanta Computer Inc.

Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

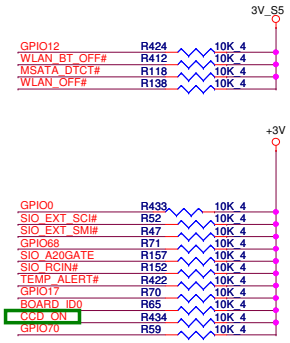


E C - A - 0 1

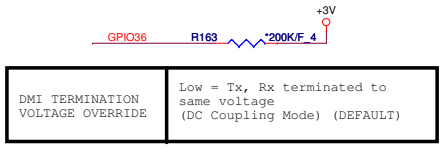
3V_S5 3,7,8,9,11,18,24,29,33
+3V 3,7,8,9,11,13,16,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39

10

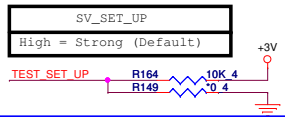
GPIO Pull-up/Pull-down(CLG)



E C - A - 0 1

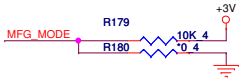


DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

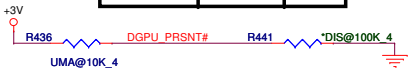


FDI TERMINATION VOLTAGE OVERRIDE	LOW = Tx, Rx terminated to same voltage

MFG-TEST



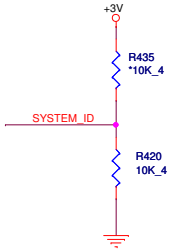
	Optimus	UMA
Stuff	R1566	R1565
No Stuff	R1565	R1566

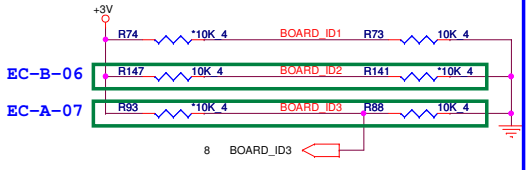


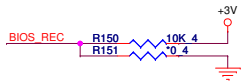
BOARD ID SETTING

Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV			
SIV			
SIT	0	1	0
SVT			
SOVP			

	SYSTEM_ID
LZ7	0
LZ8	1







BIOS RECOVERY	High = Disable (Default) Low = Enable

PROJECT : LZ7

Quanta Computer Inc.

Size	Document Number	Rev
	PCH 4/6 (GPIO/MISC)	1A

Date: Wednesday, December 21, 2011 Sheet 10 of 42

Cougar Point/Panther Point (POWER)

COUGAR POINT (POWER)

U19J — POWER

U19G — POWER

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | MISC | CPU | RTC | HDA

VCC CORE | LVDS | CRT | HVCMOS | DMI | VCCIO | DFT / SPI | FDI

FOR DEEP S3

EC-A-12

EC-A-34

EC-B-15

1.01A (60mils)

1.3 A (60mils)

2.925 A (140mils)

119mA (20mils)

119mA (15mils)

266mA (20mils)

160mA (15mils)

160mA (20mils)

3mA (10mils)

1mA (10mils)

60mA (10mils)

42mA (10mils)

190 mA (15mils)

20mA (10mils)

80mA (40mils)

55mA (10mils)

95mA (10mils)

10mA (10mils)

V_PROC_IO=1mA (10mils)

VCCRTC<1mA (10mils)

VCC5REFSUS=1mA

V5REF= 1mA

CougarPoint_R1P0

+3V_RTC	7,8,28
3V_S5	3,7,8,9,10,18,24,29,33
+3V	3,7,8,9,10,13,16,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39
5V_S5	22,25,33
+5V	7,8,17,18,20,27,33,34
+1.05V	3,5,7,8,9,33,36
1.5V_SUS	3,13,33,35
+1.8V	5,8,33,38
+3V_DSW	7,8

PROJECT : LZ7

Quanta Computer Inc.

Size	Document Number	Rev
	PCH 5/6 (POWER)	1A

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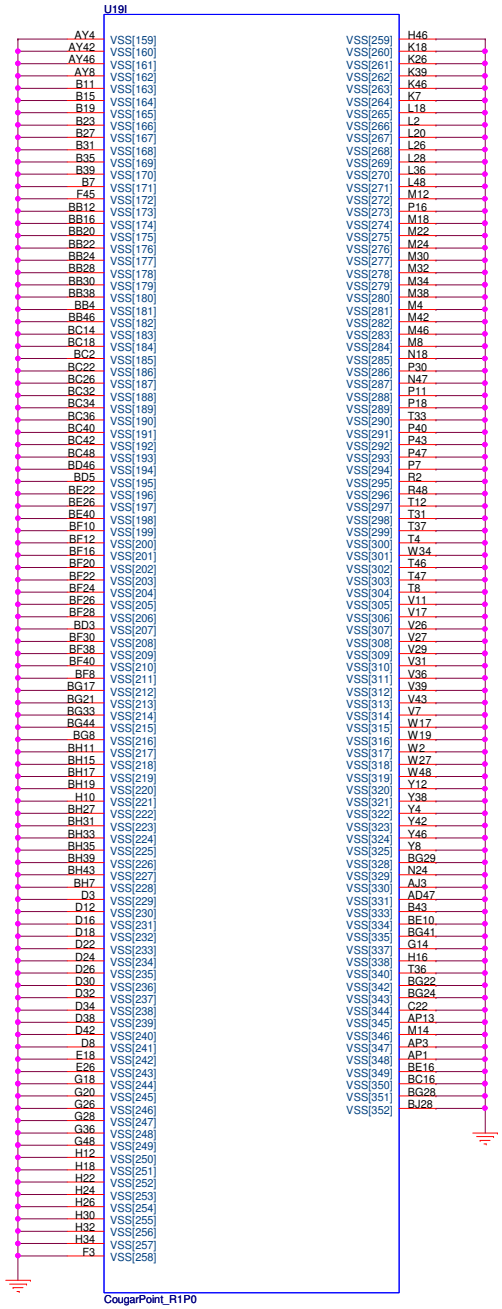
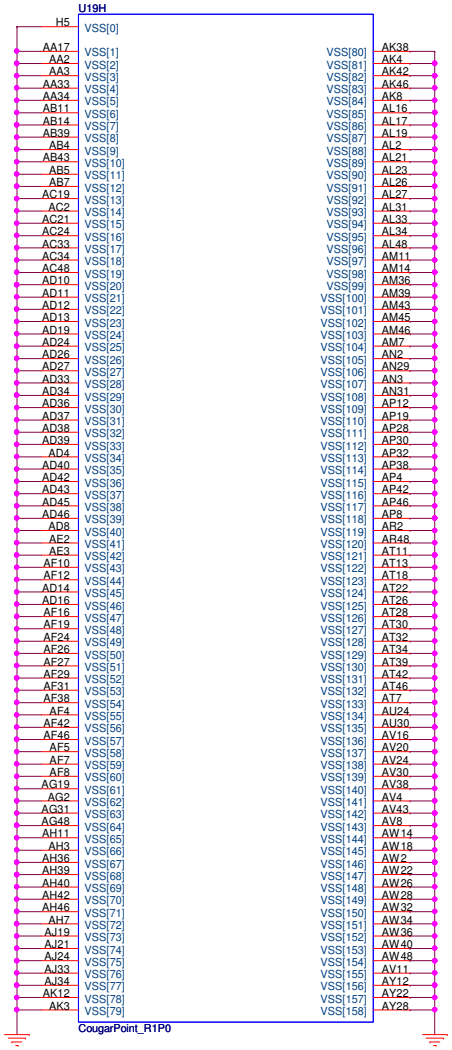
Cougar Point/Panther Point (GND)



Cougar Point/Panther Point (GND)



PROJECT : LZ7

Quanta Computer Inc.

Size	Document Number	Rev
	PCH 6/6 (GND)	1A

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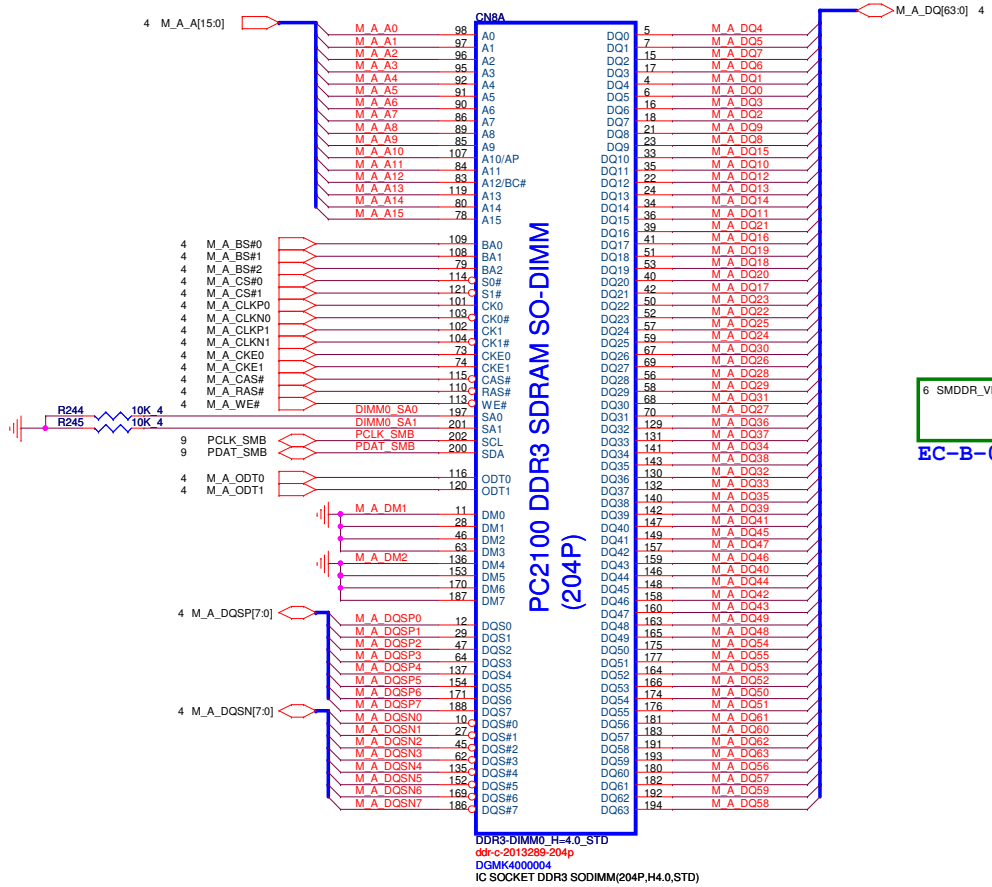
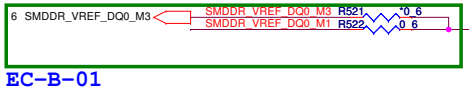
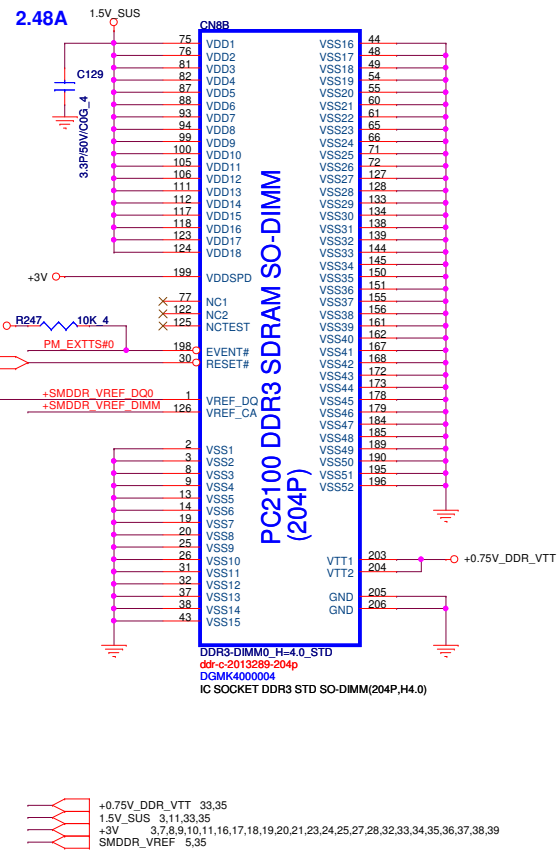
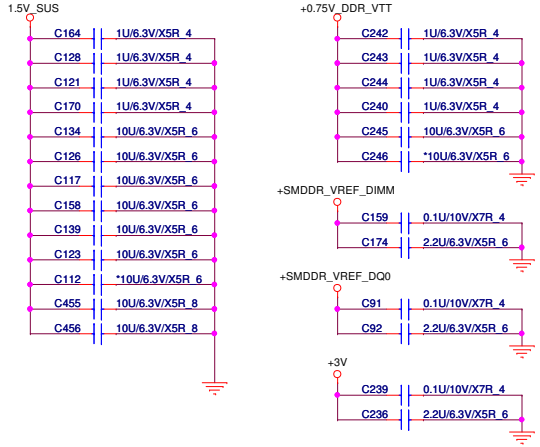


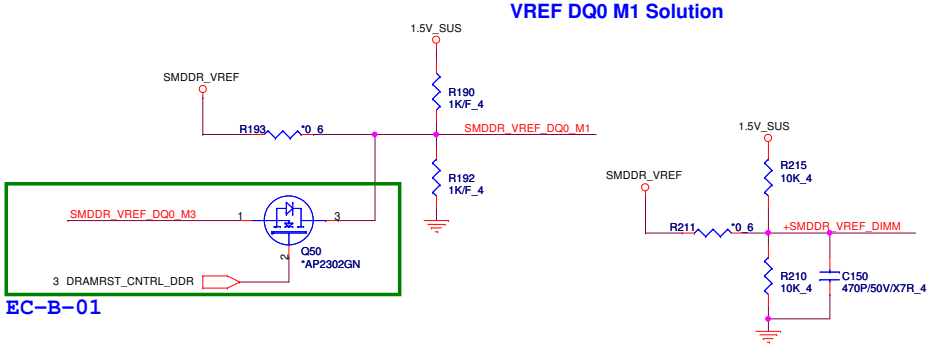




Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution



PROJECT : LZ7

Quanta Computer Inc.

Size	Document Number	Rev
	Custom DDR3 DIMM0-STD (5.2H)	1A
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EC-A-22

PROJECT : LZ7

Quanta Computer Inc.

Size	Custom	Document Number	Rev
		Blank	
Date:	Wednesday, December 21, 2011	Sheet 15 of 42	

+3V 3,7,8,9,10,11,13,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39
3VPCU 7,8,19,24,28,29,32,33,34,38
15V 32,33,35
+5V 7,8,11,17,18,20,27,33,34
VIN 32,34,35,36,37,39
5VPCU 32,33,35,36,37,38,39

LCDVCC

15V, +3V, +LCDVCC
R46 330K_4
Q8 AO3404
R27 22_8
C2 10U/6.3V/X5R_8
LCDVCC_ON
C27 0.027U/25V/X7R_6
Q6 2N7002W
Q7 2N7002W
5VPCU
R39 100K_4
Q1 PDTC144EU
7 INT_DISP_ON
R16 10K_4

Back light

3VPCU, +3V
R11 10K_4
R13 *4.7K_4
28,29 LID#
D1 RB500V-40
D2 RB500V-40
DISPON
SC1 *0.1U/10V/X7R_4
C1 0.1U/10V/X7R_4
For ESD
R29 100K_4
C14 *47P/50V/NPO_4
7 INT_LVDS_BLON
R19 2.2K_4
R18 10K_4
C5 *1U/10V/X5R_6
Q2 PDTC144EU
LCD_BK_OFF 8

For ESD

SC4 *0.1U/10V/X7R_4
C10 2.2U/6.3V/X5R_6
CN2
+LCDVCC
+3V
7 LVDS_DDC_SCL
7 LVDS_DDC_SDA
LVDS_DDC_SCL
LVDS_DDC_SDA
7 INT_TXLOUTN0
7 INT_TXLOUTP0
INT_TXLOUTN0
INT_TXLOUTP0
7 INT_TXLOUTN1
7 INT_TXLOUTP1
INT_TXLOUTN1
INT_TXLOUTP1
7 INT_TXLOUTN2
7 INT_TXLOUTP2
INT_TXLOUTN2
INT_TXLOUTP2
7 INT_TXLCLKN
7 INT_TXLCLKP
INT_TXLCLKN
INT_TXLCLKP
28 IMG_EN
28 DCR_EN
IMG_EN
DCR_EN
VADJ_PWM
DISPON
GFX_PWR_SRC
LVD-A30SFYG+

EC-B-02

EC-A-21

+3V
R41 2.2K_4
R42 2.2K_4
LVDS_DDC_SDA
LVDS_DDC_SCL

+3V
C26 *47P/50V/NPO_4
C25 *47P/50V/NPO_4
close to CN2

Camera Conn

+CAM_VCC
USBP2- R
USBP2+ R
CN4
VCC_3V
D-
D+
GND
GND_SHIELD
G1
G2
CAMERA_CONN

For EMI

INT_TXLCLKN
INT_TXLCLKP
C29 6.8P/50V/NPO_4
C30 6.8P/50V/NPO_4

LVDS_DDC_SCL
LVDS_DDC_SDA
C23 *2200P/50V/X7R_4
C24 *2200P/50V/X7R_4
For EMI

9 USBP2-
9 USBP2+
CML1 DLW21HN900SQ2L
USBP2- R
USBP2+ R
FOR ESD
U1 AZC002-02N.R7G
IO1 VIN
IO2 GND
+CAM_VCC
EC-A-13
EC-B-03
EC-A-38

CAMERA VCC Control

+3V
R502 10K_4
R503 10K_4
Q41 AOS3413
Close to Q41 pin1
RV11 TVM0G140M900R
R504 *0_6
+CAM_VCC
10 CCD_ON
Q42 PDTC144EU
RV12 TVM0G140M900R
C505 2200P/50V/X7R_6
C506 1U/6.3V/X5R_4
C507 0.1U/10V/X7R_4

EC-B-11

EC-A-01

7 INT_DPST_PWM
28 EC_DPST_PWM
R383 *0_4
R523 0_4
VADJ_PWM
C409 *47P/50V/NPO_4
EC-B-05

GFX_PWR_SRC
C412 0.1U/25V/X7R_6
C413 0.1U/25V/X7R_6
C4 *10U/25V/X6S_12
R15 *0_8@SHORT
VIN

EC-A-21

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Quanta Computer Inc.
Size
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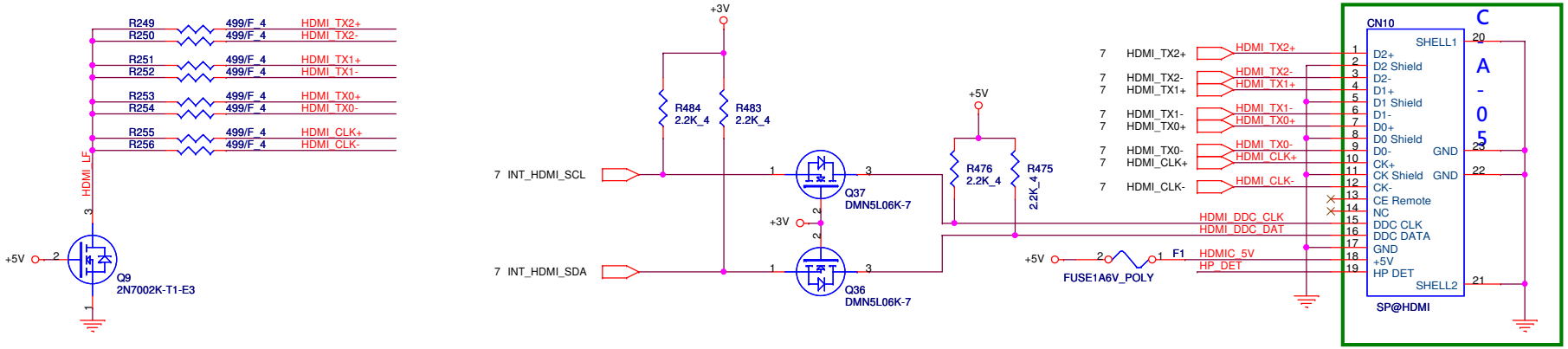
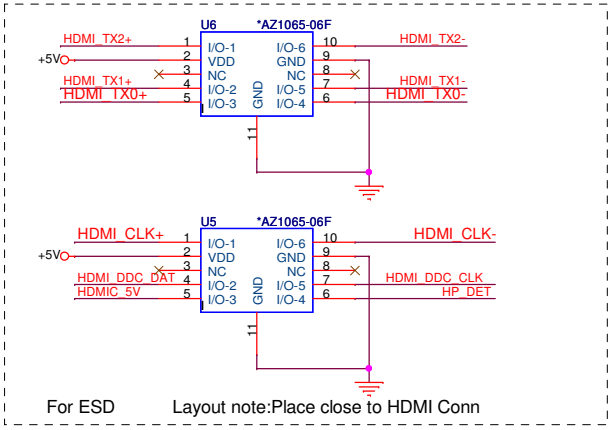
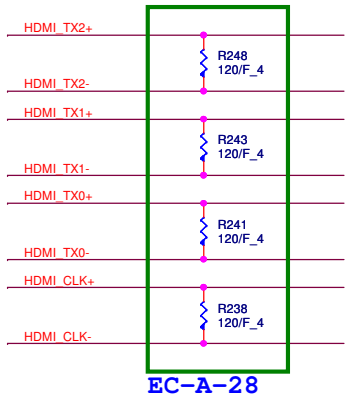
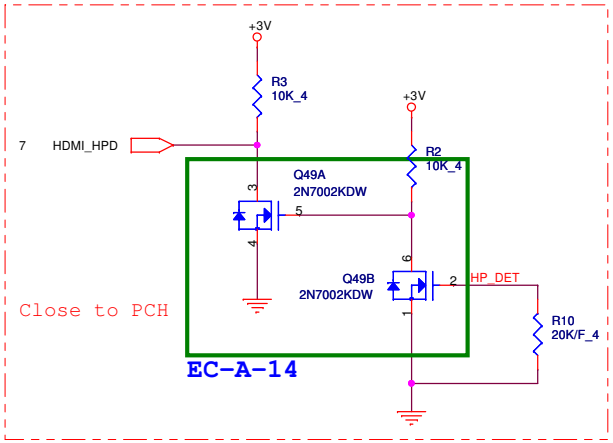
3,7,8,9,10,11,13,16,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39 +3V
7,8,11,18,20,27,33,34 +5V

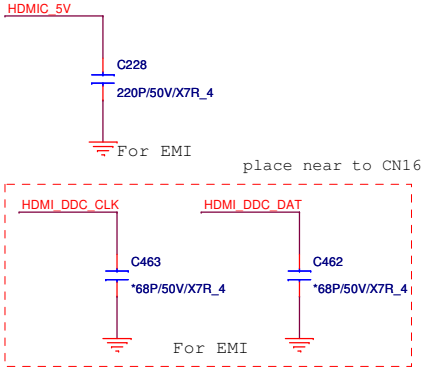




EMI reserve for HDMI







PROJECT : LZ7

Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> HDMI CONN	1A
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Note:
To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 pins must be powered by a rail that is not removed unless AC power is removed.

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.

Conexant FAE Suggest when use intel HDA interface

Mount R370 (20K) Vendor suggestion

HD Audio Bus

DIGITAL_MIC

For ESD reserved

For EMI

For RF

From EC

INT Speaker

PC BEEP CONTROL

From EC

From SB

EMI Reserved

ESD Reserved

Port Configuration

Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal analog mono or stereo MIC.
Port C: Microphone jack
Port G: Internal stereo speakers
Port J: Optional Internal stereo digital mic
Port H: S/PDIF (jack shared with headphone)

Option Only

Shared phone Mbg / combo

EC-A-02

EC-A-30

EC-A-36

PROJECT : LZ7	Quanta Computer Inc.
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Rev	3A
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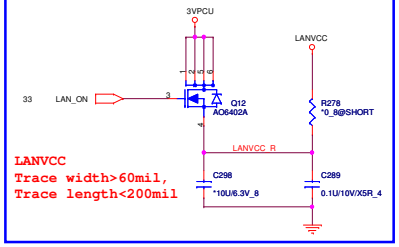
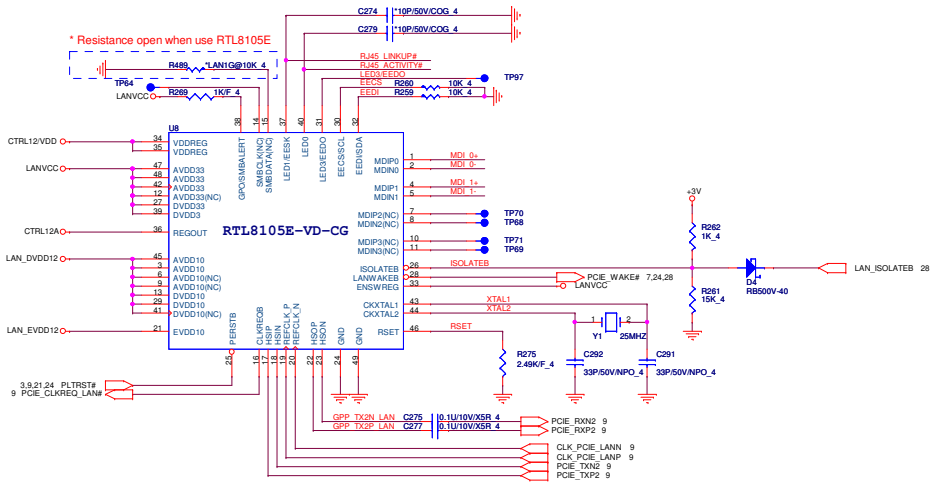
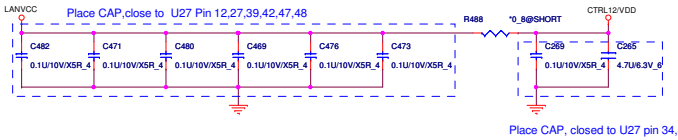
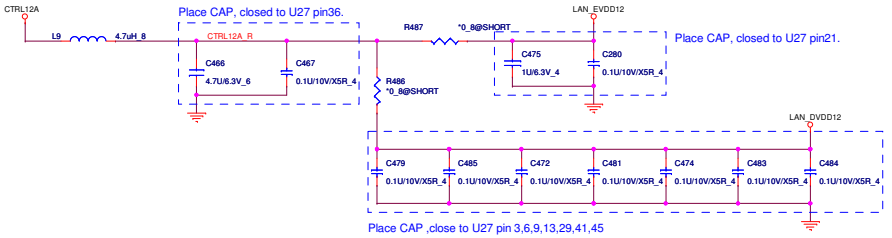
LANVCC



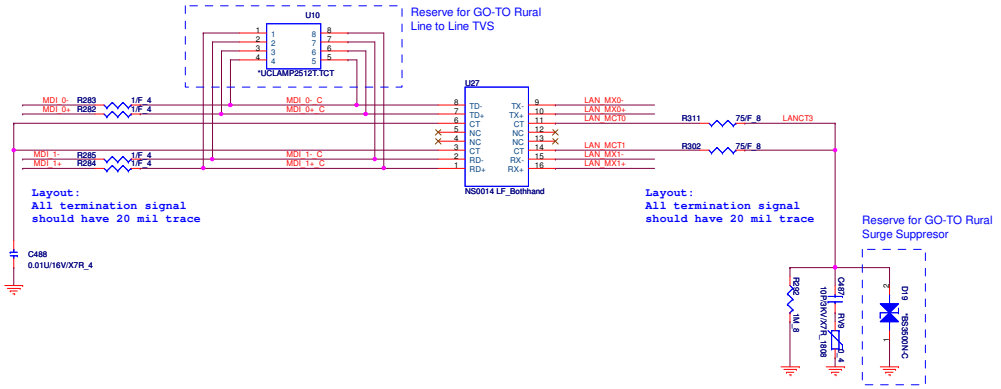
7,8,16,24,28,29,32,33,34,38 3VPCU
33 LANVCC
3,7,8,9,10,11,13,16,17,18,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39 +3V



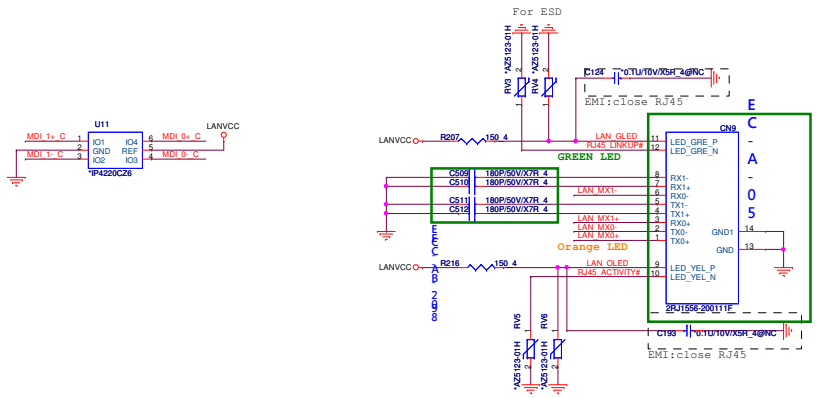




Tramsformer



RJ45 Connector



PROJECT : LZ7

Quanta Computer Inc.

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Custom	LAN[RTL8105E]	1A

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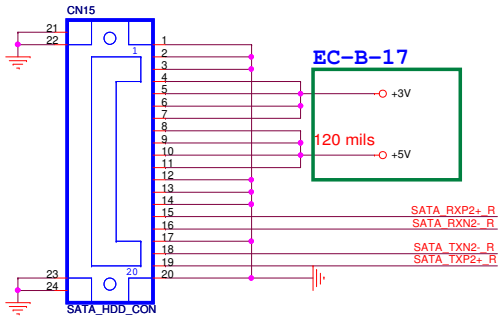
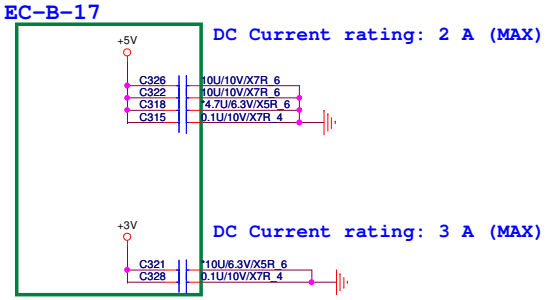
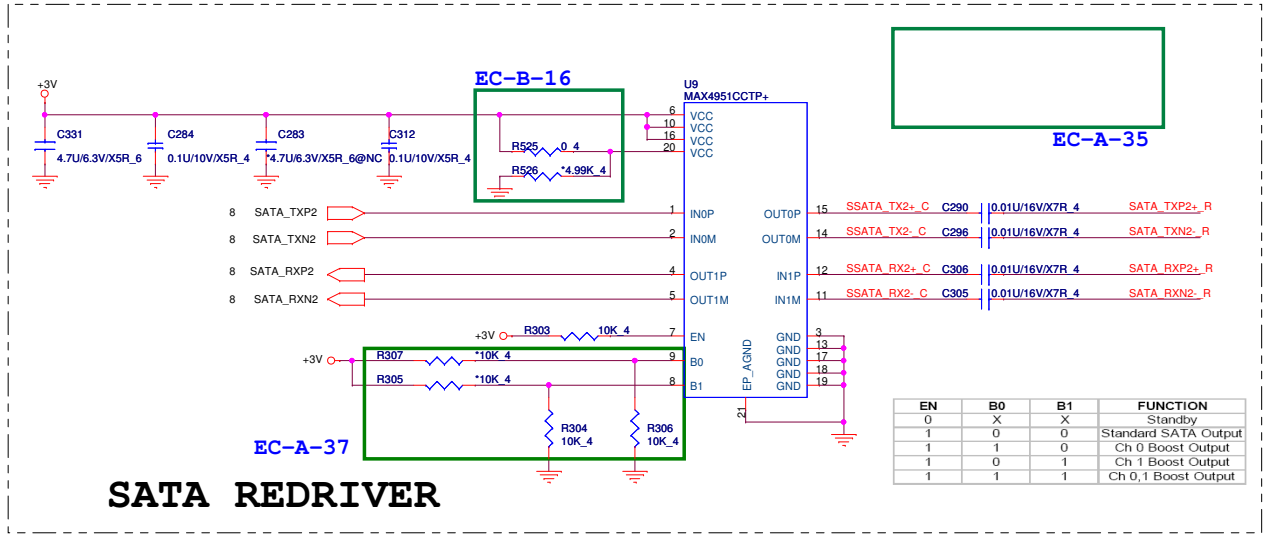
HDD

+3V 3,7,8,9,10,11,13,16,17,18,19,21,23,24,25,27,28,32,33,34,35,36,37,38,39
+5V 7,8,11,17,18,27,33,34







EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

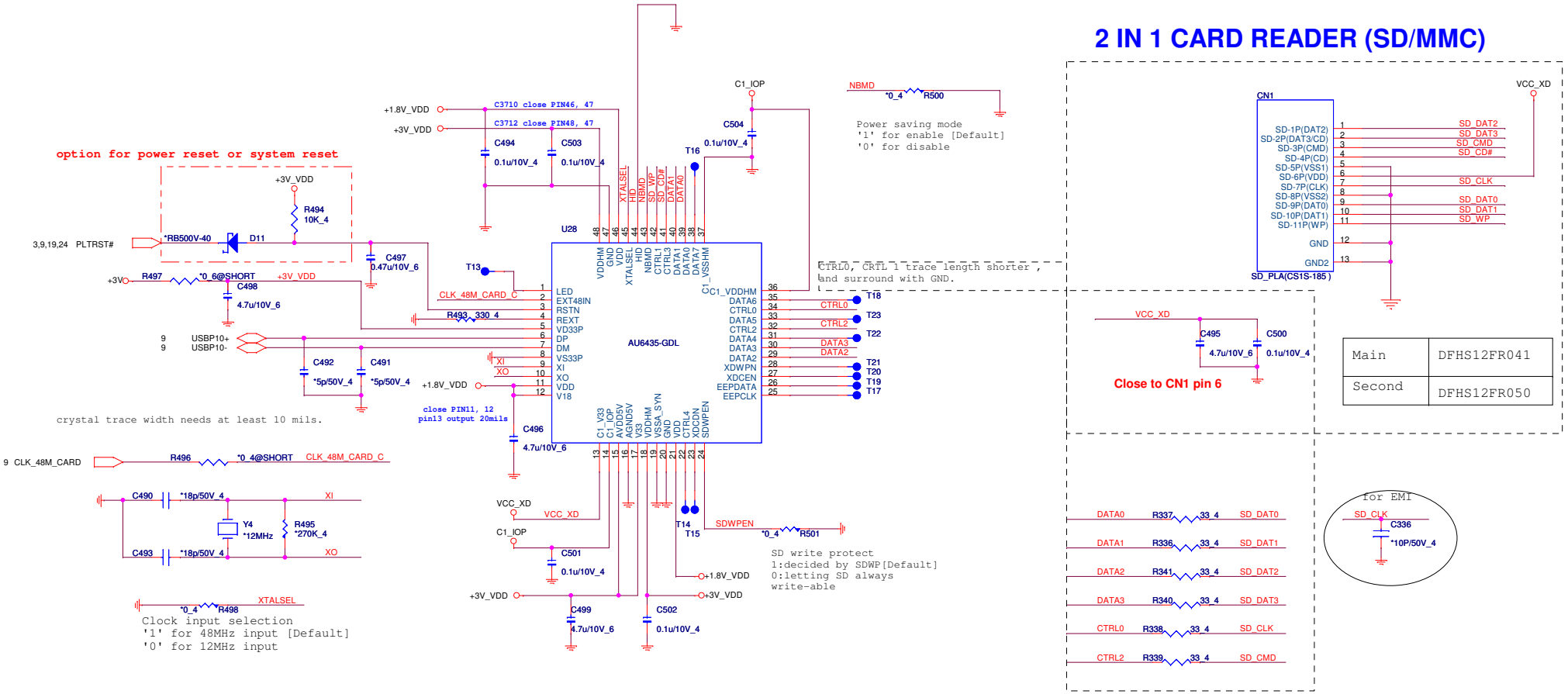
PROJECT : LZ7
Quanta Computer Inc.

Size	Document Number	Rev
	SATA	1A

Date: Wednesday, December 21, 2011 Sheet 20 of 42

AU6435-GDL CARD READER Controller

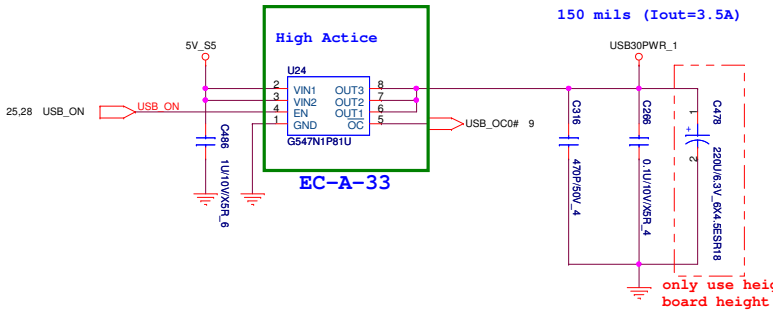
3,7,8,9,10,11,13,16,17,18,19,20,23,24,25,27,28,32,33,34,35,36,37,38,39 +3V

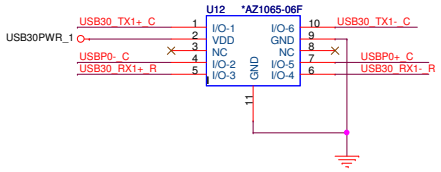


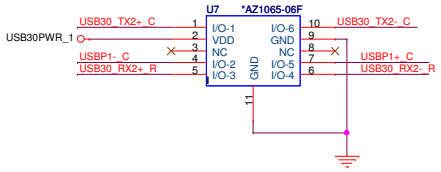
PROJECT : LZ7	
Quanta Computer Inc.	
Size	Document Number: AU6435-GDL CARD READER Controller — Rev: 1A
Date: Wednesday, December 21, 2011	Sheet 21 of 42

5V_S5 11,25,33

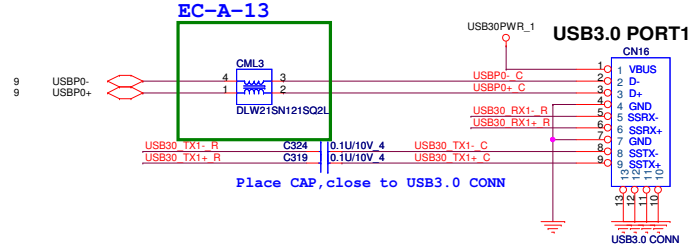
150 mils (Iout=3.5A)



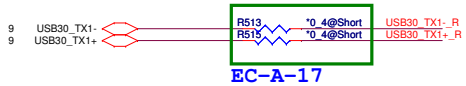




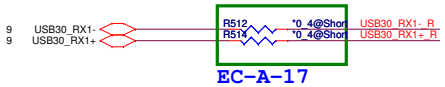
EC-A-13



Place CAP,close to USB3.0 CONN

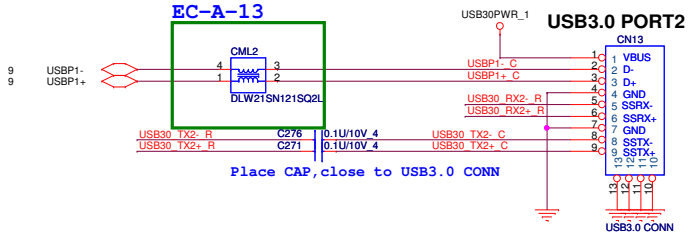


EC-A-17
EC-B-10

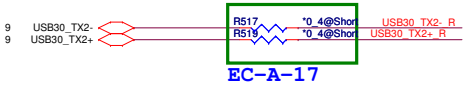


EC-A-17
EC-B-10

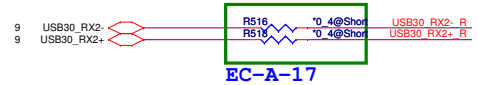
EC-A-13



Place CAP,close to USB3.0 CONN



EC-A-17
EC-B-10



EC-A-17
EC-B-10

PROJECT:LZ7

Quanta Computer Inc.

Size	Document Number	Rev
	USB3.0 x 2	1A

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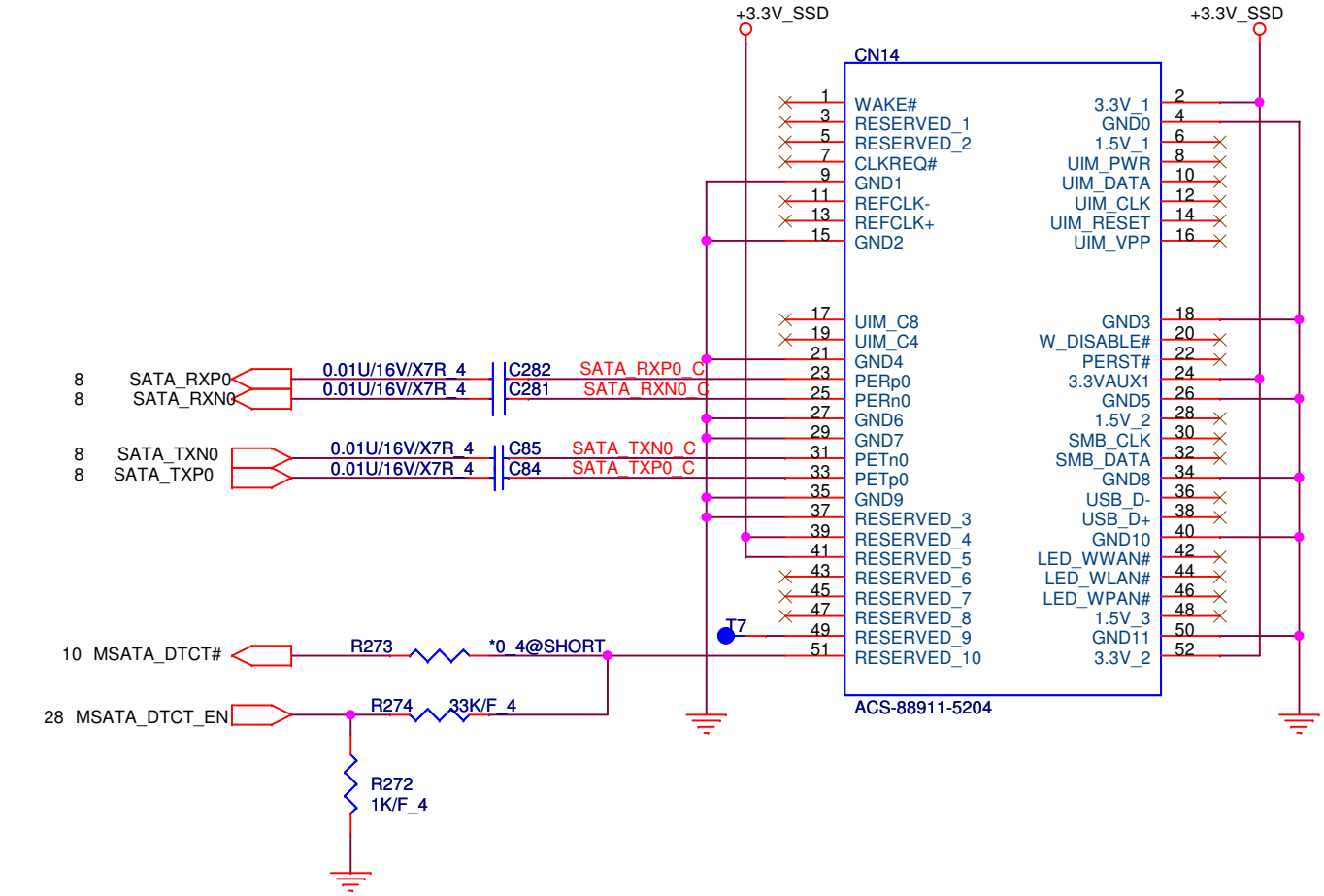
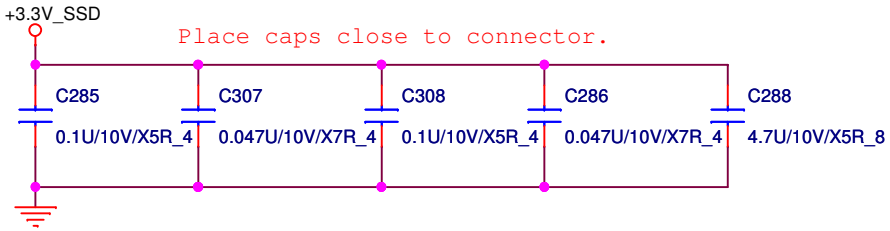
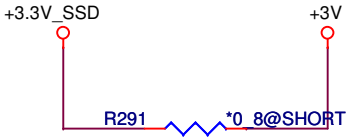
Mini PCI-E Card SSD

3,7,8,9,10,11,13,16,17,18,19,20,21,24,25,27,28,32,33,34,35,36,37,38,39 +3V
11,24,35 +1.5V

23







PROJECT : LZ7

Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI Card (SSD)	1E
Date: Wednesday, December 21, 2011	Sheet 23 of 42	

MiniCard WLAN connector

+1.5V 11,35
3V_S5 3,7,8,9,10,11,18,29,33
3VPCU 7,8,16,19,28,29,32,33,34,38
+3V 3,7,8,9,10,11,13,16,17,18,19,20,21,23,25,27,28,32,33,34,35,36,37,38,39

CN17

MINICARD_PME#	1	WAKE#	3.3V_1	2	
	3	RESERVED_1	GND0	4	
	5	BT_ DISABLE_L	1.5V_1	6	
9 PCIE_CLKREQ_WLAN#	7	CLKREQ#	UIM_PWR	8	
	9	GND1	UIM_DATA	10	LPC_FRAME# 8,28
9 CLK_PCIE_WLANN	11	REFCLK-	UIM_CLK	12	LPC_AD0 8,28
9 CLK_PCIE_WLANP	13	REFCLK+	UIM_RESET	14	LPC_AD1 8,28
	15	GND2	UIM_VPP	16	LPC_AD2 8,28
					LPC_AD3 8,28
8,28 SERIRQ	17	UIM_C8	GND3	18	
	19	UIM_C4	W_DISABLE#	20	WLAN_OFF_R#
	21	GND4	PERST#	22	R348 *0_4@SHORT PLTRST# 3,9,19,21
9 PCIE_RXN3_LAN	23	PERn0	3.3VAUX1	24	
9 PCIE_RXP3_LAN	25	PERp0	GND5	26	
	27	GND6	1.5V_2	28	
	29	GND7	SMB_CLK	30	R349 *0_4@SHORT PCLK_DEBUG 9
9 PCIE_TXN3_LAN	31	PETn0	SMB_DATA	32	R350 *0_4@SHORT LPC_DRQ#0 8
9 PCIE_TXP3_LAN	33	PETp0	GND8	34	
	35	GND9	USB_D-	36	USBP3_ R R344 *0_4@SHORT USBP3- 9
	37	RESERVED_3	USB_D+	38	USBP3+ R R342 *0_4@SHORT USBP3+ 9
	39	RESERVED_4	GND10	40	
	41	RESERVED_5	LED_WWAN#	42	
	43	GND	LED_WLAN#	44	TP91
	45	RESERVED_7	LED_WPAN#	46	TP90
	47	RESERVED_8	1.5V_3	48	
	49	RESERVED_9	GND11	50	
	51	RESERVED_10	3.3V_2	52	

ACS-88911-5204

+3.3V_WLAN +1.5V +3.3V_WLAN

R332 *0_4 TP89

PCI-Express TX and RX direct to connector

10 WLAN_BT_OFF# RB500V-40 D12 R335 *0_4@SHORT TP88

3V_S5 R343 10K_4

7,19,28 PCIE_WAKE# Q15 PDTC144EU MINICARD_PME#

WLAN_OFF_R# D13 RB500V-40 WLAN_OFF# 10

R347 *0_4

USBP3- R USBP3+ R U14 IO1 VIN IO2 GND *PJSR05 +3.3V_WLAN

+1.5V

C338 0.01U/16V/X7R_4
C342 0.1U/10V/X7R_4
C489 10U/6.3V/X5R_6
C340 *47P/50V/NPO_4
close to CN22

+3.3V_WLAN

Place caps close to connector.

C333 0.1U/10V/X7R_4
C337 0.047U/10V/X7R_4
C341 0.1U/10V/X7R_4
C339 0.047U/10V/X7R_4
C330 4.7U/6.3V/X5R_6
close to CN22
C332 *47P/50V/NPO_4

EC-A-15

3VPCU +3.3V_WLAN +3V

Q40 AO3413

R331 *0_8

EC-A-11

R333 4.7K_4

R334 *100K/F_4

7 WLAN_AOAC_ON Q14 DTC144EUA

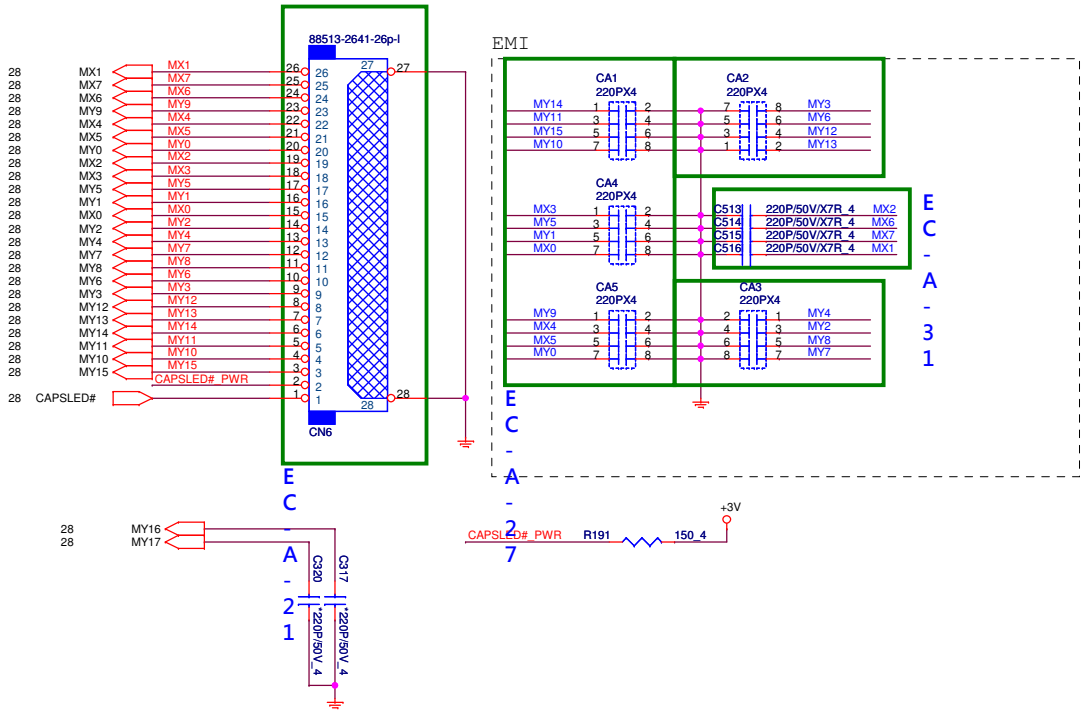
EC-A-11

PROJECT : LZ7

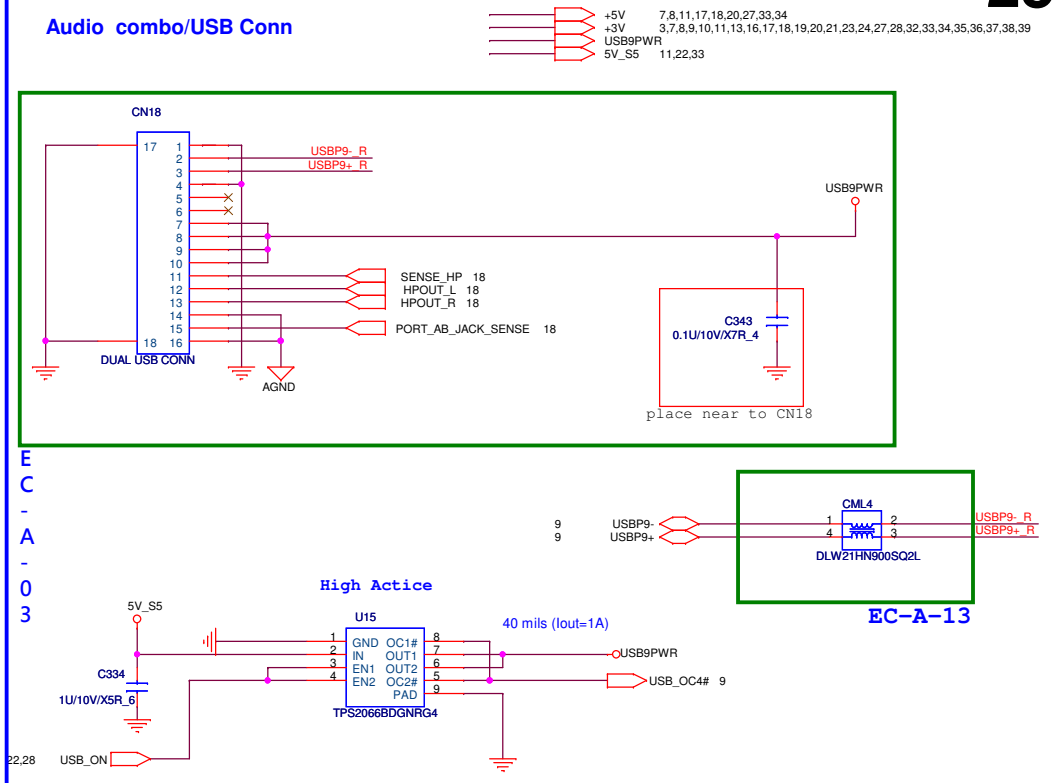
Quanta Computer Inc.

Size	Document Number	Rev
	WLAN/BT	1A
Date: Wednesday, December 21, 2011	Sheet 24 of 42	

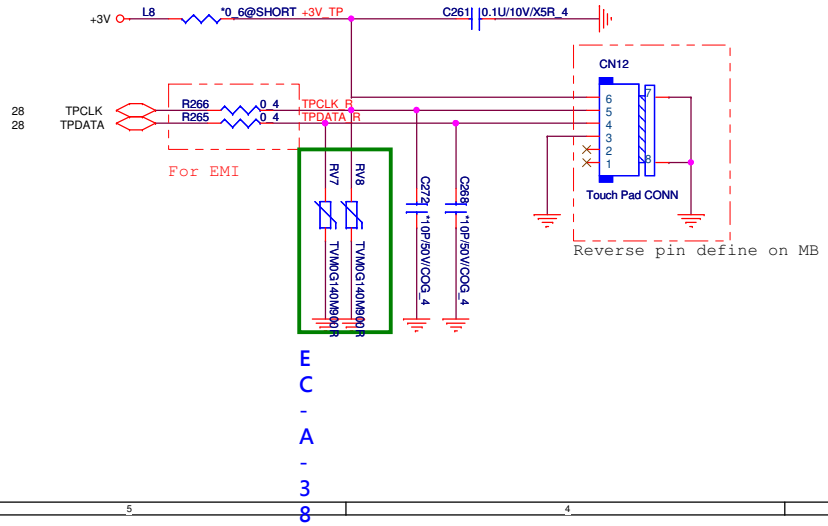
KEYBOARD



Audio combo/USB Conn



Touch pad



PROJECT : LZ7	Quanta Computer Inc.	
Size	Document Number KB/TP/LID/AUDIO-USB	Rev 1A
Date: Wednesday, December 21, 2011	Sheet 25 of 42	

PROJECT : LZ7

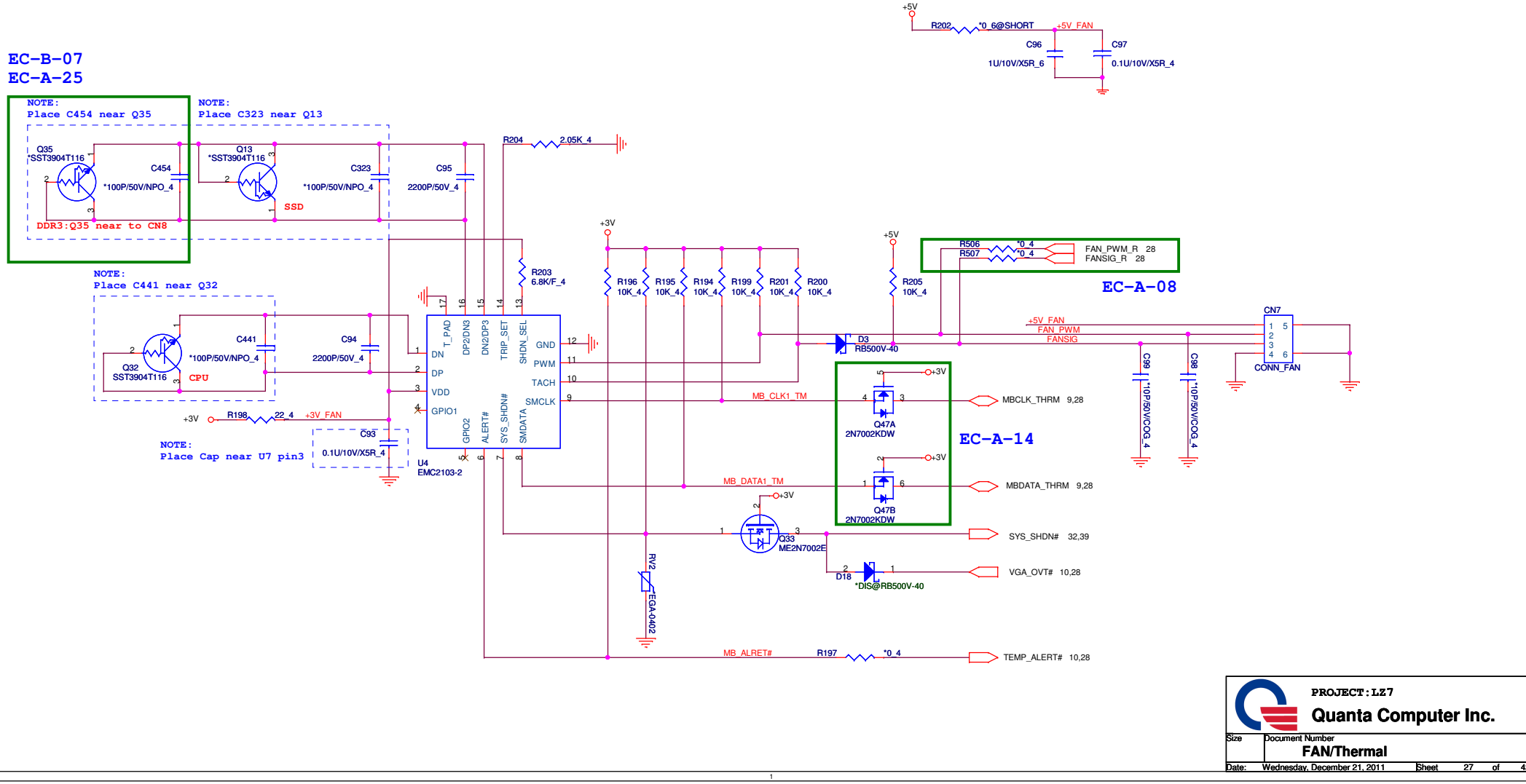
Quanta Computer Inc.

Size	Document Number	Rev
	BLANK	1A

Date:	Wednesday, December 21, 2011	Sheet	26	of	42

FAN CONTROL

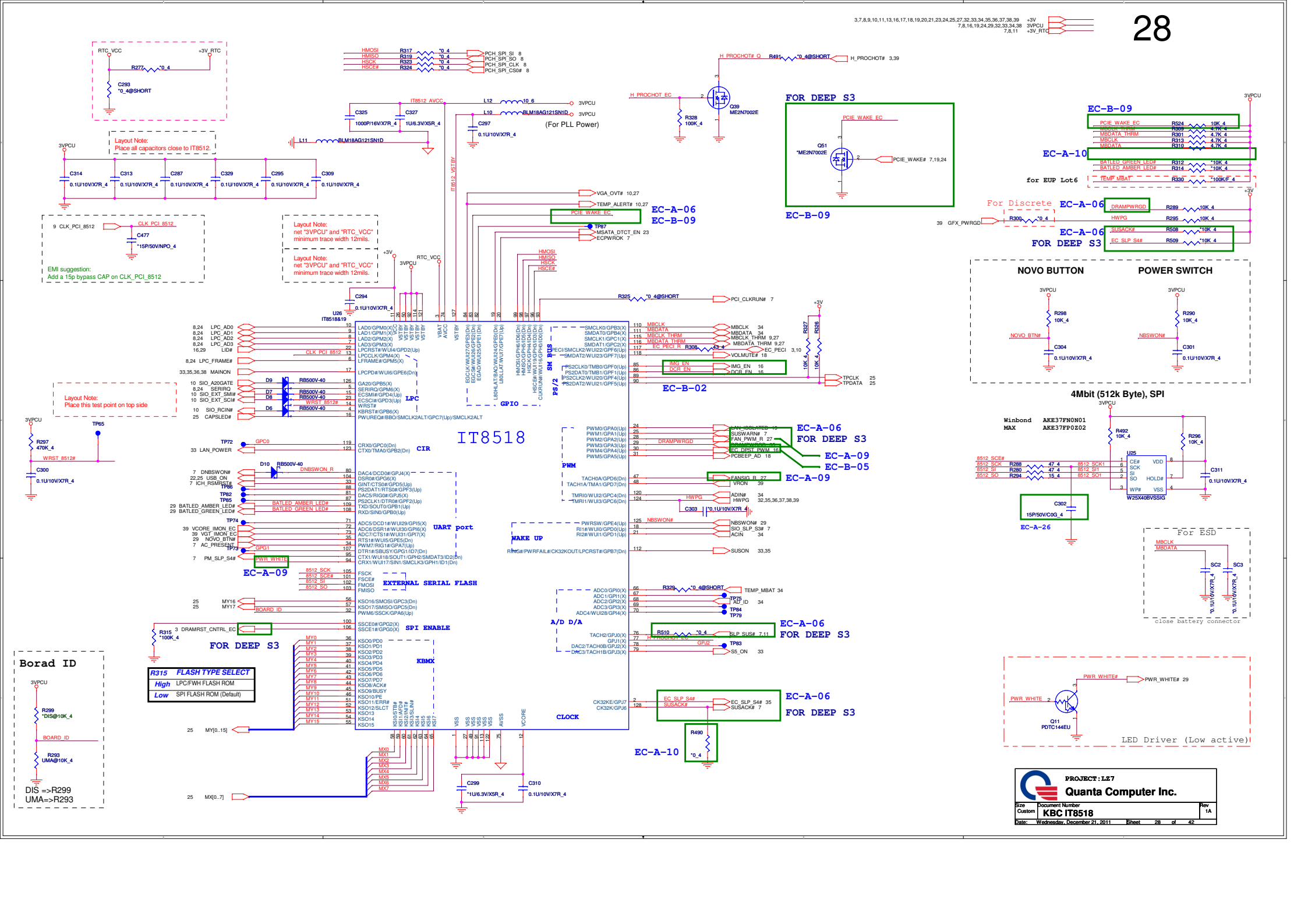
3,7,8,9,10,11,13,16,17,18,19,20,21,23,24,25,28,32,33,34,35,36,37,38,39 +3V
7,8,11,17,18,20,33,34 +5V



PROJECT : LZ7

Quanta Computer Inc.

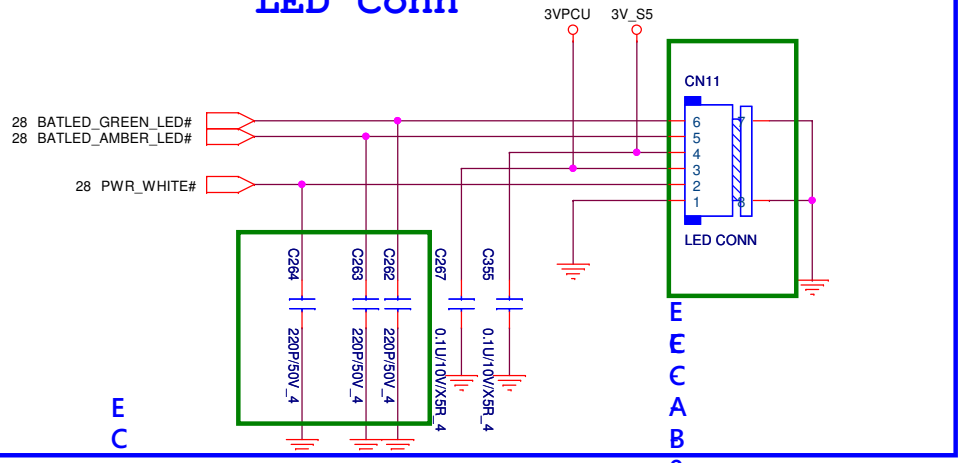
Size	Document Number	Rev
	FAN/Thermal	1A
Date: Wednesday, December 21, 2011	Sheet 27 of 42	



PROJECT : LZ7	Quanta Computer Inc.
Size: Custom	Document Number: KBC IT8518
Rev: 1A	
Date: Wednesday, December 21, 2011	Sheet 28 of 42

+3V	3,7,8,9,10,11,13,16,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39	
3VPCU	7,8,16,19,24,28,32,33,34,38	
3V_S5	3,7,8,9,10,11,18,24,33	

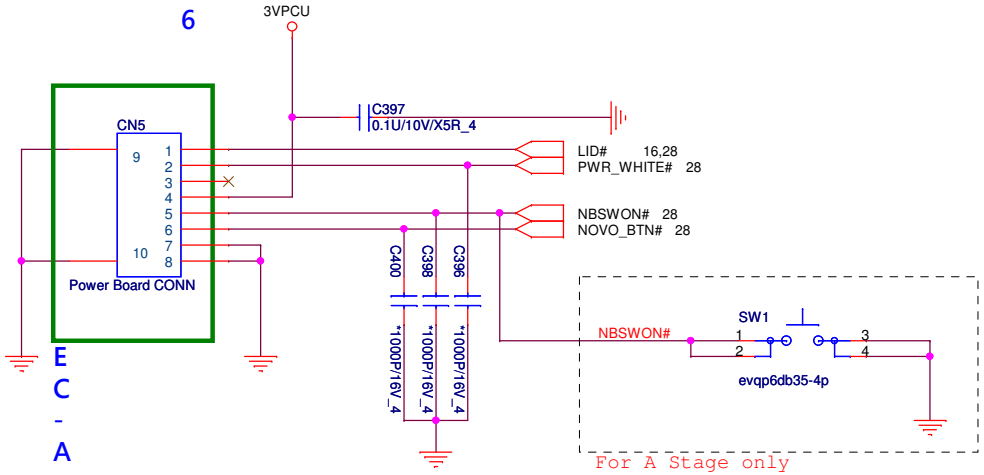
LED Conn



EC-A-26

EC-A-04

POWER/NOVO BUTTON



EC-A-04

PROJECT : LZ7		
Quanta Computer Inc.		
Size	Document Number: SW/LED	Rev: 1A
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Hole for CPU support

HOLE16 *H-C181D181N

HOLE14 *H-TIC142BC236D142N

HOLE15 *H-TIC142BC236D142N

HOLE13 *H-C142D142N

MiniCard SSD

HOLE18 H-TC217BIC142D102P2

MiniCard WLAN

HOLE17 H-TC217BIC142D102P2

HOLE20 H-TC217BIC75D35P2

PAD

GP1 *spad-re7x7

Boundary Hole

HOLE10 *H-C197D106P2

HOLE2 *H-C197D106P2

HOLE1 *H-C197D106P2

HOLE9 *HG-C394D315P2

HOLE8 *O-LZ7-1 NPTH

Round screw hole

HOLE3 *HG-C276D106P2

HOLE4 *HG-C276D106P2

HOLE5 *HG-C276D106P2

HOLE6 *H-C276D106P2

HOLE11 *HG-C276D106P2

HOLE12 *hg-lz7-2

PROJECT : LZ7

Quanta Computer Inc.

Size	Document Number	Rev
	Screw Hole/EMI	1A
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PROJECT : LS7

Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Power Block Diagram	1A
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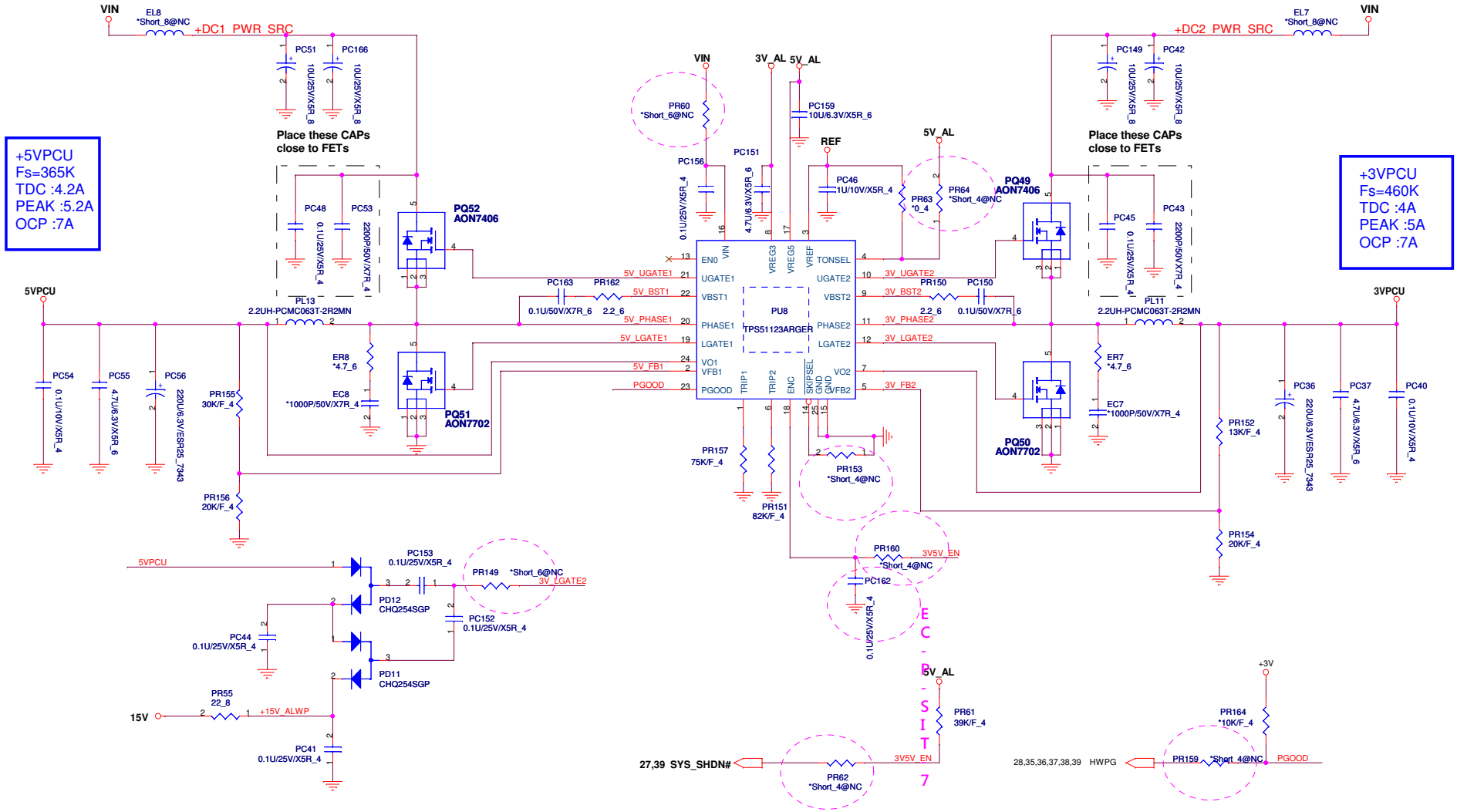

PROJECT : LZ7	Quanta Computer Inc.
Size	Document Number: 3V/5V (TPS51123ARGERR) Rev
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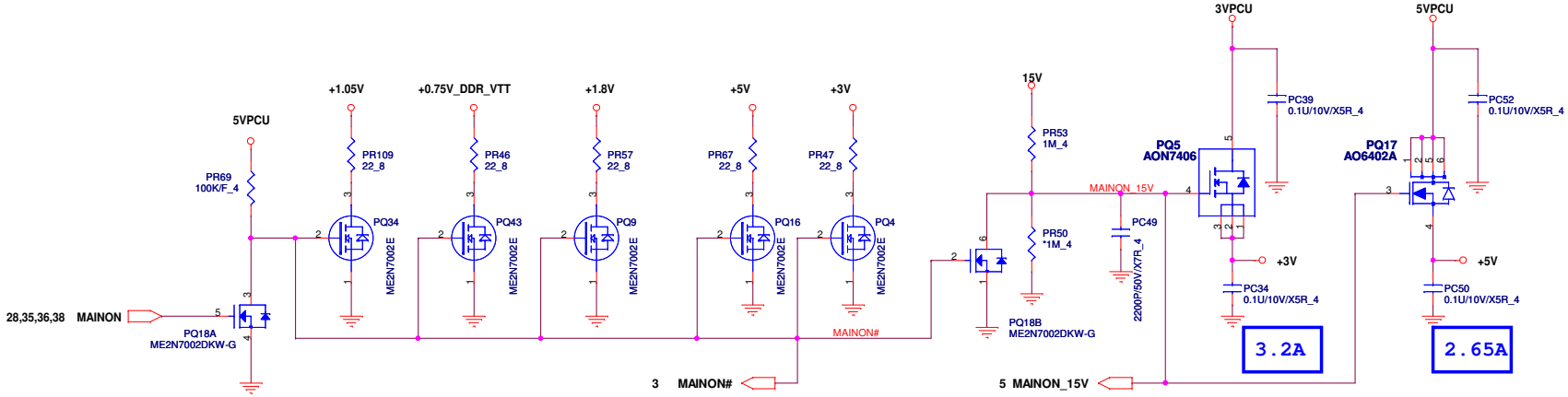
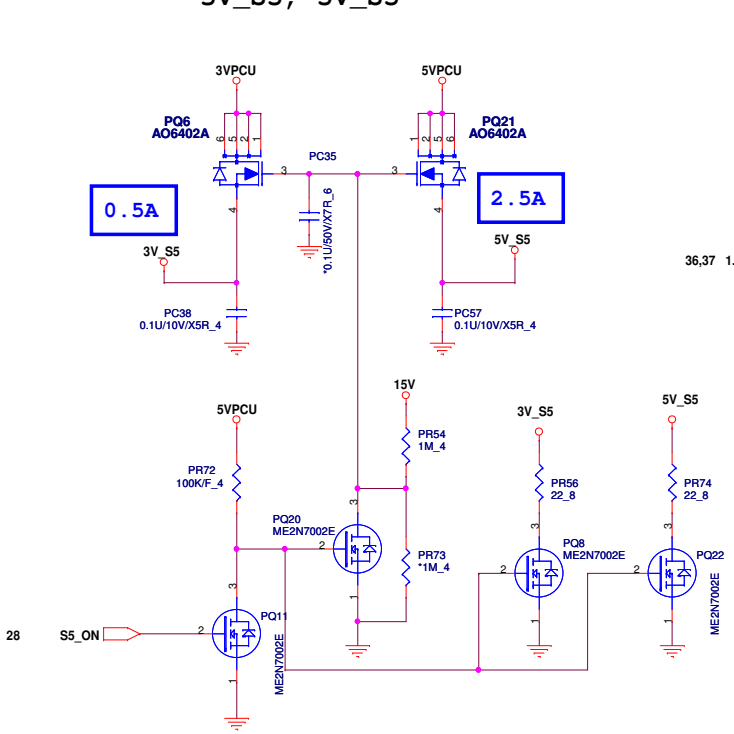
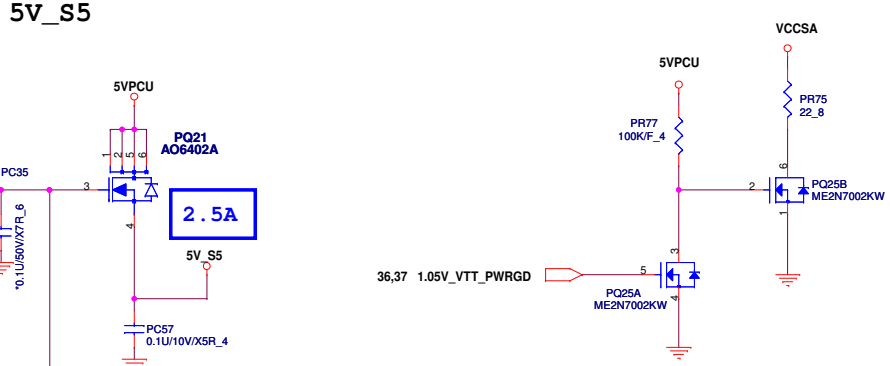
DISCHARGE

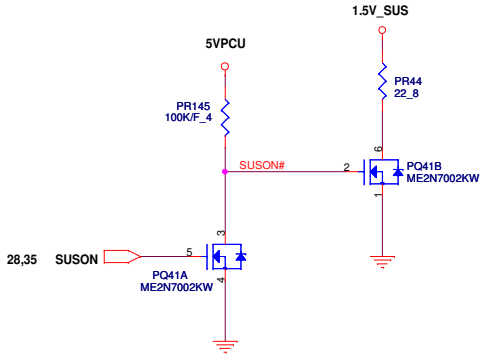
+3V, +5V



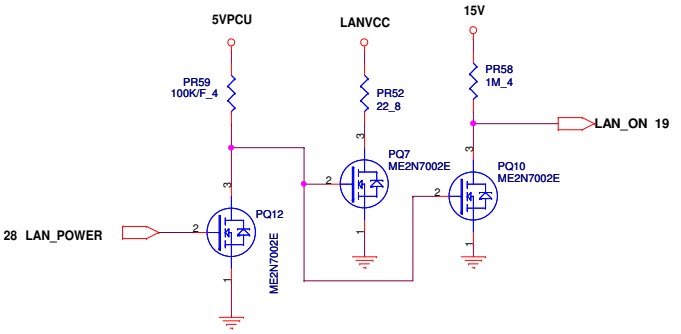
3V_S5, 5V_S5







LANVCC



PROJECT : LZ7

Quanta Computer Inc.

Size	Document Number	Rev
	Discharge	

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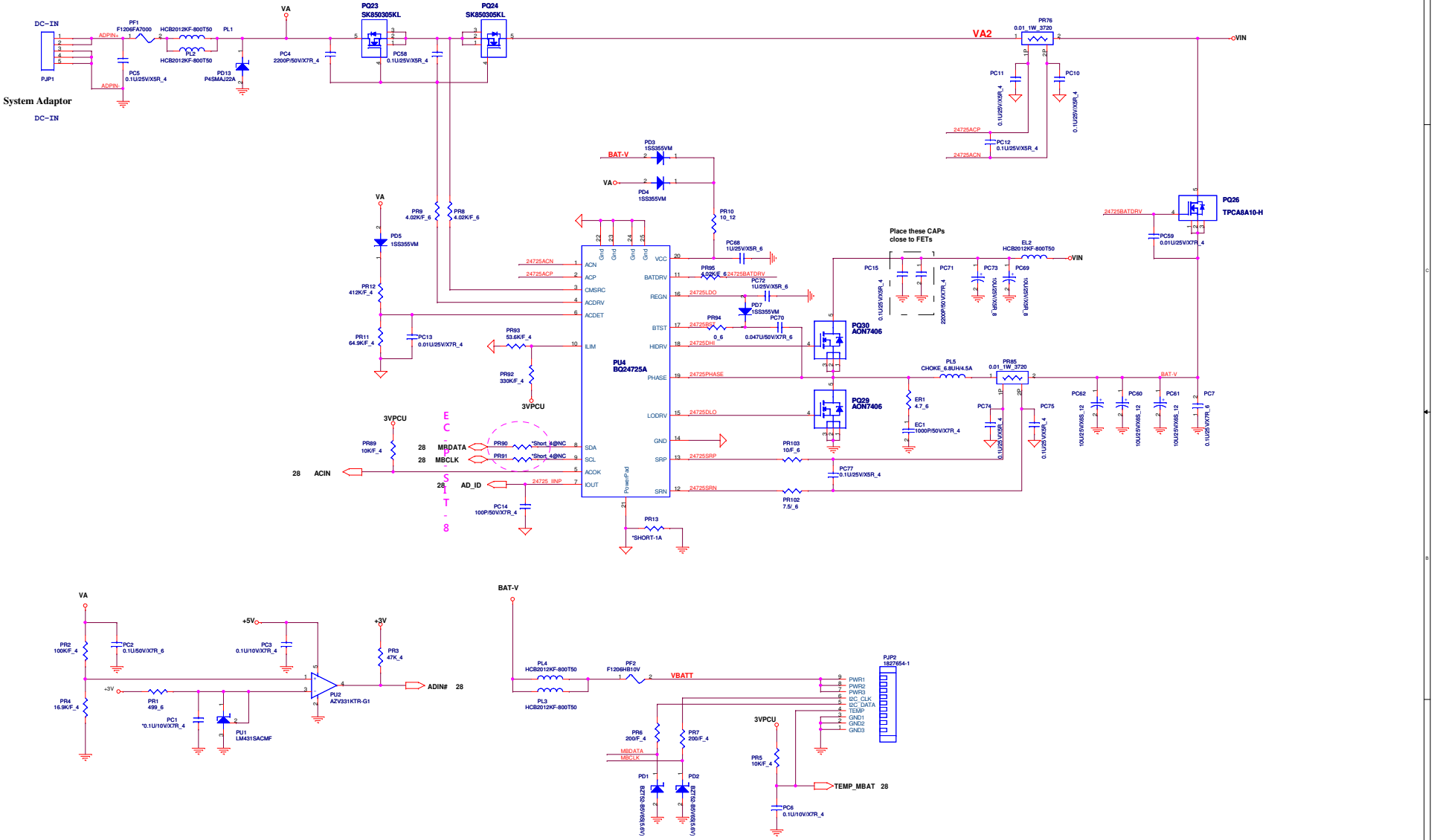

PROJECT : LZ7			
Quanta Computer Inc.			
Size	Document Number		Rev
	CHARGER (BQ24725)		1A
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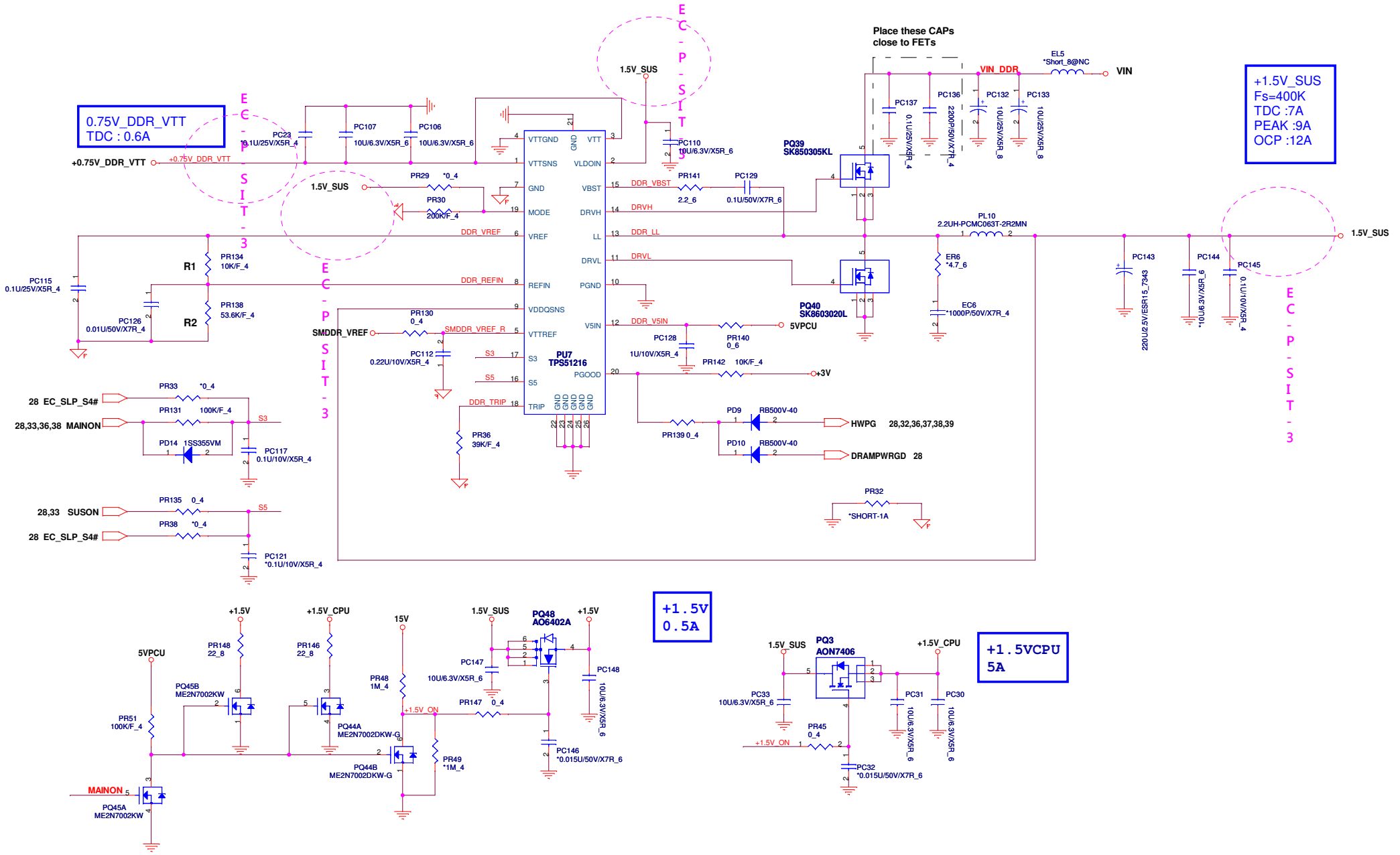
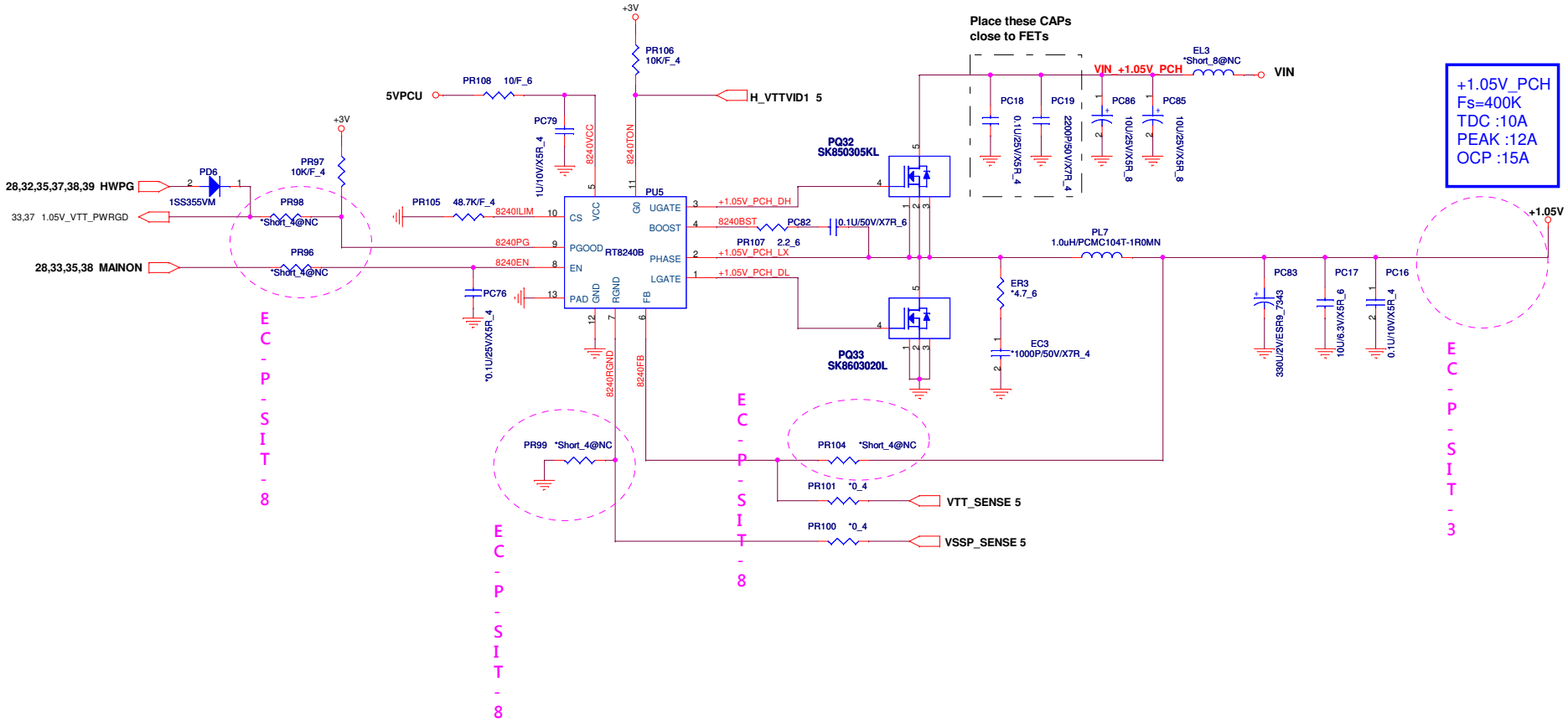
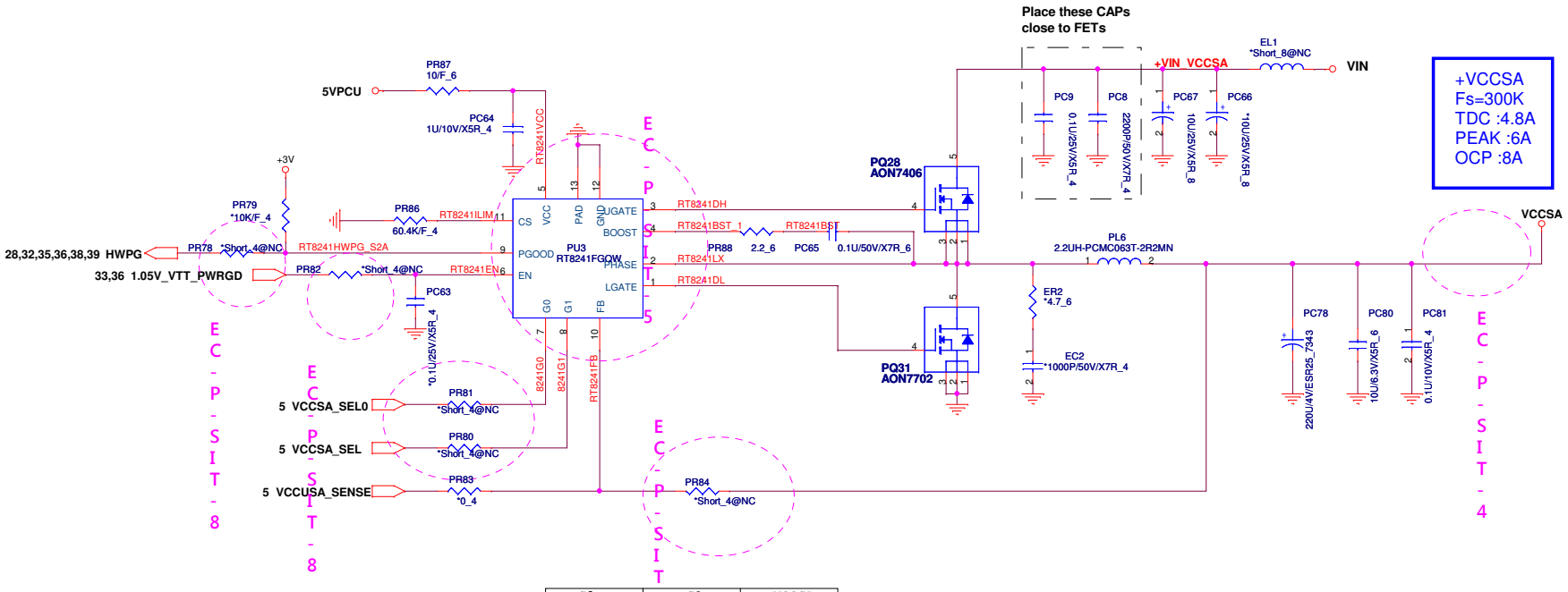


PROJECT : LZ7	
Quanta Computer Inc.	
Size	Document Number: DDR3/0.75V (TPS51216) — Rev
Date: Wednesday, December 21, 2011	Sheet 35 of 42



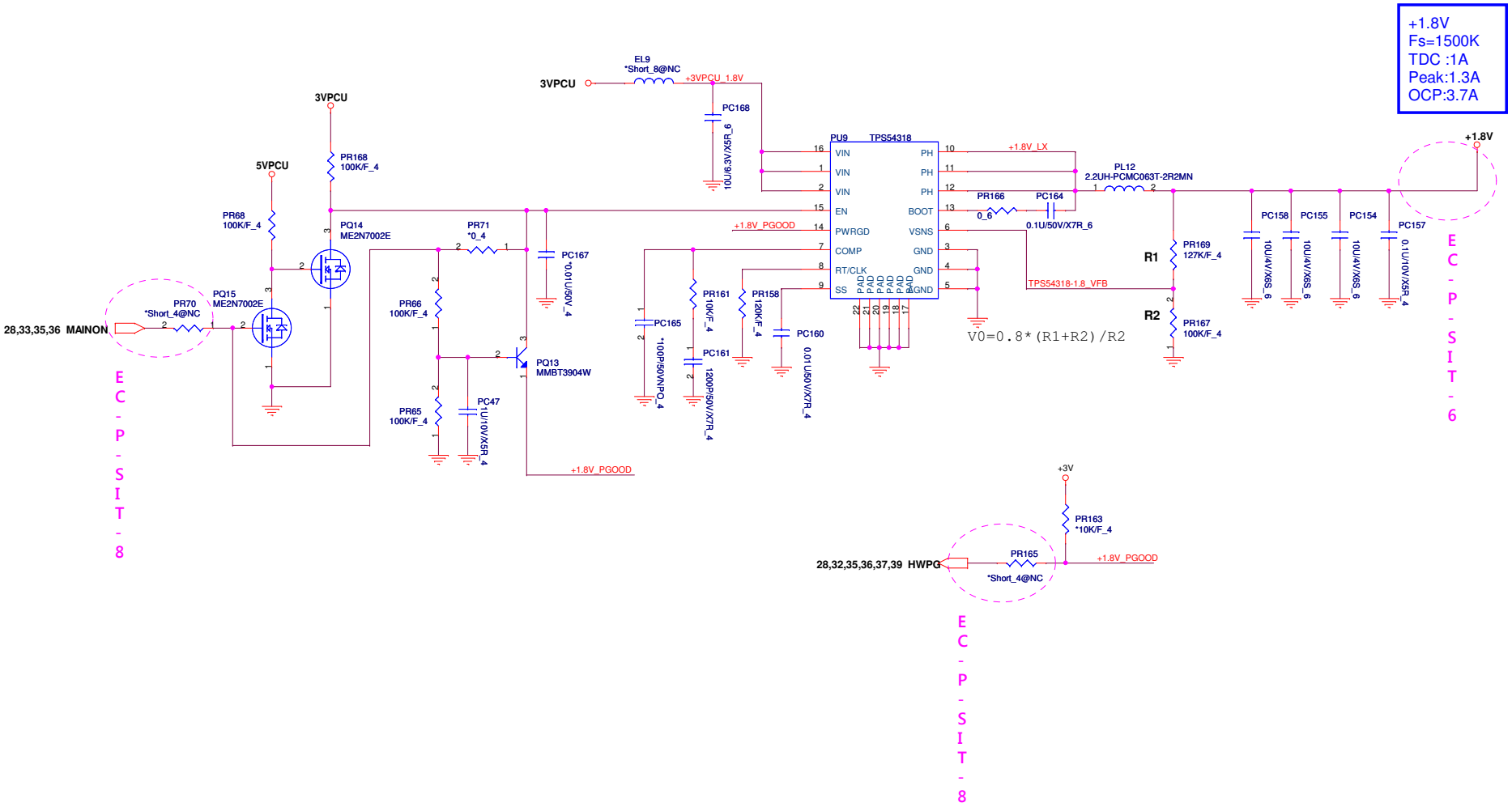
PROJECT : LZ7			
Quanta Computer Inc.			
Size	Document Number		Rev
	+1.05V_PCH(RT8240B)		
Date: Wednesday, December 21, 2011	Sheet 36	of 42	



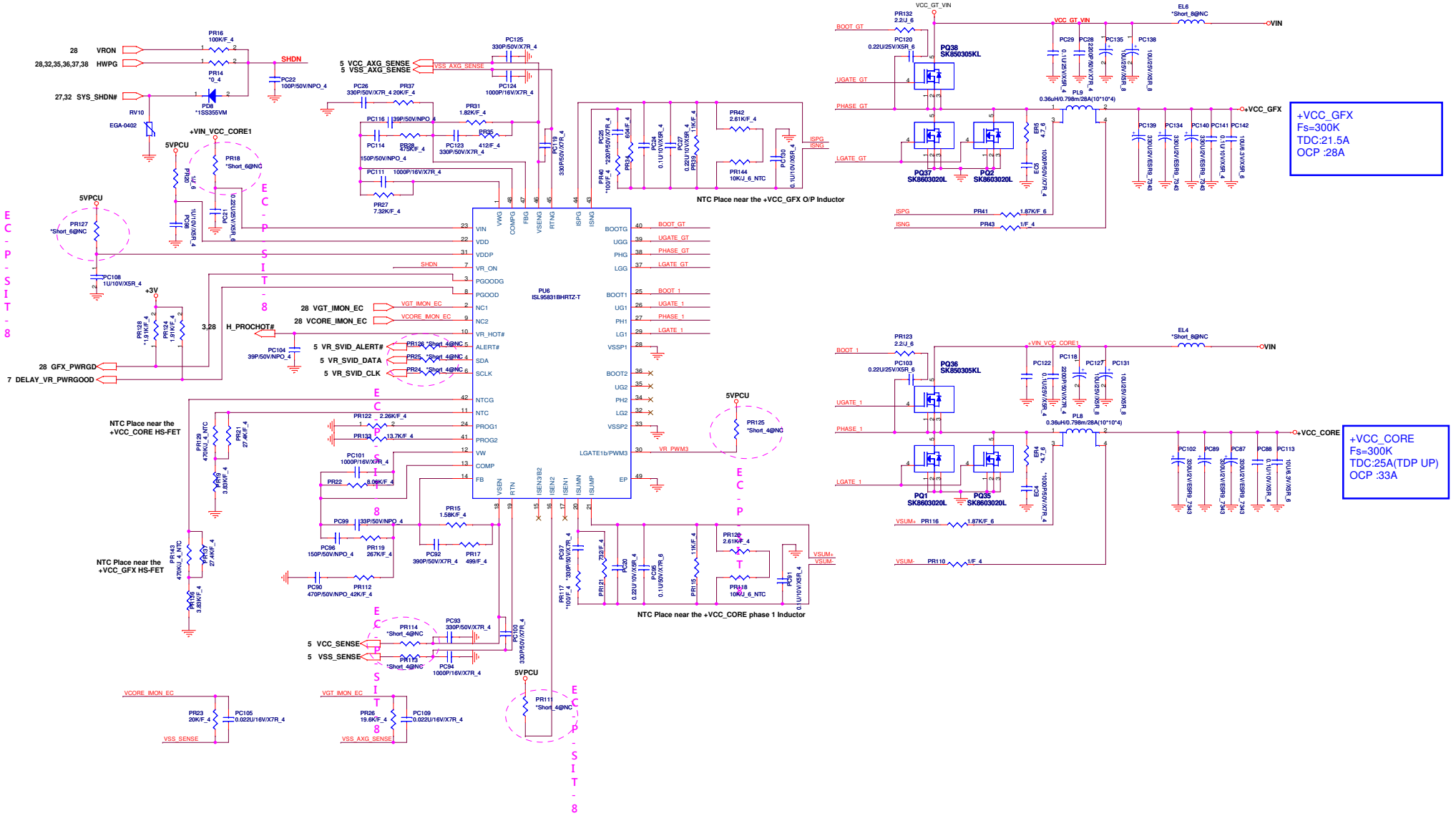
G0	G1	VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

default 0.9V

PROJECT : LZ7		
Quanta Computer Inc.		
Size	Document Number: VCCSA (RT8241D)	Rev
Date: Wednesday, December 21, 2011	Sheet 37 of 42	



PROJECT : LZ7		
Quanta Computer Inc.		
Size	Document Number: 1.8V (TPS54318)	Rev
Date: Wednesday, December 21, 2011	Sheet 38 of 42	



PROJECT : LZ7

Quanta Computer Inc.

Size	Document Number	Rev
	CPU(ISL95831)IMVP1+1	

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ECN	PG.	DATE yy/mm/dd	PART REFERENCE	DESCRIPTION
EC-A-01	10,16	11/10/04	C505,C506,C507,Q41,Q42,R502 R503,R504	change GPIO35 to CCD_ON for bios request, Add camera control circuit
EC-A-02	18	11/10/11	Q16,R373,C393,R360,R369.R368,C386,U17	modify audio combo jack circuit for audio plug in/out nosie
EC-A-03	25	11/10/11	CN18,C348,C356,CR352	Delete C348,C356,R352 change CN18 Pin define
EC-A-04	29	11/10/12	CN5,CN11	Change CN5,CN11 footprint from pitch 1.0mm to 0.5mm
EC-A-05	17,19	11/10/12	CN10,CN9	Change CN9,CN10 footprint to correct one
EC-A-06	7,28	11/10/17	R508,R509,R112	Add DEEP S3 function
EC-A-07	10	11/10/17	R88,R93	R93 Asm,R88 noAsm for Change Board ID to SIV stage
EC-A-08	27	11/10/17		Add EC detect Fan speed circuit
EC-A-09	28	11/10/17		Change EC pin define,PIN94 connect to PWR_WHITE,PIN28 connect to FAN_PWM_R,PIN47 connect to FANSIG_R
EC-A-10	28	11/10/17	R316,R490	Del R316 for pin94 use PWR_WHITE signal No Asm R490 for EC use internal clock
EC-A-11	24	11/10/17	Q14,R331	Q14 Asm,R331 No Asm for input AOAC function
EC-A-12	11	11/10/17		Add DEEP S3 function
EC-A-13	16,22, 25	11/10/17	CML1,CML2,CML3,CML4,R320, R318,R271,R270	CML2,CML3 CML4 asm R320,R318,R271,R270 R345,R346 noasm for EMI request Change common choke footprint from CHOKENCCM20C900-TR-4P to choke-dlw21s-4p for SMT request
EC-A-14	9,16, 27	11/10/17	Q25,Q24,Q26,Q27,Q31,Q34,Q44,Q45,Q49 ,Q47,Q3,Q5	del Q25,Q24,Q26,Q27,Q31,Q34,Q3,Q5 Add Q44,Q45,Q47,Q49 change from mos to Dual mos(sot363)
EC-A-15	24	11/10/17	C489	Change footprint from CH6101K9A14 0805 to CH6101M1904 0603 for ME Height limit
EC-A-16	7	11/10/18	R185	R185 asm for System PWR_OK tune
EC-A-17	22	11/10/18	CML5,6,7,8 R512,R513,R514,R515, R516,R517,R518,R519	Reserve CML5,6,7,8 R512,R513,R514,R515,R516,R517,R518,R519 asm for EMI request
EC-A-18	5	11/10/19	C508	Add 10uF 6.3V Cap on VCCSA for INTEL DG request
EC-A-19	7	11/10/21	R4,R5,R6,R379,R380,R381	Delete Reserve LVDS signal from PCH
EC-A-20	8	11/10/21		Delete SATA2 for PCH Change to HM77
EC-A-21	25	11/10/21		Change CN6 footprint from GB1RF260-1253-8F to 88513-2641-26p-l-smt for SMT request
EC-A-22	15	11/10/21	C21,C22,C33,C35,C44,C48 ,C50,C51,C52,C58,C65,C66,C87, C418,C420,C424,L4,L6,L7,L18,Q19 ,Q48,Q48,R48,R53,R60,R61,R63,R64,R66, R68,R75,R81,R94,R95,R96,R97, R103,R385,R393,U2,U18	Delete eDP to LVDS IC Page
EC-A-23	3	11/10/21	RP7,R447,R448,R467,C449,C450 ,C453,C452	R467,RP7 no asm , R447,R448 asm for eDP function disable
EC-A-24	3	11/10/21	R478,U23,R482,Q38,R120,R477	R478,R482,Q38 asm ,U23,R120,R477 Noasm Delete AND GATE for intel CRB Suggest
EC-A-25	27	11/10/21	Q35	Add Q35 for thermal request
EC-A-26	18,28, 29	11/10/22	C406,C407,C410,C411,C302, C262,C263,C264	audio C406,C407,C410,C411(CH4102K1B03)asm EC C302(CH01506JBD9)asm LED C262,C263,C264(CH12206JB00)asm for EMI request
EC-A-27	25	11/10/22	CA1,CA2,CA3,CA4,CA5	CA1,2,3,4,5 asm for KB EMI request
EC-A-28	17	11/10/22	R248,R243,R241,R238	R248,R243,R241,R238 asm for HDMI EMI request
EC-A-29	19	11/10/24	C509,C510,C511C512	Reserve C509,C510,C511C512 for LAN EMI request
EC-A-30	18	11/10/24	R386,R387,R388,R389,R366,C387	R386,R387,R388,R389 change to CX8PG181001 R366 Change to CX471T10000 C387 Change to CH0226F0B05 for EMI request
EC-A-31	25	11/10/24	CA6,C513,C514,C515,C516	delete CA6 and change from cap array to cap 0402 C513,C514,C515,C516 asm for EMI request
EC-A-32	8	11/10/24	R84,C369	Change R84 to CS02202FB12 change C369 to CH01506JBD9 for EMI request
EC-A-33	22	11/10/24	U24	Change U24 from G547E2P81U to G547N1P81U for 3.7A usb3.0 2 port Current
EC-A-34	11	11/10/24	C15,C17,C18	C15,C17,C18 asm for VCCDAC ripple voltage issue
EC-A-35	20	11/10/27		Del R276,R279,R281,R287 for SATA TX RX Signal line Branch too long issue
EC-A-36	18	11/10/27	C383,C363,C351,C365 C353,C352	C383,C363,C351,C365,C353,C352 noasm for FAE Suggest
EC-A-37	20	11/10/27	R307,R305	R307,R305 No asm , for Boost mode change to Standard mode
EC-A-38	16,25	11/10/31	U1,RV7,RV8	U1,RV7,RV8 asm , for ESD request

ECN	PG.	DATE yy/mm/dd	PART REFERENCE	DESCRIPTION
EC-B-01	06,13	11/12/05	R520,R521,R522,Q50	R522 Asm for DDR M3 mode
EC-B-02	16,28	11/12/05		Add DCR_IN,IMG_IN Signal for Lenovo request
EC-B-03	16	11/12/05	R9,R12,CML1	Delete R9,R12 CML1 asm for EMI request
EC-B-04	29	11/12/05	CN11	Change CN11 footprint from 88707-060n-6p-l to 88501-0601-6P-L-smt for assmbely line issue
EC-B-05	16,28	11/12/05	R383,R523	R383 No asm R523 asm Add LCD PWM Signal from EC for lenovo request
EC-B-06	10	11/12/06	R147,R141,R93,R88	R147,R88 asm R93,R141 no asm for board id SIT Stage
EC-B-07	27	11/12/08	Q35	Q35 no asm for thermal request
EC-B-08	19	11/12/09	C509,C510,C511,C512	C509,C510,C511,C512 CH11806JB09 asm for EMI request
EC-B-09	28	11/12/09	Q51,R524	Reserve Q51 R524(CS31002JB28) asm for DEEP S3 function
EC-B-10	22	11/12/09	CML5,CML6,CML7,CML8 R512,R513,R514,R515,R516,R517,R518,R519	CML5,CML6,CML7,CML8 delete change R512,R513,R514,R515,R516,R517,R518,R519 to short0402 for EMI request
EC-B-11	16	11/12/09	RV11,RV12	RV11,RV12 CY140M90B00 asm for ESD request
EC-B-12	09	11/12/13	C402,C401,C402	Change footprint from XTAL-5X3_2-3_8 to xtl-3_2x2_5-2_2x1_7 C401,C402 Change to CH01006JB08 (10pf)
EC-B-13	18	11/12/13	C406,C410,C411,C407	Change CH4102K1B03 (0.1uF) to CH1336J0B01 (330pF) to meet Conexant spec <1000pf for Garbage screen issue
EC-B-14	18	11/12/14	CN3	Change DFHD04MR701 to DFHD04MR211(88266-040xx-xxx-4p-l) for speaker request
EC-B-15	11	11/12/15		R511 connect to 5VPCU for Deep S3 function
EC-B-16	20	11/12/16	R525,R526	R525 asm,R526 No asm for 2nd source parade sata redriver
EC-B-17	20	11/12/20	R322,R321	Delete R322,R321 for +3V,+5V HDD transfer layer via reduce

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EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-P-SIV-1	32		PR157,PR151	3VPCU,5VPCU OCP set
EC-P-SIV-2	34		PJP1	Change DC-IN CONN footprint
EC-P-SIV-3	34		PF1,PF2	Change Fuse footprint
EC-P-SIV-4	34		PQ26	Change N-MOSFET with built-in Schottky diode
EC-P-SIV-5	34		EL2	Add charger bead
EC-P-SIV-6	34		PR85	Change PR85 to 10mohm
EC-P-SIV-7	34		PR13	Change PR13 footprint
EC-P-SIV-8	34		PR11,PR12	Change ACDET voltage
EC-P-SIV-9	34		PR92,PR93	Change ILIM voltage
EC-P-SIV-10	34			Modify MBDATA,MBCLK
EC-P-SIV-11	35		PJP8,PJP9	Change to default short
EC-P-SIV-12	35		PC144	Change to NC
EC-P-SIV-13	35		PR32	Change PR32 footprint
EC-P-SIV-14	35			Change PU7 GND
EC-P-SIV-15	35		PR138	Change PR138 for 1.5V regulation
EC-P-SIV-16	35		PD14	Add PD14 for S3
EC-P-SIV-17	35		PJP6	Change to default short
EC-P-SIV-18	35			Change netname for EE request
EC-P-SIV-19	36		PJP3,PJP4	Change to default short
EC-P-SIV-20	36		PR105	Change PR105 to 48.7K for OCP set
EC-P-SIV-21	36		PR99,PR100 PR101,PR104	Change PR99 & PR100 to 0ohm,Change PR101 & PR104 to NC
EC-P-SIV-22	37		PJP5	Change to default short
EC-P-SIV-23	37		PR86	Change PR86 to 60.4K for OCP set
EC-P-SIV-24	37		PR83,PR84	Change PR84 to 0ohm,Change PR83 to NC
EC-P-SIV-25	37		PU3	Change PU3 to RT8241E for VCCS voltage level
EC-P-SIV-26	38		PJP9	Change to default short
EC-P-SIV-27	39		PL8,PL9	Change PL8,PL9 footprint
EC-P-SIV-28	39		ER5,EC5	Add ER5,EC5 for EMI request
EC-P-SIV-29	39		PC20	Change PC20 to 0.22uF for CPU transient
EC-P-SIV-30	39		RV10	Add RV10 for ESD request
EC-P-SIV-31	39		PR23	Change PR23 to 20K for CPU IMON
EC-P-SIV-32	39		PR34	Change PR34 to 604ohm for GFX OCP&loadline

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