

SUZHOU-D

CPU : AMD Caspin
Chip Set : AMD RX881+SB710
Remarks : Tigris Platform

Model Name : Suzhou-D
PBA Name : MAIN
PCB Code : GCE :
 NAN :
 HAN :
Dev. Step : PV
Revision : 1.0
T.R. Date : 2009.11.10

Design	CHECK	APPROVAL
XIE BIN	GUO LEI	BC LEE

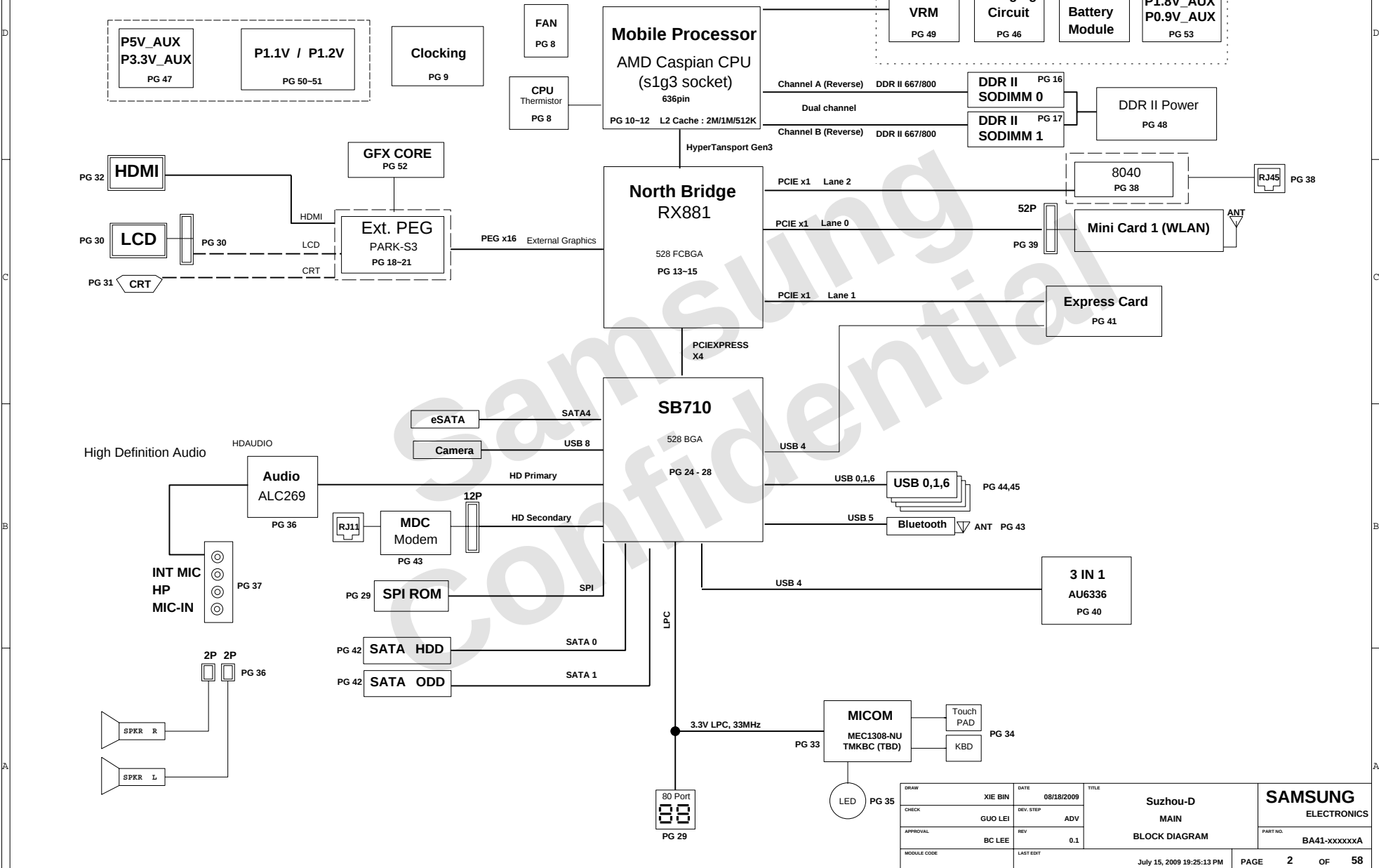
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DRAW	XIE BIN	DATE	08/18/2009	TITLE		Suzhou-D		SAMSUNG	
CHECK	GUO LEI	DEV. STEP	ADV			MAIN		ELECTRONICS	
APPROVAL	BC LEE	REV	0.1			COVER		PART NO.	BA41-xxxxxxA
MODULE CODE	LAST EDIT		July 15, 2009 19:25:13 PM			PAGE	1	OF	58

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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
CPU_CORE0	Core Voltage for CPU
CPU_CORE1	Core Voltage for CPU
EGFX_CORE	Core Voltage for GPU
P1.1V	VTT for M92,RX881
P1.2V	Core Voltage for SB710
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V_AUX	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_STB	5.0V always power rail
P12.0V_ALW	12.0V always power rail

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB710	Real Time Clock
Crystal	10MHz	MICOM	MECL308-NU
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	88E8040
Crystal	25MHz	SATA	SB710

I²C / SMB Address

Devices	Address	Hex	Bus
SB710	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 0010	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	NC
3	NC
4	3 IN 1
5	Bluetooth
6	SYSTEM PORT 2
7	NC
8	Camera
9	NC
10	EXPRESS CARD

PCI Express Assign

PORT #	ASSIGNED TO
0	Mini Card (WLAN)
1	EXPRESS CARD
2	LOM
3	NC
4	NC
5	NC

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0(strap0)
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REVISION HISTORY

See rev notes for more information.

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APPROVAL	BC LEE	REV	0.1	BOARD INFORMATION	PART NO.	BA41-xxxxxxA
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POWER DIAGRAM

Rev 0.1

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AC Adapter

Battery DC

VDC

P3.3V_MICOM

MICOM LED SB710

P5.0V_STB

USB N Charger

P12.0V_ALW

KBC3_SUSPWR
(CHP3_S4_STATE*)

P1.8V_AUX

AMD S1G3
SODIMM (DDR II)

P5V_AUX

USB connector

P0.9V_AUX

DDR II-Termination

P1.2V_AUX

SB710

P3.3V_AUX

SB710
EXPRESS CARD
WLAN
LAN
MDC
THERMAL
LVDS
LED

P1.2V_LAN

LAN

KBC3_PWRON
(CHP3_SLPS3*)

P1.8V

RX881
PARK
gDDR-3 for PARK
eSATA Reapter
AU6336

P5.0V

THERMAL CRT HDMI
SB710 MICOM AUDIO
ODD HDD CAMERA
TOUCH PAD

EGFX_CORE

PARK

P1.0V

PARK

P1.5V

CK505
WLAN
EXPRESS CARD

P2.5V

S1G3

P3.3V

CK505 THERMAL RX881
DDR2 PARK CRT
LVDS HDMI SB710
SPI WLAN LEDS
LAN AUDIO EXPRESS CARD
HDD BT AU6336

KBC3_VRON

CPU_CORE0,1

S1G3

P1.2V

S1G3
RX881
SB710

P1.1V

RX881
PARK

Power On/Off Table by S-state

Rail \ State	S0	S3	S4	S5
+V*A(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V_AUX	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

S5-S4

S3

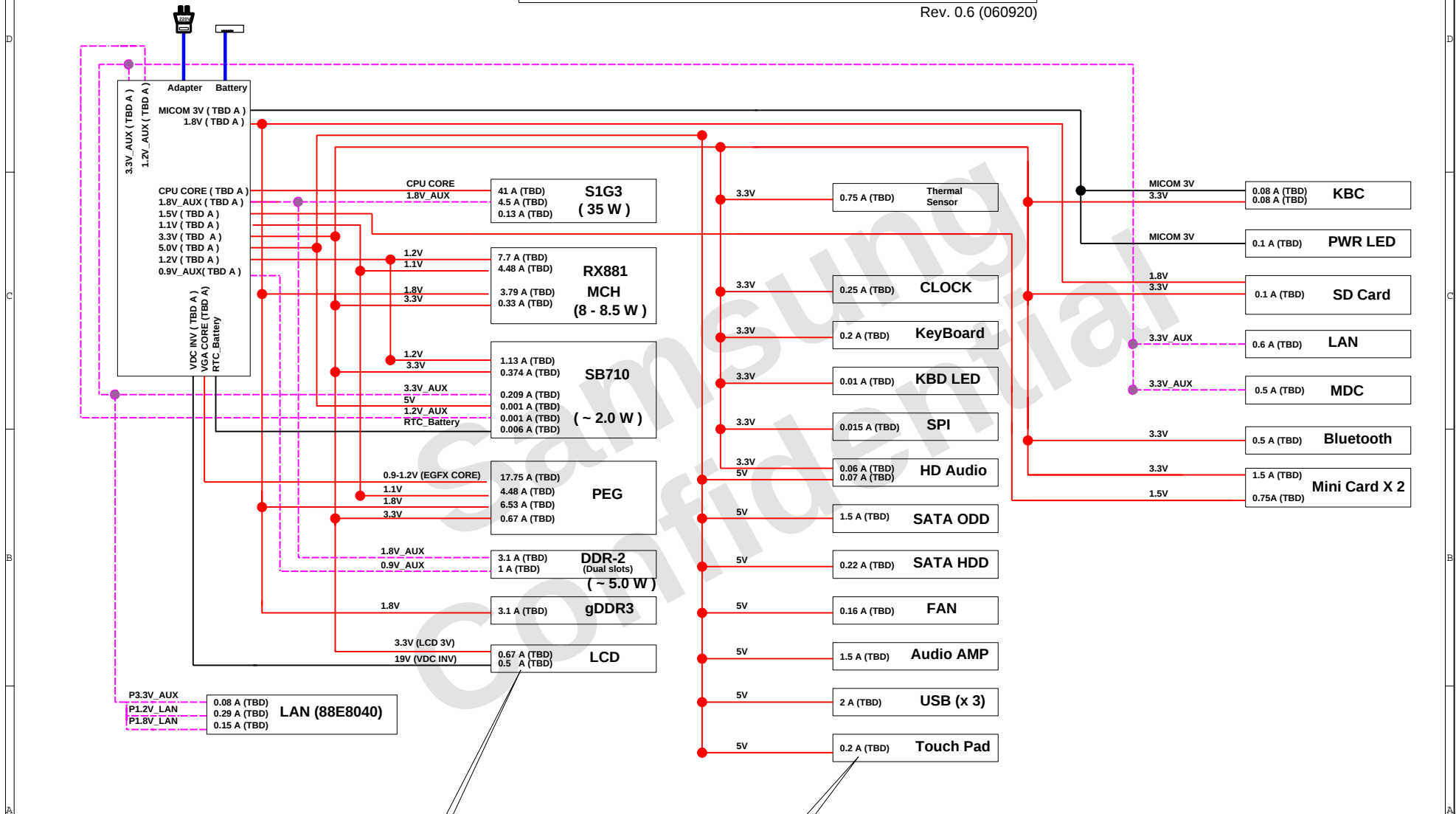
S0

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CHECK	GUO LEI	DEV. STEP	ADV	POWER DIAGRAM		
APPROVAL	BC LEE	REV	0.1			
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POWER RAILS ANALYSIS

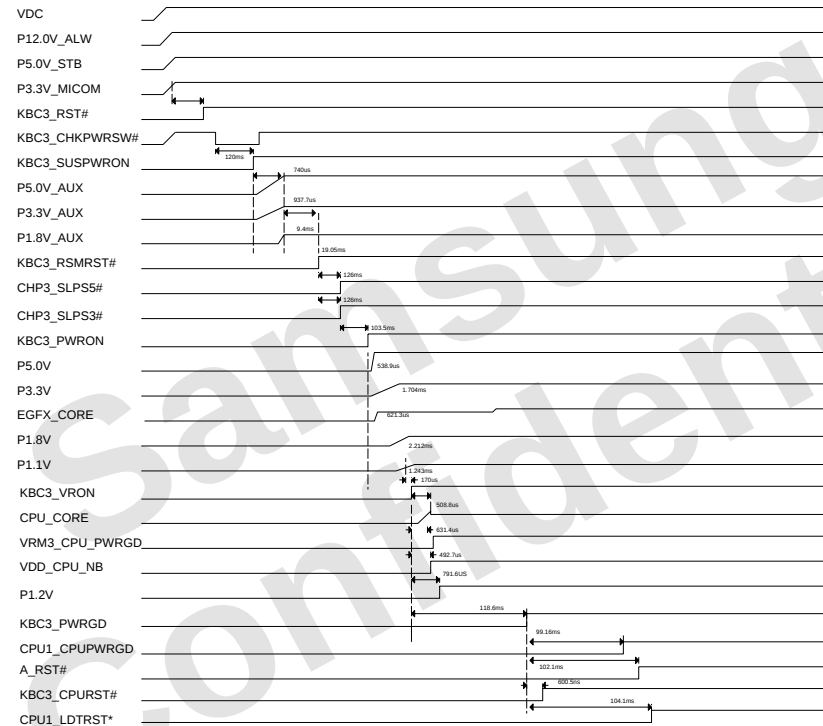
Rev. 0.6 (060920)



Value by Datasheet/Application notes (Value by measurement)

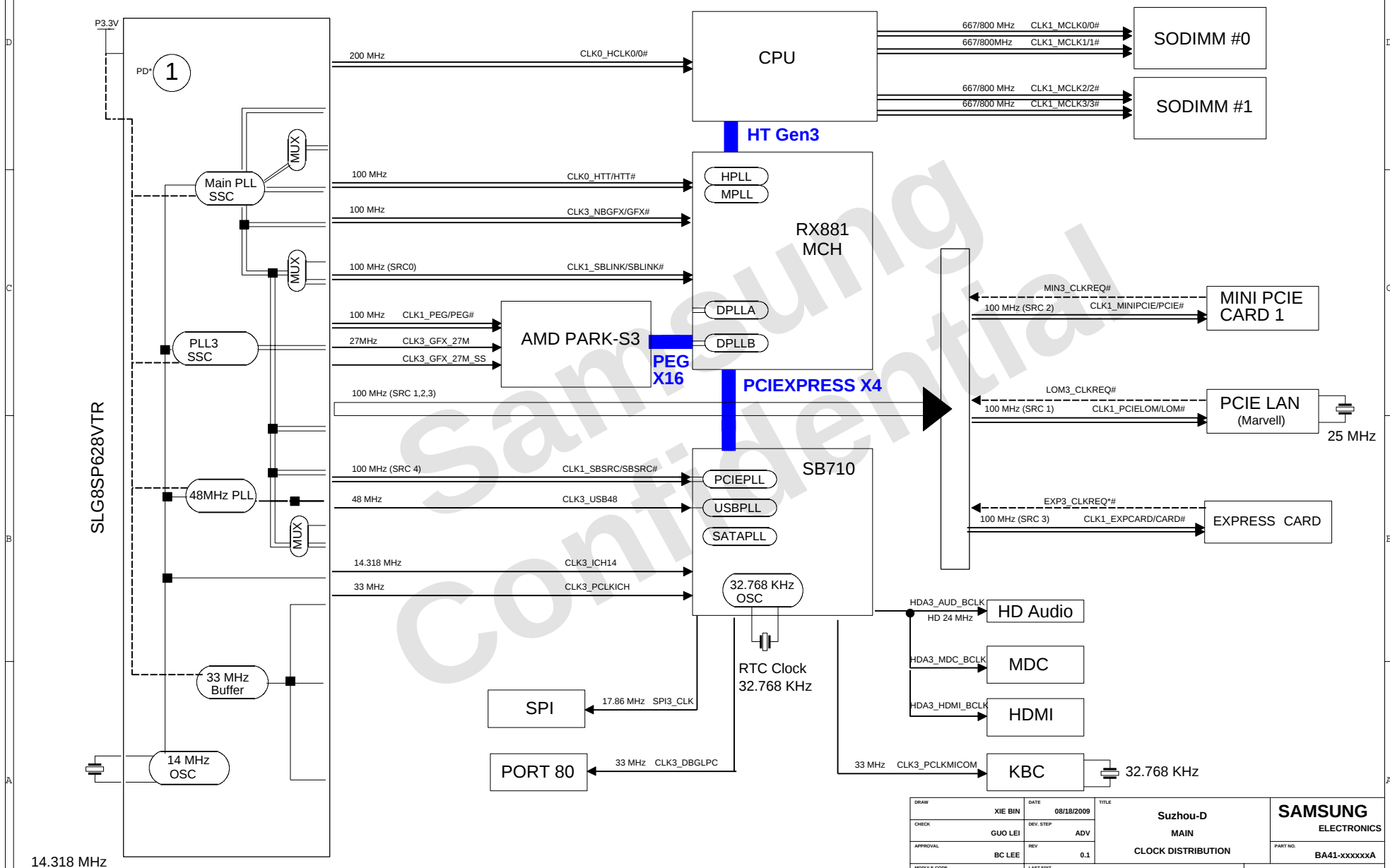
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MODULE CODE		LAST EDIT				
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Timing Diagram, Power ON Rev..1.0 2009-08-27



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CHECK	GUO LEI	DEV. STEP	ADV	MAIN		ELECTRONICS
APPROVAL	BC LEE	REV	0.1	TIMING DIAGRAM	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	6	OF 58

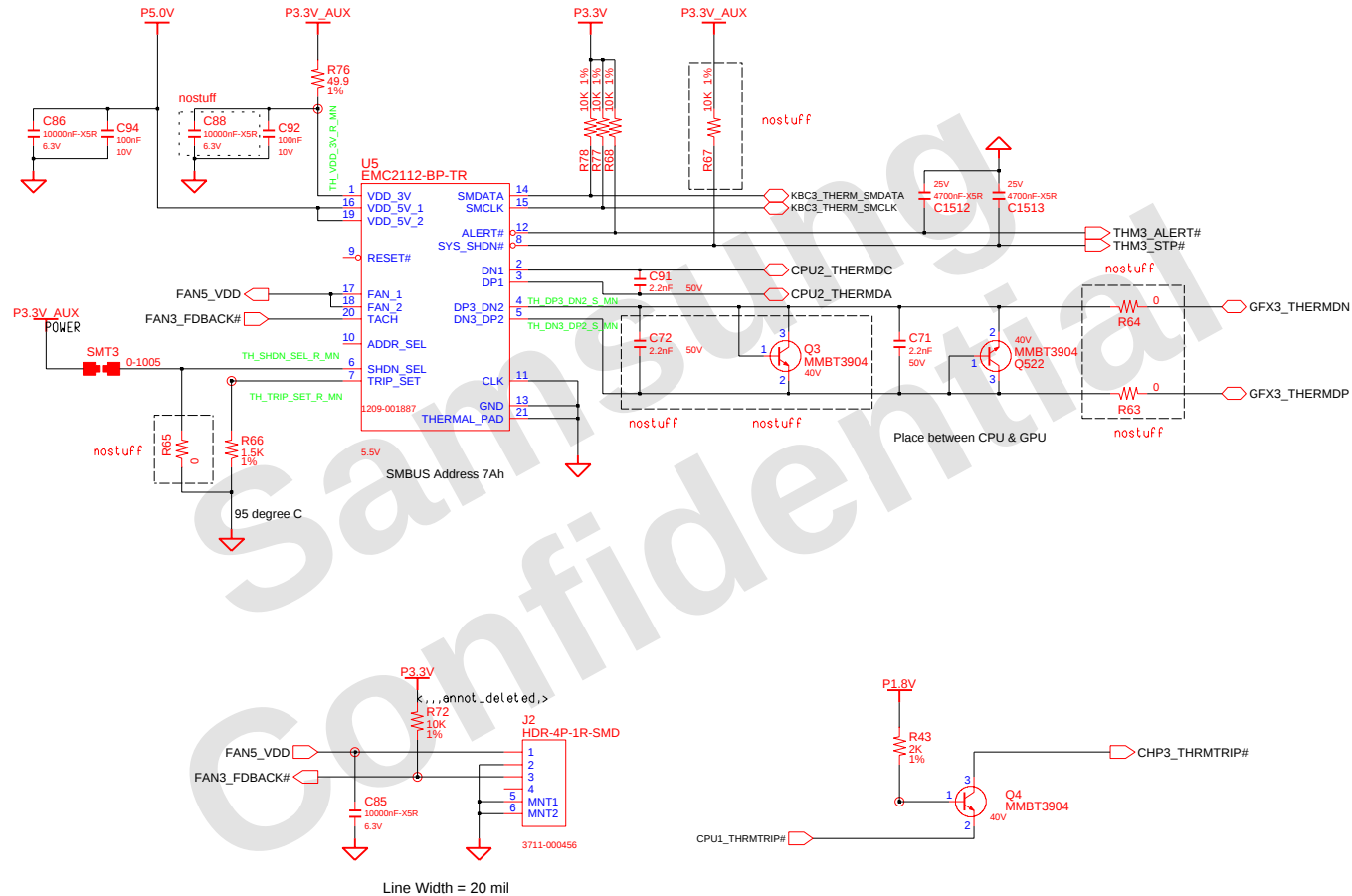
CLOCK DISTRIBUTION



14.318 MHz

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	MAIN	MAIN	ELECTRONICS
APPROVAL	BC LEE	REV	0.1	CLOCK DISTRIBUTION	PART NO.	BA41-xxxxxxA
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THERMAL SENSOR & FAN CONTROL



SHDN_SEL MODE	
0	CH1(CPU MODE)
HIGH Z	CH3(DIODE MODE)
1	N/A (SHDN# NOT USED)

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV		THERMAL SENSOR	ELECTRONICS
APPROVAL	BC LEE	REV	0.1		EMC2112	PART NO.
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	8	BA41-xxxxxxA
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Figure 500-4



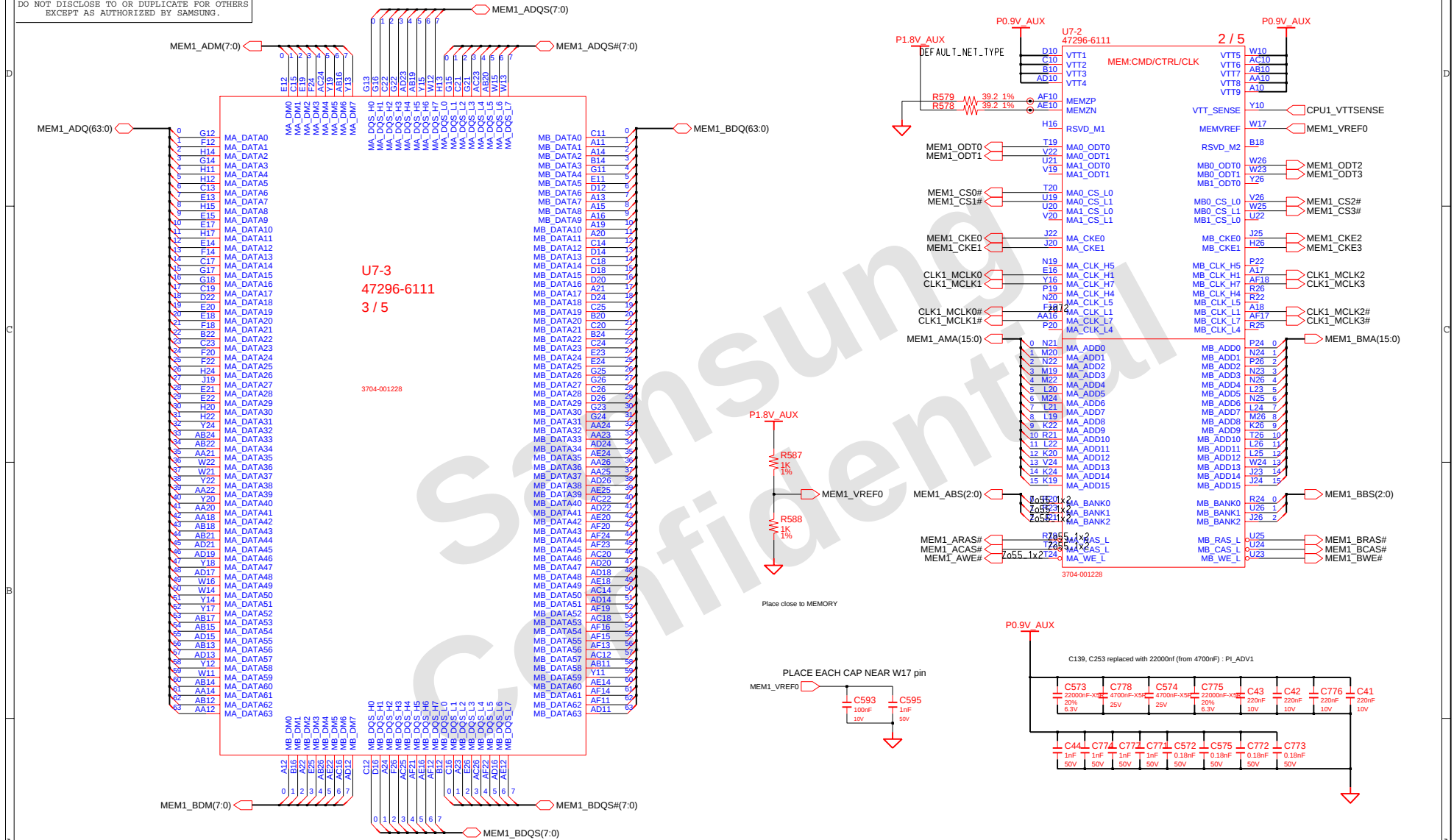
CLK REQ	DEVICE	SRC PORT
CLK REQ 0	-	SB Link
CLK REQ 1	LOM3_CLKREQ#	LOM
CLK REQ 2	MIN3_CLKREQ#	MINI CARD
CLK REQ 3	EXP3_CLKREQ#	EXP CARD
CLK REQ 4	-	SB_SRC

SEL_HTT66	(Pin 59)	1 0 *	66MHz 3.3V single HTT clock 100MHz differential clock
SEL_SATA	(Pin 58)	1 0 *	SRC6 diff. clock 100MHz spreading diff. clock
SEL_27M	(Pin 57)	1 ^a 0	27MHz/27MHz_SS graphics clock SRCHZ diff. clock

This part is 64pin QFN package.

SB710 : 1.1V (OSC_14MHz)

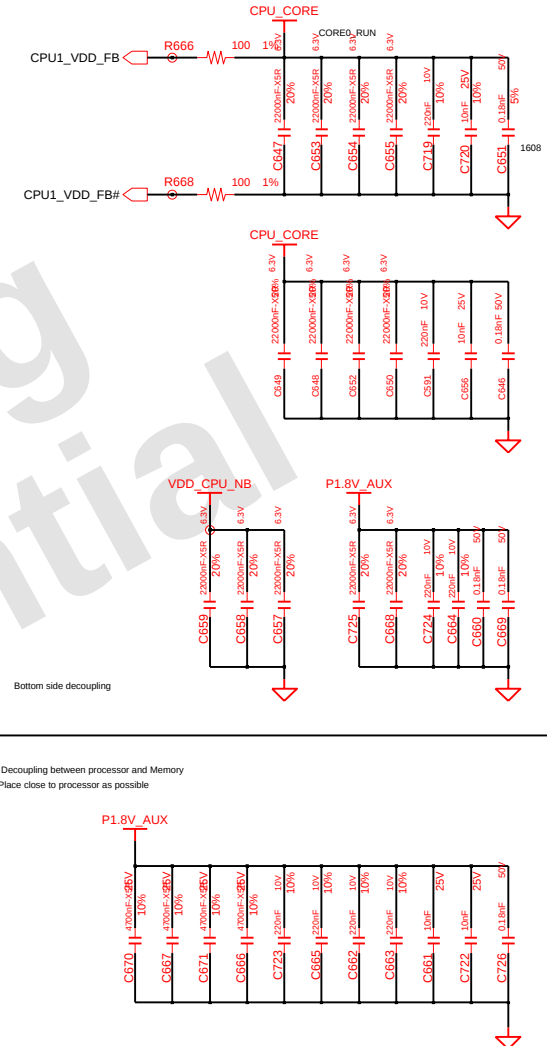
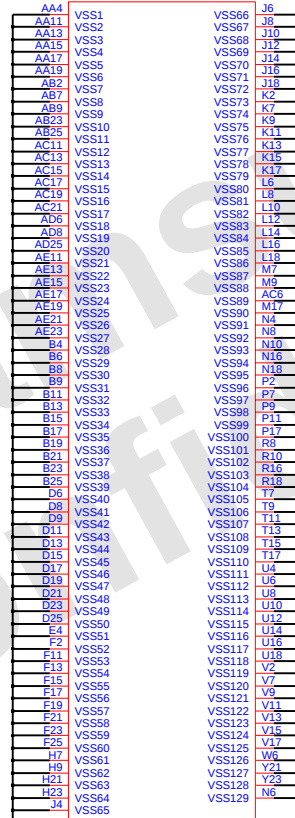
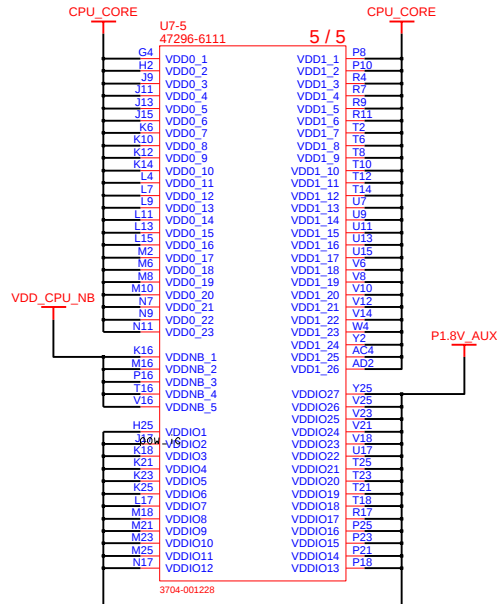
CPU_Caspian



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D
CHECK	GUO LEI	DEV. STEP	ADV	Caspian CPU	
APPROVAL	BC LEE	REV	0.1	S1G3 CPU (2/3)	
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	11 OF 58

SAMSUNG ELECTRONICS	
PART NO.	BA41-xxxxxA

CPU_Caspian



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV		Caspian CPU	ELECTRONICS
APPROVAL	BC LEE	REV	0.1		S1G3 CPU (3/3)	PART NO.
MODULE CODE		LAST EDIT				BA41-xxxxxxA
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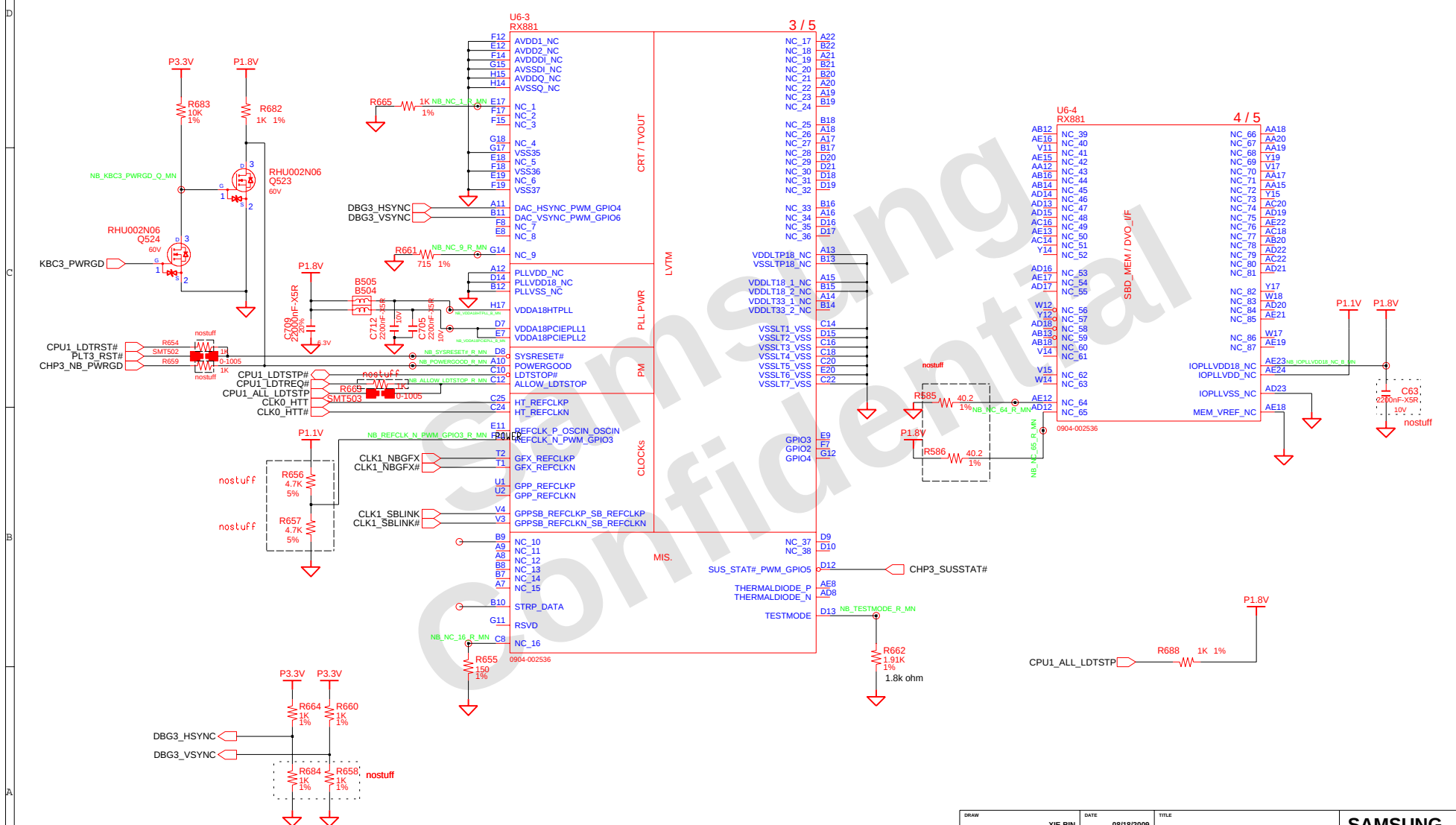
RX780 / RD780 : 1.21K ohm (for S3 issue in D/T chipset)

! nostuff

COM-22C-015(1996.6.5) REV. 3

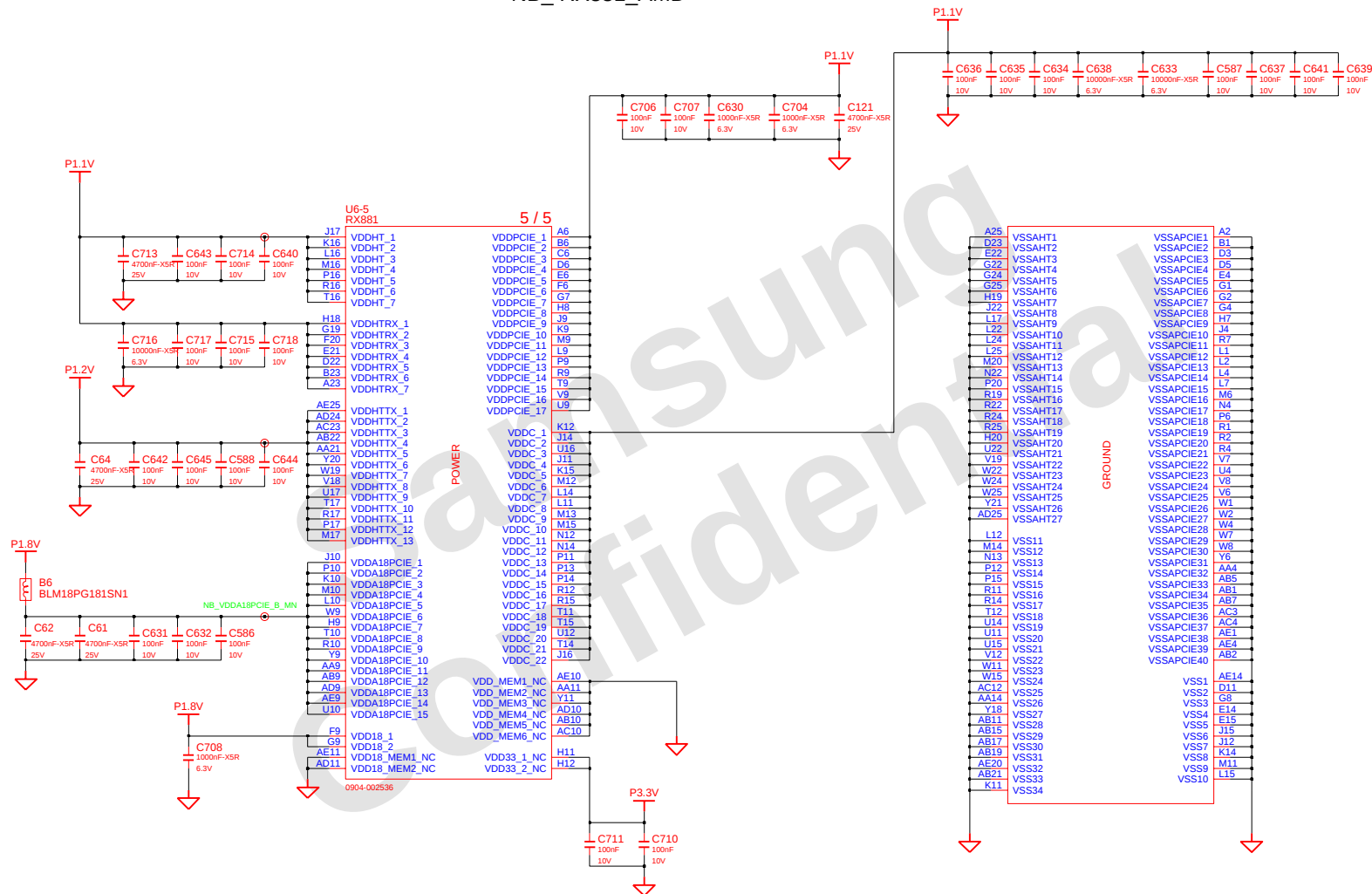
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NB RX881 AMD

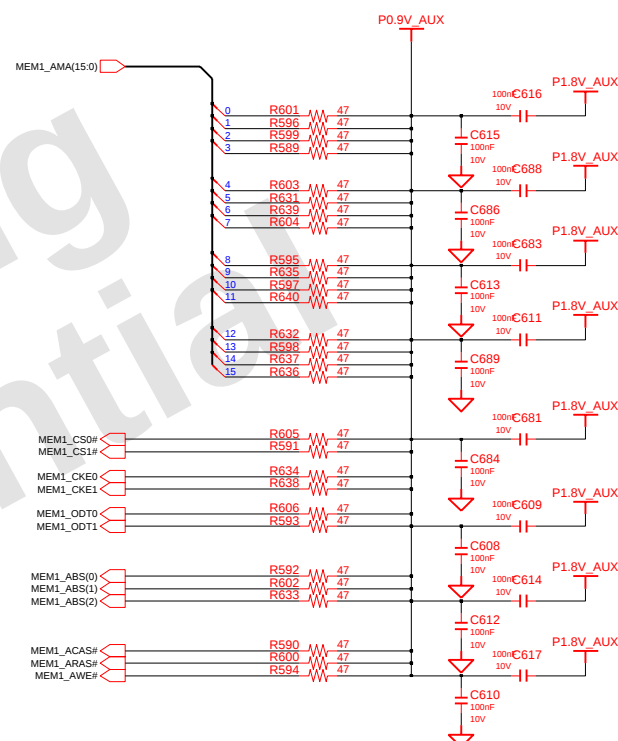


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APPROVAL	BC LEE	REV	0.1		
PART NO. BA41-xxxxxxA					
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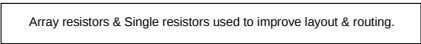
NB_RX881_AMD



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	GUO LEI	DEV. STEP	ADV	MCH		
APPROVAL	BC LEE	REV	0.1	RX881 (3/3)		
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE 15 OF 58	



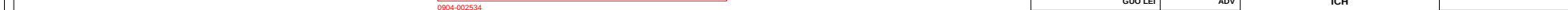
COM-22C-015 (1996.6.5) REV. 3



COM-22C-015(1996.6.5) REV. 3

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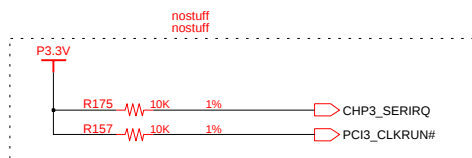
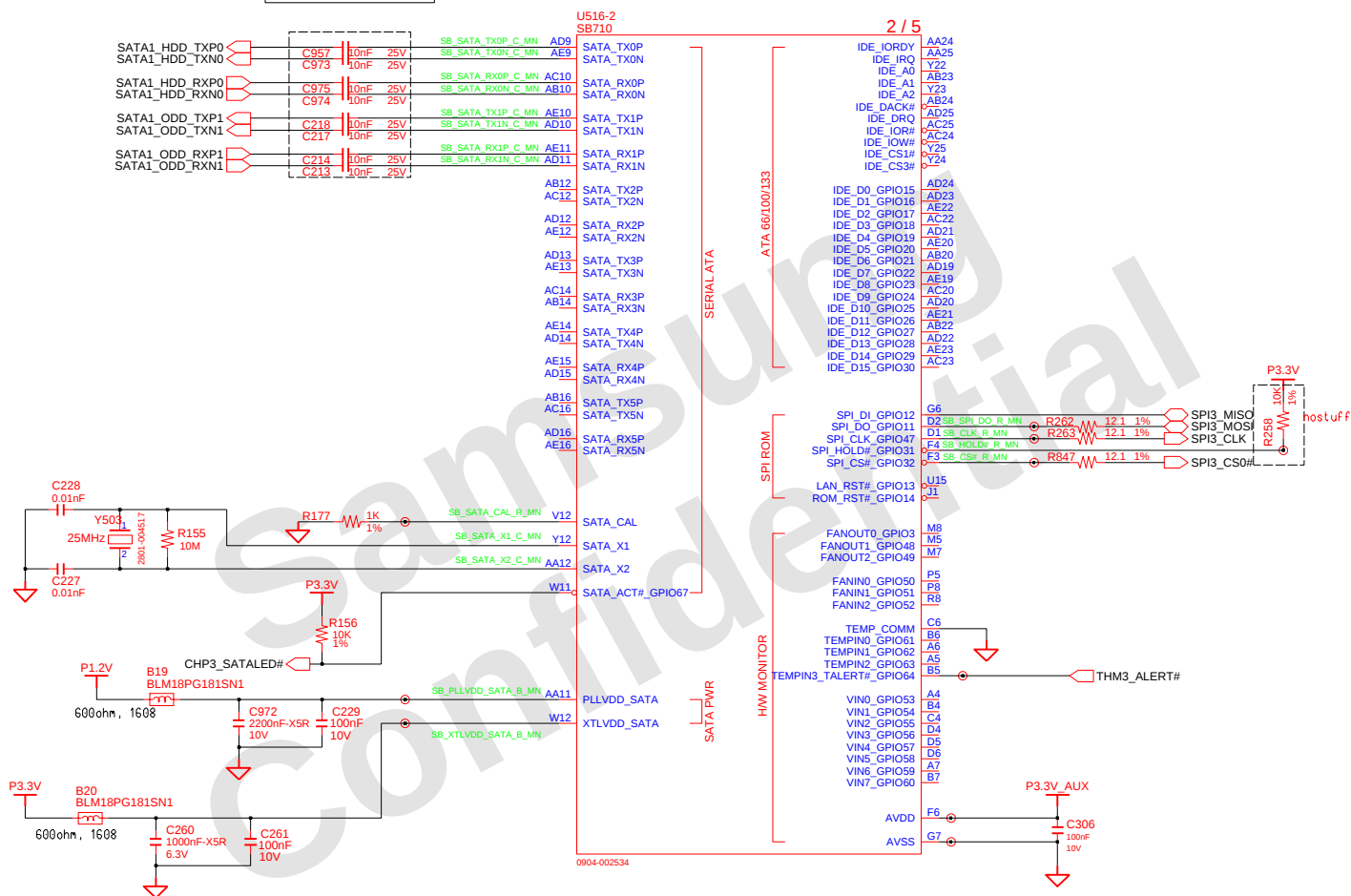
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Route to connector side closely



LPC option ; These are used with LPC

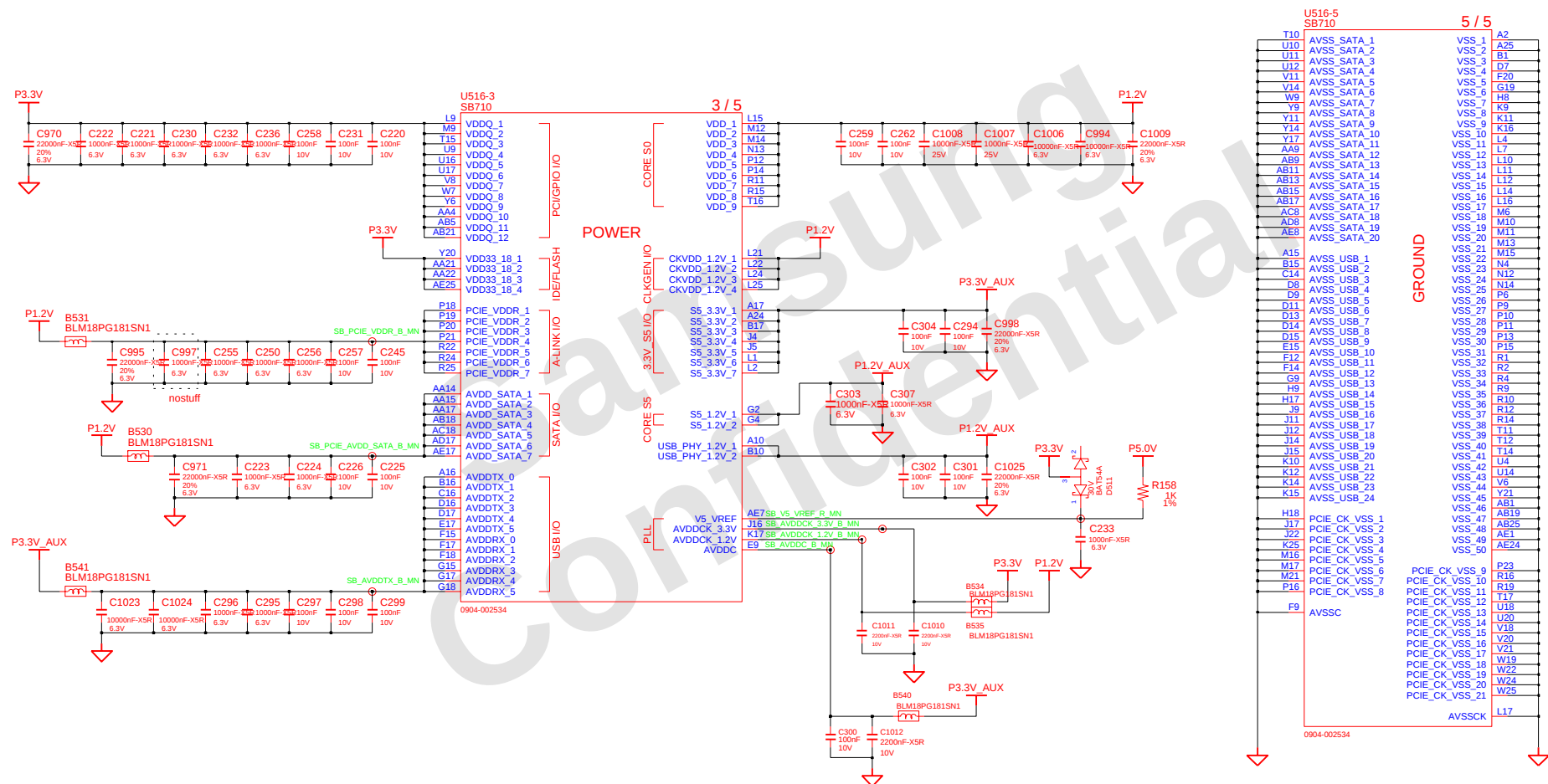
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CHECK	GUO LEI	DEV. STEP	ADV		
APPROVAL	BC LEE	REV	0.1		
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DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D ICH SB710 (3/5)			
CHECK	GUO LEI	DEV. STEP	ADV		PART NO.		
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SB 710 AMD

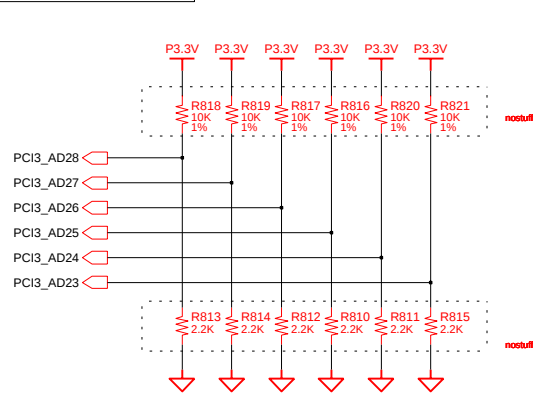


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D ICH SB710 (4/5)	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	0.1			
MODULE CODE	LAST EDIT					

Strap

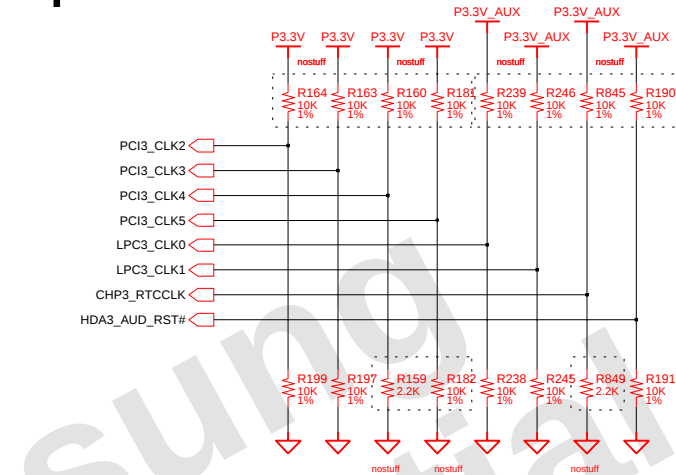
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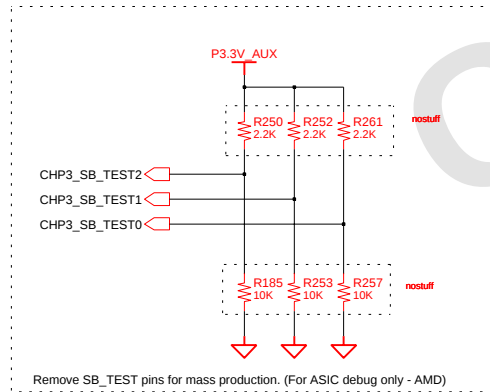


DEBUG STRAPS

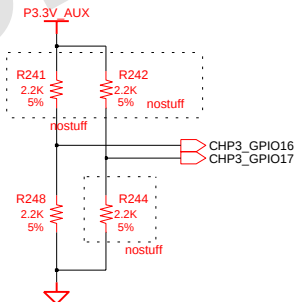
	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED



	PCI3_CLK2	PCI3_CLK3	PCI3_CLK4	PCI3_CLK5	LPC3_CLK0	LPC3_CLK1	RTC_CLK	AUD_RST#
STRAP HIGH	BOOTFAIL TIMER ENABLED	USER DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC	ENABLE PCI MEM BOOT
STRAP LOW	BOOTFAIL TIMER DISABLED	IGNORE DEBUG STRAPS	RESERVED	RESERVED	EC DISABLED	CLKGEN DISABLED	EXRTERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT



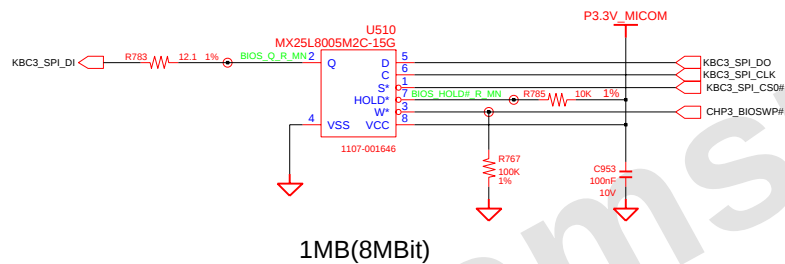
Remove SB_TEST pins for mass production. (For ASIC debug only - AMD)



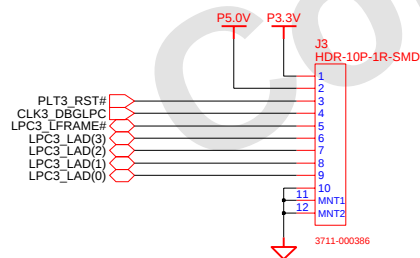
GPIO17	GPIO16
ROM TYPE	
NC, NC = RSVD	
NC, L = SPI ROM	
L, NC = LPC ROM	
L, L = FWH ROM	

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	ICH	ICH	ELECTRONICS
APPROVAL	BC LEE	REV	0.1	SB710 Strap(5/5)	PART NO.	BA41-xxxxxxA
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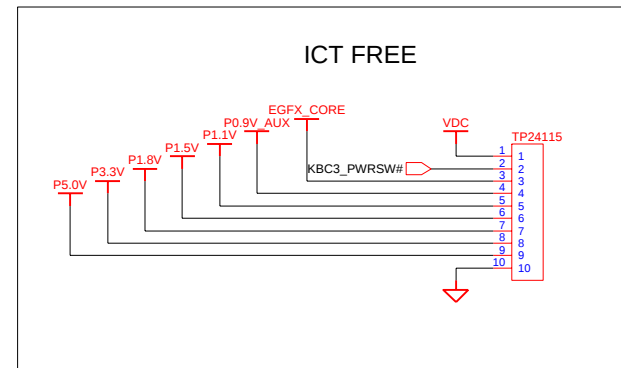
SPI_BIOS_ROM



80H DECODER CONNECTOR



02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
14	WITH INITIAL POST VALUE	88	INIT. BIOS DATA ROM
16	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
18	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
1A	8257 DMA CONTROLLER INIT.	9A	SHADOW OPTION ROMS
1C	RESET INTERRUPT CONTROLLER	9C	SETUP POWER MANAGEMENT
20	TEST DRAM REFRESH	9E	ENABLE H/W INTERRUPT
22	TEST 8742 KEYBOARD CONTROLLER	A0	SET TIME OF DAY
24	SET ES SEGMENT REG. TO 4GB	A4	INIT. TYPEMATIC RATE
26	ENABLE A20	A8	ERASE F2 PROMPT
28	AUTO SIZING DRAM	AA	SCAN FOR F2 KEY STROKE
2A	COMPUTE THE CPU SPEED	AC	ENTER SETUP
2C	TEST CMOS RAM	AE	CLEAR IN POST FLAG
2E	SHADOW SYSTEM BIOS ROM	B0	CHECK FOR ERRORS
30	AUTO SIZING CACHE	B2	POST DONE-PREPARE TO BOOT O/S
32	CONFIGURE ADVANCED CHIPSET REG.	B4	ONE BEEP
34	LOAD ALTER REG. WITH CMOS VALUE	B6	CHECK PASSWORD (OPTION)
36	INIT. INTERRUPT VECTOR	B8	ACPI INIT
38	INIT. BIOS INTERRUPT	BA	DMI INIT
3A	CHECK ROM COPYRIGHT NOTICE	BE	CLEAR SCREEN
3C	INIT. I20 SUPPORT IF INSTALLED	C0	TRY BOOT WITH INT19
3E	CHECK VIDEO CONFIGURE AGAINST CMOS	C2	INTERRUPT HANDLER ERROR
40	INIT. PCI BUS AND DEVICE	D2	UNKNOWN INTERRUPT ERROR
42	INIT. ALL VIDEO BIOS ROM	D4	PENDING INTERRUPT ERROR
44	SHADOW VIDEO BIOS ROM	D6	SHUTDOWN 5
46	DISPLAY CPU TYPE AND SPEED	DA	SHUTDOWN ERROR
48	TEST KEYBOARD	DC	EXTENDED BLOCK MOVE
4A	SET KEYCLICK IF ENABLED	DE	SHUTDOWN 10
4C	ENABLE KEYBOARD	E0	ENABLE NMI
4E	TEST FOR UNEXPECTED INTERRUPTS	89	INIT. HDD CONTROLLER
50	DISPLAY " PRESS... SETUP"	90	INIT. LOCAL BUS HDD CONTROLLER
52	TEST RAM BETWEEN 512K AND 640K	92	JUMP TO USER PATCH 2
54	TEST EXTENDED MEMORY	94	DISABLE A20 ADDRESS LINE
56	TEST EXTENDED MEMORY ADDRESS LINE	96	CLEAR HUGE ES SEGMENT REG.
58	JUMP TO USER PATCH 1	98	SEARCH FOR OPTION ROMS

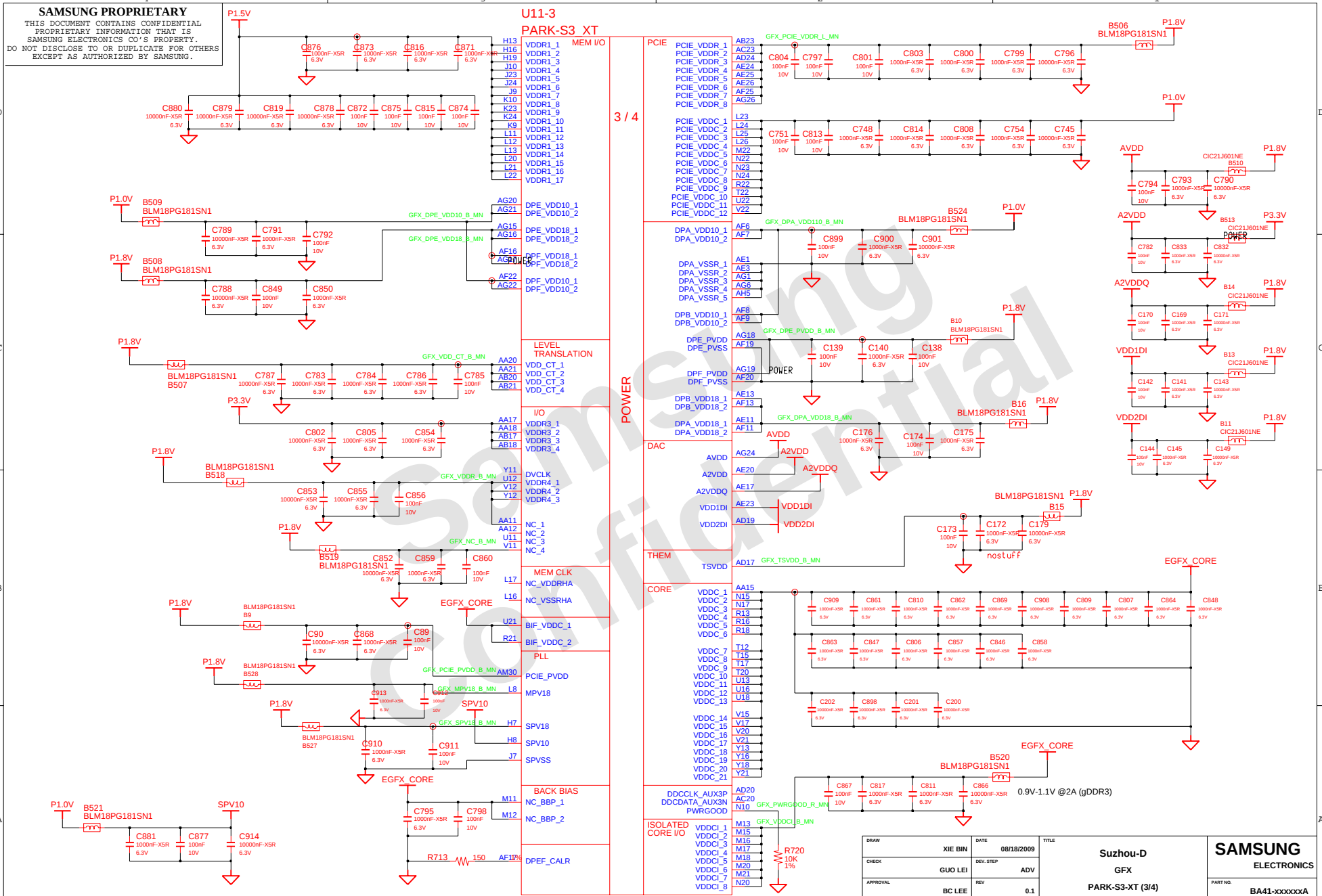


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV		SPI_BIOS_ROM	ELECTRONICS
APPROVAL	BC LEE	REV	0.1		SPI_BIOS_ROM	PART NO.
MODULE CODE		LAST EDIT				BA41-xxxxxA
				July 15, 2009 19:25:13 PM	PAGE	23 OF 58

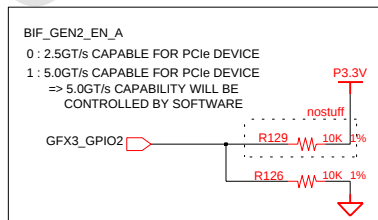
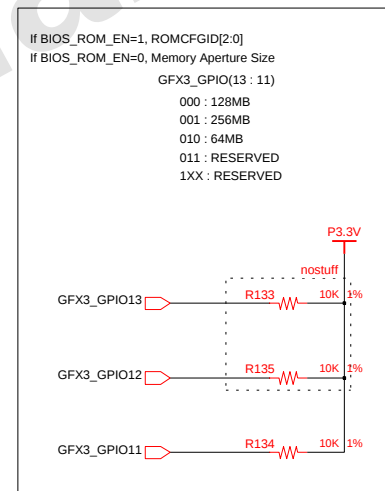
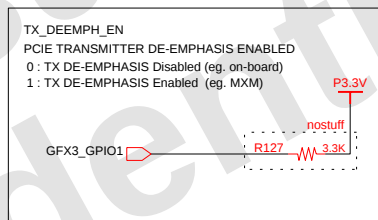
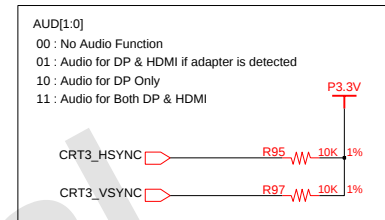
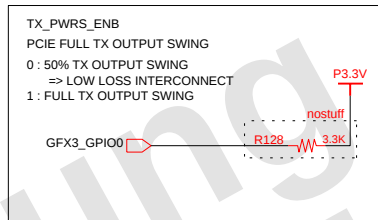
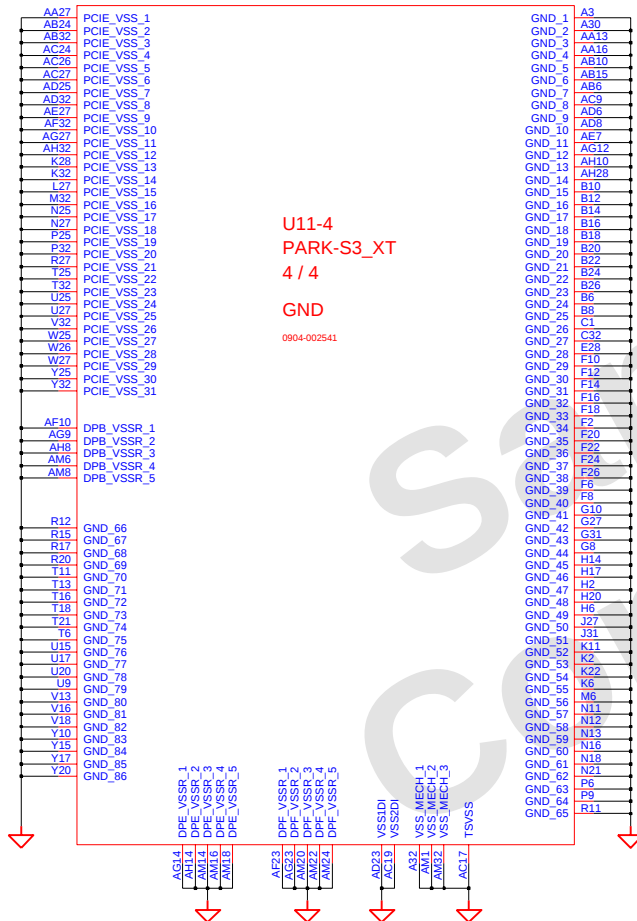
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D:/Users/mentor/Suzhou-D/Suzhou-D_adv1_0826

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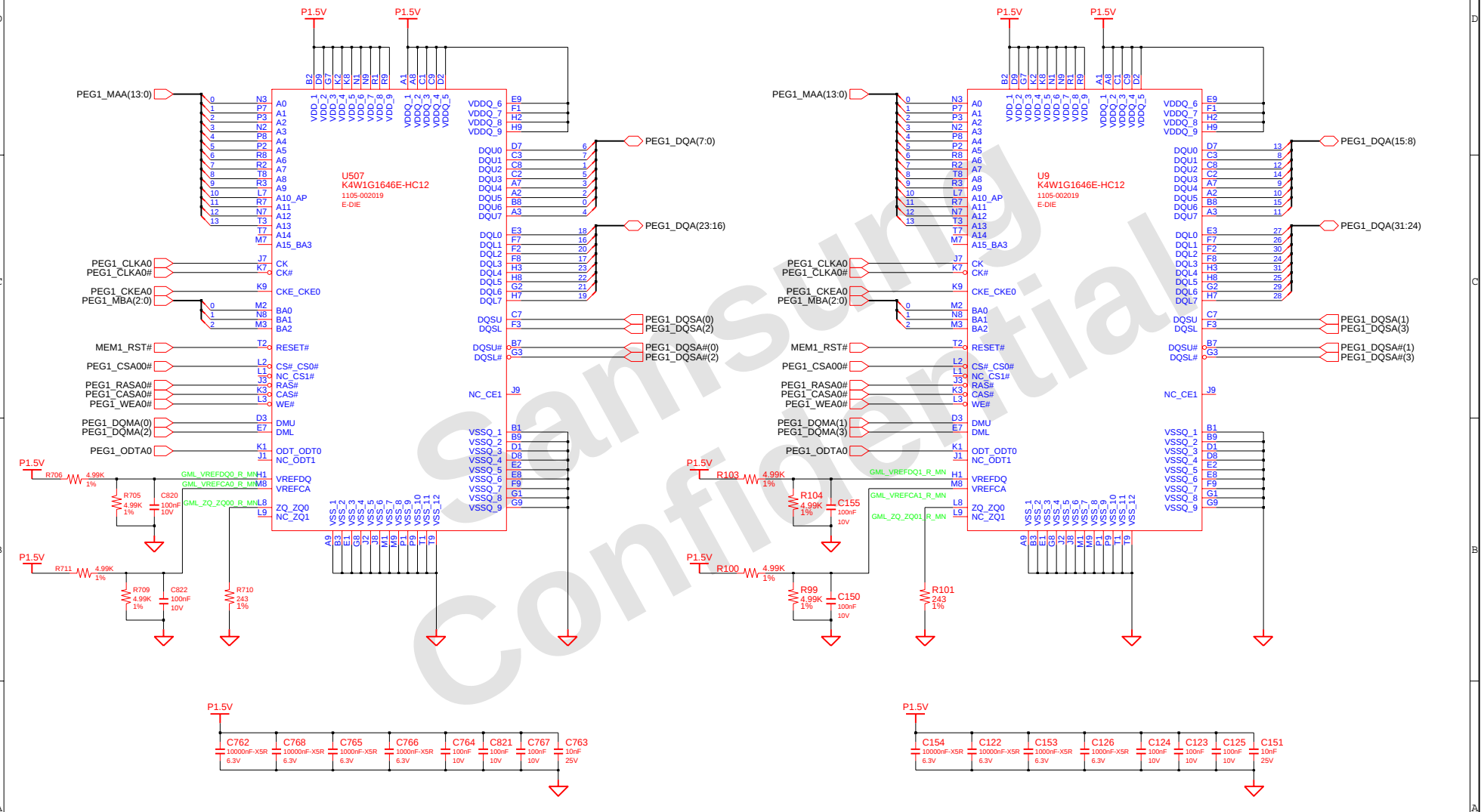


PARK Straps



DRAW		XIE BIN		DATE	08/18/2009		TITLE		Suzhou-D		SAMSUNG ELECTRONICS				
CHECK		GUO LEI		DEV. STEP		ADV		GFX							
APPROVAL		BC LEE		REV		0.1		PARK-S3-XT (4/4)		PART NO.		BA41-xxxxxxA			
MODULE CODE				LAST EDIT				July 15, 2009 19:25:13 PM				PAGE	27	OF	58

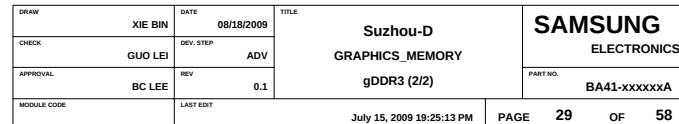
A-channel Lower Data



PEG1_CLKA0 $\rightarrow$ R708 $\rightarrow$ 56 1% $\rightarrow$ C823 $\rightarrow$ 10nF $\rightarrow$ PEG1_CLKA0_R_MN
PEG1_CLKA0# $\rightarrow$ R707 $\rightarrow$ 56 1% $\rightarrow$ PEG1_CLKA0_R_MN

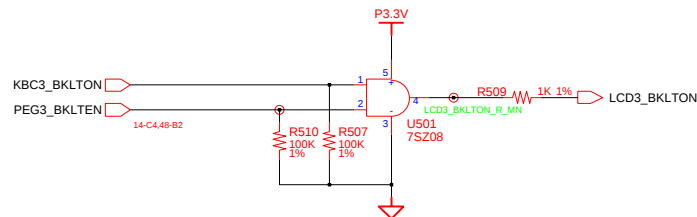
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	GRAPHICS_MEMORY		
APPROVAL	BC LEE	REV	0.1	gDDR3 (1/2)	PART NO. BA41-xxxxxA	
MODULE CODE		LAST EDIT				
July 15, 2009 19:25:13 PM						PAGE 28 OF 58

A-channel Upper Data



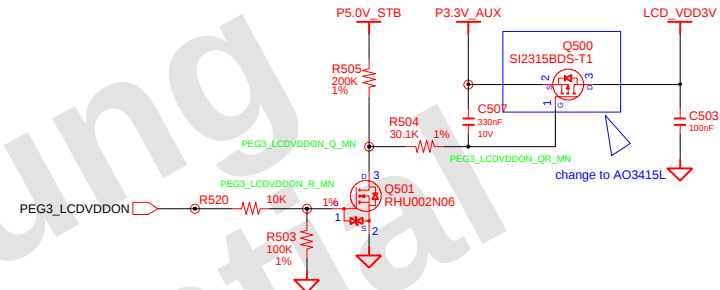
LVDS

Backlight On

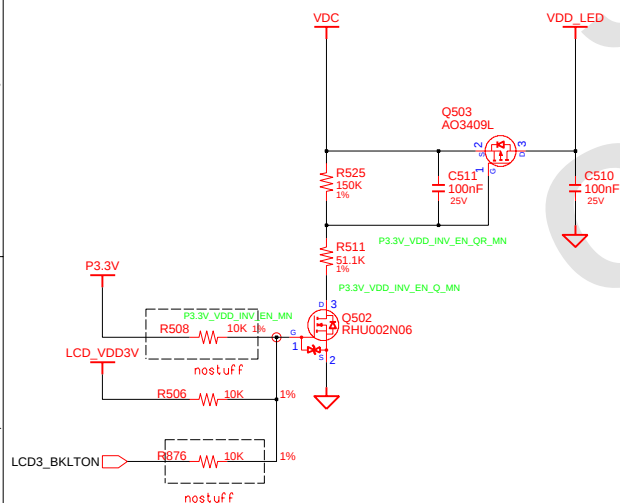


LCD Power

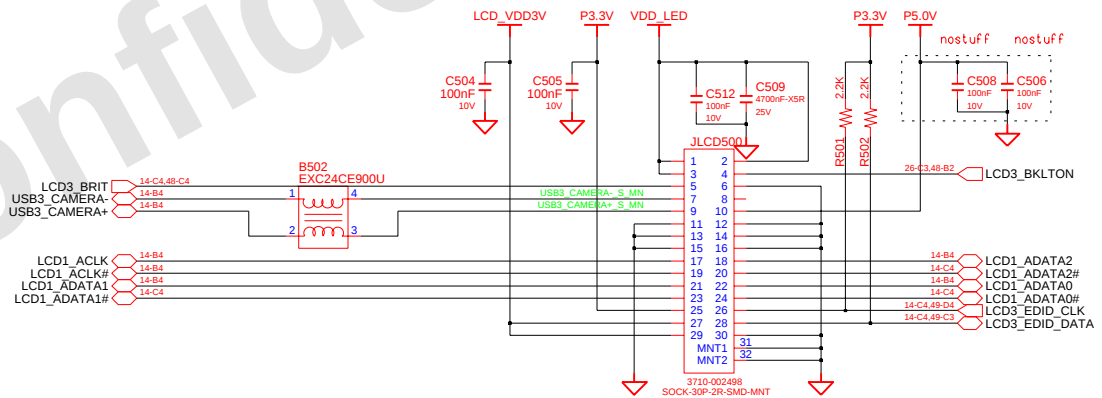
EBL Purpose



Converter Power



Camera + LCD Connector



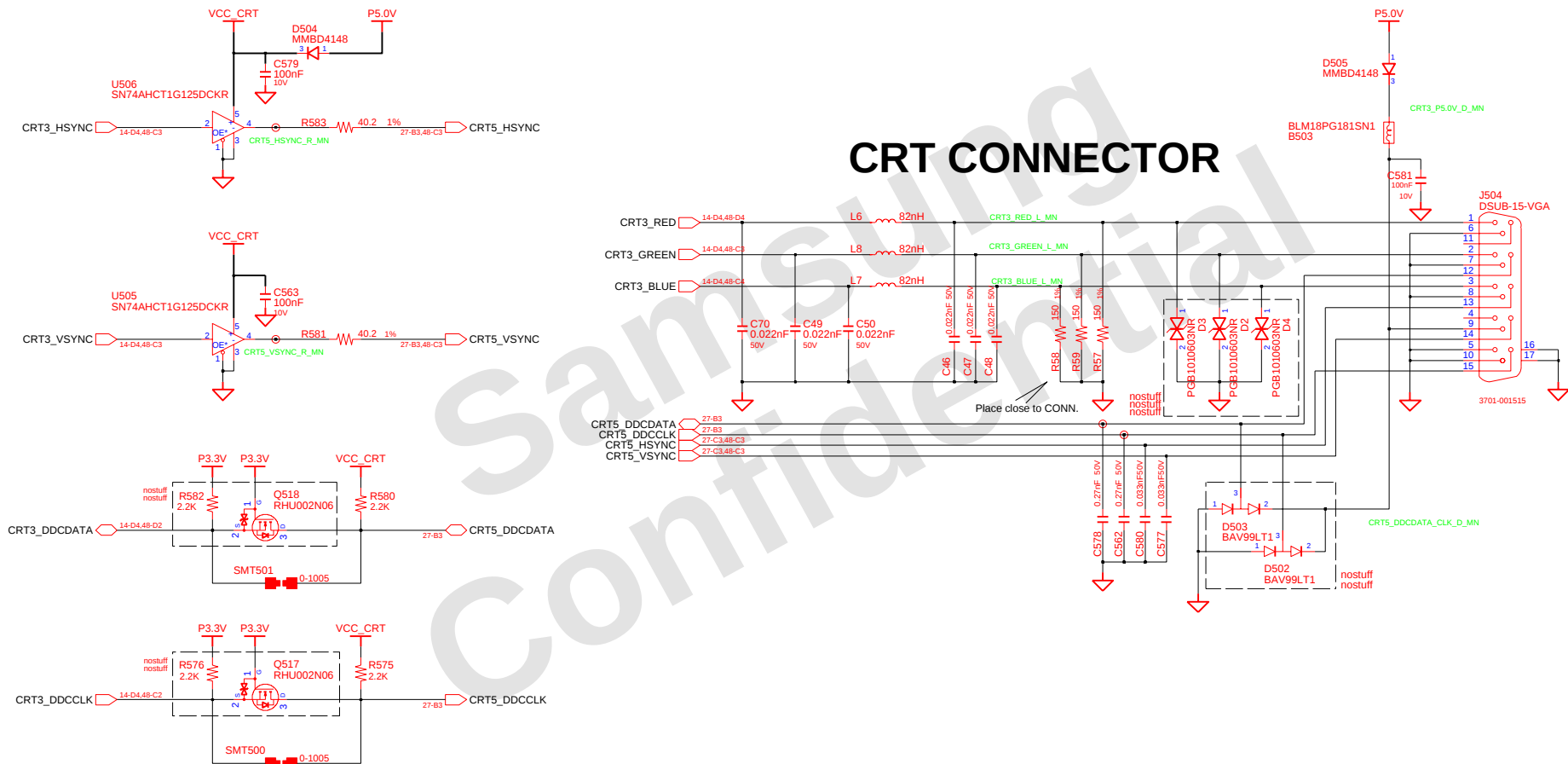
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV			PART NO. BA41-xxxxxxA
APPROVAL	BC LEE	REV	0.1	GRAPHICS_IF (1/2)		
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	30	OF 58

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CRT

CRT CONNECTOR



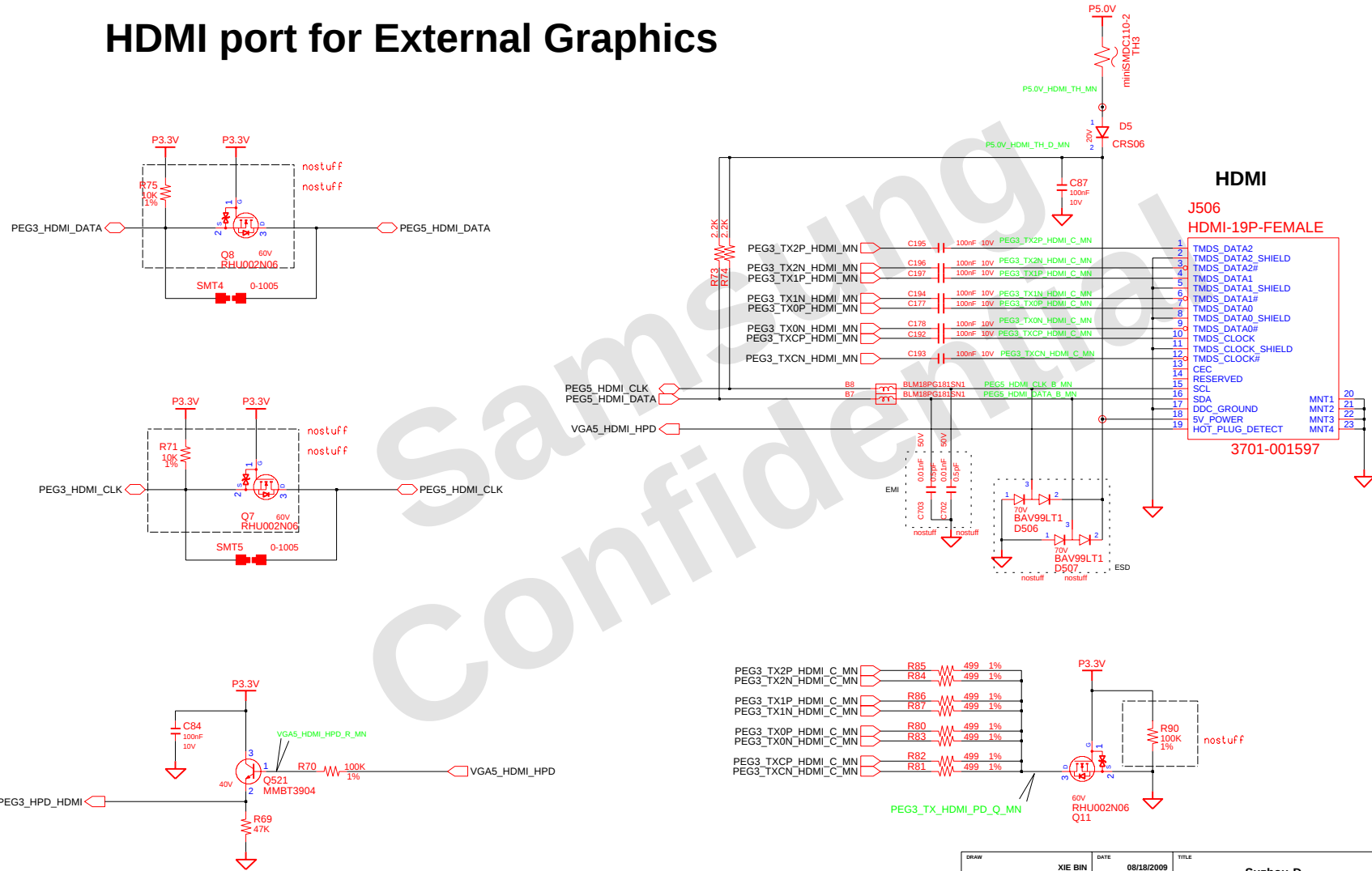
Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	GUO LEI	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	0.1	GRAPHICS_IF (2/2)		
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	31 OF 58	

HDMI

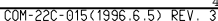
HDMI port for External Graphics

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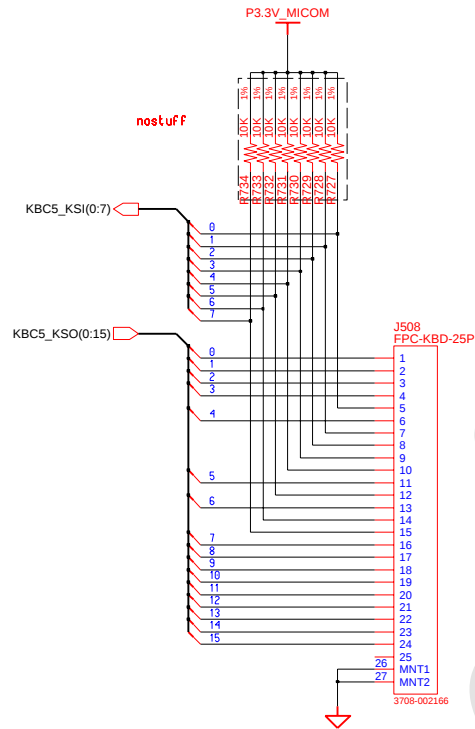
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	GRAPHICS_IF	ELECTRONICS	
APPROVAL	BC LEE	REV	0.1	HDMI	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT				
				July 15, 2009 19:25:13 PM	PAGE	32 OF 58

MICOM MEC1308-NU

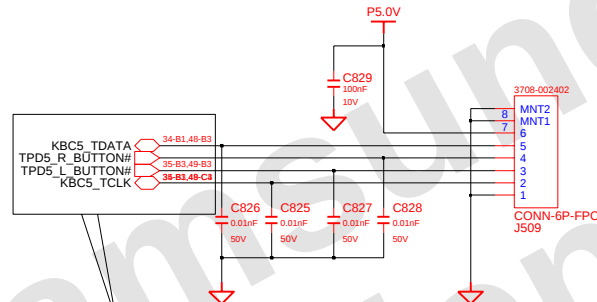
D:/Users/mentor/Suzhou-D/Suzhou-D adv1 0826

Micom Glue Logic

KEYBOARD

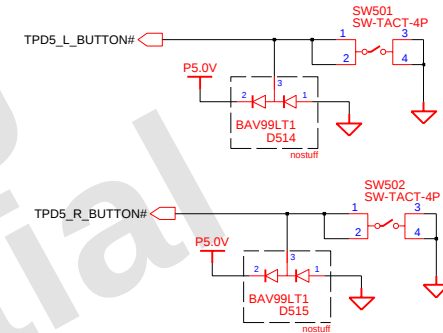


TOUCHPAD

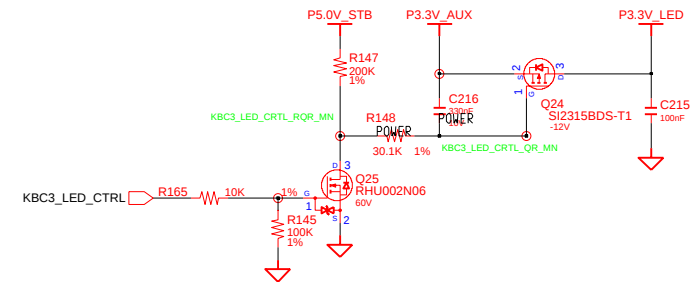


Confirm that there are PU on Touch PAD module side or micom.

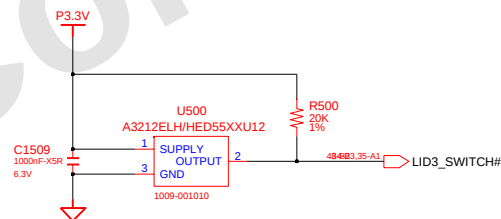
TOUCHPAD BUTTON



TOUCHPAD LED POWER



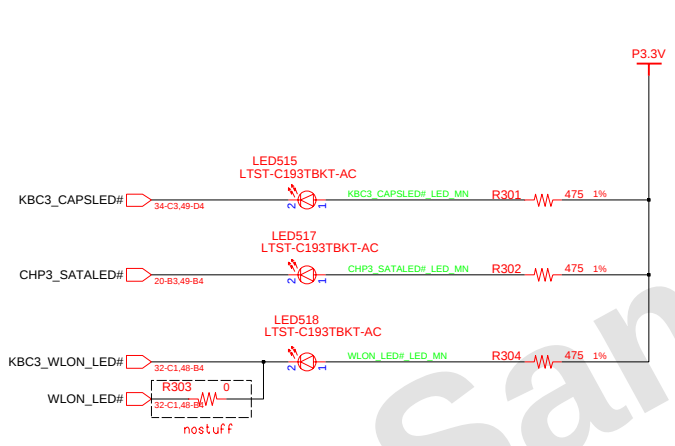
LID SWITCH



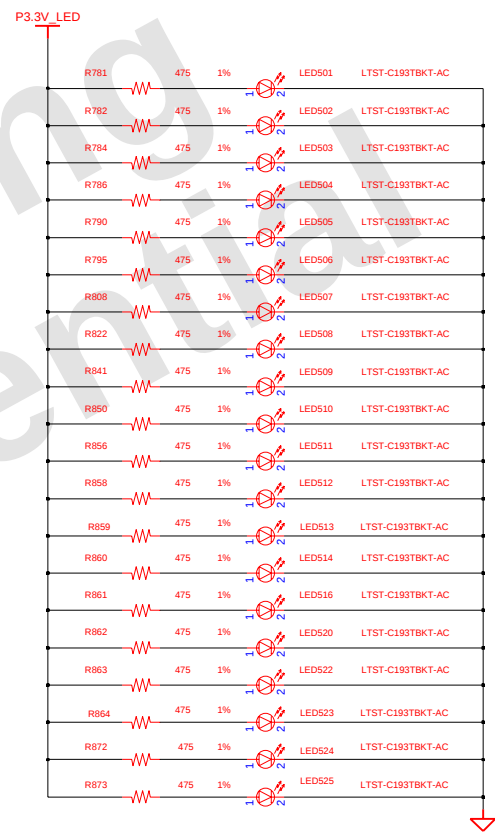
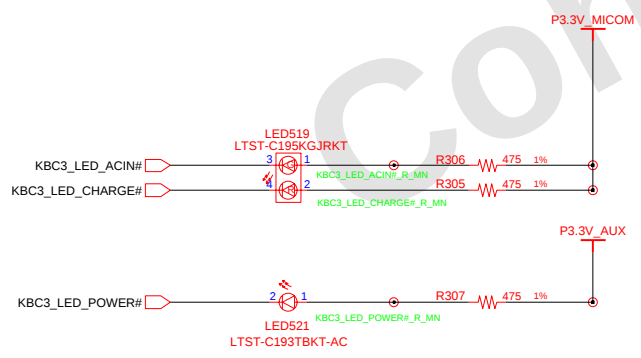
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	0.1	MICOM_GLUE		PART NO. BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	34	OF 58

LEDs

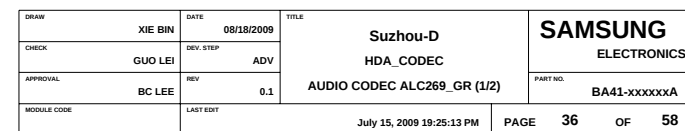
FUNCTION KEY LED



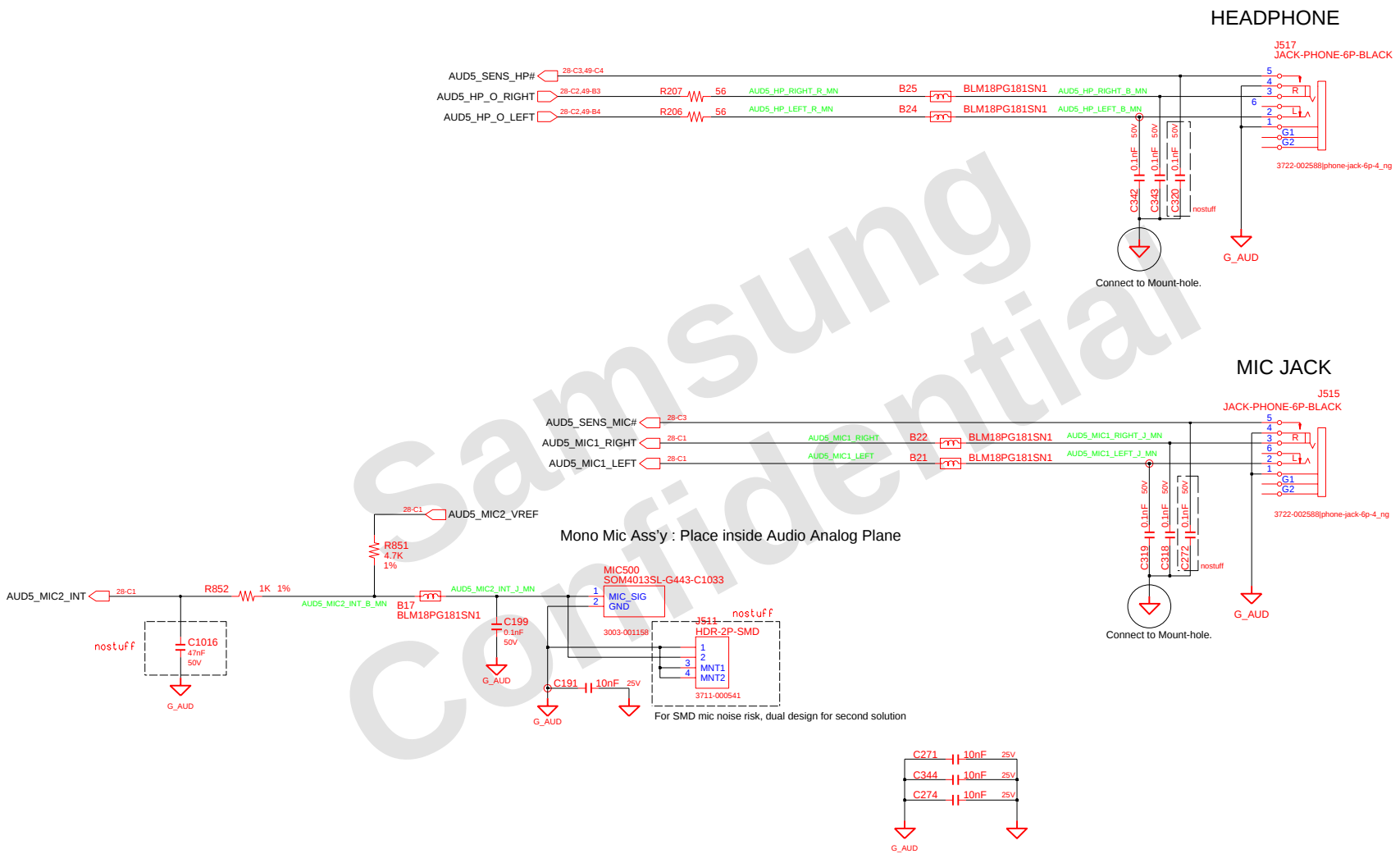
ADAPTERIN/CHARGING LED



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	LED_SWITCH	LED_SWITCH	ELECTRONICS
APPROVAL	BC LEE	REV	0.1			PART NO.
MODULE CODE		LAST EDIT				BA41-xxxxxxA
				July 15, 2009 19:25:13 PM	PAGE	35 OF 58

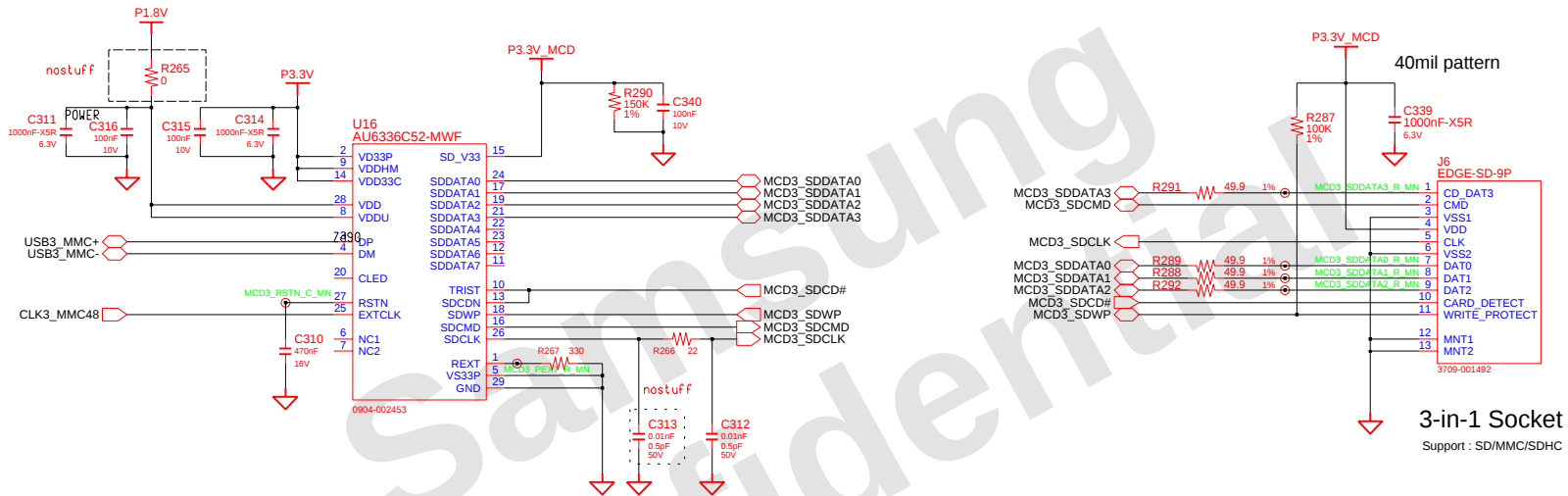


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DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	HDA_CODEC	HDA_CODEC	ELECTRONICS
APPROVAL	BC LEE	REV	0.1	AUDIO CODEC ALC269_GR (2/2)	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	37	OF 58

Card Reader (AU6336)

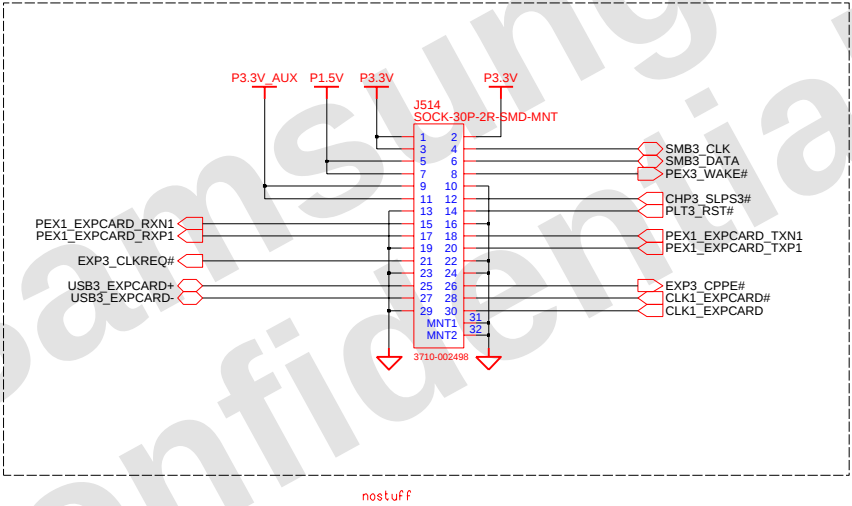


MCD3_SD_SPD	SD v1.0 Clock Option
PU / PD : No Stuff	24 MHz (default)
PU : Stuff, PD : No Stuff	15 MHz

MCD3_CLK_IN	827S Clock Source option
PU : X, PD : X	12MHz, fixed S/N
PU : No Stuff, PD : Stuff	12MHz, no S/N
PU : Stuff, PD : No Stuff	48MHz

DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D MULTICARD 3 IN 1 CARD		SAMSUNG ELECTRONICS				
CHECK	GUO LEI	DEV. STEP	ADV							
APPROVAL	BC LEE	REV	0.1							
				PART NO.		BA41-xxxxxxA				
MODULE CODE		LAST EDIT			July 15, 2009 19:25:13 PM		PAGE	40	OF	58

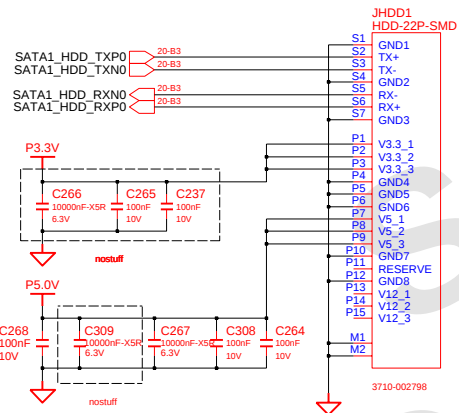
Express Card Connector



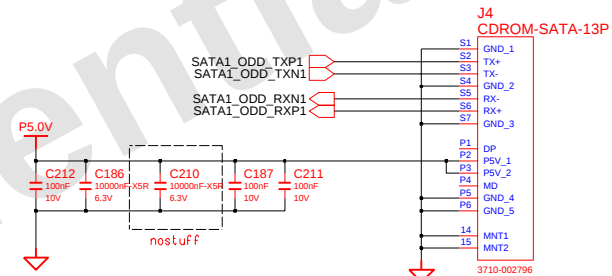
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	0.1	EXPRESS CARD		PART NO. BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	41	OF 58

SATA I/F CONN

SATA HDD CONN

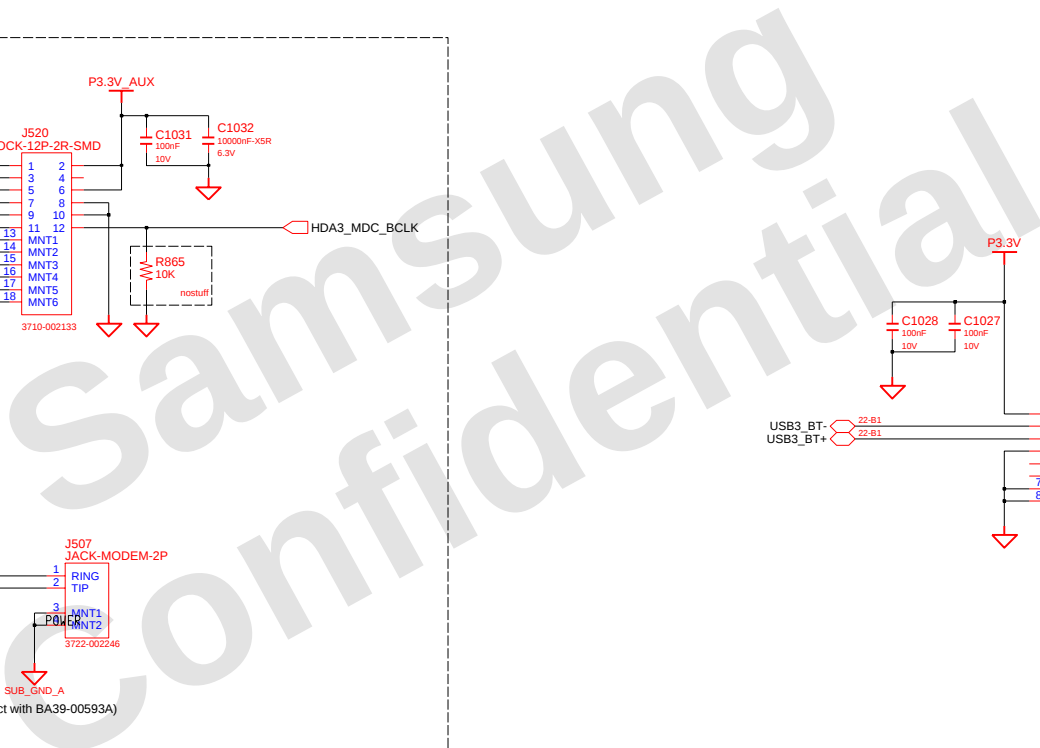


ODD CONN



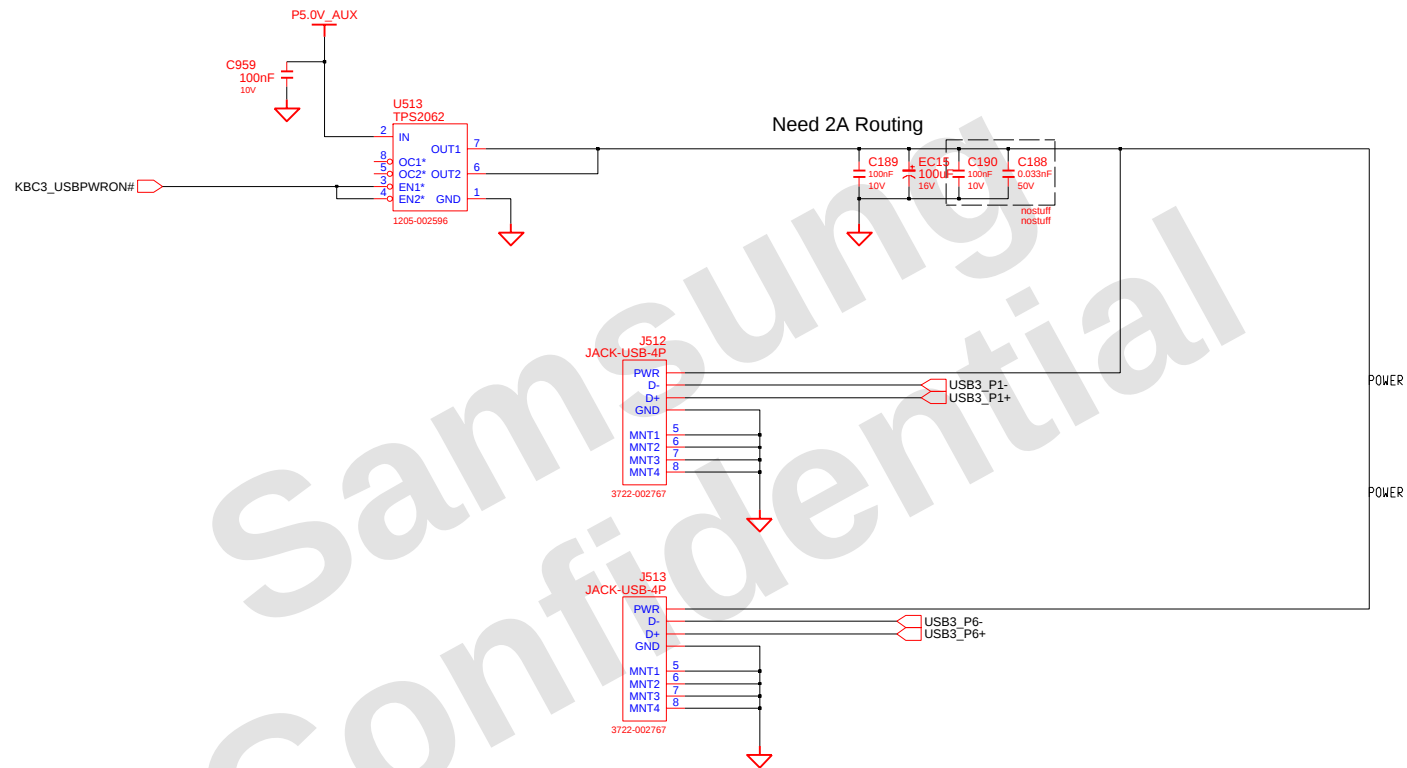
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D SATA_DEVICES HDD & ODD SUB BONNECTOR	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV			PART NO. BA41-xxxxxxA
APPROVAL	BC LEE	REV	0.1			
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE 42 OF 58	

BLUETOOTH



COM-22C-015(1996.6.5) REV. 3

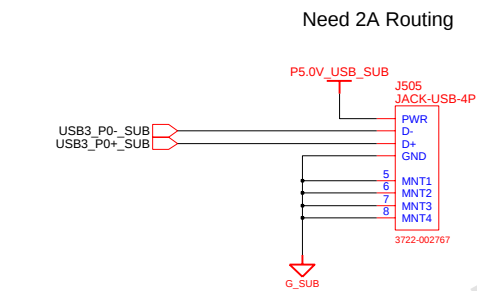
LEFT USB PORT



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	USB_CONNECTOR	USB_CONNECTOR	
APPROVAL	BC LEE	REV	0.1	USB_CONNECTOR (1/2)	PART NO.	BA41-xxxxxxA
MODULE CODE	LAST EDIT				July 15, 2009 19:25:13 PM	PAGE 44 OF 58

USB PORT & POWER S/W SUB B'D

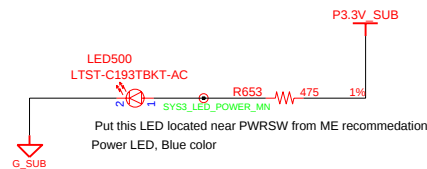
TOP RIGHT USB PORT



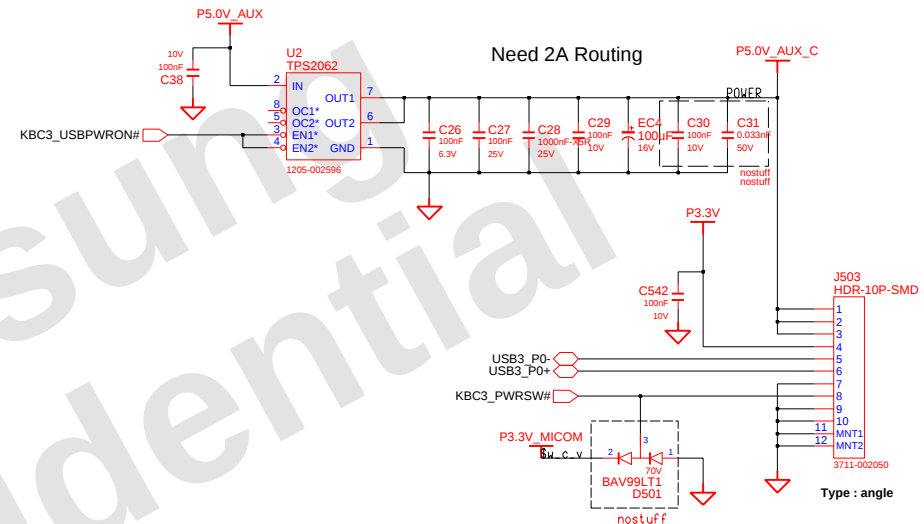
Power Button



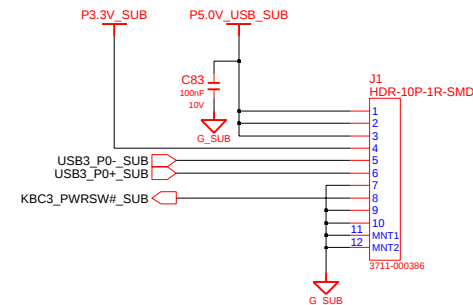
Power ON LED



MAIN TO SUB USB CONN

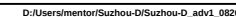


SUB TO MAIN USB CONN

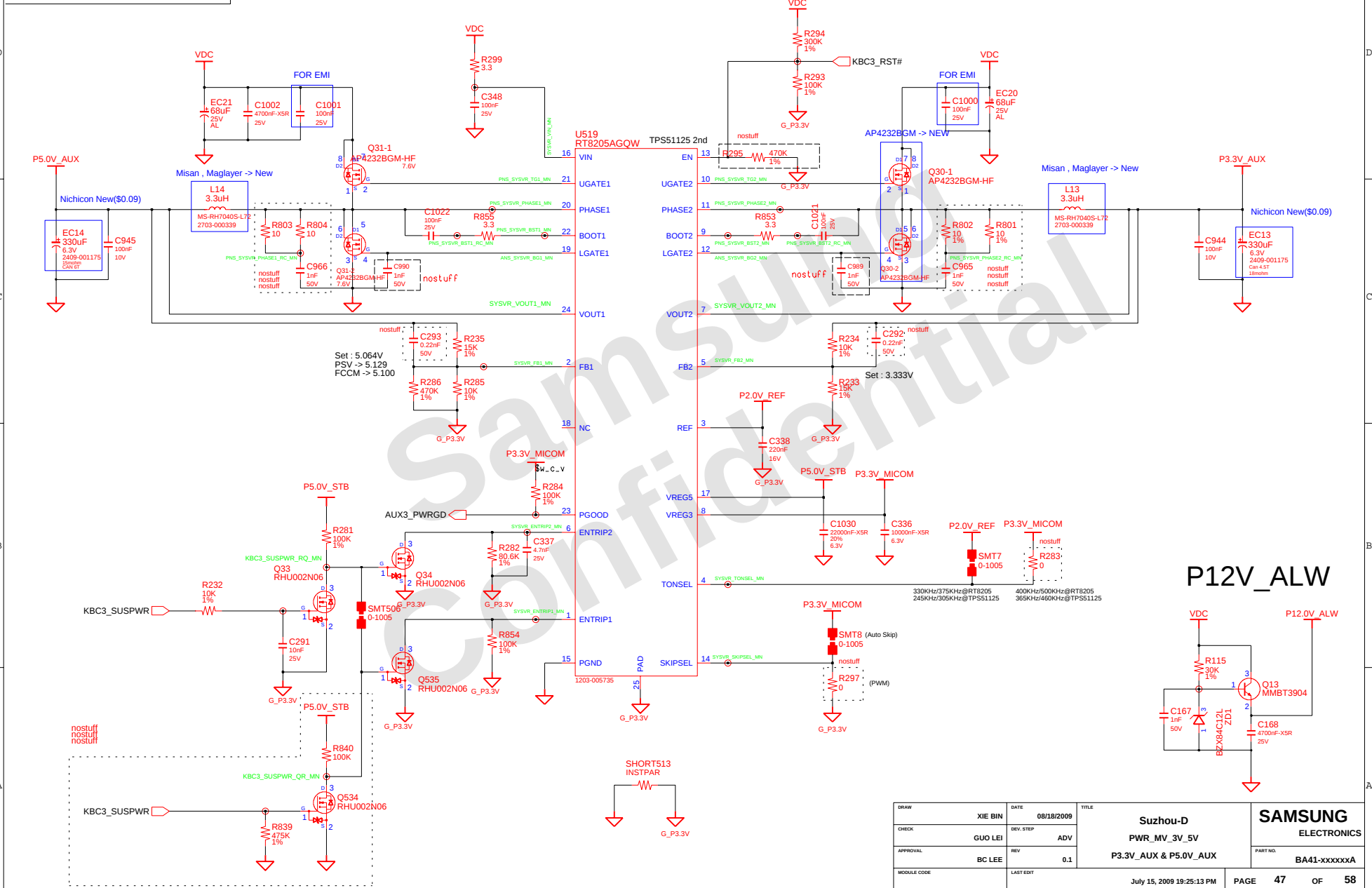


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	USB_CONNECTOR	USB_CONNECTOR	ELECTRONICS
APPROVAL	BC LEE	REV	0.1	USB_CONNECTOR (2/2)	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	45 OF 58

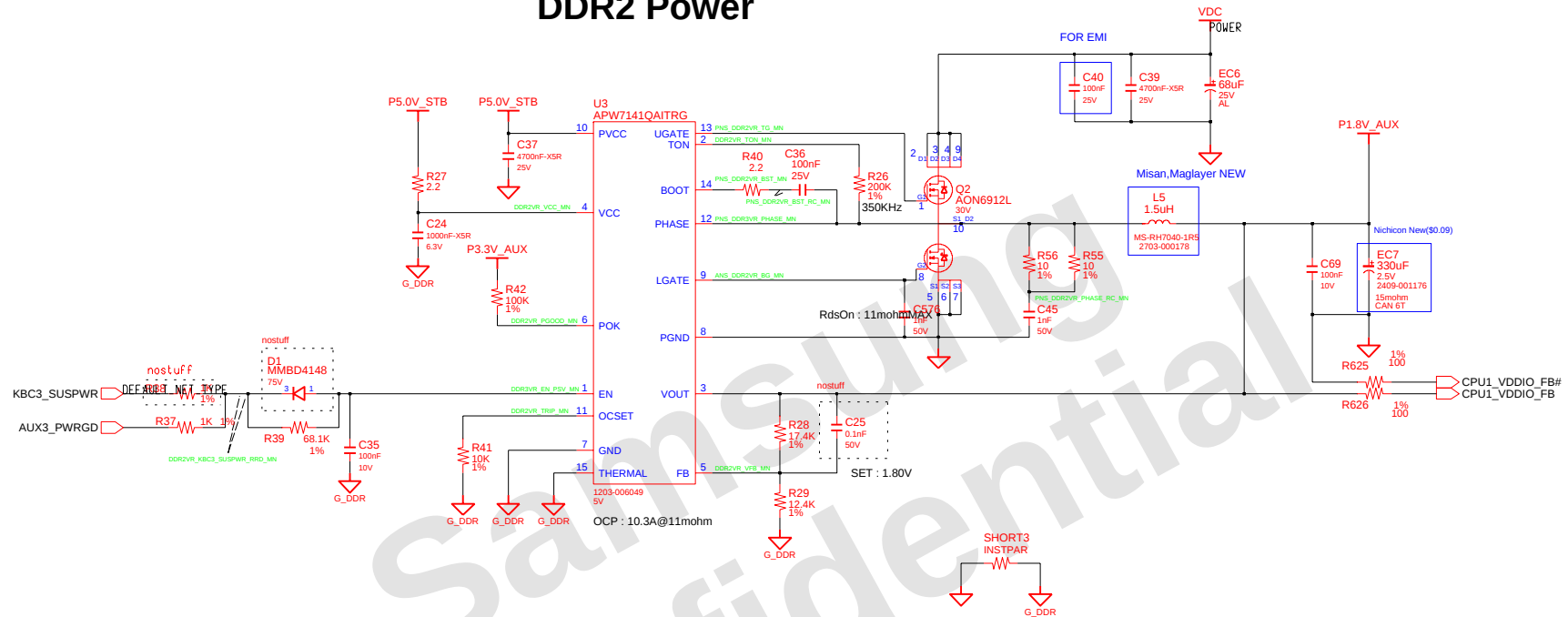
CHARGER & POWER MANAGEMENT



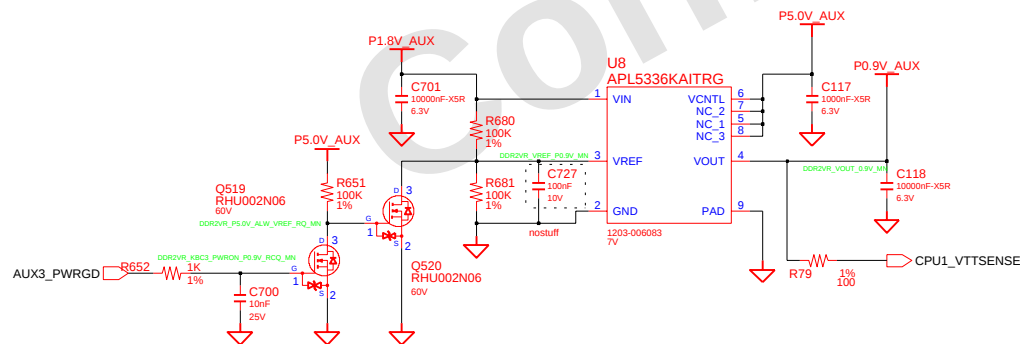
P3.3V_AUX & P5.0V_AUX



DDR2 Power



DDR2 VTT(P0.9V_AUX)

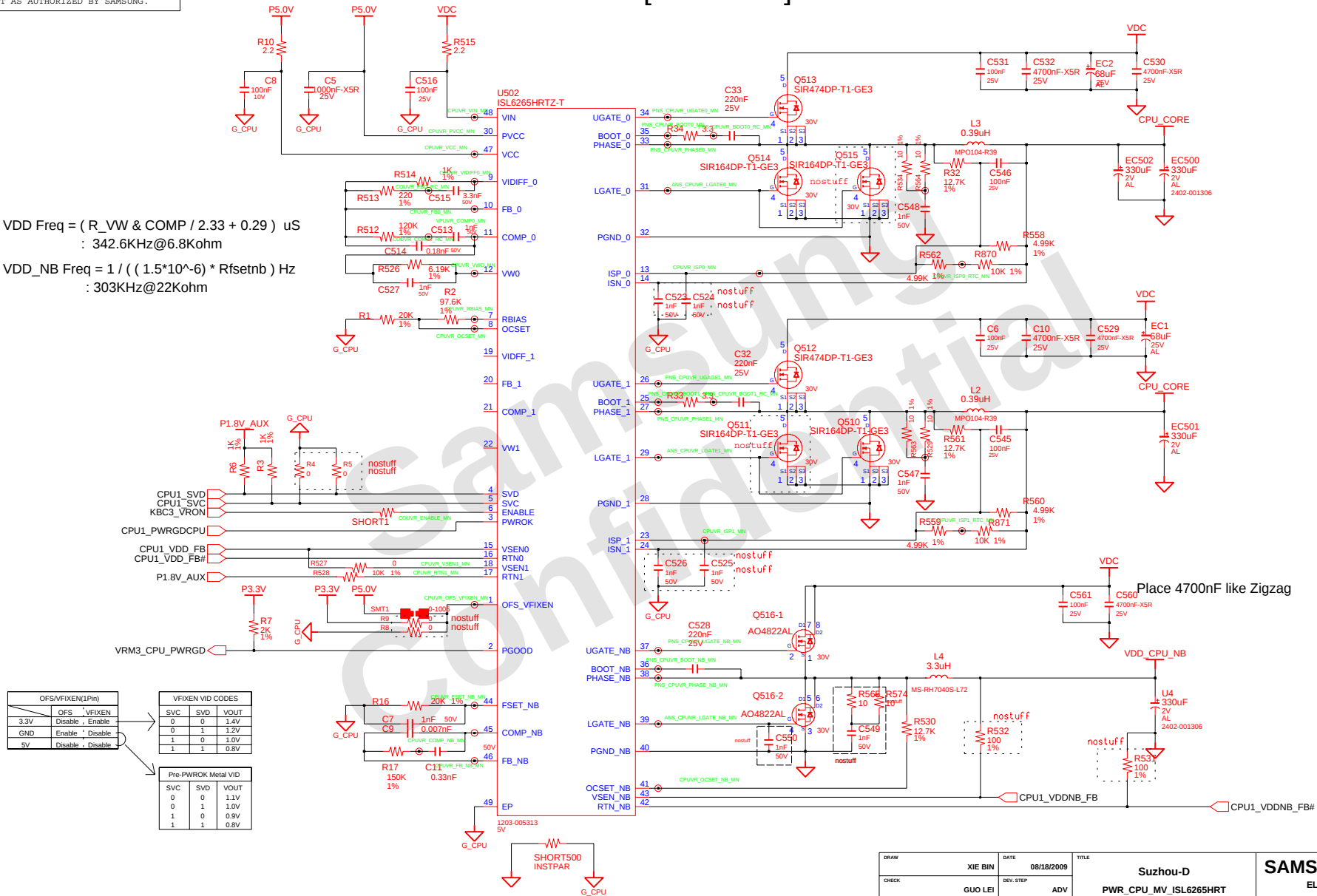


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	PWR_MEMORY	ELECTRONICS	
APPROVAL	BC LEE	REV	0.1	DDR2 POWER	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	48 OF 58

CPU VRM [INTERSIL]

VDD Freq = $(R_{VW} \& COMP / 2.33 + 0.29) \mu s$
: 342.6KHz@6.8Kohm

VDD_NB Freq = $1 / ((1.5 \cdot 10^{-6}) \cdot R_{fsetnb}) Hz$
: 303KHz@22Kohm

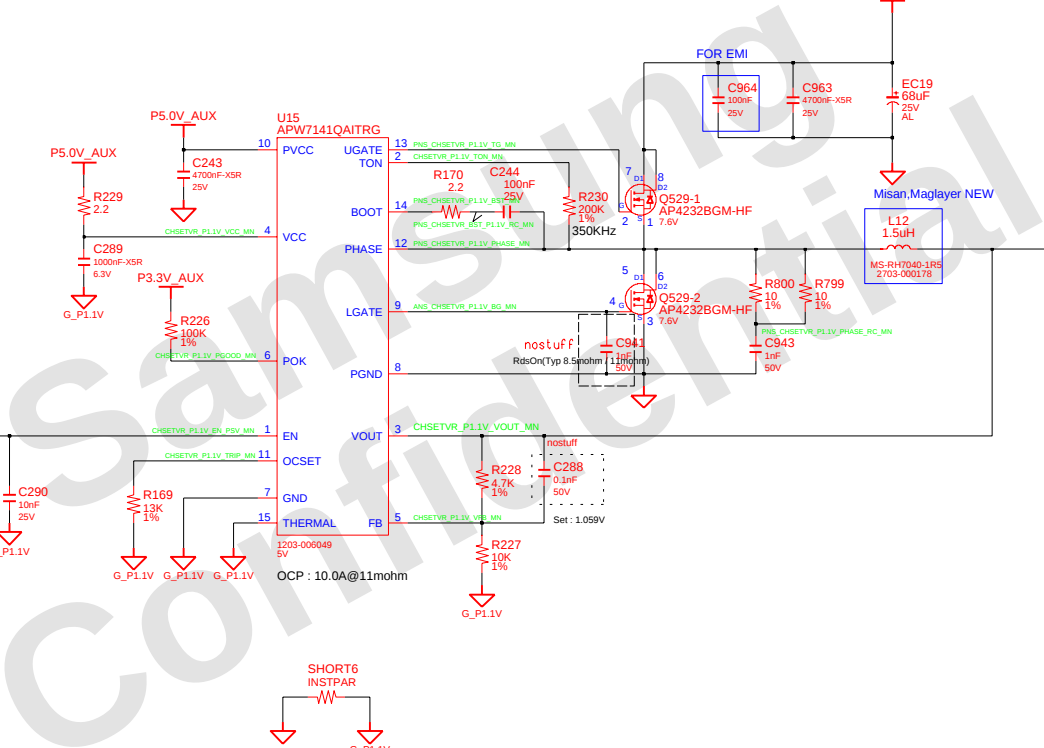


OFS/VFIXEN(1Pin)		VFIXEN VID CODES		
	OFS_VFIXEN	SVC	SVD	VOUT
3.3V	Disable, Enable	0	0	1.4V
GND	Enable, Disable	0	1	1.2V
SV	Disable, Disable	1	0	1.0V
		1	1	0.8V

Pre-PWROK Metal VID		
SVC	SVD	VOUT
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D
CHECK	GUO LEI	DEV. STEP	ADV		PWR_CPU_MV_ISL6265HRT
APPROVAL	BC LEE	REV	0.1		CPU VRM (IMVP6+)
MODULE CODE		LAST EDIT			
				July 15, 2009 19:25:13 PM	PAGE 49 OF 58

1

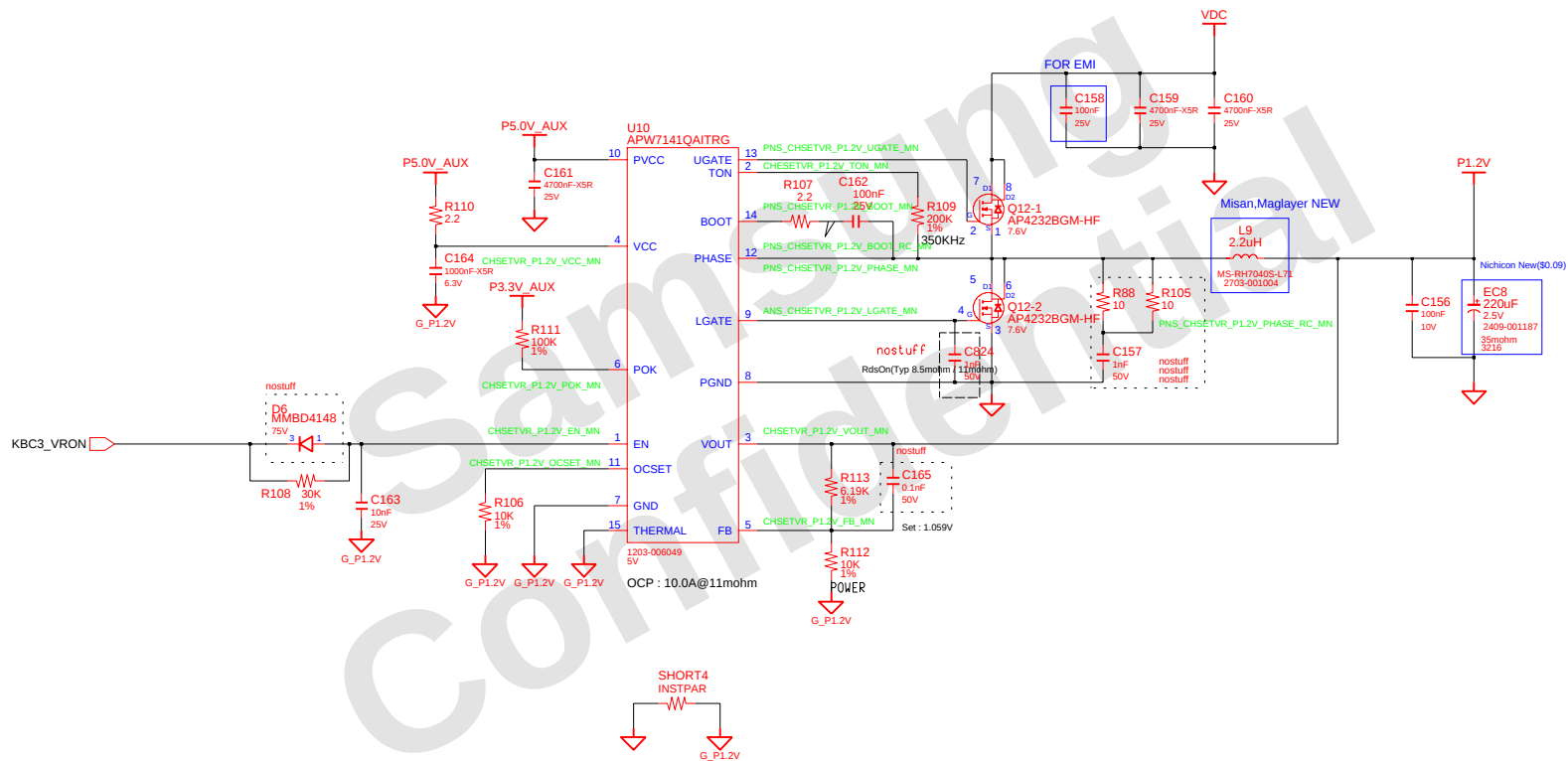


DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D PWR_MV_RX881 P1.1V SAMSUNG ELECTRONICS			
CHECK	GUO LEI	DEV. STEP	ADV				
APPROVAL	BC LEE	REV	0.1			PART NO.	BA41-XXXXXXA
MODULE CODE		LAST EDIT				Julv 15. 2009 19:25:13 PM	PAGE 50 OF 58

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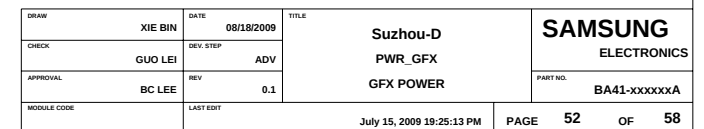
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CHIPSET POWER(P1.2V)

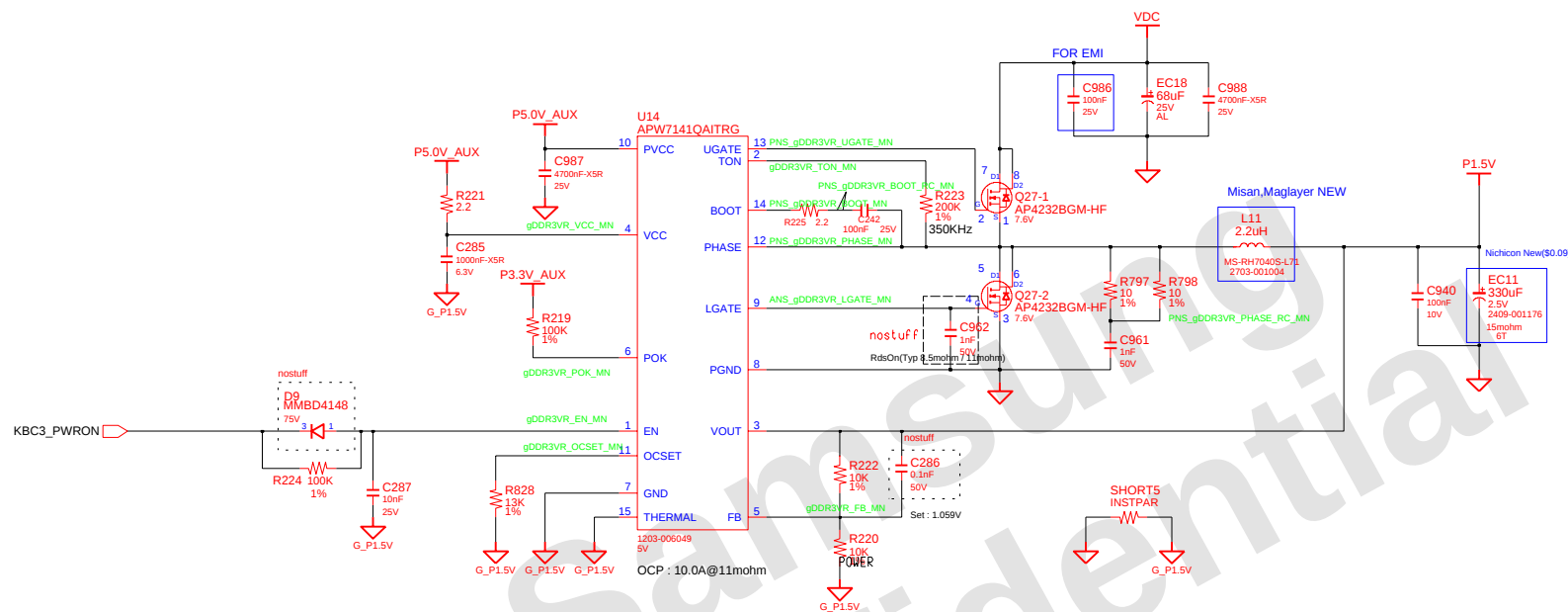


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	PWR_MV_RX881	ELECTRONICS	
APPROVAL	BC LEE	REV	0.1	P1.2V	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	51 OF 58

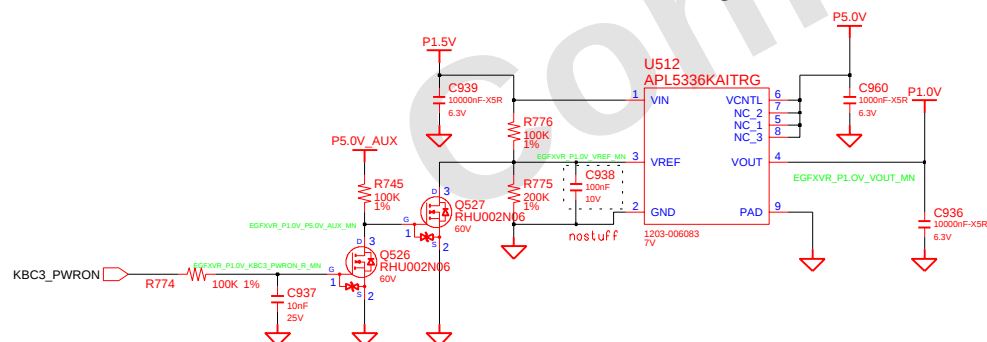
Graphic Core Power



gDDR3 POWER(P1.5V)



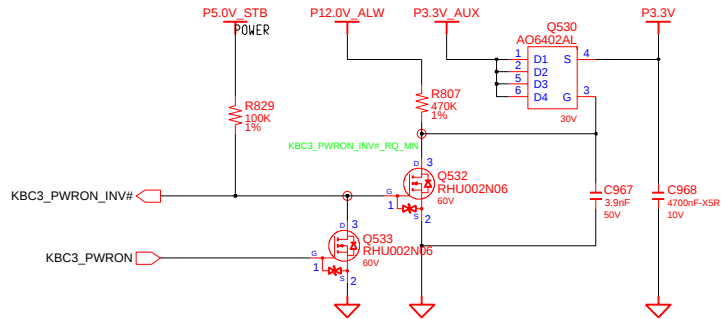
P1.0V



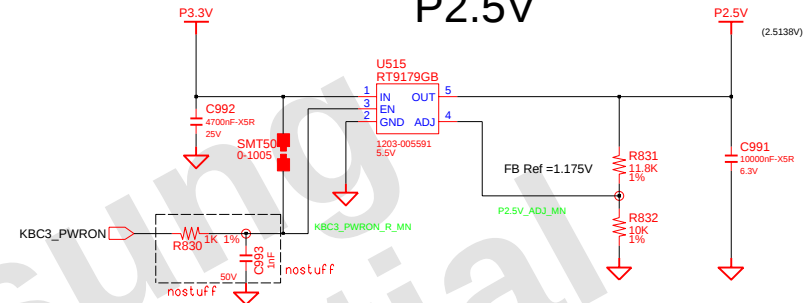
COM-22C-015(1996.6.5) REV. 3

Switched Power

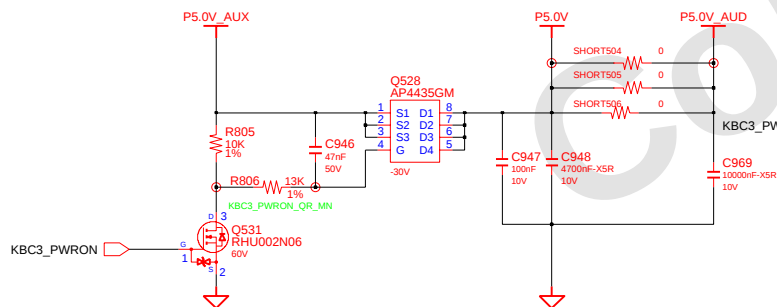
Switched Power On (P3.3V)



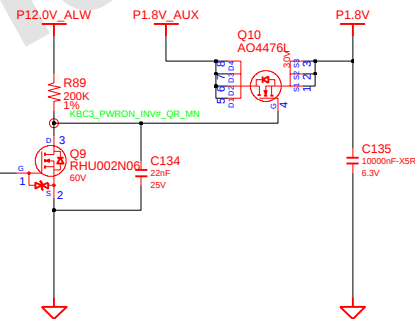
P2.5V



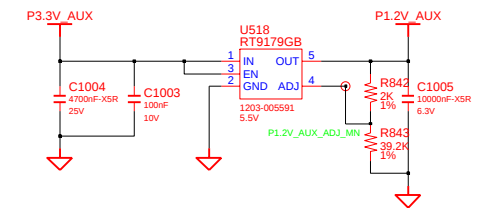
Switched Power On (P5.0V)



Switched Power On (P1.8V)

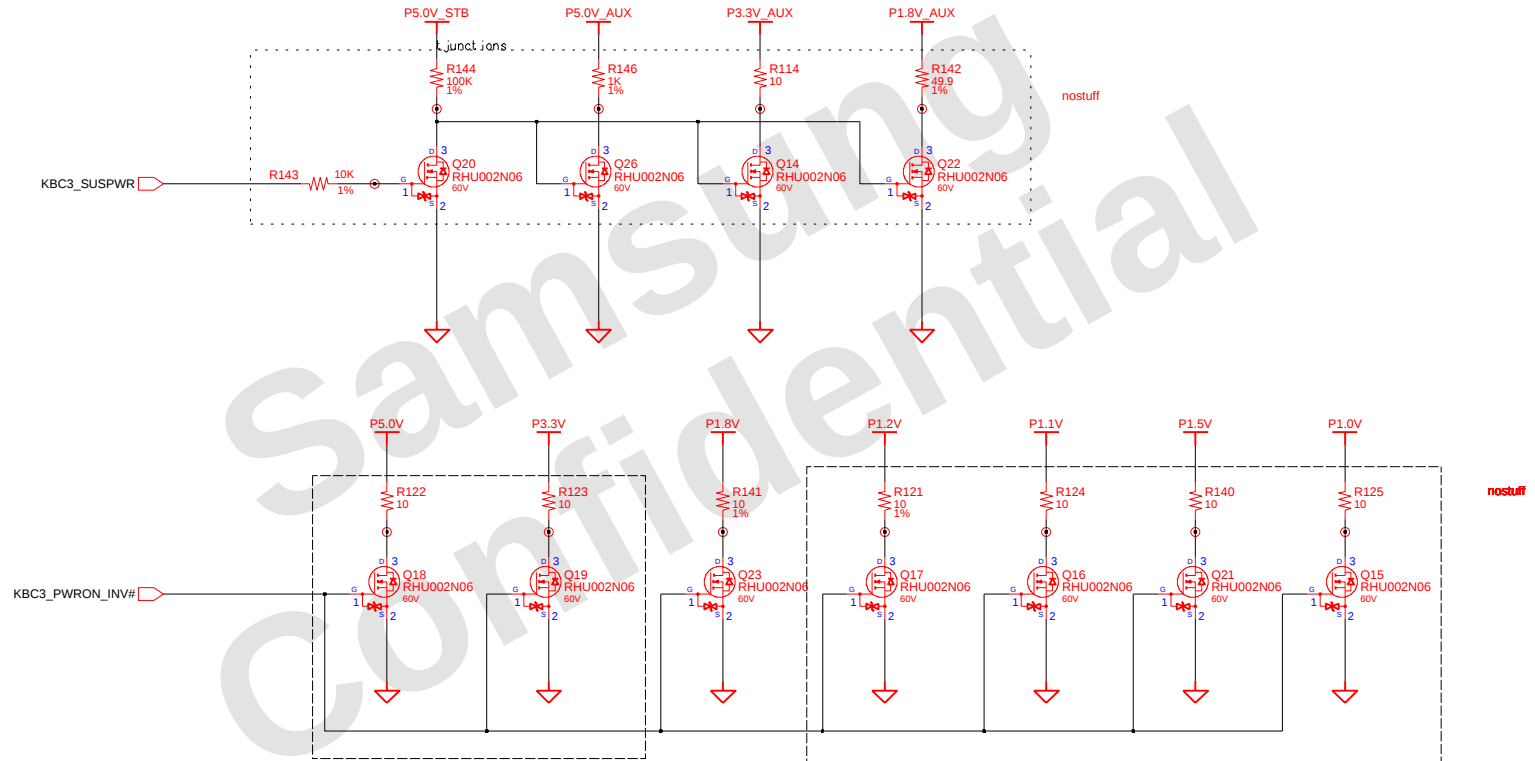


P1.2V_AUX



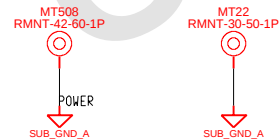
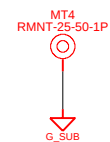
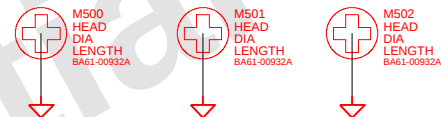
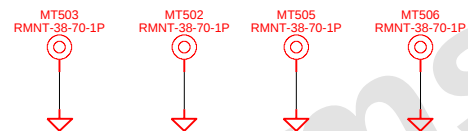
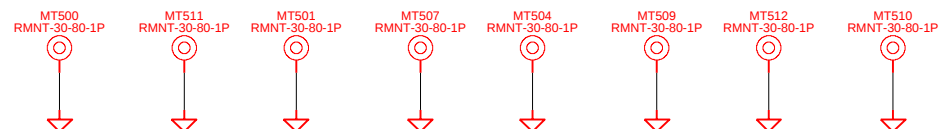
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	PWR_SWITCH		
APPROVAL	BC LEE	REV	0.1	SWITCH POWER		
MODULE CODE		LAST EDIT				
					July 15, 2009 19:25:13 PM	PAGE 54 OF 58

POWER DISCHARGER



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxxA
CHECK	GUO LEI	DEV. STEP	ADV	PWR_CPU_MV_IDISCHARGER		
APPROVAL	BC LEE	REV	0.1	DISCHARGER LOGIC		
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE 55 OF 58		

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DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D MAIN MOUNT HOLE	
CHECK	GUO LEI	DEV. STEP	ADV		
APPROVAL	BC LEE	REV	0.1		
PART NO. BA41-xxxxxxA					
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE 56 OF 58

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- ☐ CHGVR_EN_MN
- ☐ CHP3_GPIO16
- ☐ CHP3_GPIO17
- ☐ CHP3_RTCCLK
- ☐ CHP3_SERIRQ
- ☐ CHP3_SLP53#
- ☐ CHP3_SLP55#
- ☐ CK_PD#_R_MN
- ☐ CPU1_ALERT#
- ☐ CRT3_DDCLK
- ☐ GFX_NC_B_MN
- ☐ KBC3_BKLTON
- ☐ KBC3_PRECHG
- ☐ KBC3_PWRSW#
- ☐ KBC3_RFOFF#
- ☐ KBC3_SCLD#
- ☐ KBC3_SMCLK#
- ☐ KBC3_SPI_DI
- ☐ KBC3_SPI_DO
- ☐ KBC5_KSI(0)
- ☐ KBC5_KSI(1)
- ☐ KBC5_KSI(2)
- ☐ KBC5_KSI(3)
- ☐ KBC5_KSI(4)
- ☐ KBC5_KSI(5)
- ☐ KBC5_KSI(6)

KBCE5_KSI(7)
KBCE5_KSO(0)
KBCE5_KSO(1)
KBCE5_KSO(2)
KBCE5_KSO(3)
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KBCE5_KSO(6)
KBCE5_KSO(7)
KBCE5_KSO(8)
KBCE5_KSO(9)
LCD3_BKLTON
LPC3_LAD(0)
LPC3_LAD(1)
LPC3_LAD(2)
LPC3_LAD(3)
SMB3_ALERT#
BAT3_DETECT#
CHGVR_ICTM_MN
CHGVR_CSIP_MN
CPU1_LDRREQ#
CPU1_LDRTP#
CPU1_LDRTRST#
CPU1_LDRVDD_MN
EGFXVR_VO_MN
EXP3_CLKREQ#
KBCE3_BATDET#
KBCE3_CHG42V#
KBCE3_CHG5V#
KBCE3_NUMLED#
KBCE3_PWRBTR#
KBCE3_RSMRST#
KBCE3_RSMRSTC#
KBCE3_RSTA#
KBCE3_SPI_CLK
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KBCE5_KSO(11)
KBCE5_KSO(12)
KBCE5_KSO(13)
KBCE5_KSO(14)
KBCE5_KSO(15)
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LID3_SLEEP#
MCD3_SDDATA0
MCD3_SDDATA1
MCD3_SDDATA2
MCD3_SDDATA3
MCD3_SDDATA4
MCH3_EXTTST0#
MCH3_EXTTST1#
MIN3_CLKREQ#
PC13_CLKRUN#
PC13_VDD1F_MN
CHGVR_CSIN_MN
CHGVR_CSIP_MN
CHGVR_CSON_MN
CHGVR_CSDOP_MN
CHGVR_CSDON_MN
CHGVR_VADJ_MN
CHGVR_VDDP_MN
MCH3_NP_PWRG#
CHP3_SATALED#
CHP3_TEST0#
CHP3_SE_TEST2
CPU1_SUSTAT#
CPU1_VDDIO_FB#
CPU1_VDDIO_FB#
CPU1_VDDIO_FB#
CPU1_VDDIO_FB#
CPU1_VDDIO_FB#
EGFXVR_VCC_MN

GDDR3VR_EN_B_M
GFX_RESET_RN_M
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KBC3_LED_CTRL
KBC3_PSMUTEN
KBC3_SPKMUITE#
KBC3_WAKES#
LCD0_EDID_CLK
LCD0_EDID_DATA
PEGS_HDMI_CLK
VGAS_HDMI_HPD
CHGVR_ACILIM_B_M
CHGVR_ACSET_MN
CHGVR_CS0EN_B_M
CHGVR_DCSPN_RM
CHGVR_ICOMP_MN
CHGVR_SCATE_MN
CHGVR_VREFCOP_MP_M
CHP3_BIOS_Crff
CHP3_INTROSDIR
CHP3_THRMTRIP#
CPU1_FBI_FBI
CPU1_VDDEN_FB_M
CPUPVR_VSDBL_B_M
DRD2VR_TRIP_MN
EGXVR_SETO_MN
EGXVR_SETO_RM
EGXVR_SET2_MN
EGXVR_SREF_MN
GDDR3VR_POK_MN
GDDR3VR_TOH_MN
GDDR3VR_VENB_CN
GFX_MPVID_B_MN
GFX_PL_EN_RM_N
GFX_RZSET_R_MN
KBC3_KCLK_R_MN
KBC3_LED_ANC1
KBC3_USBPWRON#
KBC3_WLON_LED#
KBC3_WLON_LED2
LCD0_ID_ID_DATA
PEGS_HDMI_DATA
PEGS_HDMI_DATA
TPDS_L_BUTTON
TPDS_L_BUTTON2
VRMPR_CPU_PWRGD
CHGVR_CN_ICM_RM_N
COUVR_ENABLE_MN
CRT1_ALD_LDTSTP
CRT1_ALD_LDTSTP2
CRT3_PSVD_D_MN
DRD2VR_PG0QD_MN
EGXVR_OSCET_MN
GFX_TESTEN_R_MN
GFX_TESTEN_RM_N
GFX_VREFCOP_MP_M
KBC3_CMCLK_RM_N
KBC3_EMDAT_RM_N
KBC3_LED_POWER#
KBC3_PWRVSW_B_MN
KBC3_PWRVSW_RM_N
ANS_SYSVR_SUG1_MN
ANS_SYSVR_BG2_MN
CHGVR_SCATE_RM_N
CHGVR_VADJ_RM_N
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GDDR3VR_OSCET_MN
GFX_MVREFSA_RM_N
GFX_PWRGOOD_RM_N
GMIL_VREFCOP_RM_N
GMIL_VREFCOP_RM_N
GMIL_VREFCOP_RM_N

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 GML_Q_ZQ01_R,M
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 GMLQ_VREFCA1_R,M
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 GMLQ_ZQ01_R,M
 GMLQ_ZQ02_R,M
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 PMS_DRVVR_TG0_MN
 PMS_SYSVR_TG1_MN
 PMS_SYSVR_TG2_MN
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 SD_DDC1_SDA_R,M
 TH_SHDN_SCL_R,M
 WLON_LED_LED,MN
 CHGVR_QCOP_R,M
 CHGVR_VCOMP_RC,M
 CPUF_TEST25_H_R,MN
 CPUF_TEST25_L_R,MN
 GFGX_CLKTESTA_C,M
 GFGX_CLKP_C,M
 GFGX_TESTEN_2_R,M
 KBC3_TERN_SMDATA
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 PMS_EGFXVR_BST_MN
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 GFGX_DPA0_VDD18_B,M
 GFGX_DPD_VDD10_B,M
 GFGX_DPLD_VDD0_B,M
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 VEGAS_HDMI_HPD_R,MN
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 GFGX_MEM_CALRND_R,MN
 GFGX_MEM_CALRND_R,MN
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 GFGX_PCIE_CALRND_R,MN
 PEG3_LCDVDD0_CR,MN
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 PMS_DRVVR3_PHASE,MN
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 PMS_GDDVR3_BOOST,MN
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 CHESTRV_P11V_VFE,MN
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 CHESTRV_P12V_VCC,MN
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 EGFXVR_P10V_P09,MN
 EGFXVR_P10V_VOIT,MN
 EGFXVR_P10V_VOIT,MN
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 PMS_GDDVR3_UPATE,MN
 CHESTRV_P11V_TRIG,MN
 CHESTRV_P11V_TRIG,MN
 KBC3_LED_CHARGE_R,MN
 NEN_ALLOW_LDSTOP_R,MN
 P33V_VDD_INV_EN,MN
 P33V_VDD_INV_EN,MN
 CHESTRV_P11V_PG00D,MN
 CHESTRV_P12V_OSCET,MN
 P33V_VDD_INV_EN_OR,MN
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 PMS_DRVVR2_PHASE,R,MN
 PMS_SYSVR_PHASE2_RC,MN

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 A2VDDQ
 CPU0_CORE
 CPU0_CORE
 DPC_PVD0
 DPC_VDD018
 G. CHG
 G. CPU
 G. DDR
 G. DOR
 G. SUB
 G. EGFX
 G. P11V
 G. P12V
 G. P15V
 G. P15V
 G. P33V
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 P10V
 P25V
 P25V_AUX
 P12V_AUX
 P12V_LAN
 P18V_AUX
 P20V_REF
 P23V_LAN
 P33V_LED
 P33V_LED
 UDD_LED
 P33V_MCD
 P33V_MCD
 P33V_SUB
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 P120V_ALW
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 P50V_USB_SUB
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 SUB_GND_A
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 VDDC
 VDD01DI
 VDD01DI
 VCC_CRT

○ VCC_CRT
○ VDD_LED

DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D Test Point	SAMSUNG ELECTRONICS			
CHECK	GUO LEI	DEV. STEP	ADV		PART NO.	BA41-xxxxxxA		
APPROVAL	BC LEE	REV	0.1					
MODULE CODE	LAST EDIT							July 15, 2009 19:25:13 PM