MODEL NAME : VAW01
PROJECT CODE : ANRVAW0100
PCB NO : LA-9101P (Mars Pro)

DA60000UT00 LA-9101P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B

ZZZ R1@
PCB VAW01 LA-9101P LS-9101P/9102P/9103P
DAZ0U500100

ZZZ GCER3@
PCB VAW01 LA-9101P LS-9101P/9102P/9103P GOLD A31 !
DAZ0U500101

ZZZ TRIR3@
PCB VAW00 LA-9101P LS-9101P/9102P/9103P TRIPOD A31 !
DAZ0U500102

ZZZ HANNR3@
PCB VAW00 LA-9101P LS-9101P/9102P/9103P HANNSTARB A31 !
DAZ0U500103

ZZZ ZDTR3@
PCB VAW00 LA-9101P LS-9101P/9102P/9103P ZDT A31 !
DAZ0U500104

Dell / Compal Confidential

Schematic Document

Intel Chief River
Ivy Bridge(BGA) + Panther Point
OAK 15" UMA/DIS AMD Mars Pro

2012-08-22
Rev: 0.4

46@ : for 46 level
@ : Nopop Component
CONN@ : Connector Component
KB9012@ : ENE KB9012 Implemented
UMA@ : Only for UMA
EMC@ : EMI/ESD parts

GCLK@ : Green CLK implemented
GCLKUMA@ : Green CLK for UMA
GCLKDIS@ : Green CLK for DIS
XTAL@ : X'tal implemented
XTALDIS@ : X'tal with DIS implemented

R1@ : R1 P/N
R3@ : R3 P/N

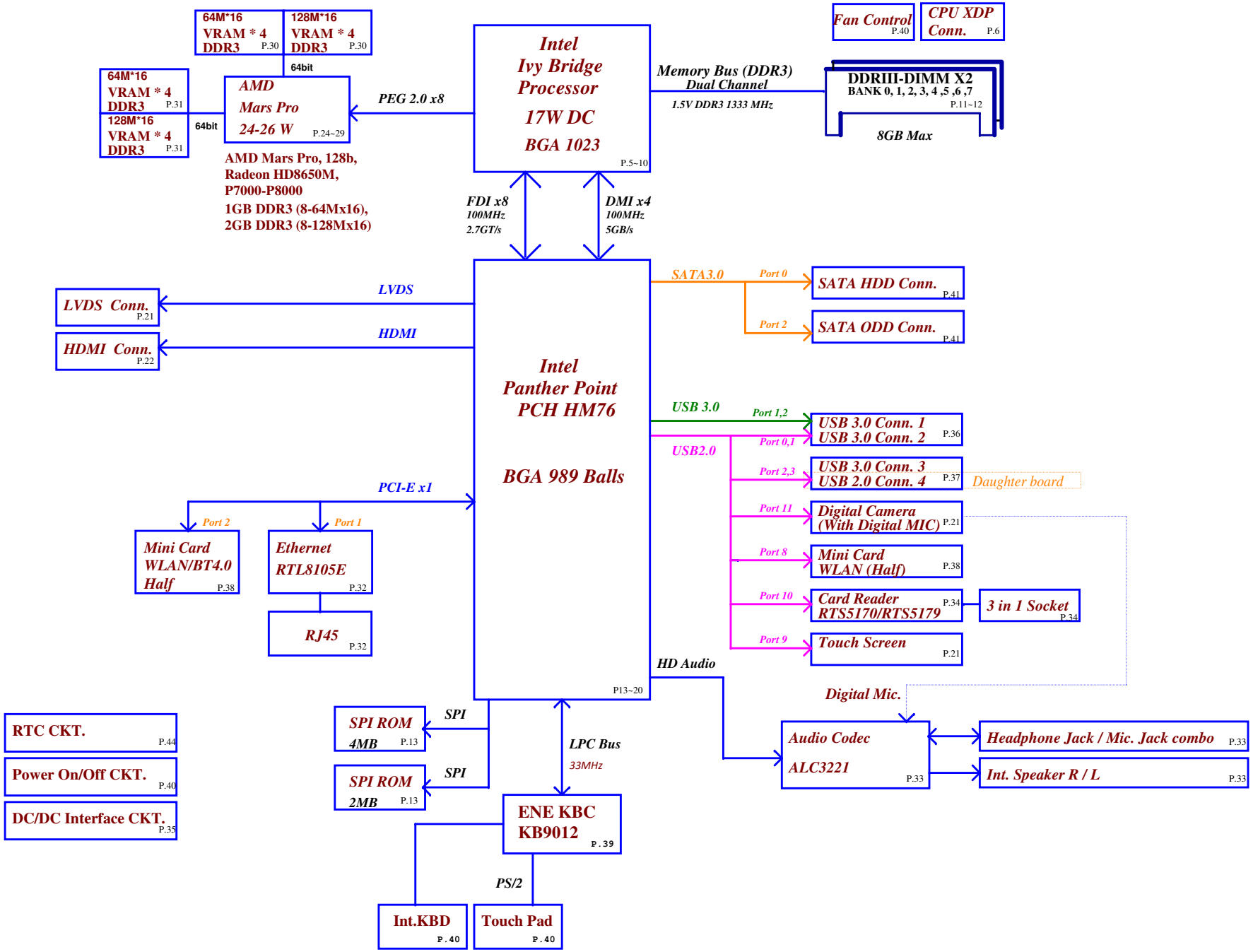
i3R1@ : CPU i3-3217 1.8G
i3VOSR1@ : CPU i3-2365 1.4G
i5R1@ : CPU i5-3317 1.7G
i7R1@ : CPU i7-3517 1.9G
CELR1@ : CPU Celeron 887 1.5G
PENR1@ : CPU Pentium 997 1.6G

DIS@ : Only for Discrete
TH@/THR1@ : Thames-XT
MS@/MSR1@ : Mars Pro
X76@ :
SPI-ROM & VRAM Group

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: Cover Page
Size: Custom | Document Number: LA-9101P | Rev: 0.4
Date: Wednesday, August 29, 2012 | Sheet 1 of 57

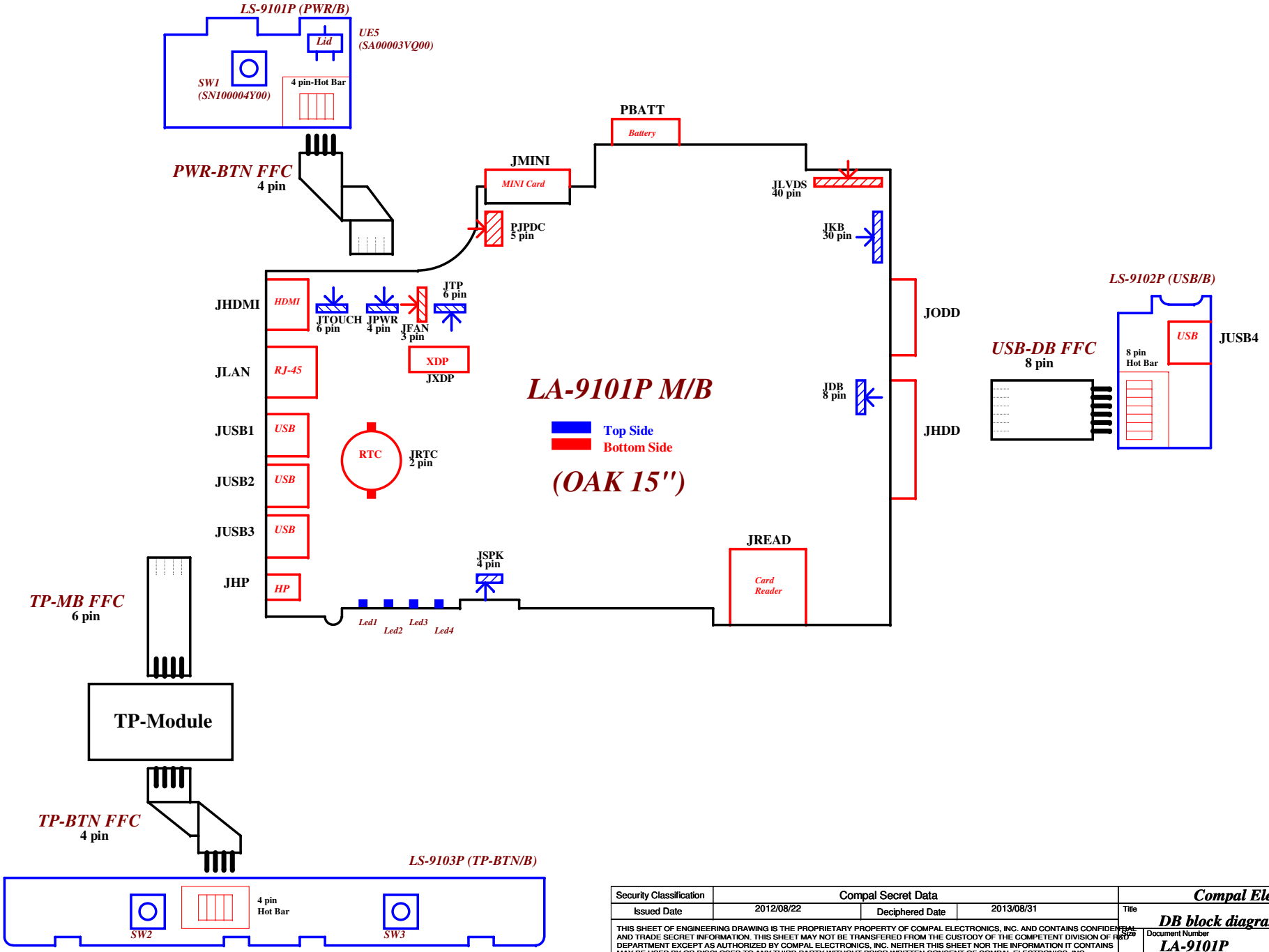


Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.			
Title: Block diagram			
Size	Document Number: LA-9101P		Rev: 0.4
Date: Wednesday, August 29, 2012	Sheet 2 of 57		

Compal Confidential

Project Code : VAW01
File Name : LA-9101P



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: **DB block diagram**

Size | Document Number: **LA-9101P** | Rev: 0.4

Date: Wednesday, August 29, 2012 | Sheet 3 of 57

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

ID	PCB Revision		
0	0.1		
1		0.1	0.1
2	0.2		
3		0.2	0.2
4	0.3		
5	0.4	0.3	0.3
6	1.0		0.4
7		1.0	1.0
	UMA	THM	MARS

Project ID Table

ID	Project Revision
0	
1	
2	
3	
4	
5	UMA
6	DIS THAMES
7	DIS MARS PRO

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Express Card	Thermal Sensor	FFS	VGA Thermal Sensor	VGA	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V
EC_SMB_CK2 EC_SMB_DA2	KB9012								V	V		
PCH_SML0CLK PCH_SML0DATA	PCH											
PCH_SML1CLK PCH_SML1DATA	PCH											
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V	V		V			V	

Link

PCH	USB PORT#	DESTINATION
	0	USB conn.2
	1	USB conn.1
	2	USB conn.3
	3	USB conn.4 (DB)
	4	NC
	5	NC
	6	NC
	7	NC
	8	MINI CARD (WLAN)
	9	Touch Screen
	10	Card Reader
	11	Camera
	12	NC
	13	NC

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100 LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

Symbol Note :

: means Digital Ground

: means Analog Ground

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Title: Notes List

Size: C | Document Number: LA-9101P | Rev: 0.4

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UC1 i3R1@ SA00005L52L
AV8063801058401-SR0N9-L1-1.8G_BGA1023~D

UC1 i3R3@ SA00005L53L
AV8063801058401-SR0N9-L1-1.8G_BGA1023~D

UC1 i3VOSR1@ SA00005UH1L
AV8062701313000-SR0U3-J1-1.4G_BGA1023~D

UC1 i3VOSR3@ SA00005UH2L
AV8062701313000-SR0U3-J1-1.4G_BGA1023~D

UC1 i5R3@ SA00005K62L
AV8063801058002-SR0N8-L1-1.7G_BGA1023~D

UC1 i7R1@ SA00005K53L
AV8063801057605-SR0N6-L1-1.9G_BGA1023~D

UC1 i7R3@ SA00005K52L
AV8063801057605-SR0N6-L1-1.9G_BGA1023~D

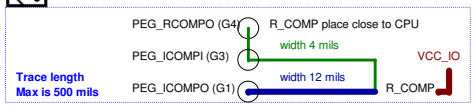
UC1 CELR1@ SA00006021L
AV8062701085401-SR0VA-Q0-1.5G_BGA1023~D

UC1 CELR3@ SA00006022L
AV8062701085401-SR0VA-Q0-1.5G_BGA1023~D

UC1 PENR1@ SA00005ZZ1L
AV8062701084801-SR0V5-Q0-1.6G_BGA1023~D

UC1 PENR3@ SA00005ZZ2L
AV8062701084801-SR0V5-Q0-1.6G_BGA1023~D

(1)PEG_RCOMPO (G4) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC1.
(2)PEG_ICOMPO use 12mil connect to RC1



PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

SA00005K63L
UC1A i5R1@
AV8063801058002-SR0N8-L1-1.7G_BGA1023~D

UC1I i5R1@
AV8063801058002-SR0N8-L1-1.7G_BGA1023~D

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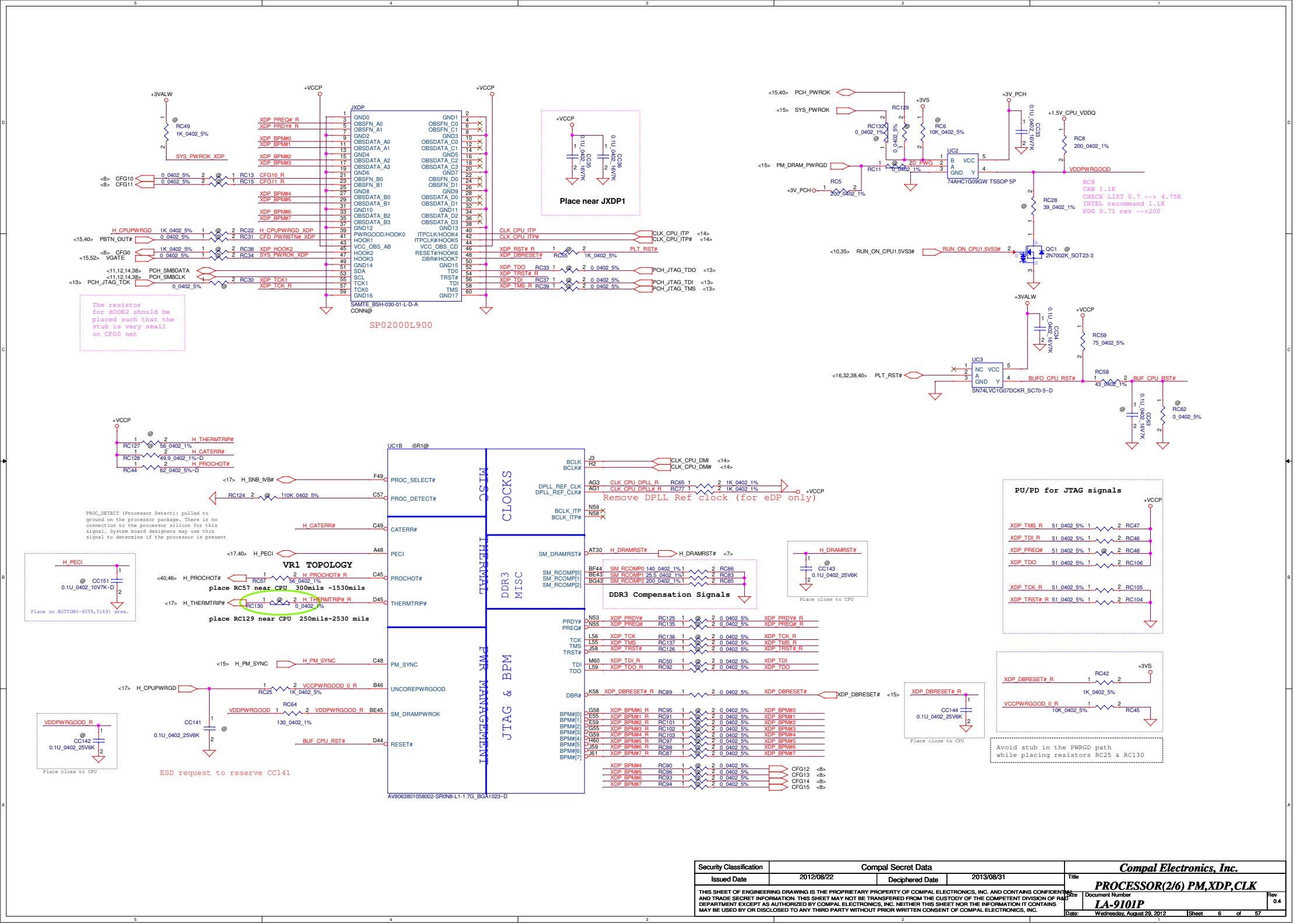
Compal Electronics, Inc.

Title: PROCESSOR(1/6) DMI,FDI,PEG

Size: | Document Number: LA-9101P | Rev: 0.4

Date: Wednesday, August 29, 2012 | Sheet 5 of 57



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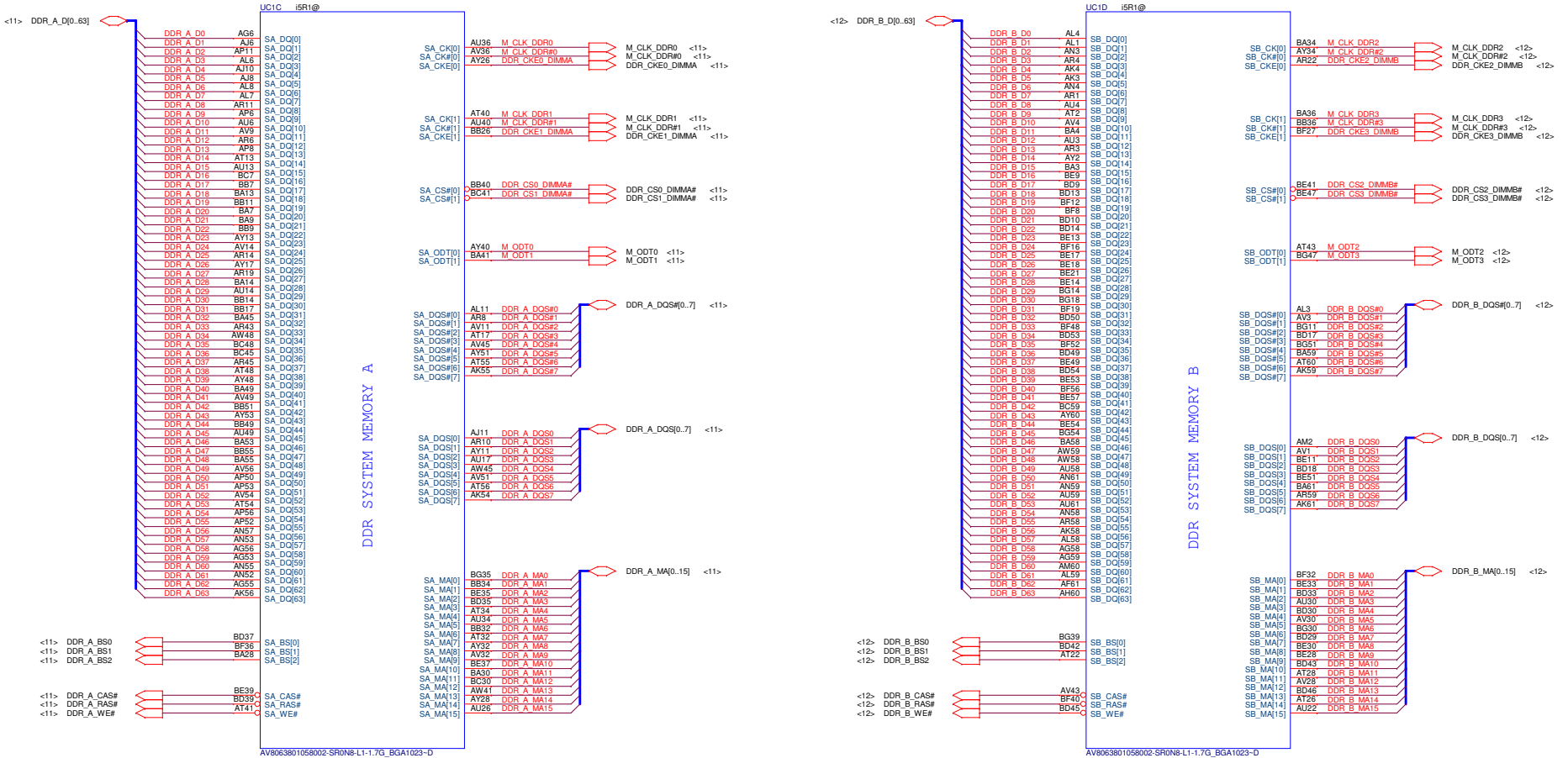
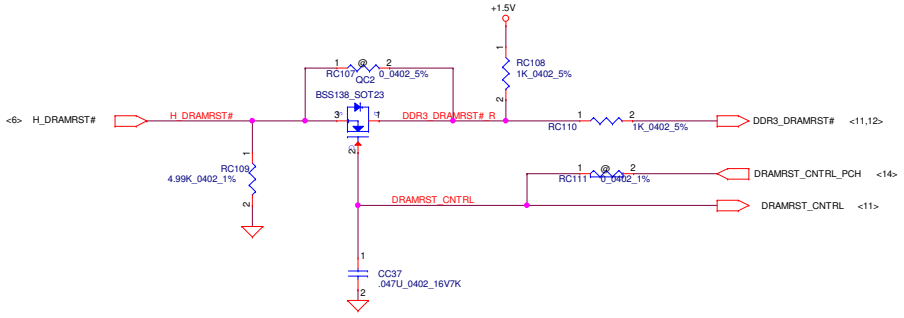
Compal Electronics, Inc.

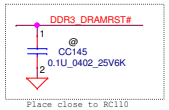
Title: **PROCESSOR(2/6) PM,XDP,CLK**

Size: | Document Number: **LA-9101P** | Rev: 0.4

Date: Wednesday, August 29, 2012 | Sheet 6 of 57

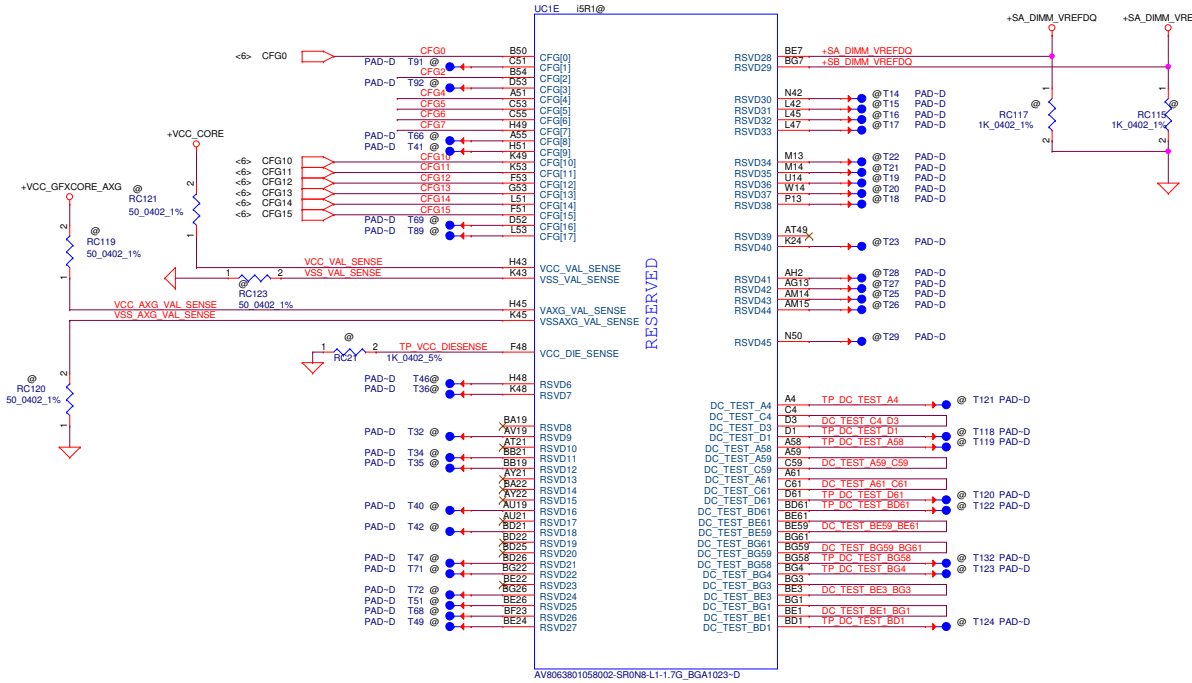


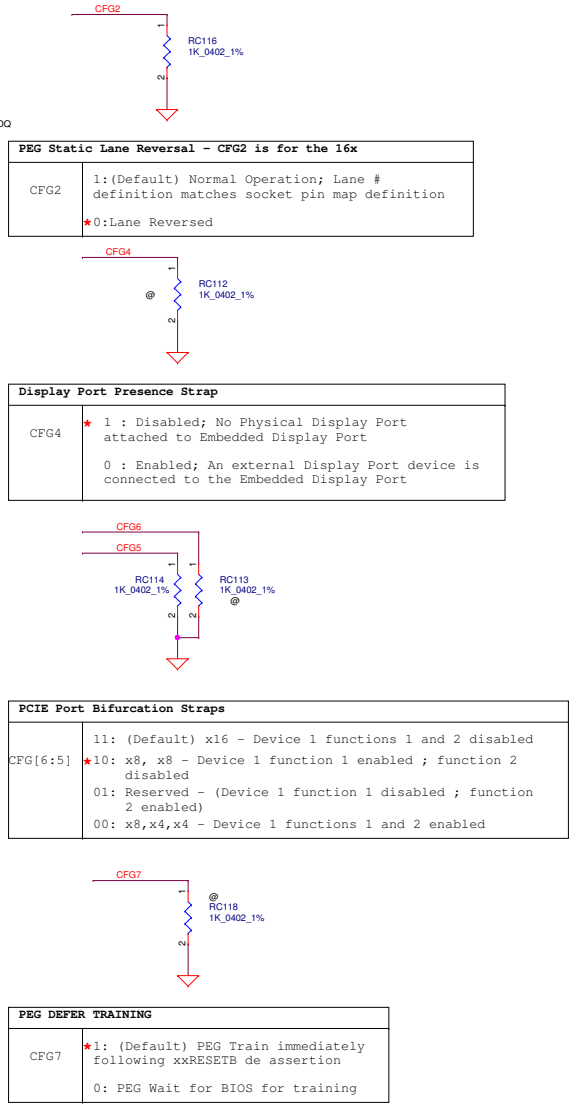




Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title: PROCESSOR(3/6) DDRIII
Size	Document Number: LA-9101P			Rev: 0.4
Date: Wednesday, August 29, 2012	Sheet 7 of 57			

CFG Straps for Processor





PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition ★0:Lane Reversed

Display Port Presence Strap	
CFG4	★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 – Device 1 functions 1 and 2 disabled ★10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	★1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

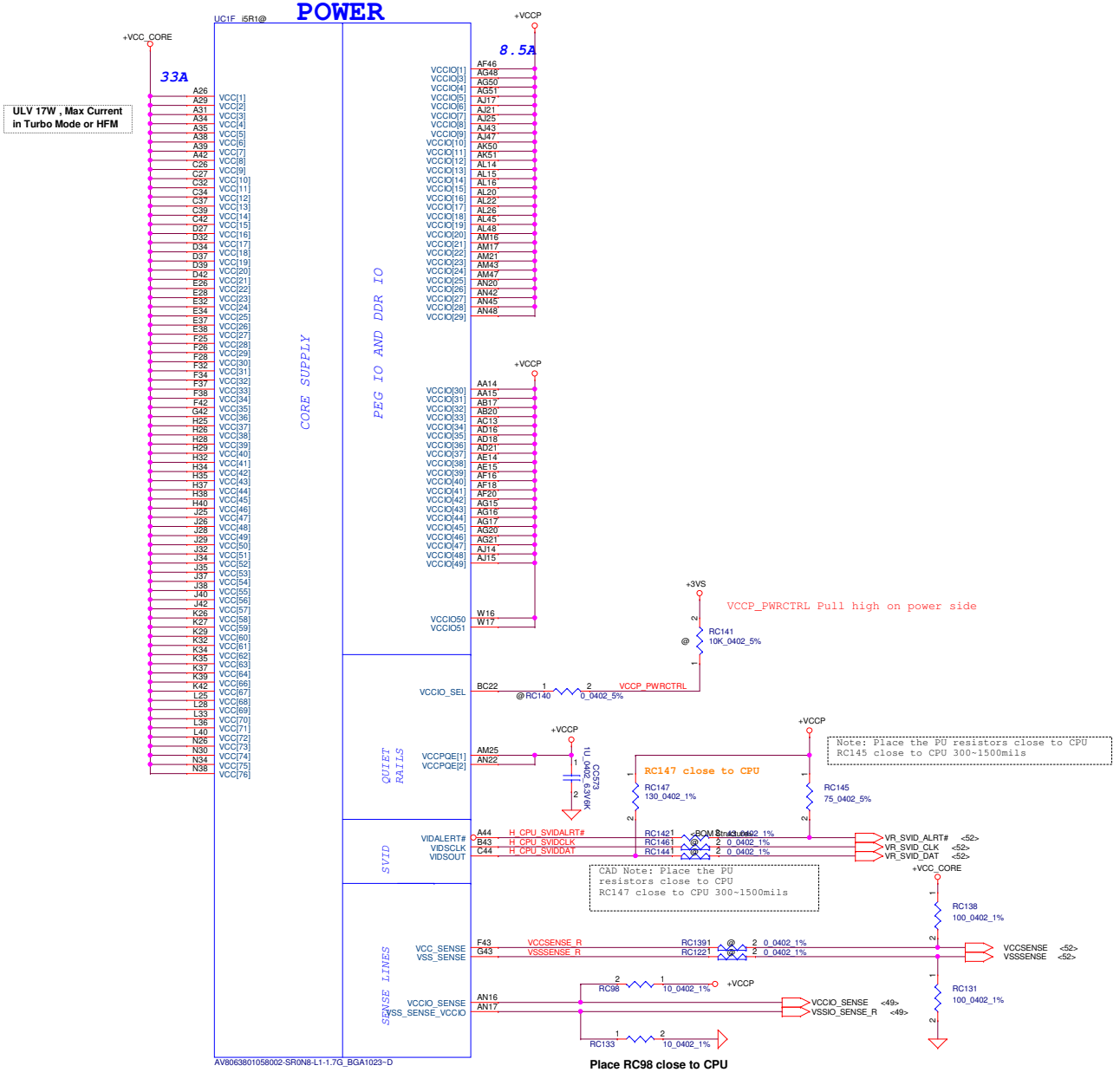
Compal Electronics, Inc.

Title: PROCESSOR(4/6) RSVD,CFG

Size | Document Number: LA-9101P | Rev: 0.4

Date: Wednesday, August 29, 2012 | Sheet 8 of 57

POWER



Place RC98 close to CPU

Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65~1.3	53
VCCIO	1.05/1	8.5
VAXG	0.0~1.1	33
VCCPLL	1.8	1.2
VDDQ	1.5	5
VCCSA	0.65~0.9	6
+1.5V_MEM	1.5	12~16 ★

★ Description

5A to Mem controller(+1.5V_CPU_VDDQ)
5~6A to 2 DIMMs/channel
2~5A to +1.5V_RUN & +0.75V_DDR_VTT

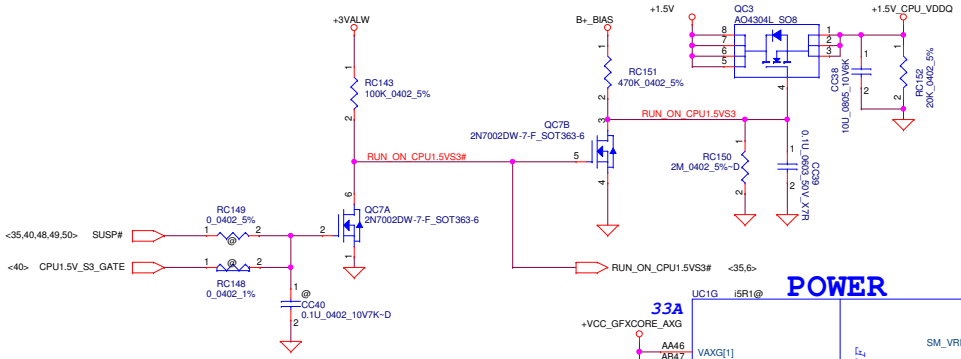
Compal Electronics, Inc.

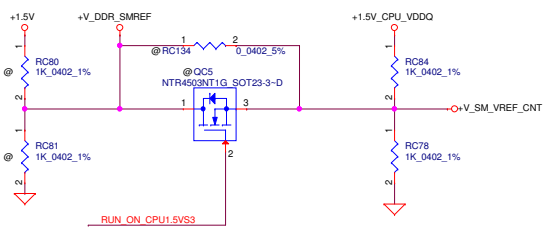
Title: PROCESSOR(5/6) PWR,BYPASS

Size | Document Number: LA-9101P | Rev: 0.4

Date: Wednesday, August 29, 2012 | Sheet 9 of 57

+1.5V_CPU_VDDQ Source





POWER

UC1G i5R1@

GRAPHICS

33A

+VCC_GFXCORE_AXG

VAXG[1..56]

VREF

SM_VREF ← +V_SM_VREF_CNT

+V_SM_VREF should have 10 mil trace width

DDR3 - 1.5V RAILS

5A

+1.5V_CPU_VDDQ

VDDQ[1..26]

CC178 0.1U_0402_10V7K-D
CC179 0.1U_0402_10V7K-D
CC149 0.1U_0402_10V7K-D
CC150 0.1U_0402_10V7K-D

6A +1.5V

10U_0603_6.3V6M ×10

330U_D2_2VM_R6M-D CC167

1U_0402_6.3V6K ×10

SENSE LINES

+VCC_GFXCORE_AXG

RC99 100_0402_1%
RC76 @ 100_0402_1%
RC100 100_0402_1%

<52> VCC_AXG_SENSE
<52> VSS_AXG_SENSE

VAXG_SENSE
VSSAXG_SENSE

QUIET RAILS

+1.5V_CPU_VDDQ

VCCDQ[1]
VCCDQ[2]

10U_0402_6.3V6K CC274

1.8V RAIL

+1.8VS

1.2A

VCCPLL[1..3]

330U_D2_2.5VM_R6M-D CC176
1U_0402_6.3V6K CC174
1U_0402_6.3V6K CC175

SENSE LINES

VDDQ_SENSE
VSS_SENSE_VDDQ

SA RAIL

+VCCSA

6A

VCCSA[1..16]

330U_D2_2VM_R6M-D CC172
10U_0603_6.3V6M ×6
1U_0402_6.3V6K ×8

VCCSA VID lines

VCCSA_SENSE
U10
VCCSA_SENSE <51>

VCCSA_VID[0]
VCCSA_VID[1]
D48
D49
VCCSA_VID0 <51>
VCCSA_VID1 <51>

AV8063801058002-SR0N8-L1-1.7G_BGA1023-D

UC1H i5R1@

VSS

VSS[1..180]

AV8063801058002-SR0N8-L1-1.7G_BGA1023-D

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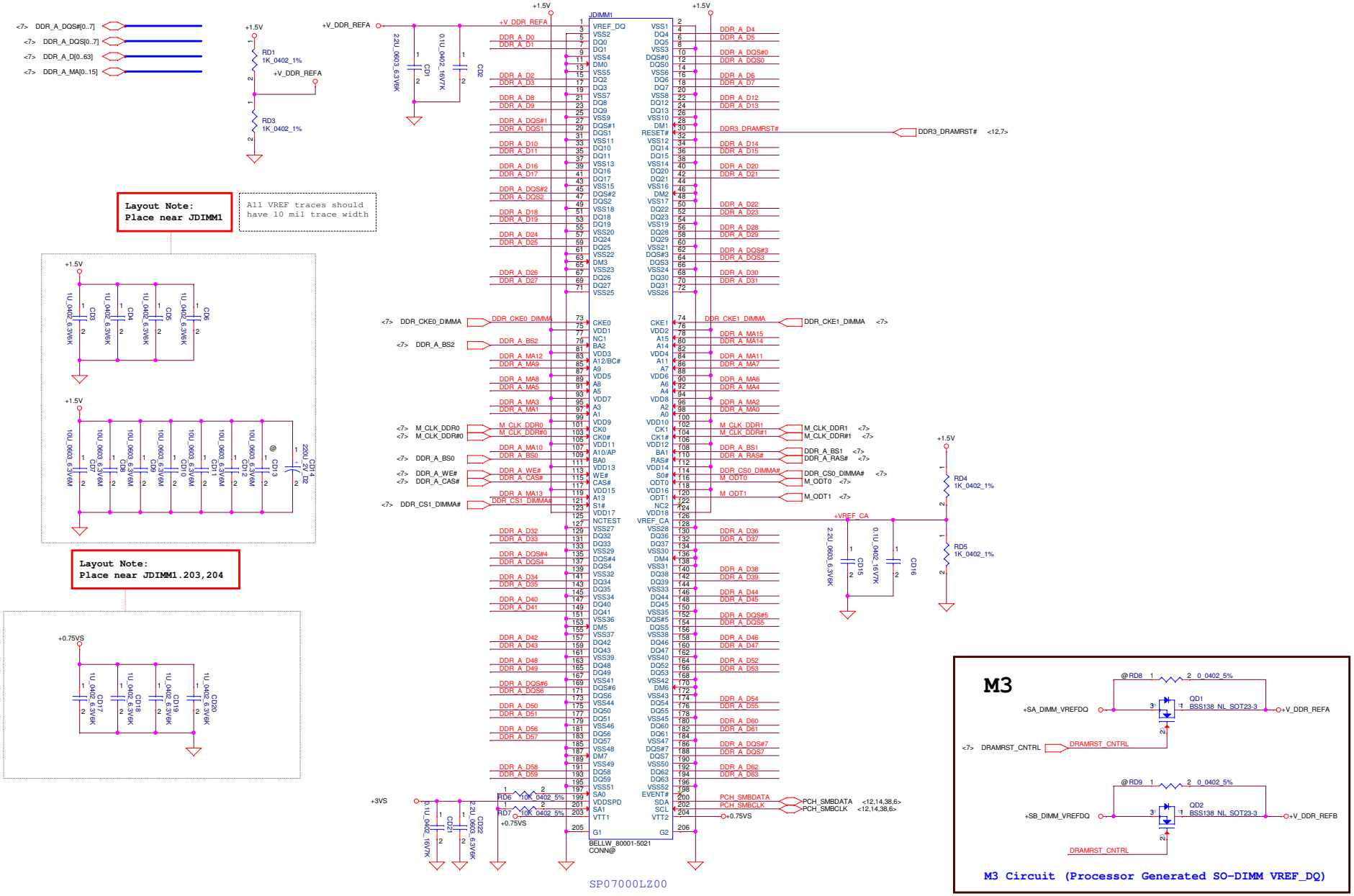
Title: PROCESSOR(6/6) PWR,VSS

Size | Document Number: LA-9101P | Rev: 0.4

Date: Wednesday, August 29, 2012 | Sheet 10 of 57



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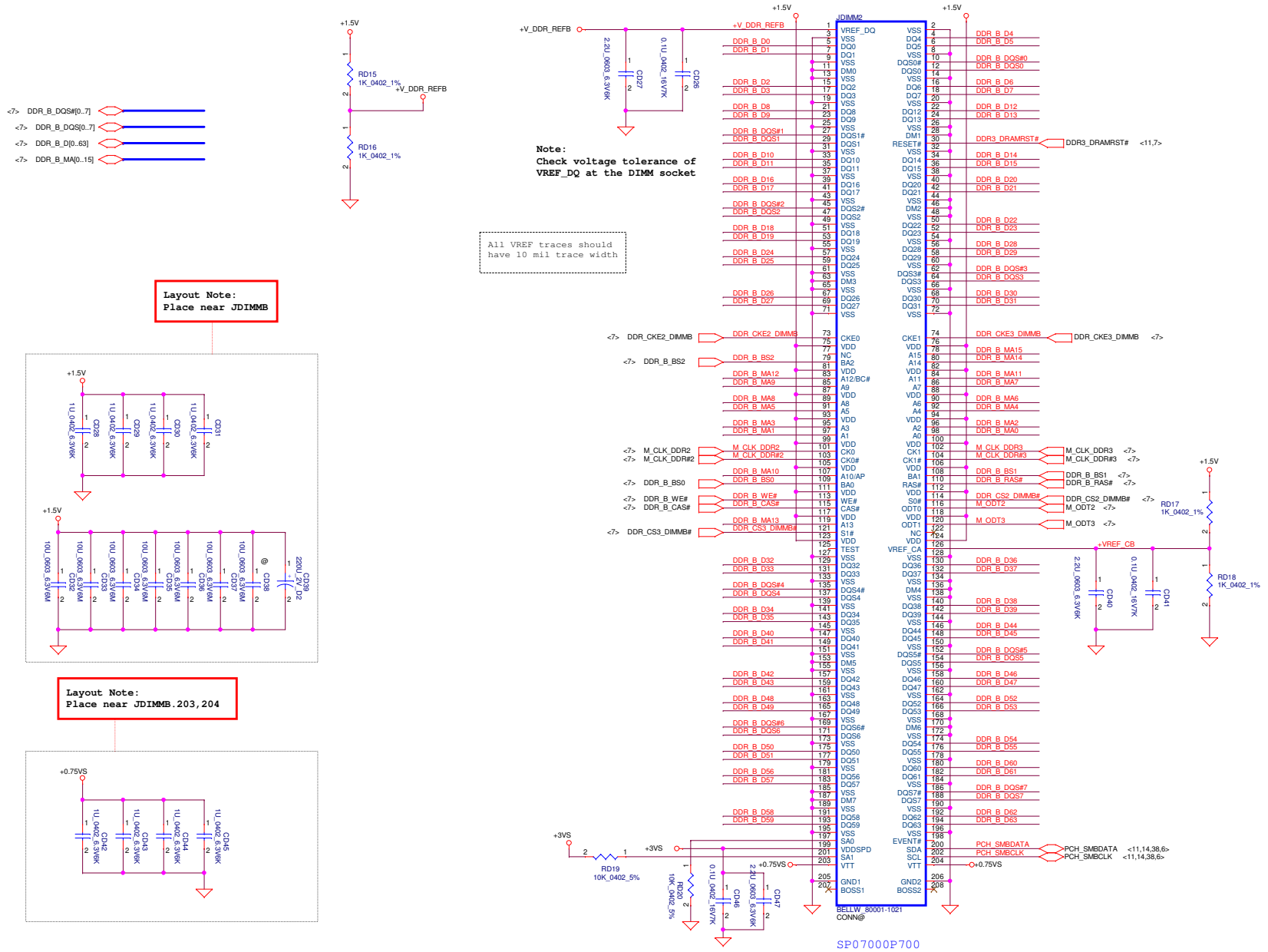
Title: **DDRIII DIMMA**

Size | Document Number: **LA-9101P** | Rev: 0.4

Date: Wednesday, August 29, 2012 | Sheet 11 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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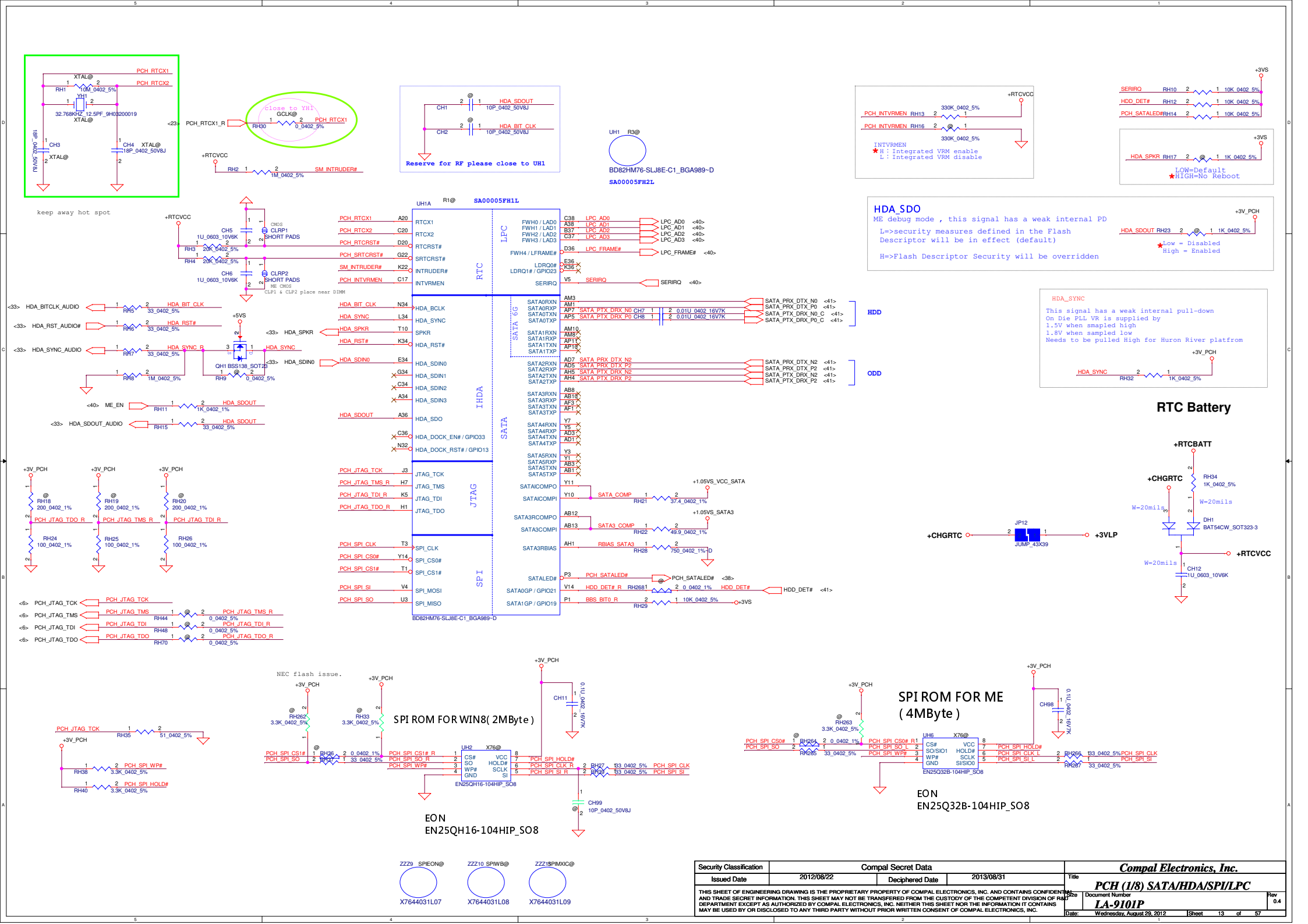
Title: **DDRIII DIMMB**

Size: | Document Number: **LA-9101P** | Rev: 0.4

Date: Wednesday, August 29, 2012 | Sheet 12 of 57



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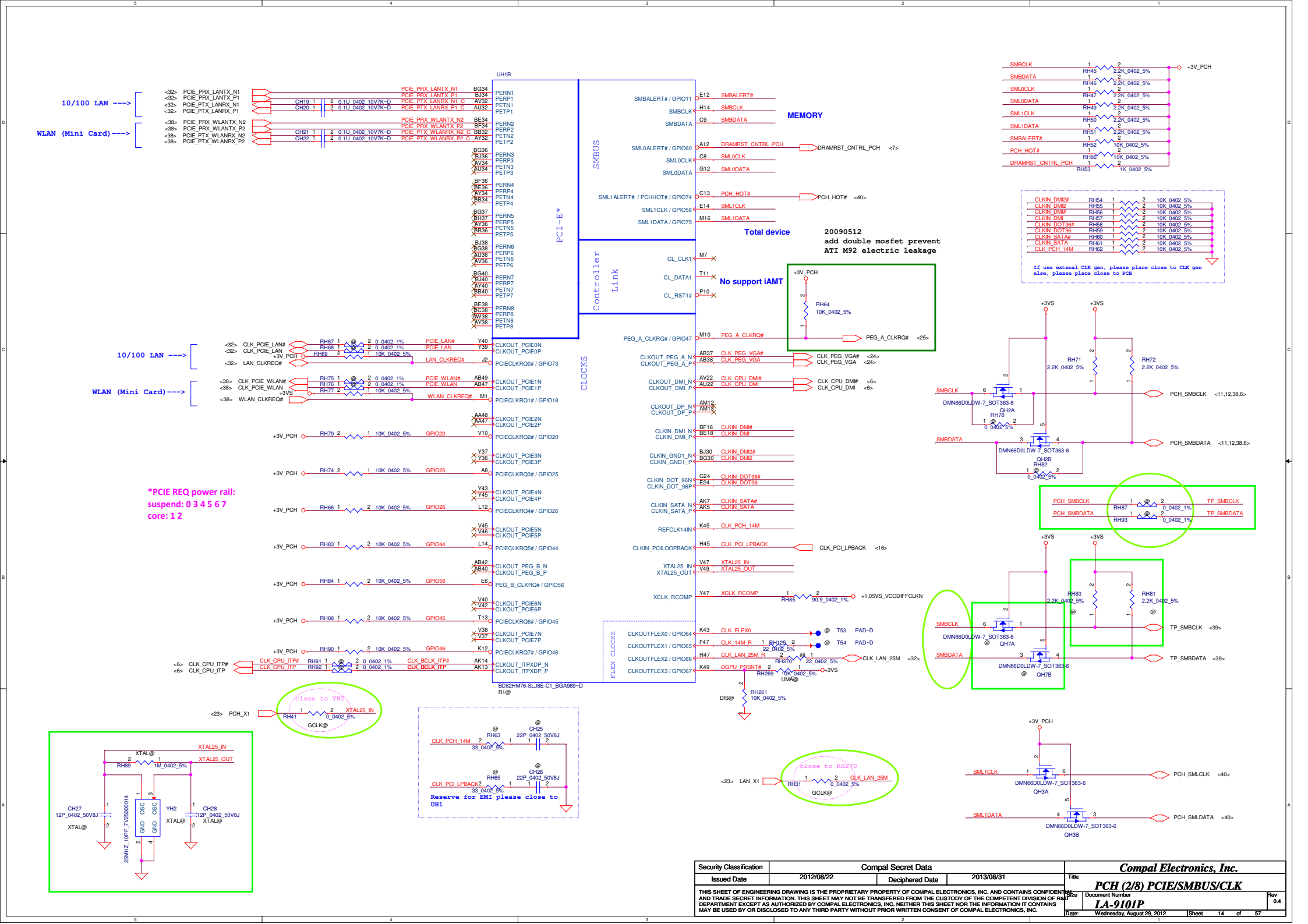
Compal Electronics, Inc.

Title: **PCH (1/8) SATA/HDA/SPI/LPC**

Size: | Document Number: **LA-9101P** | Rev: 0.4

Date: Wednesday, August 29, 2012 | Sheet 13 of 57


10/100 LAN ---->
WLAN (Mini Card)---->
UH1B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
MEMORY
Total device
20090512
add double mosfet prevent
ATI M92 electric leakage
No support iAMT
*PCIE REQ power rail:
suspend: 0 3 4 5 6 7
core: 1 2
close to YH2
close to RH270
Reserve for EMI please close to UH1
If use extenal CLK gen, please place close to CLK gen else, please place close to PCH
BD82HM76-SLJ8E-C1_BGA989~D
R1@
DMN66D0LDW-7_SOT363-6
25MHZ_10PF_7V25000014
Security Classification
Compal Secret Data
Issued Date
2012/08/22
Deciphered Date
2013/08/31
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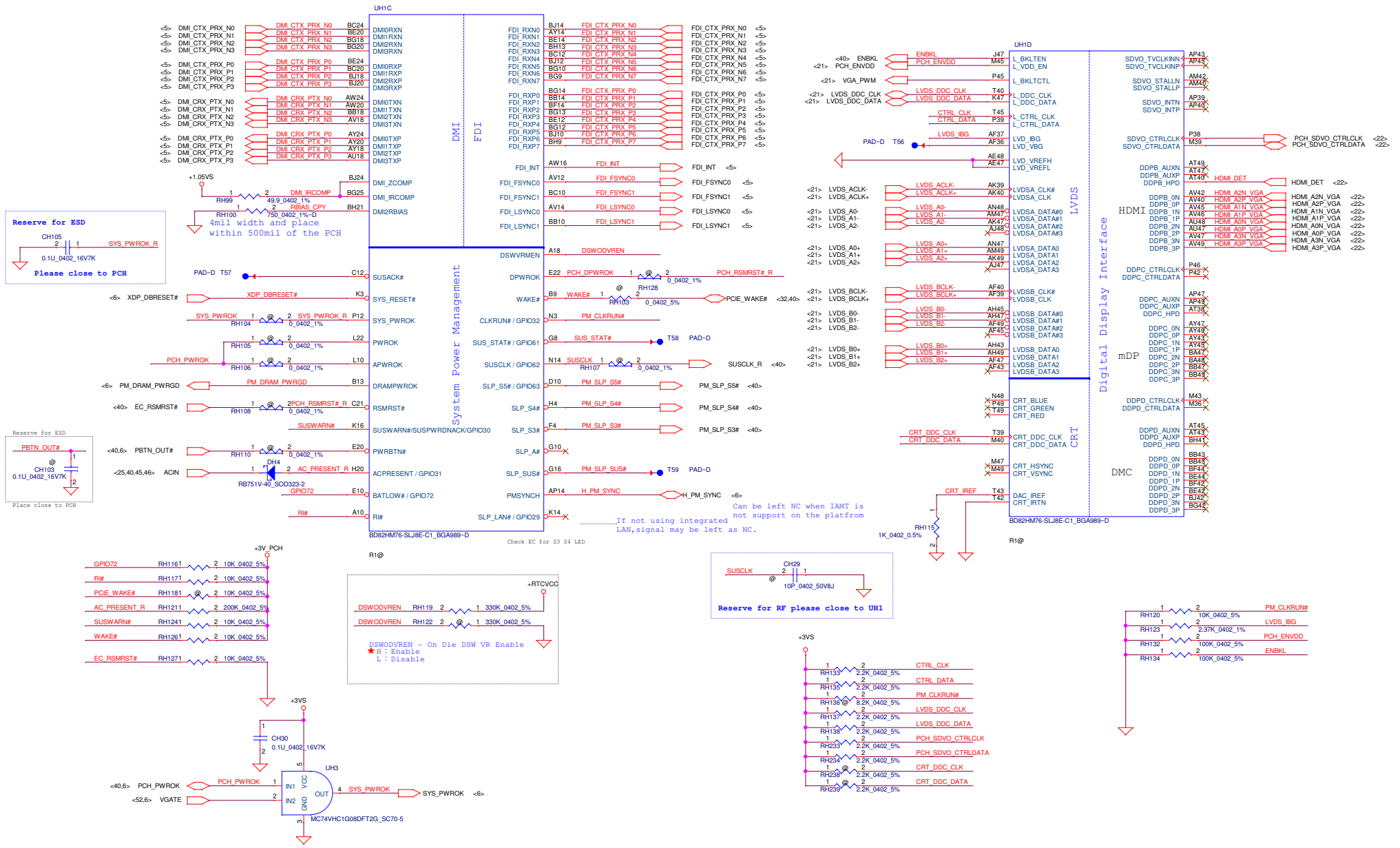
Compal Electronics, Inc.
Title
PCH (2/8) PCIE/SMBUS/CLK
Size
Document Number
LA-9101P
Rev
0.4
Date: Wednesday, August 29, 2012
Sheet 14 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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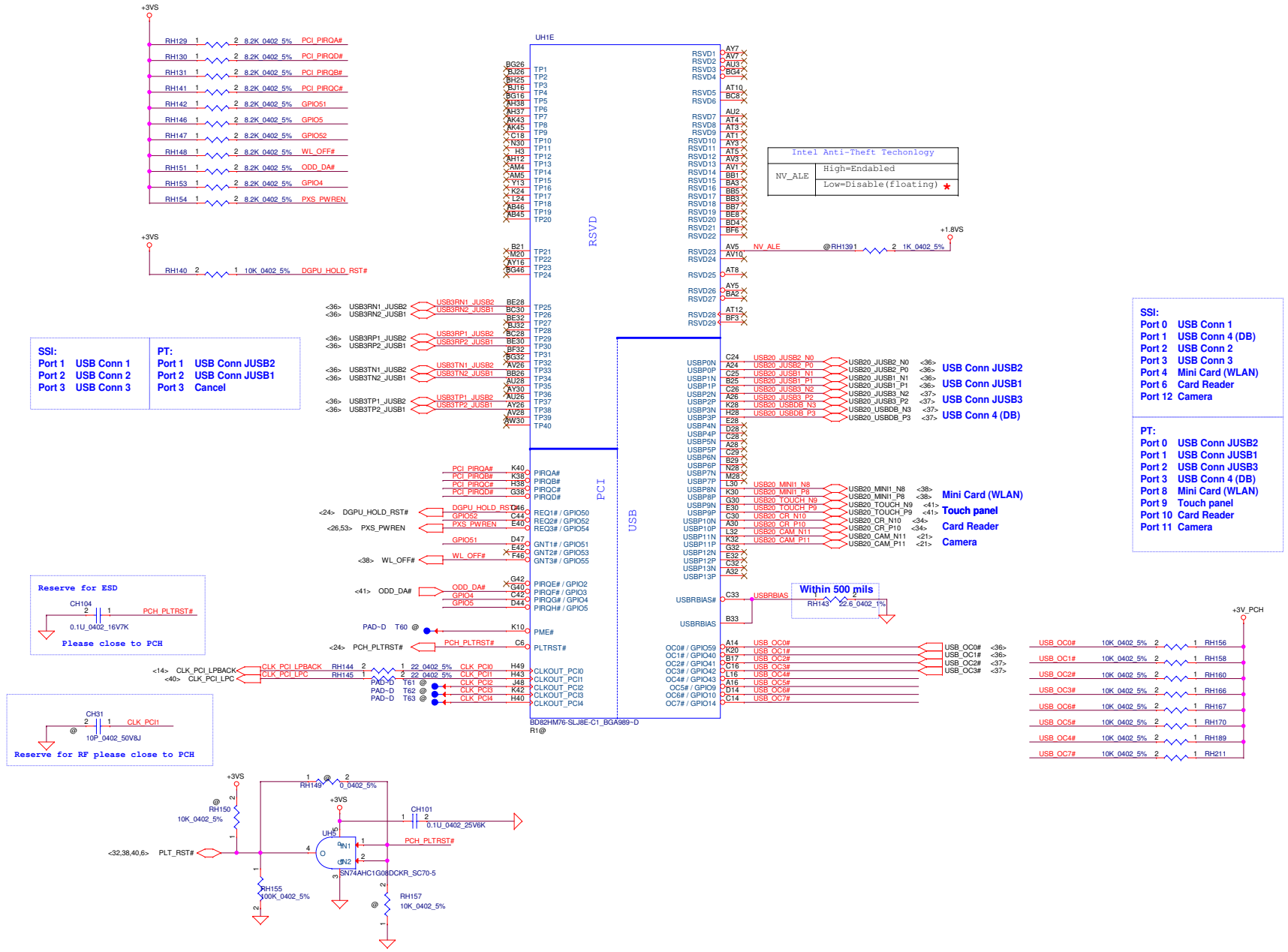
Compal Electronics, Inc.

Title: **PCH (3/8) DMI/FDI/PM/GFX/DP**

Size: | Document Number: **LA-9101P** | Rev: 0.4

Date: Wednesday, August 29, 2012 | Sheet 15 of 57



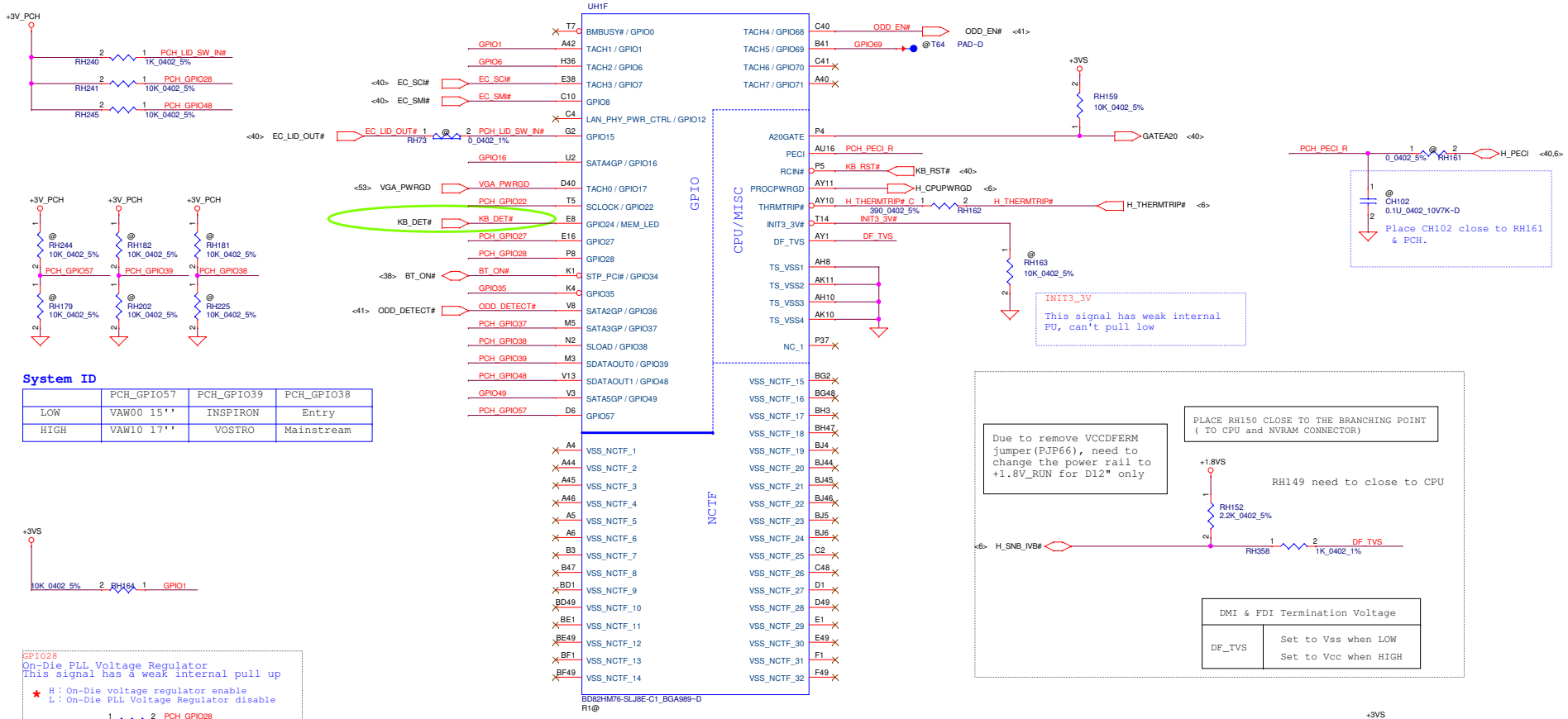
Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: **PCH (4/8) PCI/USB/NVRAM**

Size | Document Number: **LA-9101P** | Rev: 0.4

Date: Wednesday, August 29, 2012 | Sheet 16 of 57



System ID

	PCH_GPIO57	PCH_GPIO39	PCH_GPIO38
LOW	VAW00 15''	INSPIRON	Entry
HIGH	VAW10 17''	VOSTRO	Mainstream

DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH

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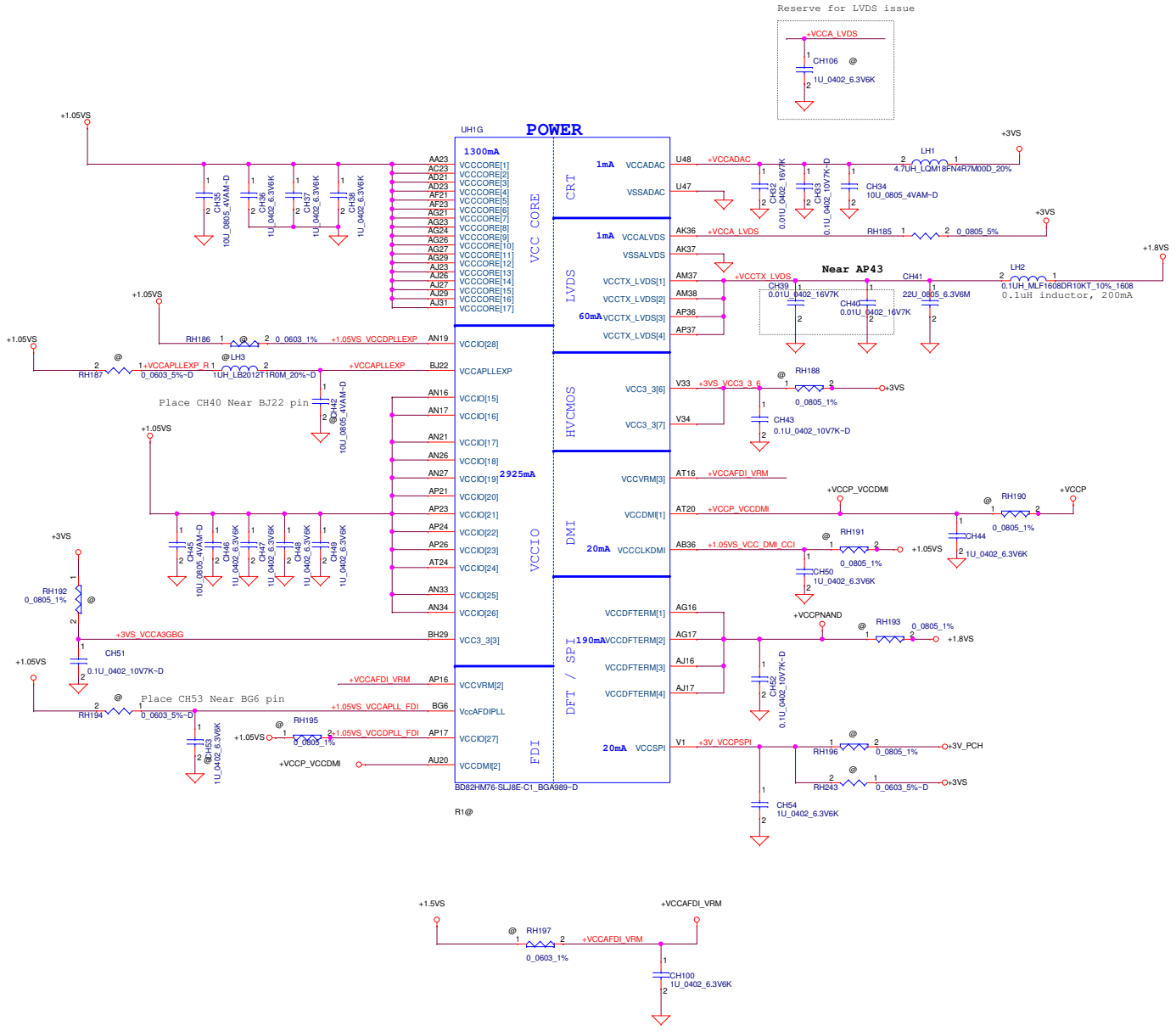
Compal Electronics, Inc.

Title: **PCH (5/8) GPIO/CPU/MISC**

Size: | Document Number: **LA-9101P** | Rev: 0.4

Date: Wednesday, August 29, 2012 | Sheet 17 of 57



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

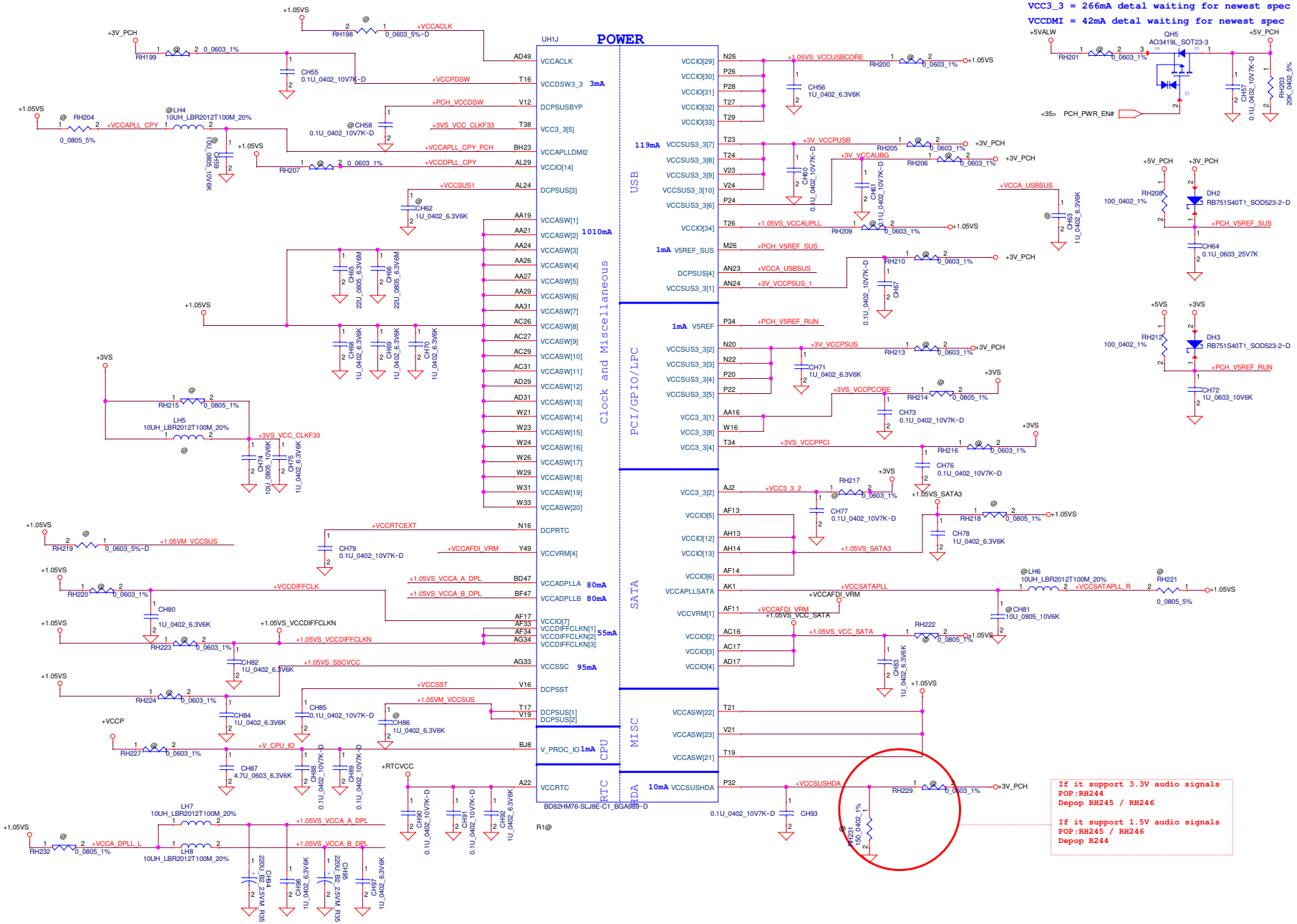
Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: PCH (6/8) PWR

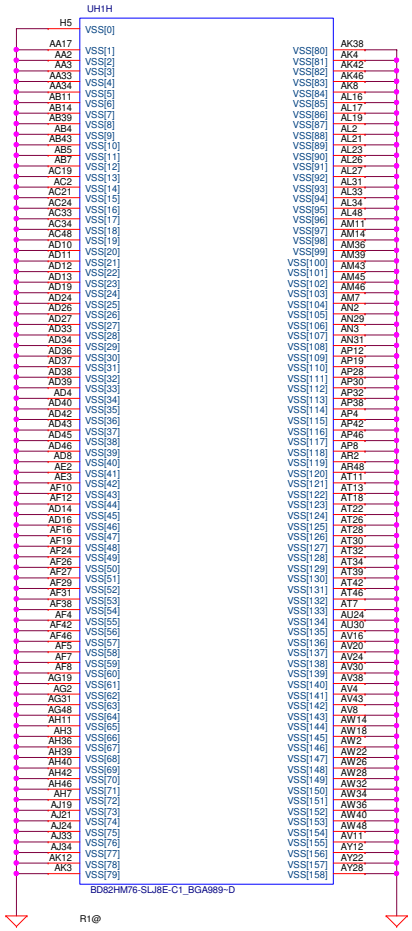
Size | Document Number: LA-9101P | Rev: 0.4

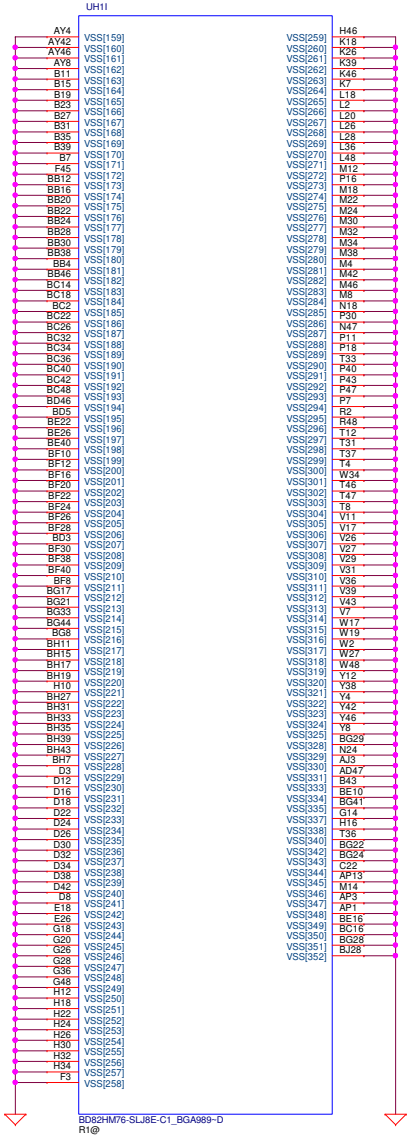
Date: Wednesday, August 29, 2012 | Sheet 18 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.			
Title: PCH (7/8) PWR			
Size	Document Number: LA-9101P		Rev: 0.4
Date: Wednesday, August 29, 2012	Sheet 19 of 57		





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Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title: PCH (8/8) VSS
Size	Document Number: LA-9101P			Rev: 0.4
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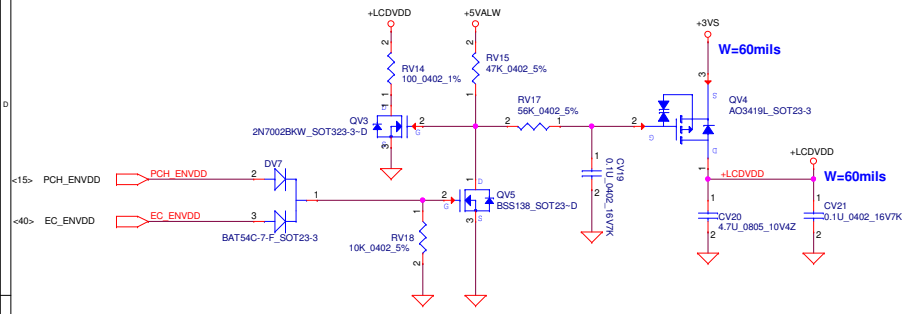
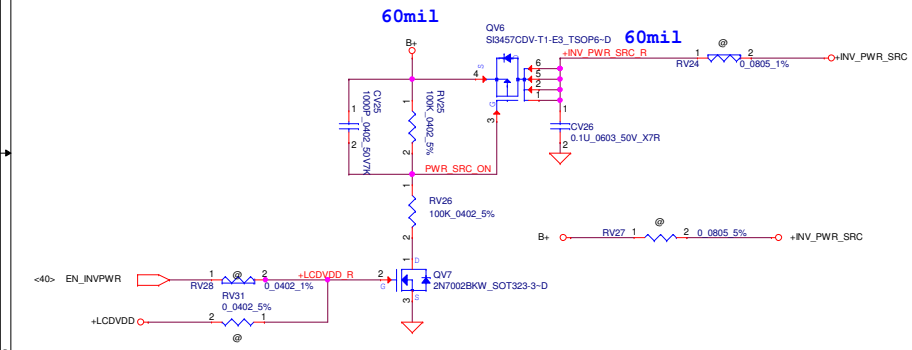
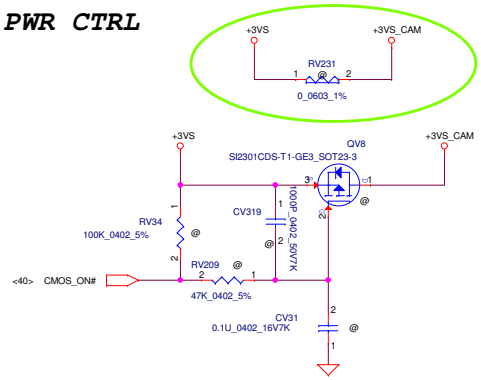
LCD PWR CTRL



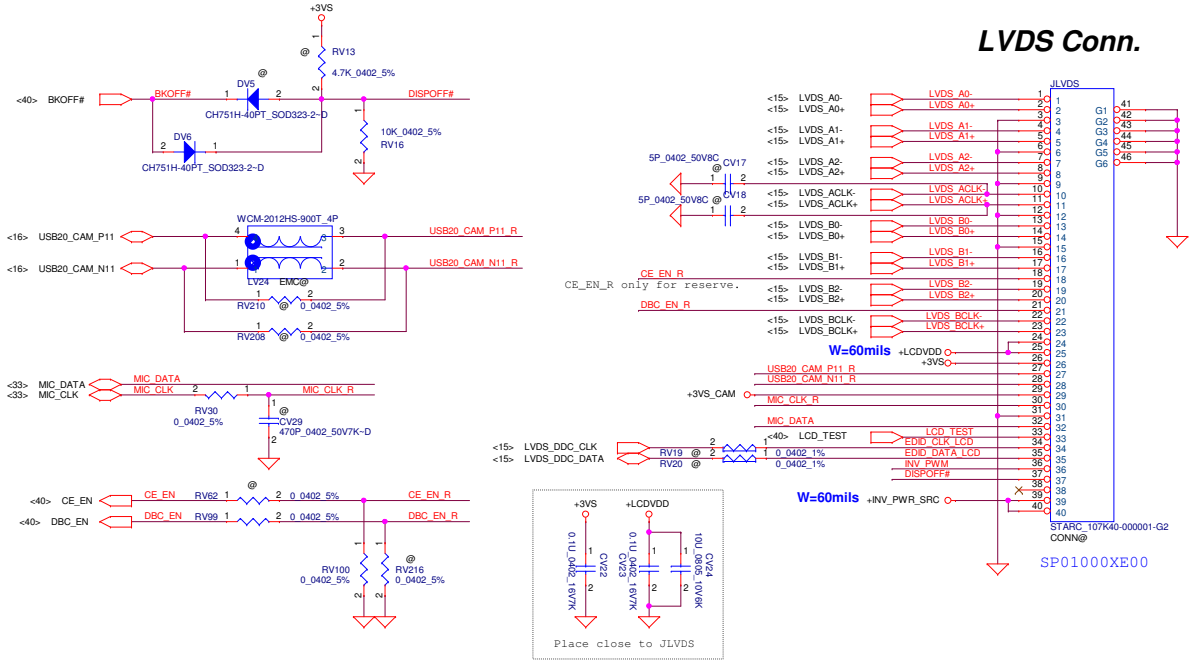
LCD backlight PWR CTRL

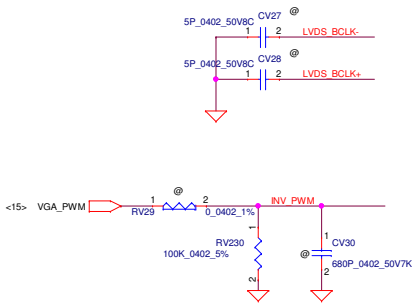


Webcam PWR CTRL

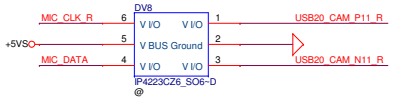


LVDS Conn.

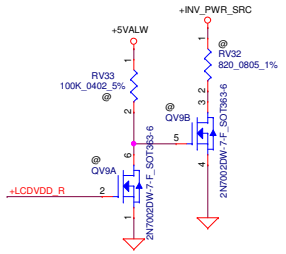




* Reserved for EMI/ESD/RF need to close to JLVDS



* Reserved for LCD sequence tuning



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Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.	
Title	LVDS/webcam
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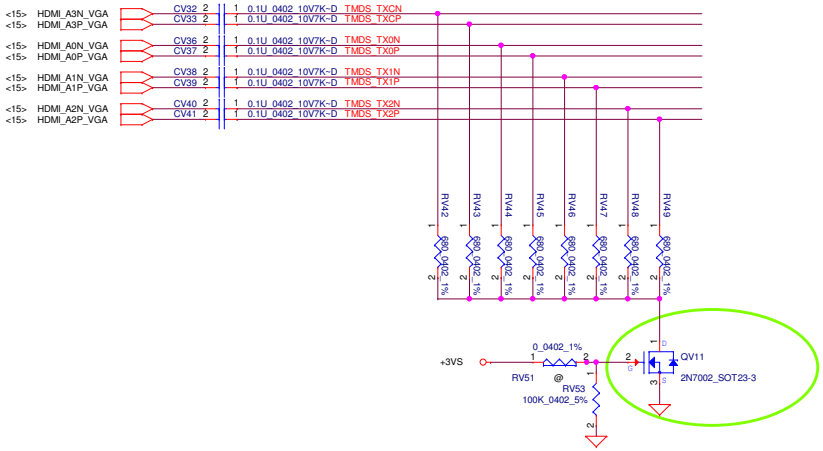
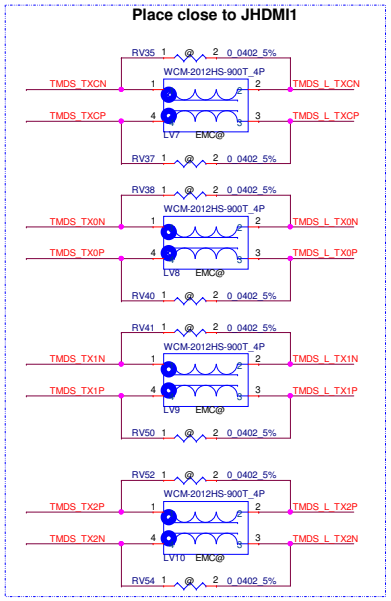
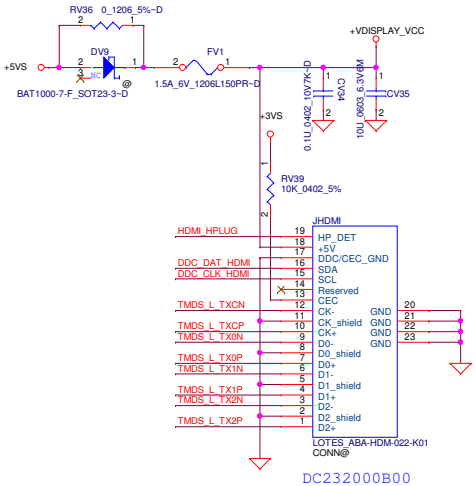
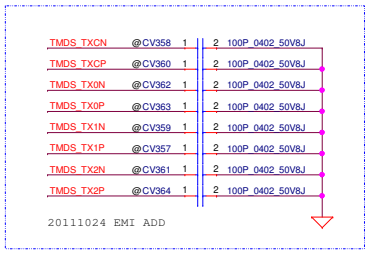
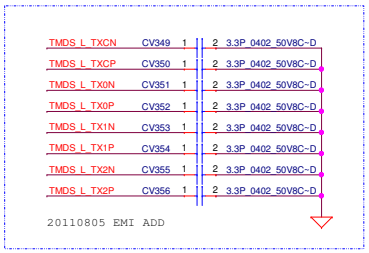
W=40mils

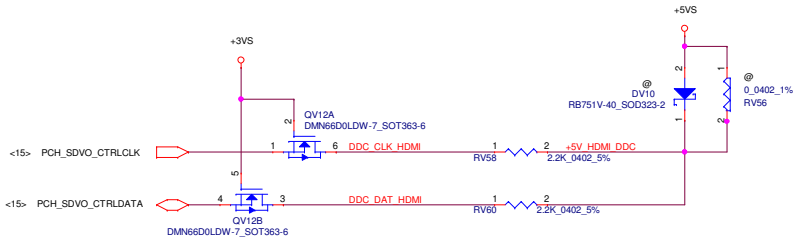


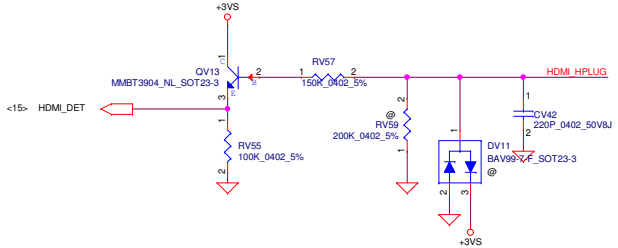












46@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: HDMI

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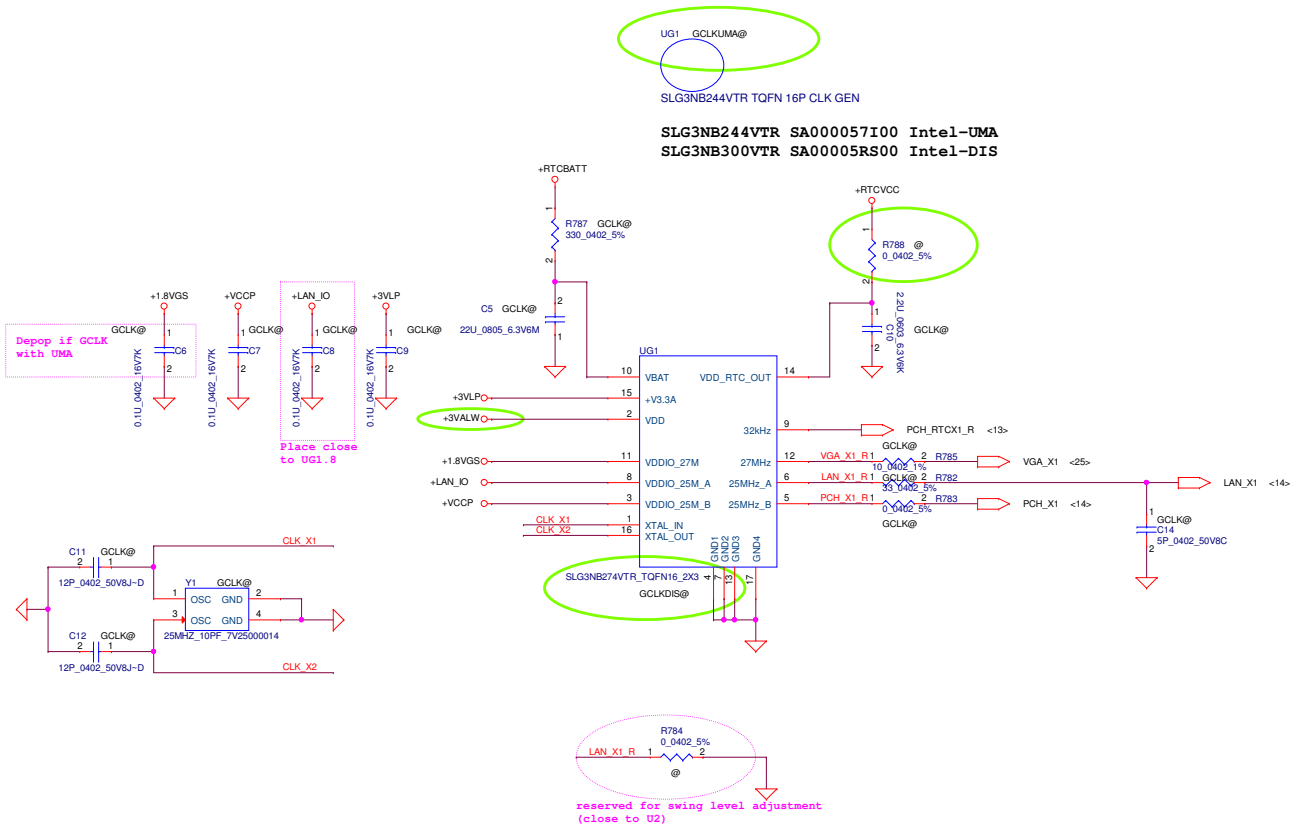

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Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: GCLK

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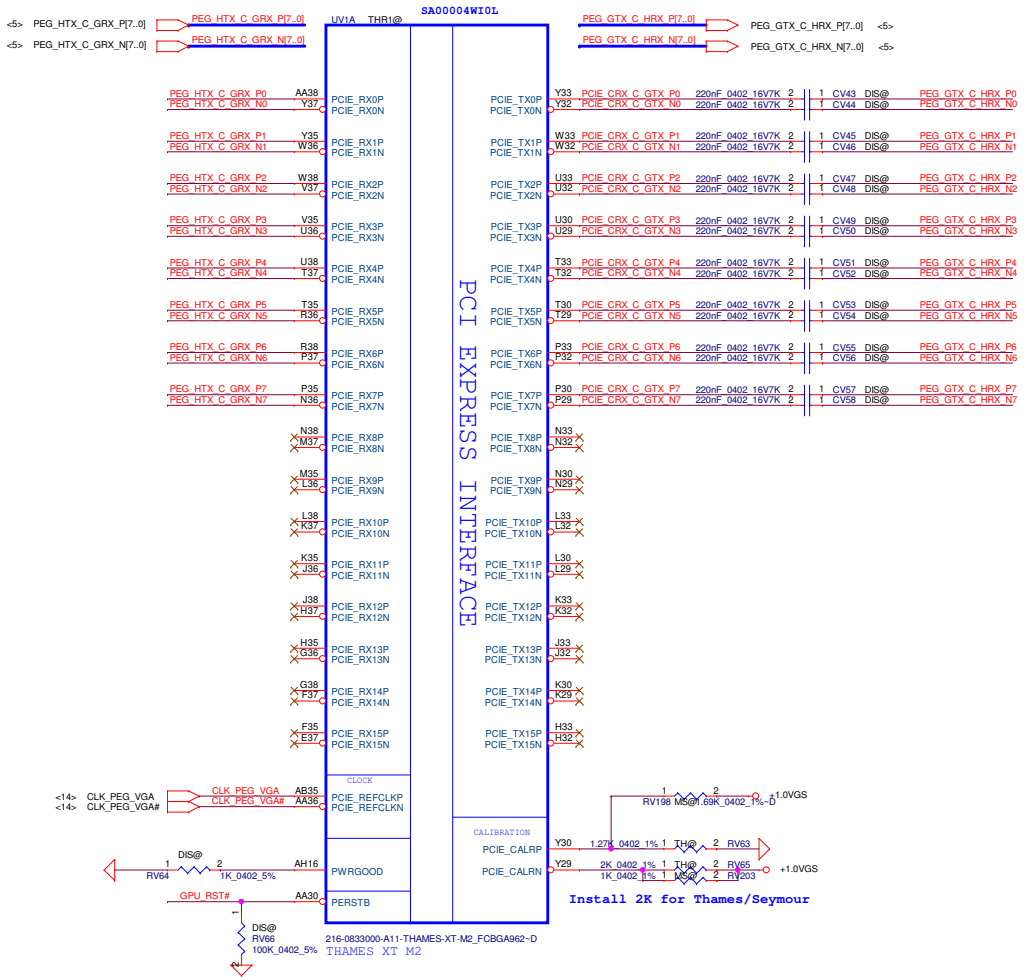
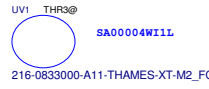
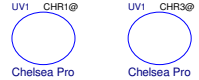
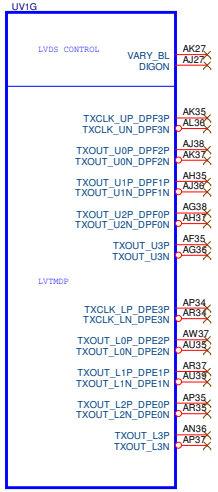
GFX PCIE LANE REVERSAL

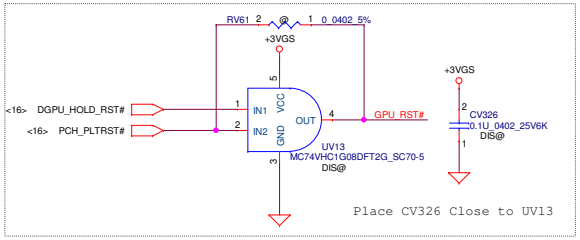






LVDS Interface





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Issued Date	2012/08/22	Deciphered Date	2013/08/31

Title	ATI_ThamesXT_M2_PCIE/LVDS		
Size	Document Number		Rev
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CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING (0: 50% swing 1: Full swing)	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS (0: disable 1: enable)	X
RSVD	GPIO2	Advertises PCIE speed when compliance test (0: 2.5GT/s 1: 5GT/s)	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (0: disable 1: enable)	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)

Mars Pro MLPs	RV241	RV242	Bits [3:1]
Hynix	NC	4.75k	000
Samsung	8.45k	2k	001
Micron	4.75k	NC	111

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
64MX16 (1G) Samsung 1GB SA000004G5OL(R1) SA000004GS1L(R3)	RV68 0	RV69 1	RV72 0
64MX16 (1G) Hynix 1GB SA000041S3L	RV67 1	RV70 0	RV72 0
64MX16 (1G) Micron 1GB SA00004Y20L(R1) SA00004Y21L(R3)	RV67 1	RV69 1	RV71 1
128Mx16 (2G) Samsung 2GB SA000055H0L(R1) SA000055H1L(R3)	RV68 0	RV69 1	RV71 1
★ 128Mx16 (2G) Hynix 2GB SA00003YO2L(R1) SA00003YO3L(R3)	RV67 1	RV70 0	RV71 1 PT
128Mx16 (2G) Micron 2GB SA00005XB0L(R1) SA00005XB1L(R3)			

STRAPS

Internal VGA Thermal Sensor

VGA Thermal Sensor ADM1032ARMZ

Closed to GPU

Address:100_1101

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Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_Main_MSIC

Size: | Document Number: LA-9101P | Rev: 0.4

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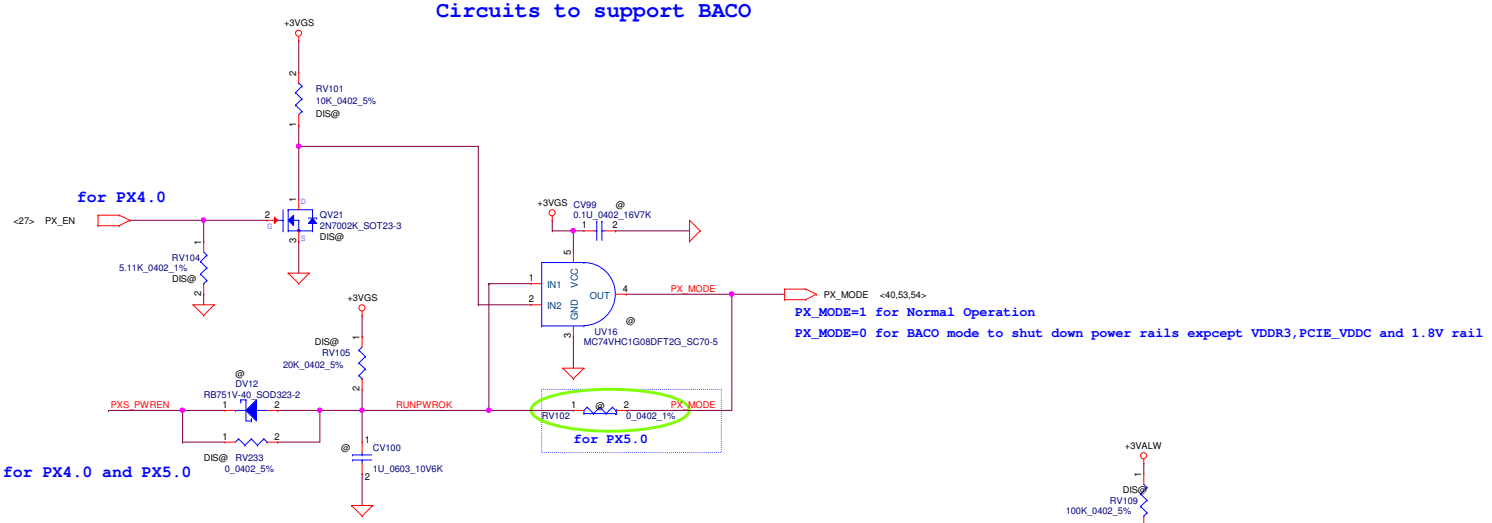
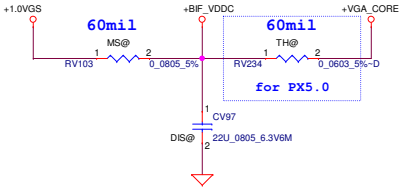
Circuits to support BACO

Switch circuits in BACO desingns for Thanes/Seymour only

55mA@1.0V, in BACO mode





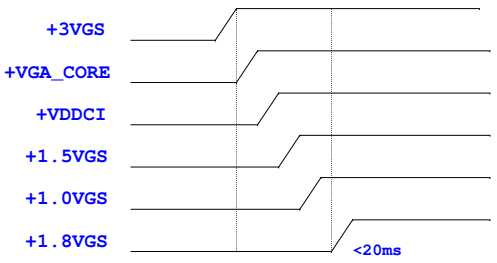
Note:

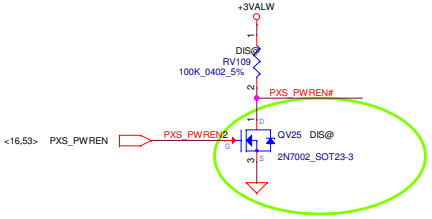
PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON

PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF

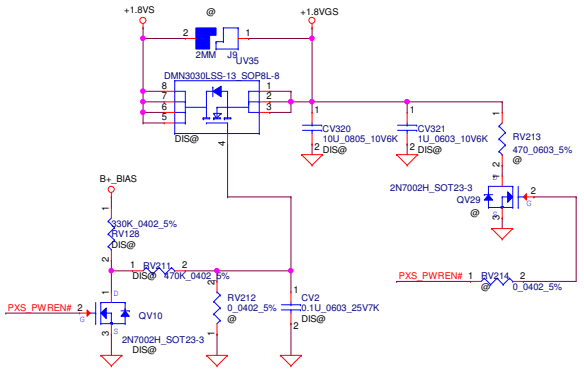
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

Power Seguence of Thames and Mars Pro

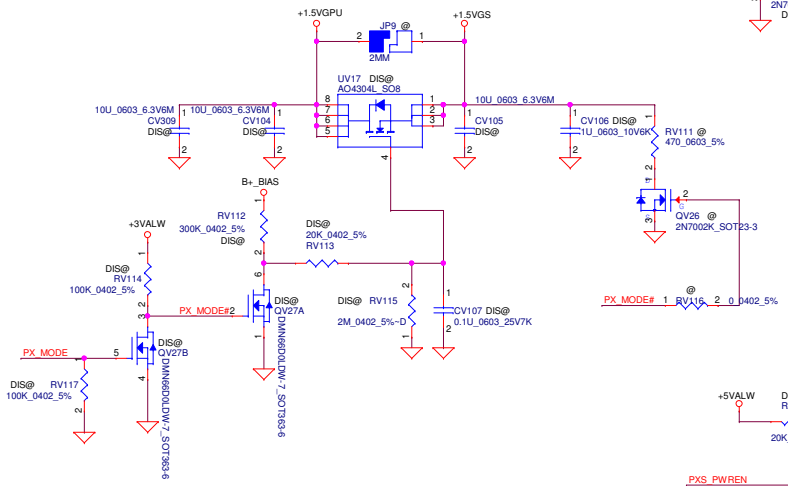




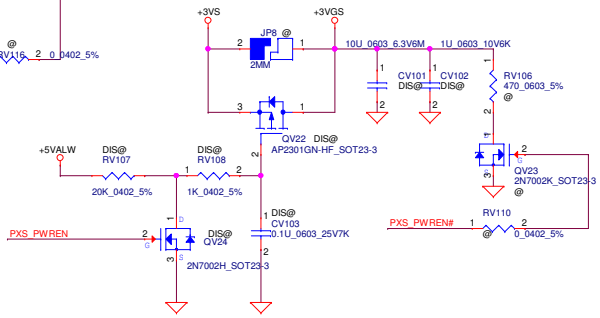
+1.8VS TO +1.8VGS



+1.5VGPU TO +1.5VGS



+3.3VS TO +3.3VGS



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Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.	
Title	ATI_ThamesXT_M2_BACO POWER
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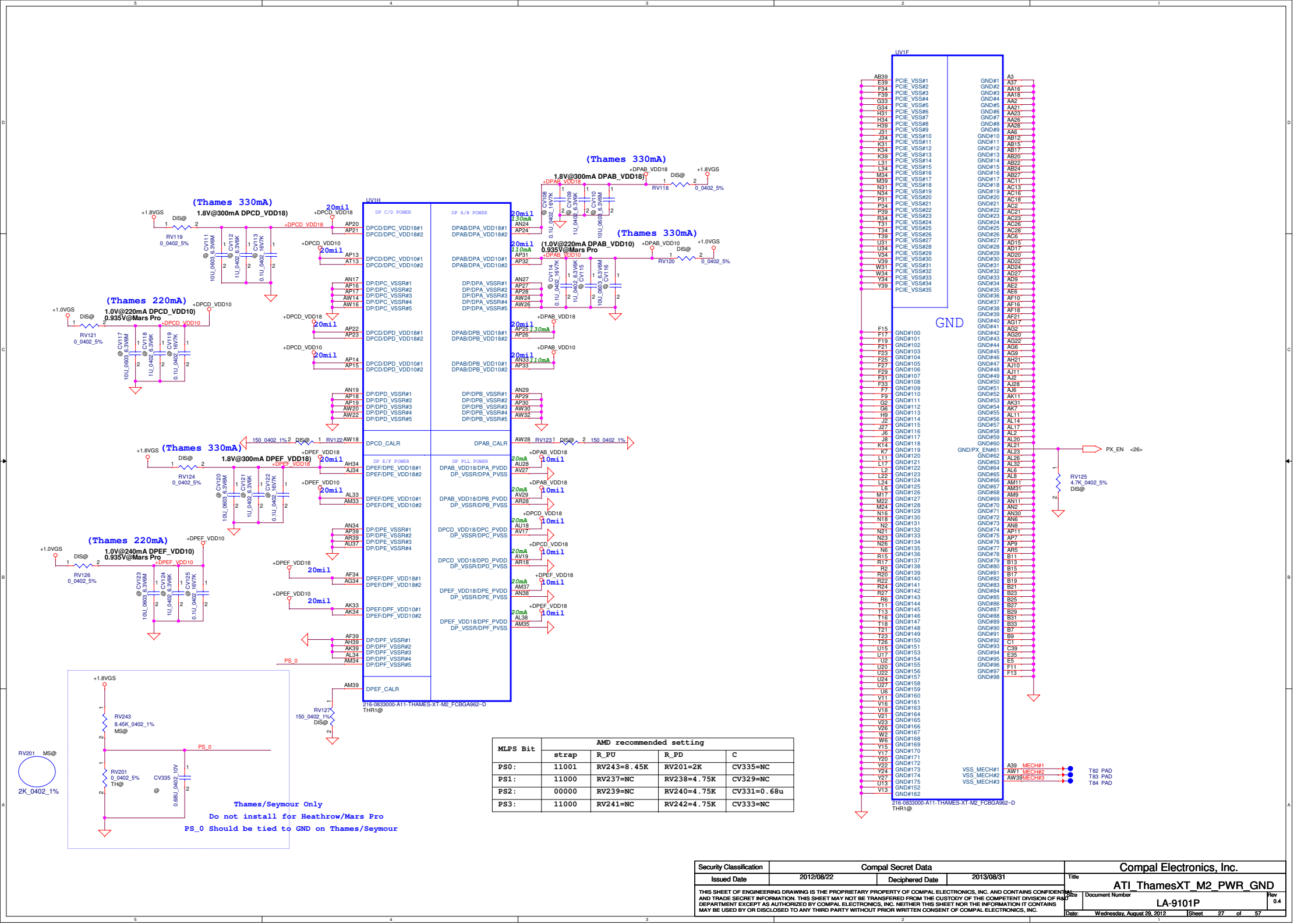

MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

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Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_PWR_GND

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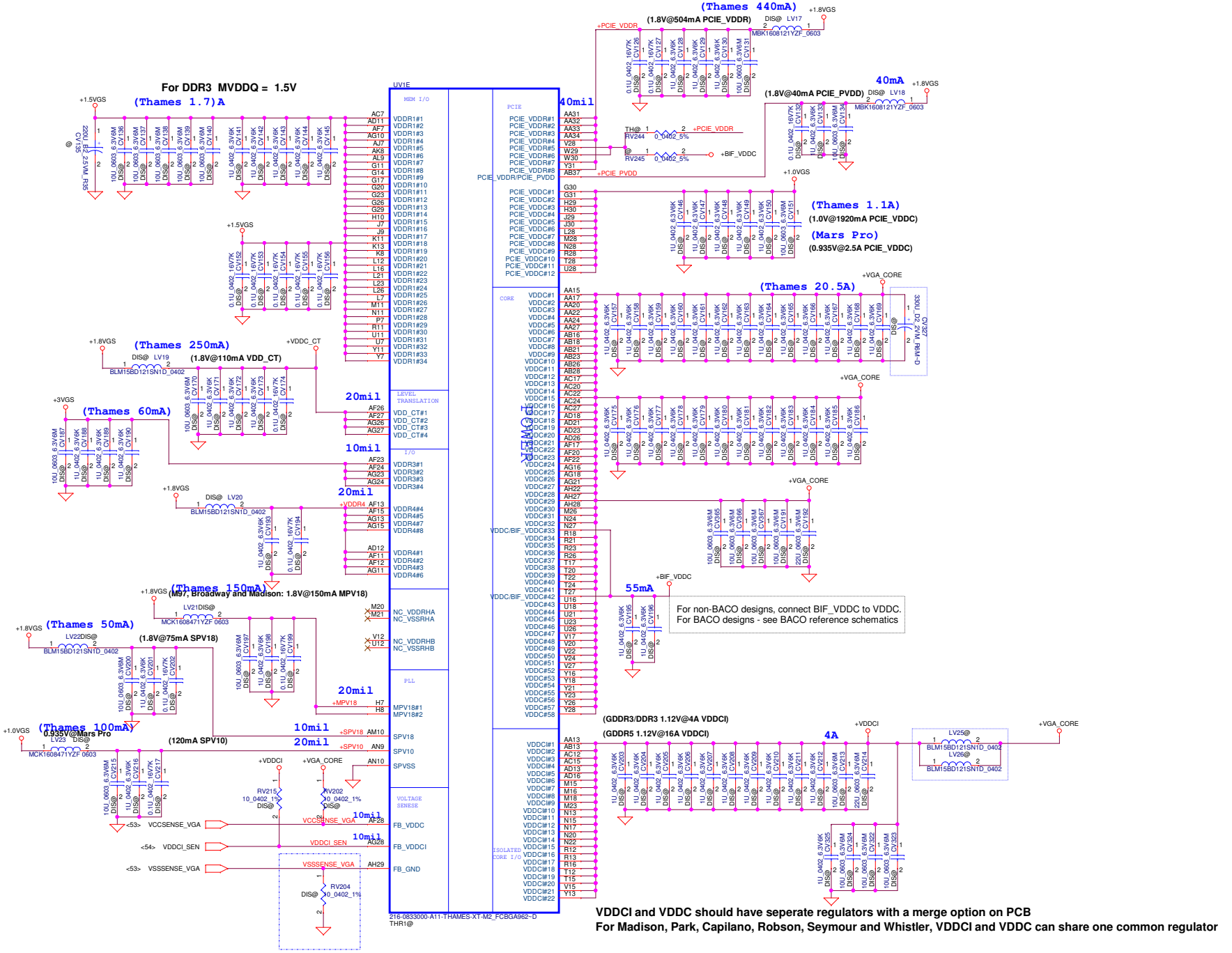
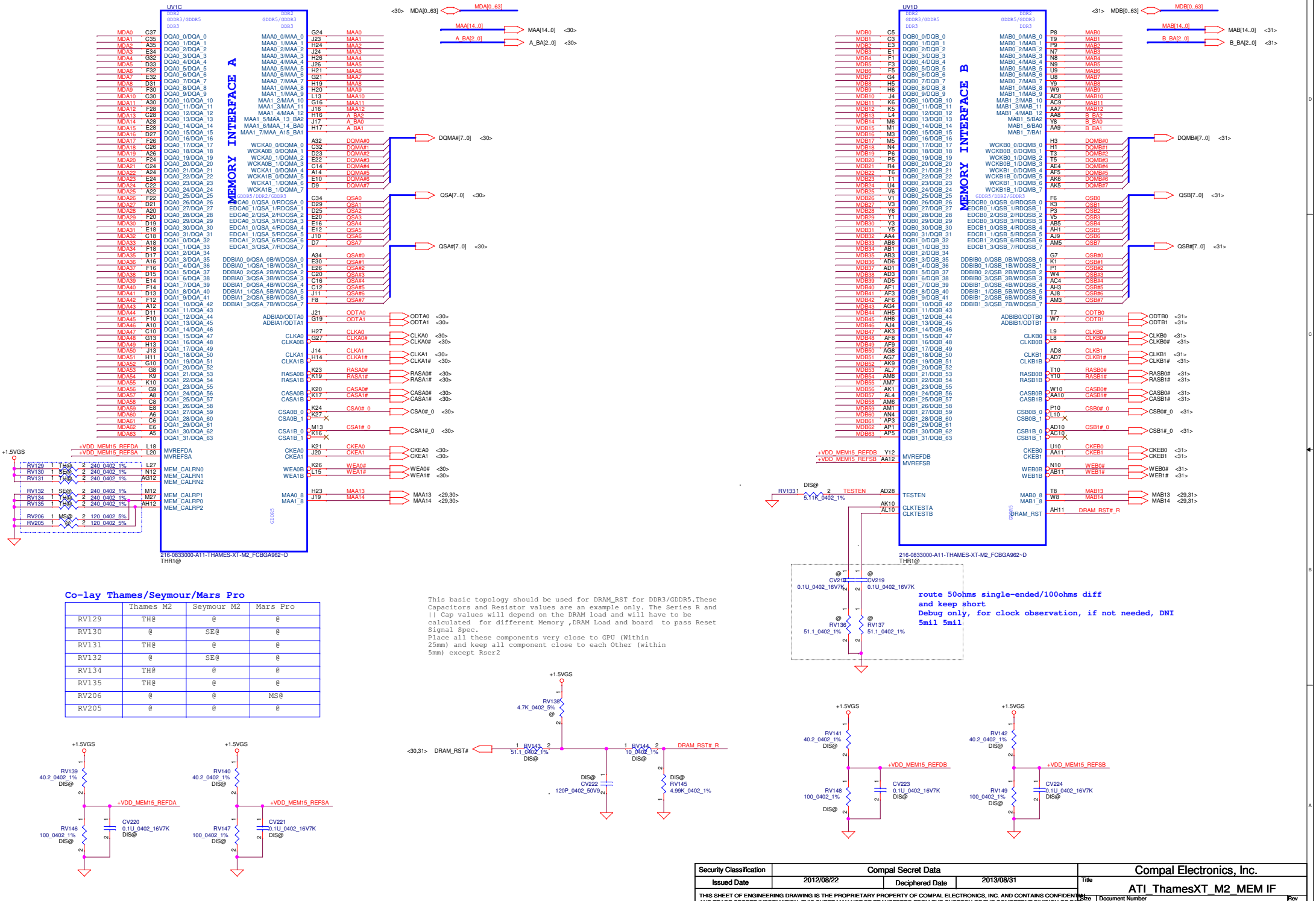
Date: Wednesday, August 29, 2012 | Sheet 27 of 57



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title	ATI_ThamesXT_M2_Power
				Size	Document Number: LA-9101P Rev: 0.4
				Date: Wednesday, August 29, 2012	Sheet 28 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_MEM IF

Size | Document Number: LA-9101P | Rev: 0.4

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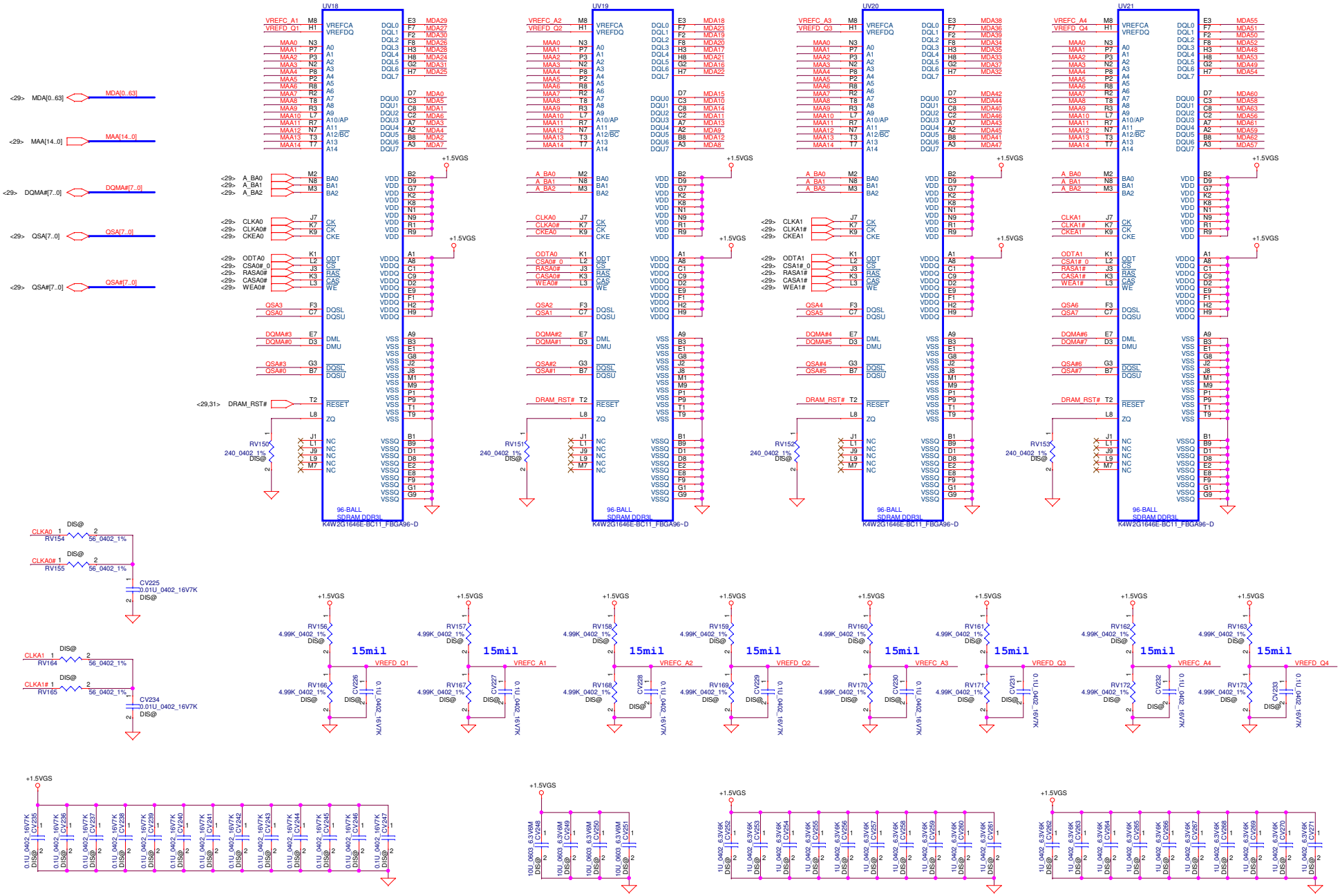
CHANNEL A: 256MB/512MB DDR3



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_VRAM_A

Size	Document Number	Rev
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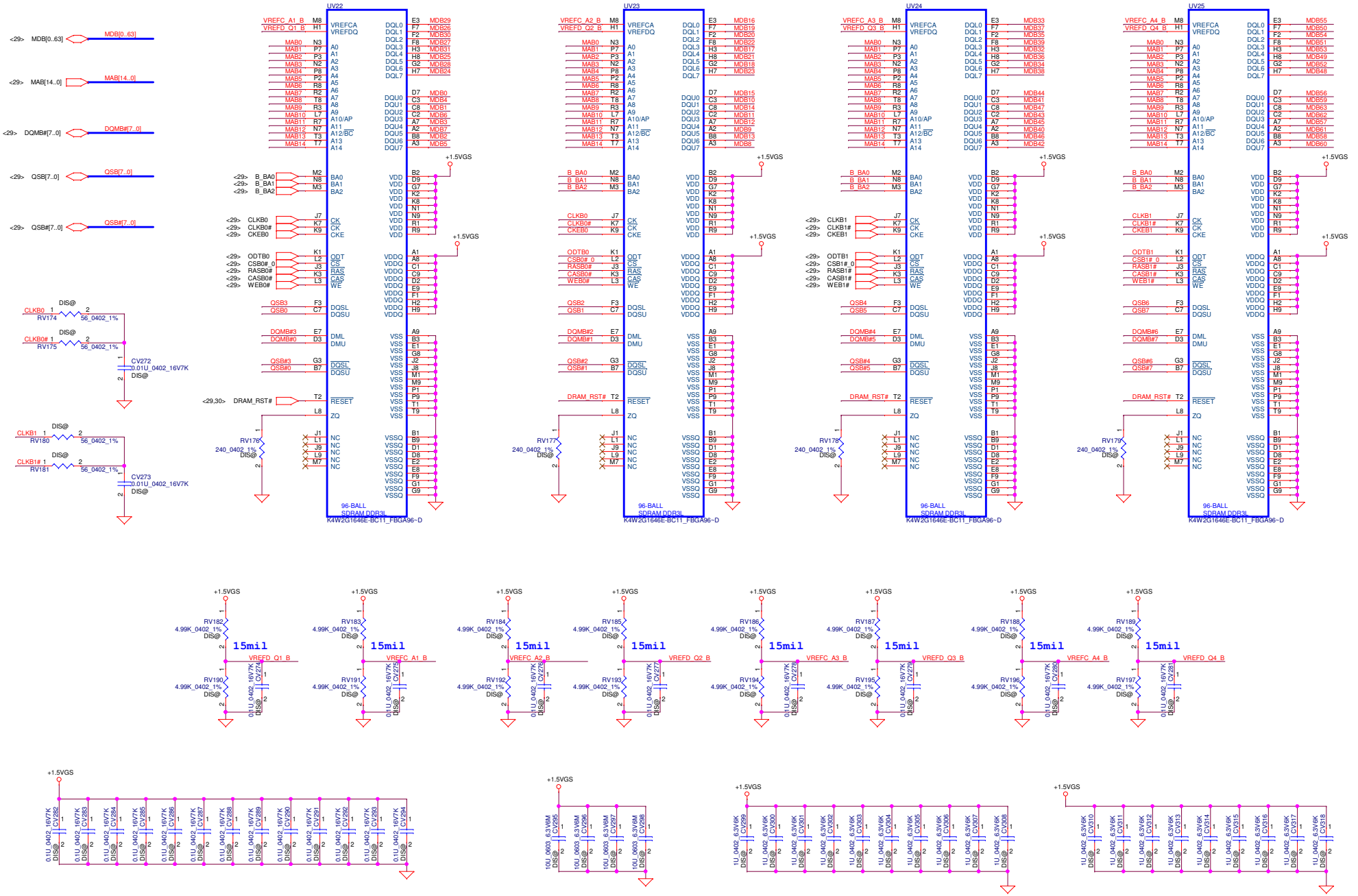
CHANNEL B: 256MB/512MB DDR3



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_VRAM_B

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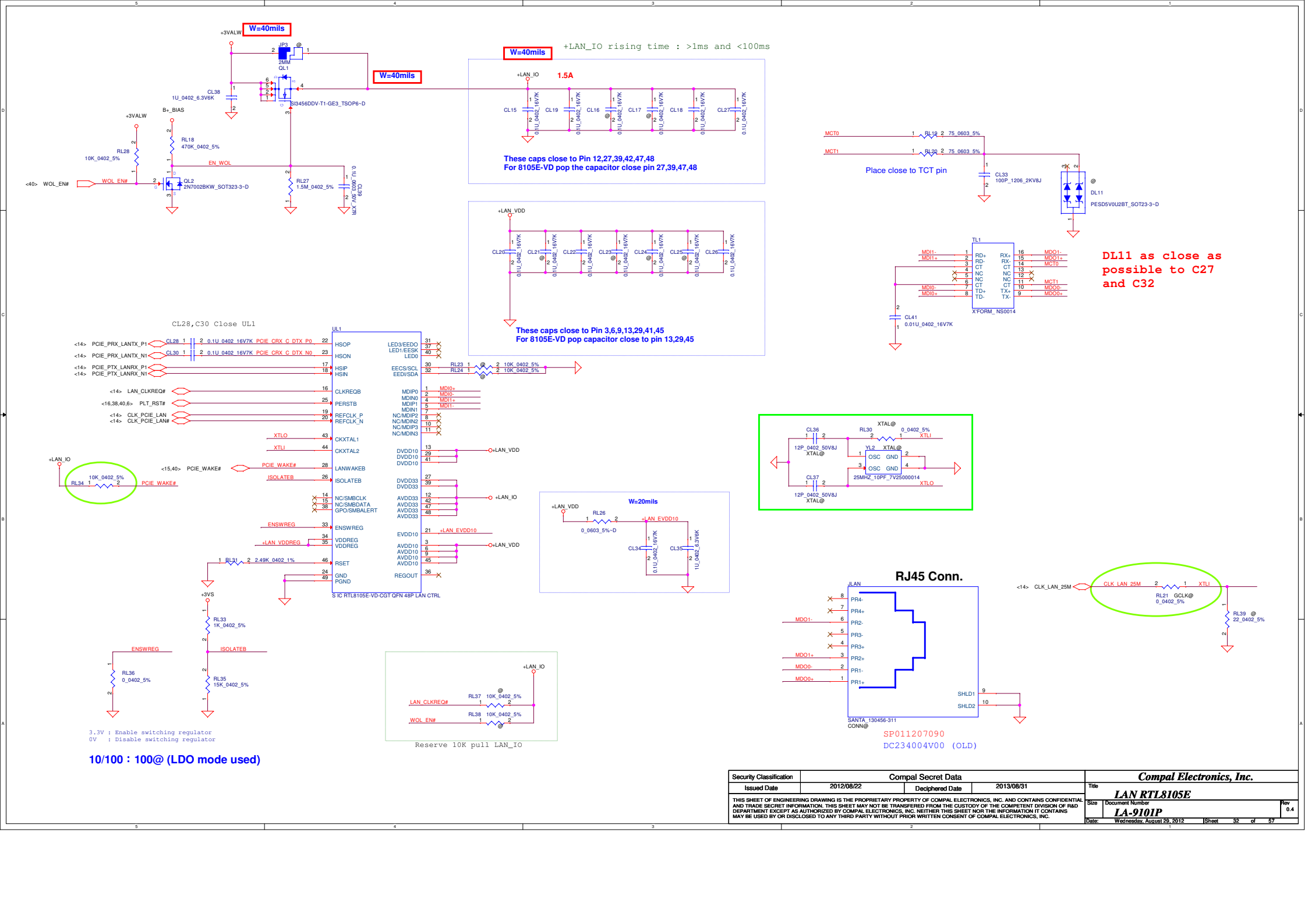
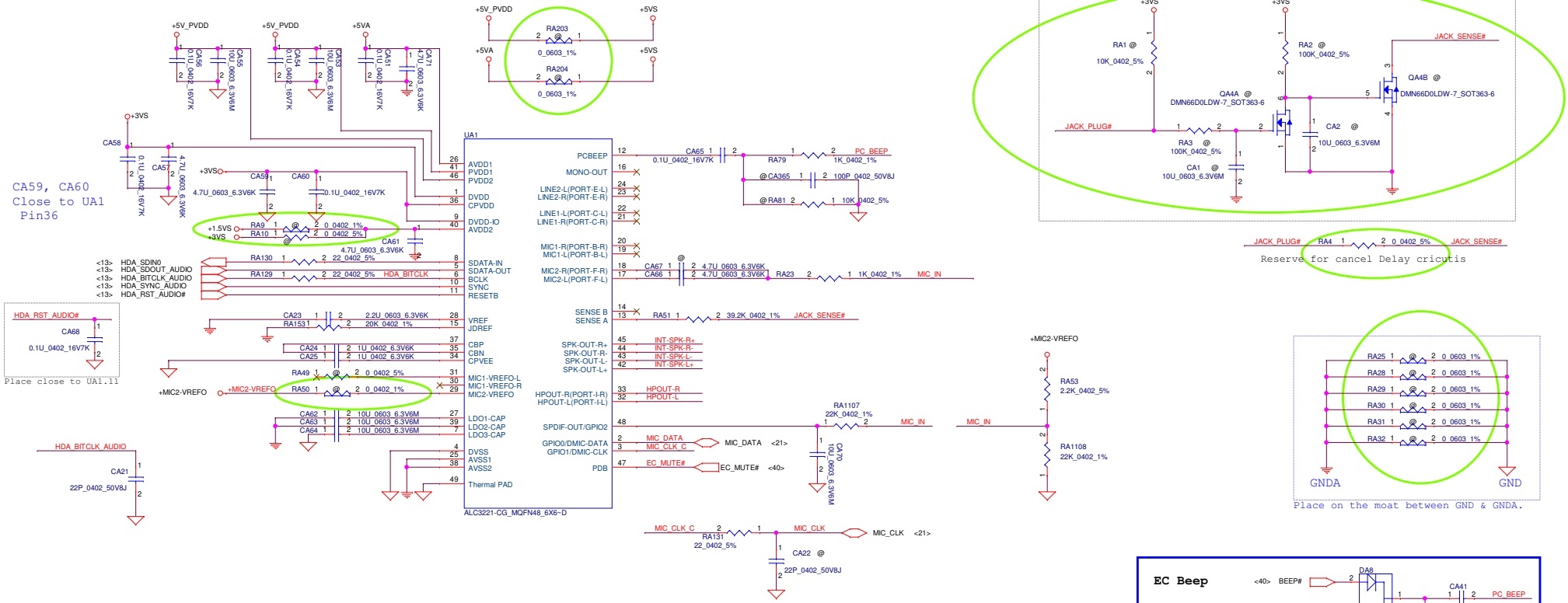
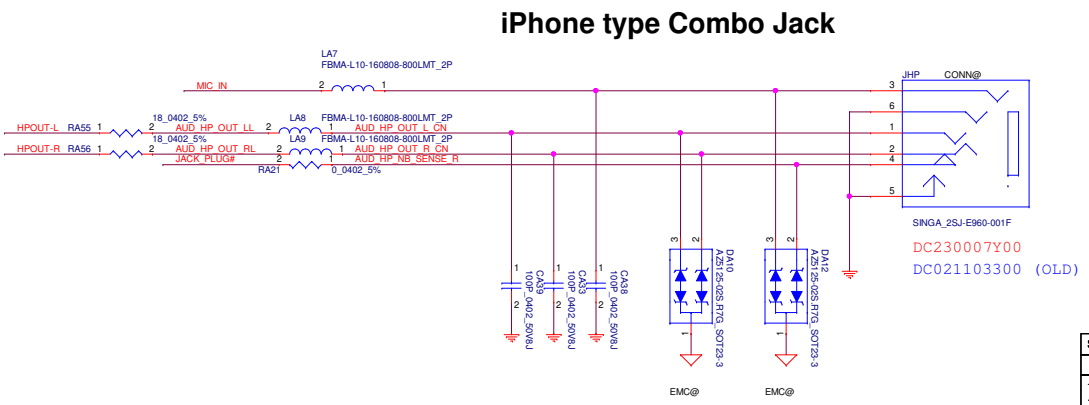


Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.			
Title: LAN RTL8105E			
Size	Document Number: LA-9101P		Rev: 0.4
Date: Wednesday, August 29, 2012	Sheet 32 of 57		





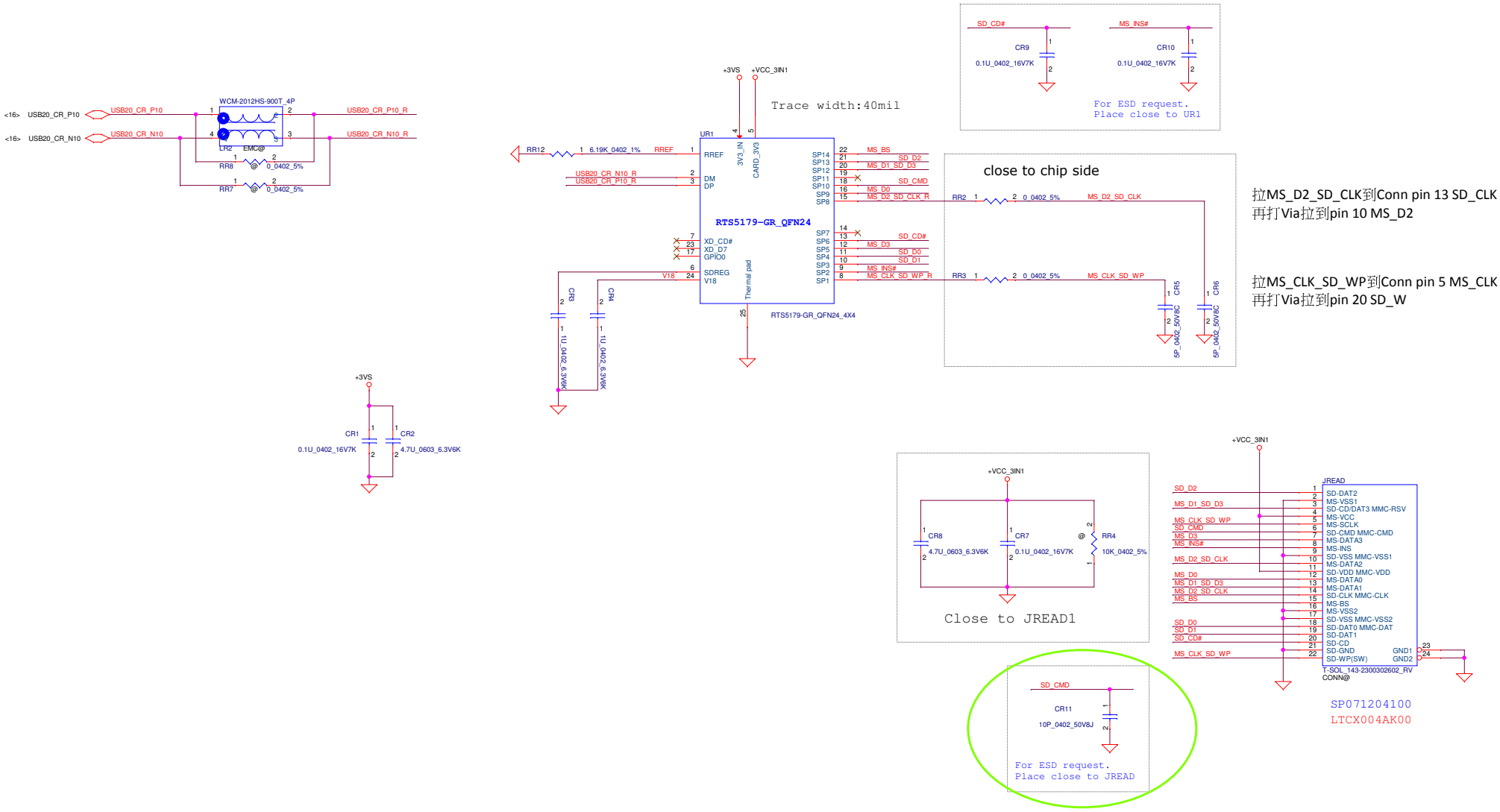
Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: Audio Codec ALC3221

Size | Document Number: LA-9101P | Rev: 0.4

Date: Wednesday, August 29, 2012 | Sheet 33 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: **Card Reader RTS5179**

Size: | Document Number: **LA-9101P** | Rev: 0.4

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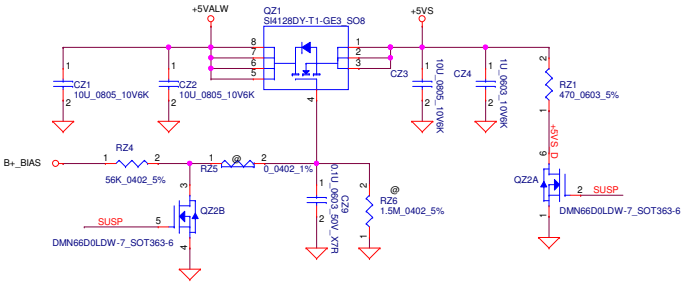
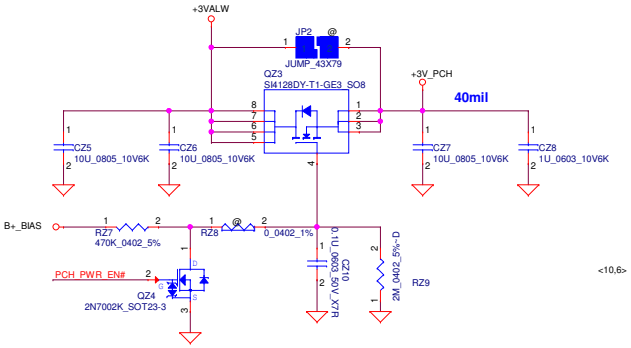
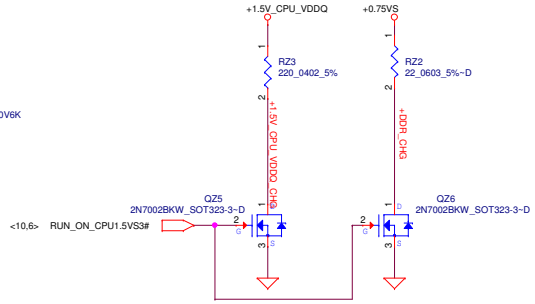
+5VALW to +5VS

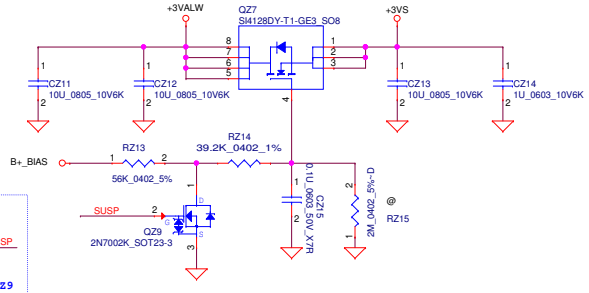


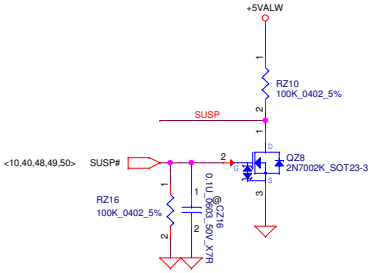
+3VALW to +3V_PCH

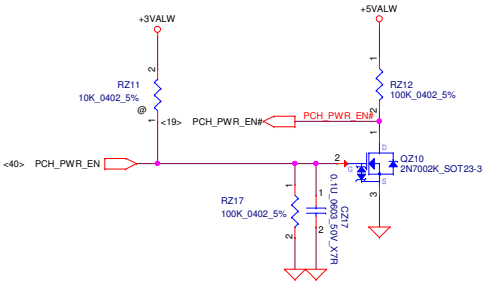




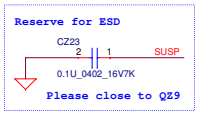
+3VALW to +3VS



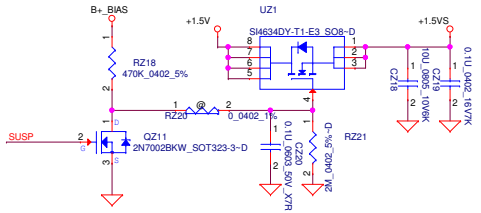


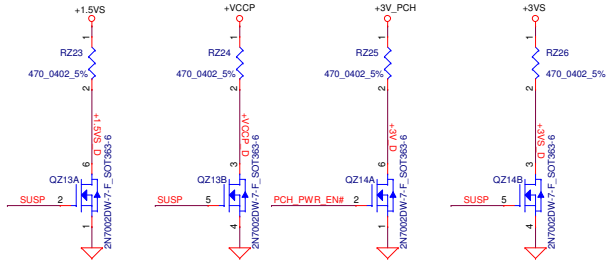


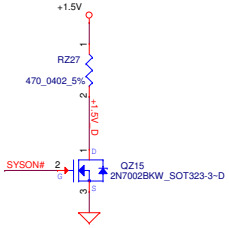
Reserve for ESD

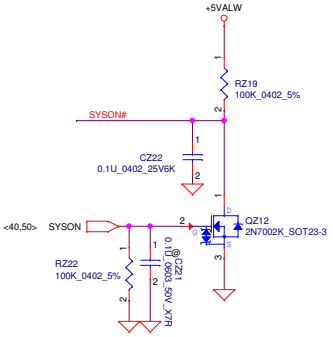


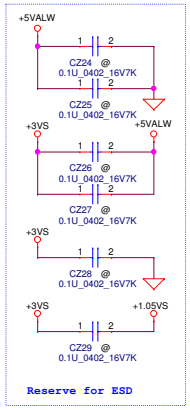
+1.5V To +1.5VS



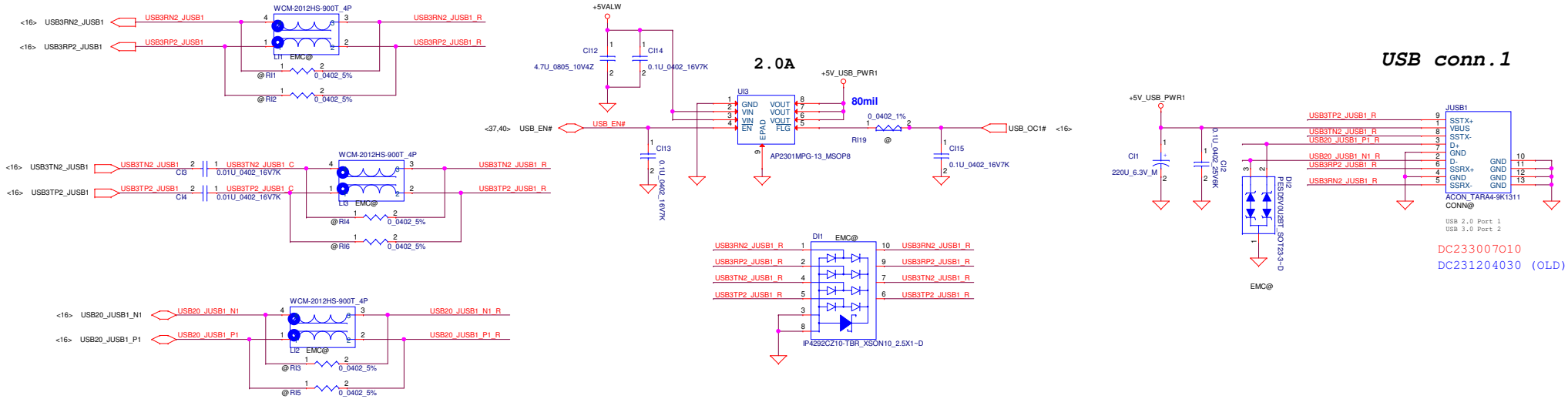


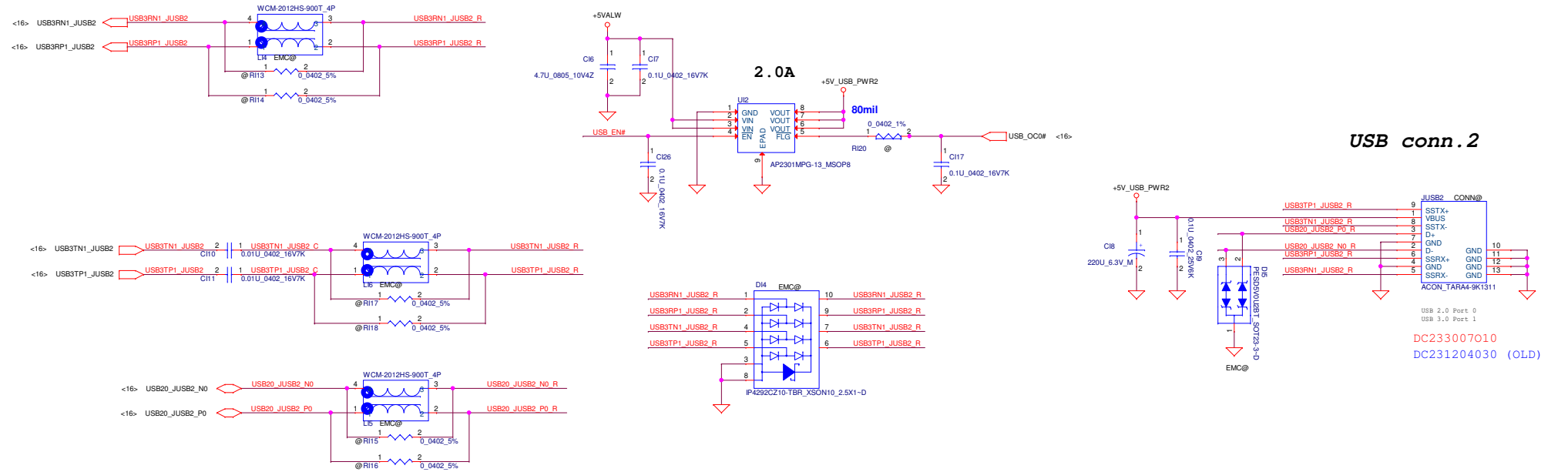






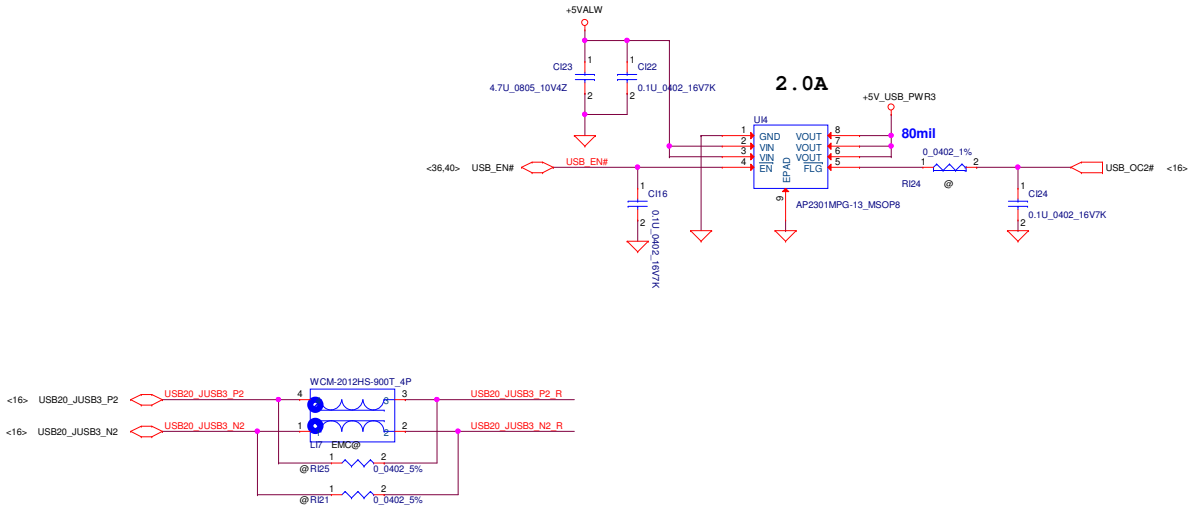
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title: DC/DC Interface
				Size: Document Number: LA-9101P Rev: 0.4
				Date: Wednesday, August 29, 2012 Sheet 35 of 57



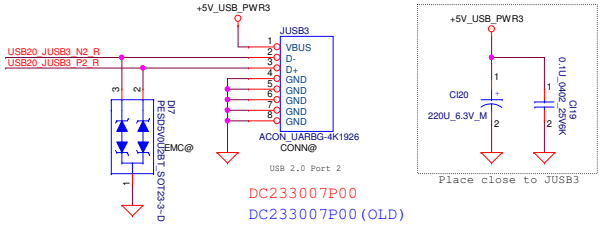


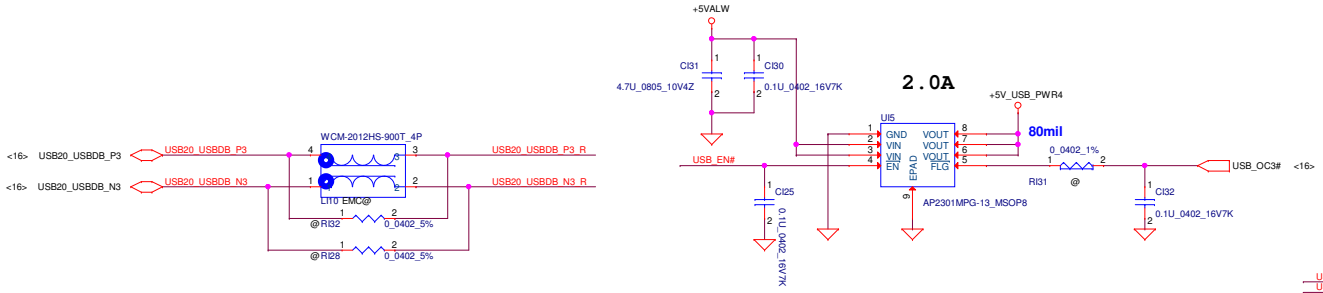
Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.			
Title: USB3.0			
Size	Document Number: LA-9101P		Rev: 0.4
Date: Wednesday, August 29, 2012	Sheet 36 of 57		

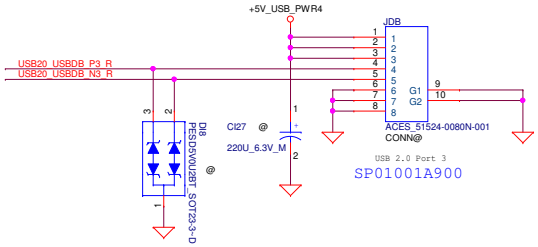


USB conn.3





USB conn.4



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.	
Title	MB to USB2.0 DB
Size	Document Number: LA-9101P
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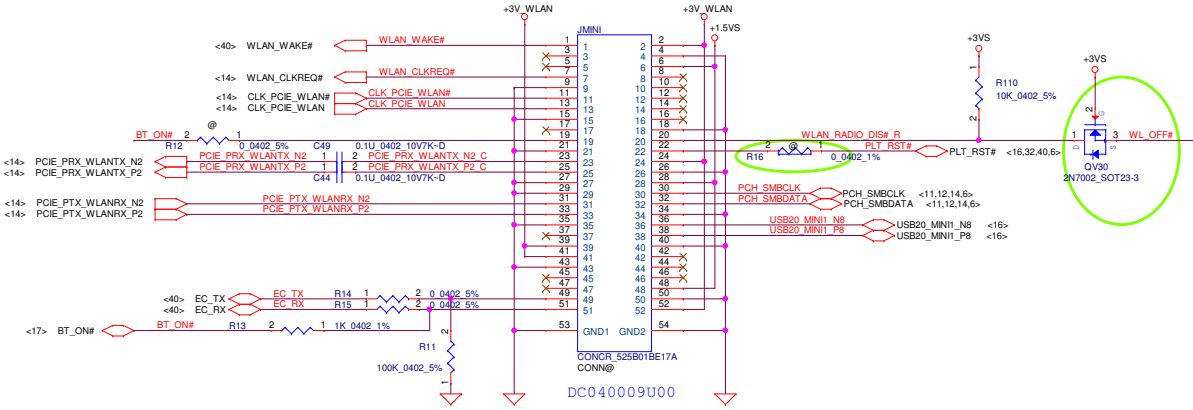
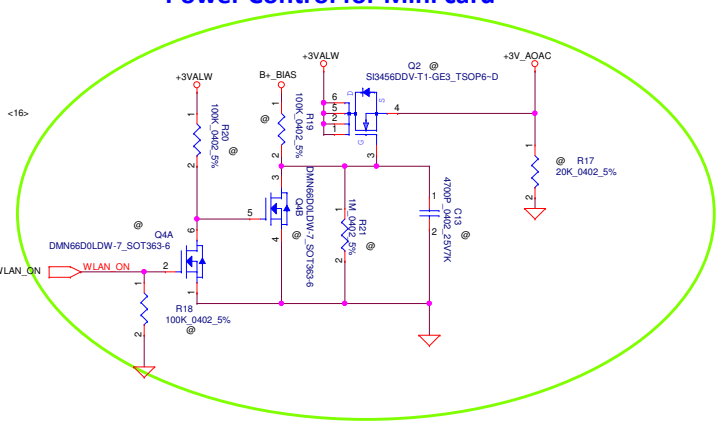
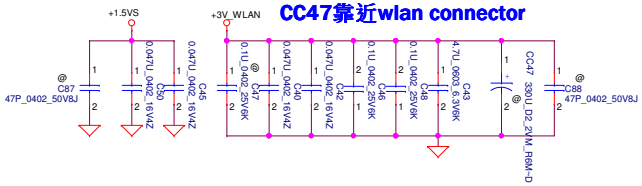
Mini WLAN/WIMAX H=6.7

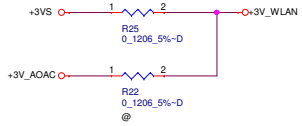


Power Control for Mini card

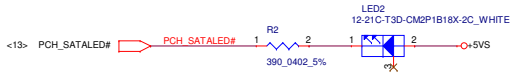


CC47靠近wlan connector

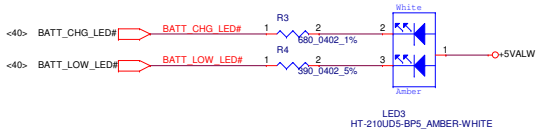




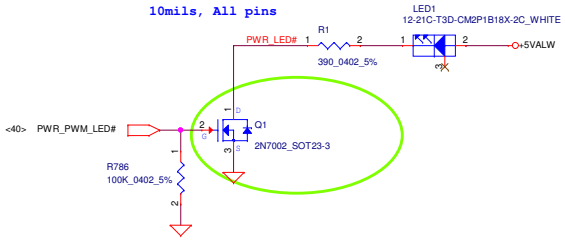
HDD LED



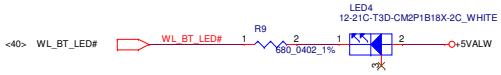
Battery LED



Power LED



Wireless LED



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: Mini Card/LED

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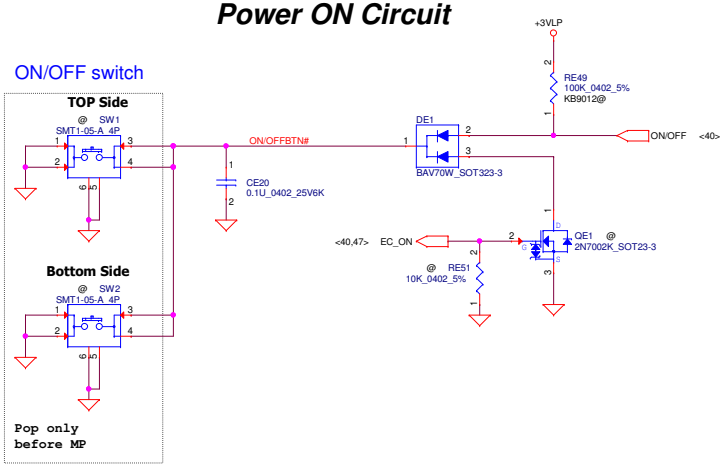
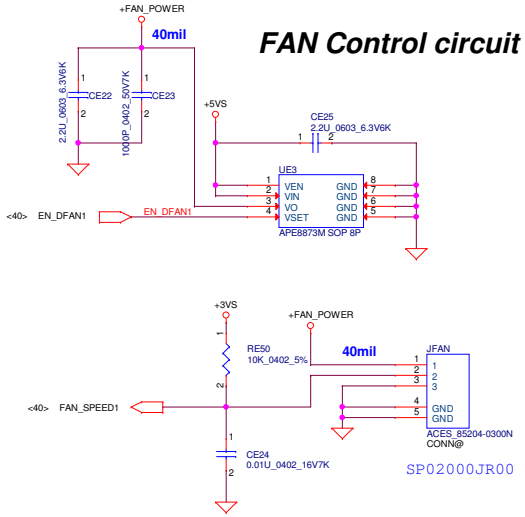
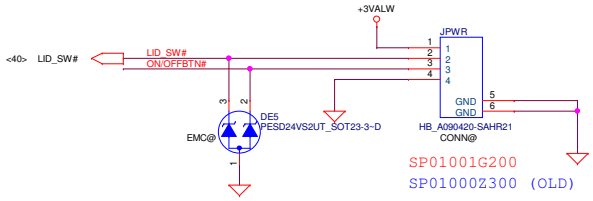
Power ON Circuit



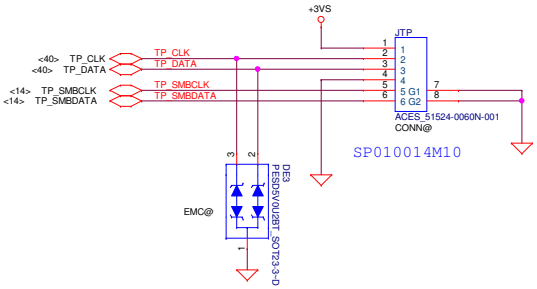
FAN Control circuit



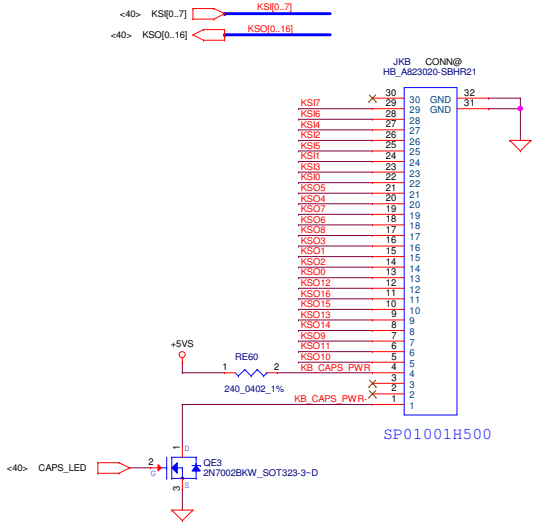
POWER/B



Touch pad



INT_KBD Conn.



Security Classification	Compal Secret Data			
Issued Date	2012/08/22	Deciphered Date	2013/08/31	

Compal Electronics, Inc.			
Title: FAN/TP/KB/PWR SW			
Size	Document Number: LA-9101P		Rev: 0.4
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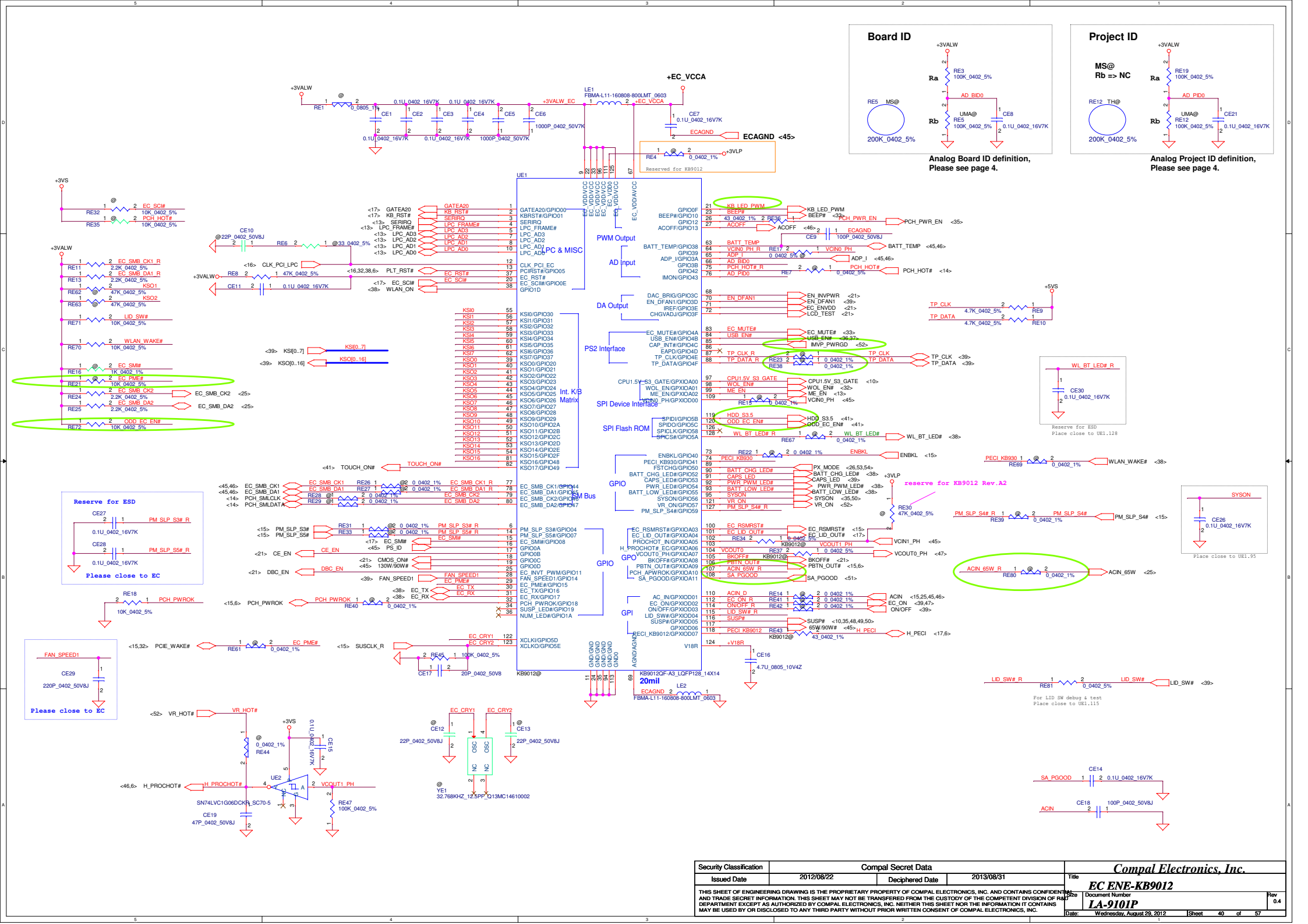

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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Compal Electronics, Inc.

Title: EC ENE-KB9012

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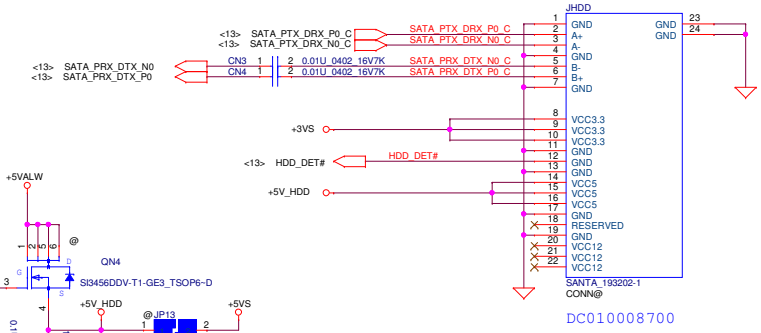
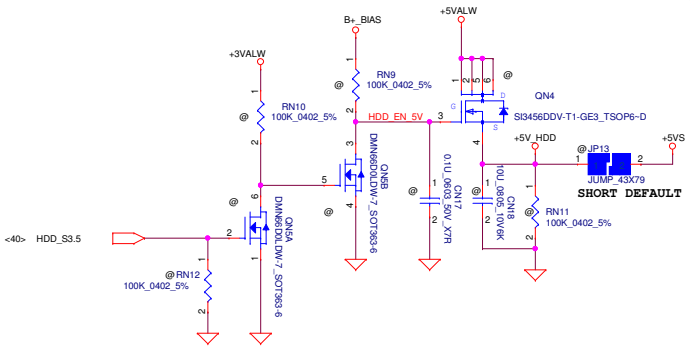
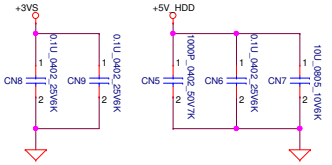
SATA HDD Conn.

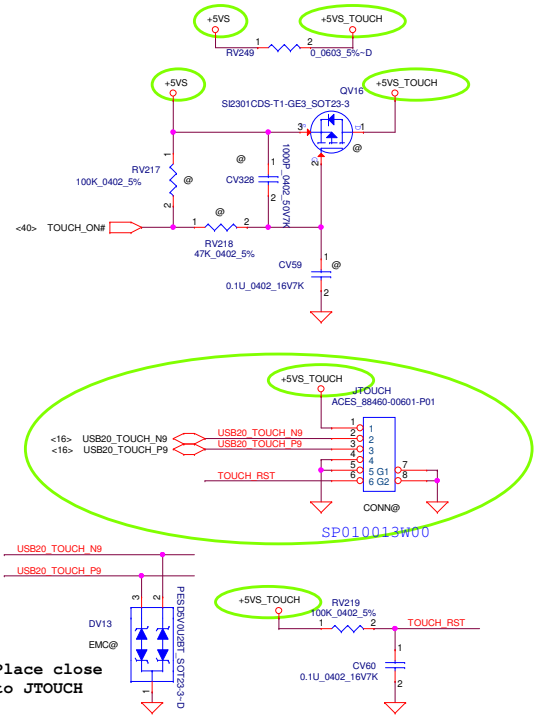


+5V_HDD Source

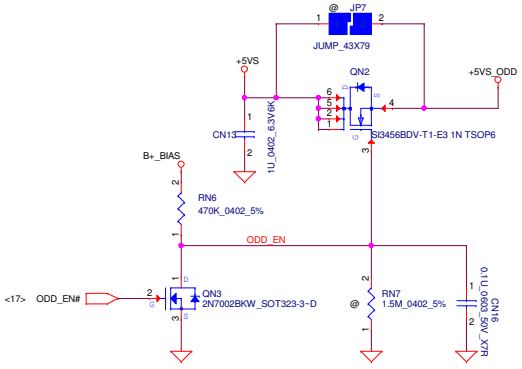


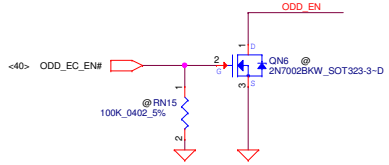


* Touch Screen Panel



ODD Power Control





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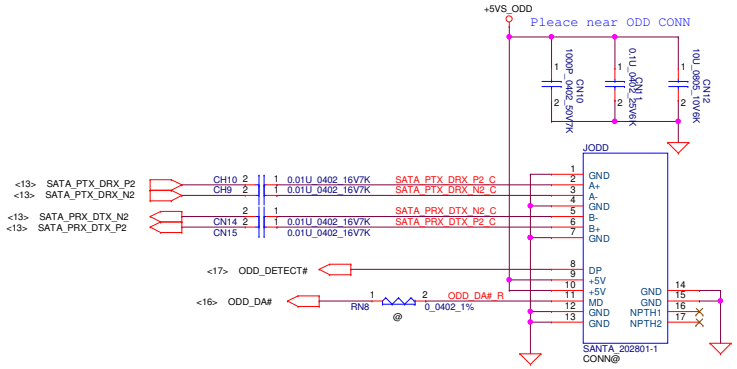

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: HDD / ODD

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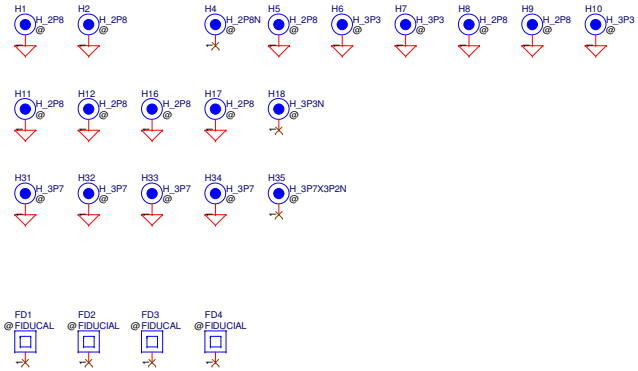
Screw Hole



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: Screw Hole

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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2	40	Keyboard	2012/05/03	SED	Keyboard pin define change.	Follow new SPEC.SWAP JKB pin define.	0.2
3	16,21,34, 36,37,38	USB	2012/05/04	Function team	Change USB port assignment for function team request	USB port change detail please reference Page.16 descrption.	0.2
4	26	VGA	2012/05/05	HW	Delete reserve BACO circuit	Delete UV15,QV16,QV17,QV18,QV19,QV20,RV99,RV100,RV249,CV96,CV98	0.2
5	42	DC/DC	2012/05/07	HW	Design change	UN-POP RZ11, POP RZ17	0.2
6	33	Audio codec	2012/05/09	ESD	ESD team ask solution	Add RA29,RA30,RA31,RA32 and place on the moat between GND & GNDA	0.2
7	6,17	PCH	2012/05/09	ESD	ESD team ask reserve solution	Add CC151,CH102 for reserve	0.2
8	32	LAN	2012/05/10	HW	Remove China Go-rural for DELL request	Remove DL7,DL8,DL9	0.2
9	16,38	USB	2012/05/10	HW	Remove JUSB3 USB3.0	Delete LI8,LI9,DI6 and change JUSB3 to USB2.0 type	0.2
10	32	Crystal	2012/05/15	HW	Crystal vendor suggestion	Change CL36,CL37 from 33p/0402 to 12p/0402	0.2
11	21,39	LVDS	2012/05/17	SED	Add FHD Panel CE_ENABLE, DBC_ENABLE function from SED request	Add CE_EN, DBC_EN control pin to EC	0.2
12	21	LVDS	2012/05/22	SED	Follow SED team request disable CE_EN function	Change RV62 to DE-POP and RV100 to POP for disable CE_EN function	0.2
13	33	Audio codec	2012/05/23	CODEC	Follow CODEC vendor suggestion	Add AUDIO JACK PLUG delay circuit, Spearate NET JACK_PLUG to => JACK_SENSE# & => JACK_PLUG#	0.2
14	16,21	Touch Screen	2012/05/29	HW	Add touch screen function	Add RV217, RV218, RV219, RV249, CV59, CV60, CV328, DV13, QV16, JTOUCH	0.2
15	39	Board ID	2012/05/30	HW	Board ID change for PT	Change RE5 from 8.2k_0402(SD028820180) to 33k_0402(SD028330280)	0.2
16	21,39	Touch Screen	2012/05/30	HW	Add touch screen function power control	Add NET "TOUCH_ON#" from JTOUCH to UE1.82(KB9012) for TOUCH SCREEN PANEL power control	0.2
17	33	Audio codec	2012/05/30	HW	Follow RealTek suggestion remove, delete reserve MUTE circuit	Delete D1,QA1,QA2,QA3,RA24,RA26,RA60,RA62,RA68,RA109,CA72,CA73	0.2
18	15,16, 39,41	ESD	2012/05/30	ESD	ESD ask CAP for reserve	Reserve 0.1u/0402 CH104,CZ23,CH105,CE27,CE28	0.2
19	14	Green CLK	2012/05/30	HW	For Green CLK test	Change RH31,RH41,RV232 0ohm form "GCLK@" to "@" for break the clock signal to device	0.2
20	10,26,41	DC/DC	2012/05/31	HW	Change "+1.5V_CPU_VDDQ", "+1.5VS", "+1.5VGS" derating	Change RC150 330K/0402 to 2M/0402, RC151 100K/0402 to 470K/0402, RZ18 100K/0402 to 470K/0402, RV115 0/0402 to 2M/0402	0.2
21	41	DC/DC	2012/05/31	HW	For power sequence trunning	Change RZ15 to DE-POP	0.2
22	06,15,16, 39,41	ESD	2012/05/31	ESD	Follow ESD team request	Change 0.1u/0402 from "@" to POP	0.2
23	32	Green CLK	2012/06/15	HW	Change for Green CLK bom control	Change RL21,RL30 from "@" to "GCLK@"	0.2
24	41	DC/DC	2012/06/15	HW	For WLAN card power sequence issue	Change RZ4,RZ13 from 470K/0402 56K/0402	0.2
25	35,41	Schematic page modify	2012/06/18	HW	Schematic page modify for easily maintain.	Swap Page. 35 & Page 41.	0.2
26	41	ODD	2012/06/18	HW	Change component location for easily maintain.	Move RH42,RH43 from Page.13 to Page.41.	0.2
27	39	FAN	2012/06/29	HW	Fan speed noise issue	Reserve 220p/0402 CE24	0.3
28	6	CPU	2012/06/29	ESD	System boot-up shot down issue.	Change CC151 from POP to "@"	0.3
29	21,35, 39,40,41	Circuit adjuest	2012/07/01	HW	Circuit & page adjust for OAK 15" & OAK 17"	1. Swap P.35 & P.41and move touch screen circuit from P.21 to P.41. 2. Swap P.39 & P.40 page no	0.3
30	40	LID SW	2012/07/01	HW	LID SW need a trace for debug and switch.	Add RE81 for LID SW.	0.3
31	25	GPU	2012/07/01	HW	Follow AMD request, MarsPro will used MPLs.	Change RV75,RV76,RV81 from "DIS@" to "TH@"	0.3
32	29	GPU	2012/07/01	HW	Follow AMD request, MEM_CALRP2 is not need for Mars ASIC now.	Change RV205 from "MS@" to "@"	0.3
33	38	MINI card	2012/07/03	HW	Power Control for Mini card didn't need	Change R17 to "@"	0.3
34	6	XDP	2012/07/06	HW	S3 return hang issue	Change RC89 from "@" to POP	0.3
35	23	GREEN CLK	2012/07/09	HW	Follow Green CLK FAE suggestion	1. Change UG1.2(+3VLP) & UG1.8(+3VALW) connect to +LAN_IO 2. Add R787 connect from +RTCBATT to C5.2 & UG1.10 3. Change C14 from 0.1u to 5p/0402 4. Change C8 connect from +3V_ALW to +LAN_IO 5. Add R788 0ohm/0402 from +RTCVCC to UG1 for GCLK & DH1 select	0.3
36	35	MOAT	2012/07/09	ESD	For ESD request reserve CAP.	Reserve those CAP for ESD MOAT.	0.3
37	18	LVDS	2012/07/10	HW	Change RES and reserve CAP for LVDS issue	Change RH185 from 0ohm-short to 0ohm/0805, and reserve CH106 1U/0402	0.3
38	41	Connector	2012/07/10	ME	For ME request	Change JBTB1 footprint from SP02000G800 (OLD) to SP02000MJ00	0.3
39	13	PCH	2012/07/11	ESD	Follow ESD team request	Add RH44,RH48,RH70 & NET PCH_JTAG_TMS_R, PCH_JTAG_TDI_R, PCH_JTAG_TDO_R for break signal trace	0.3
40	40	PCH	2012/07/11	ESD	Follow ESD team request	1. Change NET NAME "N59110727" to "WL_BT_LED#_R" 2. Reserve 0.1u/0402 on "WL_BT_LED#_R" for ESD	0.3
41	21	LVDS	2012/07/11	HW	Reserve for CE function for LVDS connector	Change CE_EN_R from dummy to JLVDS.18	0.3

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Title: HW-PIR

Size | Document Number: LA-9101P | Rev: 0.4

Date: Wednesday, August 29, 2012 | Sheet 43 of 57

Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40	32	Connector	2012/07/12	ME	For ME request	Change JLAN CPN from "DC234004V00" to "SP011207090"	0.3
41	40	FAN	2012/07/16	HW	For FAN_SPEED1 noise issue	Change CE29 from "@" to POP	0.3
42	14	Touch PAD	2012/07/17	SED	Change Touch PAD SMBUS port for SMBUS issue	Change Touch PAD SMBUS port for SMB0 to SMB	0.4
43	32	GREEN CLK	2012/07/19	HW	Follow Silego FAE request	Change RL21 from 510 ohm to 0 ohm/0402	0.4
44	41	Touch Screen	2012/08/07	SED	Follow SED team request change JTOUCH USB signal conatct.	Change JTOUCH Pin define.	0.4
45	34	Card Reader	2012/08/14	ESD	Follow ESD team request	Reserve CR11 100p/0402 close to JREAD	0.4
46	23	GREEN CLK	2012/08/16	HW	Fixed GCLK output abnormal issue	Change UG1.2(UG1/VDD) from +LAN_IO to+3VALW	0.4
47	33	CODEC	2012/08/16	HW	The issue already fixed by new CODEC.	Remove delay circuit and POP RA4	0.4
48	23	GREEN CLK	2012/08/17	HW	For RTC discharge issue	De-pop R788	0.4
49	32,34	LAN	2012/08/17	HW	For LAN Chip abnormal leakage issue	Pop RL34 and de-pop RE21	0.4
50	34	Card Reader	2012/08/20	ESD	Follow ESD team request	Change CR11 from 100p/0402 to 10p/0402 and POP	0.4
51	41	Touch Screen	2012/08/20	SED	Follow SED team request	Change Touch screen power rail for +3VS to +5VS	0.4
52	38	LED	2012/08/20	HW	Change LED light	Change LED1,LED2,LED4 CPN from SC500006O00 to SC50000DC00	0.4
53	38	WLAN	2012/08/20	HW	Remove AOAC function power control	Change R18,R19,R20,R21,C13,Q2,Q4 component BOM structure to "@"	0.4
54	41	Touch Screen	2012/08/20	HW	Add EC control for Touch Screen function	Add RN15 & QN6 and relative circuit connect	0.4

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Title: HW-PIR

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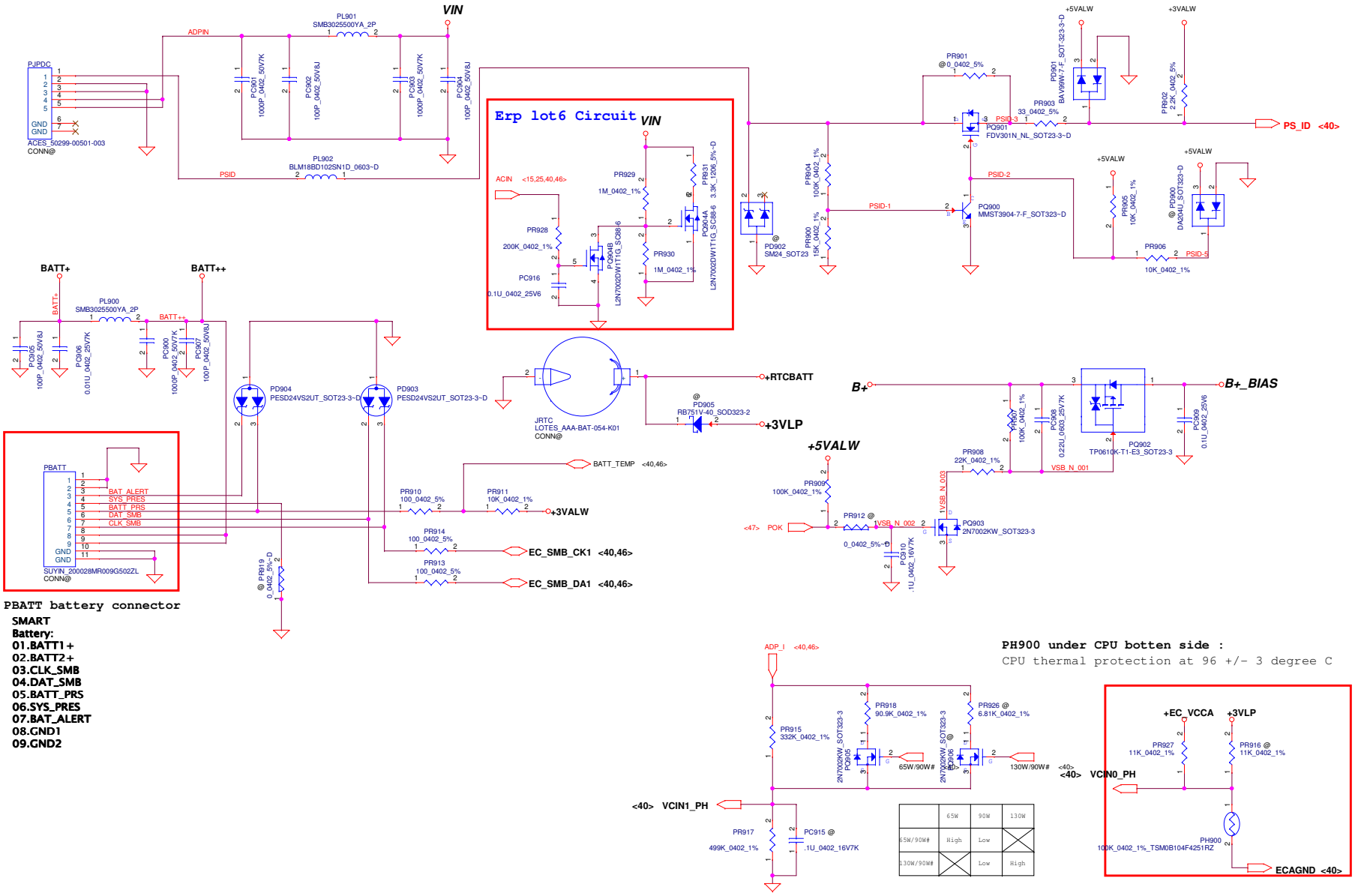

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/07/31

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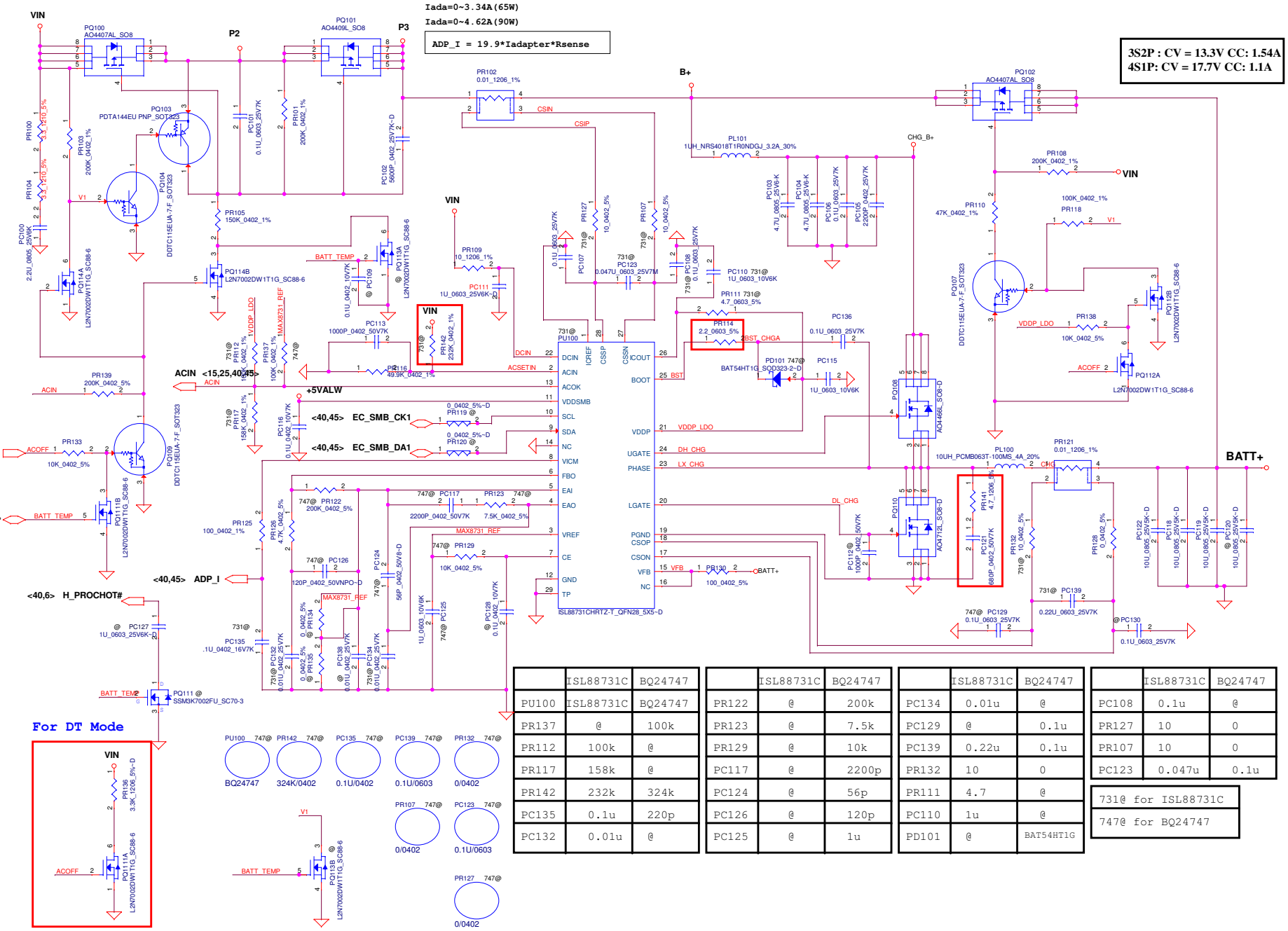
Compal Electronics, Inc.

Title: PWR_DCIN/BATT CONN/OTP

Size: | Document Number: LA-9101P | Rev: 0.4

Date: Wednesday, August 29, 2012 | Sheet 45 of 57



	ISL88731C	BQ24747
PU100	ISL88731C	BQ24747
PR137	@	100k
PR112	100k	@
PR117	158k	@
PR142	232k	324k
PC135	0.1u	220p
PC132	0.01u	@

	ISL88731C	BQ24747
PR122	@	200k
PR123	@	7.5k
PR129	@	10k
PC117	@	2200p
PC124	@	56p
PC126	@	120p
PC125	@	1u

	ISL88731C	BQ24747
PC134	0.01u	@
PC129	@	0.1u
PC139	0.22u	0.1u
PR132	10	0
PR111	4.7	@
PC110	1u	@
PD101	@	BAT54HT1G

	ISL88731C	BQ24747
PC108	0.1u	@
PR127	10	0
PR107	10	0
PC123	0.047u	0.1u

731@ for ISL88731C
747@ for BQ24747

PU100 747@	PR142 747@	PC135 747@
BQ24747	324K/0402	0.1U/0402
PC139 747@	PR132 747@	PR107 747@
0.1U/0603	0/0402	0/0402
PC123 747@	PR127 747@	
0.1U/0603	0/0402	

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/07/31

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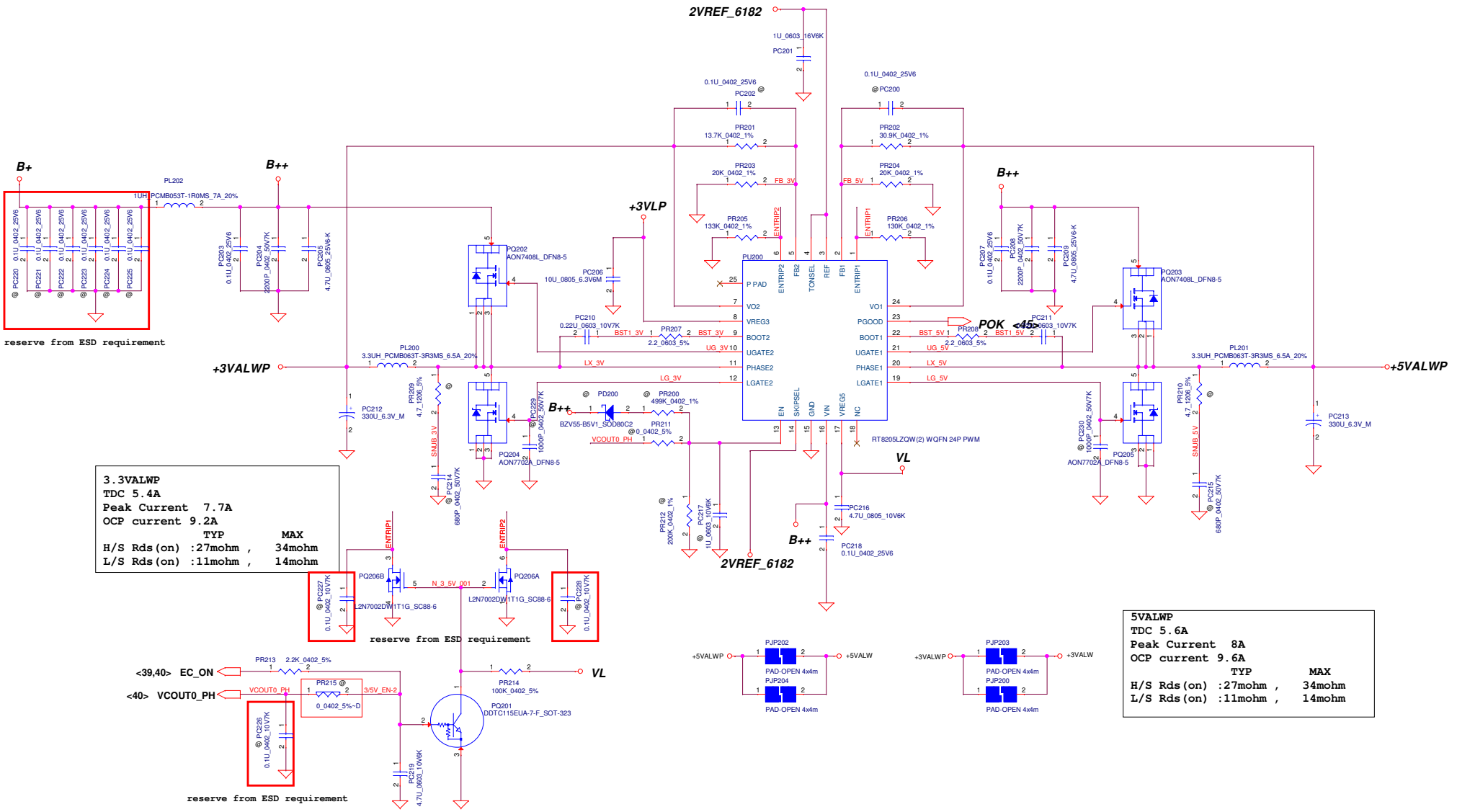
Compal Electronics, Inc.

Title: **PWR_CHARGER**

Size	Document Number	Rev
	LA-9101P	0.4

Date: Wednesday, August 29, 2012 Sheet 46 of 57



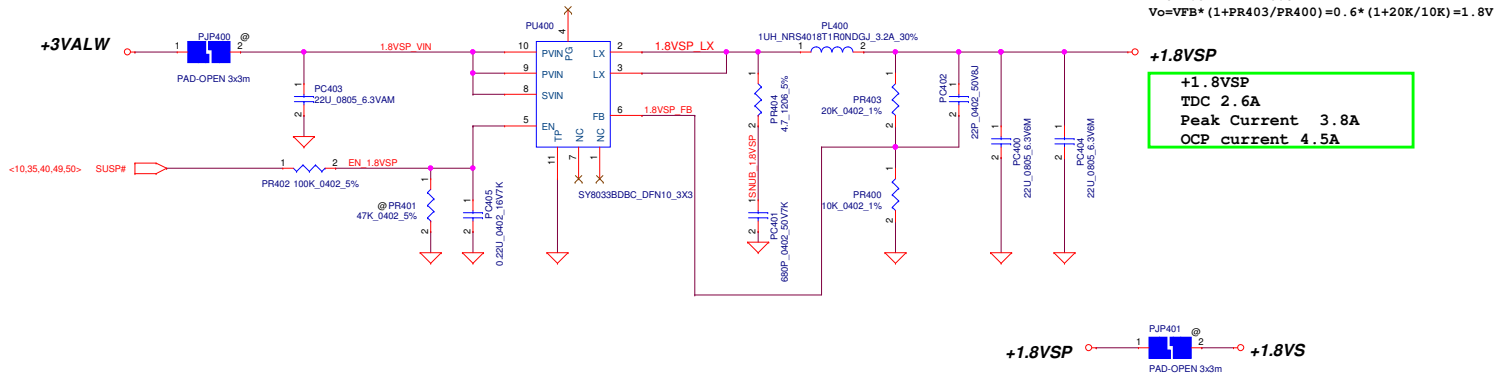
Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/07/31

Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

Size | Document Number: LA-9101P | Rev: 0.4

Date: Wednesday, August 29, 2012 | Sheet 47 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/07/31

Compal Electronics, Inc.			
Title: PWR_1.8VSP			
Size:	Document Number: LA-9101P		Rev: 0.4
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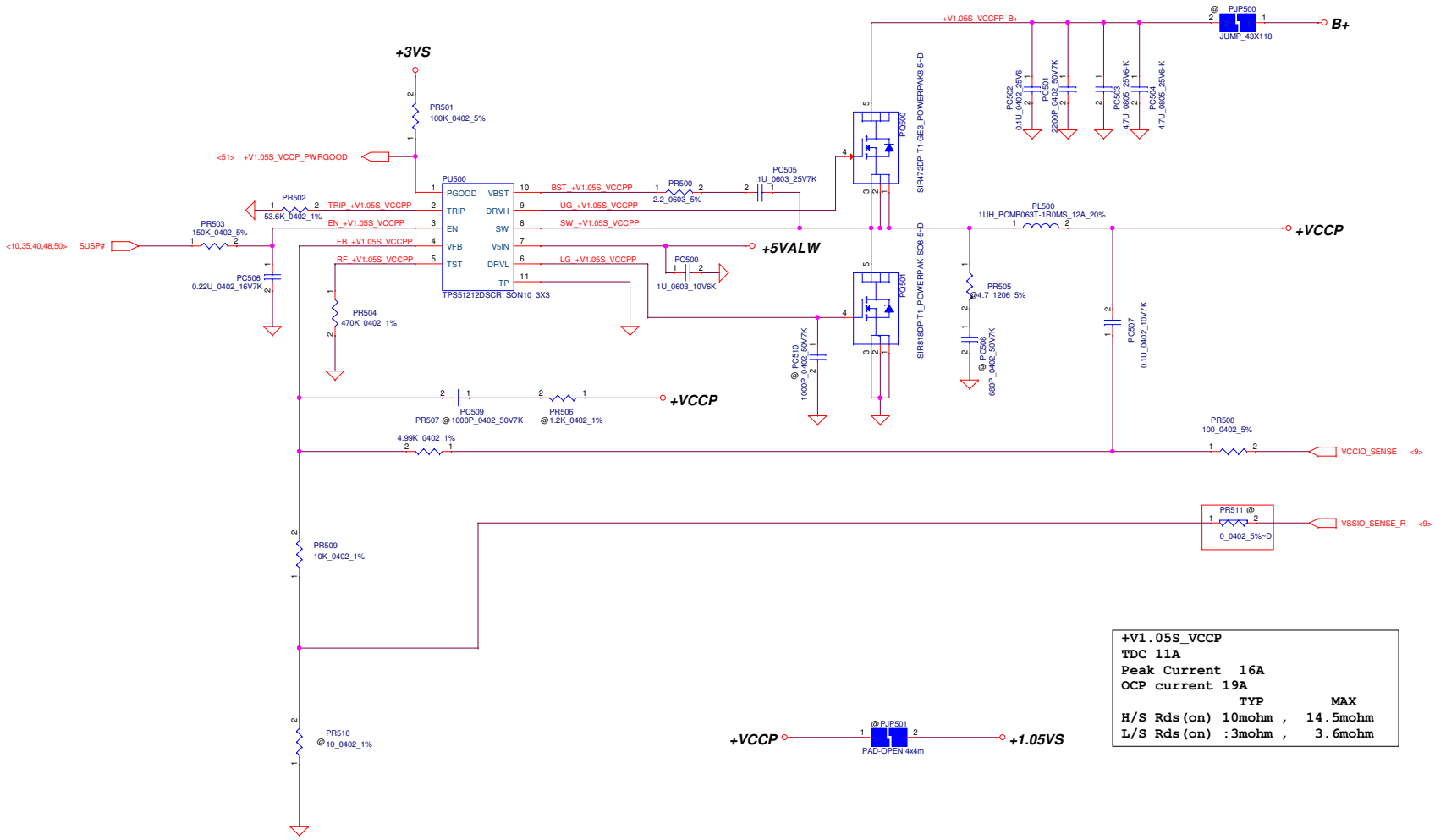

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/07/31

Compal Electronics, Inc.

Title: PWR_+VCCIO

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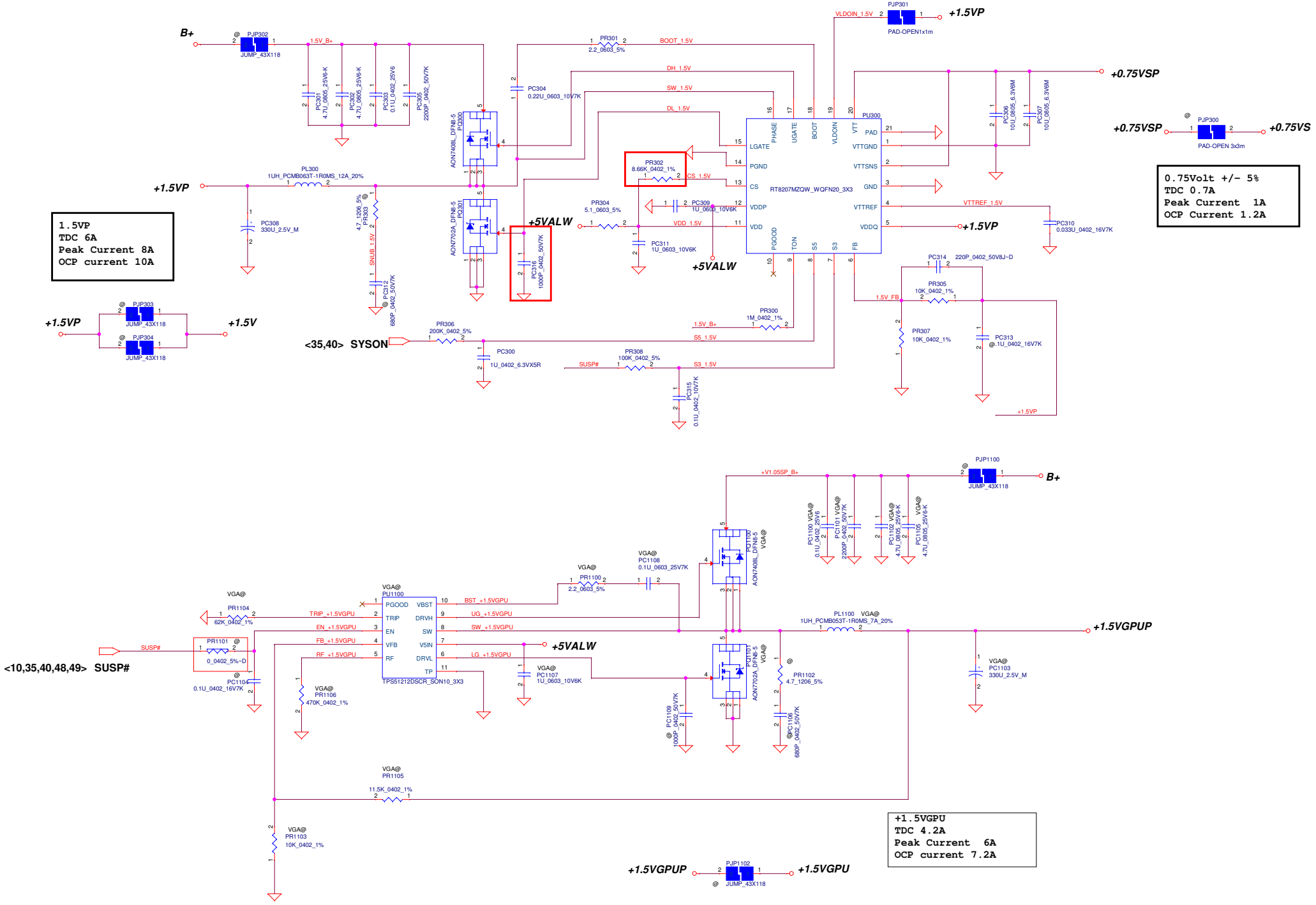

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/07/31

Compal Electronics, Inc.

Title: PWR_+1.5VP/+1.5VGPUP/0.75VSP

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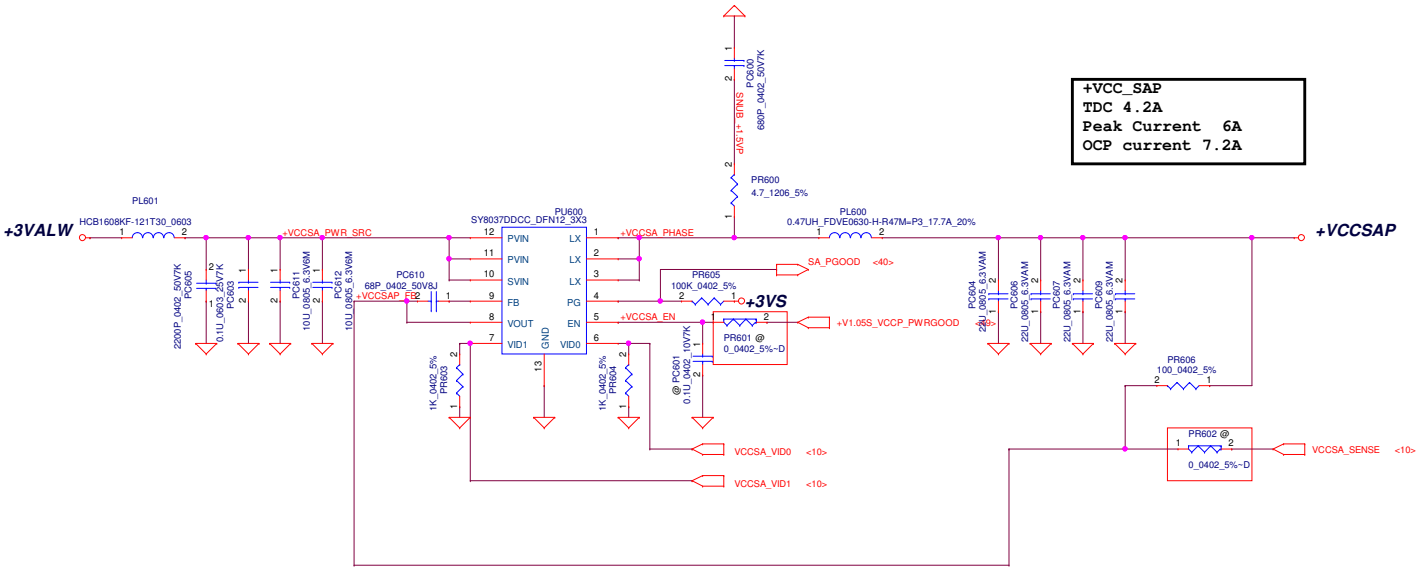
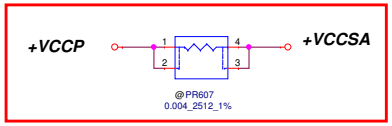
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A



The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



reserve for Pentium and Celeron only

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/07/31

Compal Electronics, Inc.

Title: PWR_+VCCSAP

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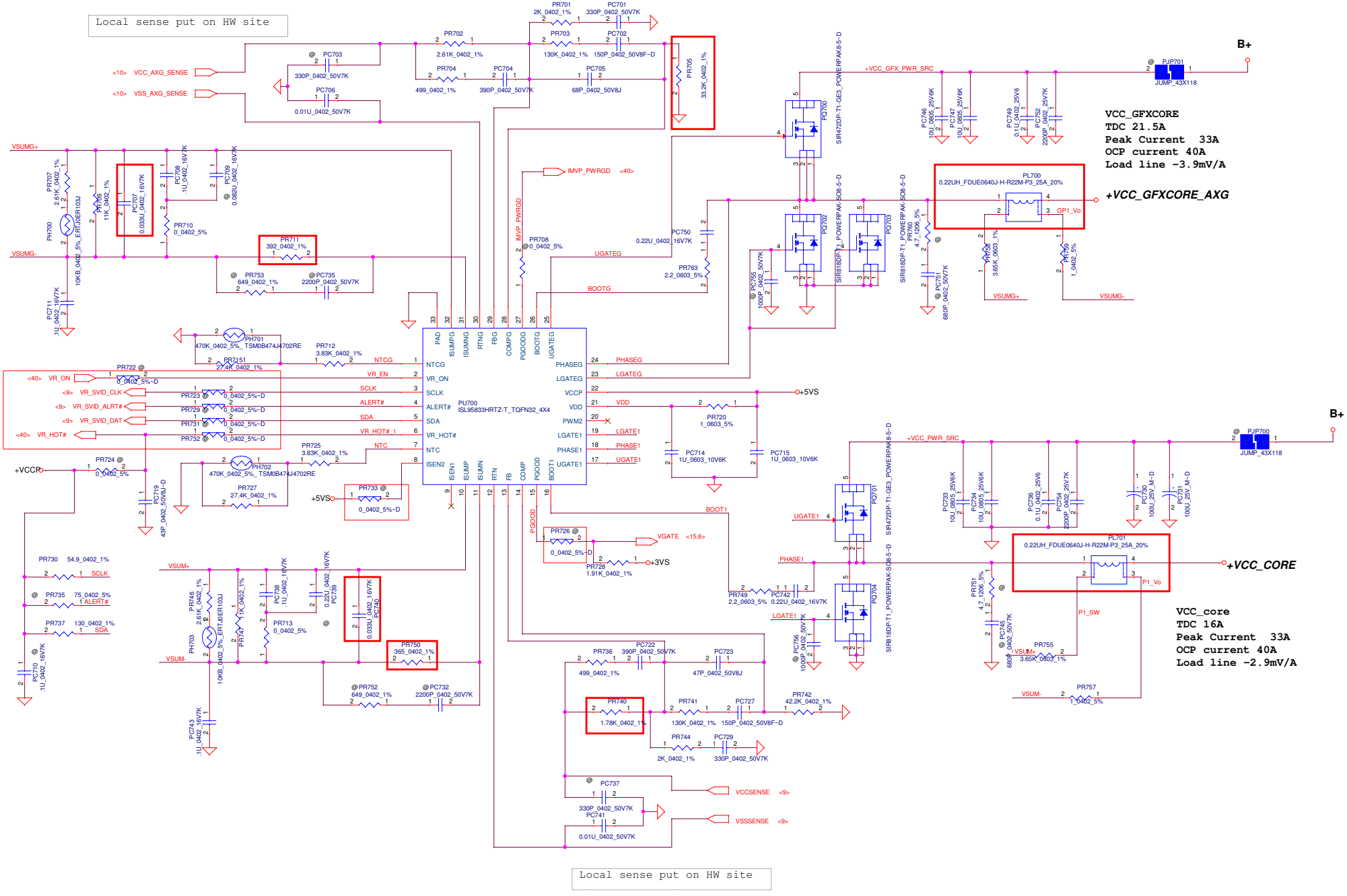

Security Classification	Compal Secret Data			
Issued Date	2012/08/22	Deciphered Date	2013/07/31	

Compal Electronics, Inc.	
Title	PWR_VCORE
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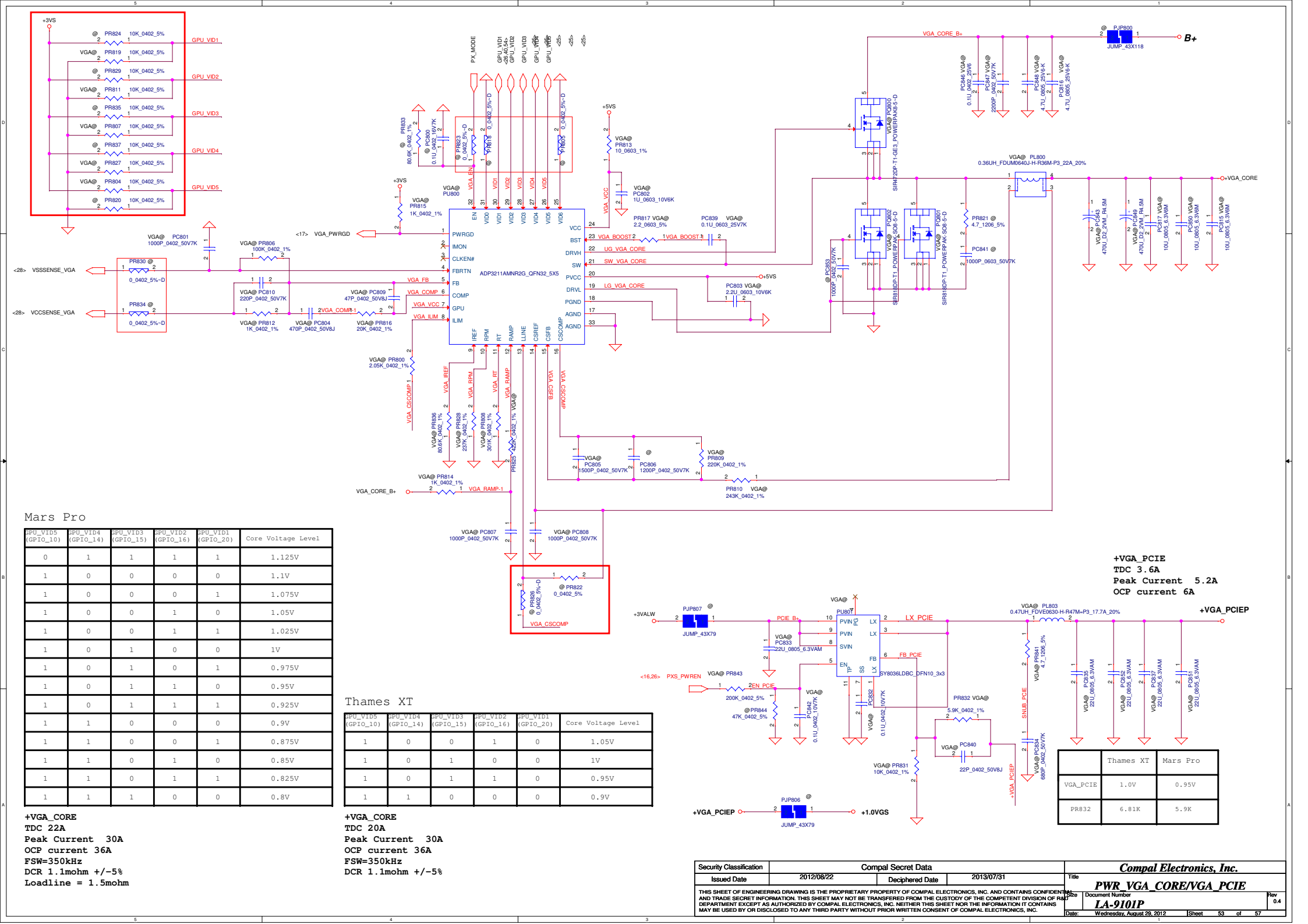

Mars Pro

GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V

+VGA_CORE
TDC 22A
Peak Current 30A
OCP current 36A
FSW=350kHz
DCR 1.1mohm +/-5%
Loadline = 1.5mohm

Thames XT

GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
1	0	0	1	0	1.05V
1	0	1	0	0	1V
1	0	1	1	0	0.95V
1	1	0	0	0	0.9V

+VGA_CORE
TDC 20A
Peak Current 30A
OCP current 36A
FSW=350kHz
DCR 1.1mohm +/-5%

+VGA_PCIE
TDC 3.6A
Peak Current 5.2A
OCP current 6A

	Thames XT	Mars Pro
VGA_PCIE	1.0V	0.95V
PR832	6.81K	5.9K

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/07/31

Compal Electronics, Inc.

Title: **PWR_VGA_CORE/VGA_PCIE**

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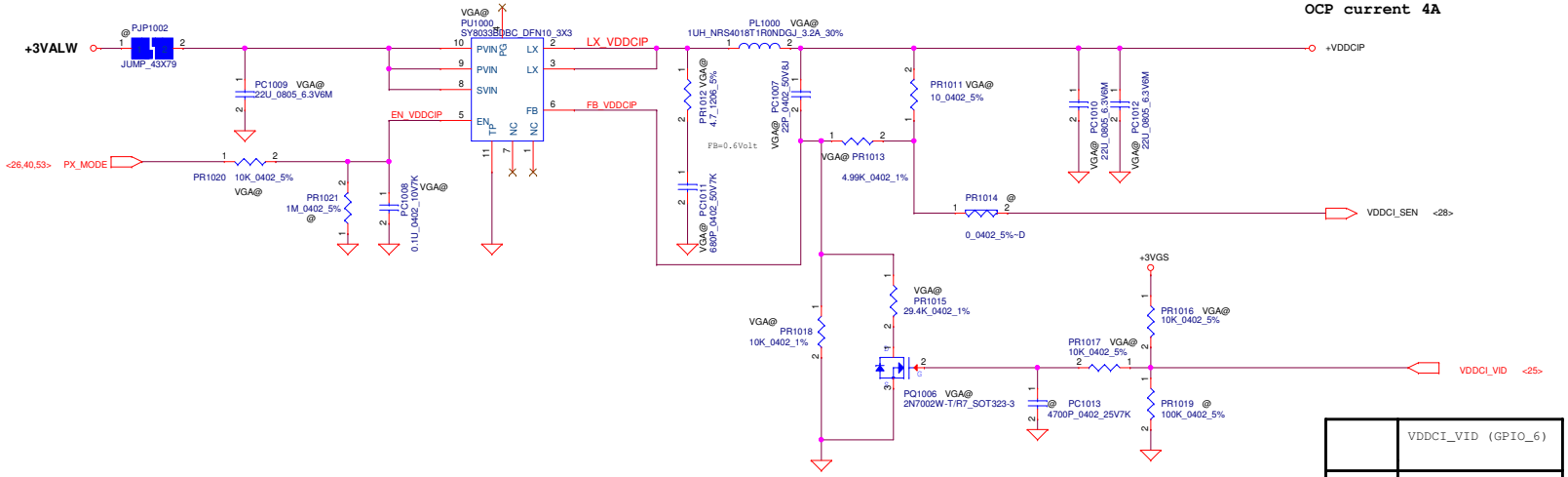
Date: Wednesday, August 29, 2012 | Sheet 53 of 57

+VDDCI
TDC 2.2A
Peak Current 2.2A
OCP current 4A



	VDDCI_VID (GPIO_6)
High	1V
Low	0.9V

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/07/31

Compal Electronics, Inc.	
Title	PWR_+VDDCIP
Size	Document Number: LA-9101P
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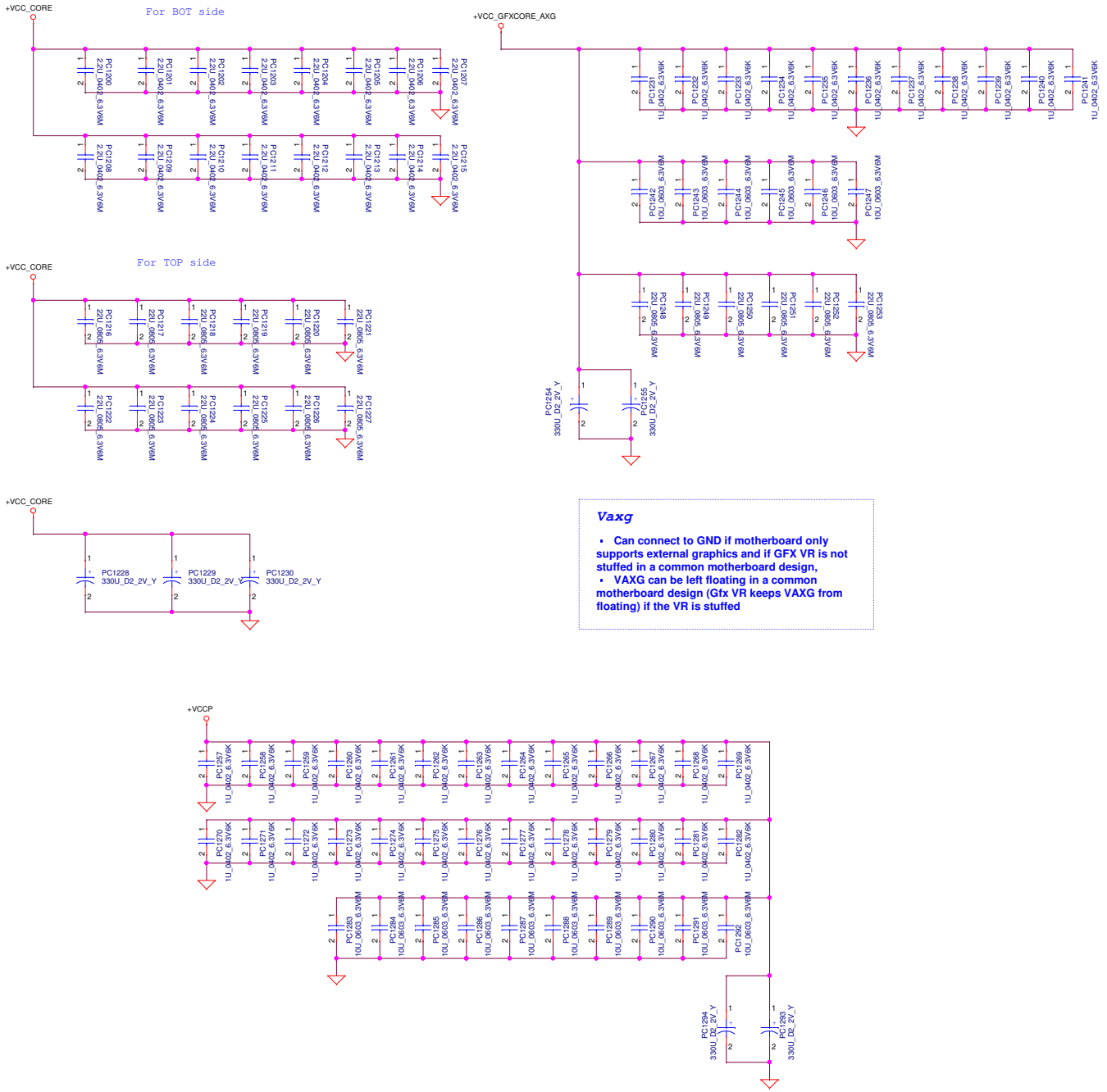

Vaxg

- **Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,**
- **VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed**

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/07/31

Compal Electronics, Inc.

Title: **PWR_PROCESSOR DECOUPLING**

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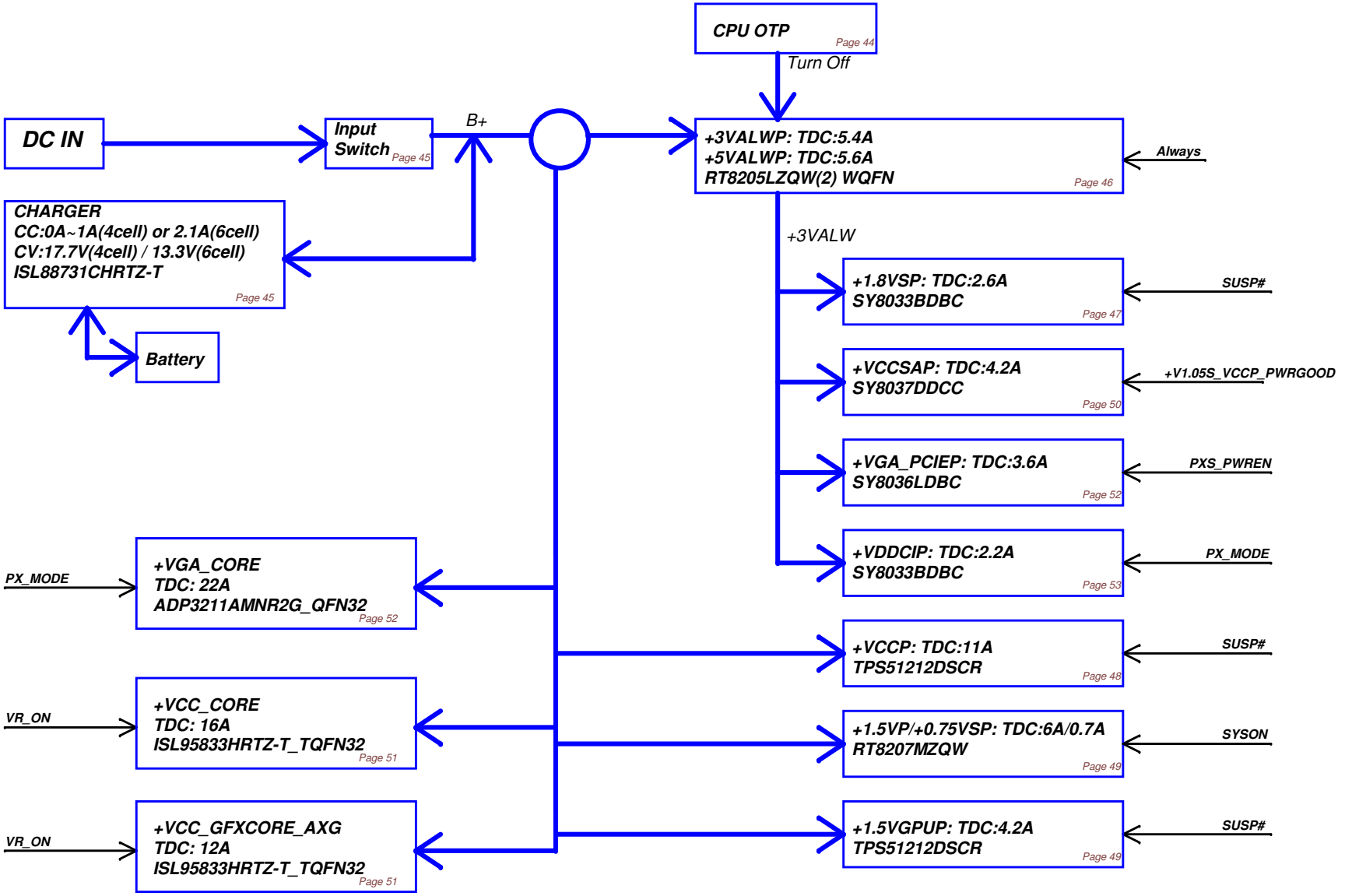
Power block



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/07/31

Compal Electronics, Inc.		
Title: PWR_POWER BLOCK DIAGRAM		
Size	Document Number: LA-9101P	Rev: 0.4
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	51	VCORE	12/05/11	Morris	adjust VR parameter	change PL700 and PL701 from 0.36u to 0.22u change PC707 and PC740 from 0.047u to 0.033u change PR750 from 649 to 365 change PR711 from 649 to 392 change PR740 from 1.91k to 1.78k change PR705 from 150k to 33.2k	X00
2	44 45 46	DCIN/BATT CONN/OTP CHARGER 3.3VALWP/5VALWP	12/05/11	Morris	follow SSI memo for part shortage issue	change PQ112,PQ114,PQ1111,PQ206,PQ904 from SB00000CQ00 to SB00000PV00	X00
3	49	+1.5VP/1.5VDGPU/0.75VSP	12/05/15	Morris	design change	change PR302 from 12k to 8.66k	X00
4	50	+VCCSAP	12/05/23	Morris	for Pentium and Celeron special BOM	add PR607 and reserve	X00
5	49	+1.5VP/1.5VDGPU/0.75VSP	12/07/06	Morris	design change to reduce low-side mosfet induce	add PC316 1000pf	X01
6	45	CHARGER	12/07/17	Morris	from EMI request	change PR114 from 0 to 2.2 add PR141 and PC121	X01
7	45	CHARGER	12/07/17	Morris	design change to solve Battery LED is still on after unplug AC when SUT in S3S4S5 issue	change PR142 from 210k to 232k for ISL88731C (X76) change PR142 from 309k to 324k for BQ24747 (X76)	X01
8	44	DCIN/BATT CONN/OTP	12/07/17	Morris	revise OTP setting to 96C from thermal request	change PR927 from 12.1k to 11k	X01

Compal Electronics, Inc.

Title: PWR-PIR

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Date: Wednesday, August 29, 2012 | Sheet 57 of 57