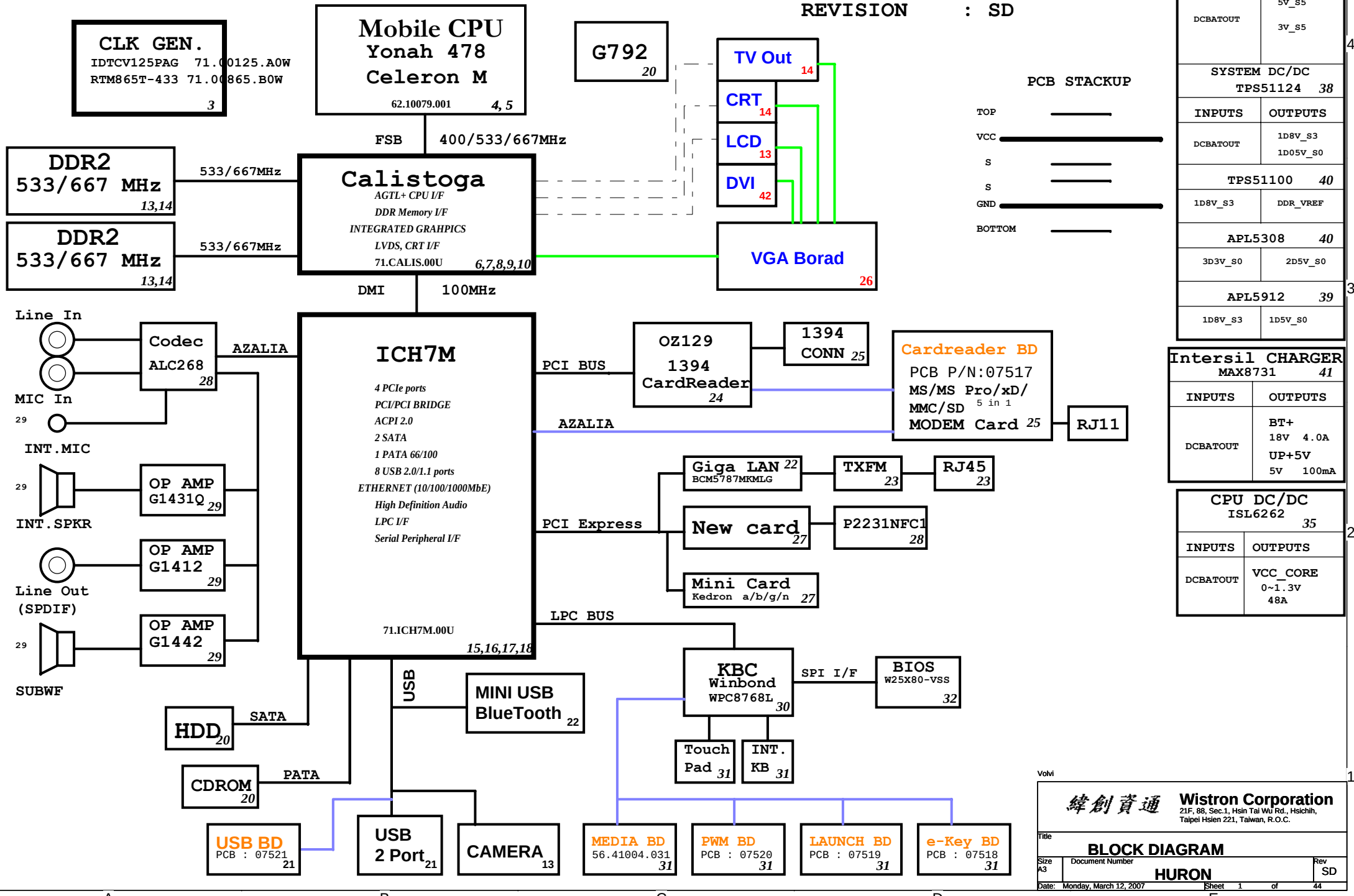


Huron Block Diagram



A

B

ICH7M Integrated Pull-up
and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN,EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT,ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS,SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

3

ICH7M IDE Integrated Series
Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPI025	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSusi_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSusi_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

C

RTM865T-433 100Mhz/LCDCLK Spread
and Frequency Selection Table

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	0.8% Down
0	0	0	1	1.0% Down
0	0	1	0	1.25% Down
0	0	1	1	1.50% Down
0	1	0	0	1.75% Down
0	1	0	1	2.0% Down
0	1	1	0	2.5% Down
0	1	1	1	3.0% Down
1	0	0	0	+0.3% Center
1	0	0	1	+0.4% Center
1	0	1	0	+0.5% Center
1	0	1	1	+0.6% Center
1	1	0	0	+0.8% Center
1	1	0	1	+1.0% Center
1	1	1	0	+1.25% Center
1	1	1	1	+1.5% Center

PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
OZ129TZ	AD22	A-G	REQ0# ->REQ0#

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	MINICARD
5	BlueTooth
6	CCD
7	NewCard

D

E

Calistoga Strapping Signals and
Configuration

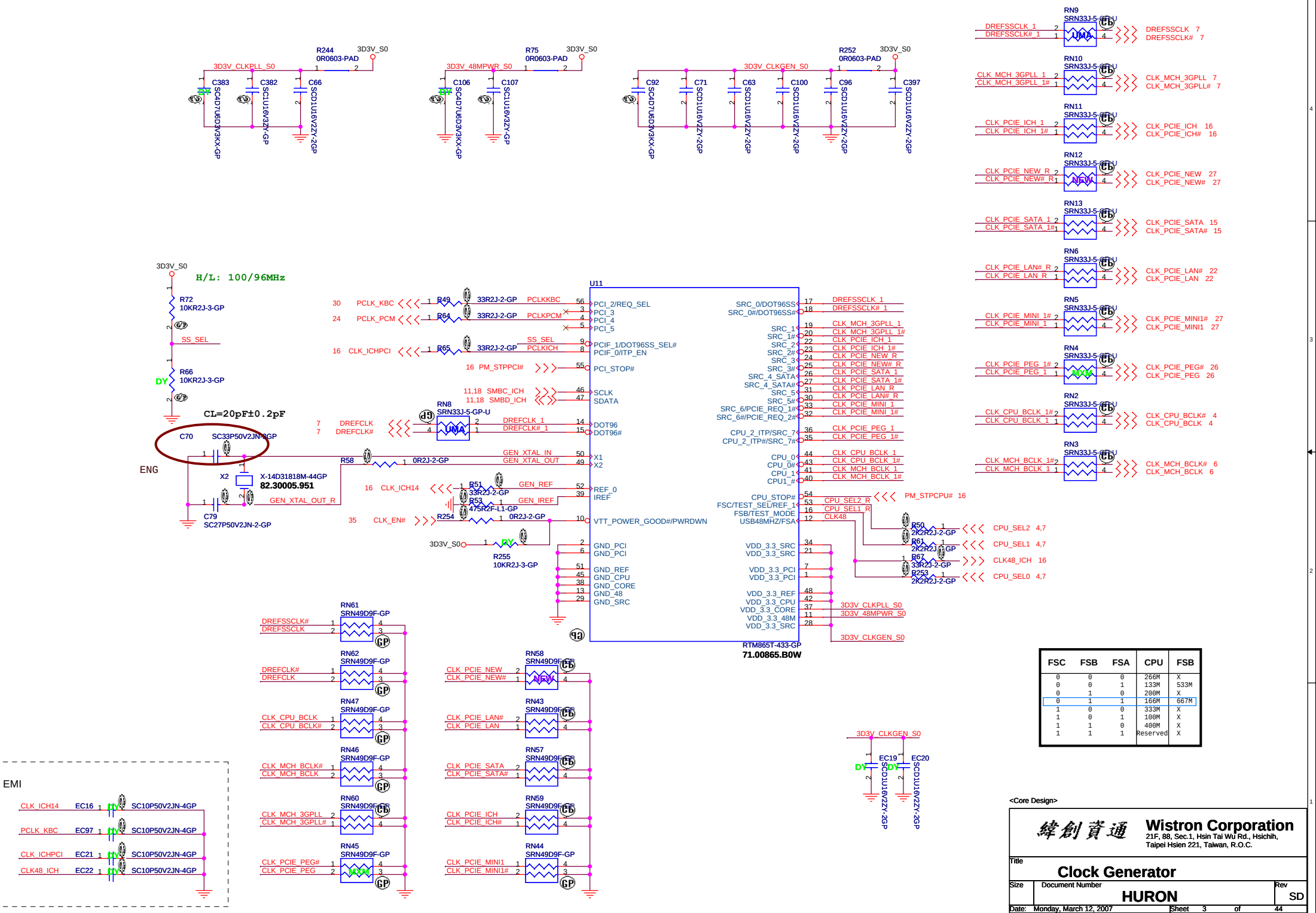
EDS 17050 0.71 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is supported 1 =SDVO and PCIE x1 operating simultaneously via the PEG port
SDV0CTRL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading
edge of the Calistoga GMCH PWORK in signal.

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Reference					
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	HURON				SD
Date:	Monday, March 12, 2007		Sheet	2	of 44



FSC	FSB	FSA	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	266M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X

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Title

Clock Generator

Size

Document Number

Date

Monday, March 12, 2007

Sheet

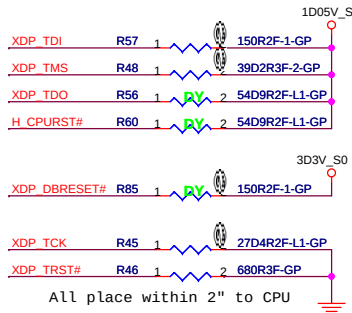
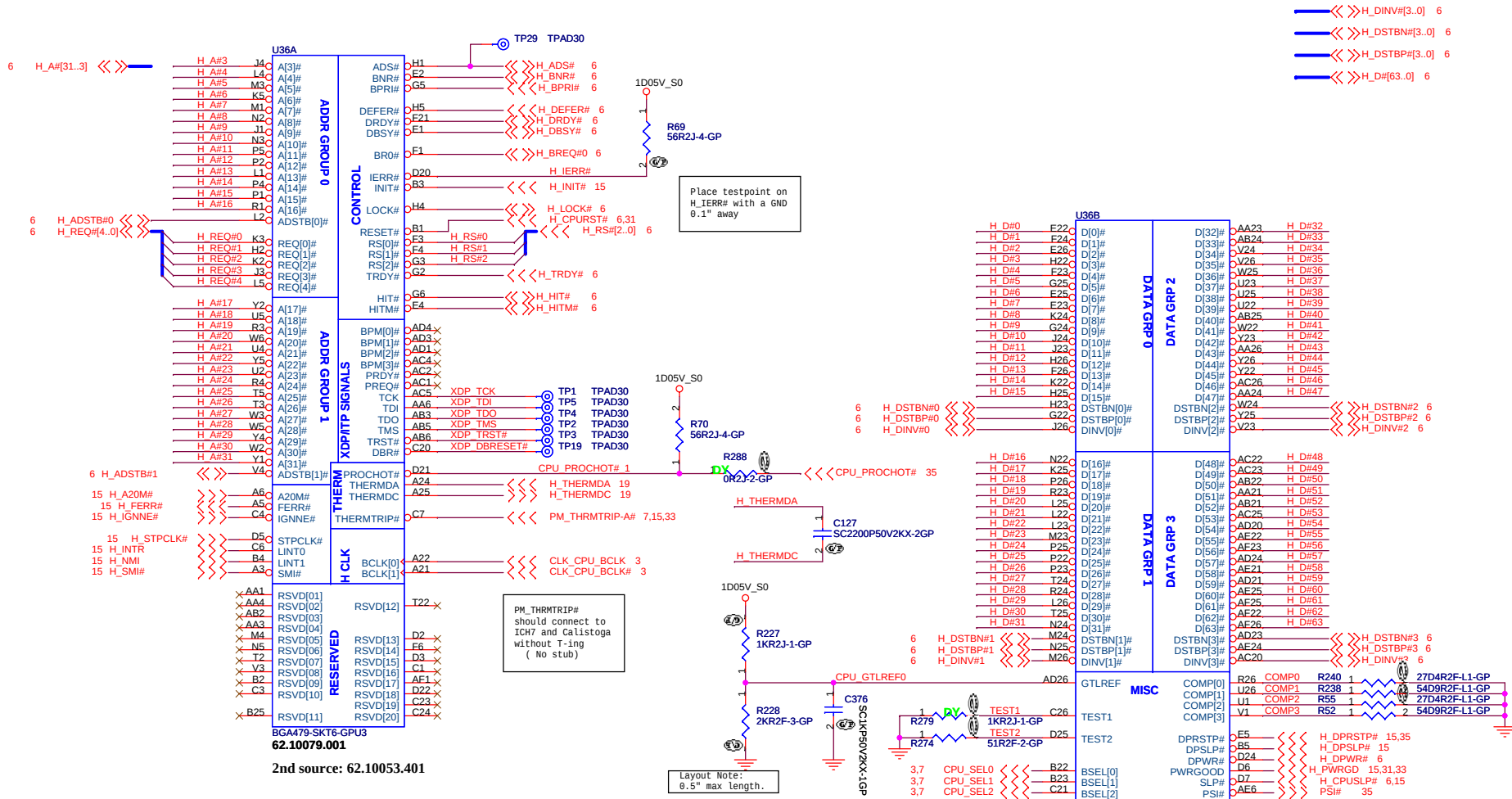
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SD

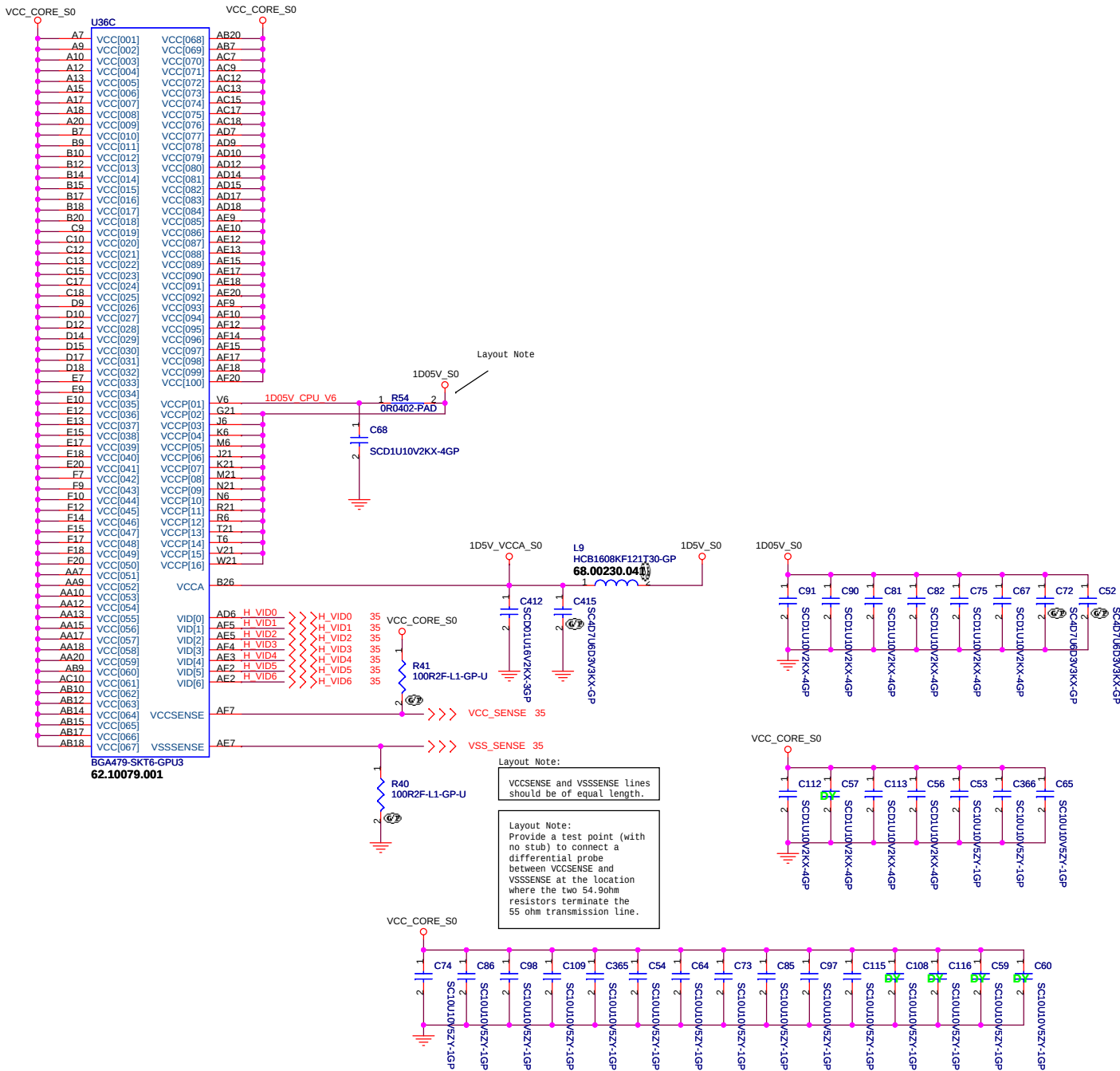


All place within 2" to CPU

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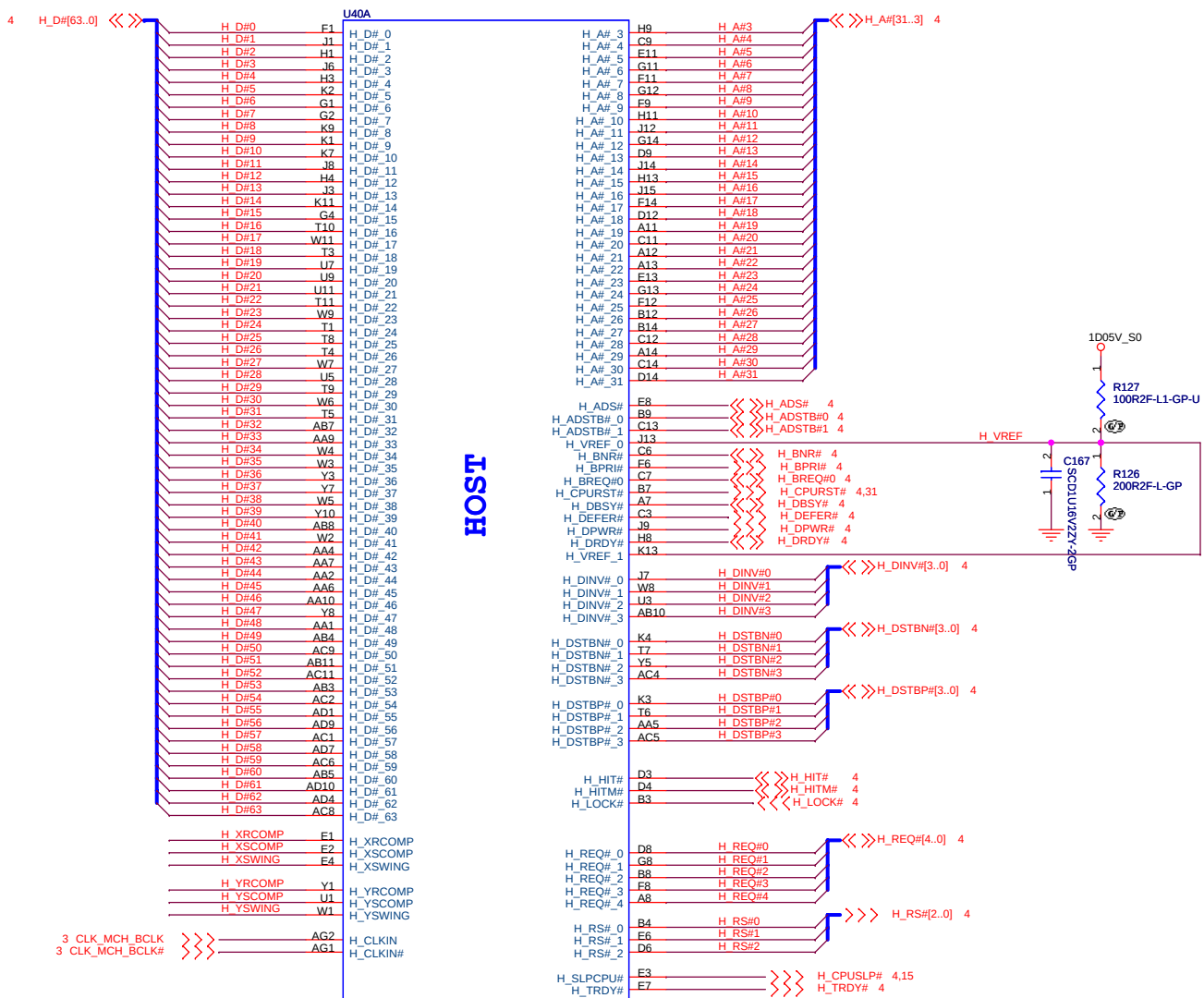
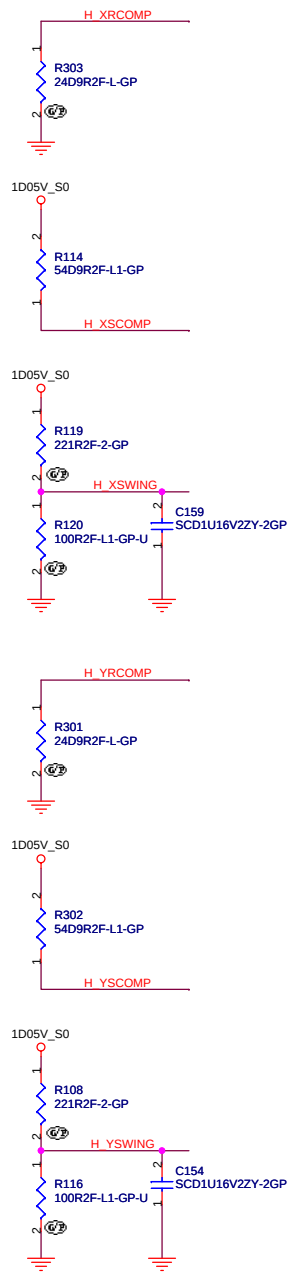
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Size		Document Number						S	
				HURON					
Date: Monday, March 12, 2007				Sheet 4		of 44			



U36D		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A26	VSS[007]	VSS[088]
B6	VSS[008]	VSS[089]
B8	VSS[009]	VSS[090]
B11	VSS[010]	VSS[091]
B13	VSS[011]	VSS[092]
B16	VSS[012]	VSS[093]
B19	VSS[013]	VSS[094]
B21	VSS[014]	VSS[095]
B24	VSS[015]	VSS[096]
C5	VSS[016]	VSS[097]
C8	VSS[017]	VSS[098]
C11	VSS[018]	VSS[099]
C14	VSS[019]	VSS[100]
C16	VSS[020]	VSS[101]
C19	VSS[021]	VSS[102]
C22	VSS[022]	VSS[103]
C25	VSS[023]	VSS[104]
C28	VSS[024]	VSS[105]
D1	VSS[025]	VSS[106]
D4	VSS[026]	VSS[107]
D8	VSS[027]	VSS[108]
D11	VSS[028]	VSS[109]
D13	VSS[029]	VSS[110]
D16	VSS[030]	VSS[111]
D19	VSS[031]	VSS[112]
D23	VSS[032]	VSS[113]
D26	VSS[033]	VSS[114]
E3	VSS[034]	VSS[115]
E6	VSS[035]	VSS[116]
E8	VSS[036]	VSS[117]
E11	VSS[037]	VSS[118]
E14	VSS[038]	VSS[119]
E16	VSS[039]	VSS[120]
E19	VSS[040]	VSS[121]
E21	VSS[041]	VSS[122]
E24	VSS[042]	VSS[123]
F5	VSS[043]	VSS[124]
F8	VSS[044]	VSS[125]
F11	VSS[045]	VSS[126]
F13	VSS[046]	VSS[127]
F16	VSS[047]	VSS[128]
F19	VSS[048]	VSS[129]
F22	VSS[049]	VSS[130]
F25	VSS[050]	VSS[131]
G4	VSS[051]	VSS[132]
G1	VSS[052]	VSS[133]
G1	VSS[053]	VSS[134]
G23	VSS[054]	VSS[135]
G26	VSS[055]	VSS[136]
H3	VSS[056]	VSS[137]
H6	VSS[057]	VSS[138]
H21	VSS[058]	VSS[139]
H24	VSS[059]	VSS[140]
J2	VSS[060]	VSS[141]
J5	VSS[061]	VSS[142]
J22	VSS[062]	VSS[143]
J25	VSS[063]	VSS[144]
K1	VSS[064]	VSS[145]
K4	VSS[065]	VSS[146]
K23	VSS[066]	VSS[147]
K26	VSS[067]	VSS[148]
L3	VSS[068]	VSS[149]
L6	VSS[069]	VSS[150]
L1	VSS[070]	VSS[151]
L21	VSS[071]	VSS[152]
L24	VSS[072]	VSS[153]
M2	VSS[073]	VSS[154]
M5	VSS[074]	VSS[155]
M22	VSS[075]	VSS[156]
M25	VSS[076]	VSS[157]
N1	VSS[077]	VSS[158]
N4	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
P3	VSS[081]	VSS[162]

BGA479-SKT6-GPU3
62.10079.001



71.CALIS.00U

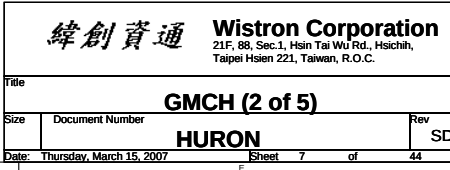
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UMA : 945GM P/N is KI.94501.005

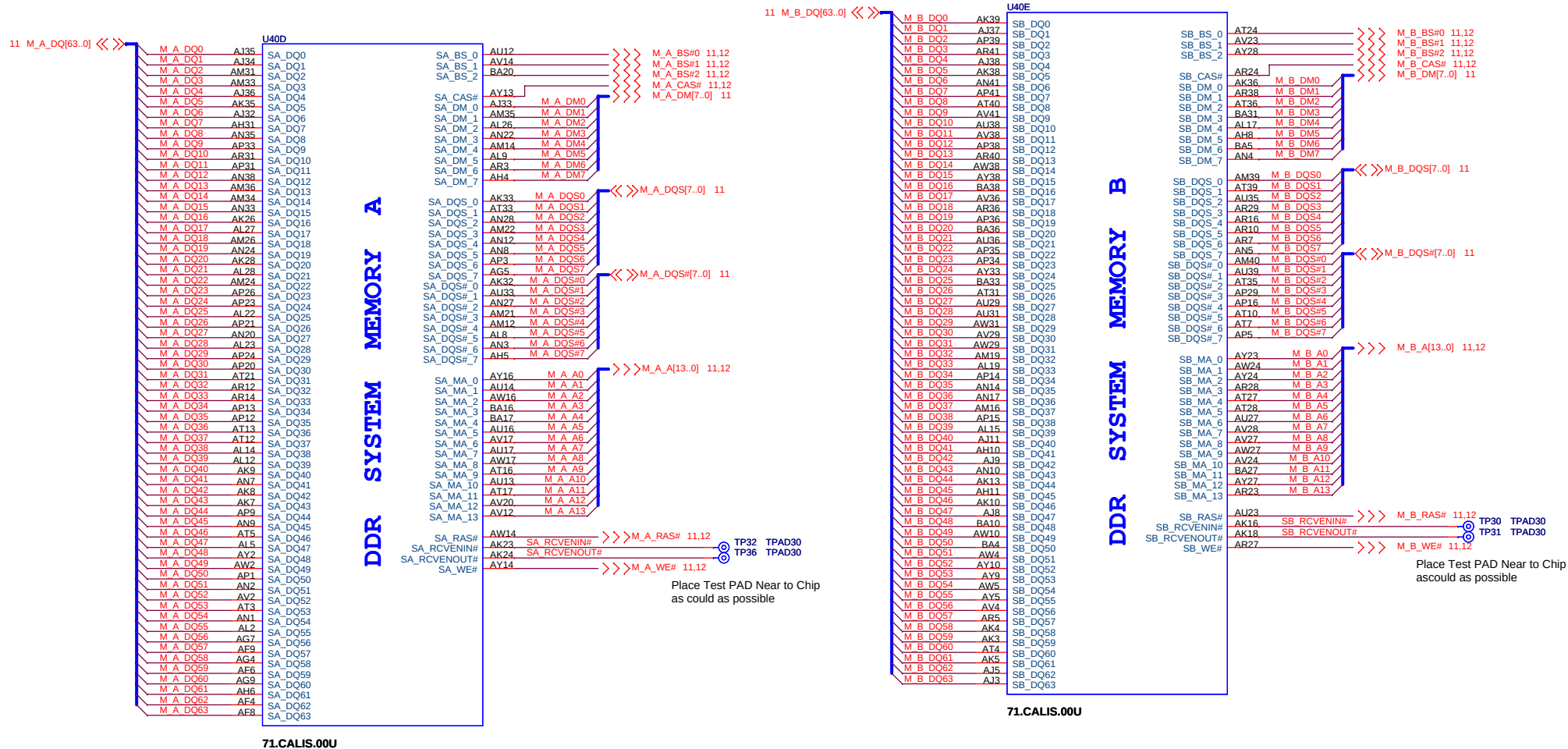
Place them near to the chip (< 0.5")

<Core Design>

Title		GMCH (1 of 5)	
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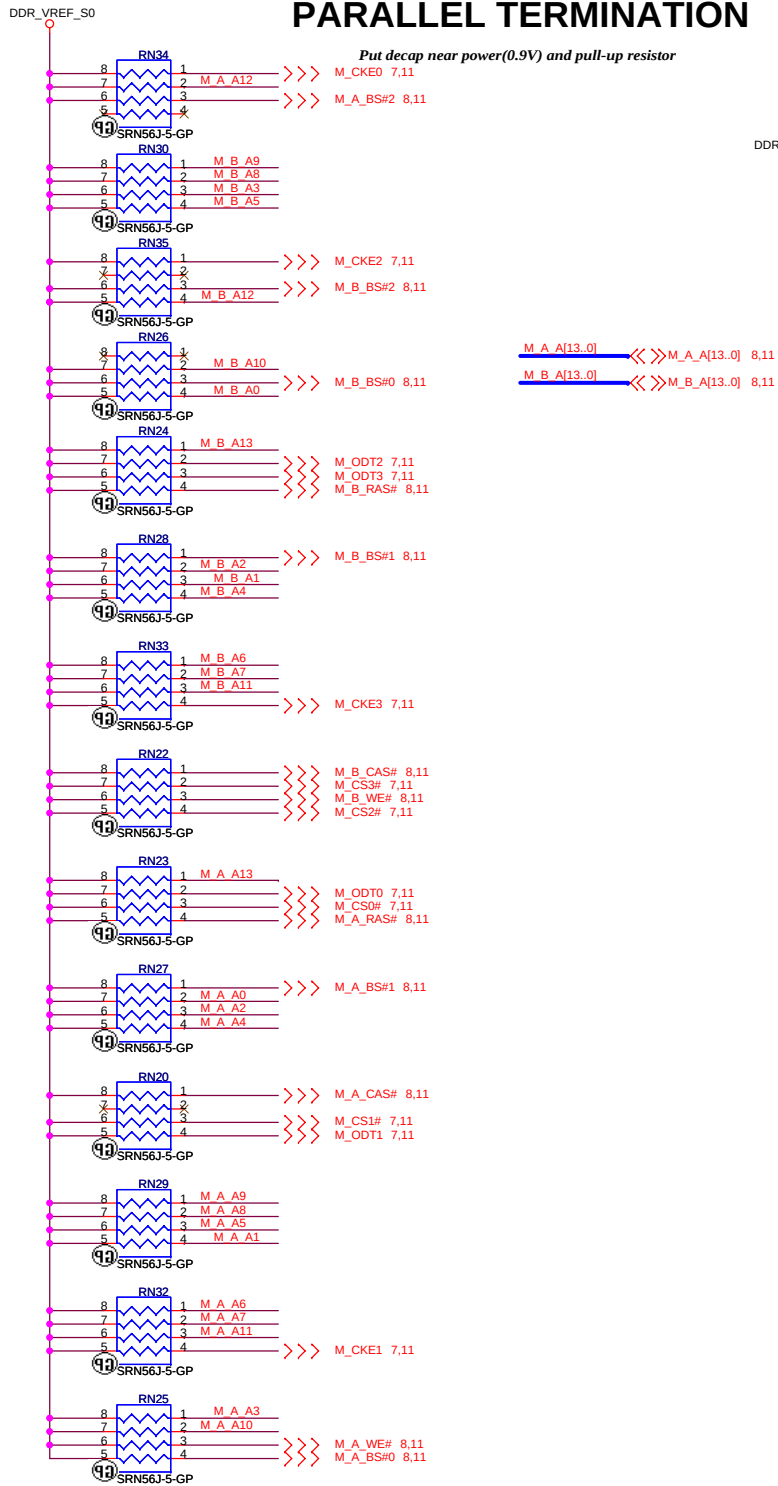
1D05V_S0	AA33	VCC_0	U40G
	W33	VCC_1	
	P33	VCC_2	
	N33	VCC_3	
	L33	VCC_4	
	J33	VCC_5	
	AA32	VCC_6	
	V32	VCC_7	
	W32	VCC_8	
	P32	VCC_9	
	N32	VCC_10	
	L32	VCC_11	
	J32	VCC_12	
	AA31	VCC_13	
	W31	VCC_14	
	P31	VCC_15	
	N31	VCC_16	
	L31	VCC_17	
	J31	VCC_18	
	AA30	VCC_19	
	W30	VCC_20	
	P30	VCC_21	
	N30	VCC_22	
	L30	VCC_23	
	J30	VCC_24	
	AA29	VCC_25	
	W29	VCC_26	
	P29	VCC_27	
	N29	VCC_28	
	L29	VCC_29	
	J29	VCC_30	
	AA28	VCC_31	
	W28	VCC_32	
	P28	VCC_33	
	N28	VCC_34	
	L28	VCC_35	
	J28	VCC_36	
	AA27	VCC_37	
	W27	VCC_38	
	P27	VCC_39	
	N27	VCC_40	
	L27	VCC_41	
	J27	VCC_42	
	AA26	VCC_43	
	W26	VCC_44	
	P26	VCC_45	
	N26	VCC_46	
	L26	VCC_47	
	J26	VCC_48	
	AA25	VCC_49	
	W25	VCC_50	
	P25	VCC_51	
	N25	VCC_52	
	L25	VCC_53	
	J25	VCC_54	
	AA24	VCC_55	
	W24	VCC_56	
	P24	VCC_57	
	N24	VCC_58	
	L24	VCC_59	
	J24	VCC_60	
	AA23	VCC_61	
	W23	VCC_62	
	P23	VCC_63	
	N23	VCC_64	
	L23	VCC_65	
	J23	VCC_66	
	AA22	VCC_67	
	W22	VCC_68	
	P22	VCC_69	
	N22	VCC_70	
	L22	VCC_71	
	J22	VCC_72	
	AA21	VCC_73	
	W21	VCC_74	
	P21	VCC_75	
	N21	VCC_76	
	L21	VCC_77	
	J21	VCC_78	
	AA20	VCC_79	
	W20	VCC_80	
	P20	VCC_81	
	N20	VCC_82	
	L20	VCC_83	
	J20	VCC_84	
	AA19	VCC_85	
	W19	VCC_86	
	P19	VCC_87	
	N19	VCC_88	
	L19	VCC_89	
	J19	VCC_90	
	AA18	VCC_91	
	W18	VCC_92	
	P18	VCC_93	
	N18	VCC_94	
	L18	VCC_95	
	J18	VCC_96	
	AA17	VCC_97	
	W17	VCC_98	
	P17	VCC_99	
	N17	VCC_100	
	L17	VCC_101	
	J17	VCC_102	
	AA16	VCC_103	
	W16	VCC_104	
	P16	VCC_105	
	N16	VCC_106	
	L16	VCC_107	
	J16	VCC_108	
	AA15	VCC_109	
	W15	VCC_110	
	P15	VCC_111	
	N15	VCC_112	
	L15	VCC_113	
	J15	VCC_114	
	AA14	VCC_115	
	W14	VCC_116	
	P14	VCC_117	
	N14	VCC_118	
	L14	VCC_119	
	J14	VCC_120	
	AA13	VCC_121	
	W13	VCC_122	
	P13	VCC_123	
	N13	VCC_124	
	L13	VCC_125	
	J13	VCC_126	
	AA12	VCC_127	
	W12	VCC_128	
	P12	VCC_129	
	N12	VCC_130	
	L12	VCC_131	
	J12	VCC_132	
	AA11	VCC_133	
	W11	VCC_134	
	P11	VCC_135	
	N11	VCC_136	
	L11	VCC_137	
	J11	VCC_138	
	AA10	VCC_139	
	W10	VCC_140	
	P10	VCC_141	
	N10	VCC_142	
	L10	VCC_143	
	J10	VCC_144	
	AA9	VCC_145	
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	P9	VCC_147	
	N9	VCC_148	
	L9	VCC_149	
	J9	VCC_150	
	AA8	VCC_151	
	W8	VCC_152	
	P8	VCC_153	
	N8	VCC_154	
	L8	VCC_155	
	J8	VCC_156	
	AA7	VCC_157	
	W7	VCC_158	
	P7	VCC_159	
	N7	VCC_160	
	L7	VCC_161	
	J7	VCC_162	
	AA6	VCC_163	
	W6	VCC_164	
	P6	VCC_165	
	N6	VCC_166	
	L6	VCC_167	
	J6	VCC_168	
	AA5	VCC_169	
	W5	VCC_170	
	P5	VCC_171	
	N5	VCC_172	
	L5	VCC_173	
	J5	VCC_174	
	AA4	VCC_175	
	W4	VCC_176	
	P4	VCC_177	
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	N0	VCC_220	
	L0	VCC_221	
	J0	VCC_222	
	AA0	VCC_223	
	W0	VCC_224	
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	J0	VCC_270	
	AA0	VCC_271	
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	P0	VCC_273	
	N0	VCC_274	
	L0	VCC_275	
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	P0	VCC_291	
	N0	VCC_292	
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	J0	VCC_294	
	AA0	VCC_295	
	W0	VCC_296	
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	N0	VCC_298	
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	J0	VCC_300	
	AA0	VCC_301	
	W0	VCC_302	
	P0	VCC_303	
	N0	VCC_304	
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	J0	VCC_306	
	AA0	VCC_307	
	W0	VCC_308	
	P0	VCC_309	
	N0	VCC_310	
	L0	VCC_311	
	J0	VCC_312	
	AA0	VCC_313	
	W0	VCC_314	
	P0	VCC_315	
	N0	VCC_316	
	L0	VCC_317	
	J0	VCC_318	
	AA0	VCC_319	
	W0	VCC_320	
	P0	VCC_321	
	N0	VCC_322	
	L0	VCC_323	
	J0	VCC_324	
	AA0	VCC_325	
	W0	VCC_326	
	P0	VCC_327	
	N0	VCC_328	
	L0	VCC_329	
	J0	VCC_330	
	AA0	VCC_331	
	W0	VCC_332	
	P0	VCC_333	
	N0	VCC_334	
	L0	VCC_335	
	J0	VCC_336	
	AA0	VCC_337	
	W0	VCC_338	
	P0	VCC_339	
	N0	VCC_340	
	L0	VCC_341	
	J0	VCC_342	
	AA0	VCC_343	
	W0	VCC_344	
	P0	VCC_345	
	N0	VCC_346	
	L0	VCC_347	
	J0	VCC_348	
	AA0	VCC_349	
	W0	VCC_350	
	P0	VCC_351	
	N0	VCC_352	
	L0	VCC_353	
	J0	VCC_354	
	AA0	VCC_355	
	W0	VCC_356	
	P0	VCC_357	
	N0	VCC_358	
	L0	VCC_359	
	J0	VCC_360	

VCC

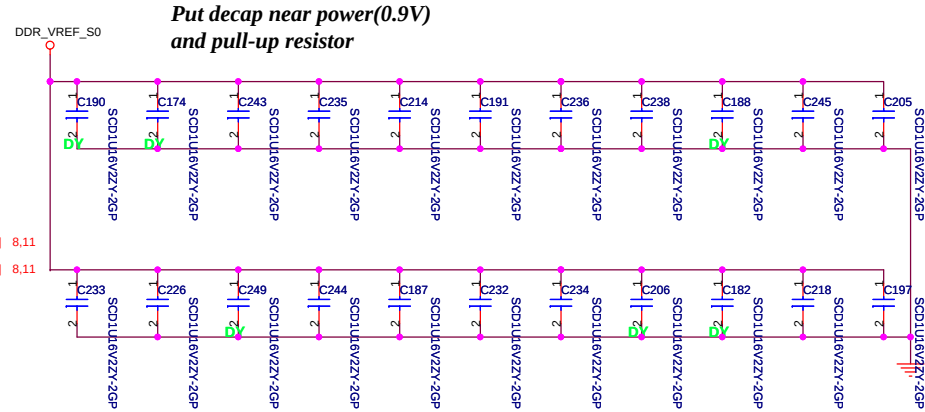
1D05V_S0	U40F		
	71.CALIS.00U		
AD27	VCC_NCTF0		AE27
AC27	VCC_NCTF1	VSS_NCTF0	AE26
AB27	VCC_NCTF2	VSS_NCTF1	AE25
AA27	VCC_NCTF3	VSS_NCTF2	AE24
Y27	VCC_NCTF4	VSS_NCTF3	AE23
W27	VCC_NCTF5	VSS_NCTF4	AE22
V27	VCC_NCTF6	VSS_NCTF5	AE21
U27	VCC_NCTF7	VSS_NCTF6	AE20
T27	VCC_NCTF8	VSS_NCTF7	AE19
R27	VCC_NCTF9	VSS_NCTF8	AE18
Q27	VCC_NCTF10	VSS_NCTF9	AE17
P27	VCC_NCTF11	VSS_NCTF10	Y17
O27	VCC_NCTF12	VSS_NCTF11	U17
N27	VCC_NCTF13	VSS_NCTF12	
M27	VCC_NCTF14		
L27	VCC_NCTF15		
K27	VCC_NCTF16		
J27	VCC_NCTF17		
I27	VCC_NCTF18		
H27	VCC_NCTF19	VCCAUX_NCTF0	AG27
G27	VCC_NCTF20	VCCAUX_NCTF1	AE27
F27	VCC_NCTF21	VCCAUX_NCTF2	AG26
E27	VCC_NCTF22	VCCAUX_NCTF3	AE26
D27	VCC_NCTF23	VCCAUX_NCTF4	AG25
C27	VCC_NCTF24	VCCAUX_NCTF5	AG24
B27	VCC_NCTF25	VCCAUX_NCTF6	AG23
A27	VCC_NCTF26	VCCAUX_NCTF7	AE24
Y26	VCC_NCTF27	VCCAUX_NCTF8	AG23
W26	VCC_NCTF28	VCCAUX_NCTF9	AE23
V26	VCC_NCTF29	VCCAUX_NCTF10	AG22
U26	VCC_NCTF30	VCCAUX_NCTF11	AE22
T26	VCC_NCTF31	VCCAUX_NCTF12	AG21
R26	VCC_NCTF32	VCCAUX_NCTF13	AE21
Q26	VCC_NCTF33	VCCAUX_NCTF14	AG20
P26	VCC_NCTF34	VCCAUX_NCTF15	AE20
O26	VCC_NCTF35	VCCAUX_NCTF16	AG19
N26	VCC_NCTF36	VCCAUX_NCTF17	AE19
M26	VCC_NCTF37	VCCAUX_NCTF18	AG18
L26	VCC_NCTF38	VCCAUX_NCTF19	AE18
K26	VCC_NCTF39	VCCAUX_NCTF20	R18
J26	VCC_NCTF40	VCCAUX_NCTF21	AG17
I26	VCC_NCTF41	VCCAUX_NCTF22	AE17
H26	VCC_NCTF42	VCCAUX_NCTF23	AE17
G26	VCC_NCTF43	VCCAUX_NCTF24	AD17
F26	VCC_NCTF44	VCCAUX_NCTF25	AB17
E26	VCC_NCTF45	VCCAUX_NCTF26	AE17
D26	VCC_NCTF46	VCCAUX_NCTF27	W17
C26	VCC_NCTF47	VCCAUX_NCTF28	T17
B26	VCC_NCTF48	VCCAUX_NCTF29	V17
A26	VCC_NCTF49	VCCAUX_NCTF30	T17
Y25	VCC_NCTF50	VCCAUX_NCTF31	AG16
W25	VCC_NCTF51	VCCAUX_NCTF32	AE16
V25	VCC_NCTF52	VCCAUX_NCTF33	AE16
U25	VCC_NCTF53	VCCAUX_NCTF34	AD16
T25	VCC_NCTF54	VCCAUX_NCTF35	AC16
R25	VCC_NCTF55	VCCAUX_NCTF36	AB16
Q25	VCC_NCTF56	VCCAUX_NCTF37	AE16
P25	VCC_NCTF57	VCCAUX_NCTF38	V16
O25	VCC_NCTF58	VCCAUX_NCTF39	AE16
N25	VCC_NCTF59	VCCAUX_NCTF40	V16
M25	VCC_NCTF60	VCCAUX_NCTF41	U16
L25	VCC_NCTF61	VCCAUX_NCTF42	T16
K25	VCC_NCTF62	VCCAUX_NCTF43	R16
J25	VCC_NCTF63	VCCAUX_NCTF44	AG15
I25	VCC_NCTF64	VCCAUX_NCTF45	AE15
H25	VCC_NCTF65	VCCAUX_NCTF46	AE15
G25	VCC_NCTF66	VCCAUX_NCTF47	AD15
F25	VCC_NCTF67	VCCAUX_NCTF48	AE15
E25	VCC_NCTF68	VCCAUX_NCTF49	AB15
D25	VCC_NCTF69	VCCAUX_NCTF50	AE15
C25	VCC_NCTF70	VCCAUX_NCTF51	W15
B25	VCC_NCTF71	VCCAUX_NCTF52	Y15
A25	VCC_NCTF72	VCCAUX_NCTF53	V15



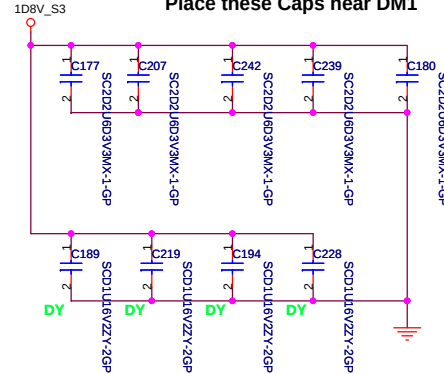
PARALLEL TERMINATION



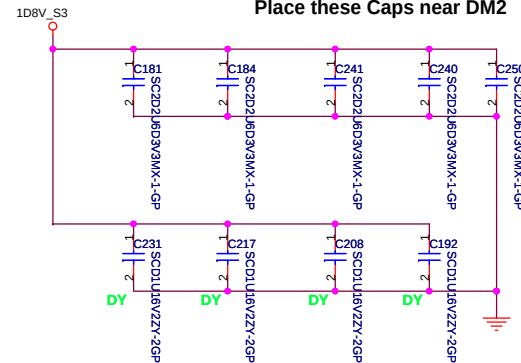
Decoupling Capacitor



Place these Caps near DM1

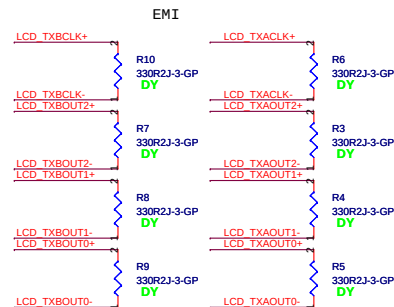
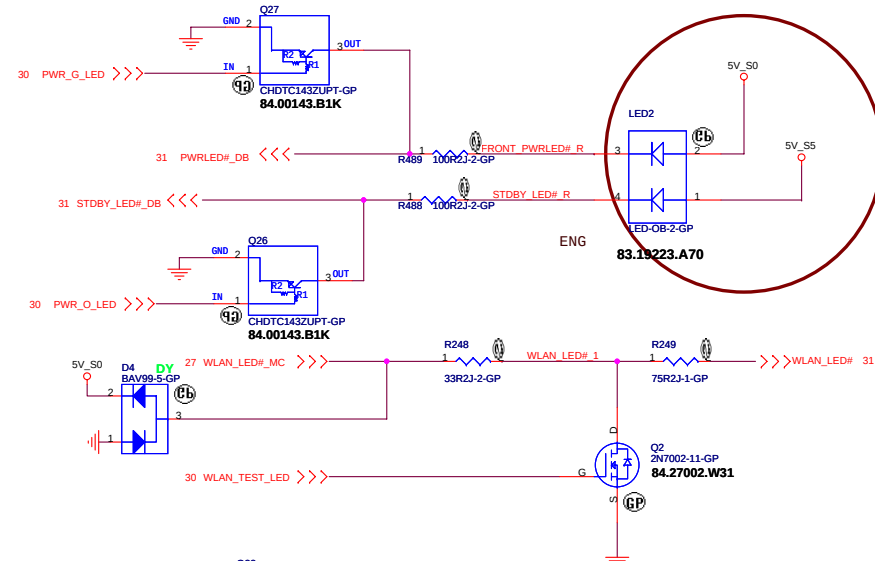


Place these Caps near DM2



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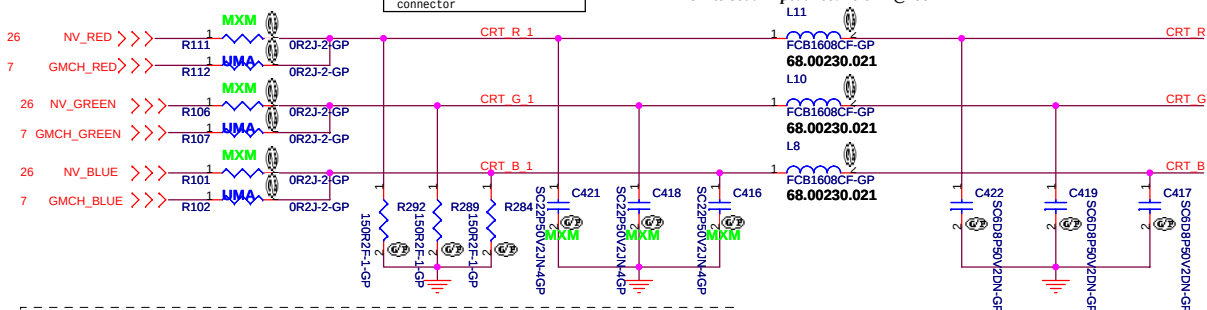
Title			
DDR2 Termination Resistor			
Size	Document Number	Rev	
		SD	
Date:	Monday, March 12, 2007	Sheet	12 of 44



CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector

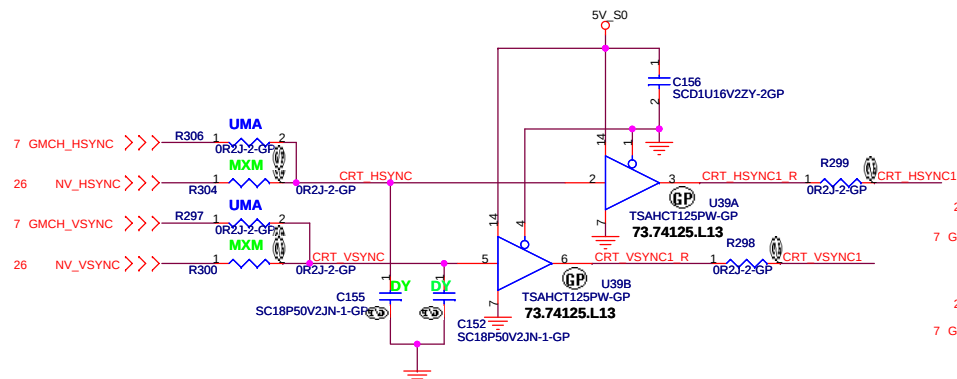
Ferrite bead impedance: 10 ohm@100MHz



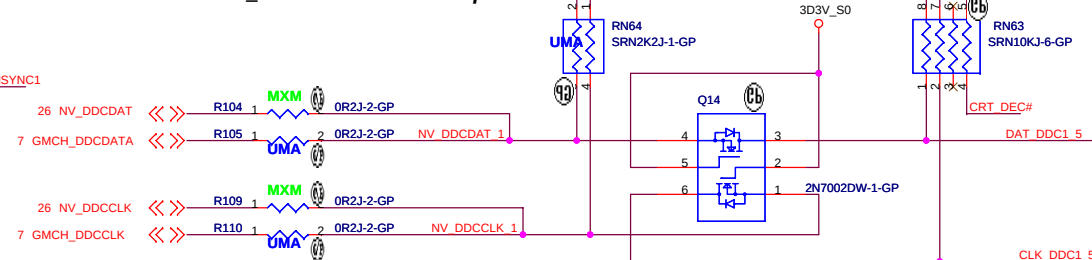
Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

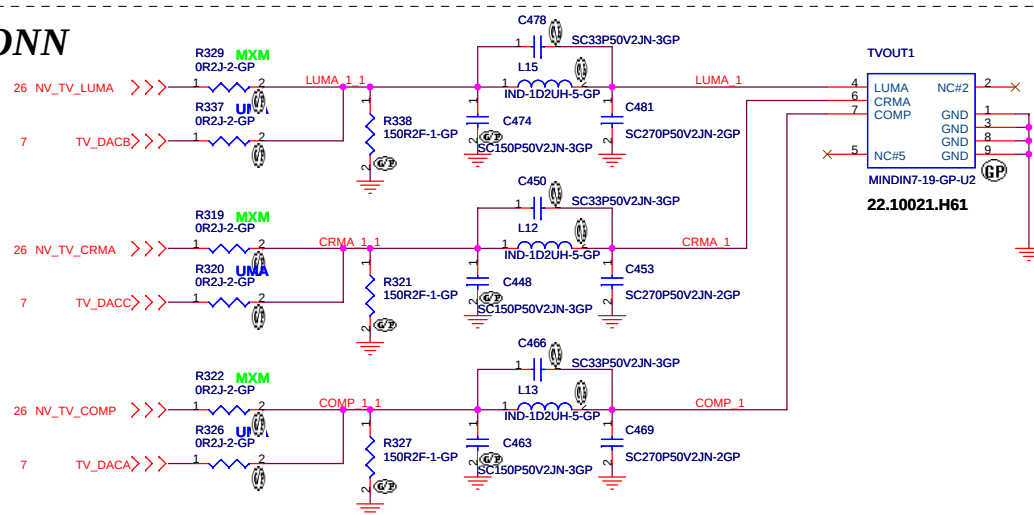
Hsync & Vsync level shift



DDC_CLK & DATA level shift

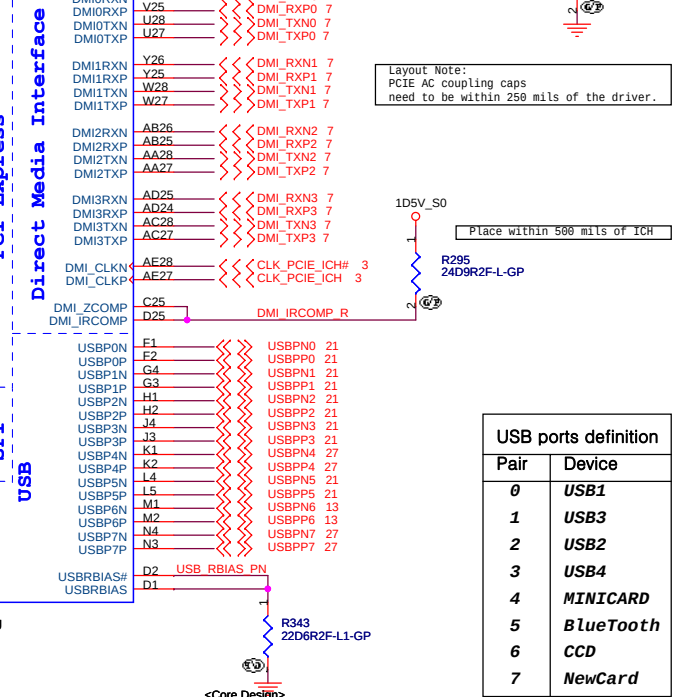
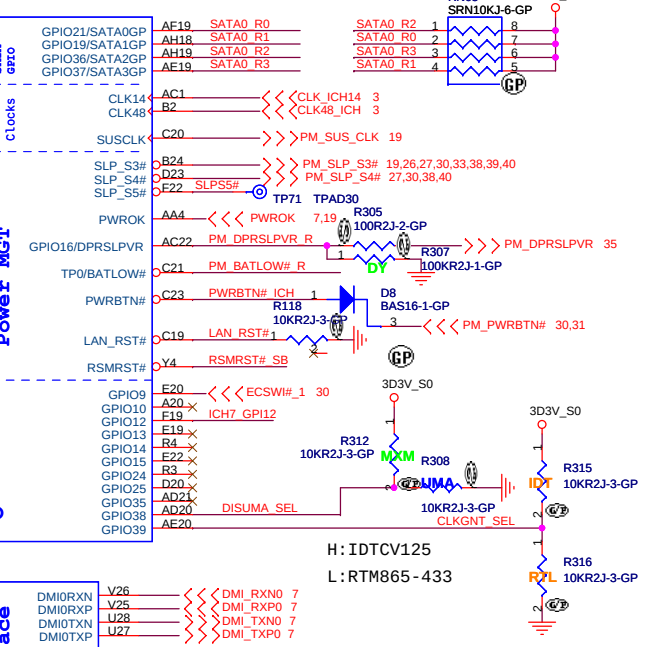


TV CONN

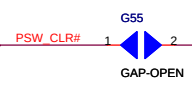


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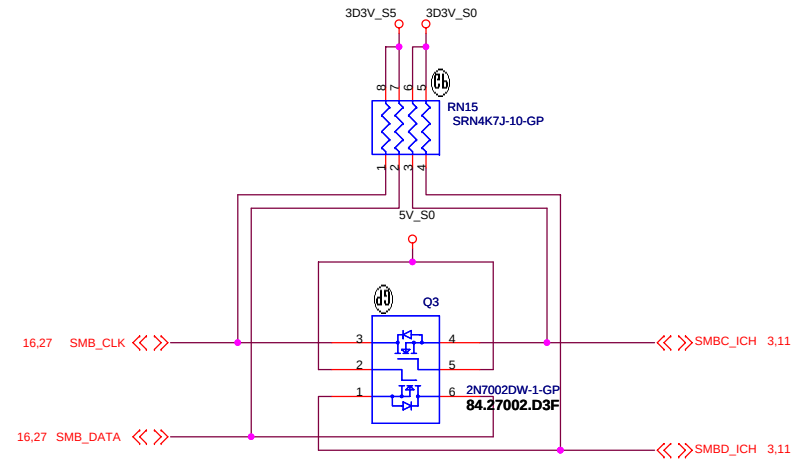
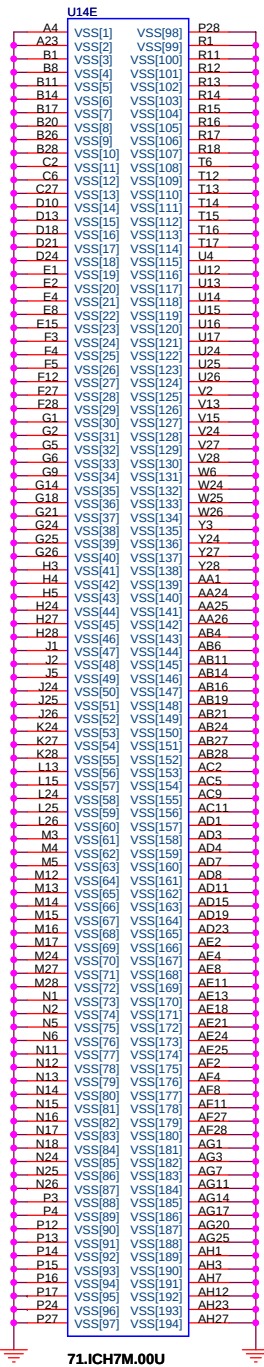
Title		
CRT/TV Connector		
Size	Document Number	Rev
		SD
Date:	Monday, March 12, 2007	Sheet 14 of 44



GAP放在Dimm Door打開可量測處



USB ports definition	
Pair	Device
0	<i>USB1</i>
1	<i>USB3</i>
2	<i>USB2</i>
3	<i>USB4</i>
4	<i>MINICARD</i>
5	<i>BlueTooth</i>
6	<i>CCD</i>
7	<i>NewCard</i>



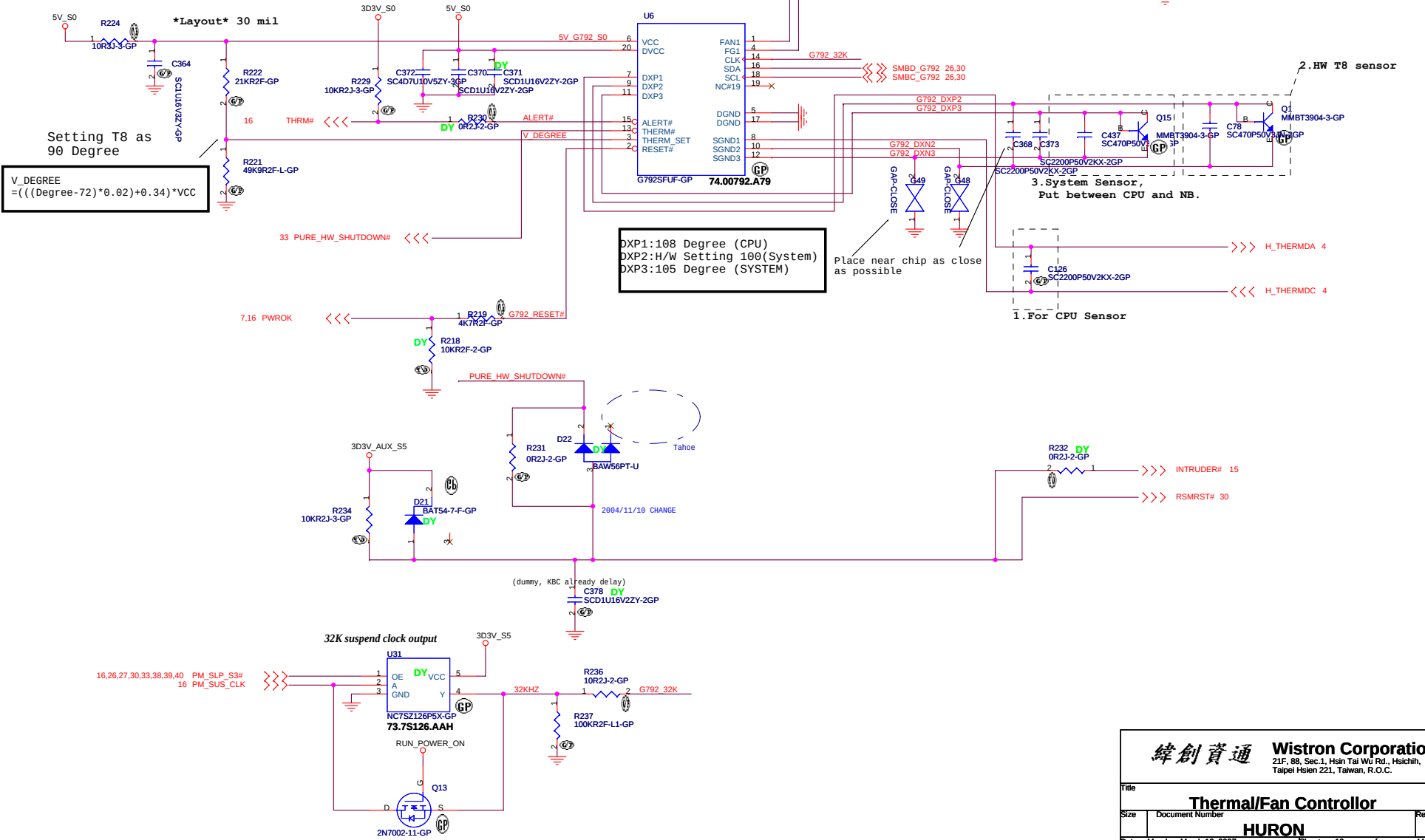
Q14 connect SMLINK and SMBUS in S) for SMBUS 2.0 compliance

SMBUS

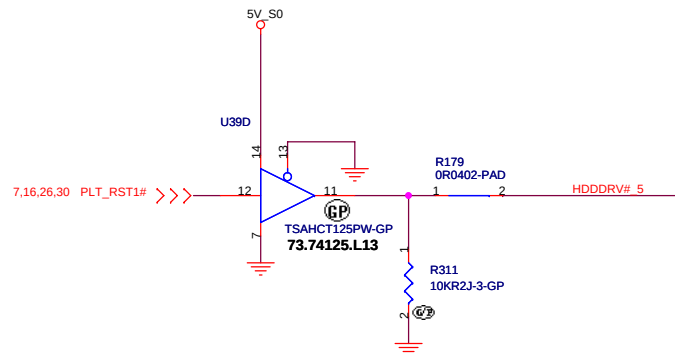
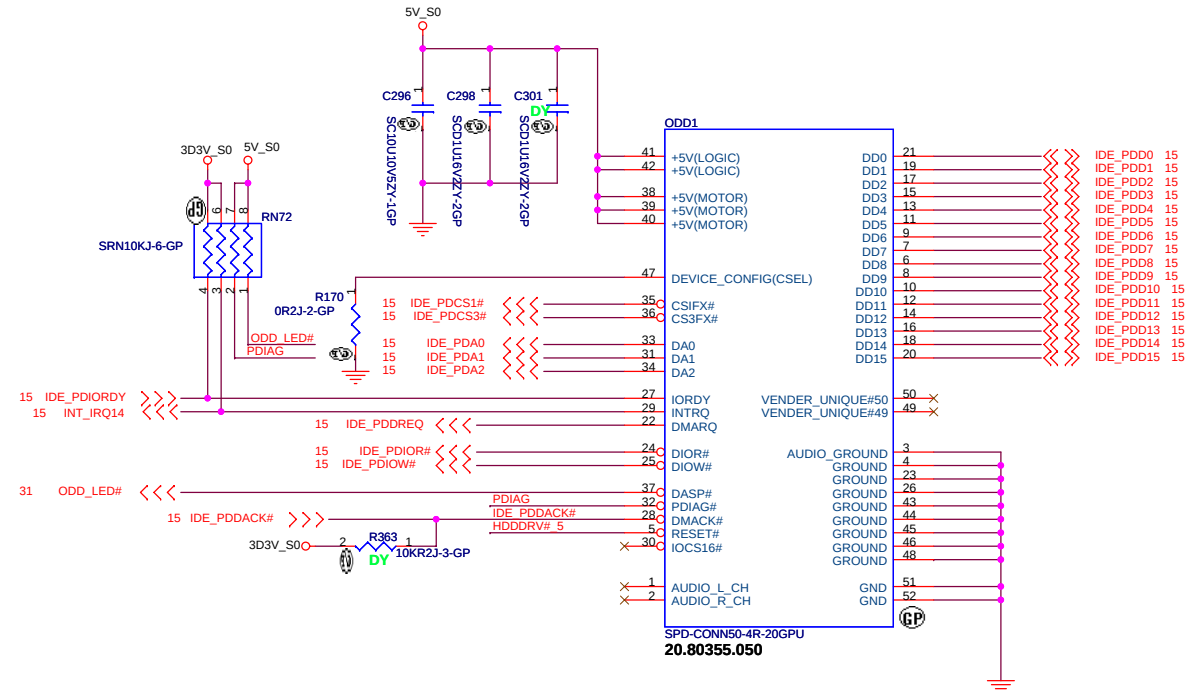
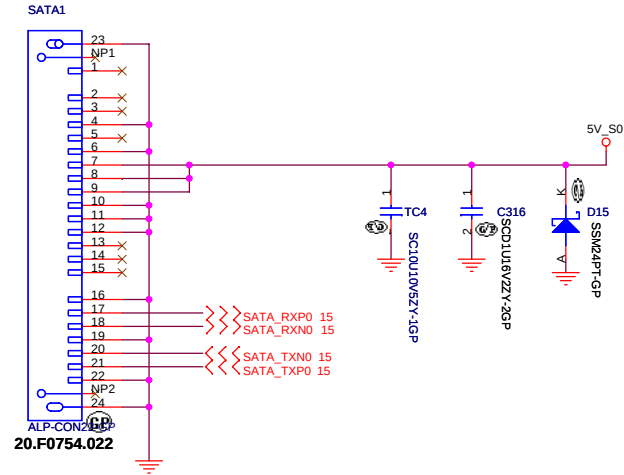
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Taipei Hsien 221, Taiwan, R.O.C.

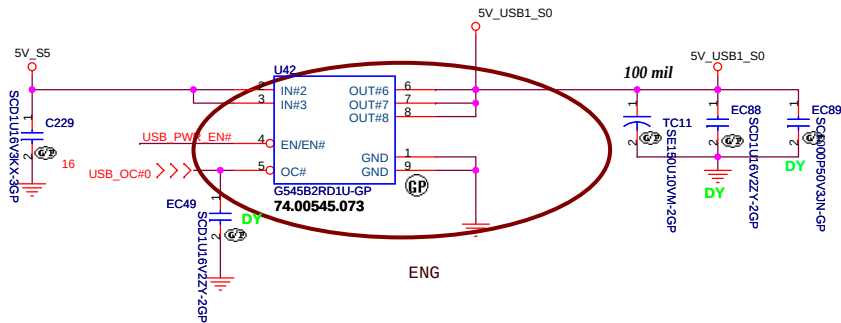
Title				
ICH7-M (4 of 4)				
Size	Document Number			Rev
HURON			SD	
Date:	Monday, March 12, 2007		Sheet 18 of 44	

TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

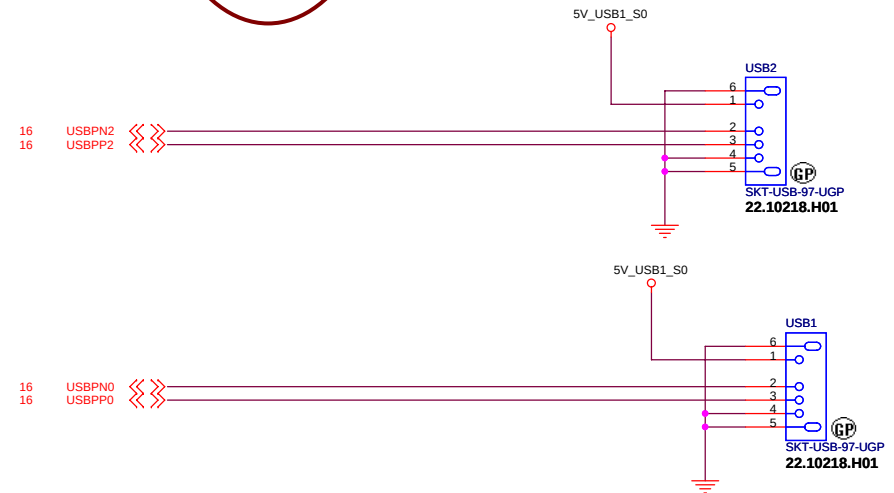
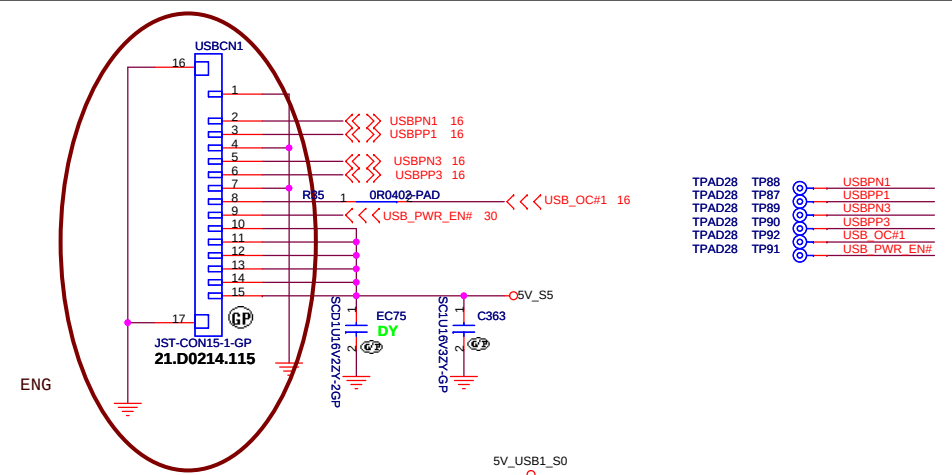
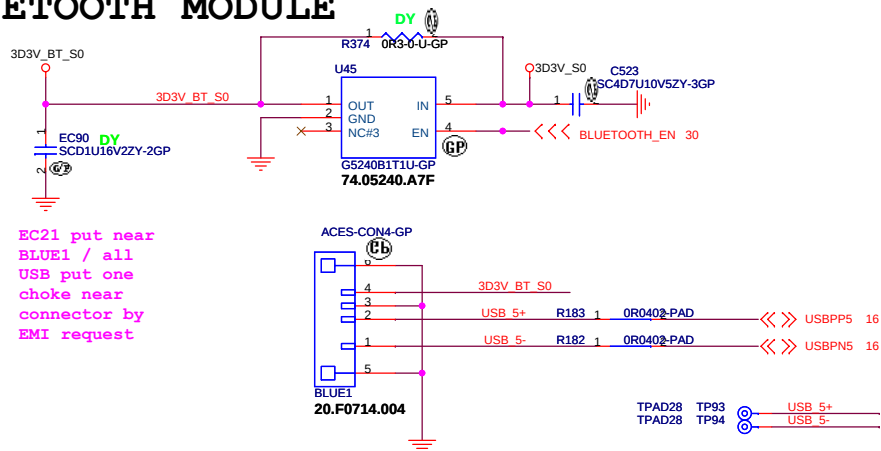


ODD Connector



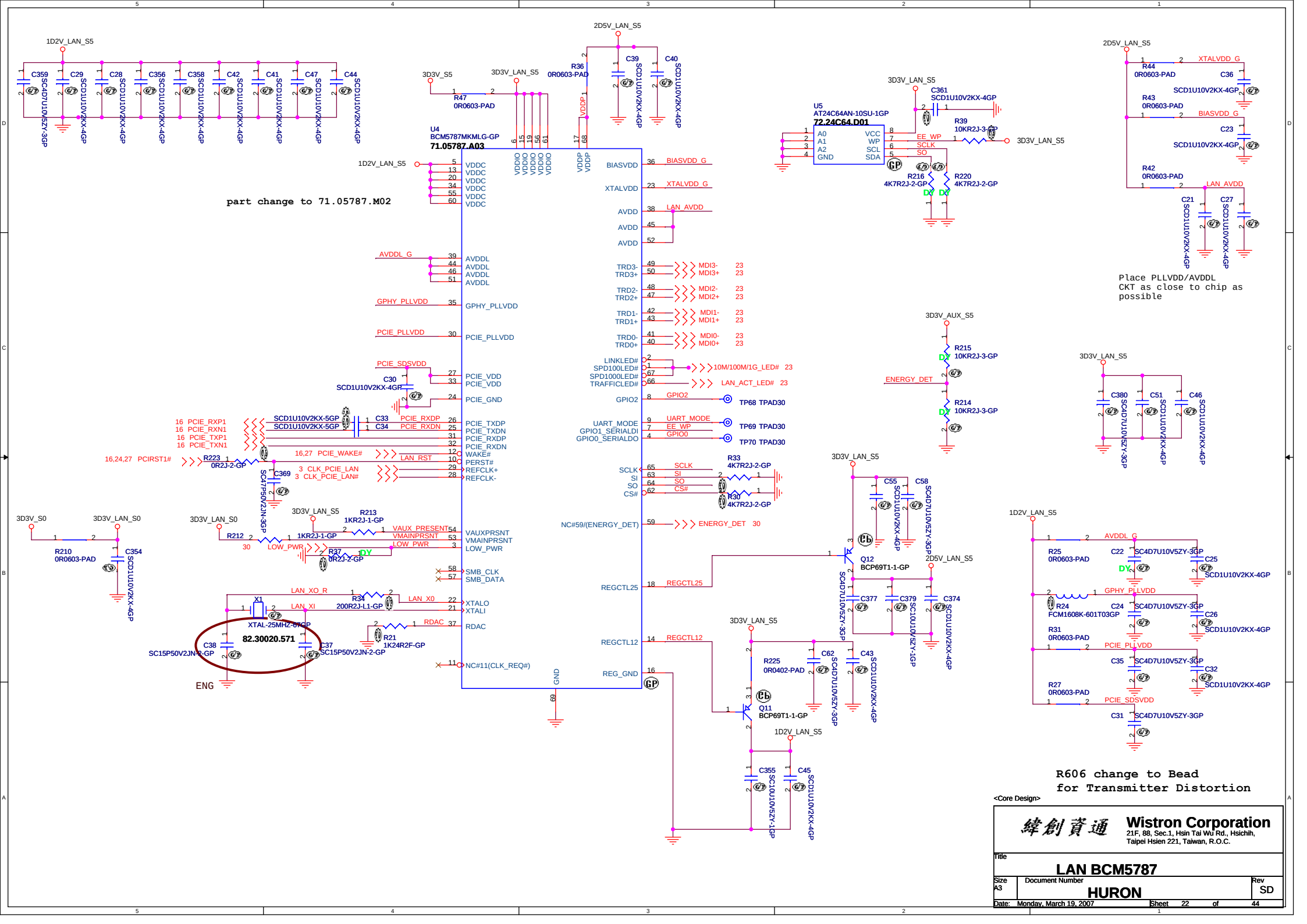


BLUETOOTH MODULE



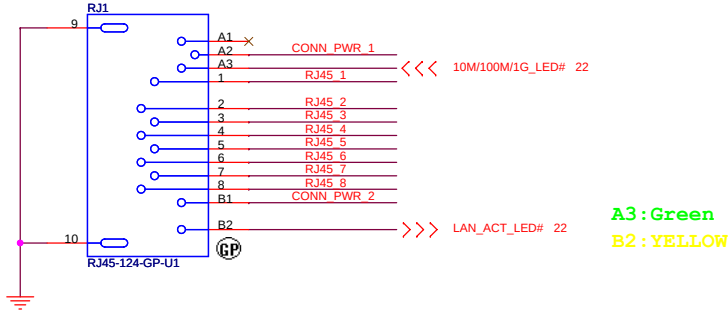
<Core Design>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB / BLUETOOTH			
Size	Document Number		Rev
	HURON		SD
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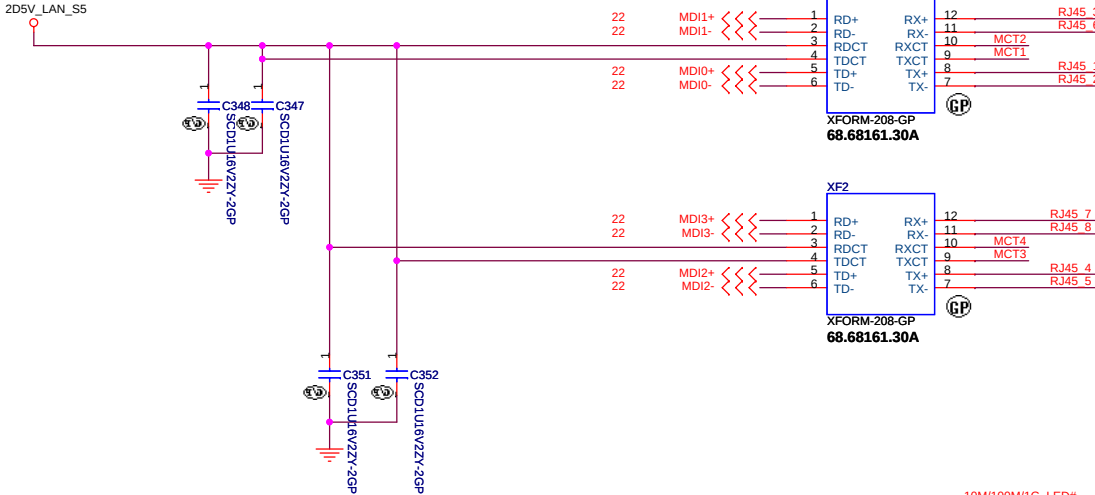
Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

LAN Connector



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
LAN Data: Yellow(B2), when LAN is transferring data.

GIGA Lan Transformer

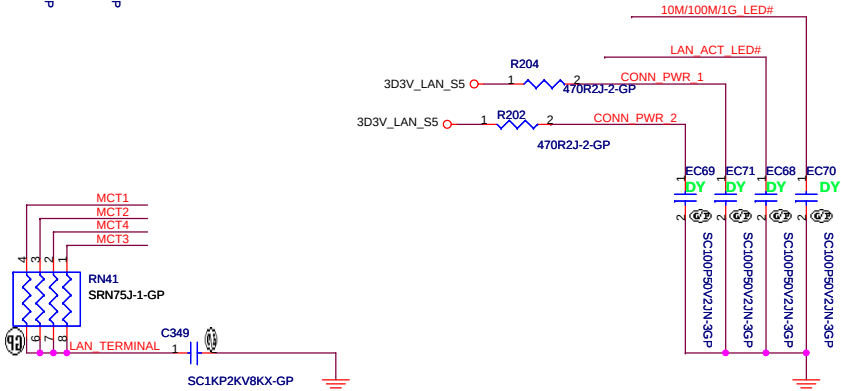


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



<Core Design>

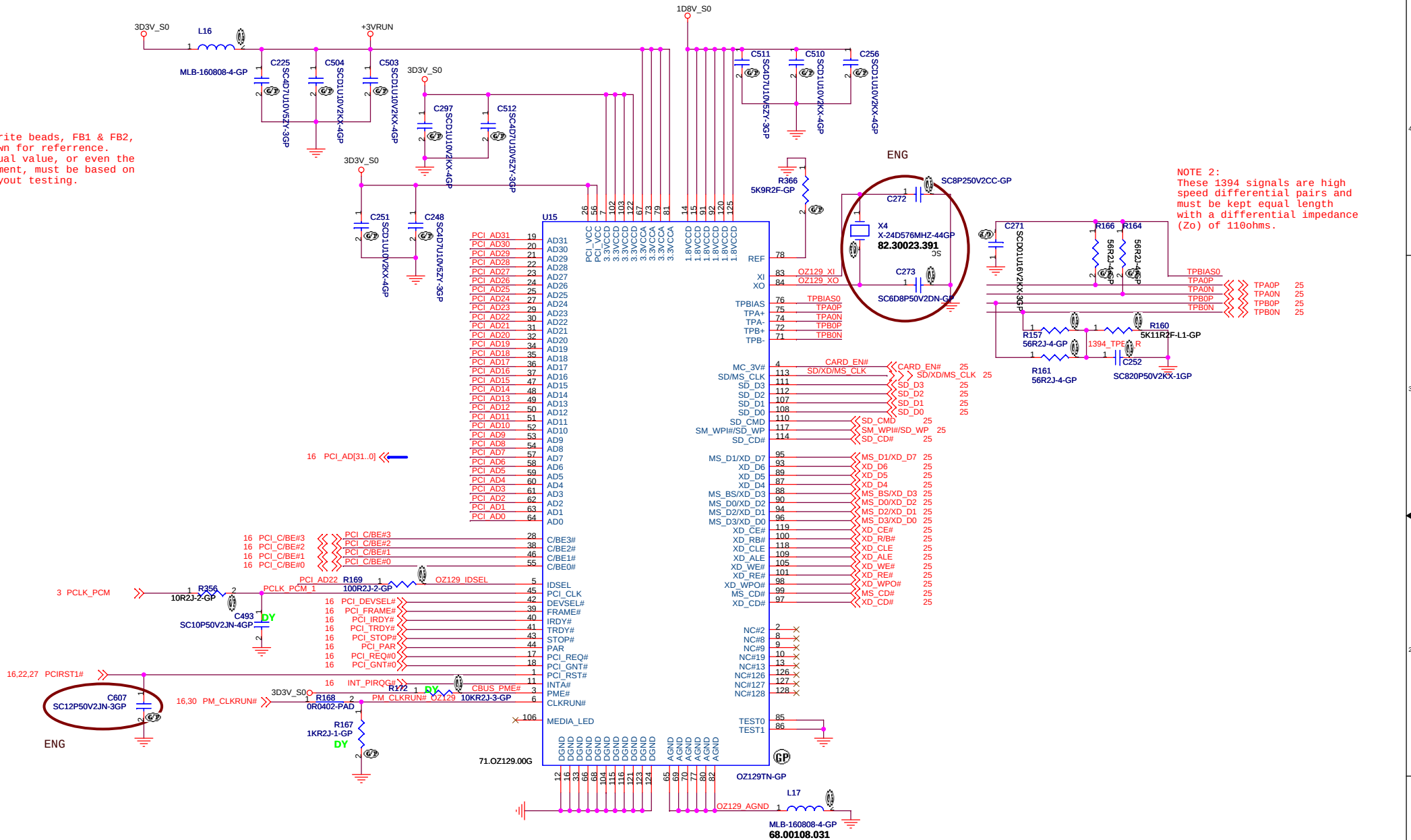
緯創資通 Wistron Corporation
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Title: **LAN Connector**

Size A3	Document Number HURON	Rev SD
Date: Monday, March 19, 2007	Sheet 23 of 44	

NOTE 1:
The Ferrite beads, FB1 & FB2,
are shown for reference.
The actual value, or even the
requirement, must be based on
post-layout testing.

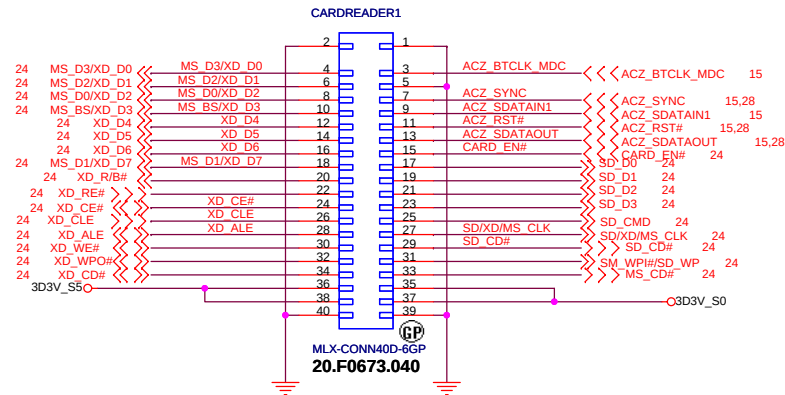
NOTE 2:
These 1394 signals are high
speed differential pairs and
must be kept equal length
with a differential impedance
(Zo) of 110ohms.



IDSEL:AD22
INTA-->:INT_PIRQG#
GNT:PCI_GNT#0
REQ:PCI_REQ#0

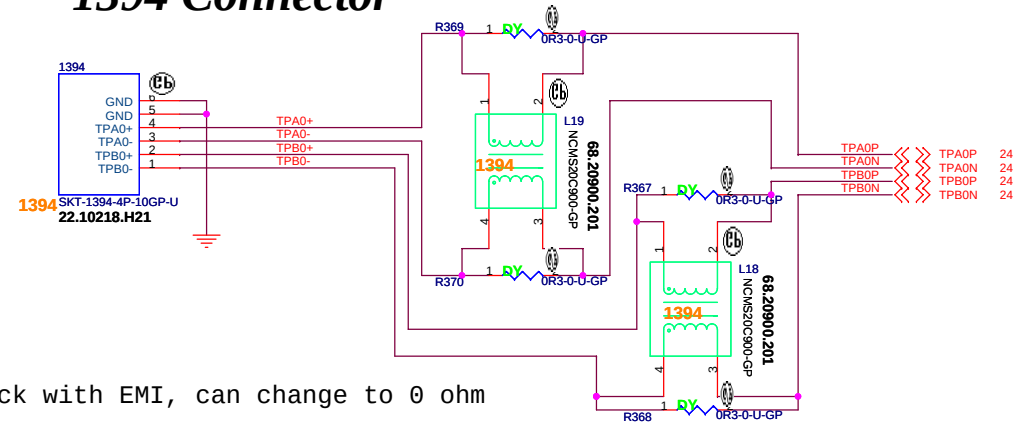
<Core Design>

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Title	
OZ129T	
Size	Document Number
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CONN on Bottom side

1394 Connector



check with EMI, can change to 0 ohm

<Core Design>

緯創資通

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Title

1394 / CARD READER BD

Size

Document Number

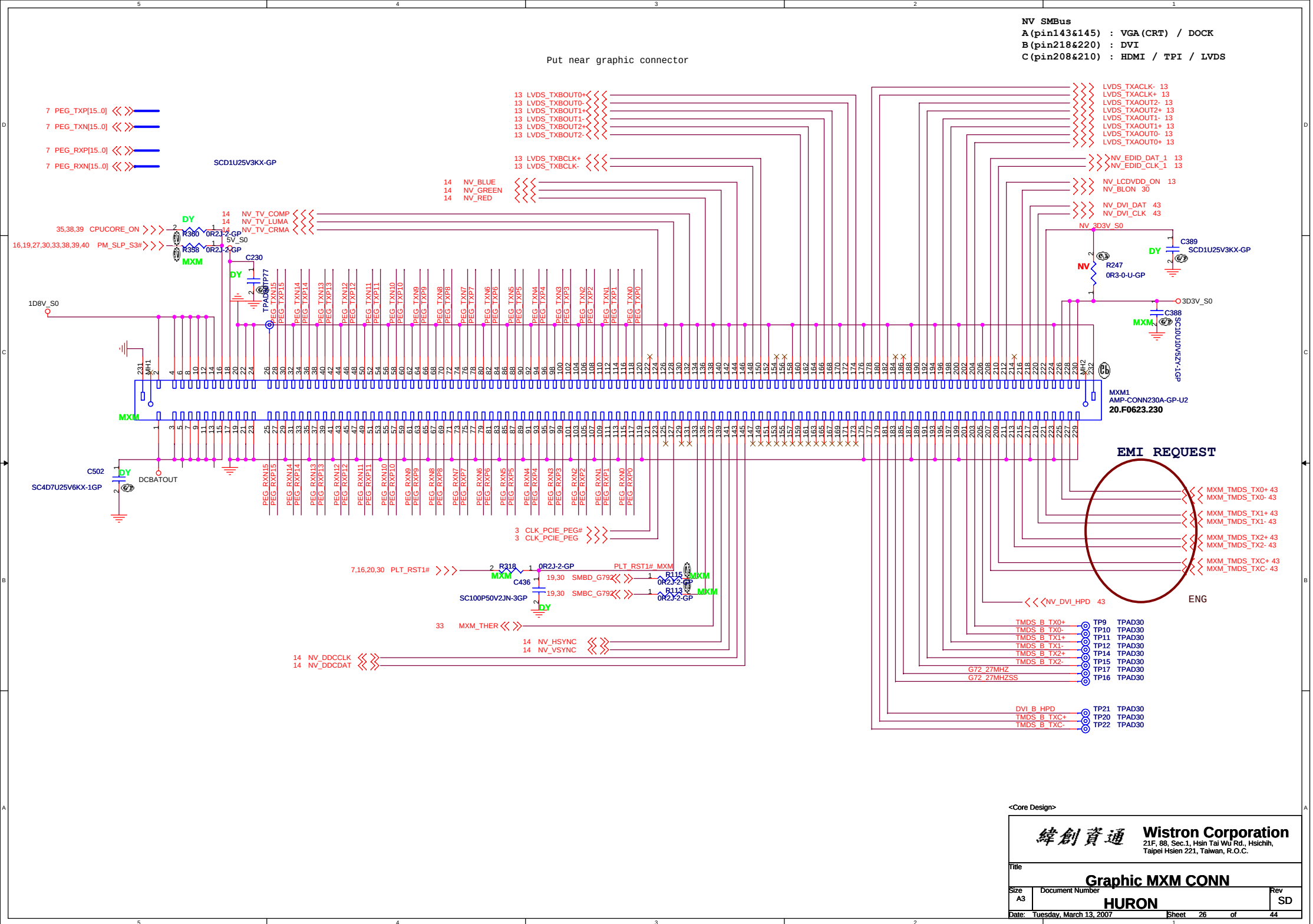
HURON

Rev

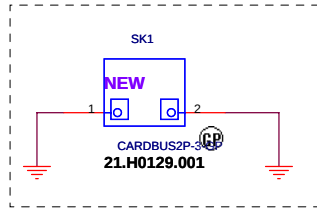
SD

Date: Tuesday, March 13, 2007

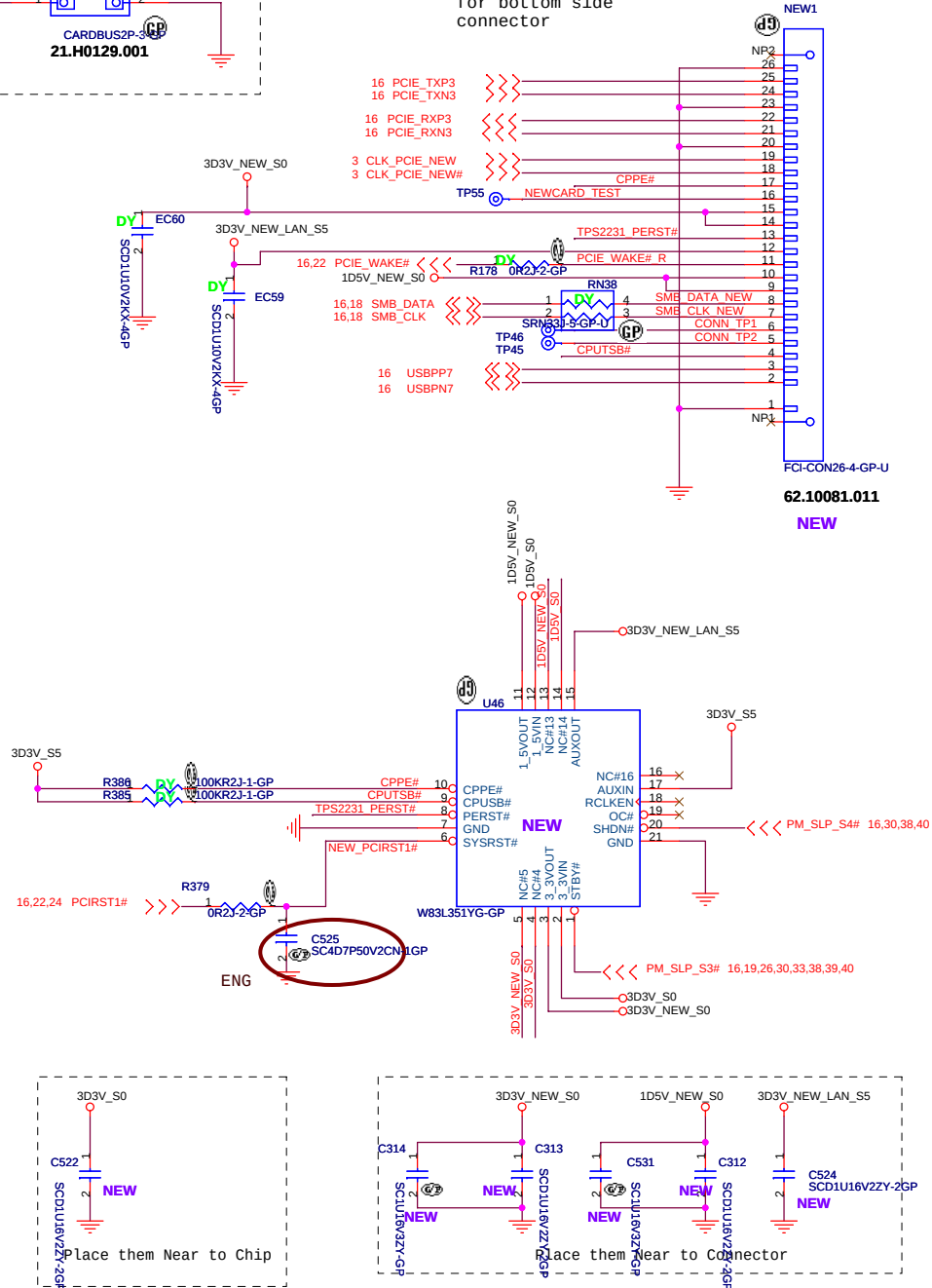
Sheet 25 of 44



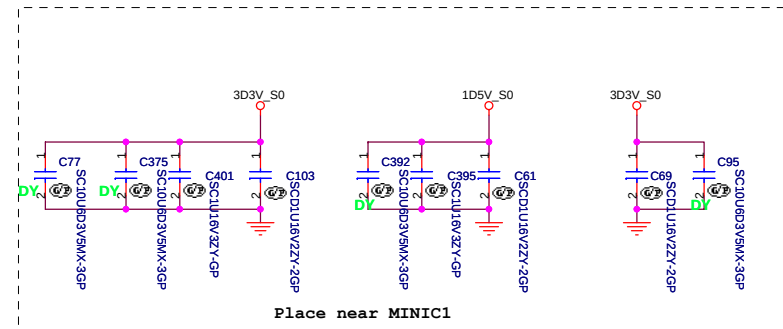
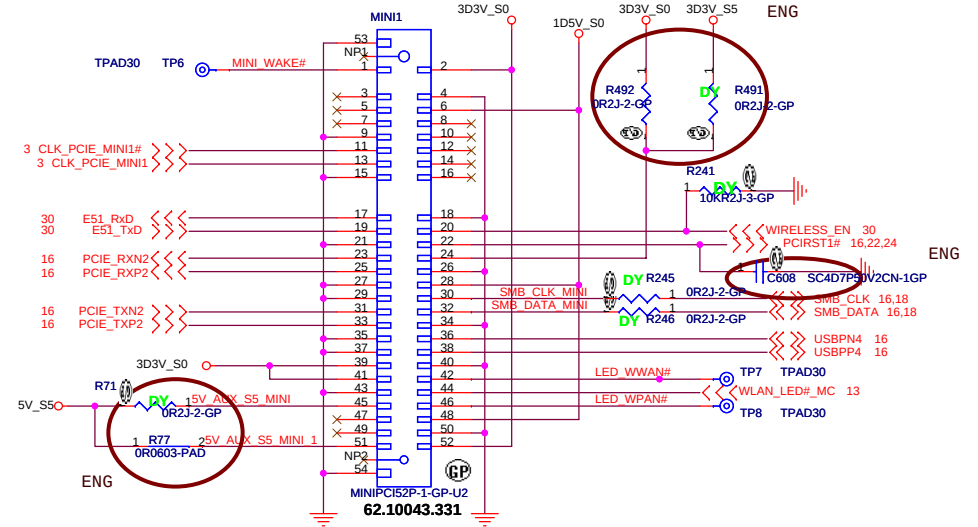
NEWCARD Connector



Reserve the symbol
for bottom side
connector



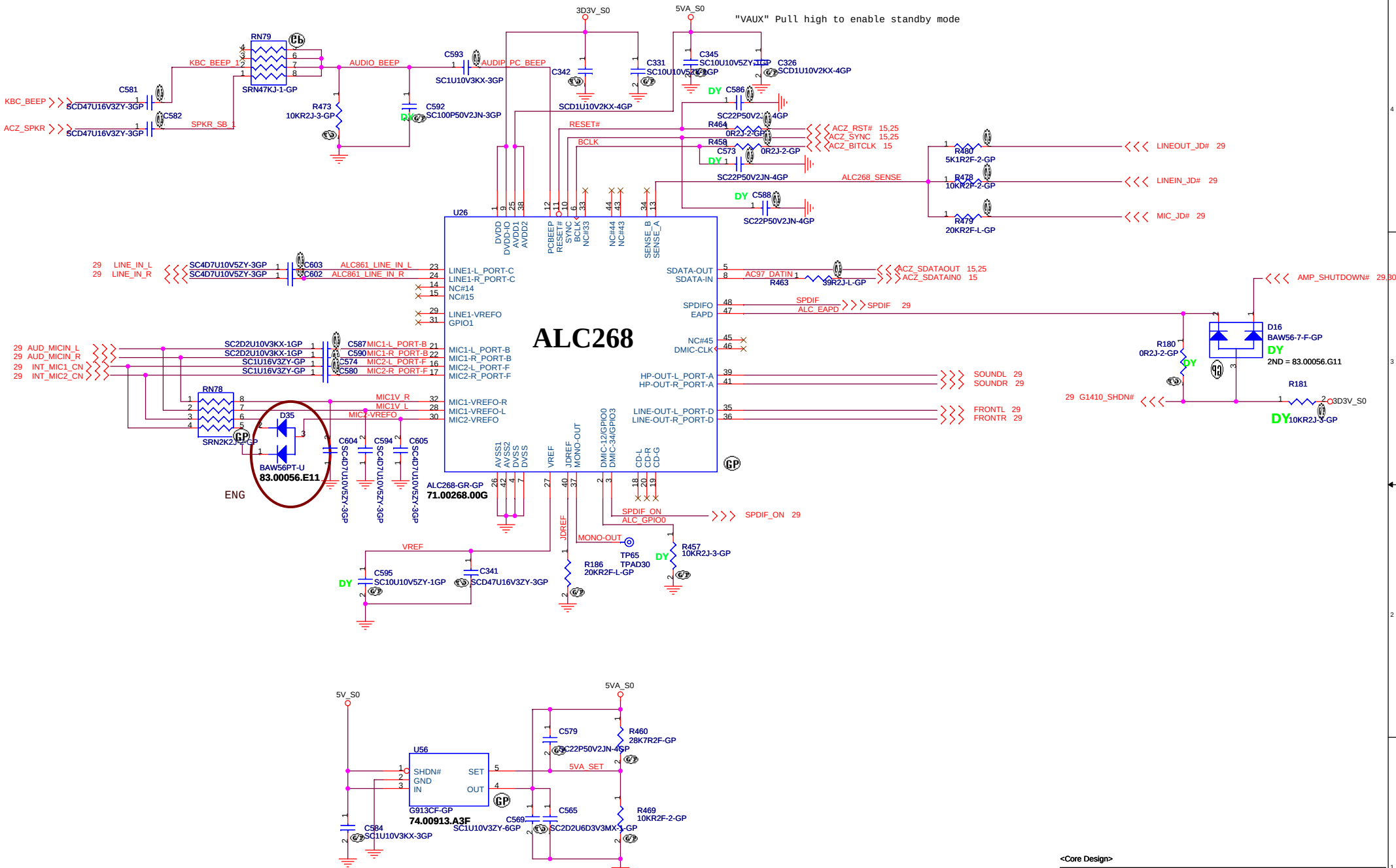
Mini Card Connector



<Core Design>

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Title			
MINI CARD / NEW CARD			
Size	Document Number	Rev	SD
HURON			
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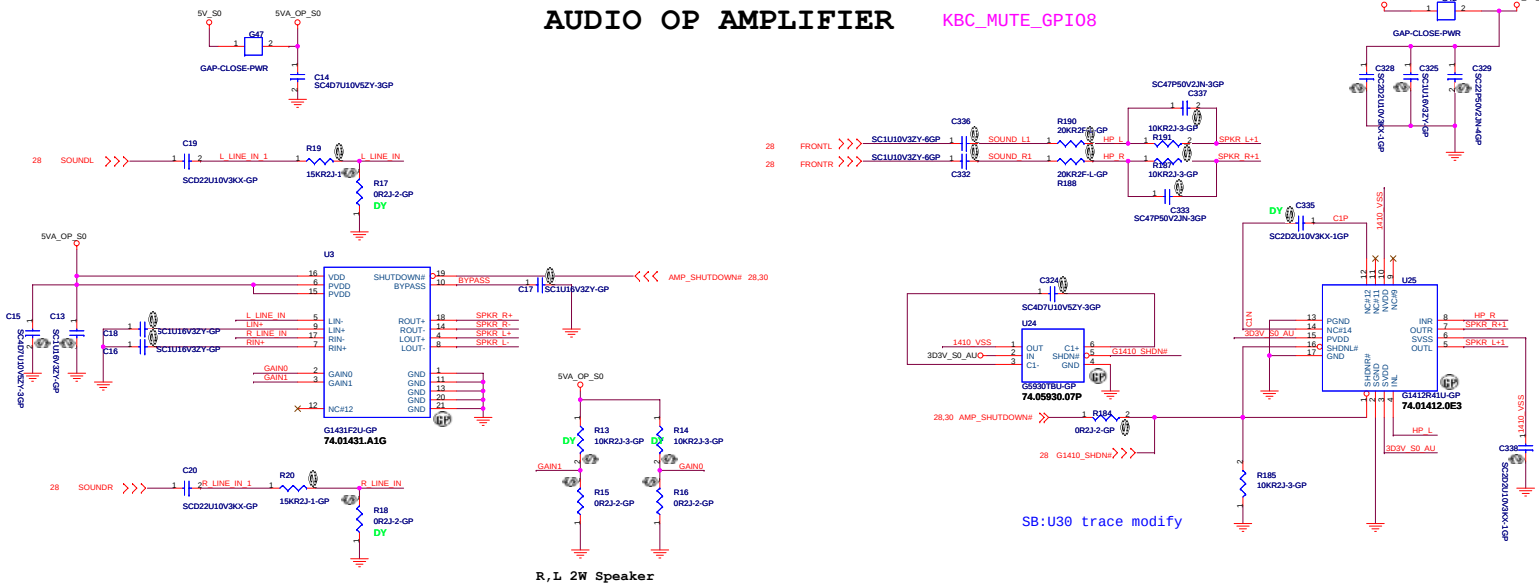


<Core Design>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AZALIA CODEC - ALC268			
Size	Document Number		Rev
	HURON		SD
Date:	Wednesday, March 14, 2007	Sheet 28 of 44	

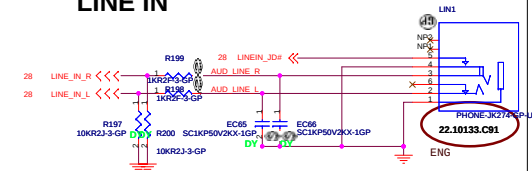
AUDIO OP AMPLIFIER

KBC_MUTE_GPI08

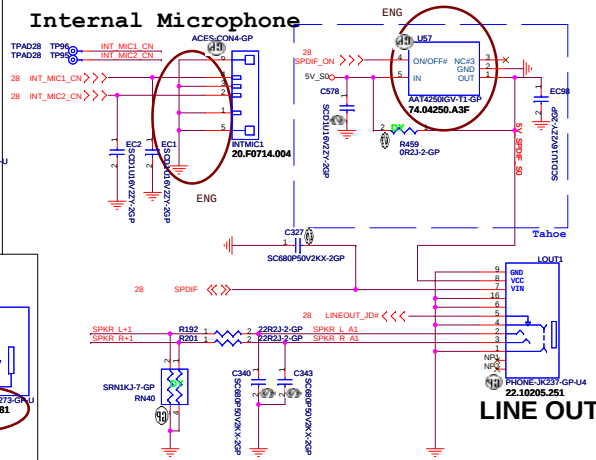


R, L 2W Speaker

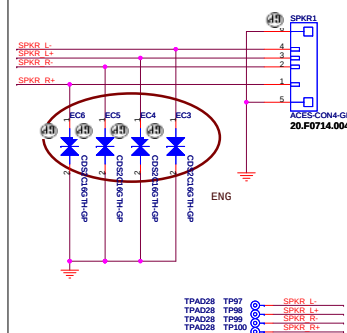
LINE IN



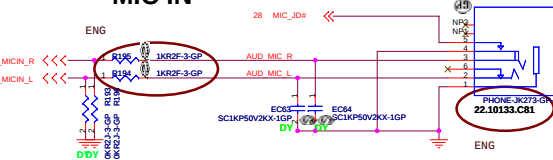
Internal Microphone



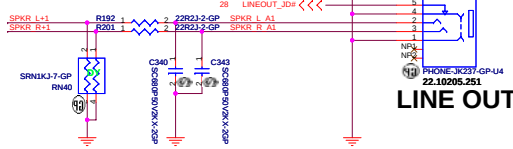
Internal Speaker



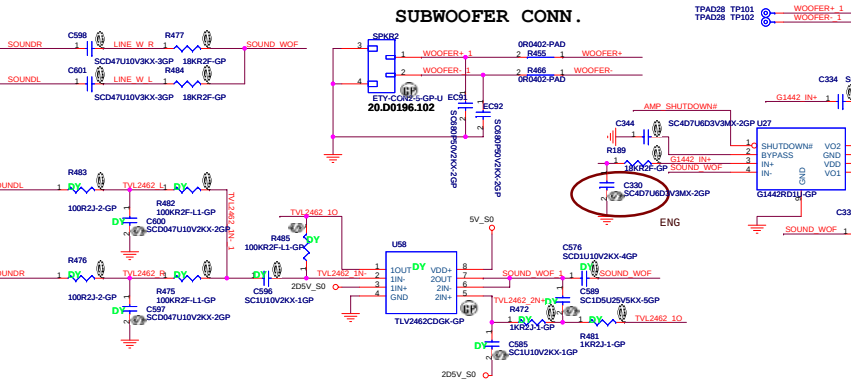
MIC IN



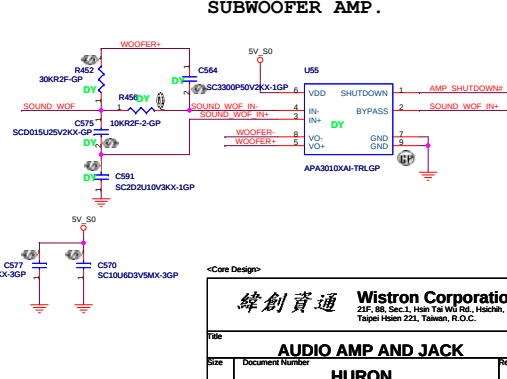
LINE OUT

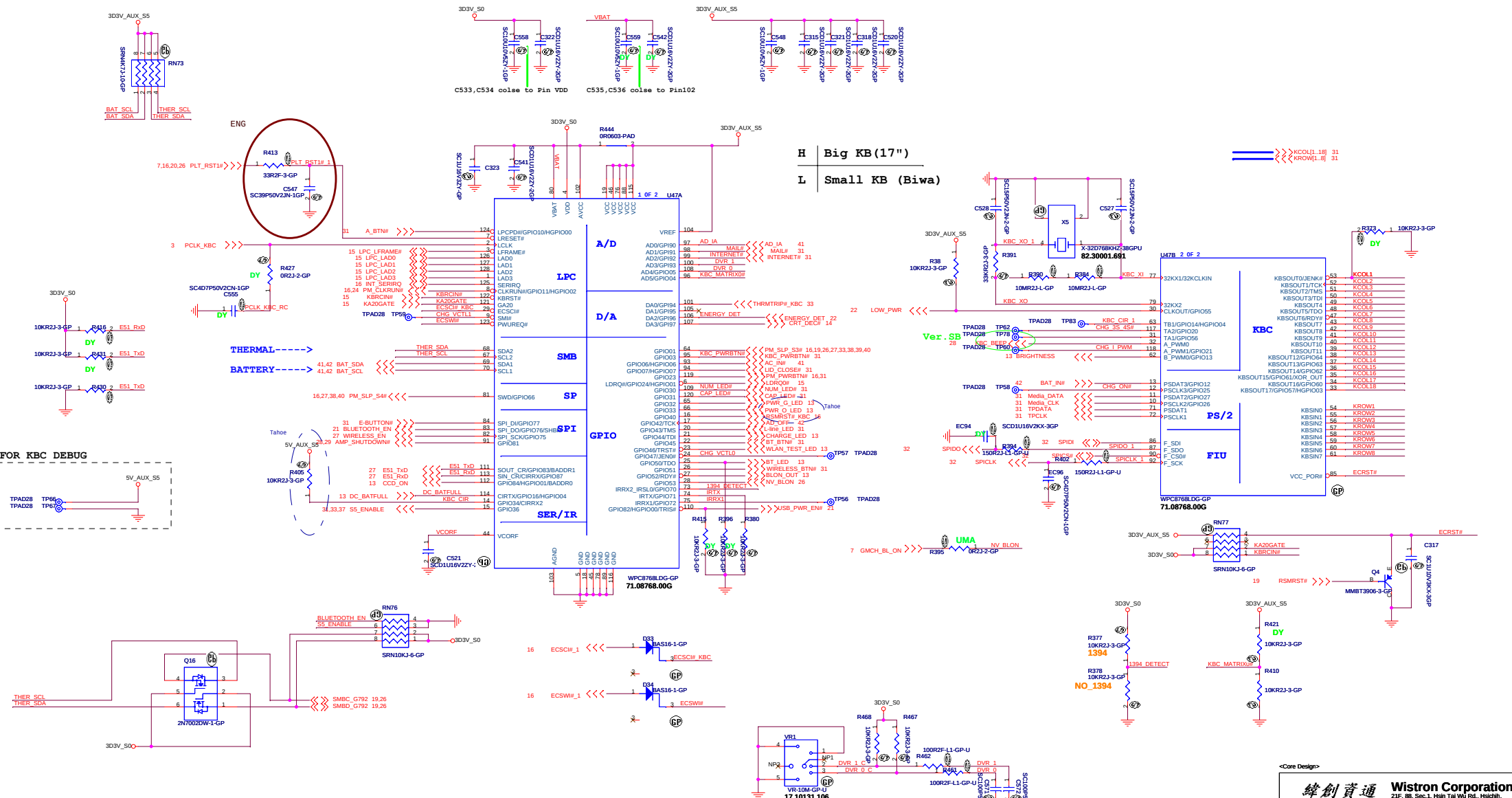


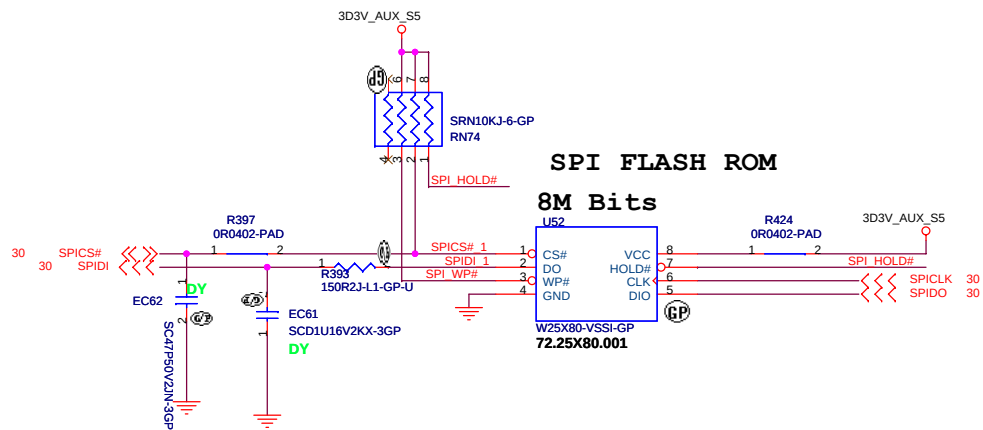
SUBWOOFER CONN.



SUBWOOFER AMP.



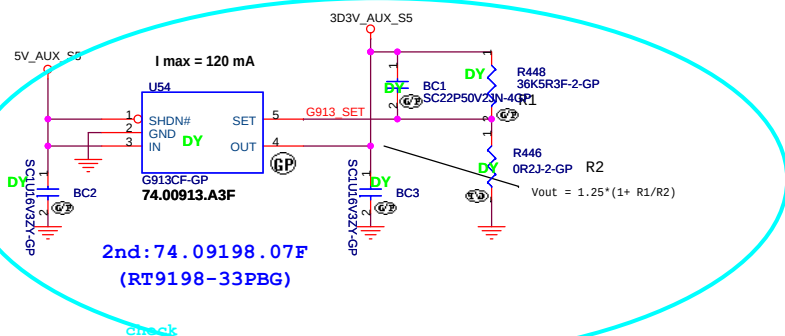
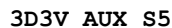




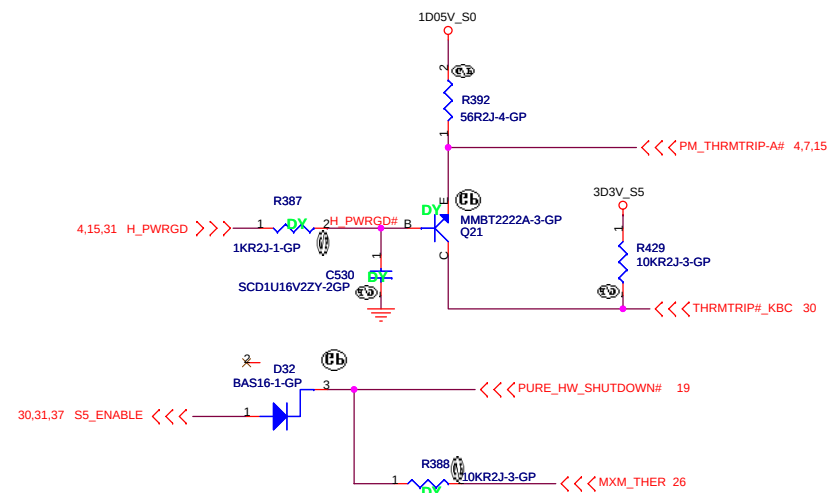
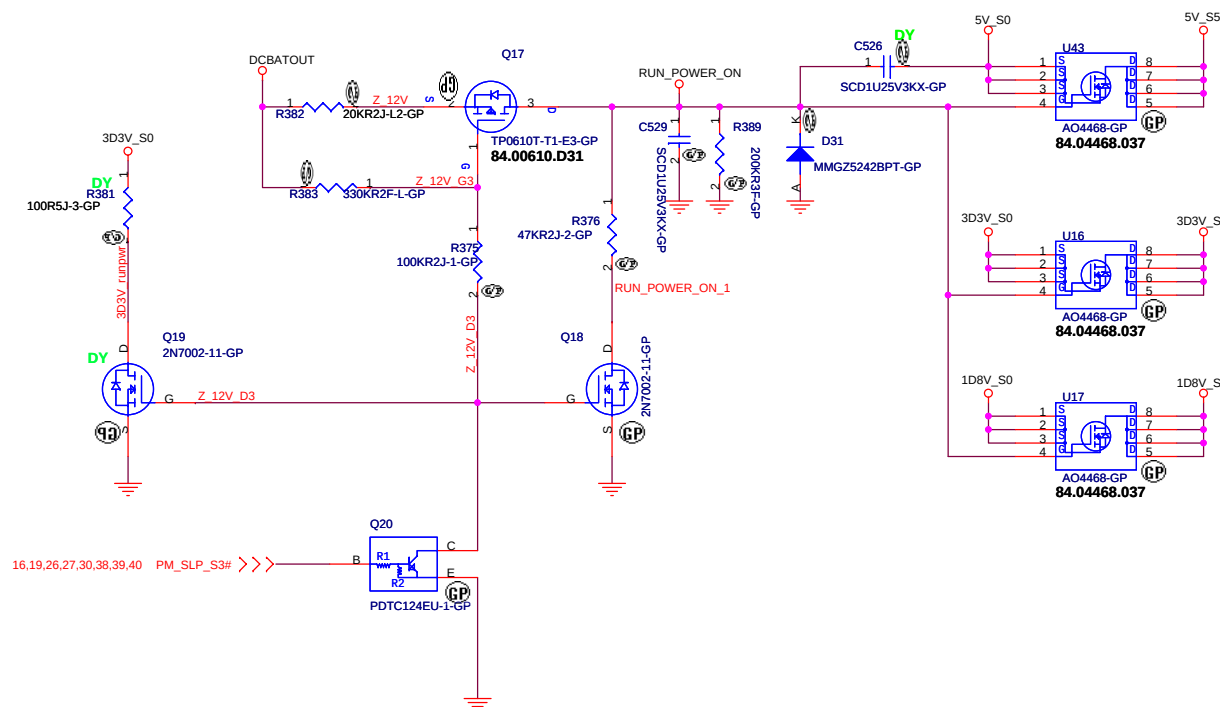
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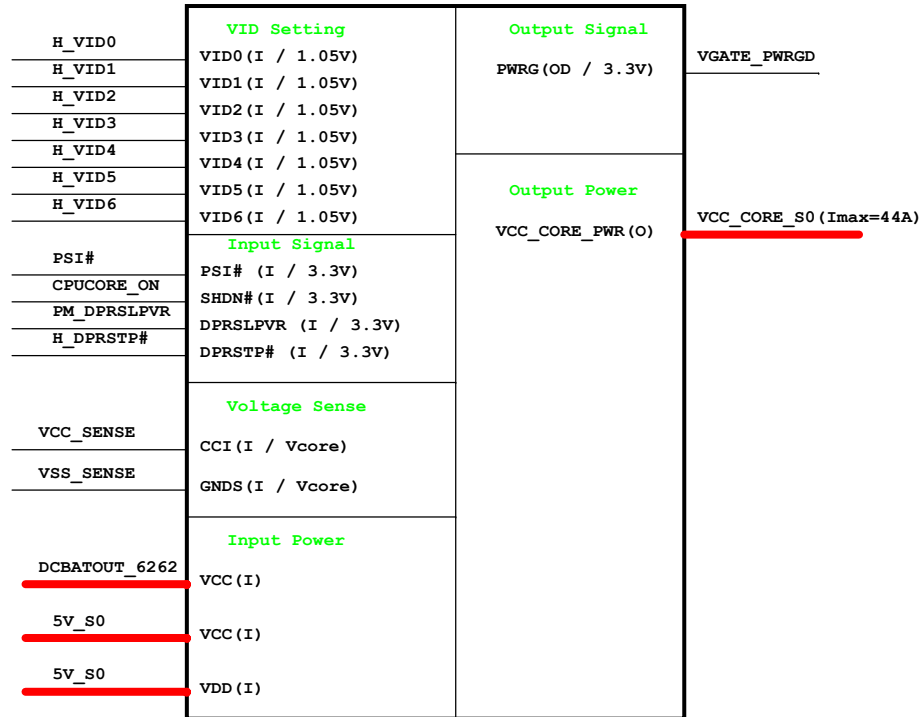
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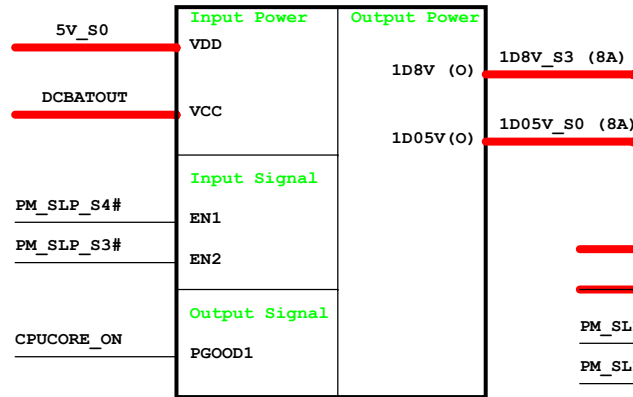
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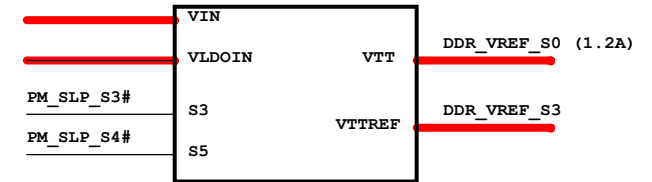
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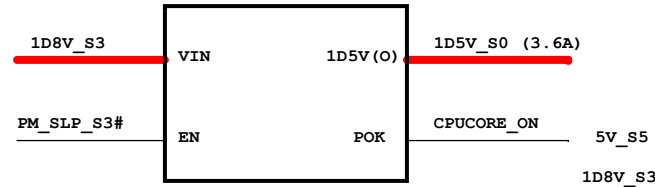
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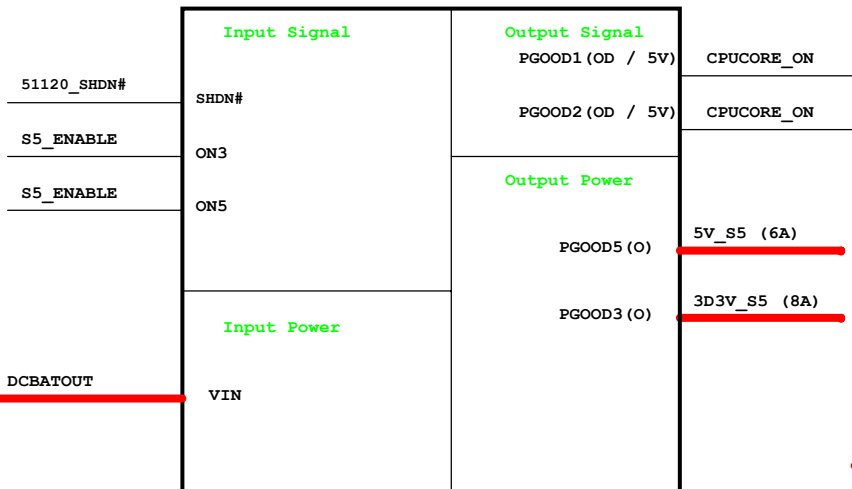
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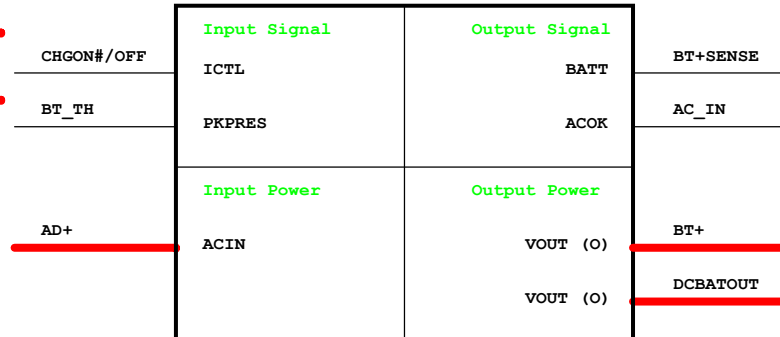
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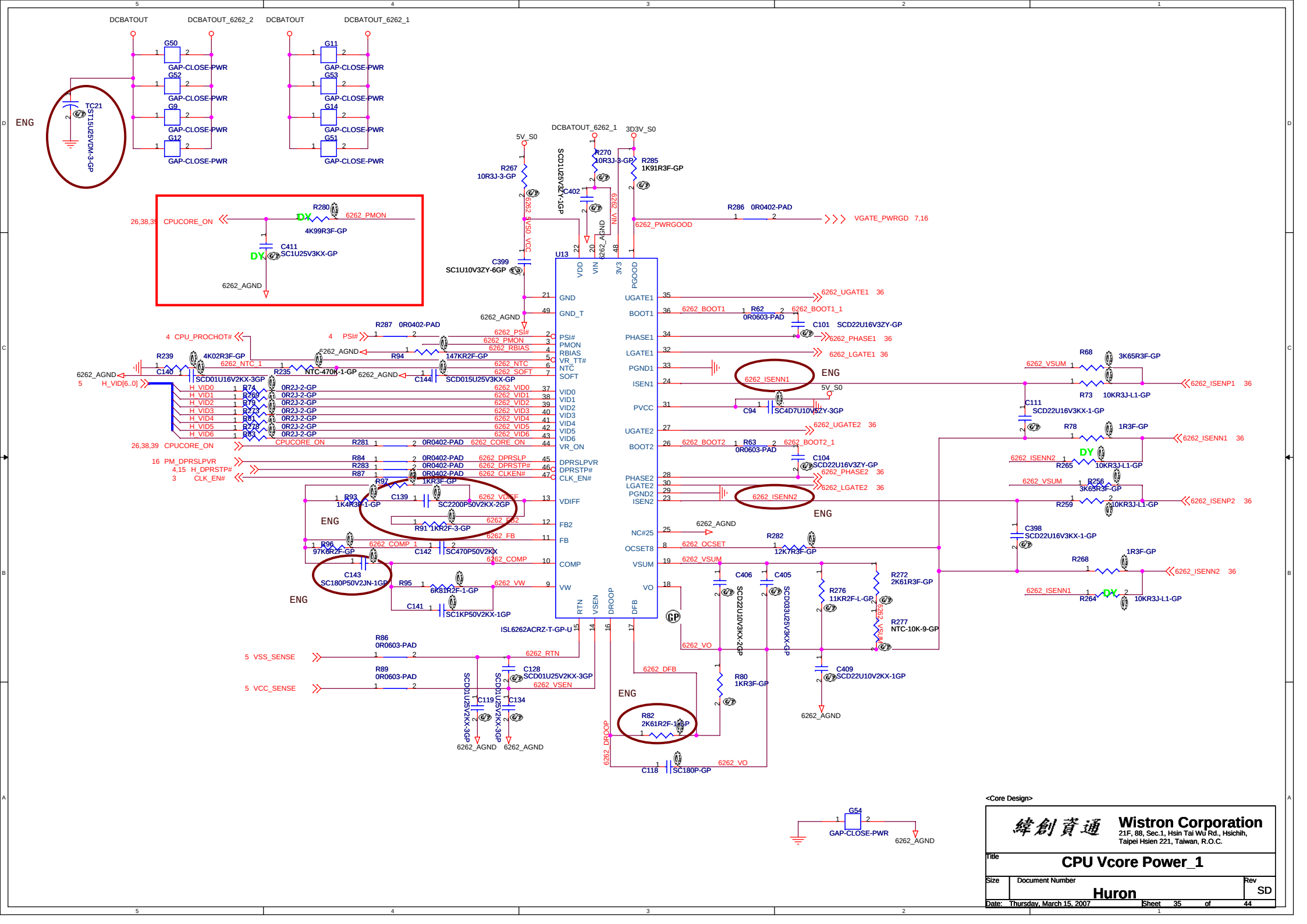


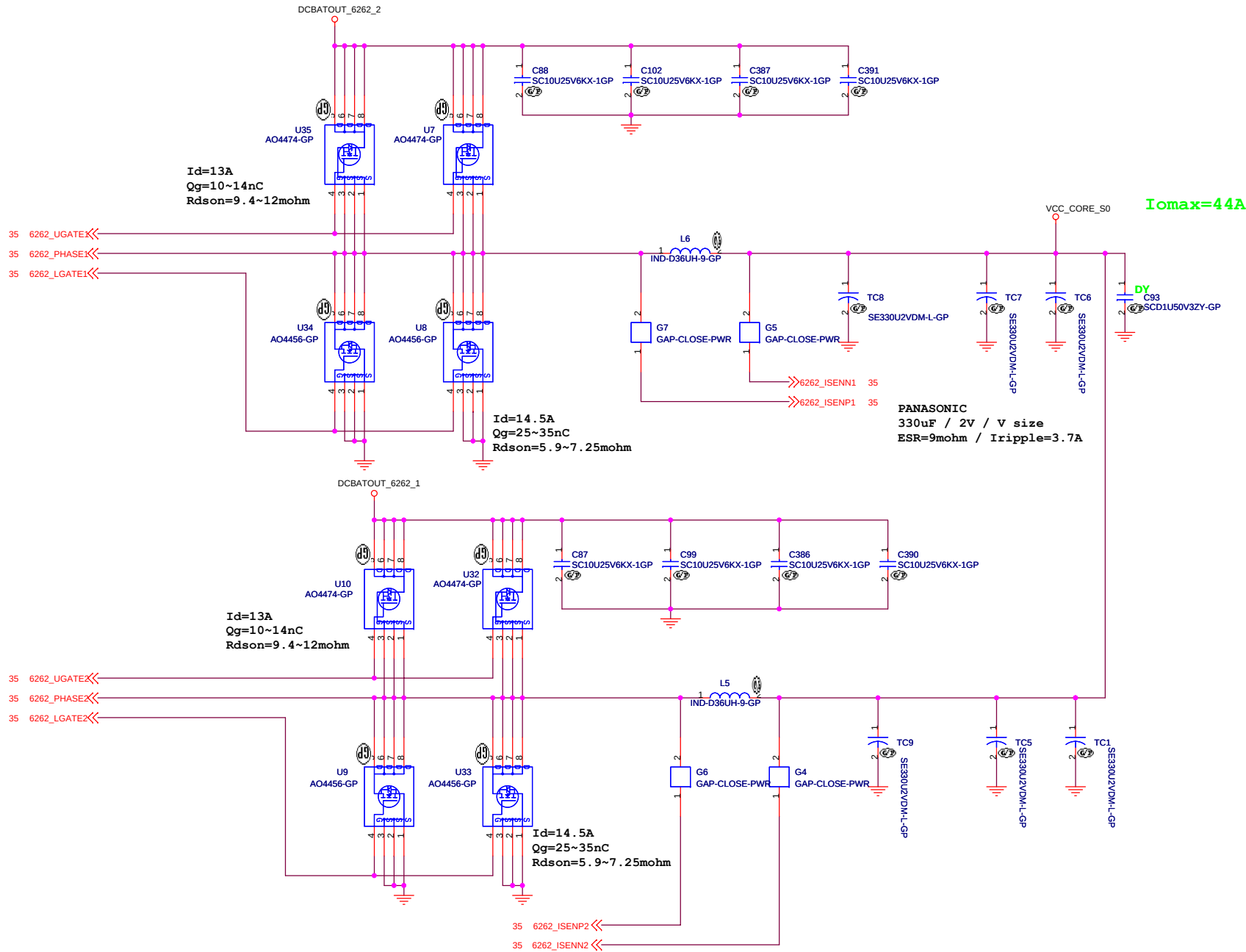
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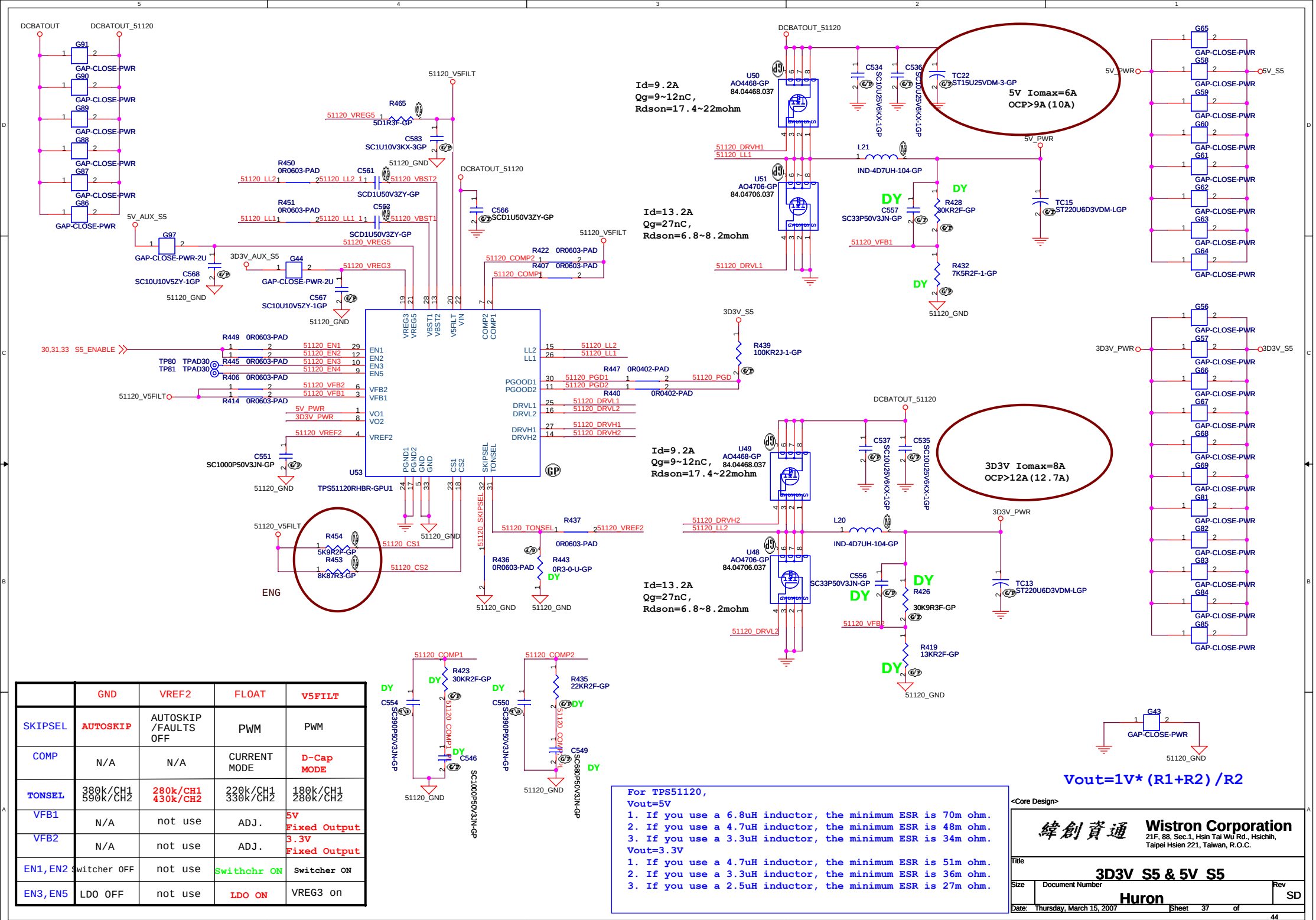
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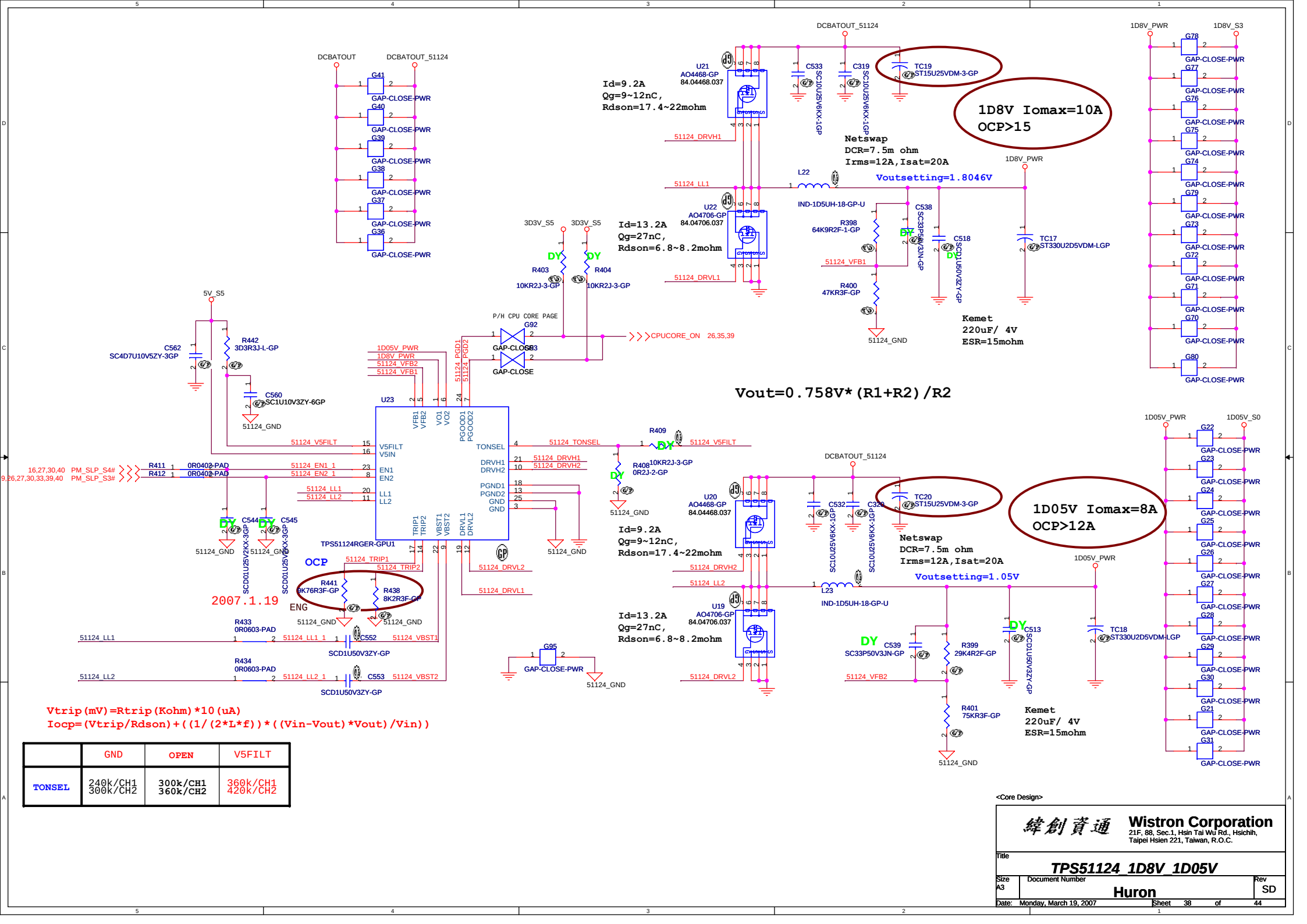




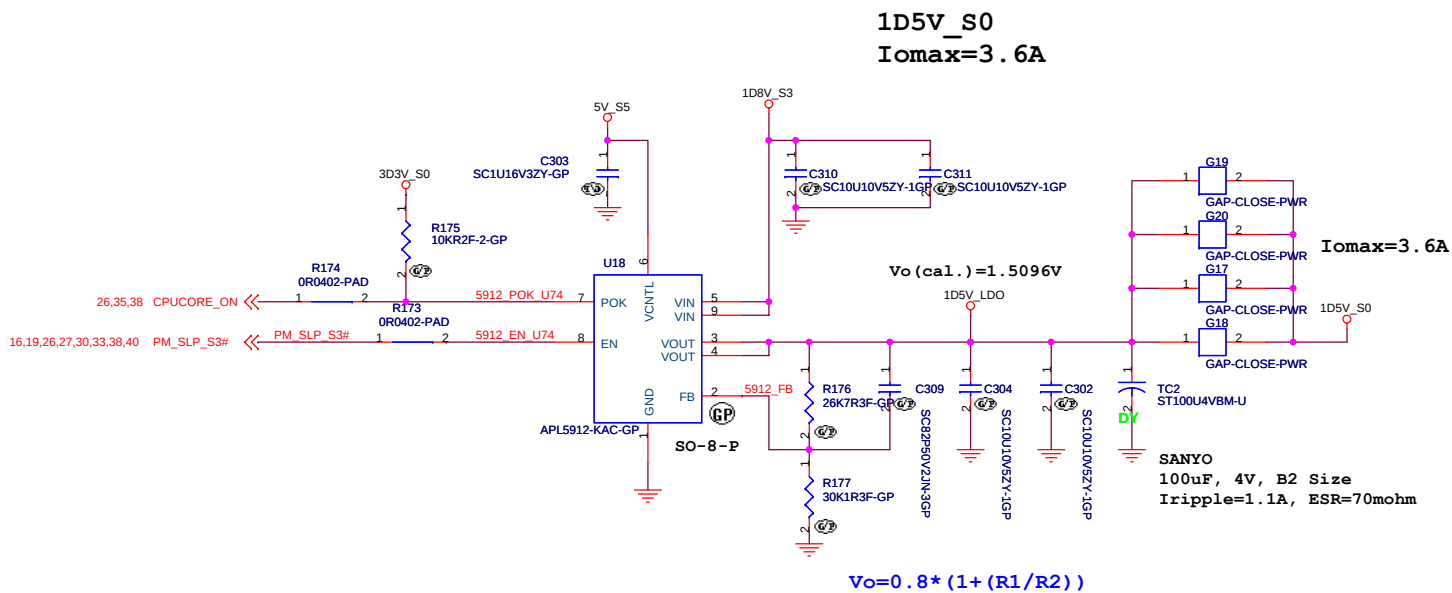
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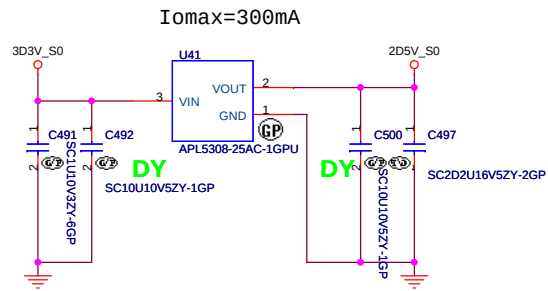
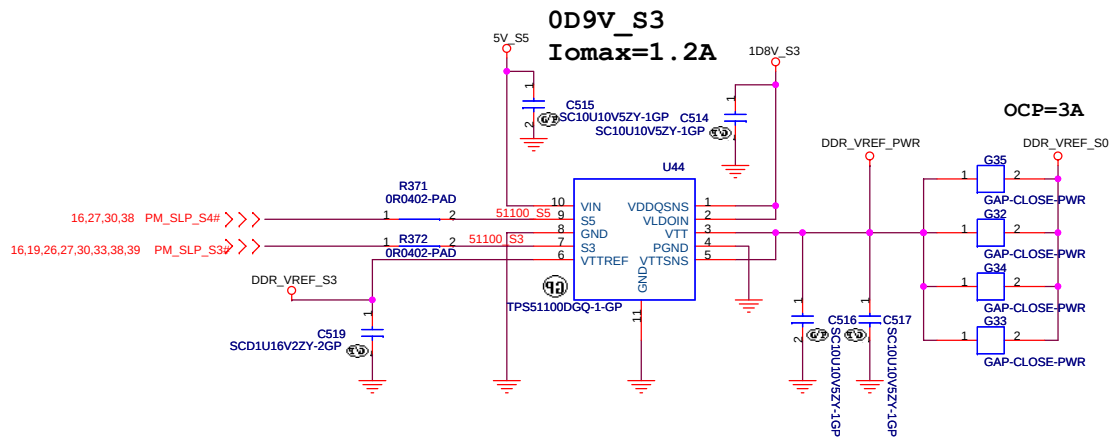


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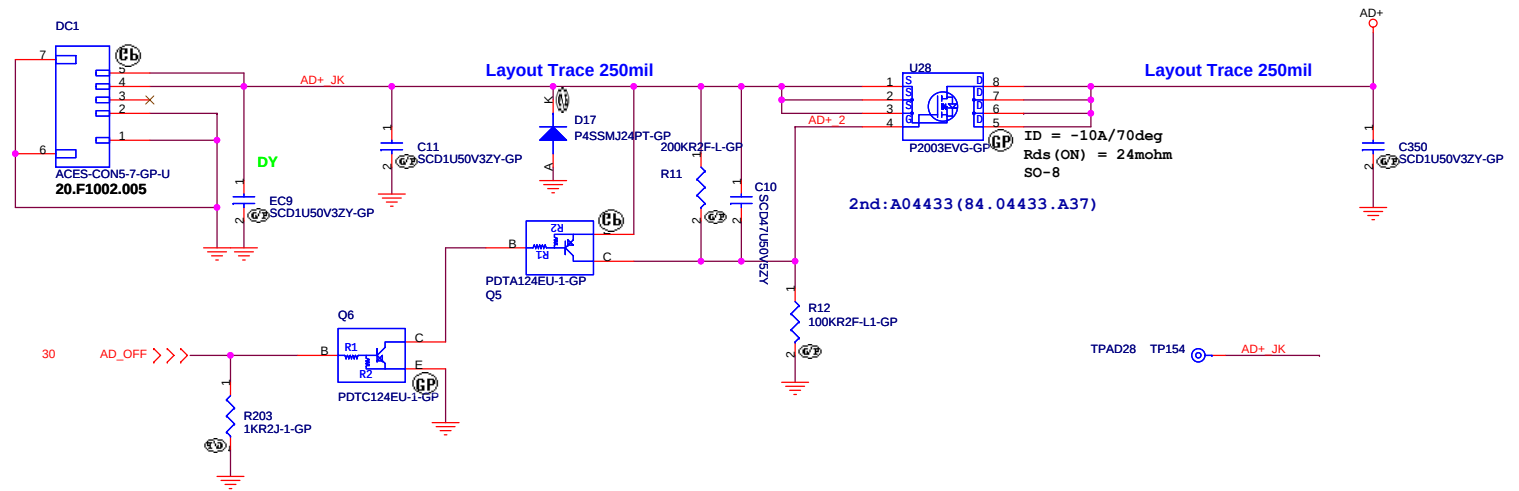
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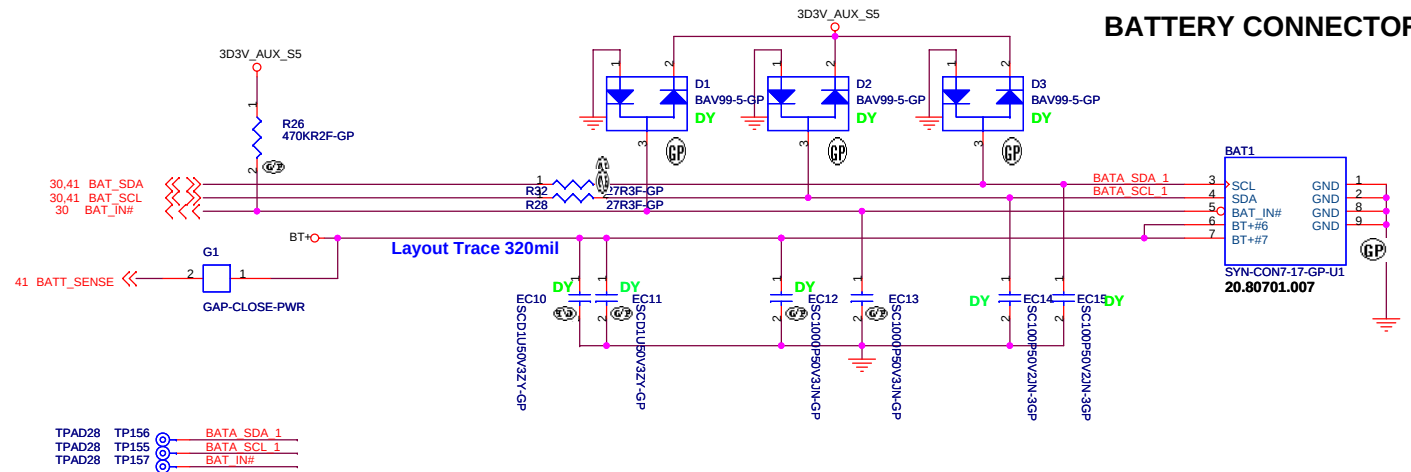
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Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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AD/BATT CONN

Size
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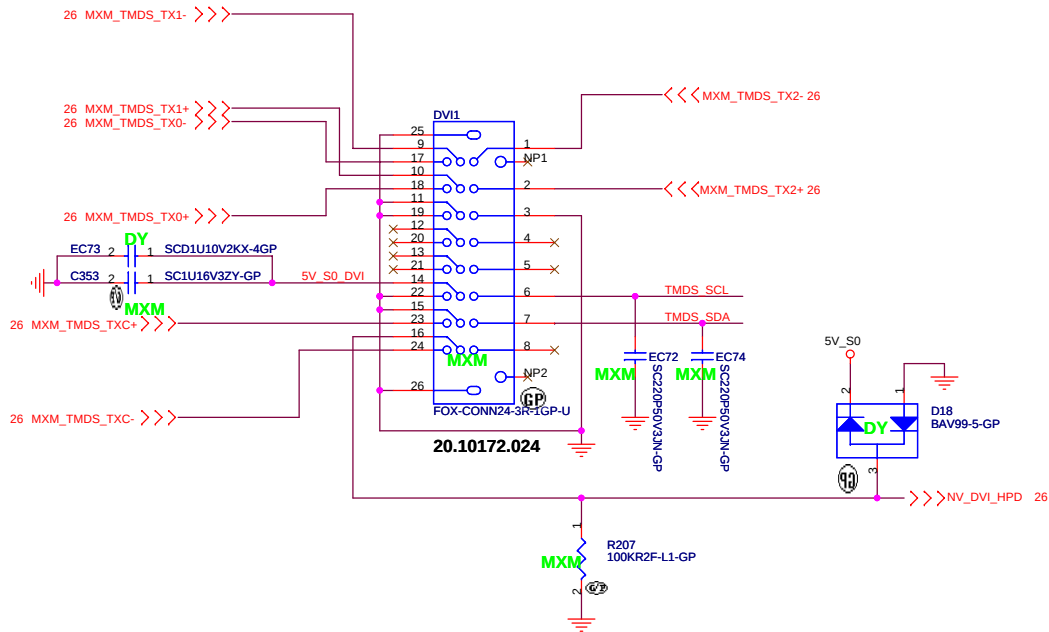
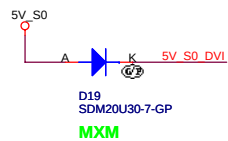
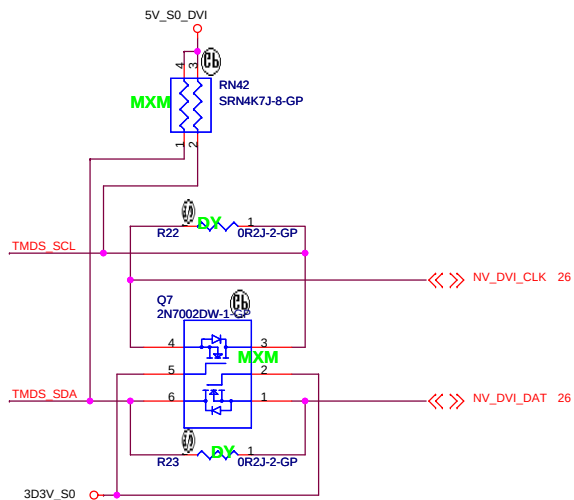
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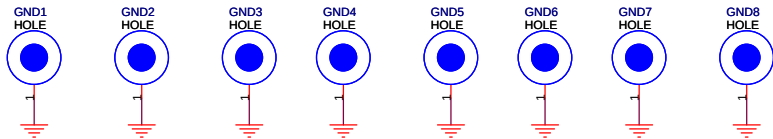
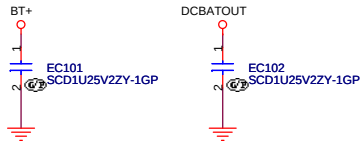
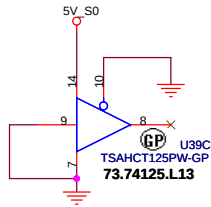
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Spring

