Compal Confidential

Model Name : V4DA2
File Name : LA-A131P
BOM P/N:43

ZZZ1
LA-A131P
DAA00072010

ZZZ2
LS-A131P
DA4001PG010

ZZZ3
LS-A132P
DA600100010

ZZZ4
LS-A133P
DA600101010

ZZZ5
LS-A134P
DA4001PH010

ZZZ6
LS-A135P
DA600102010

ZZZ7
HDMI LOGO
RO0000003HM
45@

Compal Confidential

V4DA2 M/B Schematics Document

Haswell ULT Processor + Lynx Point - LP PCH+AMD Mars

2013-08-05

Rev:1.0

Security Classification	Compal Secret Data		
Issued Date	2012/07/20	Deciphered Date	2013/07/20

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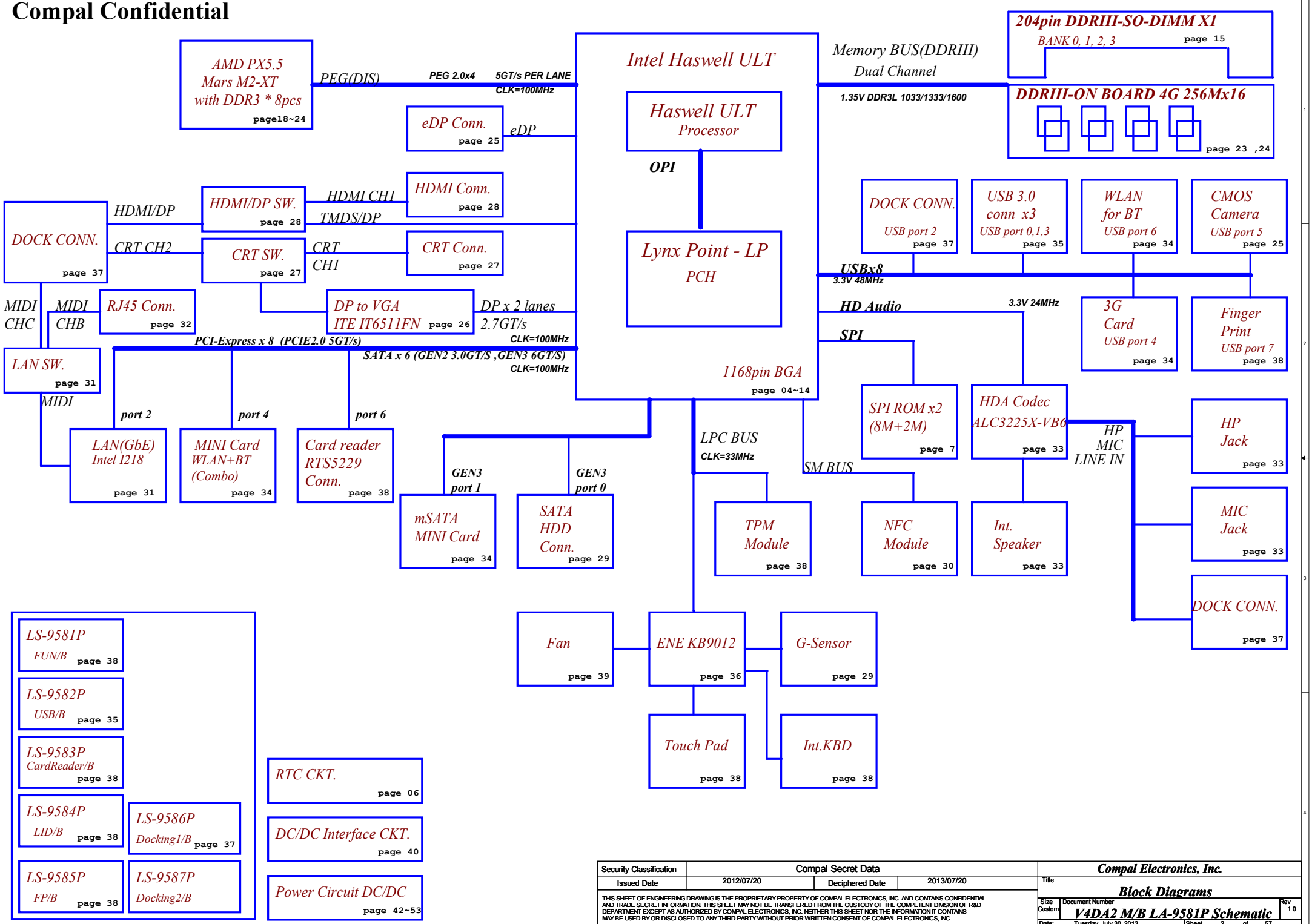
Title: Cover Page

Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0

Date: Monday, August 05, 2013 | Sheet 1 of 57



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Compal Electronics, Inc.			
Title: Block Diagrams			
Size: Custom	Document Number: V4DA2 M/B LA-9581P Schematic		Rev: 1.0
Date: Tuesday, July 30, 2013		Sheet 2 of 57	

Voltage Rails

Power Plane	Description	AC S0	AC S3	AC S4	AC S5	DC S3	DC S4	DC S5
+RTCVCC	RTC power	ON	ON	ON	ON	ON	ON	ON
VIN	Adapter power supply (19V)	N/A	ON	ON	ON	OFF	OFF	OFF
BATT+	Battery power supply (9V or 19V)	N/A	N/A	N/A	N/A	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON	ON	ON	ON	ON
+3VALW	+3VALW always on power rail	ON	ON	ON	ON	ON	ON	ON
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH	ON	ON	ON	ON	ON	ON	ON
+3VM	+3VALW to +3VM power rail for PCH	ON	ON*	ON*	ON*	ON*	ON*	ON*
+1.05VM	+1.05VS_VTT to +1.05VM switched power rail for CPU & PCH	ON	ON*	ON*	ON*	ON*	ON*	ON*
+1.05VS_VTT	+1.05VSP to +1.05VS_VTT switched power rail for CPU & PCH	ON	OFF	OFF	OFF	OFF	OFF	OFF
+1.5VS	+1.5VSP to +1.5VS switched power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF
+1.35V	+1.35VP to +1.35V switched power rail for DDR terminator	ON	ON	OFF	OFF	ON	OFF	OFF
+0.675VS	+0.675VSP to +0.675VS switched power rail for DDR terminator	ON	OFF	OFF	OFF	OFF	OFF	OFF
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU power rail	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+1.5VSDGPU	+1.5V to +1.5VSDGPU switched power rail for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+1.8VSDGPU	+1.8VSDGPU switched power rail for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+0.95VSDGPU	+1.8VSDGPU switched power rail for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+3V_LAN	LAN CHIP POWER RAIL	ON*	ON*	ON*	OFF	OFF	OFF	OFF
+3VS_WLAN	WLAN MODULE POWER RAIL	ON*	ON*	ON*	OFF	OFF	OFF	OFF
+USB3_VCCA	USB Charger PORT0 & PORT9 POWER POWER RAIL	ON	ON	ON	ON	ON*	ON*	ON*

Note : ON* WILL DEPEND ON SLP_A# TO TURN ON OR OFF(ME FIRMWARE CONTROL)

Note : ON* WILL DEPEND ON BATTERY CAPACITY TO TURN ON OR OFF

Note : ON** Depend on Optimus ON/OFF.

Note : ON* Depend on LAN wake SPEC

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
On Board Thermal Senser(CPU)	1001_101xb
On Board Thermal Senser(GPU)	1001_100xb
PCH	0100_1100b
	0100_1011b

PCH SM Bus address

Device			Address	
ChannelA	DIMM0	A0	1010 000Xb	On Board RAM(SPD)
ChannelB	DIMM0	A4	1010 010Xb	JDIMM1(SPD)
G-sensor			0011 000xb	

PCH SM Bus0 address

Device	Address
LAN	1100_100xb
NFC	0010_100xb

CPU BOM Config

0.8G SA000067060 (S IC CL8064701325206 QDJB B1 0.8G BGA)

1.2G SA00006G120 (S IC CL8064701325204 QDJ9 B1 1.2G BGA)

GPU BOM Config

MARS-XT-M2 SA000061J10 (S IC 216-0842000 A0 MARS XT M2 FCBGA 0FA)

VRAM BOM Config

HYNIX	128*16	SA00003YO90(S IC D3 128M16 H5TQ2G63DFR-11C FBGA ABO!)	HYNIX0@
HYNIX	128*16	SA00006H430(S IC D3 128M16 H5TC2G63FFR-11C FBGA ABO!)	HYNIX1@

RAM BOM Config

ELPDIA	256*16	SA000059110(S IC D3 256M16 EDJ4216EBBG-DJ-F ABO!)	ELP0@
ELPDIA	256*16	SA00005HT50(S IC 256MX16/1600 EDJ4216EFBG-GN-F FBGA 96P ABO !)	ELP1@

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S0(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

USB Port Table

USB 2.0	Port	USB Port
EHCI	0	USB Port 3.0 (I/O board)
	1	USB port 3.0 (Left side)
	2	DOCK USB3.0
	3	USB Port 3.0 (I/O board)
	4	Mini Card(3G)
	5	Camera
	6	Mini Card(WLAN+BT)
	7	Finger Print

USB 3.0	Port	
XHCI	1	USB Port 3.0 (I/O board)
	2	USB3 (Left side)

PCIE Table

Port	PCI Express Port
1	USB 3.0 DOCK
2	USB 3.0 (I/O board)
3	LAN
4	WLAN
5-L0	VGA
5-L1	
5-L2	
5-L3	
6-L0	CardReader

BTO Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
UMA Only	UMA@
DISCRETE	VGA@
CPU	
CPU	
CPU	
DRAM ELPIDA0	ELP0@
DRAM HYNIXR0	HYNIXR0@
NFC Function	NFC@
3G Function	3G@
VPRO Function	VPRO@
NO VPRO Function	NOVPRO@
EMI SOLUTION	EMI@
UMA Part Count	PC@
VGA Part Count	VGAPC@
ESD SOLUTION	ESD@
VRAM HYNIX0	HYNIX0@
VRAM HYNIX1	HYNIX1@

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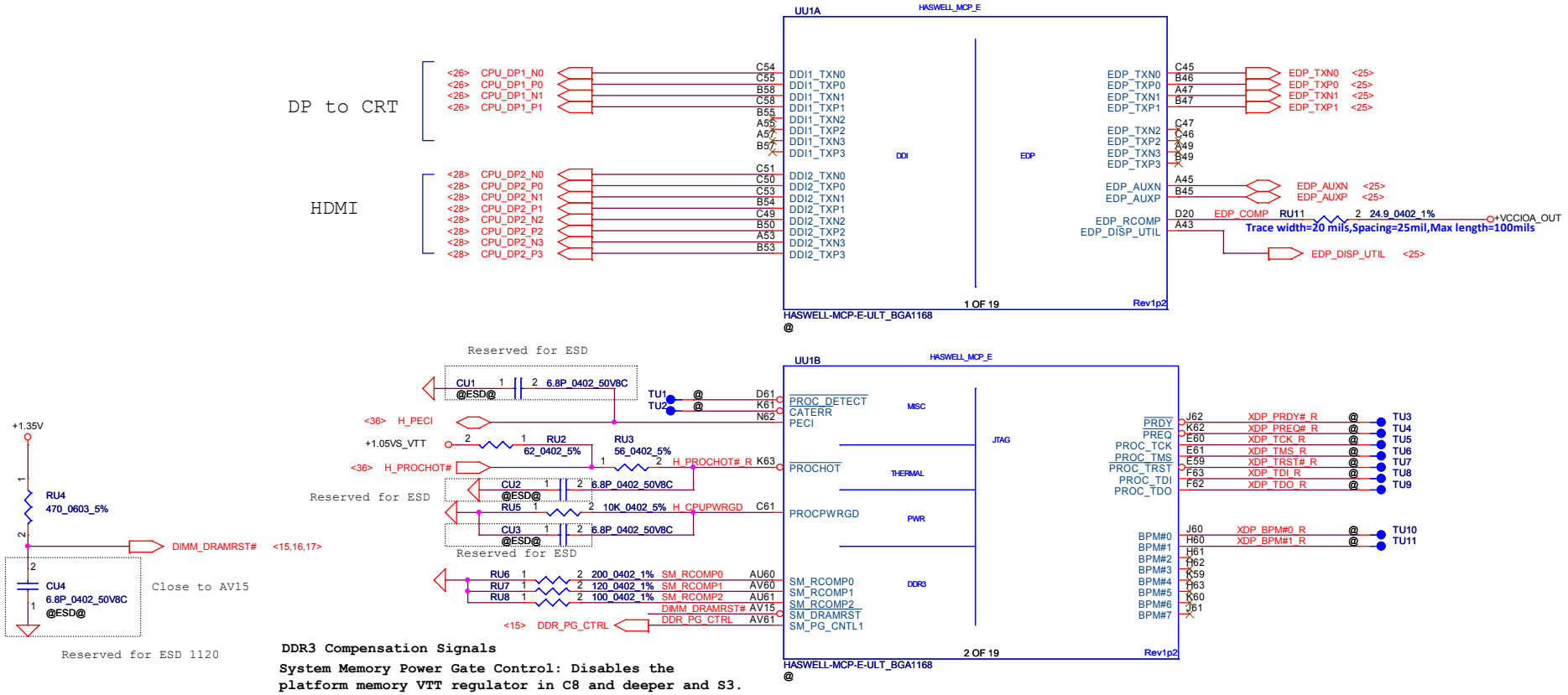
Title: Notes List

Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0

Date: Tuesday, July 30, 2013 | Sheet 3 of 57



UU1 CPU_SR16L SR16L@ SA00006ST80
UU1 CPU_QDJB B1 QDJB@ SA000067060
UU1 CPU_QDJ9 B1 QDJ9@ SA00006G120
UU1 CPU_QEVD QEVD@ SA00006SL20

UU1 CPU_SR16H SR16H@ SA00006SS70
UU1 CPU_SR1ED SR1ED@ SA000072R50
UU1 CPU_SR1EA SR1EA@ SA000072S50
UU1 CPU_SR16Z SR16Z@ SA00006SLB0

UU1 CPU_SR16H SR16H@ SA00006SS70
UU1 CPU_QEAG QEAG@ SA000072R30
UU1 CPU_SR170 SR170@ SA00006SMB0
UU1 CPU_SR16L SR16L@ SA00006ST80

UU1 CPU_SR16Q SR16Q@ SA00006SX70

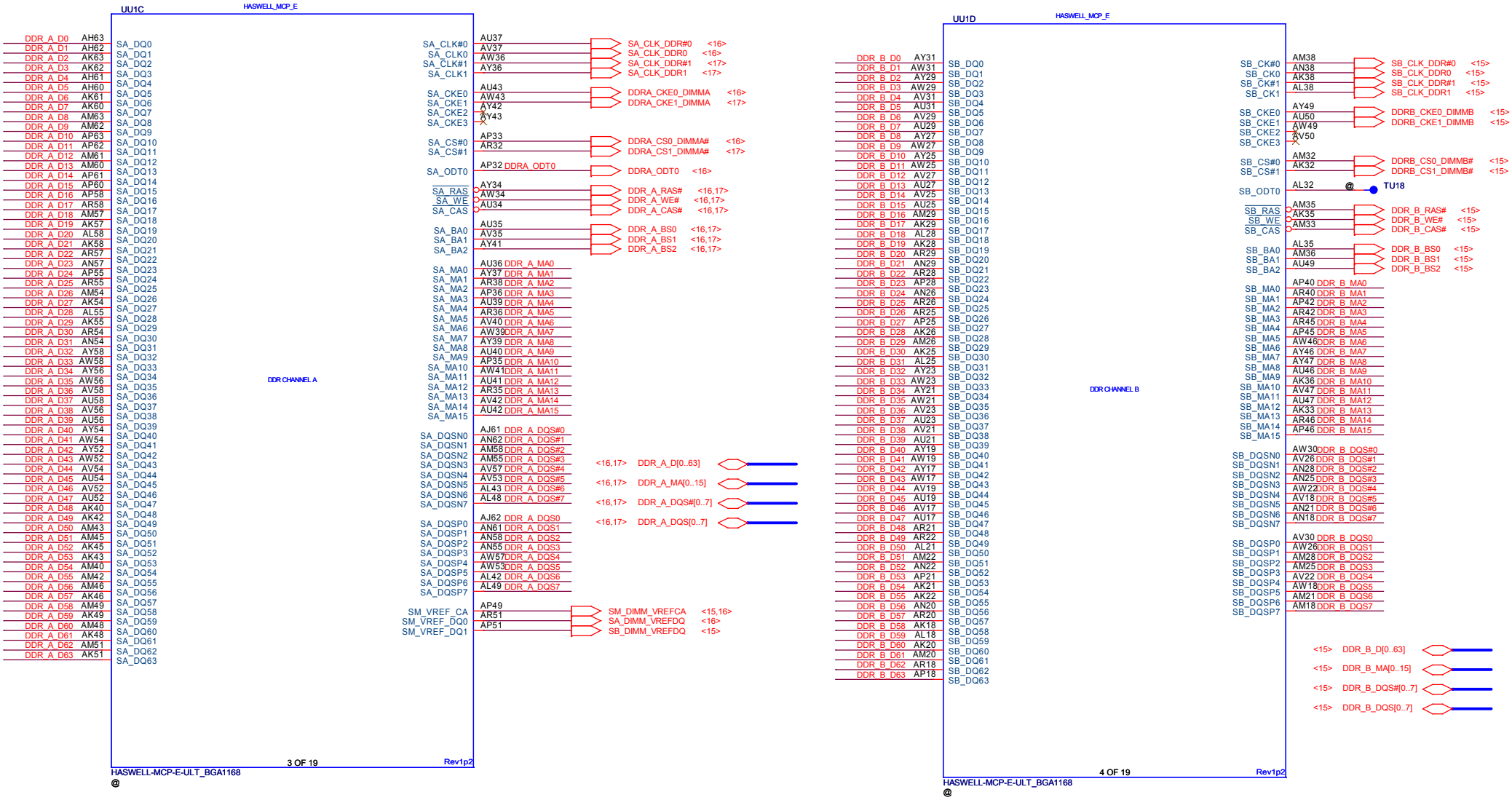
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.

Title: HSW MCP(1/11) DDI,MSIC,XDP

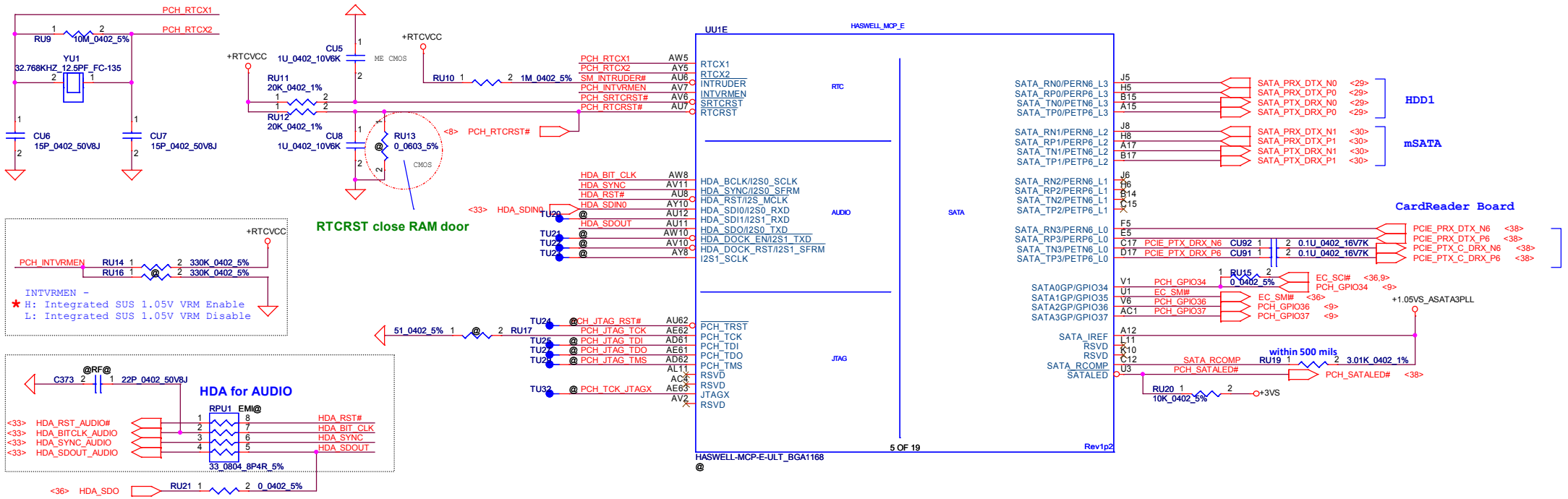
Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0

Date: Monday, August 05, 2013 | Sheet 4 of 57



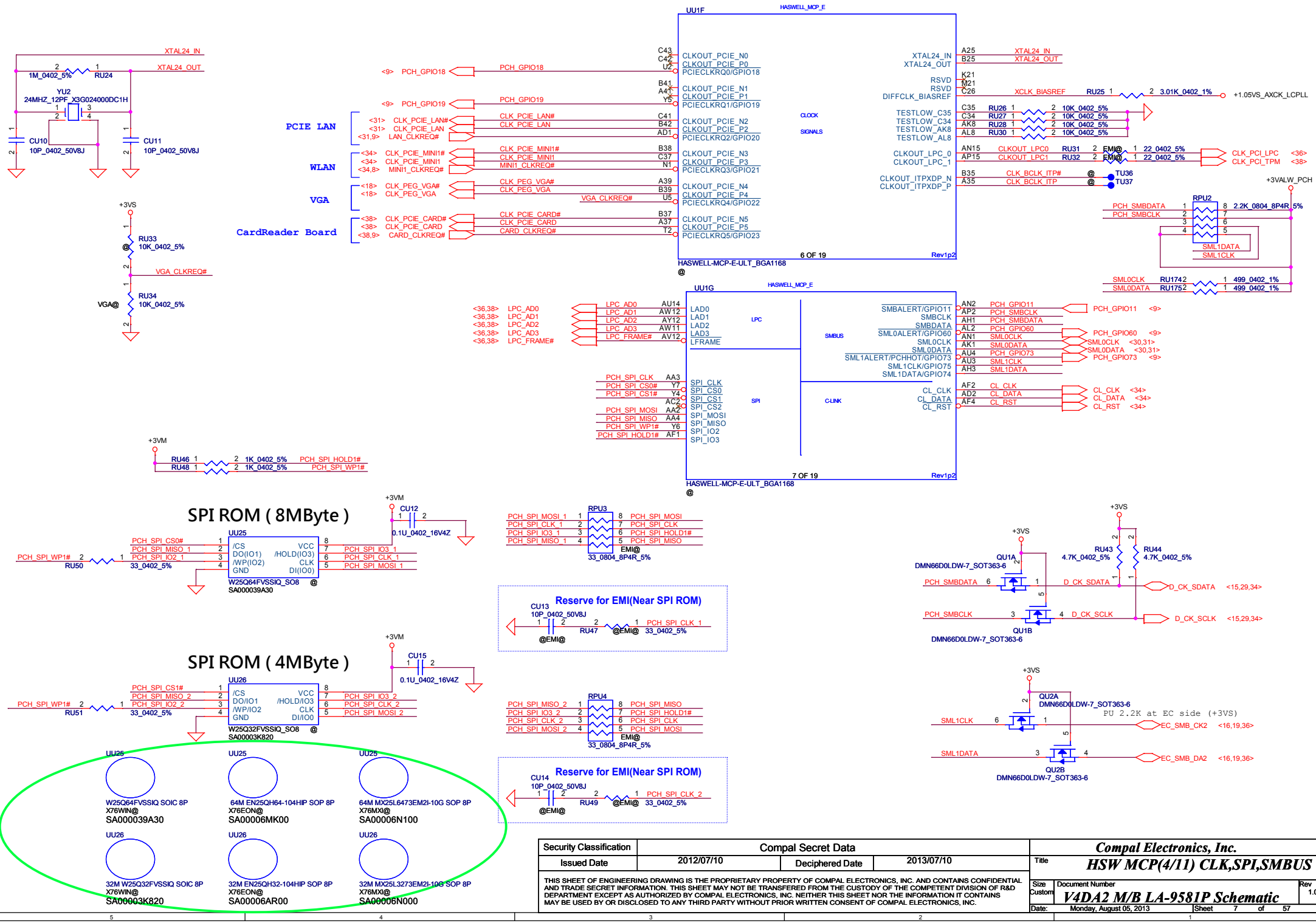
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.	
Title	HSW MCP(2/11) DDRIII
Size: Custom	Document Number: V4DA2 M/B LA-9581P Schematic
Rev	1.0
Date: Tuesday, July 30, 2013	Sheet 5 of 57



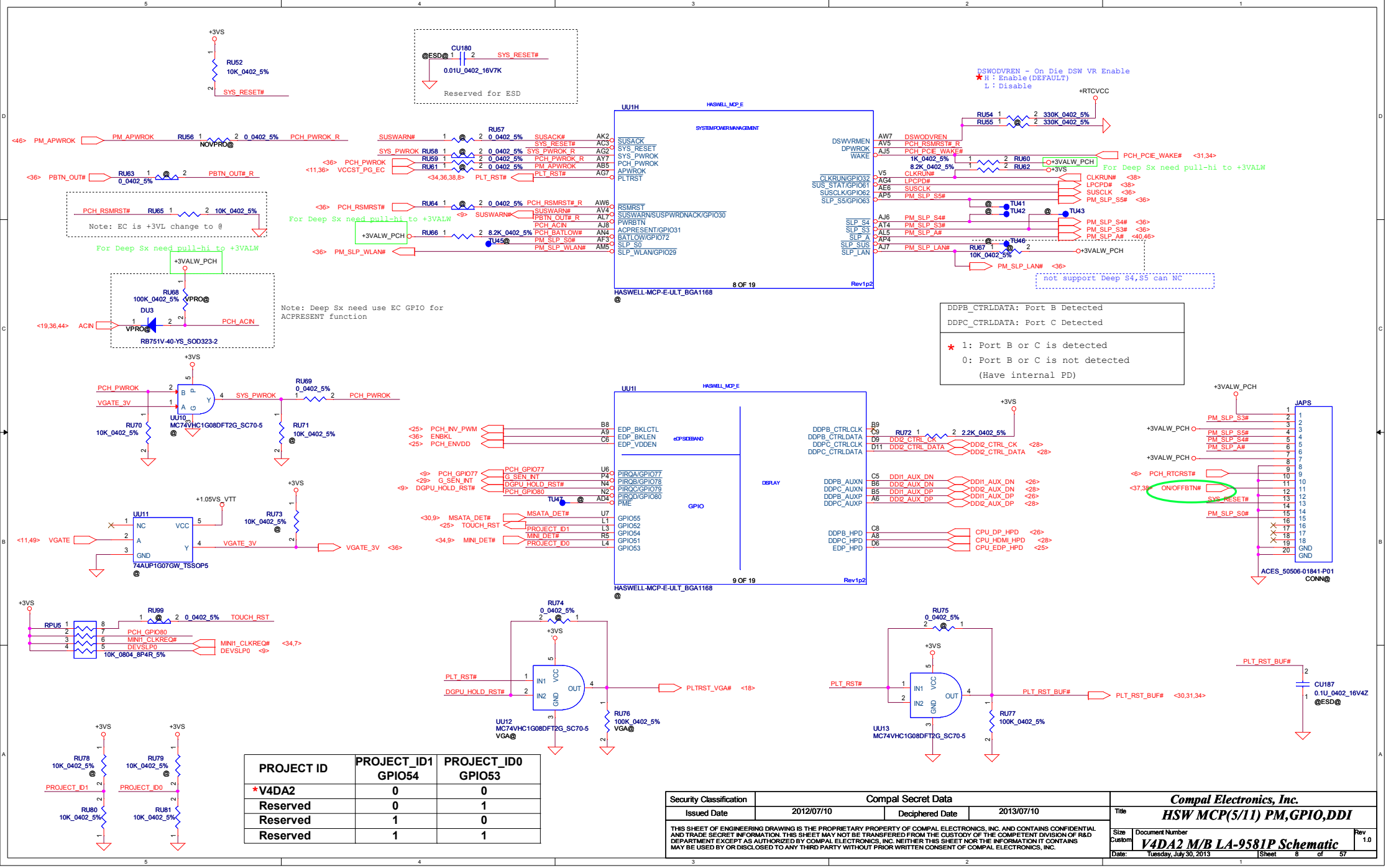
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.			
Title	HSW MCP(3/11) RTC,SATA,XDP		
Size: Custom	Document Number: V4DA2 M/B LA-9581P Schematic		Rev: 1.0
Date: Thursday, August 01, 2013	Sheet 6 of 57		



Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

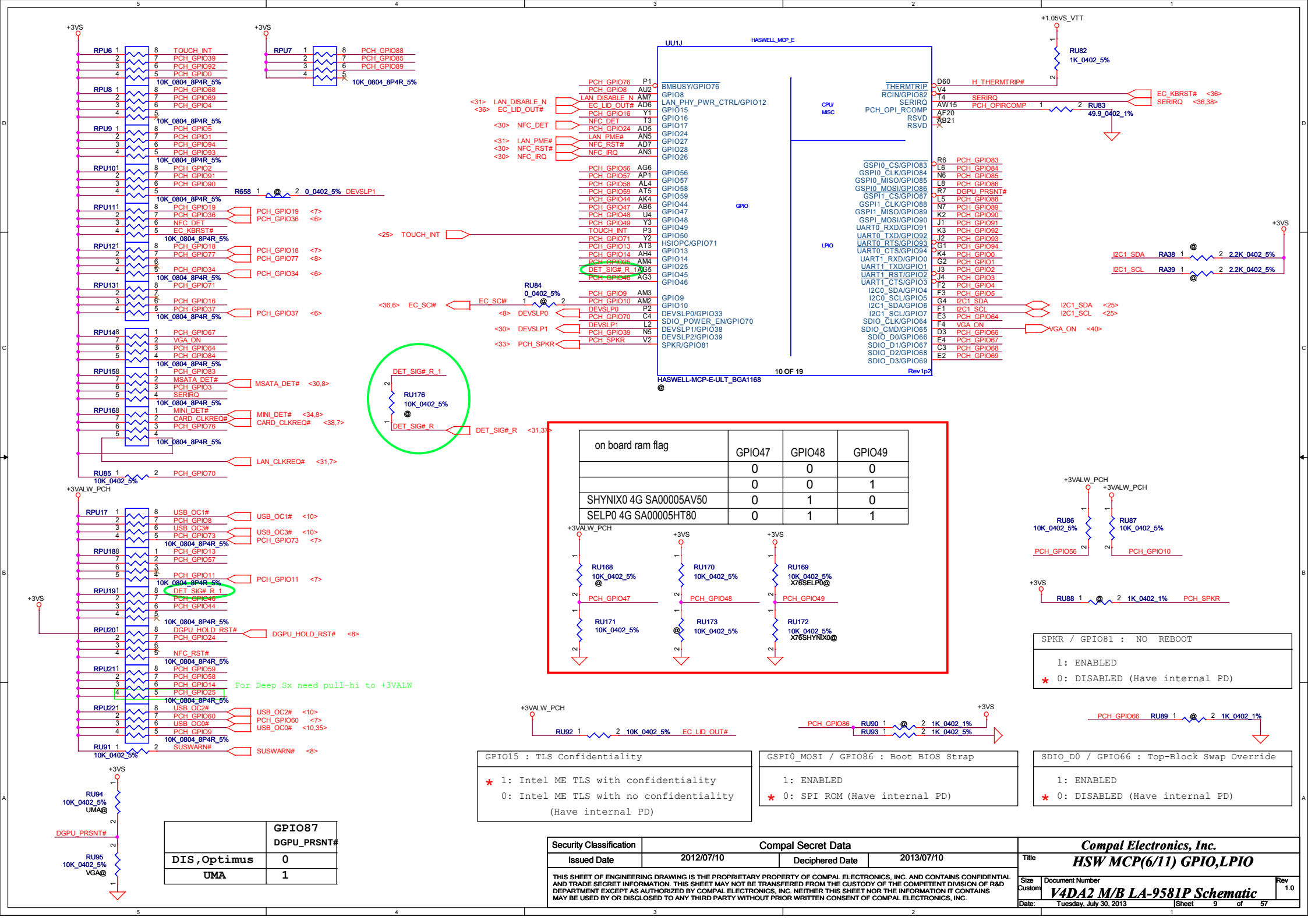
Compal Electronics, Inc.			
Title	HSW MCP(4/11) CLK,SPI,SMBUS		
Size: Custom	Document Number: V4DA2 M/B LA-9581P Schematic		Rev: 1.0
Date: Monday, August 05, 2013	Sheet 7 of 57		



PROJECT ID	PROJECT_ID1 GPIO54	PROJECT_ID0 GPIO53
*V4DA2	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.	
Title	HSW MCP(5/11) PM,GPIO,DDI
Size: Custom	Document Number: V4DA2 M/B LA-9581P Schematic
Rev	1.0
Date: Tuesday, July 30, 2013	Sheet 8 of 57



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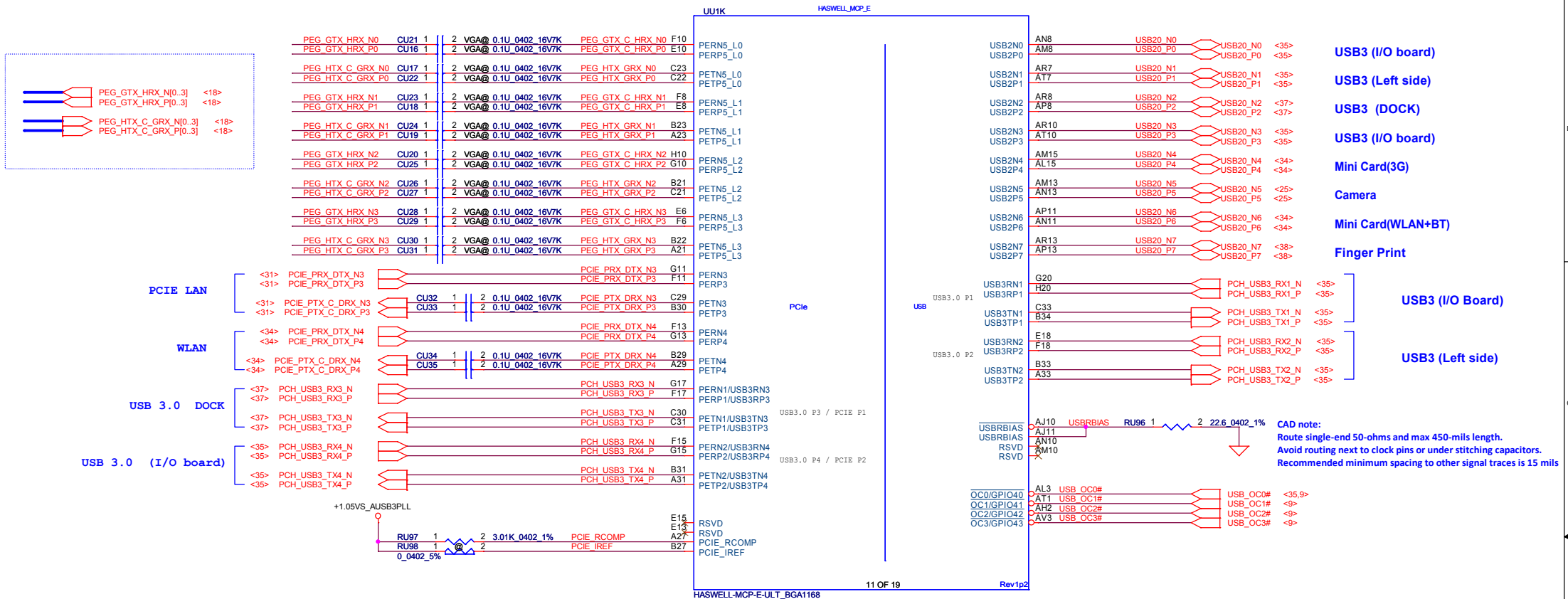

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Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.	
Title	HSW MCP(7/11) PCIE,USB
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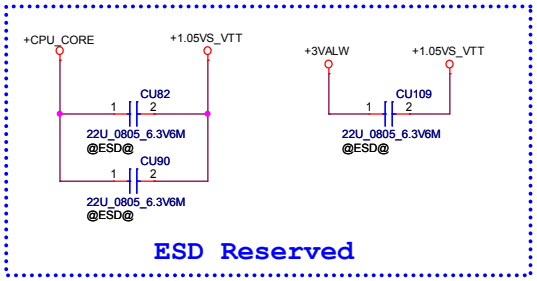
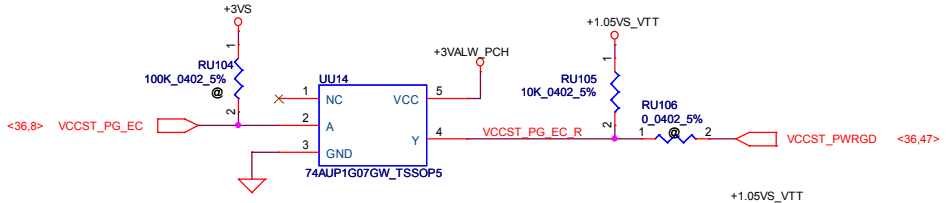
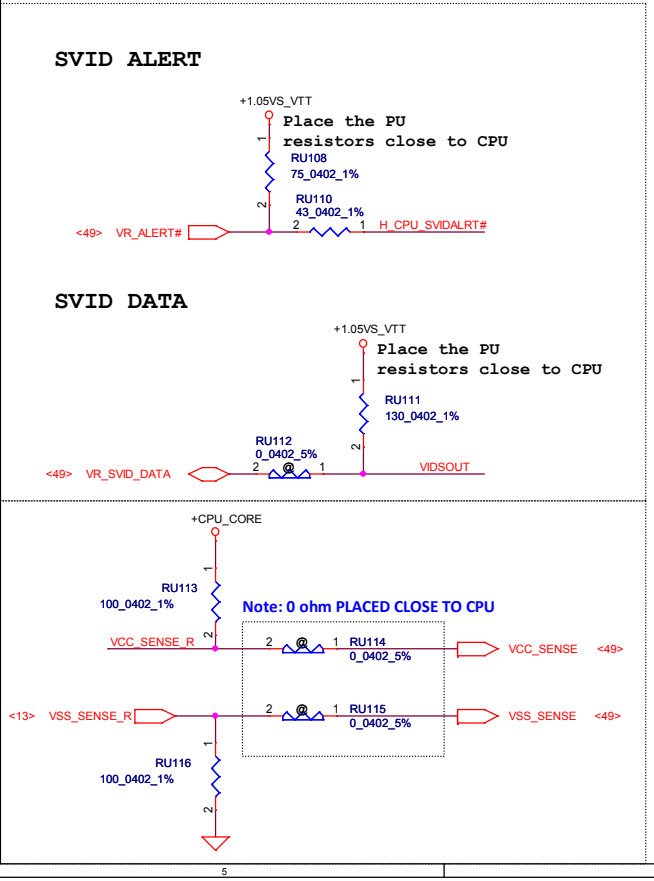
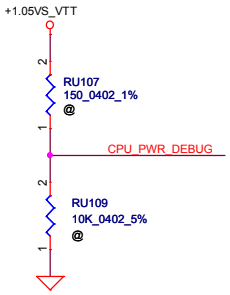
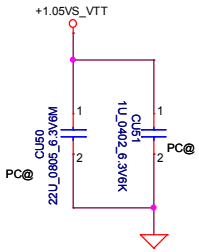
Rev	1.0
Date:	Tuesday, July 30, 2013
Sheet	10 of 57

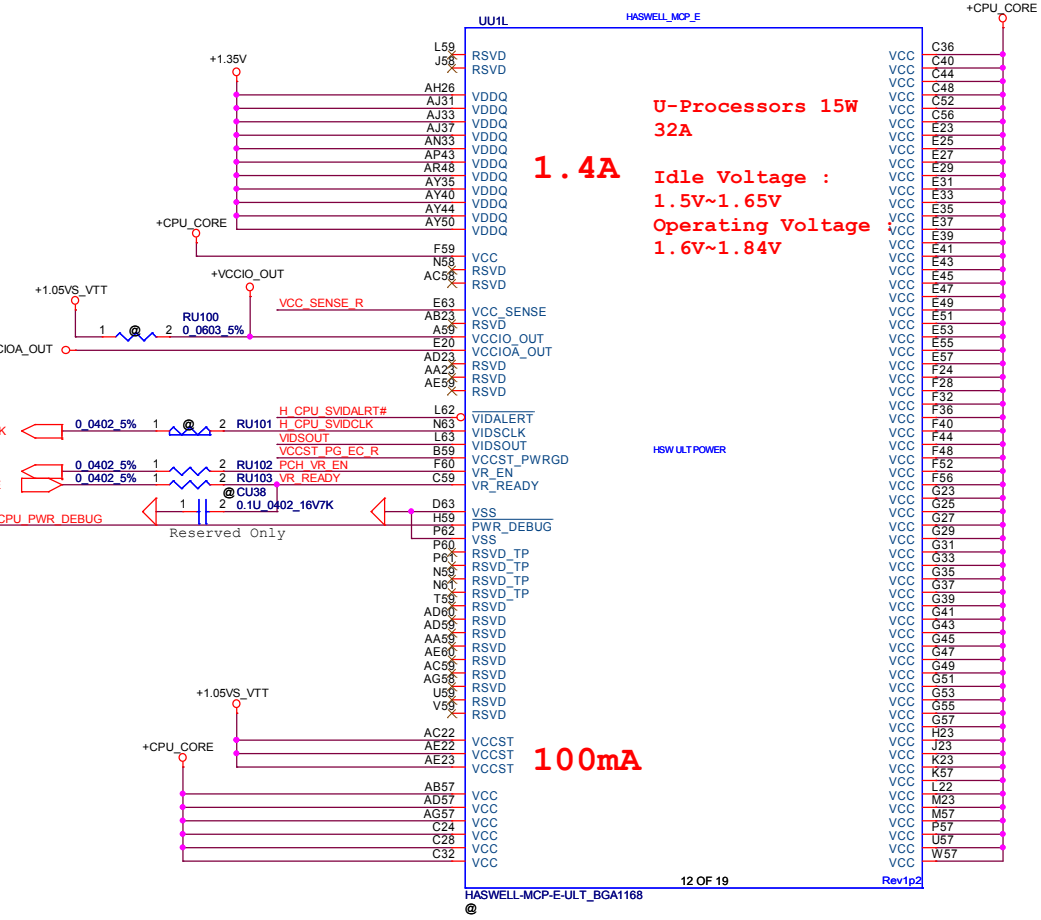


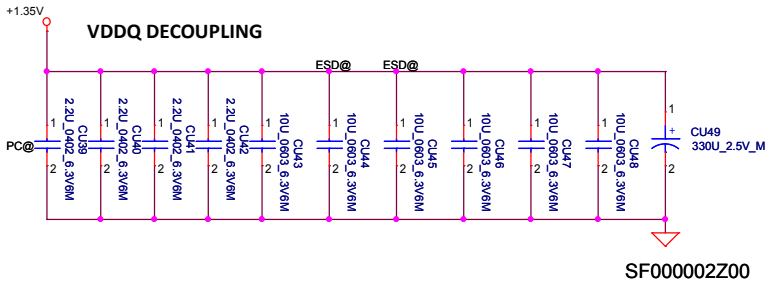












+1.35V : 470UF/2V/7343 *2
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

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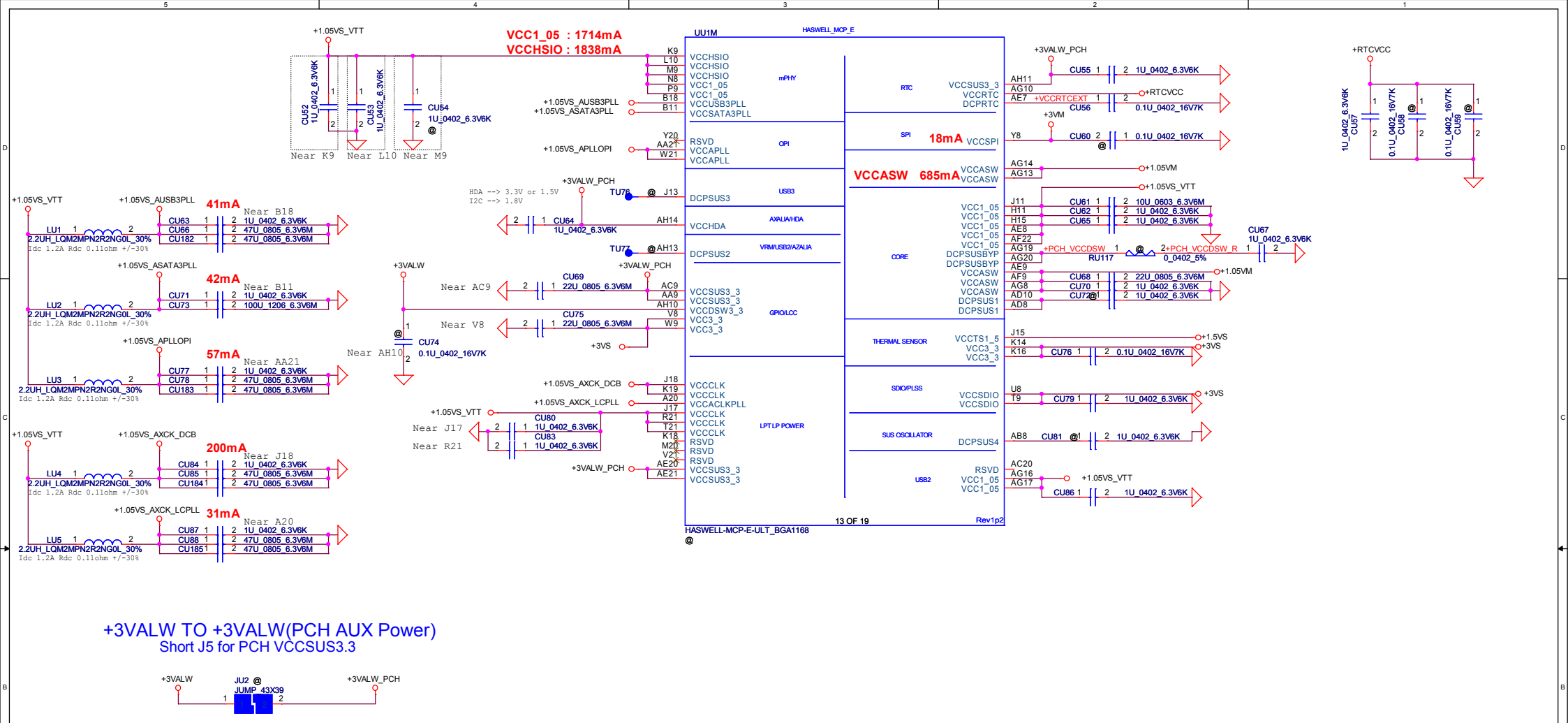
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.			
Title	HSW MCP(8/11) Power		
Size: Custom	Document Number: V4DA2 M/B LA-9581P Schematic		Rev: 1.0
Date: Tuesday, July 30, 2013	Sheet 11 of 57		



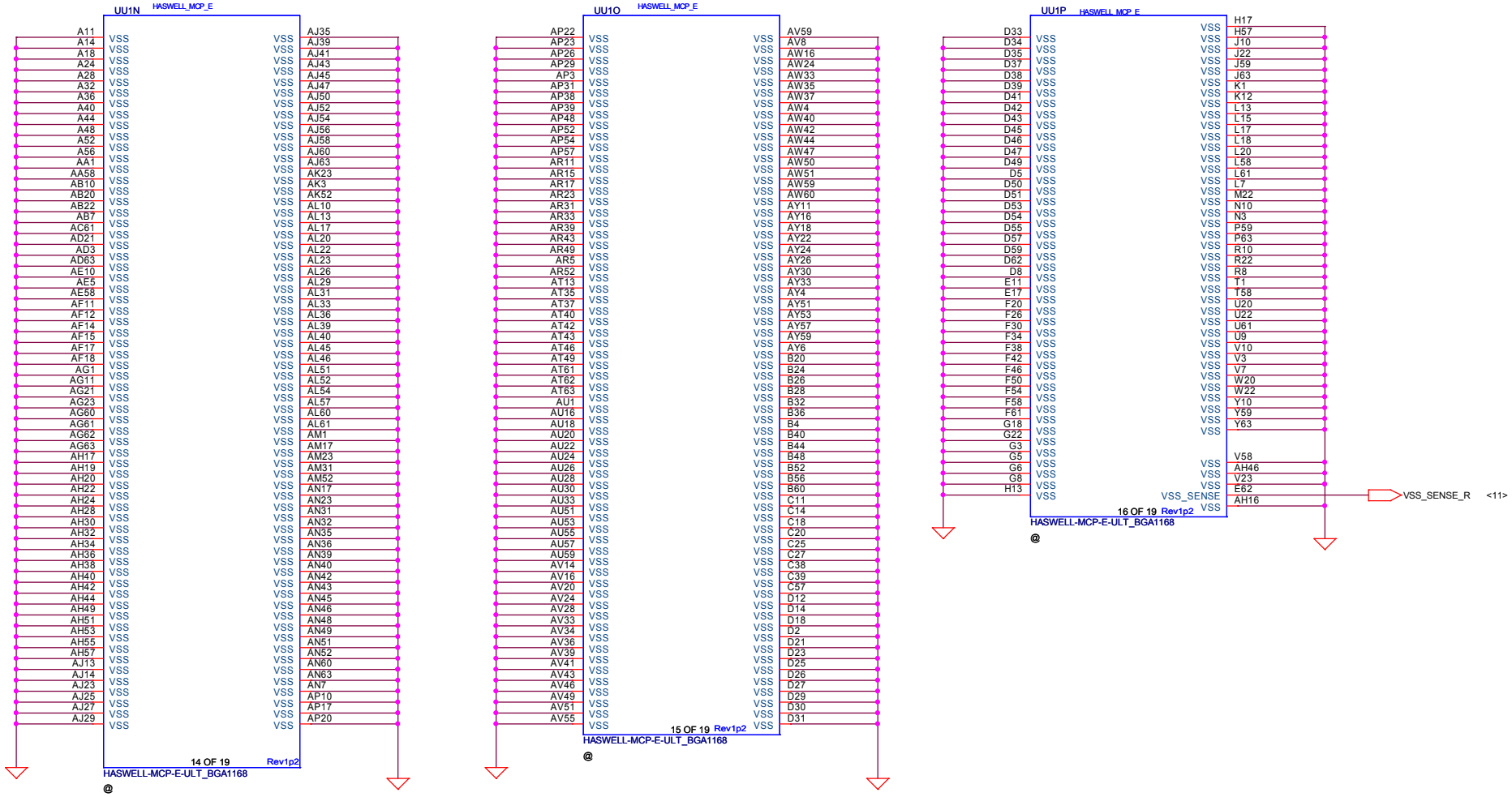
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.

Title: HSW MCP(9/11) Power

Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0

Date: Tuesday, July 30, 2013 | Sheet 12 of 57



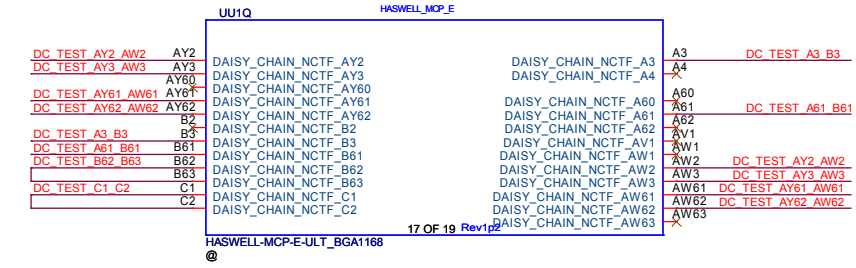
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

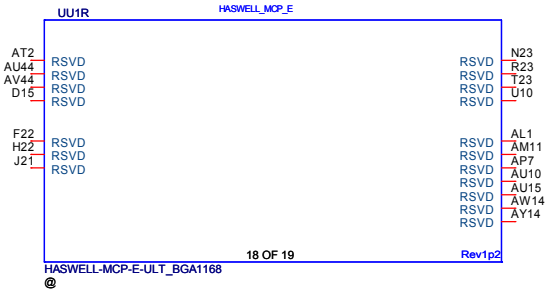
Compal Electronics, Inc.

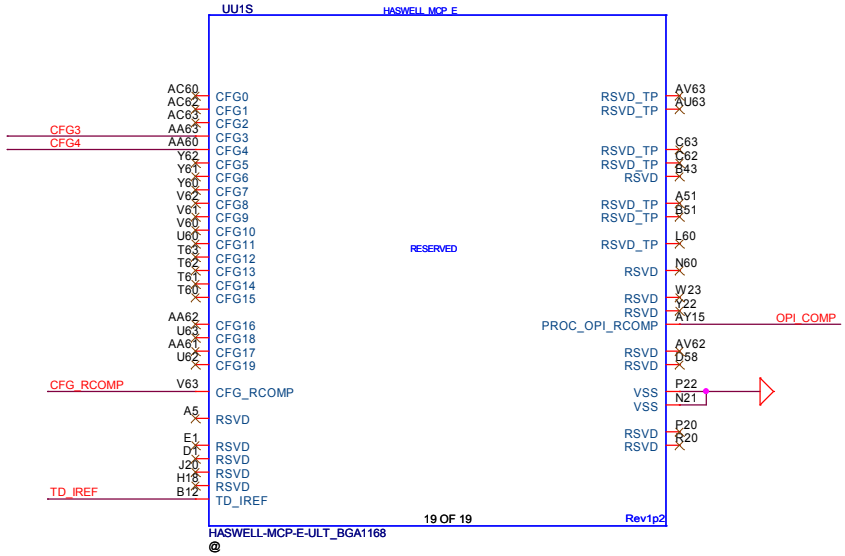
Title: HSW MCP(10/11) GND

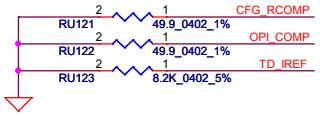
Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0

Date: Tuesday, July 30, 2013 | Sheet 13 of 57

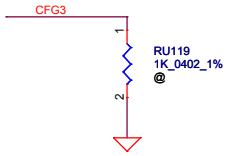




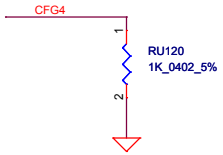




CFG Straps for Processor



Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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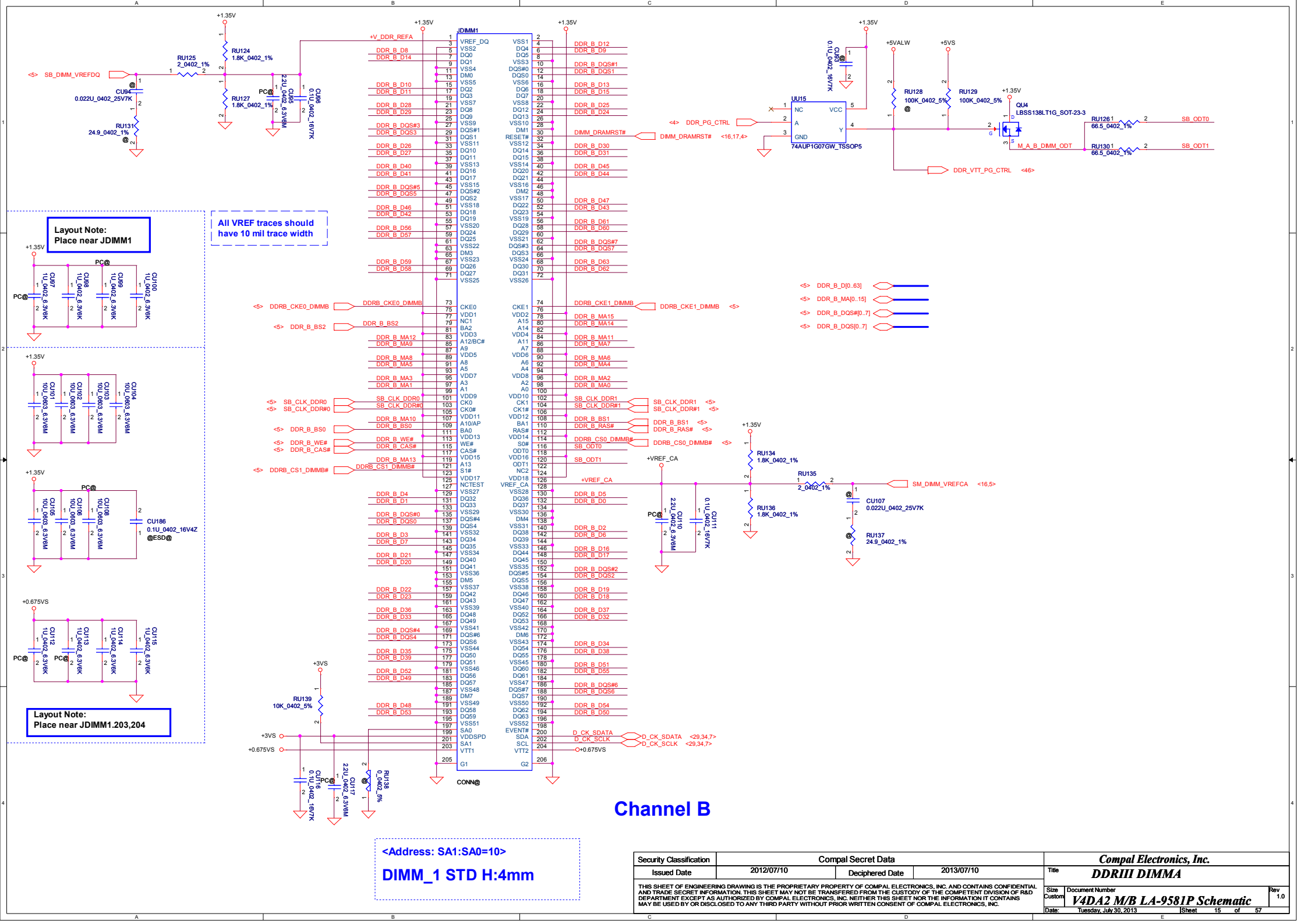
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.			
Title	HSW MCP(11/11) RSVD		
Size: Custom	Document Number: V4DA2 M/B LA-9581P Schematic		Rev: 1.0
Date: Tuesday, July 30, 2013	Sheet 14 of 57		



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Issued Date	2012/07/10	Deciphered Date	2013/07/10

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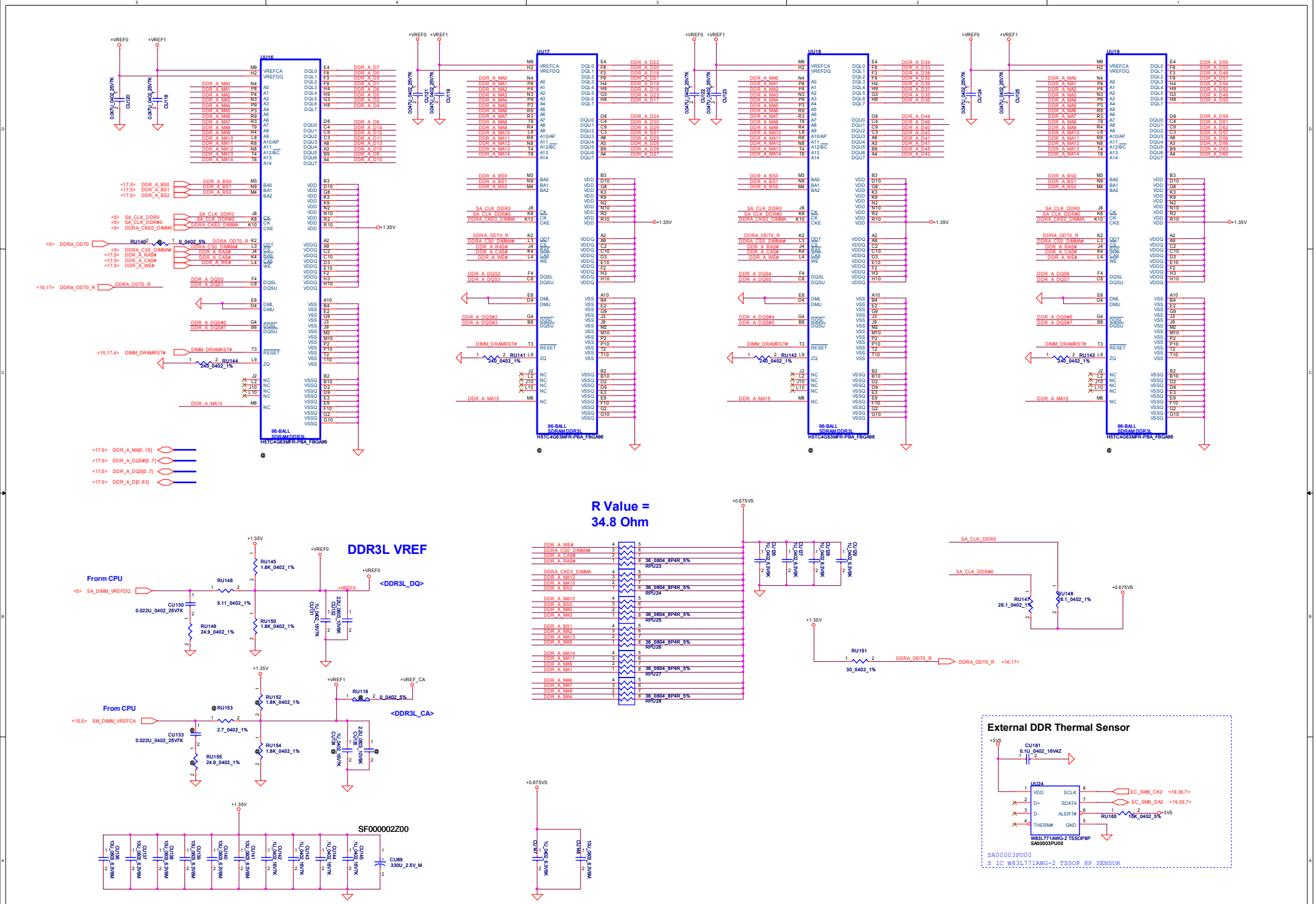
Title	DDRIII DIMMA		
Size: Custom	Document Number: V4DA2 M/B LA-9581P Schematic		Rev: 1.0
Date: Tuesday, July 30, 2013		Sheet 15 of 57	



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Issued Date	2010/04/26	Deciphered Date	2012/03/29

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Title: **DDRIII ON BOARD CHIPS**

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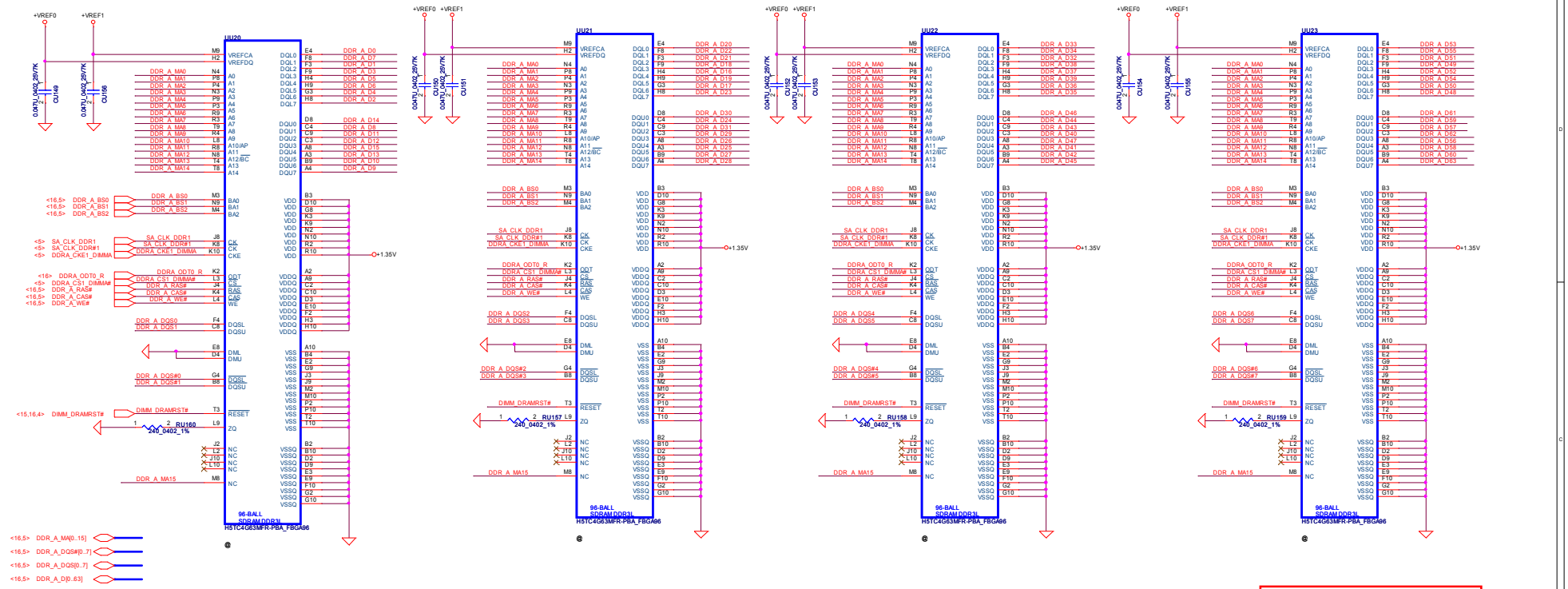
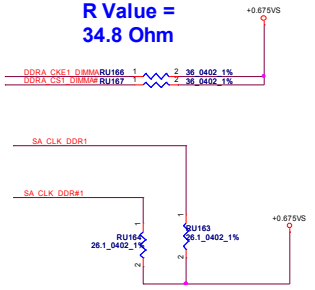
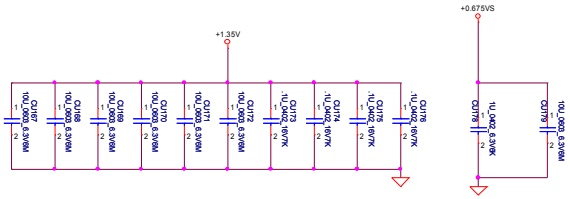
Custom		1.0

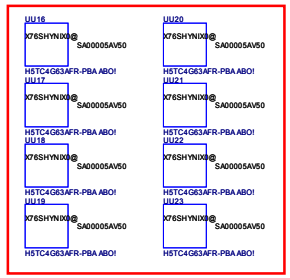
Date: Tuesday, July 30, 2013 Sheet 18 of 57

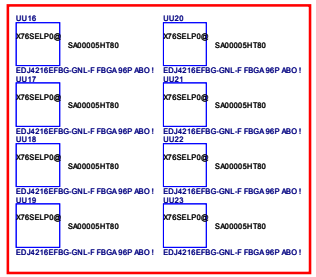


R Value = 34.8 Ohm









Security Classification	Compal Secret Data		
Issued Date	2010/04/26	Deciphered Date	2012/03/29

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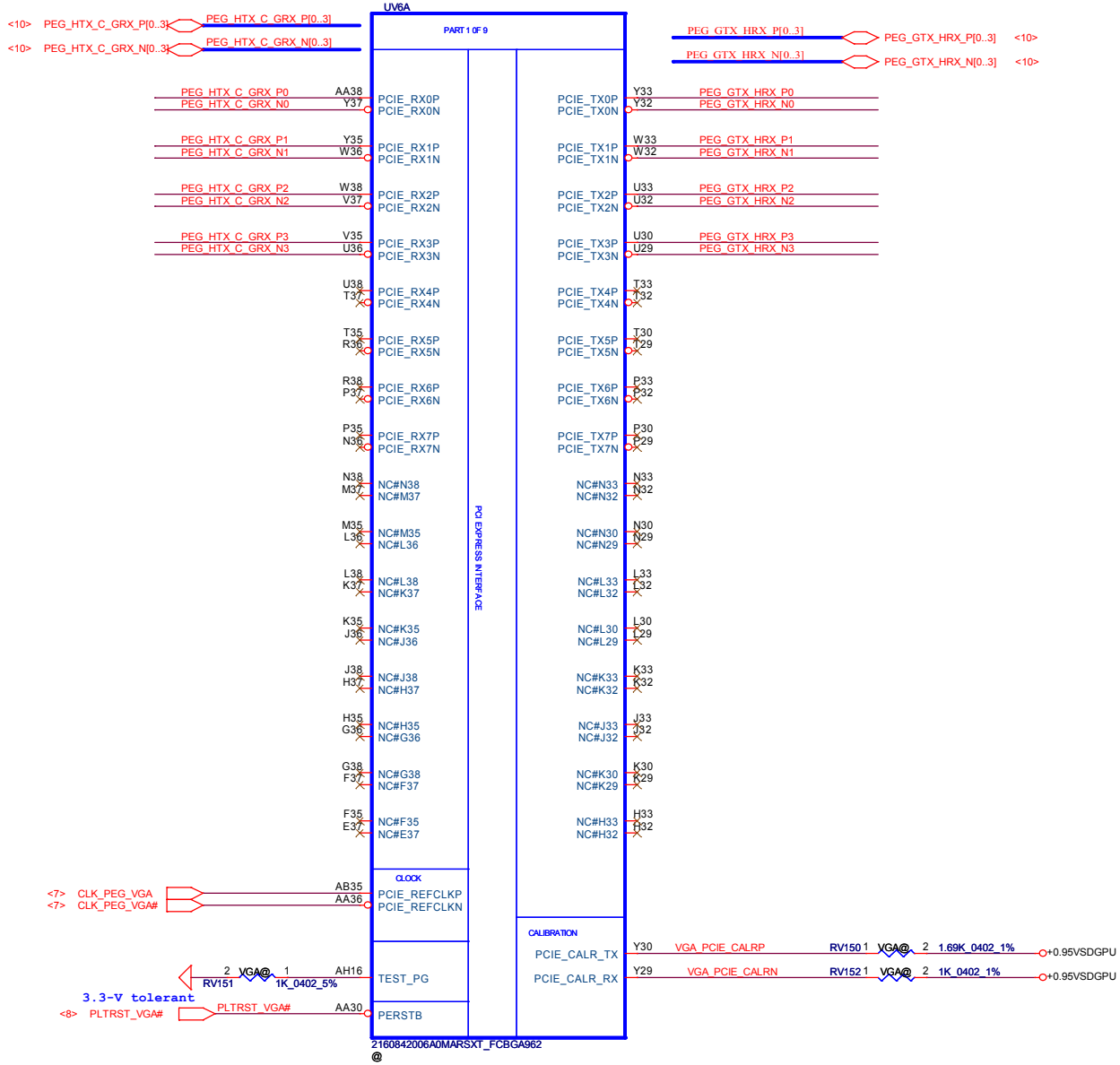
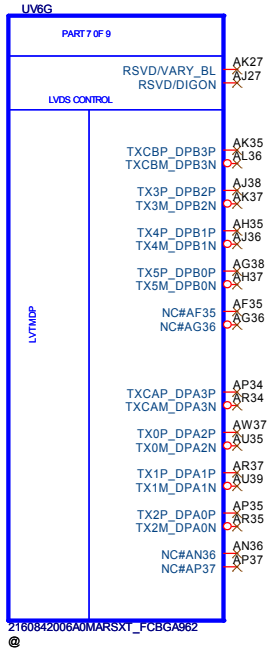
Title	DDRIII ON BOARD CHIPS		
Size	Document Number		Rev
Custom			1.0
Date:	Tuesday, July 30, 2013	Sheet	17 of 57

GFX PCIE LANE REVERSAL





UV6
SUN_XT_M2_962P
SUN@
SA00006G600

UV6
MARS_XT_M2_962P
MARS@
SA000061J20

Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.

Title: MARS-Pro_PCIE

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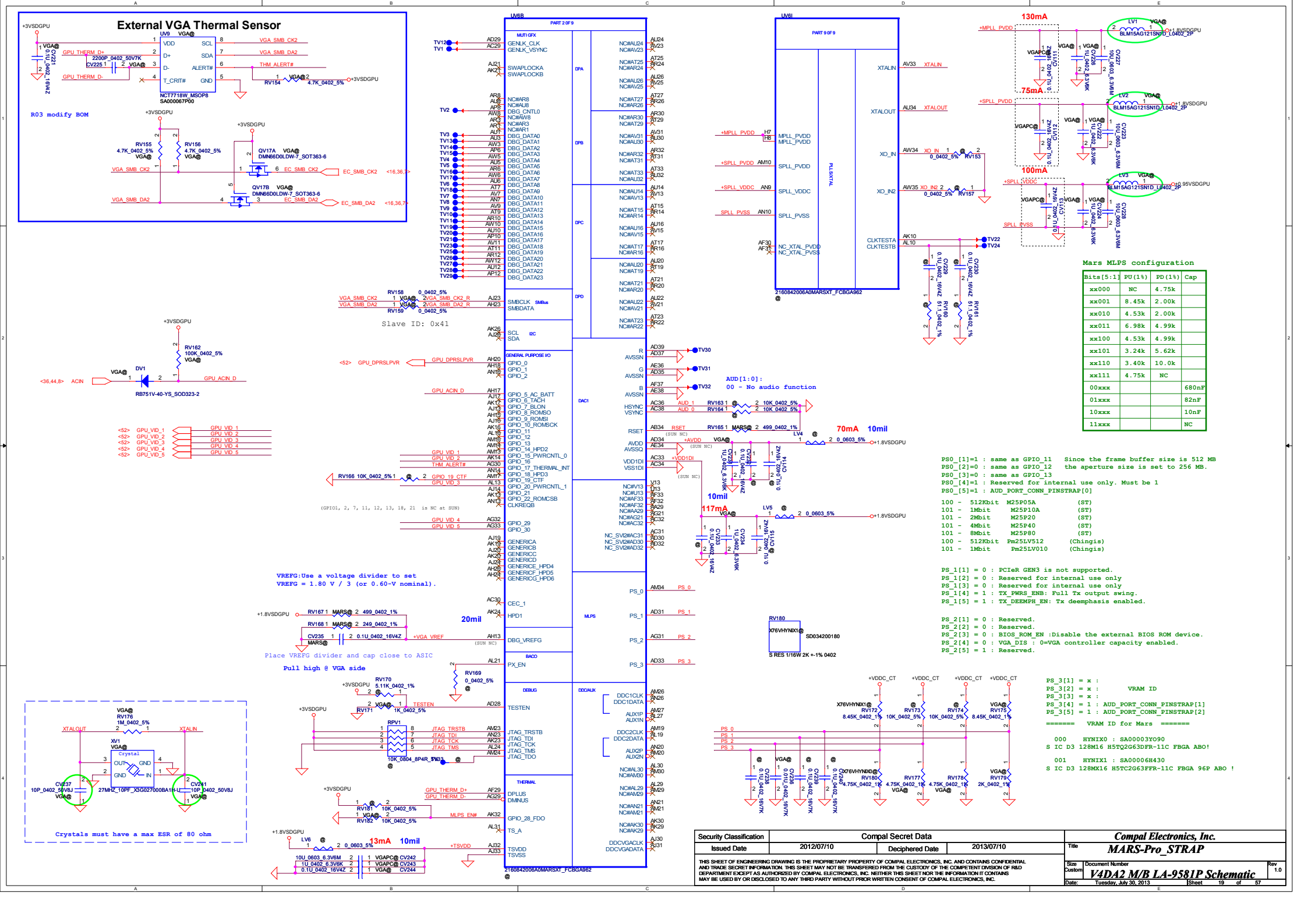
Date: Thursday, August 01, 2013 | Sheet 18 of 57



Bits[5:1]	PU(1%)	PD(1%)	Cap
xx000	NC	4.75k	
xx001	8.45k	2.00k	
xx010	4.53k	2.00k	
xx011	6.98k	4.99k	
xx100	4.53k	4.99k	
xx101	3.24k	5.62k	
xx110	3.40k	10.0k	
xx111	4.75k	NC	
00xxx			680nF
01xxx			82nF
10xxx			10nF
11xxx			NC

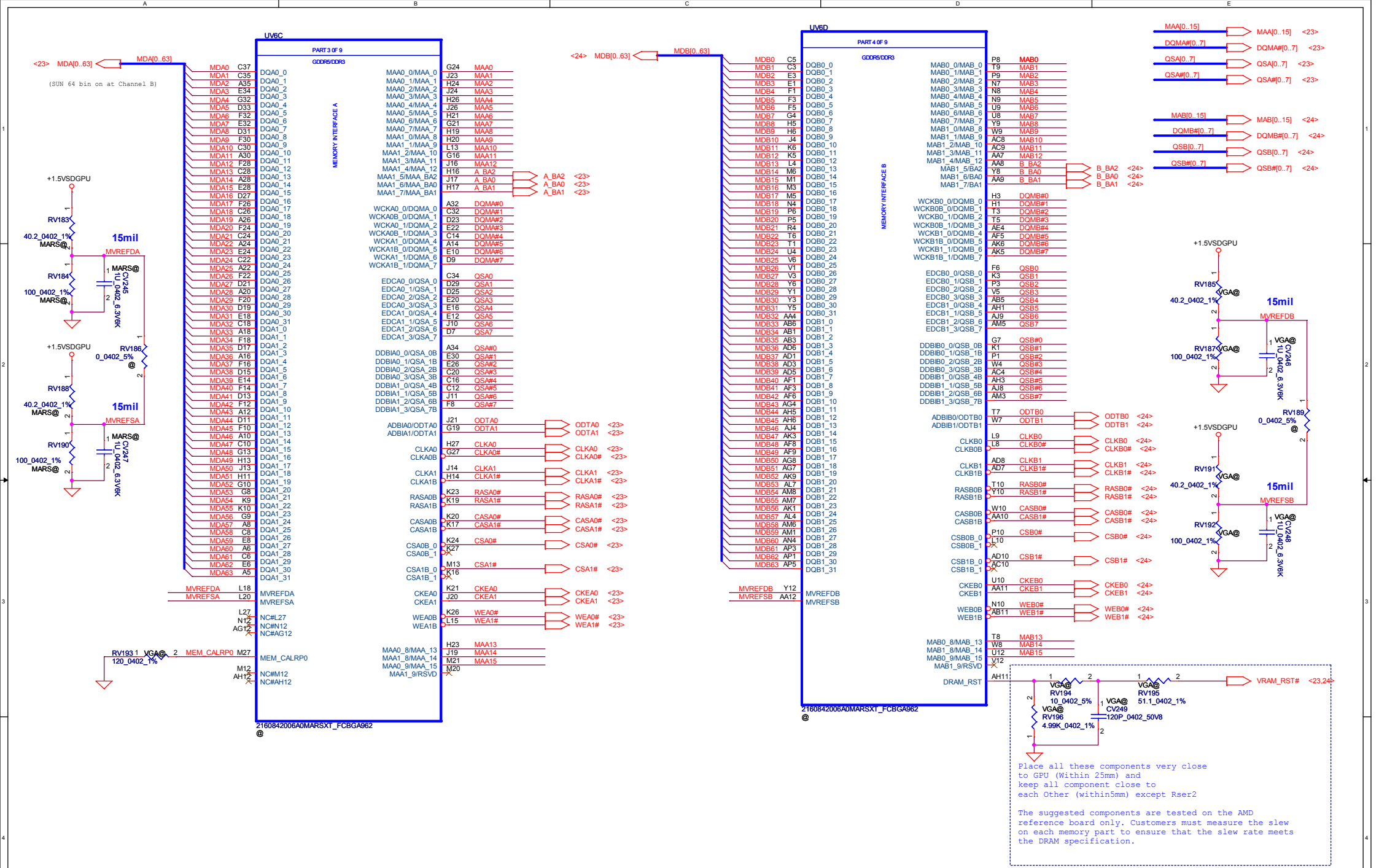
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.

Title: MARS-Pro_STRAP

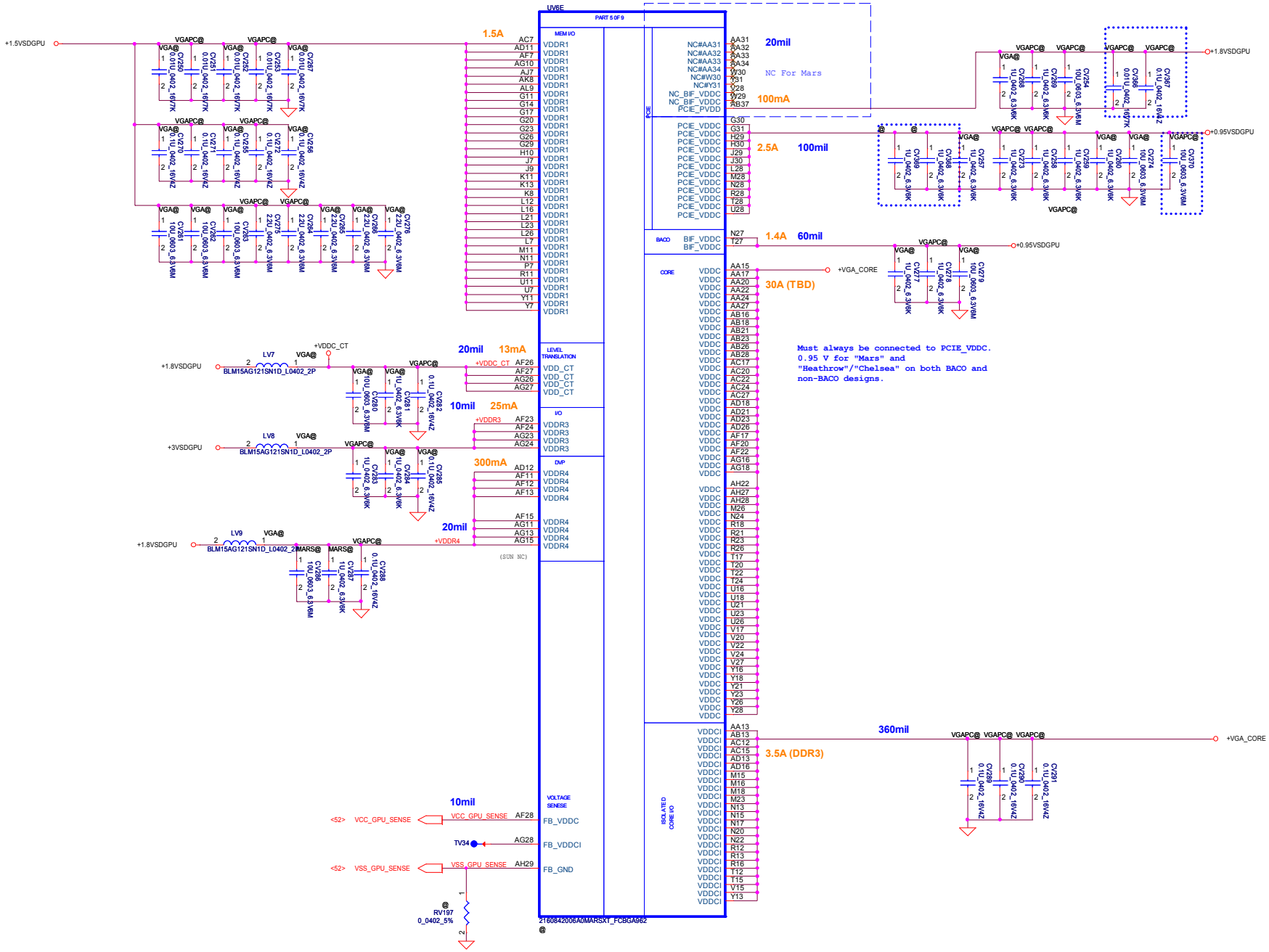
Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0

Date: Tuesday, July 30, 2013 | Sheet 19 of 57



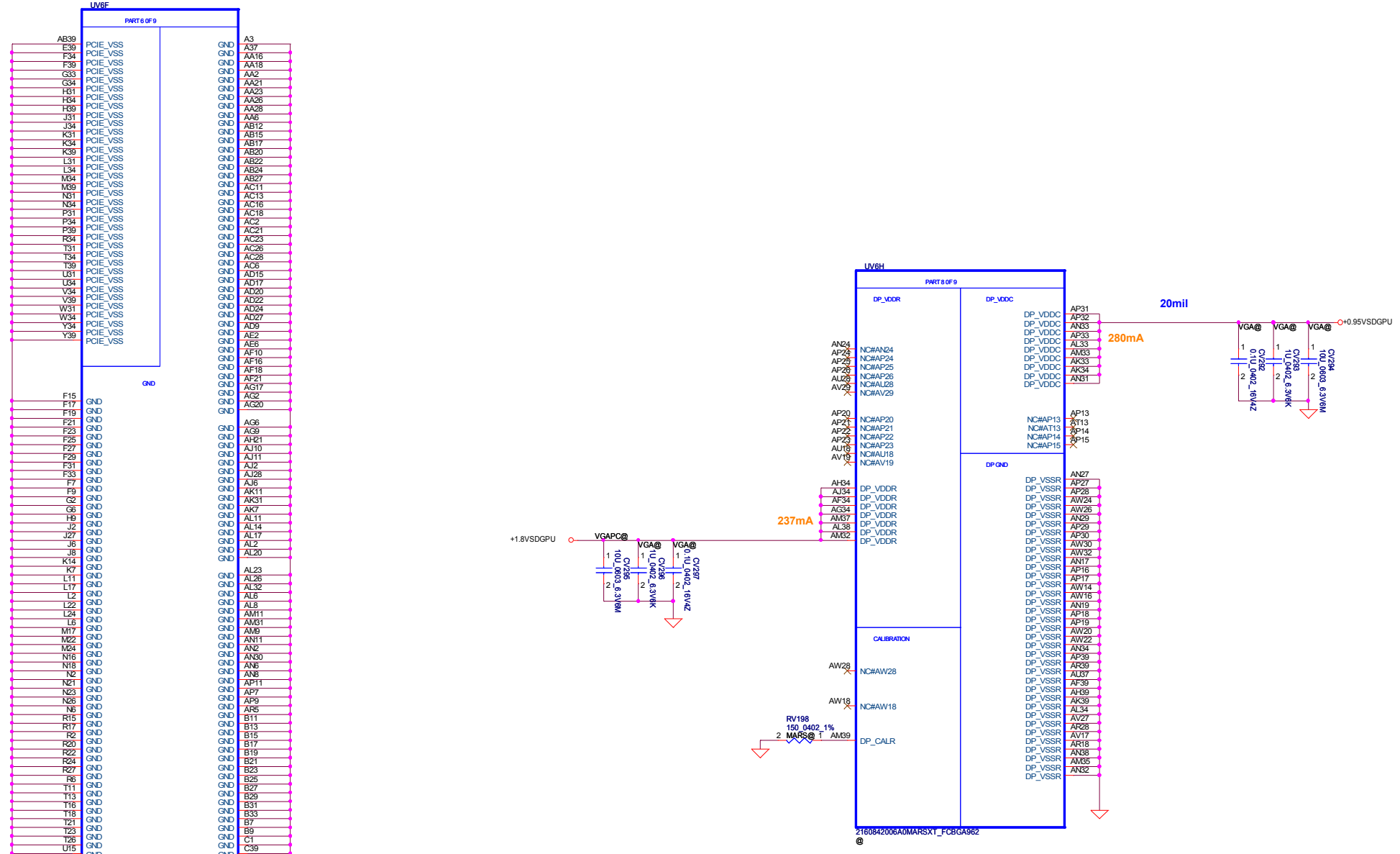
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/07/10	Deciphered Date 2013/07/10	Title: MARS-Pro_MEMORY

Size: Custom	Document Number: V4DA2 M/B LA-9581P Schematic		Rev: 1.0
Date: Tuesday, July 30, 2013	Sheet 20 of 57		



Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.			
Title: MARS-Pro_PWR/GND			
Size: Custom	Document Number: V4DA2 M/B LA-9581P Schematic		Rev: 1.0
Date: Tuesday, July 30, 2013	Sheet 21 of 57		



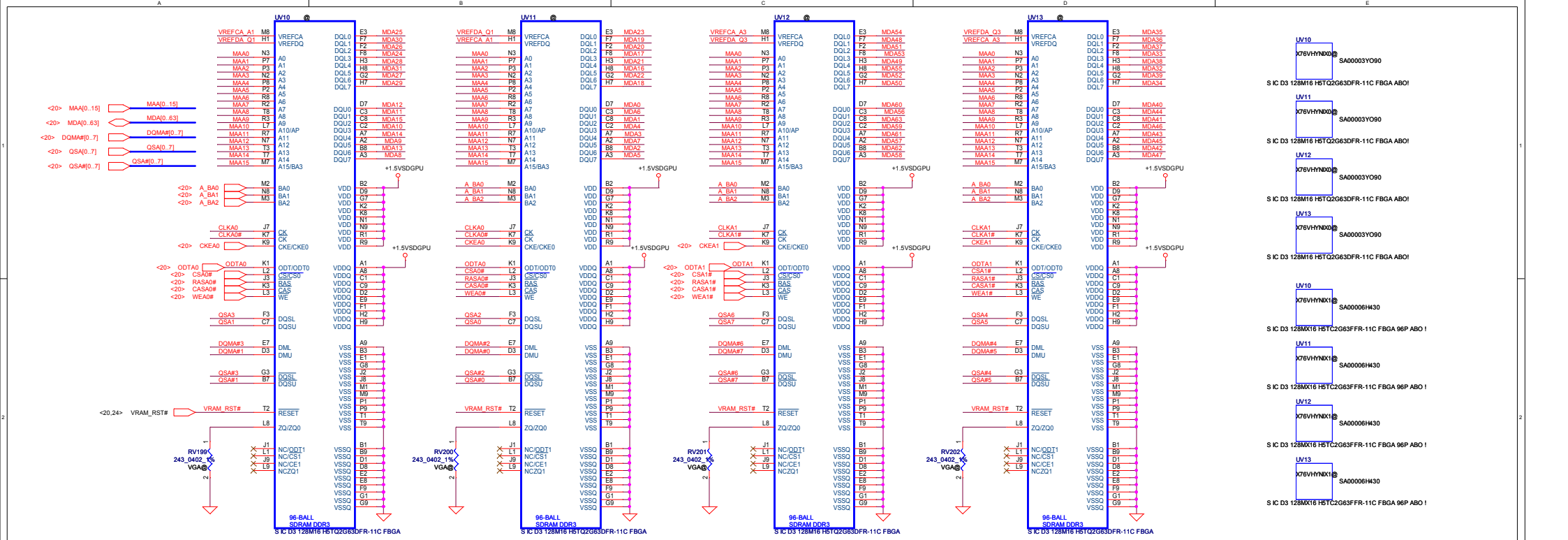
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

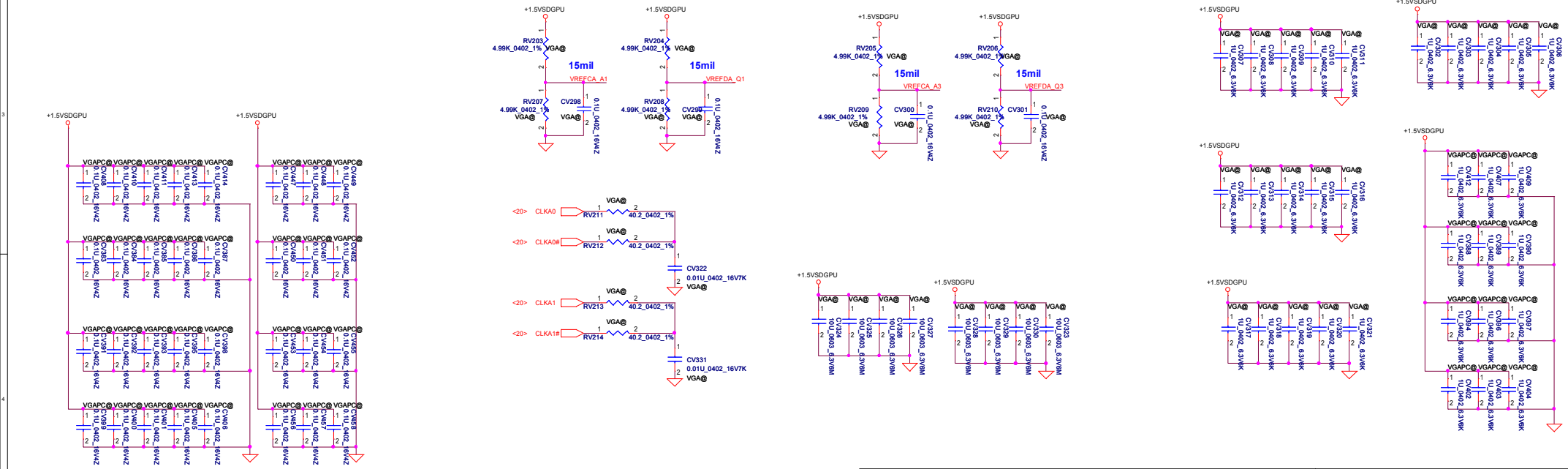
Compal Electronics, Inc.

Title: MARS-Pro_PWR/GND

Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0

Date: Tuesday, July 30, 2013 | Sheet 22 of 57





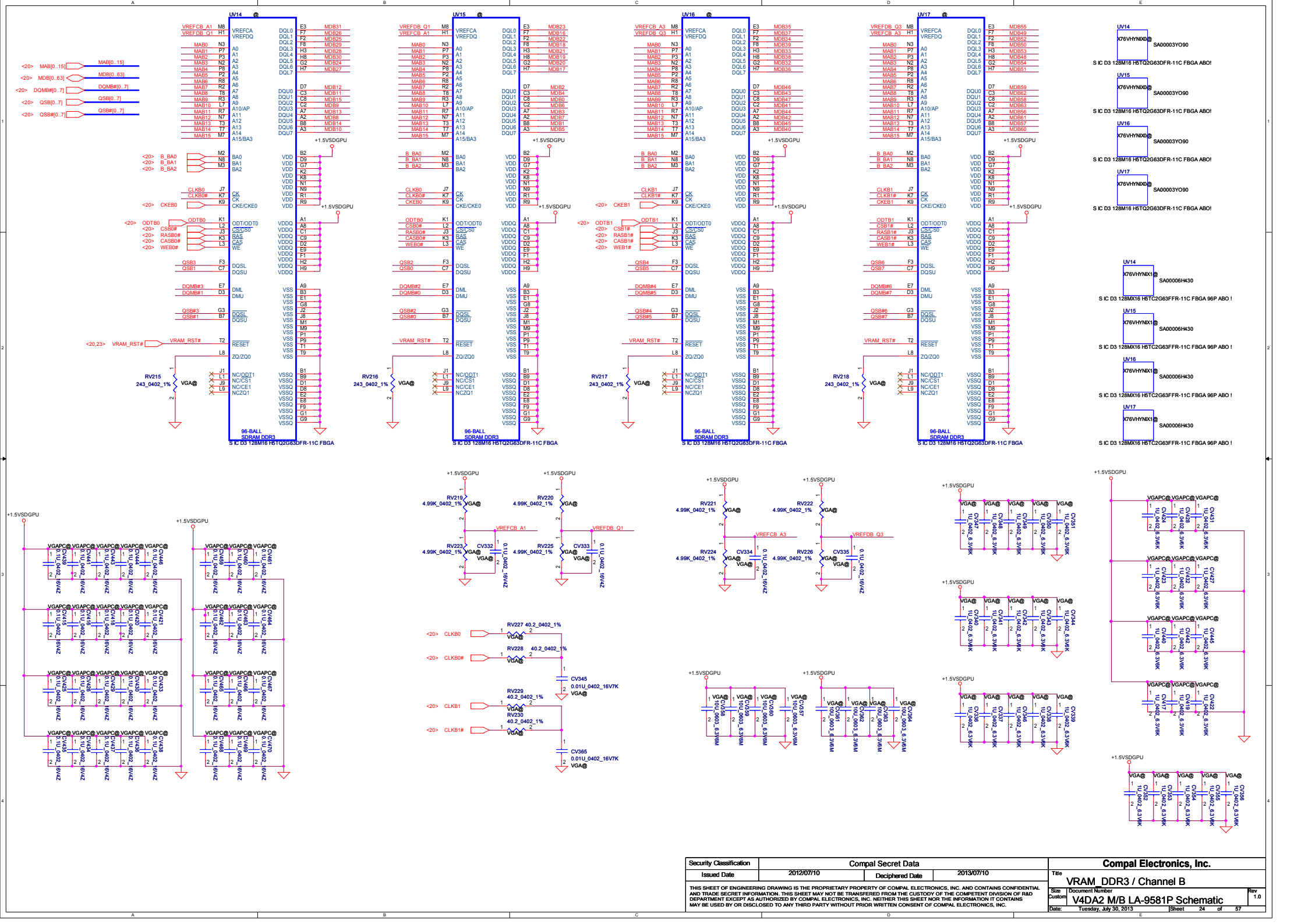
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel A

Size	Document Number	Rev
Custom	V4DA2 M/B LA-9581P Schematic	1.0

Date: Tuesday, July 30, 2013 | Sheet 23 of 57



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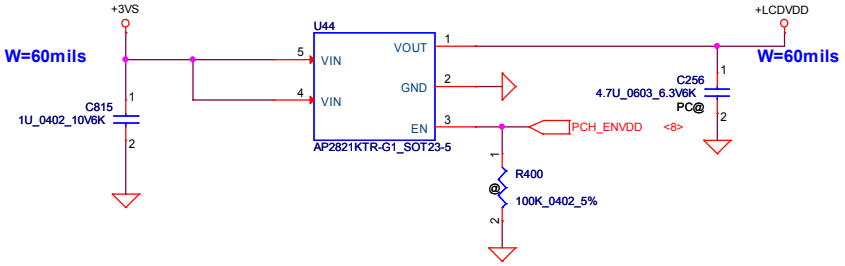
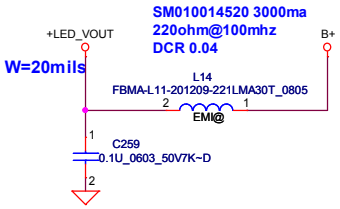
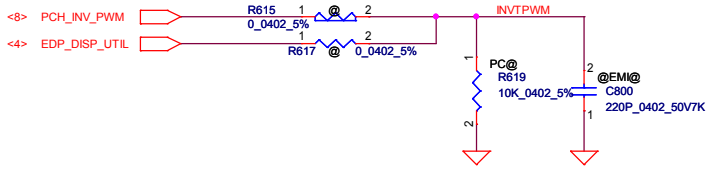
Compal Electronics, Inc.

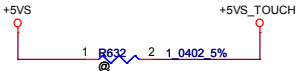
Title	VRAM_DDR3 / Channel B	
Size: Custom	Document Number: V4DA2 M/B LA-9581P Schematic	Rev: 1.0
Date: Tuesday, July 30, 2013	Sheet 24 of 57	

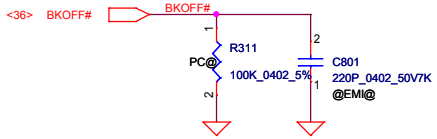
LCD POWER CIRCUIT

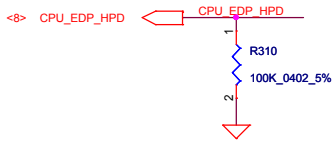


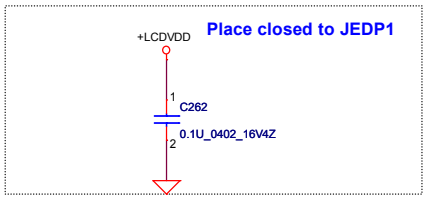




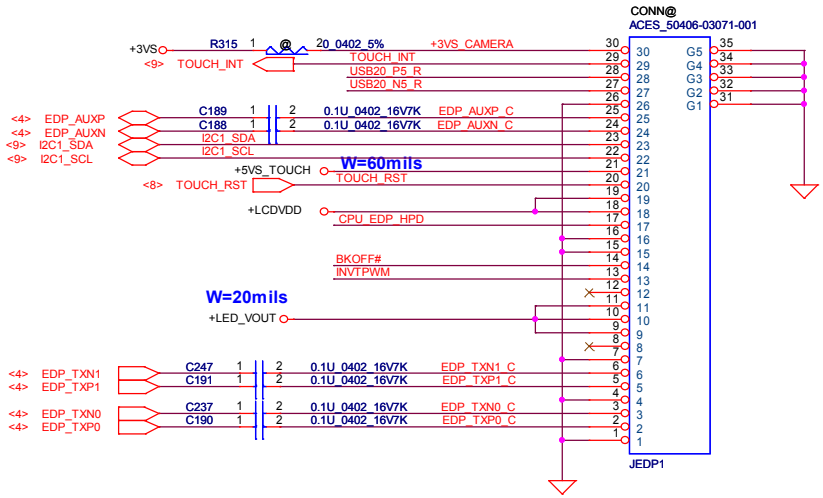




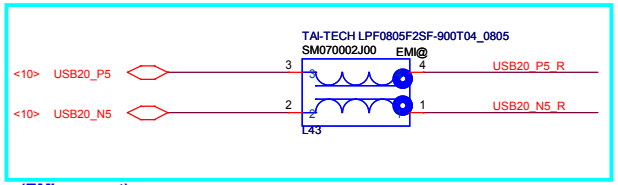




eDP PANEL Conn.



Camera



(EMI request)

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Compal Electronics, Inc.

Title: eDP CONN.

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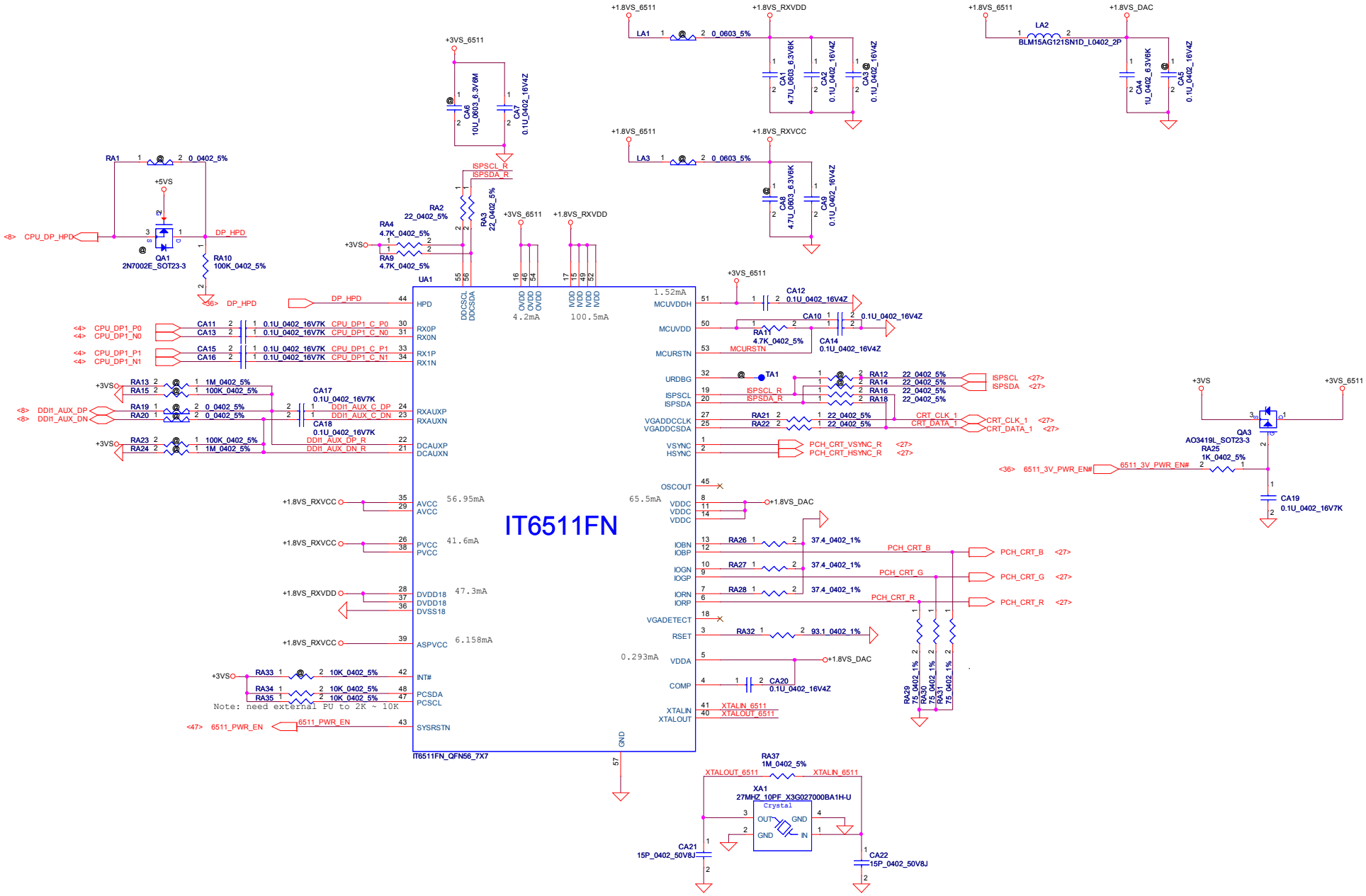
Date: Tuesday, July 30, 2013 | Sheet 25 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

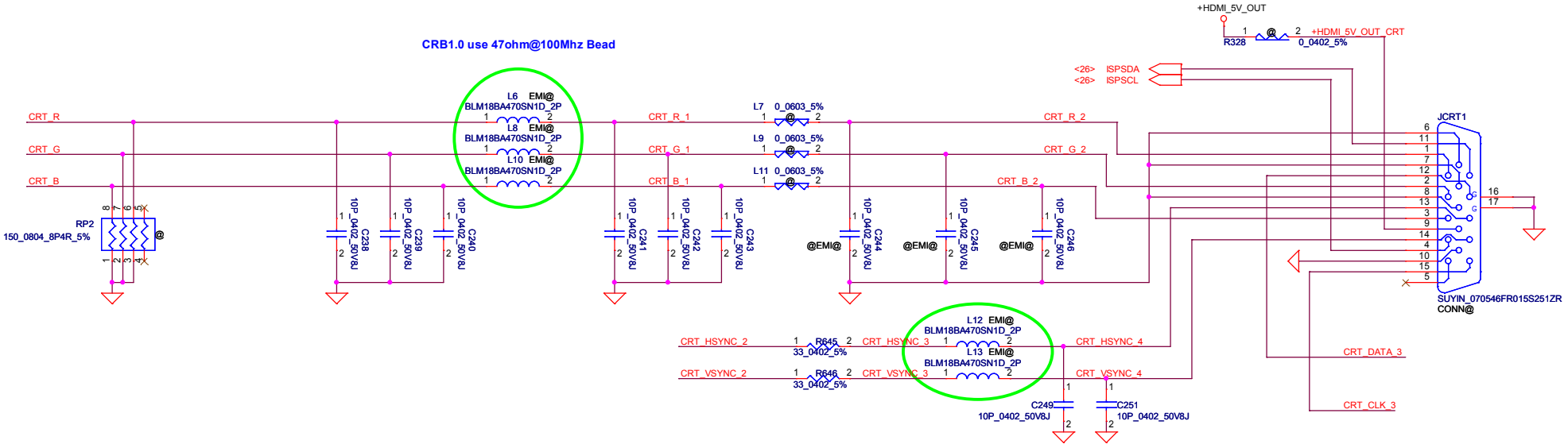
Compal Electronics, Inc.

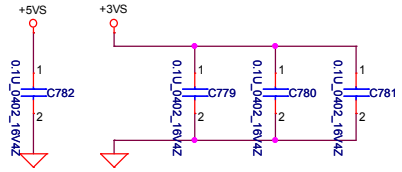
Title: ITE IT6511FN

Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0

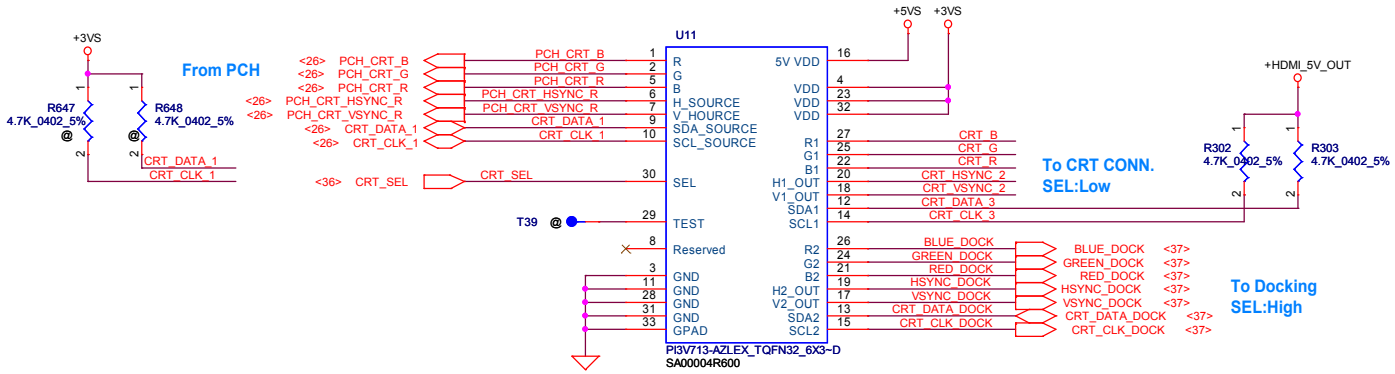
Date: Tuesday, July 30, 2013 | Sheet 26 of 57

CRT Connector



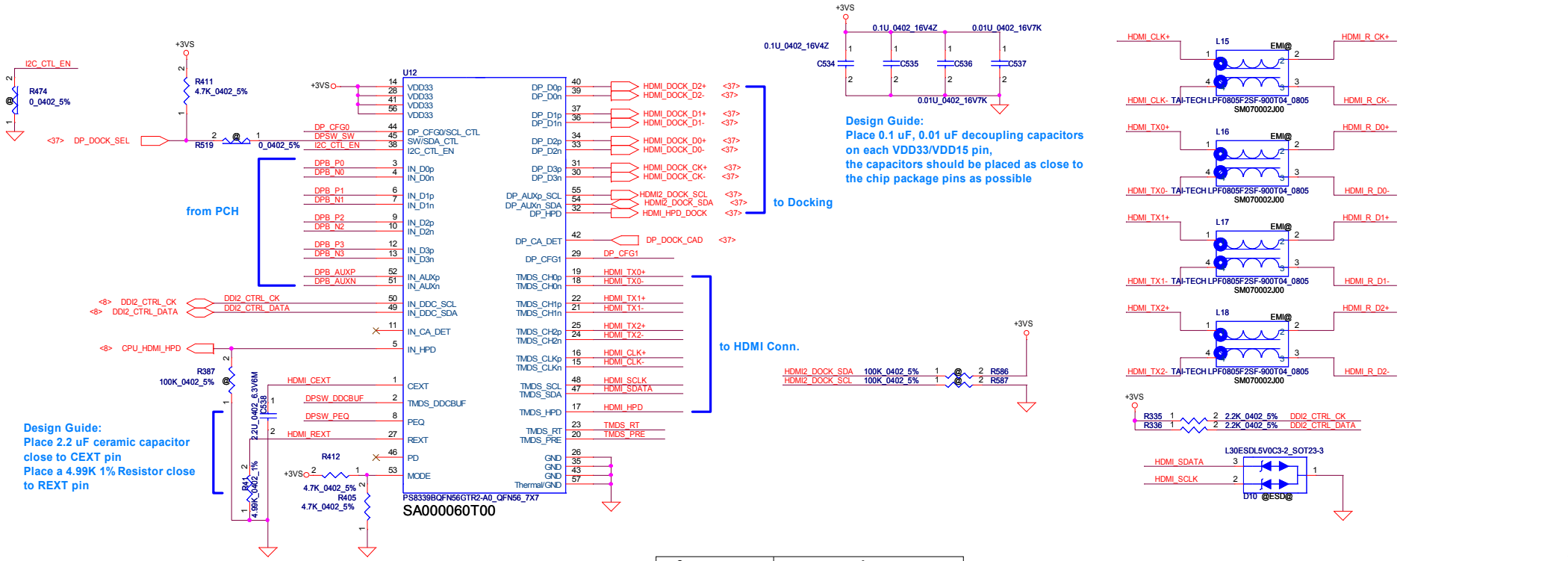


SELx	Function
L	port 1 is chose
H	port 2 is chose



Security Classification	Compal Secret Data		
Issued Date	2012/07/20	Deciphered Date	2013/07/20

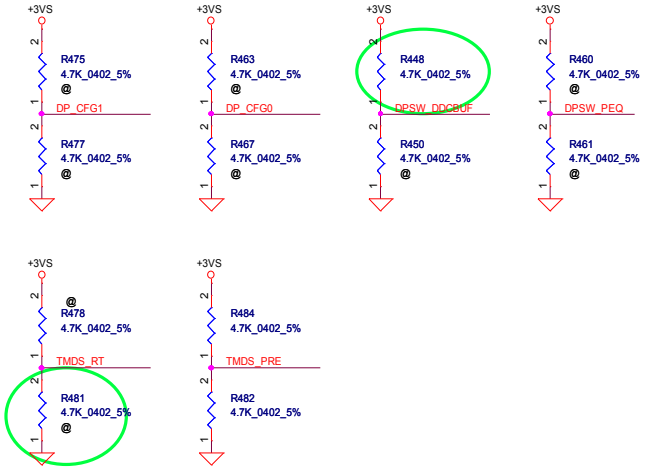
Compal Electronics, Inc.			
Title: CRT CONN.			
Size: Custom	Document Number: V4DA2 M/B LA-9581P Schematic		Rev: 1.0
Date: Tuesday, July 30, 2013	Sheet 27 of 57		

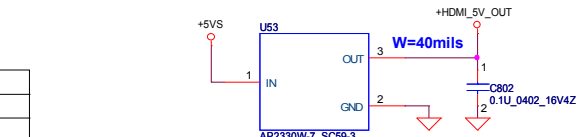


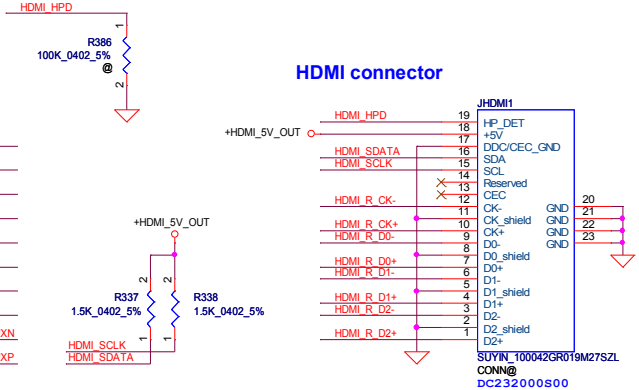
I2C_CTL_EN	Mode
Low	Pin Control Mode
High	I2C Control Mode

Control Switching Mode			
SW	DP Output	HDMI Output	HPD_SRC
0	Enable	Z	DP_HPD
1	Z	Enable	HDMI_HPD

AUTOSW_EN	Power Mode
Low	Control port switching
High	Automatic port switching







Security Classification	Compal Secret Data		
Issued Date	2012/07/20	Deciphered Date	2013/07/20

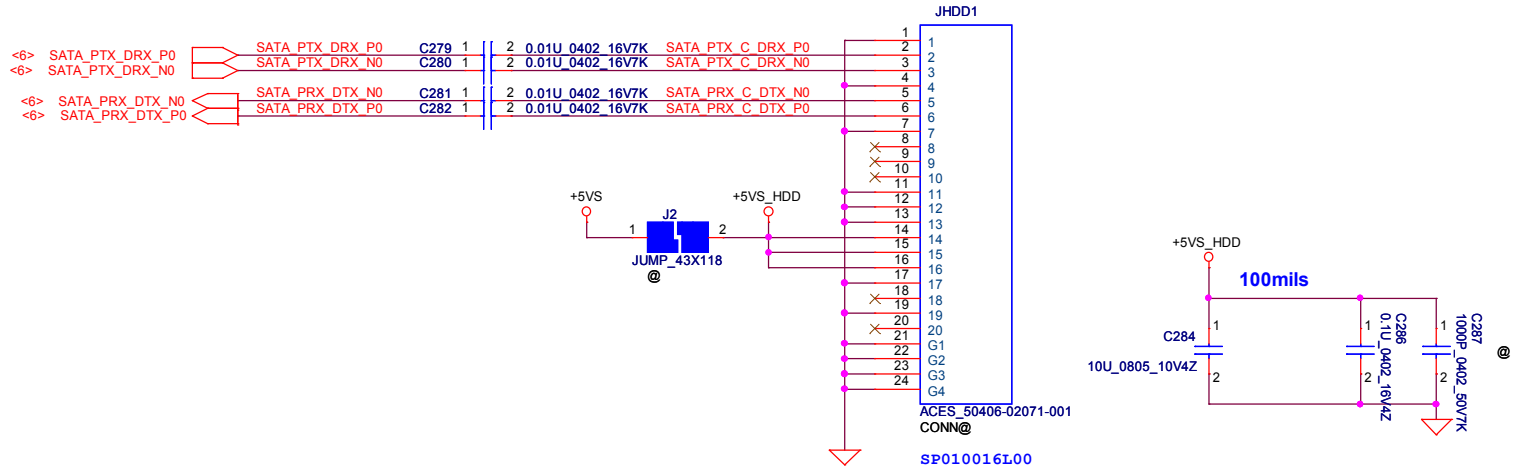
Compal Electronics, Inc.

Title: HDMI CONN.

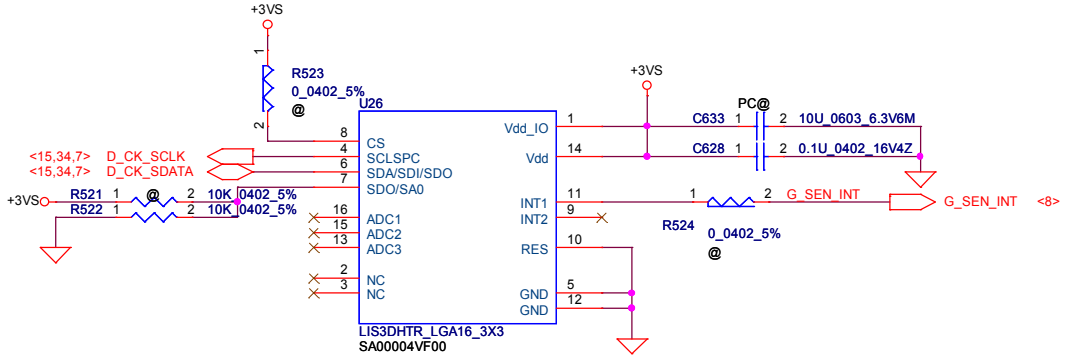
Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0

Date: Monday, August 05, 2013 | Sheet 28 of 57

HDD Board Conn



APS G-Sensor



LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)

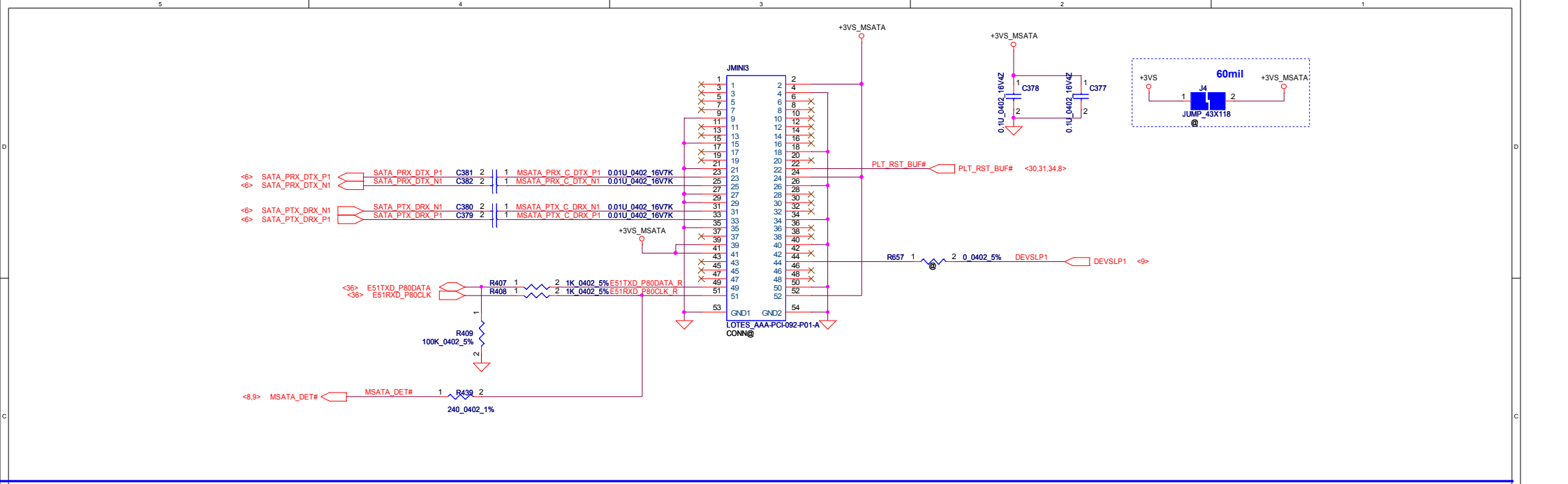
Security Classification	Compal Secret Data		
Issued Date	2012/07/20	Deciphered Date	2013/07/20

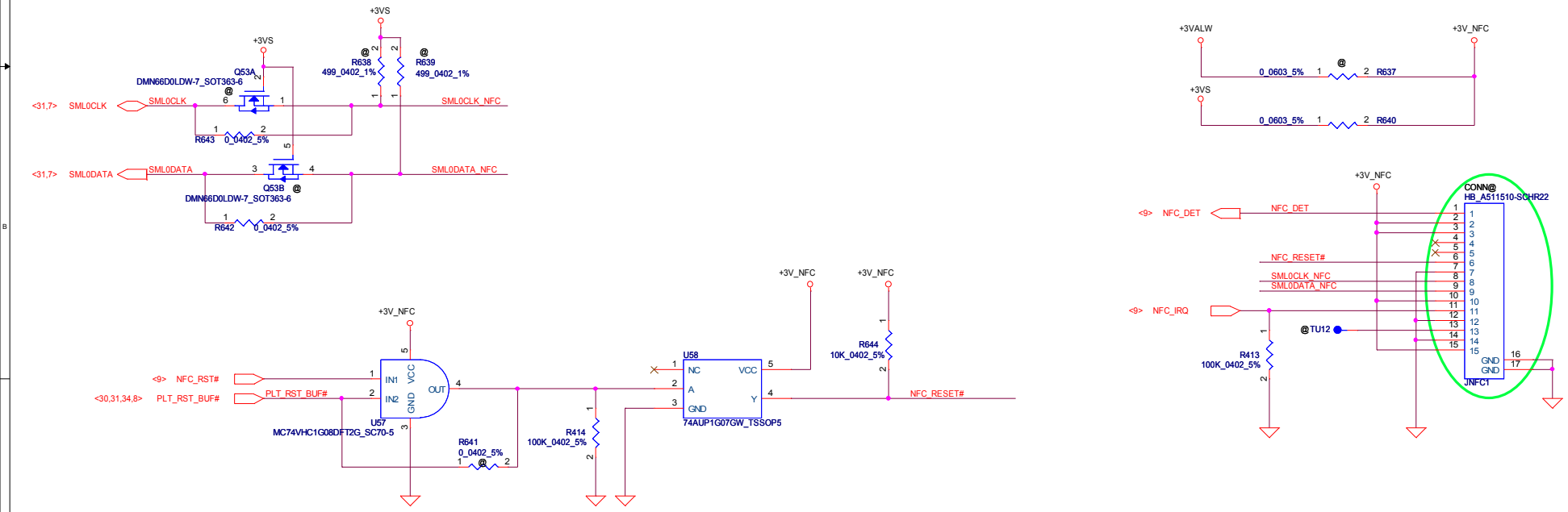
Compal Electronics, Inc.

Title: HDD & G-Sensor

Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0

Date: Tuesday, July 30, 2013 | Sheet 29 of 57



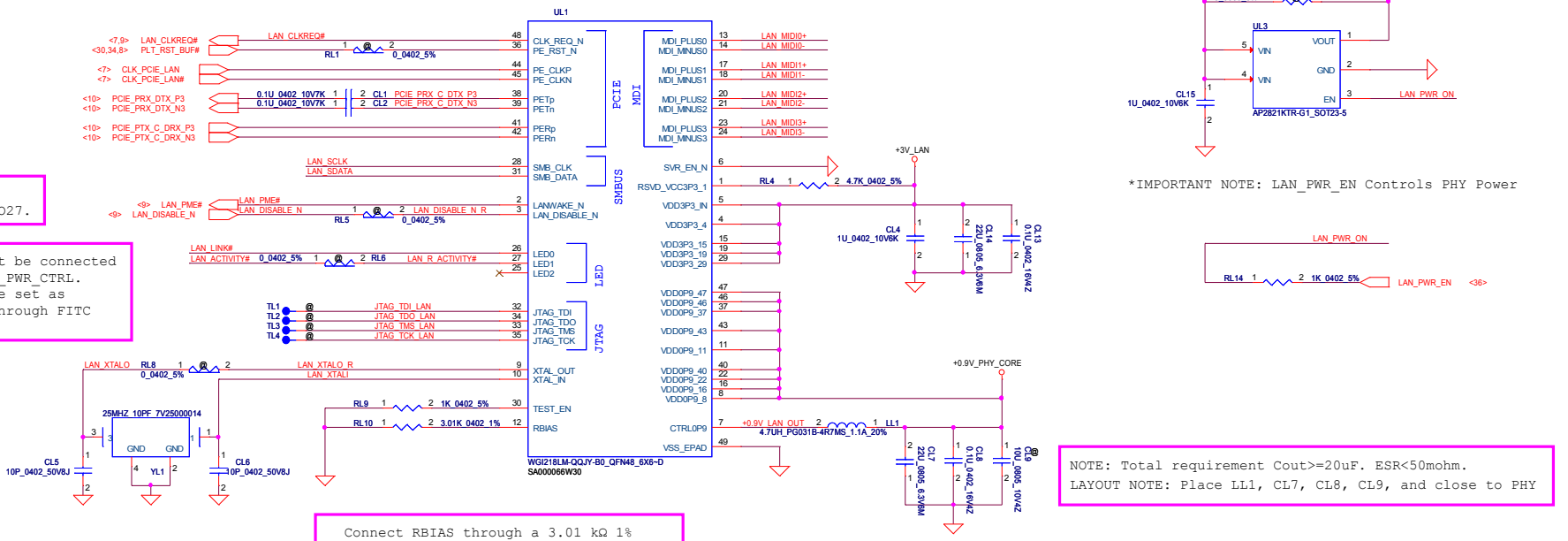


Security Classification	Compal Secret Data		
Issued Date	2012/07/20	Deciphered Date	2013/07/20

Compal Electronics, Inc.			
Title	mSATA & NFC		
Size: Custom	Document Number: V4DA2 M/B LA-9581P Schematic		Rev: 1.0
Date: Tuesday, July 30, 2013	Sheet 30 of 57		

NOTE: LANWAKE_N must be connected to PCH's GPIO27.

NOTE: LAN_DISABLE_N must be connected to PCH's GPIO12/LAN_PHY_PWR_CTRL. This GPIO12 pin must be set as "LAN_PHY_PC" function through FITC tool.

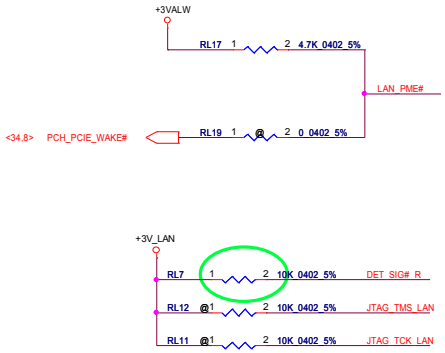


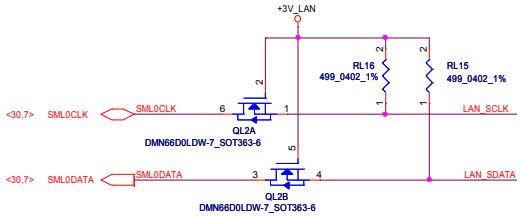
Connect RBIAS through a 3.01 kΩ 1% pull-down resistor to ground and then place it no more than one half inch (0.5") away from the PHY.

*IMPORTANT NOTE: LAN_PWR_EN Controls PHY Power

NOTE: Total requirement Cout>=20uF. ESR<50mohm.
LAYOUT NOTE: Place LL1, CL7, CL8, CL9, and close to PHY

PD	SEL	Function
L	L	Ax to Bx; LEDAx to LEDBx
L	H	Ax to Cx; LEDAx to LEDCx
H	X	Hi-Z



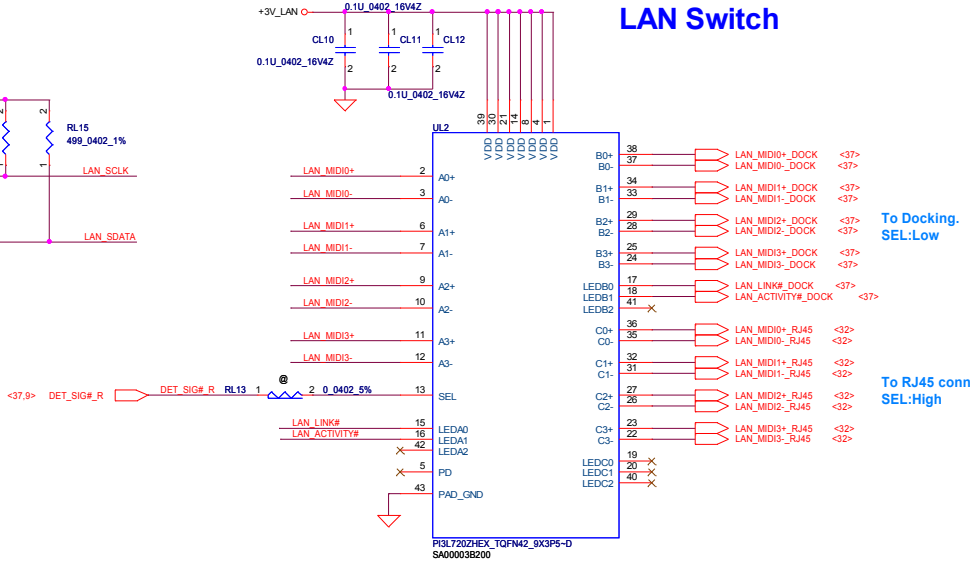


NOTE: Default SMBus Address is 0xC8

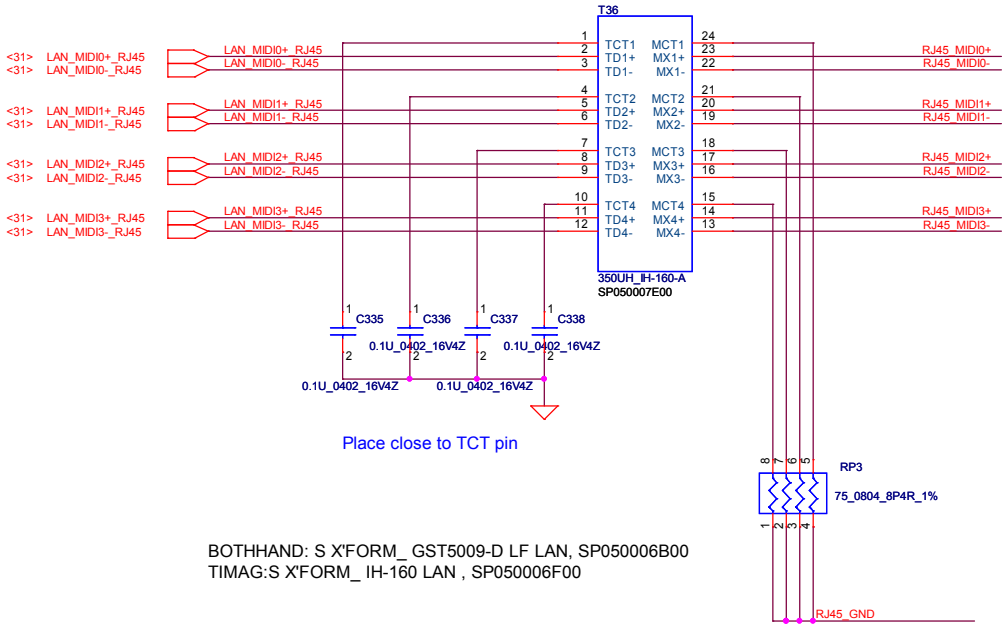
SMBUS PULL-UP OPTIONS

SMBUS SPEED	RL15 & RL16
1MHz(Defaul setting)	499ohm
100KHz/400KHz	2.2Kohm

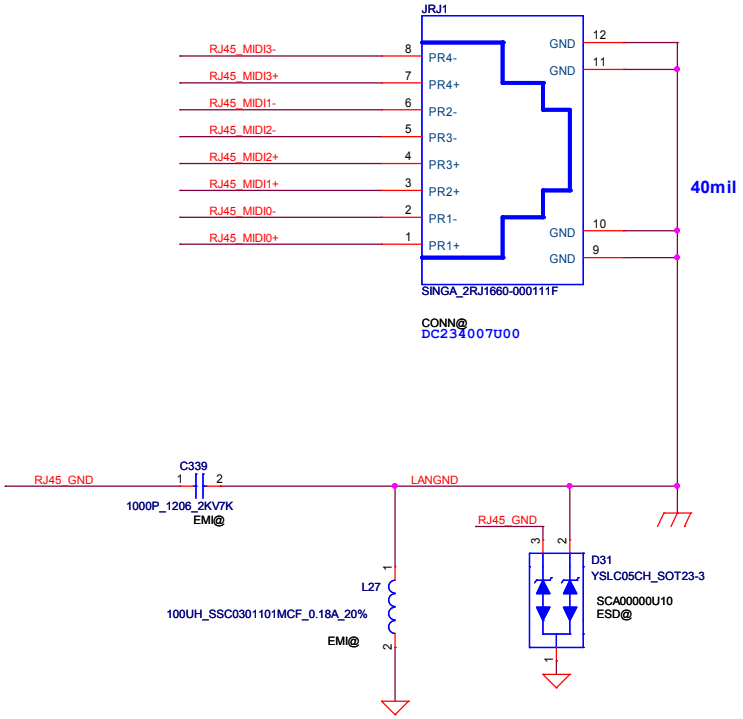
LAN Switch



LAN Connector



BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00



Security Classification	Compal Secret Data		
Issued Date	2012/07/20	Deciphered Date	2013/07/20

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0

Date: Tuesday, July 30, 2013 | Sheet 32 of 57

HD Audio Codec

Int. Speaker Conn.

Headphone Out

Mic In

Digital MIC CONN

Security Classification	Compal Secret Data		
Issued Date	2012/07/20	Deciphered Date	2013/07/20

Compal Electronics, Inc.

Title: HD Audio Codec_ALC3225X

Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0

Date: Thursday, August 01, 2013 | Sheet 33 of 57

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

R394 0_0402_5% BT_CTRL
<36> BT_ON#
Q21 2N7002E_SOT23-3

For Wireless LAN

+3VS 40mil +3VS_WLAN
R381 0_0603_5%
+3VS_WLAN C365 4.7U_0603_6.3V6K C366 0.1U_0402_16V4Z PC@ C367 0.1U_0402_16V4Z PC@
+1.5VS C368 4.7U_0603_6.3V6K @

+3VS_WLAN R398 10K_0402_5% PCH_PCIE_WAKE#_R

+3VALW U46 AP2821KTR-G1_SOT23-5 VIN VIN VOUT GND EN
C816 1U_0402_10V6K
40mil(1A) +3VS_WLAN
WLAN_ON <36>
R399 100K_0402_5%

Mini Card Power Rating

<36> WLAN_PME# R317 0_0402_5%
<31,8> PCH_PCIE_WAKE# R397 0_0402_5% PCH_PCIE_WAKE#_R
<7,8> MINI1_CLKREQ# R316 0_0402_5%
<7> CLK_PCIE_MINI1#
<7> CLK_PCIE_MINI1
<10> PCIE_PRX_DTX_N4
<10> PCIE_PRX_DTX_P4
<10> PCIE_PTX_C_DRX_N4
<10> PCIE_PTX_C_DRX_P4
<7> CL_CLK
<7> CL_DATA
<7> CL_RST
R410 0_0402_5% BT_CTRL

JMINI1 CONN@ SP07000LL00(H:4.0mm)
+1.5VS +3VS_WLAN
MINI1_SMBCLK R403 0_0402_5% D_CK_SCLK <15,29,7>
MINI1_SMBDATA R404 0_0402_5% D_CK_SDATA <15,29,7>
USB20_N6 <10>
USB20_P6 <10>
WL_OFF#
PLT_RST#_W
WL_OFF# <36>

+3VS_WLAN R663 10K_0402_5%
D38 RB751V-40-YS_SOD323-2
PLT_RST# <36,38,8>
R664 0_0402_5%
R665 0_0402_5%
PLT_RST_BUF# <30,31,8>

MINI CARD(Wireless LAN & BT)

+3VS_3G R406 3G@ 10K_0402_5% WAKE_OUT_WWAN
<36> EC_3G_WKAE# R630 0_0402_5% WAKE_OUT_WWAN R402 10K_0402_5% BODYSAR_DET#
<8,9> MINI_DET#
TU155 @ 3G_CONFIG3
USB20_P4_L USB20_N4_L
TU156 @ 3G_CONFIG0

JMINI2 BELLW_80149-3223_67P CONN@
CONFIG_3 Ground Ground USB_D+ USB_D- Ground
CONFIG_0 Wake_On_WWAN# BODYSAR_N Ground NC NC Ground NC NC Ground NC NC Ground NC NC Ground NC NC Ground ANTCTL0 ANTCTL1 ANTCTL2 ANTCTL3 Reset# CONFIG_1 Ground Ground CONFIG_2 GND
3.3V 3.3V Power_On_Off W_DISABLE# LED# Reserved Reserved Reserved GPS_DISABLE# Reserved UIM-RESET UIM-CLK UIM-DATA UIM-PWR NC Reserved Reserved Reserved Reserved NC NC NC NC NC NC NC Reserved Reserved Reserved Reserved SIM_DET NC 3.3V 3.3V 3.3V GND

R401 3G@ 10K_0402_5% +3VS_3G
3G_OFF# <34,36>
GPS_DISABLE#
UIM_RST UIM_CLK UIM_DATA UIM_PWR
MINI_DET#

33P_0402_50V8K C520 @
330P_0402_50V7K C445 @
330P_0402_50V7K C446 @
330P_0402_50V7K C447 @
330P_0402_50V7K C448 @

TU149 @ ANT_TUNE_0_AP R621 0_0402_5% ANT_TUNE_0
TU150 @ ANT_TUNE_1_AP R622 0_0402_5% ANT_TUNE_1
TU151 @ ANT_TUNE_2_AP R623 0_0402_5% ANT_TUNE_2
TU152 @ ANT_TUNE_3_AP R624 0_0402_5% ANT_TUNE_3
+3VS_3G R416 3G@ 10K_0402_5% 3G_RESET#
TU153 @ 3G_CONFIG1
TU154 @ 3G_CONFIG2

JSIM1 JAE_SF7W006S4AE1000
UIM_CLK UIM_RST UIM_PWR UIM_DATA
CLK RST VCC I/O VPP GND

UIM_CLK C523 33P_0402_50V8K
UIM_RST C524 33P_0402_50V8K
UIM_DATA C525 33P_0402_50V8K
UIM_PWR C526 33P_0402_50V8K
C809 1U_0402_10V6K

<36> 3G_PWR_ON#
3G_PWR_ON# 5 Q51B DMN66D0LDW-7_SOT363-6

+3VALW TO +3VS_3G

+3VALW U52 DMN3030LSS-13_SOP8L-8 +3VS_3G
240mil
C382 4.7U_0603_6.3V6K
R616 470_0603_5%
Q51A DMN66D0LDW-7_SOT363-6
20mil 470K_0402_5% R620 3G_PWR_ON#_R
10mil
C813 0.1U_0603_25V7K
3G_PWR_ON#

+3VS_3G
33P_0402_50V8K C522 @EMI
330P_0402_50V7K C444
0.1U_0402_16V4Z C807
1U_0402_10V6K C808
22U_0805_6.3V6M C808
220U4V Y D2 ESR15M C803
220U4V Y D2 ESR15M C804
220U4V Y D2 ESR15M C805

+3VS_3G R418 10K_0402_5% 3G_OFF# <34,36>
R417 3G@ 10K_0402_5% +3VALW +3VS
R318 0_0402_5%

U59 PI3USB102ZLEX_TQFN10_1P6X1P3
<10> USB20_N4 USB20_N4
<10> USB20_P4 USB20_P4
Y+ Y- GND M- M+ SEL Vdd OE D+ D-
USB20_N4_D USB20_P4_D

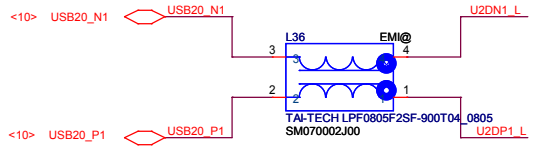
L37 EMI@ TAI-TECH LPF0805F2SF-900T04_0805 SM070002J00
USB20_P4_D USB20_N4_D USB20_P4_L USB20_N4_L

Truth Table

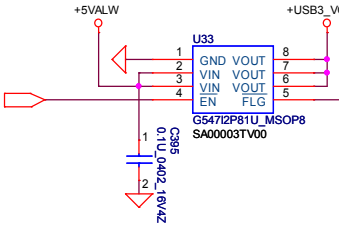
SEL	OE#	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

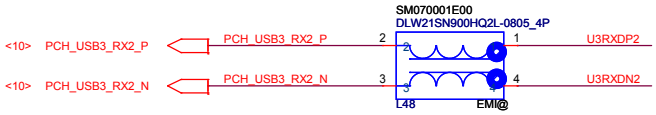
Security Classification	Compal Secret Data		
Issued Date	2012/07/20	Deciphered Date	2013/07/20

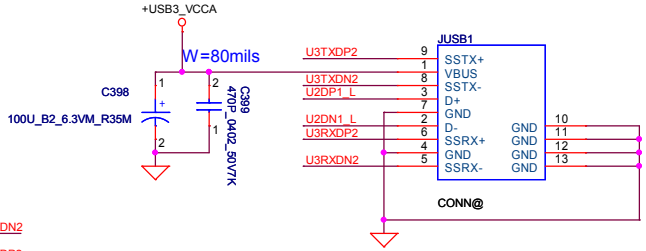
Compal Electronics, Inc.
Title: mini Card & 3G/SSD CONN.
Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0
Date: Tuesday, July 30, 2013 | Sheet 34 of 57

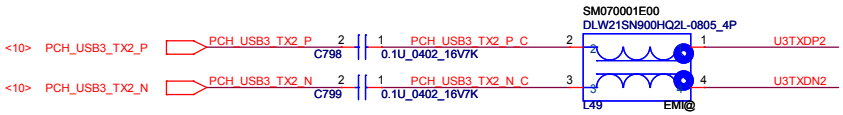


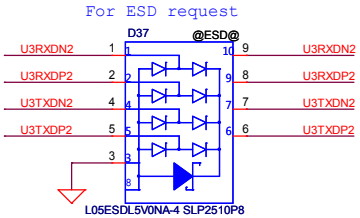
SM070000S80 WCM2012F2SF-670T04 67ohm



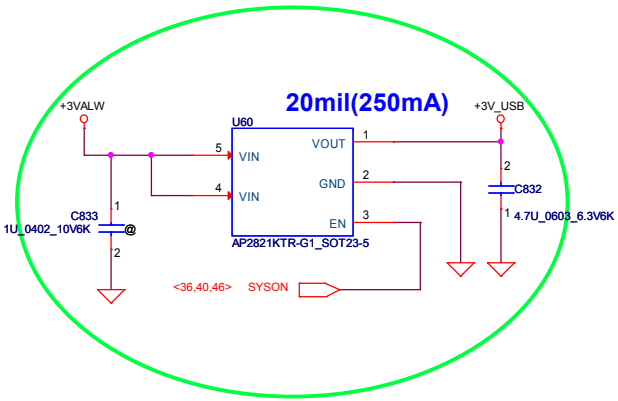




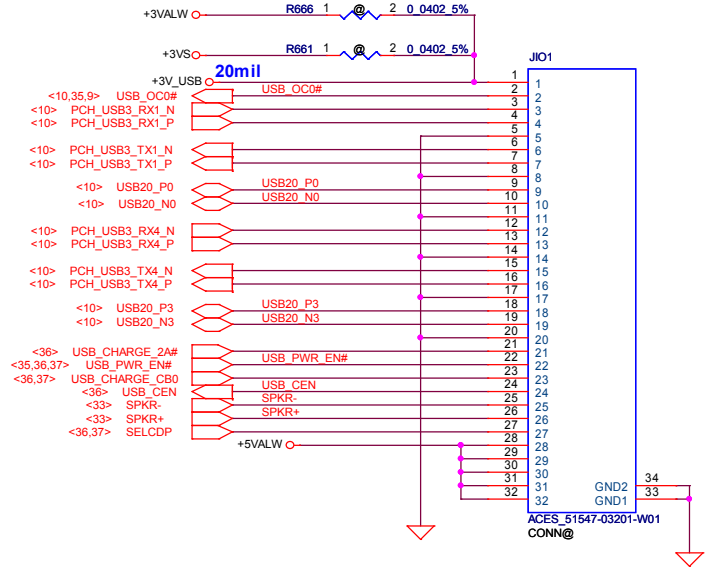




USB3.0 Conn.(MB)



IO Board Conn(For FFC,FPC)



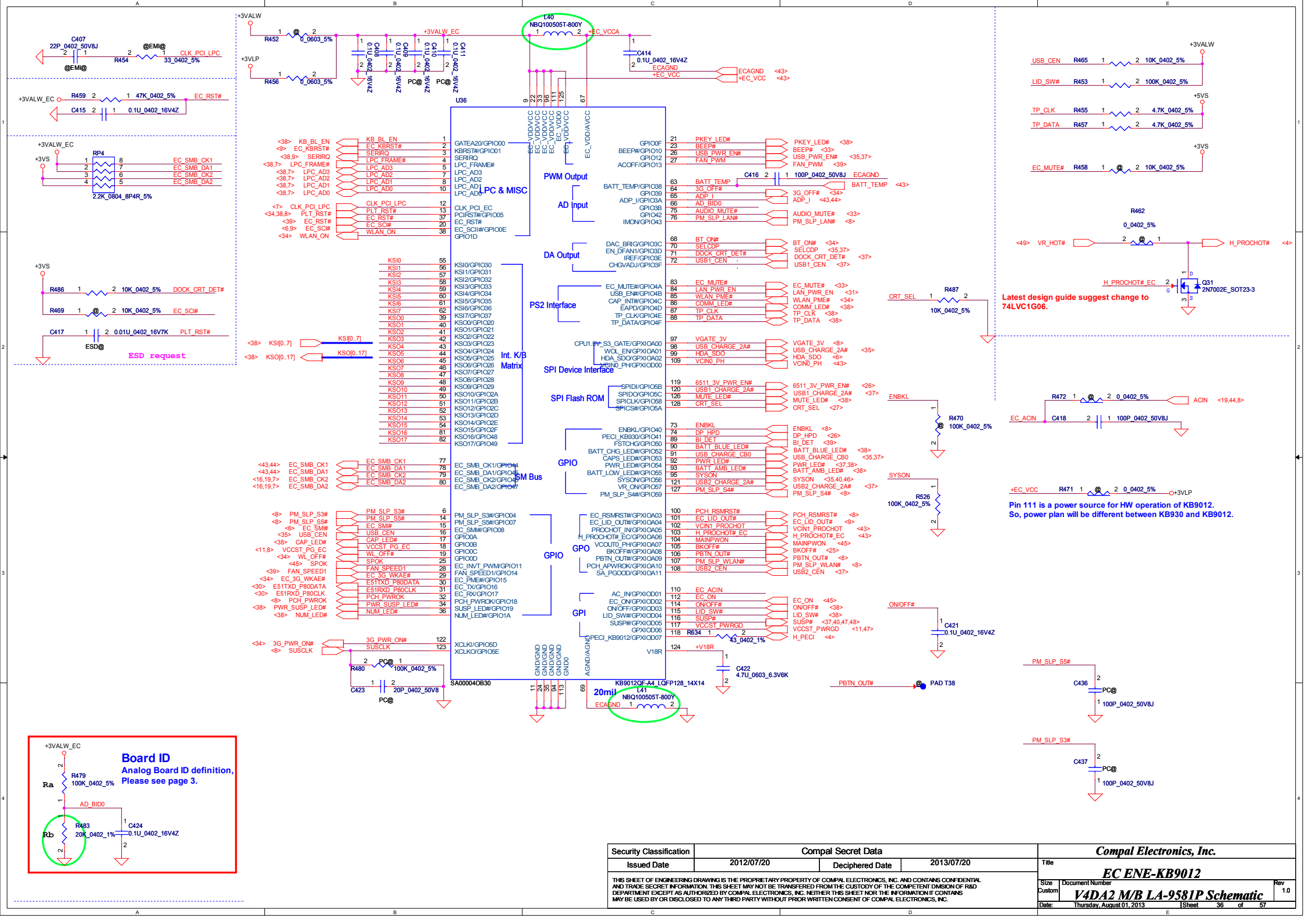
Security Classification	Compal Secret Data		
Issued Date	2012/07/20	Deciphered Date	2013/07/20

Compal Electronics, Inc.

Title: USB3.0 & SSD

Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0

Date: Tuesday, July 30, 2013 | Sheet 35 of 57



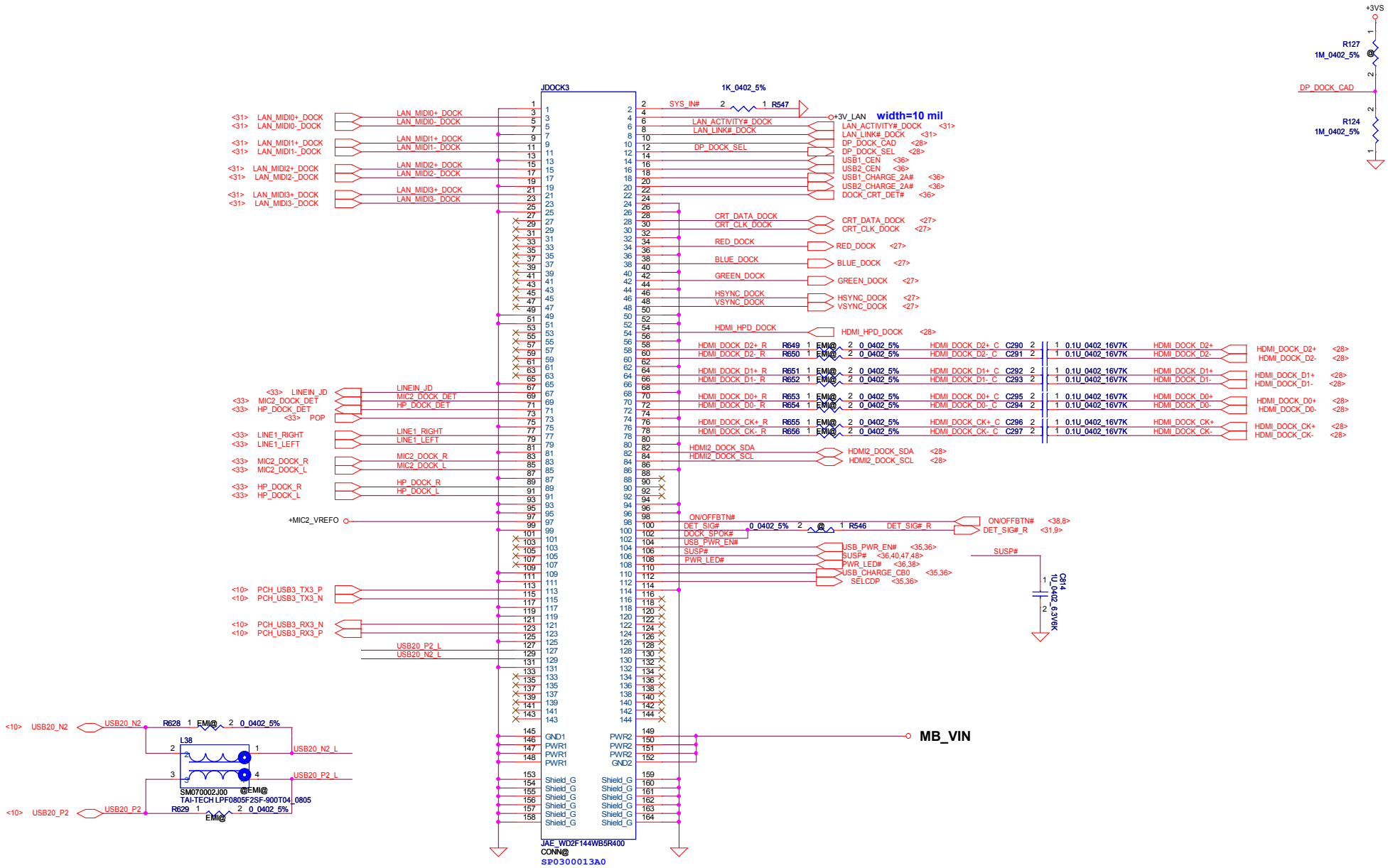
Security Classification	Compal Secret Data		
Issued Date	2012/07/20	Deciphered Date	2013/07/20

Compal Electronics, Inc.

Title: **EC ENE-KB9012**

Size: Custom | Document Number: **V4DA2 M/B LA-9581P Schematic** | Rev: 1.0

Date: Thursday, August 01, 2013 | Sheet 36 of 57



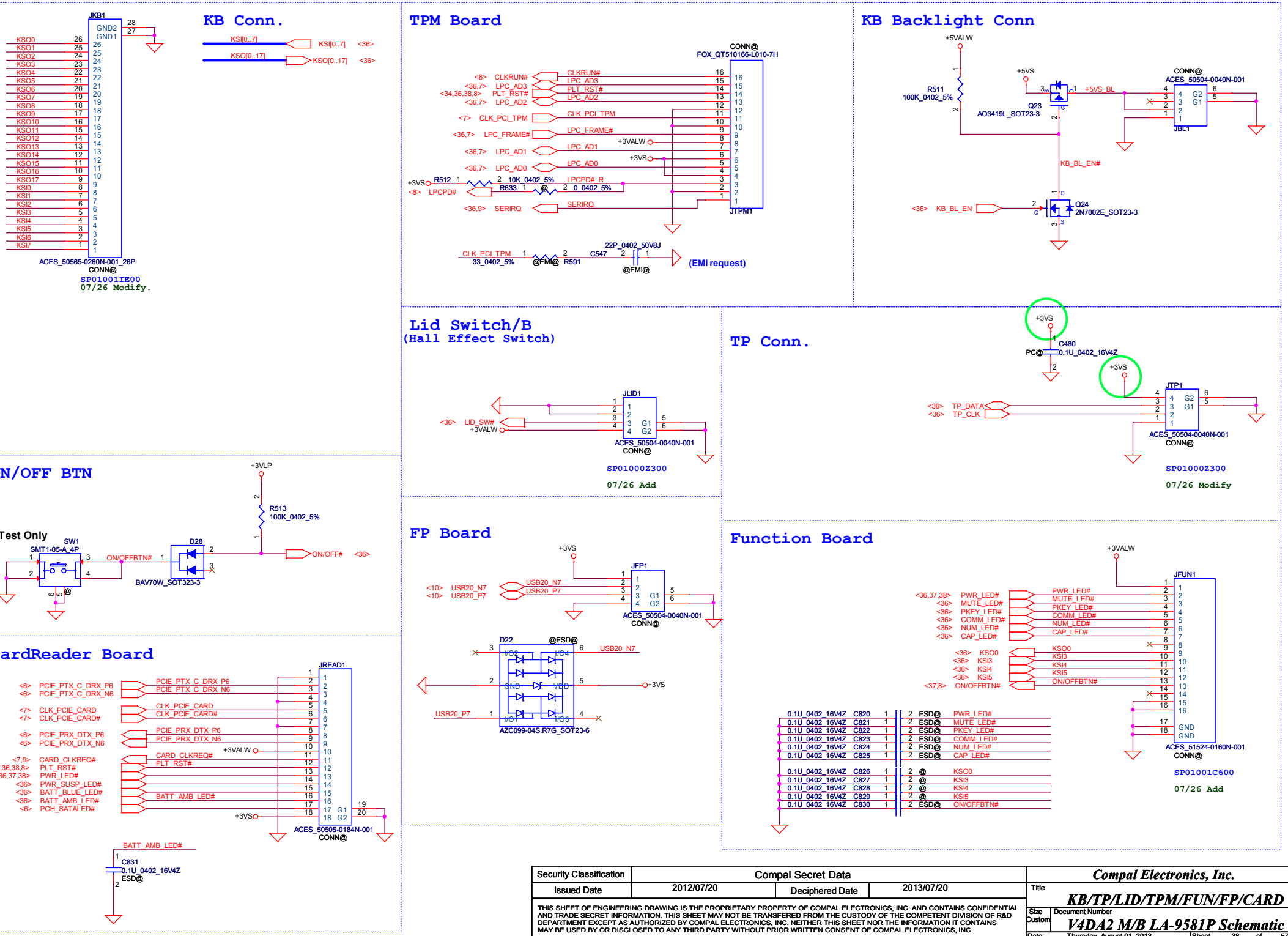
Security Classification	Compal Secret Data		
Issued Date	2012/07/20	Deciphered Date	2013/07/20

Compal Electronics, Inc.

Title: E Series Dcok CONN.

Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0

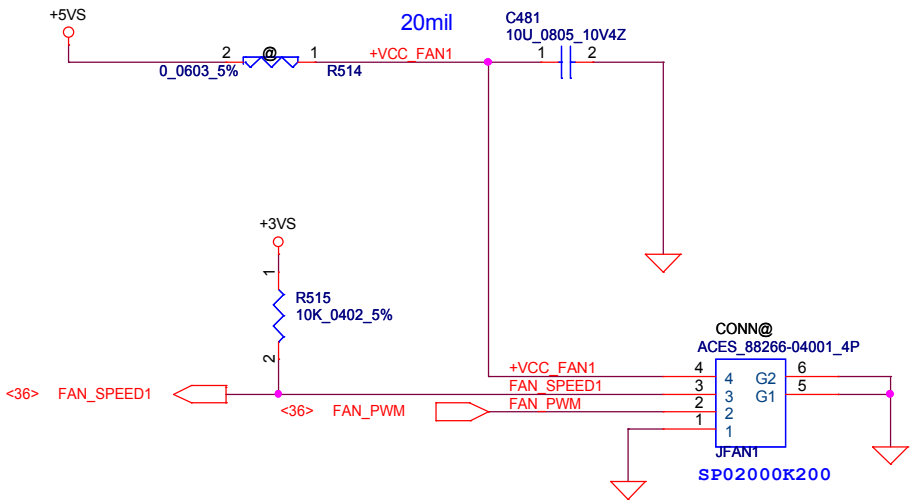
Date: Tuesday, July 30, 2013 | Sheet 37 of 57



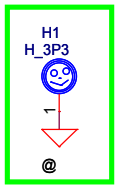
Security Classification	Compal Secret Data		
Issued Date	2012/07/20	Deciphered Date	2013/07/20

Compal Electronics, Inc.	
Title	KB/TP/LID/TPM/FUN/FP/CARD
Size: Custom	Document Number: V4DA2 M/B LA-9581P Schematic
Rev	1.0
Date: Thursday, August 01, 2013	Sheet 38 of 57

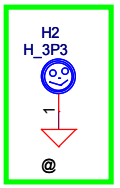
FAN Conn



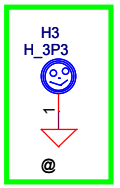
WIFI Stand off



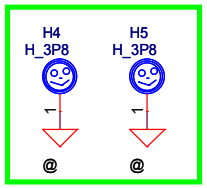
3G Stand off

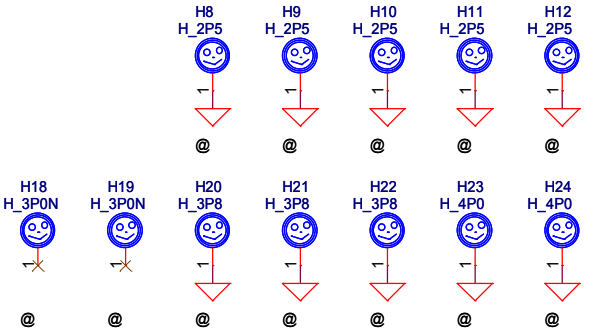


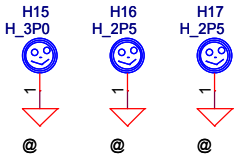
SSD Stand off

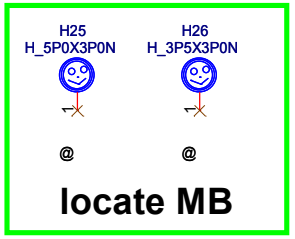


FAN Stand off

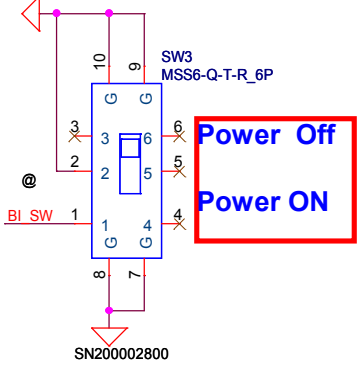


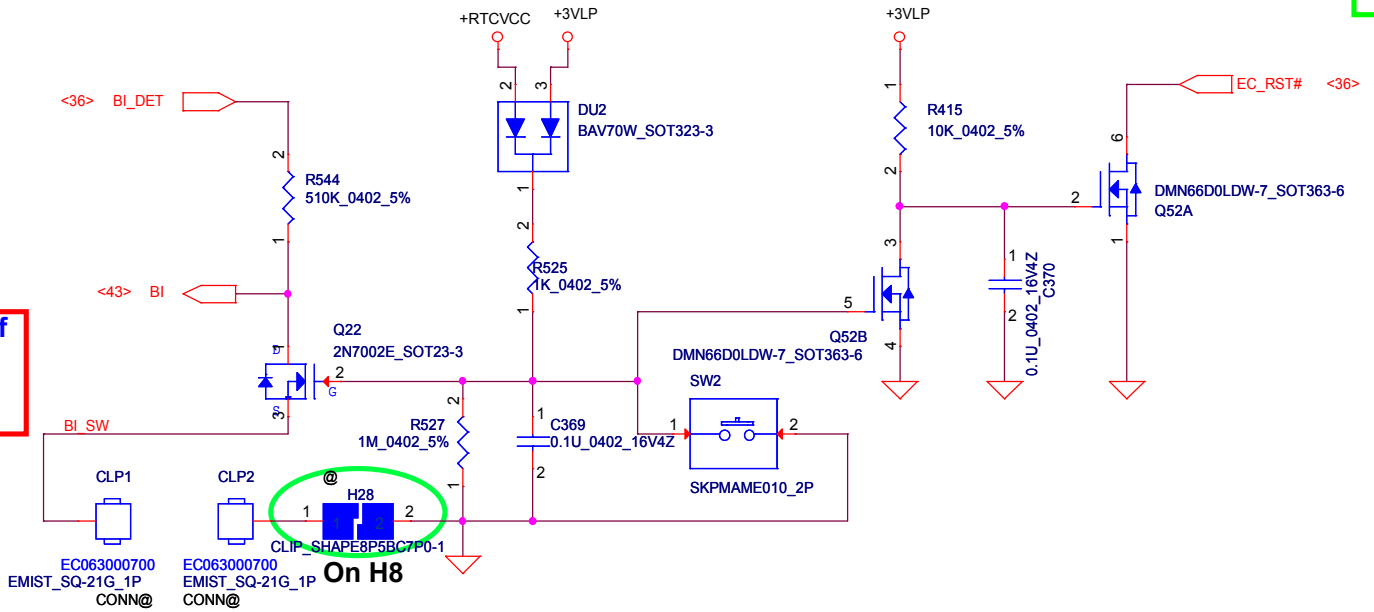


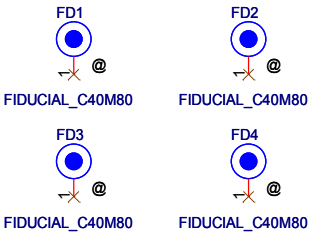




Debug SW







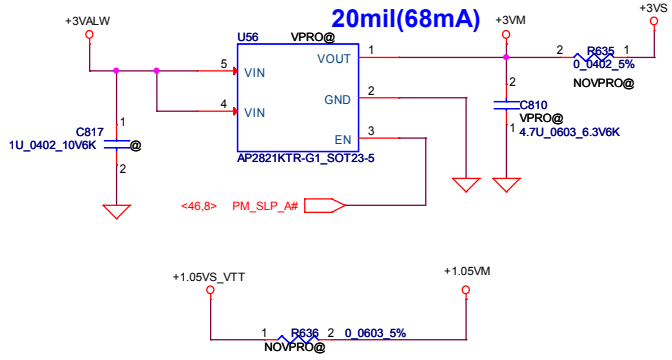
Security Classification	Compal Secret Data		
Issued Date	2012/07/20	Deciphered Date	2013/07/20

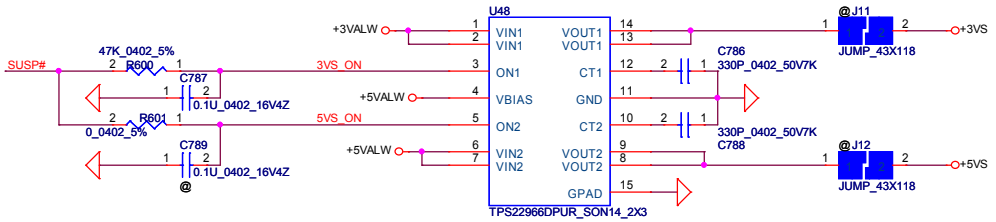
Compal Electronics, Inc.

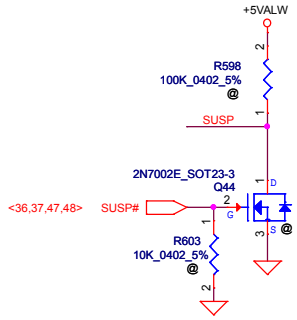
Title: **FAN & Screw**

Size	Document Number	Rev
Custom	V4DA2 M/B LA-9581P Schematic	1.0
Date: Monday, August 05, 2013	Sheet 39 of 57	

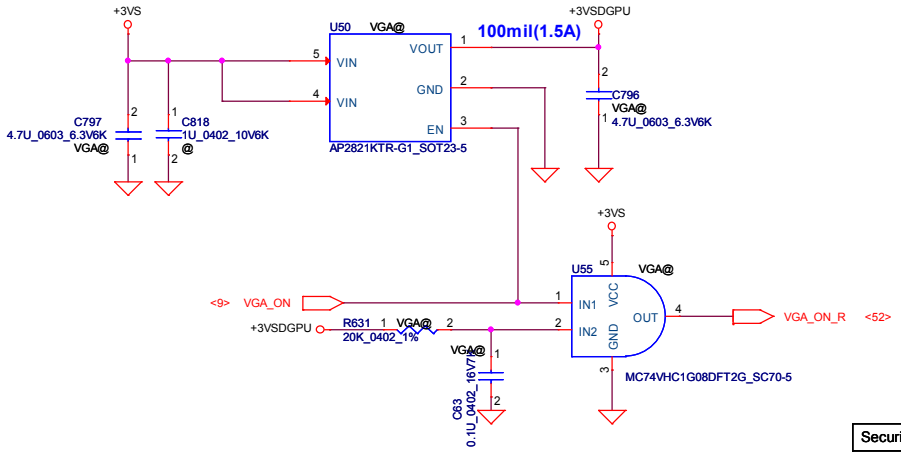
+3VALW to +3VM for Intel AMT

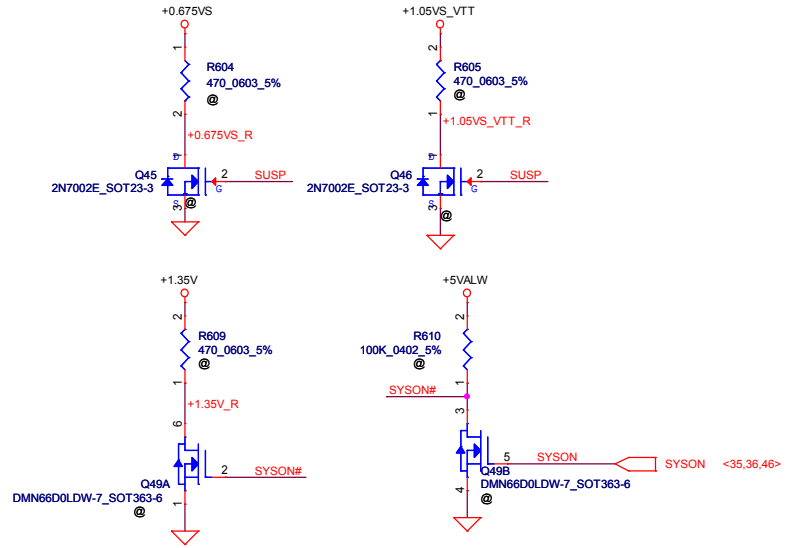






+3VS to +3VSDGPU for GPU





Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.

Title: DC Interface

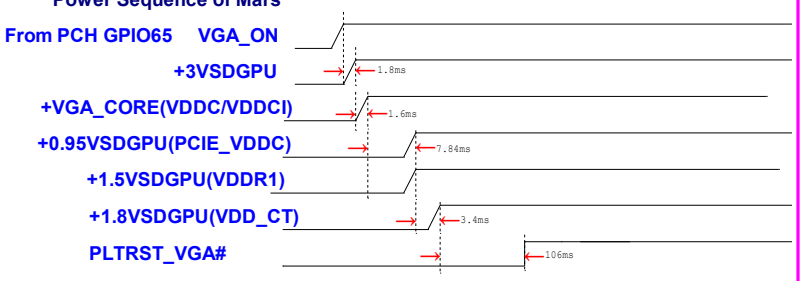
Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0

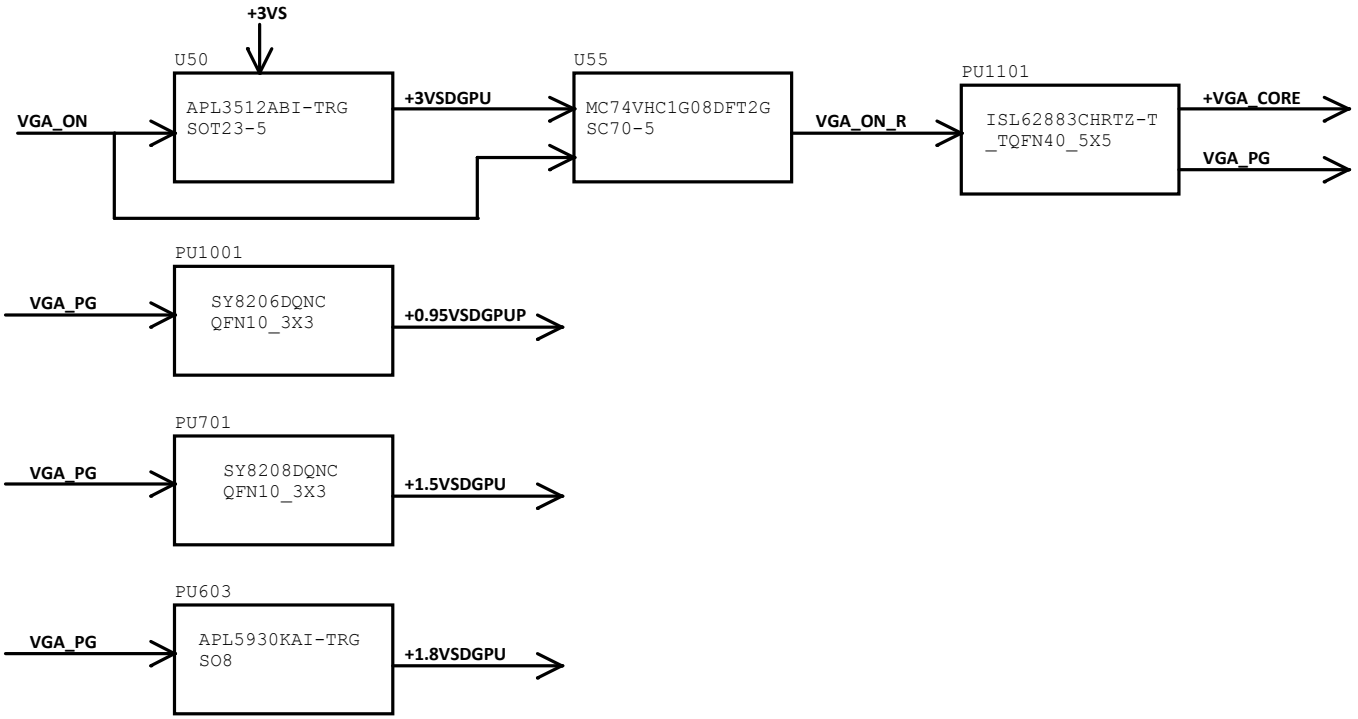
Date: Tuesday, July 30, 2013 | Sheet 40 of 57

Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
2. VDD_CT must remain powered whenever VDDR3 is powered.
3. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.
4. VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).
5. BIF_VDDC should always be tied to PCIE_VDDC.

Power Sequence of Mars





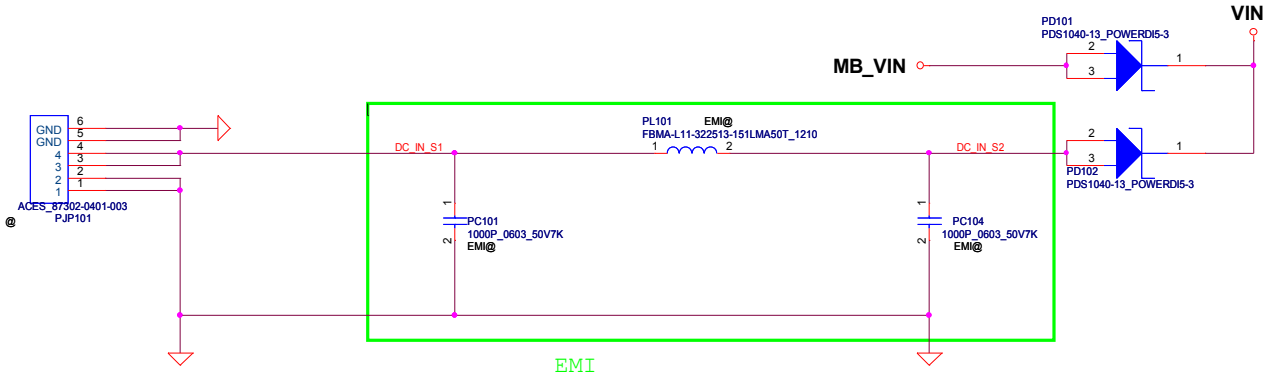
Security Classification	Compal Secret Data		
Issued Date	2012/07/20	Deciphered Date	2013/07/20

Compal Electronics, Inc.

Title: Mars_M2 Block Diagram

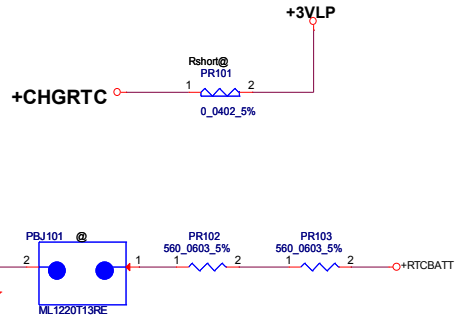
Size: Custom | Document Number: V4DA2 M/B LA-9581P Schematic | Rev: 1.0

Date: Tuesday, July 30, 2013 | Sheet 41 of 57



BOM Config

DDR3L	UMA	EMI@
	DIS	EMI@/VGA@/VGAEMI@



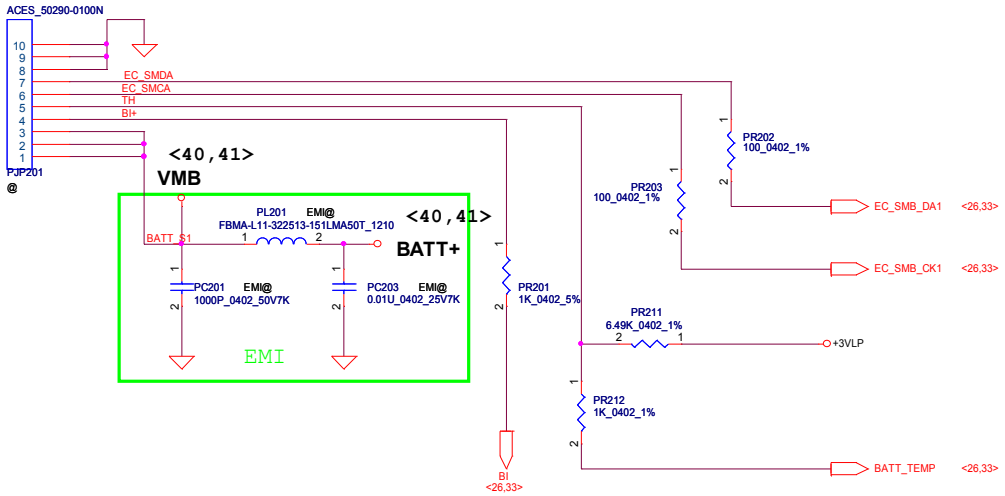
Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

Title: **DCIN**

Size	Document Number	Rev
Custom	*V4DA2 LAA131P Schematic*	1.0

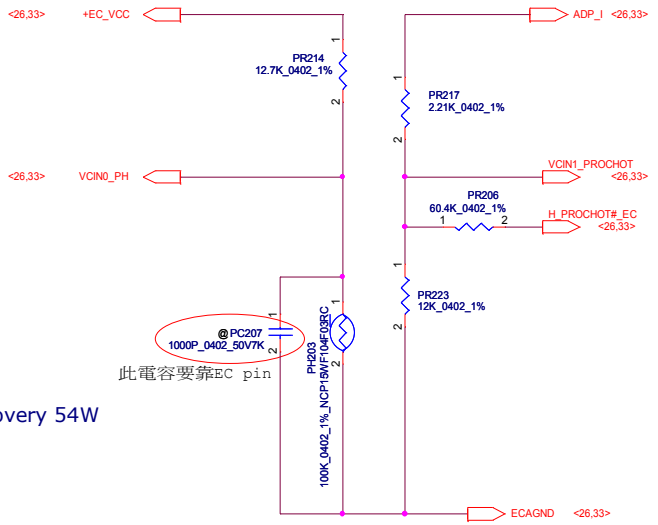
Date: Thursday, August 01, 2013 | Sheet 42 of 56



ENE9012	Action 70W (throttling)	Recovery 54W
ADP_I	1.466V	1.131V
VCIN1 (EC setting)	1.2V	1.025V

CPU thermal protection at 92 degree C
PH203 under CPU botten side :
(92 degree = 6.99K ohm) => VCIN0_PH = 1.2V
(56 degree = 26.02k ohm) => VCIN0_PH = 2.22V

(70W/19V)*19.9*20m =1.466V
1.466*10/12.21=1.2V



For 65W adapter==>action 70W , Recovery 54W

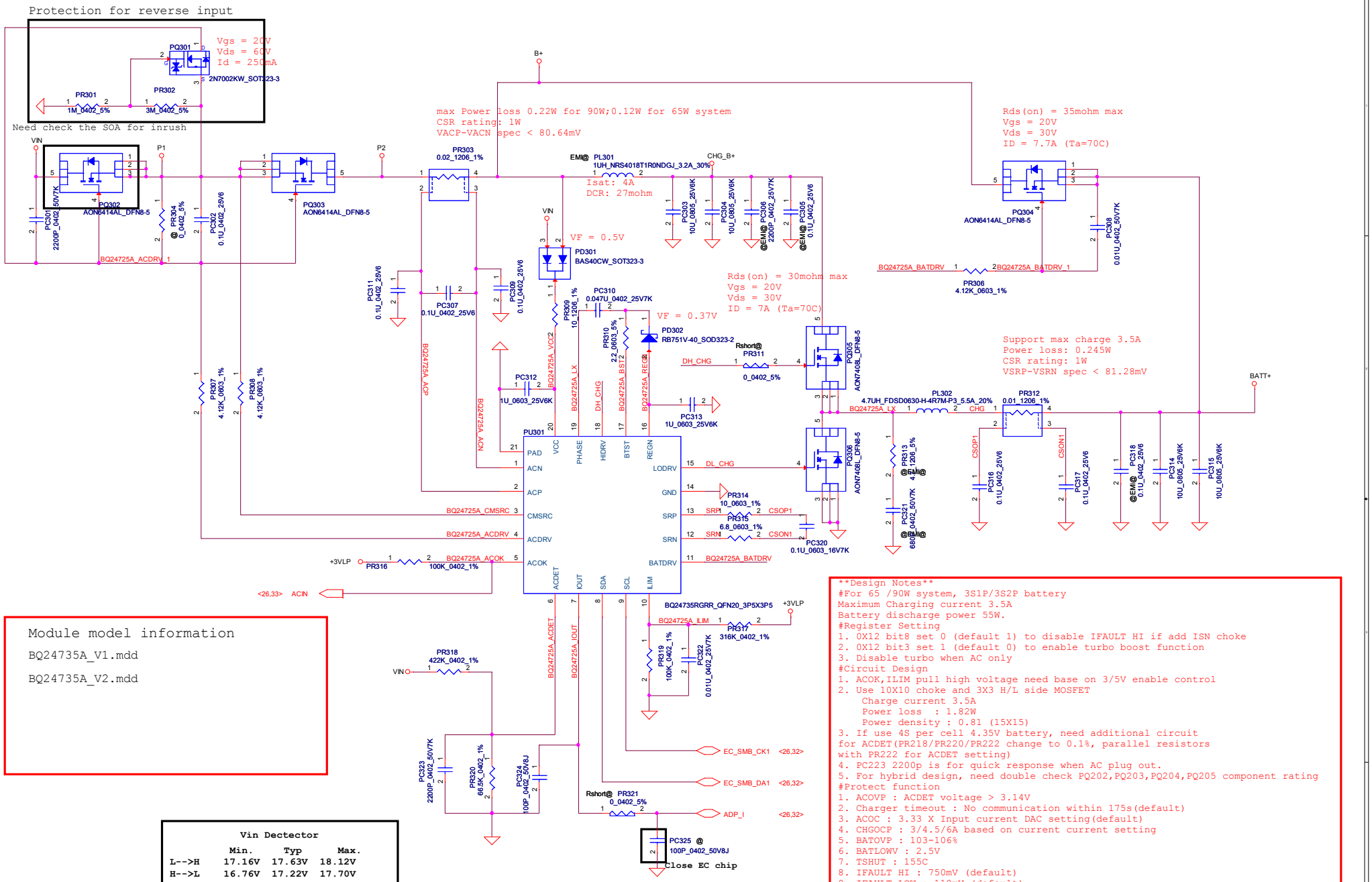
Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

Title: **BATTERY CONN / OTP**

Size	Document Number	Rev
Custom	*V4DA2 LAA131P Schematic*	1.0

Date: Thursday, August 01, 2013 | Sheet 43 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

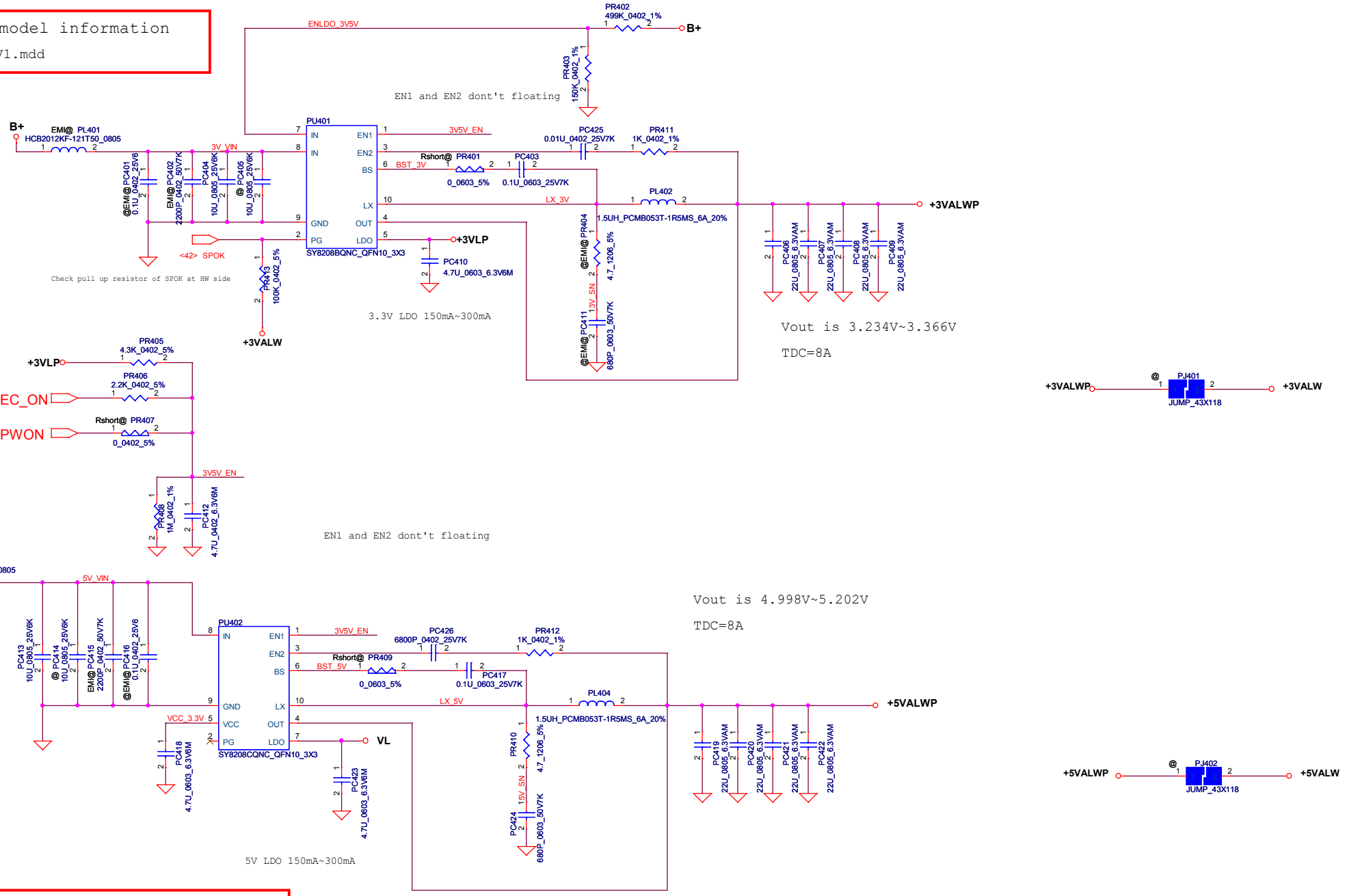
Title: CHARGER

Size: Custom | Document Number: V4DA2 LAA131P Schematic | Rev: 1.0

Date: Thursday, August 01, 2013 | Sheet 44 of 56

Module model information

SY8208B_V1.mdd



Module model information

SY8208C_V1.mdd

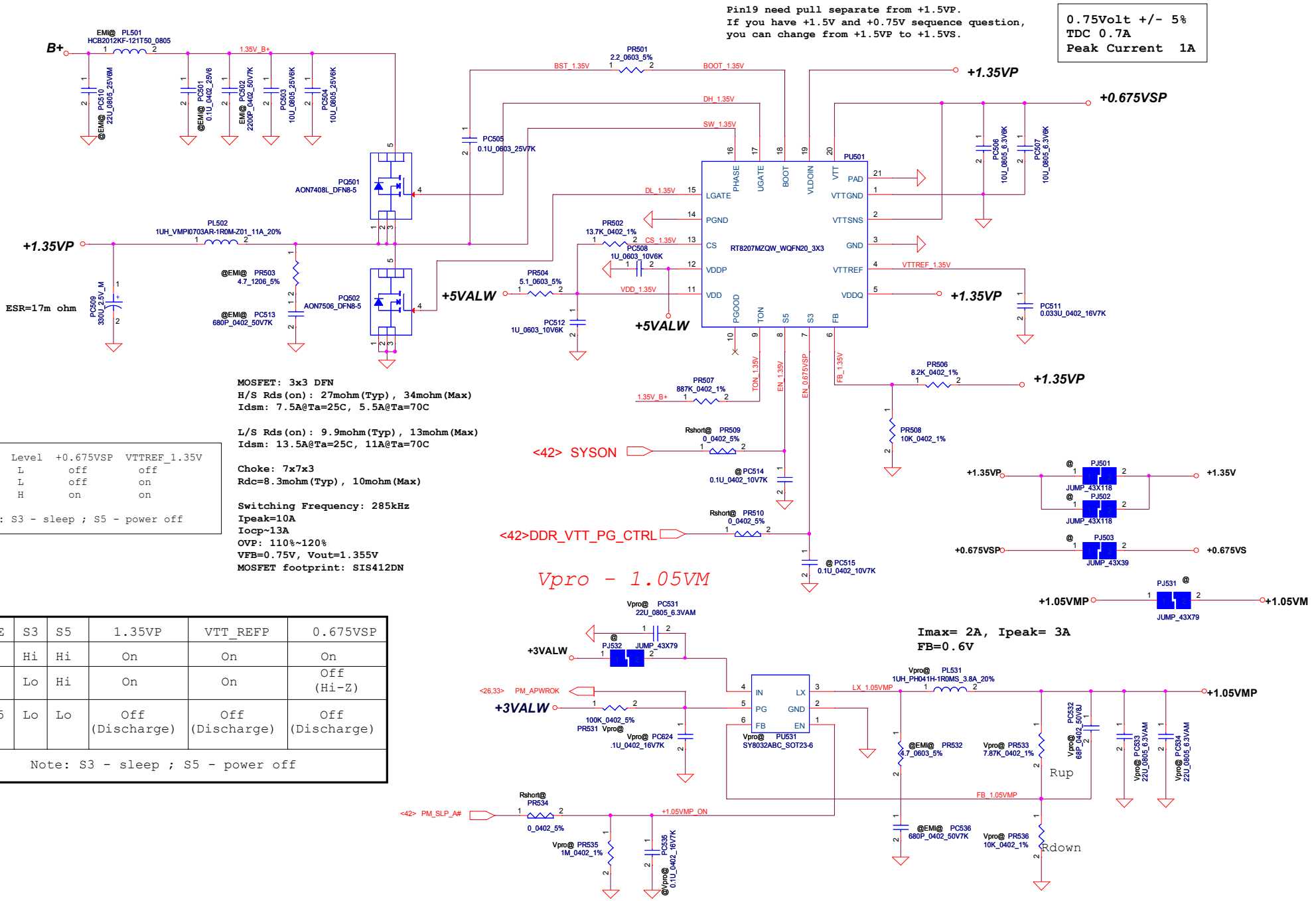
Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size: Custom | Document Number: V4DA2 LAA131P Schematic | Rev: 1.0

Date: Thursday, August 01, 2013 | Sheet 45 of 56



MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
VFB=0.75V, Vout=1.355V
MOSFET footprint: SIS412DN

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

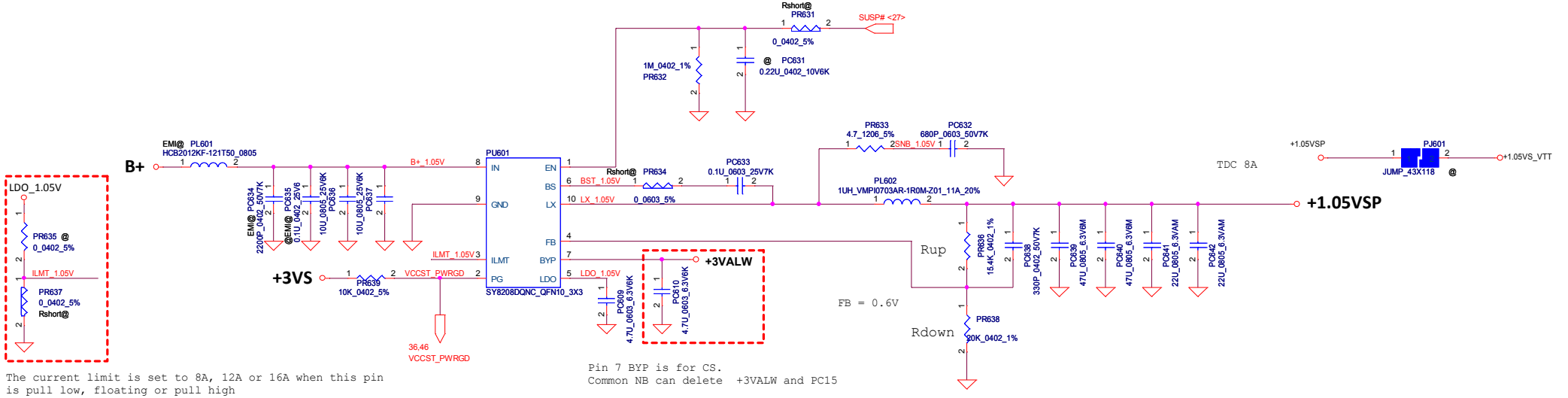
Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Title: 1.35VP/0.675VSP

Size	Document Number	Rev
Custom	V4DA2 LAA131P Schematic	1.0

Date: Thursday, August 01, 2013 Sheet 46 of 56

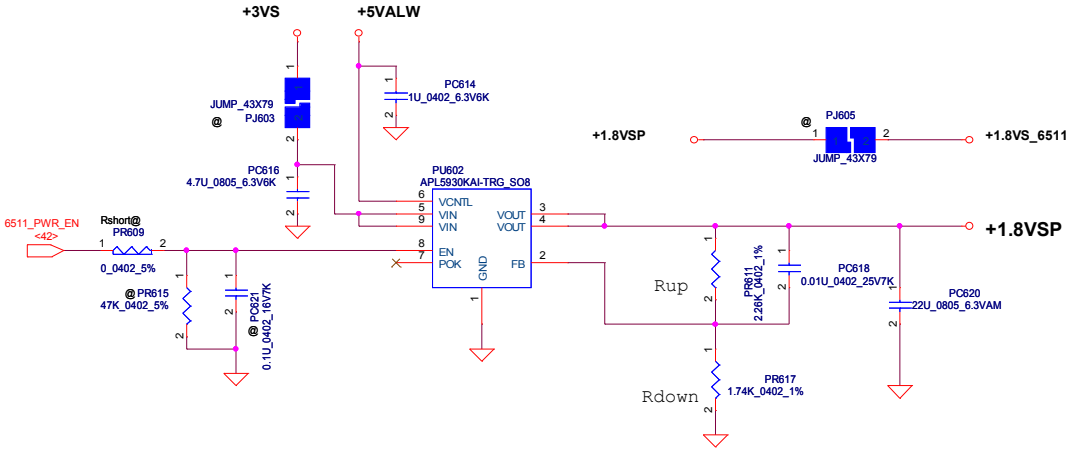
EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



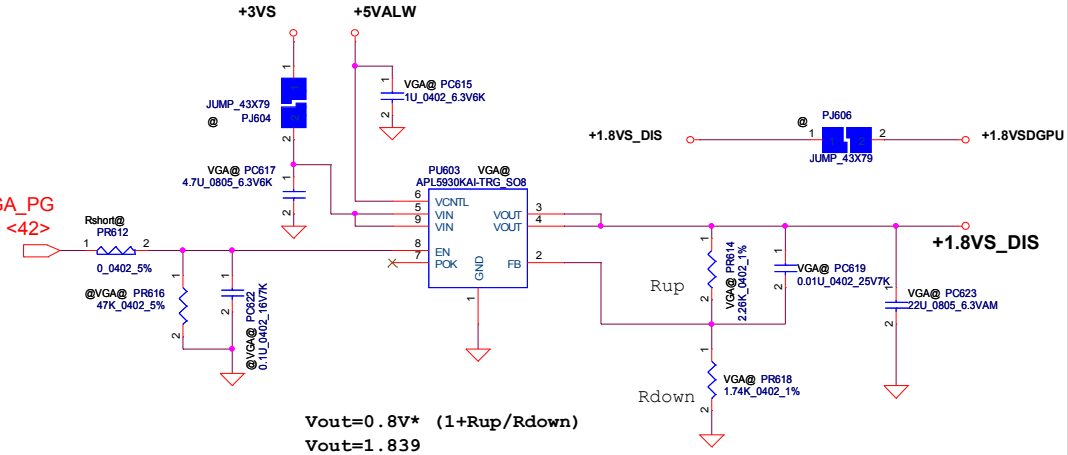
The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=1.062V



Vout=0.8V* (1+Rup/Rdown)
Vout=1.839
Ultra Low Dropout 0.23V(typical) at 3A Output Current



Vout=0.8V* (1+Rup/Rdown)
Vout=1.839
Ultra Low Dropout 0.23V(typical) at 3A Output Current

Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

Title: 1.05VS_VTT/1.8VS_6511/1.8VS_DIS

Size	Document Number	Rev
Custom	V4DA2 LAA131P Schematic	1.0

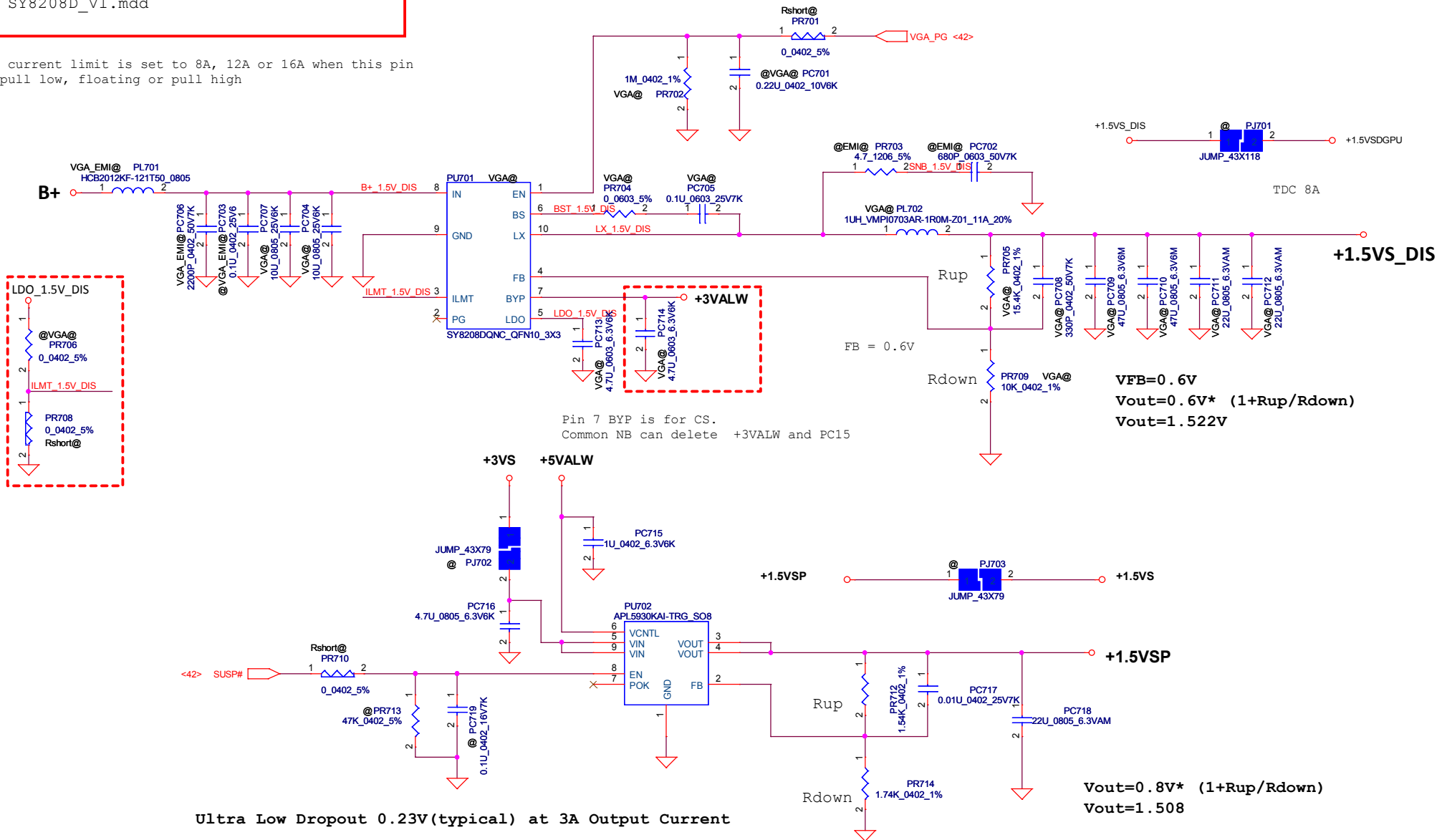
Date: Thursday, August 01, 2013 Sheet 47 of 56

Module model information

SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high



Ultra Low Dropout 0.23V(typical) at 3A Output Current

Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

Title: 1.5VSDGPUP/1.5VS

Size: | Document Number: V4DA2 LAA131P Schematic | Rev: 1.0

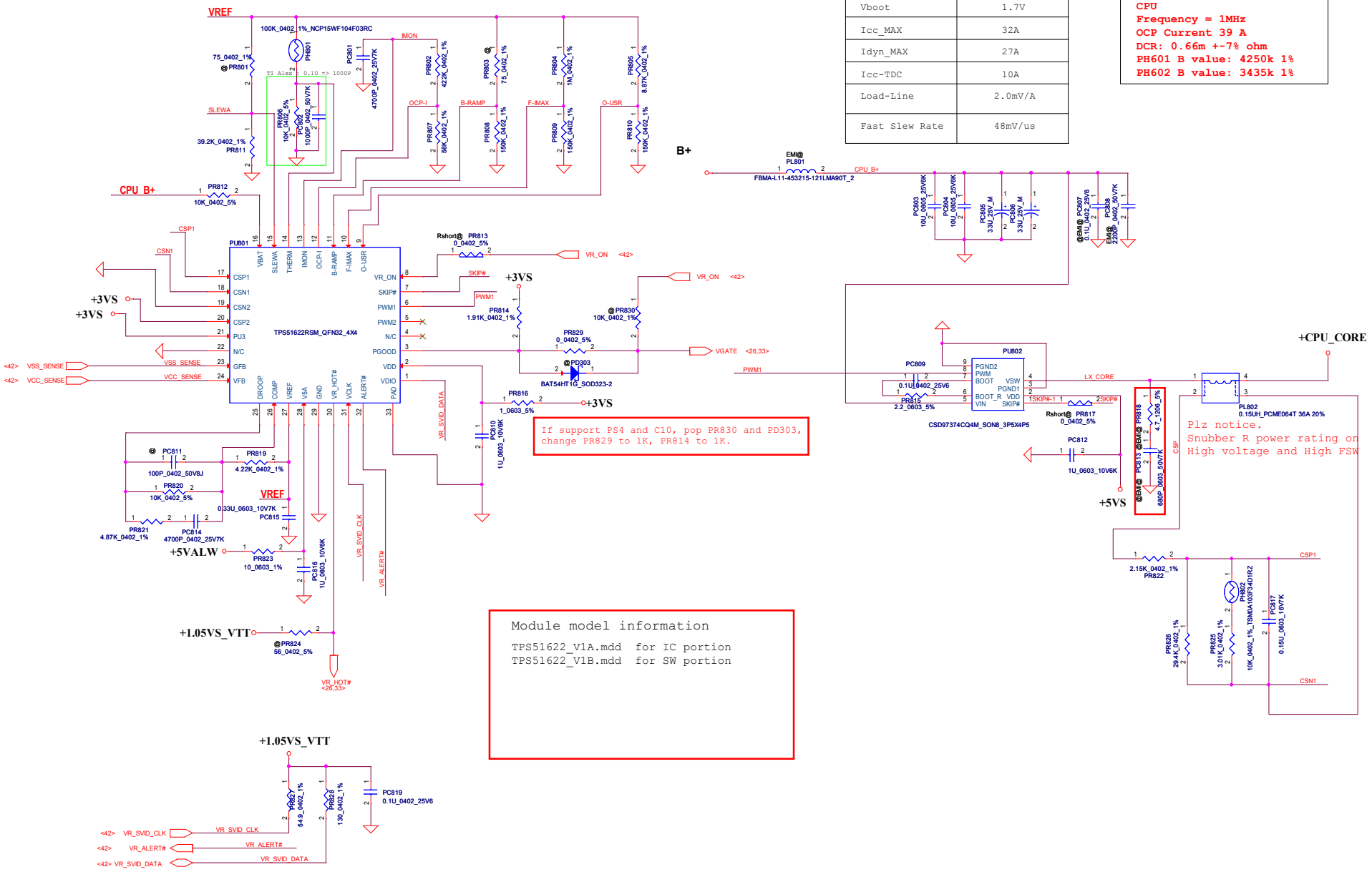
Date: Thursday, August 01, 2013 | Sheet 48 of 56

Follow Intel SB_ULT_PDDG 1.0

	Specifications
Vps0	1.8V
Vboot	1.7V
Icc_MAX	32A
Idyn_MAX	27A
Icc-TDC	10A
Load-Line	2.0mV/A
Fast Slew Rate	48mV/us

CPU
Frequency = 1MHz
OCP Current 39 A
DCR: 0.66m +-7% ohm
PH601 B value: 4250k 1%
PH602 B value: 3435k 1%

VR_HOT#
PR806 10K ohm for 100 degree
PR806 8K ohm for 110 degree



Module model information

TPS51622_V1A.mdd for IC portion
TPS51622_V1B.mdd for SW portion

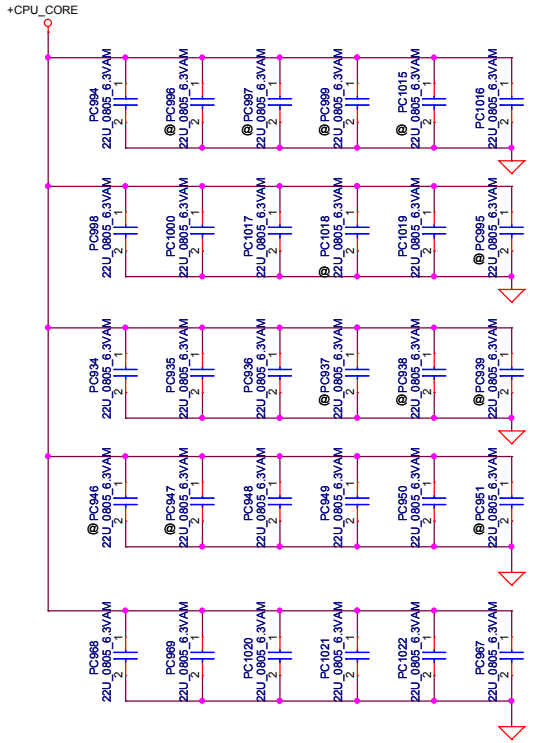
Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

Title: CPU_CORE

Size	Document Number	Rev
C	V4DA2 LAA131P Schematic	1.0

Date: Thursday, August 01, 2013 Sheet 49 of 56



CPU LL=2m ohm dedign 22uF *18, 22uF*12(un-pop)

Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

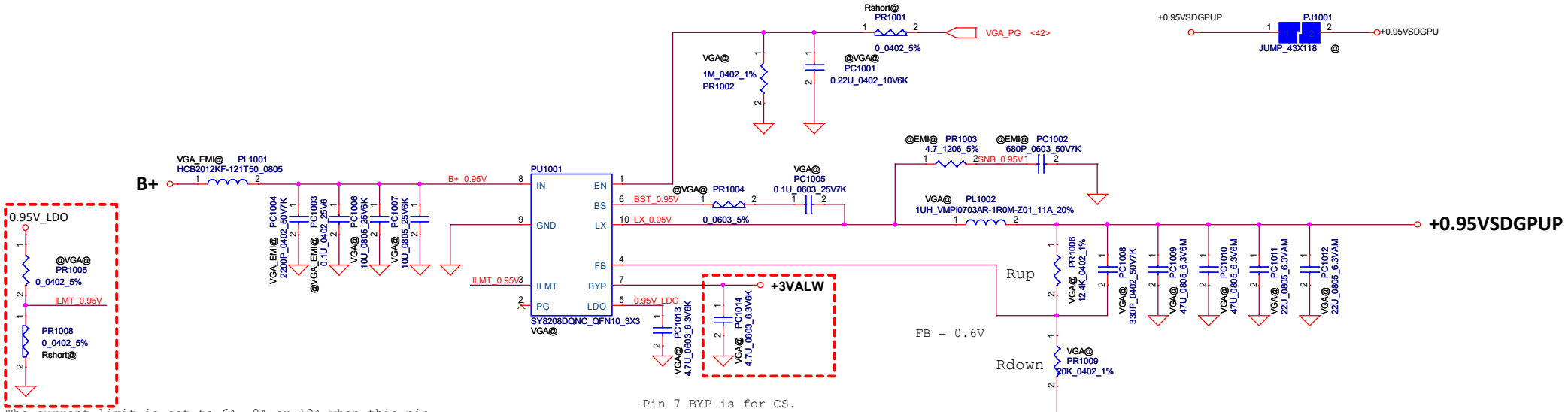
Compal Electronics, Inc.

Title: CPU_CORE_CAP

Size	Document Number	Rev
Custom	V4DA2 LAA131P Schematic	1.0

Date: Thursday, August 01, 2013 | Sheet 50 of 56

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=0.972

Security Classification	Compal Secret Data	Vout=1.05V	Compal Electronics, Inc.
Issued Date	2012/06/19	Deciphered Date	2012/07/31
Title	*0.95VSDGPUP*		
Size	Document Number		Rev
	V4DA2 LAA131P Schematic		1.0
Date: Thursday, August 01, 2013	Sheet 51 of 56		

VGA Chipset	Default Voltage	VID6	VID5	VID4	VID3	VID2	VID1	VID0
Mars	1.1V	0	1	0	0	0	0	0

boot resistor to 1.1V

Rds(on)
typ=2.7m Ω
max=3.3m Ω

Rds(on)
typ=2.7m Ω
max=3.3m Ω

LL Disable, Fsw = 300 kHz (typ)
Mars with turbo
I_TDC=25A
I_EDC =37.5A
I_OCP = 45A
VGA_CORE LL= disable
VGA_CORE cap = 330uF*3 (ESR 6m ohm)

Layout Note:
Place near Phase1 Choke

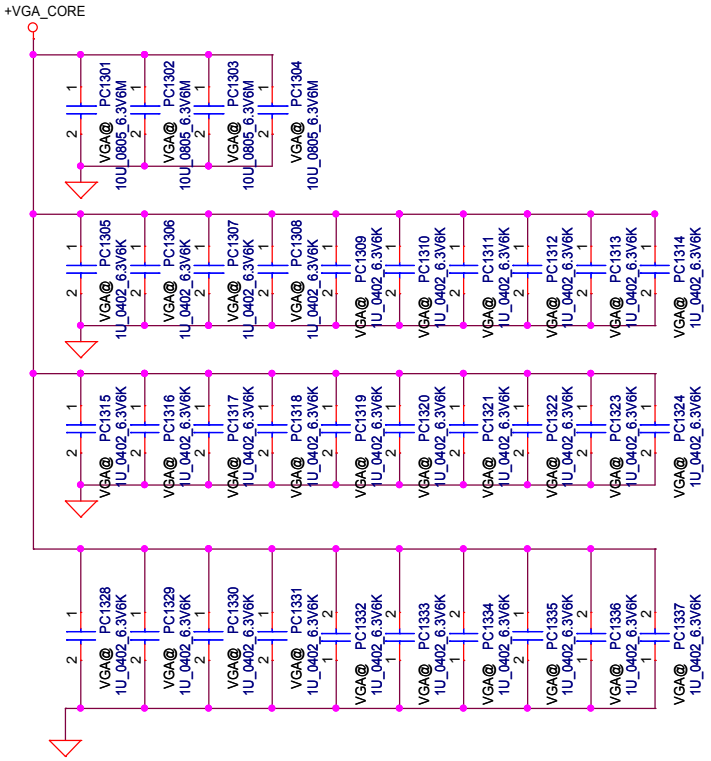
Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

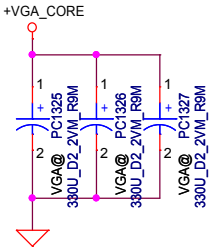
Compal Electronics, Inc.

Title: VGA_CORE

Size: Custom | Document Number: V4DA2 LAA131P Schematic | Rev: 1.0

Date: Thursday, August 01, 2013 | Sheet 52 of 56





AMD MARS
GPU_CORE
330uF*2
10uF*4+1uF*30

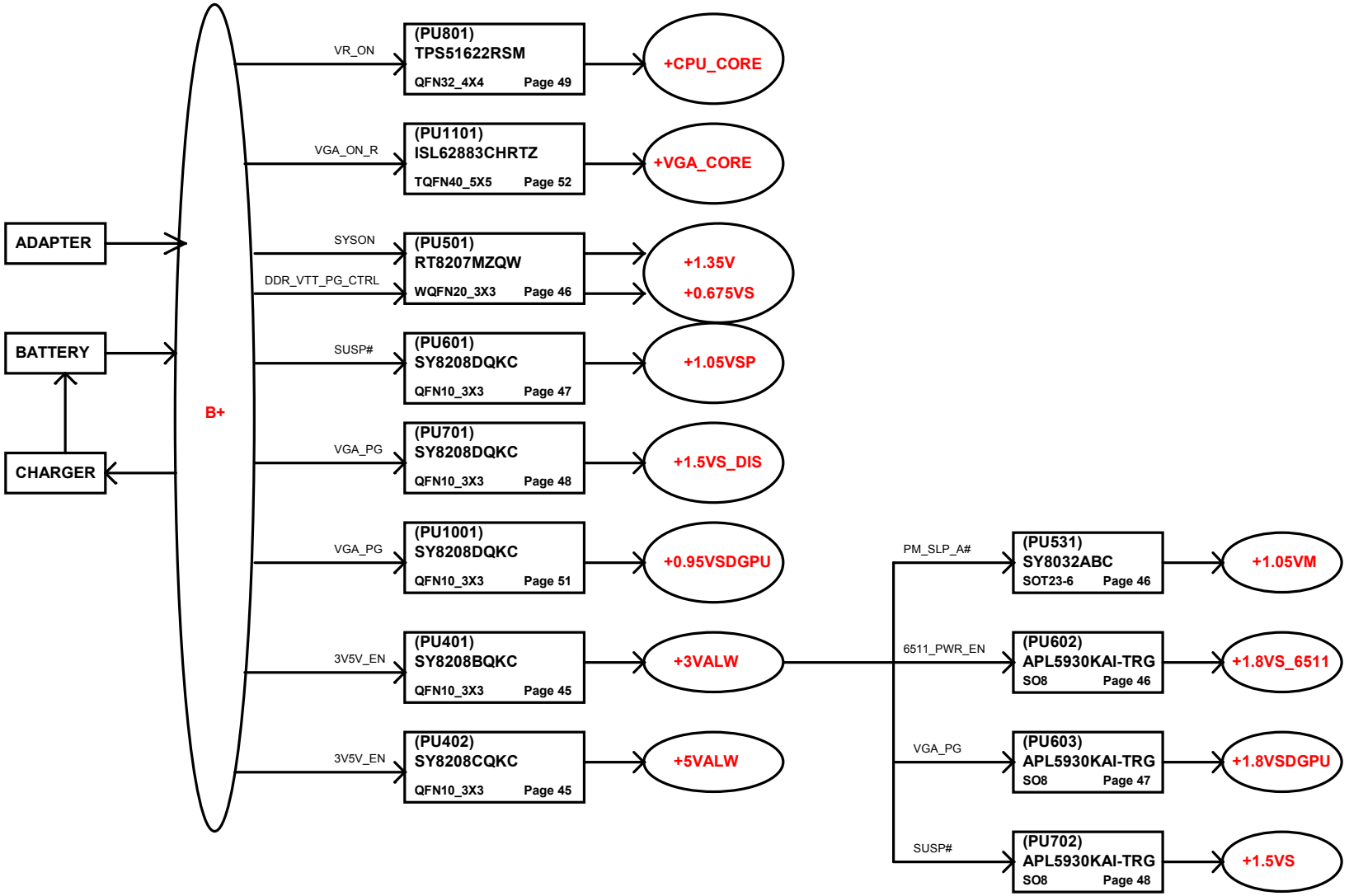
Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

Title: VGA_CORE CAP

Size: Custom | Document Number: V4DA2 LAA131P Schematic | Rev: 1.0

Date: Thursday, August 01, 2013 | Sheet 53 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

Title: Power Tree

Size: Custom | Document Number: V4DA2 LAA131P Schematic | Rev: 1.0

Date: Thursday, August 01, 2013 | Sheet 54 of 56

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01		change Cff to 6.8nF of SY8208C (5V) and 10nF if SY8208B (3V). The 5VALW will fast than 3VALW and the rising time will under 2mS.	0.2	45	Change PC425 From SE075472K80 - 4700P 25V K X7R 0402 to SE075103K80 - .01U 25V K X7R 0402	20130426	DVT
02		change Cff to 6.8nF of SY8208C (5V) and 10nF if SY8208B (3V). The 5VALW will fast than 3VALW and the rising time will under 2mS.	0.2	45	Change PC426 From SE075472K80 - 4700P 25V K X7R 0402 to SE075682K80 - 6800P 25V K X7R 0402	20130426	DVT
03		modify 1.35VP output voltage from 1.515V modify to 1.355V	0.2	46	Change PR506 From SD028102280 - 10.2K +-1% 0402 to SD034806180 - 8.06K +-1% 0402	20130426	DVT
04		modify 1.05VMP output voltage from 1.2V modify to 1.0722V	0.2	46	Change PR533 From SD034200280 - 20K +-1% 0402 to SD034787180 - 7.87K +-1% 0402	20130426	DVT
05		modify 1.8VSP and 1.8VS_DIS output voltage from 1.508V modify to 1.839V	0.2	47	Change PR611, PR614 From SD034154180 - 1.54K +-1% 0402 to SD034226180 - 2.26K +-1% 0402	20130426	DVT
06		modify 1.5VSP output voltage from 1.05V modify to 1.5V	0.2	48	Change PR709 From SD034200280 - 20K +-1% 0402 to SD034100280 - 10K +-1% 0402	20130426	DVT
07		modify 0.95VSDGPUP output voltage from 1.05V modify to 0.972V	0.2	51	Change PR1006 From SD034150280 - 15K +-1% 0402 to SD00000AJ80 - 12.4K +-1% 0402	20130426	DVT
08		CPU_CORE choke DCR from 0.85m ohm adjust to 0.66m ohm, modify component to setting VREF, OCP,etc.	0.2	49	Change PR819 from SD034487100 - 4.87K +-1% 0402 to SD00000J280 - 4.32K +-1% 0402 Change PR826 from SD034200280 - 20K +-1% 0402 to SD034523280 - 52.3K +-1% 0402 Change PR822 from SD034226180 - 2.26K +-1% 0402 to D034210180 - 2.1K +-1% 0402 - Change PR807 from SD034390280 - 39K +-1% 0402 to SD034560280 - 56K +-1% 0402 Change PR802 from SD034365380 - 365K +-1% 0402 to SD034442300 - 442K +-1% 0402 Change PC817, PC818 to PC817 from SE076823K80 - 0.082U 16V K X7R 0402 to SE00000X80 0.15U 16V K X7R 0603	20130524	DVT
09		modify 1.05VSP output voltage from 1.05V modify to 1.062V for EA test voltage drop under 1.05V	0.2	47	Change PR636 From SD034150280 - 15K +-1% 0402 to SD034154280 - 15.4K +-1% 0402	20130524	DVT
10		modify 1.5VS_DIS output voltage from 1.5V modify to 1.522V for EA test voltage drop under 1.5V	0.2	48	Change PR705 From SD034150280 - 15K +-1% 0402 to SD034154280 - 15.4K +-1% 0402	20130524	DVT
11		modify VGA output capacitor from 560U*1+330U*2 reduce to 330U*3 static Pk-Pk ripple from 32.12mV up to 35.63mV dynamic Pk-Pk ripple from 88mV up to 94mV.	0.2	48	Change PC1327 From SGA00006J00 - 560U 2V M D2 LESR4.5M SX H1.9 to SGA00006100 - 330U 2V M D2 ESR9M S H1.9	20130524	DVT
12		modify 1.05VS/1.5VSDGPU/0.95VSDGPU choke from 1.5U change to 1U, for efficiency heavy load improve 1.05V => from 83.2% to 85.5% 1.5V => from 83.7% to 85.5% 0.95V => from 80.6% to 84.8%	0.2	47, 48, 51	Change PL602, PL702, PL1002 From SH000008800 - 1.5UH +-20% PCMC063T-1R5MN 9A to SH00000KS00 - 1UH +-20% VMPI0703AR-1R0M-Z01 11A	20130524	DVT
13		Part count reduce PR609, PR612, PR710; PR615, PR616, PR713; PC621, PC622, PC719 are +1.5VS/1.8VS/1.8VSDGPU enable RC.	0.3	47, 48	Change PR609, PR612, PR710 change to Rshort@ From SD028100380-S RES 1/16W 100K +-5% 0402 to SD028000080-S RES 1/16W 0 +-5% 0402 Un-pop PR615, PR616, PR713 From SD028470280 - S RES 1/16W 47K +-5% 0402 to un-pop Un-pop PC621, PR622, PC719 From SE076104K80 - S CER CAP .1U 16V K X7R 0402 to un-pop	20130531	PVT
14		Part count reduce PR824 is VR-HOT# pull high resistor, beacuse there have a 0 ohm between VR_HOT# and H_PROCHOT#, H_PROCHOT# also have a pull high voltage, discuss with HW, we could un-pop PR824	0.3	49	Un-pop PR824 From SD028560A80 - S RES 1/16W 56 +-5% 0402 to un-pop	20130531	PVT

Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

Title: PIR (PWR)

Size	Document Number	Rev
Custom	V4DA2 LAA131P Schematic	1.0

Date: Thursday, August 01, 2013 | Sheet 55 of 56

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
15		modify 1.35VP output voltage from 1.3515V modify to 1.365V	0.3	46	Change PR506 From SD034806180 - 8.06K +-1% 0402 to SD000004100 - 8.2K +-1% 0402	20130606	PVT
16		part count reduce	0.3	45 47 51	Change PR401, PR409, PR634, PR1004 From SD013000080 - 0_0603_5% to R_short	20130606	PVT
17		part count reduce	0.3	44,46 47,48 51,52	Change PR311, PR534, PR631, PR635, PR701, PR706, PR1001, PR1008, PR1115, PR1150, PR1154, PR1155, PR1156 From SD028000080 - 0_0402_5% to R_short	20130606	PVT
18	PS51622 which might cause system hang when exit C10 with PS4. TI solution : RC filter to ignore the ~4us glitch on PGOOD.	TI suggest, If support PS4 and C10, pop PR830 and PD303, change PR829 to 1K, PR814 to 1K.	0.3	49	reserve PD303, SCS00003M00 - SCH DIO BAT54HT1G SOD323 reserve PR830, SD034100280 - 10K +-1% 0402 Add PR829, SD034100180 - 0 +-5% 0402	20130628	PVT
19		MOS AON7702A EOL	0.3	46	Change PQ502 from SB00000T600 - AON7702A 1N DFN to SB000010A00 - AON7506 1N DFN	20130628	PVT
20		Finetune RC for CPU Transient Voltage Testing	0.3	49	Change PR819 from SD00000J280 - 4.32K +-1% 0402 to SD034422180 - 4.22K +-1% 0402 Change PR822 from SD034210180 - 2.1K +-1% 0402 to SD034215180 - 2.15K +-1% 0402 Change PR826 from SD034523280 - 52.3K +-1% 0402 to SD034294280 - 29.4K +-1% 0402 Change PR802 from SD034442300 - 442K +-1% 0402 to SD034422380 - 422K +-1% 0402	20130628	PVT
21		part count reduce output capacitor reference CPU Transient Voltage Testing	0.3	49	Change PC1005, PC938, PC939, PC946, PC951, PC997 from SE000008L80 - CER CAP 22U 6.3V M X6S 0805 H1.25 to un-pop	20130628	PVT
22		EMT test 5V and 1.05VS, Main source SY8208C/D could PASS, but 2nd source SY8206C/D fail, EMI add snubber the both could PASS.	0.4	45, 47	Add EMI solution Snubber at 5V and 1.05VS PC424 680pF, PC632 680pF PR410 4.7 ohm, PR633 4.7 ohm	20130731	PVT2/ Pre-MP
23							
24							
25							
26							
27							
28							

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: V4DA2 LAA131P Schematic | Rev: 1.0

Date: Thursday, August 01, 2013 | Sheet 56 of 56

EVT-->DVT Change List

1.page36, pin 68 and pin 21 SWAP and pin 89 and pin 17
2.page30, R407,R408,change to 1K and R439 connect to JMINI3.51 and R439 change to 240 ohm
3.page28, R478, R482 change to mount
4.page39, R527 change to 1M
5.page33, R592 and R593 change to 60.4 ohm
6.page27, remove C248,C253,C404,C405,QA2,RA5,RA6,RA7,RA8,U45
update U11 and add T39
add R645 ,R646 ,L12,L13
U11.16 connect to +5VS
C782 connect to +5VS
add R647 and R648
R647 and R648 change to @
R645 ,R646 change to SD028100A80
C249 and C251 change to mount
7.page26, RA12 and RA14 mount ,RA16 and RA18 un-mount
RA2,RA3,RA4,RA9 mount
RA32 change to 93.1 ohm
CA22 and CA21 change to SE071150J80
8.page30, JNFC1.15 connect to GPIO 17
R637 change to unmount ,R640 change to mount
9.page37, add C814 and C814 change to 1UF
10.page30, JMINI3.44 connect to UU1.L2 and add R657 ,R658
11.page32, T36 change PN to SP050007E00
12.page34, R620 change to 470K

ESD modify
1.page37, add R649~R656

DVT-->PVT Change List

1.page36, remove JIO2
2.page27, L6,L8,L10,L12,L13 from SM01000GA00 change to SM01000FH00 for downsize of source suggest
3.page36, L40,L41,L44,L45,L46,L47 from SM010015410 to SM01000N000 for downsize of source suggest
4.page33, L31 from SM010017710 to SM01000FH00 for downsize of source suggest
5.page26, LA2 from SM010030010 to SM010028100 for downsize of source suggest
6.page19,21 LV1,LV2,LV3,LV7,LV8,LV9 from SM010030010 to SM010028100 for downsize of source suggest
7.page25, U44 from SA00003AR00 to SA00006EE00 for cost down
8.page34, U46 from SA00003AR00 to SA00006EE00 for cost down
9.page40, U50 and U56 from SA00003AR00 to SA00006EE00 for cost down
10.page31, UL3 from SA00003AR00 to SA00006EE00 for cost down
11.page37, C814 change to SE000000K80 for downsize
12.page33, add R659 and R660 for audio suggest
13.page27, R645 and R646 change to 33 ohm for CRT overshoot
14.page33, L31 change to SM01000II00 for downsize of source suggest
15.page38, update JLID1 pin define
16.page34, update C803 ,C804,C805 SN to SGA00000Y80

ESD modify
1.page38 add 831
2.page38 add C820~830
3.page15 add CU186 (@ESD@)
4.page8, add CU187 (@ESD@)

PVT-->Per-MP Change List

1.page30, JNFC1 SWAP
2.page38, C480 and JTP1.4 connect to +3VS
3.page8, JAPS.11 connect to ON/OFFBTN#
4.page31,add RU176 to @
5.page9, RPU19.8 and UU1.AG5 connect to DET_SIG#_R_1
6.page9, add RU176
7.page35, JIO1.1 connect to +3VALW and reserve +3VS ,add R661 and R662
8.page27, L6,L8,L10,L12,L13 from SM01000FH00 change to SM01000GA00
9.page35, add U60 ,C833, C832 ,R666,R661
10.page34, add R664 ,D38,R663
11.page33, R659 and R660 change to 0 ohm
12.page38, C826~C829 change to @
13.page36, L40 and L41 change to SM01000DS00 (NBQ100505T-800Y)
14.page33, L44~L47 change to SM01000DS00 (NBQ100505T-800Y)
15.page36, R483 change to 20K
16.page38, SW1 to @
17.page39, SW3 to @
18.page7, add second source
19.page28, R478 un-mount ,R448 mount

Title: PIR(HW)		
Size: A	Document Number: V4DA2 LAA131P Schematic	Rev: 1.0
Date: Monday, August 05, 2013	Sheet 57 of 57	