

Compal Confidential

NAYF0 M/B Schematics Document

Intel Arrandale/Clarkfield Processor with DDRIII + Ibex Peak-M

2009-08-27

REV: 0.1

PCB

ZZZ
DAZ@
DA80000GT00

NAYF0 LA-5881P REV0 M/B
LA-5881P MB Rev0: DA80000GT00

VRAM PARK

ZZZ
VRAM PARK@
X76193BOL01
512M HIX

VRAM MAD

ZZZ
VRAM MAD@
X76193BOL03
1G HIX

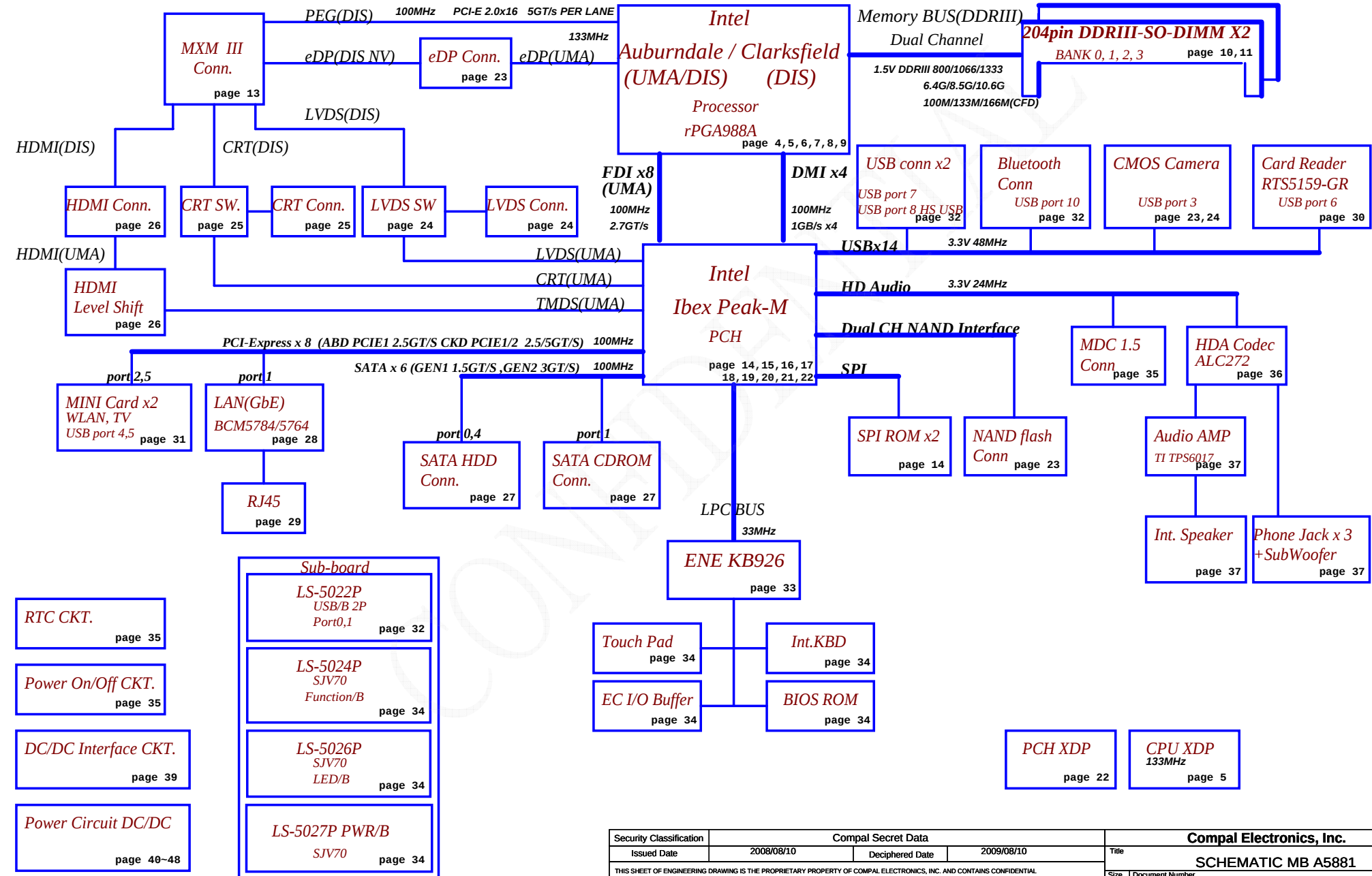
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Model Name : NAYF0
File Name : LA5881

Fan Control
page 38

Clock Generator
IDT: 9LRS3199AKLFT
SILEGO: SLG8SP587
133/120/100/96/14.318MHZ to PCH
48MHZ to CardReader
page 12



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for PCH	ON	ON	ON
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5V	5V power rail for PCH	ON	ON	ON
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
ISL90727	0101 1100b
ISL90728	0111 1100b

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	ClOCK
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra/Rc/Re	100K +/- 5%				
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0	0 V	0 V	0 V	
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

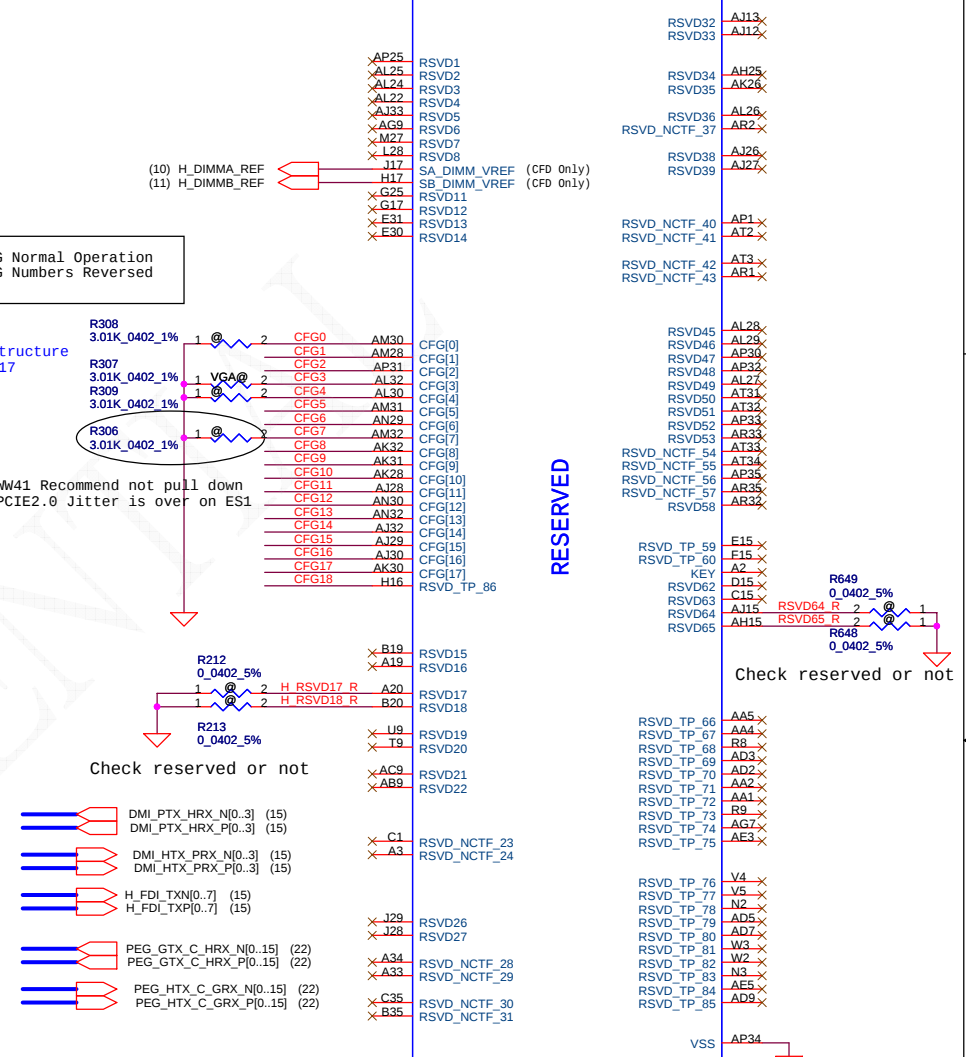
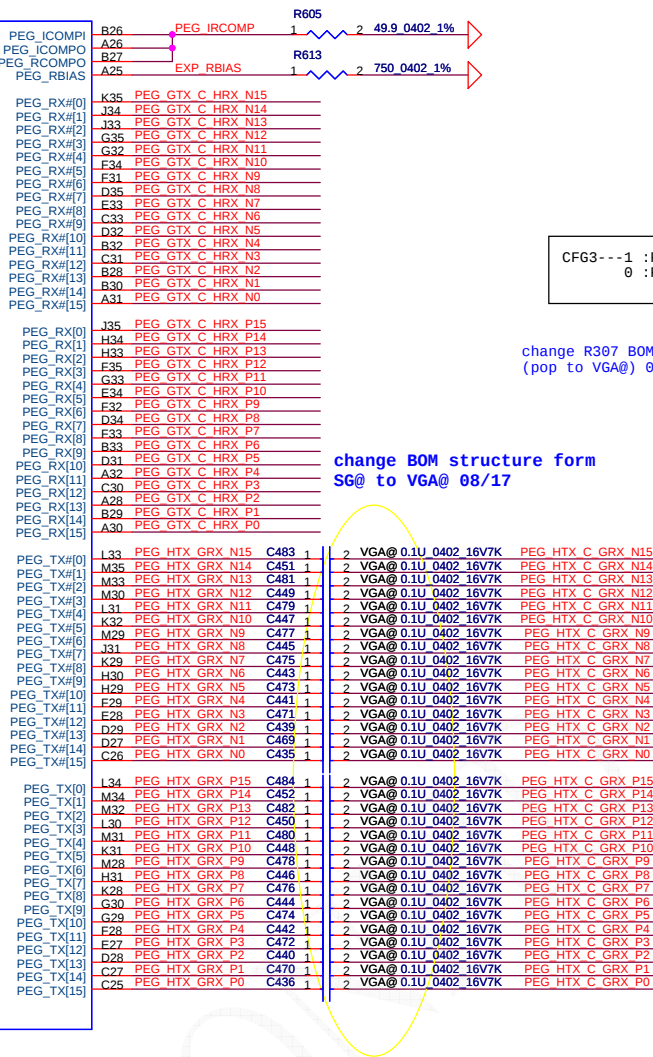
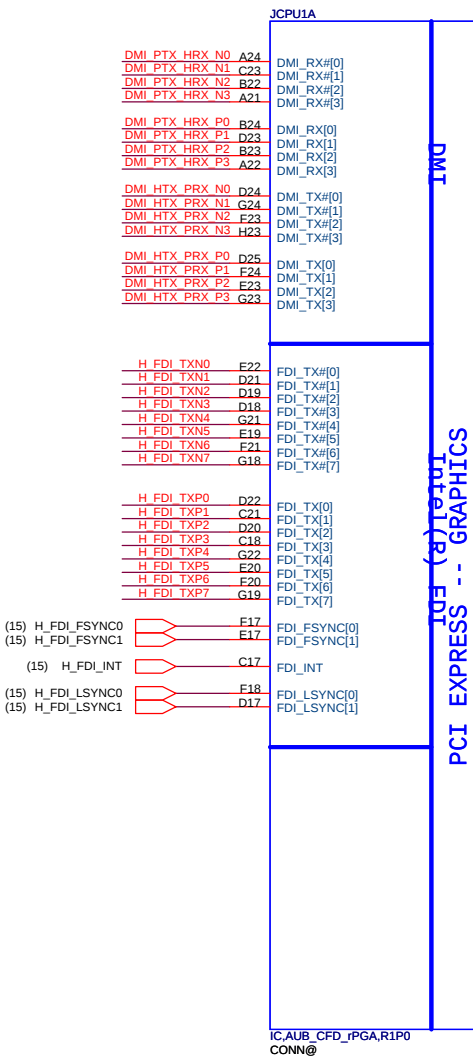
BTO Item	BOM Structure
ALC 271	271@
ALC 272	272@
ASM1442	ASM@
CH7318	CH@
S3	S3@
NONS3	NONS3@
XDP	XDP@
Switchable	SG@
VGA	VGA@
UMA	UMA@
UMAO	UMAO@
DISO	DISO@
MADISON	MAD@
PARK	PARK@
VRAM MADISON	VRAM MAD@
VRAM PARK	VRAM PARK@

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port	3 External USB Port
EHCI1	UHCI0	0	Ext1 USB	Ext1 USB
		1	Ext2 USB	Ext2 USB
	UHCI1	2	Ext3 USB (JV only)	
		3	Camera	Camera
	UHCI2	4	1st Min-Card	1st Min-Card
		5	2st Min-Card	2st Min-Card
EHCI2	UHCI3	6	Card Reader	Card Reader
		7	Ext3 USB (JM only)	
	UHCI4	8	Ext4 HS USB	Ext3 HS USB
		9		
	UHCI5	10	Blue Tooth	Blue Tooth
		11		
	UHCI6	12		
		13		

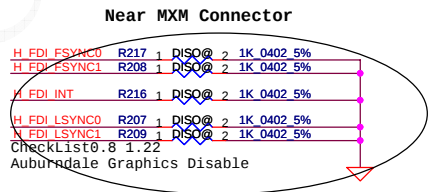
BOM Config
UMA only SKU:UMAO@/UMA@
Switchable PARK SKU: SG@/VGA@/PARK@/VRAM PARK@
Switchable MADISON SKU: SG@/VGA@/MAD@/VRAM MAD@
The same: 272@/ASM@/NONS3@/DAZ@

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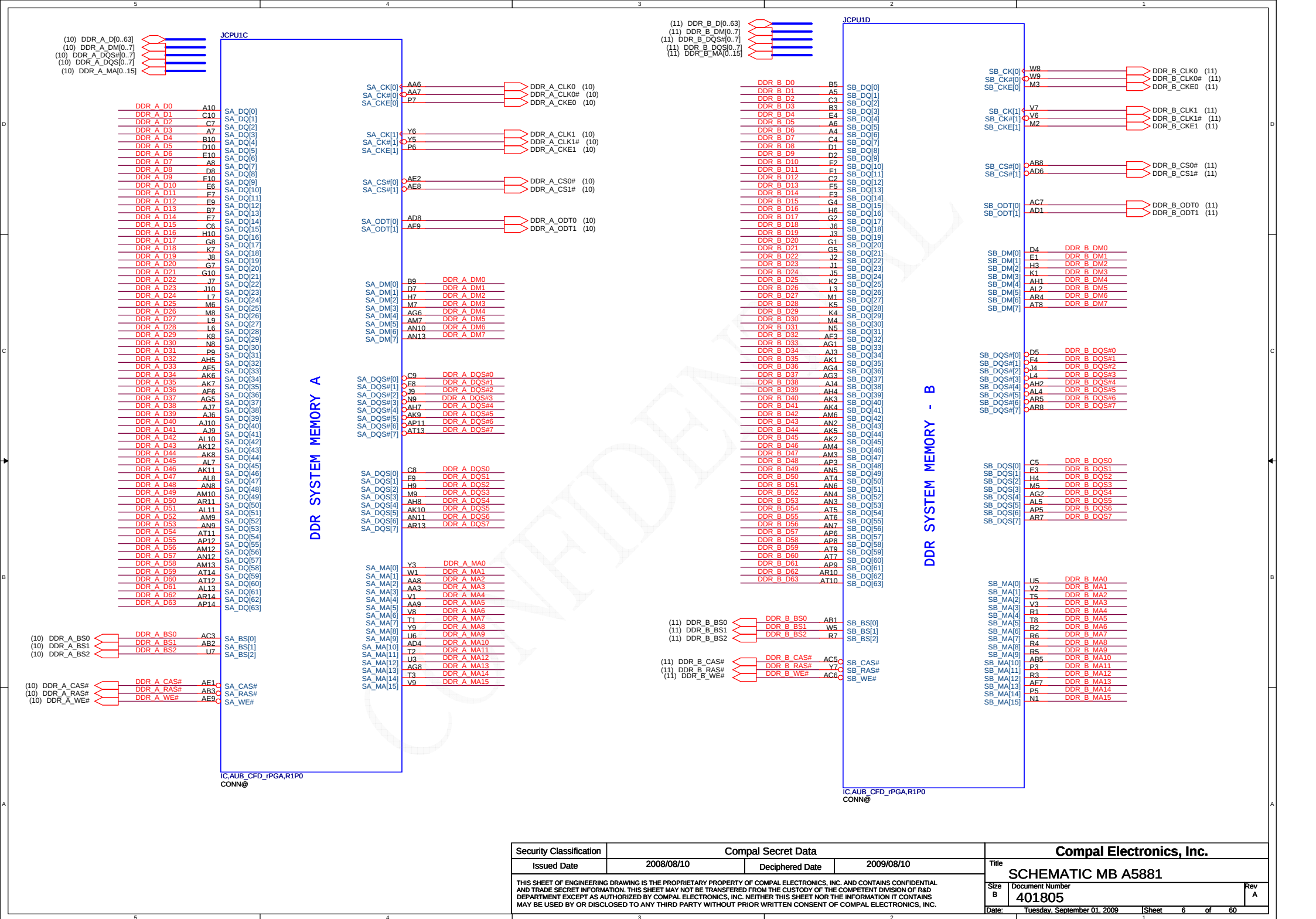
eDP Signals MAPPING

eDP Signal	PEG Singals	Lane Reversal
eDP_TX0	PEG HTX C GRX_P15	PEG HTX C GRX_P0
eDP_TX#0	PEG HTX C GRX_N15	PEG HTX C GRX_N0
eDP_TX1	PEG HTX C GRX_P14	PEG HTX C GRX_P1
eDP_TX#1	PEG HTX C GRX_N14	PEG HTX C GRX_N1
eDP_TX2	PEG HTX C GRX_P13	PEG HTX C GRX_P2
eDP_TX#2	PEG HTX C GRX_N13	PEG HTX C GRX_N2
eDP_TX3	PEG HTX C GRX_P12	PEG HTX C GRX_P3
eDP_TX#3	PEG HTX C GRX_N12	PEG HTX C GRX_N3
eDP_AUX	PEG GTX C HRX_P13	PEG GTX C HRX_P2
eDP_AUX#	PEG GTX C HRX_N13	PEG GTX C HRX_N2
eDP_HPD#	PEG GTX C HRX_P12	PEG GTX C HRX_P3

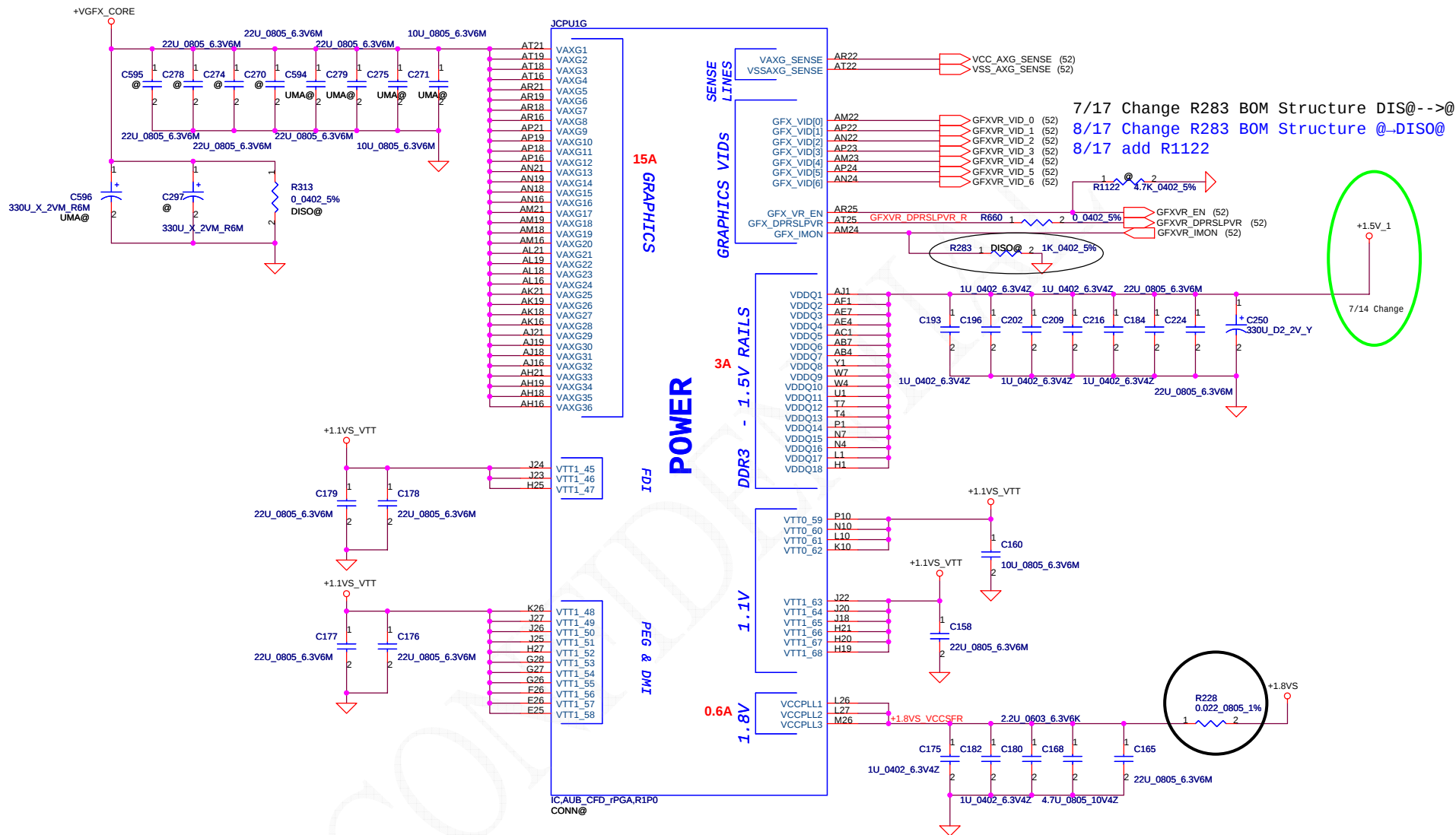


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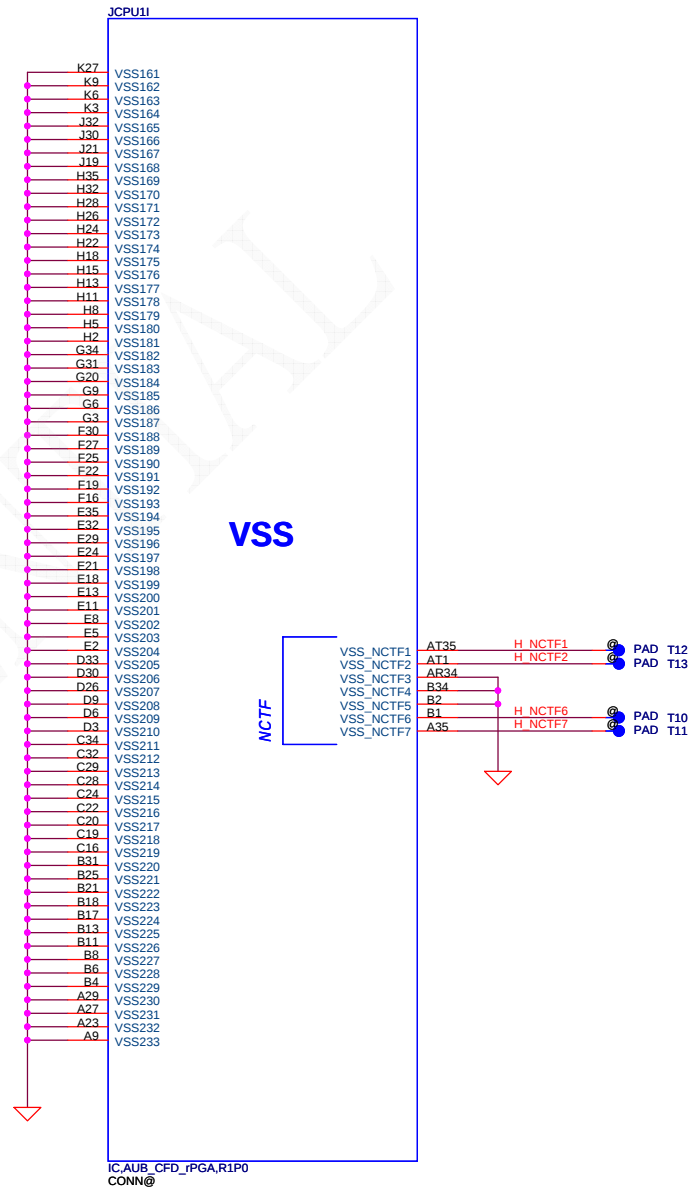
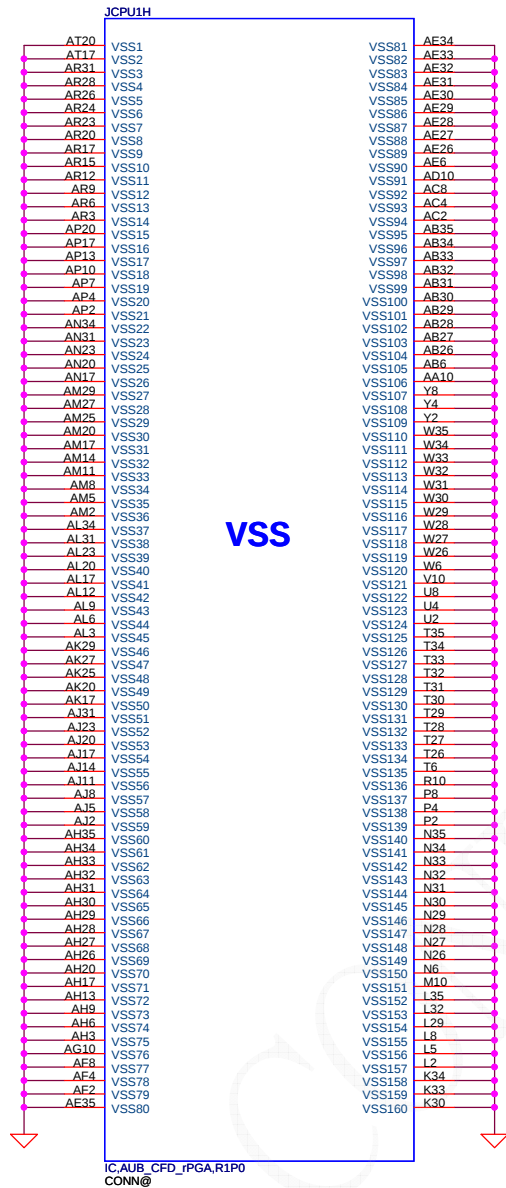
CFG0 - PCI-Express Configuration Select		CFG3 - PCI-Express Static Lane Reversal	
*1:Single PEG 0:Bifurcation enabled		*1:Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	
CFG4 - Display Port Presence		Compal Electronics, Inc.	
*1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port		Title SCHEMATIC MB A5881	
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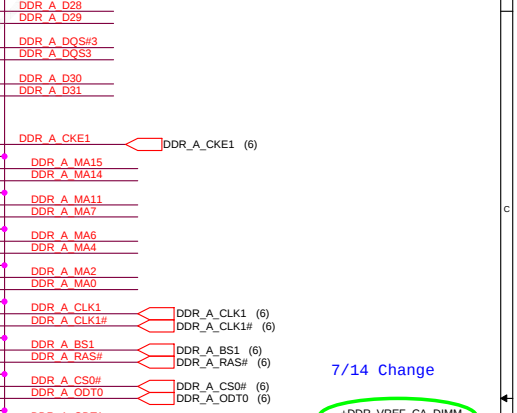
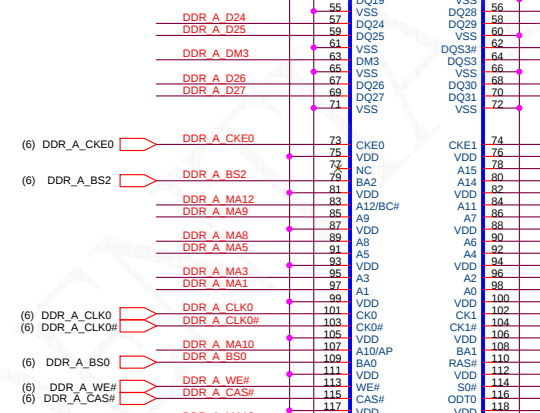
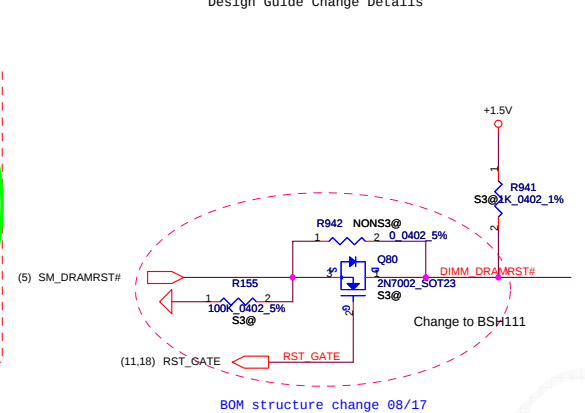
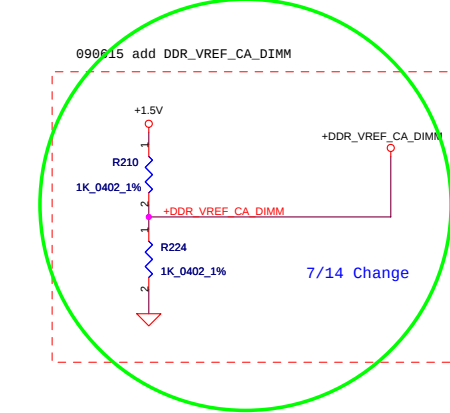
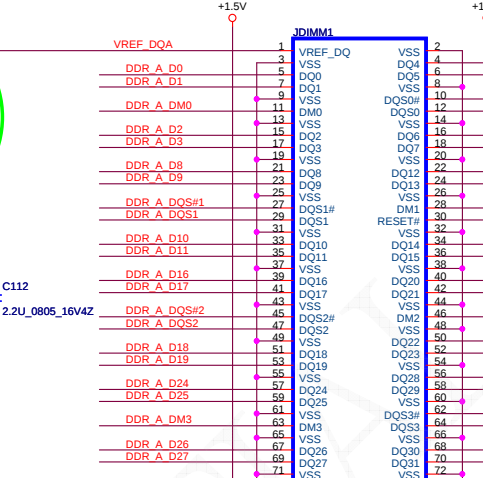
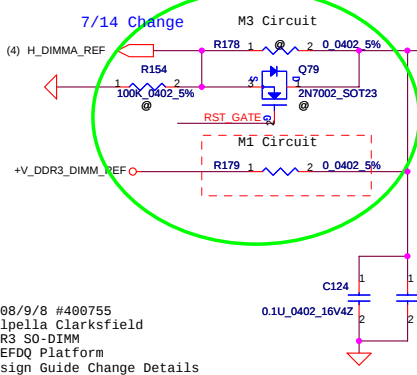
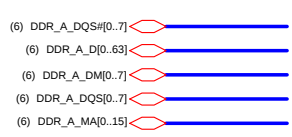
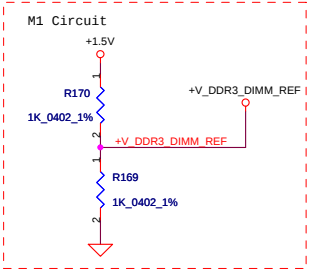
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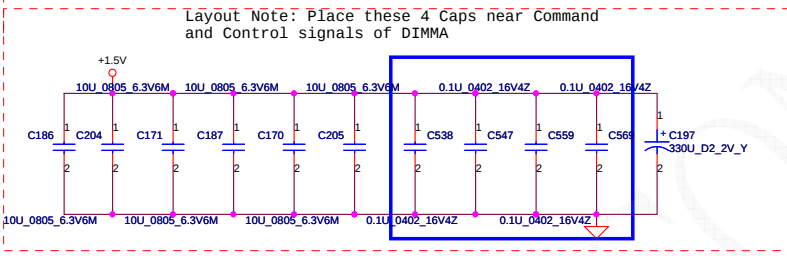
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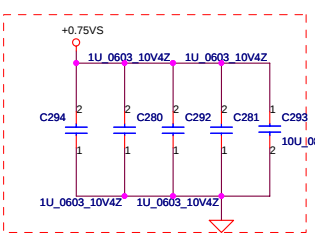
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Layout Note:
Place near JDIMM1

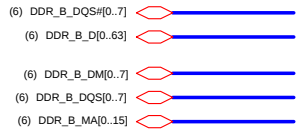


Layout Note:
Place near JDIMM1.203 & JDIMM1.204



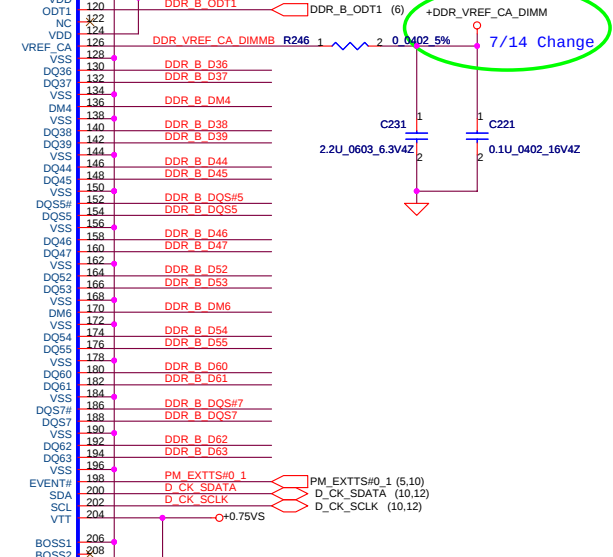
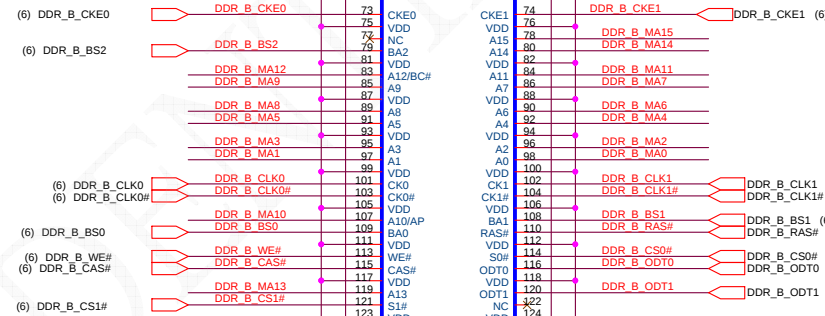
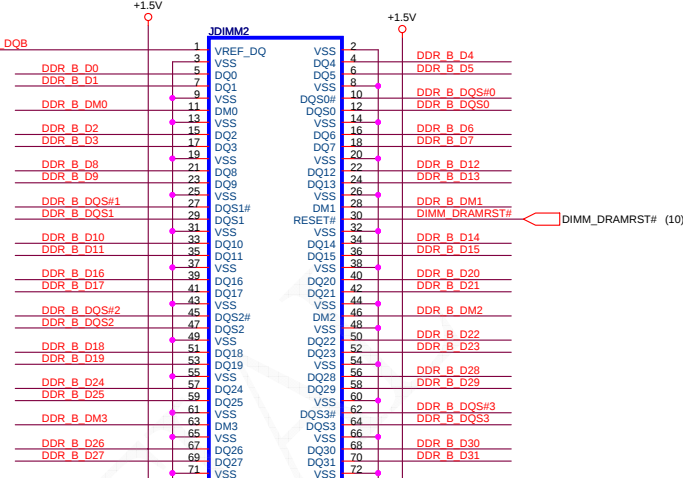
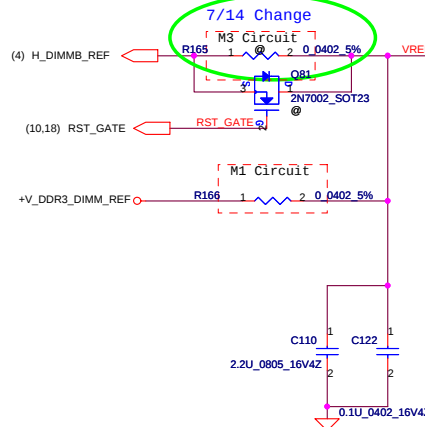
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**DDR3 SO-DIMM A
Standard Type**



2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

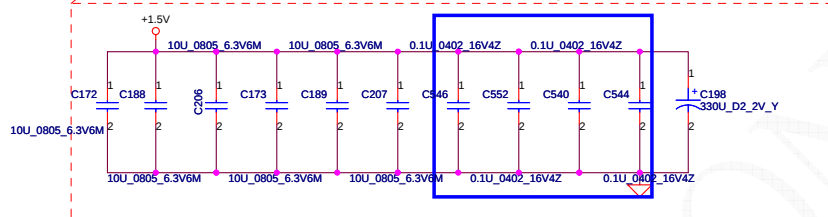
2009/05/19
M2 Circuit unpop
Pop M3 Circuit



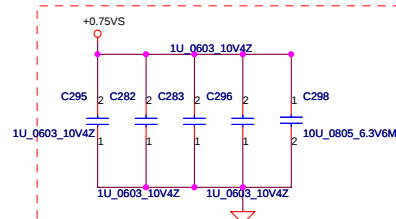
DDR3 SO-DIMM B
Standard Type

Layout Note:
Place near JDIMM2

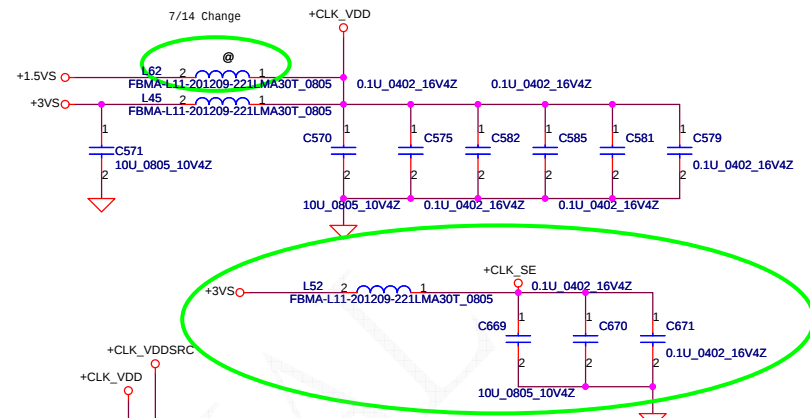
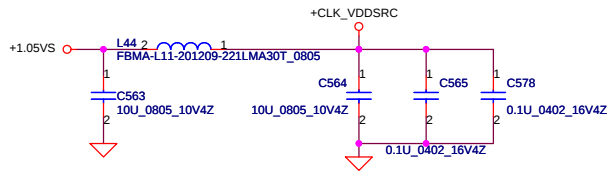
Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA



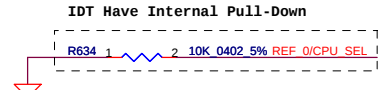
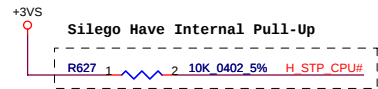
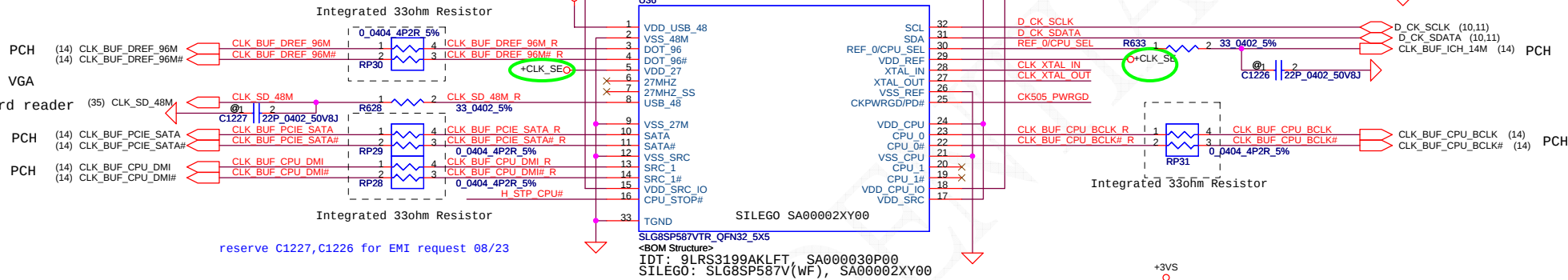
Layout Note:
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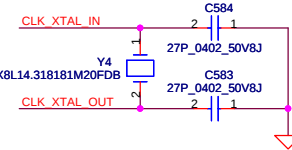
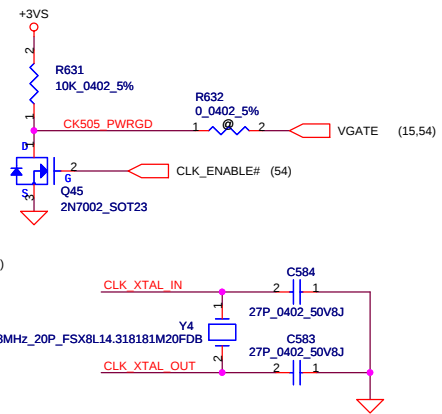
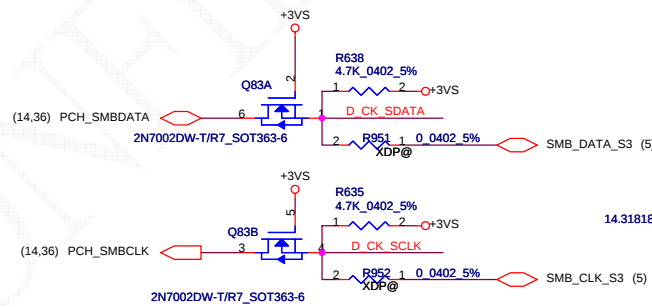
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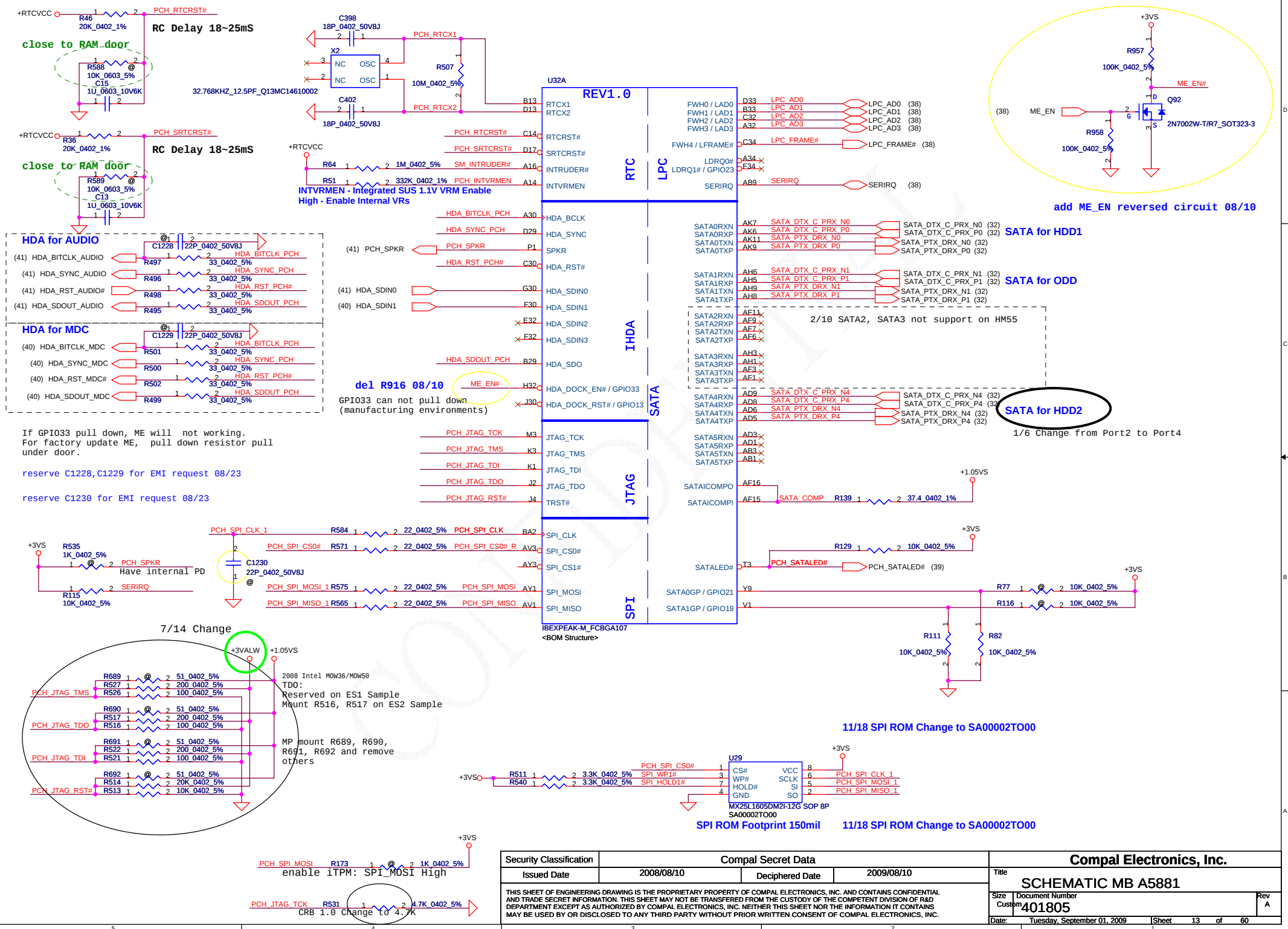


Clock Generator



PIN	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz





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For PCIE LAN

For Wireless LAN

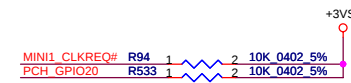
For Mini2

For PCIE LAN

For Wireless LAN

For Mini2

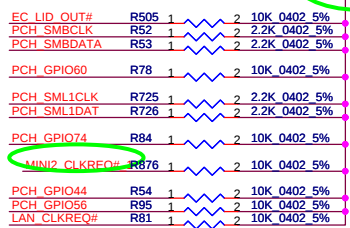
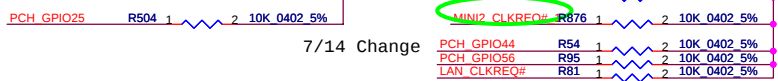
PCIECLKREQ(0,3,4,5,6,7)# Should have a 10K pull up to +3VALW,PCIECLKREQ(1,2),Should have a 10K pull up to +3VS



7/17: Change to +3VALW



7/14 Change



U32B

REV1.0

PCI-E*

Controller

Link

PEG

From CLK BUFFER

Clock Flex

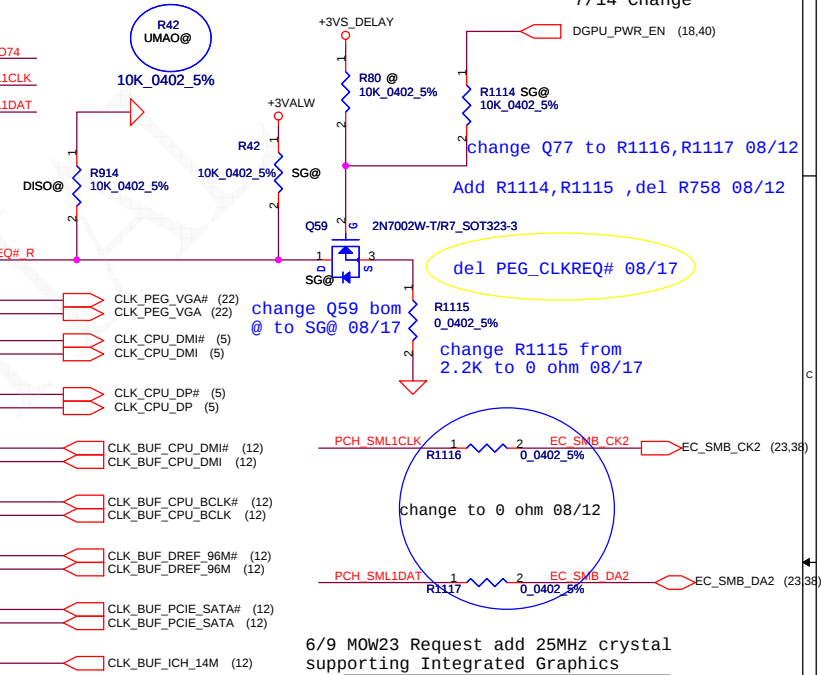
Project ID		
ID1	ID0	Project
0	0	JV
0	1	Future

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				Custom	401805
				Date	Tuesday, September 01, 2009
				Sheet	14 of 60

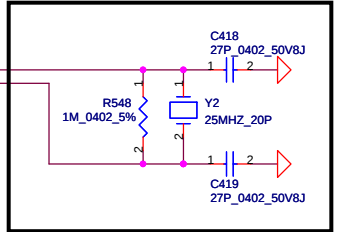
1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

7/14 Change

20090512 add double mosfet prevent ATI M92 electric leakage



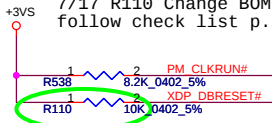
6/9 M0W23 Request add 25MHz crystal supporting Integrated Graphics



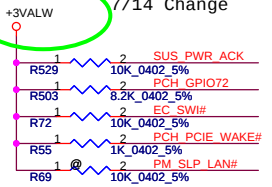
(4) DMI_HTX_PRX_N[0..3] DMI_HTX_PRX_N[0..3]
(4) DMI_HTX_PRX_P[0..3] DMI_HTX_PRX_P[0..3]
(4) DMI_PTX_HRX_N[0..3] DMI_PTX_HRX_N[0..3]
(4) DMI_PTX_HRX_P[0..3] DMI_PTX_HRX_P[0..3]

(4) H_FDI_TXN[0..7] H_FDI_TXN[0..7]
(4) H_FDI_TXP[0..7] H_FDI_TXP[0..7]

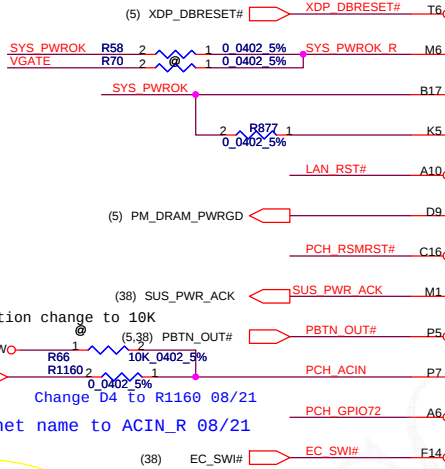
7/17 R110 Change BOM Structure for follow check list p.23



7/14 Change



7/17 R72 KAV60 DEL

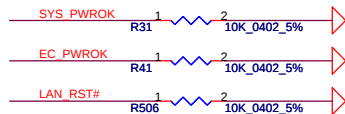
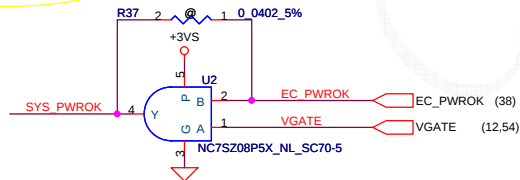


10/2 Intel suggestion change to 10K

7/14 Change

(23.38) ACIN_R (23.38) ACIN_R
Change D4 to R1160 08/21
change EC_ACIN net name to ACIN_R 08/21

del R917 08/21



No used Integrated LAN,
connecting LAN_RST# to GND

U32C
REV1.0
DMI HTX PRX N0 BC24
DMI HTX PRX N1 B122
DMI HTX PRX N2 AW20
DMI HTX PRX N3 B120
DMI HTX PRX P0 BD24
DMI HTX PRX P1 BC22
DMI HTX PRX P2 BA20
DMI HTX PRX P3 BG20
DMI PTX HRX N0 BE22
DMI PTX HRX N1 BF21
DMI PTX HRX N2 BD20
DMI PTX HRX N3 BE18
DMI PTX HRX P0 BD22
DMI PTX HRX P1 BH21
DMI PTX HRX P2 BC20
DMI PTX HRX P3 BD18

DMIORXN
DMI1RXN
DMI2RXN
DMI3RXN
DMIORXP
DMI1RXP
DMI2RXP
DMI3RXP
DMIOTXN
DMI1TXN
DMI2TXN
DMI3TXN
DMIOTXP
DMI1TXP
DMI2TXP
DMI3TXP

System Power Management

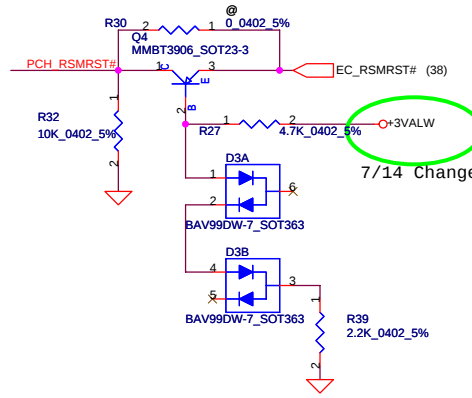
FDI_RXN0
FDI_RXN1
FDI_RXN2
FDI_RXN3
FDI_RXN4
FDI_RXN5
FDI_RXN6
FDI_RXN7
FDI_RXP0
FDI_RXP1
FDI_RXP2
FDI_RXP3
FDI_RXP4
FDI_RXP5
FDI_RXP6
FDI_RXP7

FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1

BA18
BH17
BD16
BJ16
BA16
BE14
BA14
BC12
BB18
BE17
BC16
BG16
AW16
BD14
BB14
BD12

H_FDI_TXN0
H_FDI_TXN1
H_FDI_TXN2
H_FDI_TXN3
H_FDI_TXN4
H_FDI_TXN5
H_FDI_TXN6
H_FDI_TXN7
H_FDI_TXP0
H_FDI_TXP1
H_FDI_TXP2
H_FDI_TXP3
H_FDI_TXP4
H_FDI_TXP5
H_FDI_TXP6
H_FDI_TXP7

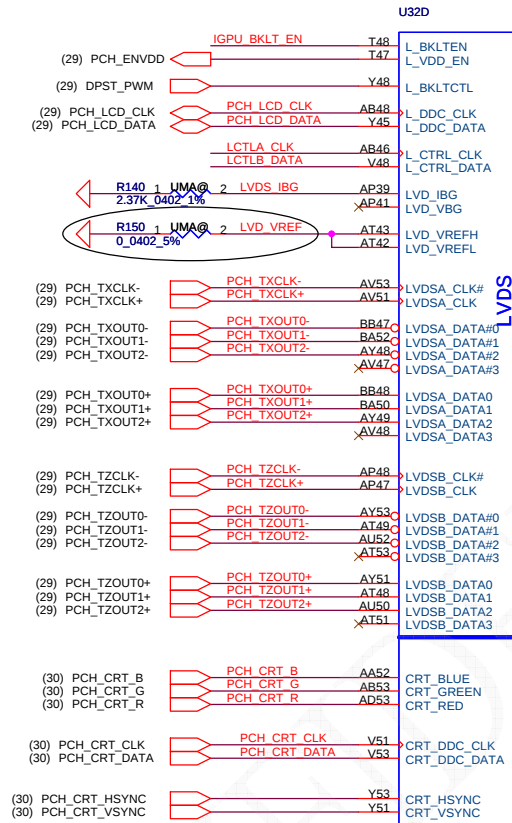
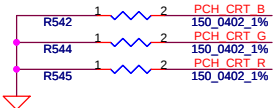
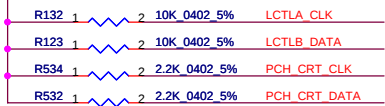
WAKE#
CLKRUN# / GPIO32
SUS_STAT# / GPIO61
SUSCLK / GPIO62
SLP_S5# / GPIO63
SLP_S4#
SLP_S3#
SLP_M#
TP23
PMSYNCH
SLP_LAN# / GPIO29
PCH_PCIE_WAKE#
PM_CLKRUN#
PCH_GPIO61
PCH_GPIO62
PM_SLP_S5#
PM_SLP_S4#
PM_SLP_S3#
PM_SLP_M#
PM_SLP_DS#
H_PM_SYNC
H_FDI_INT (4)
H_FDI_FSYNC0 (4)
H_FDI_FSYNC1 (4)
H_FDI_LSYNC0 (4)
H_FDI_LSYNC1 (4)



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				Date	Tuesday, September 01, 2009
				Sheet	15 of 60

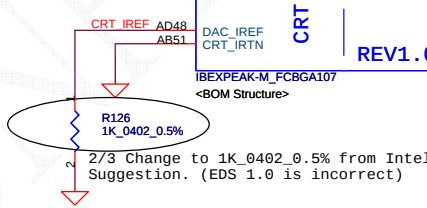
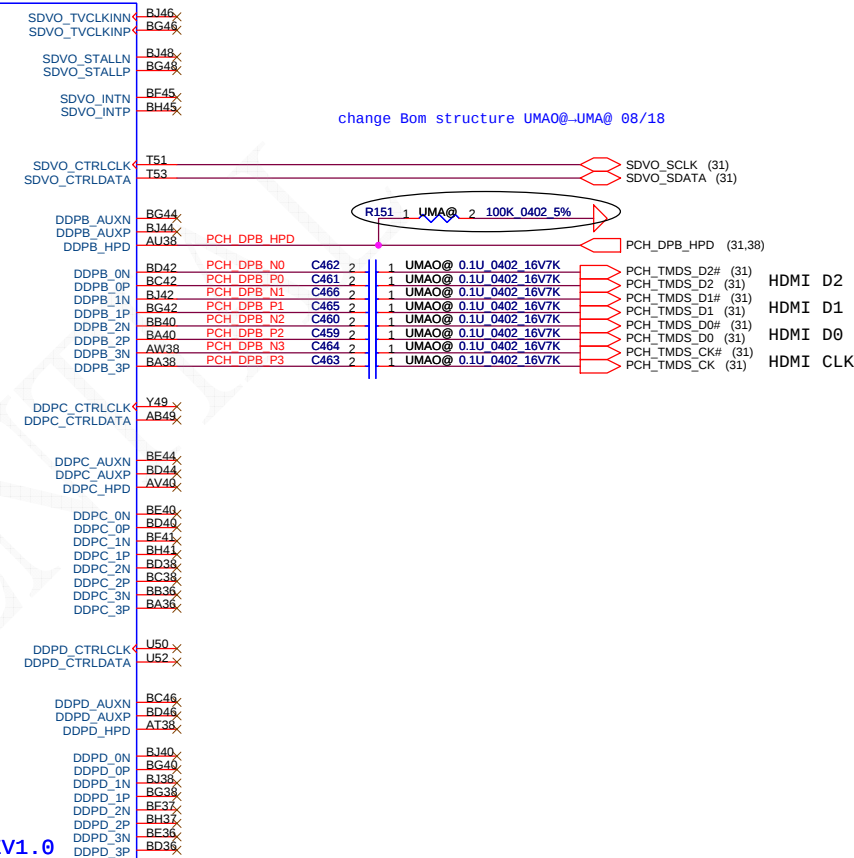
7/14 Change

+3VS
11/21 intel JIM suggest Pull high at LVDS Conn

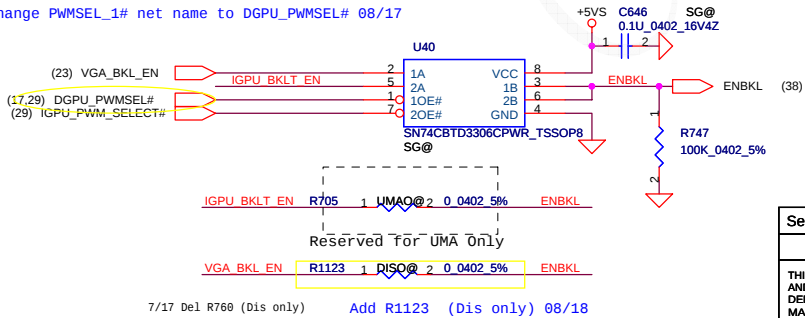


Digital Display Interface

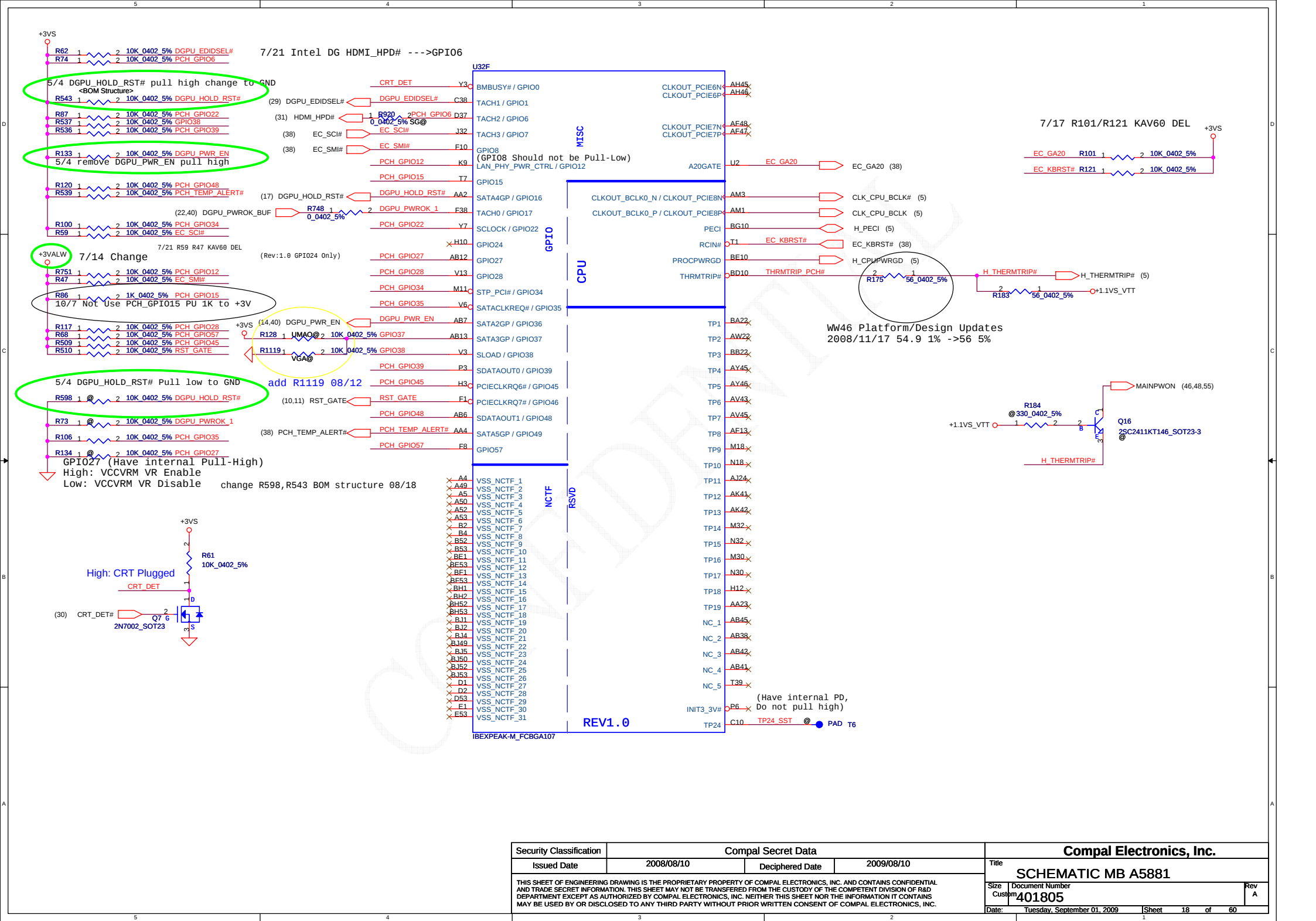
REV1.0



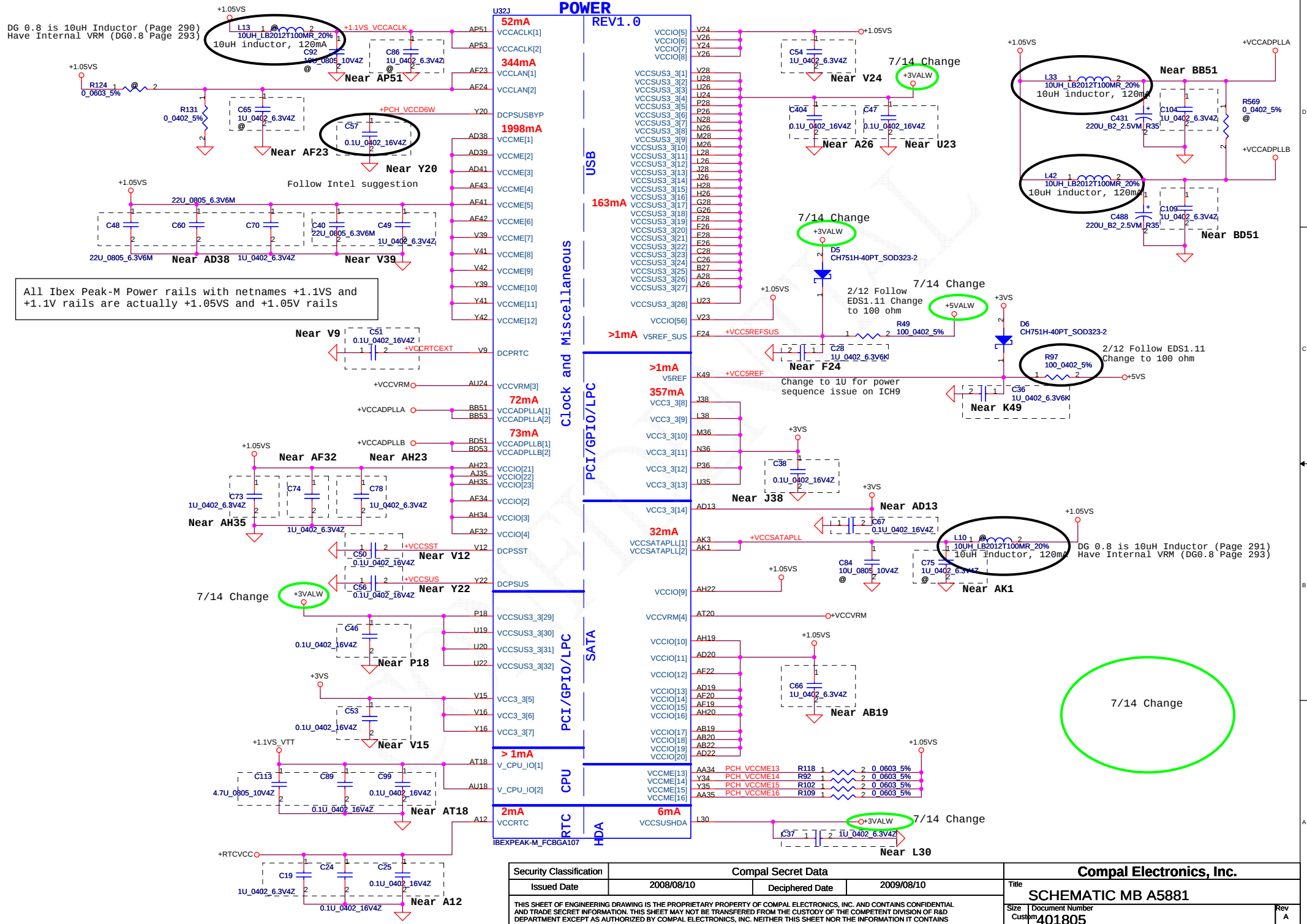
change PWMSEL_1# net name to DGPU_PWMSEL# 08/17



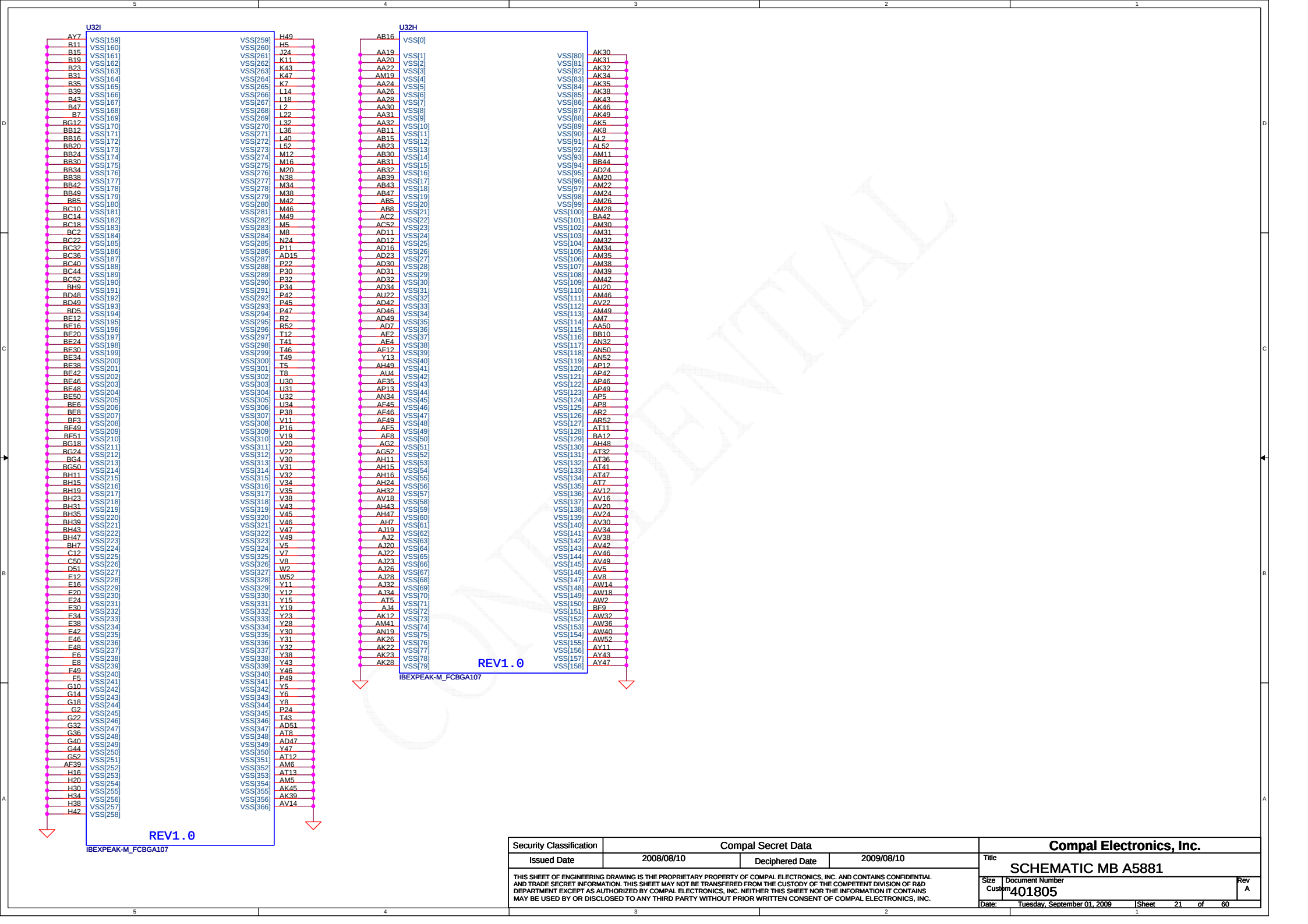
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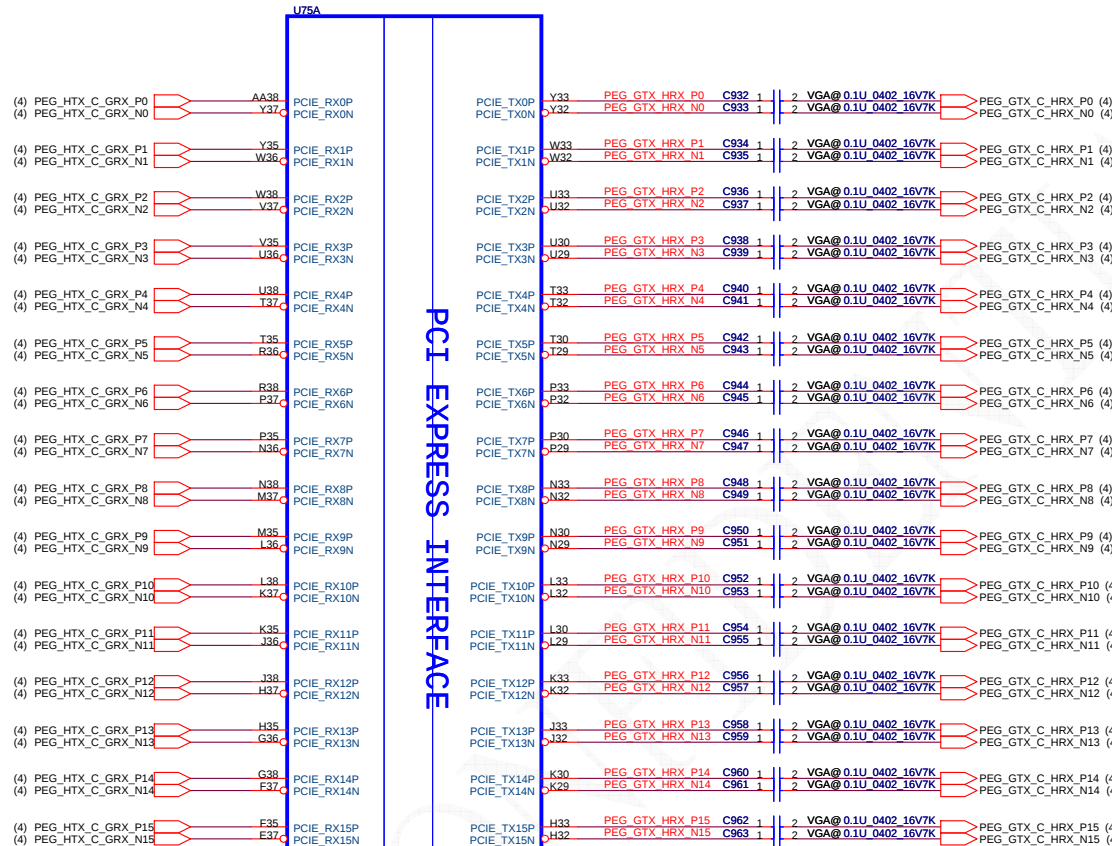
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				Custom	401805	A
				Date:	Tuesday, September 01, 2009	Sheet 20 of 60



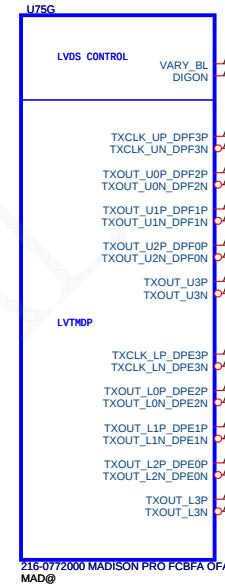
PARK@ U75

216-0774007 All PARK PRO M2 0FA

add for DPST support.



PCI EXPRESS INTERFACE



216-0772000 MADISON PRO FCBFA 0FA
MAD@

(14) CLK_PEG_VGA#
(14) CLK_PEG_VGA#

R962
0.0402 5%
8/19 change net name

R964
10K 0402 1%
VGA@

(17) PLTRST_VGA#

AA30 PERSTB

AB35 PCIE_REFCLKP
AA38 PCIE_REFCLKN

NC#1
NC#2
NC_PWRGOOD

216-0772000 MADISON PRO FCBFA 0FA
MAD@

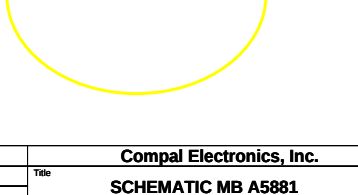
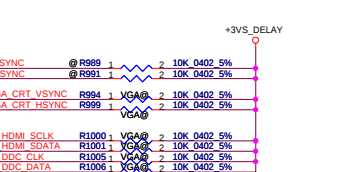
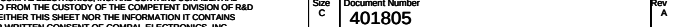
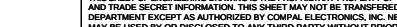
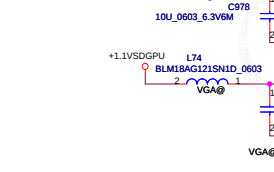
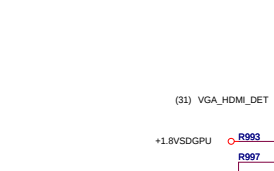
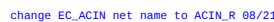
M96 P/N : SA00002UQ50 (S IC 216-0729042-00 A13 M96 FCBGA962 0FA)
M92 P/N : SA00002YX10 (S IC 216-0728014 A12 M92-M2 XT FCBGA 0FA)

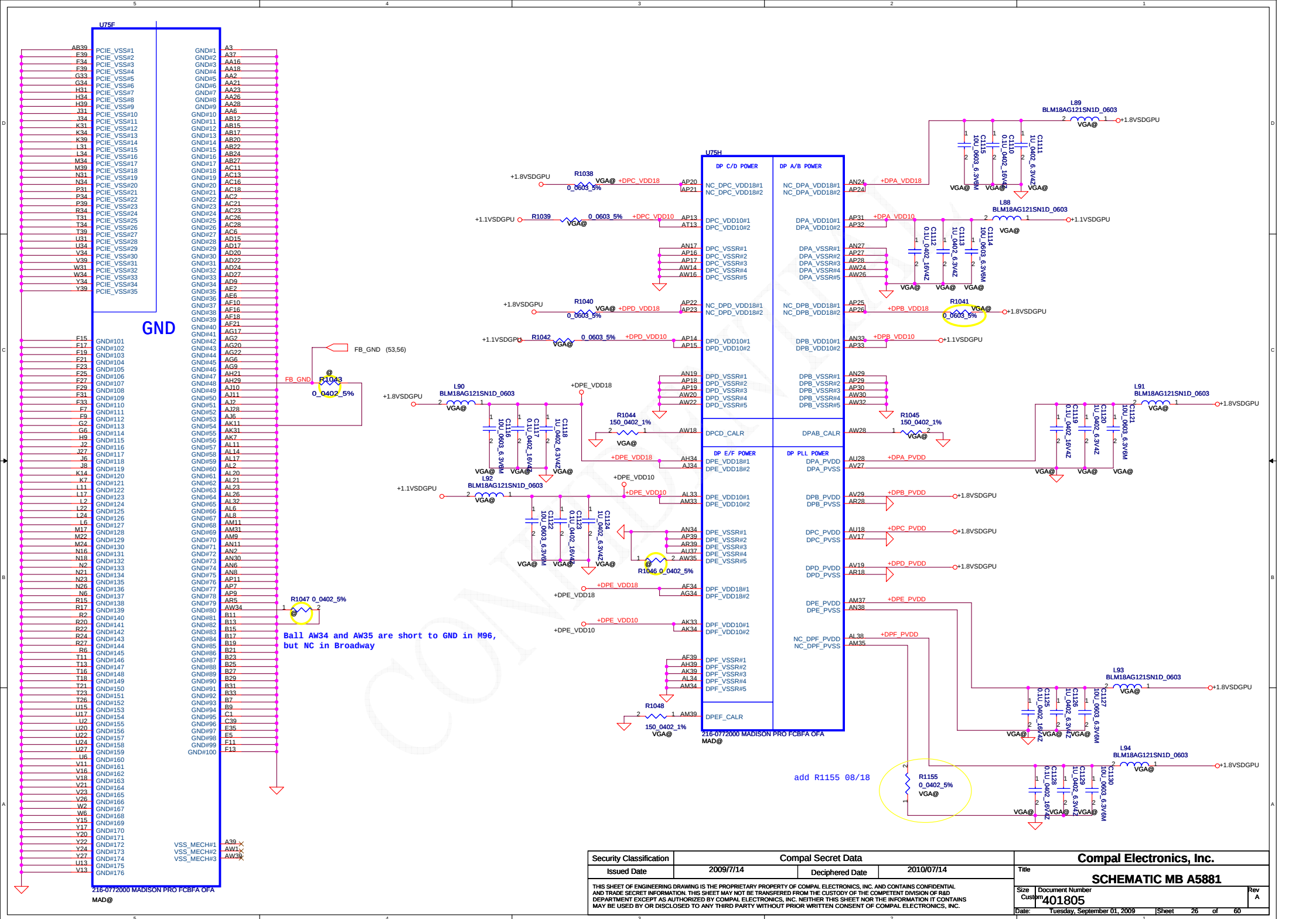
MADISON P/N:SA00003M300 (S IC 216-0772000 MADISON PRO FCBGA 0FA)
PARK P/N:SA00003MC00 (S IC 216-0774007 All PARK PRO M2 0FA)

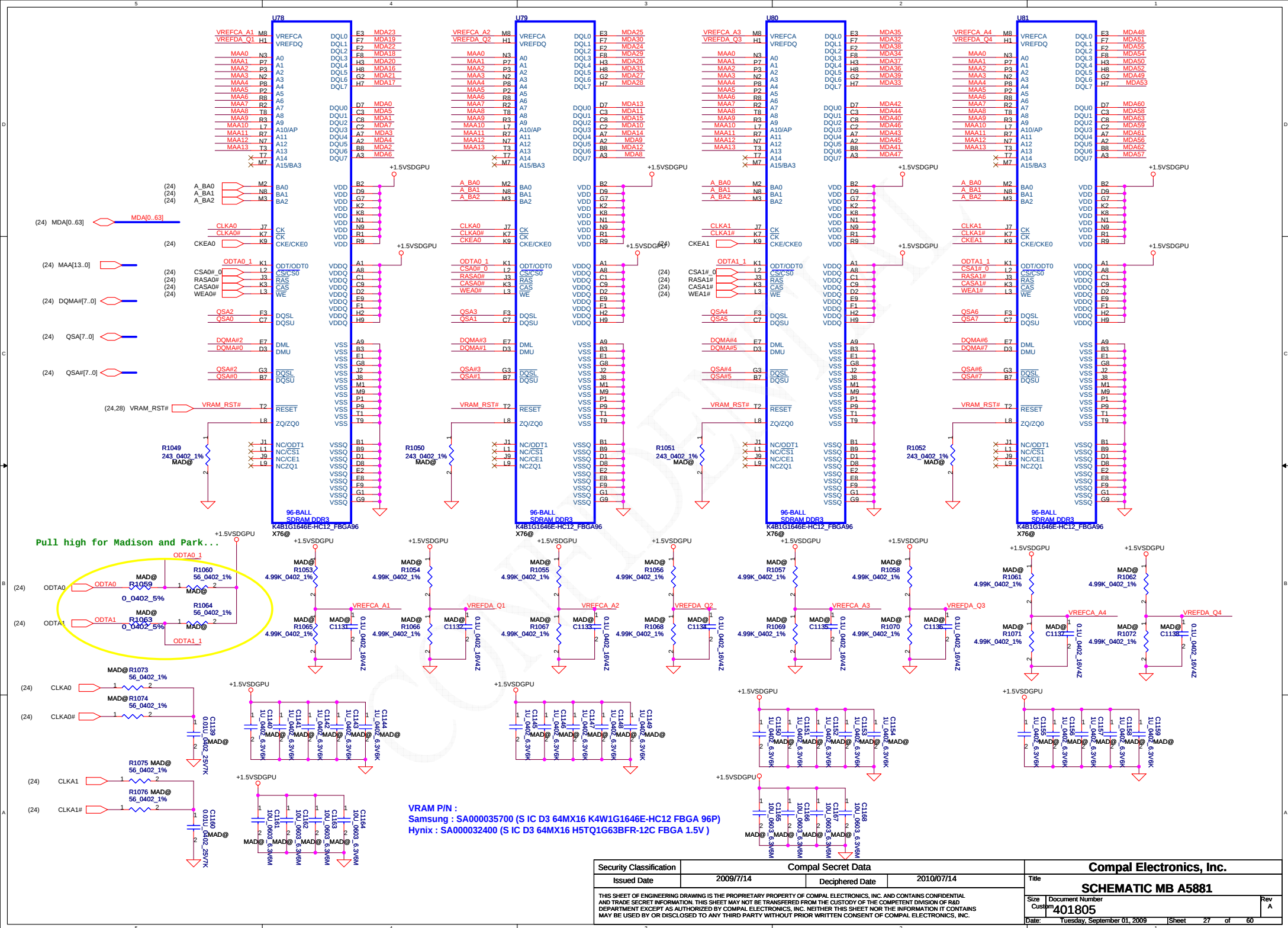
Mannhattan Only
NC in M96

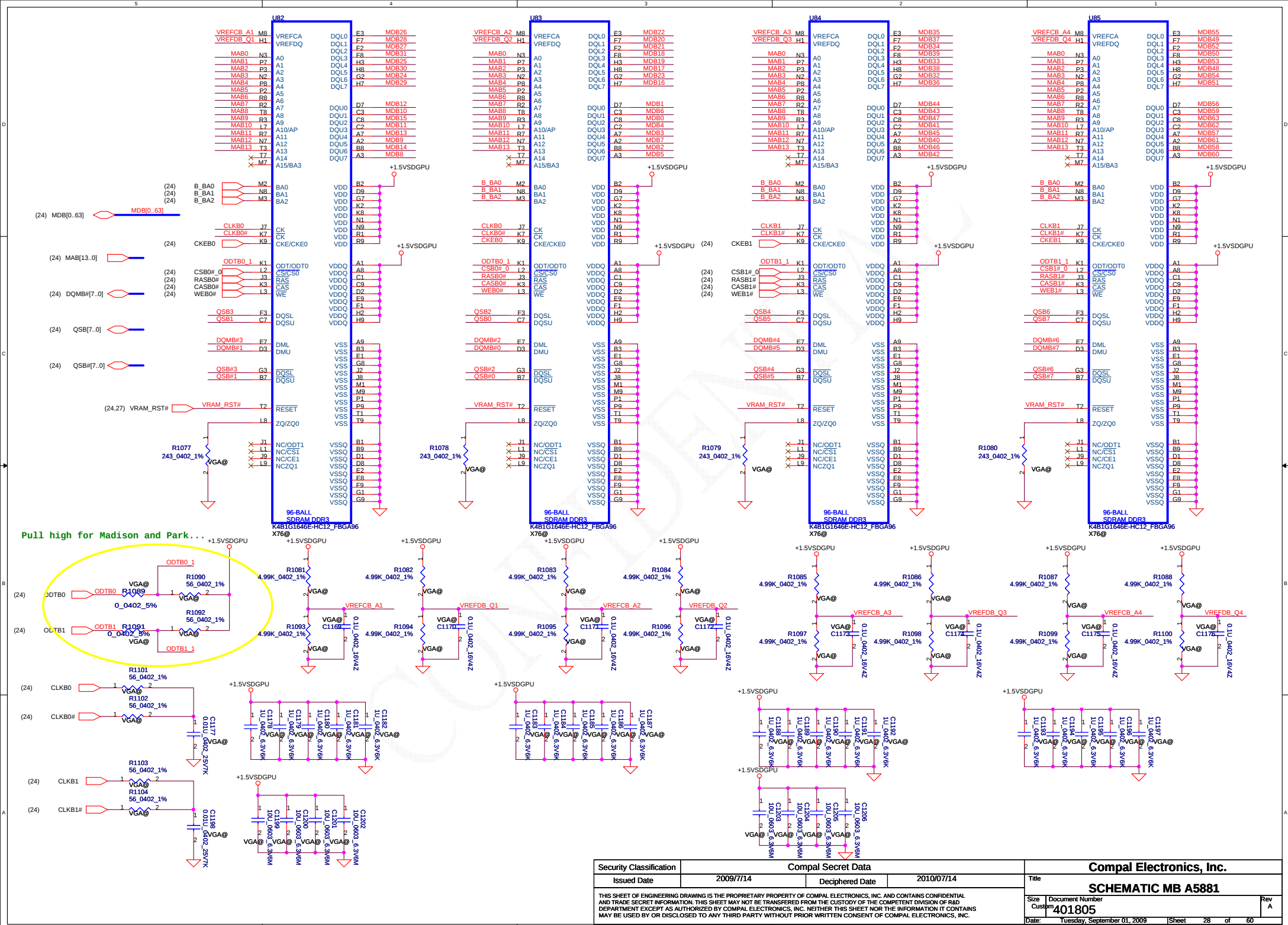
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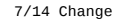
Location VRAM	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung	0	0	0	0
HYNIX	1	0	0	0











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CRT Connector

Change L31,L28,L26,C415,C411,C405,C412,C409,C401
BOM structure UMA@_POP 08/18

Change to 0 ohm for Discrete

Change to 15pf for Discrete

Change to 12pf for Discrete

PCH DDC PU 2.2K
on Page 17

add R1133,R1134,R1135,R1136 08/18

7/17 Del R895 R897 DIS only@
add R1131,R1132 DIS only 08/18
del R1131,R1132 08/19

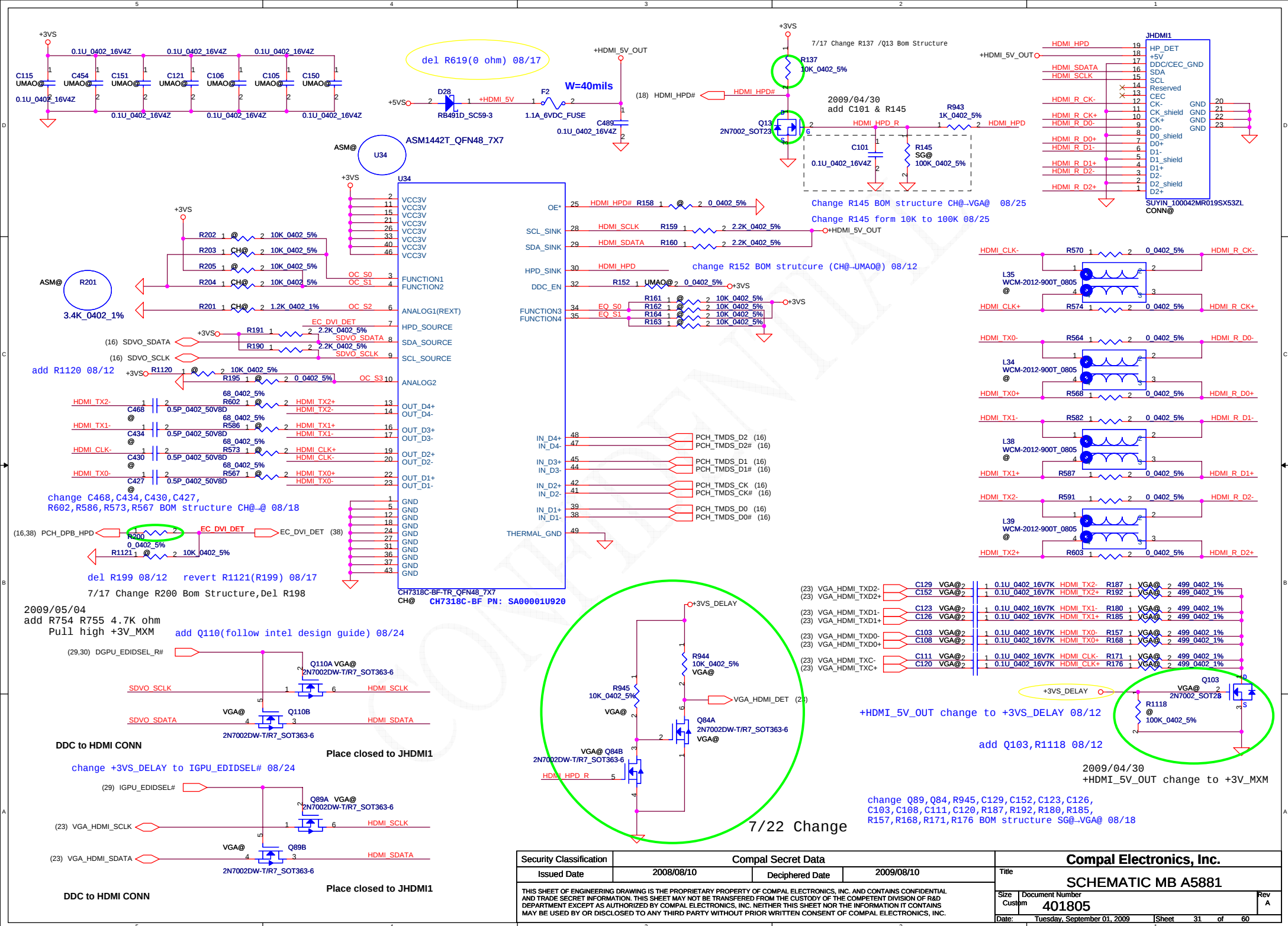
Check bom

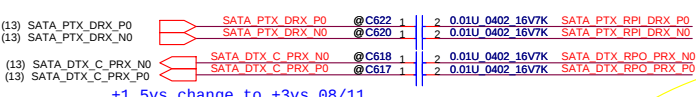
SEL1->Port 0-4
(L--B1 Output H--B2 Output)

Reserved for UMA only

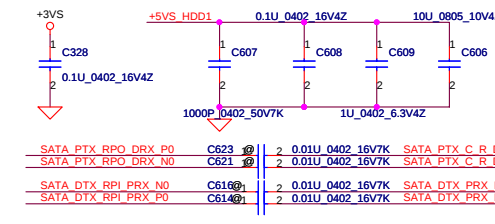
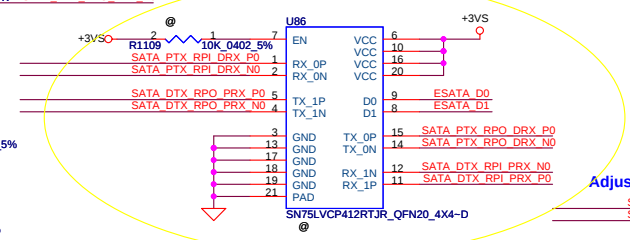
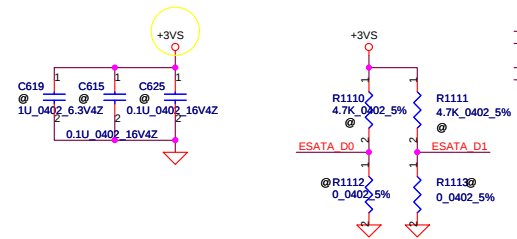
PCH CRT_R R699 2 UMA@ 0.0402 5% CRT_R
PCH CRT_G R700 2 UMA@ 0.0402 5% CRT_G
PCH CRT_B R701 2 UMA@ 0.0402 5% CRT_B
PCH CRT_HSYNC R702 2 UMA@ 0.0402 5% CRT_HSYNC
PCH CRT_VSYNC R703 2 UMA@ 0.0402 5% CRT_VSYNC

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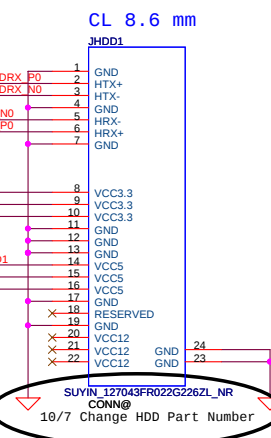




PI2EQX323BLZHE change to SN75LVCP412R



SATA HDD1 Conn.



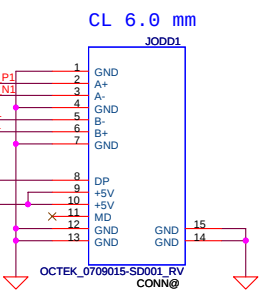
x_EQ	Compliance Channel @ 1.5 GHz
0	1.5dB ± 1.0dB
1	5.5dB ± 1.0dB

x_EM	Compliance Channel @ 1.5 GHz
0	0dB
1	-3.5dB

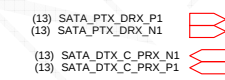
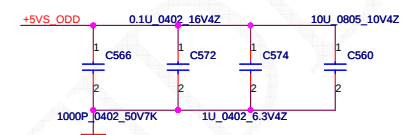
Adjust HDD1 PCH TX Swing

Add R953,R954,R955,R956 08/10

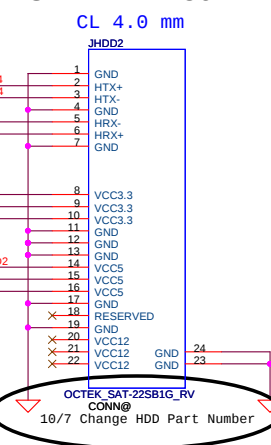
SATA ODD Conn.

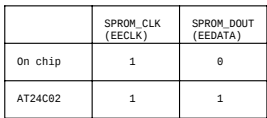


Placea caps. near ODD CONN.

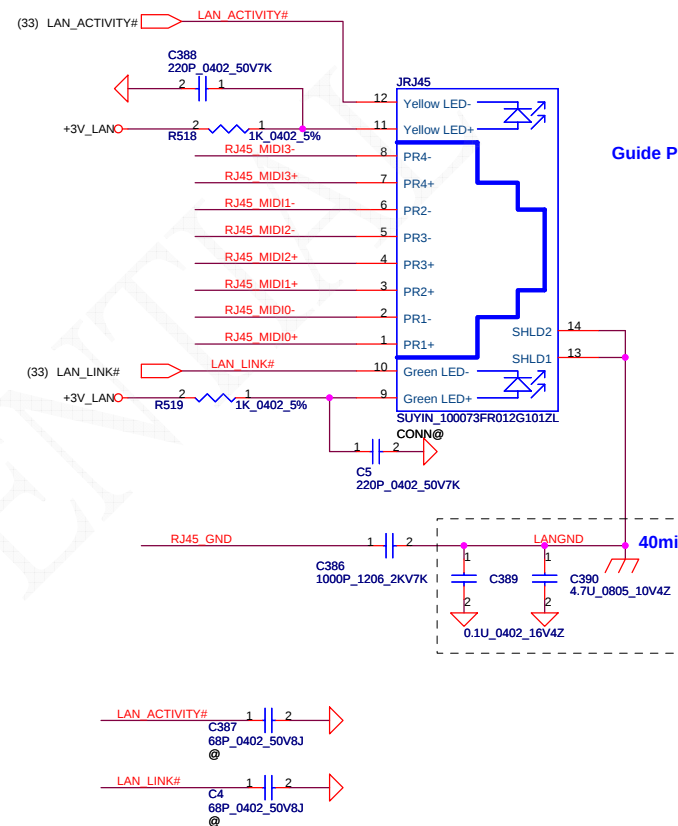
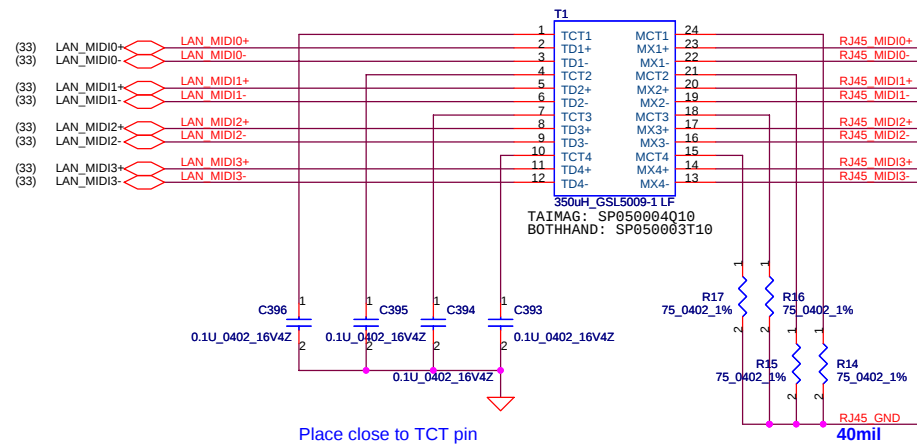


SATA HDD2 Conn.



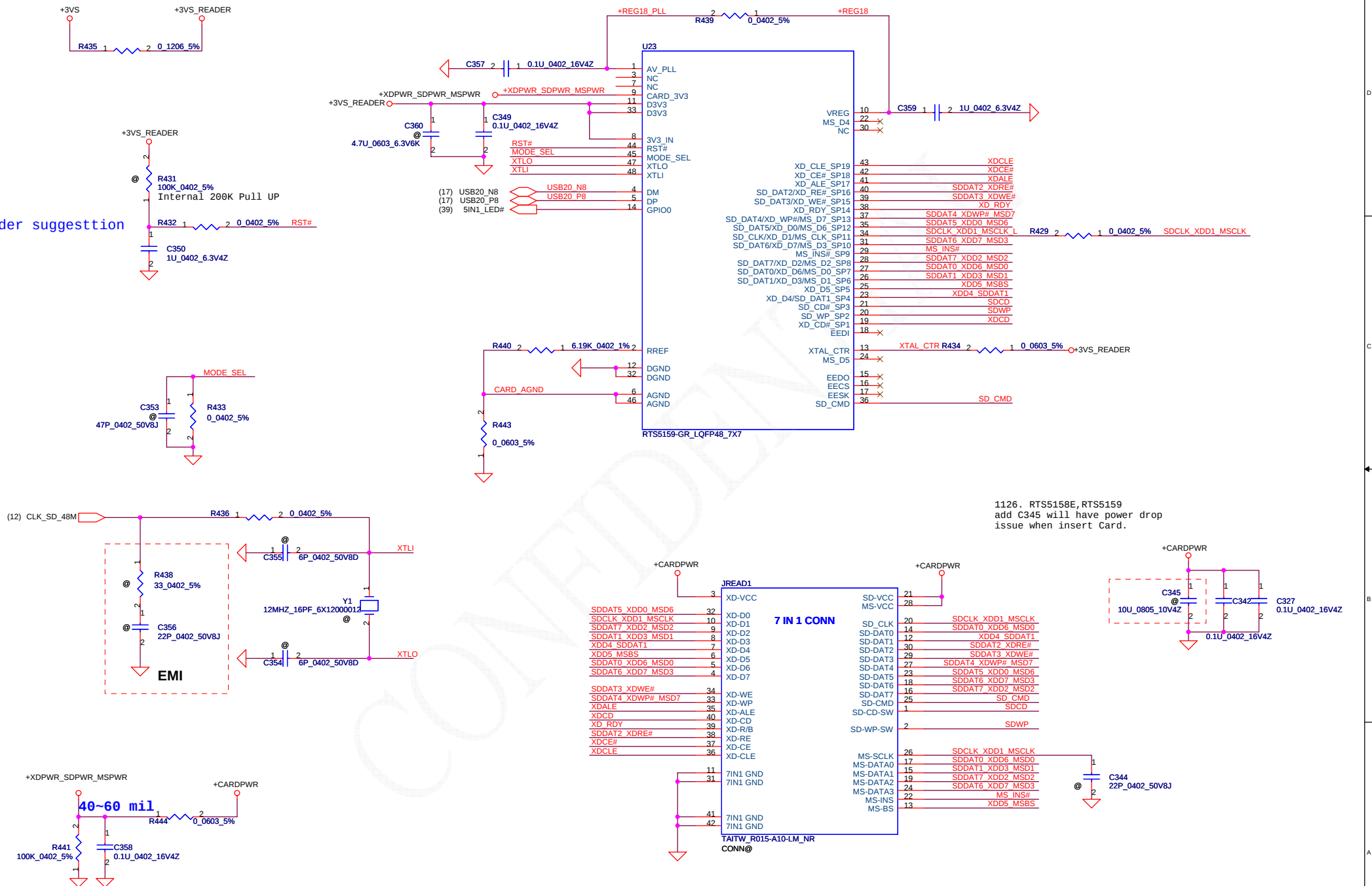


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				Custom	401805	A
				Date:	Tuesday, September 01, 2009	Sheet 33 of 60

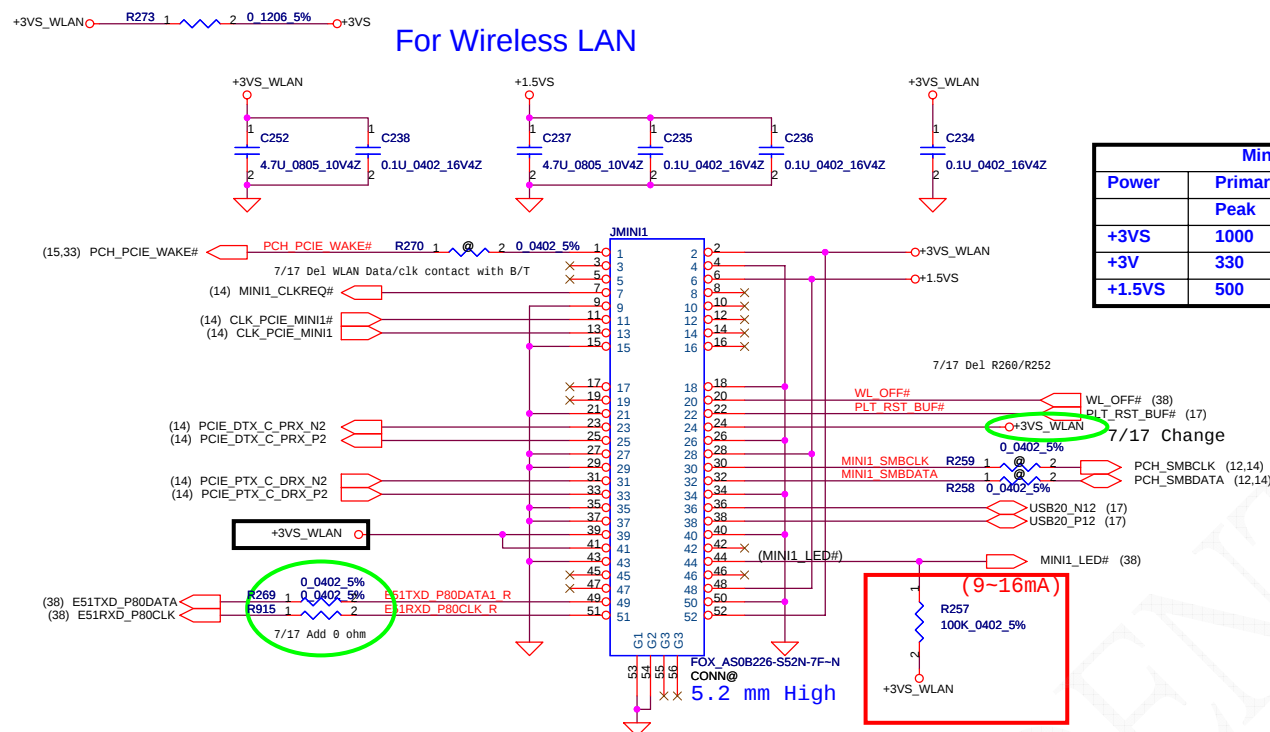


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Size B	Document Number	401805		Date	Rev A
Tuesday, September 01, 2009		Sheet 34 of 60			

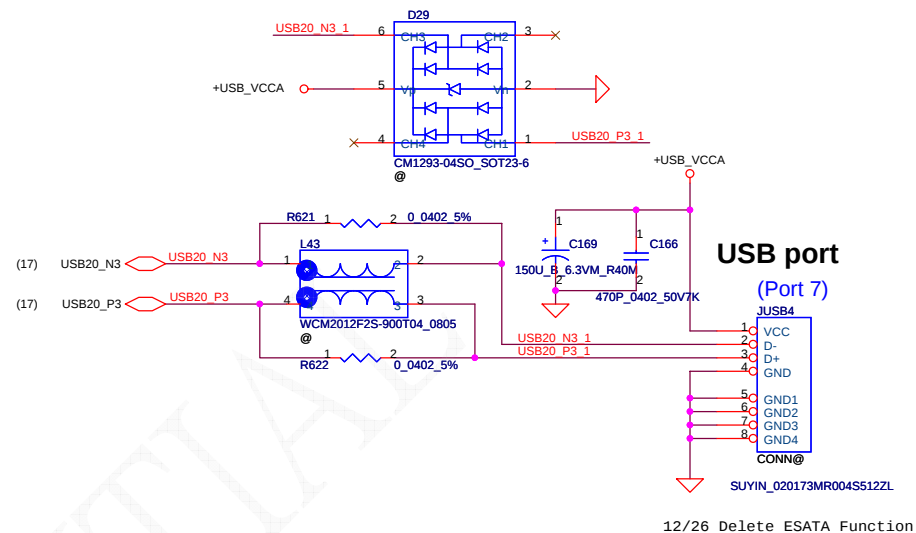
Vender suggestion



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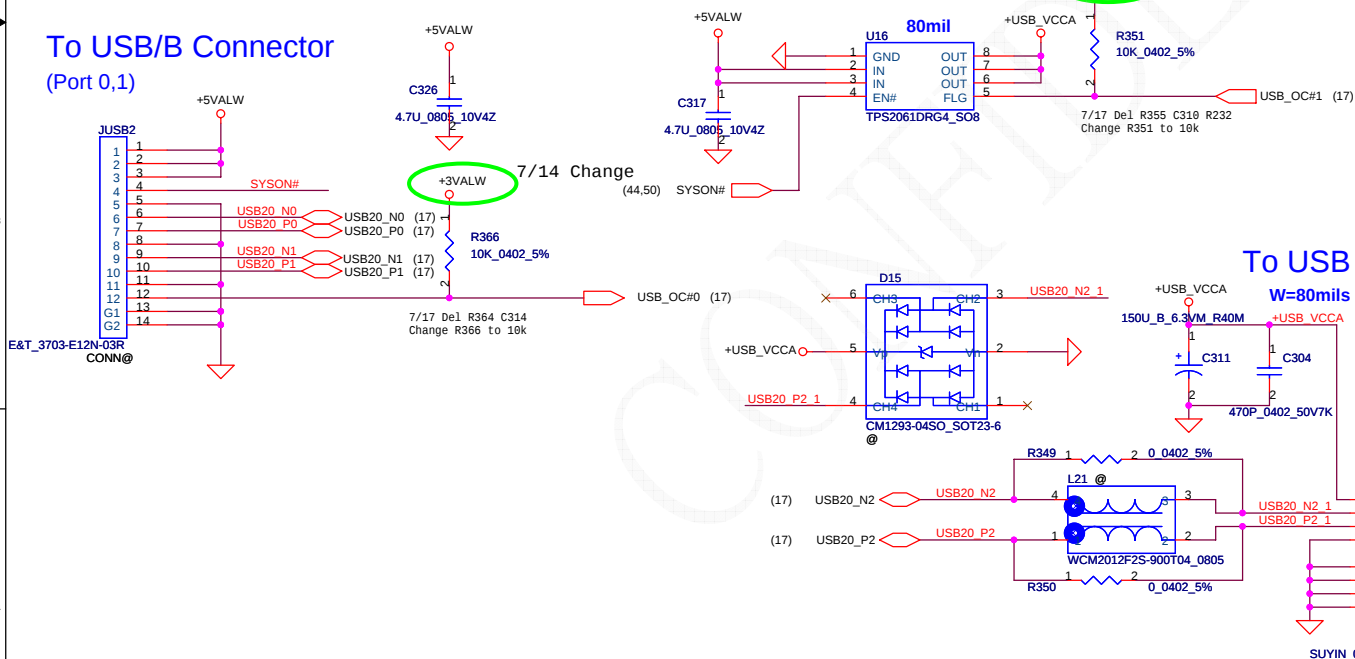


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

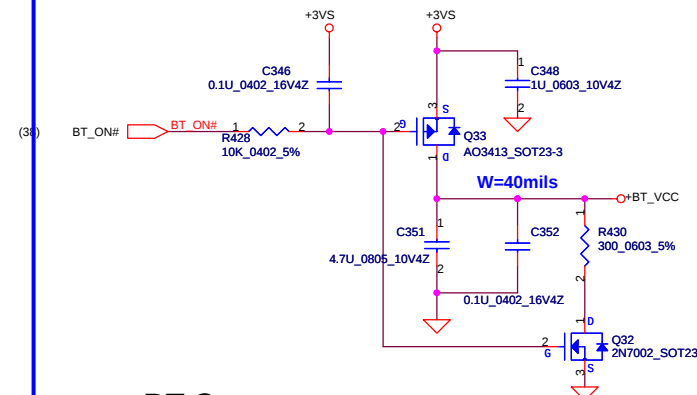


7/14 Change

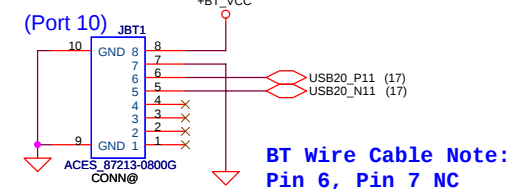
To USB/B Connector
(Port 0,1)



Bluetooth Conn.



BT Conn.



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7/14 DEL PCH_SPKR (PCH to EC)

For EC Tools

Place on RAM door

Place on MiniCard

add R1158, R1159 08/21

將 INVT_PWM 跟 EC_ACIN 交換 08/11

change ME_EN for U18.75 to U18.19 08/20

change MEDIA_LED#_OUT to MEDIA_LED_OUT 08/10

del D17 08/21

Analog Board ID definition, Please see page 3.

7/14 Pin 19/99 DEL

del R385 R378(0 ohm) 08/10

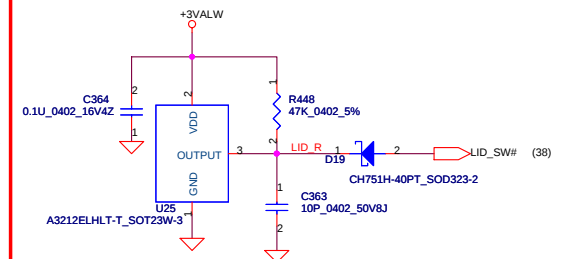
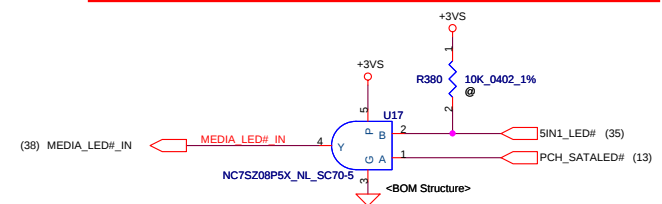
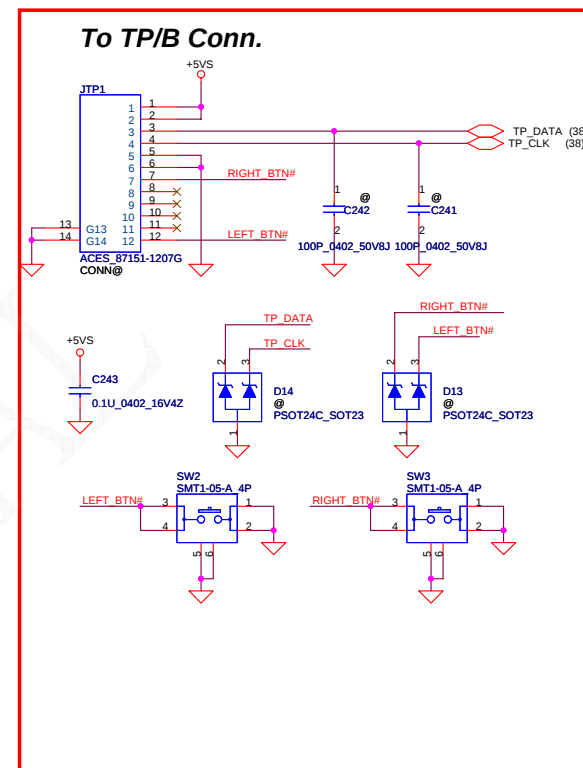
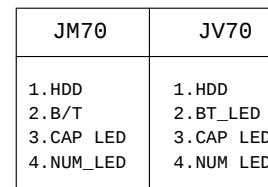
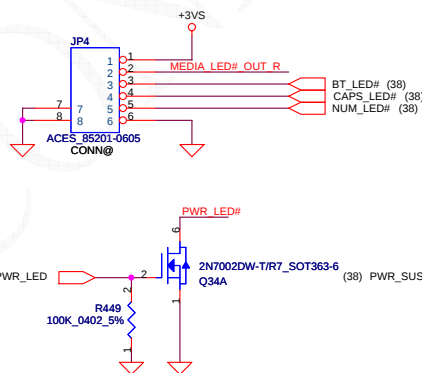
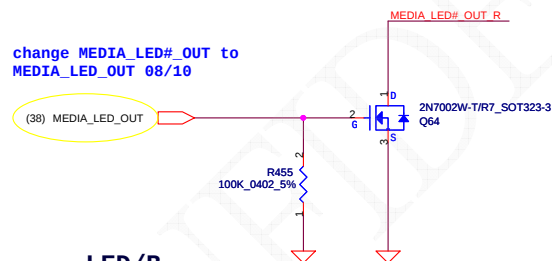
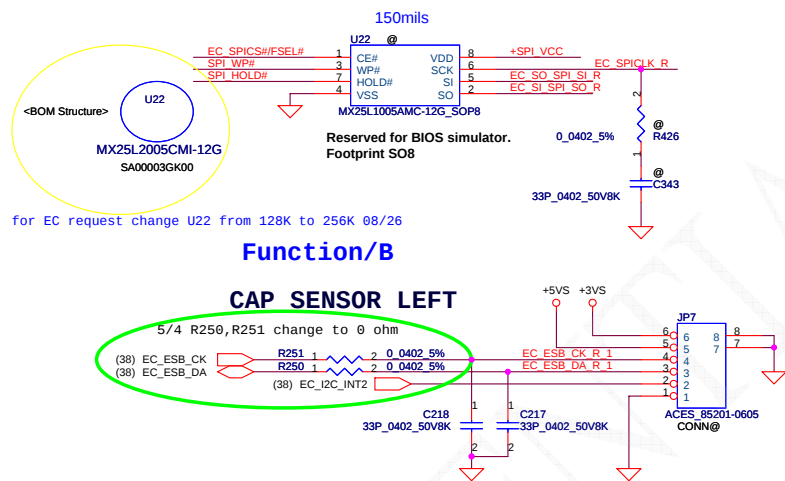
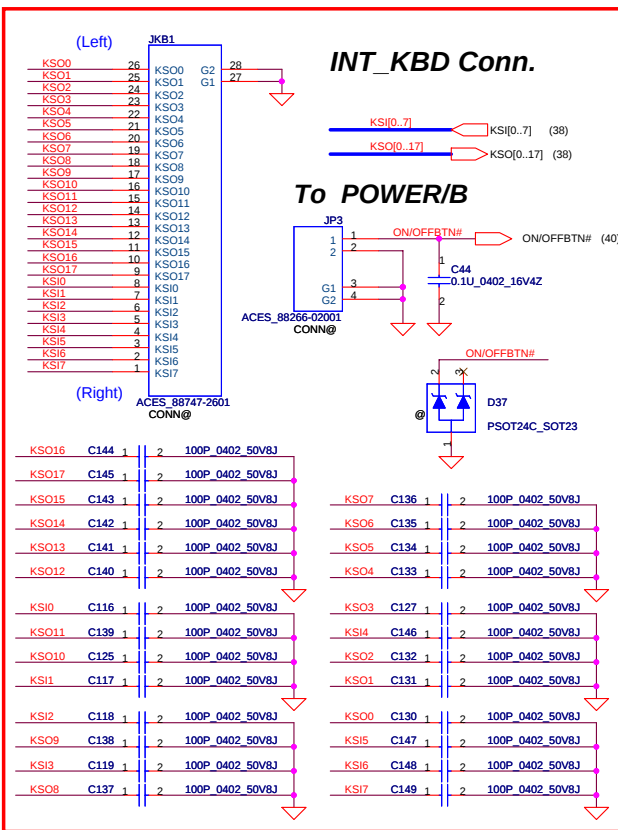
change R376.R391 BOM structure 08/12

del C1(15P) 08/10

change net name 08/17

del R404, R412 08/12

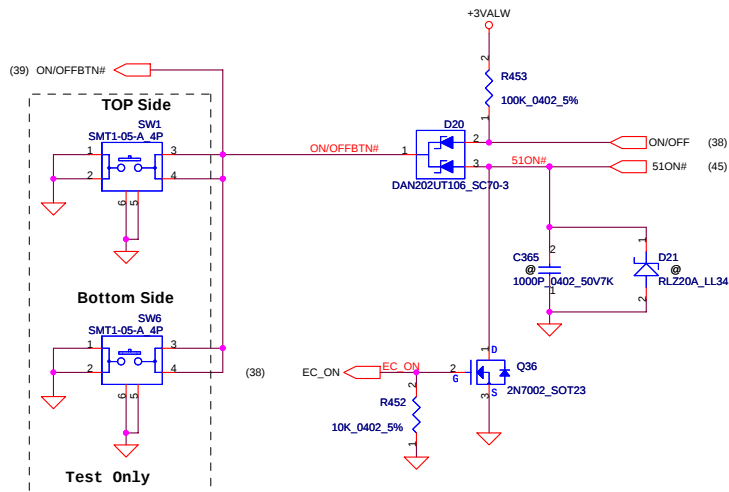
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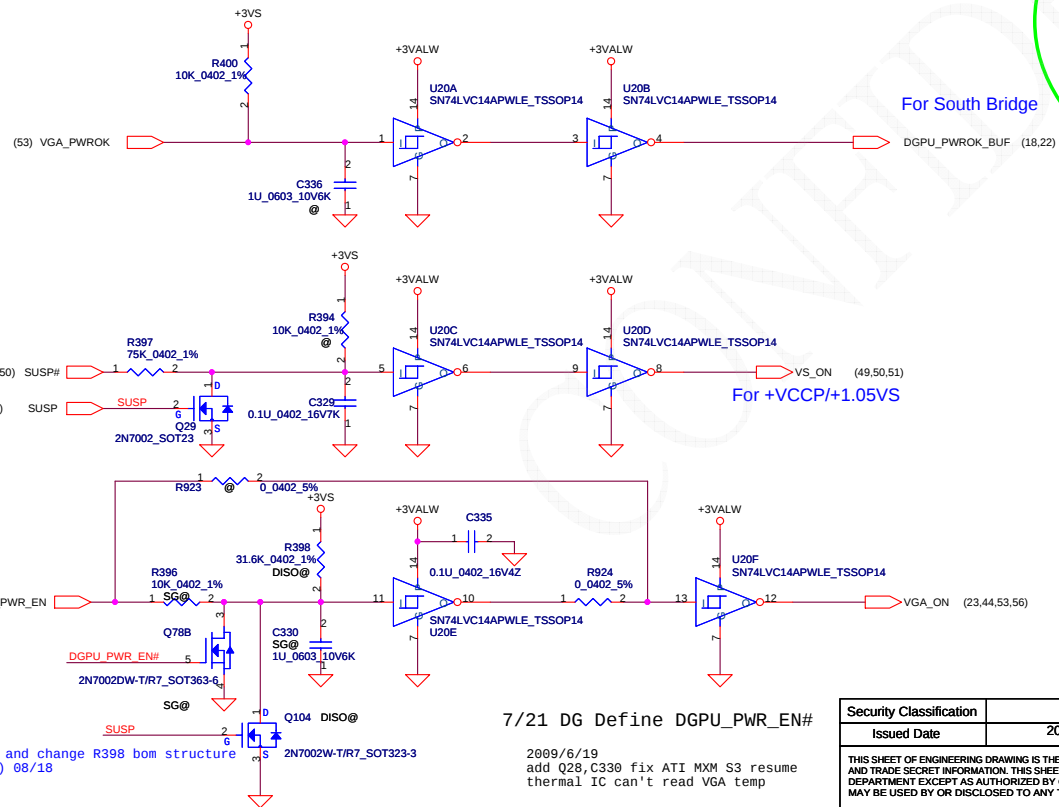
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Power Button

ON/OFF switch

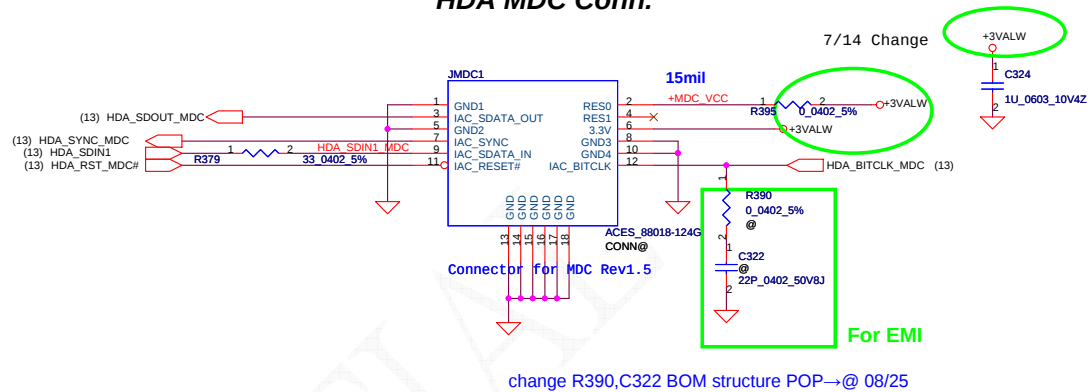


Power ON Circuit

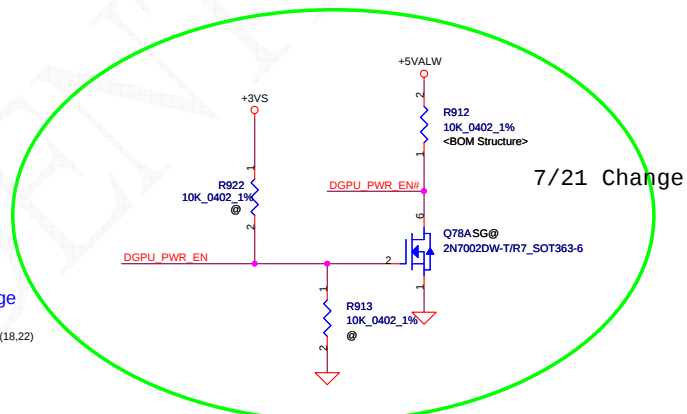


```
7/21 DG Define DGPU_PWR_EN#
```

```
2009/6/19
add Q28,C330 fix ATI MXM S3 resume
thermal IC can't read VGA temp
```

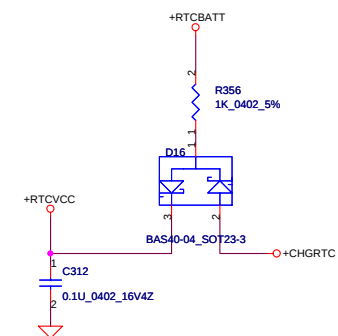
HDA MDC Conn.

change R390,C322 BOM structure POP→@ 08/25

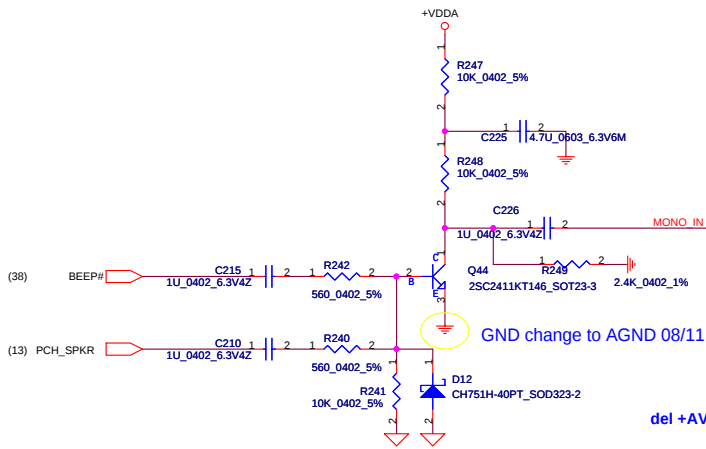


For South Bridge

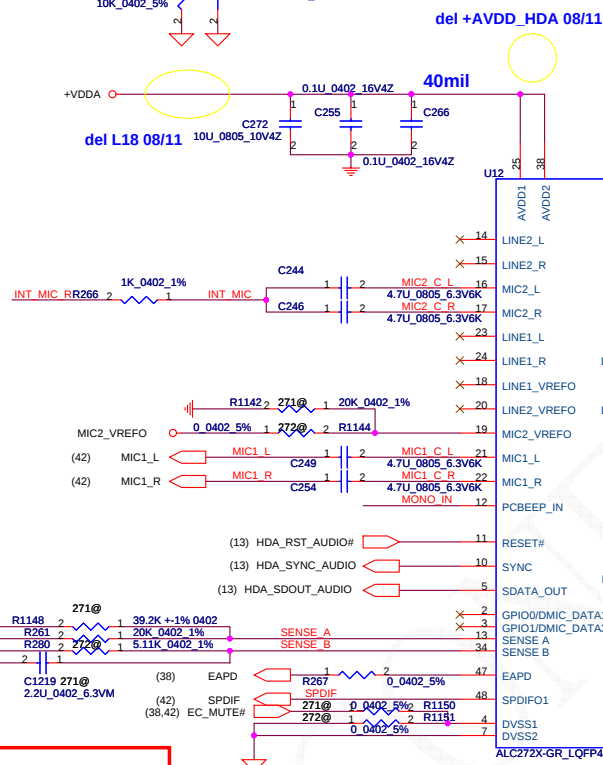
del R442,C362,C361,IR1(CIR) 08/21



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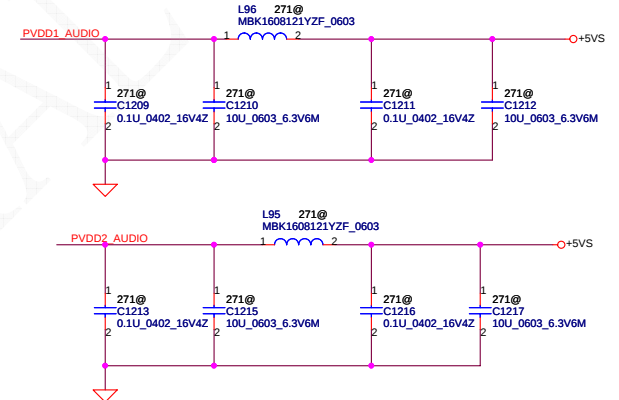
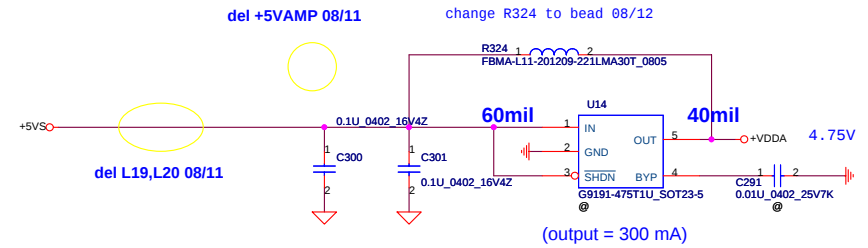
HD Audio Codec



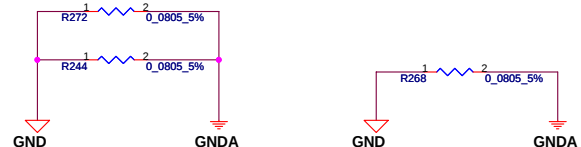
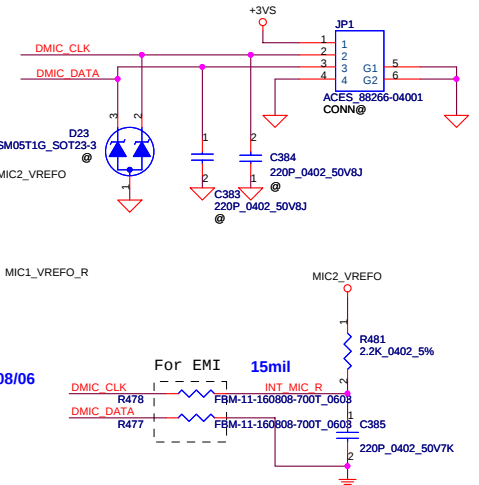
Need update this table

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

add 271 colay circuit 08/18

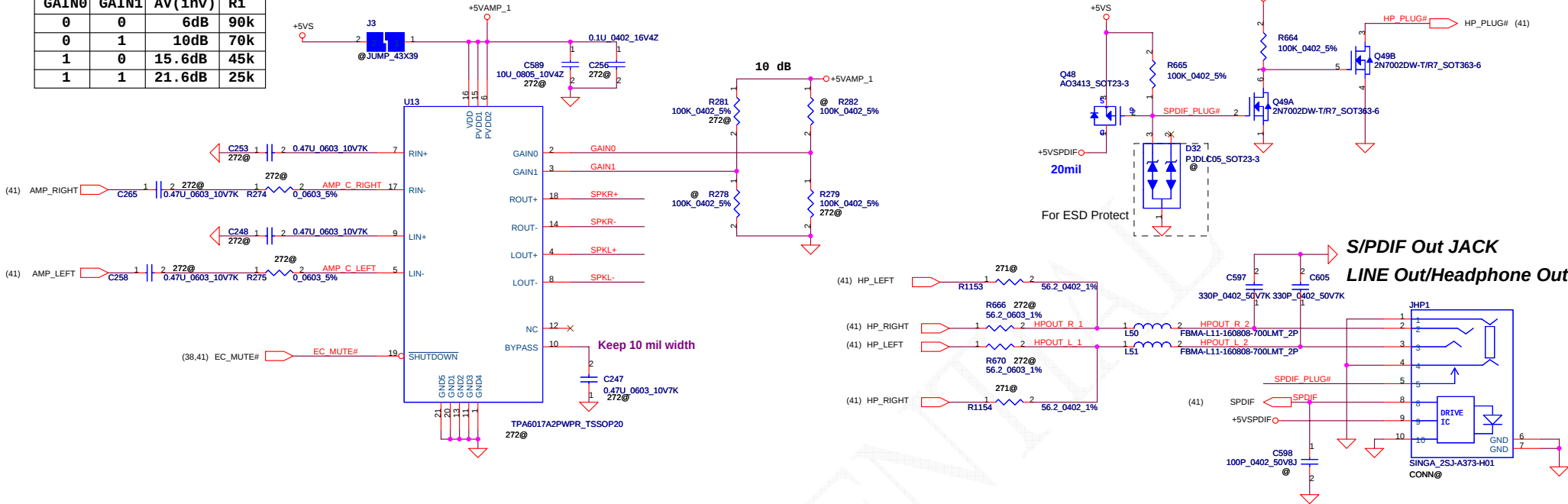


Digital MIC

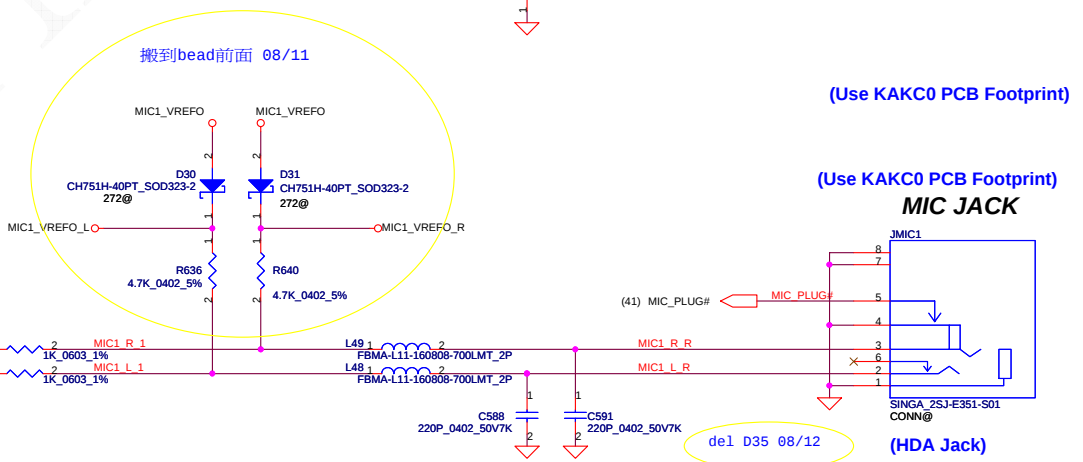
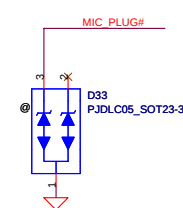
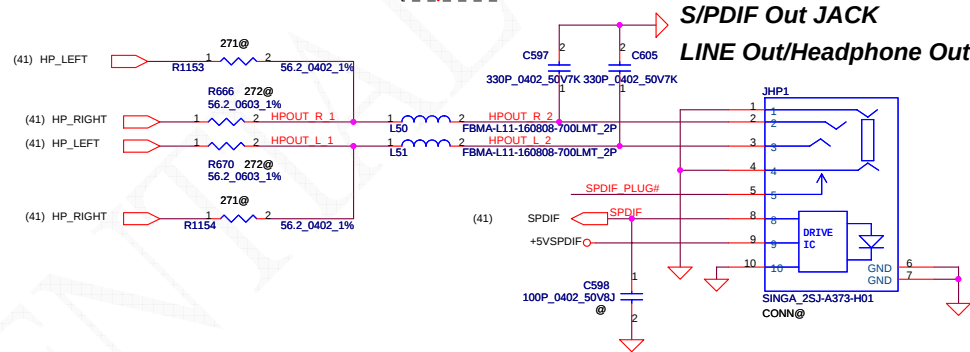
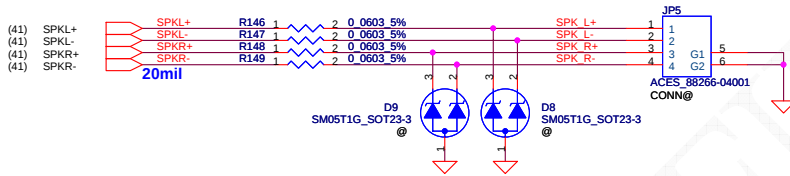


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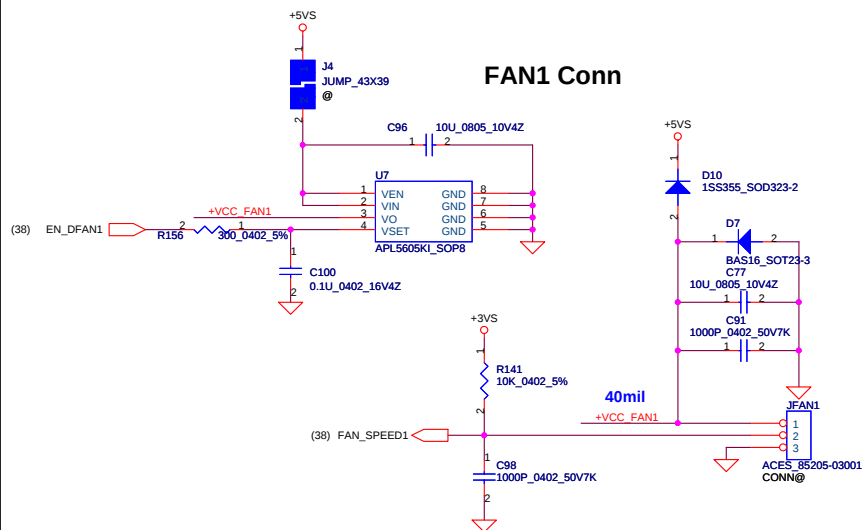
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k



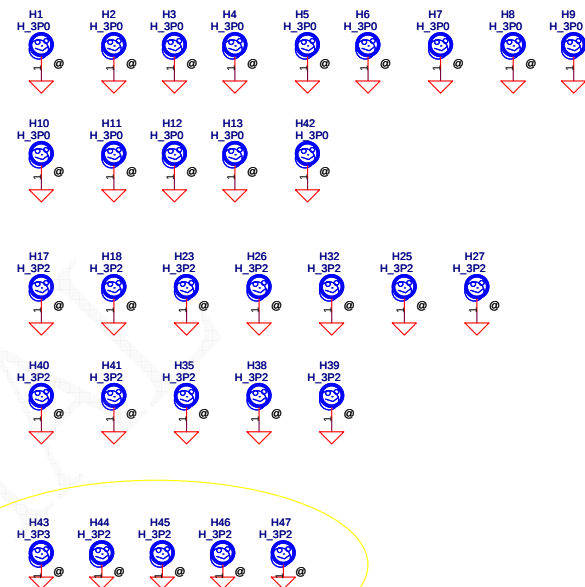
Int. Speaker Conn.



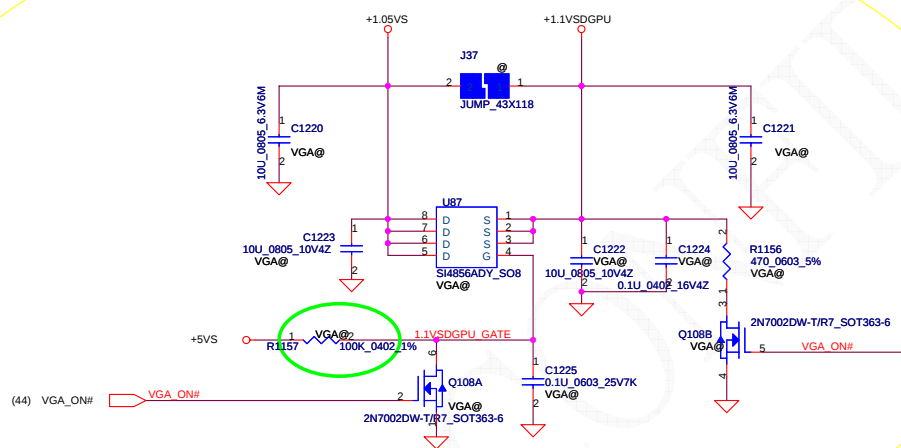
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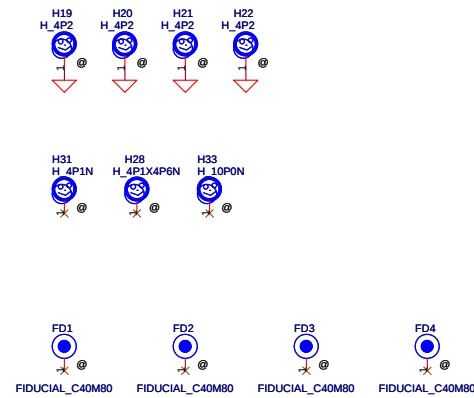
7/20 Del



+1.05VS to +1.1VSDGPU Transfer



add screw 08/19

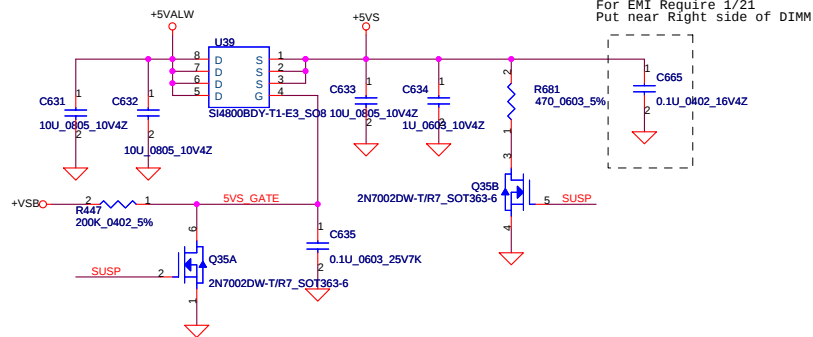


add +1.05VS to +1.1VSDGPU Transfer 08/20

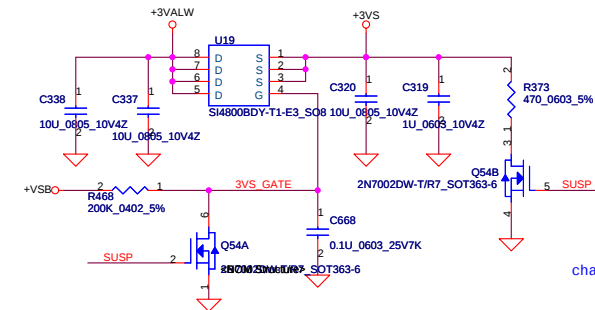
change BOM structure @-VGA@ 08/25

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+5VALW TO +5VS

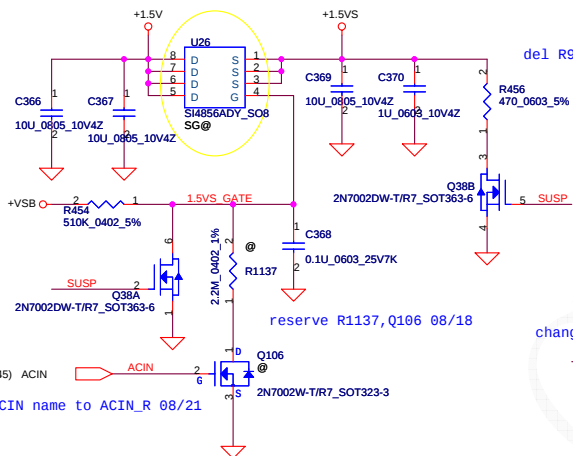


+3VALW TO +3VS



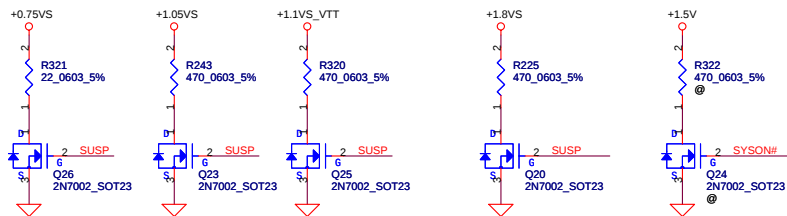
+1.5V to +1.5VS

U26 change to SI4856(Vgs=20) 08/18



reserve R1137, Q106 08/18

change ACIN name to ACIN_R 08/21



+3VALW TO +3V(PCH AUX Power)

+3VALW to +3VMXM Transfer

+5VALW to +5VMXM Transfer

7/14 Change

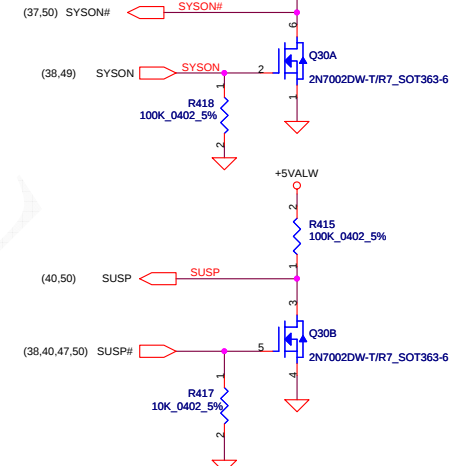
+1.5V to +1.5VSDGPU Transfer

change R904 from 100K to 47K 08/27

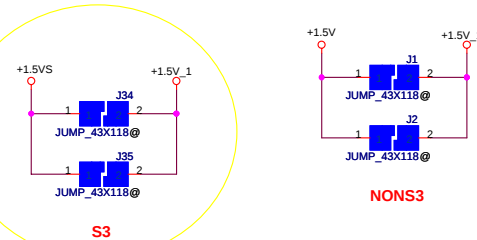
+1.8VS to +1.8VSDGPU Transfer

change R904 from 100K to 200K 08/27

add J36 08/18



For Calpella CPU S3 DRAM Power
(1.5V_CPU VDDQ)



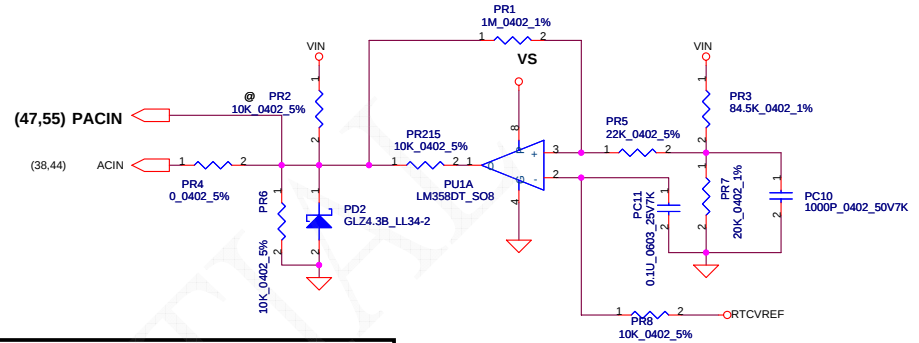
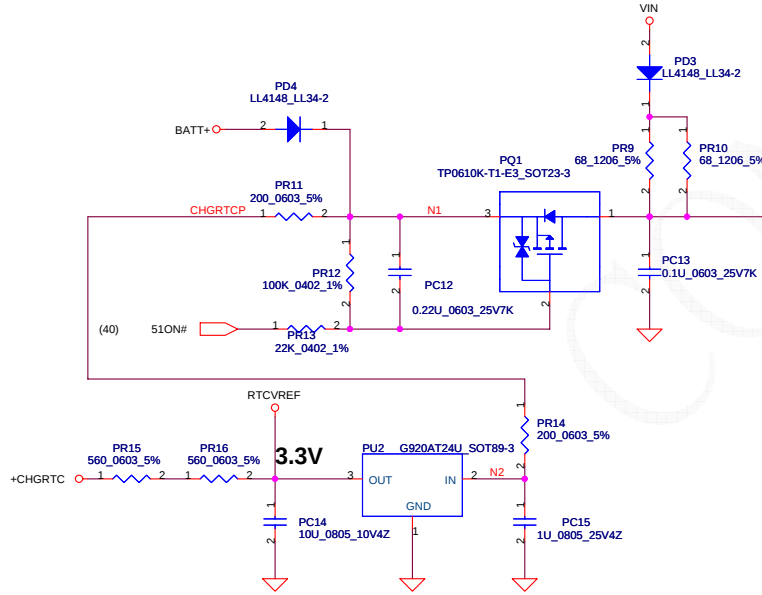
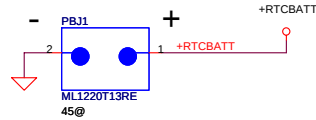
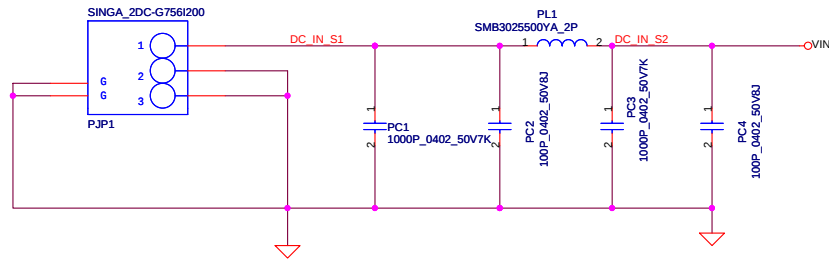
S3

NONS3

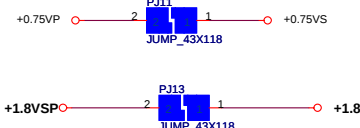
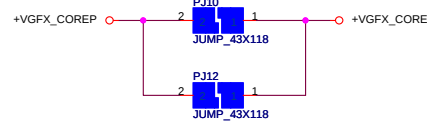
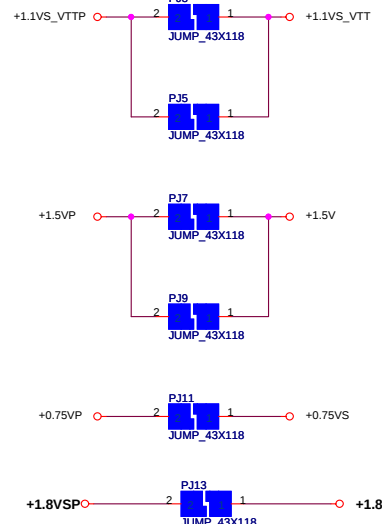
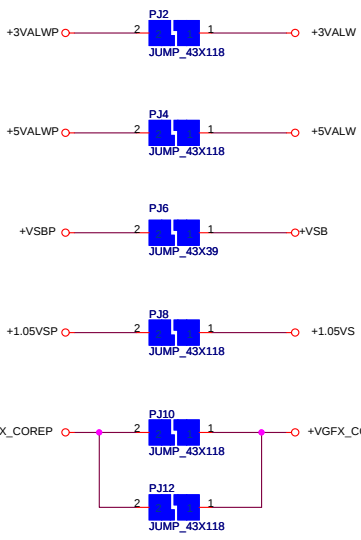
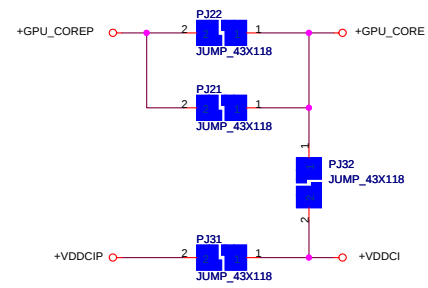
del U74 C929, C930, R948, R949, Q90, Q91
(+1.5V to +1.5V_1 circuit) 08/17

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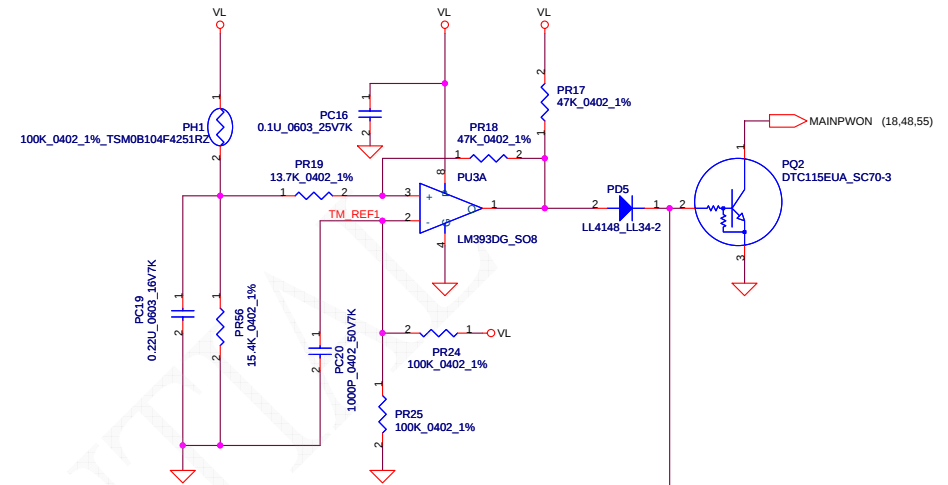
DC231000500



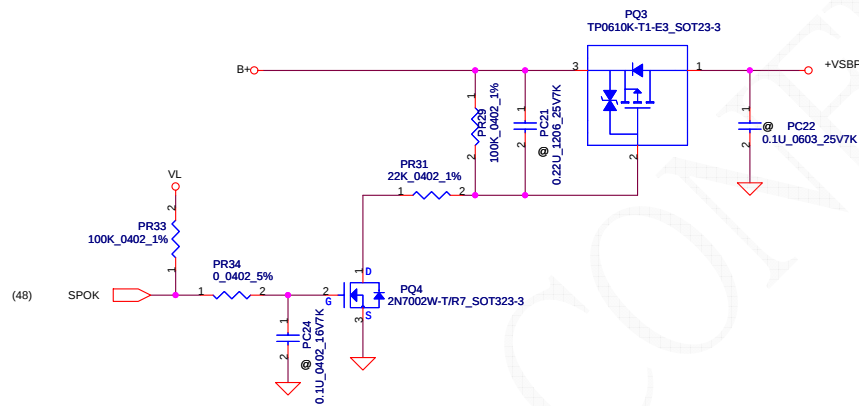
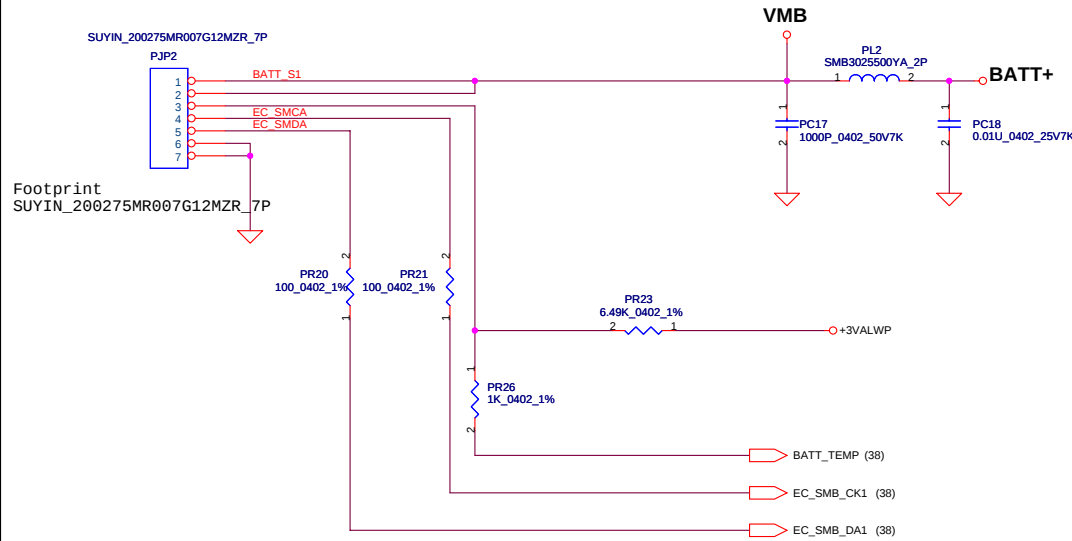
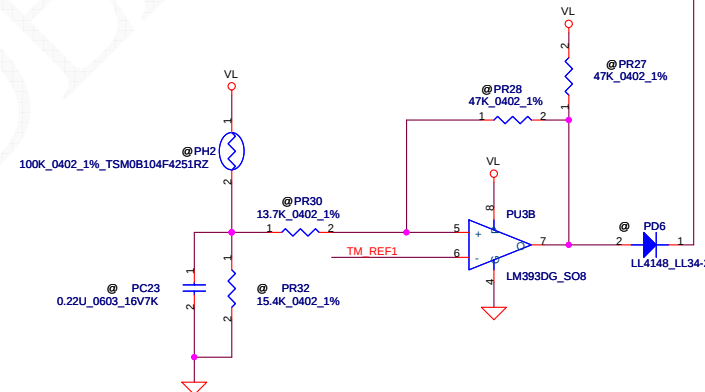
	Min.	Typ	Max.
H-->L	17.208V	17.212V	17.217V
L-->H	17.879V	17.894V	17.909V



PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C

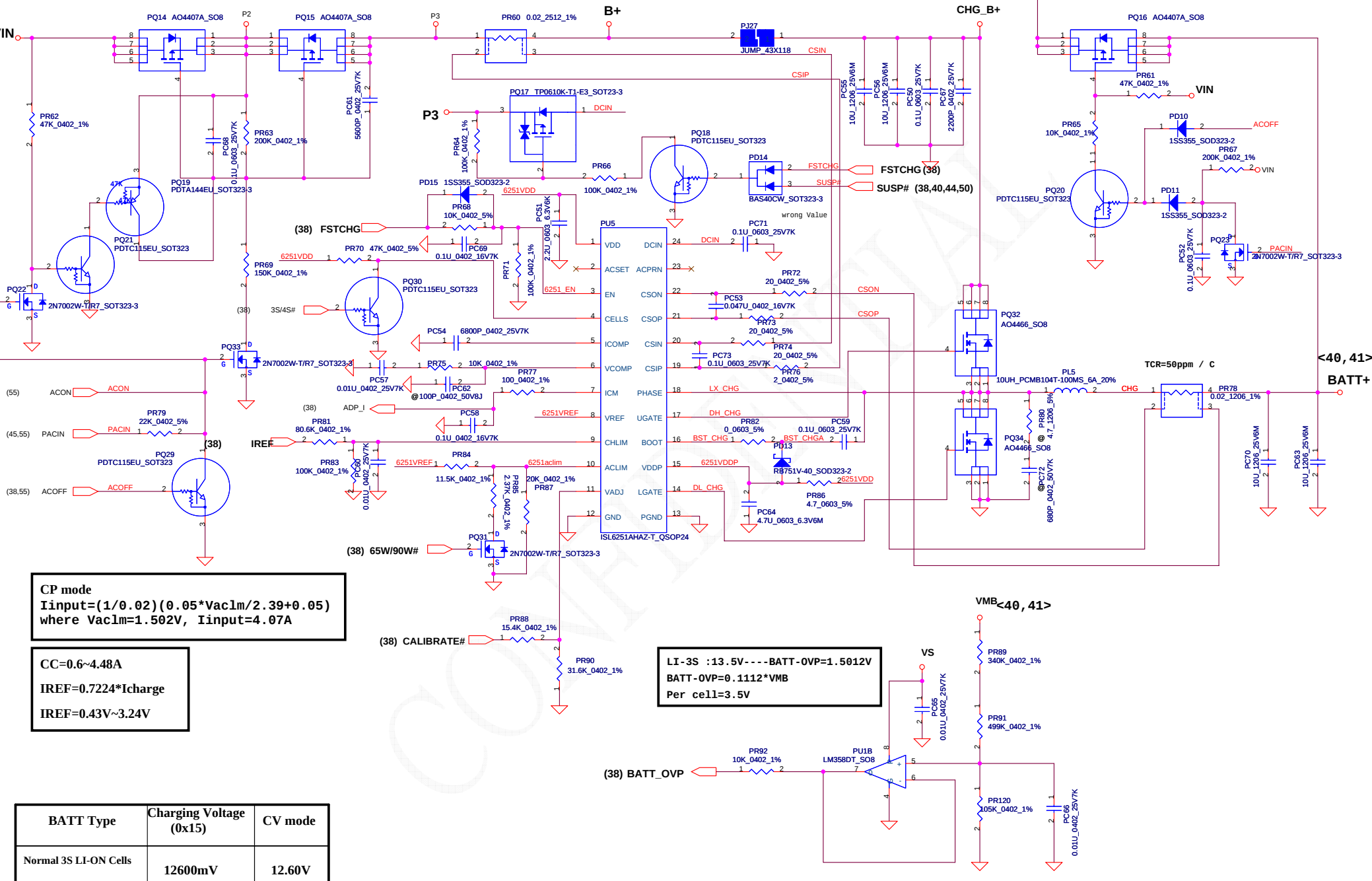


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Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
 $I_{input} = (1/0.02)(0.05 \cdot V_{ac1m}/2.39 + 0.05)$
where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

CC=0.6~4.48A
 $I_{REF} = 0.7224 \cdot I_{charge}$
 $I_{REF} = 0.43V \sim 3.24V$

LI-3S :13.5V---BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

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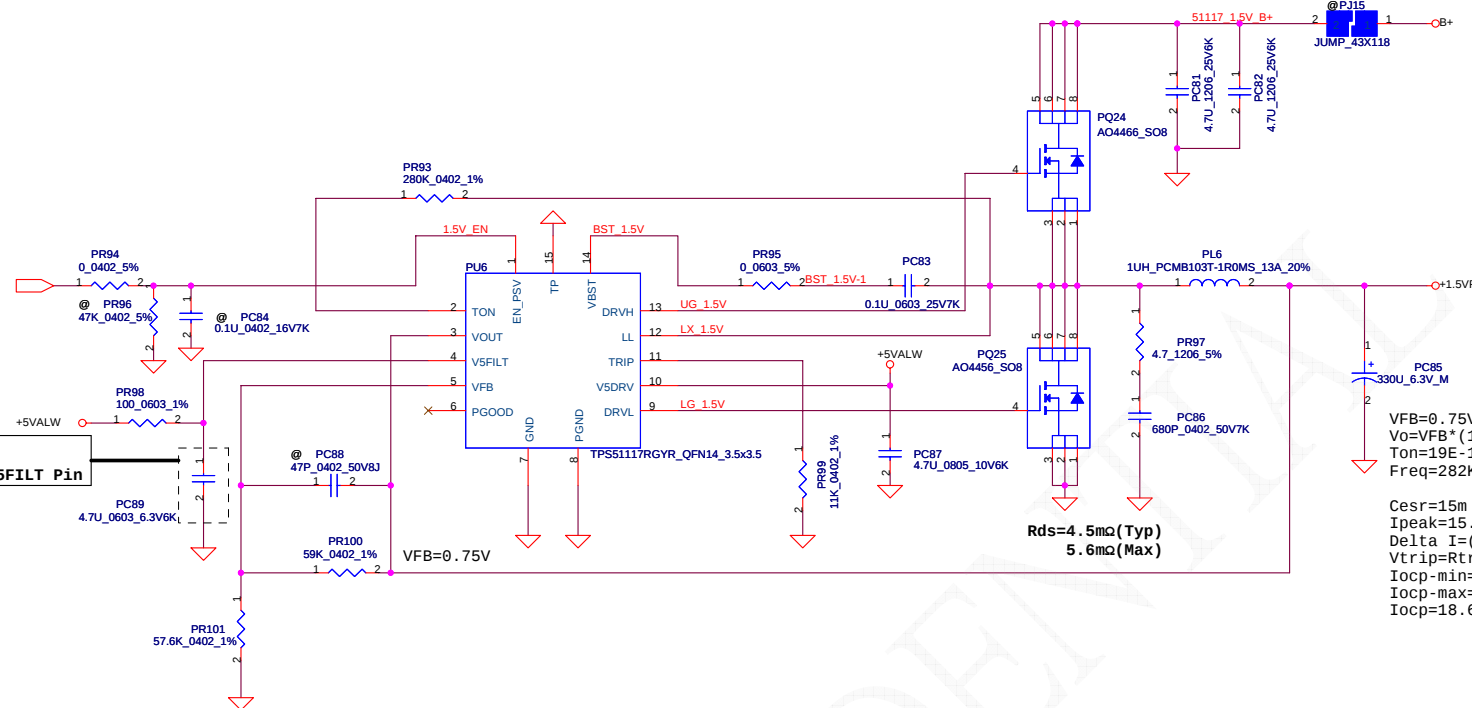
+3.3VALWP Ipeak=7A ; Imax=4.9A
 Choke DCRmax=40m ohm, DCRtyp=37m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 $V_{limit} = (5E-06 * 330K) / 10 = 165mV$
 $I_{limit} = 165mV / 18m \sim 165mV / 15m$
 $= 9.167A \sim 11A$
 $I_{ocp} = I_{limit} + \Delta I / 2$
 $= 10.134A \sim 11.967A$
 $\Delta I = 1.934A$ (Freq=300KHz)

+5VALWP Ipeak=7A ; Imax=4.9A
 Choke DCRmax=40m ohm, DCRtyp=37m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 $V_{limit} = (5E-06 * 330K) / 10 = 165mV$
 $I_{limit} = 165mV / 18m \sim 165mV / 15m$
 $= 9.167A \sim 11A$
 $I_{ocp} = I_{limit} + \Delta I / 2$
 $= 10.147A \sim 11.980A$
 $\Delta I = 1.96A$ (Freq=400KHz)

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(38,44) SYSON

Layout Note:
Place near V5FILT Pin

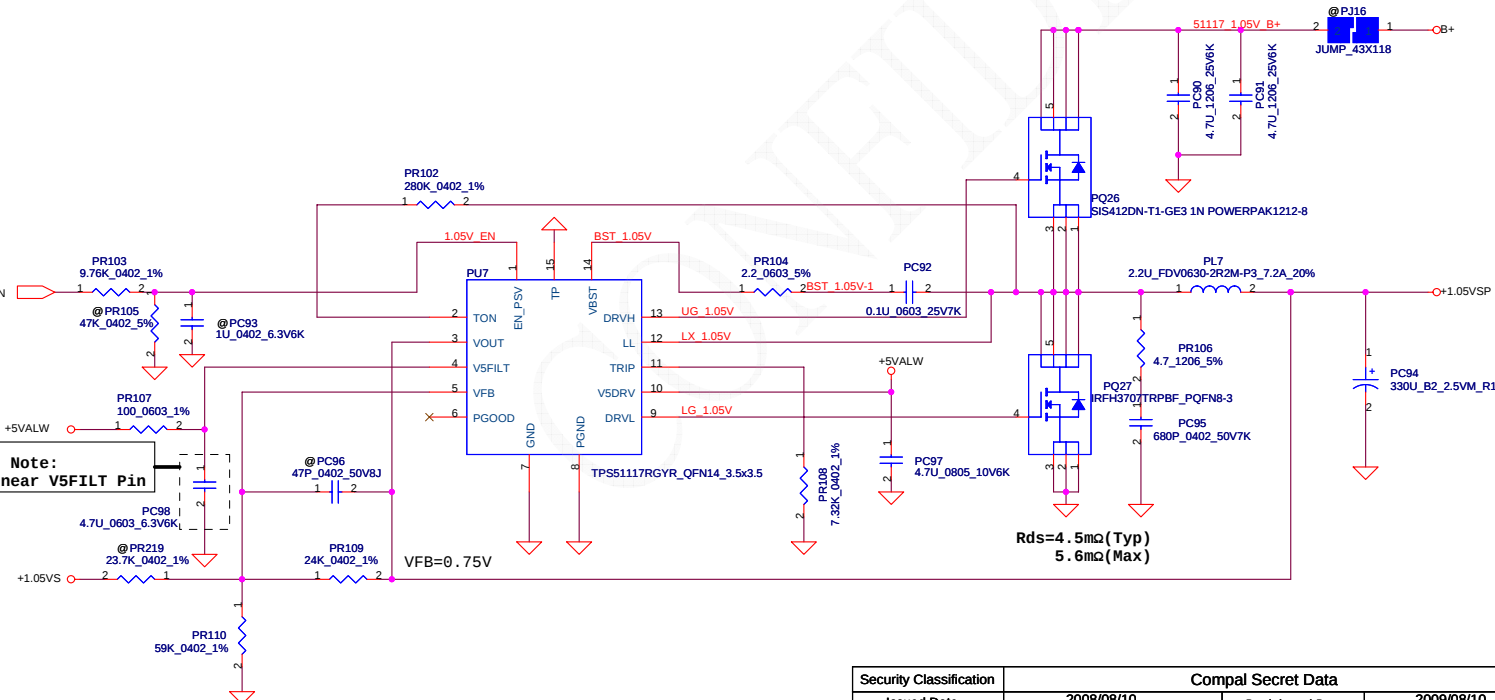


VFB=0.75V
 $V_o = VFB * (1 + PR298 / PR299) = 1.52V$
 $T_{on} = 19E-12 * R_{on} * (((2/3) * V_o + 100mV) / V_{in}) + 50ns = 3.8E-7$
Freq=282KHz(min) , 300KHz(typ)

Cesr=15m ohm
Ipeak=15.58A Imax=10.906A
 $\Delta I = ((19-1.5) * (1.5/19)) / (L * Freq) = 4.61A$
 $V_{trip} = R_{trip} * I_{ocp} = 0.11V$
 $I_{ocp-min} = V_{trip} / (R_{ds(on)}(max) * 1.2) + \Delta I / 2 = 18.674A$
 $I_{ocp-max} = V_{trip} / (R_{ds(on)}(typ) * 1.2) + \Delta I / 2 = 22.675A$
Iocp=18.674-22.675A

0,50,51) VS_ON

Layout Note:
Place near V5FILT Pin



VFB=0.75V
 $V_o = VFB * (1 + PR308 / PR309) = 1.05V$
 $T_{on} = 19E-12 * R_{on} * (((2/3) * V_o + 100mV) / V_{in}) + 50ns = 2.74E-07$
Freq=282KHz , 300KHz(typ)

Cesr=15m ohm
Ipeak=10.9A Imax=7.63A
 $\Delta I = ((19-1.05) * (1.05/19)) / (L * Freq) = 1.837A$
 $V_{trip} = R_{trip} * I_{ocp} = 0.0732V$
 $I_{ocp-min} = V_{trip} / (R_{ds(on)}(max) * 1.2) + \Delta I / 2 = 11.81A$
 $I_{ocp-max} = V_{trip} / (R_{ds(on)}(typ) * 1.2) + \Delta I / 2 = 14.47A$
Iocp=11.81-14.47A

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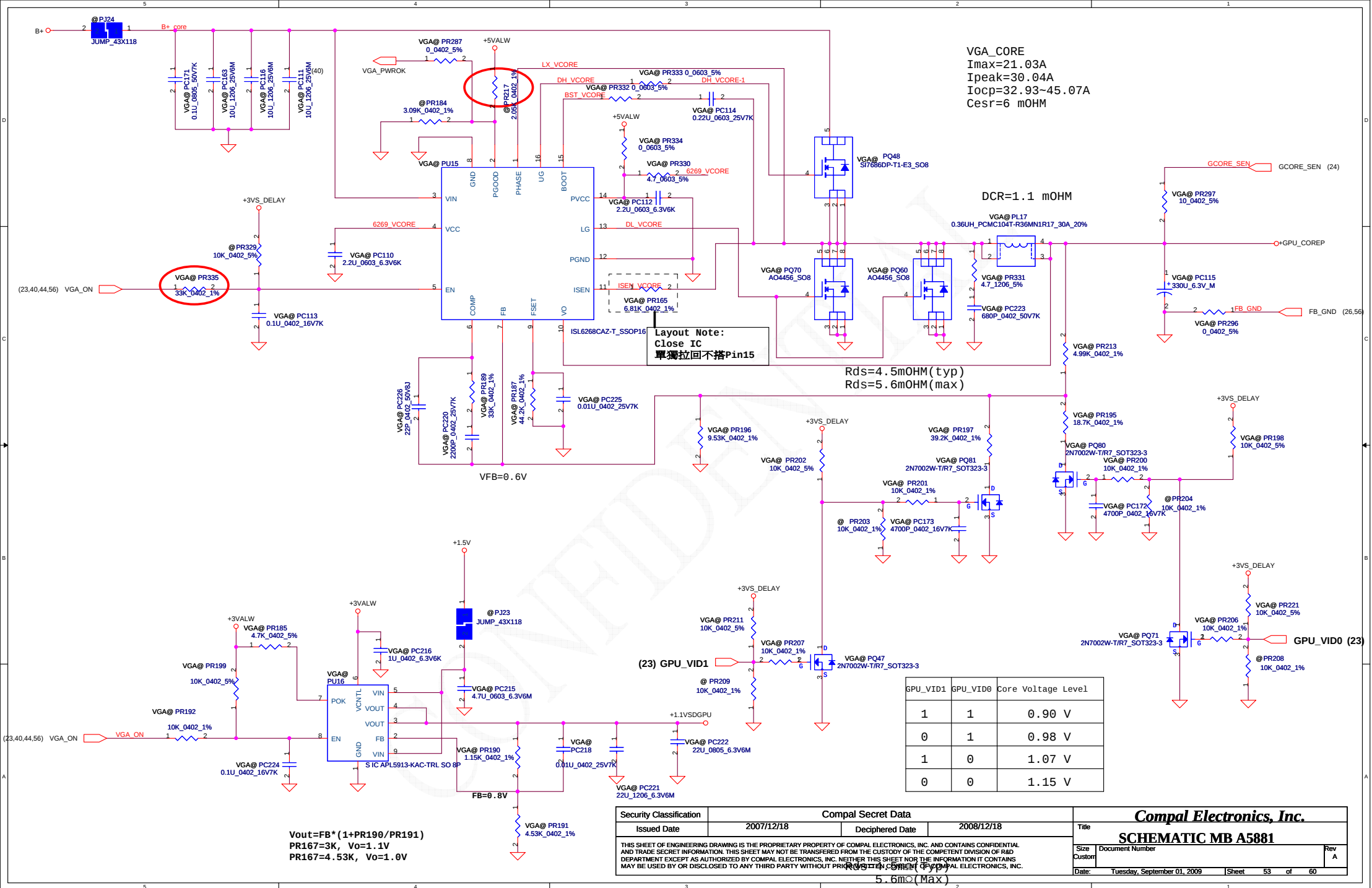
Layout Note:
Place near high-side MOS Drain
and low-side MOS Source

Layout Note:
Close IC

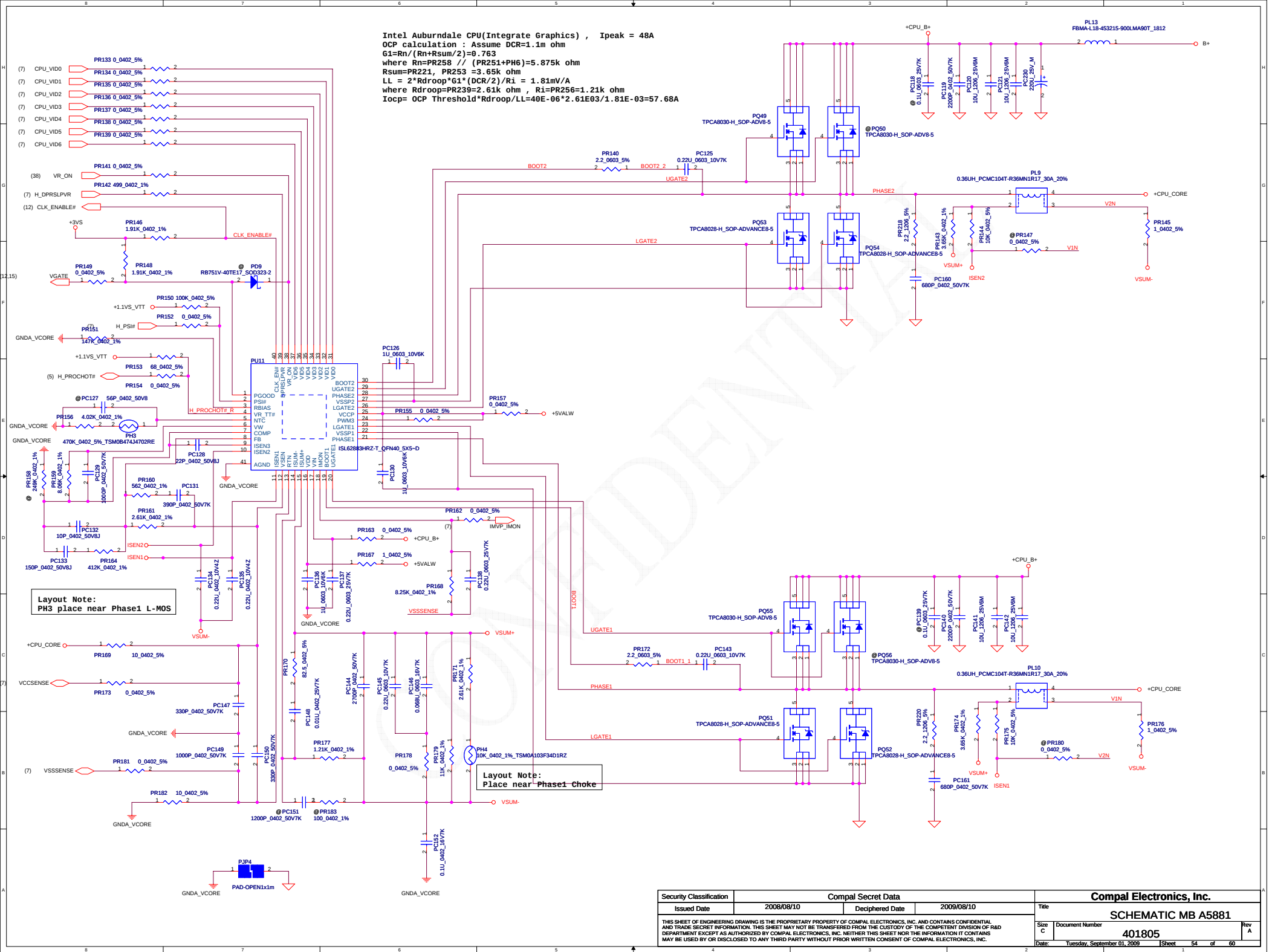
Material Note:
330uF/6 mΩ, number
are 3, Power 1, HW 2

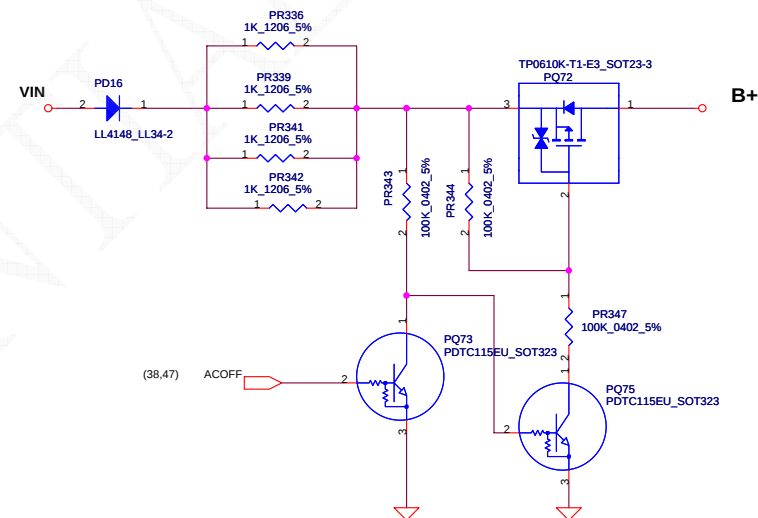
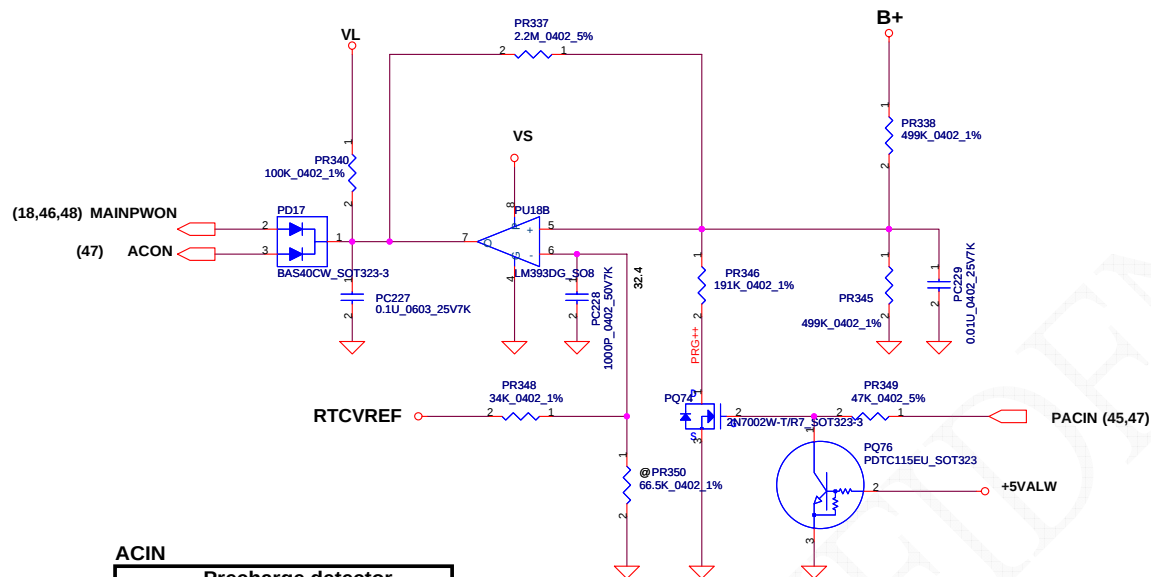
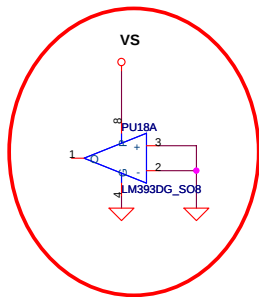
+1.1VS_VTT
Ipeak=25.41A
Imax=17.79A
Delta I / 2 = 2.176A , Freq=230K Hz
Iocp(min)=Ipeak + Delta I / 2 = 27.586A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=2.787K ohm
ISEN(min)=19uA , Rds(on)=3.2m ohm(max) , 2.3m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=38.372A
Iocp=27.586-38.272A

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Intel Auburndale CPU(Integrate Graphics) , Ipeak = 48A
OCP calculation : Assume DCR=1.1m ohm
 $G1 = R_n / (R_n + R_{sum} / 2) = 0.763$
where $R_n = PR258 // (PR251 + PH6) = 5.875k \text{ ohm}$
 $R_{sum} = PR221, PR253 = 3.65k \text{ ohm}$
 $LL = 2 * R_{droop} * G1 * (DCR / 2) / R_i = 1.81mV/A$
where $R_{droop} = PR239 = 2.61k \text{ ohm}$, $R_i = PR256 = 1.21k \text{ ohm}$
 $I_{ocp} = OCP \text{ Threshold} * R_{droop} / LL = 40E-06 * 2.61E03 / 1.81E-03 = 57.68A$





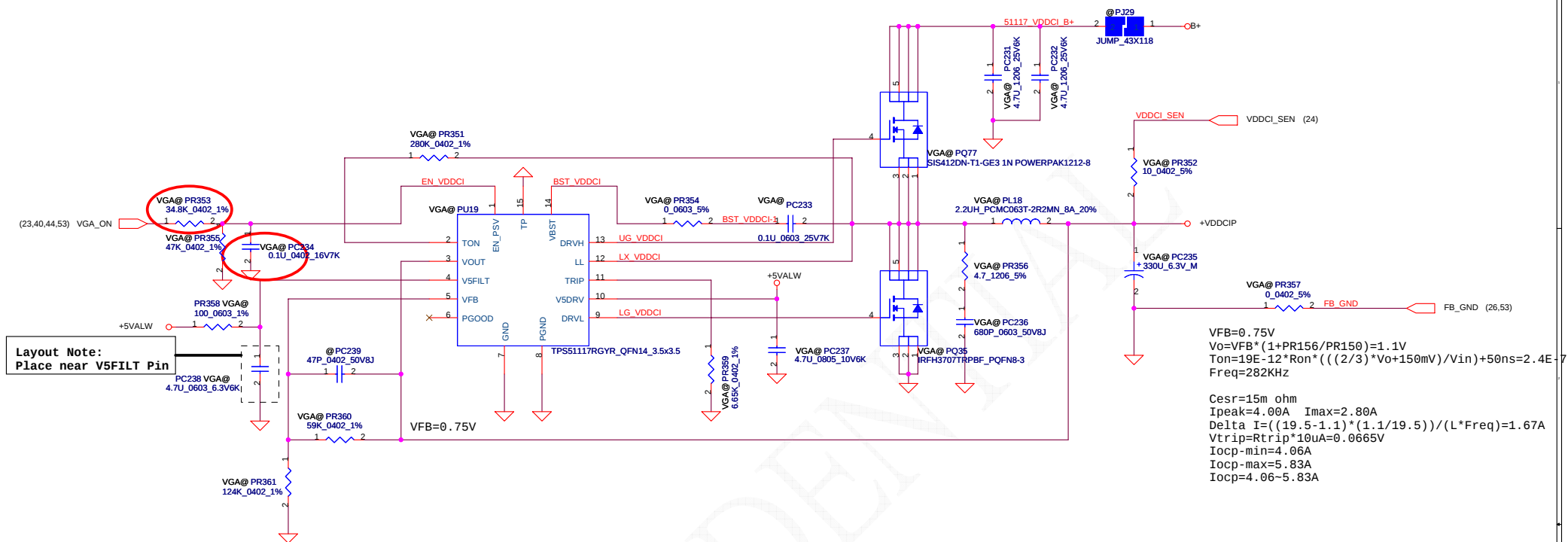
ACIN

Precharge detector			
Min.	typ.	Max.	
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector			
Min.	typ.	Max.	
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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A --> B Change List

Reference to KBLA0 LA4811 Change List Excel File

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	add all sunbber R	EMI solution	0.1	52		09/08/27	DVT
2	add all sunbber C	EMI solution	0.1	52		09/08/27	DVT
3	remove VGA enable R	HW request	0.1	53	delete PR217 2.05K_0402_1%	09/08/27	DVT
4	VDDCI EN sequency regulate	HW request	0.1	53	PR335:32k P/N:SD034330280	09/08/27	DVT
5	VGA EN sequency regulate	HW request	0.1	53	PR353 : 35k P/N:SD00000UD80 PC234 : @==> add	09/08/27	DVT
6							
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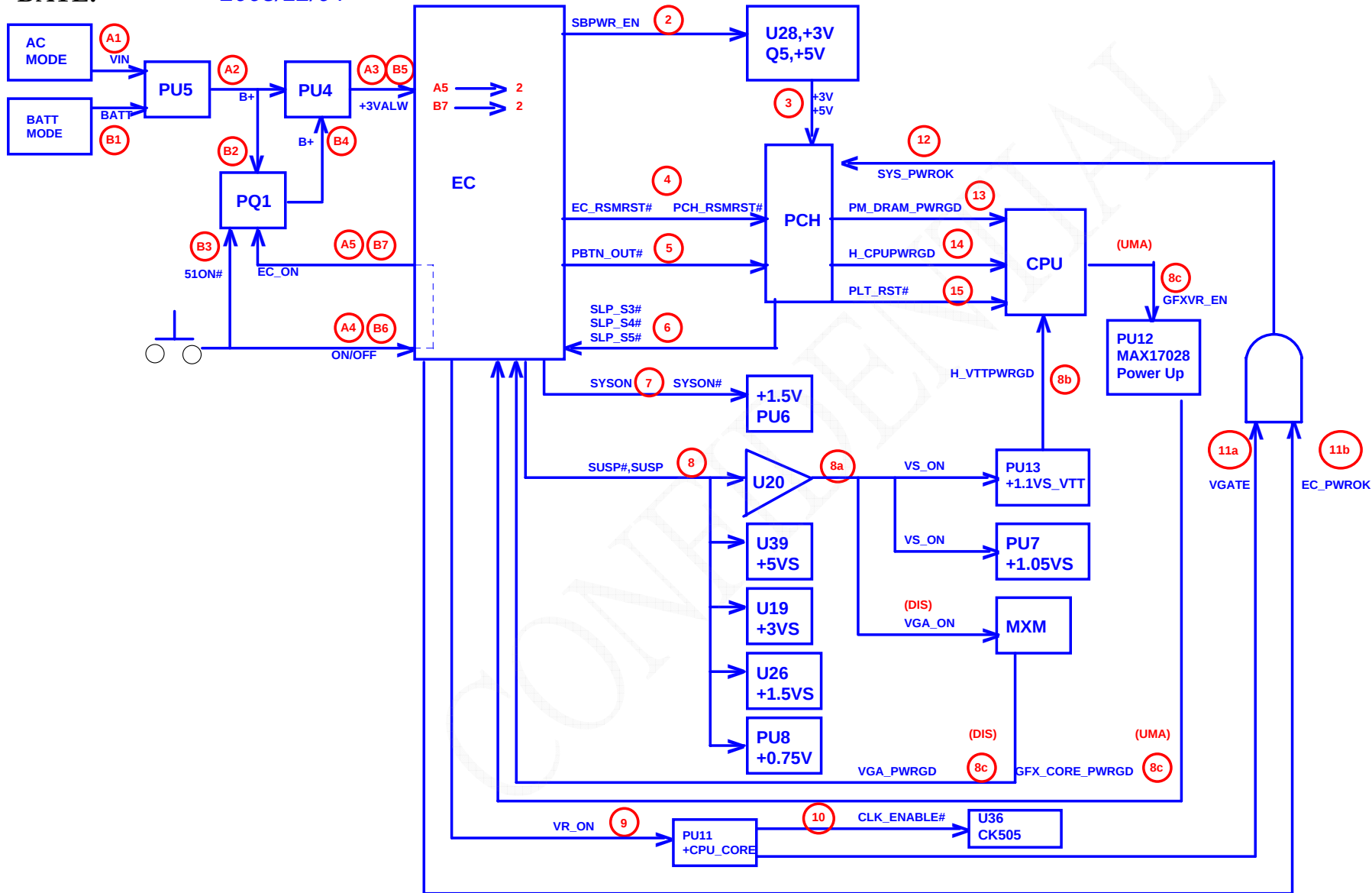
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MODEL NAME: *KBLA0 Power Sequence Block Diagram*

PCB NAME: *LA4811P*

REVISION:

DATE: *2008/12/04*



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