

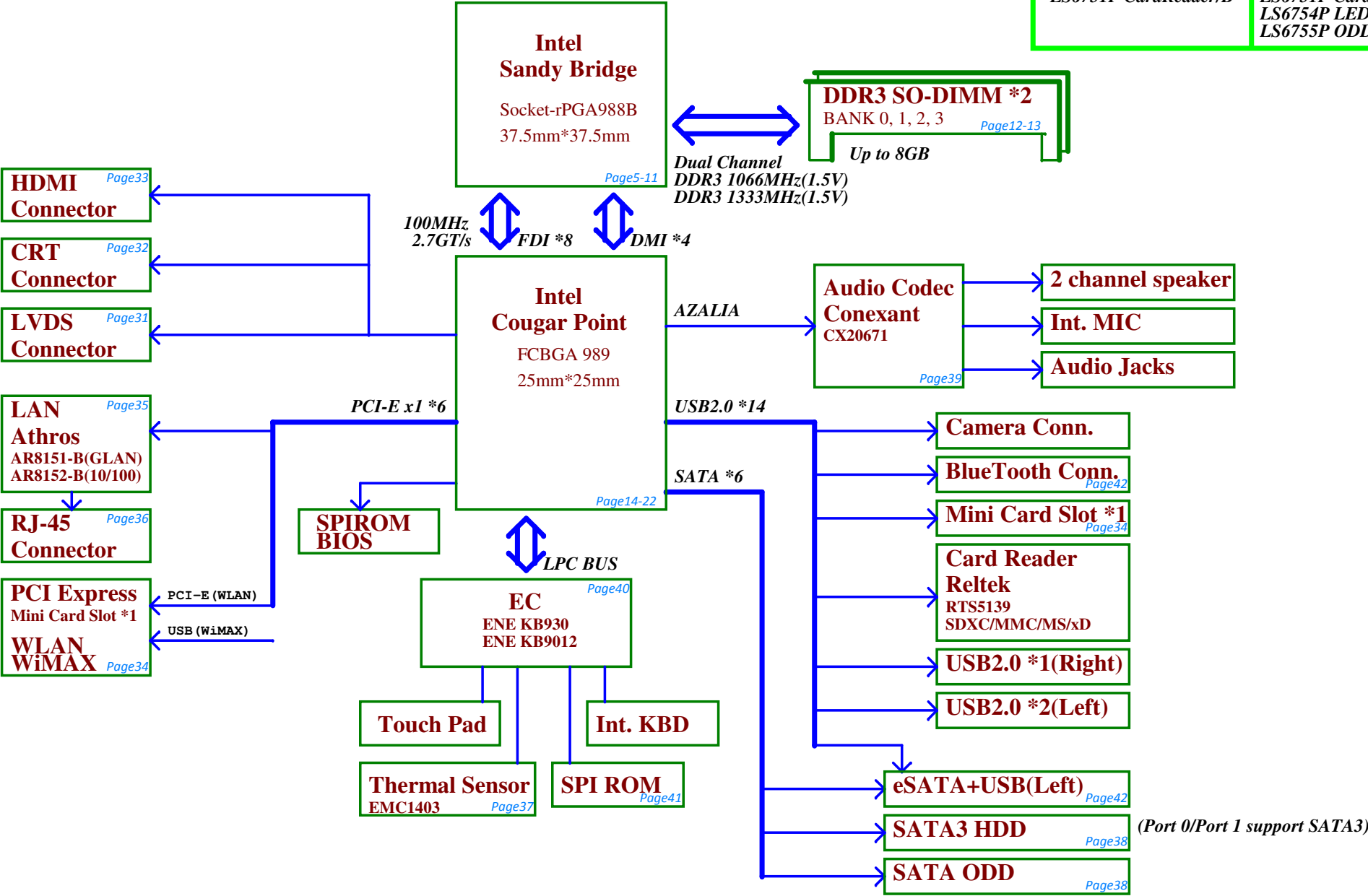
Compal Confidential
G470/G570 UMA M/B Schematics Document
Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH

2010-10-22
LA-6752P / LA-6754P
REV:0.2

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For 14"(Page 4x)
LS6753P PWR/B
LS6751P CardReader/B

For 15"(Page 4x+1)
LS6753P PWR/B
LS6751P CardReader/B
LS6754P LED/B
LS6755P ODD/B



Voltage Rails				
power plane	State	+B	+5VALW +3VALW	+1.5V +5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0		○	○	○
S3		○	○	×
S5 S4/AC		○	○	×
S5 S4/ Battery only		○	×	×
S5 S4/AC & Battery don't exist		×	×	×

EC SM Bus1 address			EC SM Bus2 address		
Device	Address		Device	Address	
Smart Battery	0001 011X b		Thermal Sensor EMC1403-2	1001_101xb	

PCH SM Bus address	
Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

SMBUS Control Table								
	SOURCE	VGA	BATT	KE930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB930	×	✓	×	×	×	×	×
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB930	×	×	×	×	×	×	✓
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	×	×	×	✓	✓	×	×
SMBDATA	+3VALW				+3VS	+3VS		
SML0CLK	PCH	×	×	×	×	×	×	×
SML0DATA	+3VALW							
SML1CLK	PCH	✓	×	✓	×	×	✓	×
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra/Rc/Re	100K +/- 5%				
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0	0 V	0 V	0 V	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	MP
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB Port (Left Side)
		3	USB Port (Left Side)
	UHCI2	4	
		5	Camera
	UHCI3	6	
EHCI2		7	
		8	Mini Card(WLAN)
	UHCI4	9	
		10	
	UHCI5	11	Card Reader
		12	
	UHCI6	13	Blue Tooth

BOM Structure Table

BTO Item	BOM Structure
CAMERA DEVICE	CMOS@
Blue Tooth	BT@
eSATA	ESATA@
COMMON HDMI	HDMI@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8152@
GIGA LAN	GIGA@
Unpop	@

Power-Up/Down Sequence

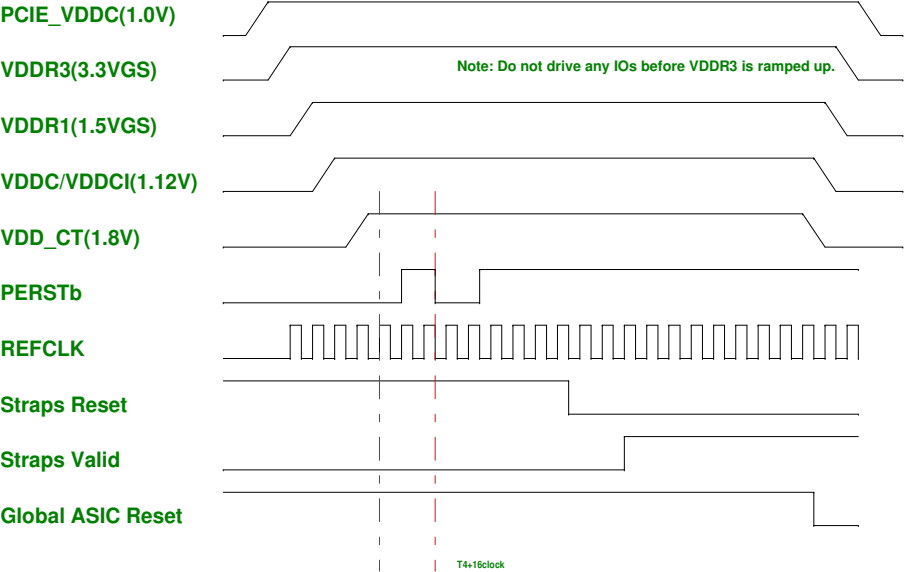
All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

VDDR3 should ramp-up before or simultaneously with VDDC.

For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation

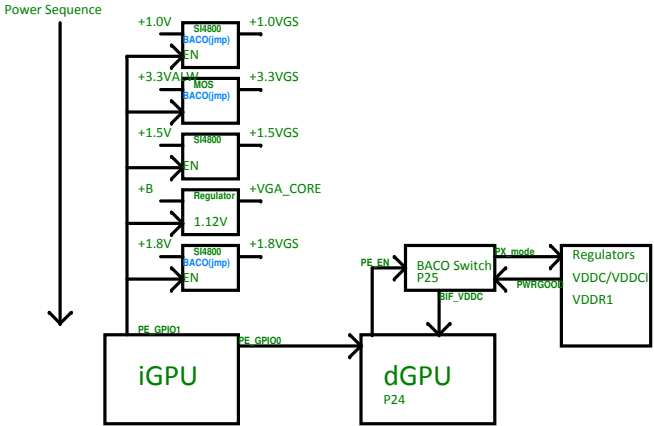
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)

PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

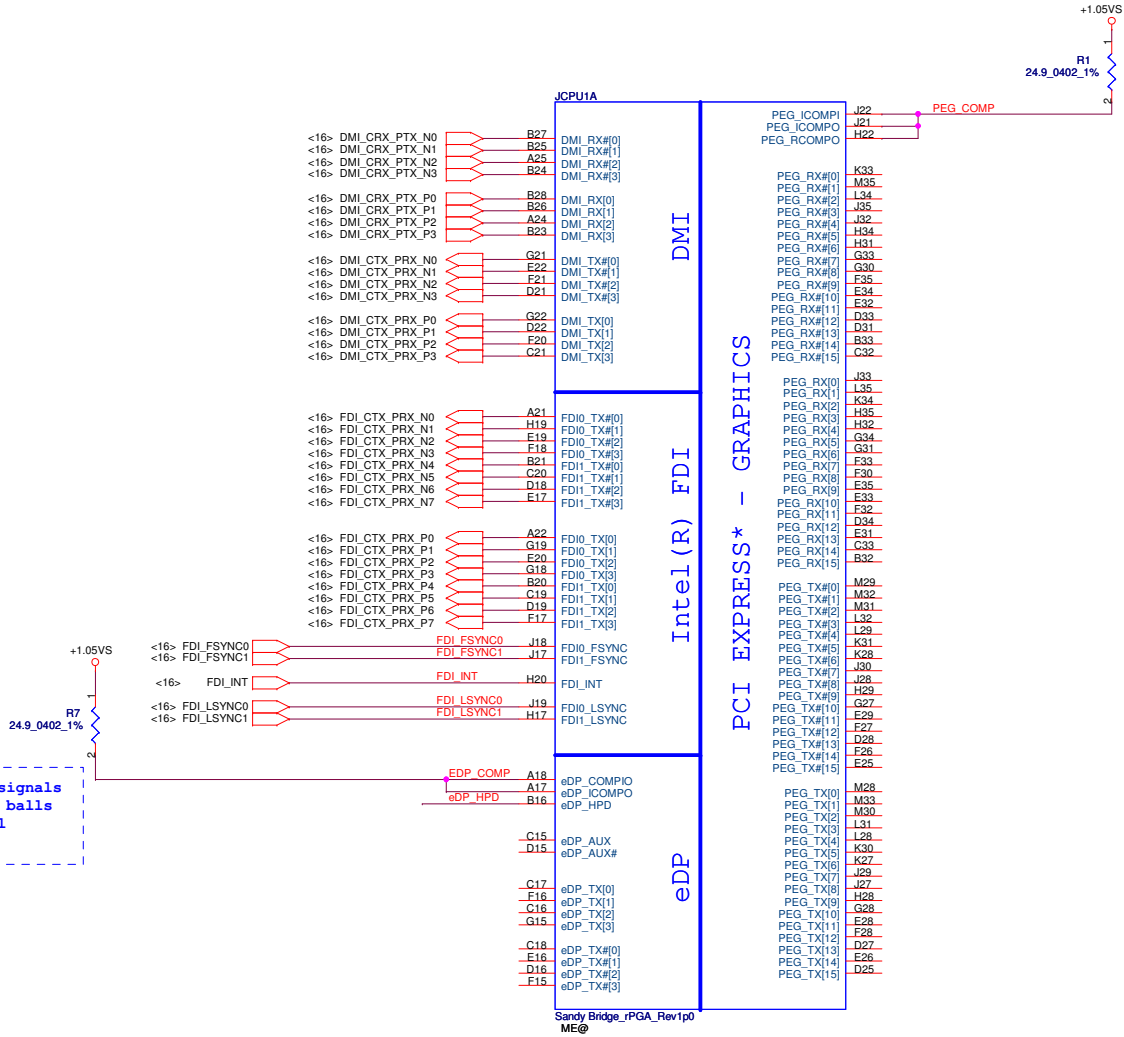
dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIe_PVDD, PCIe_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIe_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIe_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A

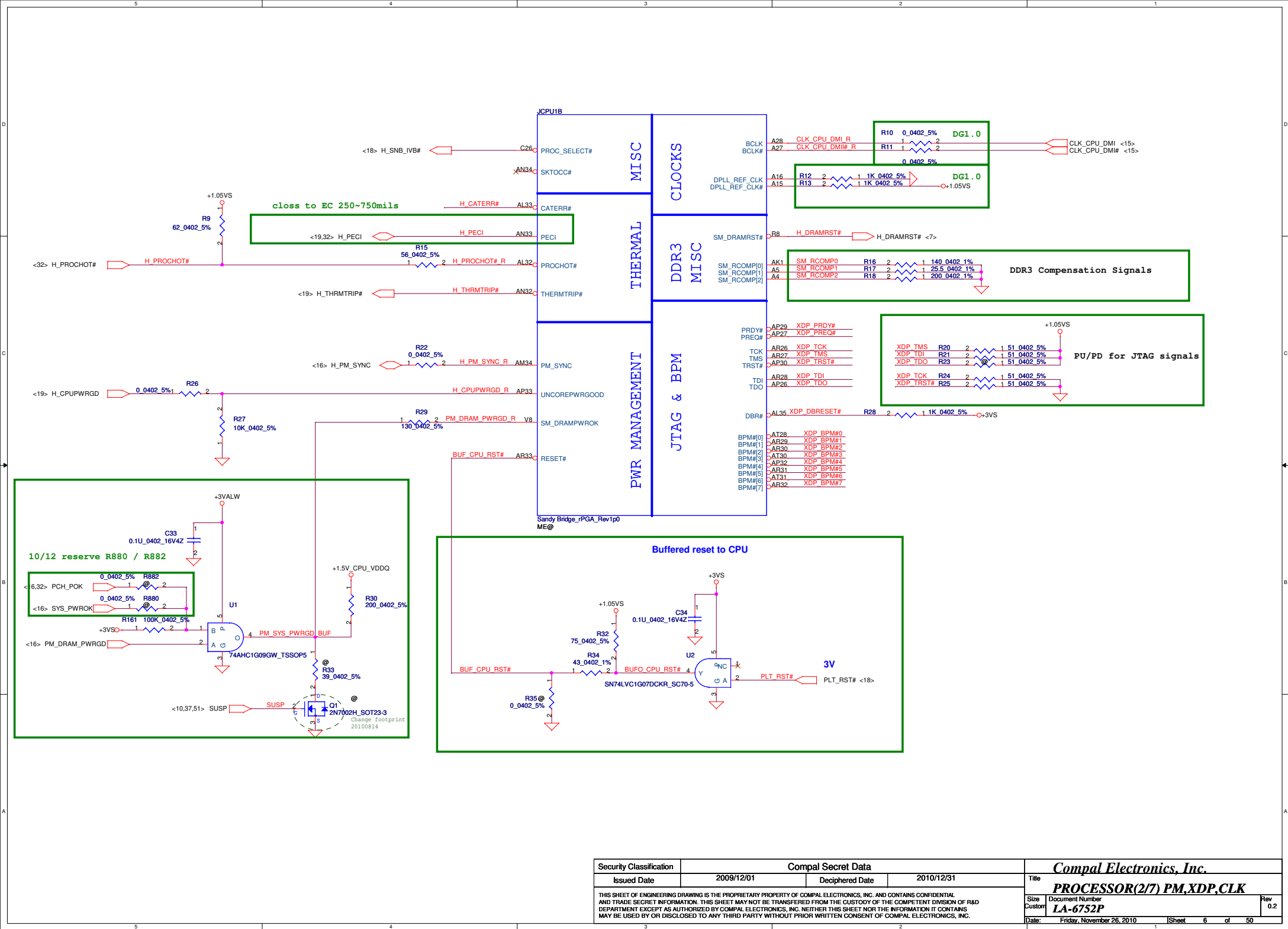


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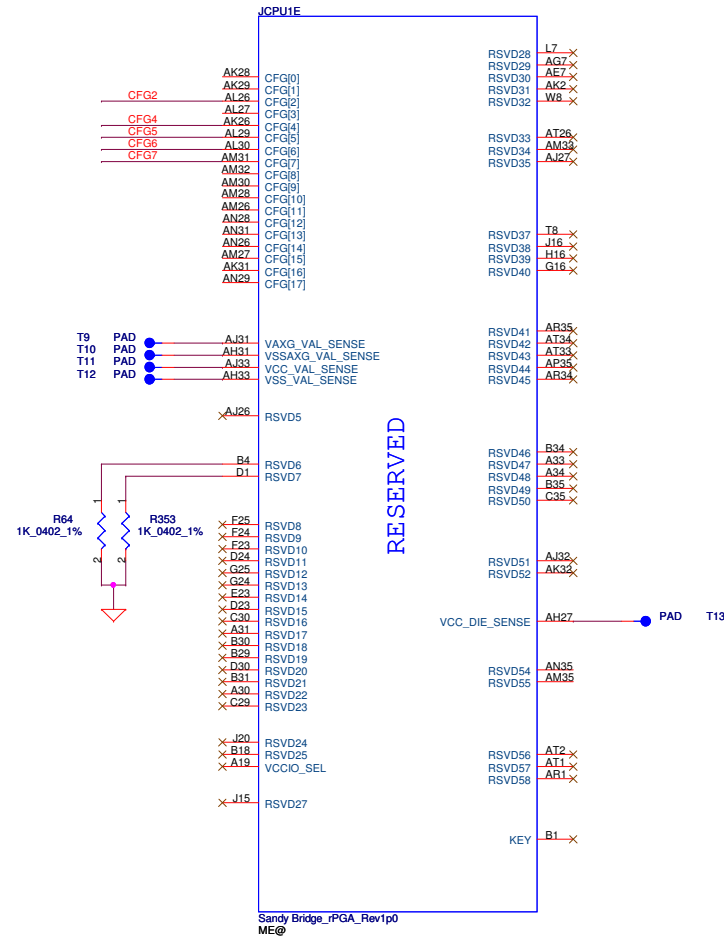
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms





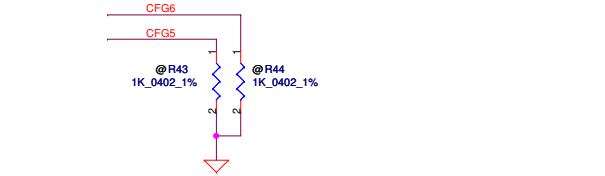
CFG Straps for Processor



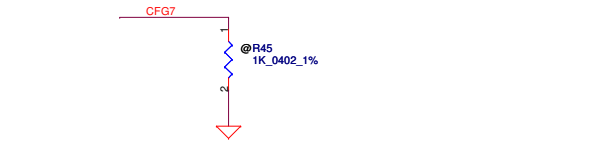
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

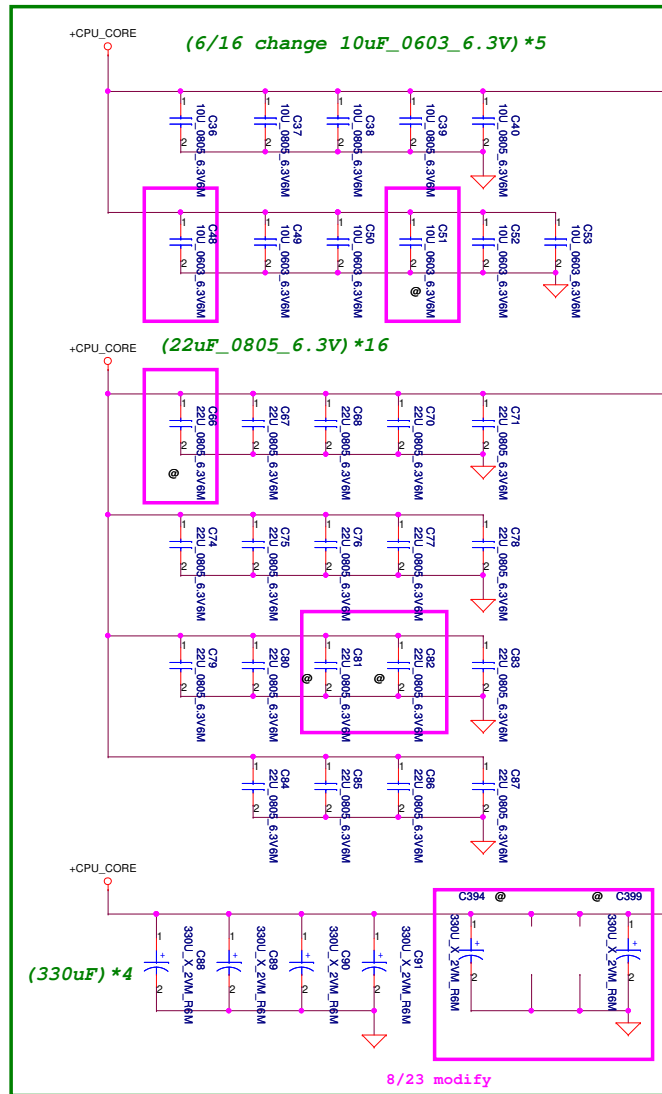


PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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	50						

Compal Electronics, Inc.

PROCESSOR(4/7) RSVD,CFG



QC=94A
DC=53A

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
Y35	VCC50
Y34	VCC51
Y33	VCC52
Y32	VCC53
Y31	VCC54
Y30	VCC55
Y29	VCC56
Y28	VCC57
Y27	VCC58
Y26	VCC59
Y25	VCC60
Y24	VCC61
Y23	VCC62
Y22	VCC63
Y21	VCC64
Y20	VCC65
Y19	VCC66
Y18	VCC67
Y17	VCC68
Y16	VCC69
Y15	VCC70
Y14	VCC71
Y13	VCC72
Y12	VCC73
Y11	VCC74
Y10	VCC75
Y09	VCC76
Y08	VCC77
Y07	VCC78
Y06	VCC79
Y05	VCC80
Y04	VCC81
Y03	VCC82
Y02	VCC83
Y01	VCC84
Y00	VCC85
Y00	VCC86
Y00	VCC87
Y00	VCC88
Y00	VCC89
Y00	VCC90
Y00	VCC91
Y00	VCC92
Y00	VCC93
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Y00	VCC97
Y00	VCC98
Y00	VCC99
Y00	VCC100

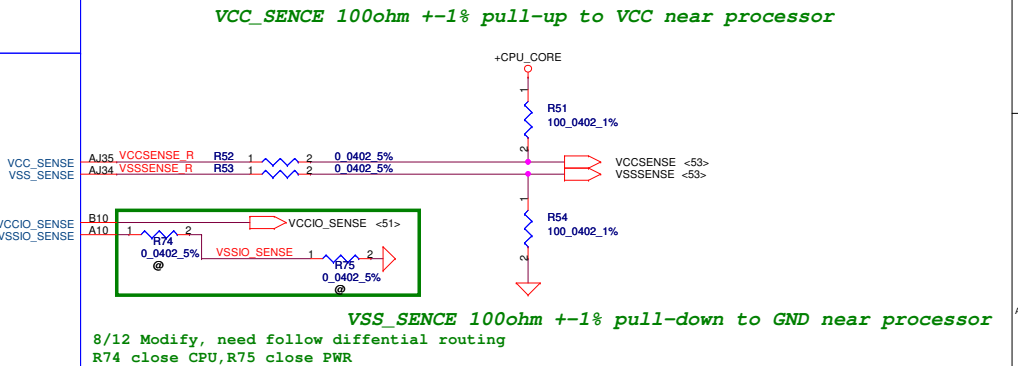
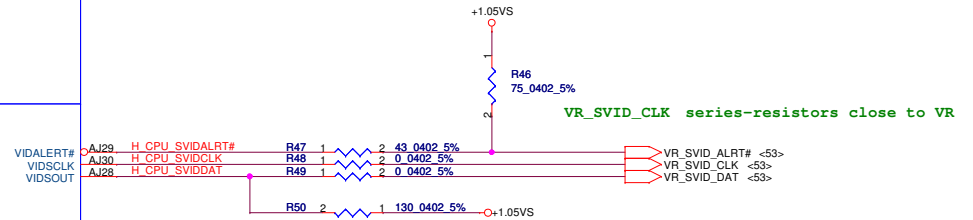
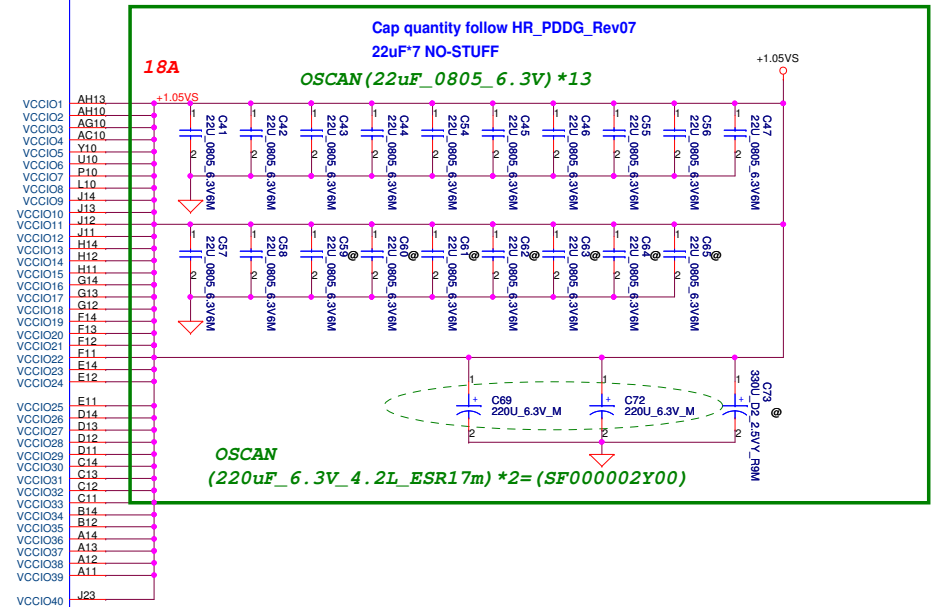
POWER

PEG AND DDR

CORE SUPPLY

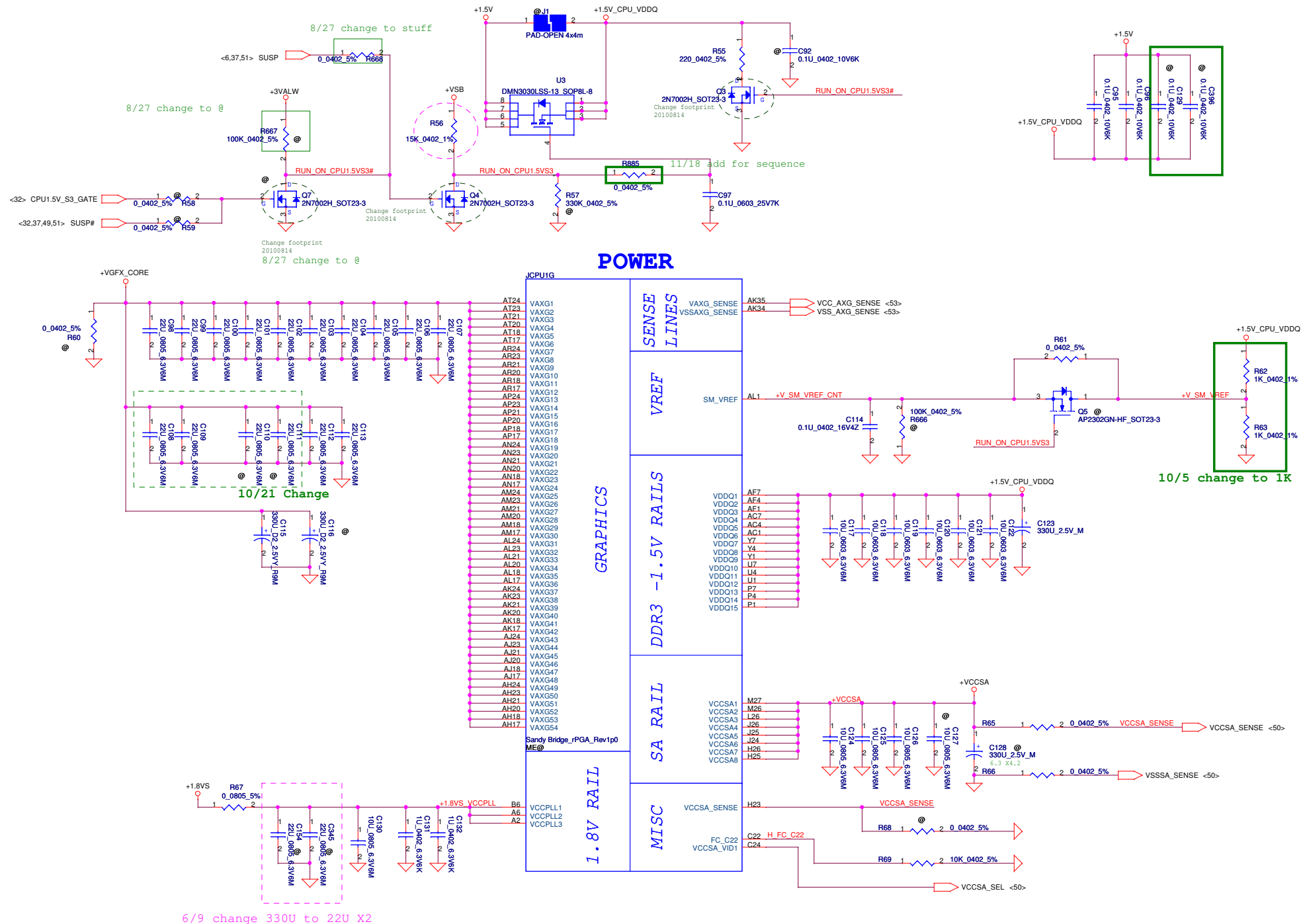
SVID

SENSE LINES

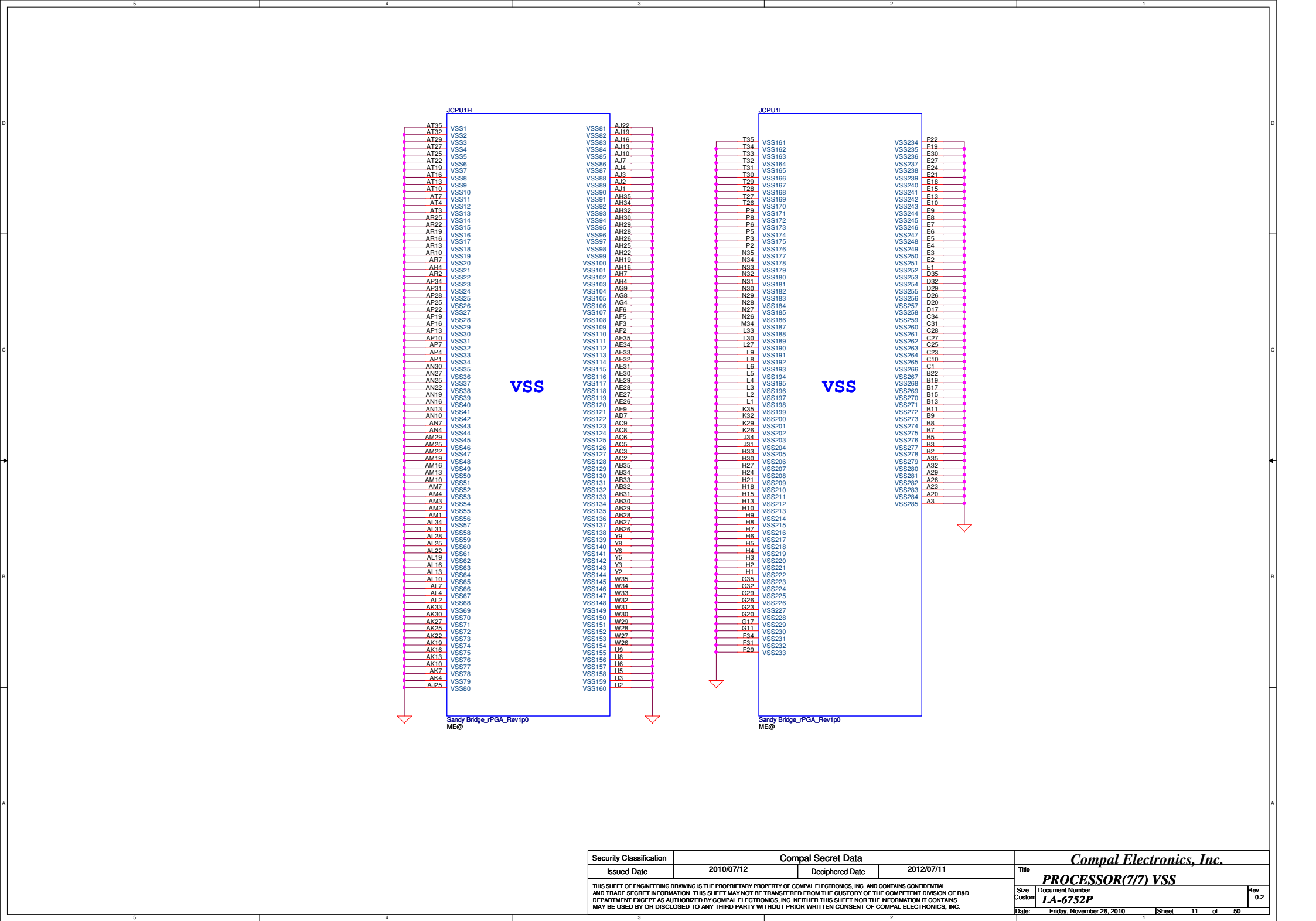


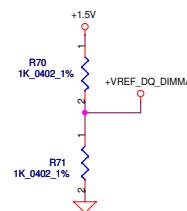
Sandy Bridge_rPGA Rev10A
ME@

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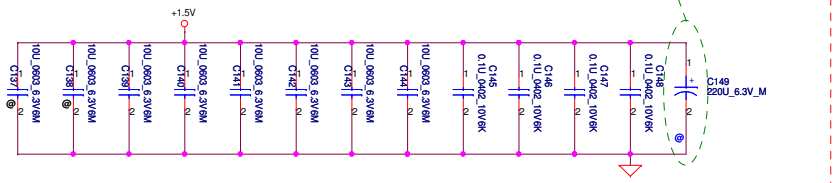


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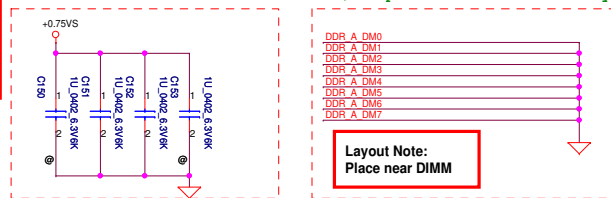




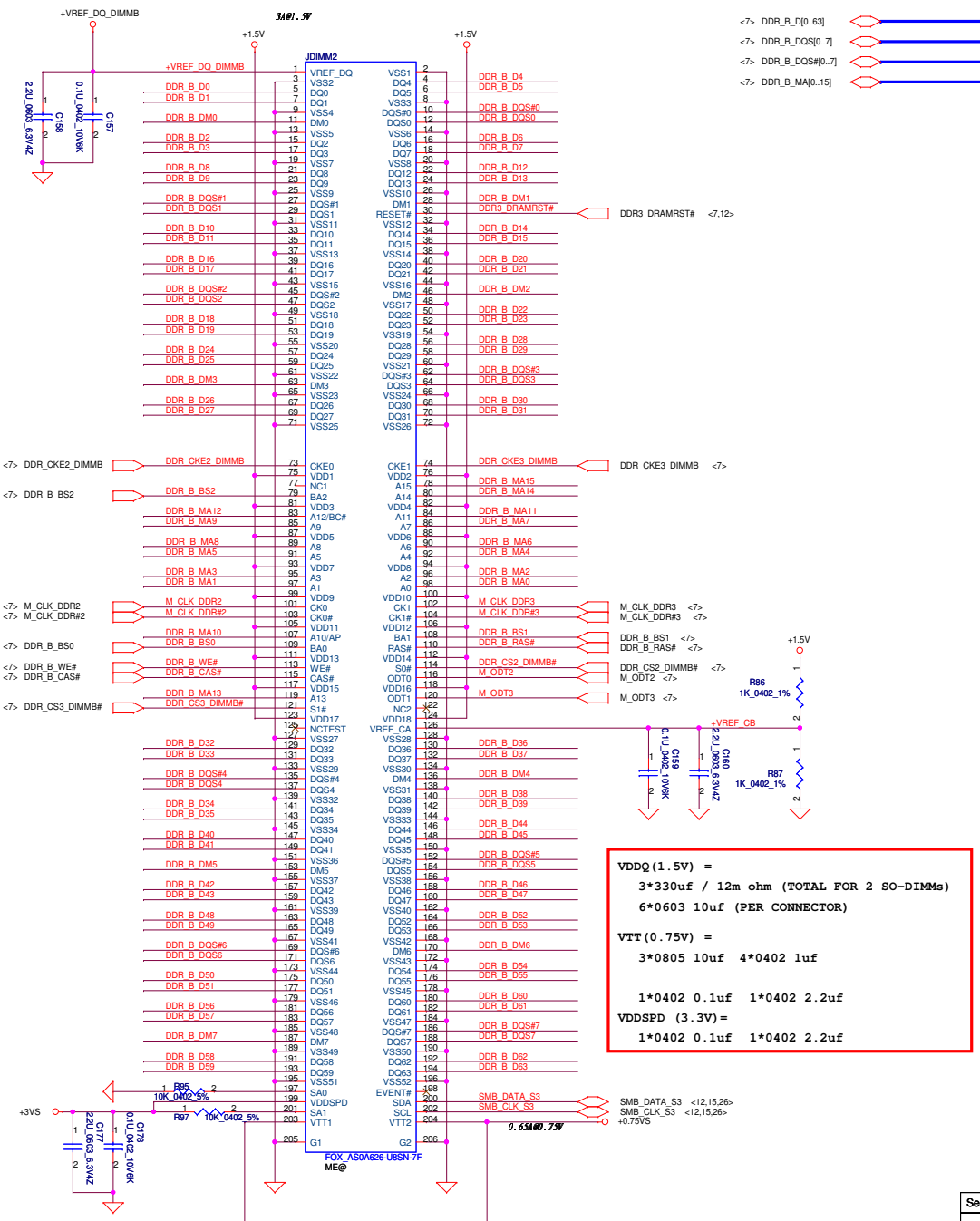
Layout Note:
Place near DIMM



Layout Note:
Place near DIMM



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For Arranale only +VREF_DQ_DIMMB supply from a external 1.5V voltage divide circuit.

07/17/2009

Layout Note:
Place near DIMM

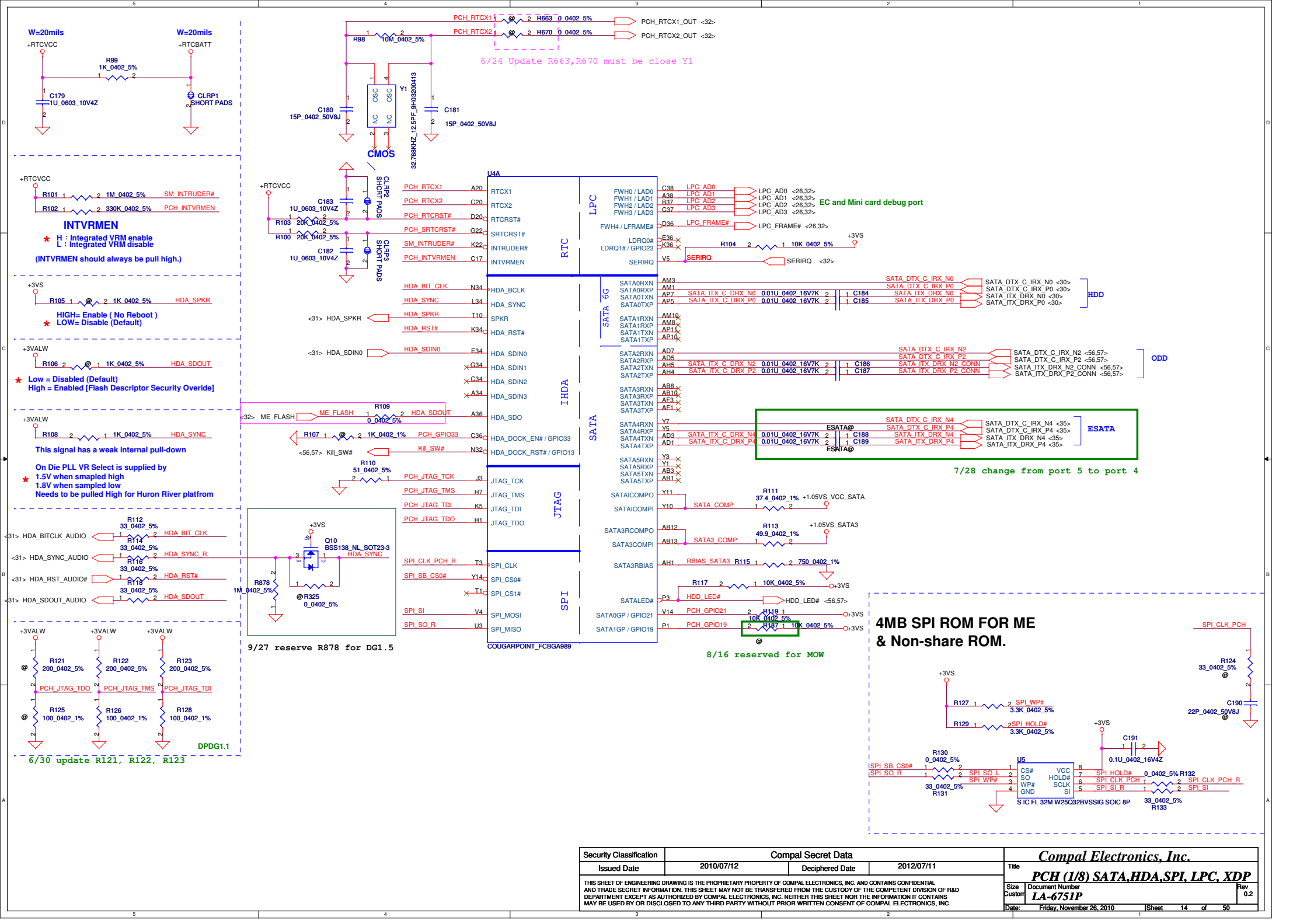
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

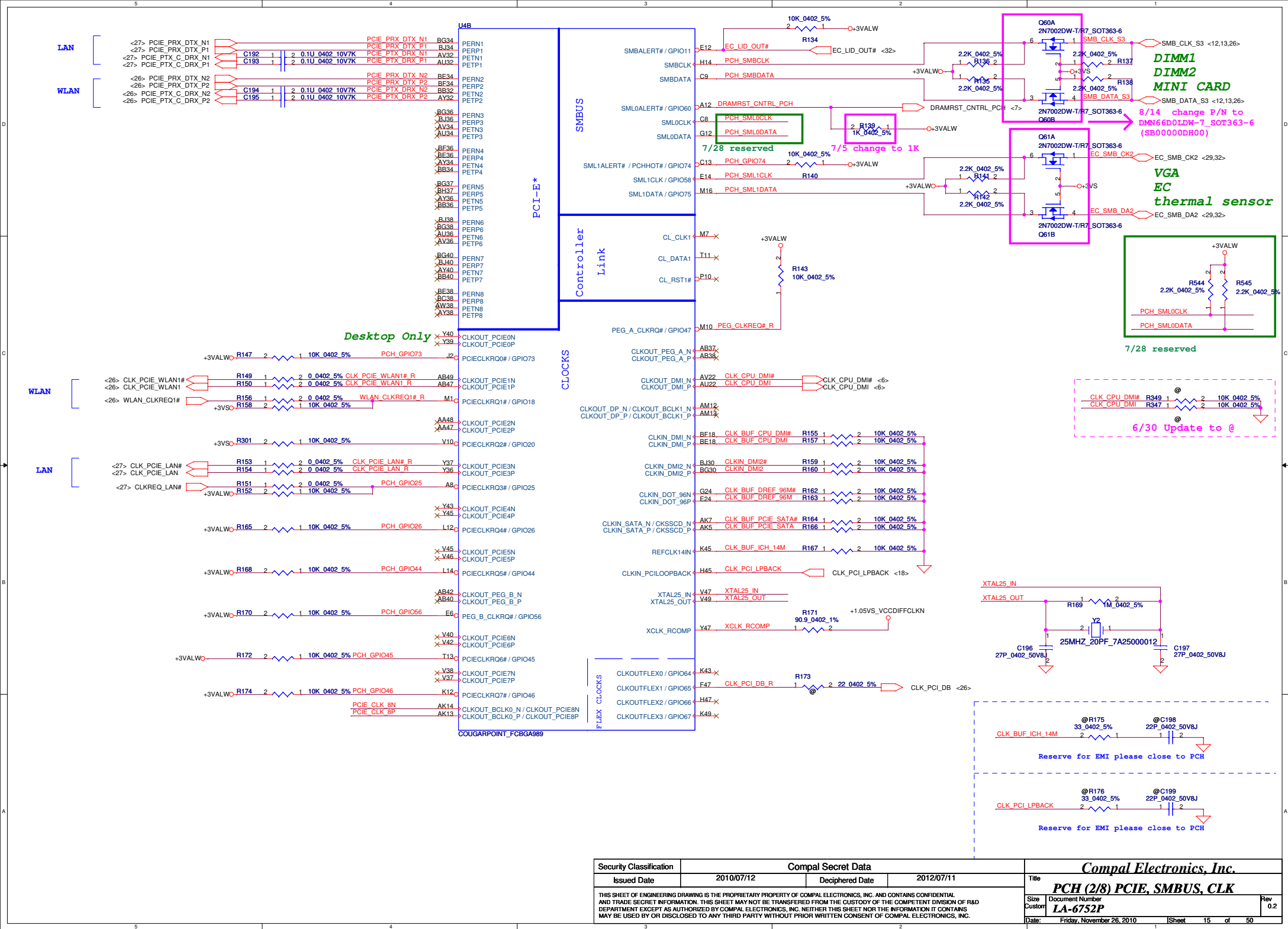
Layout Note:
Place near DIMM

7/28 Update connect GND directly

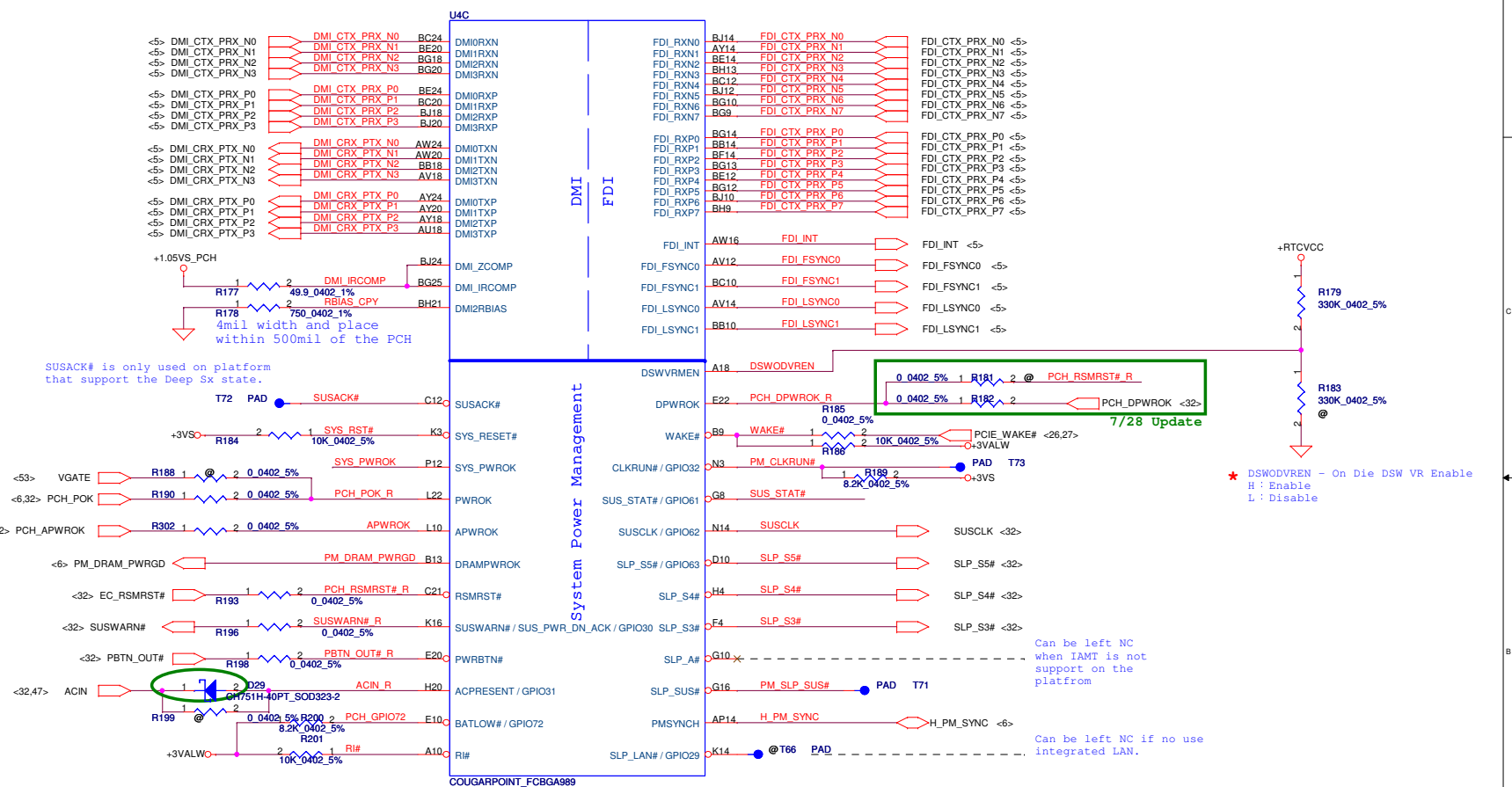
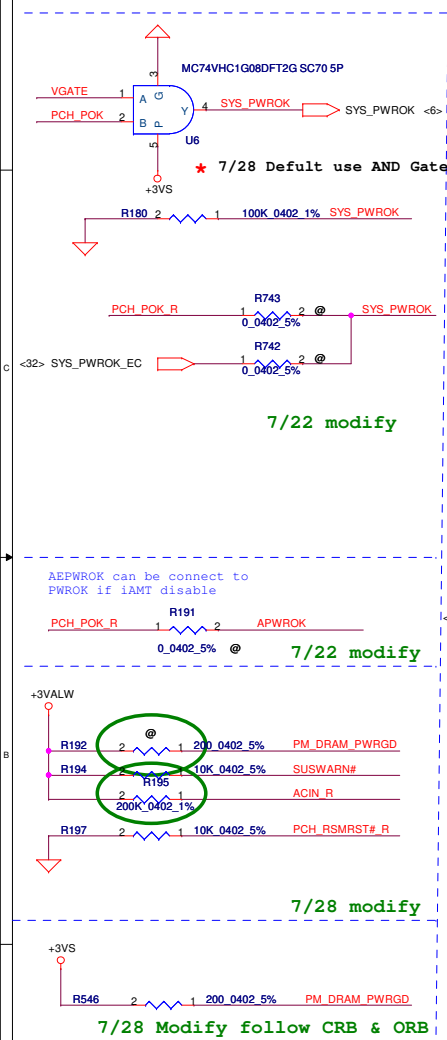
Layout Note:
Place near DIMM

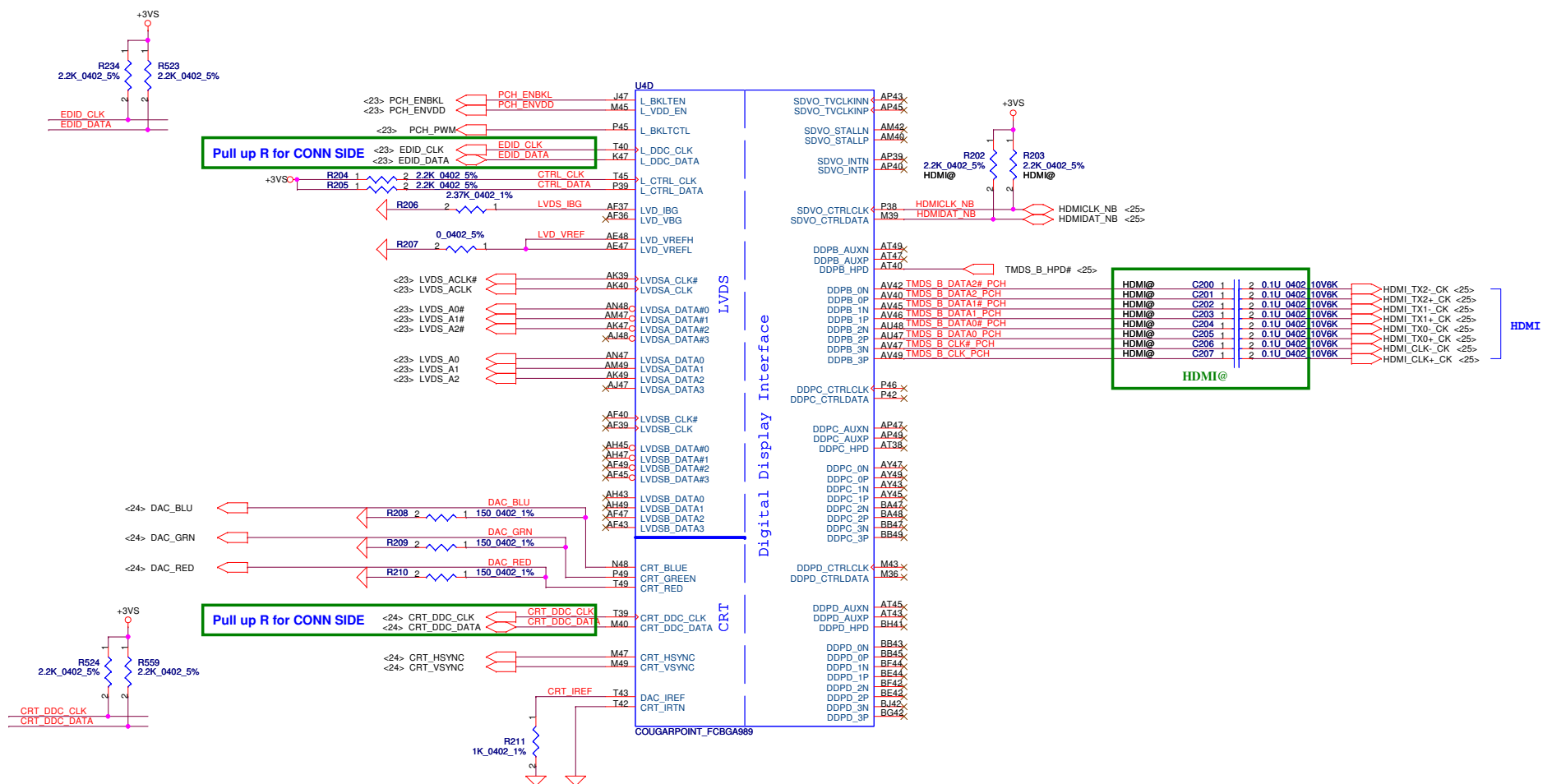
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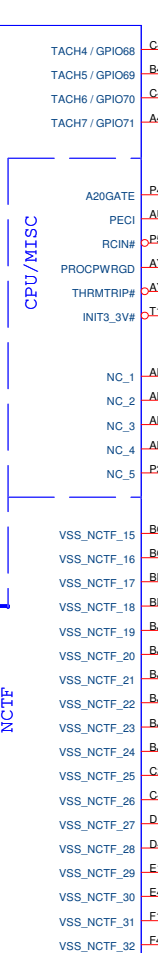
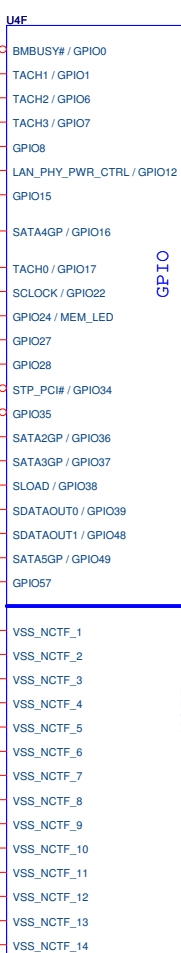
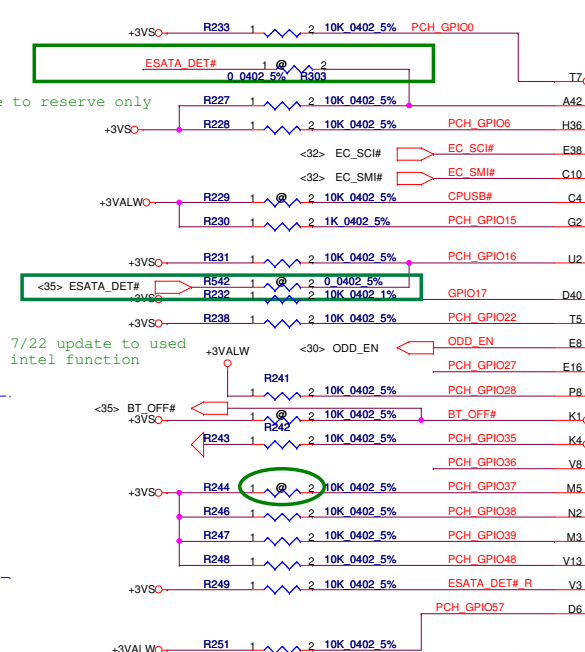
ICC_EN#
Integrated Clock Chip Enable
H ; Disable
★ L ; Enable
7/22 update to reserve only
R235 1 2 1K 0402 5% EC_SMI#
Weak internal pull-high

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable
R240 1 2 1K 0402 5% PCH_GPIO28

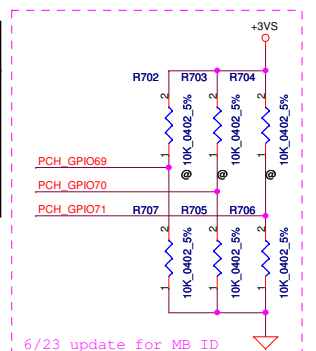
PCH_GPIO27 (Have internal Pull-High)
★ High: VCCVRM VR Enable
Low: VCCVRM VR Disable
R245 1 2 1K 0402 5% PCH_GPIO27

R250 1 2 1K 0402 5% PCH_GPIO36
R547 1 2 1K 0402 5%
8/5 update to pull down

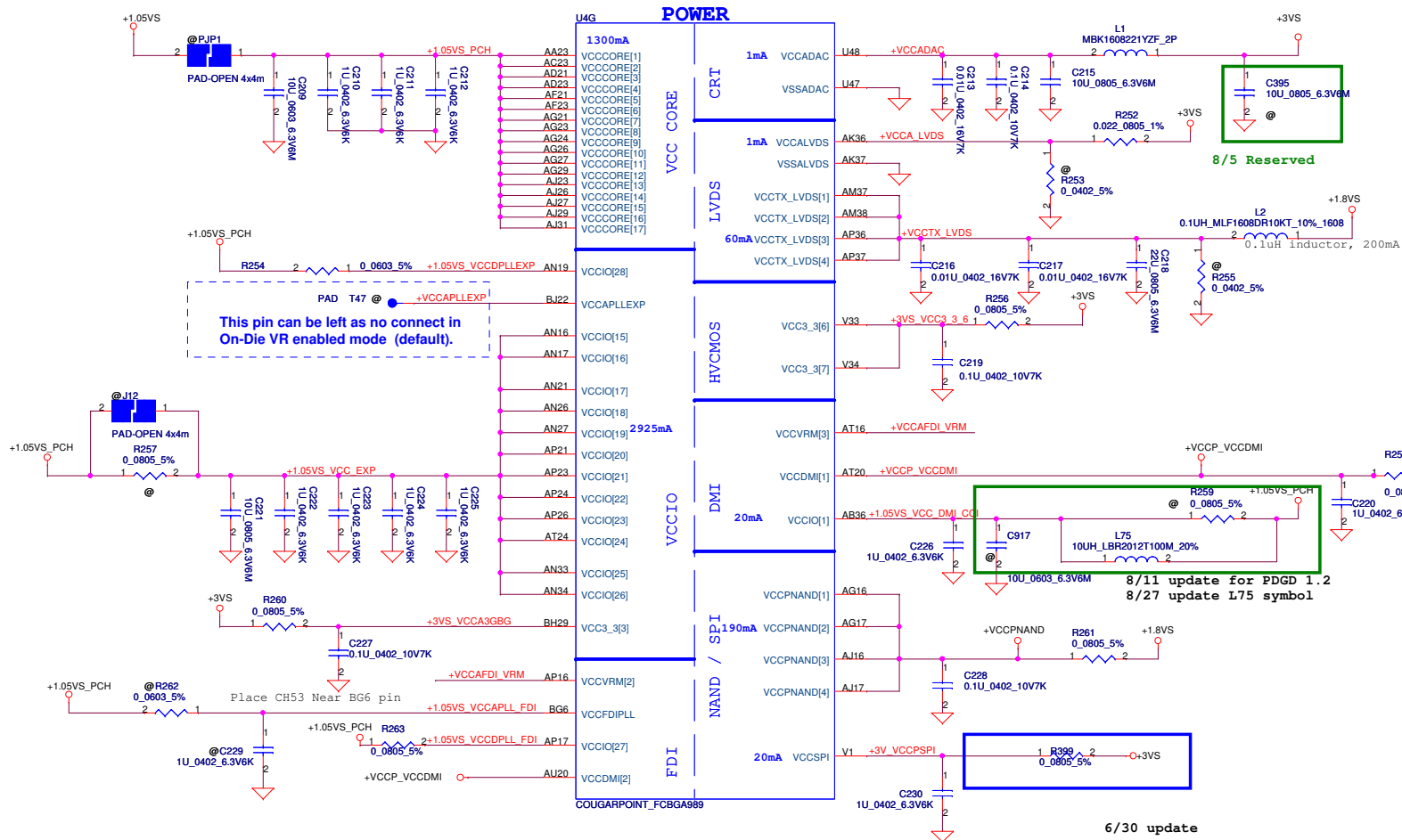
R881 1 2 1K 0402 5% PCH_GPIO37
10/8 update to pull down for checklist Rev1.2



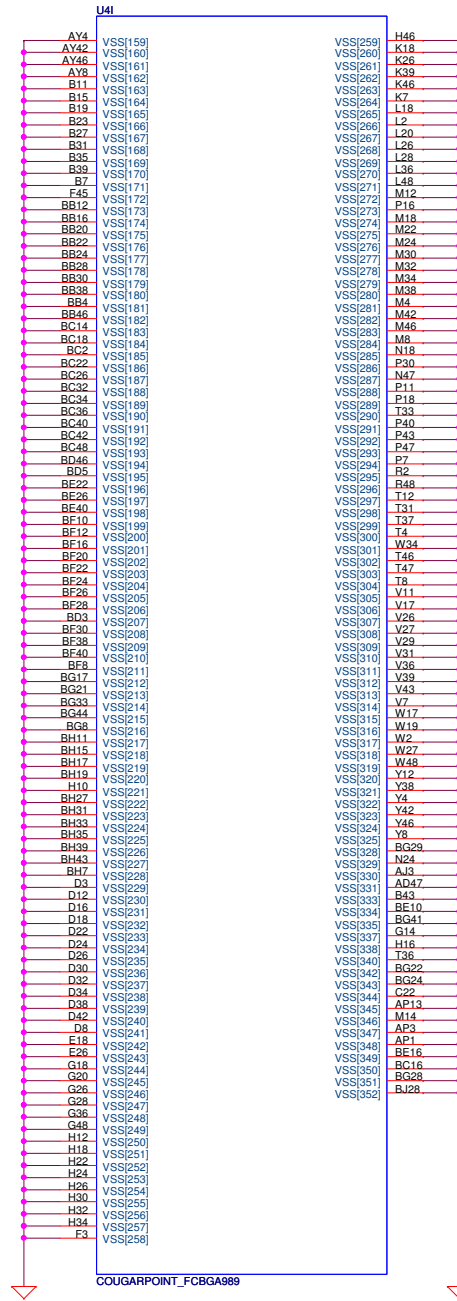
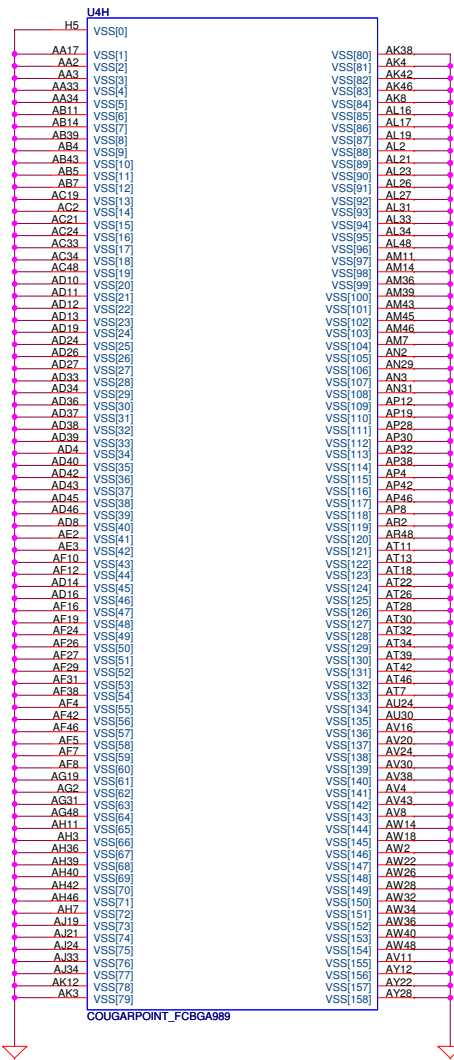
PCH_GPIO69	PCH_GPIO70	PCH_GPIO71	Function
0	0	0	UMA ★
1	0	0	DIS
0	1	0	PX3.0
1	1	0	PX4.0



INIT3_3V
This signal has weak internal PU, can't pull low
Intel schematic review recommend.

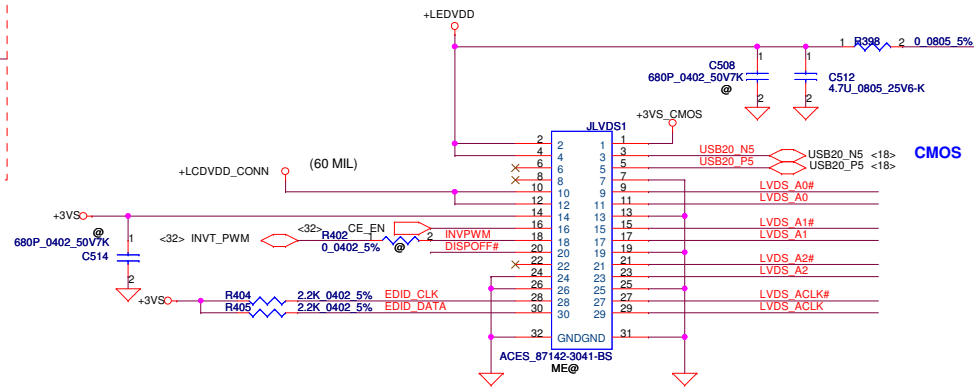
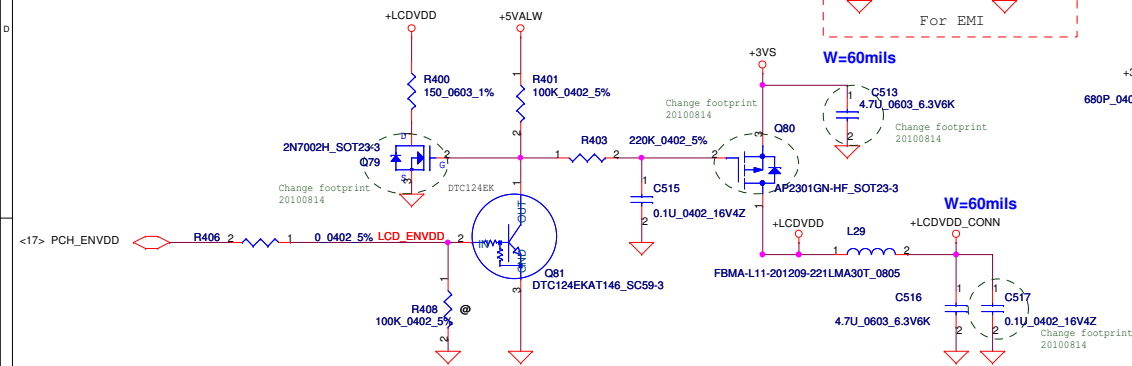


PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

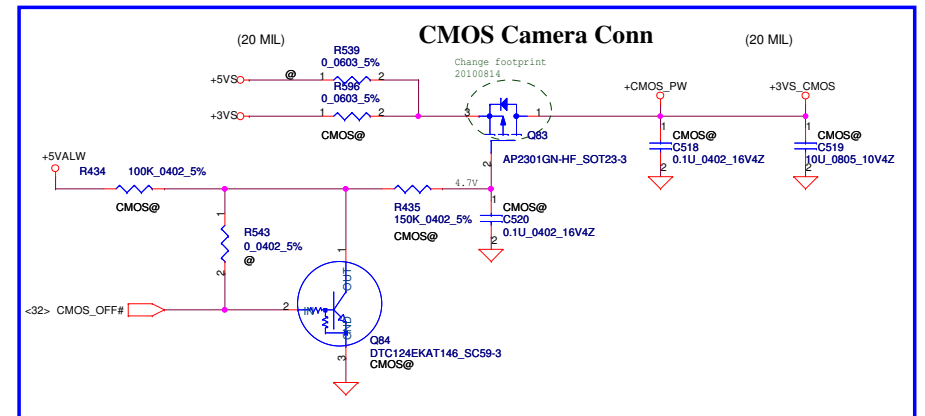
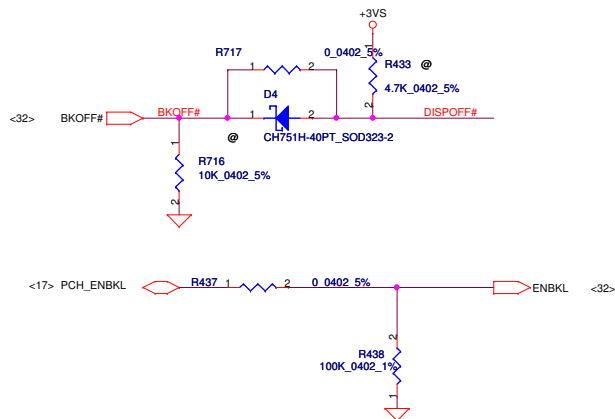
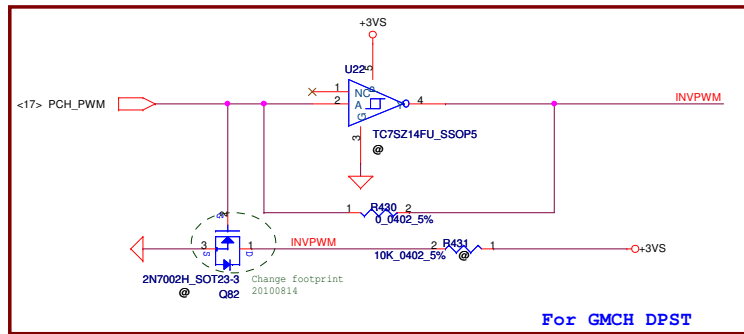


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Size	Custom	Document Number	LA-6752P	Rev	0.2
Date:	Friday, November 26, 2010	Sheet	22	of	50

LCD POWER CIRCUIT



<17> EDID_CLK EDID_CLK
 <17> EDID_DATA EDID_DATA
 <17> LVDS_A0 LVDS_A0#
 <17> LVDS_A1 LVDS_A1#
 <17> LVDS_A2 LVDS_A2#
 <17> LVDS_ACLK LVDS_ACLK#



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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title LVDS/CAMERA		
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				LA-6752P		
				Date:	Friday, November 26, 2010	Sheet 23 of 50

UMA only

<17> DAC_RED
<17> DAC_GRN
<17> DAC_BLU

8/6 Modify,

CLOSE TO CONN

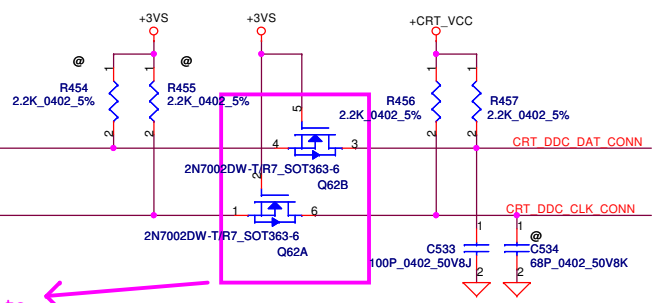
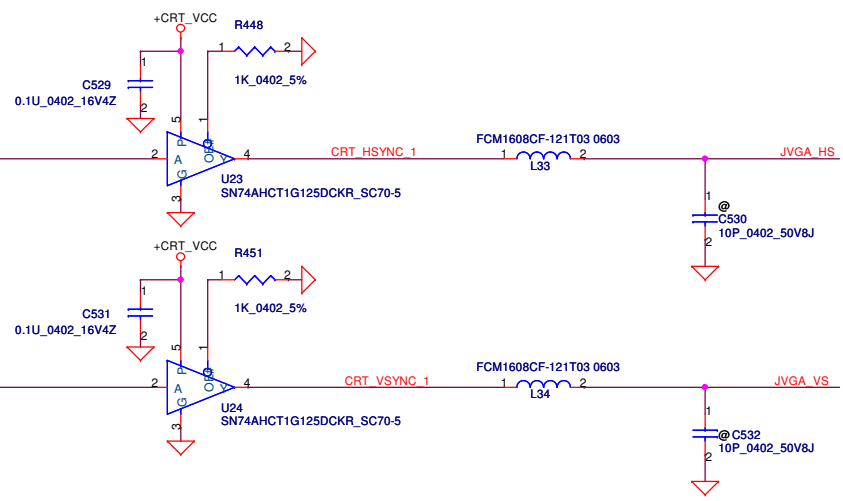
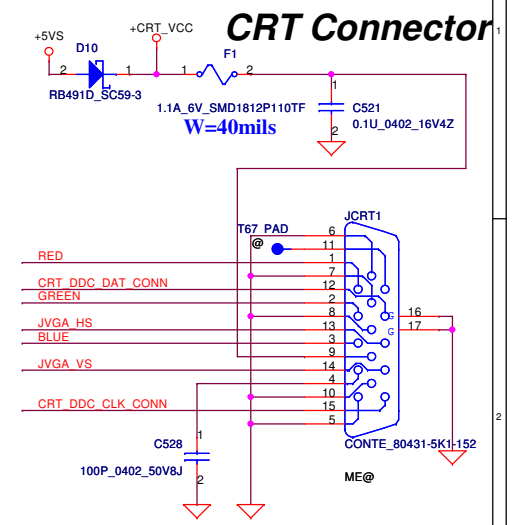
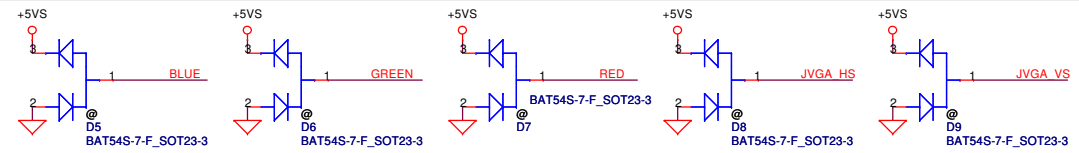
<17> CRT_HSYNC

<17> CRT_VSYNC

<17> CRT_DDC_DATA

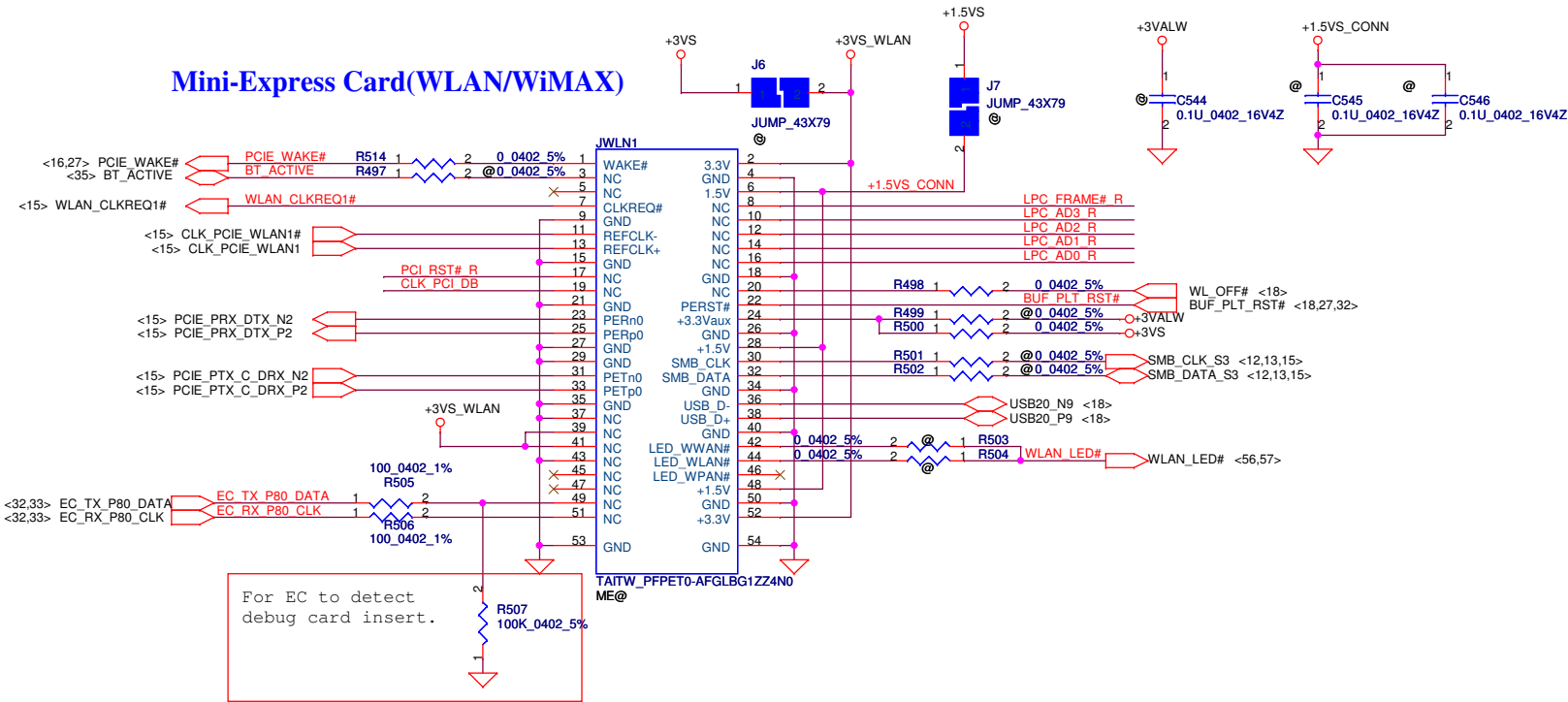
<17> CRT_DDC_CLK

8/14 change P/N to
DMN66D0LDW-7_SOT363-6
(SB00000DH00)



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						Size		Document Number		Rev	
						Custom		LA-6752P		0.2	
						Date:		Friday, November 26, 2010		Sheet 24 of 50	
						C		D			

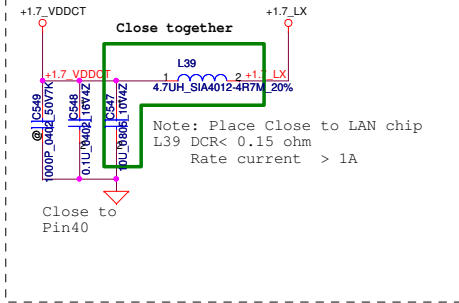
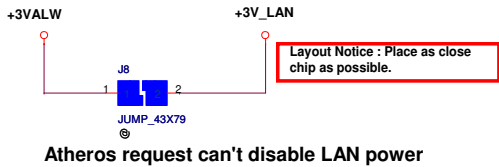
Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R508	1	2	0.0402 5%	LPC_FRAME#	LPC_FRAME# <14,32>
LPC_AD3 R	R509	1	2	0.0402 5%	LPC_AD3	LPC_AD3 <14,32>
LPC_AD2 R	R510	1	2	0.0402 5%	LPC_AD2	LPC_AD2 <14,32>
LPC_AD1 R	R511	1	2	0.0402 5%	LPC_AD1	LPC_AD1 <14,32>
LPC_AD0 R	R512	1	2	0.0402 5%	LPC_AD0	LPC_AD0 <14,32>
PCI_RST# R	R513	1	2	0.0402 5%	PCI_RST#	PCI_RST# <14,32>
CLK_PCIE_DB					CLK_PCIE_DB	CLK_PCIE_DB <15>

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				Size	Document Number
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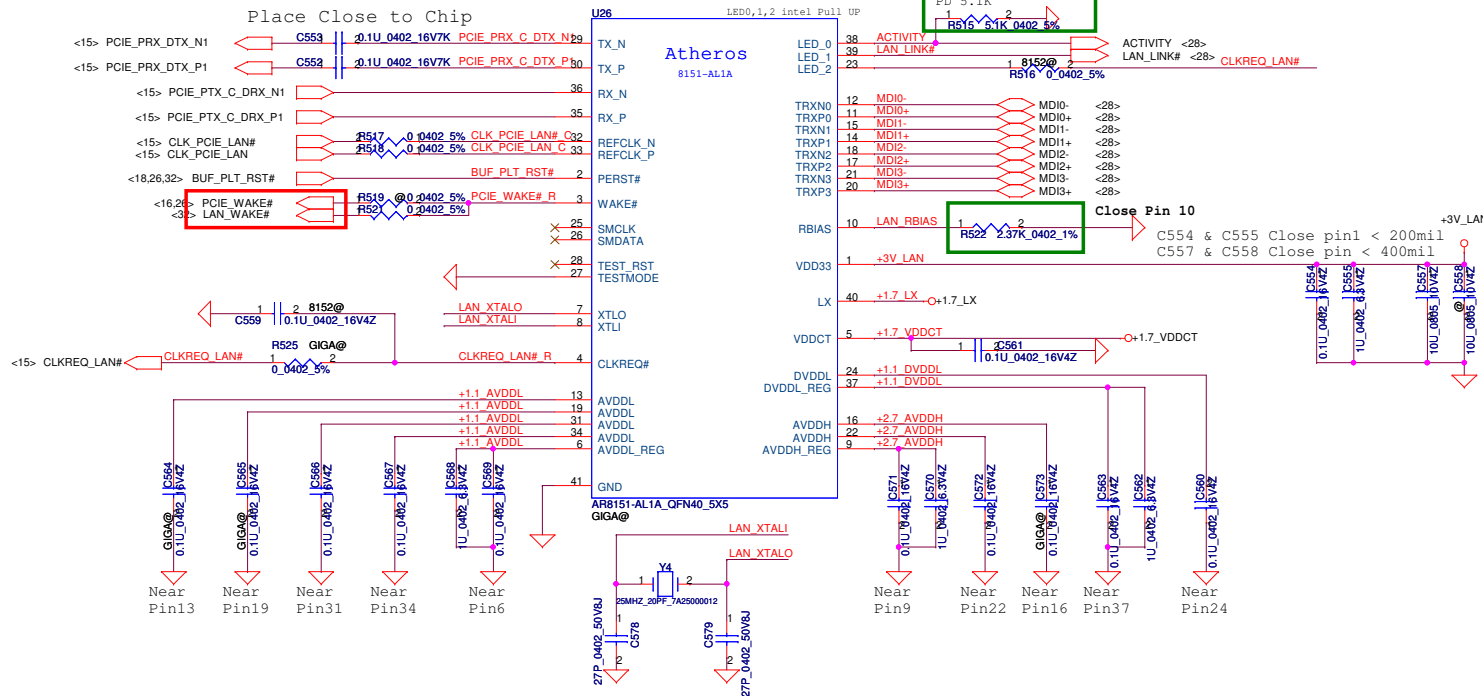


Power On strapping

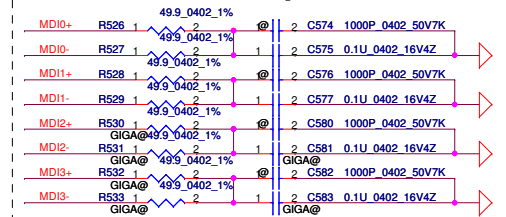
Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED2	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--



S IC AR8152-AL1E QFN 40P E-LAN CTRL

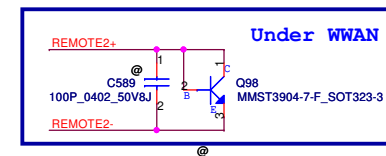
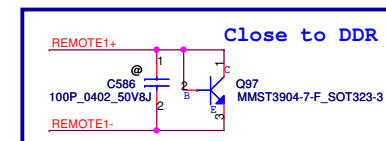
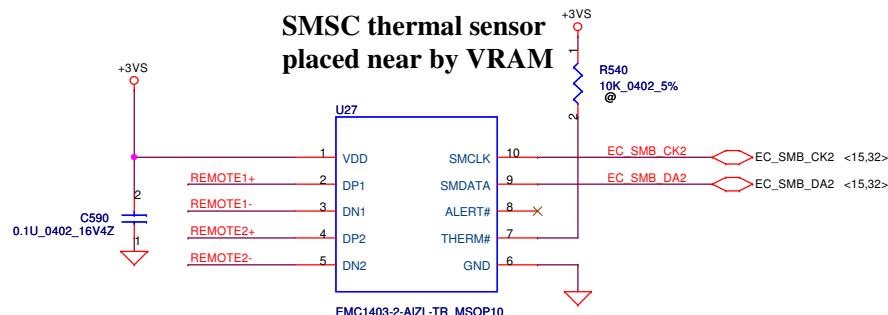
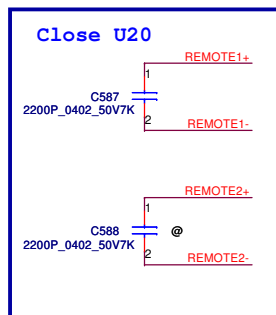


Place Close to LAN chip

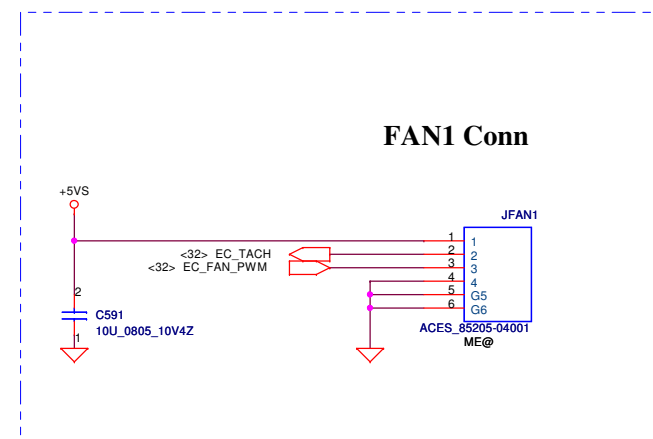


	Pin4	Configure		Pin23	Configure
AR8152	VDDCT_REG	R525	C559 *	CLKREQn	R516 *
AR8151	CLKREQn	*		LED [2]	

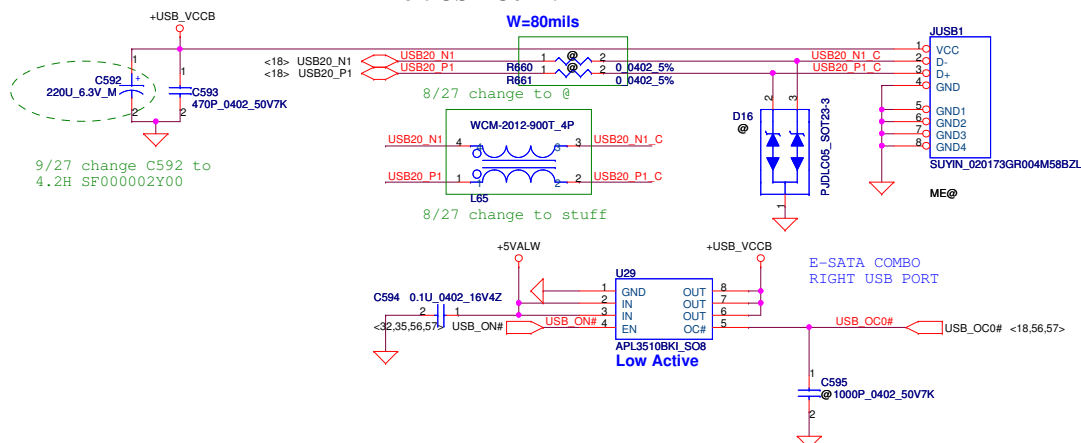
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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	LAN-AR8151/8152
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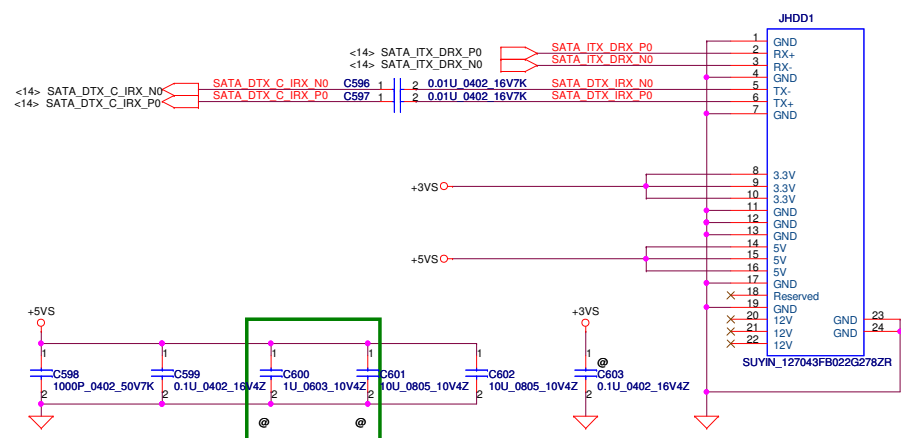
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



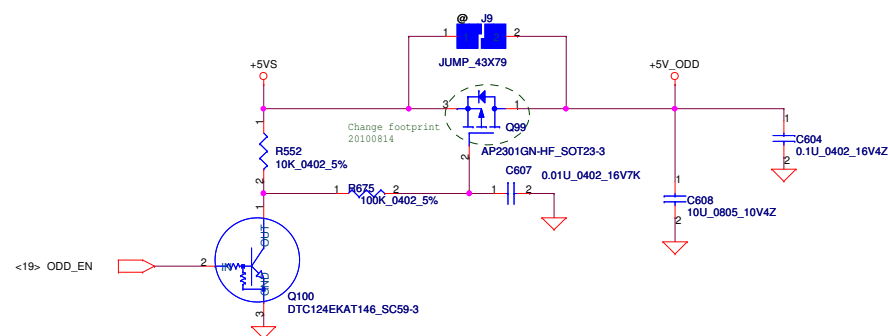
Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
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Left USB Conn.

SATA HDD Conn.

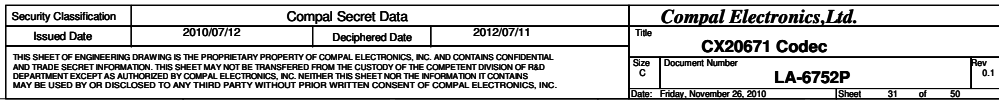
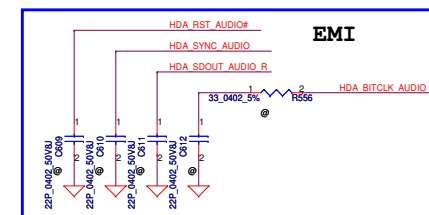


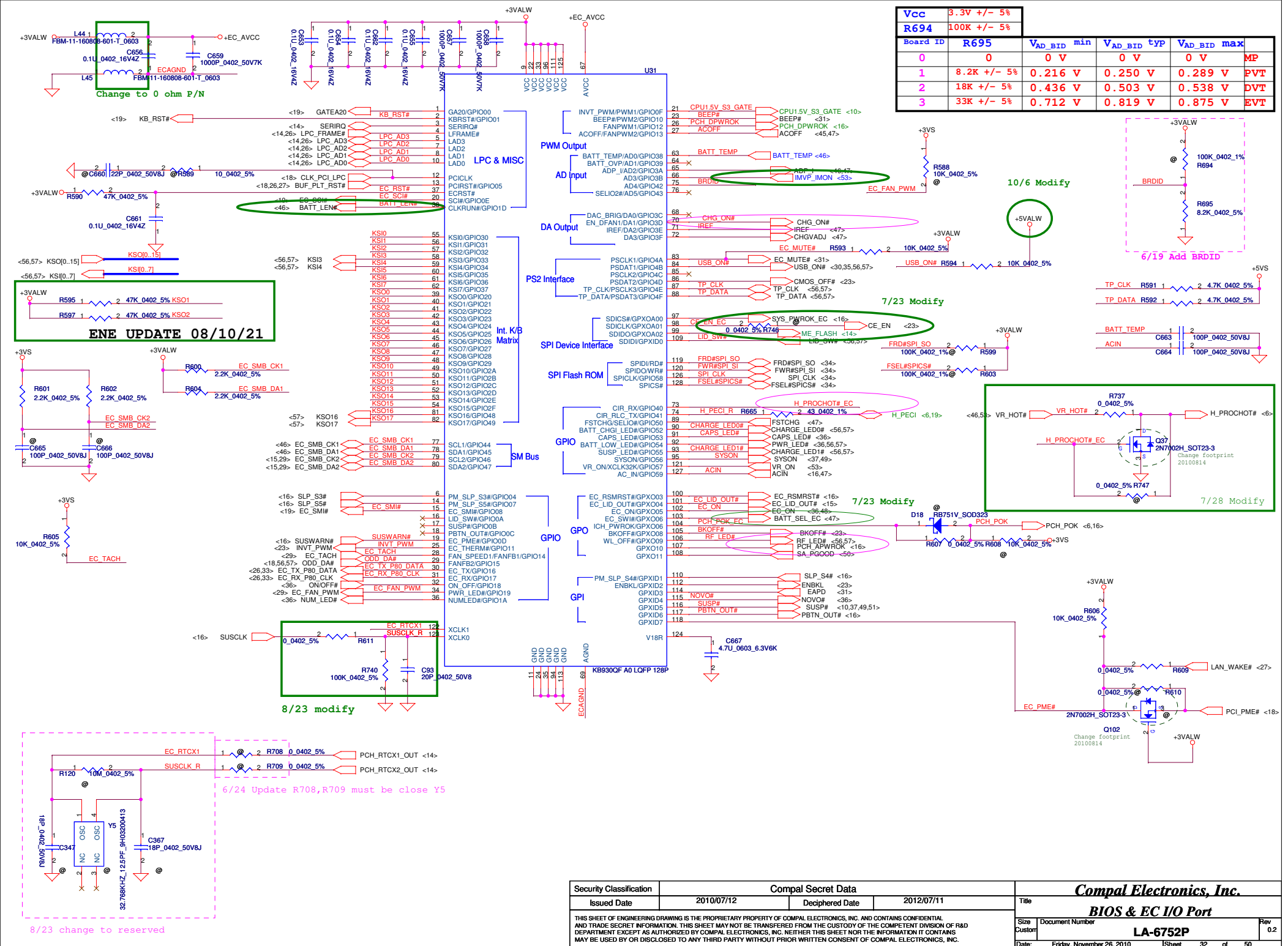
ODD Power Control



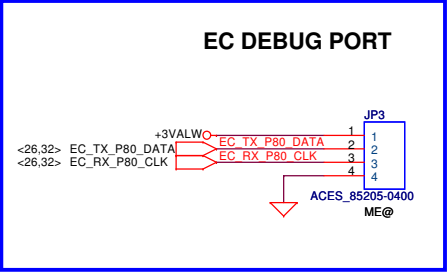
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9/27 Update U30 P/N to SA00003K410



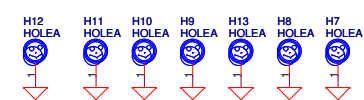
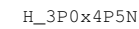
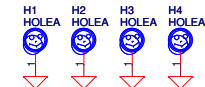
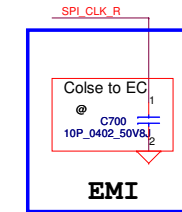
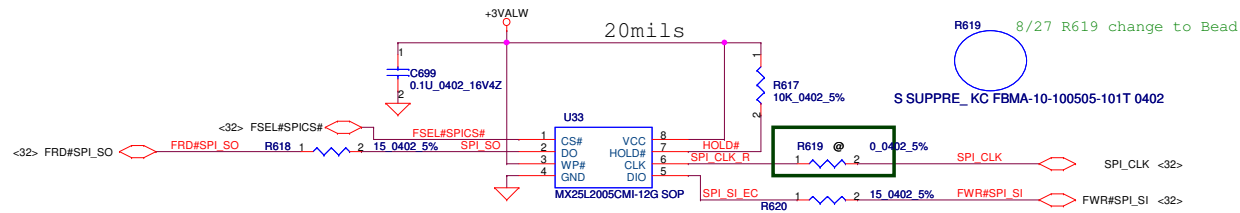


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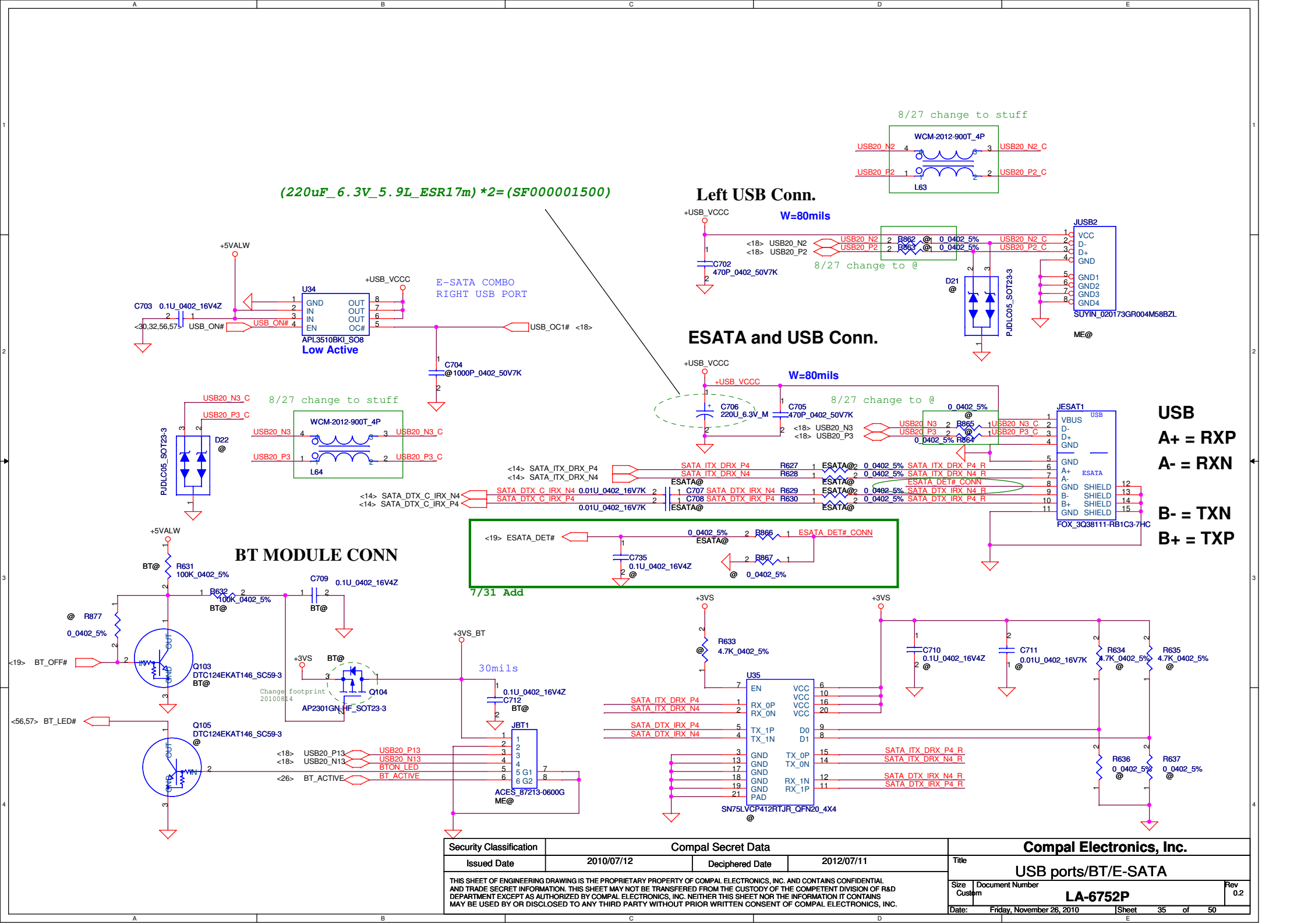


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**FOR EC 128KB SPI ROM
(150mil PACKAGE)
SA00003FL10
SA00003JD00**



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(220uF_6.3V_5.9L_ESR17m)*2=(SF000001500)

Left USB Conn.

+USB_VCC W=80mils

ESATA and USB Conn.

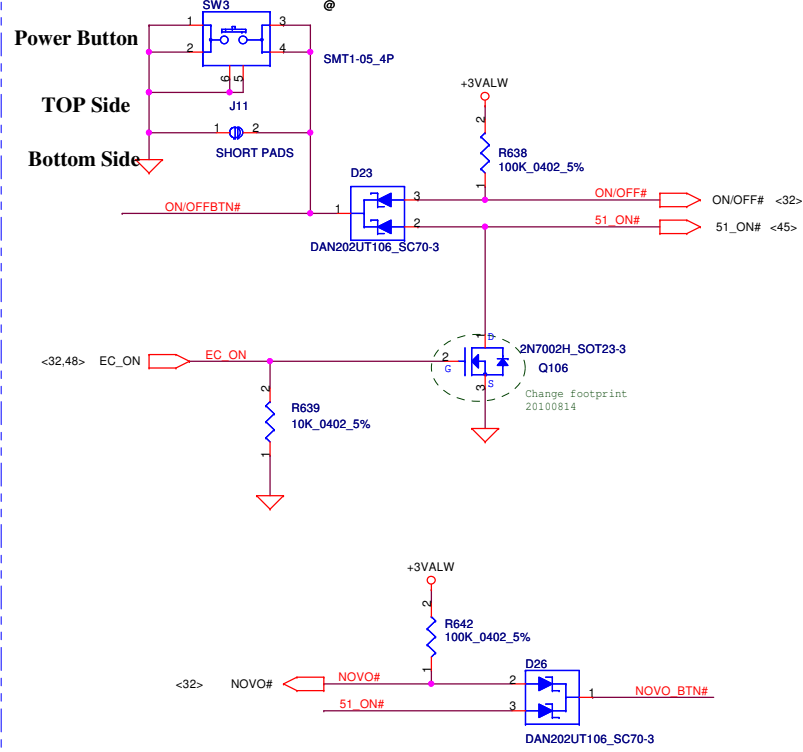
+USB_VCC W=80mils

BT MODULE CONN

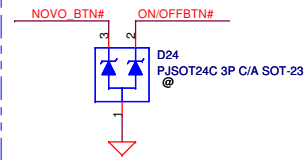
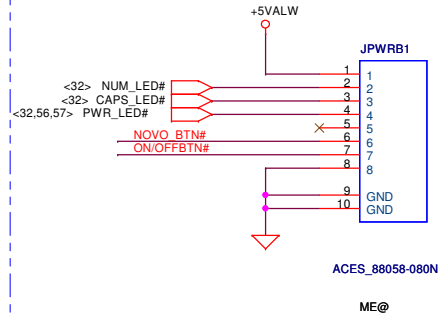
USB
A+ = RXP
A- = RXN
B- = TXN
B+ = TXP

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								Size	Document Number			Rev			
								Custom	LA-6752P			0.2			
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ON/OFF switch

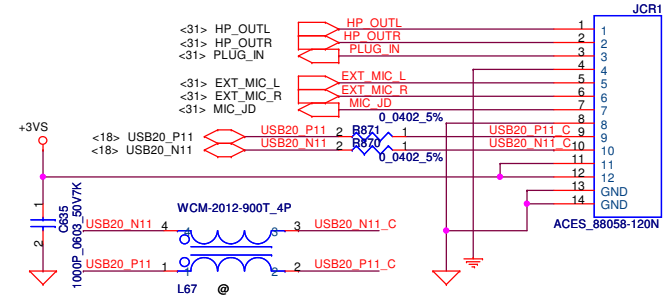


Power Bottom Board Conn. 8pin

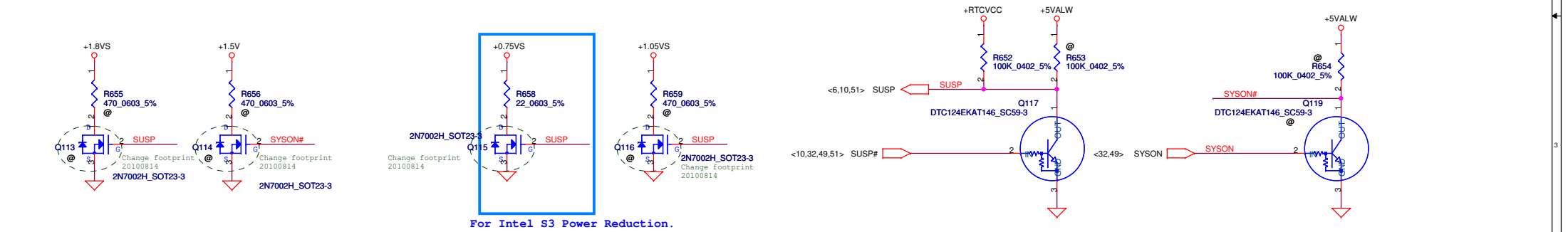
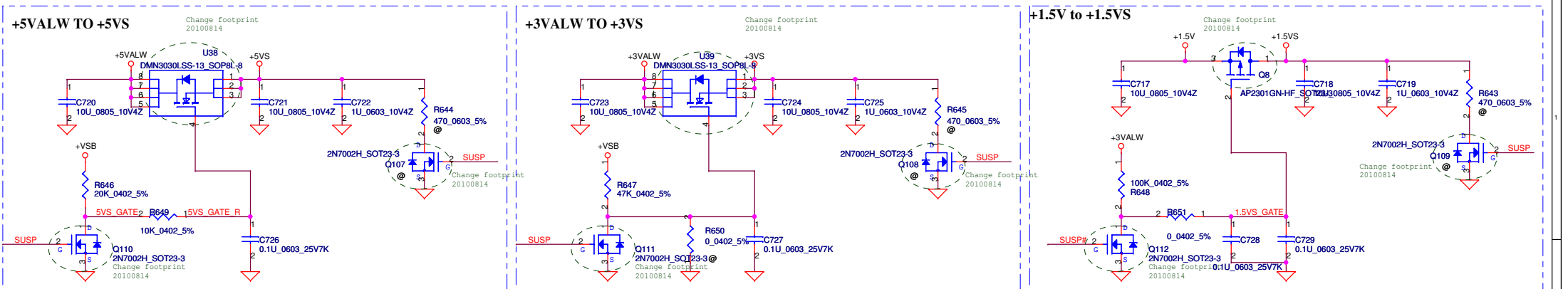


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

Card Reader/Audio Jack SB CONN

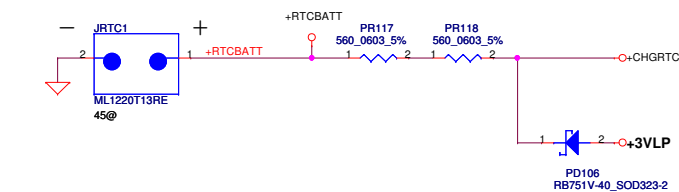
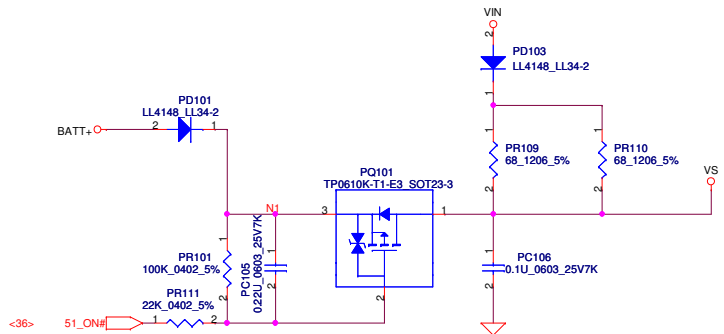
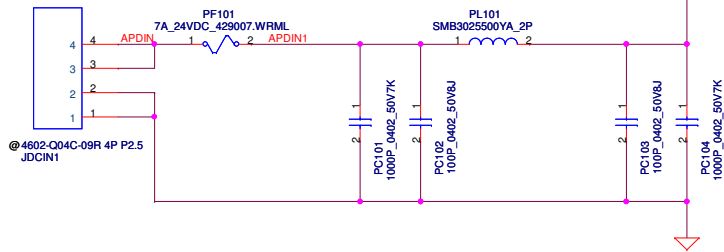


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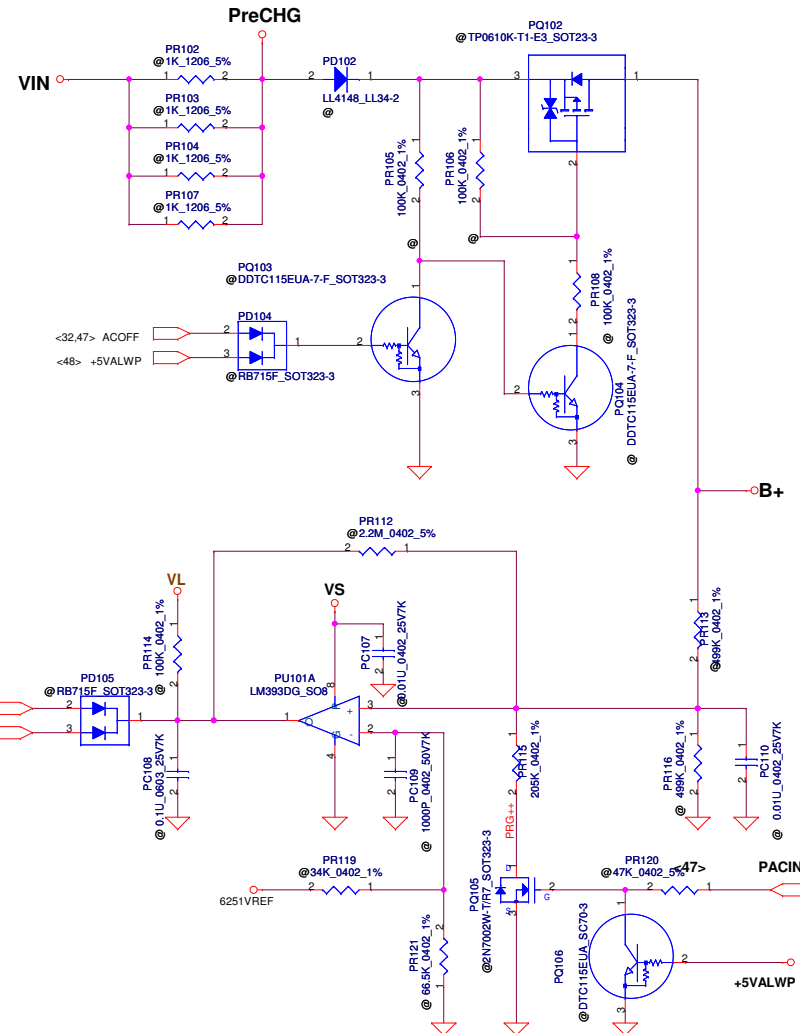


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						Date:	Friday, November 26, 2010	Sheet	37 of 50
						C	D	E	F

DC030006J00



Precharge detector 15.97V/14.84V FOR ADAPTOR



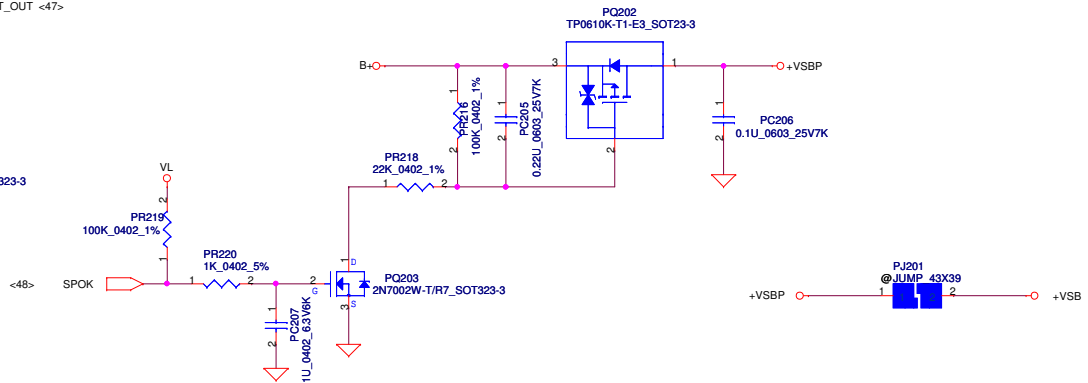
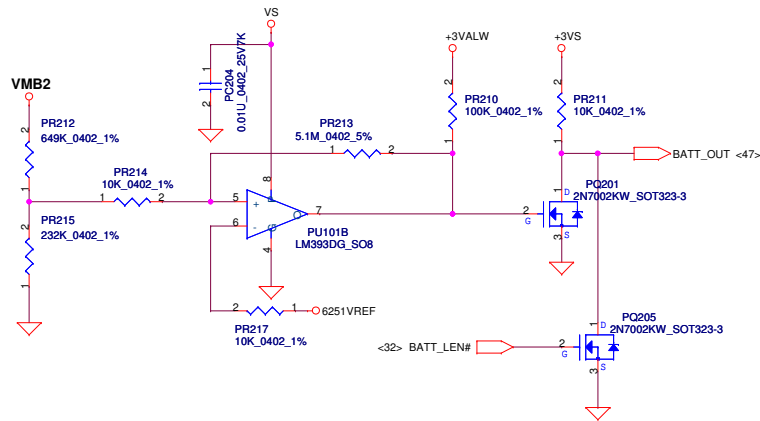
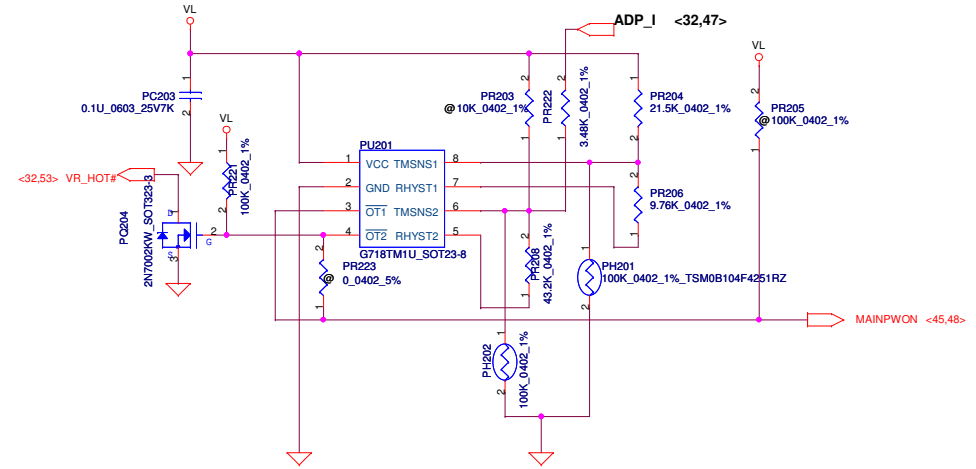
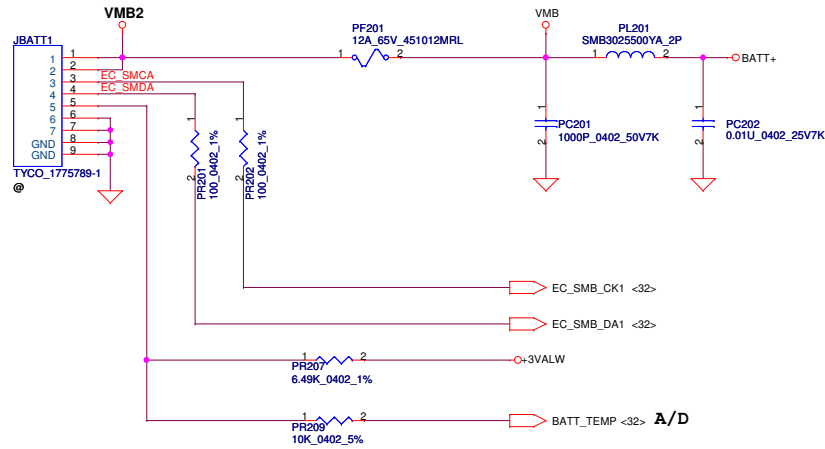
ACIN

Precharge detector		
Min.	typ.	Max.
L-->H	14.991V	15.381V
H-->L	13.860V	14.247V

BATT ONLY

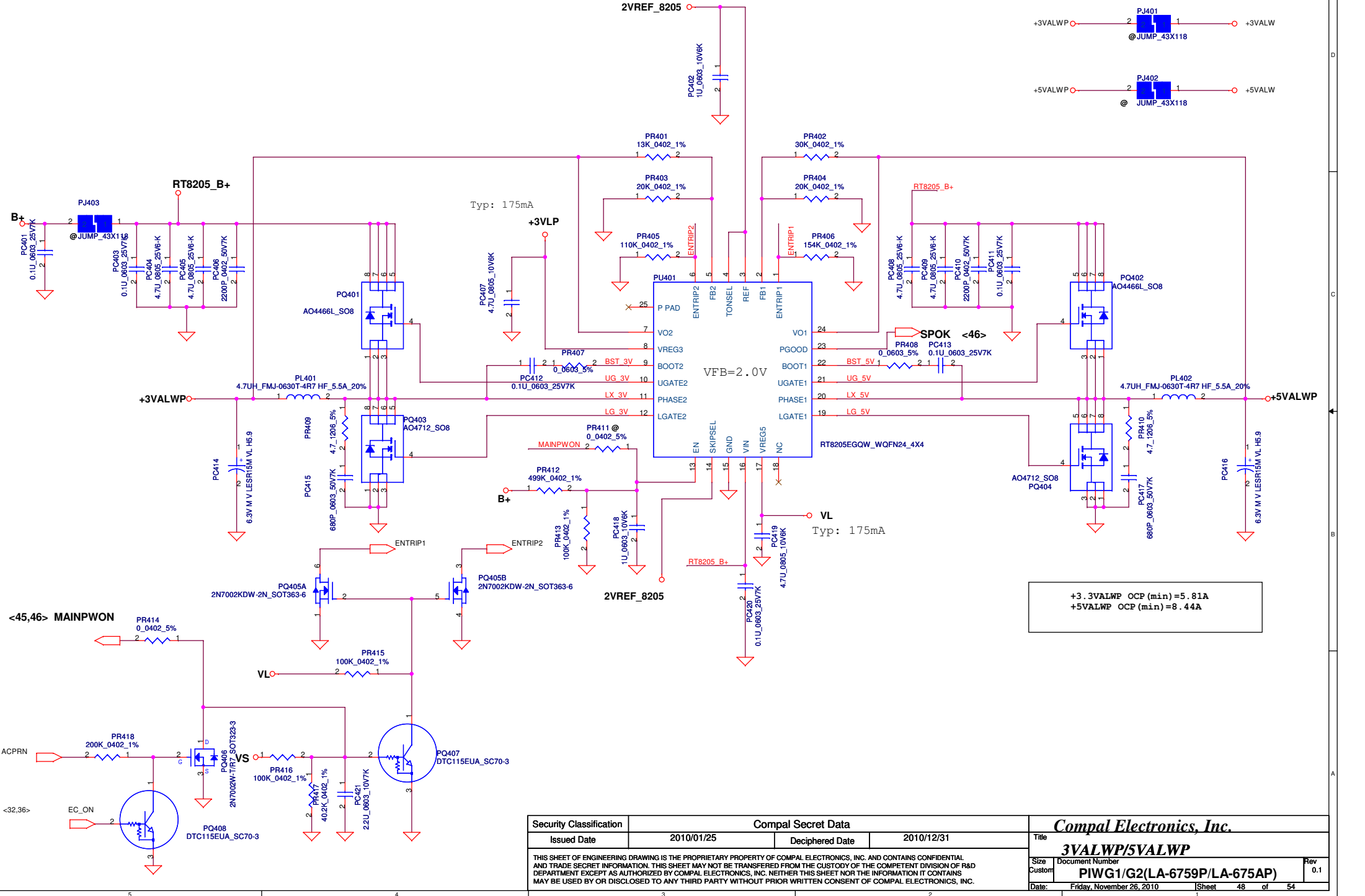
Precharge detector		
Min.	typ.	Max.
L-->H	7.196V	7.349V
H-->L	6.138V	6.214V

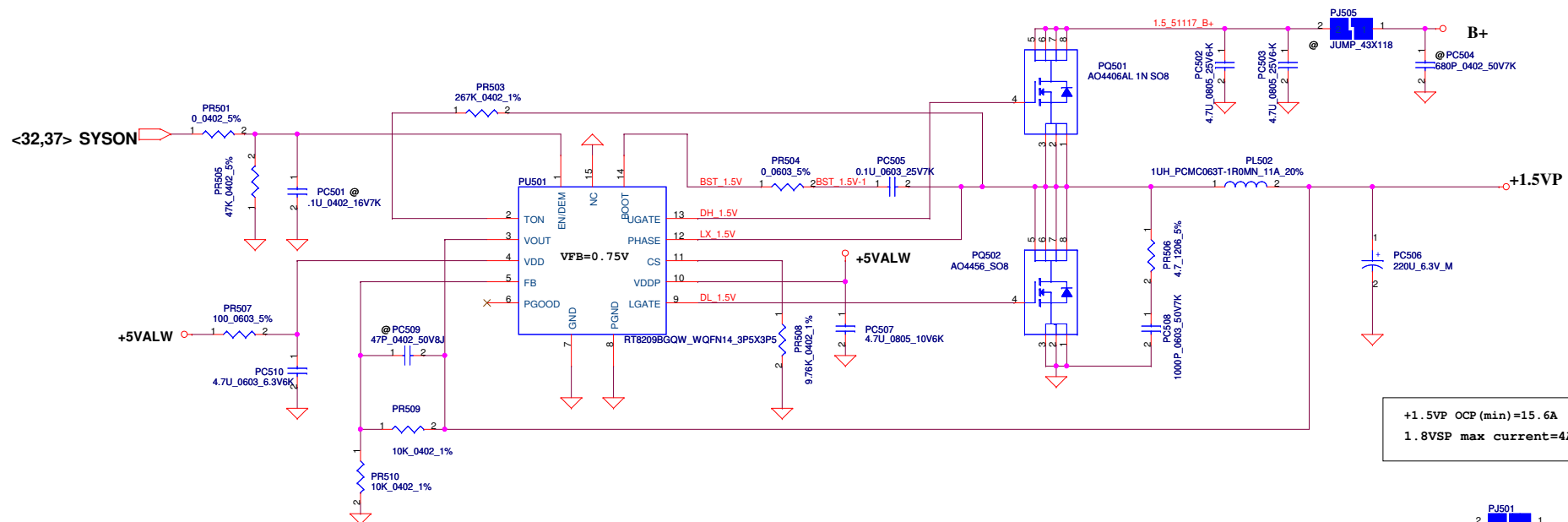
PH201 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



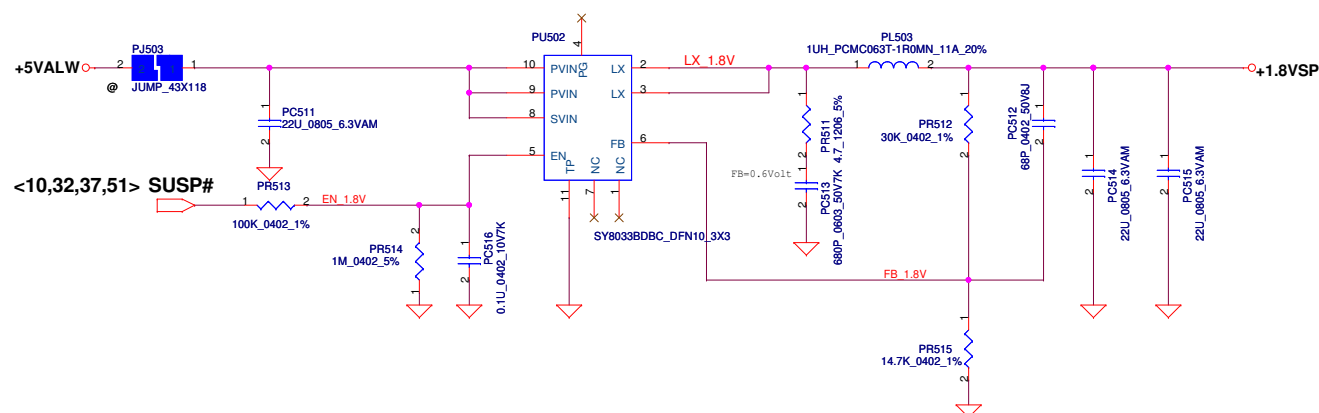
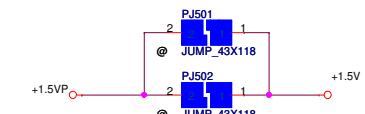
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	PWR-BATTERY CONN/OTP
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				Custom	0.1
				Date	Friday, November 26, 2010
				Sheet	46 of 54

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO





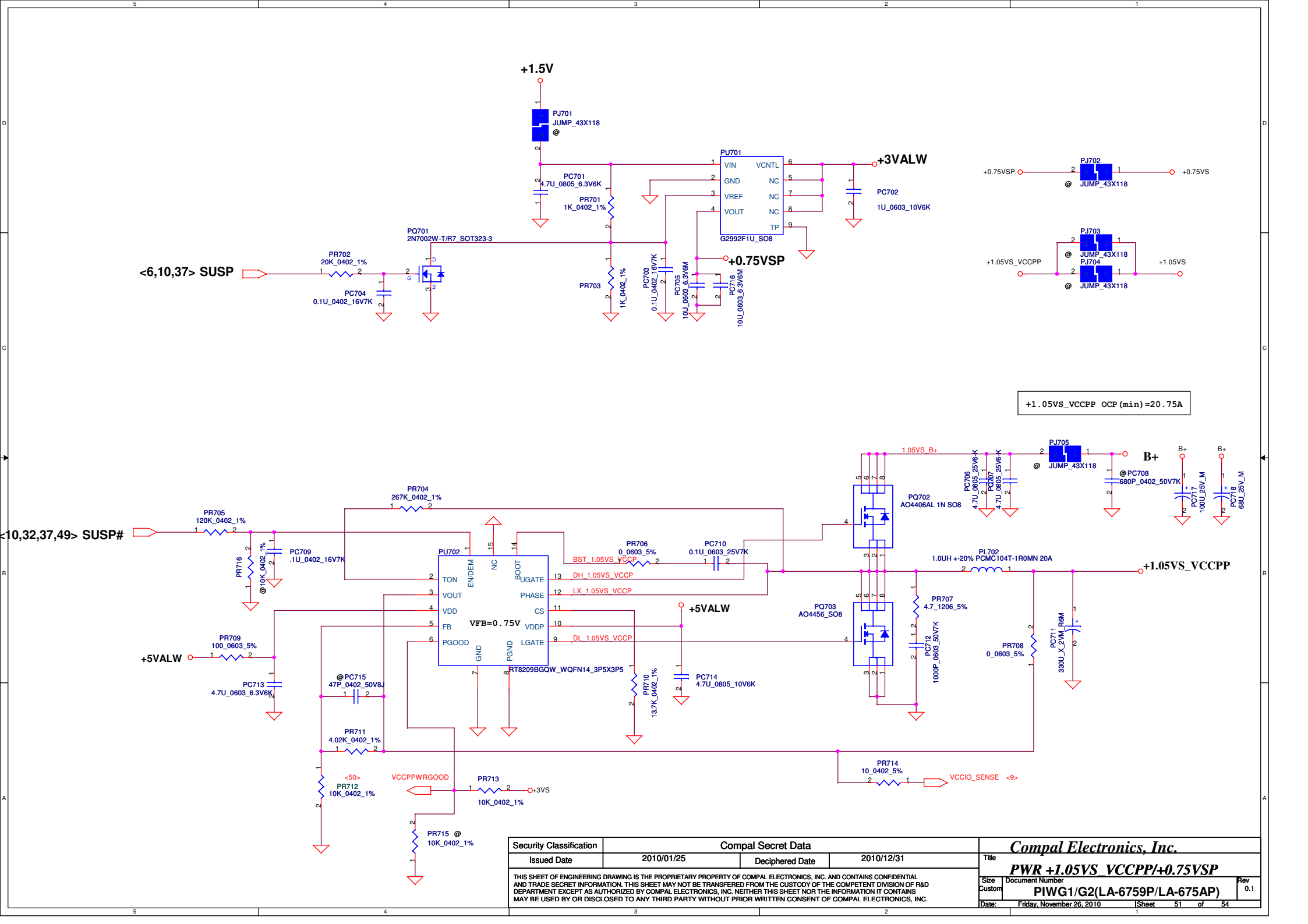
+1.5VP OCP (min)=15.6A
1.8VSP max current=4A



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Size		Document Number		Rev	
Custom		PIWG1/G2(LA-6759P/LA-675AP)		0.1	
Date:		Friday, November 26, 2010		Sheet 49 of 54	

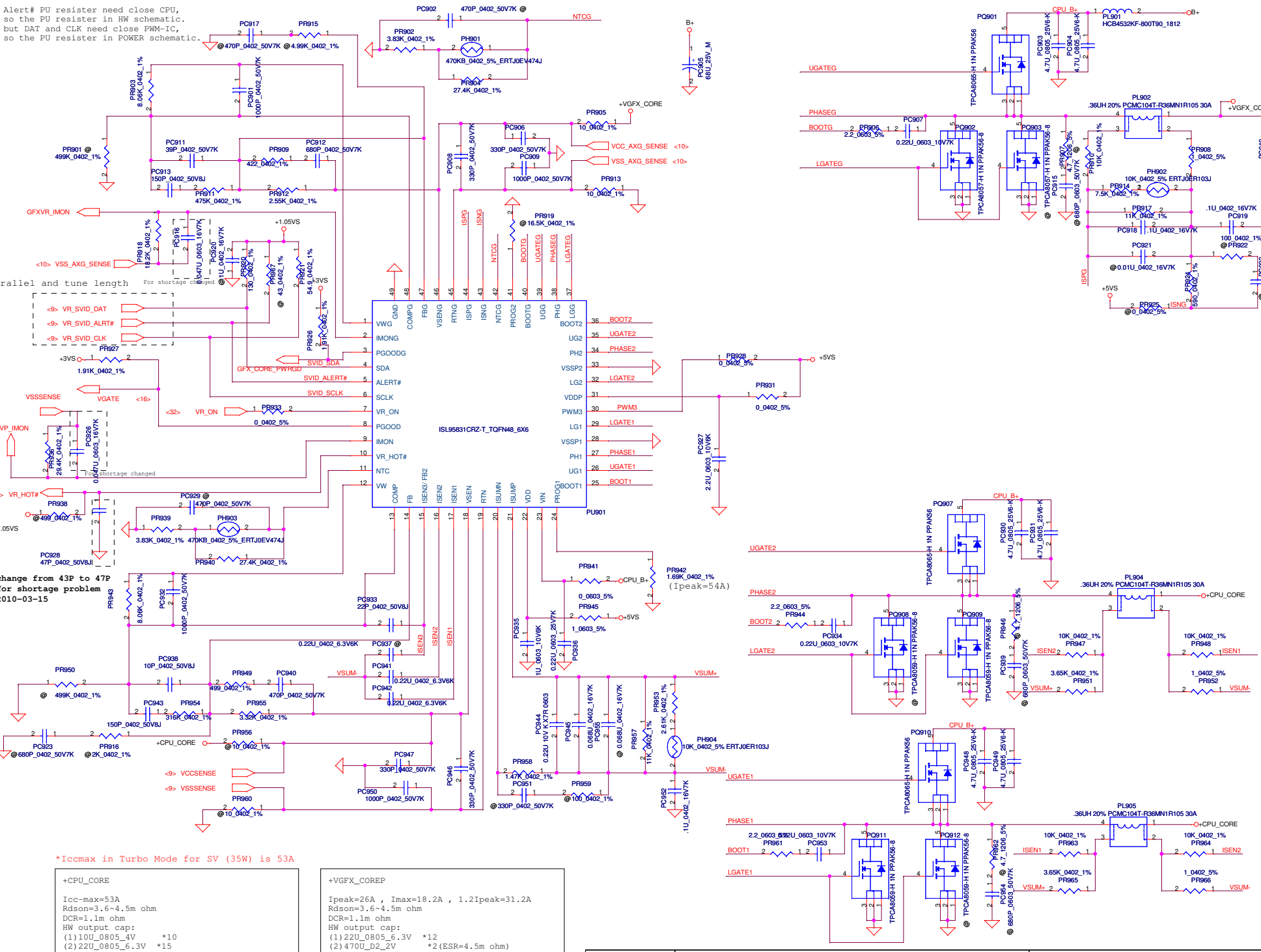


Note: Use VCCSA_SEL to switch High & Low Level for VID[1] (ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.



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				Date	Friday, November 26, 2010
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Alert# PU resistor need close CPU,
so the PU resistor in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resistor in POWER schematic.



*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE	
Icc-max=53A	
Rdson=3.6~4.5m ohm	
DCR=1.1m ohm	
HW output cap:	
(1) 10U_0805_4V	*10
(2) 22U_0805_6.3V	*15
(3) 470U_D2_2V	*4 (ESR=4.5m ohm)

*OCP setting value=71.5A

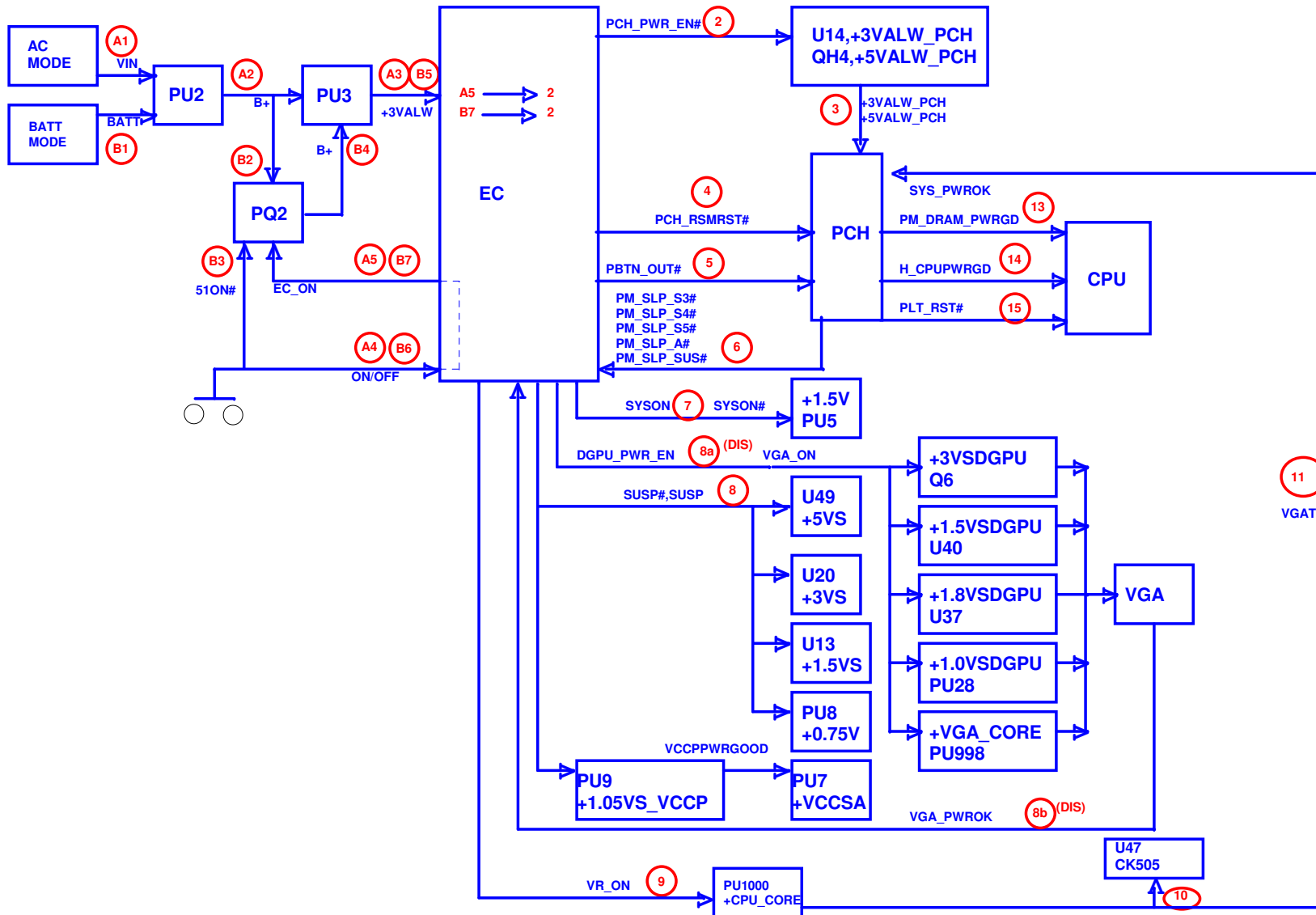
+VGFX_COREP	
Ipeak=26A, Imax=18.2A, 1.2Ipeak=31.2A	
Rdson=3.6~4.5m ohm	
DCR=1.1m ohm	
HW output cap:	
(1) 22U_0805_6.3V	*12
(2) 470U_D2_2V	*2 (ESR=4.5m ohm)

*OCP setting value=37A

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Title		Compal Electronics, Inc. PWR +CPU_CORE/+VGFX_CORE	
Size	Custom	Document Number	PWVG1/G2(LA-6759P/LA-675AP)
Date	Friday, November 26, 2010	Sheet	53 of 54

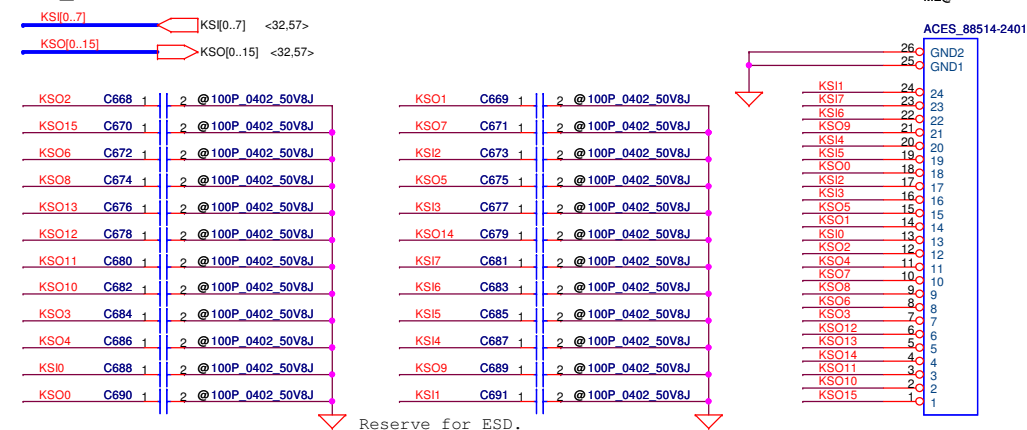
Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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				Size	Document Number	Rev
				Custom	PIWG1/G2(LA-6759P/LA-675AP)	0.1
Date:				Friday, November 26, 2010	Sheet 54 of 54	

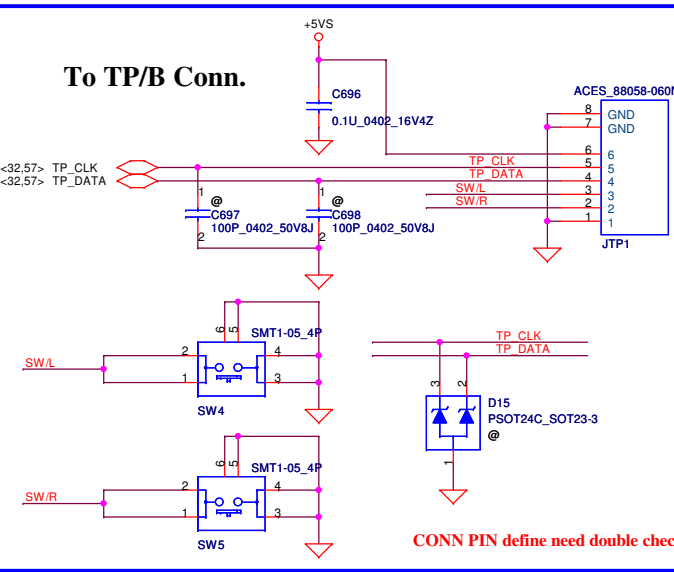


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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	
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Size	Custom	Document Number	LA-6752P	Rev	0.2
Date:	Friday, November 26, 2010	Sheet	55	of	60

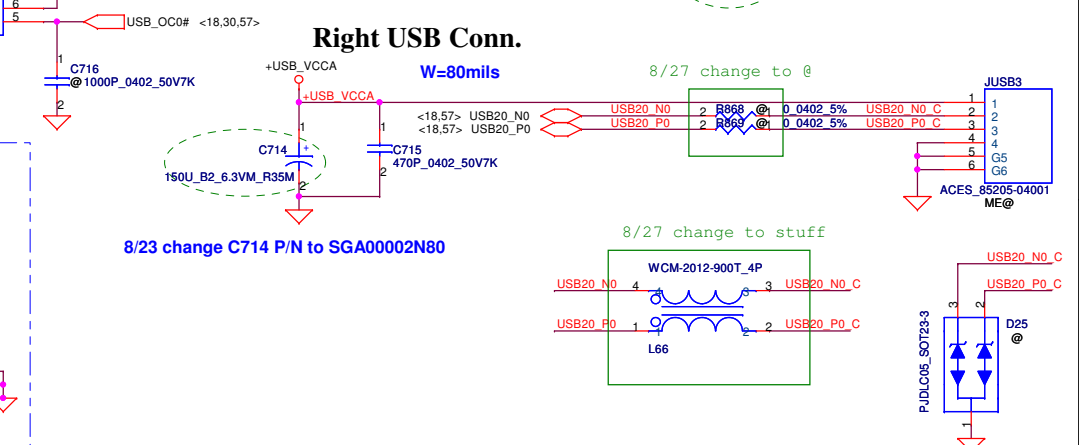
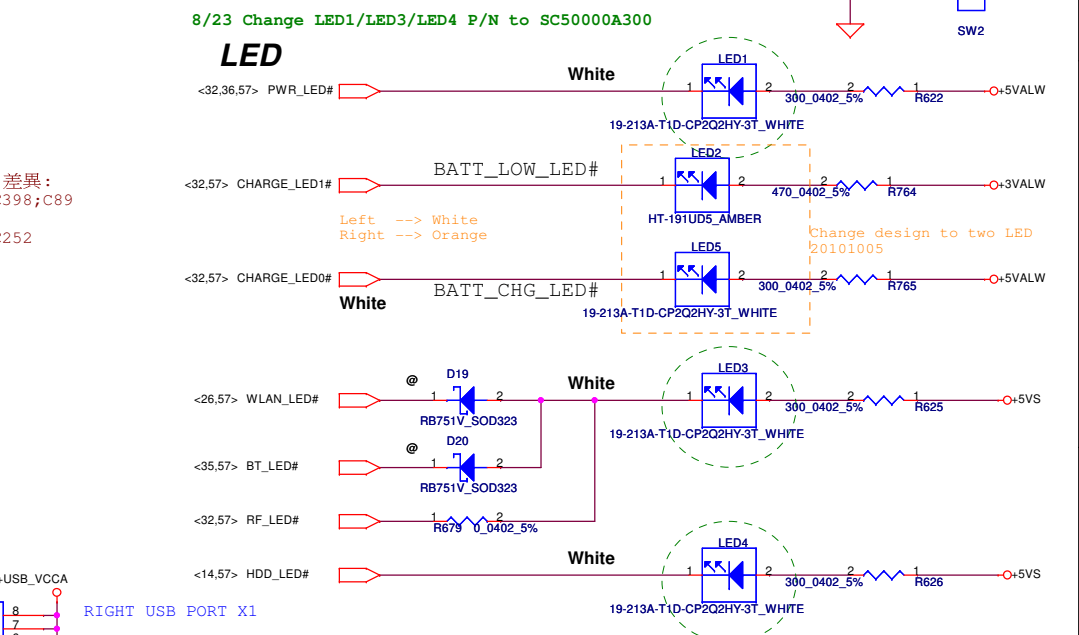
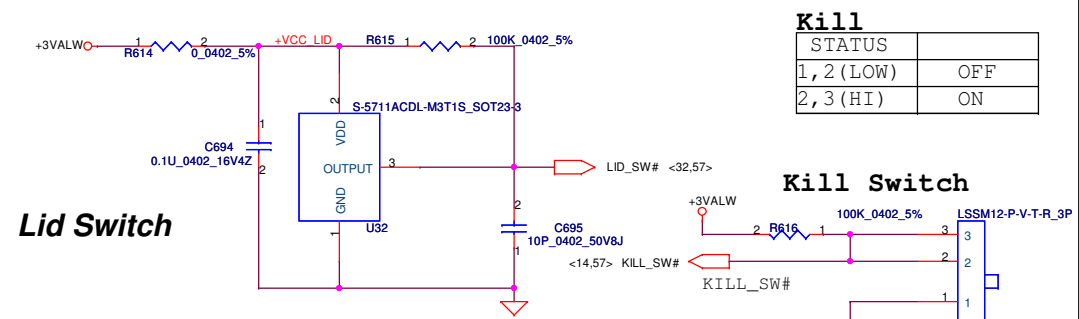
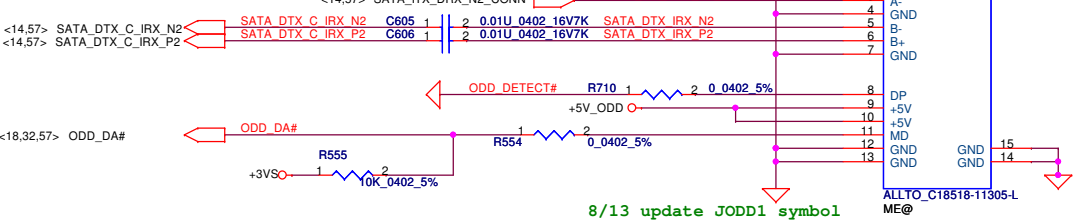
INT_KBD Conn.



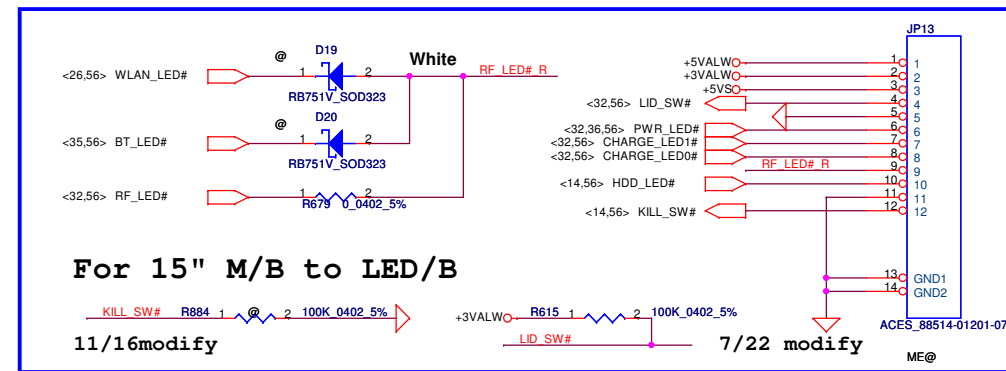
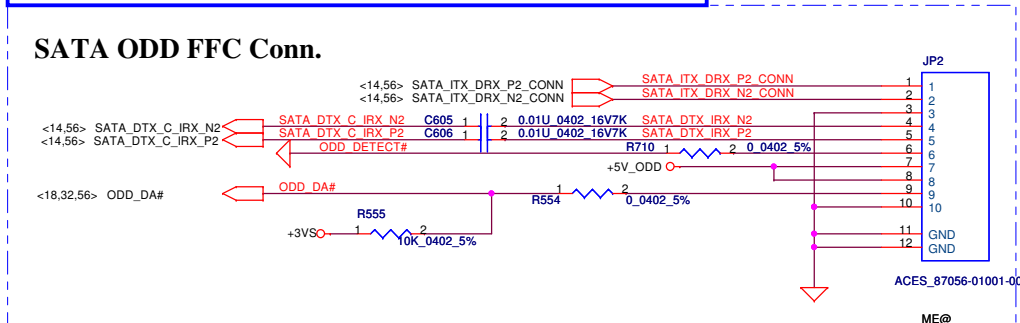
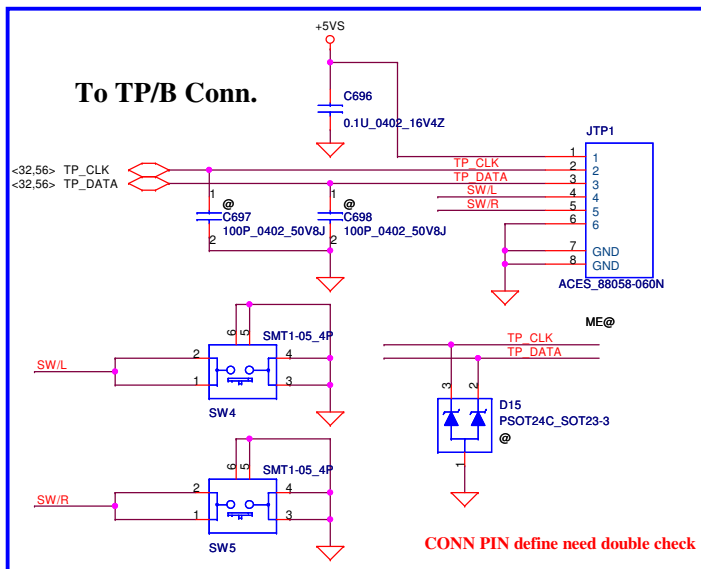
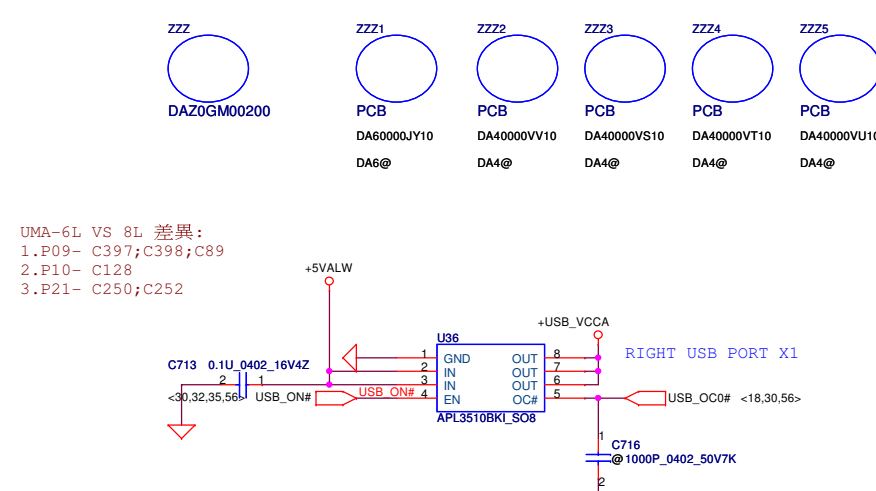
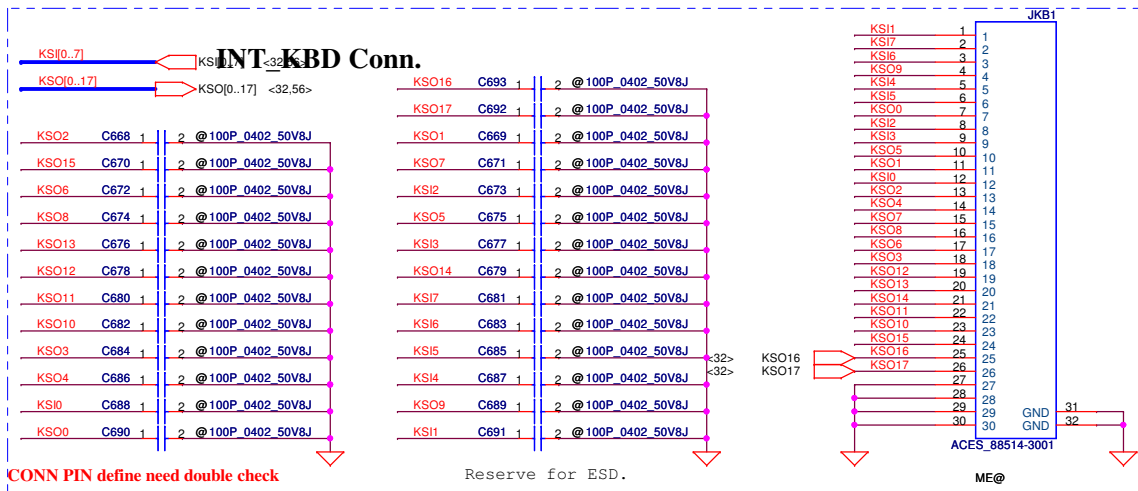
CONN PIN define need double check



SATA ODD Conn.



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Size	Document Number	LA-6751P		Rev 0.2	
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	5		4	3	2	1
D	PHASE	PAGE	Modification list	PURPOSE		
	0.2	P31	Change CRT Symbol	For CRT footprint issue		
	0.2	P31	Del C510	For Non-used part		
	0.2	P39	change C610 pin 1 net name	change C610 pin 1 net name to correct		
	0.2	P35	U25 change to U26	For co-lay 10/100 and GIGA		
	0.2	P40	Add R740, C93	For EC request		
	0.2	P18	Change R215 pin1 net name	Change R215 pin1 net name to correct		
	0.2	P16	Add R742, R743	For PCH power sequence		
	0.2	P38	Del U28, R542~R551 , J12	Del USB charger circuit		
	0.2	P40	Add EC pin 97,98,103	Add EC pin 97 for SYS_PWROK_EC , pin 98 for CE_EN , pin 103 for BATT_SEL_EC		
	0.2	P39	Change JI0 footprint and Add J13	Change JI0 footprint by DFX request and Add J13 by vendor suggestion		
	0.2	P39	Change PC_BEEP circuit	Change PC_BEEP circuit		
	0.2	P6	Add R161,	Follow ORB circuit		
	0.2	P58/59	Add R615 in 15" and 17" page	Pull high LiD_SW# at M/B side		
	0.2	P31	Add Q83 pin 1 power net name +CMOS_PW	For power trace net		
	0.2	P56/57/58	Change JP21 to JKBI	Change connector to standard name		
	0.2	P56/57/58	Change JP4 to JTP1	Change connector to standard name		
	0.2	P43/60	Change JP6 to JPWRB1	Change connector to standard name		
	0.2	P34	Change JP1 to JWLN1	Change connector to standard name		
	0.2	P42	Change JP5 to JBTL	Change connector to standard name		
C	0.2	P43/60	Change JP7 to JCRI	Change connector to standard name		
	0.2	P19	Add R542	For ESATA detect function		
	0.2	P42	Add R866, R886 , C735	For ESATA detect function		
	0.2	P31	Add R543	For reserve EC control directly		
	0.2	P39	Change JI0 footprint, Del C635, C636	Change JI0 for DFX and Del component for layout		
	0.2	P42	Add R877	For reserve EC control directly		
	0.2	P42	SW3 BOM structure change to @	For ME ASSY concern		
	0.2	P42	Change ESATA from port 5 to port 4	For intel risk		
	0.2	P15	Add R544,R545	For Pull high SMBus		
	0.2	P12/I3	Del R74-R80,R82 R88-R94,R96	For DDR3 DM Bus to GND		
	0.2	P16	Add R182,R546	Add 186 for reserve sequence, Add R546 for follow CRB & ORB		
	0.2	P20	Del Add J12, R257 change to @	For voltage drop		
	0.2	P6	R161 change to 100K	Follow CRB		
	0.2	P19	Add R547 , R250 change to @	Follow Module and CRB		
B	0.2	P18	WLAN USB port for port8 to port9	For debug port		
	0.2	P39	Del J13	For layout space		
	0.2	P20,39,42	Add C395 , R581 , R583 , R584 , R586 , R587	For customer request reserved		
	0.2	P20	Add C129, C396 , Del R264	For reserved		
	0.2	P40	Add PIN 66 , R740,C93 change to @	Add IMVP_IMON		
	0.2	P9	Add R74	For VCCIO_SENSE / VSPIO_SENSE differential routing		
	0.2	P30	Del R419~425, R427~R429	Del 0 ohm for UMA only		
	0.2	P31	Del R439 , R440, R441	Del 0 ohm for UMA only		
	0.2	P32	Del RQ51 ~ Q54 Add Q95	For DIS HDMI		
A	0.2	P38	Del JI0, C637,C640,R576,R577,R579 change to @ , L40-L43 change to R720-R723 Del C643, R578 , MIC_INN connect MIC_INL , Add R578	For Vendor suggestion and EMI Del C653, R578 connect MIC_INN/L for vendor suggestion , Add R578 for EMI		
	0.2	P20	Add L75 , R264 , C917, R259 C226 change to @	For intel PDG update		
	0.2	P43	C714 change to OSCON CAP	C714 change to OSCON CAP		
	0.2	P9	Add C394, C397 ,C398 , C399 ,Add R75	For CPU_CORE power reserved at Bottom side, Add R75 for reserved at cpu side and pwr side		
	0.2	P42	Change C706 P/N to SF000001500	Change to H=6 OSCAN		
	0.2	P10	Change CI28 to @	For Reserved		
	0.2	P56	Update JODDI symbol	For ME update drawing		
	5		4	3	2	1
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