

Compal Confidential

JE50/HM50/SJV50_BZ P5WE6/P5WH6/P5WS6 Schematics Document

AMD Brazos

Brazos with Zacate / Hudson M1 / Seymour XT

DIS only / UMA only / PX Muxless / PX Muxless with BACO

2010-11-16
LA-7092P REV: 1.0

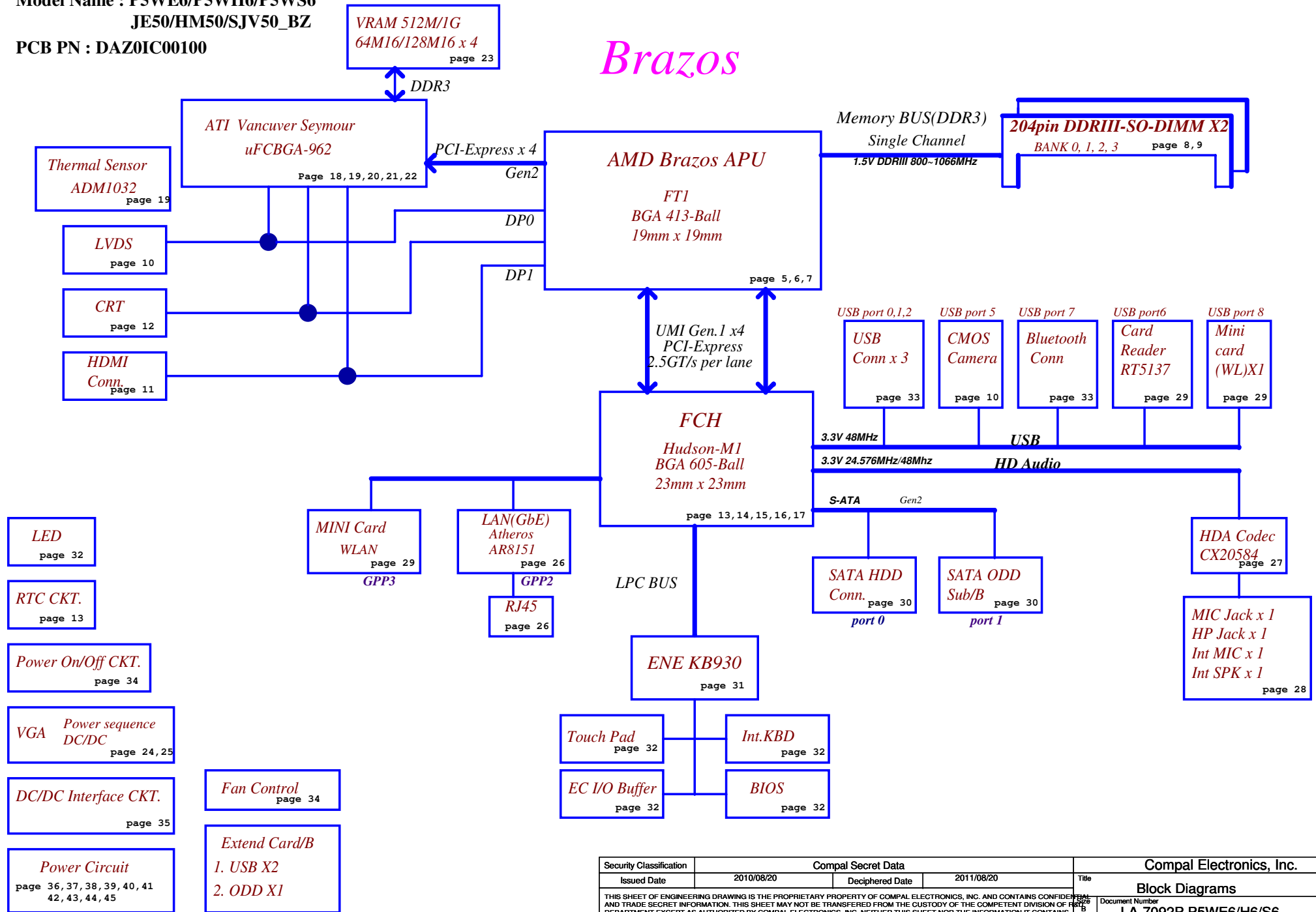


Part Number = DAZ0IC00100

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Issued Date	2010/08/20	Deciphered Date	2011/08/20	Title	Cover Page
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Model Name : P5WE6/P5WH6/P5WS6
JE50/HM50/SJV50_BZ
PCB PN : DAZ0IC00100



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VSB	VSB always on power rail	ON	ON	ON*
+3VALW	3.3V always on power rail	ON	ON	ON*
+5VALW	5V always on power rail	ON	ON	ON*
+1.1VALW	1.1V always on power rail	ON	ON	ON*
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for APU VDD10	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+3VSG	3.3V switched power rail for GPU	ON	OFF	OFF
+1.8VSG	1.8V switched power rail for GPU	ON	OFF	OFF
+1.5VSG	1.5V switched power rail for GPU	ON	OFF	OFF
+1.0VSG	1.0V switched power rail for GPU	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
			ADM1032 (GPU)	1001-101xb	9AH

SM Bus Controller 0

(FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

SM Bus Controller 1

(FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

Project ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

BOARD ID Table

Board ID	PCB Revision
0	w/ X'tal X1
1	wo/ X'tal X1
2	
3	
4	
5	
6	
7	

Project ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Display from APU	UMA@
Display from VGA	DISO@
Use VGA	VGA@
Muxless w/BACO	BACO@
Muxless wo/BACO	WOBACO@
Muxless	PX@
w/Vancouver Serise	VAN@
w/Manhattan Serise	MAN@
Bluetooth	BT@
AR8151	8151@
Seymour	Seymour@
wo/Muxless	WOPX@
wo/VGA	WOVGA@
APU 1.5G	15G@
APU 1.6G	16G@

*UMA only :UMA@ BT@ 8151@ WOVGA@ WOPX@

VGA Chip SEL: APU Chip SEL:
1. Seymour@ + Van@ 1. 16G@
2. Robson@ + Man@ 2. 15G@

*DIS only :VGA@ DISO@ WOBACO@ BT@ 8151@ WOPX@
*Muxless w/BACO : UMA@ VGA@ PX@ BACO@ BT@ 8151@
Muxless wo/BACO : UMA@ VGA@ PX@ WOBACO@ BT@ 8151@

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Power-Up/Down Sequence

1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5. VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)

VDDR3(3.3VSG)

PCIE_VDDC(1.0V)

VDDR1(1.5VSG)

VDDC/VDDCI(1.12V)

VDD_CT(1.8V)

PERSTb

REFCLK

Straps Reset

Straps Valid

Global ASIC Reset

Note: Do not drive any IOs before VDDR3 is ramped up.

T4+16clock

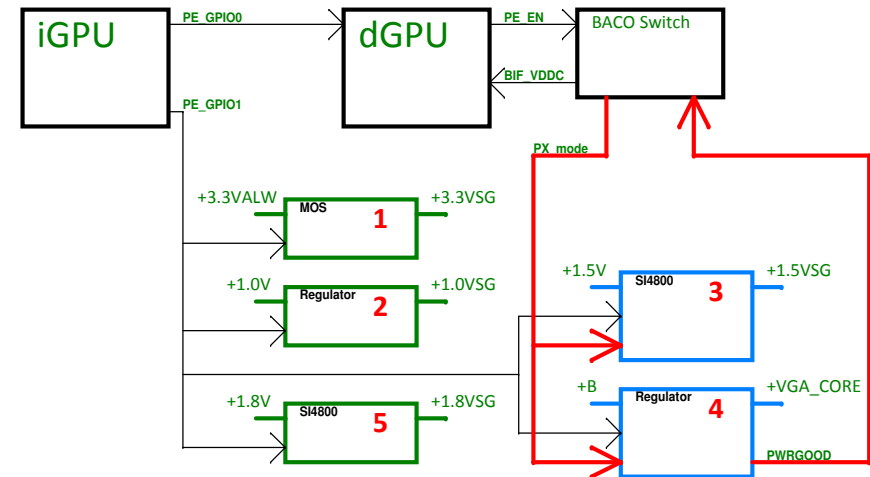
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High -> Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

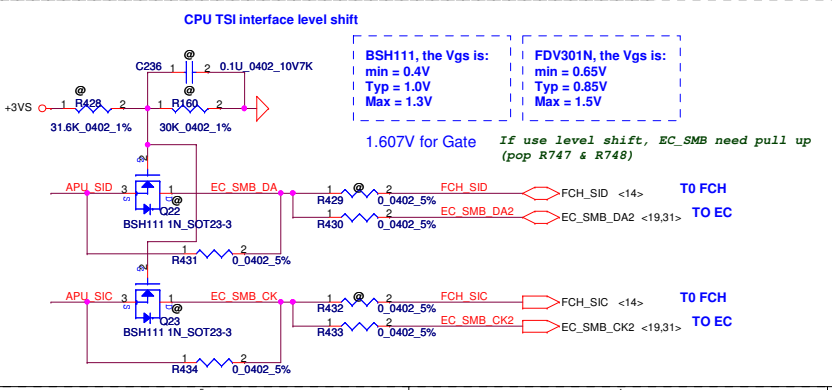
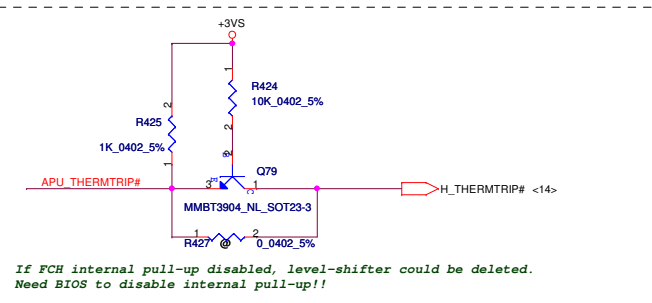
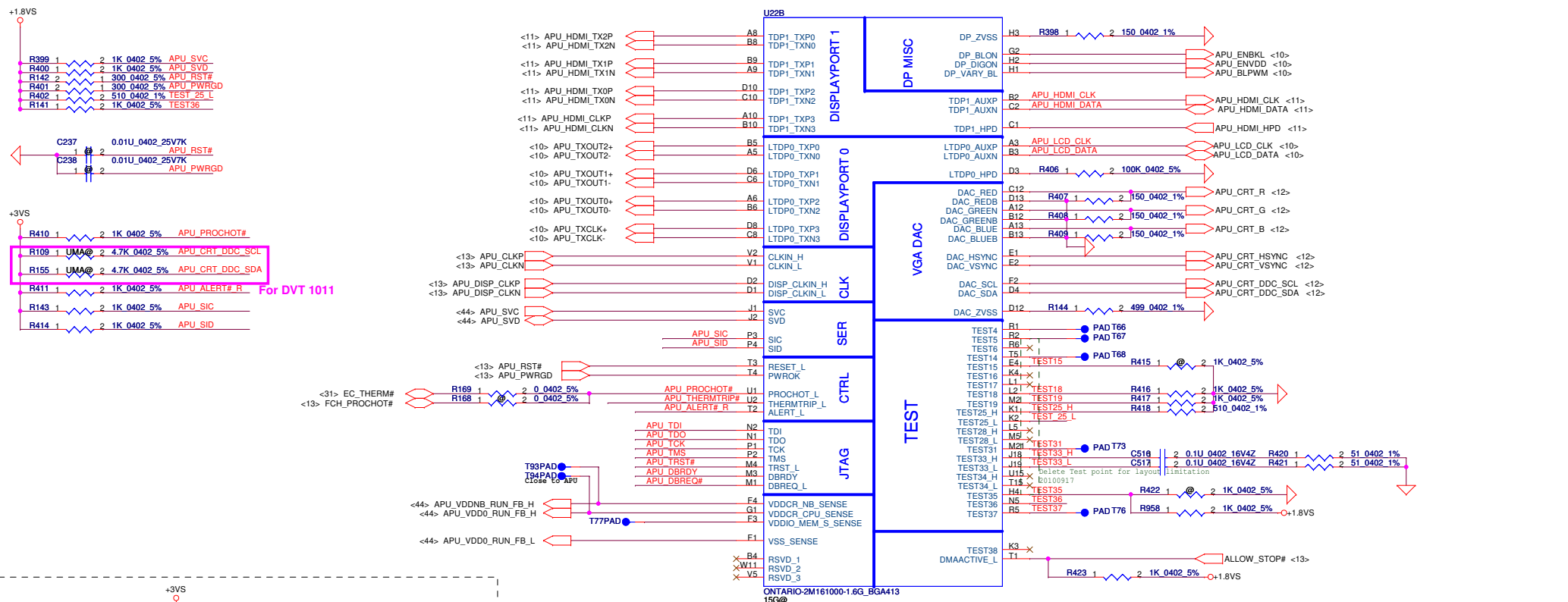
BACO option :

PE_GPIO0 : High -> Normal operation (dGPU is not reset on BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

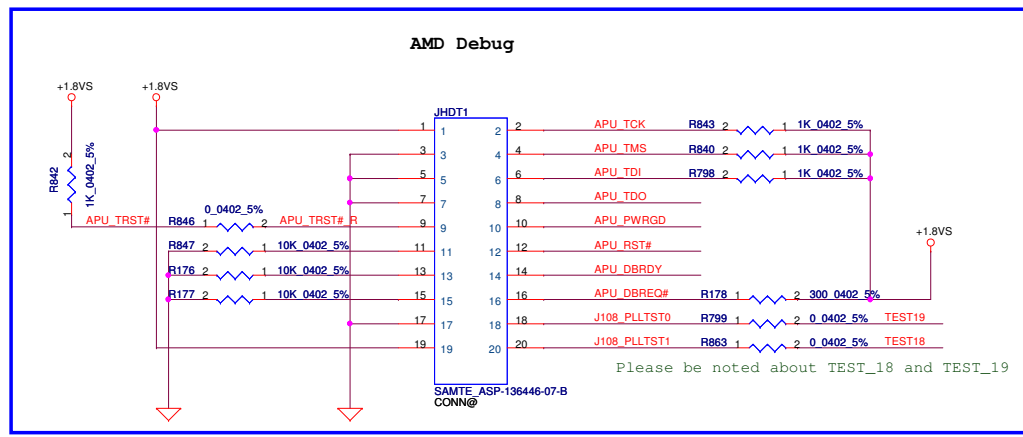
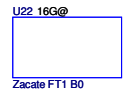
dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



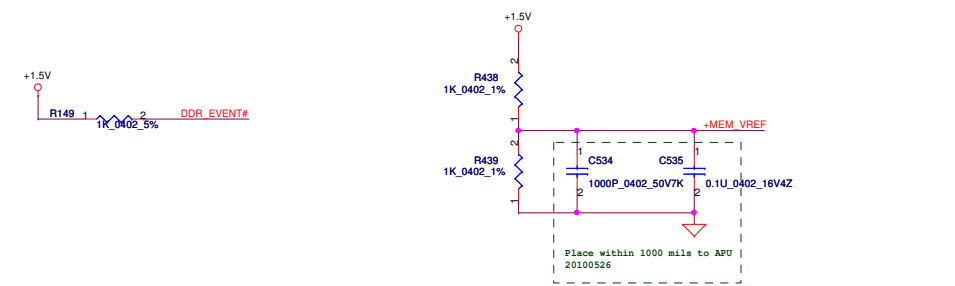
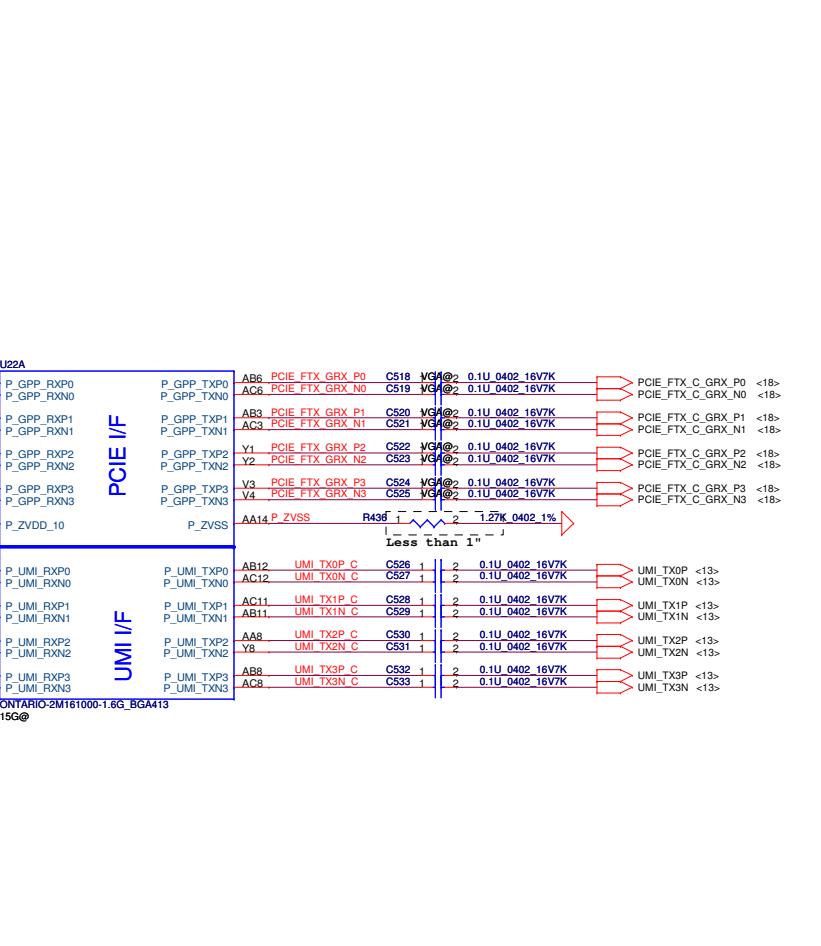
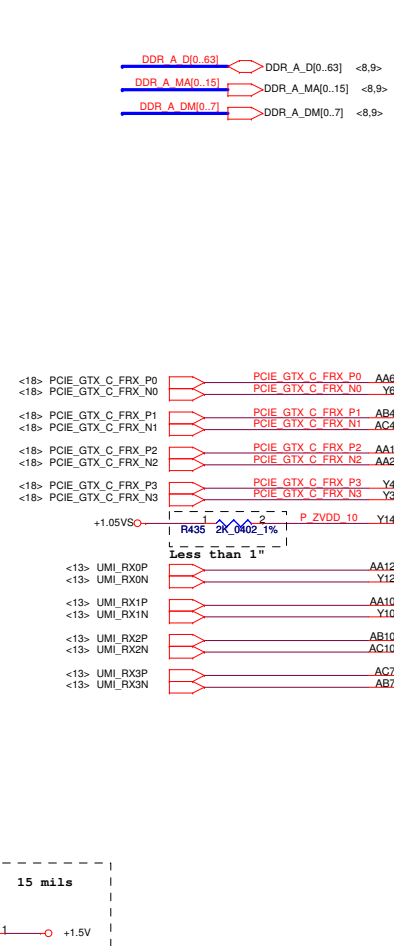
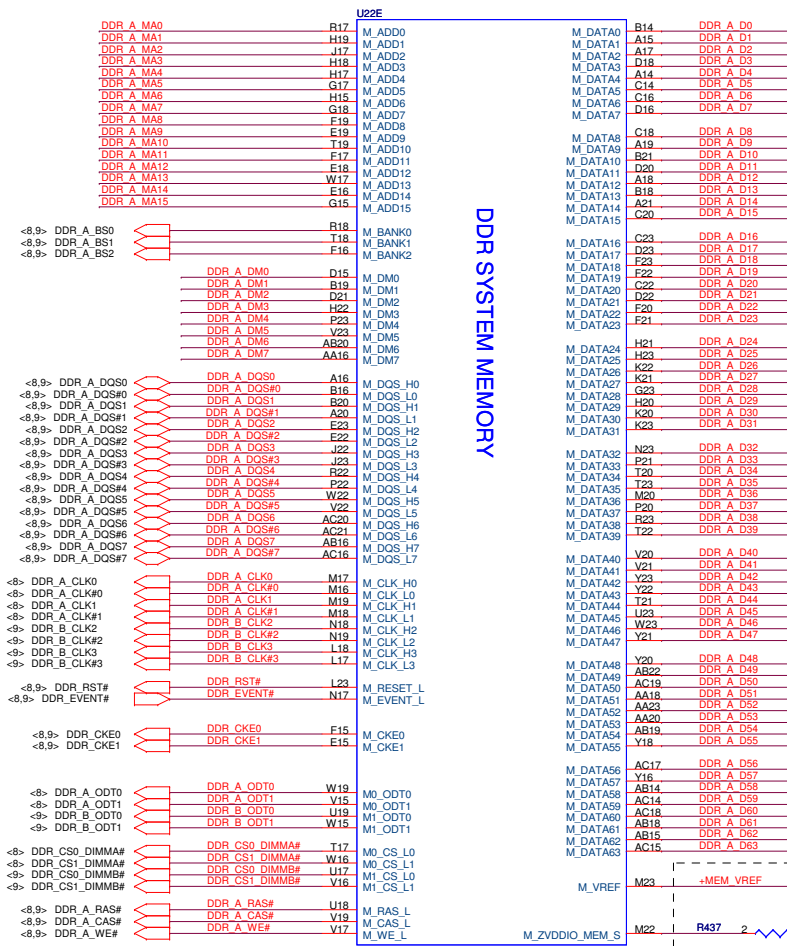
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Issued Date	2010/08/20	Deciphered Date	2011/08/20	Title	dGPU Block Diagram
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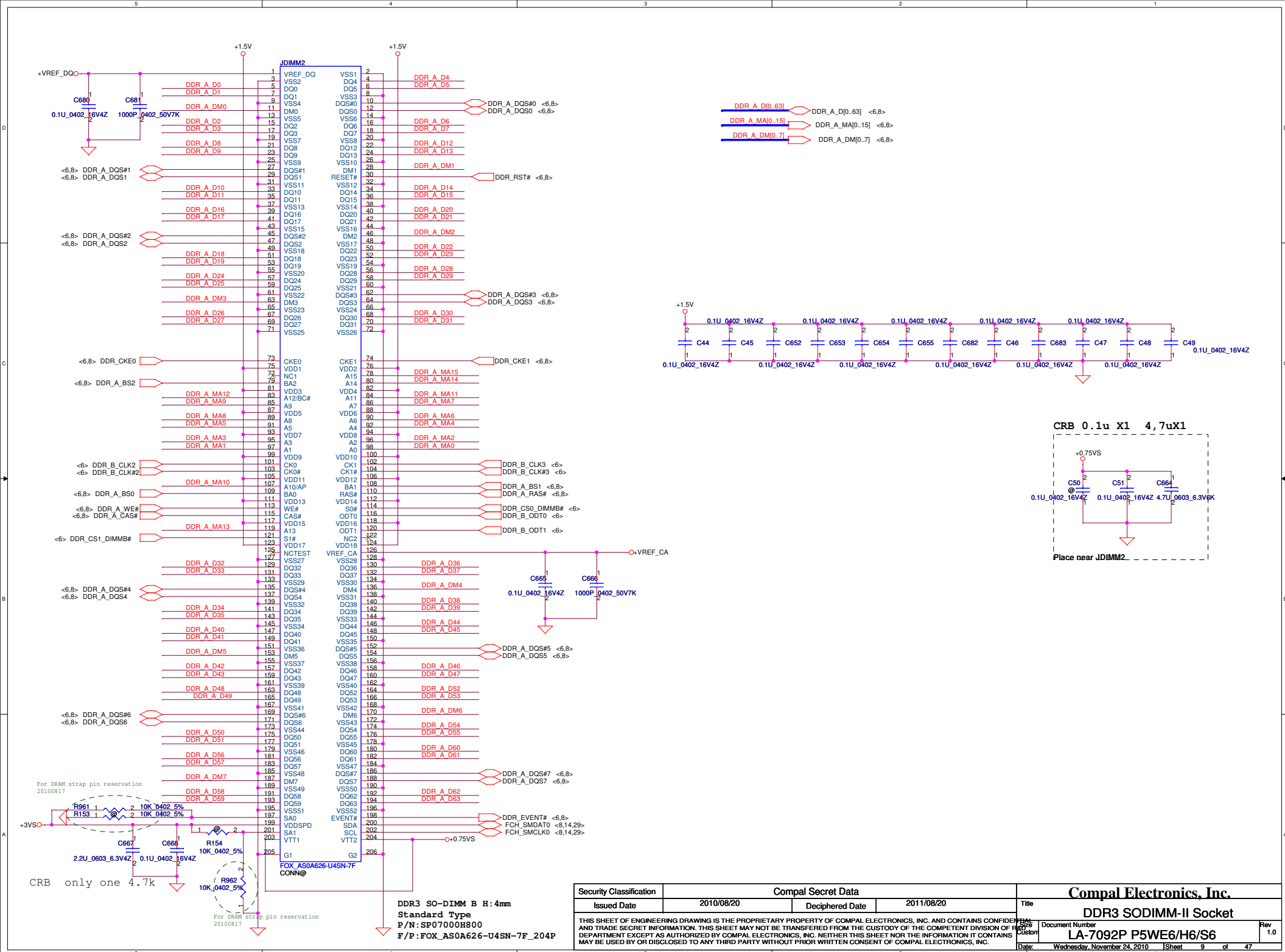
APU : SA00004D060 (S IC ZACATE 2M151132B1240 1.5G BGA)
APU : SA000046G80 (S IC ZACATE 2M161232B2240 1.6G BGA)



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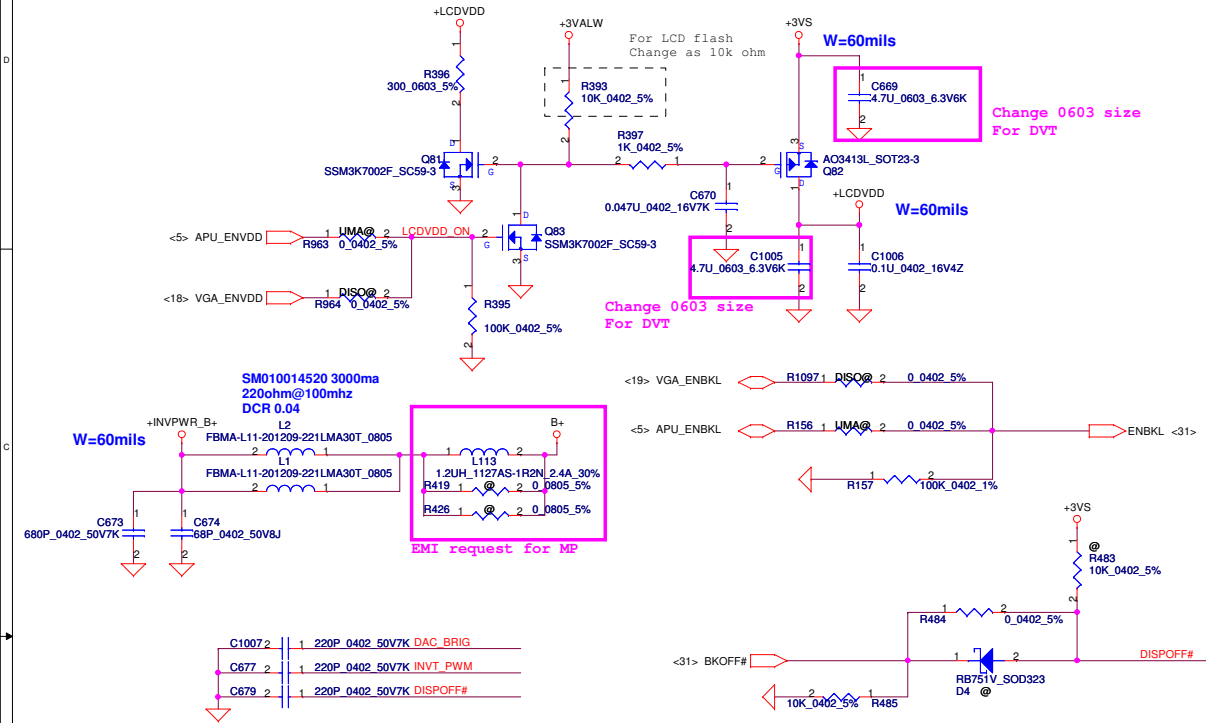


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								FT1 DDRIII/UMI/PCIE									
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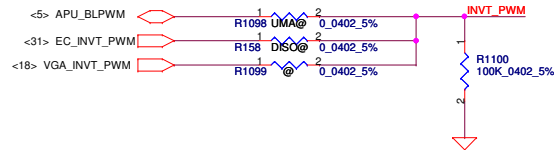
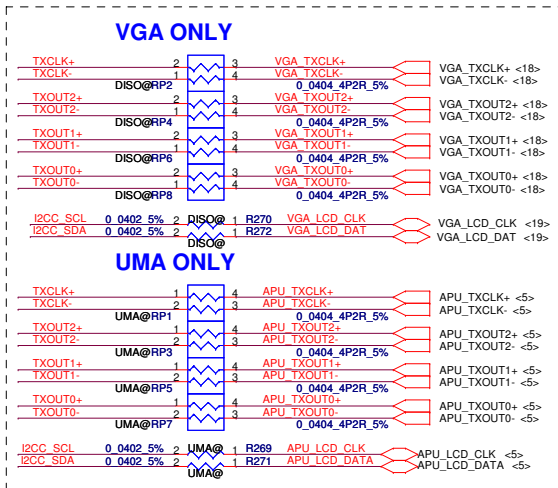
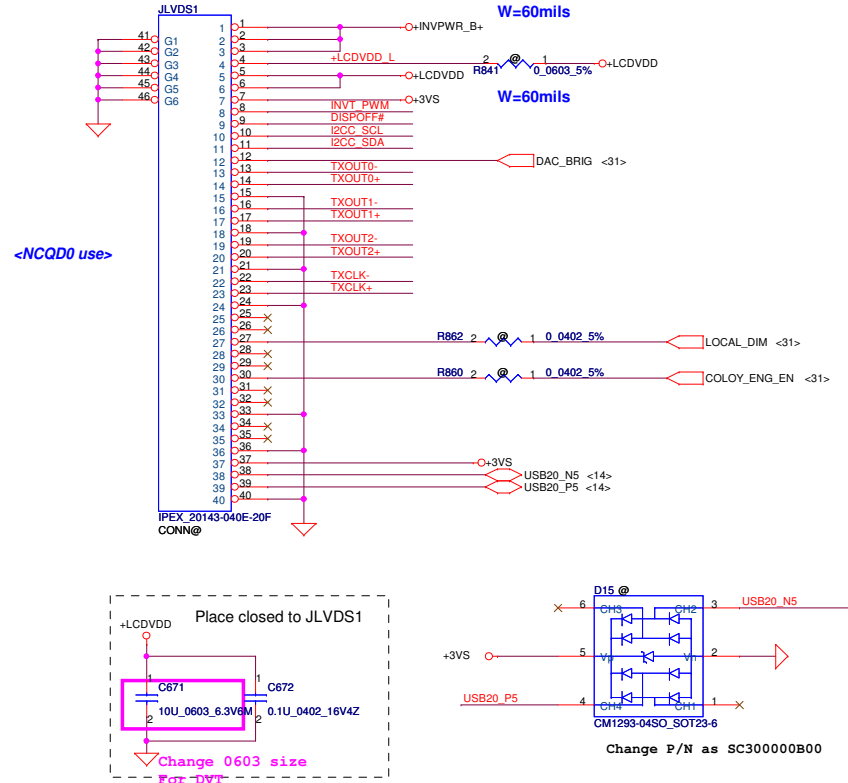


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Deciphered Date		2011/08/20		DDR3 SODIMM-II Socket	
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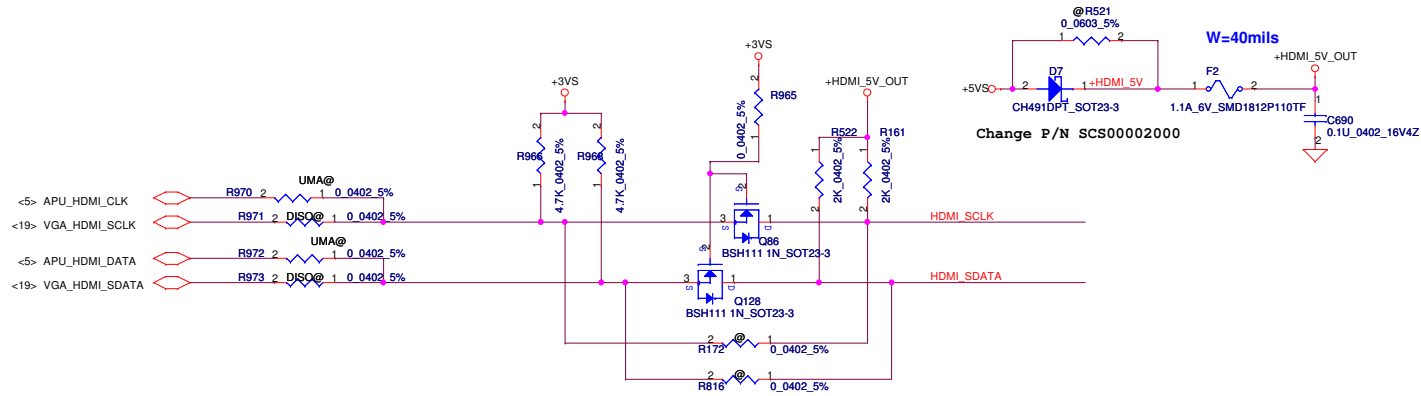
LCD POWER CIRCUIT



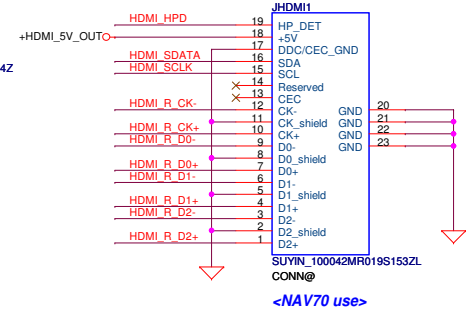
LCD/LED PANEL Conn.



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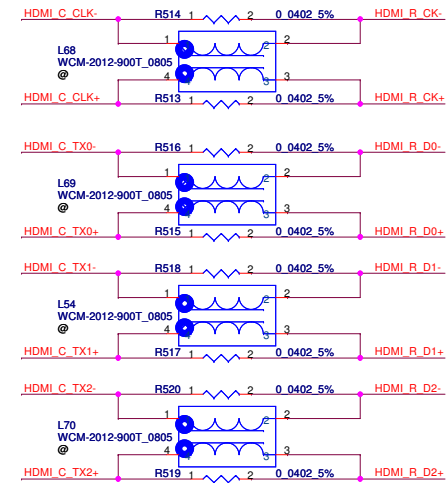


HDMI connector



Place closed to JHDMI1

SM070001310 400ma 90ohm@100mhz DCR 0.3



Use common via on related pair

From VGA

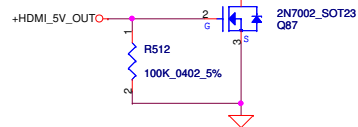
<19> VGA_HDMI_TXD2-	R974	1	DISO@	0.0402_5%	HDMI_C_TX2- R
<19> VGA_HDMI_TXD2+	R975	1	DISO@	0.0402_5%	HDMI_C_TX2+ R
<19> VGA_HDMI_TXD1-	R976	1	DISO@	0.0402_5%	HDMI_C_TX1- R
<19> VGA_HDMI_TXD1+	R977	1	DISO@	0.0402_5%	HDMI_C_TX1+ R
<19> VGA_HDMI_TXD0-	R978	1	DISO@	0.0402_5%	HDMI_C_TX0- R
<19> VGA_HDMI_TXD0+	R979	1	DISO@	0.0402_5%	HDMI_C_TX0+ R
<19> VGA_HDMI_TXC-	R980	1	DISO@	0.0402_5%	HDMI_C_CLK- R
<19> VGA_HDMI_TXC+	R981	1	DISO@	0.0402_5%	HDMI_C_CLK+ R

From APU

<5> APU_HDMI_TX2N	R984	1	UMA@	0.0402_5%	HDMI_C_TX2- R
<5> APU_HDMI_TX2P	R985	1	UMA@	0.0402_5%	HDMI_C_TX2+ R
<5> APU_HDMI_TX1N	R986	1	UMA@	0.0402_5%	HDMI_C_TX1- R
<5> APU_HDMI_TX1P	R987	1	UMA@	0.0402_5%	HDMI_C_TX1+ R
<5> APU_HDMI_TX0N	R988	1	UMA@	0.0402_5%	HDMI_C_TX0- R
<5> APU_HDMI_TX0P	R989	1	UMA@	0.0402_5%	HDMI_C_TX0+ R
<5> APU_HDMI_CLKN	R990	1	UMA@	0.0402_5%	HDMI_C_CLK- R
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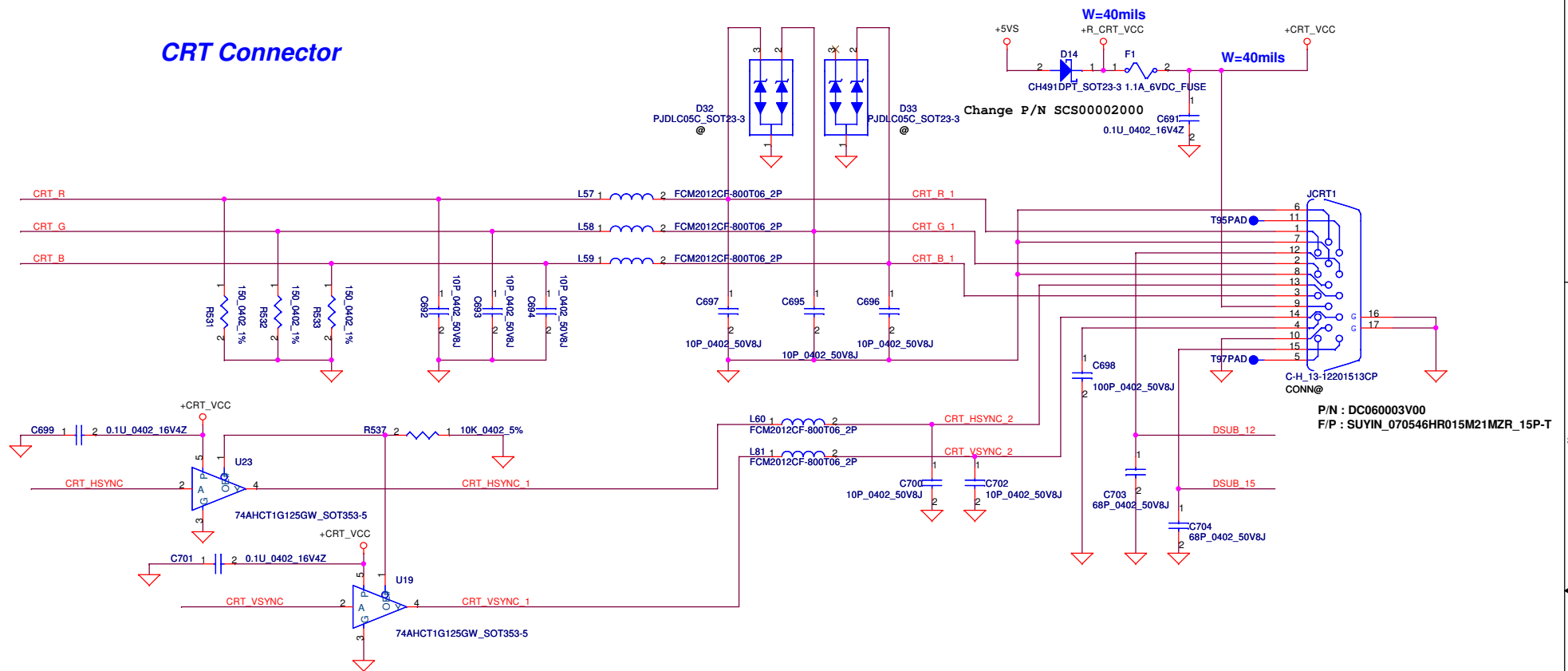
Place closed to JHDMI1

HDMI_C_TX2- R	C508	2	1	0.1U_0402_16V7K	HDMI_C_TX2- R509	1	2	499_0402_1%
HDMI_C_TX2+ R	C509	2	1	0.1U_0402_16V7K	HDMI_C_TX2+ R508	1	2	499_0402_1%
HDMI_C_TX1- R	C510	2	1	0.1U_0402_16V7K	HDMI_C_TX1- R506	1	2	499_0402_1%
HDMI_C_TX1+ R	C511	2	1	0.1U_0402_16V7K	HDMI_C_TX1+ R505	1	2	499_0402_1%
HDMI_C_TX0- R	C512	2	1	0.1U_0402_16V7K	HDMI_C_TX0- R503	1	2	499_0402_1%
HDMI_C_TX0+ R	C513	2	1	0.1U_0402_16V7K	HDMI_C_TX0+ R502	1	2	499_0402_1%
HDMI_C_CLK- R	C514	2	1	0.1U_0402_16V7K	HDMI_C_CLK- R501	1	2	499_0402_1%
HDMI_C_CLK+ R	C515	2	1	0.1U_0402_16V7K	HDMI_C_CLK+ R500	1	2	499_0402_1%

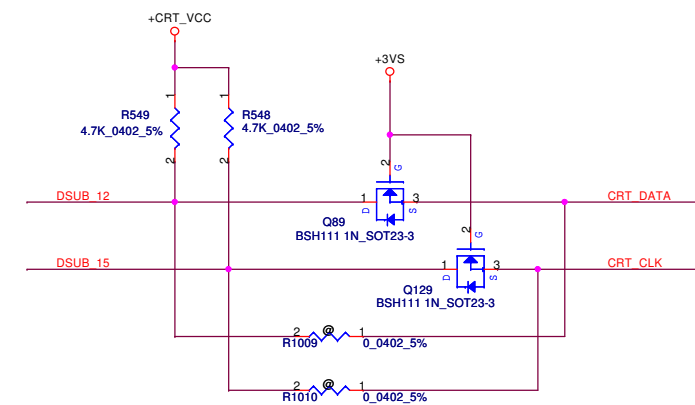


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Deciphered Date				2011/08/20				HDMI Connector			
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CRT Connector



Close to Conn side



Use common via on related pair

From APU

<5> APU_CRT_R		APU CRT R	R995	2	UMA@	1	0	0402	5%	CRT R
<5> APU_CRT_G		APU CRT G	R996	2	UMA@	1	0	0402	5%	CRT G
<5> APU_CRT_B		APU CRT B	R997	2	UMA@	1	0	0402	5%	CRT B
<5> APU_CRT_HSYNC		APU CRT HSYNC	R998	2	UMA@	1	0	0402	5%	CRT HSYNC
<5> APU_CRT_VSYNC		APU CRT VSYNC	R999	2	UMA@	1	0	0402	5%	CRT VSYNC
<5> APU_CRT_DDC_SDA		APU CRT DDC SDA	R1000	2	UMA@	1	0	0402	5%	CRT DATA
<5> APU_CRT_DDC_SCL		APU CRT DDC SCL	R1001	2	UMA@	1	0	0402	5%	CRT CLK

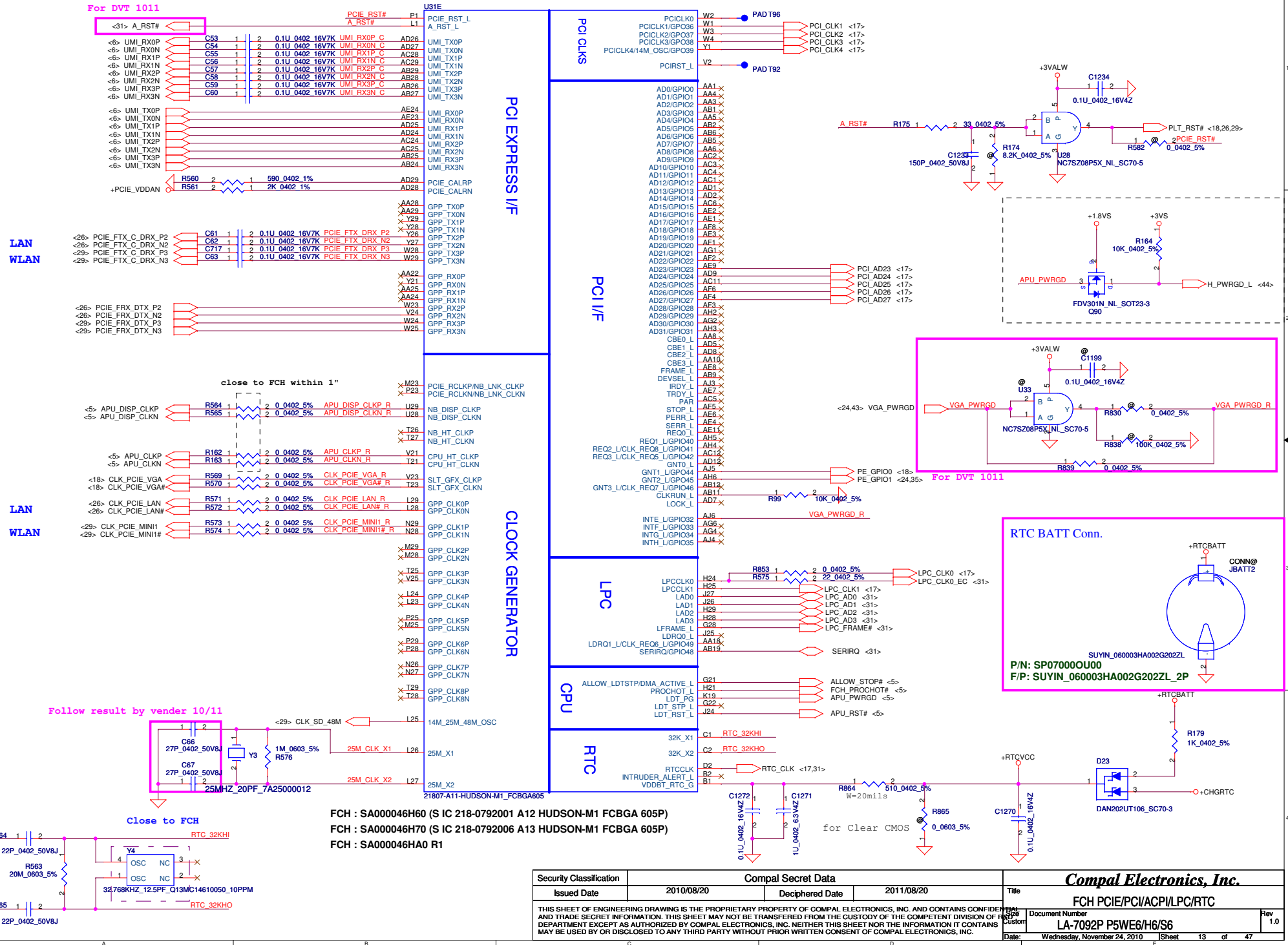
From VGA

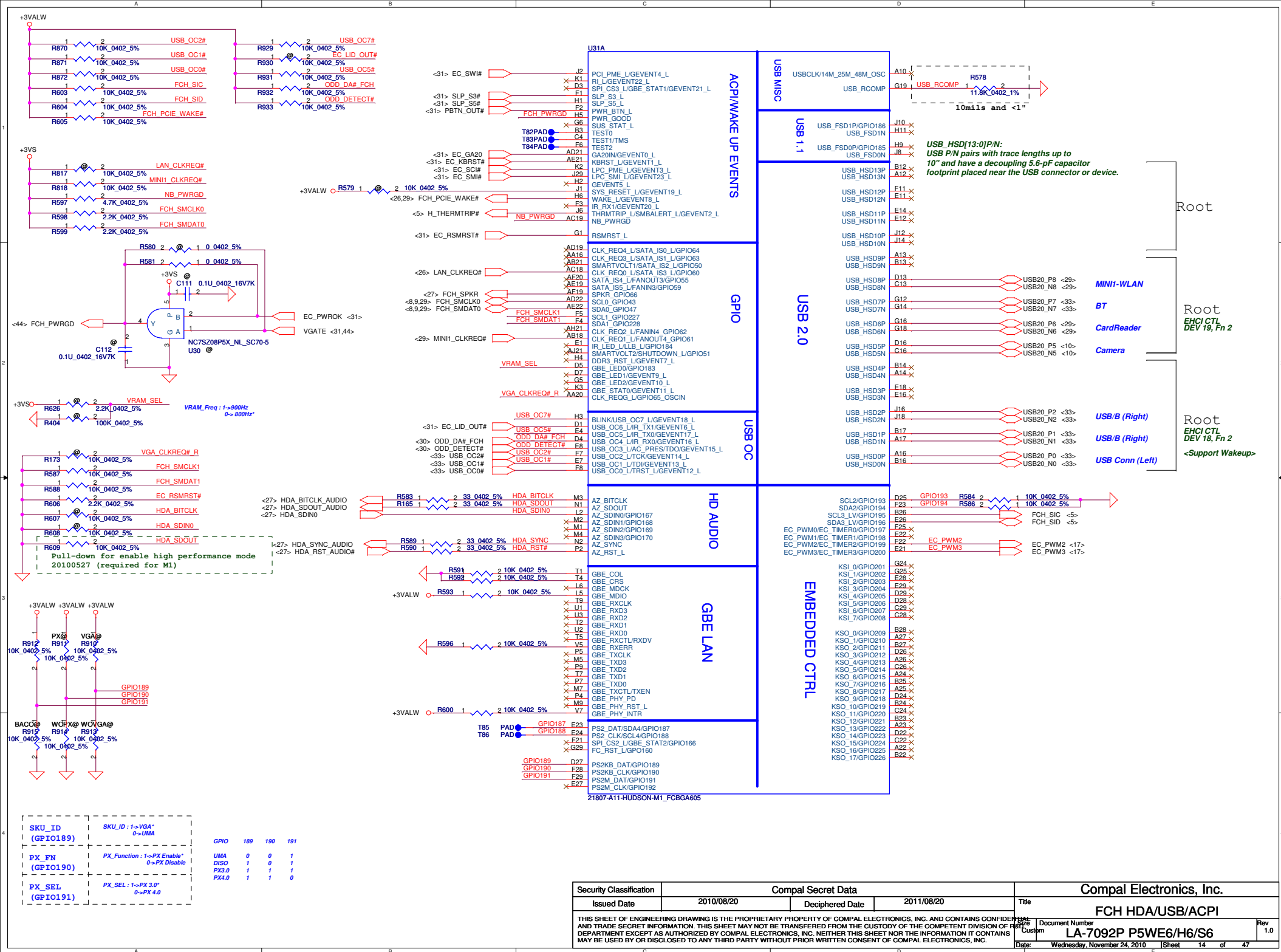
<19>	VGA_CRT_R	VGA CRT R	R1002	2	RISOR	1	0	0402	5%	CRT R
<19>	VGA_CRT_G	VGA CRT G	R1003	2	RISOR	1	0	0402	5%	CRT G
<19>	VGA_CRT_B	VGA CRT B	R1004	2	RISOR	1	0	0402	5%	CRT B
<19>	VGA_CRT_HSYNC	VGA CRT HSYNC	R1005	2	RISOR	1	0	0402	5%	CRT HSYNC
<19>	VGA_CRT_VSYNC	VGA CRT VSYNC	R1006	2	RISOR	1	0	0402	5%	CRT VSYNC
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<19>	VGA_CRT_CLK	VGA CRT CLK	R1008	2	RISOR	1	0	0402	5%	CRT CLK

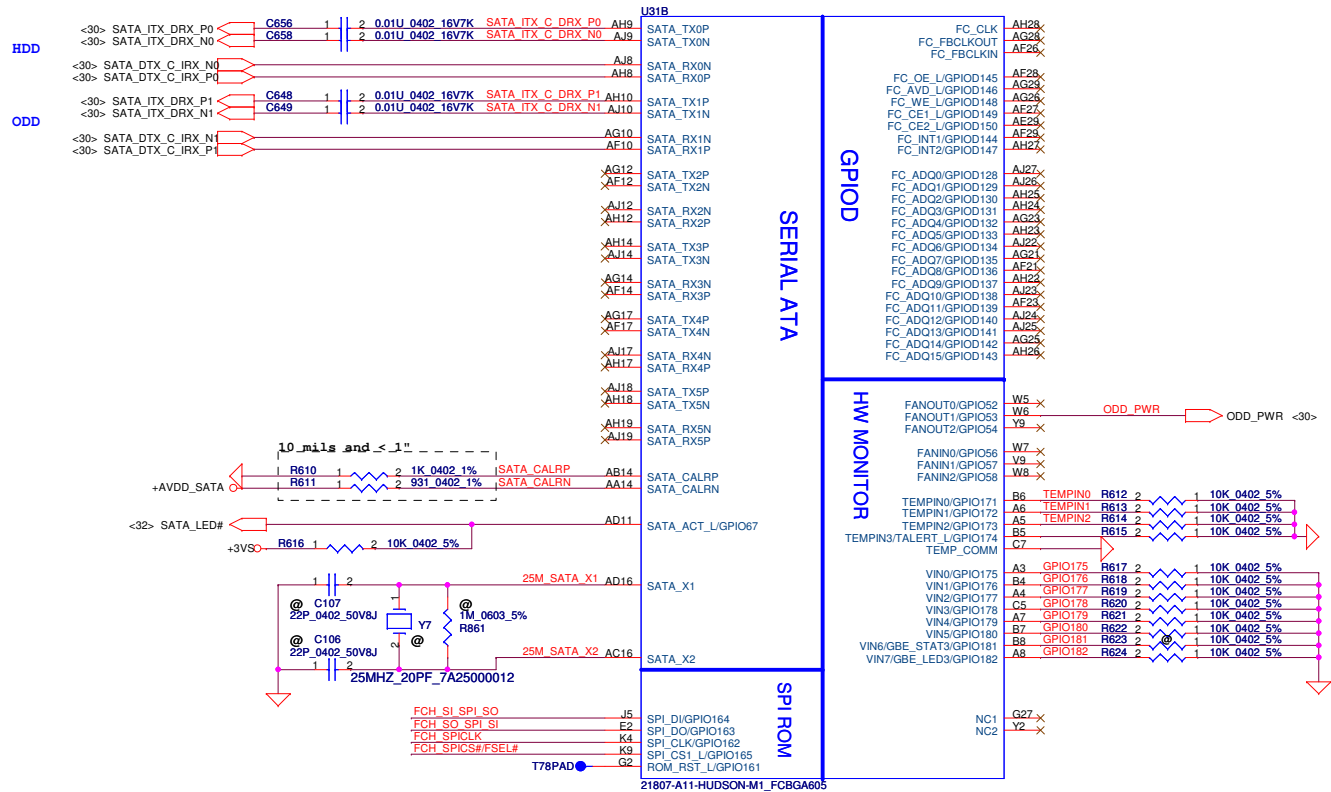
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2010/08/20	Deciphered Date	2011/08/20	Title CRT Connector			
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				Custom	LA-7092P P5WE6/H6/S6	1.0	
				Date:	Wednesday, November 24, 2010	ISheet 12 of 47	

For PCIE device reset on FS1 (GFX, GLAN, WLAN, LVDS Travis)

For DVT 1011

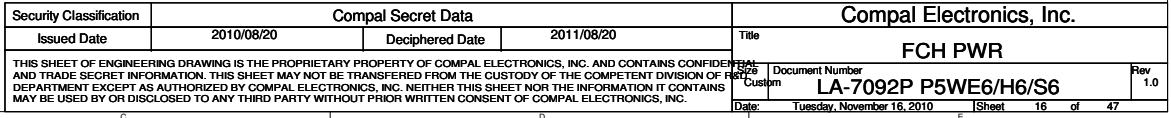


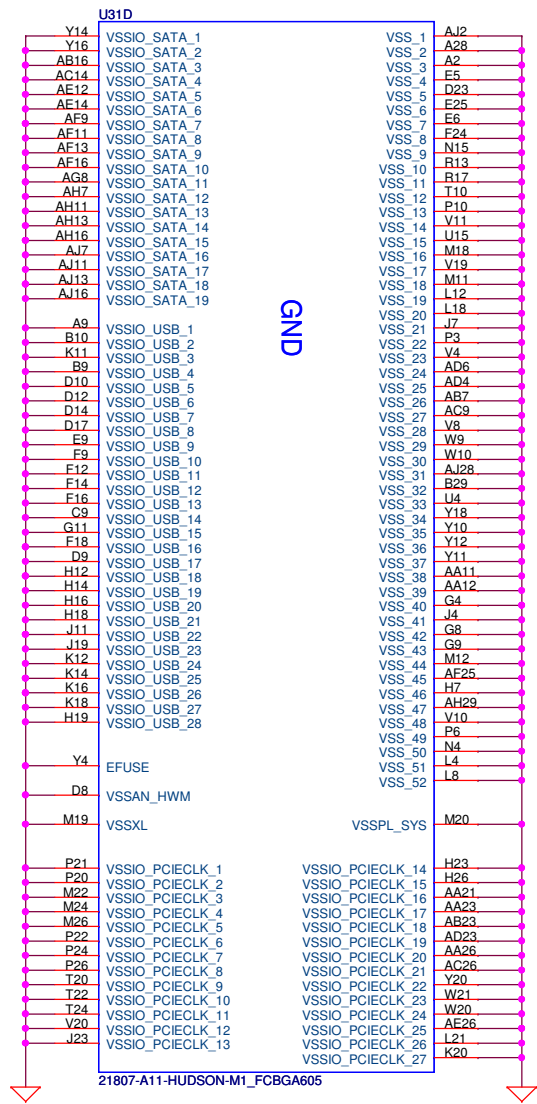




VIN6/GBE_STAT3/GPIO181
 Enable integrated pull-down/up and leave unconnected

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								2011/08/20			
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				Document Number				LA-7092P P5WE6/H6/S6			
				Date				Wednesday, November 24, 2010			
				Sheet				15 of 47			

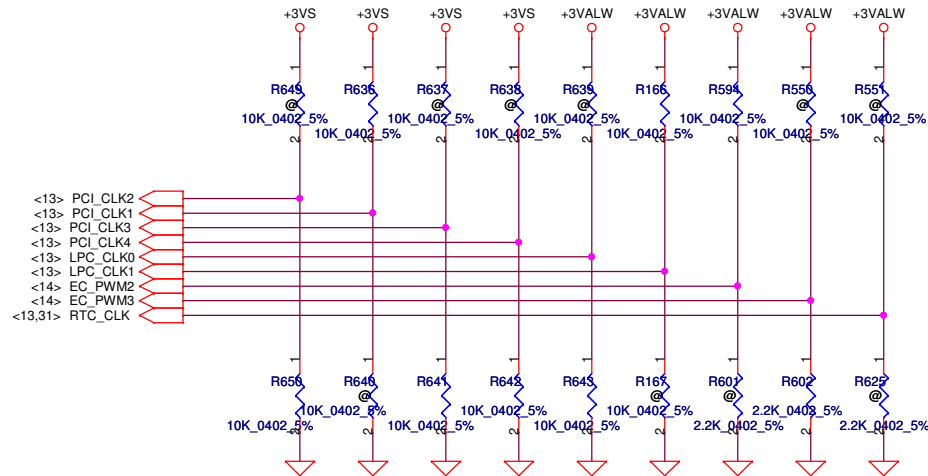




REQUIRED STRAPS

Check Internal PU/PD

PULL HIGH	PCI_CLK2	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	RTC_CLK	EC_PWM2 EC_PWM3
	WATCHDOG TIMER ENABLE	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAP	NON Fusion CLOCK Mode	Internal EC ENABLE	Internal CLKGEN Mode DEFAULT	S5 PLUS MODE DISABLED DEFAULT	LPC ROM (H,L) DEFAULT
PULL LOW	WATCHDOG TIMER DISABLE DEFAULT	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK Mode DEFAULT	Internal EC DISABLE DEFAULT	External CLKGEN Mode	S5 PLUS MODE ENABLED	SPI ROM(L,H)



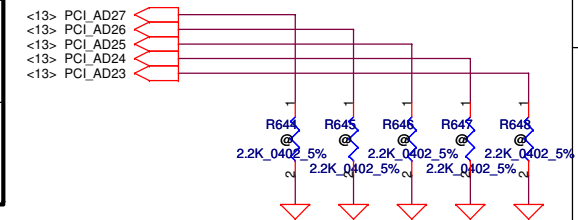
DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

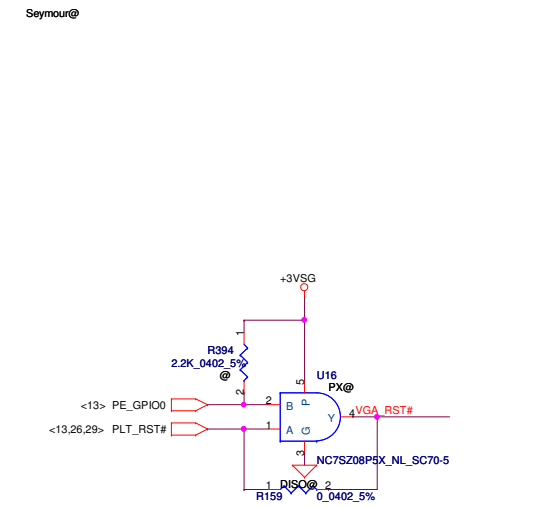
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH	USE internal PLL generated PLL CLK DEFAULT	ILA AUTORUN Disabled DEFAULT	Selects FC PLL DEFAULT	Disable I2C ROM DEFAULT	Required Setting DEFAULT
PULL LOW	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

Check AD29,AD28 strap function

check default



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				LA-7092P P5WE6/H6/S6	1.0
				Date: Wednesday, November 24, 2010	Sheet 17 of 47

[illegible]

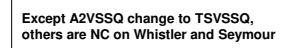
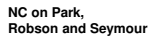
U2 Robson@
Robson XT-M2 A11
Robson A11 (SA00004DR20)

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				Customer	LA-7092P P5WE6/H6/S6	1.0	
				Date:	Wednesday, November 24, 2010	Sheet 18 of 47	

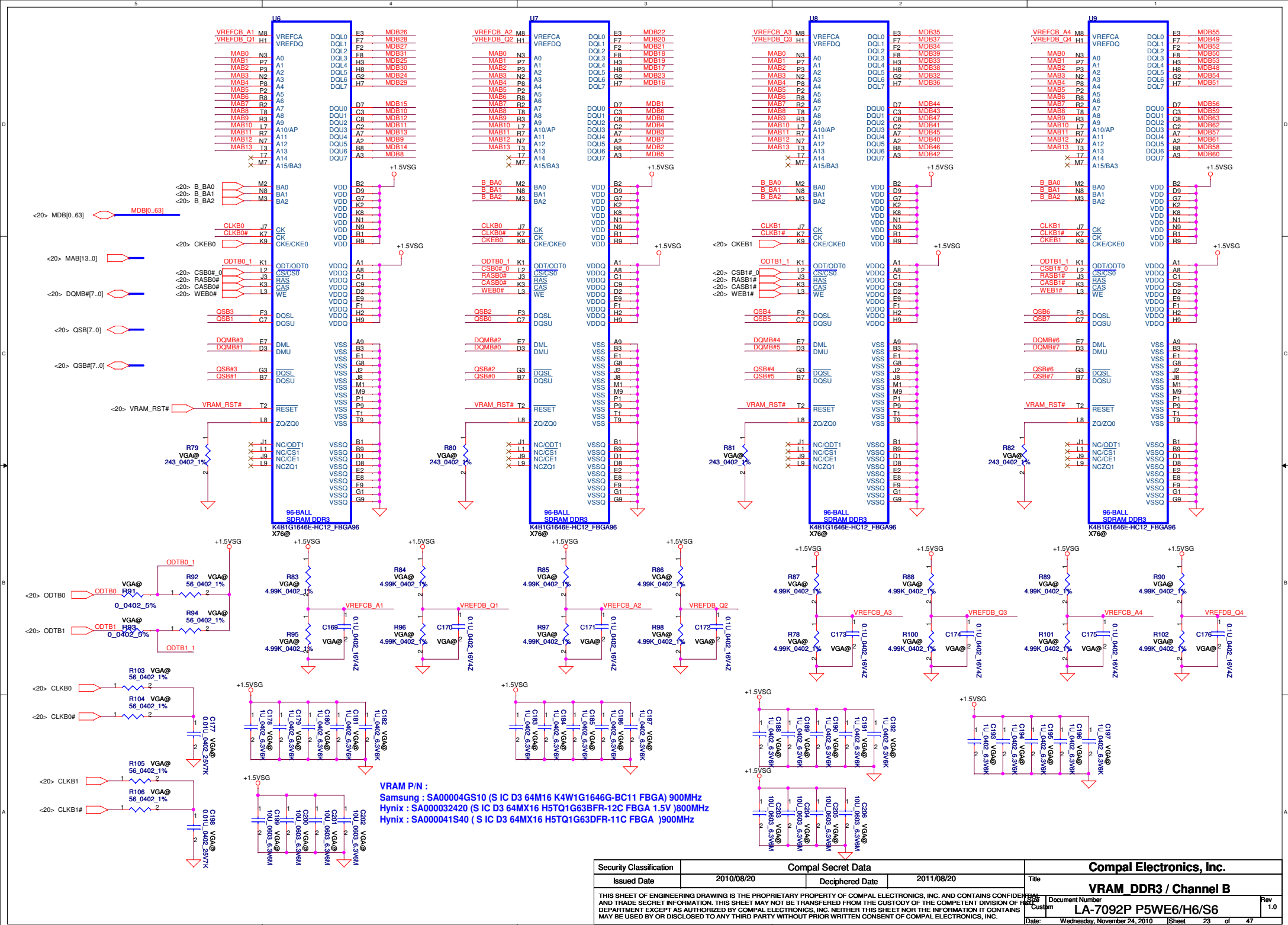
**Don't have this strap on
Whistler and Seymour**

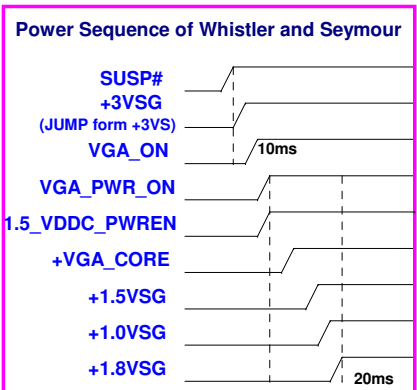
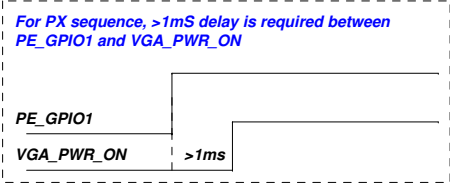
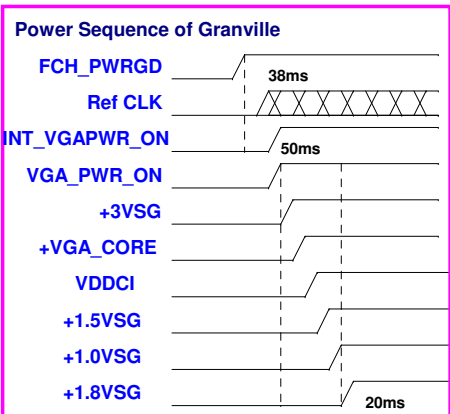


- Internal PD
- PD-Reset



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				Date:	Wednesday, November 24, 2010	Sheet



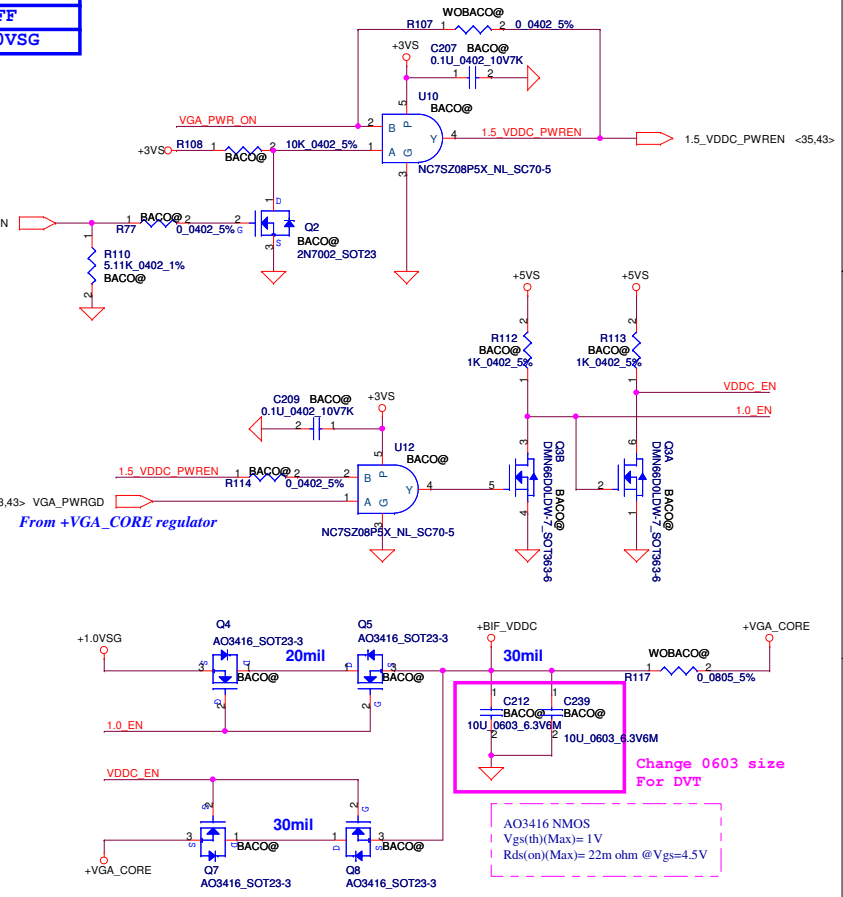
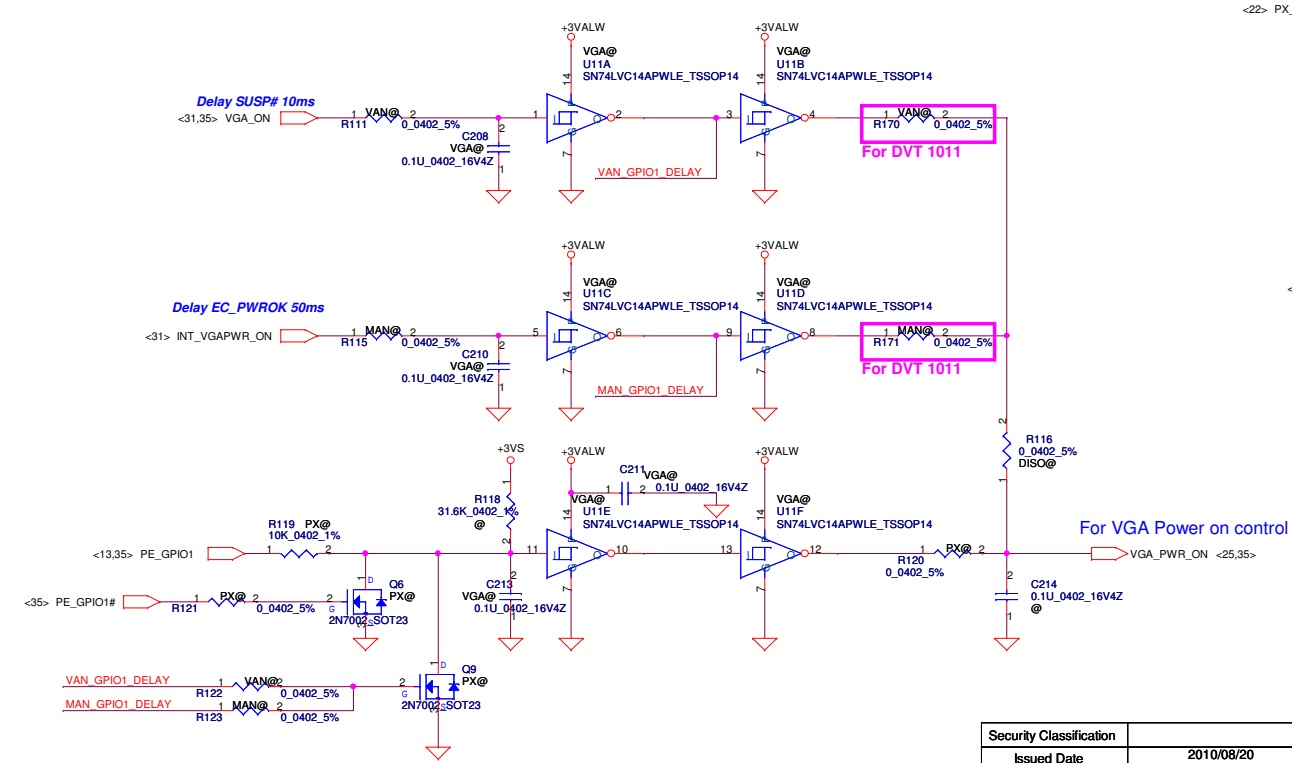


VGA Muxless and Dis only Status Mapping table			
	Dis only	Muxless High performance GPU	Muxless Power-saving GPU
VGA_PWR_ON	1	1	0
1.5_VDDC_PWREN	1	1	0
+3.3VSG	ON	ON	OFF
+1.8VSG	ON	ON	OFF
+1.0VSG	ON	ON	OFF
+VGA_CORE	ON	ON	OFF
+1.5VSG	ON	ON	OFF
+BIF_VDDC	+VGA_CORE	+VGA_CORE	OFF

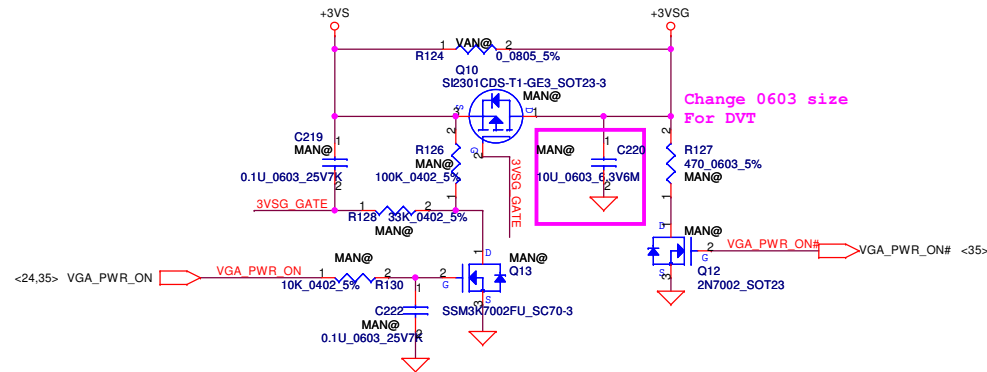
VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table		
	Graville	Whistler and Seymour
VGA_PWR_ON source signal	INT_VGAPWR_ON	VGA_ON
+3.3VSG	VGA_PWR_ON	SUSP#
+1.8VSG	VGA_PWR_ON	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON	VGA_PWR_ON
+VDDCI	VGA_PWR_ON	Combine with +VGA_CORE
+VGA_CORE	VGA_PWR_ON	1.5_VDDC_PWREN
+1.5VSG	VGA_PWR_ON	1.5_VDDC_PWREN

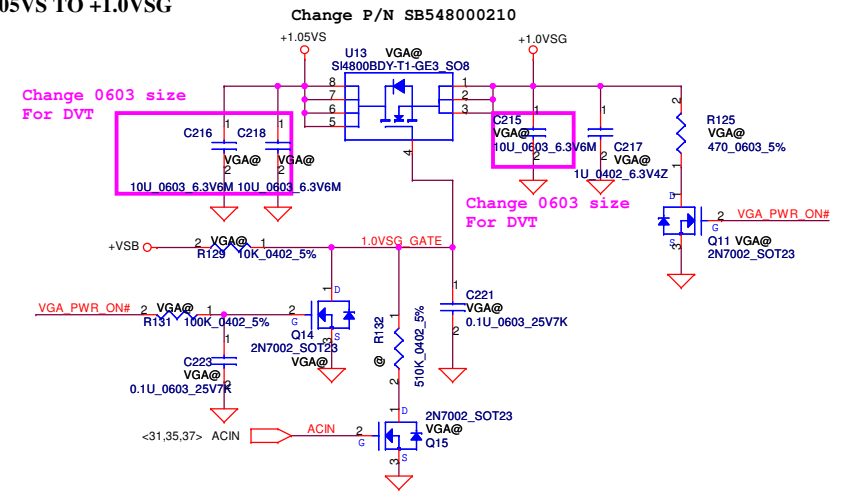
VGA Power ON Circuit



+3.3VS TO +3.3VSG

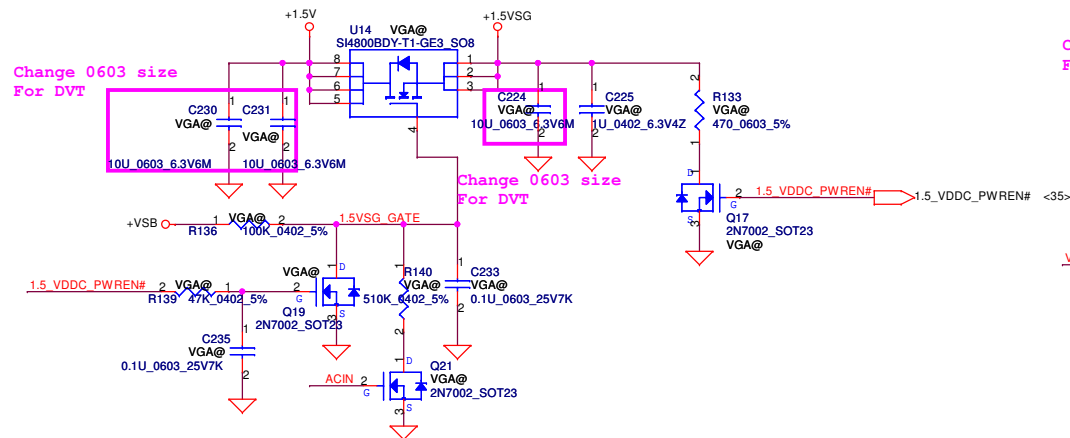


1.05VS TO +1.0VSG



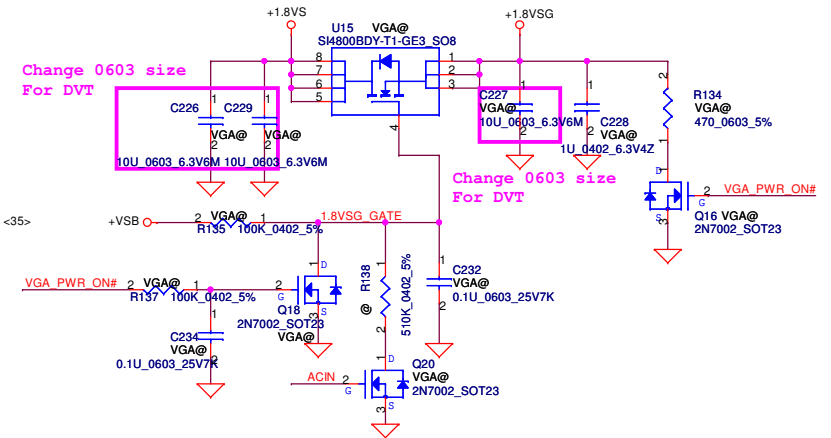
+1.5V TO +1.5VSG

Change P/N SB548000210

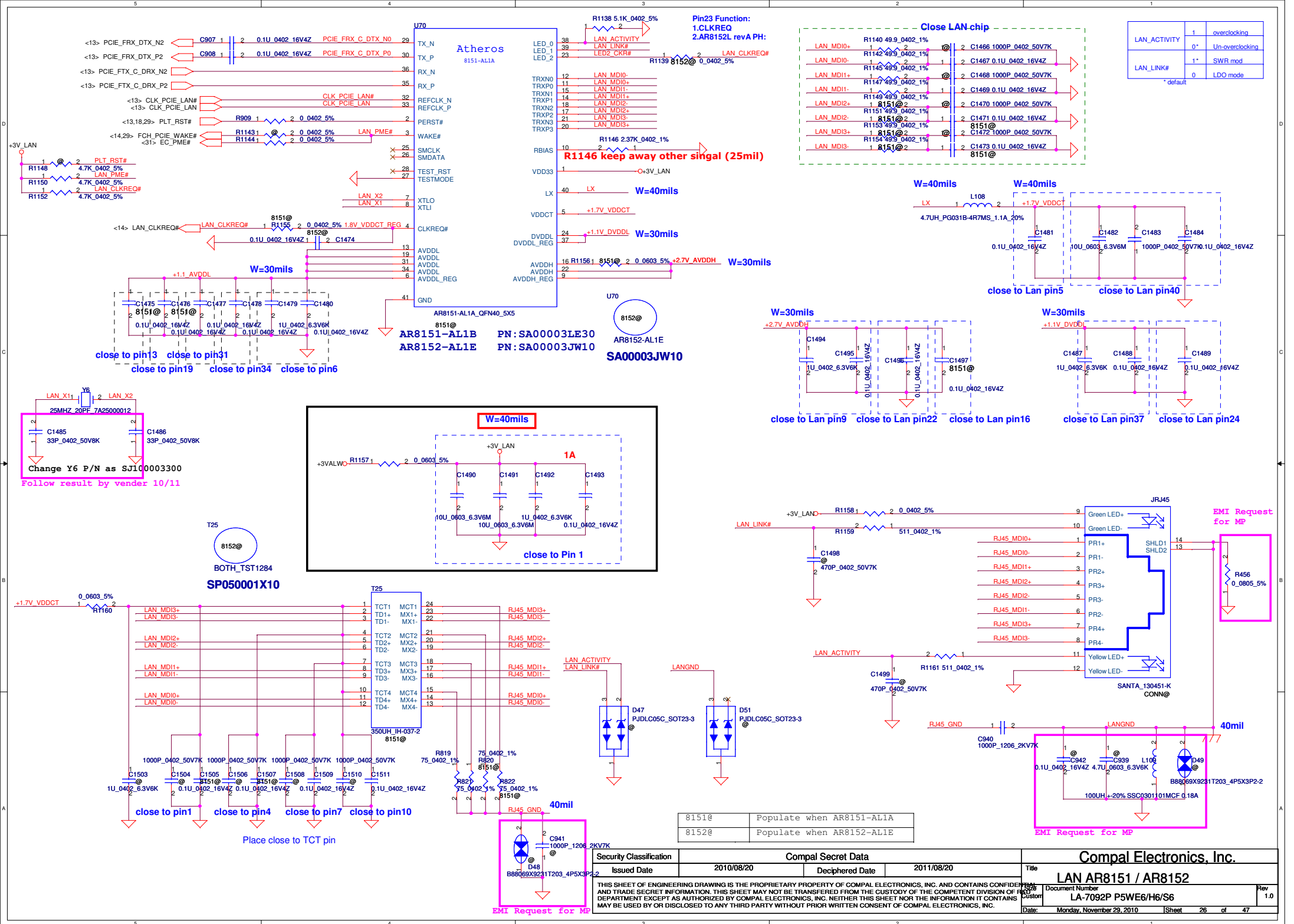


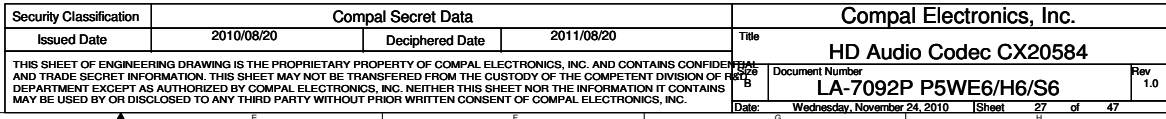
+1.8VS TO +1.8VSG

Change P/N SB548000210

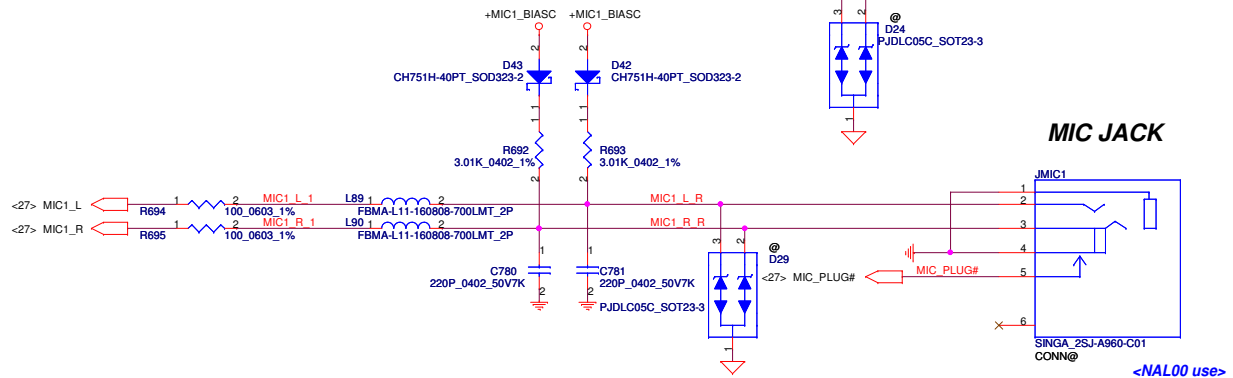
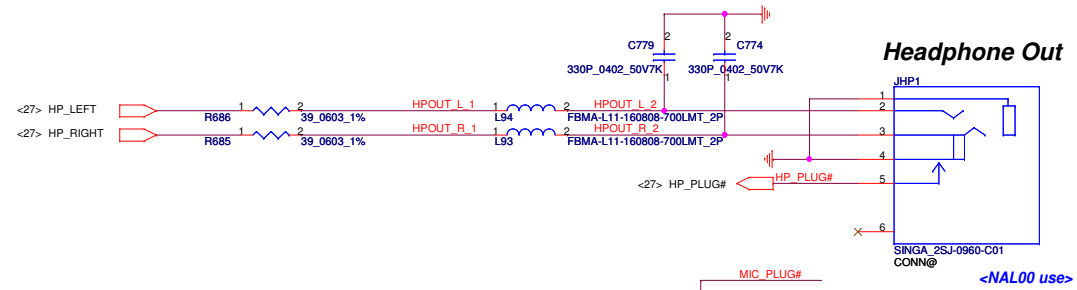
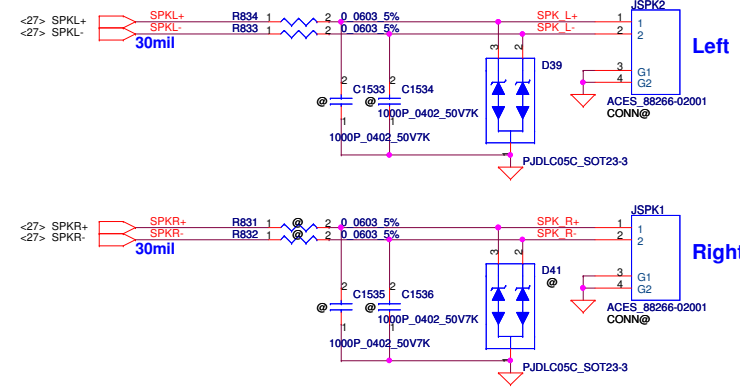


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				Date Monday, November 29, 2010	Sheet 25	of 47



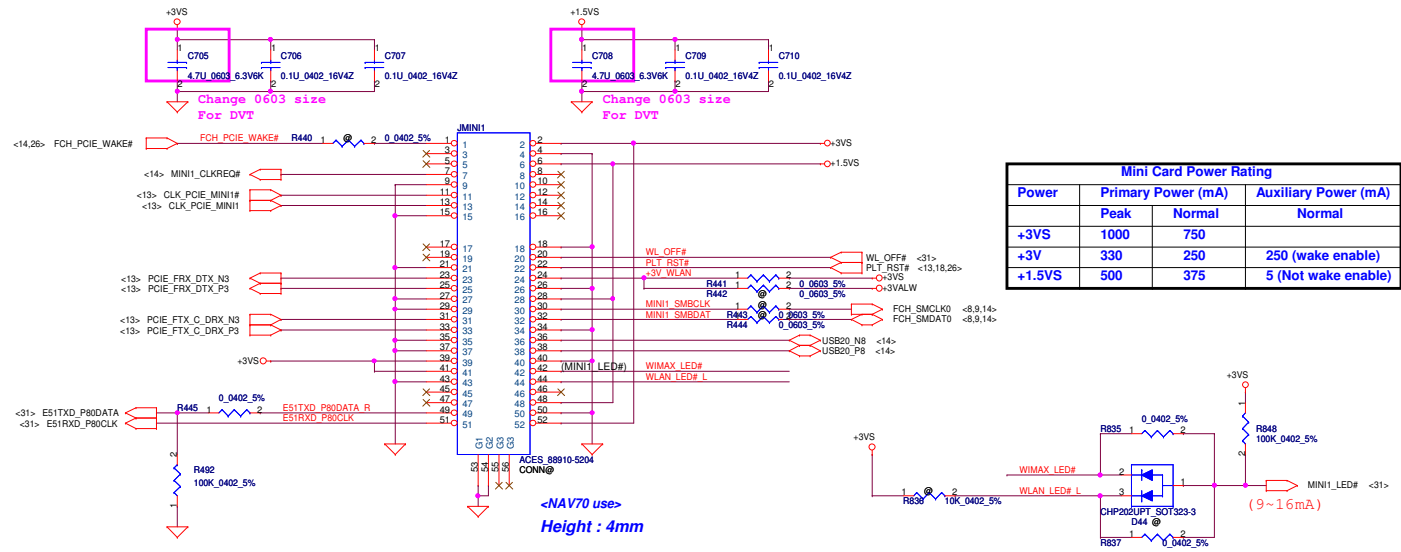


Int. Speaker Conn.



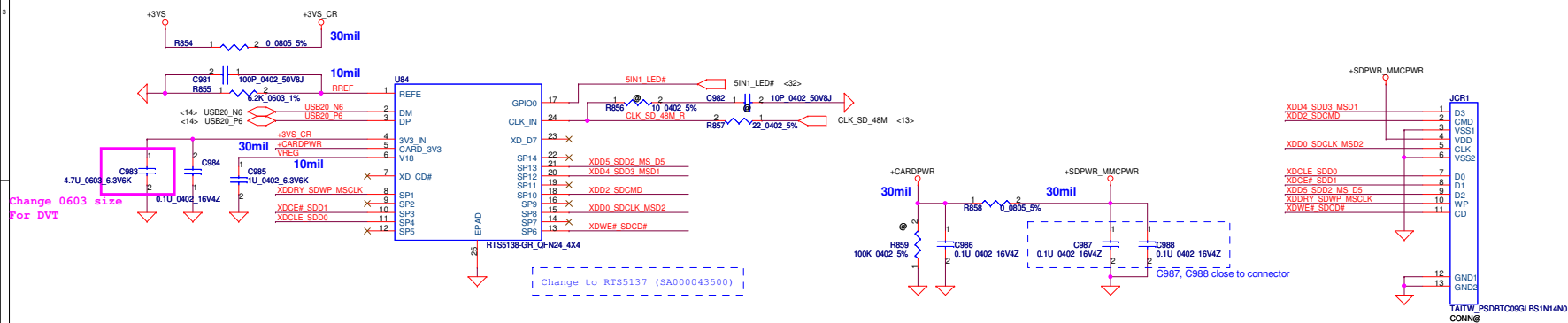
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Issued Date	2010/08/20	Deciphered Date	2011/08/20	Title		
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Mini-Express Card for WLAN

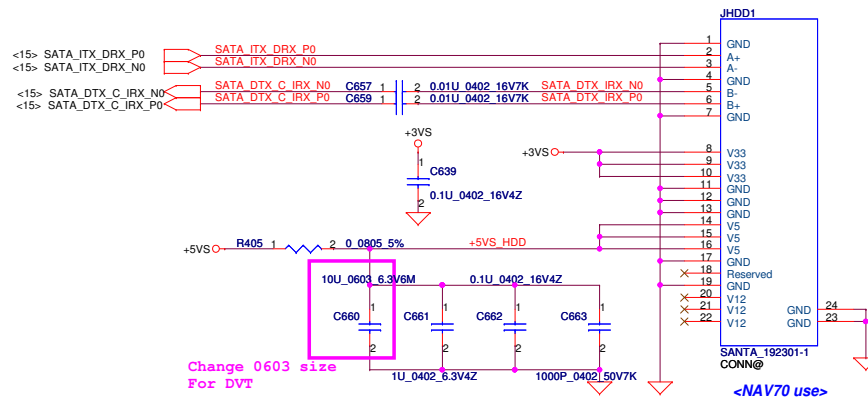


Card Reader RTS5138 / RTS5137
(only SD+MMC function)

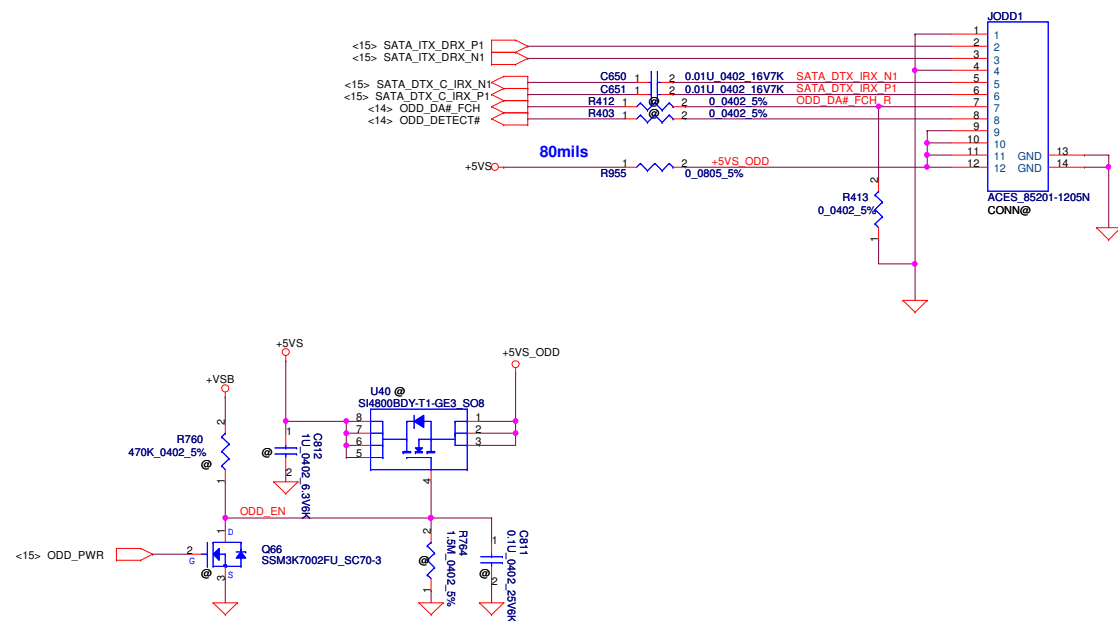
Card Reader Connector



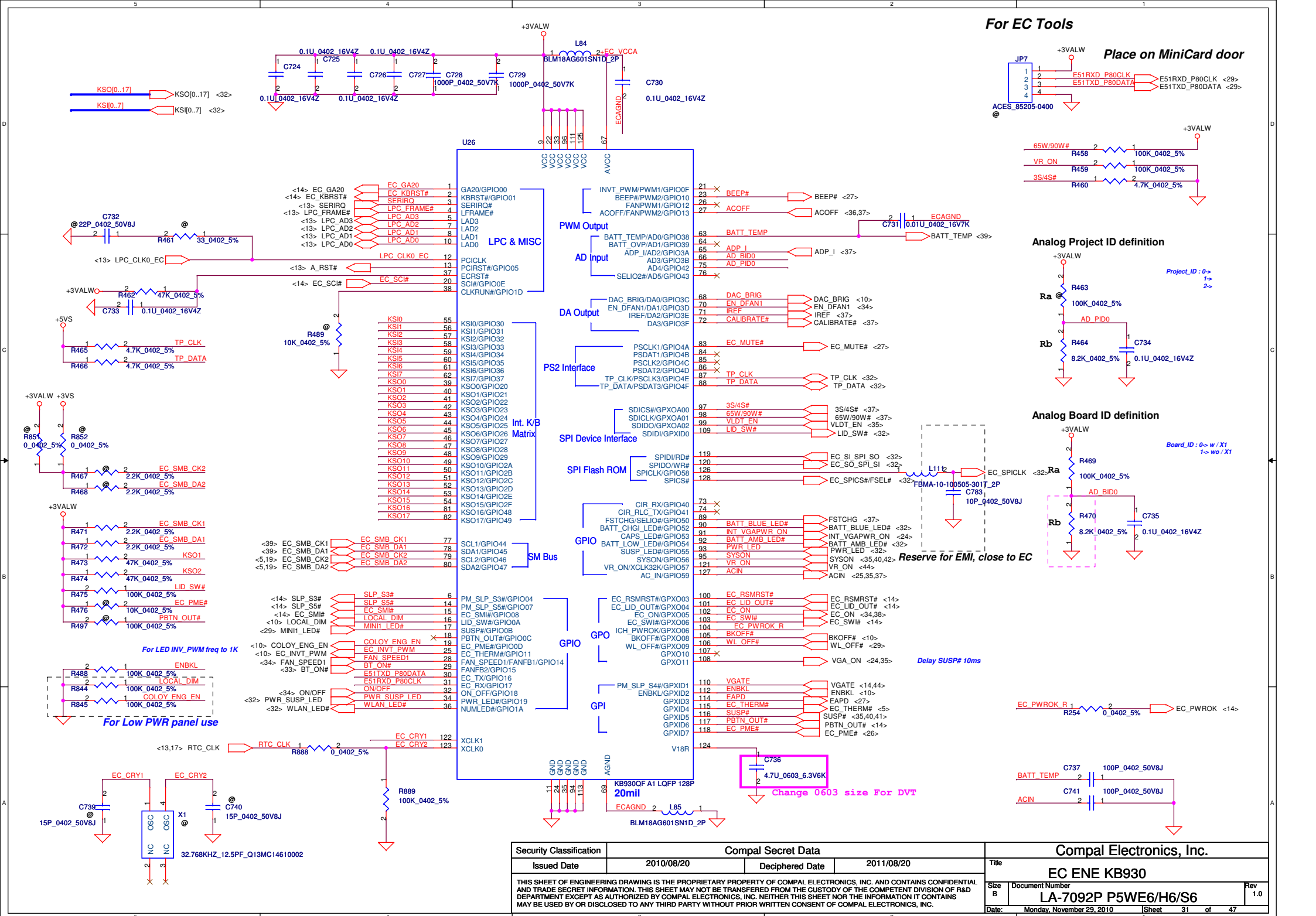
SATA HDD Conn.



SATA ODD FFC Conn.



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				LA-7092P P5WE6/H6/S6	
				Date	Wednesday, November 24, 2010



For EC Tools

Place on MiniCard door

Analog Project ID definition

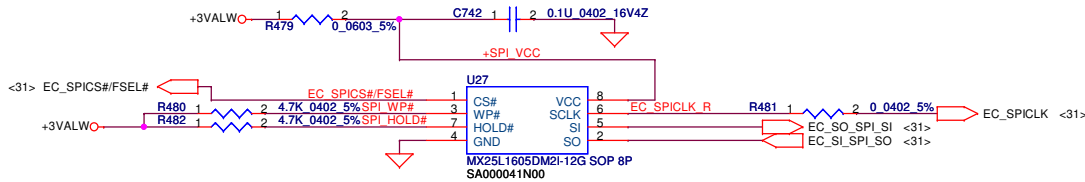
Analog Board ID definition

Reserve for EMI, close to EC

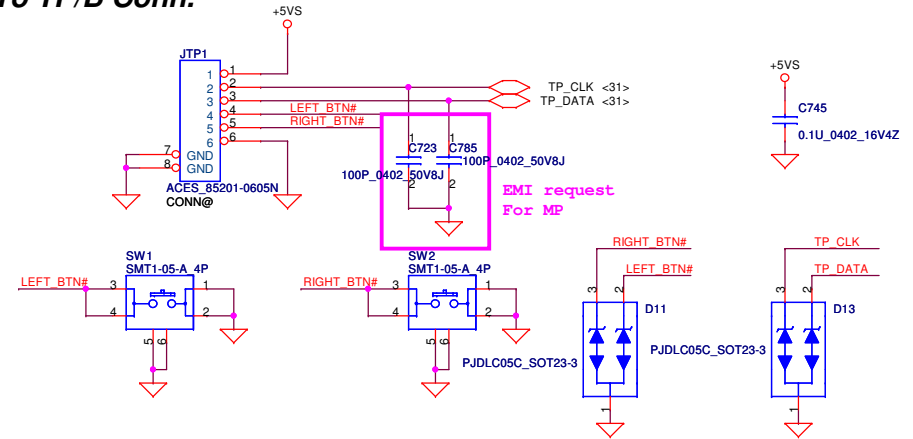
Delay SUSP# 10ms

Change 0603 size For DVT

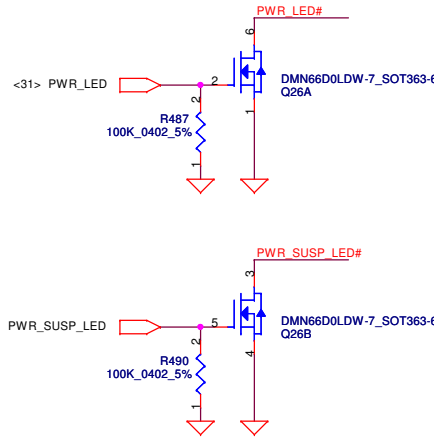
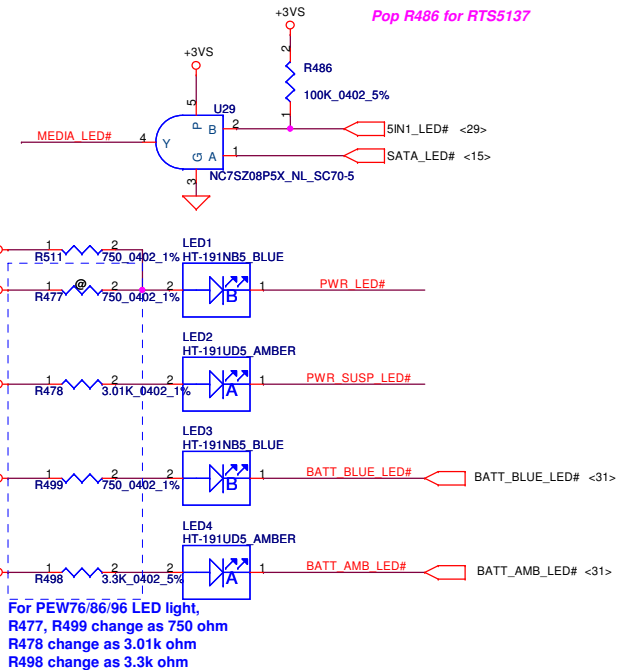
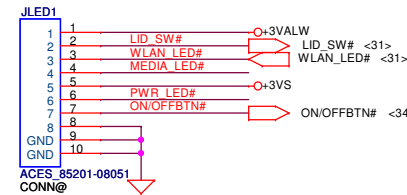
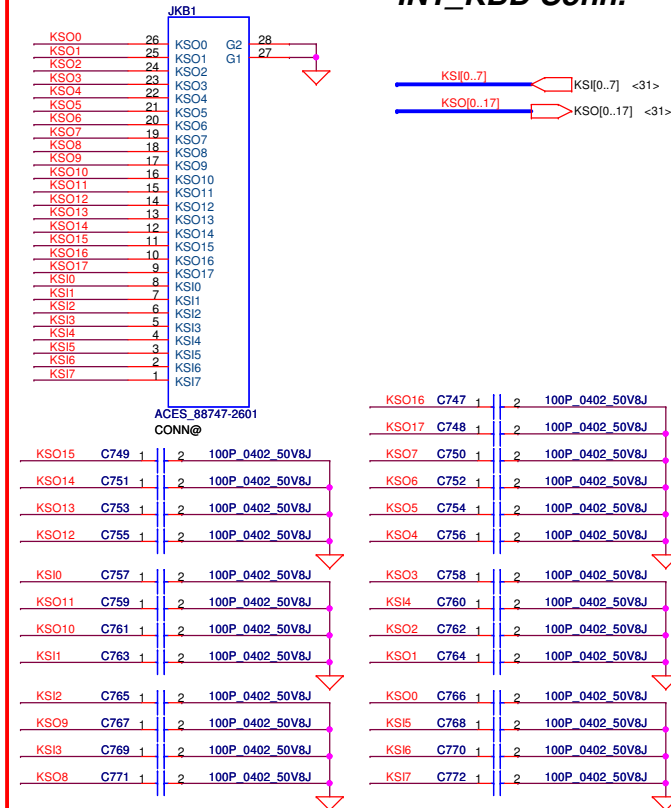
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Issued Date		2010/08/20		Deciphered Date		2011/08/20		Title	
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								Size	Document Number
								B	LA-7092P P5WE6/H6/S6
								Date:	Monday, November 29, 2010



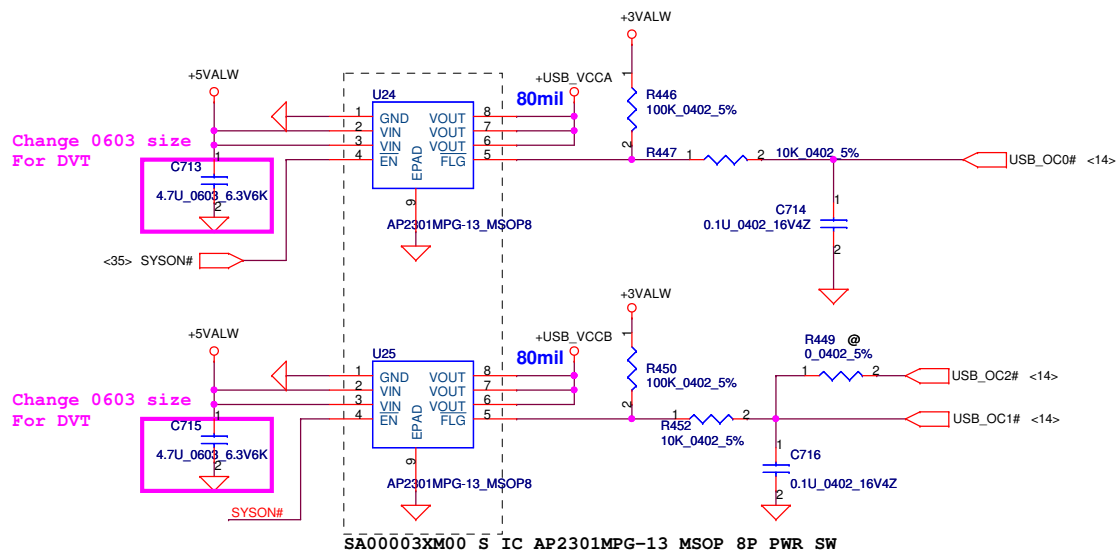
To TP/B Conn.



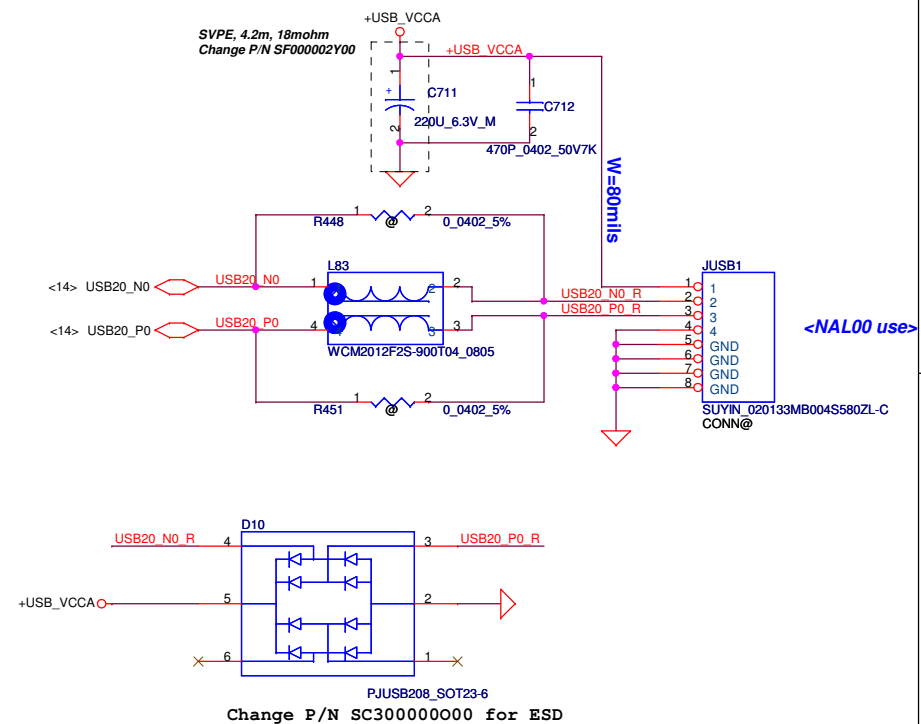
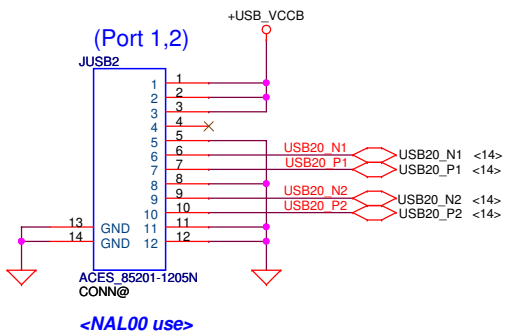
INT_KBD Conn.



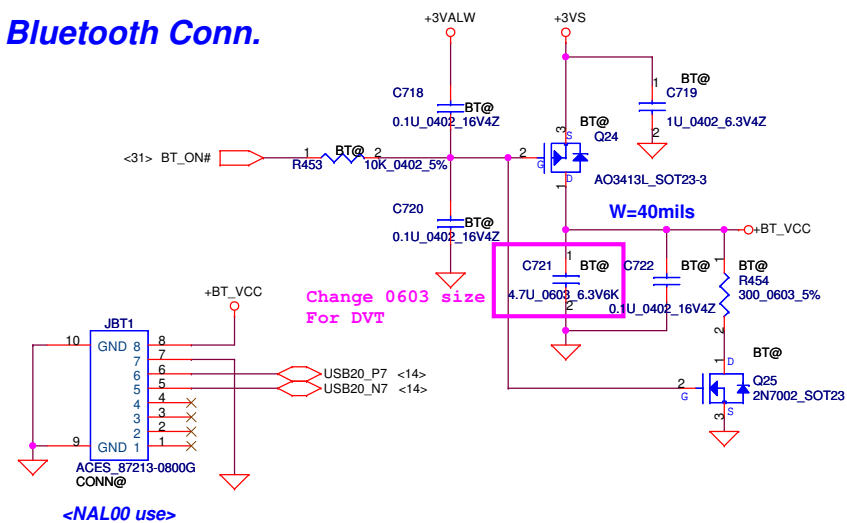
Security Classification		Compal Secret Data		Title	
Issued Date	2010/08/20	Deciphered Date	2011/08/20	KB/TP/LED/SPI ROM/PWRb	
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				LA-7092P P5WE6/H6/S6	
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To USB/B Connector

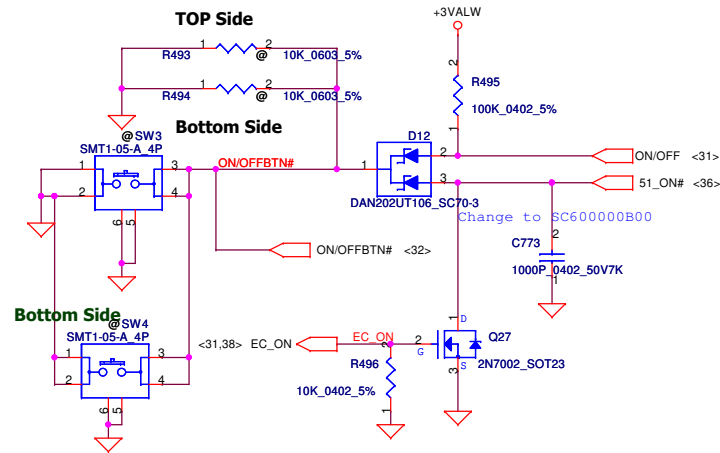


Bluetooth Conn.

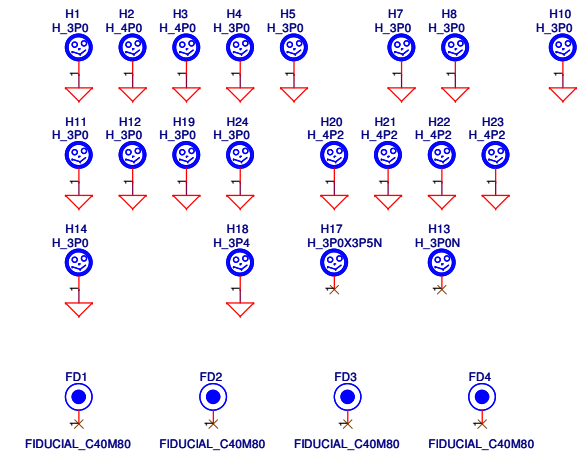
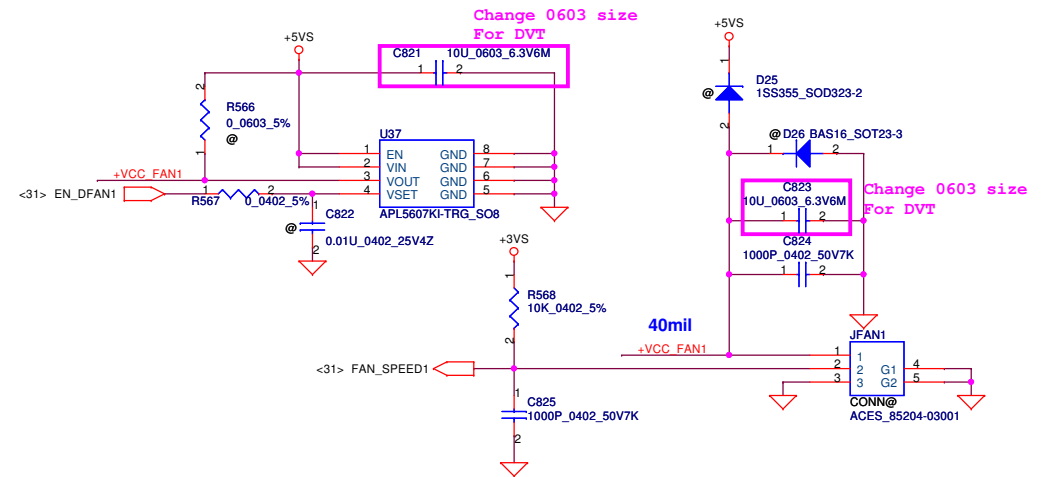


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				Date	Monday, November 29, 2010
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				Rev	1.0

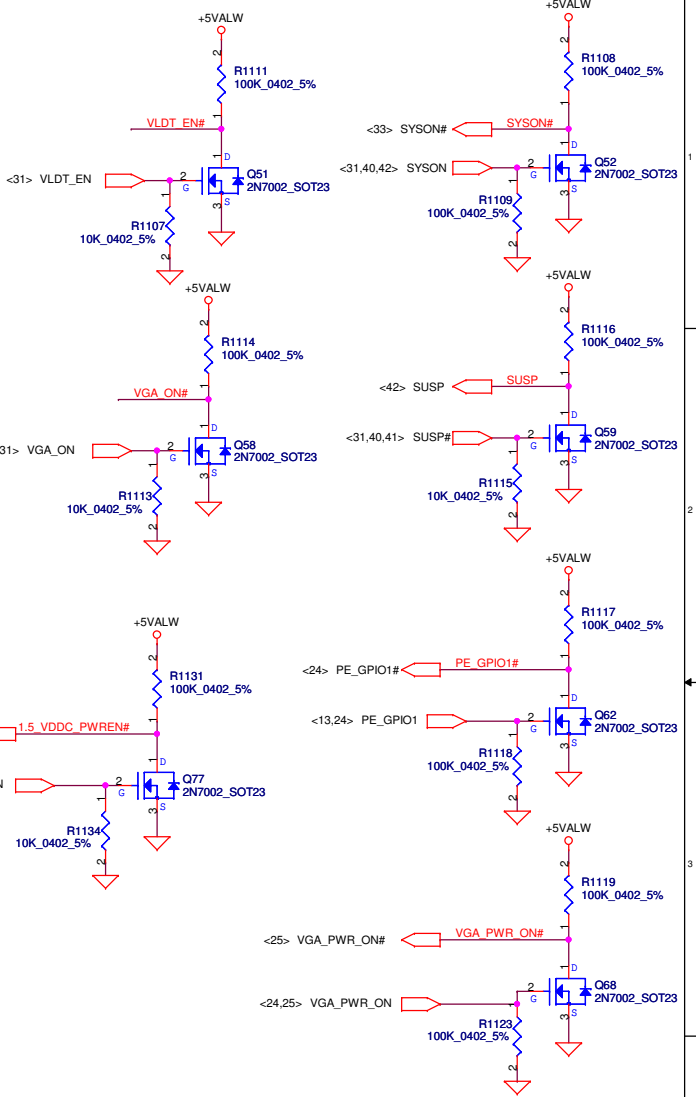
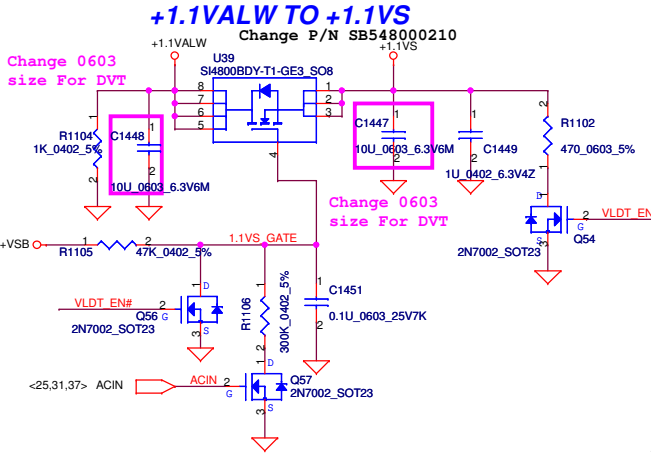
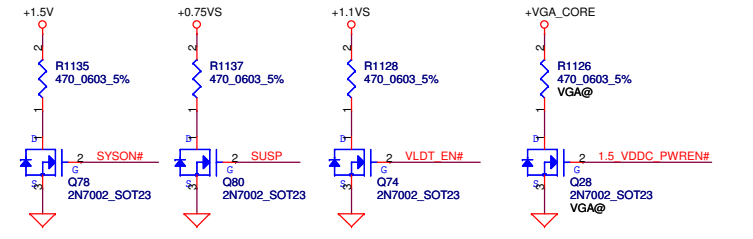
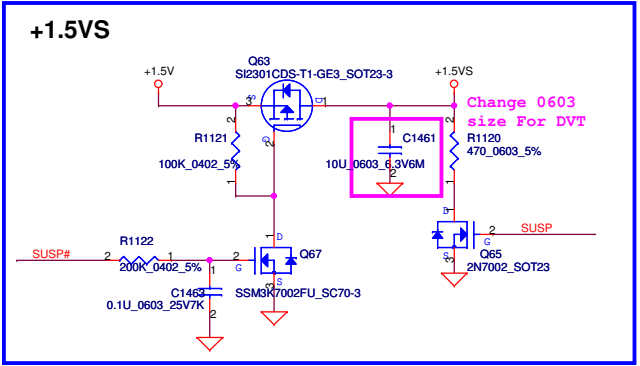
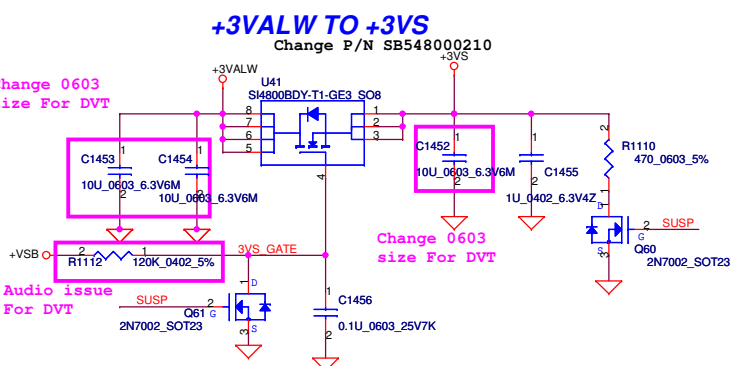
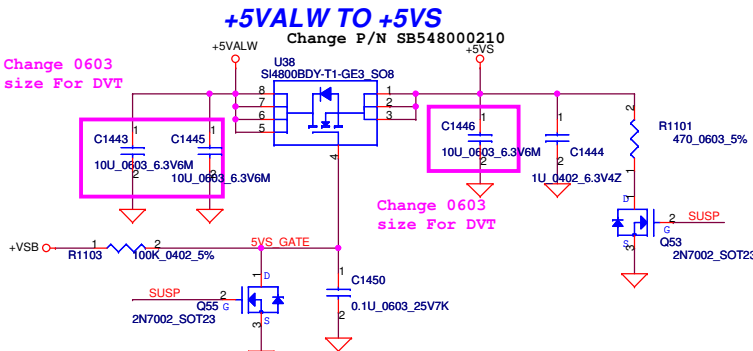
ON/OFF switch *Power Button*



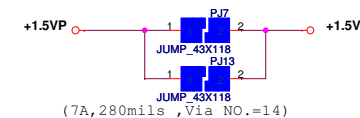
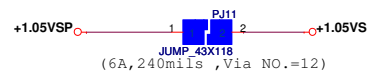
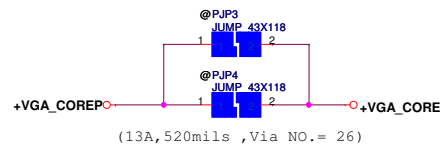
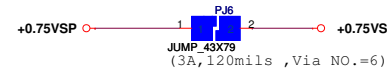
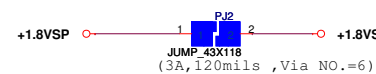
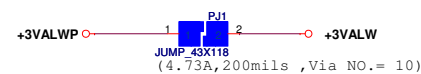
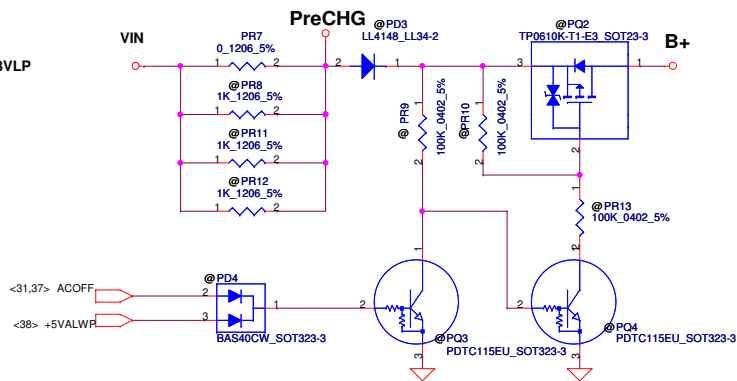
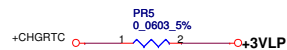
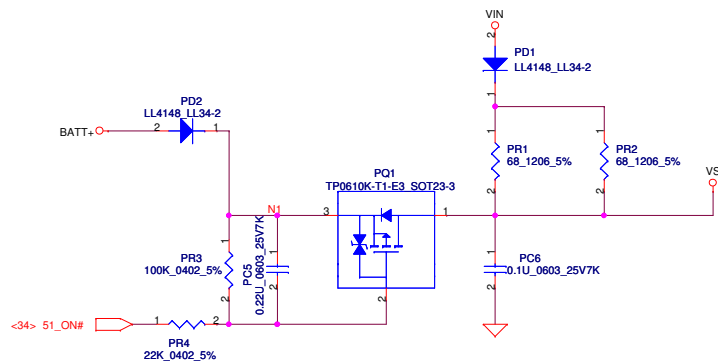
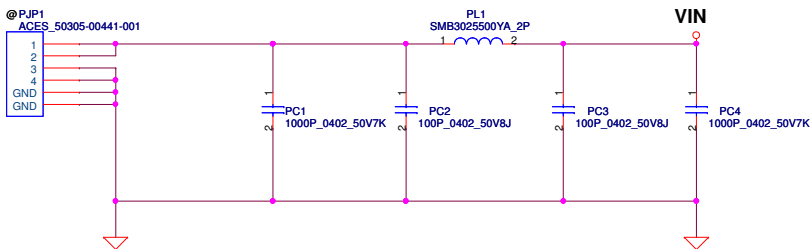
FAN1 Conn



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Issued Date	2010/08/20	Deciphered Date	2011/08/20	Title	Other IO/USB (right)	
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					LA-7092P P5WE6/H6/S6	1.0
				Date: Wednesday, November 24, 2010	Sheet 34 of 47	



Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2010/08/20		Deciphered Date		2011/08/20		Title			
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						Size		Document Number		Rev	
						Custom		LA-7092P P5WE6/H6/S6		1.0	
						Date:		Monday, November 29, 2010		Sheet 35 of 47	



Security Classification	Compal Secret Data			Title	
Issued Date	2010/07/13	Deciphered Date	2011/07/13	PWR DCIN / Pre-charge	
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				P5WE0 M/B LA-6901P Schematic	0.1
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$$CP = 85\% \cdot I_{ada} ; CP = 4.07A$$

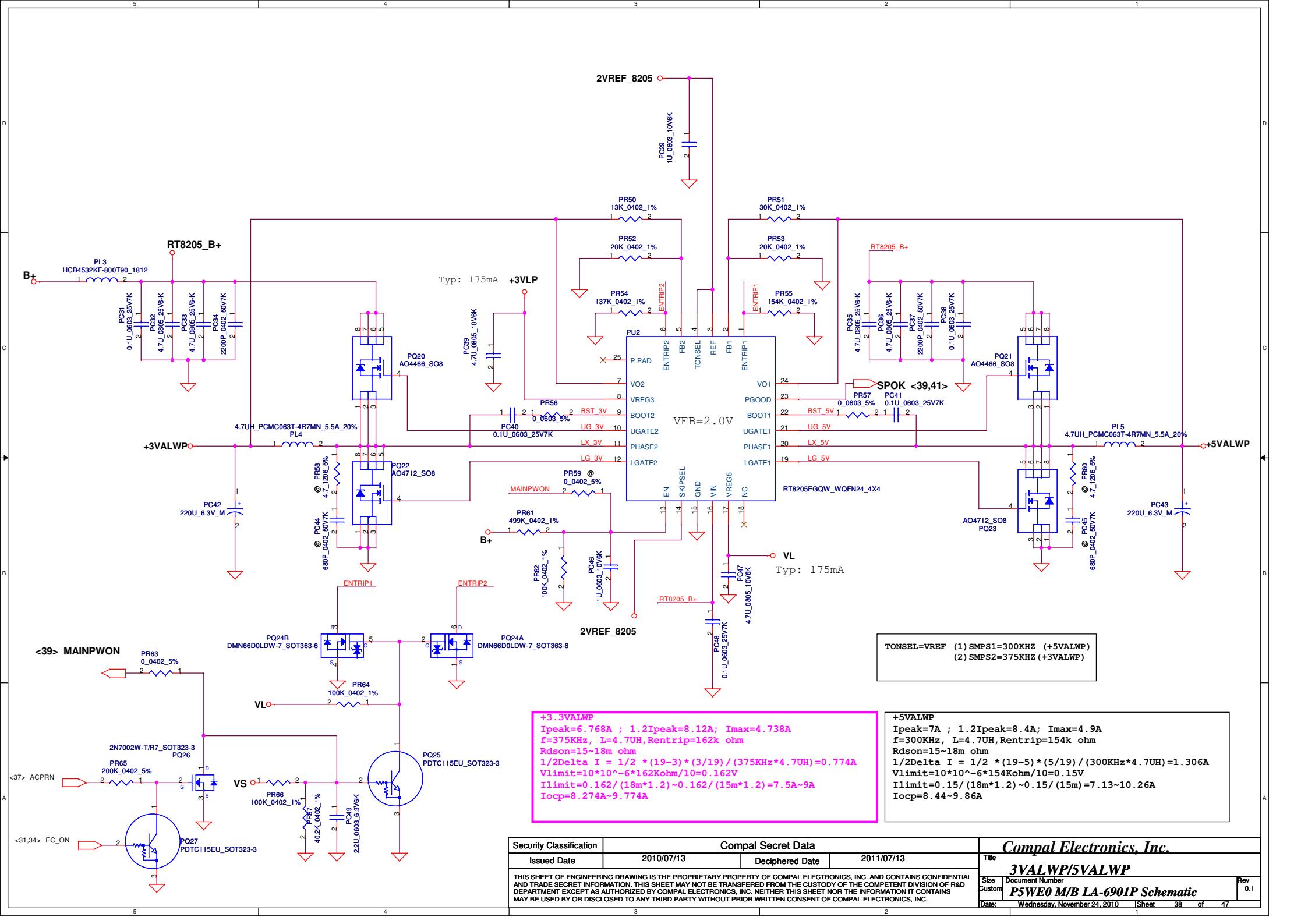
$I_{input} = (1/0.02) (0.05 \cdot V_{ac1m} / 2.39 + 0.05)$
where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

BATT Type	Charging Voltage (0x15)	CV mode	CC=0.6~4.48A IREF=0.7224*Icharge
Normal 3S LI-ON Cells	12600mV	12.60V	IREF=0.43V~3.24V

```
Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichange=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichange =>Ki=0.7224
```

```
Kv
Rinternal Ec=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99v =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.493=CALIBRATE/0.6046 =>CALIBRATE=1.89
1.89=(4.2-(Vcell/A*0.175))*KvKv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451
```

Security Classification		Compal Secret Data		Compal Electronics, Inc. PWR-CHARGER	
Issued Date	2010/07/13	Deciphered Date	2011/07/13	Title	P5WE0 M/B LA-6901P Schematic
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				Date:	Wednesday, November 24, 2010 Sheet 37 of 47

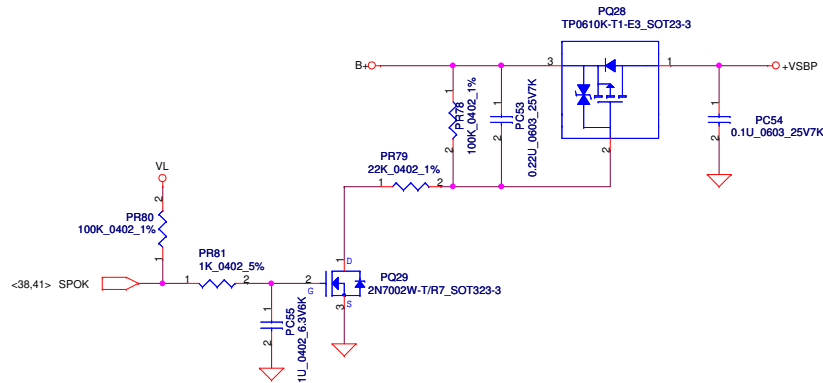
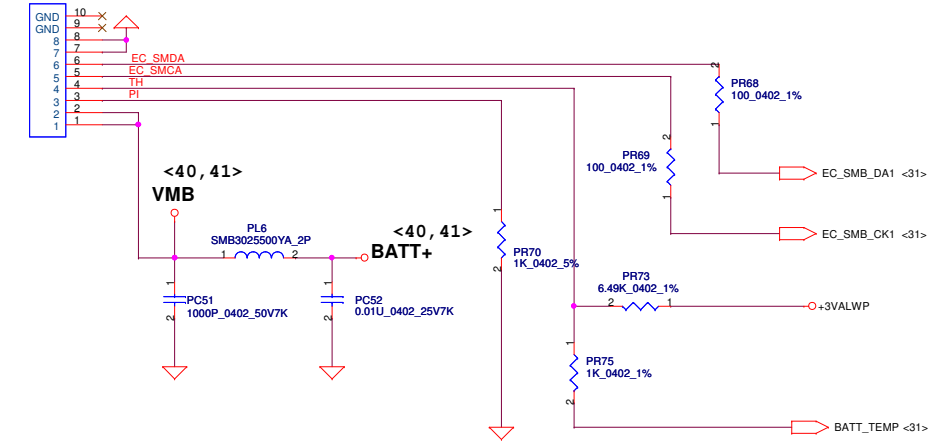


+3.3VALWP
Ipeak=6.768A ; 1.2Ipeak=8.12A; Imax=4.738A
f=375KHz, L=4.7UH, Rentrrip=162k ohm
Rdson=15~18m ohm
 $1/2\Delta I = 1/2 * (19-3) * (3/19) / (375KHz * 4.7UH) = 0.774A$
Vlimit=10*10^-6*154Kohm/10=0.162V
Ilimit=0.162/(18m*1.2)~0.162/(15m*1.2)=7.5A~9A
Iocp=8.274A~9.774A

+5VALWP
Ipeak=7A ; 1.2Ipeak=8.4A; Imax=4.9A
f=300KHz, L=4.7UH, Rentrrip=154k ohm
Rdson=15~18m ohm
 $1/2\Delta I = 1/2 * (19-5) * (5/19) / (300KHz * 4.7UH) = 1.306A$
Vlimit=10*10^-6*154Kohm/10=0.15V
Ilimit=0.15/(18m*1.2)~0.15/(15m)=7.13~10.26A
Iocp=8.44~9.86A

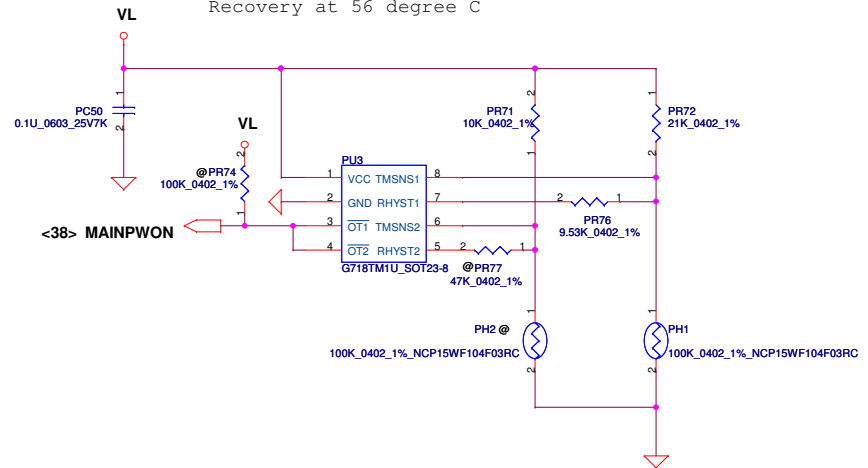
TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
(2) SMPS2=375KHZ (+3VALWP)

PJP2
SUYIN_200275GR008G13GZR

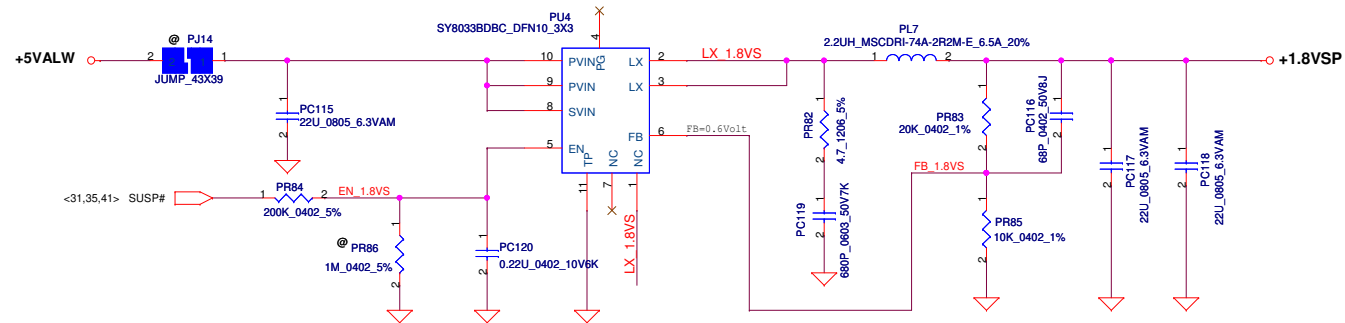


PH1 under CPU botten side :

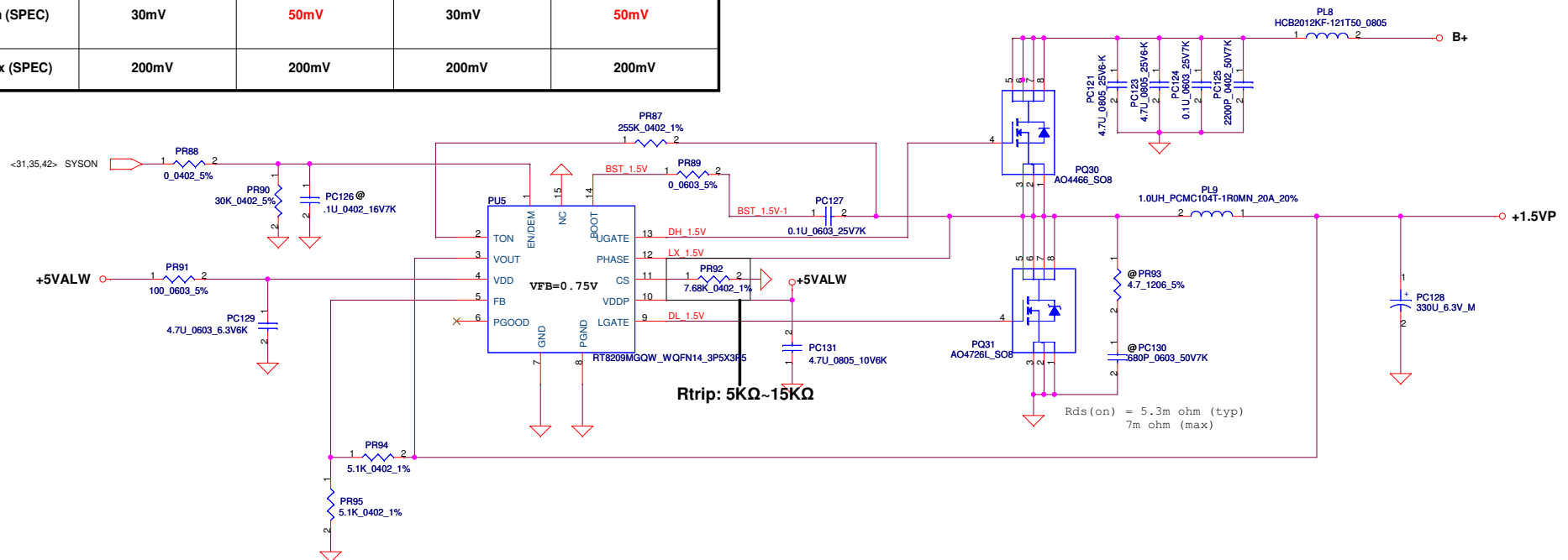
CPU thermal protection at 92 degree C
Recovery at 56 degree C



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/07/13	Deciphered Date	2011/07/13	Title	PWR-BATTERY CONN/OTP
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				Date	Wednesday, November 24, 2010
				Sheet	39 of 47
				Rev	0.1

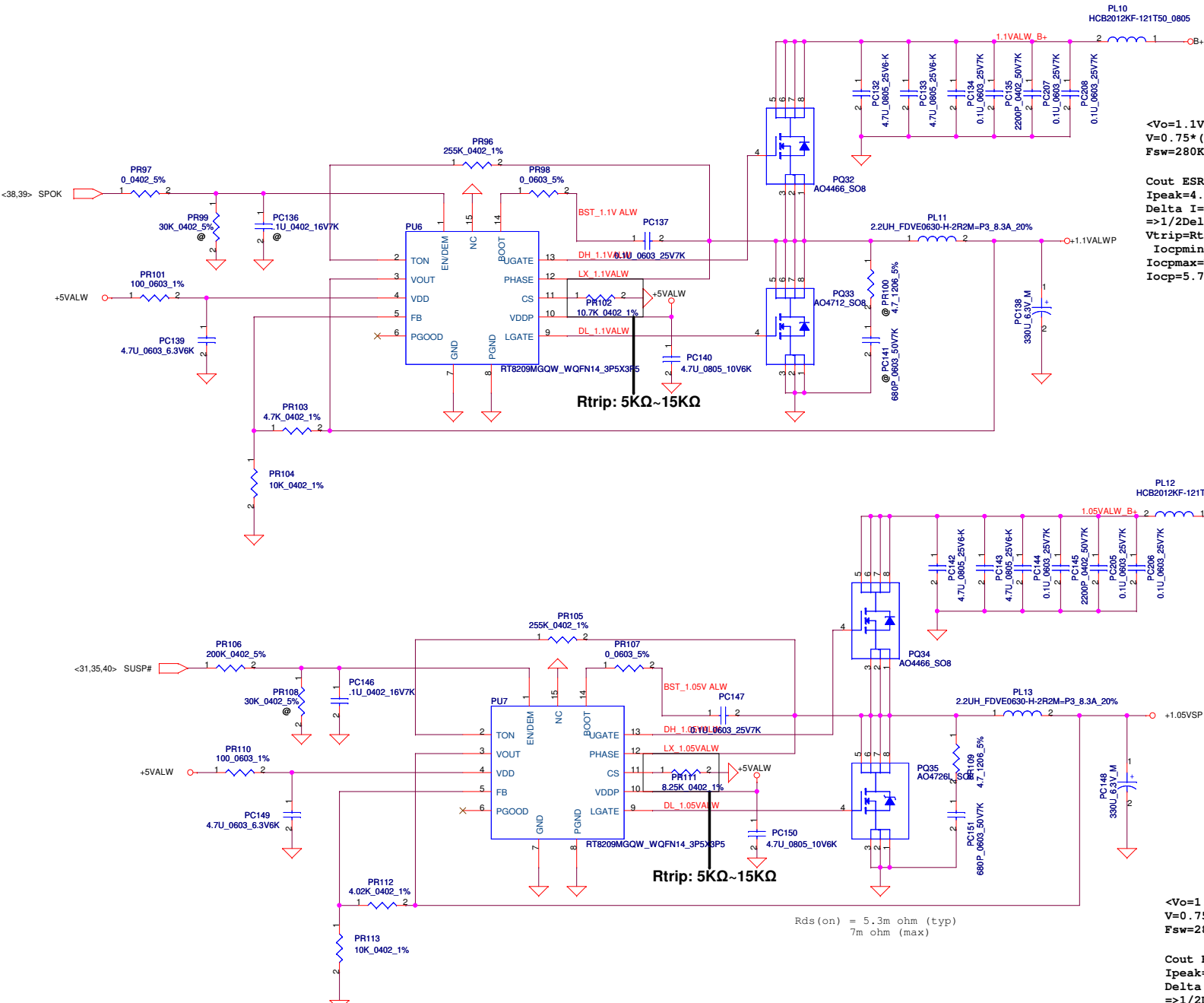


	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/°C	1600ppm/°C	4500ppm/°C	4800ppm/°C
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV



$V_o = 1.5V$ $V_{FB} = 0.75V$
 $V_o = 0.75 * (1 + 10K/10K) = 1.5V$
 $F_{sw} = 280KHz$
 $C_{out} ESR = 17 \text{ mohm}$ $R_{ds(on)}(max) = 7 \text{ mohm}$ $R_{ds(on)}(typ) = 5.3 \text{ mohm}$
 $I_{peak} = 9.45A$, $I_{max} = 6.615A$
 $\Delta I = ((19 - 1.5) * (1.5/19)) / (L * F_{sw}) = 4.93A$
 $\Rightarrow 1/2 \Delta I = 2.467A$
 $V_{trip} = R_{trip} * I_{out} = 0.0768$
 $I_{ocpmin} = V_{trip} / (R_{ds(on)}(max) * 1.2) + \Delta I / 2 = 11.61A$
 $I_{ocpmax} = V_{trip} / (R_{ds(on)}(typ) * 1.2) + \Delta I / 2 = 14.54A$
 $I_{ocp} = 11.61A \sim 14.54A$

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/01/25	Deciphered Date	2009/04/28	Title	1.8VSP/1.5VSP	
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<Vo=1.1V> VFB=0.75V
V=0.75*(1+4.7K/10K)=1.1V
Fsw=280KHz

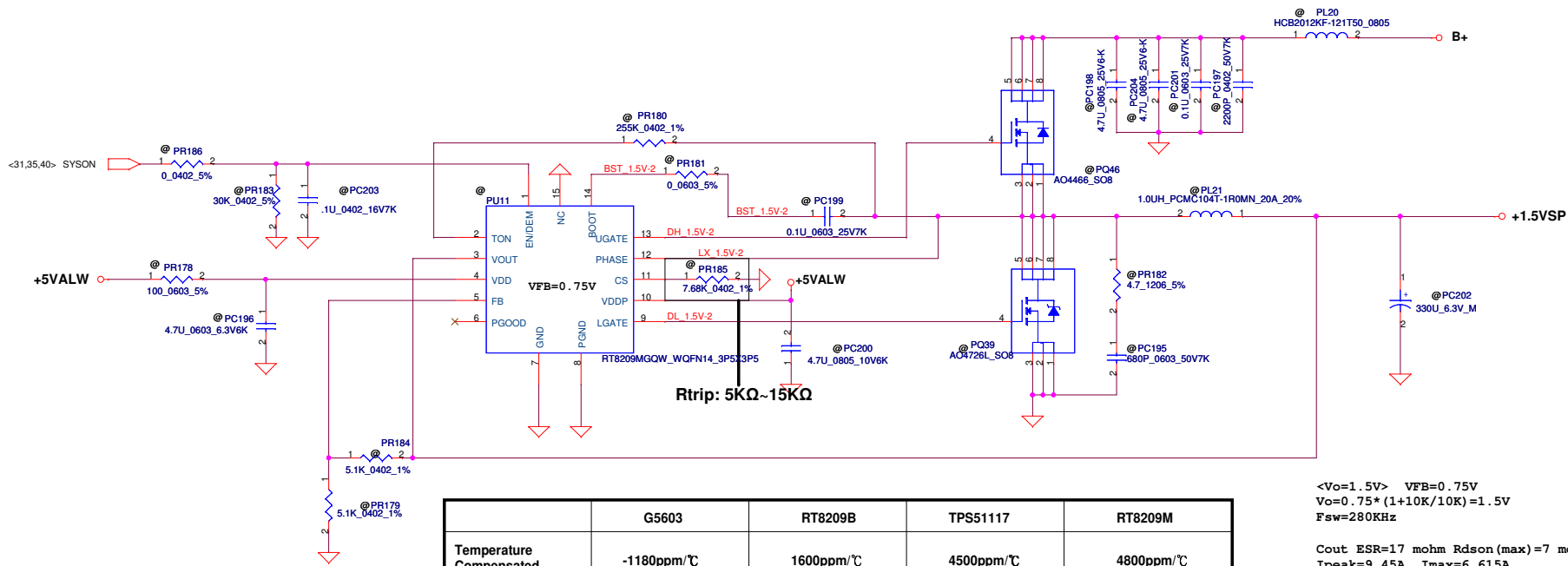
Cout ESR=17 mohm Rds(on)(max)=18 mohm Rds(on)(typ)=15 mohm
Ipeak=4.5A, Imax=3.15A
Delta I=((19-1.1)*(1.1/19))/(L*Fsw)=1.68A
=>1/2Delta I=0.84A
Vtrip=Rtrip*10uA=0.107
Iocpmin=Vtrip/(Rds(on)(max)*1.2)+Delta I/2=5.79A
Iocpmax=Vtrip/(Rds(on)(typ)*1.2)+Delta I/2=6.78A
Iocp=5.79A~6.78A

<Vo=1.05V> VFB=0.75V
V=0.75*(1+4.02K/10K)=1.05V
Fsw=280KHz

Cout ESR=17 mohm Rds(on)(max)=7 mohm Rds(on)(typ)=5.3 mohm
Ipeak=8.7A, Imax=6.09A
Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=1.61A
=>1/2Delta I=0.81A
Vtrip=Rtrip*10uA=0.0825
Iocpmin=Vtrip/(Rds(on)(max)*1.2)+Delta I/2=10.63A
Iocpmax=Vtrip/(Rds(on)(typ)*1.2)+Delta I/2=13.78A
Iocp=10.63A~13.78A

	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/°C	1600ppm/°C	4500ppm/°C	4800ppm/°C
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV

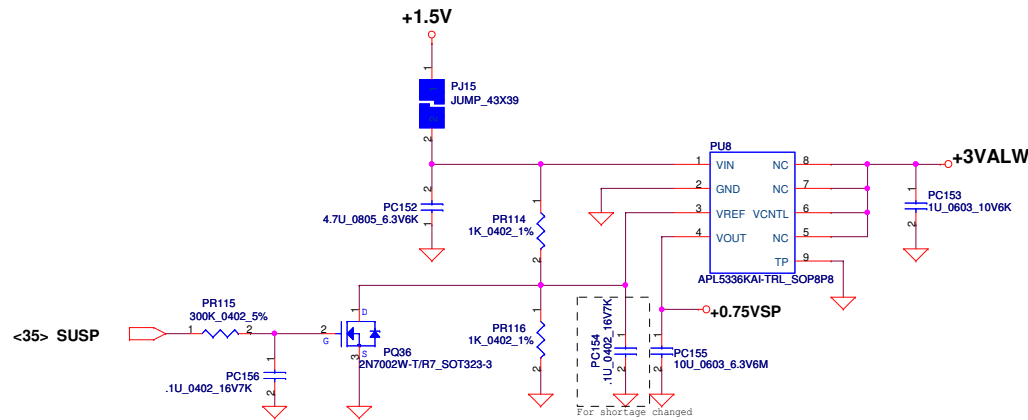
Security Classification		Compal Secret Data				Compal Electronics, Inc.				
Issued Date		2010/01/25		Deciphered Date		2009/04/28		Title		
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								Size	Document Number	Rev
								Custom		0.1
								Date:	Wednesday, November 24, 2010	Sheet

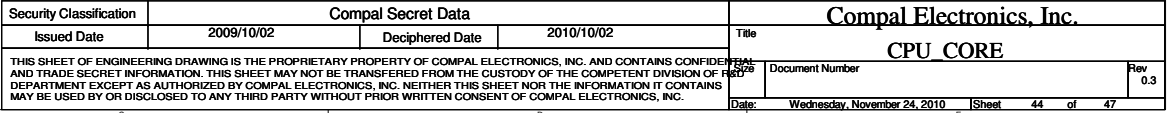


	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/°C	1600ppm/°C	4500ppm/°C	4800ppm/°C
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV

<Vo=1.5V> VFB=0.75V
Vo=0.75*(1+10K/10K)=1.5V
Fsw=280KHz

Cout ESR=17 mohm Rds(on)=7 mohm Rds(on)(typ)=5.3 mohm
Ipeak=9.45A, Imax=6.615A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=4.93A
=>1/2Delta I=2.467A
Vtrip=Rtrip*10uA=0.0768
Iocpmin=Vtrip/(Rds(on)(max)*1.2)+Delta I/2=11.61A
Iocpmax=Vtrip/(Rds(on)(typ)*1.2)+Delta I/2=14.54A
Iocp=11.61A~14.54A





Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	0.75VSP EN RC value	HW adjust timing	0.1	42	Change PR115 from SD028000080 to SD028300380(S RES 1/16W 300K +-5% 0402) Add PC156 SE076104K80(S CER CAP .1U 16V K X7R 0402)	2010/09/24	DVT
2	1.8VSP EN RC value	HW adjust timing	0.1	40	Change PR84 from SD028000080 to SD028200380(S RES 1/16W 200K +-5% 0402) Add PC120 SE095224K00(S CER CAP 0.22U 10V K X5R 0402)	2010/09/24	DVT
3	1.05VSP EN RC value	HW adjust timing	0.1	41	Change PR106 from SD028000080 to SD028200380(S RES 1/16W 200K +-5% 0402) Add PC146 SE076104K80(S CER CAP .1U 16V K X7R 0402)	2010/09/24	DVT
4	VGA_COREP EN RC value	HW adjust timing	0.1	43	Change PR123 from SD034100280 to SD034200280(S RES 1/16W 20K +-1% 0402)	2010/09/24	DVT
5	change BOM structure	1.5VSP change BOM structure to VGA@ for cost down of UMA	0.1	42	Change PU11, PL21, PQ39, PQ46, PR178, PR179, PR180, PR181, PR184, PR185, PR186, PC196, PC197, PC198, PC199, PC200, PC201, PC202, PC204 BOM structure to VGA@ del PL20 SM01000C000(S SUPPRE_ TAI-TECH HCB2012KF-121T50 0805)	2010/10/05	DVT
6	Adjust APU_CORE_NB OCP	Adjust APU_CORE_NB OCP to 15A	0.1	44	Change PR151 from SD034110280 to SD034237280(S RES 1/16W 23.7K +-1% 0402)	2010/10/07	DVT
7	Add input choke in charger circuit.	Add input choke for EMI ISN test in charger circuit.	0.1	37	Change PL17 from SM010018710 to SH000000Y00(S COIL 1.2UH +-30% 1231AS-B-1R2N-P3 2.9A)	2010/10/18	DVT
8	Add snubber	Add snubber in APU_COREP and APU_CORE_NB circuit.	0.1	44	Add PR146, PR161 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC180, PC188 SE025681K80(S CER CAP 680P 50V K X7R 0603) Add PR188 SD034220080(S RES 1/16W 220 +-1% 0402)	2010/10/18	DVT
9	Add snubber and input Cup.	Add snubber and input Cup. in 1.05VSP circuit.	0.1	41	Add PR161 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC188 SE025681K80(S CER CAP 680P 50V K X7R 0603) Add PC205, PC206 SE042104K80(S CER CAP .1U 25V K X7R 0603)	2010/10/18	DVT
10	Add input Cup.	Add input Cup. in 1.1VALWP circuit for EMI test.	0.1	41	Add PC207, PC208 SE042104K80(S CER CAP .1U 25V K X7R 0603)	2010/10/18	DVT
11	Add input Cup.	Add input Cup. and H/S gate resistance in CPU_COREP circuit for EMI ISN test.	0.1	44	Add PC209, PC210, PC211, PC212 SE042104K80(S CER CAP .1U 25V K X7R 0603) Add PC57, PC58 SE142106M80(S CER CAP 10U 25V N X5R 1206 H1.7) Add PR189, PR190 SD013000080(S RES 1/10W 0 +-5% 0603)	2010/10/19	DVT
12	Adjust VGA_COREP VID value	Adjust VGA_COREP VID value	0.1	43	Change PR128 from SD034100280 to SD034931180(S RES 1/16W 9.31K +-1% 0402) Change PR127 from SD034200280 to SD034154280(S RES 1/16W 15.4K +-1% 0402) Change PR131 from SD000009K00 to SD034301280(S RES 1/16W 30.1K +-1% 0402)	2010/10/21	DVT
13	change BOM structure	1.5VSP change BOM structure to @ for cost down	0.1	42	Change PU11, PL21, PQ39, PQ46, PR178, PR179, PR180, PR181, PR184, PR185, PR186, PC196, PC197, PC198, PC199, PC200, PC201, PC202, PC204 BOM structure to @ del PL20 SM01000C000(S SUPPRE_ TAI-TECH HCB2012KF-121T50 0805)	2010/10/21	DVT
14	change main source	change main source for reduce source	0.1	42	Change PQ36 from SB000009610 to SB000006800(S TR 2N7002W 1/R7 1N SOT-323)	2010/10/26	DVT
15	Adjust VGA_COREP VID timing	Adjust VGA_COREP VID timing to avoid OVP.	0.1	43	Change PR130 from SD028100280 to SD034402280(S RES 1/16W 40.2K +-1% 0402)	2010/11/01	DVT
16	Delete precharge circuit	Delete precharge circuit to avoid adapter UVP.	0.1	36	del PR8, PR11, PR12 SD001100180(S RES 1/4W 1K +-5% 1206) del PD3 SC100001Y80(S DIO LL4148 LL-34 PANJIT) del PR9, PR10, PR13 SD028100380(S RES 1/16W 100K +-5% 0402) change PR7 SD001100180 to SD011000080(S RES 1/4W 0 +-5% 1206)	2010/11/01	DVT

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Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title	PIR (PWR)
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				Document Number	0.1
				PEW96 LA-6552P	
				Date	Monday, November 15, 2010
				Sheet	45 of 47

Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Delete precharge circuit	Delete precharge circuit to avoid adapter UVP.	0.1	36	del PQ2 SB906100210(S TR TP0610K-T1-E3 1P SOT23) del PQ3, PQ4 SB301150200(S TR PDTCT115EU NPN SOT323) del PD4 SCS00001200(S SCH DIO BAS40CW SOT-323)	2010/11/01	DVT
2	Delete precharge 連動 circuit	Delete precharge 連動 circuit to avoid adapter UVP.	0.1	37	change PQ7 SB00000DL00 to SB00000I600(S TR SI4459ADY-T1-GE3 1P SO8)	2010/11/01	DVT
3	Delete precharge 連動 circuit	Delete precharge 連動 circuit to avoid adapter UVP.	0.1	37	del PR21 SD034100380(S RES 1/16W 100K +-1% 0402) del PC17 SE075222K80(S CER CAP 2200P 25V K X7R 0402) del PQ12 SB000006800(S TR 2N7002W T/R7 1N SOT-323)	2010/11/01	DVT
4	Delete precharge 連動 circuit	Delete precharge 連動 circuit to avoid adapter UVP.	0.1	37	Add PR357 SD034200380(S RES 1/16W 200K +-1% 0402) add PC253 SE042104K80(S CER CAP .1U 25V K X7R 0603) add PQ61 SB000006800(S TR 2N7002W T/R7 1N SOT-323)	2010/11/01	DVT
5	Delete precharge 連動 circuit	Delete precharge 連動 circuit to avoid adapter UVP.	0.1	37	Add PD9, PD12 SC100001K00(S DIO 1SS355 SOD323 T/R-5K)	2010/11/01	DVT
6	Add input Cup.	Add input Cup. in CPU_COREP circuit for EMI ISN test.	0.1	44	Add PC213, PC214 SE042104K80(S CER CAP .1U 25V K X7R 0608)	2010/11/12	PVT
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Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title	PIR (PWR)
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PHASE	PAGE	Modification list	PURPOSE
0.1	P08	First release	Base on PEW96, change platform (NB,CPU-->APU,SB820-->FCH)
0.2	P--	C220, C336, C347, C357, C359, C360, C387, C388, C389, C390, C391, C392, C393, C421, C427, C428, C1461 change 0603 size	Follow Standard Part 0805-->0603
0.2	P--	C721, C669, C1005, C705, C708, C713, C715, C736, C794, C797, C932, C934, C983 change 0603 size	Follow Standard Part 0805-->0603
0.2	P--	C215, C216, C218, C224, C226, C227, C229, C230, C231, C660, C671, C821, C823, C1210, C1517, C1522, C1526, C1529, C1532, C1512, C1523, C1443, C1445, C1446, C1447, C1448, C1452, C1453, C1454 change 0603 size	Follow Standard Part 0805-->0603
0.2	P35	R1I22 change as 200k ohm, C1463 change as 0.1UF	Adjust sequence
0.2	P5	Add R1O9, R155	Pull up 4.7k ohm for CRT_EDIE
0.2	P16	Unpop R632, C744, C69, C746; Pop R633	+VDDIO_18_FC Tie to GND for Nun-share ROM
0.2	P16	Add R635; Unpop R634	AMD suggestion for +VDDIO_AZ
0.2	P24	Add R170, R171	For DISO BOM option
0.2	P13	Add U33, C1I99, R830, R838, R839	For VGA_PWRGD
0.2	P13	Remove C52, R557	For A_RST#
0.2	P27	EC_MUTE# change as I2 PIN form 46 PIN in Codec	For External Mute Fail issue
0.2	P16	C1I3, C77, C743, C96 change 0603 size and add C121, C105, C108, C109	22uF cap. change two 10uF cap. 0603 size
0.2	P19	C14 change 0603 size and add C52	22uF cap. change two 10uF cap. 0603 size
0.2	P13	C66, C67 change 27pF	Follow suggestion by TXC result
0.2	P26	C1485, C1486 change 33pF	Follow suggestion by TXC result
0.2	P33	C711 Change as SF000003I00	Material shortage
0.2	P9	Add C643, C675, C676, C678	For DDR3 moat issue
0.2	P26	Remove C939 ; Reserve C941, D48, D49, D51, L109	For LAN
0.2	P7	Add C604, C684	For CRT Monitor issue
0.3	P--	C2I2, C623 change 0603 size ; add C628, C685	Follow Standard Part 0805-->0603
0.3	P27	R786 change as 15k ohm	Dos Beep Issue
0.3	P19	change R21, R22 as DISO@	Device Menage Audio issue
1.0	P27	Add R797, R800	Mic noise issue
1.0	P26,I0	Reverse C939, C942, R456, R419, R426	for EMI ISN solution
1.0	P32	Add C753, C785	for EMI request

Change footprint : For cost down purpose to change parts

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