Compal Confidential

QML70 Schematics Document

AMD Comal

APU Trinity / Hudson M3 / Thames XT M2
UMA Only / PX Muxless with BACO

2011-10-17

LA-8371P REV: 0.2

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Model Name : QML70

ZZZ1
PCB 0OG LA-8371P REV0 MB
DA80000RG00

Comal

VRAM 2G/1G
128M x16 x 8 /
64M x 16 x 8
page 24, 25

DDR3

Thermal Sensor
ADM1032
page 19

ATI Thames XT M2
uFCBGA-962
+1.0VSG, +1.5VSG, +1.8VSG,
+3VSG, +VGA_CORE, +VDDCI
Page 18~25

GFX x 16 Gen2

DP x4 (DP0 TXP/N0 ~ 3)
APU HDMI
(UMA / Muxless)
DP x2 (DP2 TXP/N0 ~ 1)

AMD FS1r2 APU
Trinity
uPGA-722 Package
+APU_CORE, +APU_CORE_NB,
+1.5V, +1.2VS, +2.5VS
Page 6~10

Memory BUS(DDR3)
Dual Channel
1.5V DDRIII 800~1333MHz

204pin DDRIII-SO-DIMM X2
BANK 0, 1, 2, 3
Page 11,12

HDMI Conn.
page 29

LVDS Conn.
page 28

LVDS

LVDS Translator
RTD2136S-VE-CG
page 27

P_GPP x 2
GEN1

DP x4 (DP1 TXP/N0 ~ 3)

UMI

CRT Conn.
page 28

FCH CRT (VGA DAC)

FCH
Hudson-M3
uFCBGA-656
+3V_PCH, +1.1VALW, +1.1VS
Page 13~17

USB 2.0 + 3.0
page 35

USB 2.0 + 3.0
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USB2.0
page 30

USB2.0
page 30

CMOS Camera
page 28

Mini Card
(with BT)
page 33

USB3.0 Port 0
USB2.0 Port 10

USB3.0 Port 1
USB2.0 Port 11

USB2.0 Port 0

USB2.0 Port 1

USB2.0 Port 2

USB2.0 Port 3

USB
3.3V 48MHz

USB2.0 Port 4

HD Audio
3.3V 24.576MHz/48Mhz

Card Reader
RTS5137-GR
page 32

SATA Gen2

port 0

port 1

port 2

SATA HDD1
Conn.
page 34

SATA HDD2
Conn.
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ODD
Conn.
page 34

HDA Codec
ALC269Q-VB5-GR
page 31

GPP1

GPP2

LAN(GbE)
RTL8111F-CGT
page 30

MINI Card 1
WLAN w/ BT
page 33

RJ45
page 30

SPI ROM
4MB
page 15

LPC BUS

ENE KB9012
page 37

SPI ROM
128KB
(Reserve) page 37

Touch Pad
page 38

Int.KBD
page 38

LED
page 39

RTC CKT.
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DC/DC
Interface CKT.
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VGA DC/DC
Interface CKT.
page 26

Power Circuit
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硬體

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Title: Block Diagrams

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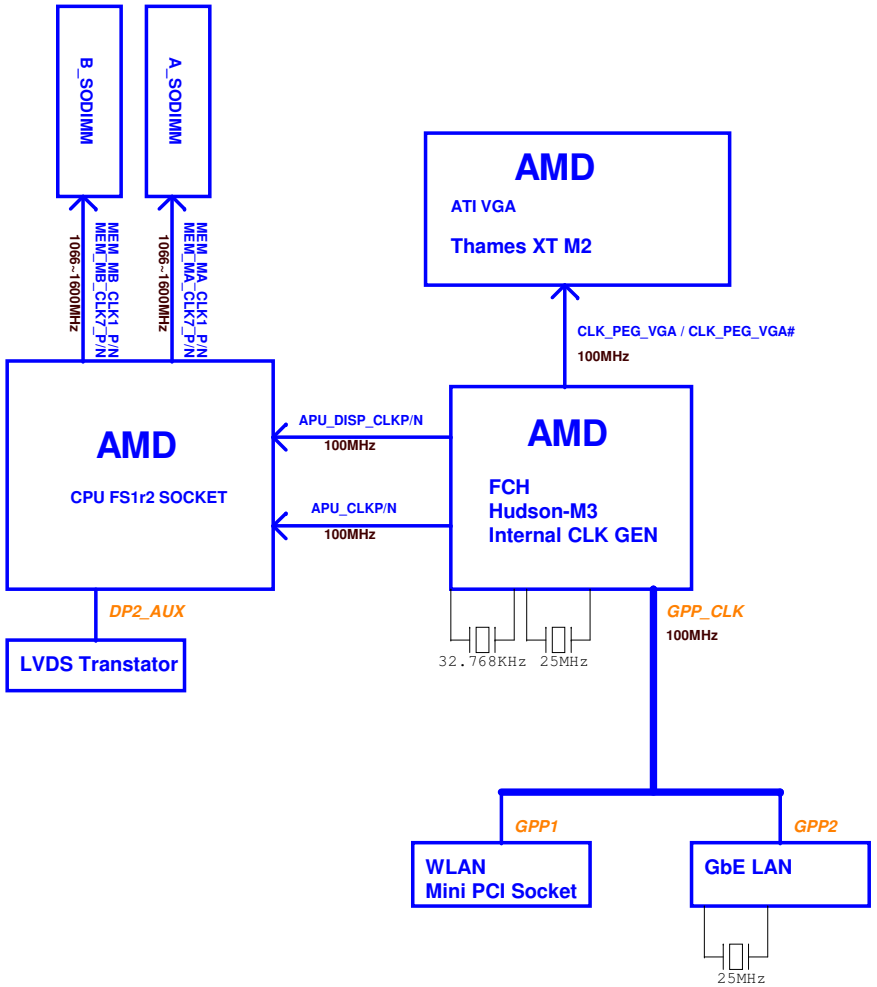
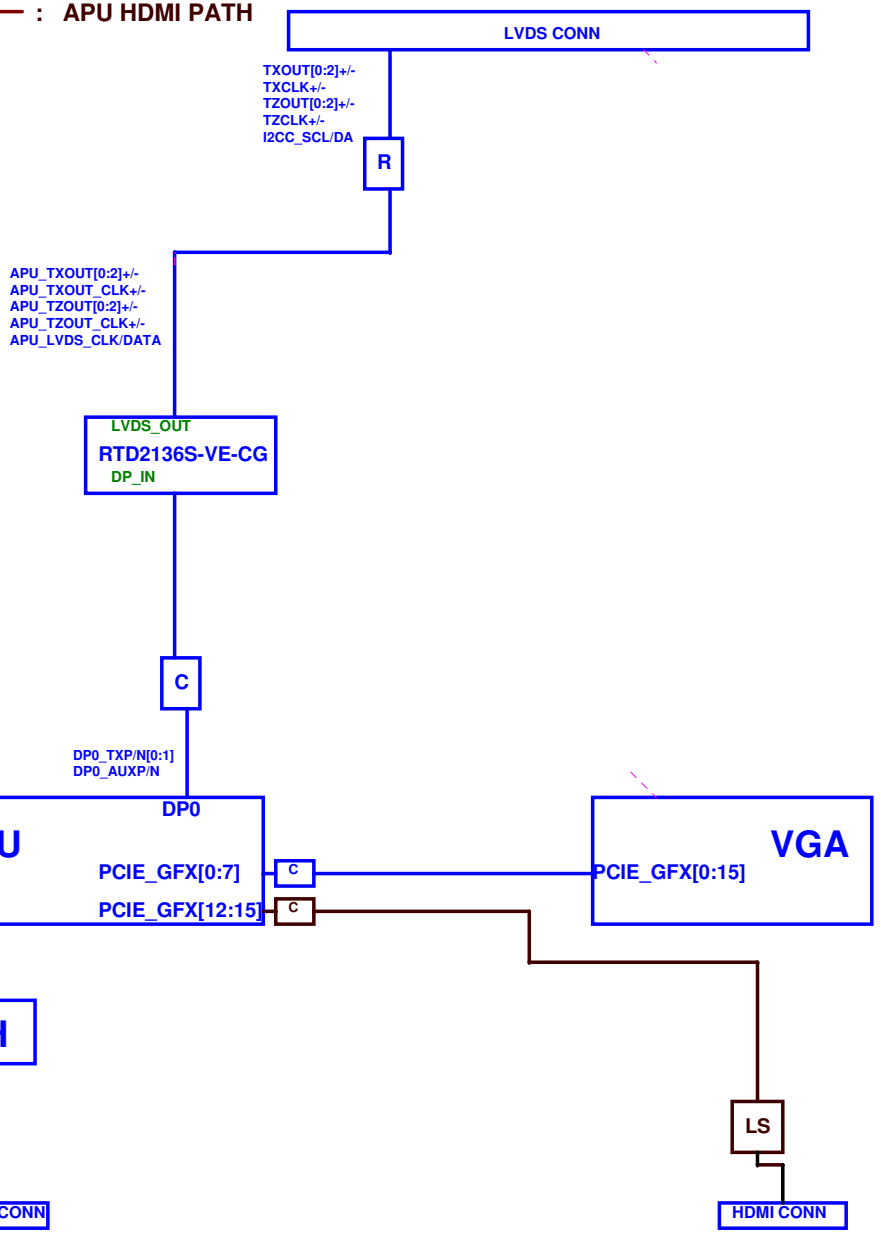
CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION

: LVDS PATH

: APU HDMI PATH



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Title	CLOCK / DISPLAY DISTRIBUTION		
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Voltage Rails

Power Plane	Description	S1	S3	S4/S5	Deep S3
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF	ON
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*	OFF
+3V_PCH	3.3V switched power rail for FCH	ON	ON	ON*	OFF
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF	OFF
+3VSG	1.8V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF	ON
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*	ON
+LAN_IO	3.3V power rail for LAN	ON	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*	ON
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*	ON
+RTCVCC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

BOM Structure	BTO Item
PX@	Use VGA (Mux)
X76@	VRAM ID Table
AI	Use AI Charger
nonAI@	Do not use AI Charger
CARD@	Use Card Reader IC
nonCARD@	do not use Card Reader IC
X76L01@	Use Hynix GDDR3 1GB VRAM
X76L02@	Use Hynix GDDR3 2GB VRAM
X76L03@	Use Samsung GDDR3 1GB VRAM
X76L04@	Use Samsung GDDR3 2GB VRAM
930@	Use EC KB930
9012@	Use EC KB9012

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032	1001 101X b	9AH
AMD Thames XT M2	1000 001X b	82H
AMD FS1r2 (APU)	1001 1000 b	98H
RTD2132S (TL)	1010 1000 b	A8H

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	D0
DDR DIMM2	1101 001X b	D2

FCH SM Bus 1 address

Device	Address	HEX

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0 +/- 5%	0 V	0 V	0.155 V
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V

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Title: Notes List

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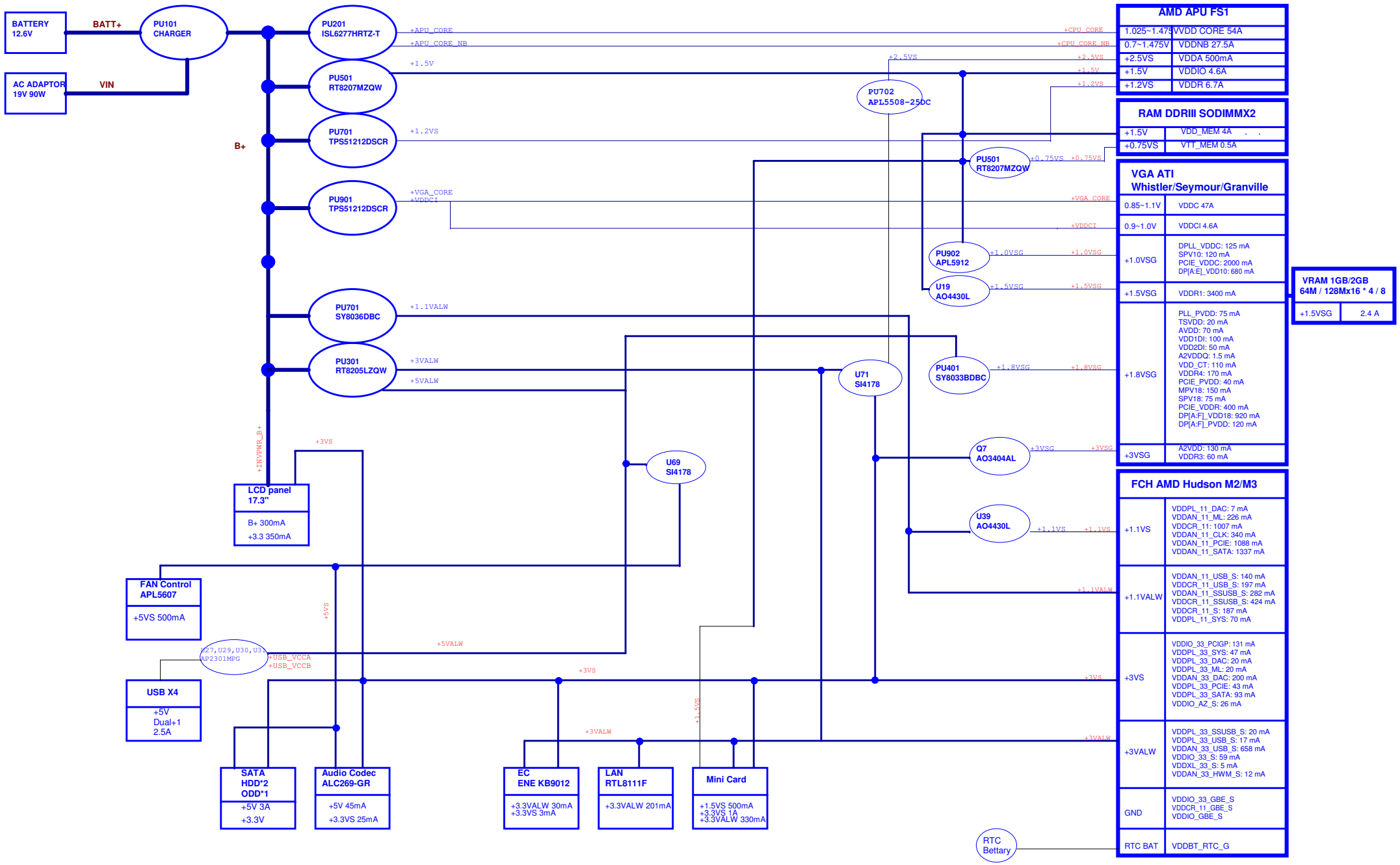

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18 PCIE_CRX_GTX_P[0..15]
18 PCIE_CRX_GTX_N[0..15]

PCIE_CTX_GRX_P[0..15] 18
PCIE_CTX_GRX_N[0..15] 18

JCPU1A

PCI EXPRESS

PCIE_CRX_GTX_P0	AB8	P_GFX_RXP0	P_GFX_TXP0	AB2	PCIE_CTX_C_GRX_P0	C1	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_P0
PCIE_CRX_GTX_N0	AB7	P_GFX_RXN0	P_GFX_TXN0	AB1	PCIE_CTX_C_GRX_N0	C2	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_N0
PCIE_CRX_GTX_P1	AA9	P_GFX_RXP1	P_GFX_TXP1	AA3	PCIE_CTX_C_GRX_P1	C3	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_P1
PCIE_CRX_GTX_N1	AA8	P_GFX_RXN1	P_GFX_TXN1	AA2	PCIE_CTX_C_GRX_N1	C4	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_N1
PCIE_CRX_GTX_P2	AA5	P_GFX_RXP2	P_GFX_TXP2	Y5	PCIE_CTX_C_GRX_P2	C5	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_P2
PCIE_CRX_GTX_N2	AA6	P_GFX_RXN2	P_GFX_TXN2	Y4	PCIE_CTX_C_GRX_N2	C6	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_N2
PCIE_CRX_GTX_P3	Y8	P_GFX_RXP3	P_GFX_TXP3	Y2	PCIE_CTX_C_GRX_P3	C7	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_P3
PCIE_CRX_GTX_N3	Y7	P_GFX_RXN3	P_GFX_TXN3	Y1	PCIE_CTX_C_GRX_N3	C8	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_N3
PCIE_CRX_GTX_P4	W9	P_GFX_RXP4	P_GFX_TXP4	W3	PCIE_CTX_C_GRX_P4	C9	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_P4
PCIE_CRX_GTX_N4	W8	P_GFX_RXN4	P_GFX_TXN4	W2	PCIE_CTX_C_GRX_N4	C10	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_N4
PCIE_CRX_GTX_P5	W5	P_GFX_RXP5	P_GFX_TXP5	V5	PCIE_CTX_C_GRX_P5	C11	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_P5
PCIE_CRX_GTX_N5	W6	P_GFX_RXN5	P_GFX_TXN5	V4	PCIE_CTX_C_GRX_N5	C12	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_N5
PCIE_CRX_GTX_P6	V8	P_GFX_RXP6	P_GFX_TXP6	V2	PCIE_CTX_C_GRX_P6	C13	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_P6
PCIE_CRX_GTX_N6	V7	P_GFX_RXN6	P_GFX_TXN6	V1	PCIE_CTX_C_GRX_N6	C14	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_N6
PCIE_CRX_GTX_P7	U9	P_GFX_RXP7	P_GFX_TXP7	U3	PCIE_CTX_C_GRX_P7	C15	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_P7
PCIE_CRX_GTX_N7	U8	P_GFX_RXN7	P_GFX_TXN7	U2	PCIE_CTX_C_GRX_N7	C16	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_N7
PCIE_CRX_GTX_P8	U5	P_GFX_RXP8	P_GFX_TXP8	T5	PCIE_CTX_C_GRX_P8	C17	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_P8
PCIE_CRX_GTX_N8	U6	P_GFX_RXN8	P_GFX_TXN8	T4	PCIE_CTX_C_GRX_N8	C18	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_N8
PCIE_CRX_GTX_P9	T8	P_GFX_RXP9	P_GFX_TXP9	T2	PCIE_CTX_C_GRX_P9	C19	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_P9
PCIE_CRX_GTX_N9	T7	P_GFX_RXN9	P_GFX_TXN9	T1	PCIE_CTX_C_GRX_N9	C20	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_N9
PCIE_CRX_GTX_P10	R9	P_GFX_RXP10	P_GFX_TXP10	R3	PCIE_CTX_C_GRX_P10	C21	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_P10
PCIE_CRX_GTX_N10	R8	P_GFX_RXN10	P_GFX_TXN10	R2	PCIE_CTX_C_GRX_N10	C22	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_N10
PCIE_CRX_GTX_P11	R5	P_GFX_RXP11	P_GFX_TXP11	P5	PCIE_CTX_C_GRX_P11	C23	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_P11
PCIE_CRX_GTX_N11	R6	P_GFX_RXN11	P_GFX_TXN11	P4	PCIE_CTX_C_GRX_N11	C24	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_N11
PCIE_CRX_GTX_P12	P8	P_GFX_RXP12	P_GFX_TXP12	P2	PCIE_CTX_C_GRX_P12	C25	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_P12
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PCIE_CRX_GTX_P15	M8	P_GFX_RXP15	P_GFX_TXP15	M2	PCIE_CTX_C_GRX_P15	C31	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_P15
PCIE_CRX_GTX_N15	M7	P_GFX_RXN15	P_GFX_TXN15	M1	PCIE_CTX_C_GRX_N15	C32	PX@	1	2	0.1U_0402_16V7K	PCIE_CTX_GRX_N15

GRAPHICS

	AE5	P_GPP_RXP0	P_GPP_TXP0	AD5							
	AE6	P_GPP_RXN0	P_GPP_TXN0	AD4							
	AD8	P_GPP_RXP1	P_GPP_TXP1	AD2	PCIE_CTX_DRX_P1	C35	1		2	0.1U_0402_16V7K	
	AD7	P_GPP_RXN1	P_GPP_TXN1	AD1	PCIE_CTX_DRX_N1	C36	1		2	0.1U_0402_16V7K	
	AC9	P_GPP_RXP2	P_GPP_TXP2	AC3	PCIE_CTX_DRX_P2	C71	1		2	0.1U_0402_16V7K	
	AC8	P_GPP_RXN2	P_GPP_TXN2	AC2	PCIE_CTX_DRX_N2	C72	1		2	0.1U_0402_16V7K	
	AC5	P_GPP_RXP3	P_GPP_TXP3	AB5							
	AC6	P_GPP_RXN3	P_GPP_TXN3	AB4							

GPP

LAN 30 PCIE_DTX_C_CRX_P1
LAN 30 PCIE_DTX_C_CRX_N1
WLAN 33 PCIE_DTX_C_CRX_P2
WLAN 33 PCIE_DTX_C_CRX_N2

PCIE_CTX_C_DRX_P1 30 LAN
PCIE_CTX_C_DRX_N1 30 LAN
PCIE_CTX_C_DRX_P2 33 WLAN
PCIE_CTX_C_DRX_N2 33 WLAN

13 UMI_MTX_C_CRX_P0	AG8	P_UMI_RXP0	P_UMI_TXP0	AG2	UMI_CTX_MRX_P0	C37	1		2	0.1U_0402_16V7K	UMI_CTX_C_MRX_P0 13
13 UMI_MTX_C_CRX_N0	AG9	P_UMI_RXN0	P_UMI_TXN0	AG3	UMI_CTX_MRX_N0	C38	1		2	0.1U_0402_16V7K	UMI_CTX_C_MRX_N0 13
13 UMI_MTX_C_CRX_P1	AG6	P_UMI_RXP1	P_UMI_TXP1	AF4	UMI_CTX_MRX_P1	C39	1		2	0.1U_0402_16V7K	UMI_CTX_C_MRX_P1 13
13 UMI_MTX_C_CRX_N1	AG5	P_UMI_RXN1	P_UMI_TXN1	AF5	UMI_CTX_MRX_N1	C40	1		2	0.1U_0402_16V7K	UMI_CTX_C_MRX_N1 13
13 UMI_MTX_C_CRX_P2	AF7	P_UMI_RXP2	P_UMI_TXP2	AF1	UMI_CTX_MRX_P2	C41	1		2	0.1U_0402_16V7K	UMI_CTX_C_MRX_P2 13
13 UMI_MTX_C_CRX_N2	AF8	P_UMI_RXN2	P_UMI_TXN2	AF2	UMI_CTX_MRX_N2	C42	1		2	0.1U_0402_16V7K	UMI_CTX_C_MRX_N2 13
13 UMI_MTX_C_CRX_P3	AE8	P_UMI_RXP3	P_UMI_TXP3	AE2	UMI_CTX_MRX_P3	C43	1		2	0.1U_0402_16V7K	UMI_CTX_C_MRX_P3 13
13 UMI_MTX_C_CRX_N3	AE9	P_UMI_RXN3	P_UMI_TXN3	AE3	UMI_CTX_MRX_N3	C44	1		2	0.1U_0402_16V7K	UMI_CTX_C_MRX_N3 13

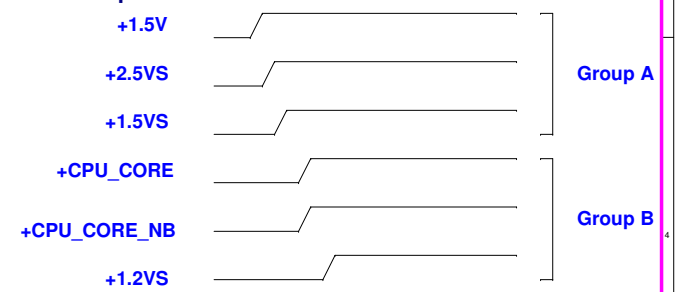
UMI

+1.2VS 1 R1 2 P_ZVDDP AG11
P_ZVDDP
196_0402_1%

P_ZVSS AH11 1 R2 2
196_0402_1%

CONN@ LOTES_ACA-ZIF-109-P12-A_FS1R2

Power Sequence of APU



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Title	FS1r2 PCIE/UMI		
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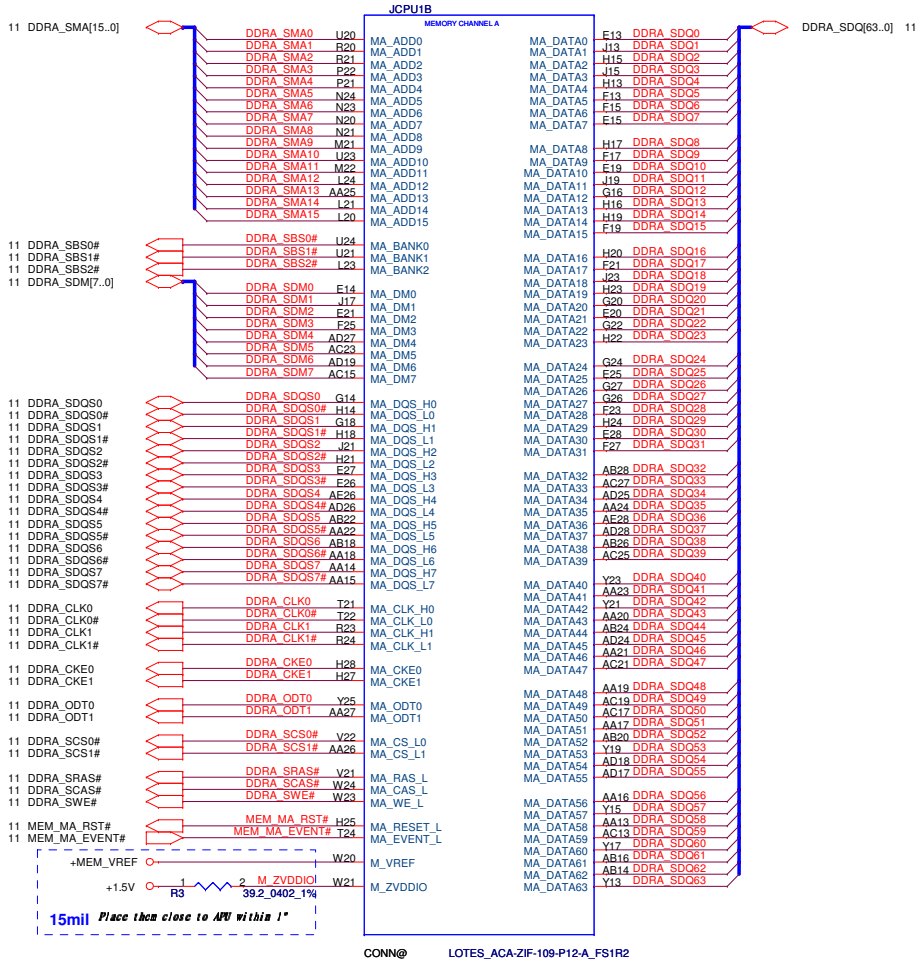
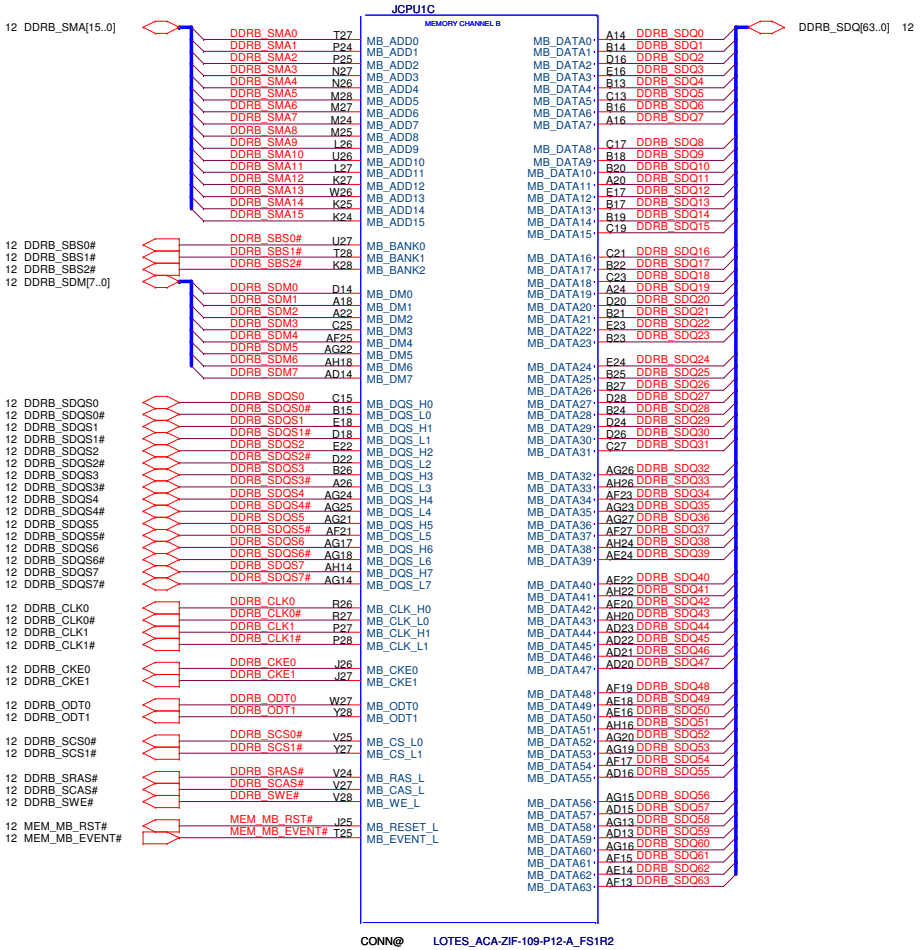
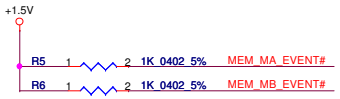
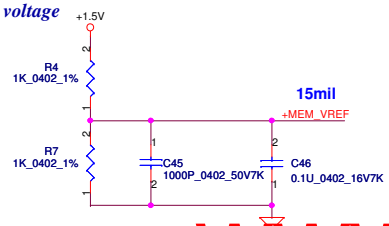




EVENT# pull high



0.75V reference voltage



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Compal Electronics, Inc.

Title: FS1r2 DDRIII Memory I/F

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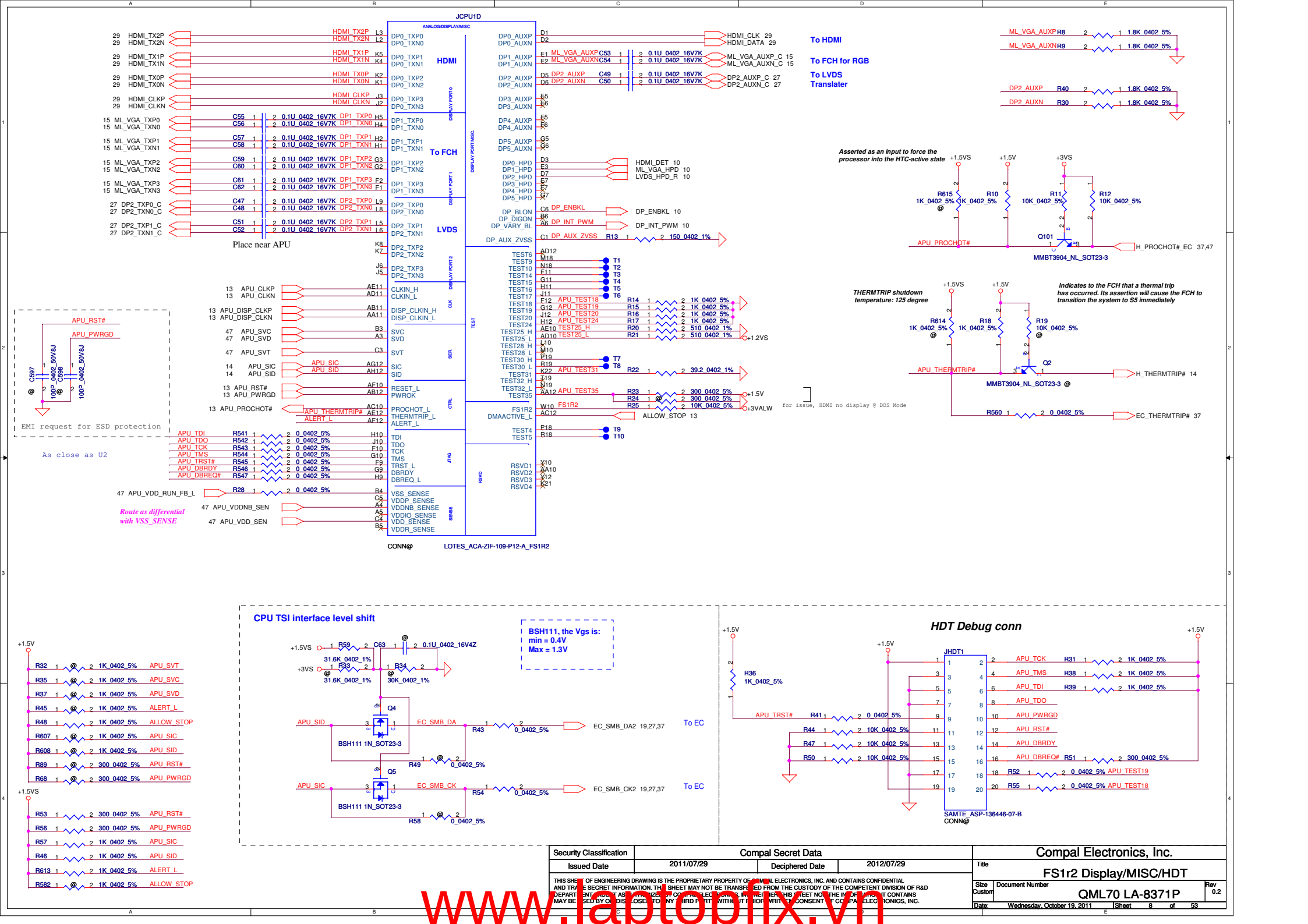

Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: FS1r2 Display/MISC/HDT

Size	Document Number	Rev
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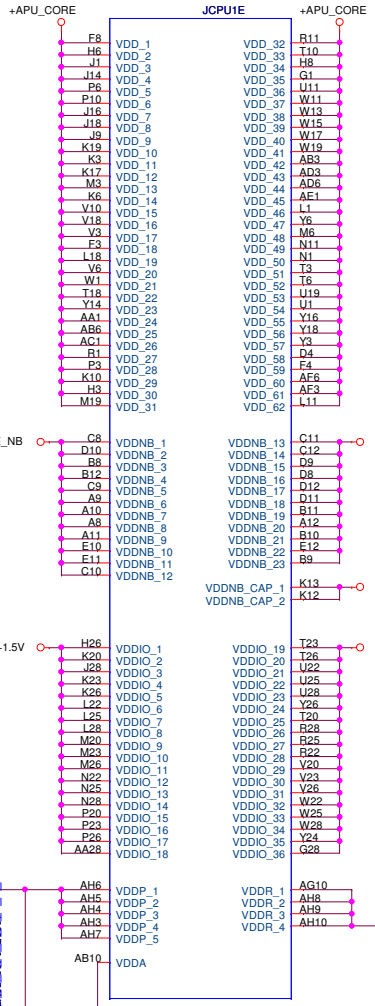
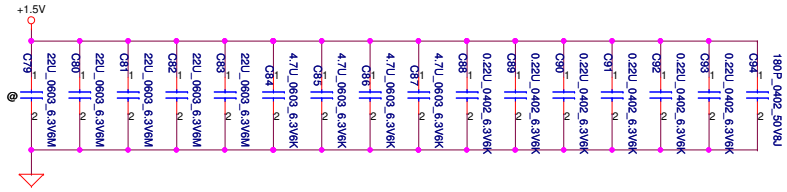
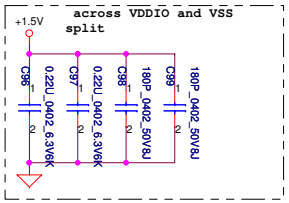
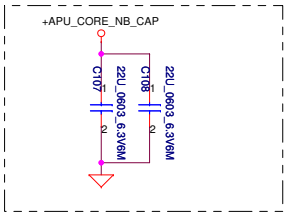
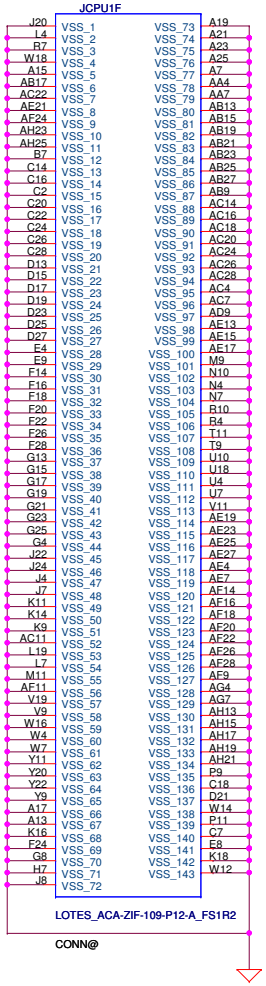
Power Name	Consumption
VDD +CPU_CORE	60A
VDDNB +CPU_CORE_NB	29A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A

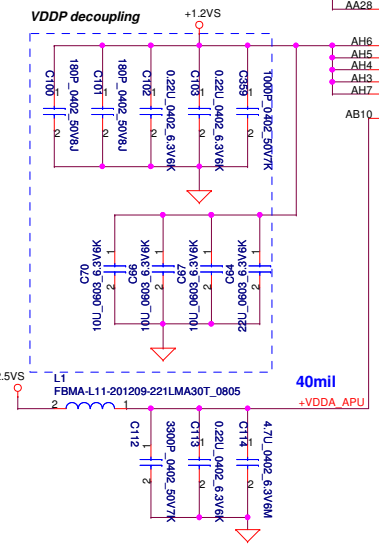


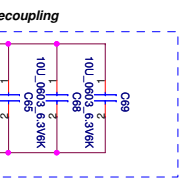












Demo Board Capacitor

APU_CORE	CORE_NB	CORE_NB_CAP
22uF x 7	22uF x 2	22uF x 2
0.22uF x 2	10uF x 1	
0.01uF x 3	0.22uF x 2	
180pF x 2	180pF x 3	

VDDP	VDDR	VDDA
22uF x 1	10uF x 3	4.7uF x 1
10uF x 3	0.22uF x 2	0.22uF x 1
0.22uF x 2	1nF x 1	3.3nF x 1
180pF x 2	180pF x 2	
1nF x 1		

Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: FS1r2 PWR/GND

Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.2

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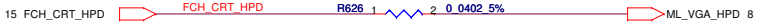
HPD

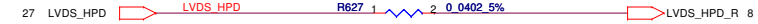
CRT HPD

From FCH



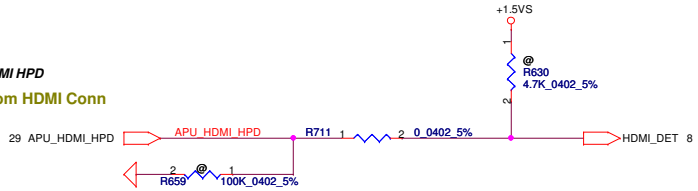
Translator HPD

From Translator

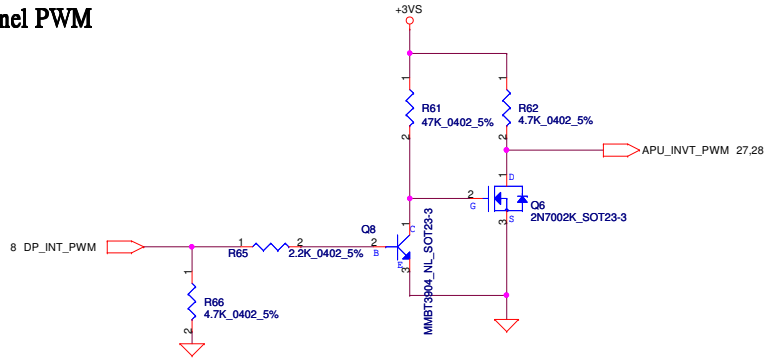


HDMI HPD

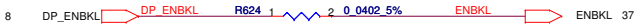
From HDMI Conn



Panel PWM



Panel ENBKL



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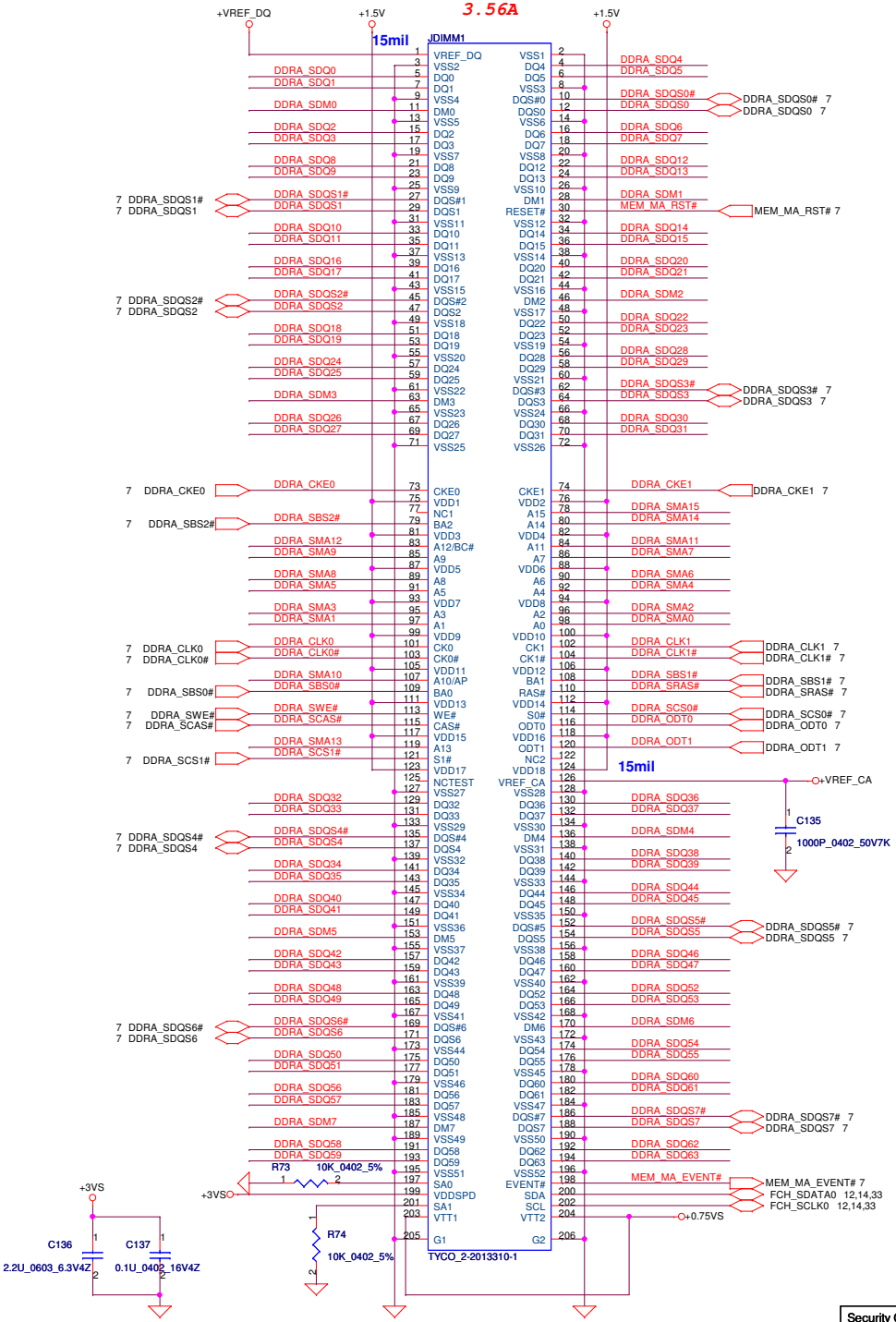
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.			
Title: FS1r2 Signal Level Shifter			
Size: Custom	Document Number: QML70 LA-8371P		Rev: 0.2
Date: Wednesday, October 19, 2011	Sheet 10 of 53		

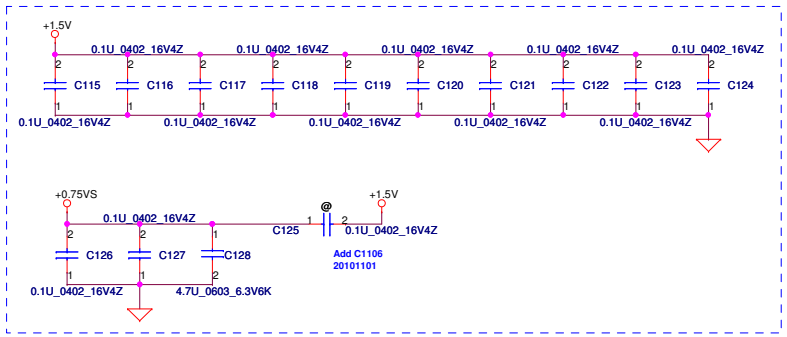


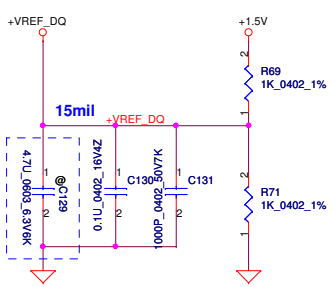
DIMM_A STD H:9.2mm

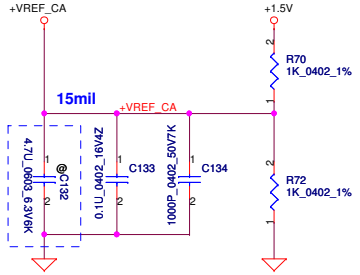
<Address: 00>

DDRA_SDQ[0..63] → DDRA_SDQ[0..63] 7
DDRA_SDM[0..7] → DDRA_SDM[0..7] 7
DDRA_SMA[0..15] → DDRA_SMA[0..15] 7

Place near DIMM1







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Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: DDRIII SO-DIMM 1

Size	Document Number	Rev
Custom	QML70 LA-8371P	0.2

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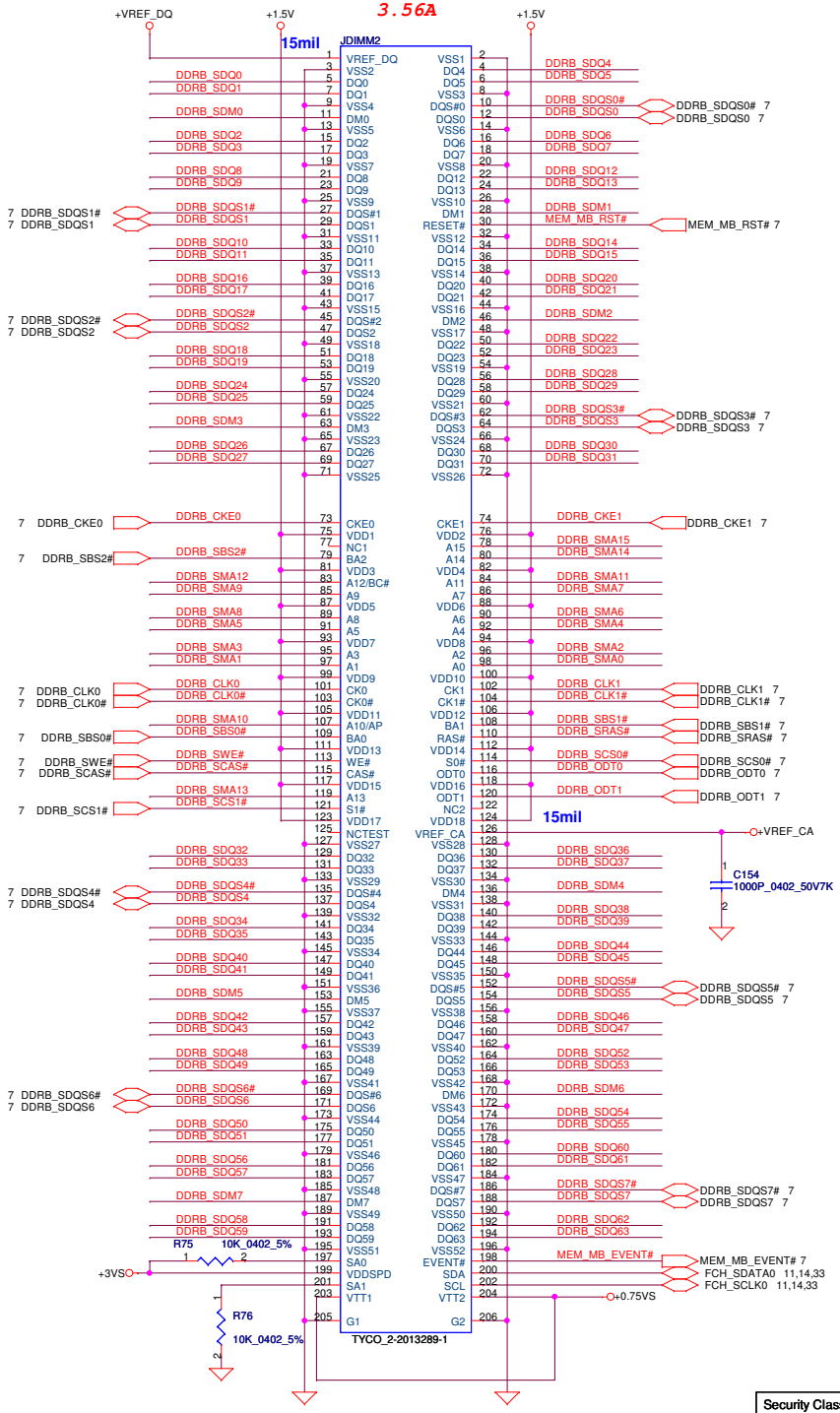


DIMM_B STD H:5.2mm

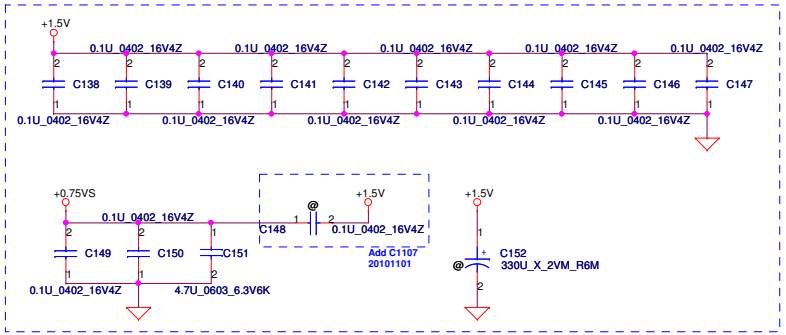
<Address: 01>

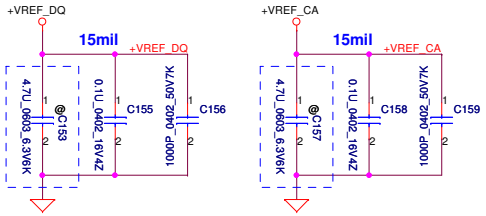
DDRB_SDQ[0..63] DDRB_SDQ[0..63] 7

DDRB_SDM[0..7] DDRB_SDM[0..7] 7

DDRB_SMA[0..15] DDRB_SMA[0..15] 7

Place near DIMM2





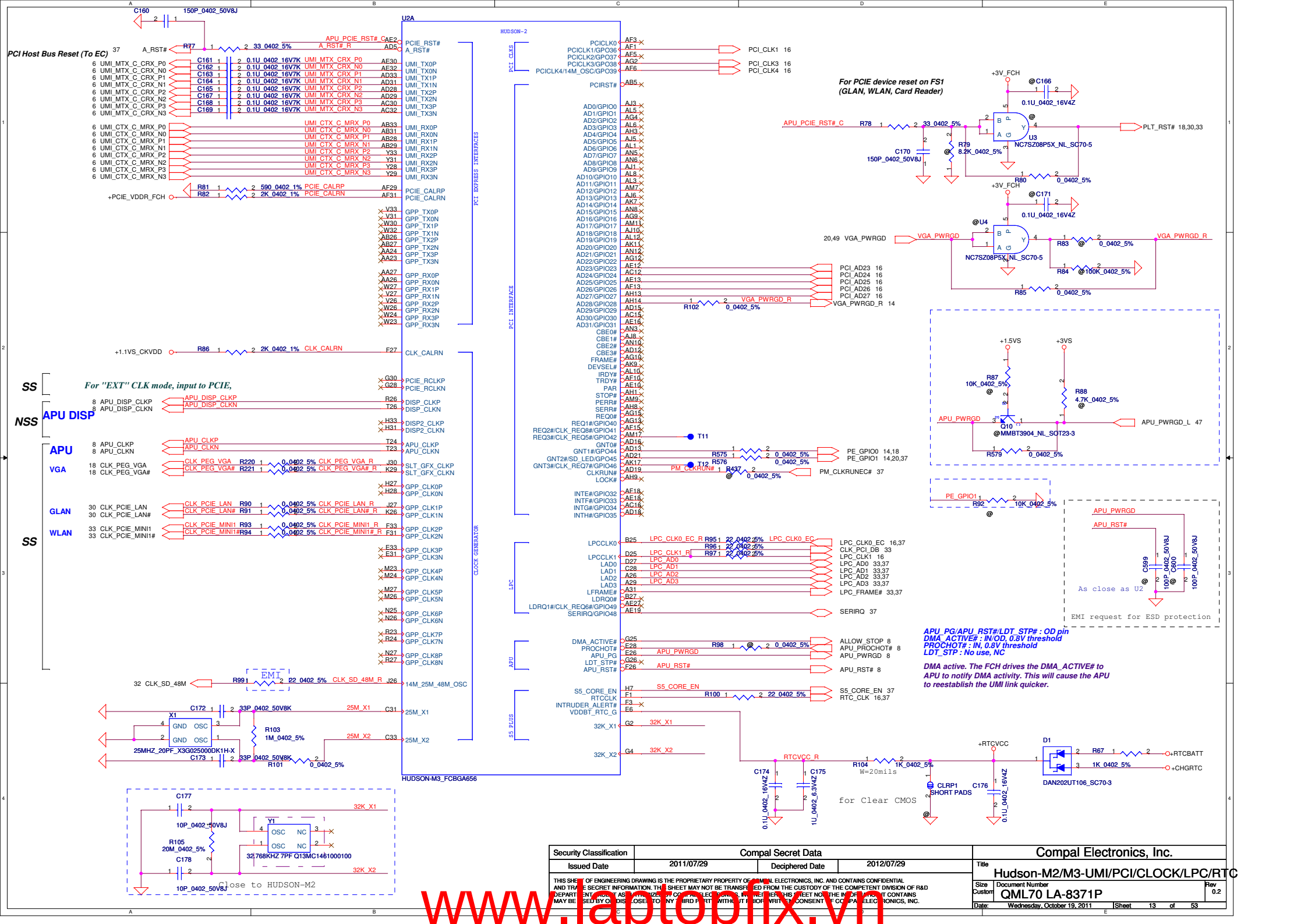
Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: DDRIII SO-DIMM 2

Size	Document Number	Rev
Custom	QML70 LA-8371P	0.2

Date: Wednesday, October 19, 2011 Sheet 12 of 53



PCIE_RST2 : Reset PCIE device on Hudson2

U2D

HUDSON-2

THERMTRIP:
Need level shift from +3VALW to +1.5V

SM bus 0-->S0 PWR domain
SM bus 1-->S5 PWR domain
VGA_PD: Support MLDAC power save if connect
0: MLDAC power on
1: MLDAC power off

Modify 2010212-AMD request

USB_OC0#: for USB3.0 w/ AI Charger (JUSB1)
USB_OC1#: for USB2.0 port (JUSB3, 4)
USB_OC2#: for USB3.0 port (JUSB2)

Hudson-M2 EHCI CTL DEV 22, Fn 2 <Disable CTL of M2>
Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0

USB2.0 + 3.0, JUSB2
USB2.0 + 3.0, JUSB1
Hudson-M2/M3 EHCI CTL DEV 19, Fn 2
Card Reader
Mini Card (WLAN w/ BT)
Camera
Hudson-M2/M3 EHCI CTL DEV 18, Fn 2
USB2.0 Conn. JUSB4
USB2.0 Conn. JUSB3
Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0
On board USB Conn

HUDSON-M3_FCBGA656

Project SKU ID

Add Project ID Table
201011301600

For FCH internal debug use

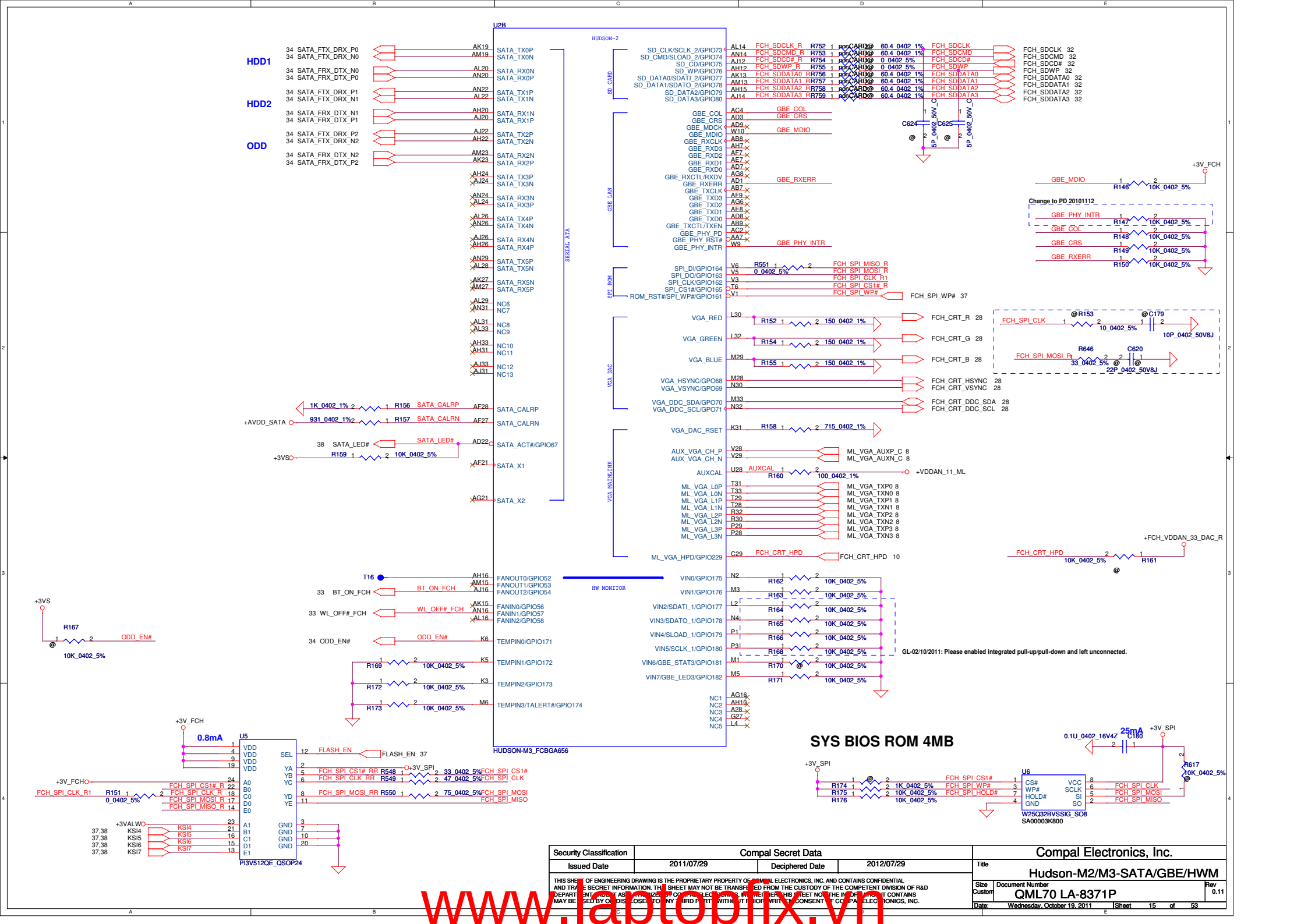
Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: Hudson-M2/M3-ACPI/USB/EC

Size	Document Number	Rev
Custom	QML70 LA-8371P	0.2

Date: Wednesday, October 19, 2011 | Sheet 14 of 53



Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

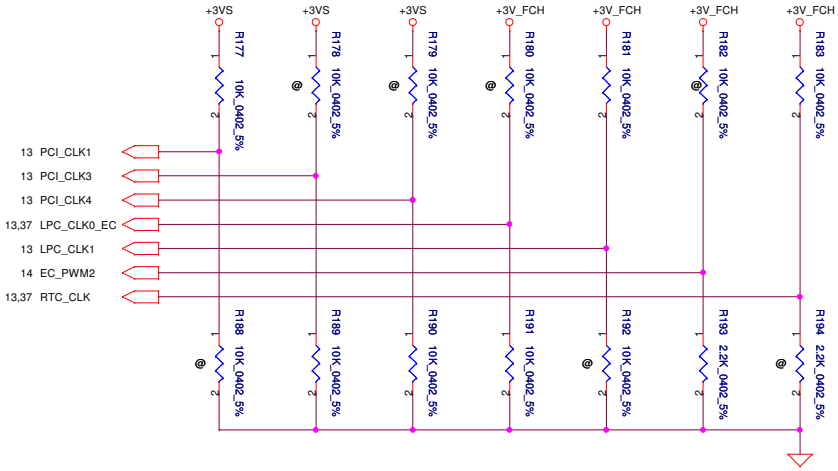
Title: Hudson-M2/M3-SATA/GBE/HWM

Size	Document Number	Rev
Custom	QML70 LA-8371P	0.11

Date: Wednesday, October 19, 2011 | Sheet 15 of 53

STRAP PINS

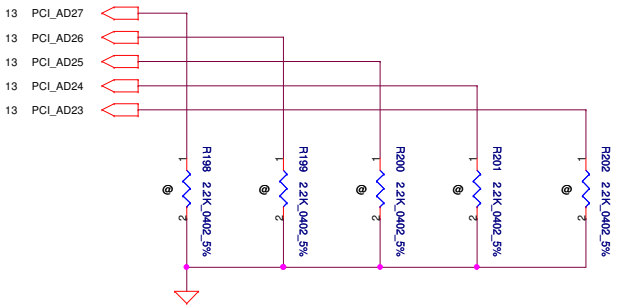
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED

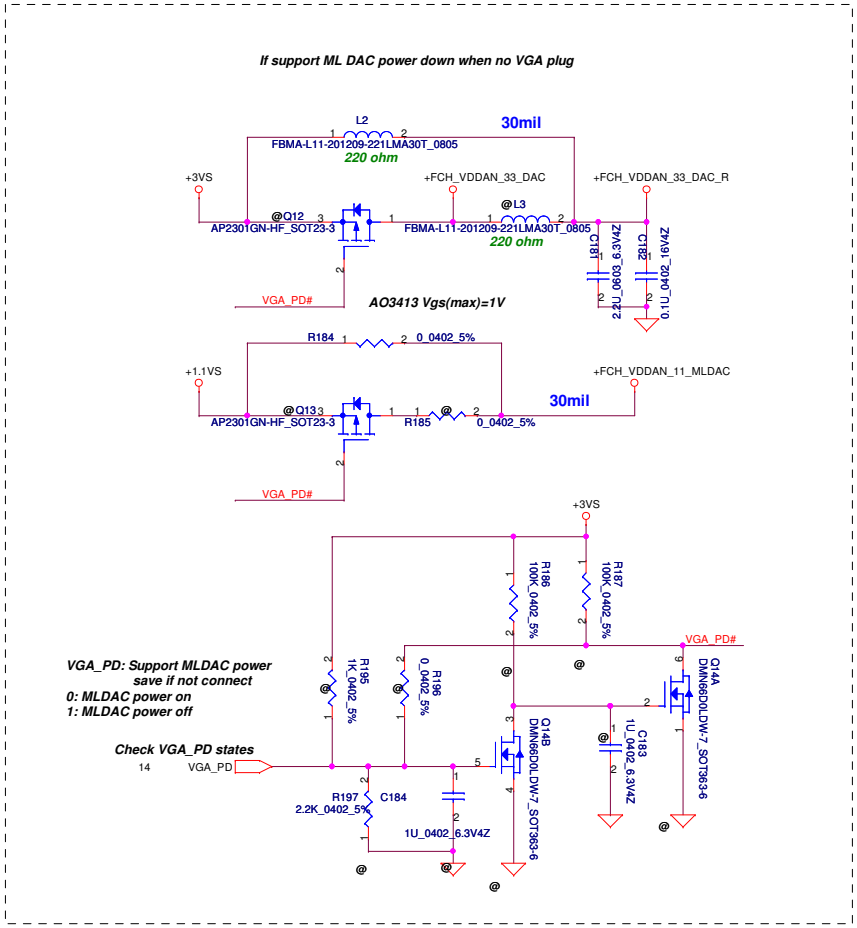


DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

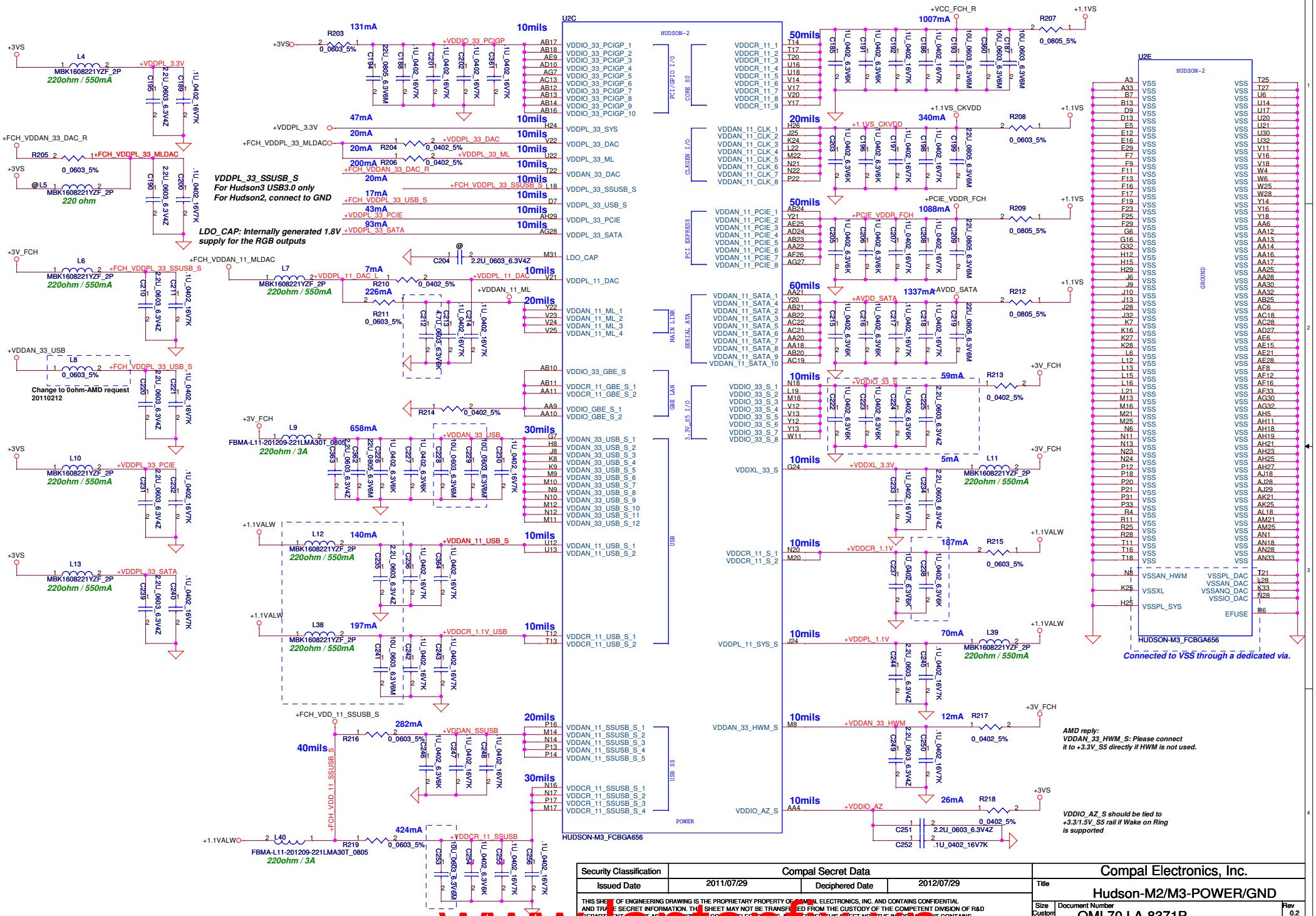
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.	
Title	Hudson-M2/M3-STRAP
Size: Custom	Document Number: QML70 LA-8371P
Rev	0.2
Date: Wednesday, October 19, 2011	Sheet 16 of 53



Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: Hudson-M2/M3-POWER/GND

Size	Document Number	Rev
Custom	QML70 LA-8371P	0.2

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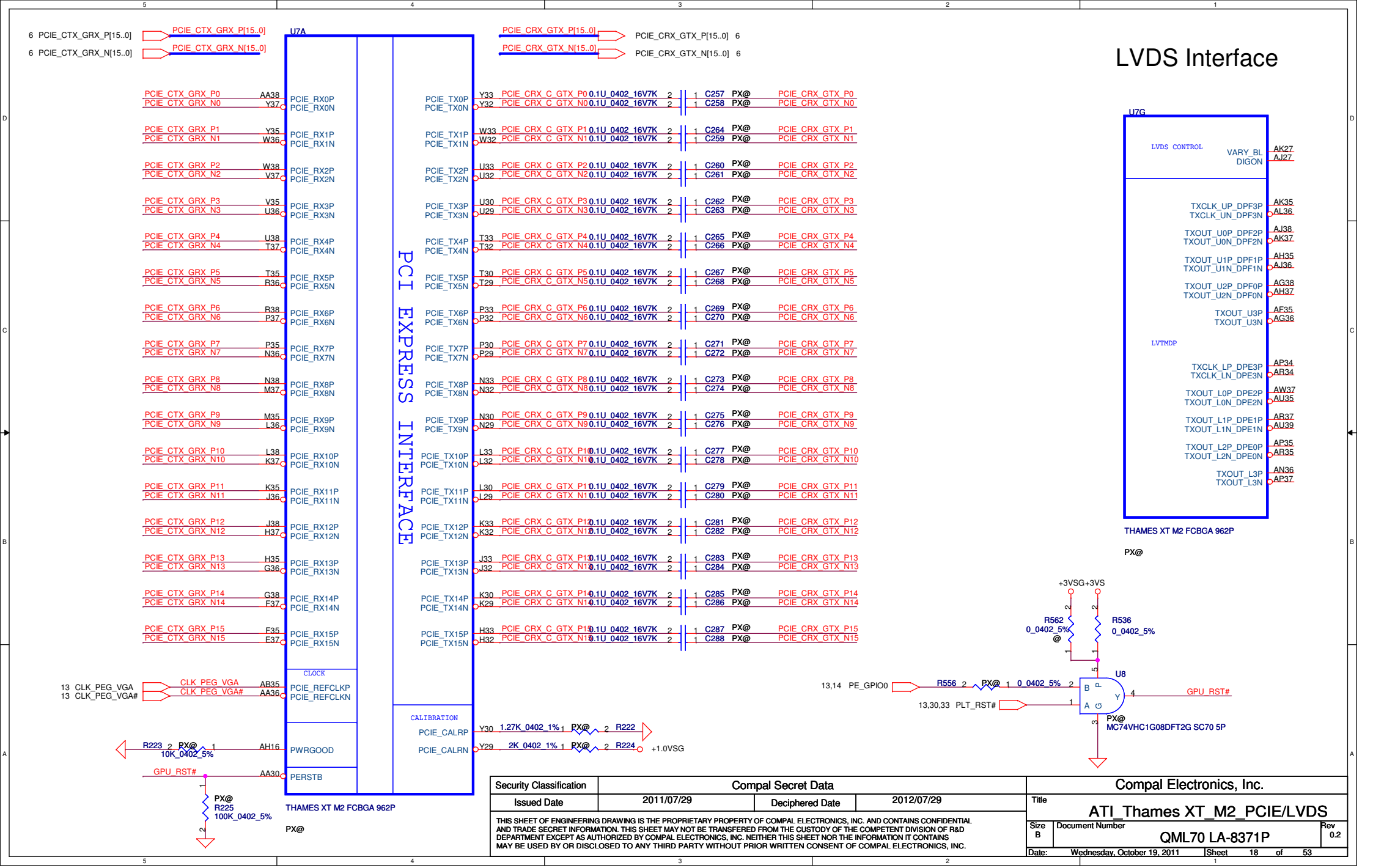
LVDS Interface



Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title	ATI_Thames XT_M2_PCIE/LVDS		
Size B	Document Number QML70 LA-8371P		Rev 0.2
Date: Wednesday, October 19, 2011	Sheet 18 of 53		

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test 0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort only 1 0 Audio for DisplayPort and HDMI, if dongle is detected. 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21 H2SYNC GENERICC GPIO2 GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)

STRAPS

Internal VGA Thermal Sensor

External VGA Thermal Sensor

Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

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Compal Electronics, Inc.

Title: ATI_Thames XT_M2_Main_MSIC

Size: C | Document Number: QML70 LA-8371P | Rev: 0.2

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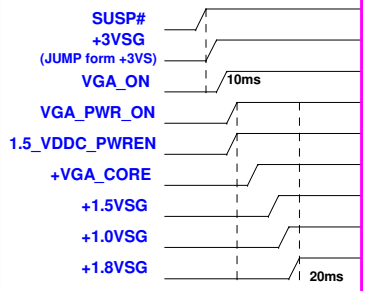
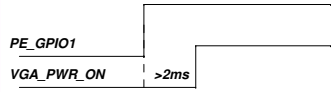
Power Sequence of Whistler and Seymour

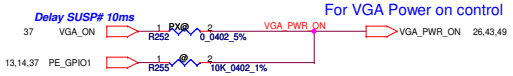


For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

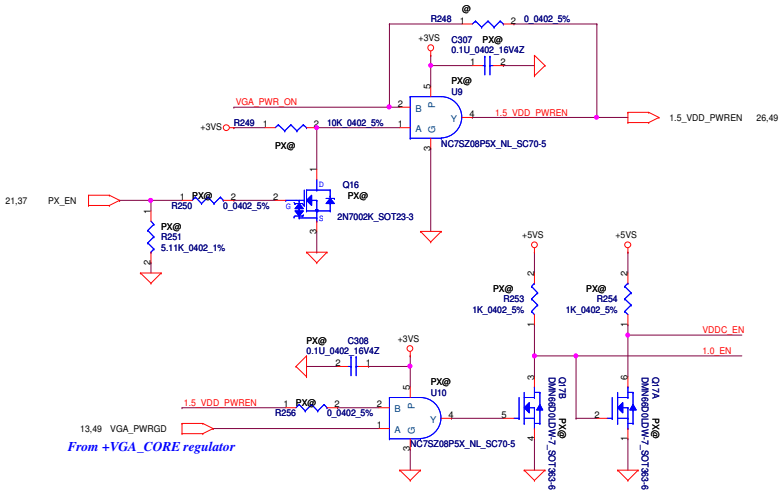


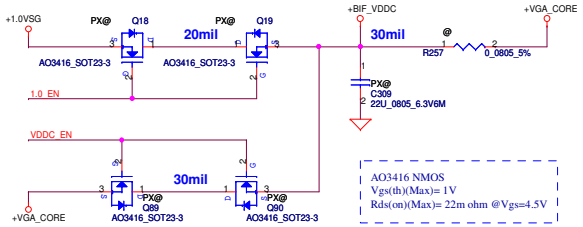
VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table	
	Whislter
VGA_PWR_ON source signal	VGA_ON
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN



For VGA Power on control





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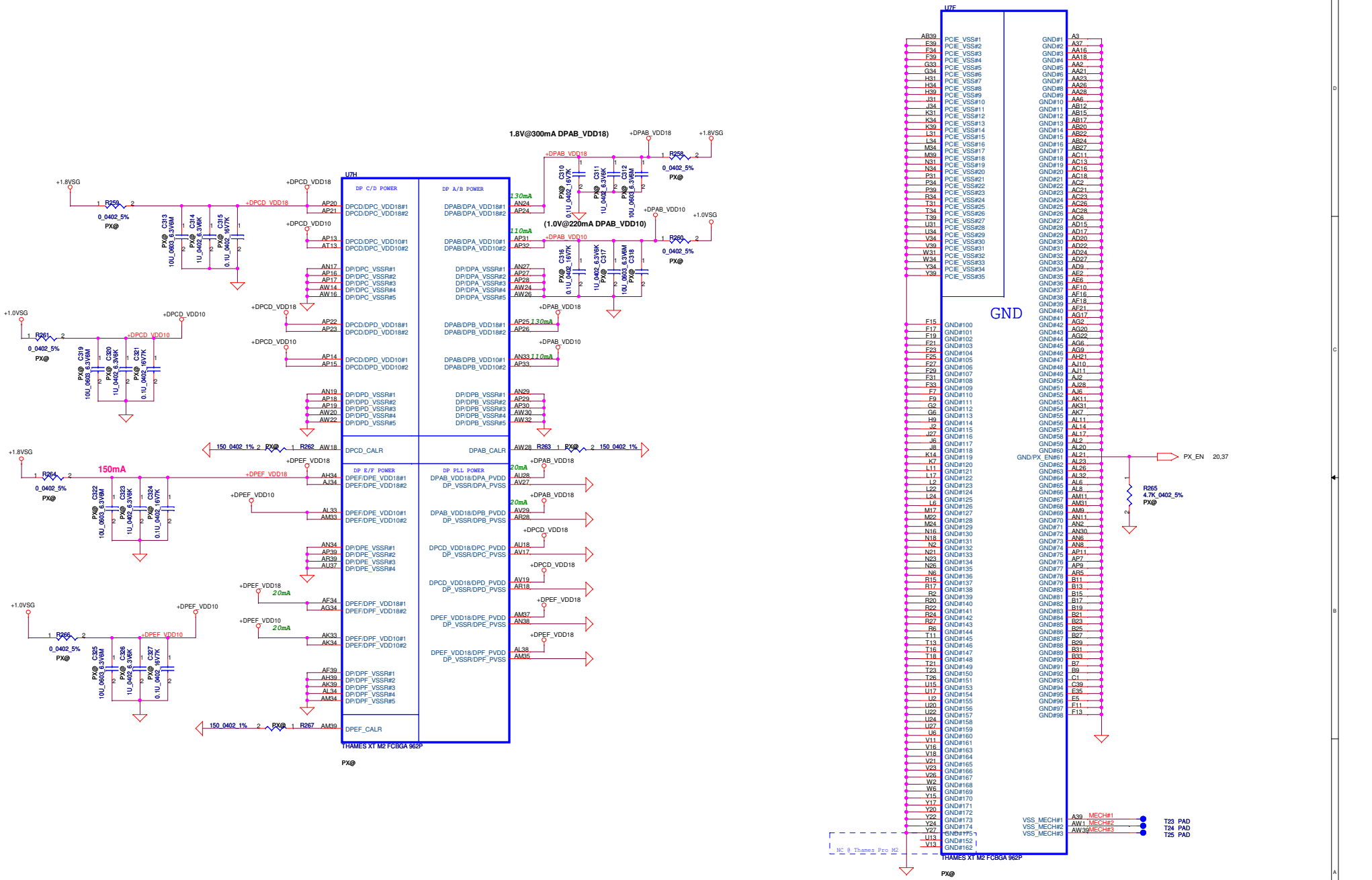
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Title	ATI_Thames XT_M2_BACO POWER		
Size C	Document Number QML70 LA-8371P		Rev 0.2
Date: Wednesday, October 19, 2011	Sheet 20 of 53		



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Issued Date	2011/07/29	Deciphered Date	2012/07/29

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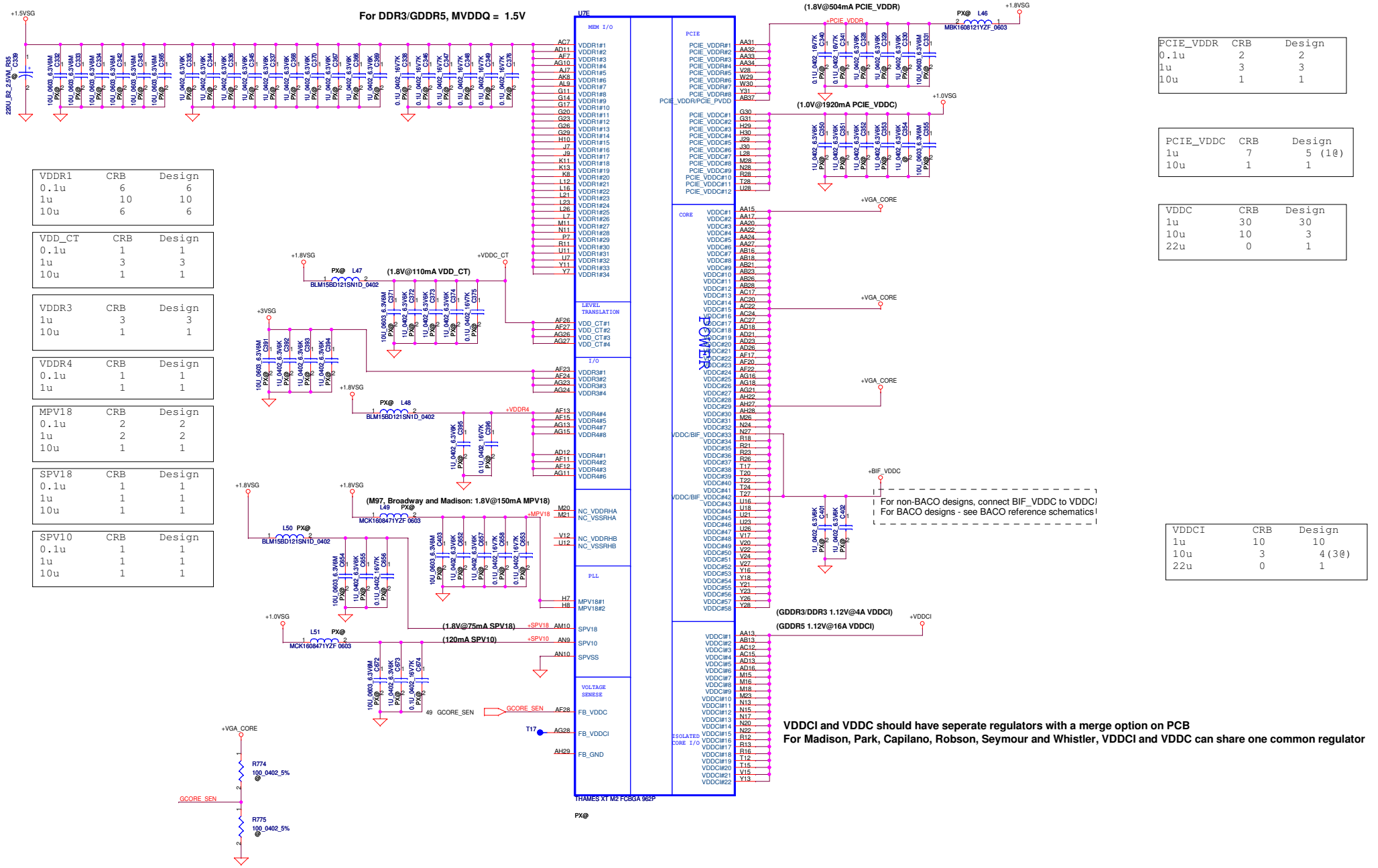
Compal Electronics, Inc.

Title: ATI_Thames XT_M2_PWR_GND

Size	Document Number	Rev
C	QML70 LA-8371P	0.2

Date: Wednesday, October 19, 2011 Sheet 21 of 53



VDDR1	CRB	Design
0.1u	6	6
1u	10	10
10u	6	6

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

VDDR3	CRB	Design
1u	3	3
10u	1	1

VDDR4	CRB	Design
0.1u	1	1
1u	1	1

MPV18	CRB	Design
0.1u	2	2
1u	2	2
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

PCIE_VDDR	CRB	Design
0.1u	2	2
1u	3	3
10u	1	1

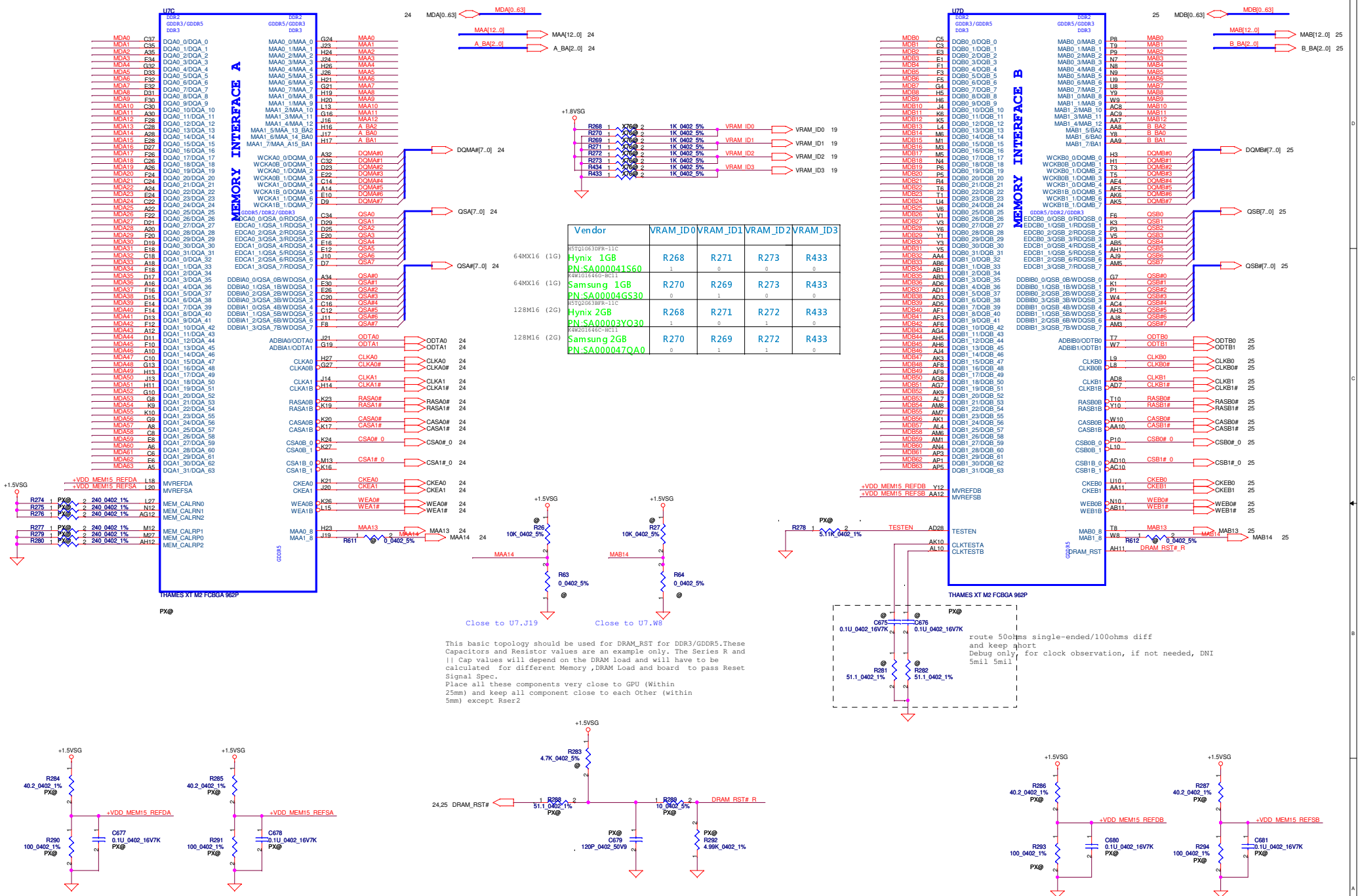
PCIE_VDDC	CRB	Design
1u	7	5 (1@)
10u	1	1

VDDC	CRB	Design
1u	30	30
10u	10	3
22u	0	1

VDDCI	CRB	Design
1u	10	10
10u	3	4(3@)
22u	0	1

Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.			
Title	ATI_Thames XT_M2_Power		
Size C	Document Number QML70 LA-8371P		Rev 0.2
Date: Wednesday, October 19, 2011	Sheet 22 of 53		



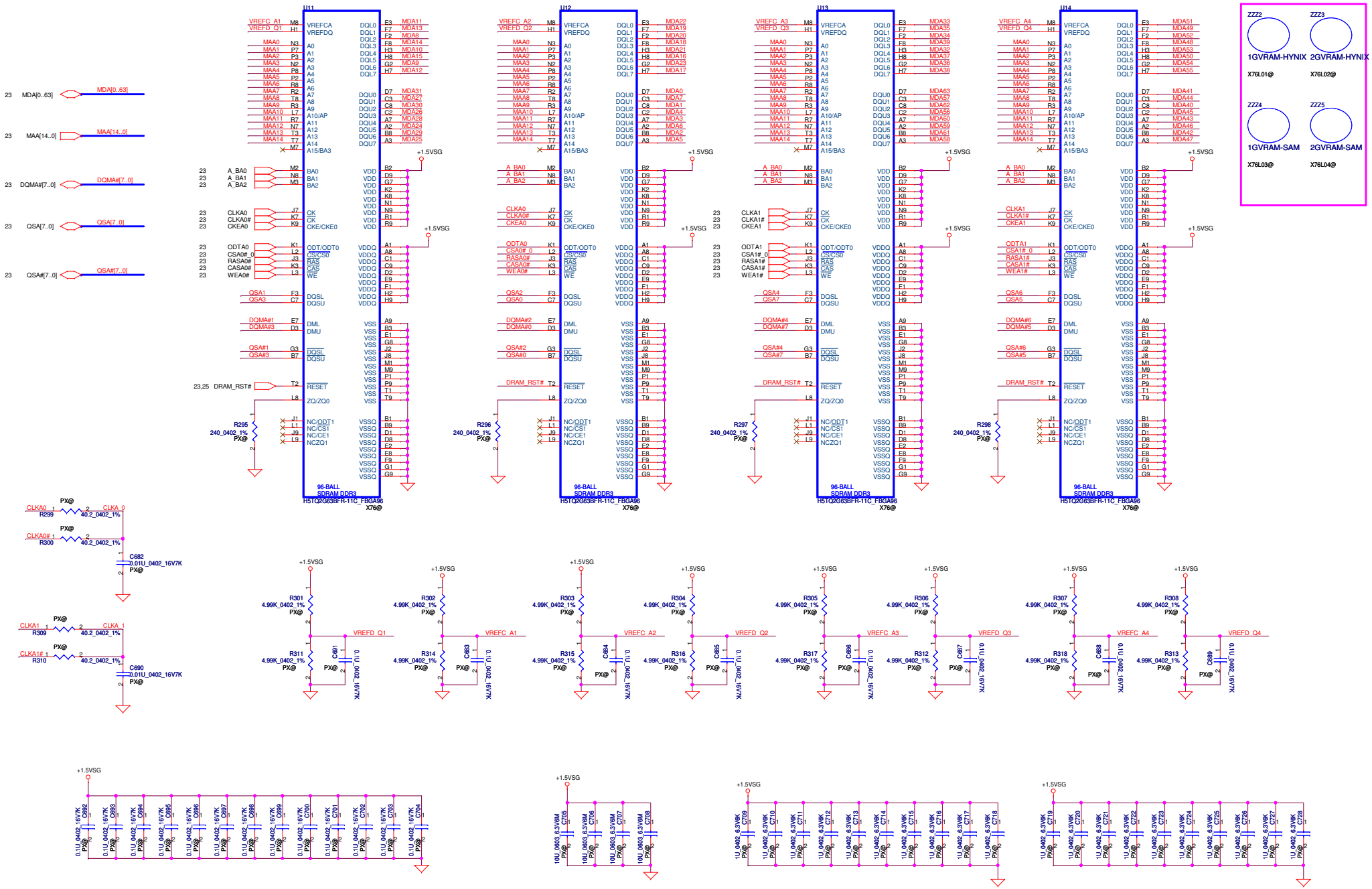
Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: ATI_Thames XT_M2_MEM IF

Size	Document Number	Rev
C	QML70 LA-8371P	0.2

Date: Wednesday, October 19, 2011 Sheet 23 of 53



Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

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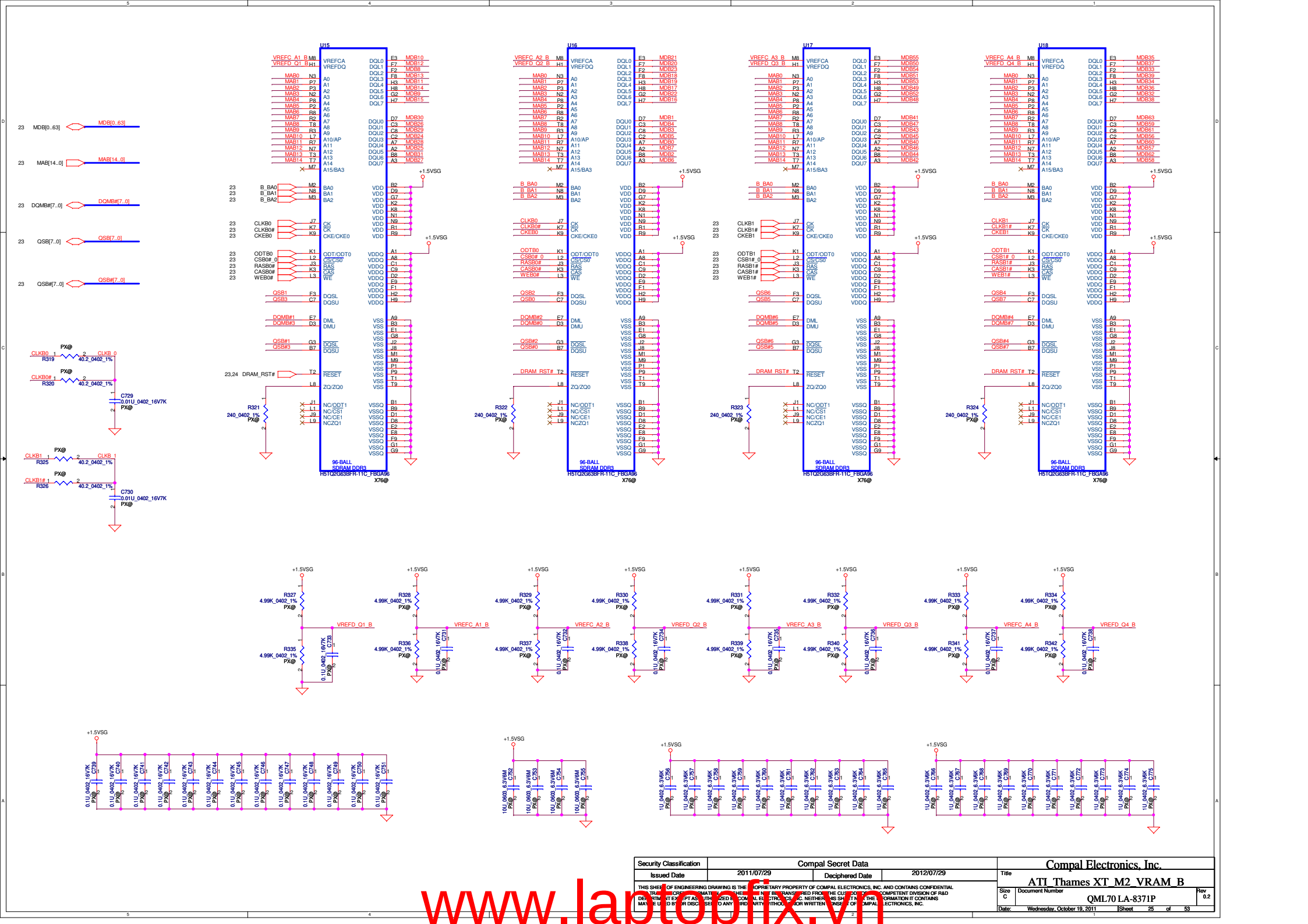
Compal Electronics, Inc.

Title: ATI_Thames XT_M2_VRAM_A

Size: C | Document Number: QML70 LA-8371P | Rev: 0.2

Date: Wednesday, October 19, 2011 | Sheet 24 of 53



Compal Electronics, Inc.

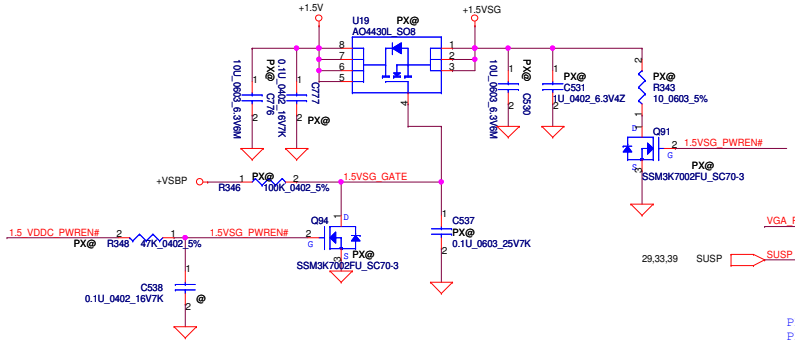
Title: ATI_Thames XT_M2_VRAM_B

Size	Document Number	Rev
C	QML70 LA-8371P	0.2

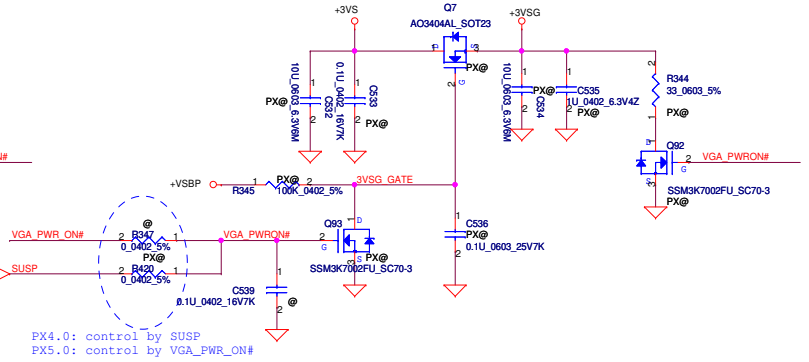
Date: Wednesday, October 19, 2011 | Sheet 25 of 53

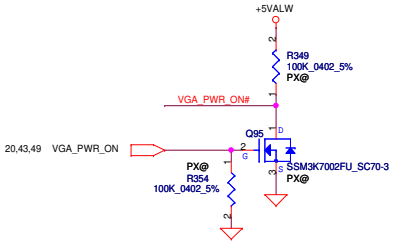
VGA Power

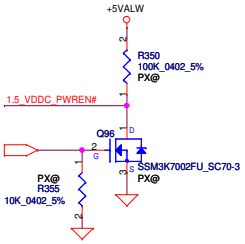
+1.5V to +1.5VSG (5.2A)

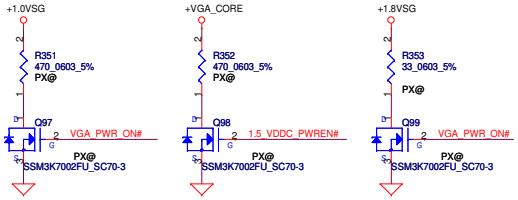


+3VS to +3VSG (60mA)









Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	QML70 LA-8371P	0.2

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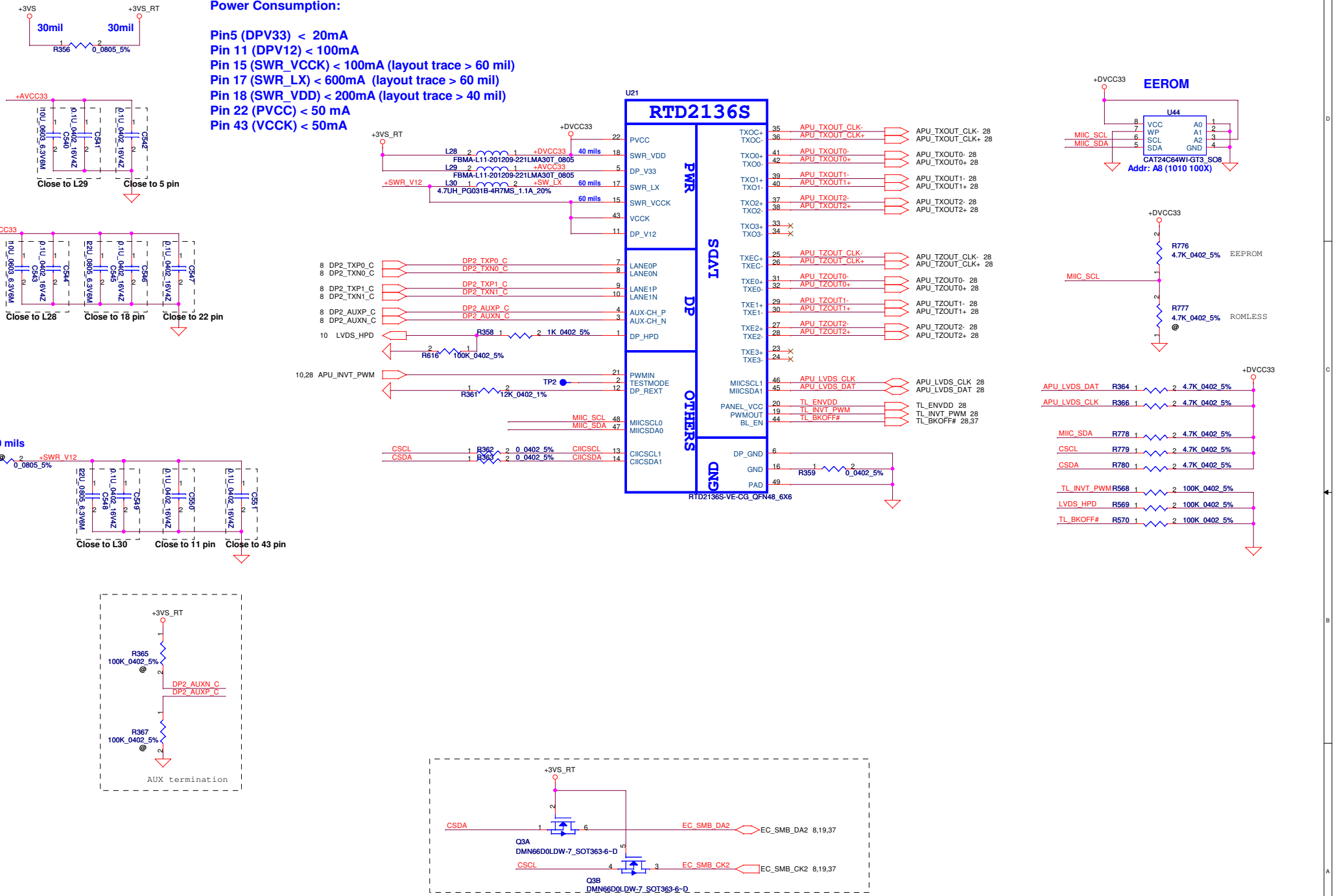
Power Consumption:

Pin5 (DPV33) < 20mA
Pin 11 (DPV12) < 100mA
Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
Pin 22 (PVCC) < 50 mA
Pin 43 (VCCK) < 50mA



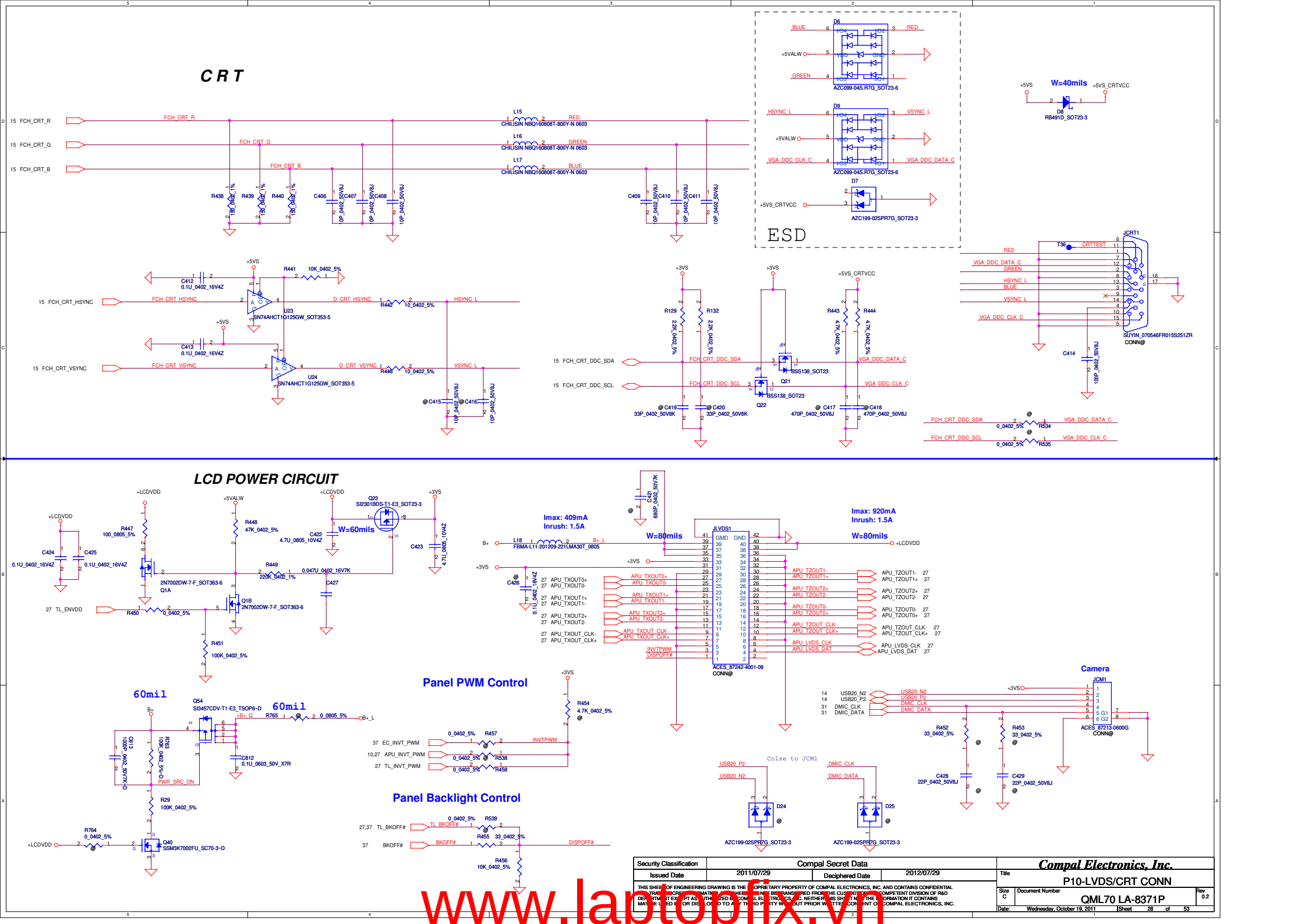
Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

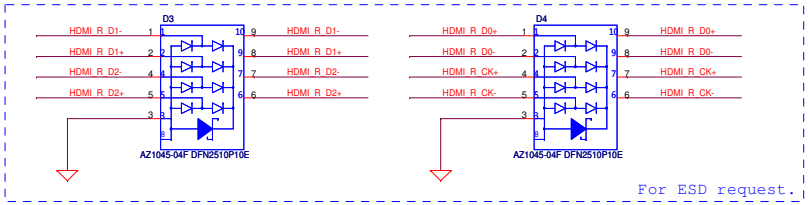
Compal Electronics, Inc.

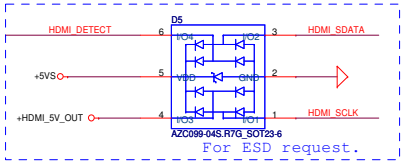
Title: LVDS Translator - RTD2132S

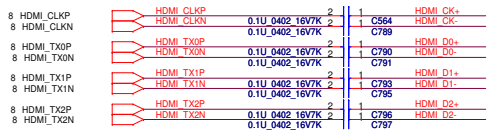
Size	Document Number	Rev
Custom	QML70 LA-8371P	0.11

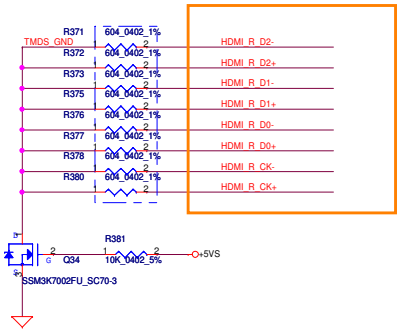
Date: Wednesday, October 19, 2011 Sheet 27 of 53

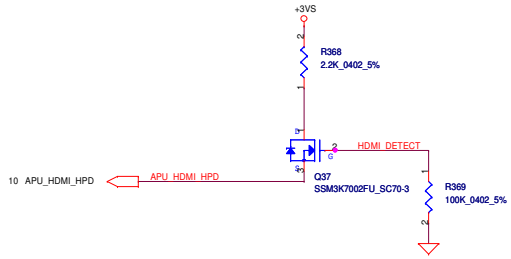


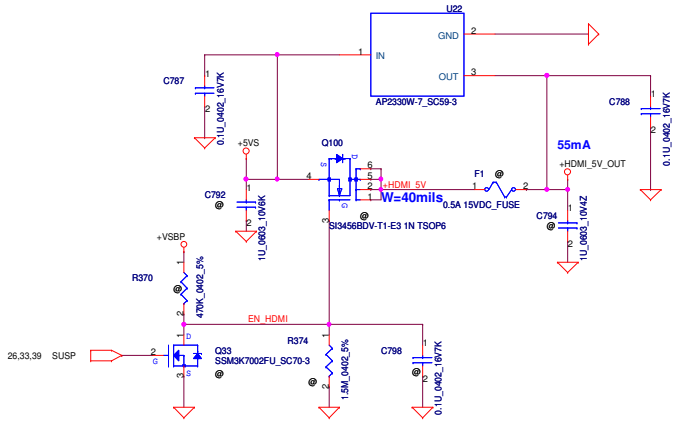


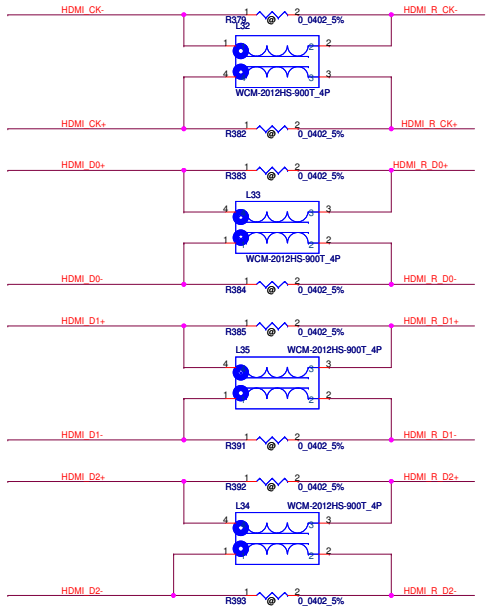


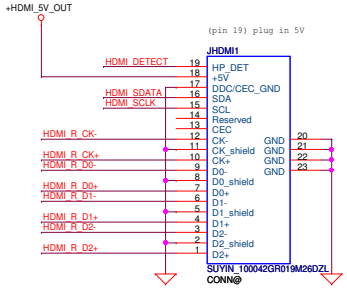


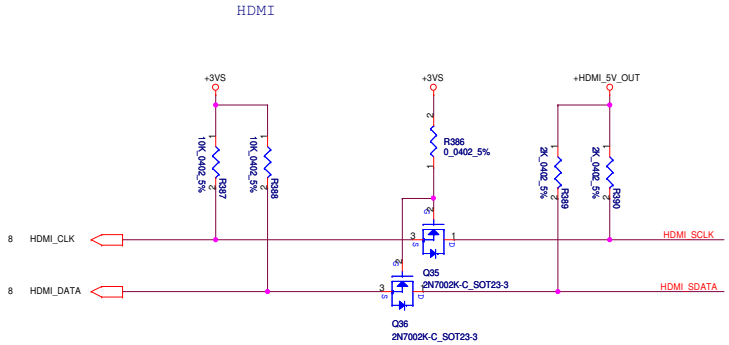












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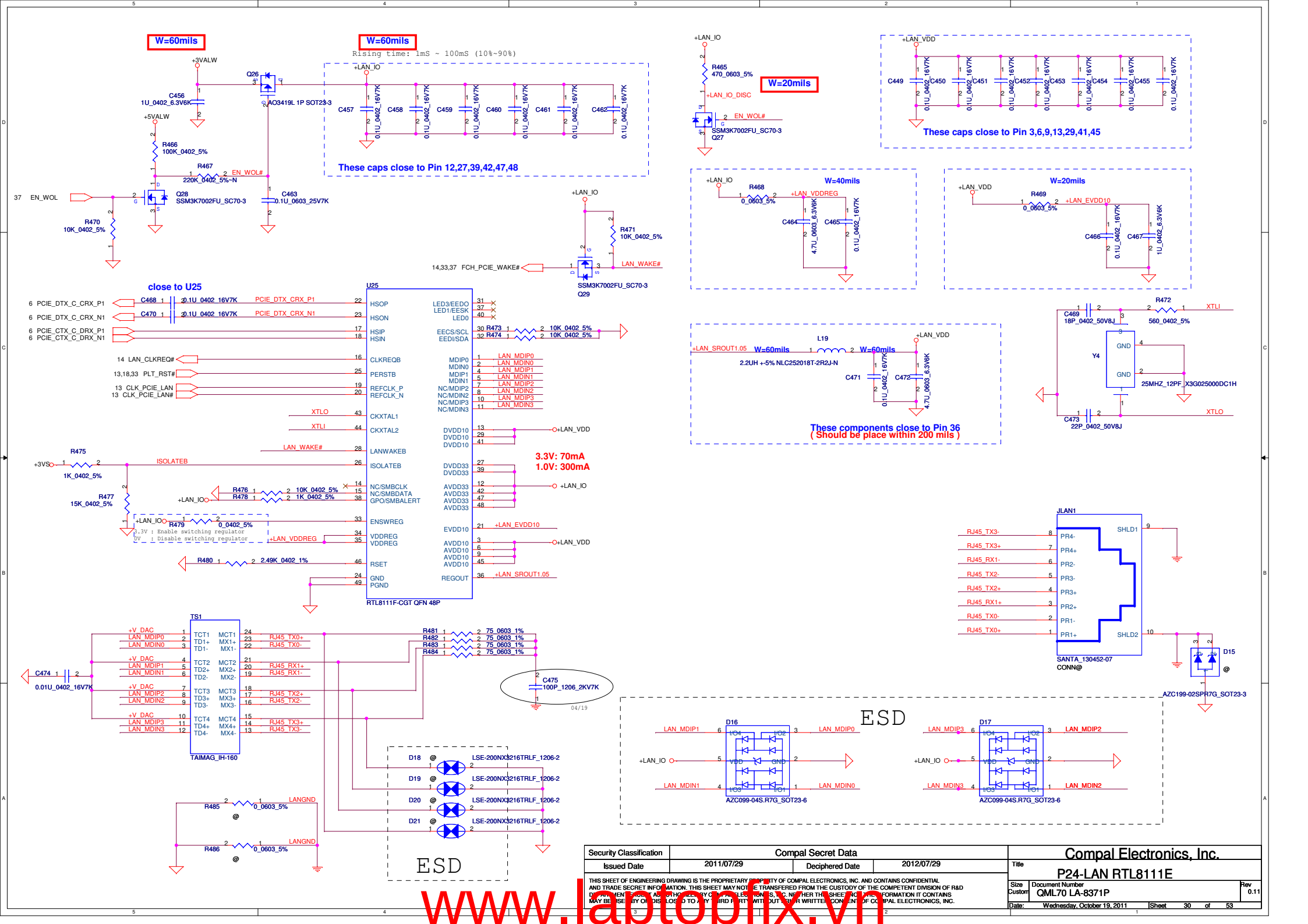
Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
C	QML70 LA-8371P	0.2

Date: Wednesday, October 19, 2011 | Sheet 29 of 53



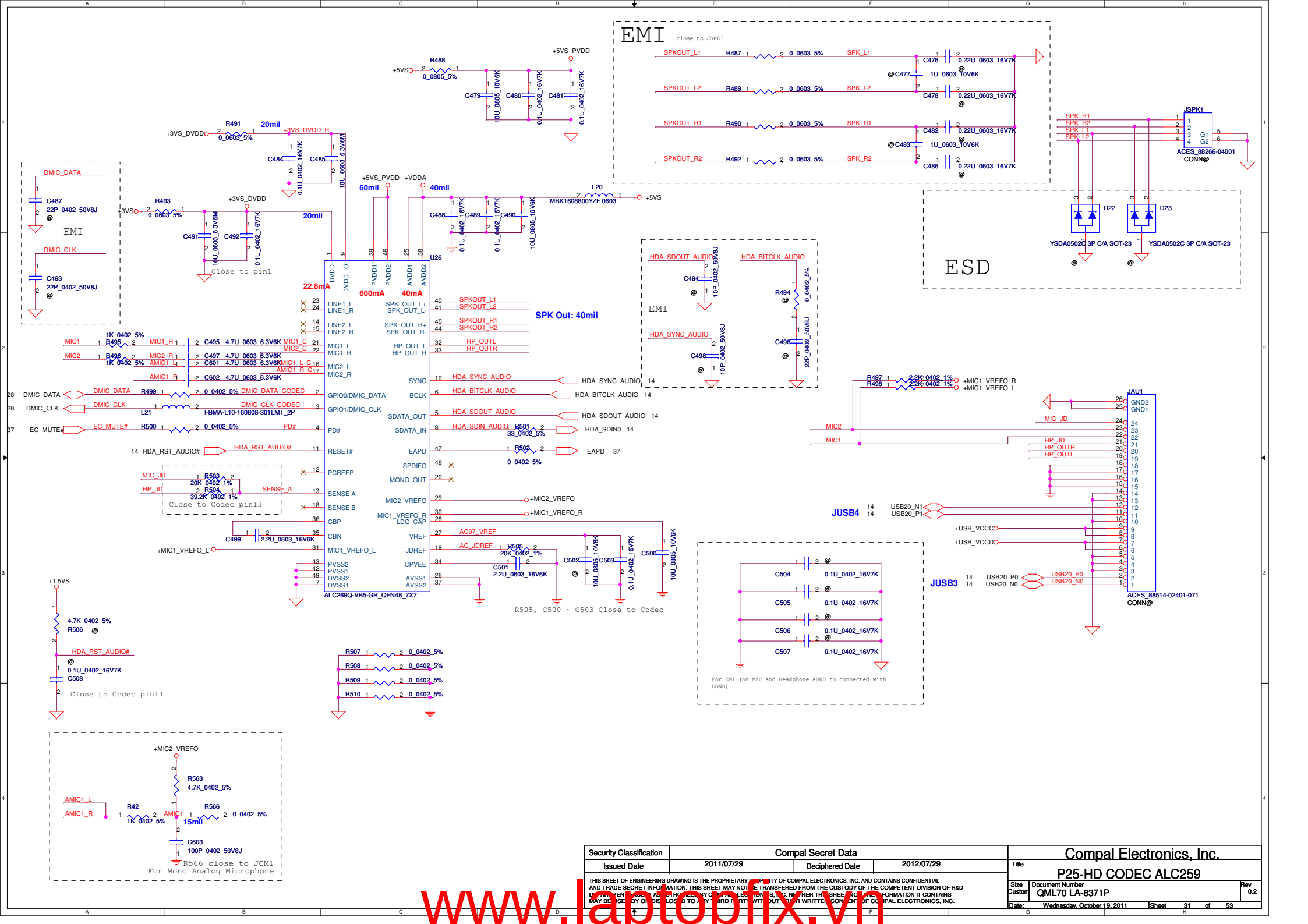
Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: P24-LAN RTL8111E

Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.11

Date: Wednesday, October 19, 2011 | Sheet 30 of 53



Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

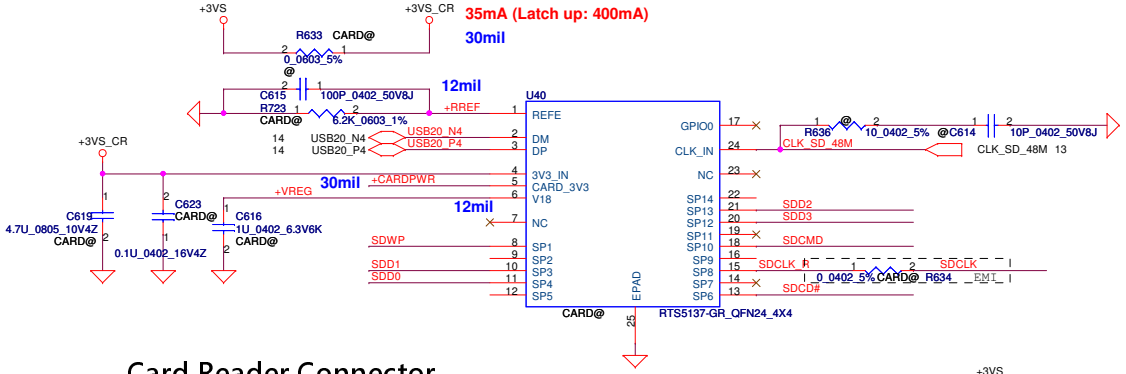
Compal Electronics, Inc.

Title: P25-HD CODEC ALC259

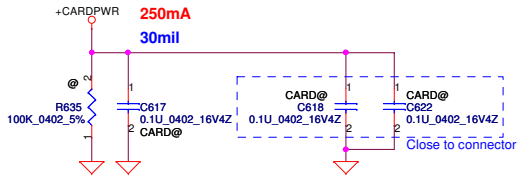
Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.2

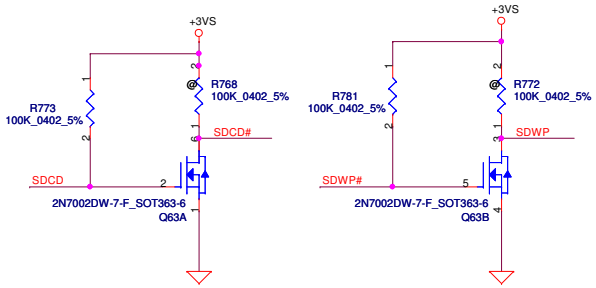
Date: Wednesday, October 19, 2011 | Sheet 31 of 53

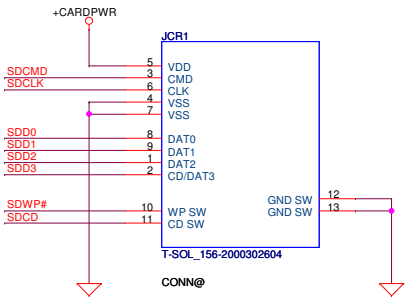
Card Reader RTS5137
(only SD/MMC/MS function)

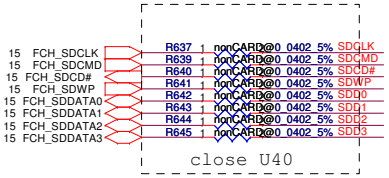


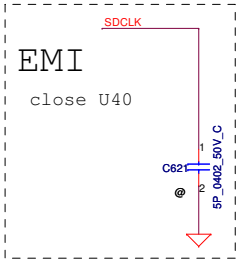
Card Reader Connector

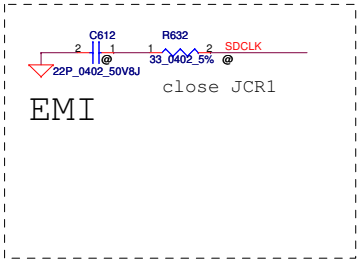


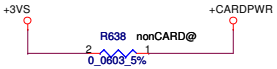












Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: P26-RTS5137 Media Card Controller

Size	Document Number	Rev
Custom	QML70 LA-8371P	0.11

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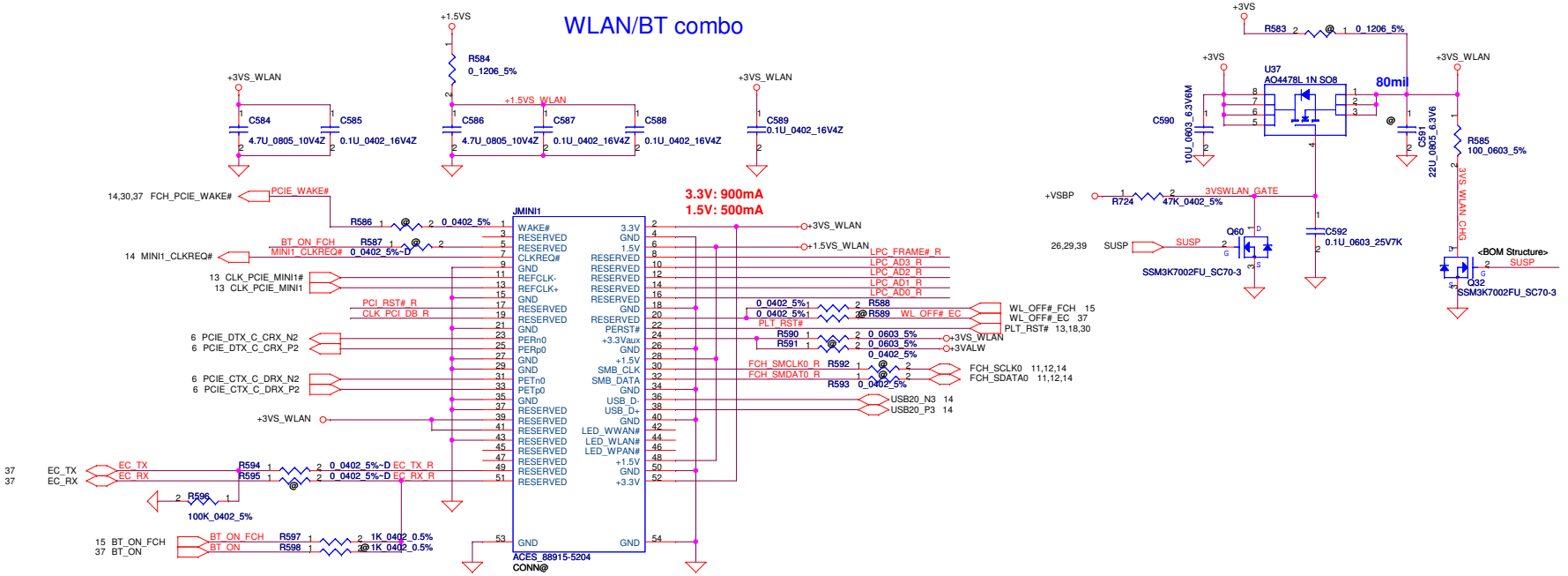
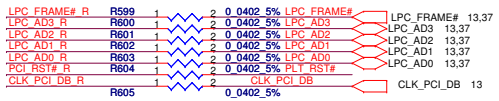
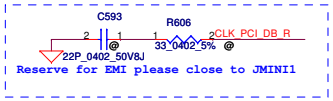
WLAN/BT combo



5.2 mm High

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.





Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: WLAN/ WWAN/ m-SATA

Size	Document Number	Rev
Custom	QML70 LA-8371P	0.2

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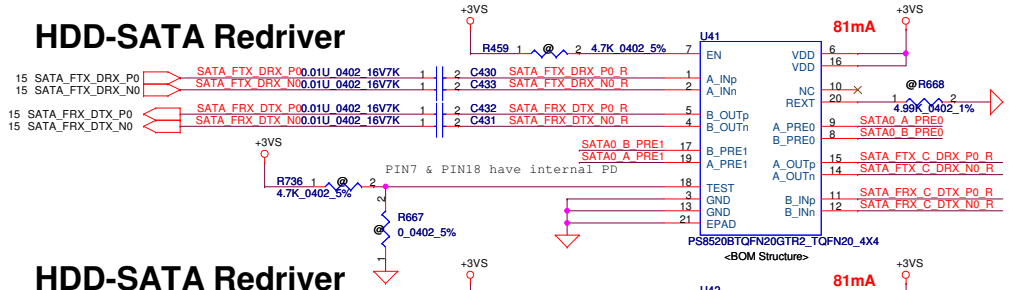
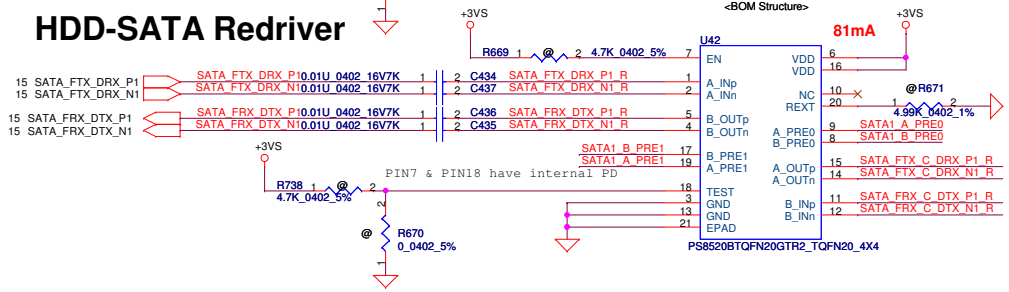
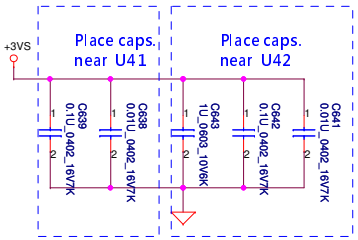
HDD-SATA Redriver

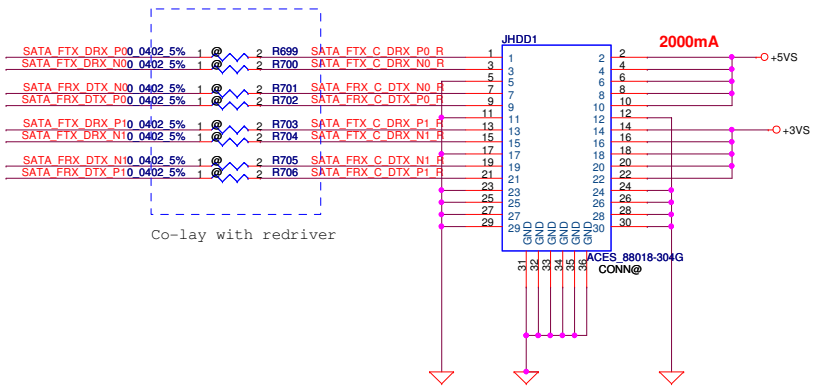


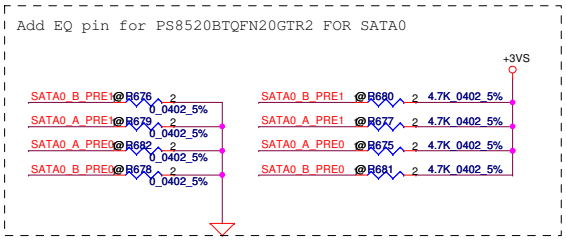
HDD-SATA Redriver

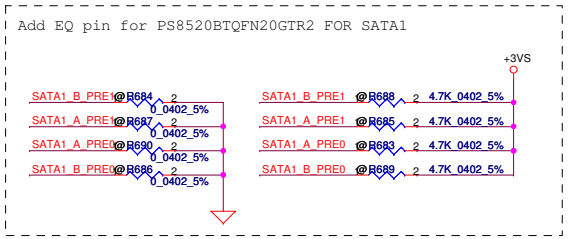


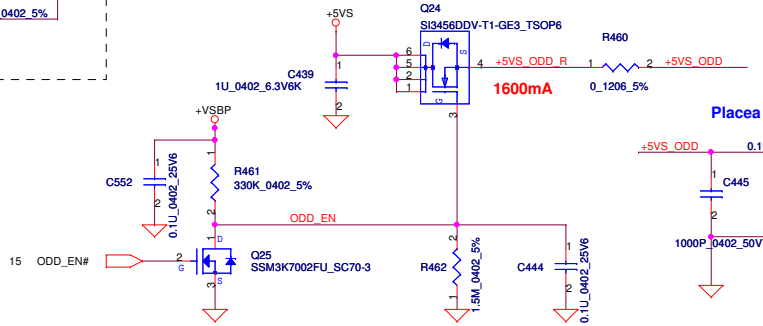


SATA HDD BTB Conn.

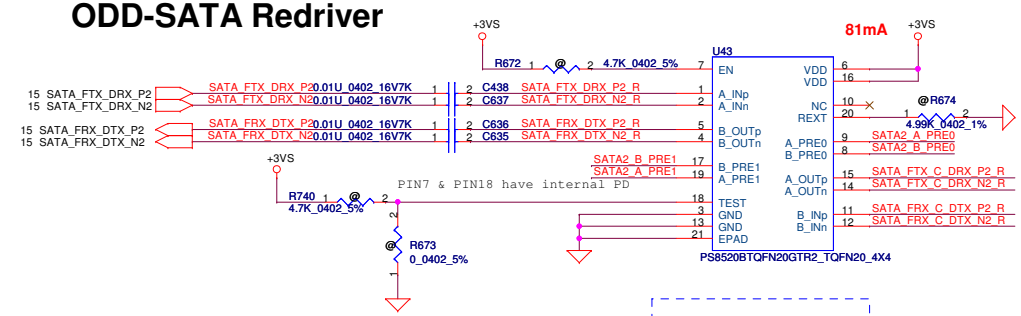


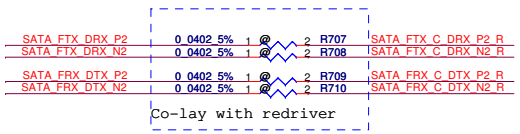


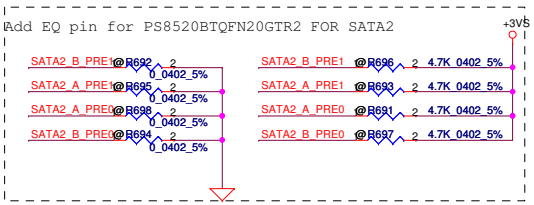


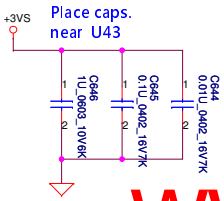


ODD-SATA Redriver

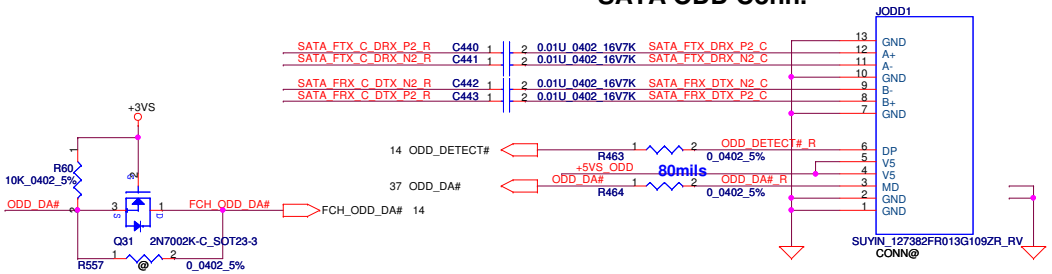








SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: P28-HDD & ODD CONN

Size	Document Number	Rev
B	QML70 LA-8371P	0.11

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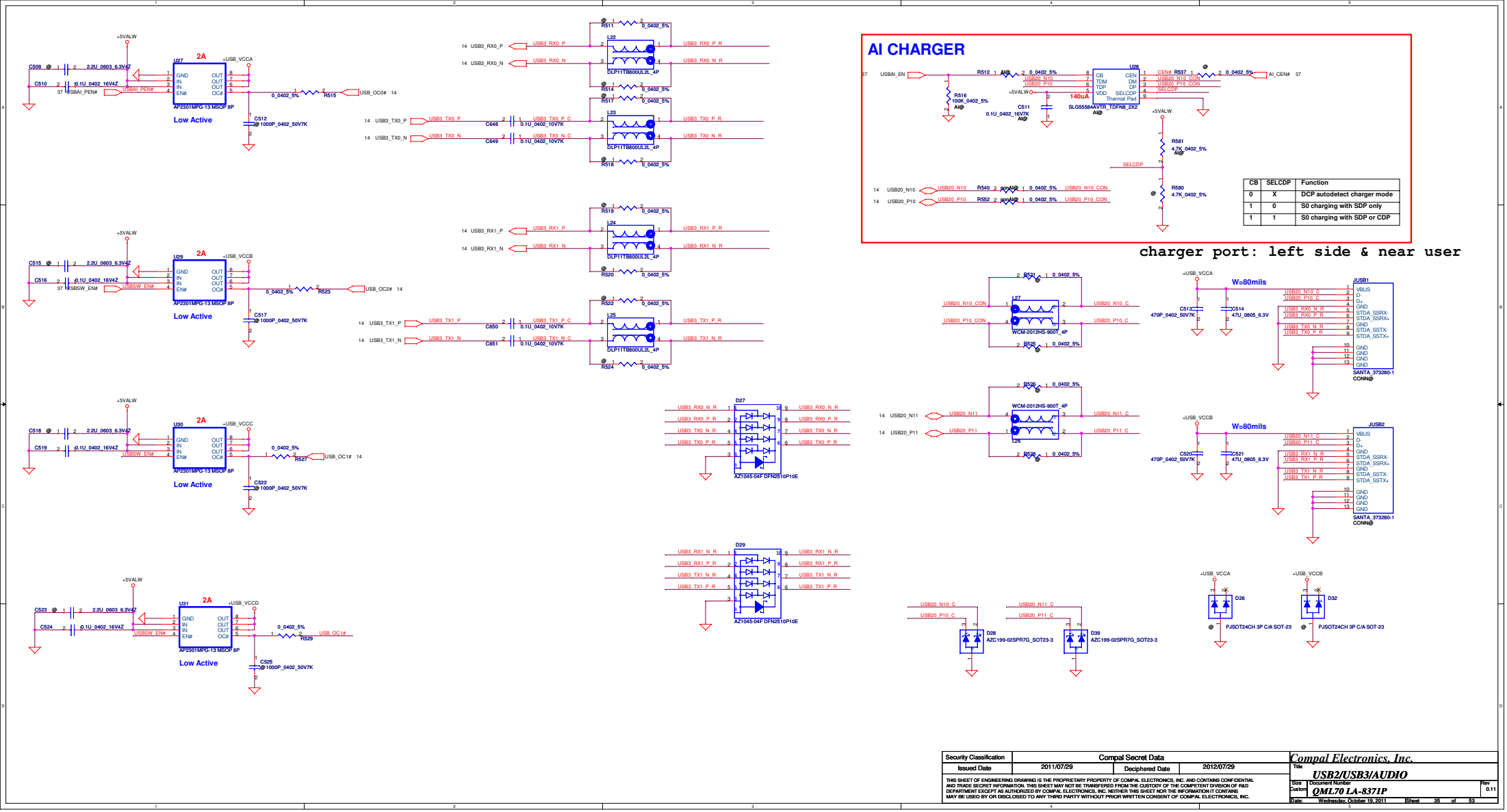
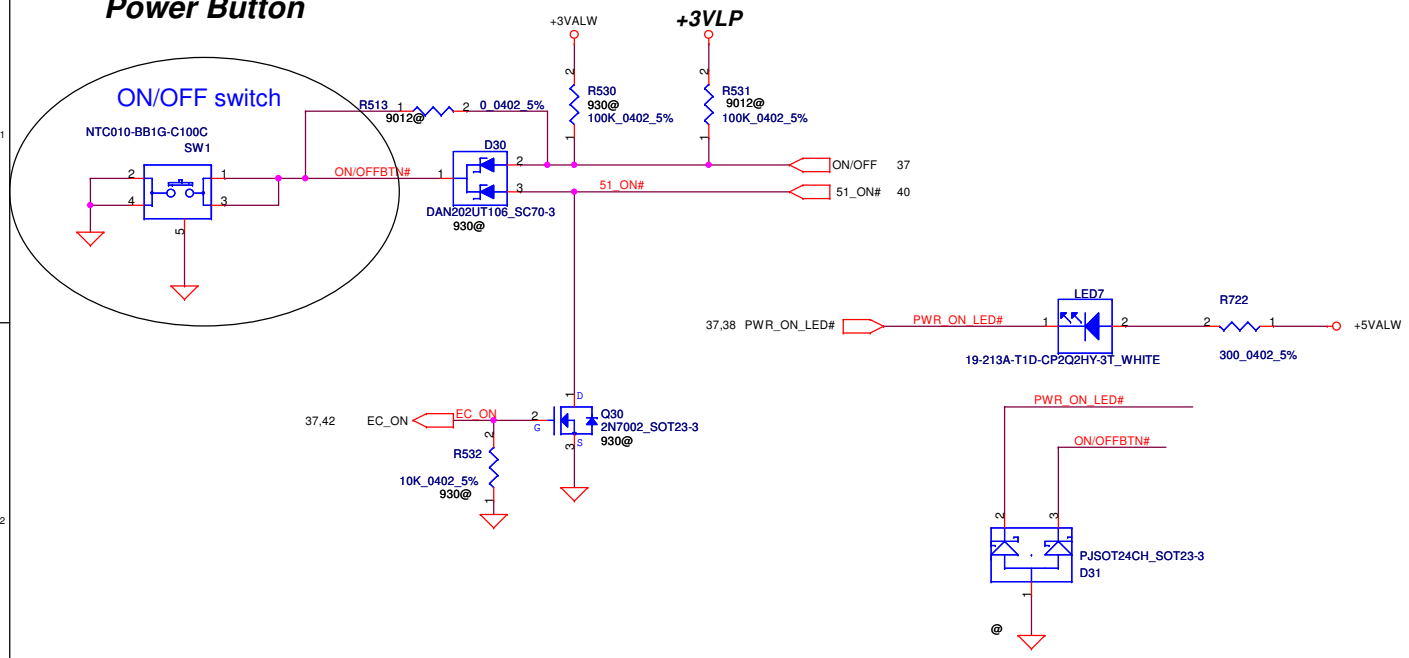
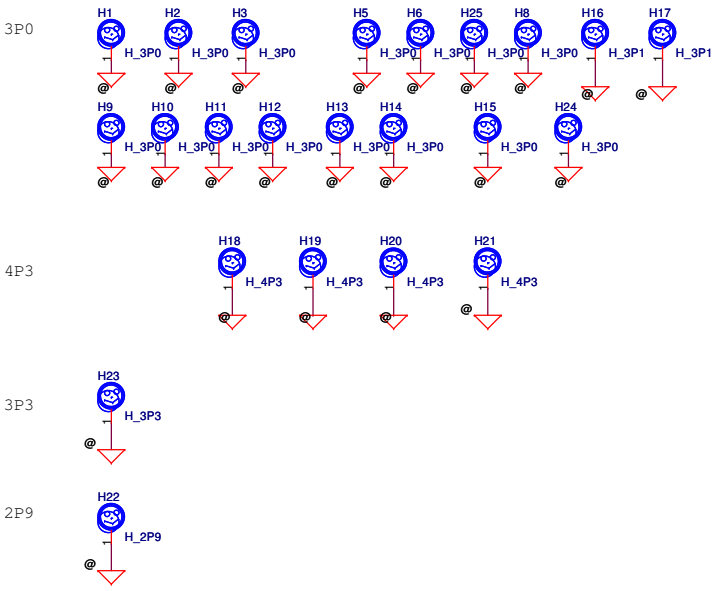


CB	SELCDP	Function
0	X	DCP autodetect charger mode
1	0	S0 charging with SDP only
1	1	S0 charging with SDP or CDP

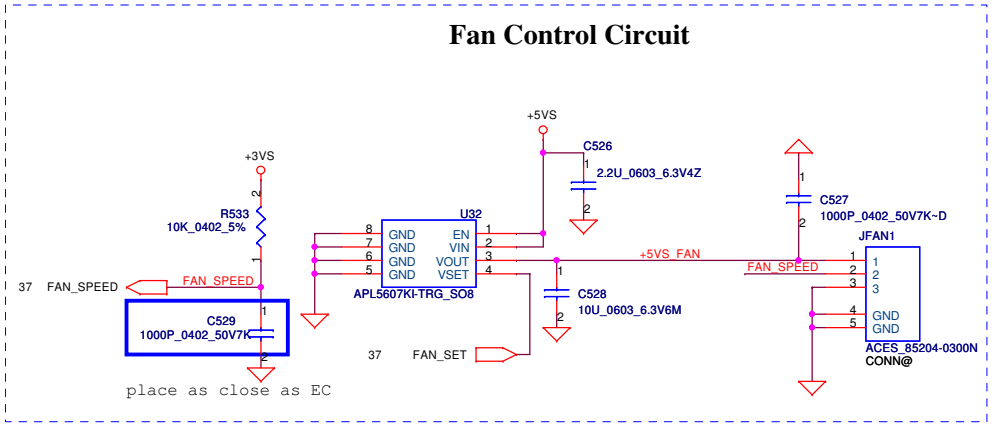
Power Button



Screw Hole



Fan Control Circuit



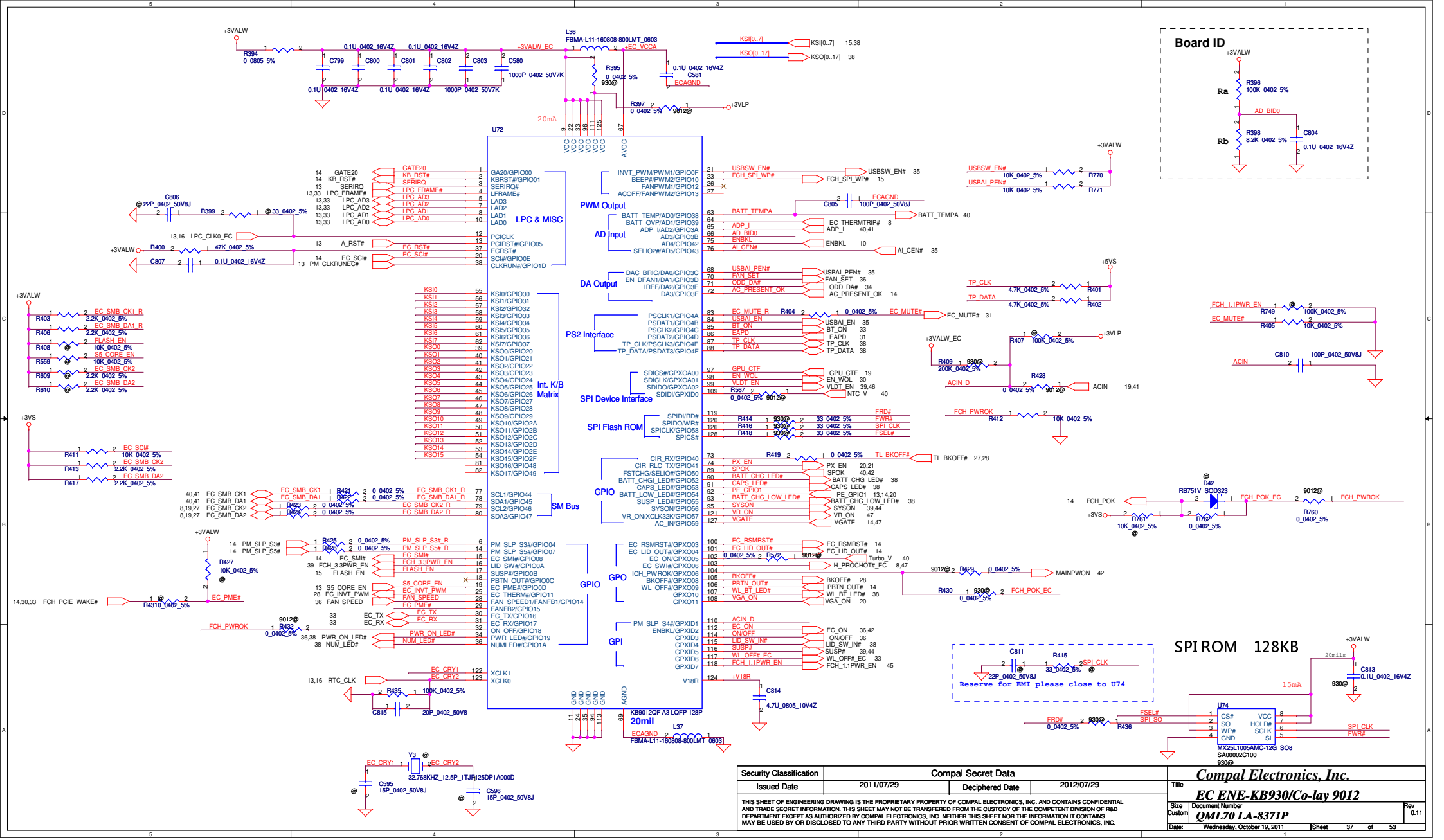
Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

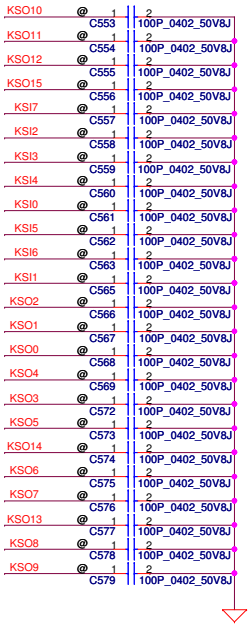
Compal Electronics, Inc.

Title: PWRBTN/ FAN / Screws

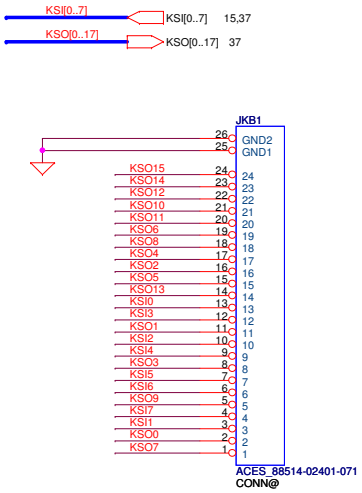
Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.11

Date: Wednesday, October 19, 2011 | Sheet 36 of 53

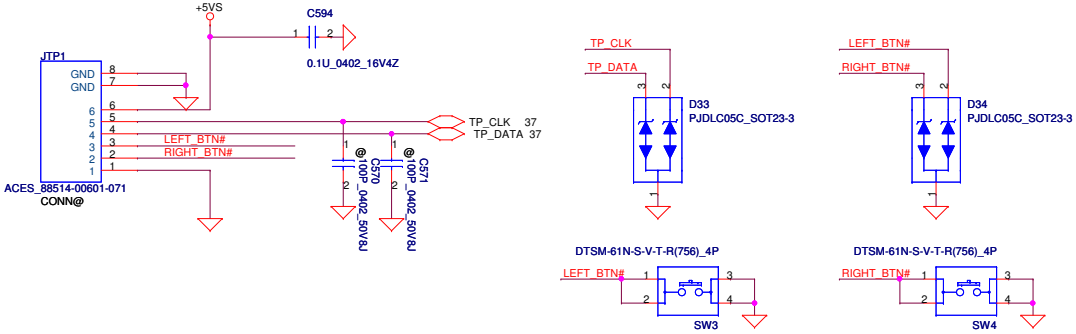




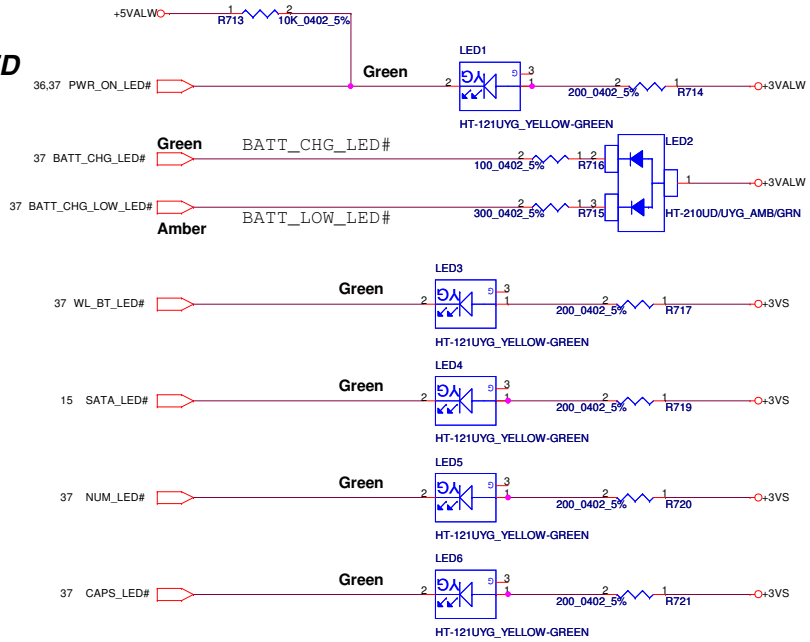
INT_KBD Conn.



Touch/B Connector

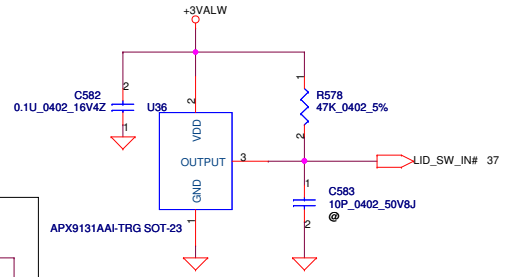


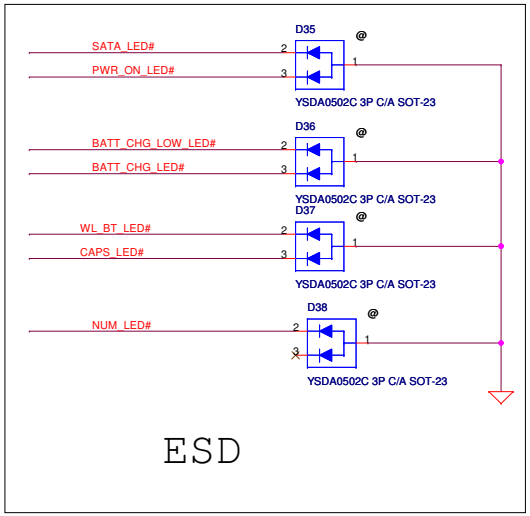
LED



Lid Switch

(Hall Effect Switch)





Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: KB/EC ROM/TP/FUN/LED

Size	Document Number	Rev
B	QML70 LA-8371P	0.2

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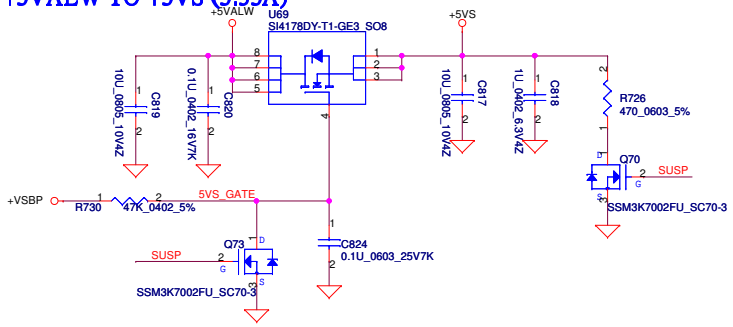
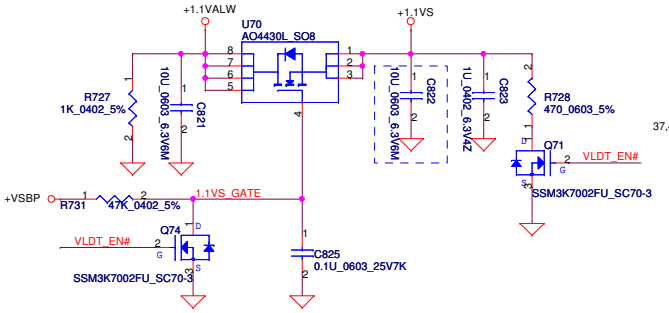
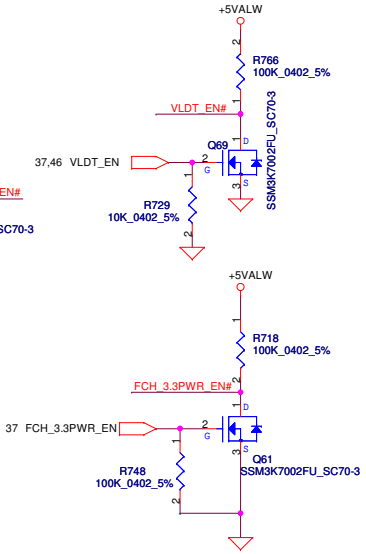
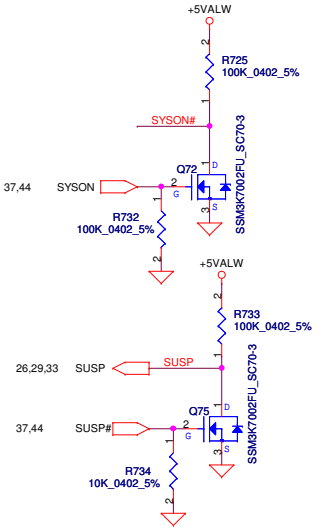
+5VALW TO +5VS (5.35A)



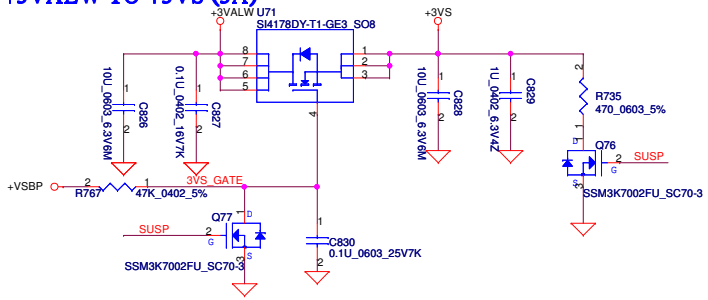
+1.1VALW TO +1.1VS (4A)





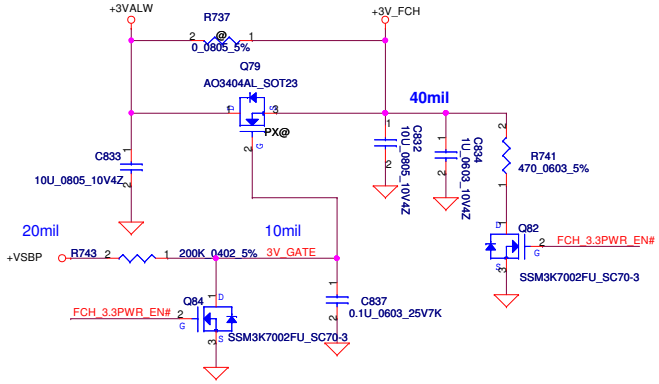


+3VALW TO +3VS (3A)

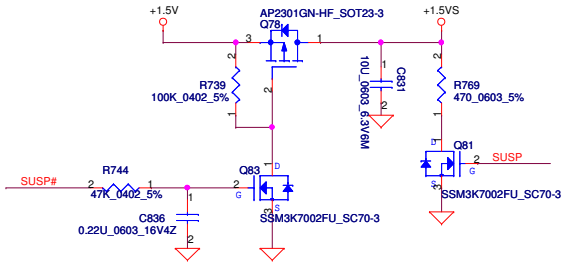


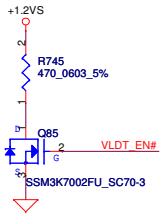
Instant On

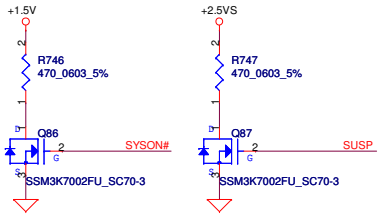
+3VALW TO +3V_FCH (1A)

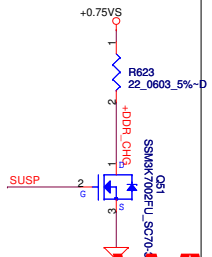


+1.5V TO +1.5VS (0.5A)









Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
B	QML70 LA-8371P	0.11

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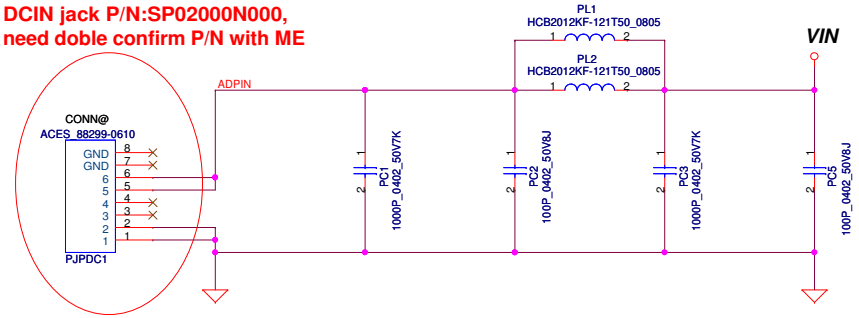
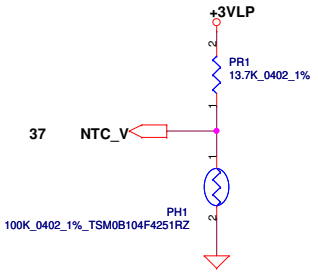
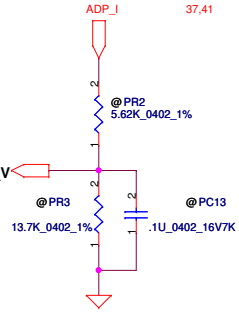
DCIN jack P/N:SP02000N000,
need doble confirm P/N with ME

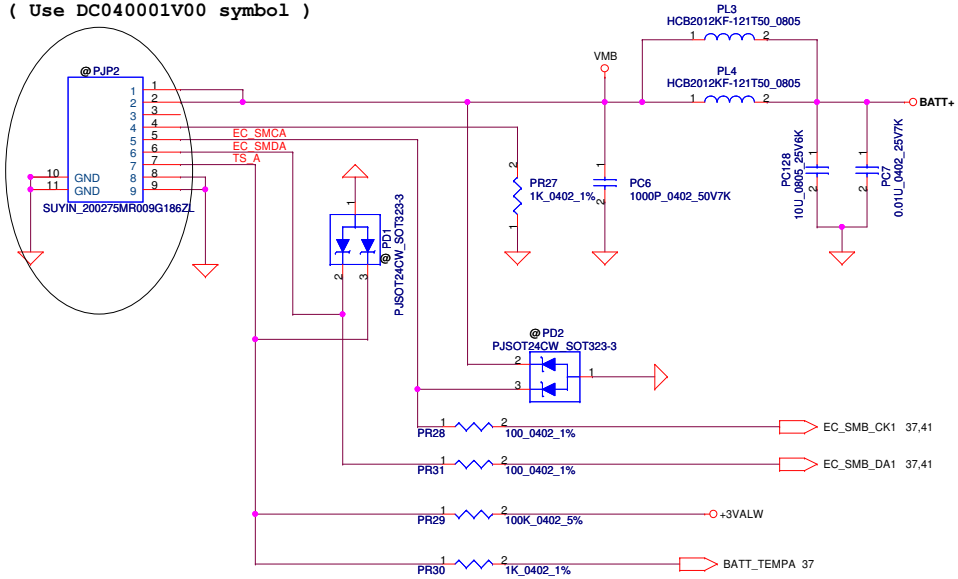


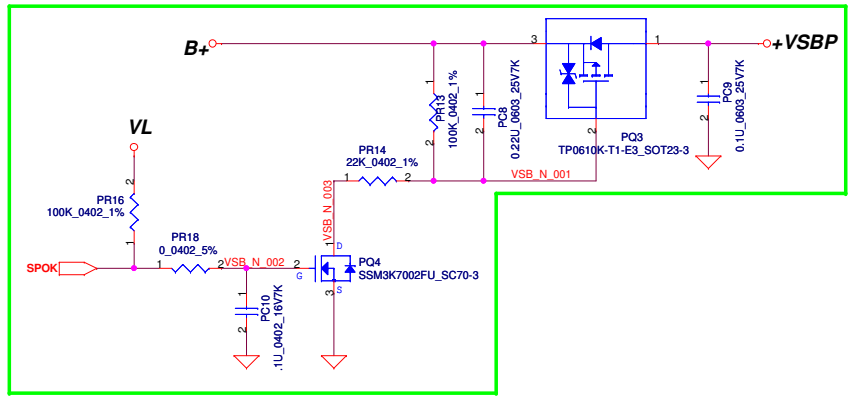
PH901 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C

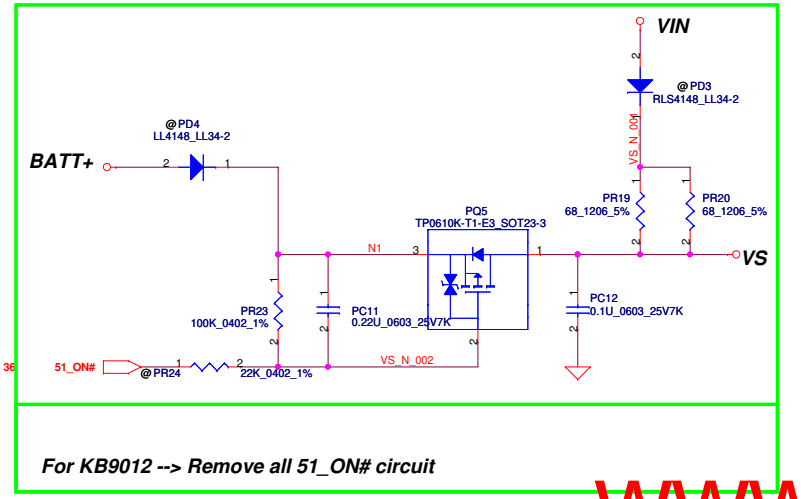




Change DC040007T0L to DC040004L00
(Use DC040001V00 symbol)

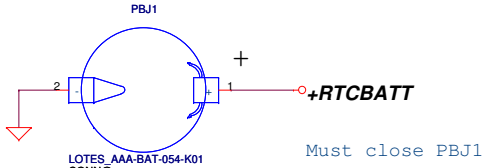






For KB9012 --> Remove all 51_ON# circuit

RTC Battery



Must close PBJ1

Change RTC For Cost Down
SP07000H700

Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.	
Title	PWR-DCIN / BATT CONN / OTP
Size	Document Number: QML70 LA-8371P
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Date:	Wednesday, October 19, 2011
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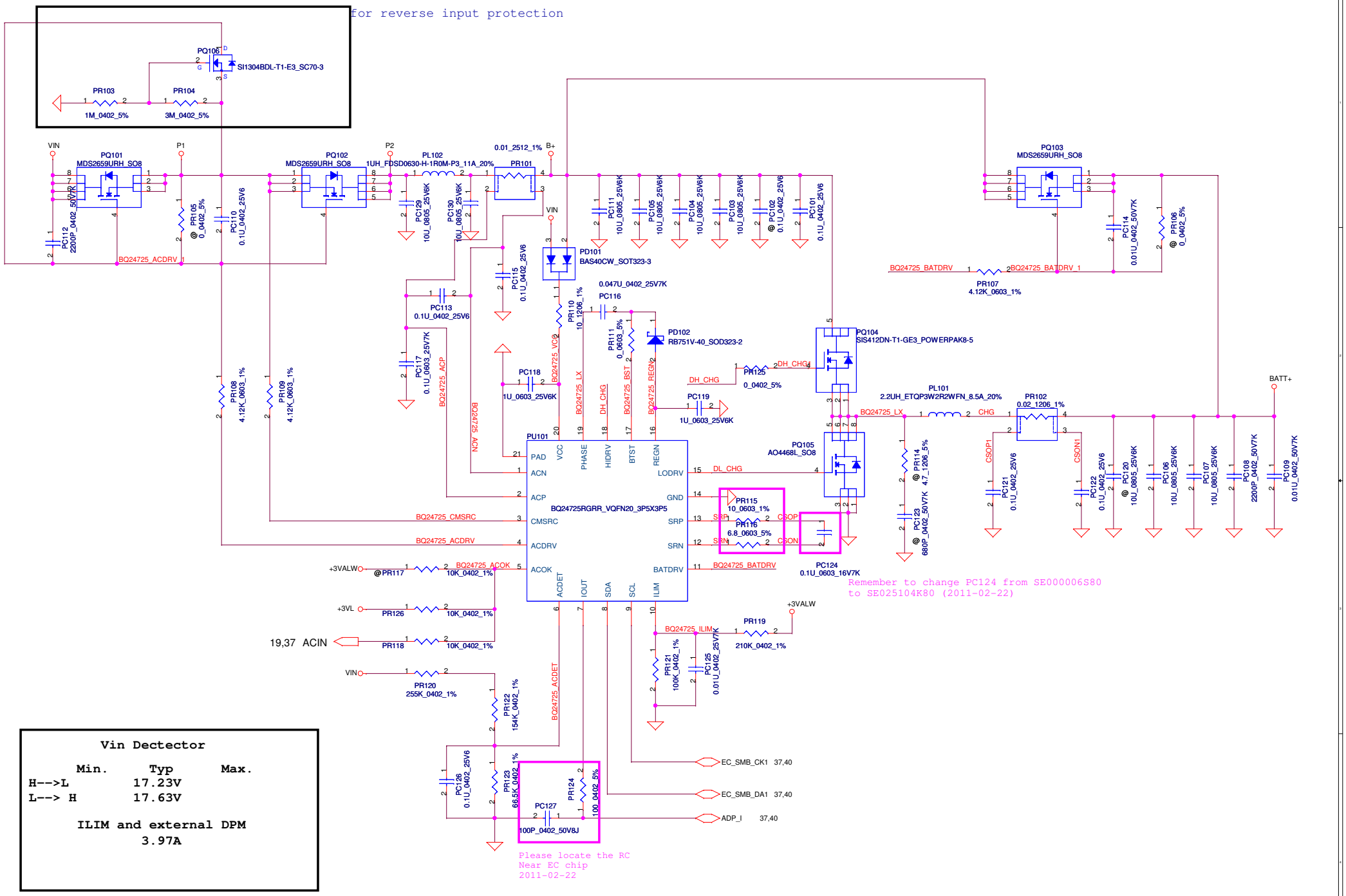
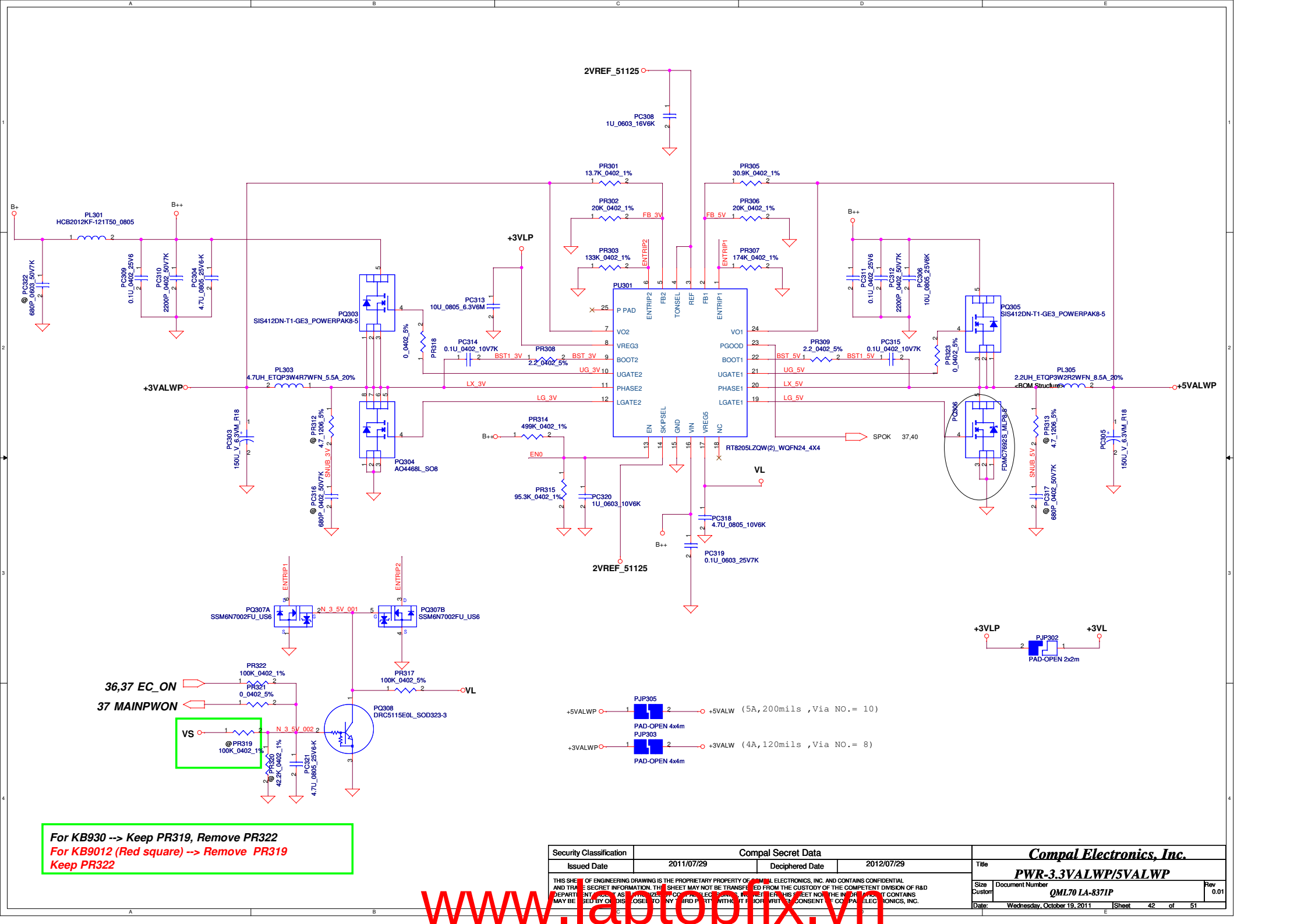
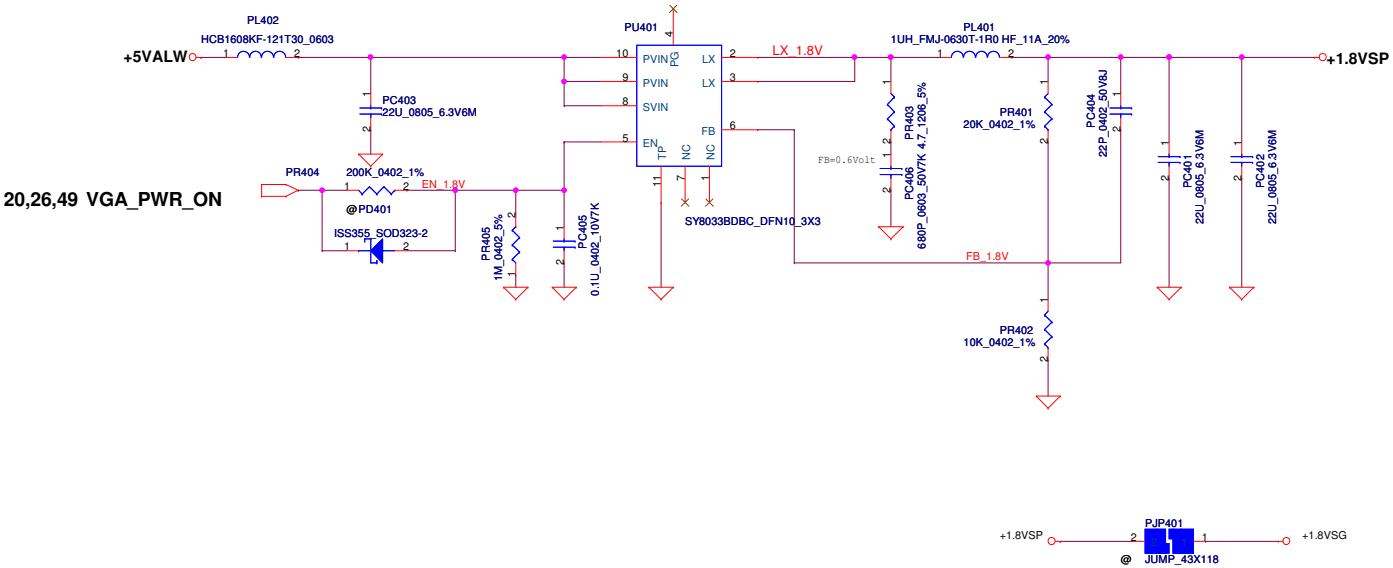


Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.	
Title	PWR-CHARGER
Size	Document Number: QML70 LA-8371P
Rev	0.2
Date: Wednesday, October 19, 2011	Sheet 41 of 53





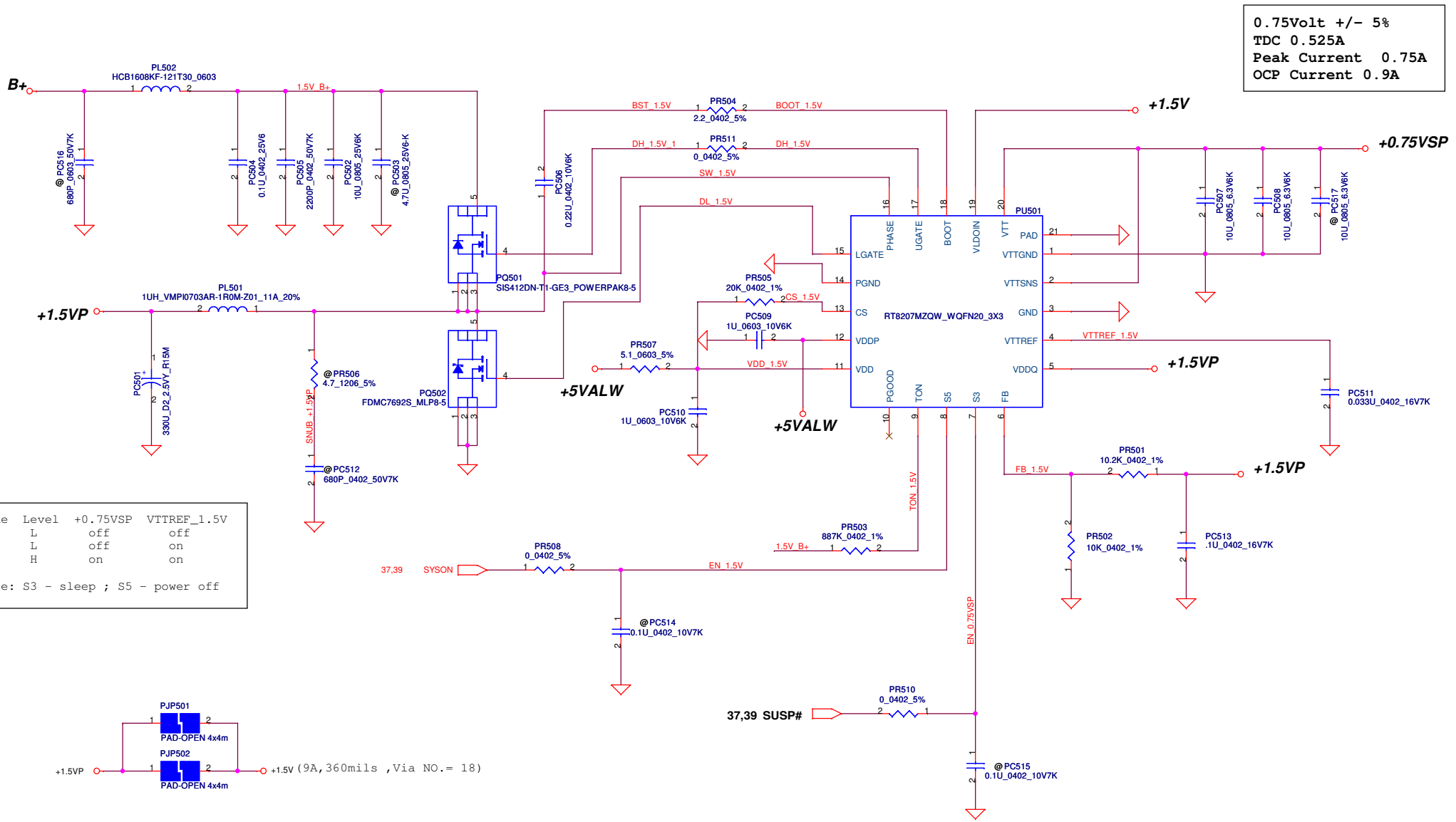
Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	

Compal Electronics, Inc.

Title: +1.8VP

Size	Document Number	Rev
	QML70 LA-8371P	0.01

Date: Wednesday, October 19, 2011 | Sheet 43 of 51



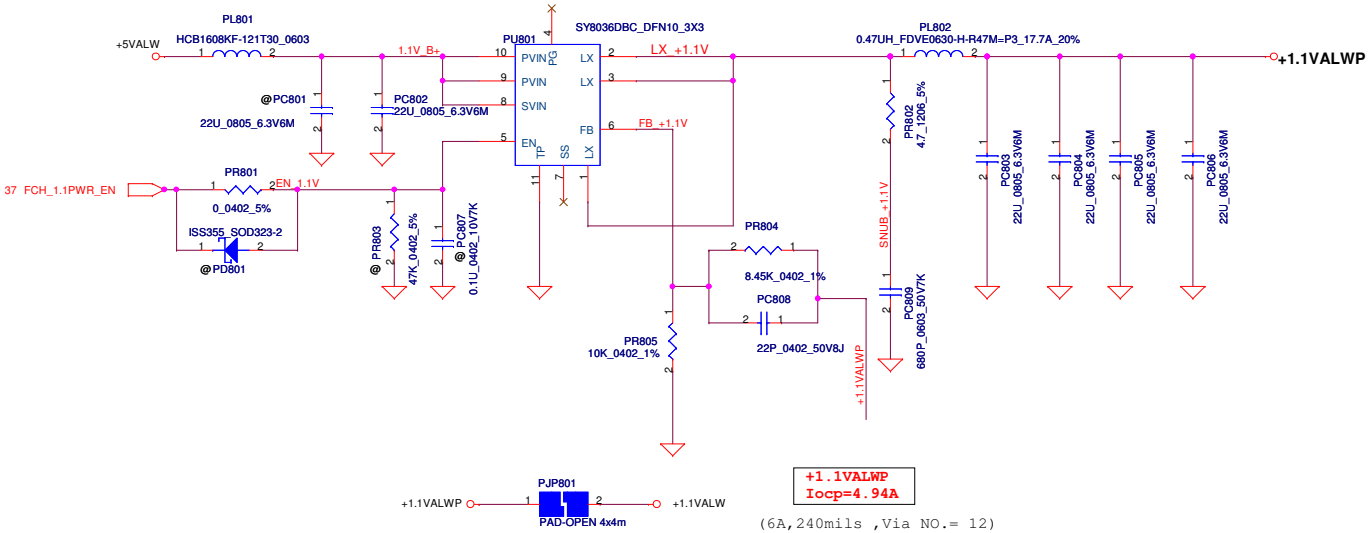
Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: PWR-1.5VP / +0.75VSP

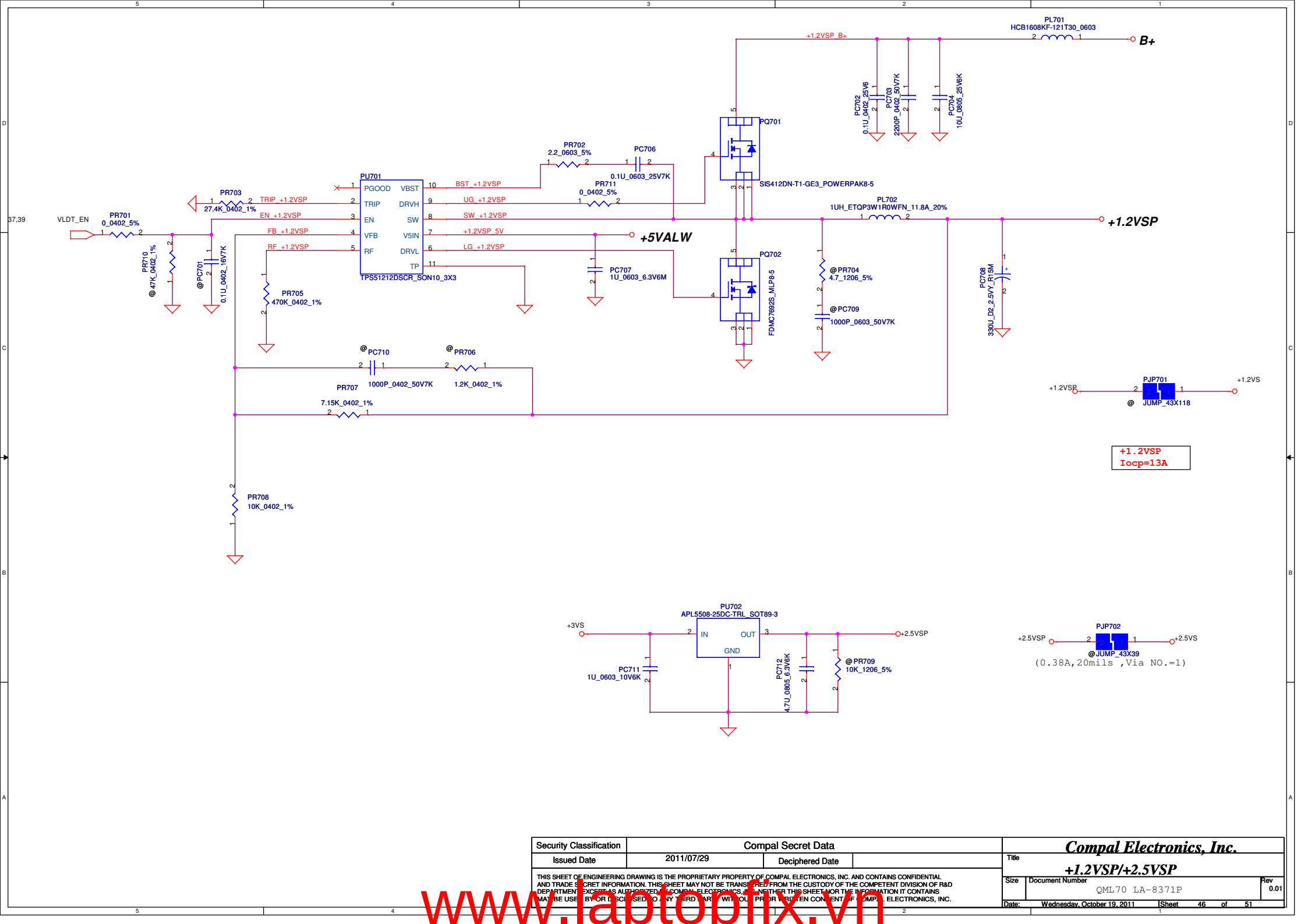
Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.01

Date: Wednesday, October 19, 2011 | Sheet 44 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	

Compal Electronics, Inc.		
Title	+1.1VALWP	
Size	Document Number	Rev
	QML70 LA-8371P	0.01
Date: Wednesday, October 19, 2011	Sheet 45 of 51	



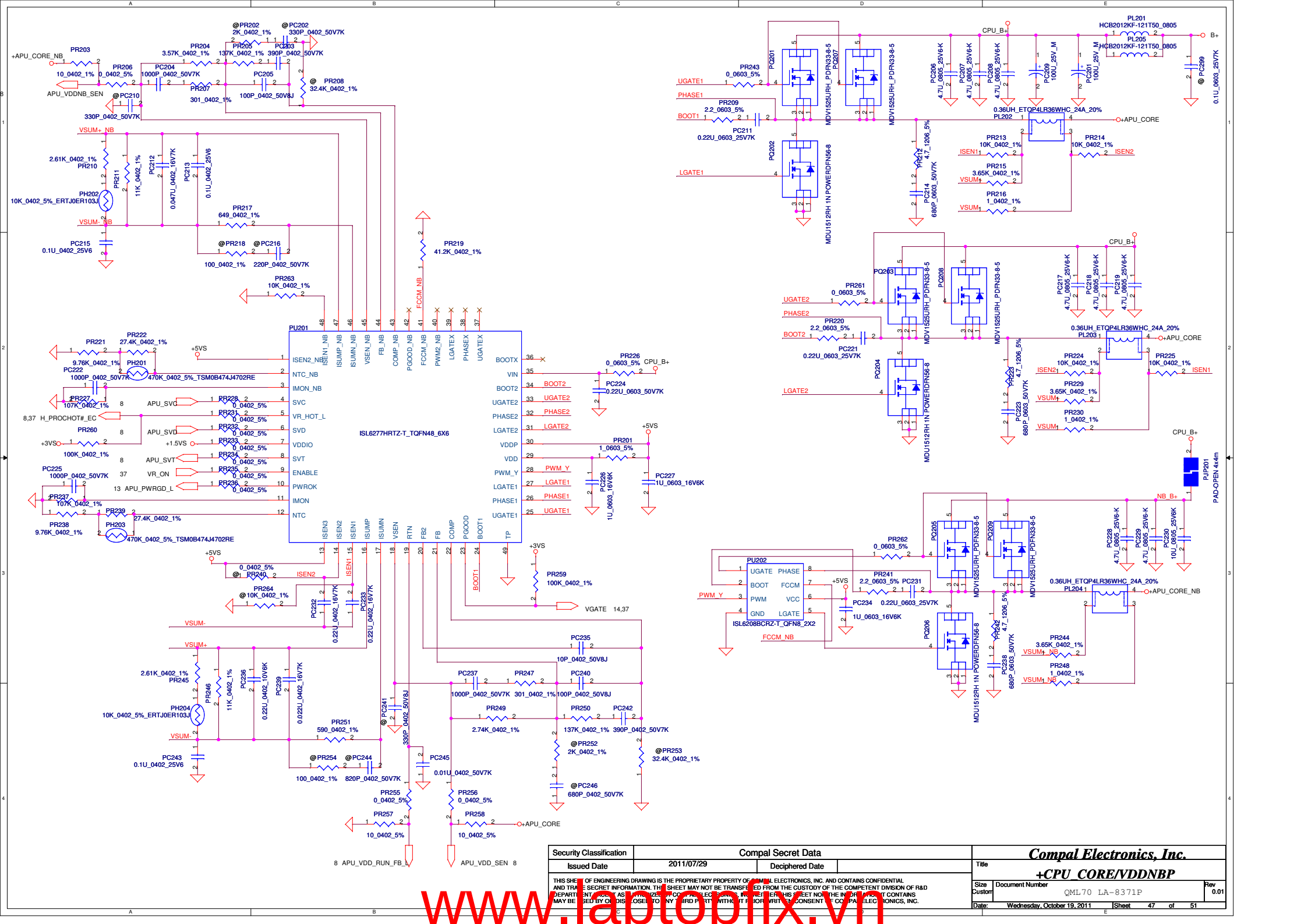
Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	

Compal Electronics, Inc.

Title: +1.2VSP/+2.5VSP

Size	Document Number	Rev
	QML70 LA-8371P	0.01

Date: Wednesday, October 19, 2011 | Sheet 46 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	

Compal Electronics, Inc.

Title: +CPU_CORE/VDDNBP

Size	Document Number	Rev
Custom	QML70 LA-8371P	0.01

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+APU_CORE

+APU_CORE

PC247 22U_0805_6.3V6M
PC248 22U_0805_6.3V6M
PC249 22U_0805_6.3V6M
PC250 22U_0805_6.3V6M
PC251 22U_0805_6.3V6M
PC257 22U_0805_6.3V6M
PC258 22U_0805_6.3V6M
PC261 22U_0805_6.3V6M
PC262 22U_0805_6.3V6M
PC259 22U_0805_6.3V6M
@ PC263 22U_0805_6.3V6M
@ PC264 22U_0805_6.3VAM
@ PC265 22U_0805_6.3V6M
PC273 0.22U_0402_16V7K
PC274 0.22U_0402_16V7K
PC277 0.01U_0402_50V7K
PC278 0.01U_0402_50V7K
PC279 0.01U_0402_50V7K
PC280 180P_0402_50V8J
PC281 180P_0402_50V8J

+APU_CORE Local

PC268 330U_D2_2V_Y
PC269 330U_D2_2V_Y
PC270 330U_D2_2V_Y
PC271 330U_D2_2V_Y

+APU_CORE_NB

+APU_CORE_NB

PC252 22U_0805_6.3V6M
@ PC253 22U_0805_6.3V6M
PC254 22U_0805_6.3V6M
PC255 22U_0805_6.3V6M
PC256 10U_0805_6.3V6K
@ PC260 22U_0805_6.3V6M
PC275 0.22U_0402_16V7K
PC276 0.22U_0402_16V7K
PC282 180P_0402_50V8J
PC283 180P_0402_50V8J
PC284 180P_0402_50V8J

capacitors under processor on bottom side of board

+APU_CORE_NB Local

PC266 330U_D2_2V_Y
PC267 330U_D2_2V_Y

+VGA_CORE

+VGA_CORE +VDDC

PC932 10U_0603_6.3V6M
PC931 10U_0603_6.3V6M
PC923 10U_0603_6.3V6M
PC924 10U_0603_6.3V6M
PC925 10U_0603_6.3V6M
PC926 10U_0603_6.3V6M
PC928 10U_0603_6.3V6M
PC927 10U_0603_6.3V6M
PC929 10U_0603_6.3V6M
PC933 10U_0603_6.3V6M
PC965 1U_0402_6.3V6K
PC966 1U_0402_6.3V6K
PC964 1U_0402_6.3V6K
PC937 1U_0402_6.3V6K
PC938 1U_0402_6.3V6K
PC969 1U_0402_6.3V6K
PC940 1U_0402_6.3V6K
PC941 1U_0402_6.3V6K
PC942 1U_0402_6.3V6K
PC943 1U_0402_6.3V6K
PC944 1U_0402_6.3V6K
PC945 1U_0402_6.3V6K
PC946 1U_0402_6.3V6K
PC947 1U_0402_6.3V6K
PC948 1U_0402_6.3V6K
PC949 1U_0402_6.3V6K
PC950 1U_0402_6.3V6K
PC951 1U_0402_6.3V6K
PC952 1U_0402_6.3V6K
PC953 1U_0402_6.3V6K
PC970 1U_0402_6.3V6K
PC955 1U_0402_6.3V6K
PC971 1U_0402_6.3V6K
PC957 1U_0402_6.3V6K
PC958 1U_0402_6.3V6K
PC959 1U_0402_6.3V6K
PC960 1U_0402_6.3V6K
PC961 1U_0402_6.3V6K
PC962 1U_0402_6.3V6K
PC963 1U_0402_6.3V6K

+VGA_CORE +VDDCI

PJP902 JUMP_43X79 @

+VDDCI

PC934 1U_0402_6.3V6K
PC939 1U_0402_6.3V6K
PC935 1U_0402_6.3V6K
PC954 1U_0402_6.3V6K
PC968 1U_0402_6.3V6K
PC956 1U_0402_6.3V6K
PC936 1U_0402_6.3V6K
PC967 1U_0402_6.3V6K
PC972 1U_0402_6.3V6K
PC973 1U_0402_6.3V6K
PC921 10U_0603_6.3V6M
PC922 10U_0603_6.3V6M
PC930 10U_0603_6.3V6M

Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size	Document Number	Rev
A3	QML70 LA-8371P	0.01

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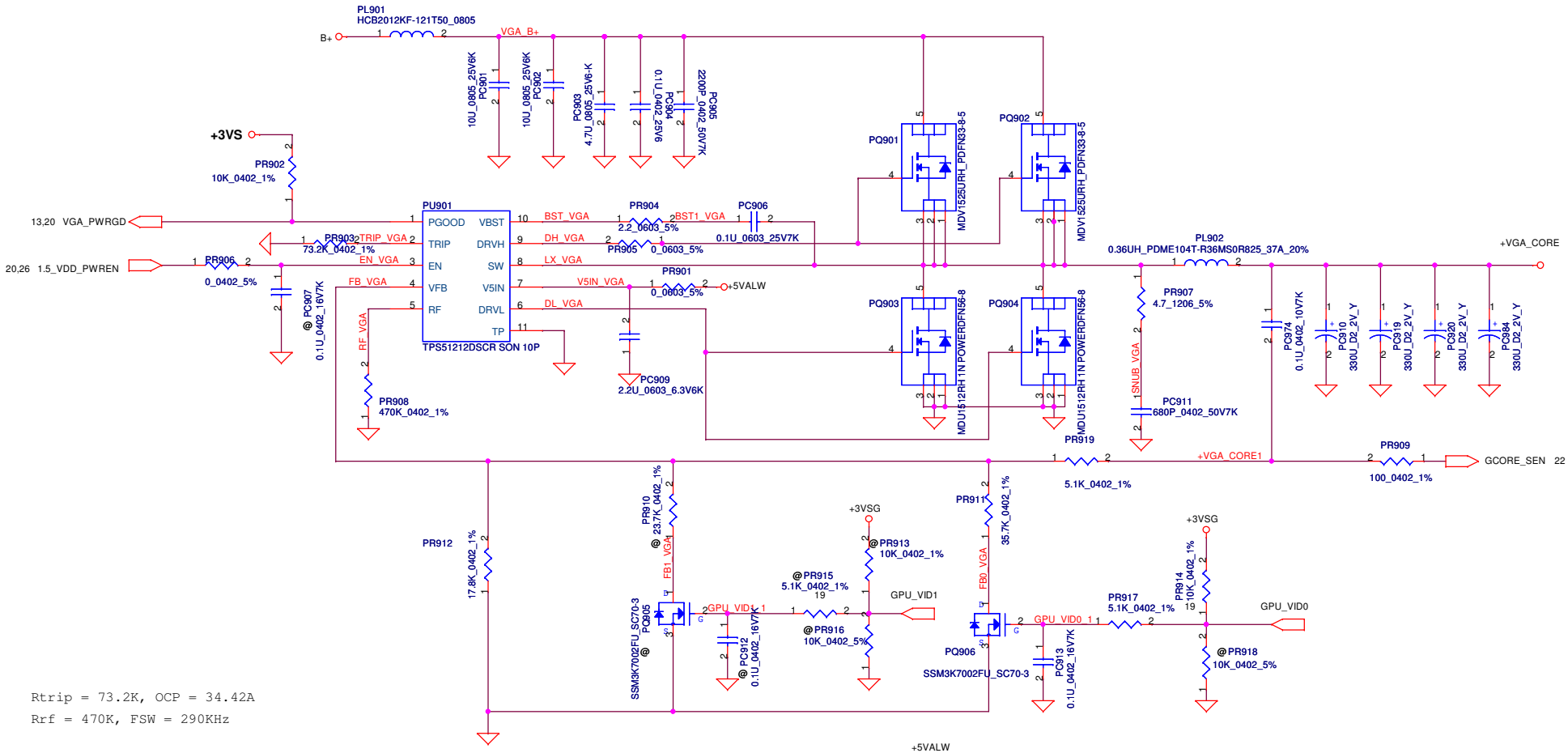
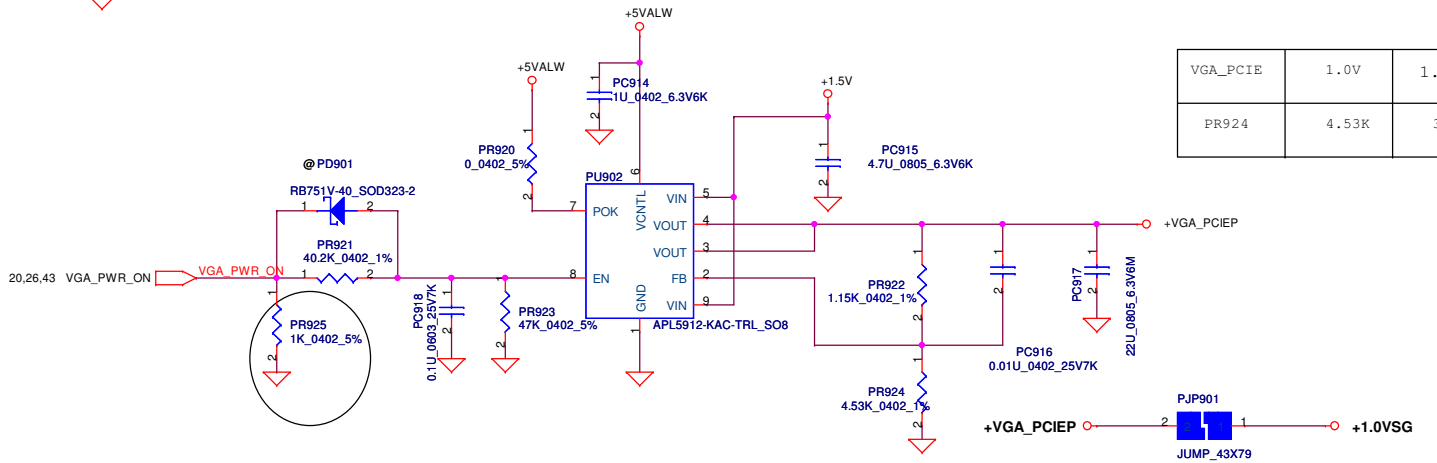


Rtrip = 73.2K, OCP = 34.42A
Rrf = 470K, FSW = 290KHz

For Whistler (Thames)
1/2Delta I=4.05A
Vtrip=36.5K*10uA=0.365V
Iocpmin=0.365V/(8*1.6m)+1/2Delta I=28.51A+4.05A
=32.56A

	Thames
GPU_VID0	Core Voltage Level
1	0.9V
0	1.0V



VGA_PCIE	1.0V	1.1 V
PR924	4.53K	3K

Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: VGA_CORE

Size | Document Number: QML70 LA-8371P | Rev: 0.01

Date: Wednesday, October 19, 2011 | Sheet 49 of 51

Version Change List (P. I. R. List) for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description

Compal Electronics, Inc.

Title: Power PIR

Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.2

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Base on GPU Reference schematic	0.02	22	Reserve pull-up / pull-down resistor 100ohm on GCORE_SEN	08/30	SR
2			0.02	15	Modify Netname of SPI signal of U5	08/30	SR
3			0.02	26	Change Q91.2 from 1.5_VDDC_PWREN# to 1.5VSG_PWREN#	08/30	SR
4		These components are for VGA	0.02	26	Change BOM Structure of R349, R350, R354, R355, Q95, Q96 to PX@	08/30	SR
5		Base on AMD Comal CRB	0.02	8	Change pull-up voltage of APU_RST#, APU_PWRGD, APU_SVT, APU_SVC, APU_SVD, ALERT_L, ALLOW_STOP from +1.5V to +1.5VS	08/30	SR
6		For EMI request	0.02	15	Reserve R559, R561, C624, C625 @ FCH_SDCLK / FCH_SDWP	08/30	SR
7			0.02	36	Remove USB3.0 Host contorller circuit	09/01	SR
8			0.02	17	Remove componets of HUDSON_M2	09/01	SR
9		Set PCIE FULL TX OUTPUT SWING to High (Full Swing)	0.02	19	Modify GPU Straps: GPU_GPIO0 pull-high	09/01	SR
10			0.02	23	Reserve pull-high and pull-down resistor of MAA14/MBB14	09/01	SR
11		Base on Thames M2 datasheet	0.02	21	Modify U7.U13, U7.14 to NC	09/01	SR
12			0.02	19	Add THM_ALERT# to from U7.AG30 (GPU_THERMAL INT) to U34.6 (ADM1032) Add GPU_CTF from U7.AM17 (GPU_CTF) to U72.97 (EC)	09/02	SR
13			0.02	31	Reserve Analog mircophone circuit	09/02	SR
14			0.02	9, 39,45	Change contorl singal of 1.1VALWP from SPOK to FCH_1.1PWR_EN Change +1.1V_FCH to +1.1VALW	09/02	SR
15			0.02	15,37	Connect U72.92 (EC) to U2.V1 (FCH)for SYS ROM Write Protect	09/02	SR
16			0.02	35	Co-lay AI Charger	09/02	SR
17			0.03	31	Modify Analog Microhpone circut base on Vendor suggestion	09/05	SR
18			0.03	22	Add decoupling cap. base on GPU check list	09/06	SR
19			0.03	17	Change decoupling cap. base on FCH check list	09/06	SR
20			0.03	27	Change LVDS translator to RTD2136	09/06	SR
21			0.03	28	Add pull-up resistor R129, R132 (2.2K) of FCH_CRT_DDC_SDA / SCL	09/06	SR
22			0.03	13	Change R99 to 22ohm (CLK_SD_48M)	09/07	SR
23			0.03	14	Pull-down PEG_CLKREQ#	09/08	SR
24			0.03	37	Change Board ID, R398: 0ohm	09/08	SR
25			0.03	34	Change Power source of ODD from +5VS to +5VALW	09/09	SR
26			0.03	33	Change Power source of WLAN from +3VALW to +3VS	09/09	SR
27			0.03	32	Add power source for none Card Reader IC solution	09/09	SR

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1			0.2	15	Change U5 power from +3V_PCH to +3V_FCH	10/11	SR2
2			0.2	15	Change GBE_MDIO pull-up voltage from +3VALW to +3V_FCH	10/11	SR2
3	Blue Screen after install VGA Driver		0.2	25	SWAP QSB7 and QSB#7	10/11	SR2
4			0.2	32	Delete Net SDCD, SDWP# that connect to EC Add MOSFET inverter of SDWP#	10/11	SR2
5			0.2	8	Un-mount pull-high resistor of APU_SVT, APU_SVC, APU_SVD	10/11	SR2
6			0.2	28	Follow QCL70 pin define	10/11	SR2
7			0.2	38	Modify Touch Pad pin define	10/11	SR2
8		For voltage leakage	0.2	8	Change pull-high voltage of APU_PROCHOT#, APU_THERMTRIP#, APU_SVT, APU_SVC, APU_SVD, ALERT_L, ALLOW_STOP, APU_RST#, APU_PWRGD, APU_SIC, APU_SID	10/11	SR2
9		Base on AMD recommend	0.2	24, 25	Change R299, R300, R309, R310, R319, R320, R325, R326 from 56ohm to 40.2ohm	10/11	SR2
10			0.2	37	Change Board ID to "1" for SR2	10/13	SR2
11			0.2	22	Seperate VDDC and VDDCI of VGA	10/14	SR2
12			0.2	23	Reserve R611, R612 for MAA14, MAB14	10/14	SR2
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