

Compal confidential

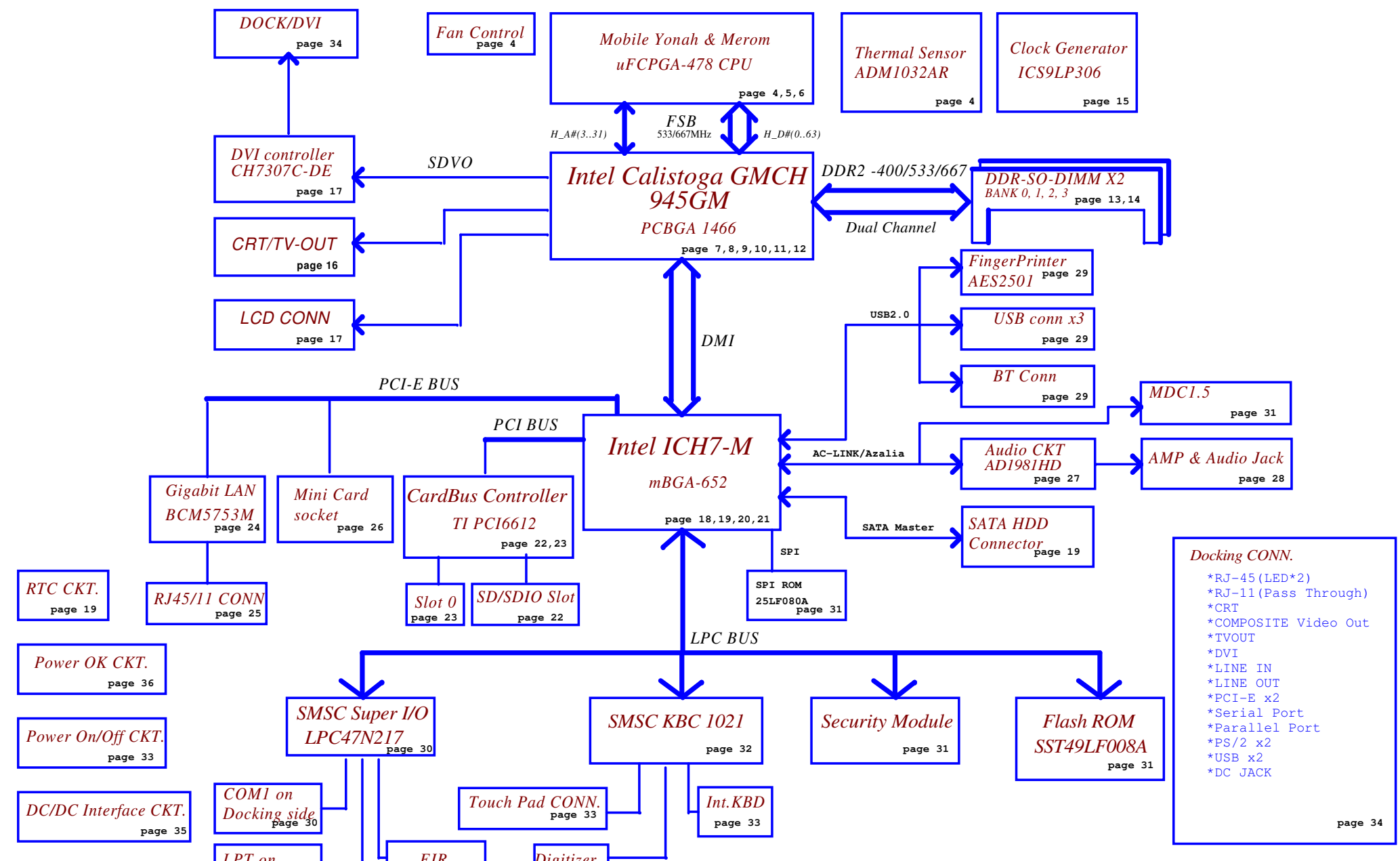
Schematics Document Mobile Yonah uFCPGA with Intel Calistoga_GM+ICH7-M core logic 2006-02-27

REV: 0.5

硬體二部	
機密	
解密日期	Feb 27, 2007

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Heavenly 2.0



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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH core power	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Symbol note:

 :means digital ground.

 :means analog ground.

@ :means reserved.

@ : means just reserve , no build

SPI@ : means just build when SPI I/F BIOS function enable.

FWH@ : means just build when FWH I/F BIOS function enable.

NOXDP@ : means just build when XDP function disable.

XDP@ : means just build when XDP function enable. When this time, docking PCI express will not work.

TPM@ : means just build when TPM1.2 function enable.

250@ : means just build when SMC LPC47N250 chip selected.

1021@ : means just build when SMC KBC1021 chip selected.

45@ : means need be mounted when 45 level assy or rework stage.

ACCEL@ : means just build when Accelerometer chip LIS3LV02DQ selected.

DVI_7307@ : means just build when DVI chip CH7307 selected.

DVI_1362@ : means just build when DVI chip SIL1362 selected.

Internal PCI Devices

DEVICE	PCI Device ID	IDSEL #	
LAN	D8	AD24	
Azalia	D27	AD11	
PCI-E	D28	AD12	
USB1.1/2.0	D29	AD13	
PCI to PCI (DMI to PCI)	D30	AD14	
AC97 MODEM	D30	AD14	(Disabled by BIOS)
AC97 Audio	D30	AD14	(Disabled by BIOS)
PATA/SATA	D31	AD15	(PATA is Disabled by BIOS)
LPC I/F	D31	AD15	
SMBUS	D31	AD15	

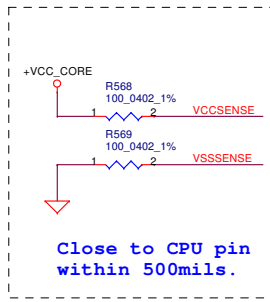
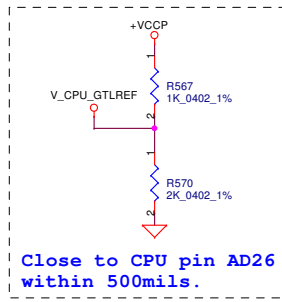
External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
CARD BUS	D6	AD22	2	C D E G

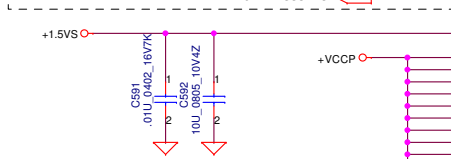
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

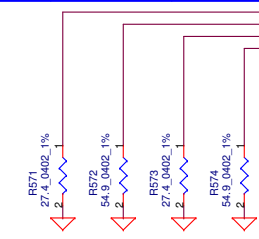
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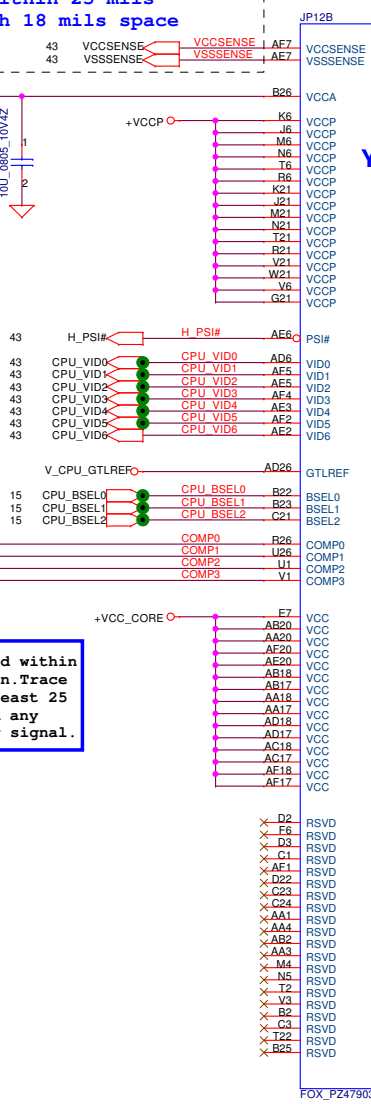
Length match within 25 mils
The trace width 18 mils space 7 mils



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

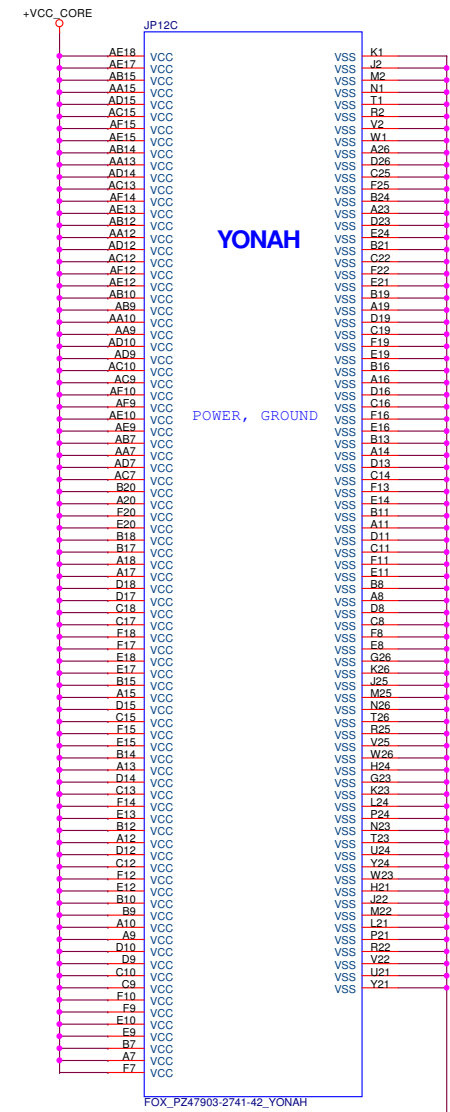


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.



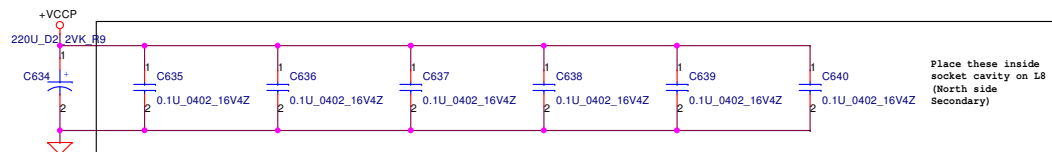
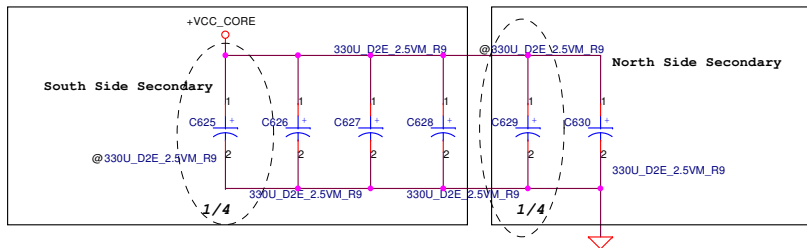
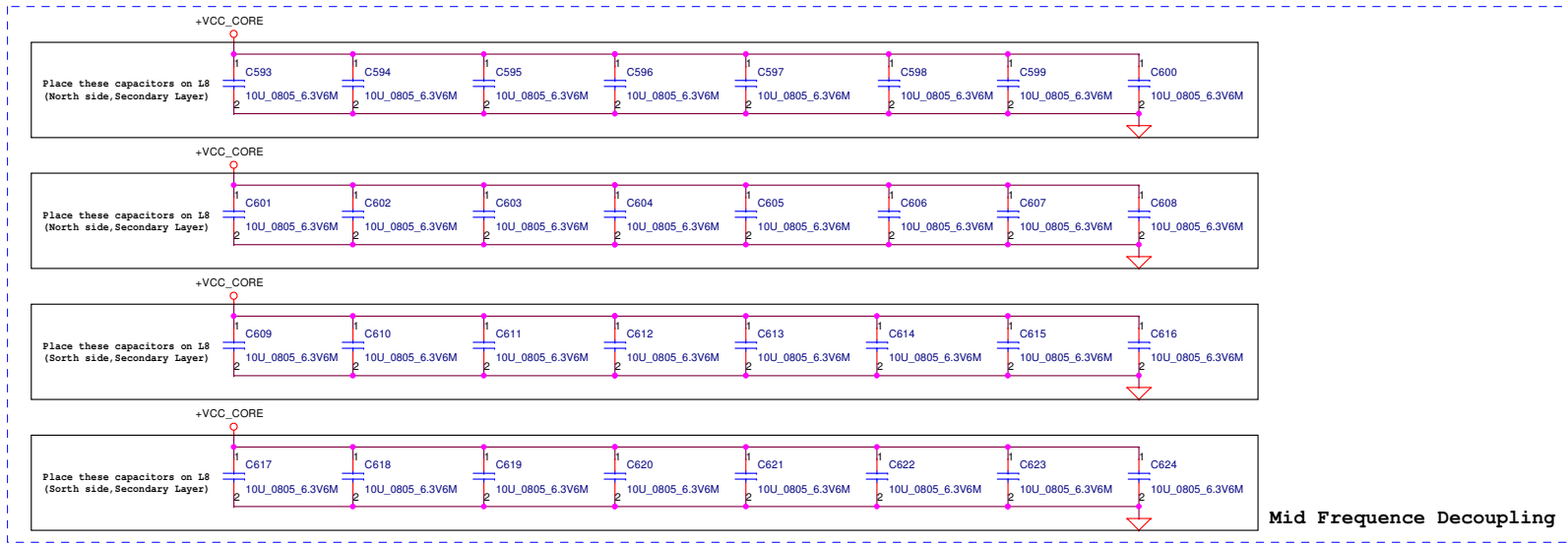
YONAH

POWER, GROUND, RESERVED SIGNALS AND NC

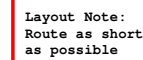
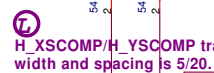


YONAH

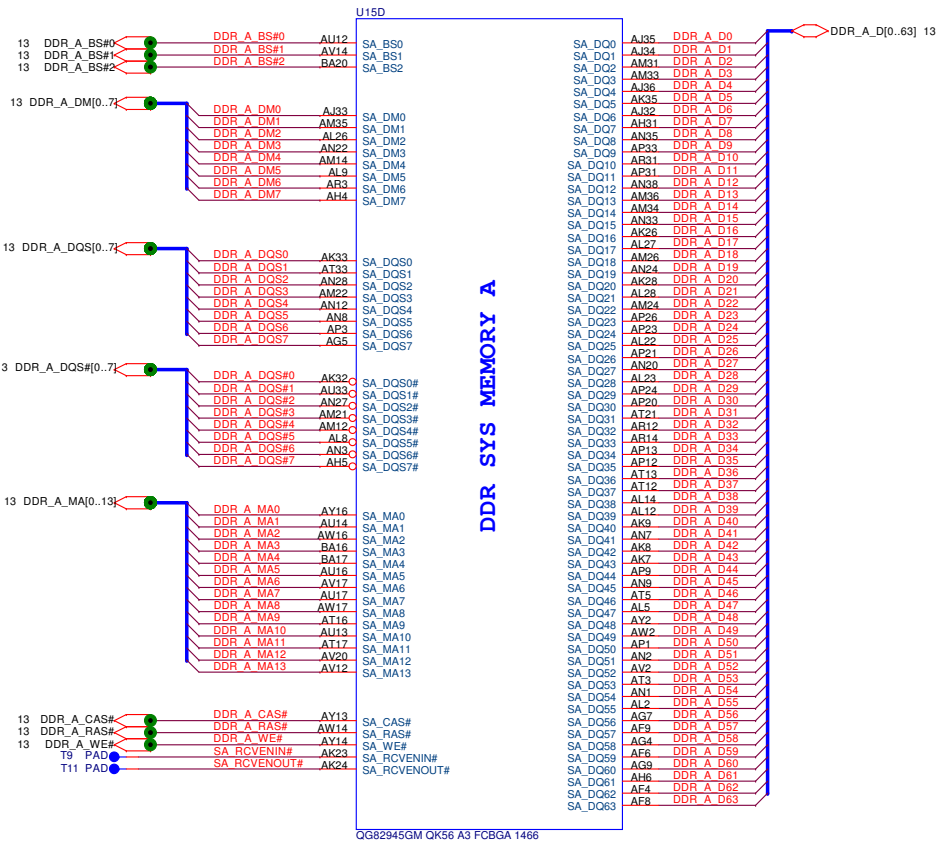
POWER, GROUND



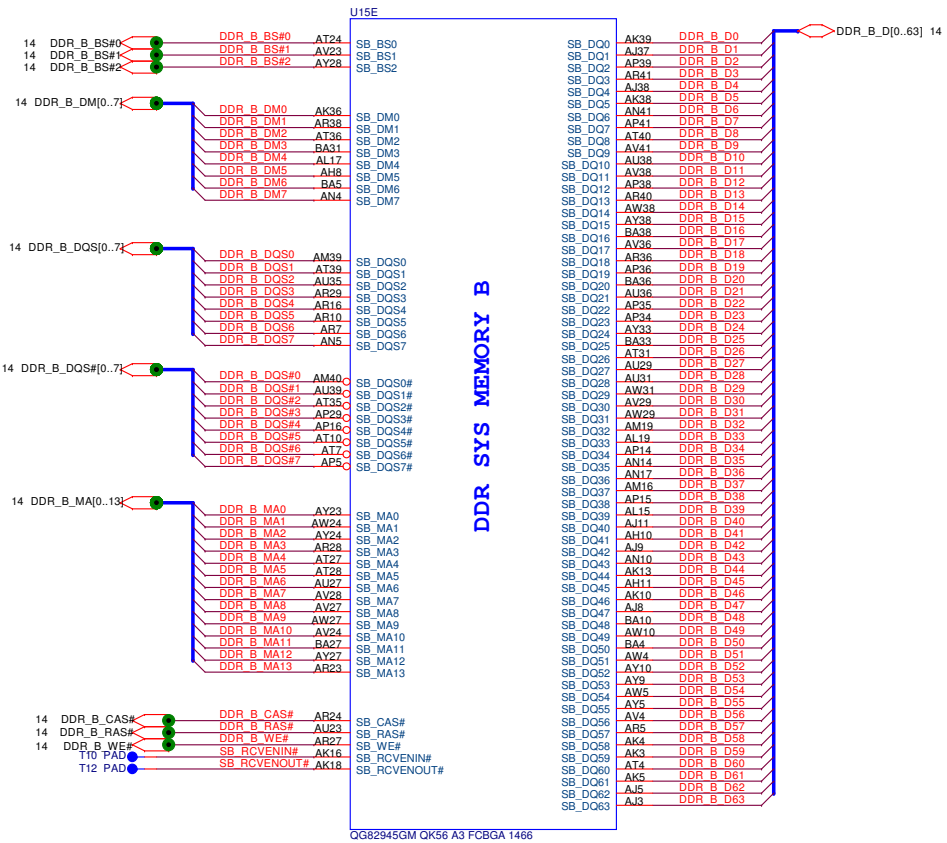
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QG82945GM QK56 A3 FCBGA 1466



QG82945GM QK56 A3 FCBGA 1466

PEGCOMP trace width
and spacing is 18/25 mils.

+1.5VS_PCIE

7/14

PCI-EXPRESS GRAPHICS

LVDS

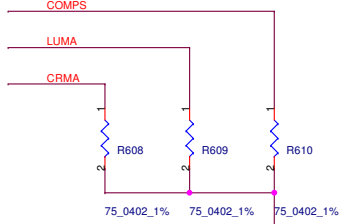
TV

CRT

OG82945GM QK56 A3 FCBGA 1466

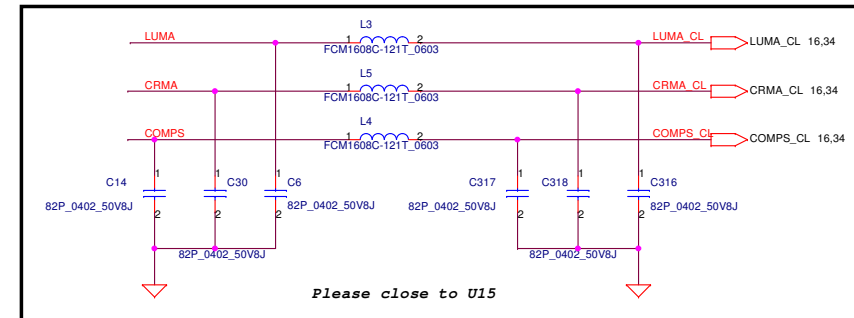
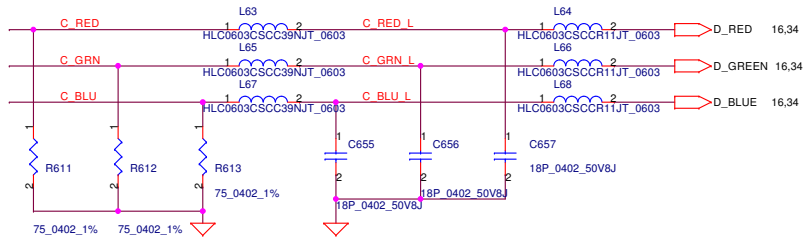
TV-Out Termination

Place close to U15



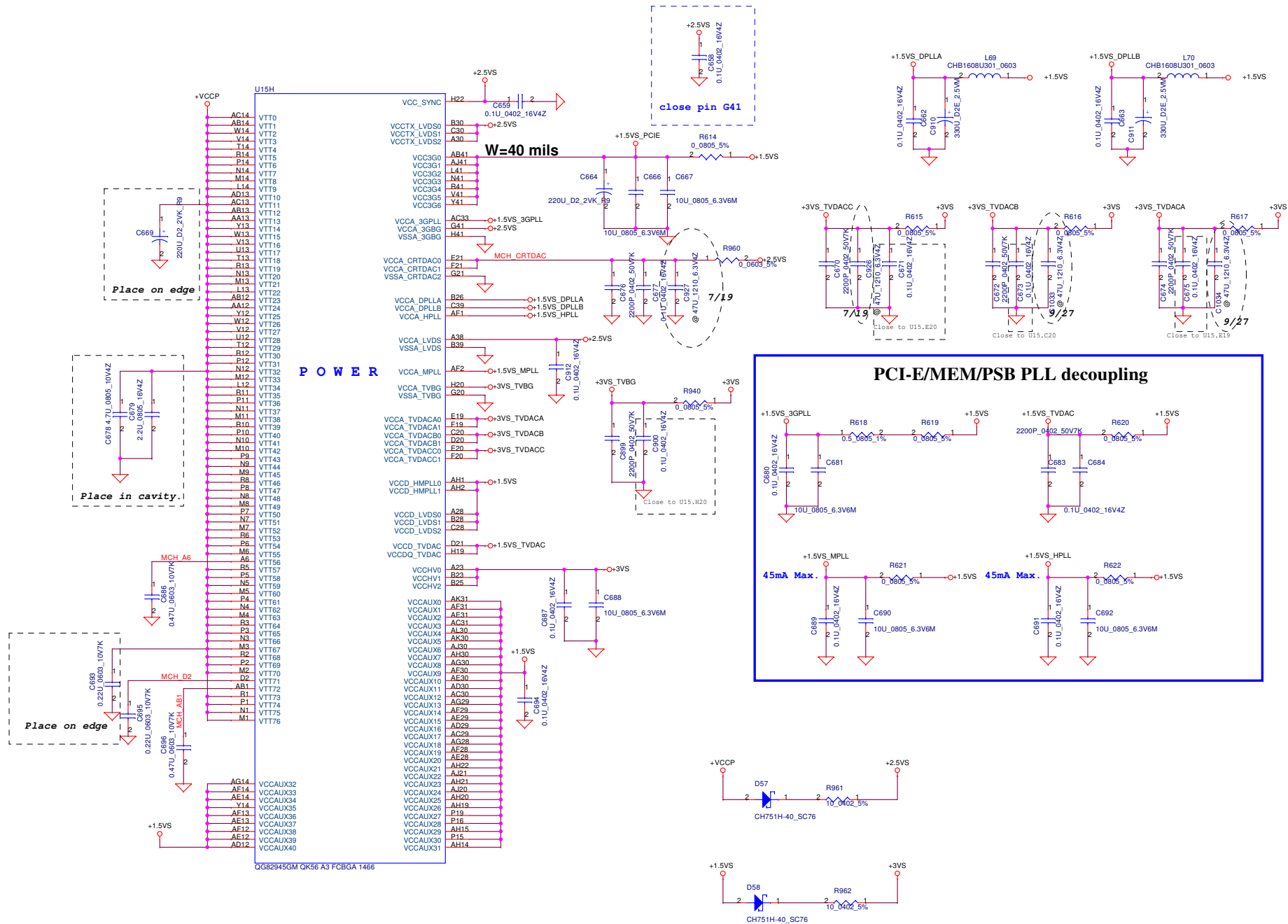
CRT Termination/EMI Filter

Place close to U15



Please close to U15

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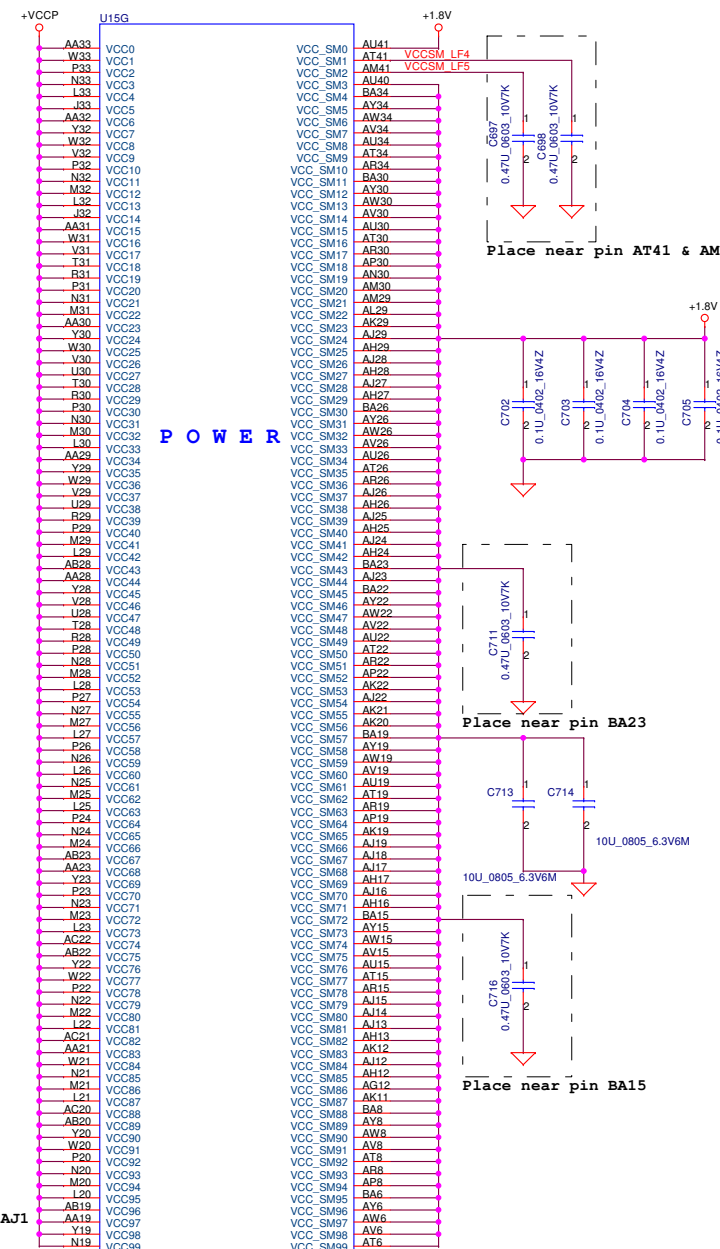
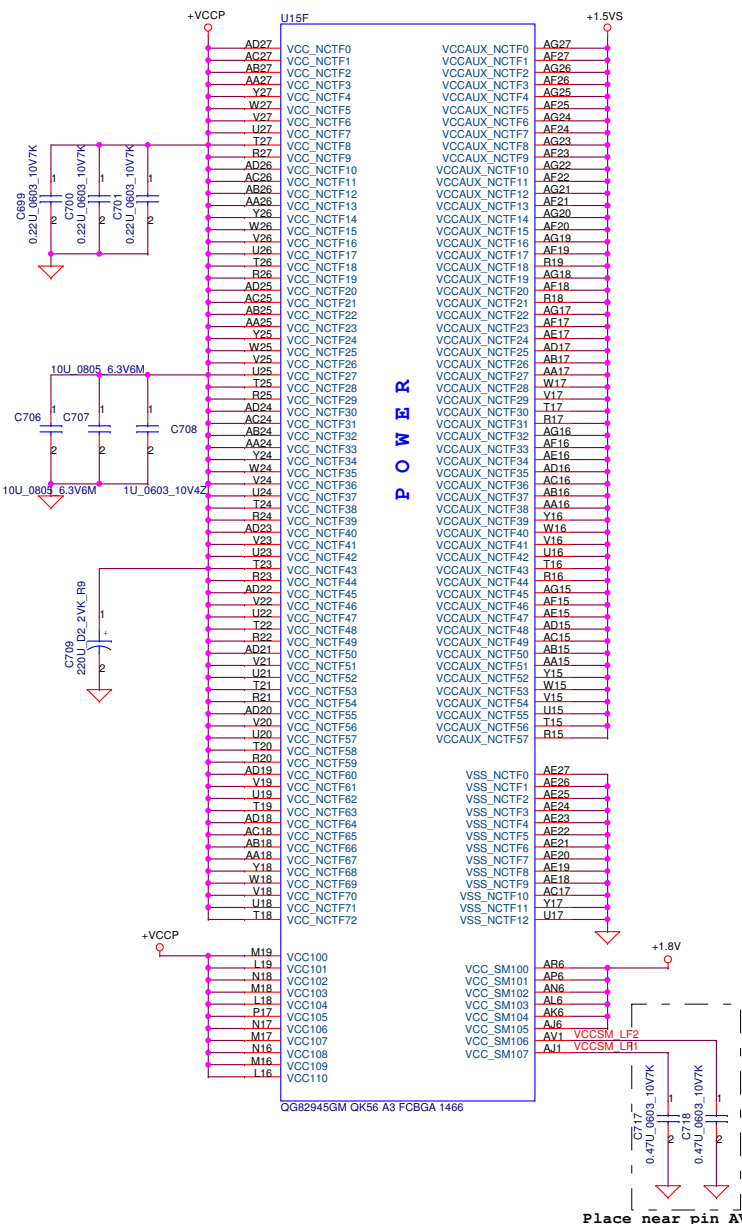
Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

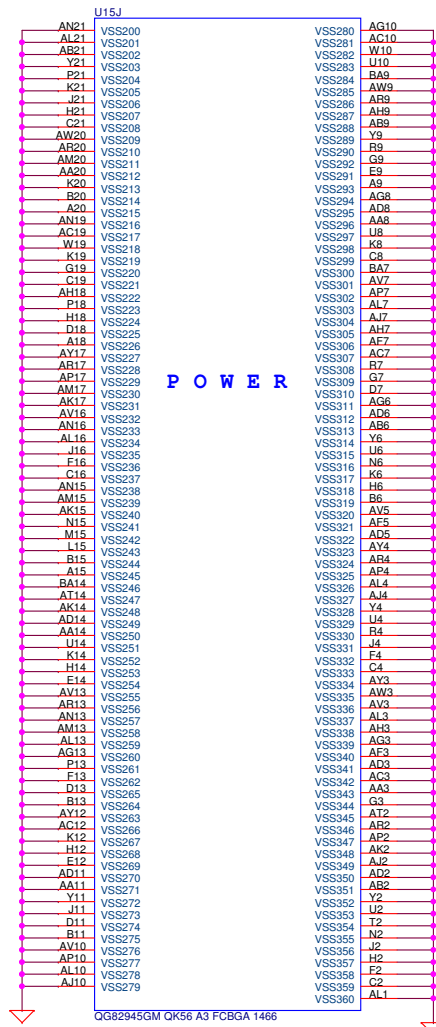
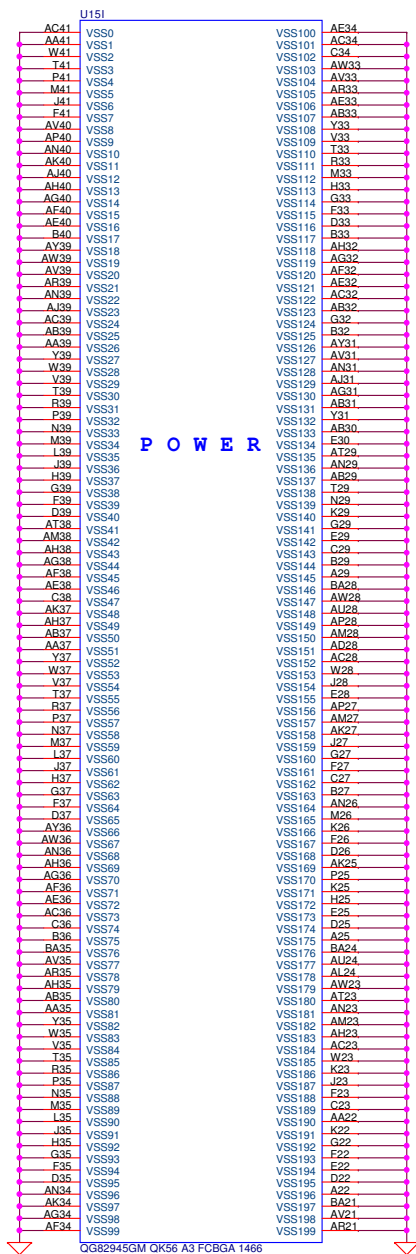
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU* (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal operation (Default)*
CFG11	0 = Calistoga * (According to Intel Napa schematic Checklist & CRB Rev1.301 document 2.2Kohm pull-down resistor request) 1 = Reserved
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG18	0 = 1.05V * (Default) 1 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present (Default) 1 = SDVO Device Present *
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.

7	CFG5	R623	1	2	@ 2.2K 0402 5%
7	CFG7	R624	1	2	@ 2.2K 0402 5%
7	CFG9	R625	1	2	@ 2.2K 0402 5%
7	CFG11	R626	1	2	@ 2.2K 0402 5%
7	CFG12	R627	1	2	@ 2.2K 0402 5%
7	CFG13	R628	1	2	@ 2.2K 0402 5%
7	CFG16	R629	1	2	@ 2.2K 0402 5%
7	CFG18	R630	1	2	@ 1K 0402 5%
7	CFG19	R631	1	2	@ 1K 0402 5%
7	CFG20	R632	1	2	@ 1K 0402 5%



QG82945GM QK56 A3 FCBGA 1466

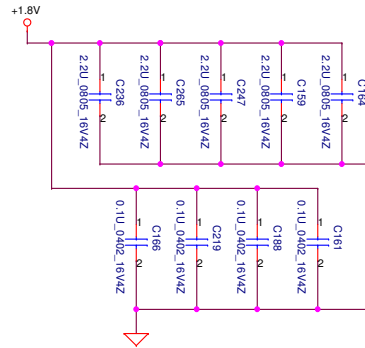
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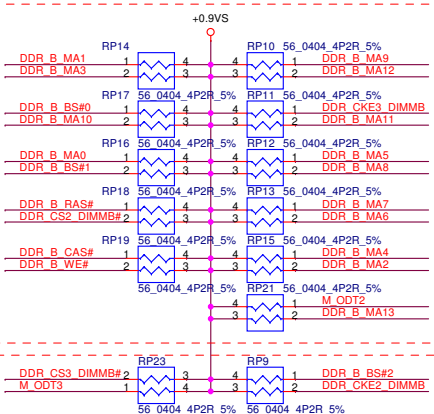
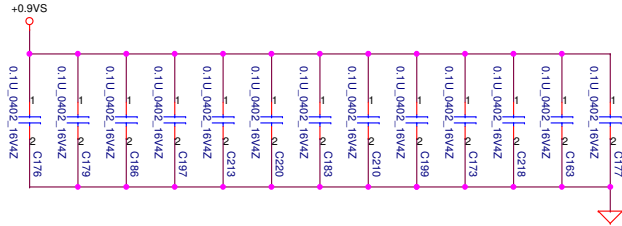


8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..13]

Layout Note:
Place near JP10



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT

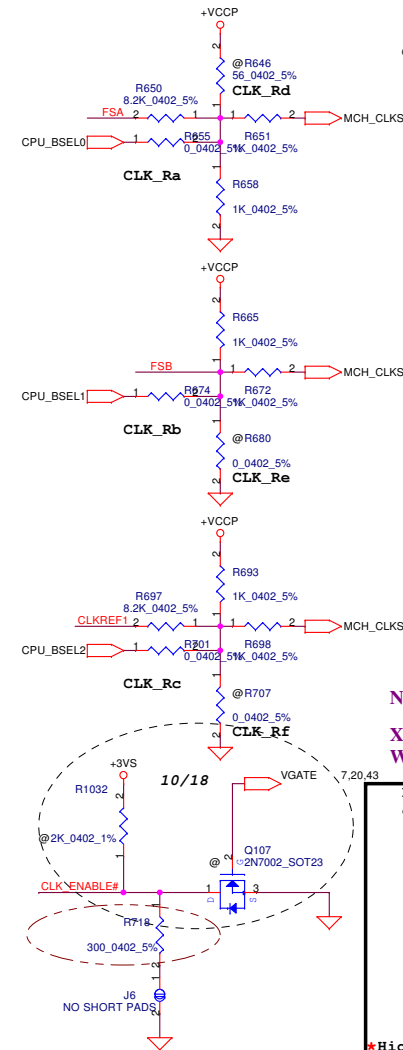


FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954306

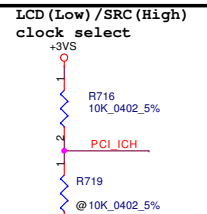
FSB Frequency Set:

CPU Driven	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
* (Default)	No Stuff	CLK_Rd	CLK_Re	CLK_Rf
533MHz	Stuff	CLK_Rd	CLK_Re	CLK_Rf
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
667MHz	Stuff	CLK_Rd	CLK_Rf	
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc

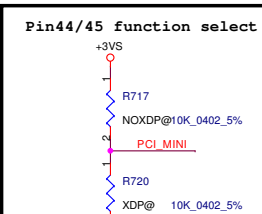


NOXDP@ : means just build when XDP function disable.

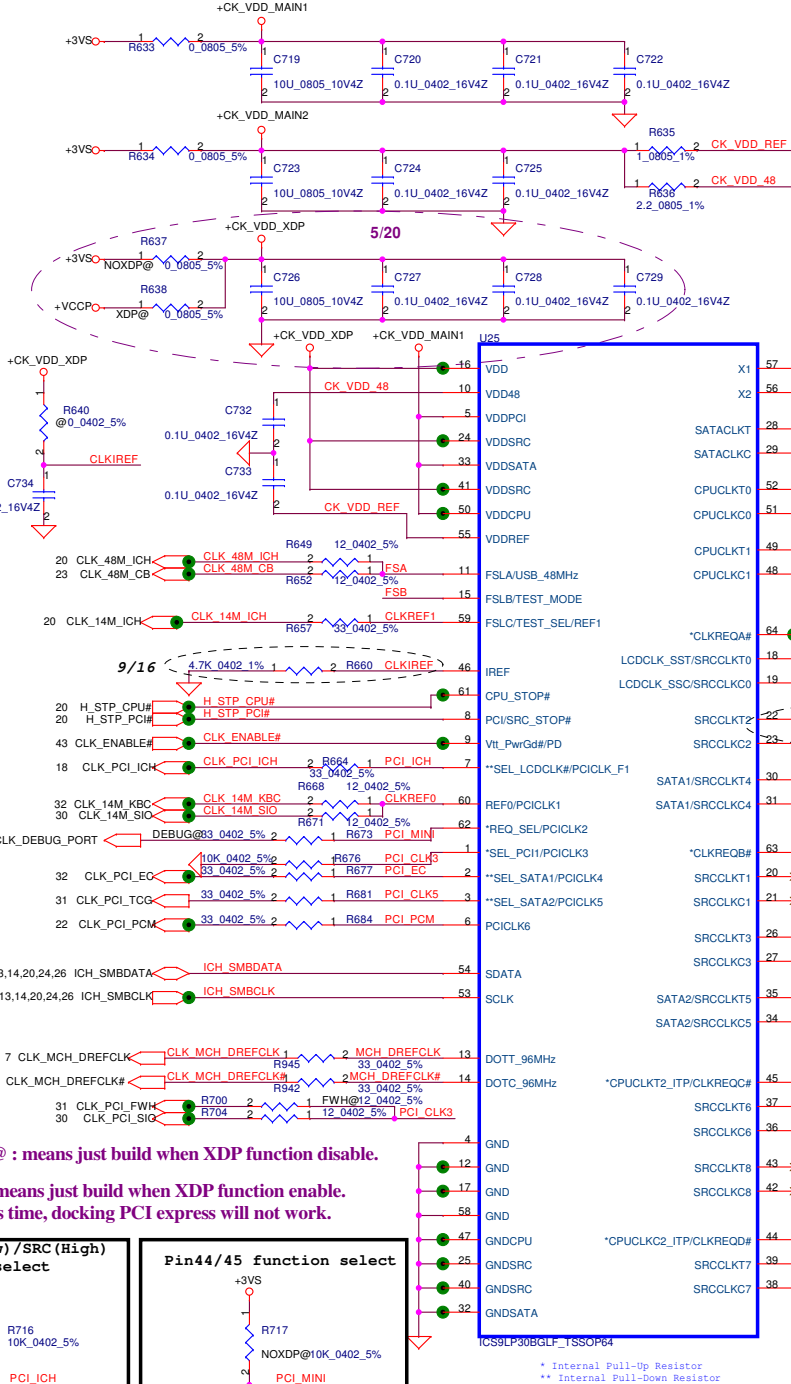
XDP@ : means just build when XDP function enable.
When this time, docking PCI express will not work.



*High: Pin18/19 = 100MHz
Low: Pin18/19 = 96MHz

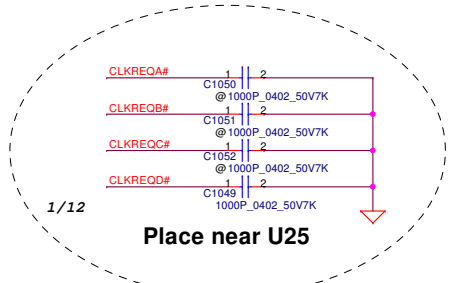


*High: Pin44/45 = CLKREQ
*Low: Pin44/45 = CPUCLK2_1TP



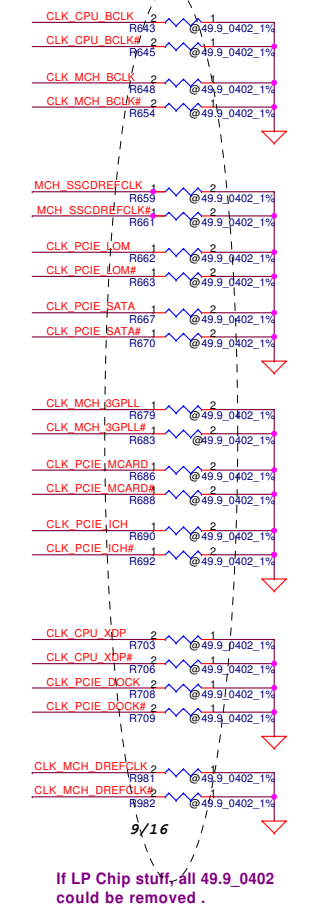
* Internal Pull-Up Resistor
** Internal Pull-Down Resistor

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Place near U25

Place near U25
Place these components
near each pin within 40
mils.



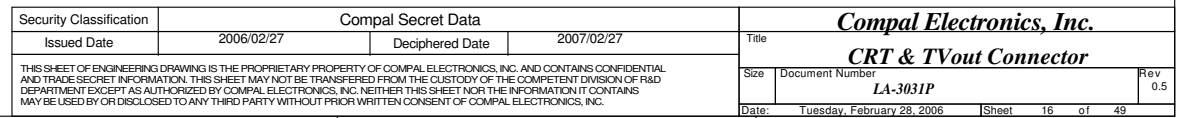
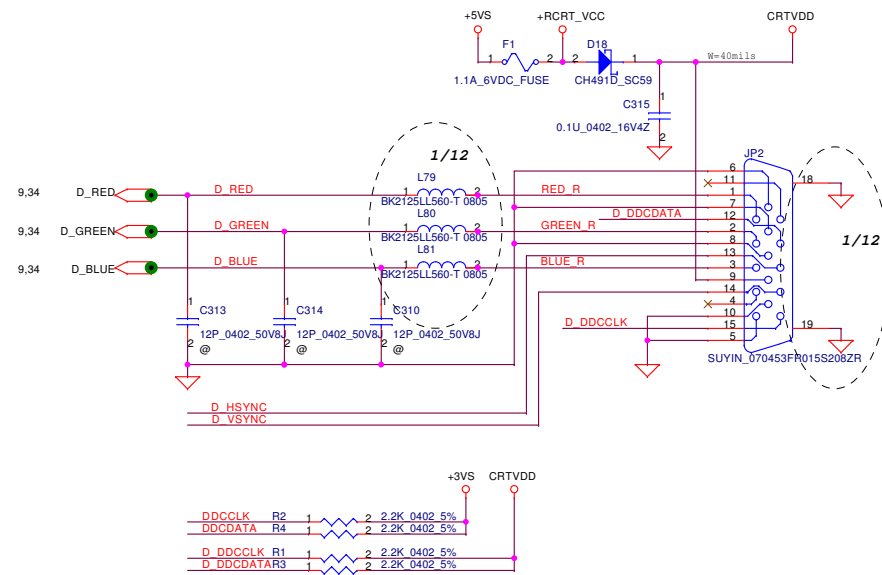
If LP Chip stuff, all 49.9_0402
could be removed.

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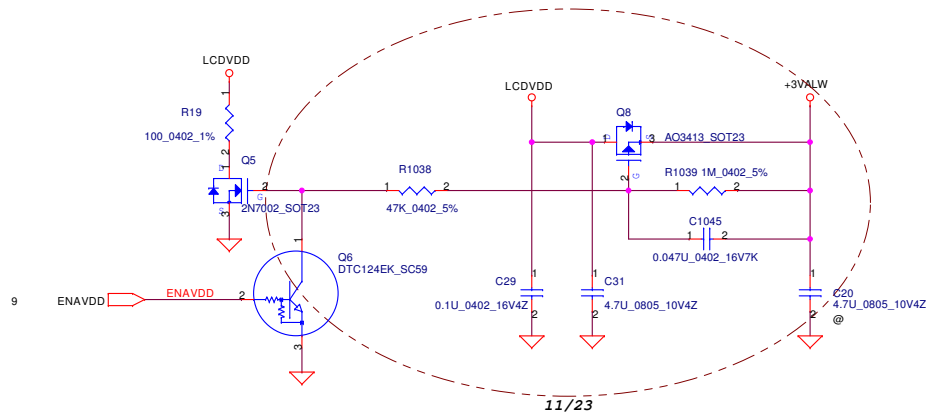
Clock generator

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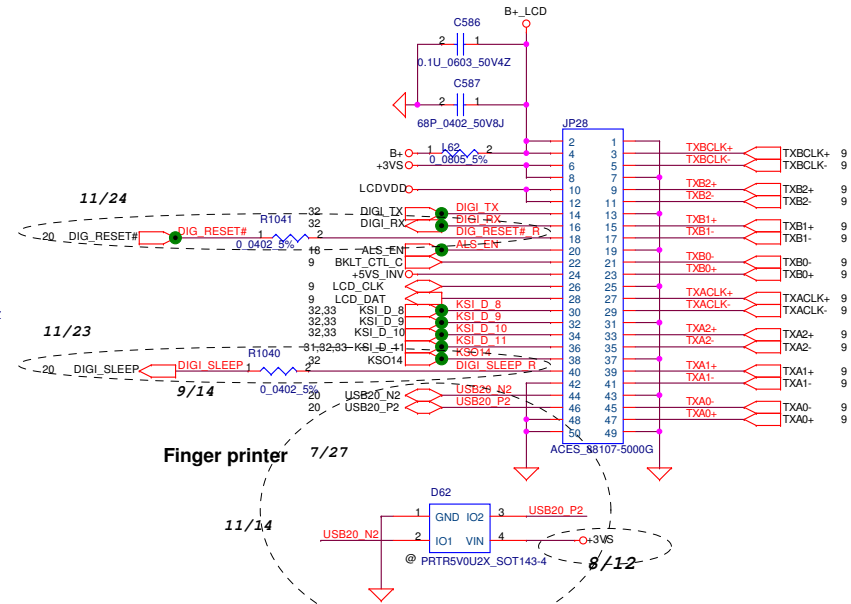
TV-Out Connector



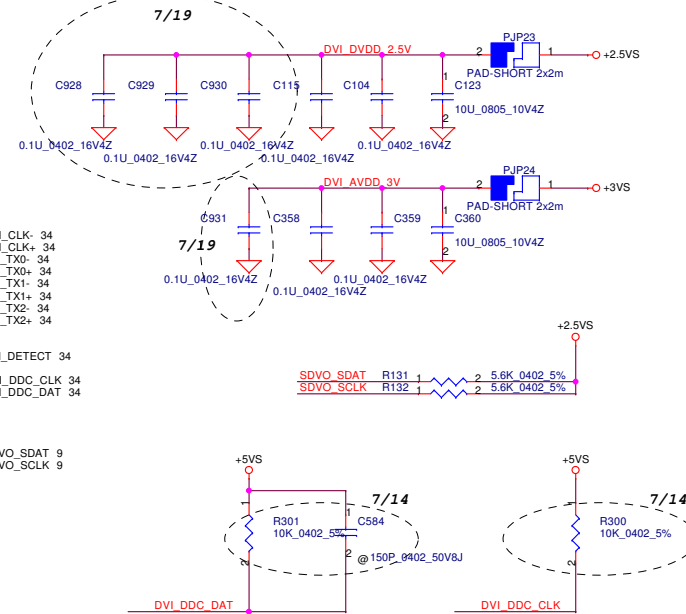
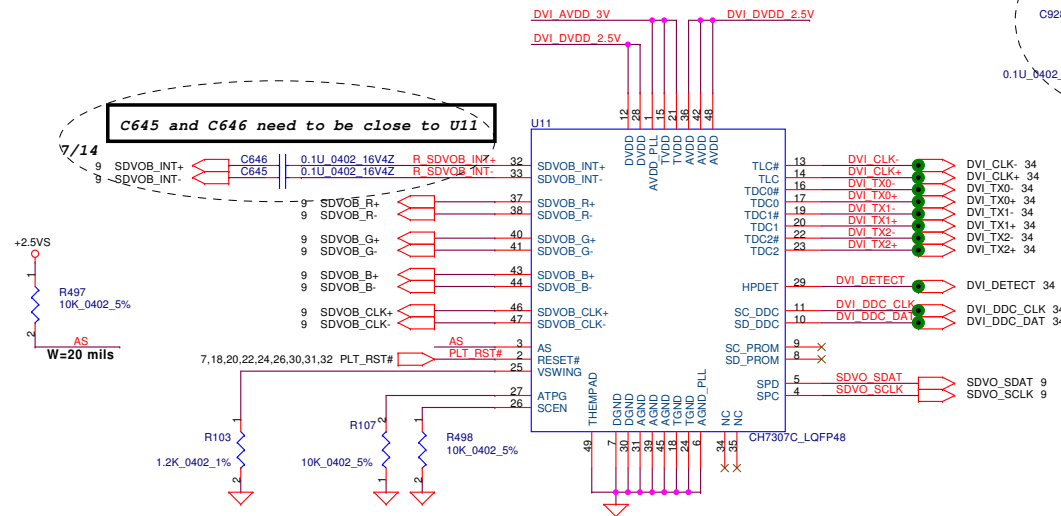
LCD POWER CIRCUIT



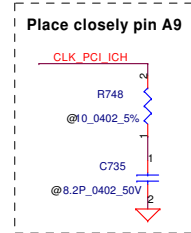
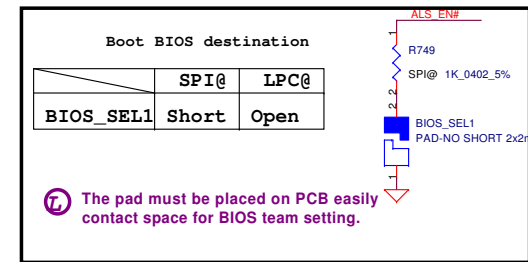
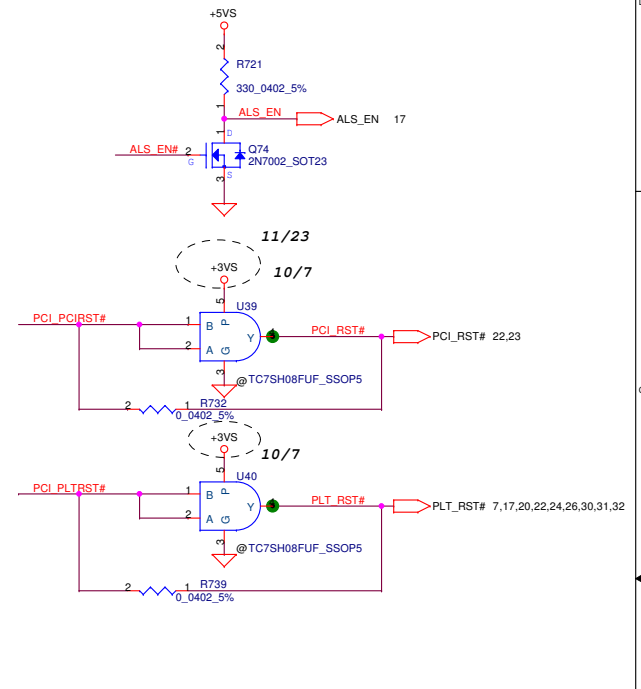
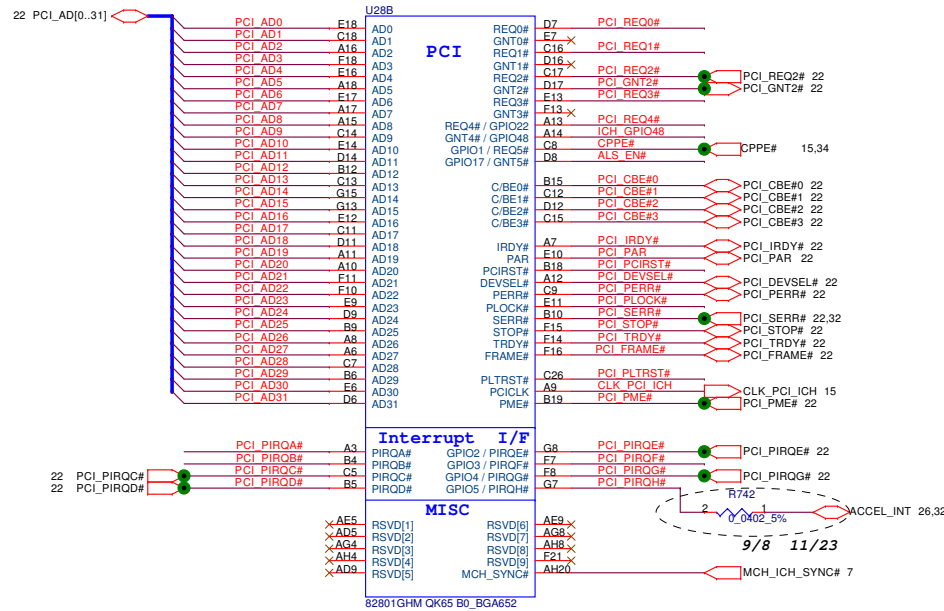
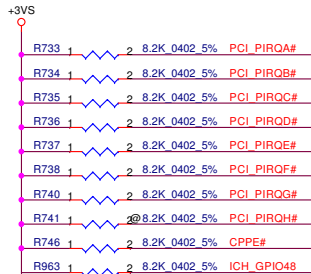
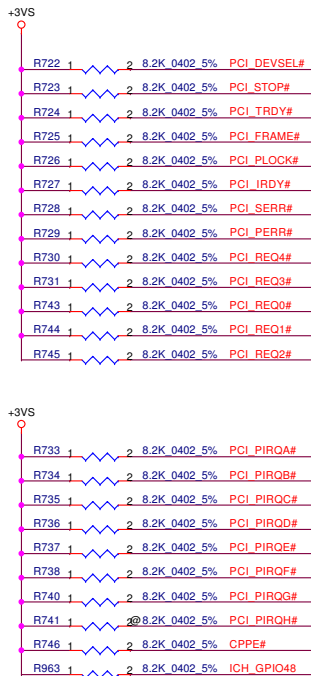
LCD/PANEL BD. CONN.



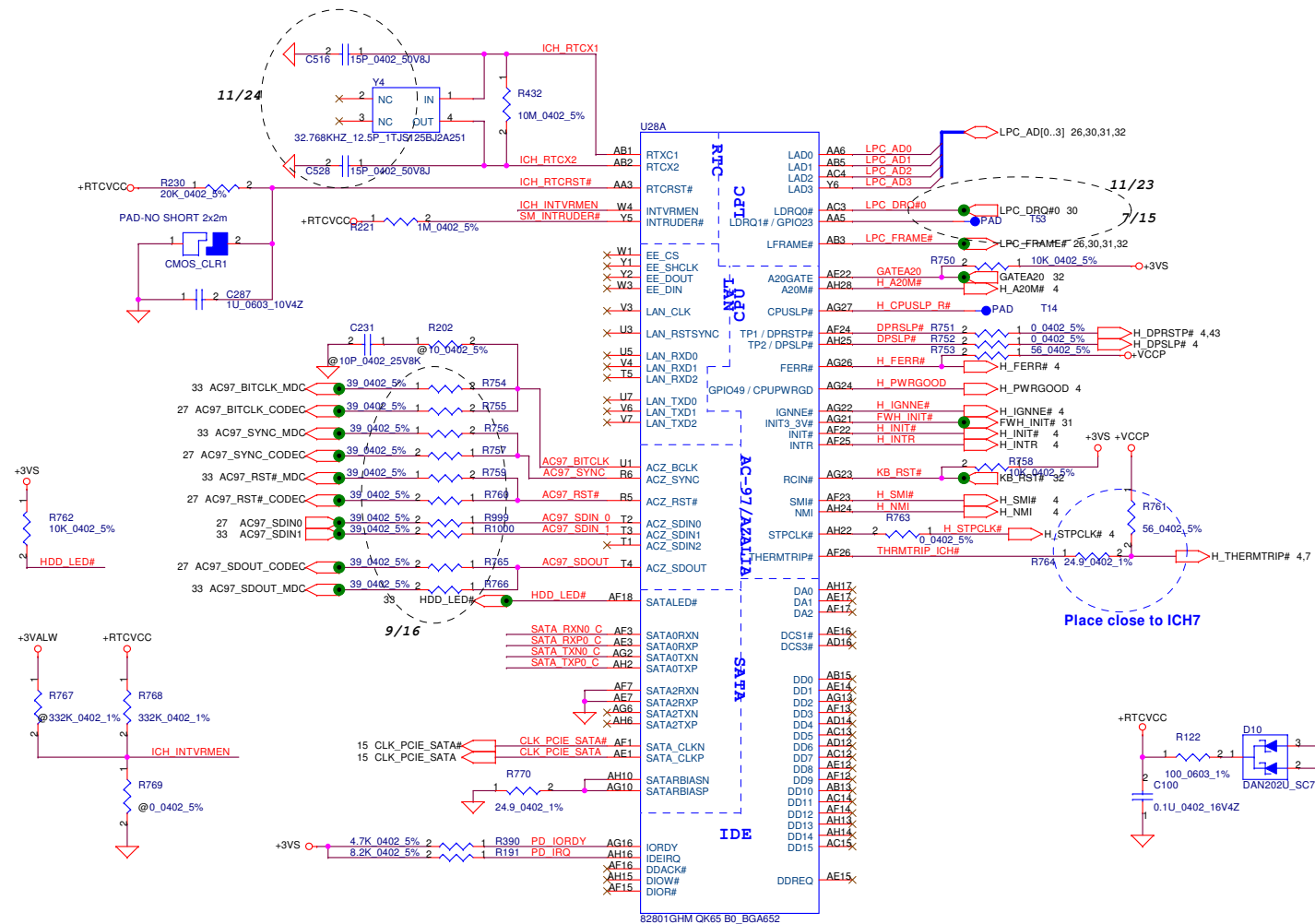
DVI CONTROLLER



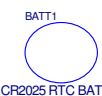
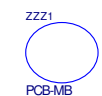
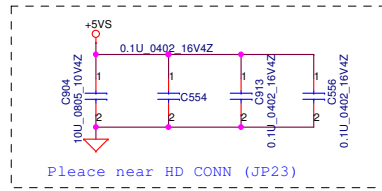
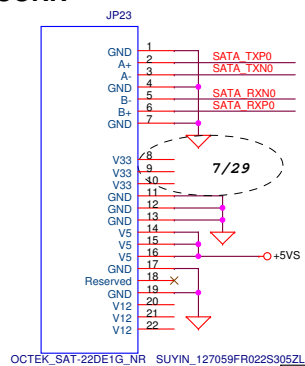
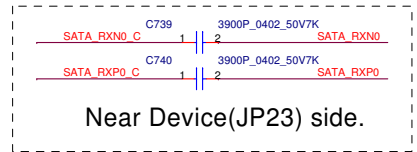
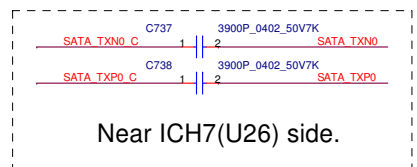
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2006/02/27				Title			
Deciphered Date				2007/02/27				DVI (CH7307)/LCD CONN.			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED FOR ANY OTHER PURPOSE WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.				Size				Document Number			
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				0.5				Date			
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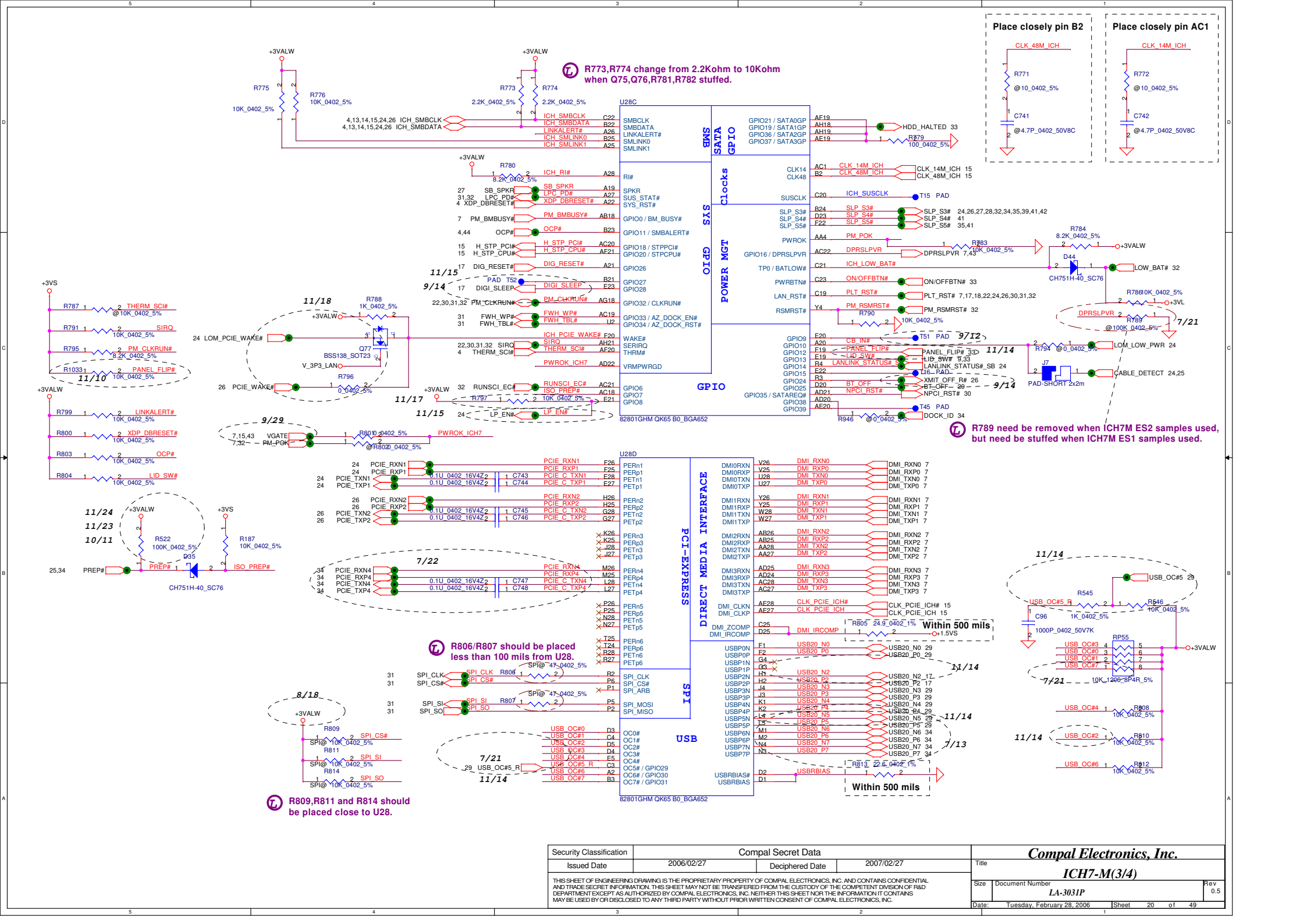
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Issued Date	2006/02/27	Deciphered Date	2007/02/27	1CH7-M(1/4)	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
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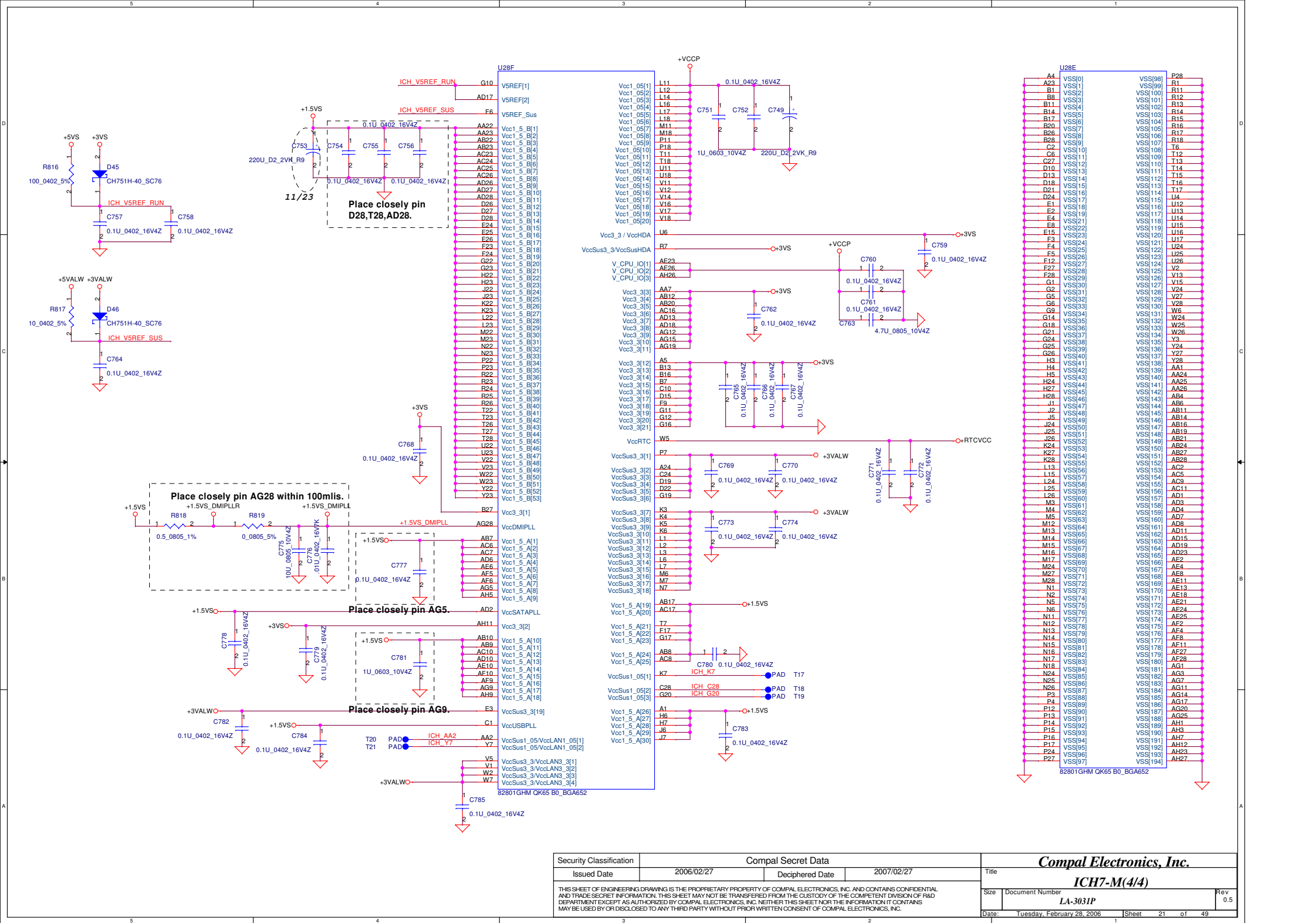


SATA CONN

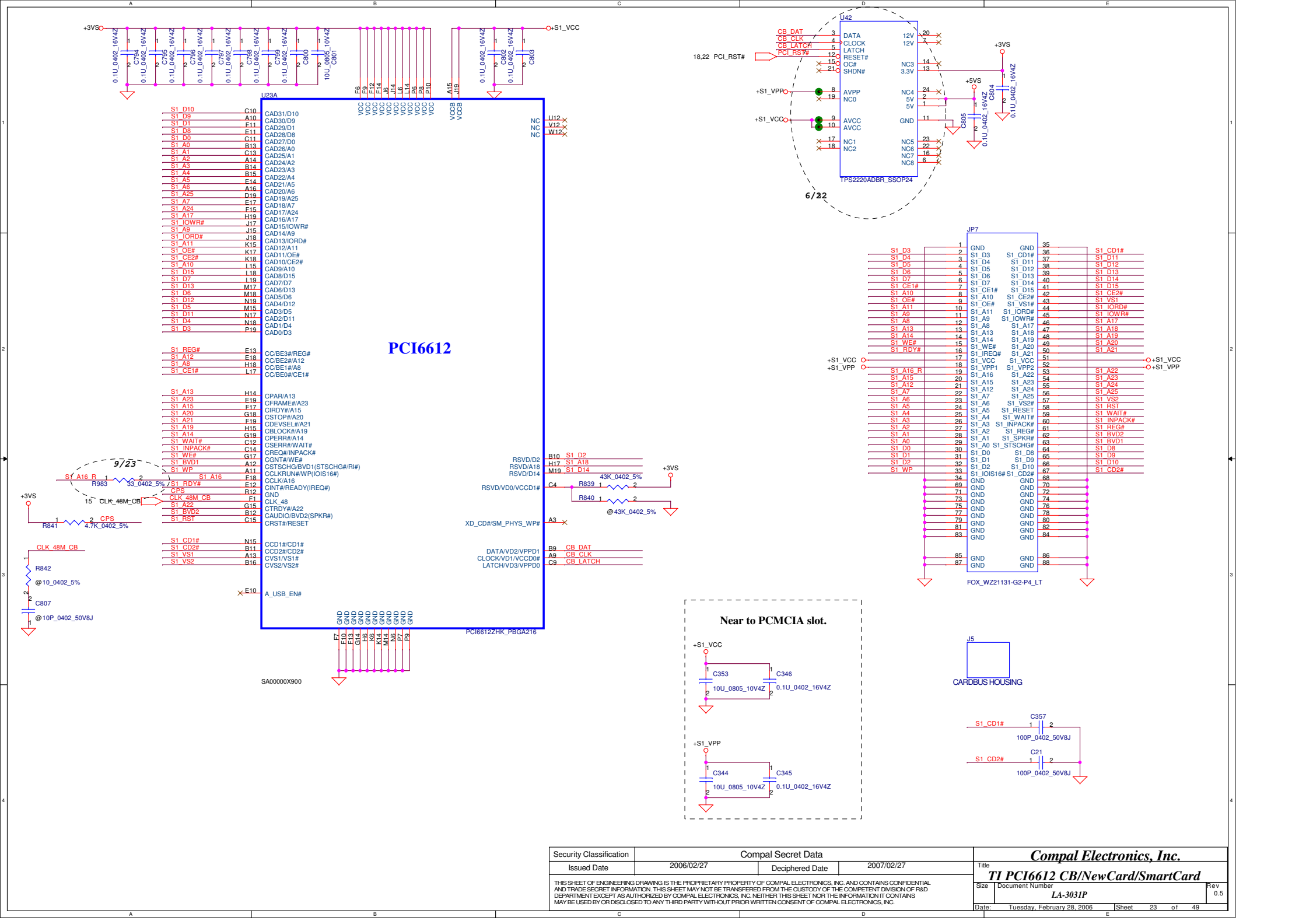


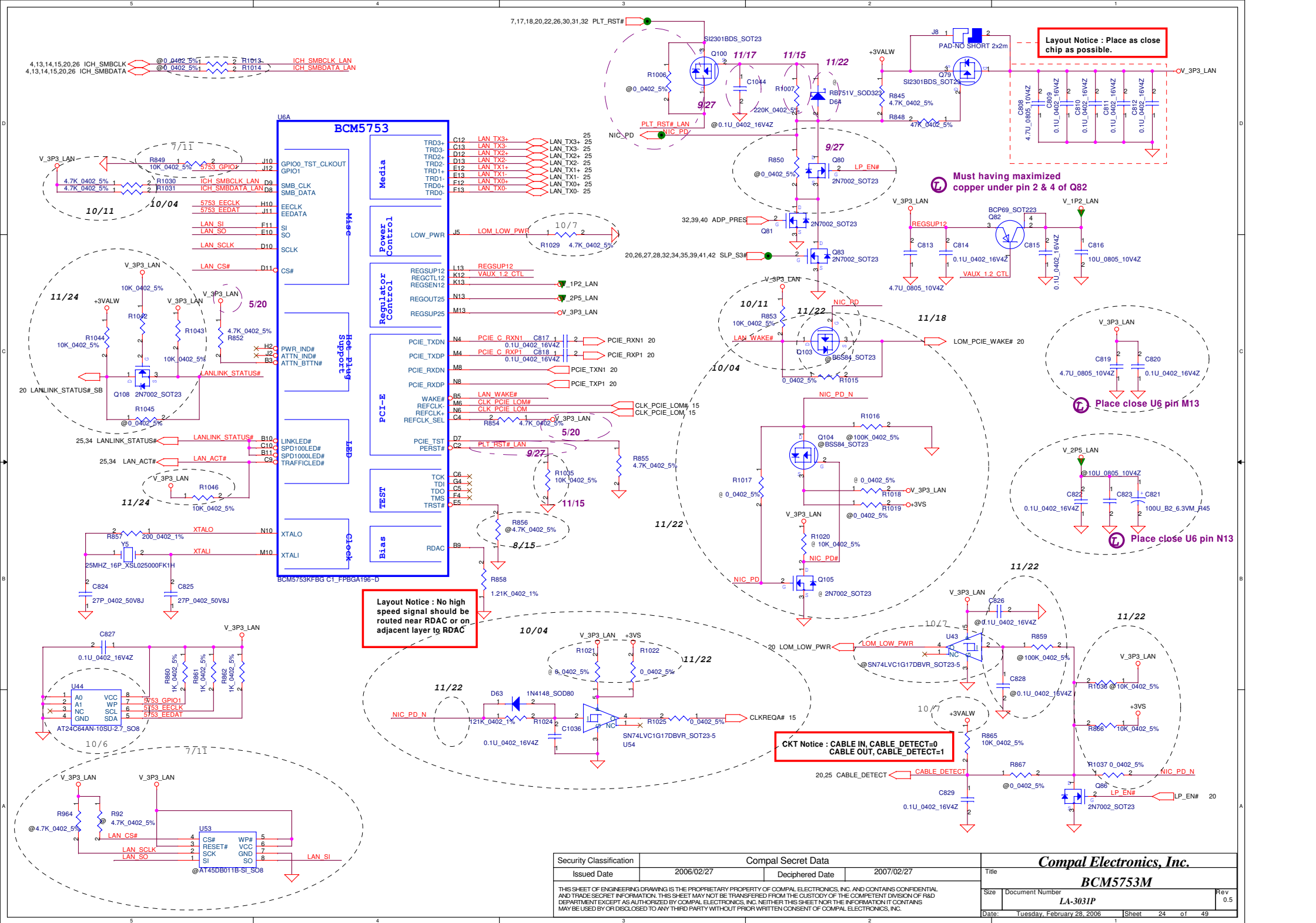
Security Classification		Compal Secret Data		Title	
Issued Date	2006/02/27	Deciphered Date	2007/02/27	Compal Electronics, Inc.	
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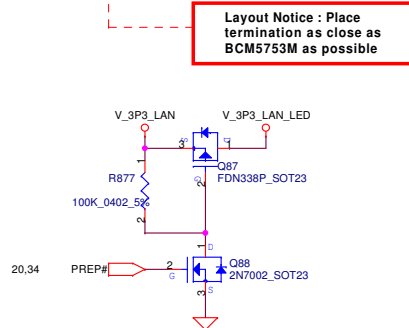
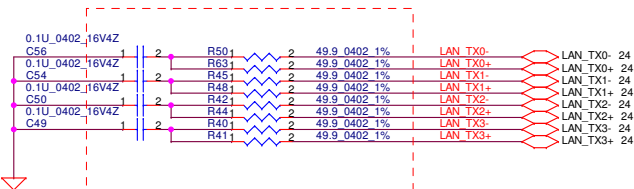
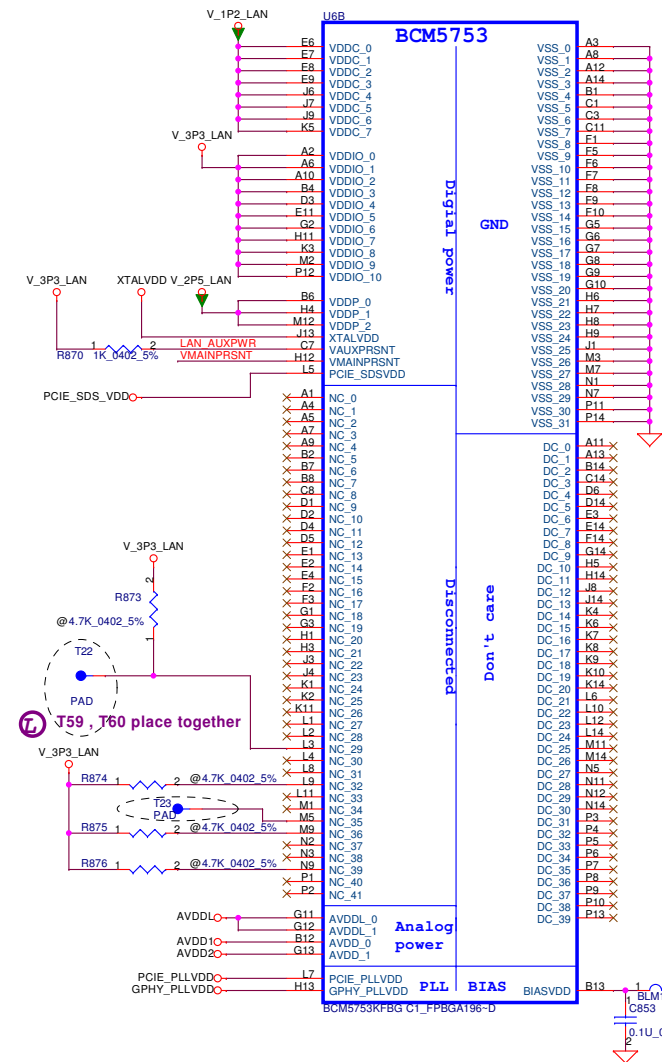
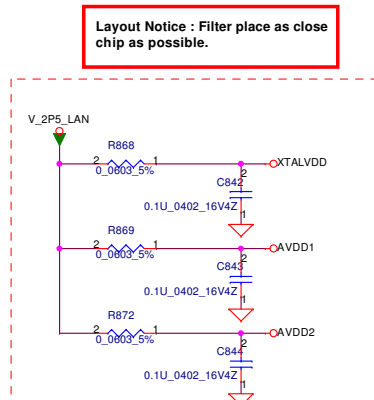
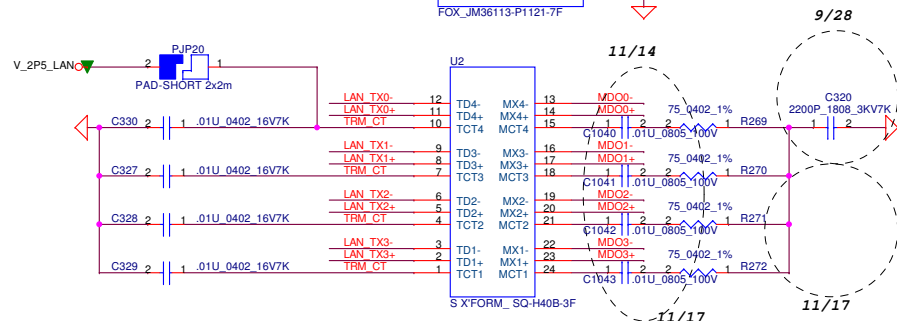
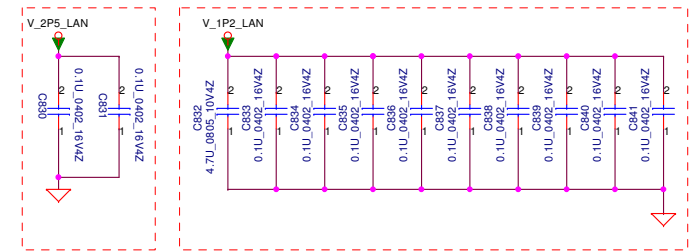
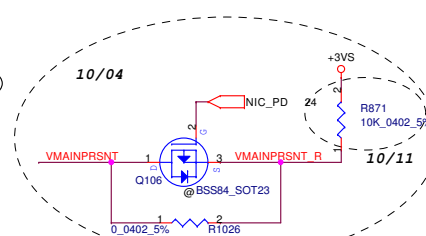
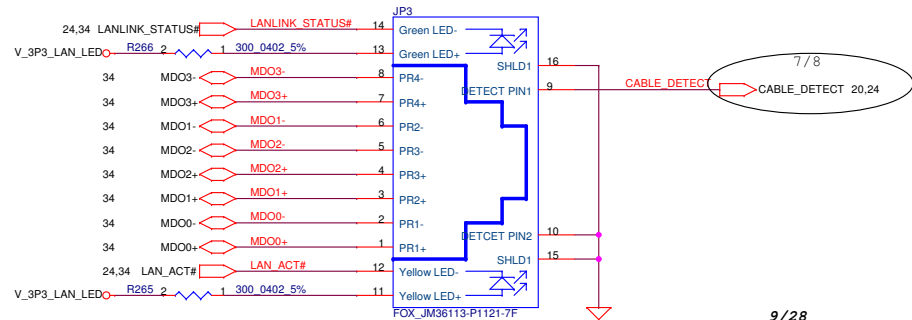
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Issued Date		2006/02/27		Deciphered Date		2007/02/27	
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				Size		Document Number LA-3031P	
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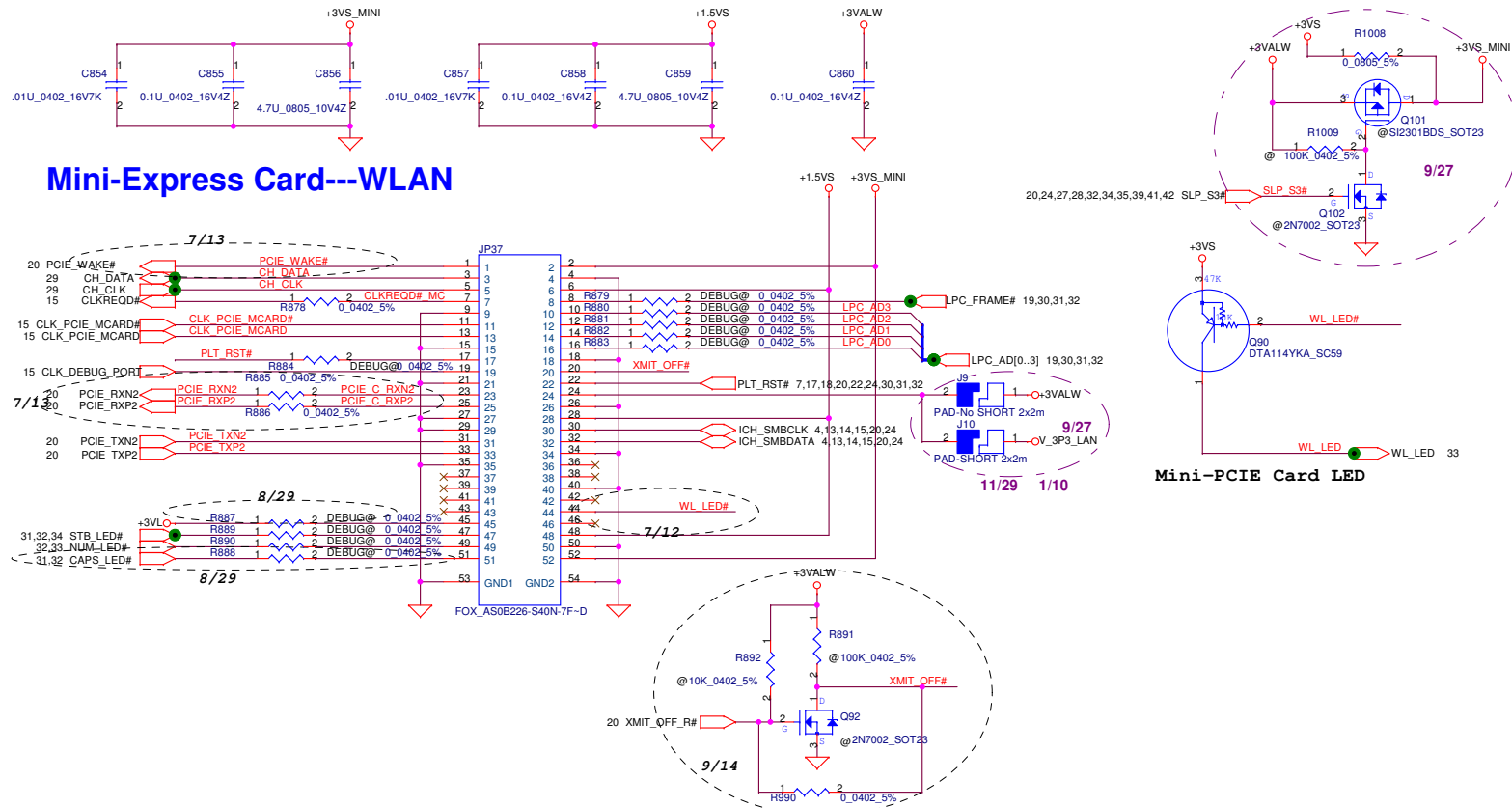
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/02/27	Deciphered Date	2007/02/27	Title	BCM5753M	
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RJ-45 CONN.

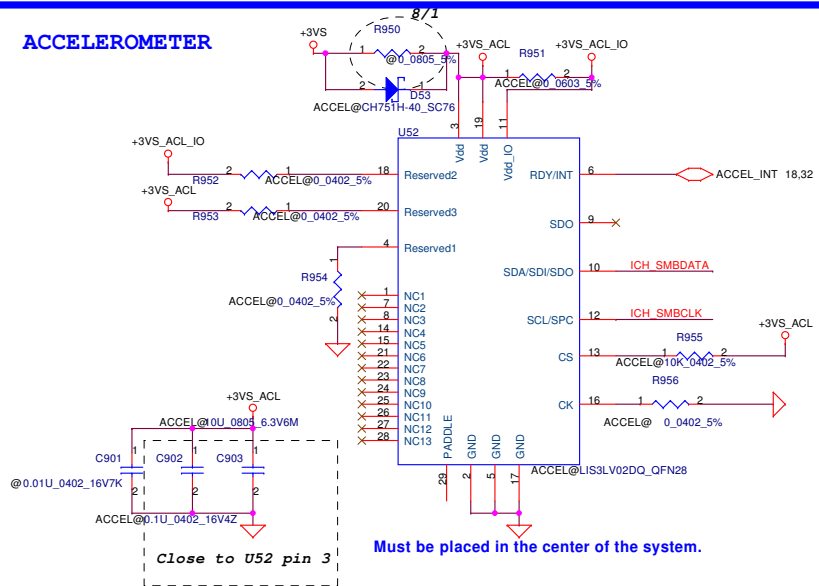


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2006/02/27	Deciphered Date	2007/02/27			
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				Magnetic & RJ45/RJ11		
				Size	Document Number	Rev
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Mini-Express Card---WLAN

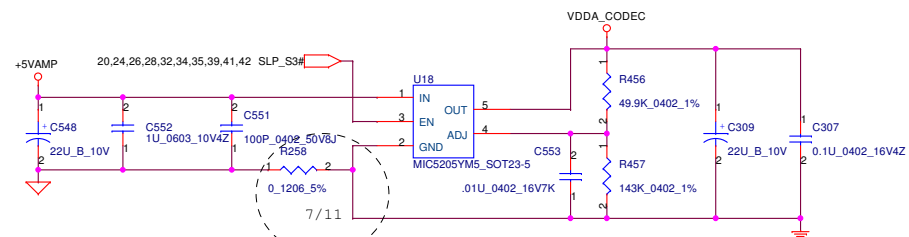


ACCELEROMETER

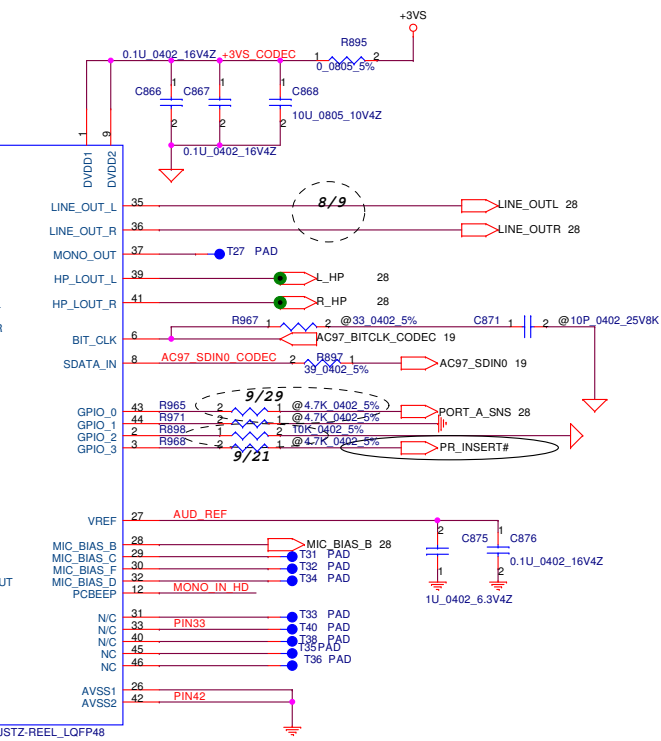


Must be placed in the center of the system.

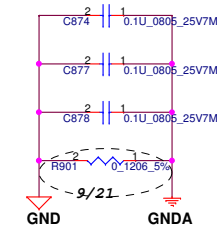
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2006/02/27	Deciphered Date	2007/02/27	Title Mini-Card/ACCELEROMETER		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
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7/19



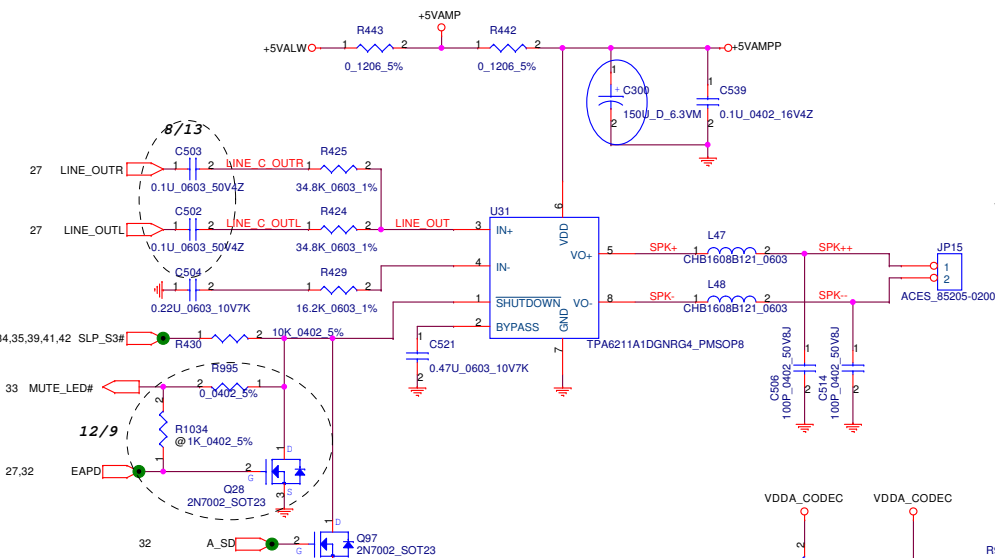
Place close to U14



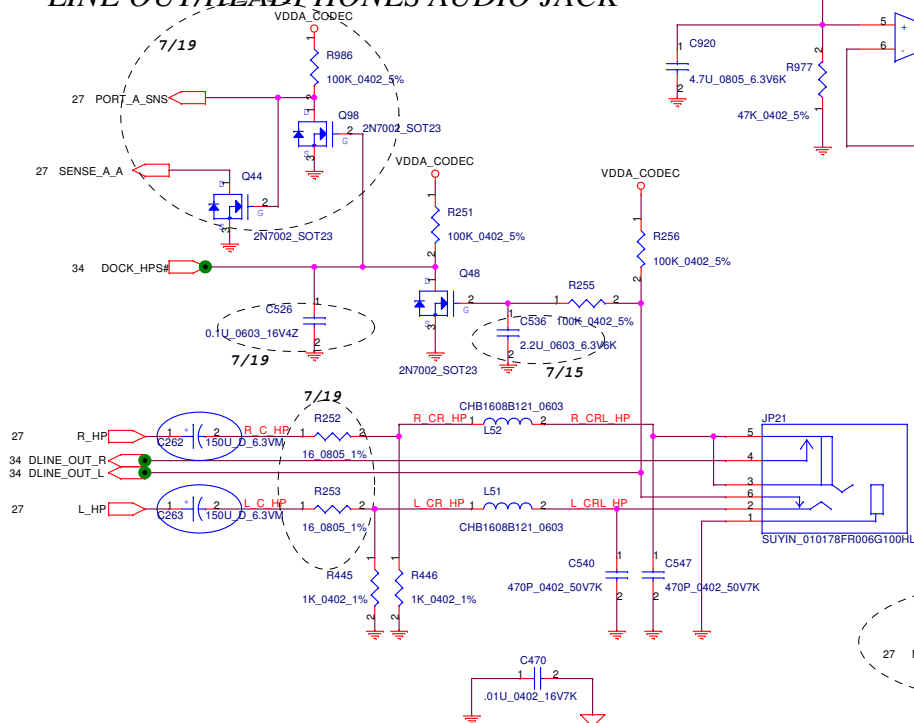
PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT, DOCK HP I
PORT B	M/B MIC
PORT C	DOCK LI
PORT D	M/B SPK
PORT E	X
PORT F	Internal MIC

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Issued Date	2006/02/27	Deciphered Date	2007/02/27	Title	
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				Document Number	0
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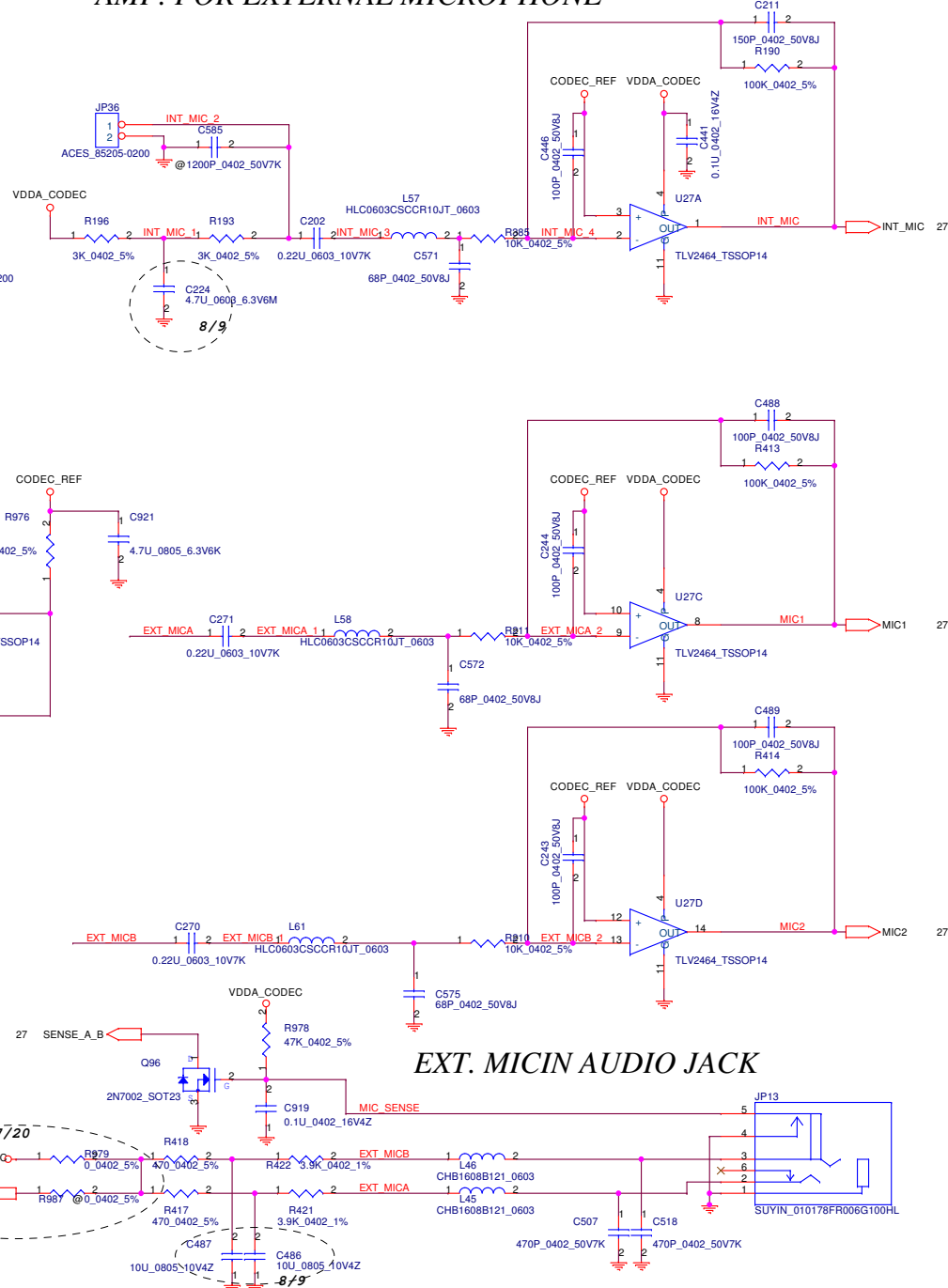
AMP. FOR INTERNAL SPEAKER



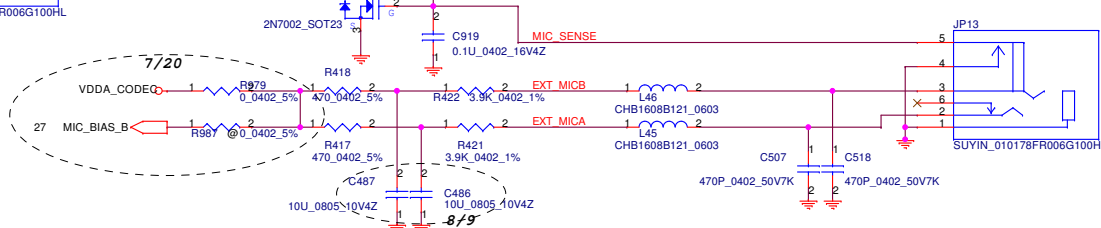
LINE OUT/HEADPHONES AUDIO JACK



AMP. FOR INTERNAL MICROPHONE AMP. FOR EXTERNAL MICROPHONE



EXT. MICIN AUDIO JACK

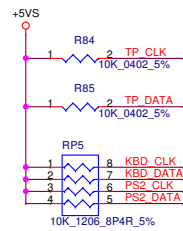
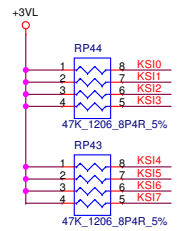
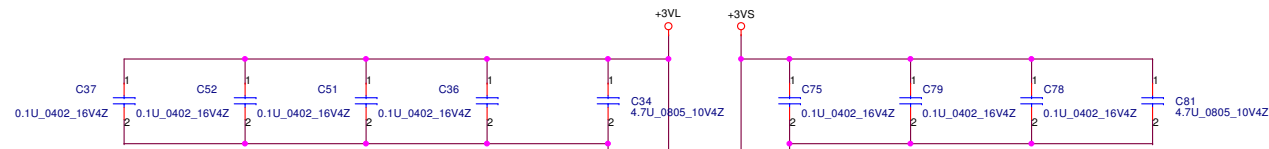


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Date: Tuesday, February 28, 2006				Sheet 28 of 49

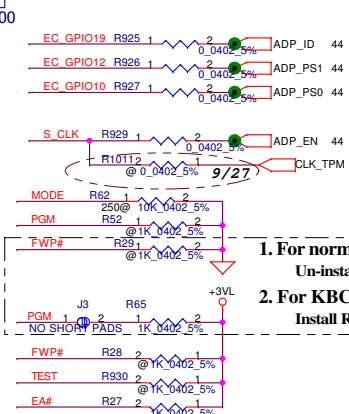
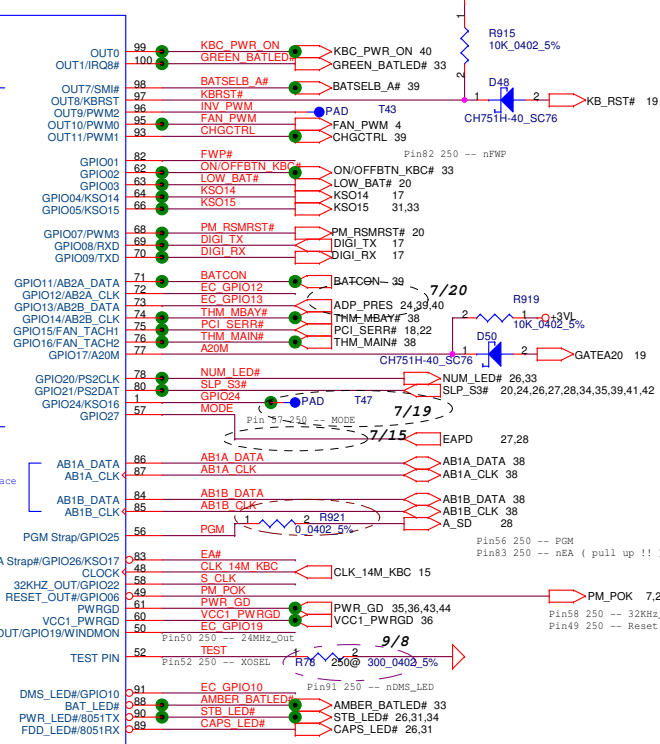
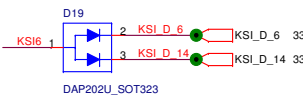
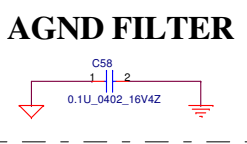
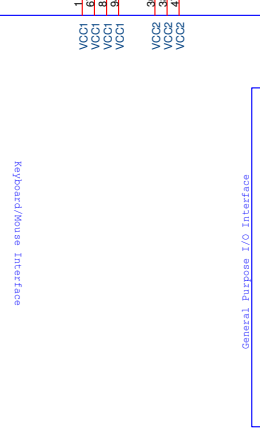
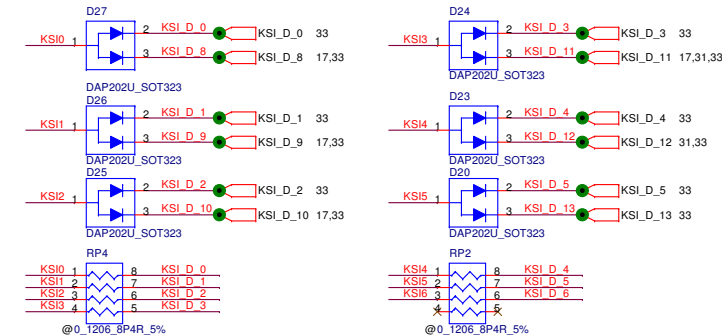
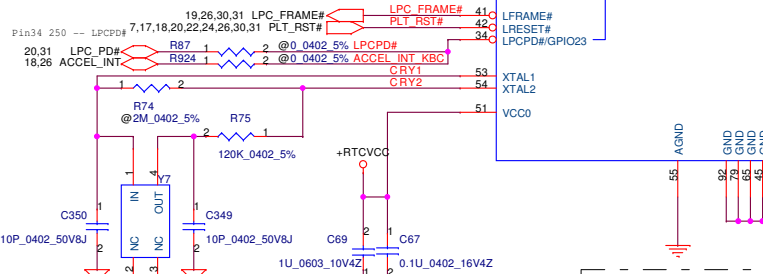
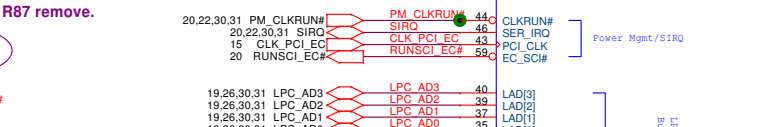
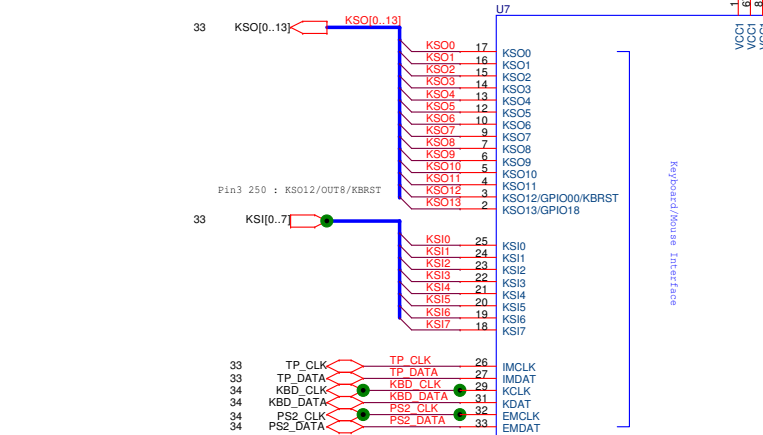
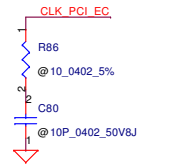
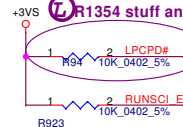
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Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2006/02/27	Deciphered Date	2007/02/27	USB & BT Connector		
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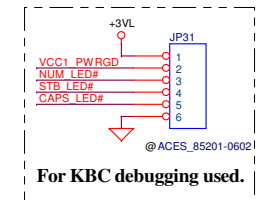
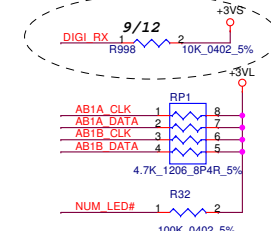
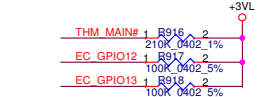
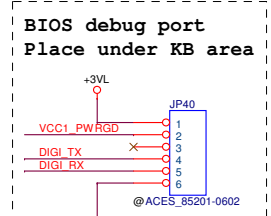
250@	1021@
R78	R930
R62	



Note: R94 must be removed when R1354 stuff and R87 remove.



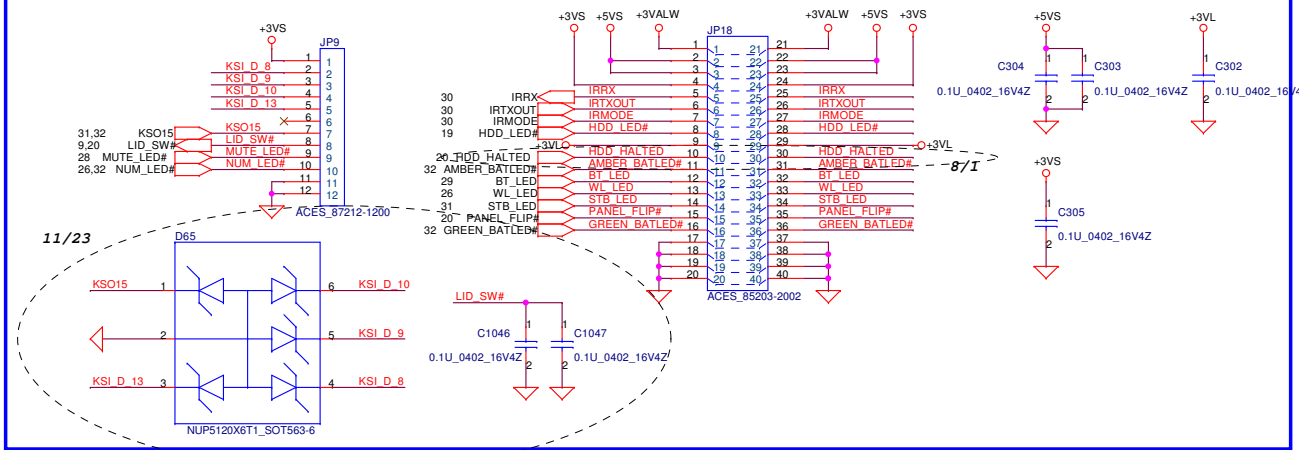
1. For normal operation:
Un-install R29,R65
2. For KBC internal ROM flash:
Install R29,R65



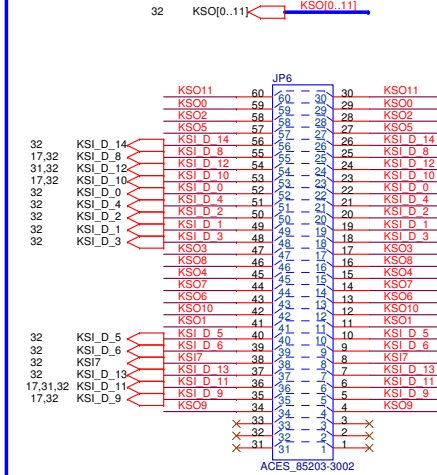
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Issued Date	2006/02/27	Deciphered Date	2007/02/27	Title		
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FUN BD.

FIR & LED BD.

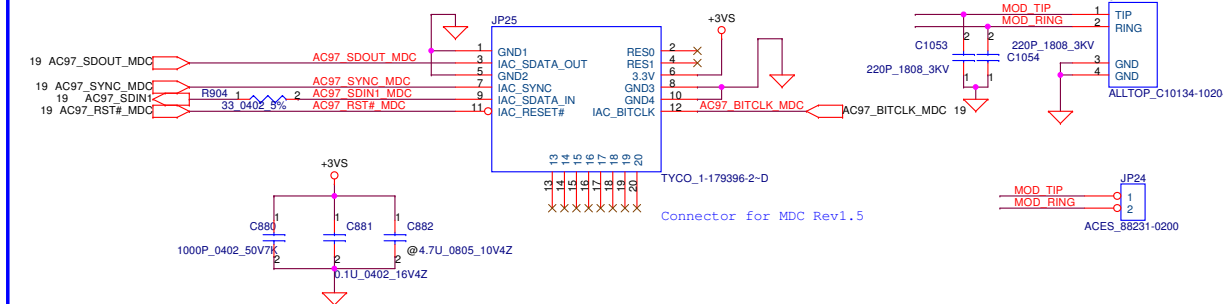


INT_KBD CONN.

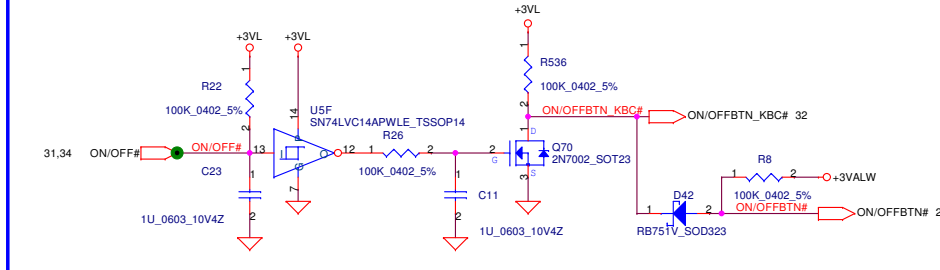


MDC 1.5 Conn.

RJ-11 CONN.

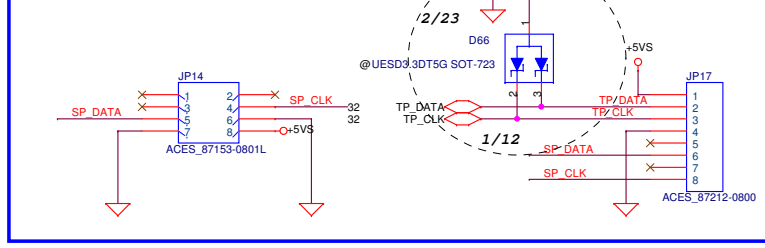


Power button



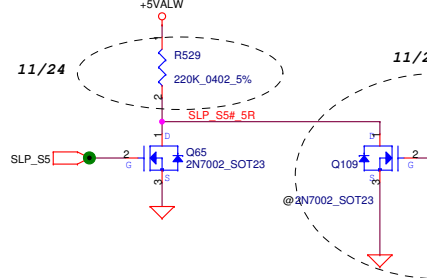
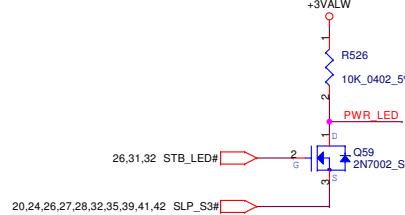
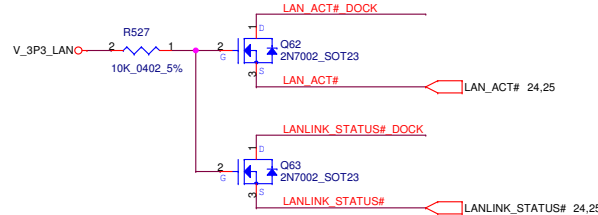
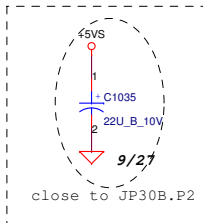
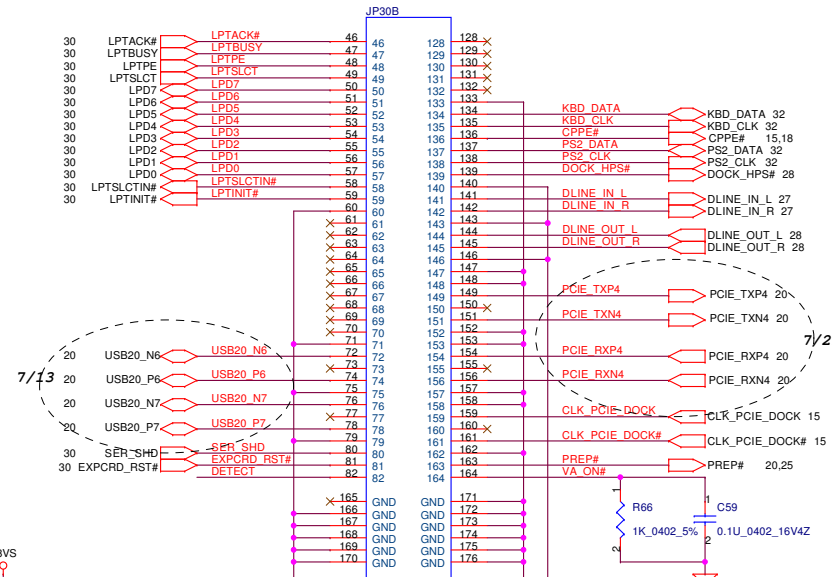
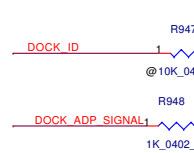
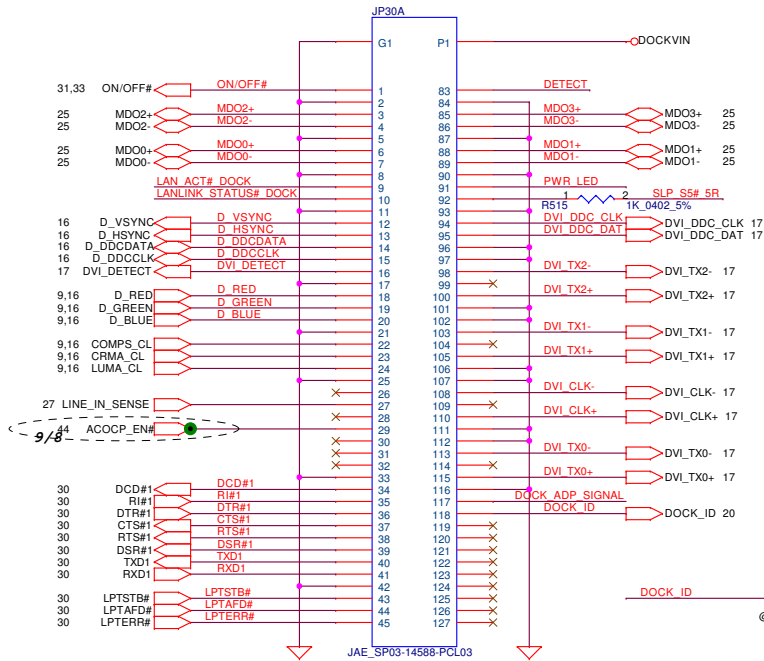
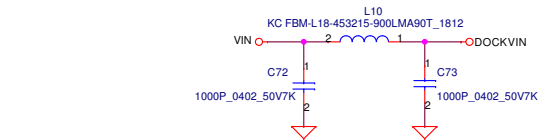
TrackPoint CONN.

TP BD.

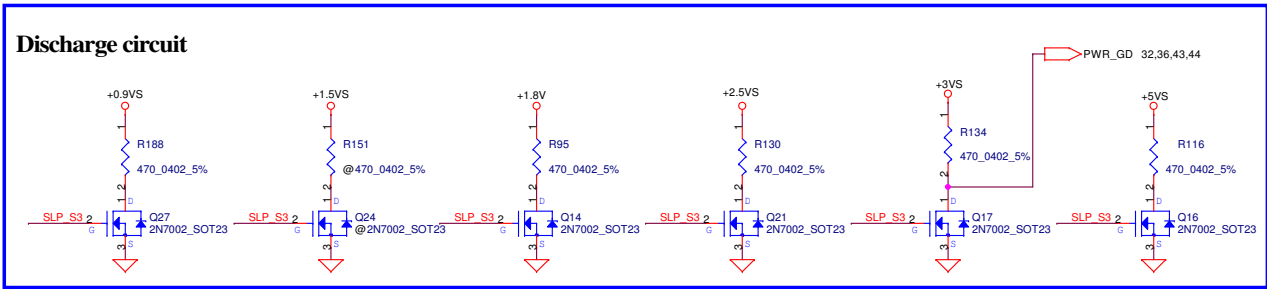
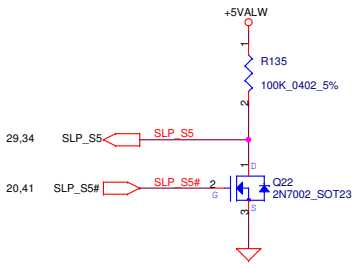
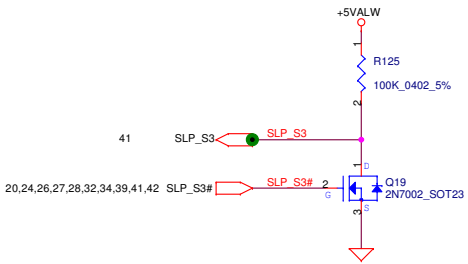
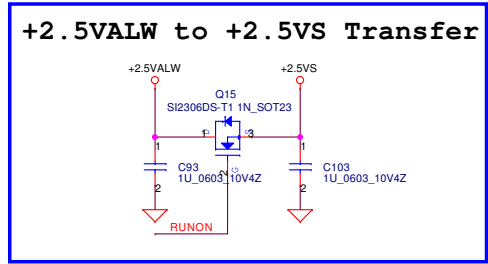
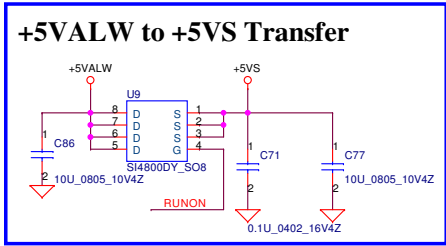
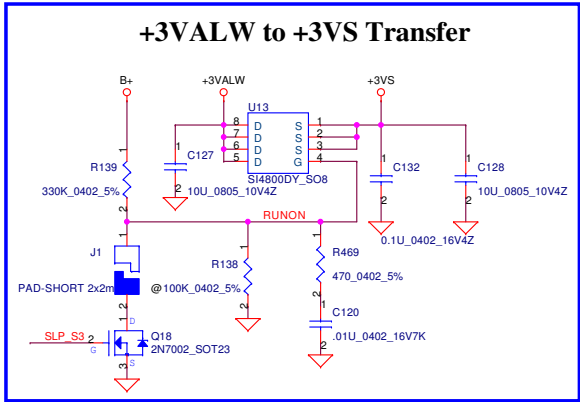


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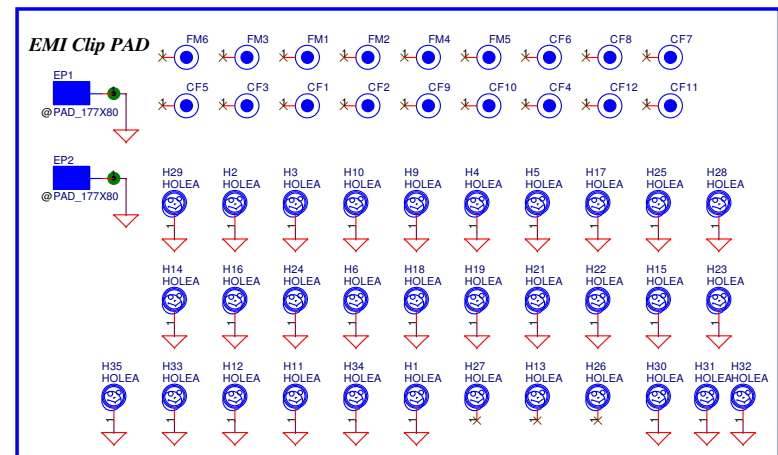
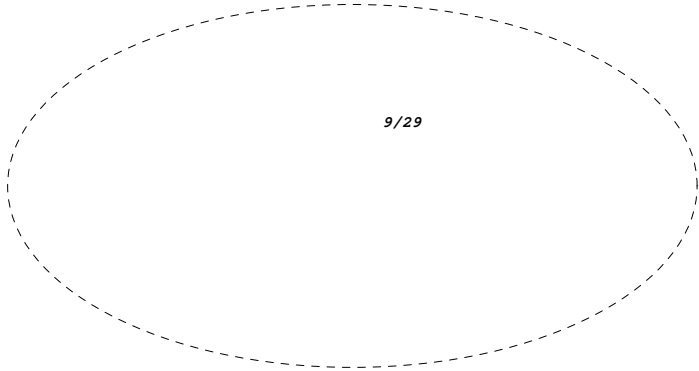
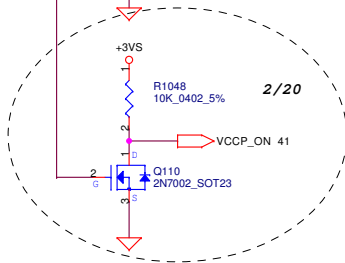
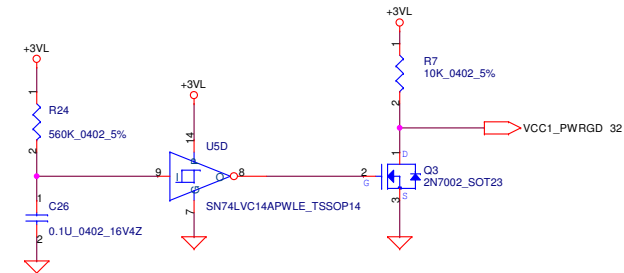
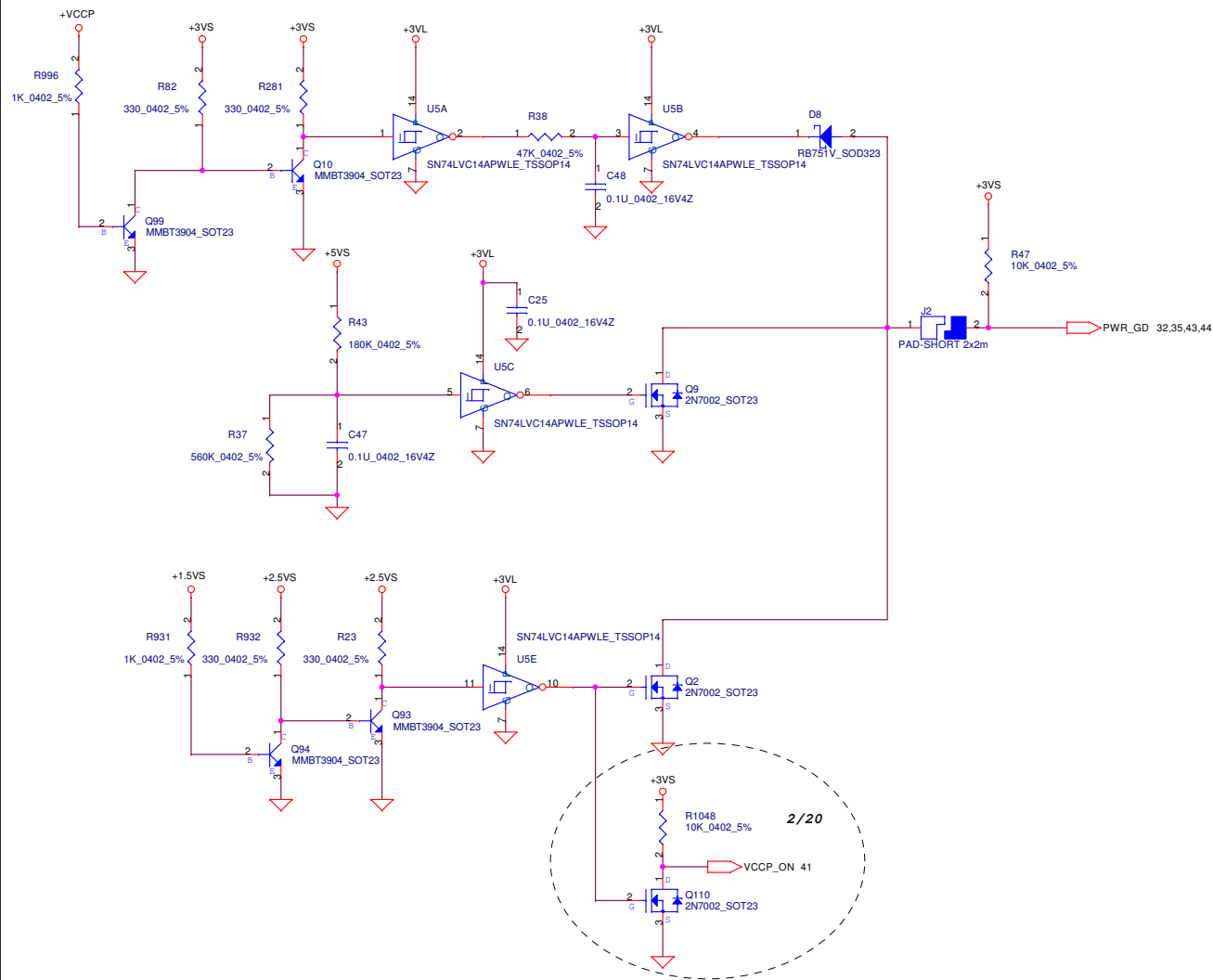
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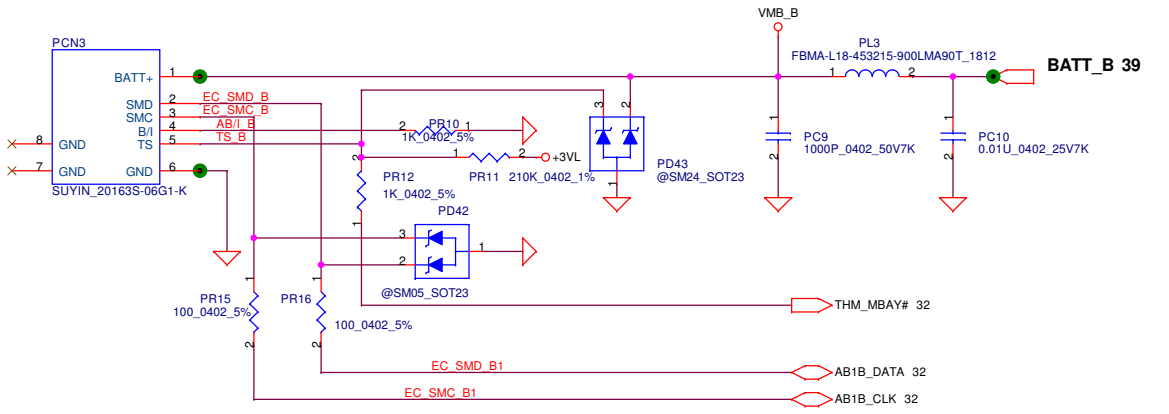
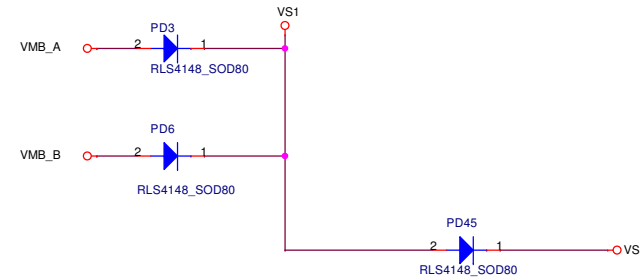
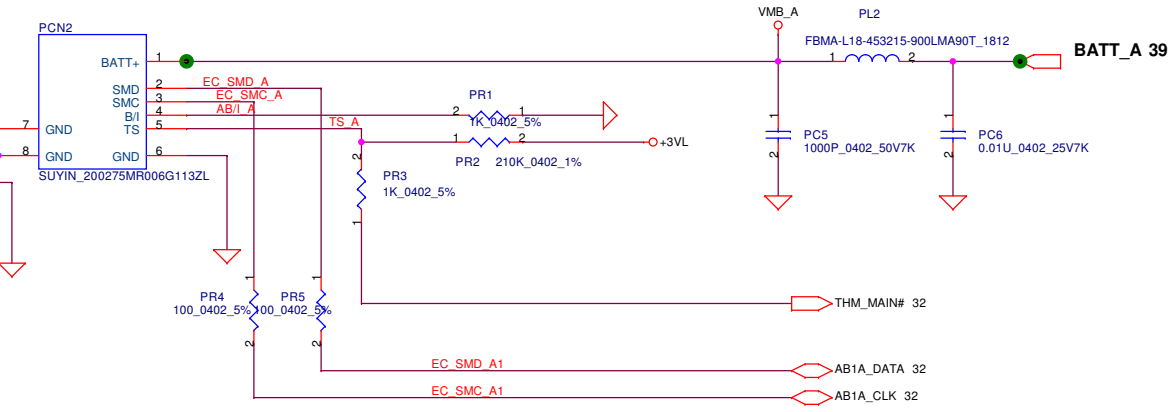
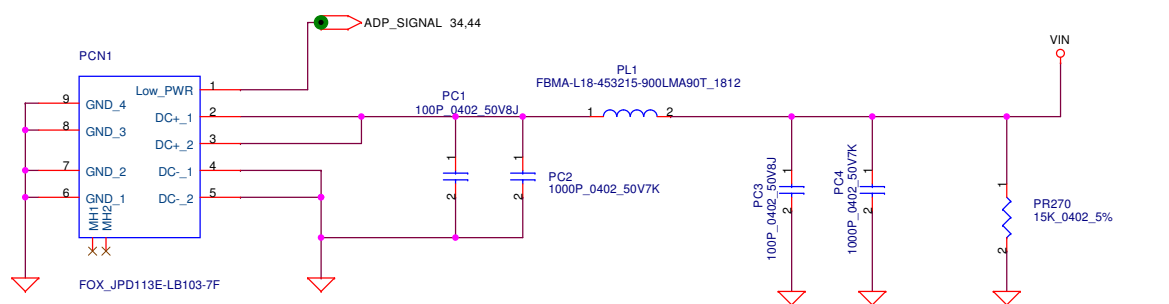
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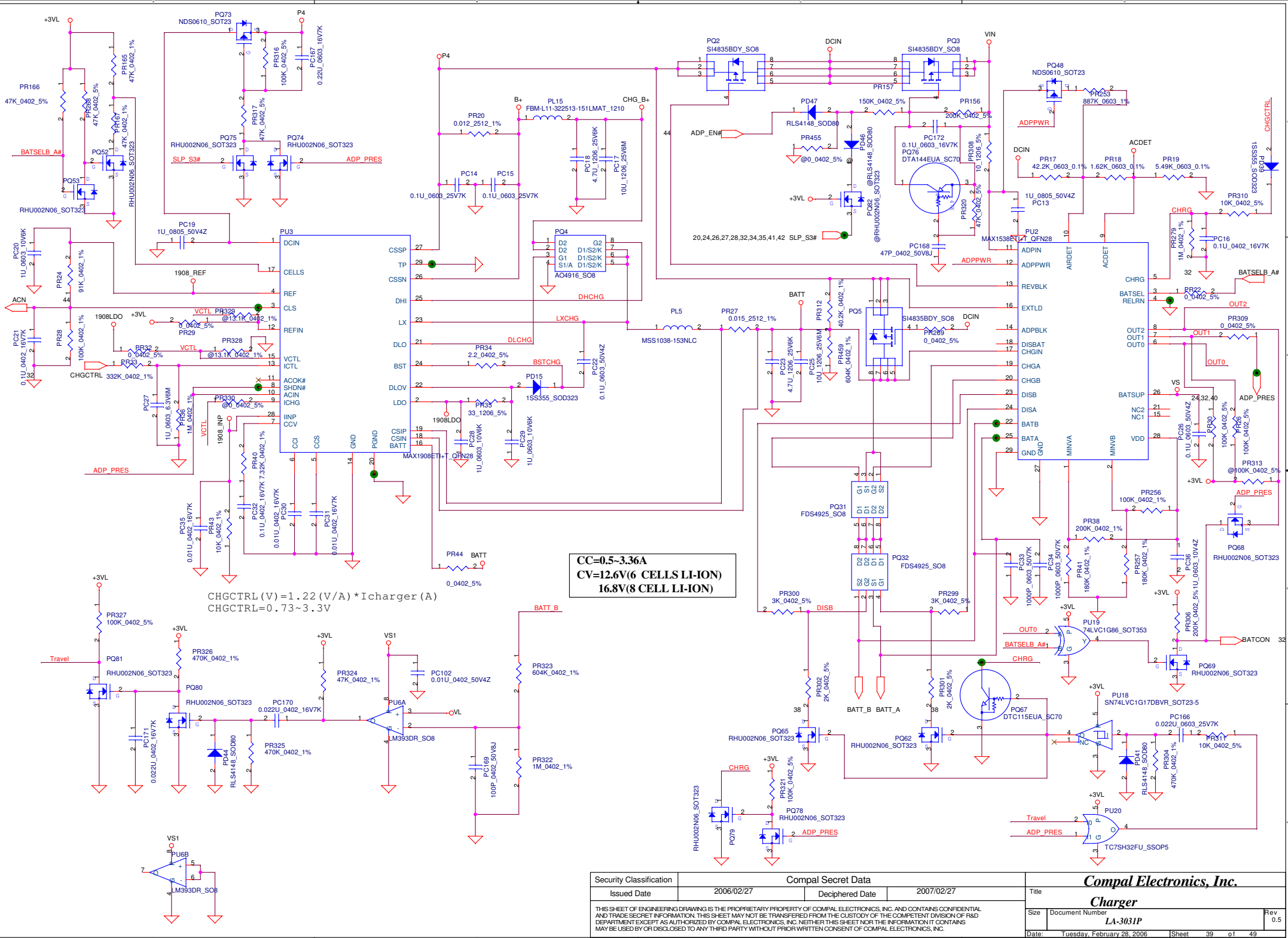
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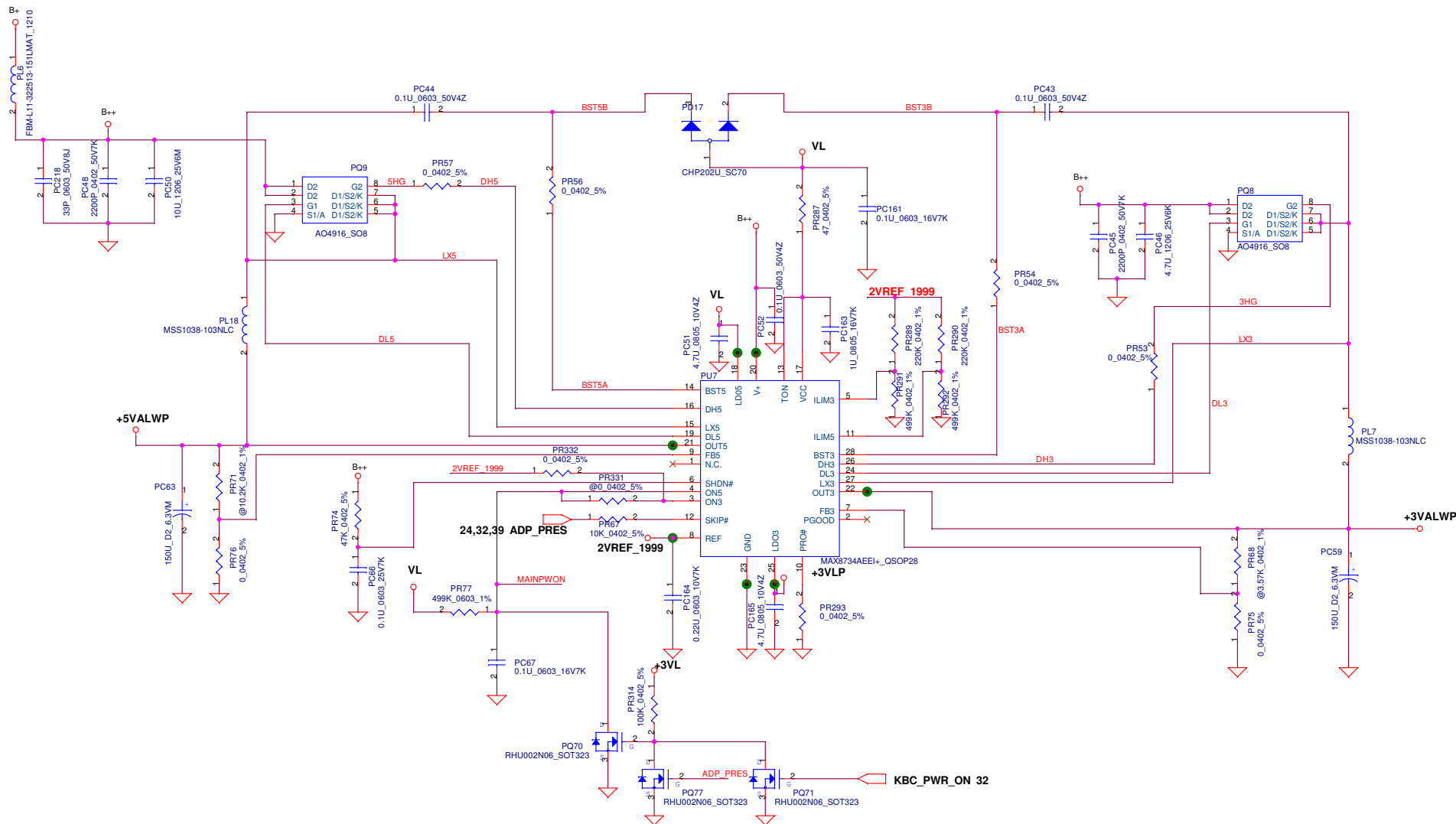
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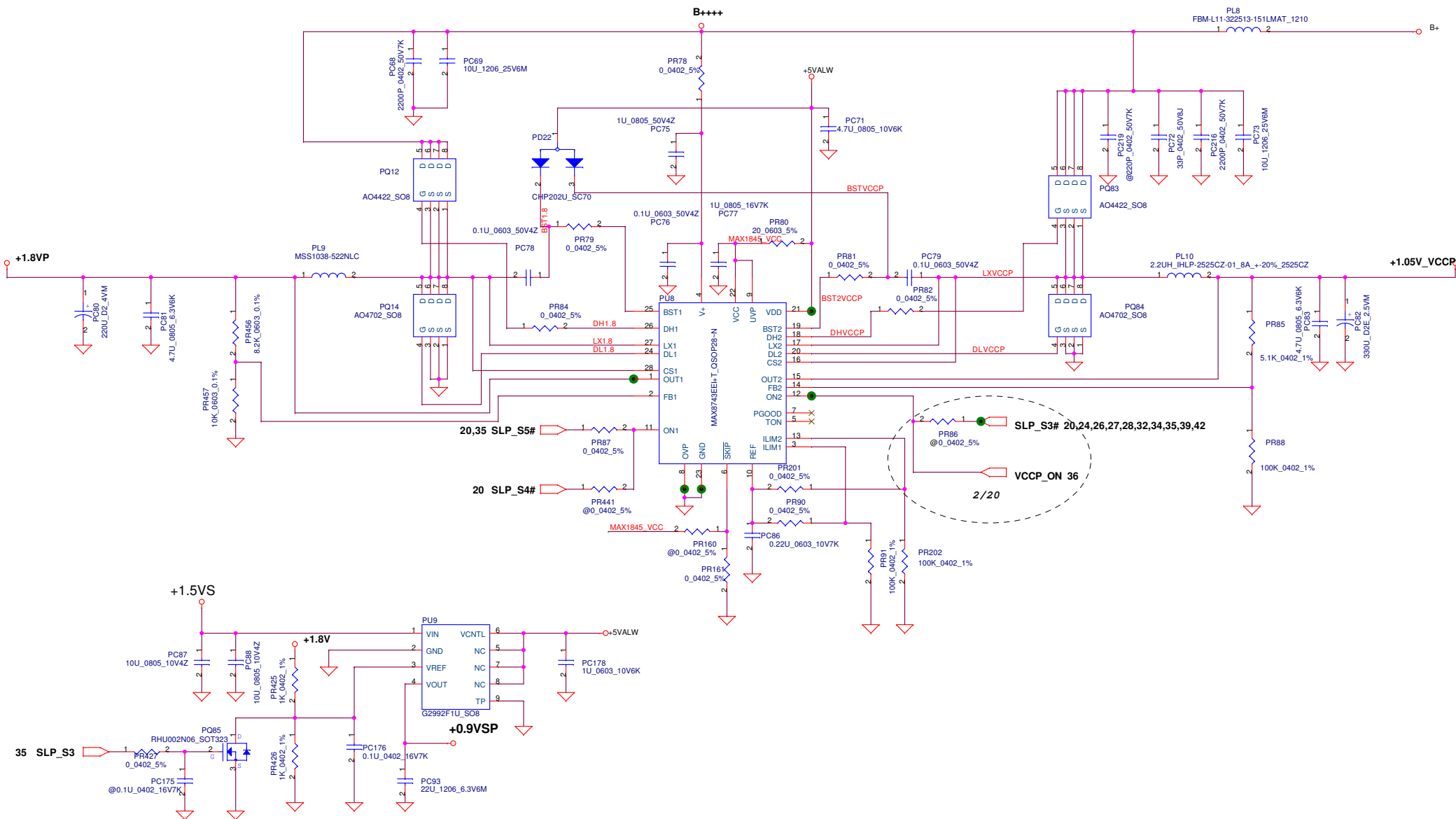
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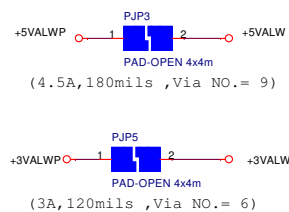
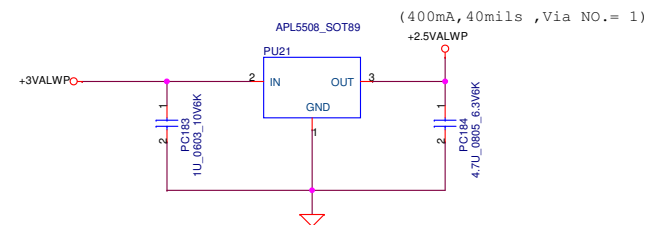
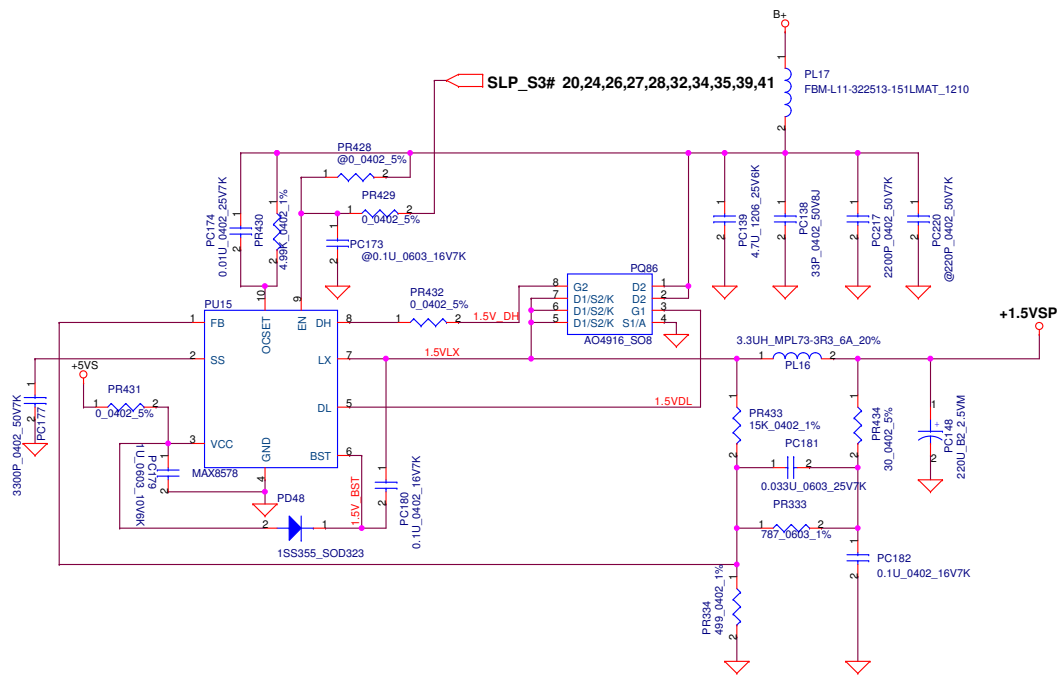
+3.3V/+5V



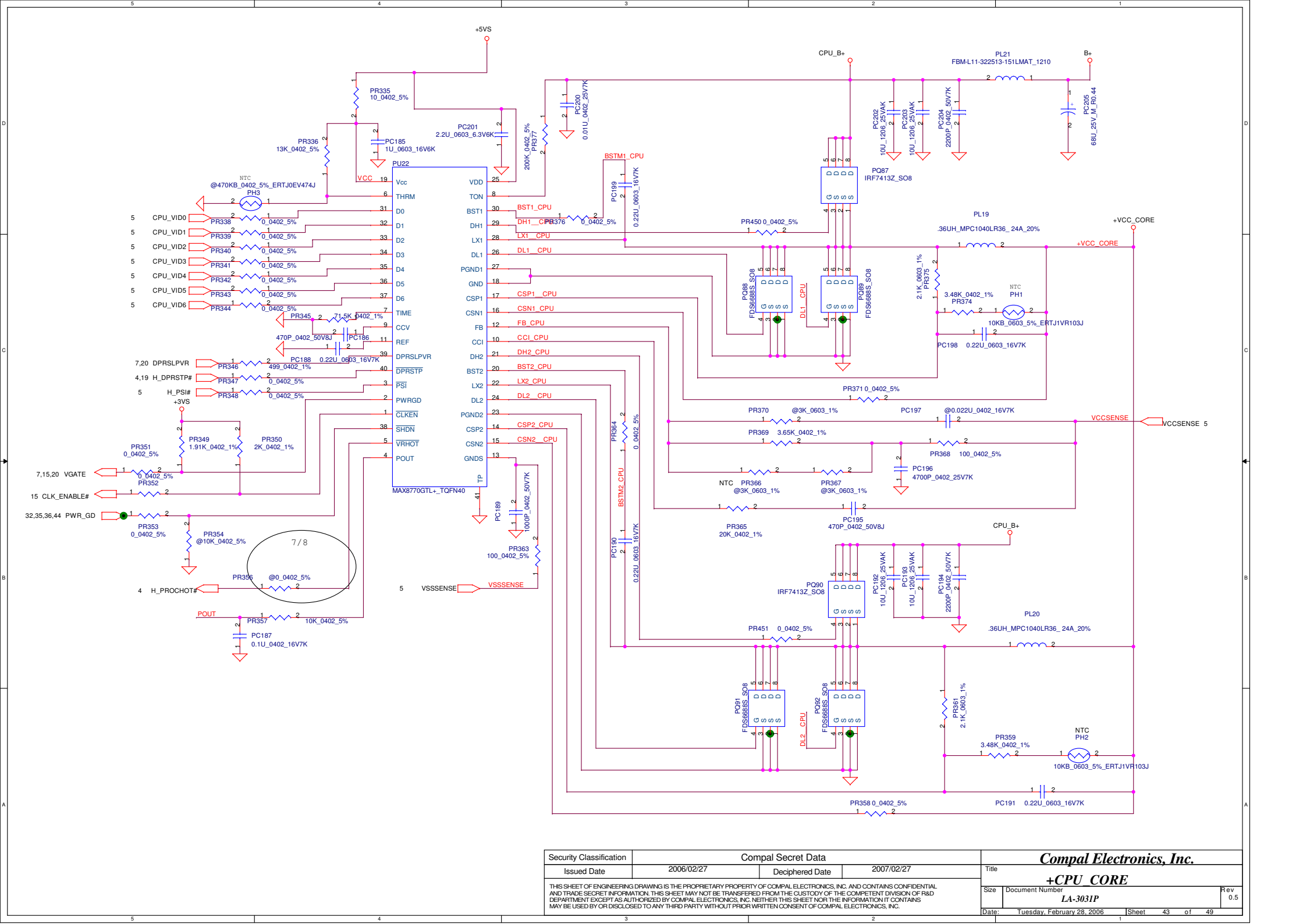
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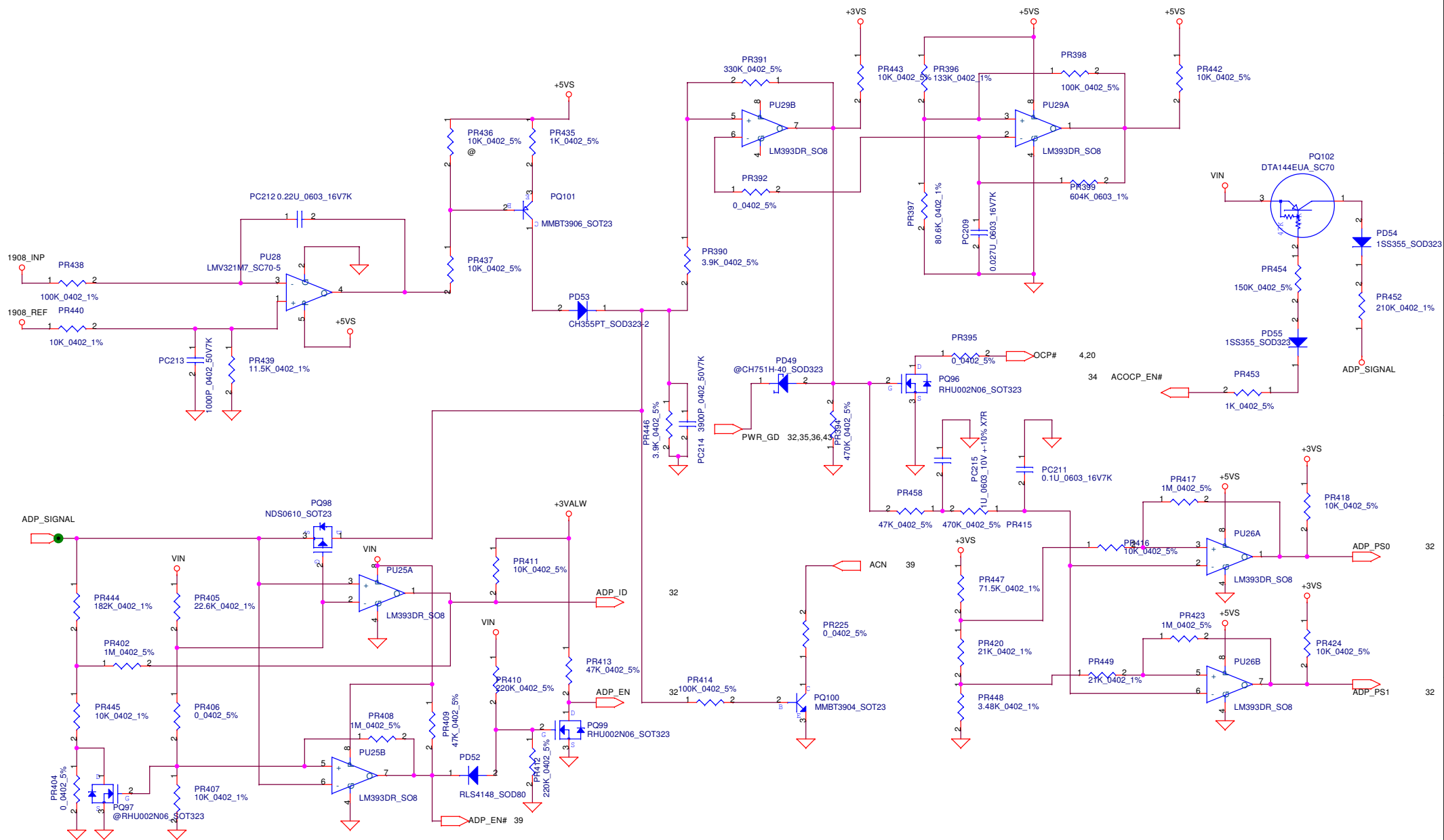


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DB Build:

07/19/2005

Page 4 -Remove R565 and R566 and disconnect from +VCCP.

Page 10 - Add a 47uF cap on U15H.E21,F21 for resolution of possible wavy video issues..

Page 10 - Add a 47uF cap on R615-2 for resolution of possible wavy video issues.

Page 16 - Add R988 and R989 to leave the option in the future to change the values for impedance matching.

Page 20 - Make U28C.E23 a test point.

Page 27 - Change DOCK_HPS# to PORT_A_SNS at R965

Page 27 - delete R979 and jumper

Page 27 - delete R894 and jumper

Page 27 - delete R900 and jumper

Page 27 - Change CODEC_REF to MIC_BIAS_B on pin 28 of U14

Page 27 - Connect LINE_IN_SENSE to pin 27 of JP30A docking connector

Page 27 - Change R526 from 1uF to 0.1uF

Page 27 - Reserve C917.

Page 27 - Reserve R901

Page 28 - add zero ohm mic bias options to VDDA_CODEC and MIC_BIAS_B

Page 28 - add inverting fet and PORT_A_SNS sense signal

Page 28 - Change R252, R253 from 0402 to 0805 package size.

Page 32 - Remove R928

Page 32 - Remove R538 and disconnect net EC_GPIO12 from +3VL.

Remove J10 and J12. EC_GPIO12 should be directly connected to ADP_P51

Page 32 - Remove J15 and disconnect net BATCON from OUT0.

Page 32 - Remove J11 and connect diode CH751H-40_SC76 (pin 2) to EC_GPIO13 and pin1 to ADP_PRES.

Page 34 - Connect JP30A.27 to LINE_IN_SENSE

07/20/2005

Page 28 - Connect R418 and R417 side 1 together to apply the bias voltage (VDDA_Codec or the optional MIC_BIAS_B) to both the tip and ring.

Page 32 - Remove D62

07/21/2005

Page 20 - Remove connections for USB_OC#3 and USB_OC#4 from the USB ports and USB_OC#2 net from RP55.

Page 20 - Reserve R789 for Calistoga A1.

Page 20 - Connect Net PM_EXTTS#0 (U15B.F25) to JP34.50 and JP10.50 for TS.

Page 26 - Remove Mini-Card Clip JP38.

Page 26 - Reserve 0-ohm option resistor from XMIT_OFF to XMIT_OFF# to bypass Q92

07/22/2005

Page 17 - Modify fingerprint signal.

Page 20 - Change PCIE port 5 to PCIE port 4 for the PCIE channel for the dock

07/25/2005

Page 7 - Reserve R586. because IMVP6 VR had installed a series Resistor (500-Ohm)

07/27/2005

Page 17 - add 2 pins GND by removing B+_LCD *1 and LCDVDD *1 and modify all signals except LVDS

Page 29 - Install D54, D55 and D56 for HP request.

07/28/2005

Page 4 - Add C932 and C933 for EMI request.

Page 27 - Add L78 for EMI request.

07/29/2005

Page 4 - Modify the thermal sensor from ADM1032 to ADT7461.

Page11 - Reserve R626 per the latest Intel CRB schematics v1.502

Page19 - Remove +3VS from SATA for HP request.

08/01/2005

Page22 - Modify R957 and R958 from 2.2K to 100K for TI request.

Page26 - Reserve R950.

EE PIR list

08/03/2005

Page16 - Add R991, R992 and R993 for EMI.

08/09/2005

Page 27 - add open pull down resistor (R994) option on SENSE B for ADI request.

Page 27 - delete C915 and C916 for ADI request.

Page 28 - add resistor (R995) jumper option between pins 1 and 2 of Q97 for ADI request.

Page 28 - change C224 from 1uF to 4.7uF for ADI request.

Page 28 - change C487, C486 from 4.7uF to 10uF for ADI request.

08/12/2005

Page 17 - change D62.4 from _USB_VCCA to +3VS.

08/13/2005

Page 28 - change the option bypass R995 to bypass Q28

Page 28 - Change C502 and C503 from 0.1uF to 0.22uF

08/15/2005

Page 24 - reserve R856by Boardcom request.

08/17/2005

Page 28 - Change C502 and C503 from 0.22uF to 0.1uF

SI-1 Build:

08/19/2005

Page 7 - Install R587 and R592 for V_DDR_MCH_REF.

Page 26 - Move +3VL from JP37.39 to JP37.45 and move CAPS_LED# from jp37.41 to JP37.51.

09/08/2005

Page 4 - Change the Thermal Sensor U16 back to ADM1032.

Page 18 - Install R742 to connect ACCEL_INT to PCI_PIRQH# (U28B.G7).

Page 20 - R793 on U28C.E20 should be NC (with @ symbol NOT ACCEL@) to disconnect U28C.E20 from ACCEL_INT.

Page 25 - disconnect R270 & R271 from C320.

Add another 1000pF 2 to 3KV capacitor to ground for R270 & R271 connection

Page 29 - Change the timing capacitor C582 on U12 pin 3 from 0.1UF to 0.001UF

Page 32 - R78 should have an "250@" symbol and should not be installed for the 1021.

Page 34 - Route ACOC_P_EN# from the circuit to the docking connector JP30A.29 and remove net SM_ADPTR.

09/12/2005

Page 20 - Remove R792 and R793 and disconnect nets ADP_ID and ACCEL_INT from U28C.E20. Make U28C.E20 a TP.

Page 32 - Add R998 for KBC TX issue.

09/14/2005

Page 17, 20 - Connect JP28.40 to U28.E23 for digitizer sleep pin.

Page 26 - install R990 and un-install R891, R892 and Q92 for BIOS code implement.

09/16/2005

Page 15 - Modify R660 from 475 ohm to 4.7K ohm to meet ICS spec

Page 15 - Install R639, R641 to meet ICS spec

Page 15 - Modify R642, R644, R647, R653, R943, R944, R666, R669, R678, R682, R685, R687, R689, R691, R702, R705, R713, R714 from 33 ohm to 24 ohm to meet ICS spec

Page 15 - NI R643, R645, R648, R654, R659, R661, R662, R663, R667, R670, R679, R683, R686, R688, R690, R692, R703, R706, R708, R709, R981, R982 to meet ICS spec

Page 19 - Change R754, R755, R756, R757, R759, R760, R765, R766 from 330hm to 390hm.

Add 390hm series resistors to AC97_SDIN0, AC97_SDIN1.

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EE PIR list (II)

9/21/2005

- Page 27 - Install 10K ohm resistor in the R898 location and install R901 with 0 ohm.
- Page 28 - Resistor R995 should be placed from gate of Q28 to drain pin 1

9/23/2005

- Page 22 - Add damping resistor on SD_DAT/SD_CMD.
- Page 23 - Modify R983 from 4.7K to 33 ohm for CARDBUS issue.

9/27/2005

- Page 10 - Add placeholder for 47uF capacitor at R616.2 to GND and R617.2 to GND for bulk capacitance on +3VS_TVDACB and +3VS_TVDACA.
- Page 24 - Disconnect PLT_RST from U6A.C2. Add circuit shown for PLT_RST#_LAN and connect signal PLT_RST#_LAN to U6A.C2.
- Page 26 - Add circuit for +3VS_MINI. Add pads for JP37.24 to +3VS and +3VALW.
- Page 29 - At R454.2 node, add placeholder NI for @0.1uF cap to GND.
- Page 31 - Add CLK_TPM signal at R929.1 with NI @00hm option. Connect this to U47.13 with another NI @00hm option on this pin.
- Page 34 - At JP30B.P2, add placeholder for 22uF NI @ capacitor.

9/28/2005

- Page 25 - Modify C320 and C934 from 1000p 3KV to 2200p 2KV.

9/29/2005

- Page 22 - Add the termination resistor for SD card overshoot and undershot.
- Page 27 - install R965 to fix the issue of "internal speaker no sound" that found on all DB-B M/B.
- Page 36 - Remove the PGD_IN circuit
- Page 36 - Remove the VGATE_INTEL circuit

10/04/2005

- Page 15 - Move PCIE_LOM/PCIE_LOM# from SCRCLKT1/C1 to SRCCLKT2/C2 (U25.22, U25.23).
- Page 24 - Add Circuits to prevent leakage from BCM5753M and is urgent to implement in SI-1.
- Page 24 - Remove R656 and disconnect from +3VS and connect CLKREQA# to circuit
- Page 24 - Add 0-Ohm NI resistors on ICH_SMBCLK and ICH_SMBDATA on U6A.D9/D8. This is to leave I2C disconnected and reserved for ASF implementation.

10/06/2005

- Page 7 - add 0-Ohm jumper Installed for DDR_THERM#.
- Page 22 - At U23B.G6, add 0-Ohm jumper to +S1_VCC. Change R829 to 0-Ohm and NI R829.
- Page 24 - Change U44 from AT24C512N (512kB) to AT24C64A which is a 64kbit EEPROM.

10/07/2005

- Page 18 - Change U39.5 and U40.5 to +3VALW.
- Page 24 - Add 4.7kOhm pulldown to GND on LOM_LOW_PWR U6A.J5 and NI U43.
- Page 24 - Change R865.1 rail to +3VALW

10/11/2005

- Page 20 - modify R522 from 10K to 100k and the rail from V_3P3_LAN to +3VALW
- Page 24 - Install 4.7kOhm Pullup Resistors to +V_3P3_LAN at R1013.2 and R1014.2.
- Page 25 - Change R871 to 10K-Ohm.

11/10/2005

- Page 15 - Reserve the workaround circuit for MAXIM IC issue.
- Page 20 - Swap PANEL_FLIP# from GPIO39 to GPIO12 and add a pull-up resistor.

11/14/2005

- Page 17,20,29 - Change USB20_P1, N1 to No Connects. Connect USB20_P2,N2 to Fingerprint. Change JP11.2 and JP11.4 from USB20_N2/P2 to USB20_N5/P5 respectively. Swap USB_OC#5 and USB_OC#2.
- Page 25 - Add 4x 12nF 100V capacitor placeholders at R269.2, R270.2, R271.2, and R272.2.
- Page 28 - Add the R1034(1Kohm) and the R995(00hm) between EAPD and EAPD#. Change net name from EAPD# to MUTE_LED#.

11/15/2005

- Page 20 - Move LP_EN# from GPIO27 (U28C.B21) to GPIO8 (U28C.E21). Make U28C.B21 a Test Point
- Page 24 - AF30 have black screen issue when AC plug-in(LP_EN# inactive).
This issue is caused by PLT_RST# dropped to 1.12V.
Change R1007 from 0 ohm to 220K ohm for solving this issue.

Add R1025 (10k ohm) in PLT_RST#_LAN.

11/17/2005

- Page 24 - Add C1044 (0.1uF cap.) to GND at Q57.2.
- Page 25 - Change C1040, C1041, C1042, C1043 in series with R269-2, R270-2, R271-2, and R272-2. INSTALL C1040, C1041, C1042, and C1043. Remove C934. Connect C320 to R269-1, R270-1, R271-1, and R272-2.

11/18/2005

- Page 25 - Change C1040,C1041,C1042,C1043 value from 12nF to 10nF.
- Page 24 - Change Q103.1 net name to LOM_PCIE_WAKE#.
- Page 20 - Change Q77.3 net name to LOM_PCIE_WAKE# and disconnect from R796.1. Install R796 and give R796.1 net name PCIE_WAKE#.
- Page 24 - Change C1044 to no stuff.

11/22/2005

- Page 24 - NI C826,R859,C828,R1017, R1016, R1018, R1020 and Q105. Reverse Q103.1 to LAN_WAKE# and Q103.3 to LOM_PCIE_WAKE#.
NI R1021 and Install R1022. +3VS should be powering this Schmidt Trigger.
Remove R1023, we don't need this option. Connect NIC_PD_N to D63.1 directly.
At Q86.1, add 0-Ohm(R1037) Installed option and call output NIC_PD_N.
Add Option 10K ohm(R1036) Pullup at Q86.1 but NI and pull-up to V_3P3_LAN.
Add a NI Zener Diode RB751V_SOD23(D64) in parallel with R1007.

11/23/2005

- Page 21 - Change C753 to 220uF 6.3V.
- Page 17 - Change the LCD Power Circuit from AF and Caymus. Delete R12,R474 and C28. Add R1038,R1039 and C1045. No install C20. On JP28.40, add 0-Ohm jumper on DIGI_SLEEP.
- Page 18 - Change U39.5 and U40.5 to +3VS. Install R742 and NI R741.
- Page 19 - Remove R984 and disconnect from +3VS. Make U28A.AA5 a TP.
- Page 20 - Change R522.2 to V_3P3_LAN.
- Page 33 - Add function board ESD solution. Add C1046,C1047 and D65.

11/24/2005

- Page 17 - Add 0-Ohm Jumper on JP28.18 also (DIG_RESET).
- Page 20 - Change R522.2 to +3VALW.
- Page 34 - Change R529 to 220K and at node SLP_S5#_5R add 2N7002 FET (NI) pin 1, pin 3 to GND, and Pin 2 output should have 1uF 10V Cap to GND NI, and 22Kohm series NI. Connect output of 22K to PREP#.
- Page 20 - Add LANLINK_STATUS# isolation circuit.Cange U26C.R4 (GPIO14) to LANLINK_STATUS#_SB. Add 0-Ohm option NI to bypass this circuit if necessary.
- Page 19 - Change C516 and C528 from 10pf to 15pf to solve the RTC issue.
- Page 24 - On DC mode without LAN cable plugged, system dose not provide power for LAN chip. So LANLINK_STATUS# will be driven low by LAN chip. We will add isolation CKT to solve this issue.
Add R1042,R1043,R1044,R1046,Q108.

11/29/2005

- Page 29 - Change C582 from 0.001uF to 0.047uF.
- Page 26 - J9 short and J10 open to solve that 3.3V Aux power is not present on Mini Card slot.

12/09/2005

- Page 28 - Add Q28 and delete R1034 because audio driver not ready.
- Page 29 - Change C582 from 0.047uF to 1500pF.

01/04/2006

- Page 6 - Reserve C625 and C629 to solve PCA Acoustic Noise .
- Page 26 - Add C1049 to solve EMI issue.
- Page 26 - Short J10 and un-short J9 to fix WLAN leakage.

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EE PIR list (II)

1/10/2006
Page 26 - Change J10.1 from +3VS to V_3P3_LAN to ensure that WoWLAN is supported but no leakage on DC.

1/12/2006
Page 15 - Reserve C1050, C1051 and C1052 for EMI.
Page 16 - Add L79, L80 and L81 to fix EMI issue.
Page 24 - Change RDAC R858 from 1.24kOhm to 1.21kOhm.
Page 29 - Change R513 to 1kOhm, C582 to 2200pF and C102to 220uF.
Page 33 - Reserve D66 on TP_DATA / TP CLK for EMI.
Page 33 - Add C1053 and C1054 on MOD_TIP / MOD_RING near RJ-11.

2/20/2006
Page 36 - Add the circuit for power sequence timing between +1.5VS and VCCP.

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Version Change List (P. I. R, List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	44	ADP_OCP	7/29	HP	PC212 change from 2200pF to 0.22uF	PC212 change from 2200pF to 0.22uF	
2	44	ADP_OCP	7/29	HP	PR416 change from 10K to 3.3K	PR416 change from 10K to 3.3K	
3	44	ADP_OCP	7/29	HP	PR449 change from 3.3K to 10K	PR449 change from 3.3K to 10K	
4	44	ADP_OCP	7/29	HP	PC211 change from 2.2uF to 10V_0805_6.3V6M	PC211 change from 2.2uF to 10V_0805_6.3V6M	
5	41	1.05V/1.8Vp	10/3	Intel	Intel modify DDR2 spec can not less than 1.75V.	Modify 1.8Vp soultion from fix mode to adjustable mode.	
6	39	Charger/OCP	11/14	HP	Remove PQ82 and PD46	Remove PQ82 and PD46	
7	39	Charger/OCP	11/14	HP	PR36 change from 560k to 1M.	PR36 change from 560k to 1M.	
8	44	ADP_OCP	11/14	HP	PR390 change from 27K to 3.9K_5%	PR390 change from 27K to 3.9K_5%	
9	44	ADP_OCP	11/14	HP	PC209 change from 0.22uF to 0.027uF	PC209 change from 0.22uF to 0.027uF	
10	44	ADP_OCP	11/14	HP	PR399 change from 649K to 604K	PR399 change from 649K to 604K	
11	44	ADP_OCP	11/14	HP	PC211 change from 10uF to 0.1uF X7R	PC211 change from 10uF to 0.1uF X7R	
12	44	ADP_OCP	11/14	HP	PR411 change from 47K to 10K_5%	PR411 change from 47K to 10K_5%	
13	44	ADP_OCP	11/14	HP	PR420 change from 10K to 21K_1%	PR420 change from 10K to 21K_1%	
14	44	ADP_OCP	11/14	HP	R448 change from 11.5K to 3.48K_1%	R448 change from 11.5K to 3.48K_1%	
15	44	ADP_OCP	11/14	HP	PR416 change from 3.3K to 10K_5%	PR416 change from 3.3K to 10K_5%	
16	44	ADP_OCP	11/14	HP	PR449 change from 10K to 21K_1%	PR449 change from 10K to 21K_1%	

Version Change List (P. I. R. List) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
17	44	ADP_OCP	11/14	HP	Add new 47K_5% resistor in series with PR415-2	Add new 47K_5% resistor in series with PR415-2	
18	44	ADP_OCP	11/14	HP	Add new 1uF X7R capacitor from PR415-2 to GND	Add new 1uF X7R capacitor from PR415-2 to GND	
19	41	0.9VSP	01/10	Compal	Change PU9 from APL5331 to G2992F1U		
20	40	3.3V/5V	02/27	HP	WWAN noise issue	Add new 33pF X7R capacitor from PL6,2 to PC59 2.	
21	41	1.05V	02/27	HP	WWAN noise issue	Add new 2200pF X7R capacitor to parallel PC72	
22	41	1.05V	02/27	HP	WWAN noise issue	Change PC73 from 2200pF to 33pF X7R capacitor.	
23	41	1.5V	02/27	HP	WWAN noise issue	Add new 2200pF X7R capacitor to parallel PC138	
24	41	1.5V	02/27	HP	WWAN noise issue	Change PC138 from 2200pF to 33pF X7R capacitor.	
25	41	1.05V	02/28	HP	EMI issue	Reserve PC219 220pF X7R capacitor to parallel PC72	
26	41	1.5V	02/28	HP	EMI issue	Reserve PC220 220pF X7R capacitor to parallel PC138	
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