Compal confidential

Schematics Document

Mobile AMD S1G2 CPU with ATI RX781(NB) & SB700(SB) core logic

2008-11-07

REV:0.1

Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.		
Title: *Cover Sheet*		
Size: Custom	Document Number: *LA-4114P*	Rev: 0.1
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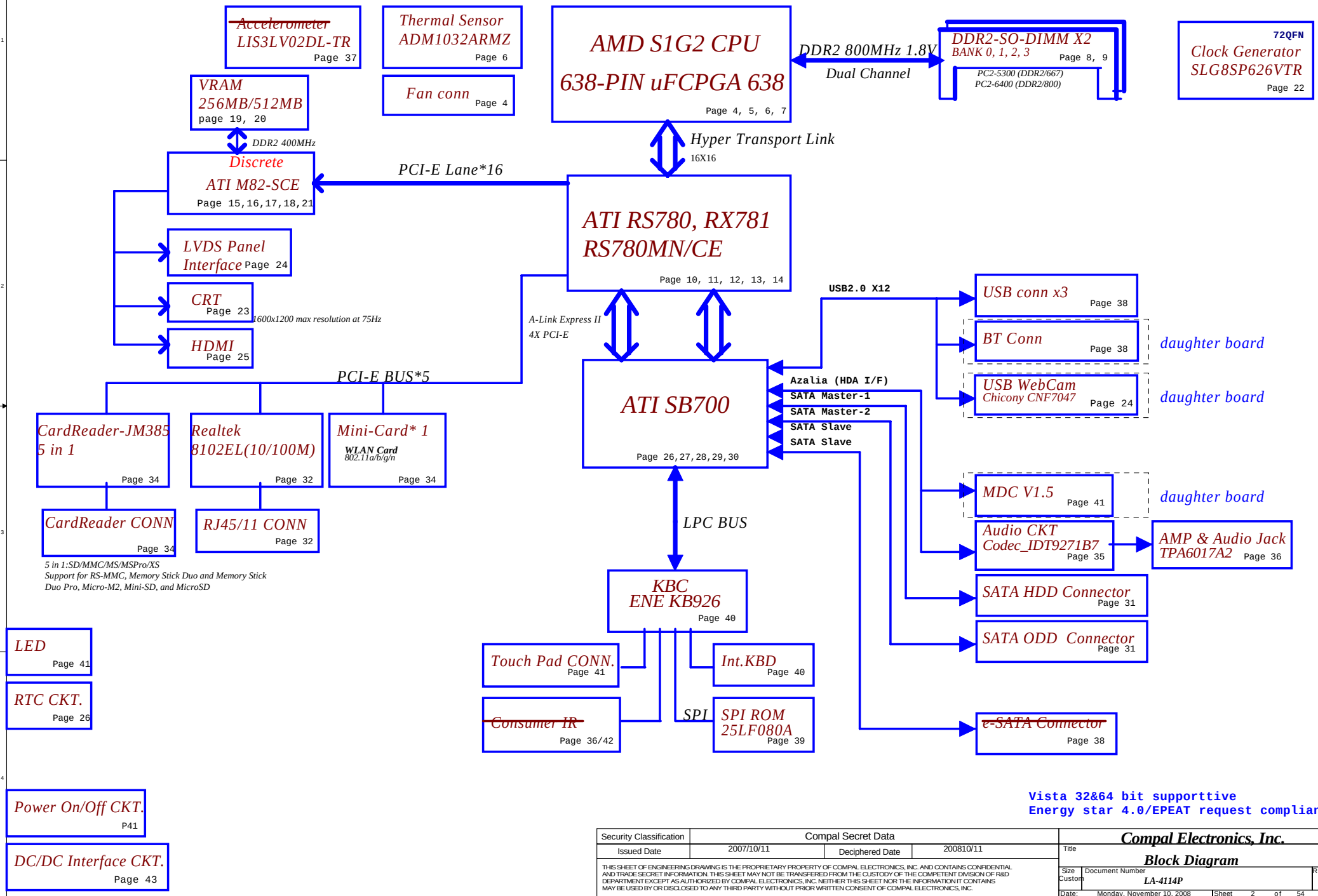
OPP Rachman AMD 14" Discrete - LA-4112P



Vista 32&64 bit supporttive
Energy star 4.0/EPEAT request compliant

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Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.			
Title: Block Diagram			
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Voltage Rails

O MEANS ON X MEANS OFF

State \ power plane	+B +3VL +5VL	+5VALW +3VALW +1.2VALW	+1.8V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_0 +CPU_CORE_1 +CPU_CORE_NB
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

<BOM Structure>
ZZZ
X76-VRAM
X76-VRAM
X7613432L04

<BOM Structure>
ZZZ
PCB-MB
LA-4114P

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010
~~ACCELEROMETER~~	3A	00111010

EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
~~24C16~~	A0H	1010 000X b
CPU SIC interface	98H	1001 100X b

EC SM Bus2 address

Device	HEX	Address
ADI1032-2 CPU	9AH	1001 101X b
ADI1032-1 VGA	98H	1001 100X b

SMBUS Control Table

	SOURCE	THERMAL SENSOR VGA M82-SE ADM1032	BATT	SERIAL EEPROM	THERMAL SENSOR CPU & ADM1032	SODIMM I / II	CLK CHIP	WL MINI CARD Slot 1	LCD	HDMI	CRT	~~G-Sensor~~
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	X	X	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	V	X	X	V	X	X	X	X	X	X	X
SCL SDA	VGA M82-SE	X	X	X	X	X	X	X	V	X	X	X
DDC4CLK DDC4DATA	VGA M82-SE	X	X	X	X	X	X	X	X	V	X	X
DDC3CLK DDC3DATA	VGA M82-SE	X	X	X	X	X	X	X	X	X	V	X
SCL0 SDA0	SB700	X	X	X	X	V	V	X	X	X	X	V
SCL1 SDA1	SB700	X	X	X	X	X	X	V	X	X	X	X
SCL2 SDA2	SB700	X	X	X	X	X	X	X	X	X	X	X
SCL3 SDA3	SB700	X	X	X	X	X	X	X	X	X	X	X

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Compal Electronics, Inc.

Title: Notes List

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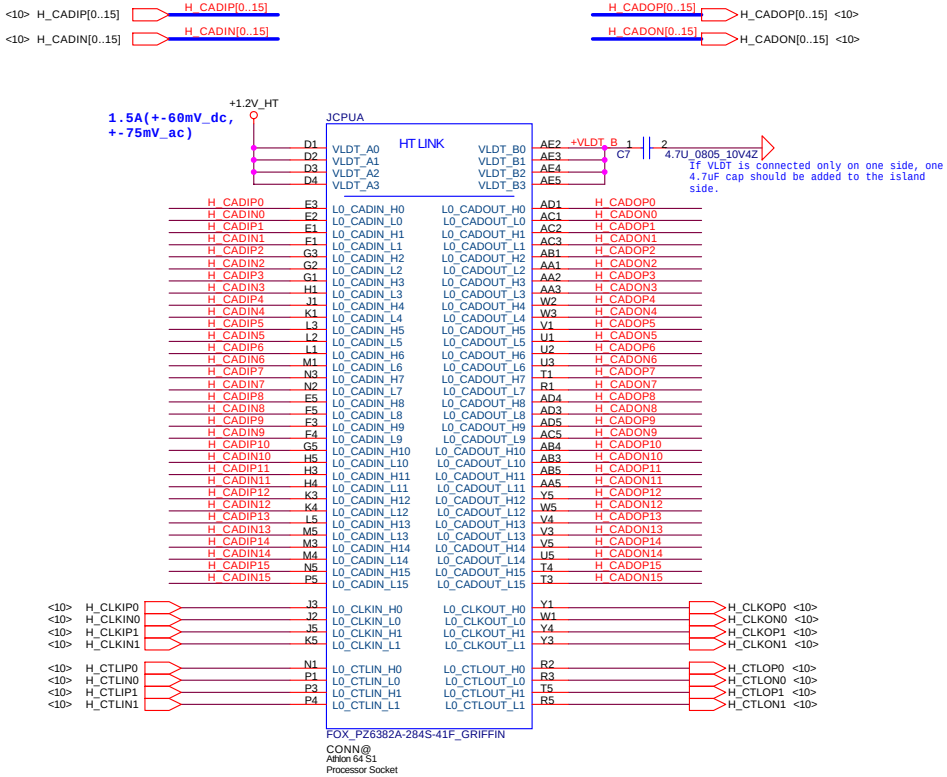

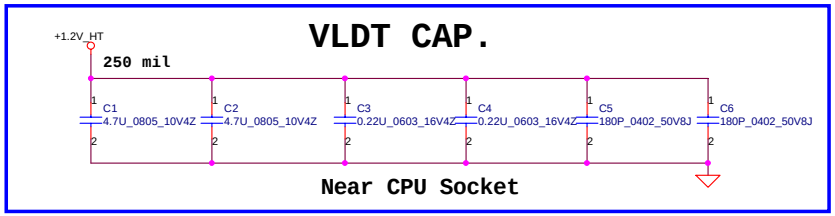

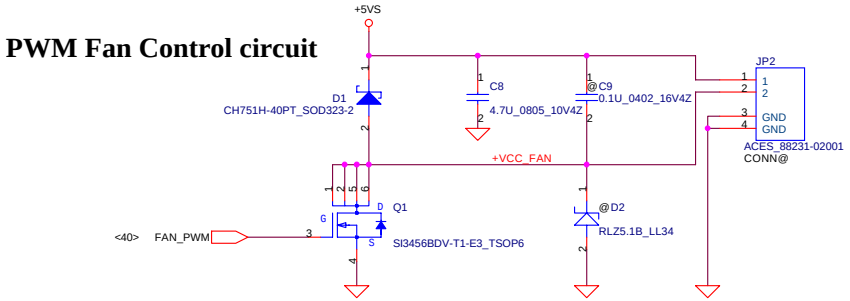

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Compal Electronics, Inc.	
Title	AMD CPU S1G2 HT I/F
Size: Custom	Document Number: LA-4114P
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Processor DDR2 Memory Interface

PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

DDR_A_CLK0 — C10 1.5P_0402_50V9C — DDR_A_CLK#0
DDR_A_CLK1 — C11 1.5P_0402_50V9C — DDR_A_CLK#1
DDR_B_CLK0 — C14 1.5P_0402_50V9C — DDR_B_CLK#0
DDR_B_CLK1 — C15 1.5P_0402_50V9C — DDR_B_CLK#1

+1.8V — R1 1K_0402_1% — +MCH_REF — R2 1K_0402_1% — C12 0.1U_0402_16V4Z — C13 1000P_0402_25V8J

Place them close to CPU within 1"
MEMZP/N=W/S=5mil/10mil
+1.8V — R4 39.2_0402_1% — MEMZP — R3 39.2_0402_1% — MEMZN — T2 PAD H16

750mA(+-50mV_dc, +-75mV_ac)
VTT_SENSE=W/S=10mil/10mil
VTT_SENSE — PAD T1
PAD T3

JCPUB

+0.9V
MEM:CMD/CTRL/CLK
VTT_SENSE
MEMVREF
RSVD_M1
RSVD_M2
MA0_ODT0, MA0_ODT1, MA1_ODT0, MA1_ODT1
MB0_ODT0, MB0_ODT1, MB1_ODT0
MA0_CS_L0, MA0_CS_L1, MA1_CS_L0, MA1_CS_L1
MB0_CS_L0, MB0_CS_L1, MB1_CS_L0
MA_CKE0, MA_CKE1
MB_CKE0, MB_CKE1
MA_CLK_H5, MA_CLK_L5, MA_CLK_H1, MA_CLK_L1, MA_CLK_H7, MA_CLK_L7, MA_CLK_H4, MA_CLK_L4
MB_CLK_H5, MB_CLK_L5, MB_CLK_H1, MB_CLK_L1, MB_CLK_H7, MB_CLK_L7, MB_CLK_H4, MB_CLK_L4
MA_ADD0 … MA_ADD15
MB_ADD0 … MB_ADD15
MA_BANK0, MA_BANK1, MA_BANK2
MB_BANK0, MB_BANK1, MB_BANK2
MA_RAS_L, MA_CAS_L, MA_WE_L
MB_RAS_L, MB_CAS_L, MB_WE_L

FOX_PZ6382A-284S-41F_GRIFFIN
Athlon 64 S1
Processor
Socket
CONN@

JCPUC

+0.9V
MEM:DATA
MB_DATA0 … MB_DATA63
MA_DATA0 … MA_DATA63
MB_DM0 … MB_DM7
MA_DM0 … MA_DM7
MB_DQS_H0 … MB_DQS_H7
MB_DQS_L0 … MB_DQS_L7
MA_DQS_H0 … MA_DQS_H7
MA_DQS_L0 … MA_DQS_L7

FOX_PZ6382A-284S-41F_GRIFFIN
Athlon 64 S1
Processor Socket
CONN@

<9> DDR_B_D[63..0]
DDR_A_D[63..0] <8>
<9> DDR_B_DM[7..0]
DDR_A_DM[7..0] <8>
<9> DDR_B_DQS0 … DDR_B_DQS7
DDR_A_DQS0 … DDR_A_DQS7 <8>
<8> DDR_A_MA[15..0]
<9> DDR_B_MA[15..0] <9>
<8> DDR_A_BS#0, DDR_A_BS#1, DDR_A_BS#2
<9> DDR_B_BS#0, DDR_B_BS#1, DDR_B_BS#2
<8> DDR_A_RAS#, DDR_A_CAS#, DDR_A_WE#
<9> DDR_B_RAS#, DDR_B_CAS#, DDR_B_WE#
<8> DDR_A_ODT0, DDR_A_ODT1
<9> DDR_B_ODT0, DDR_B_ODT1
<8> DDR_CS0_DIMMA#, DDR_CS1_DIMMA#
<9> DDR_CS0_DIMMB#, DDR_CS1_DIMMB#
<8> DDR_CKE0_DIMMA, DDR_CKE1_DIMMA
<9> DDR_CKE0_DIMMB, DDR_CKE1_DIMMB
<8> DDR_A_CLK0, DDR_A_CLK#0, DDR_A_CLK1, DDR_A_CLK#1
<9> DDR_B_CLK0, DDR_B_CLK#0, DDR_B_CLK1, DDR_B_CLK#1

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Compal Electronics, Inc.

Title: AMD CPU S1G2 DDRII I/F

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250mA(+-100mV_dc, +-150mV_ac)

VDDA=300mA

Place close to CPU wihtin 1.5"

0718 Silego -- 216 ohm

Address:100_1100

CPU_THERMTRIP#_R/ENTRIP2/H_THERMTRIP#=4mil/12mil

+1.8V sense no support

CPU_PROCHOT#_1.8/H_PROCHOT#=4mil/12mil

0718 AMD --> 1K ohm

CPU_VDD0_FB_H/L(Differential pair)=10/5/5/5/10

CPU_VDD1_FB_H/L(Differential pair)=10/5/5/5/10

VDDIO_FB_H/L=10mil/10mil

VDD_NB_FB_H/L(Differential pair)=10/5/5/5/10

Close to CPU

CPU_TEST28_H_PLLCHRZ_P /CPU_TEST28_L_PLLCHRZ_N (85ohm Differential pair)

route as differential as short as possible testpoint under package

CPU_TEST29_H_FBCLKOUT_P /CPU_TEST29_L_FBCLKOUT_N (85ohm Differential pair)

LDT_RST#=4mil/12mil

H_PWRGD_CPU=4mil/12mil

LDT_STOP#=4mil/12mil

0718 AMD , need check with AMD

CPU_LDT_REQ#=4mil/12mil

2.09V for Gate

FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V

EC is PU to 5VALW

2200p change to 1000p for ADT7421

Address:100_1101

HDT Connector

NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

9/20 SP020016900

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Compal Electronics, Inc.

Title: AMD CPU S1G2 CTRL

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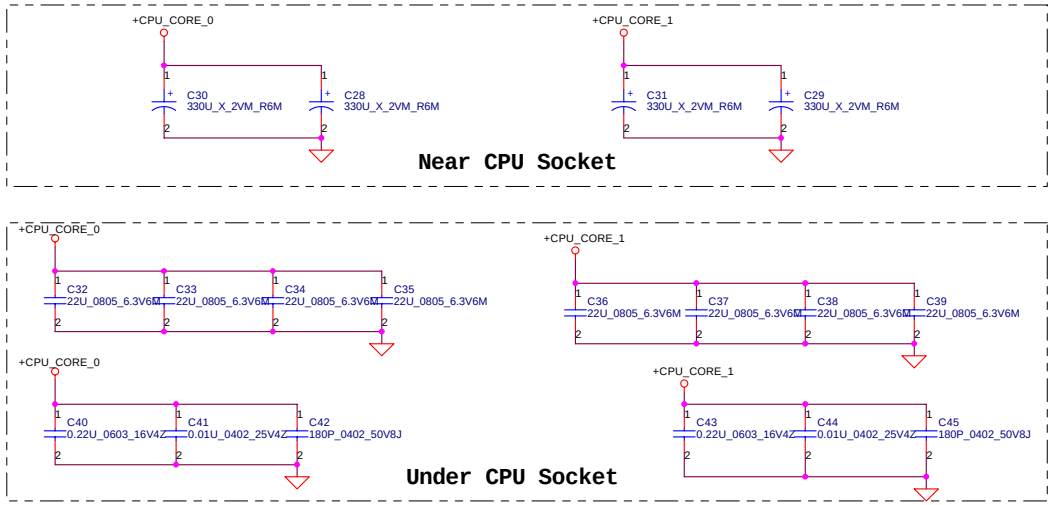
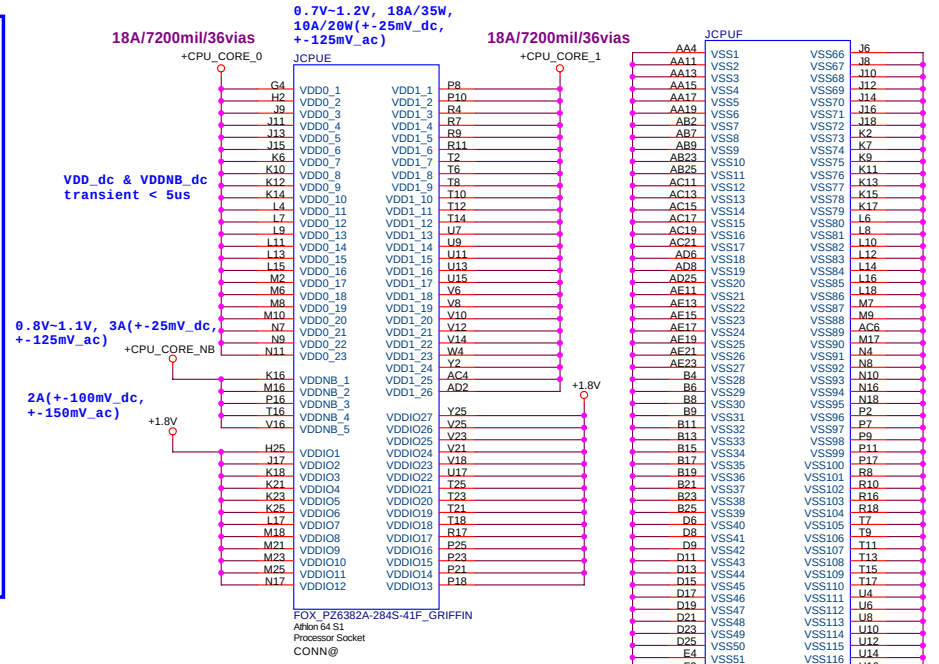
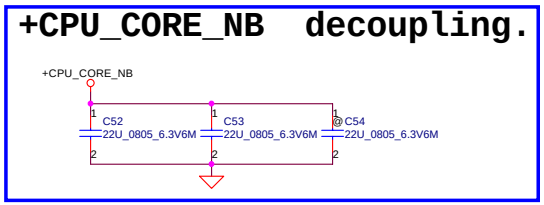
VDD(+CPU_CORE) decoupling.

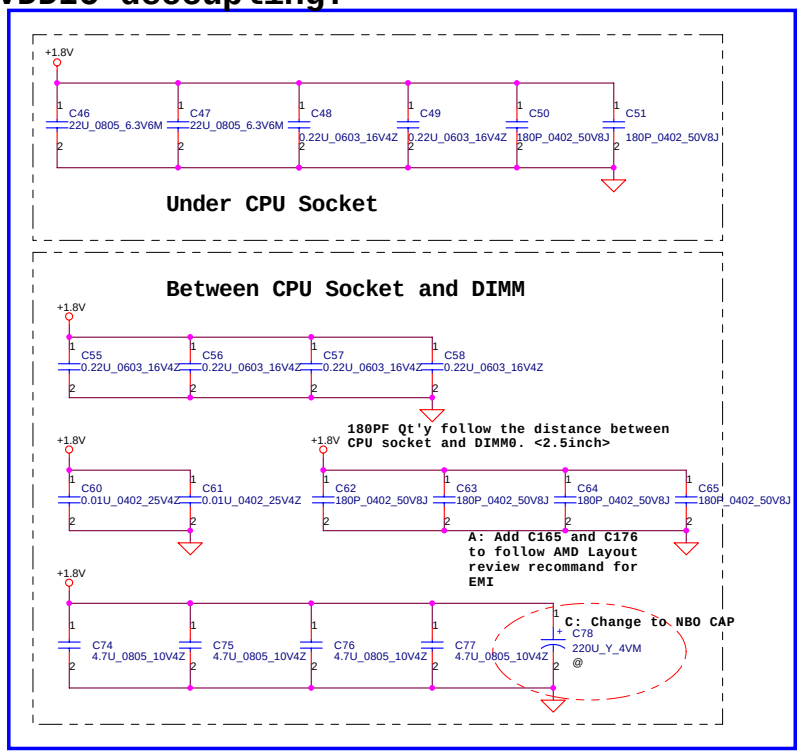




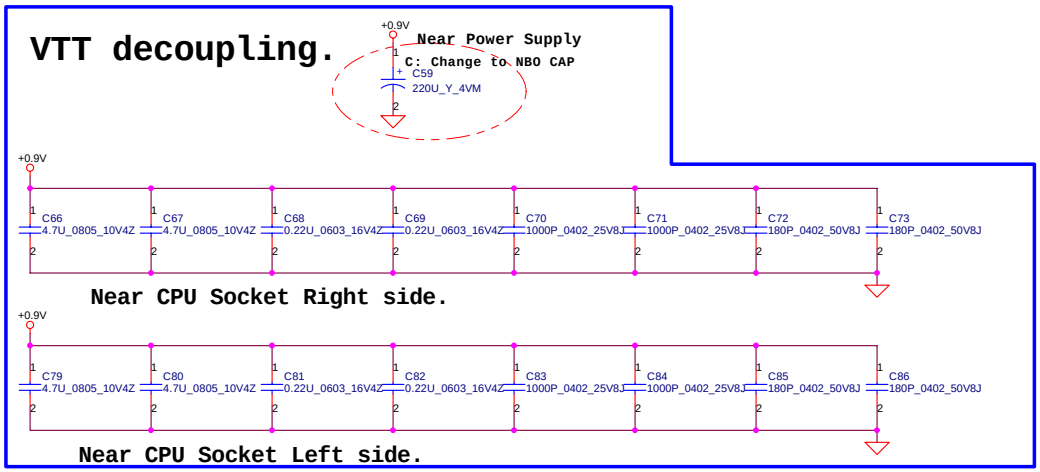
+CPU_CORE_NB decoupling.



VDDIO decoupling.



VTT decoupling.



Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: AMD CPU S1G2 PWR & GND

Size: Custom | Document Number: LA-4114P | Rev: 0.1

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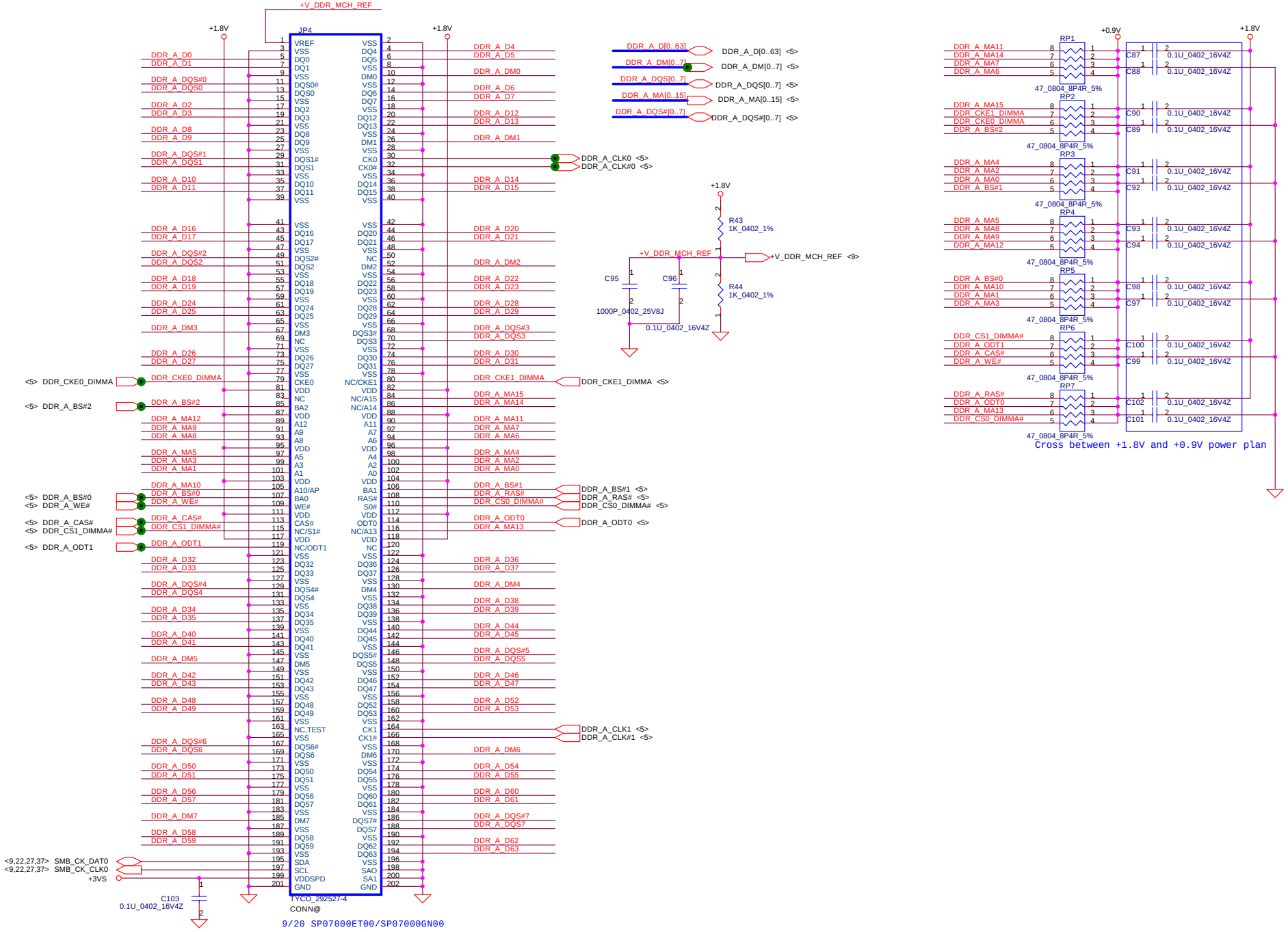

Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **DDRII SO-DIMM 0**

Size	Document Number	Rev
Custom	LA-4114P	0.1

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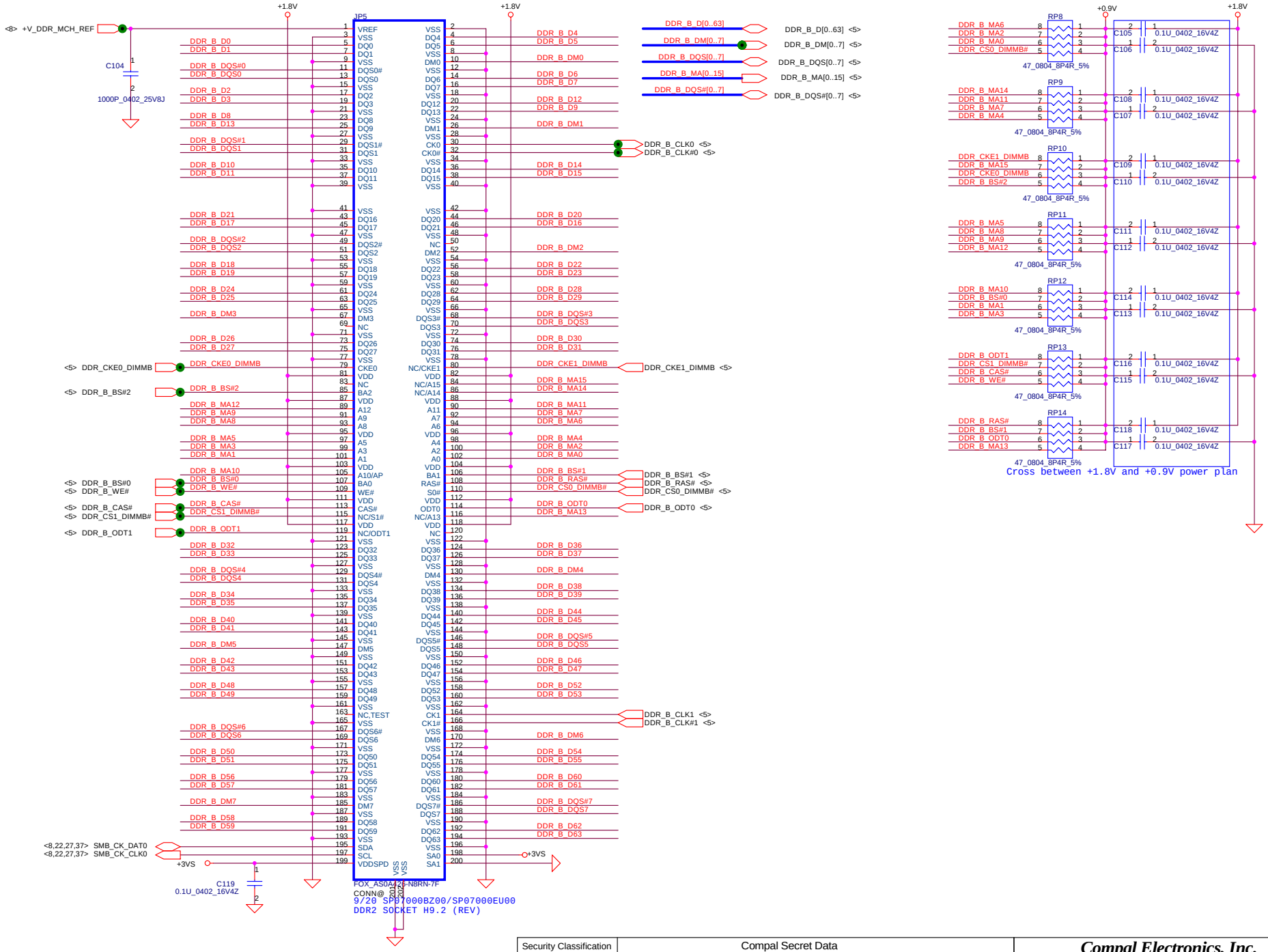

Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **DDRII SO-DIMM 1**

Size	Document Number	Rev
Custom	LA-4114P	0.1

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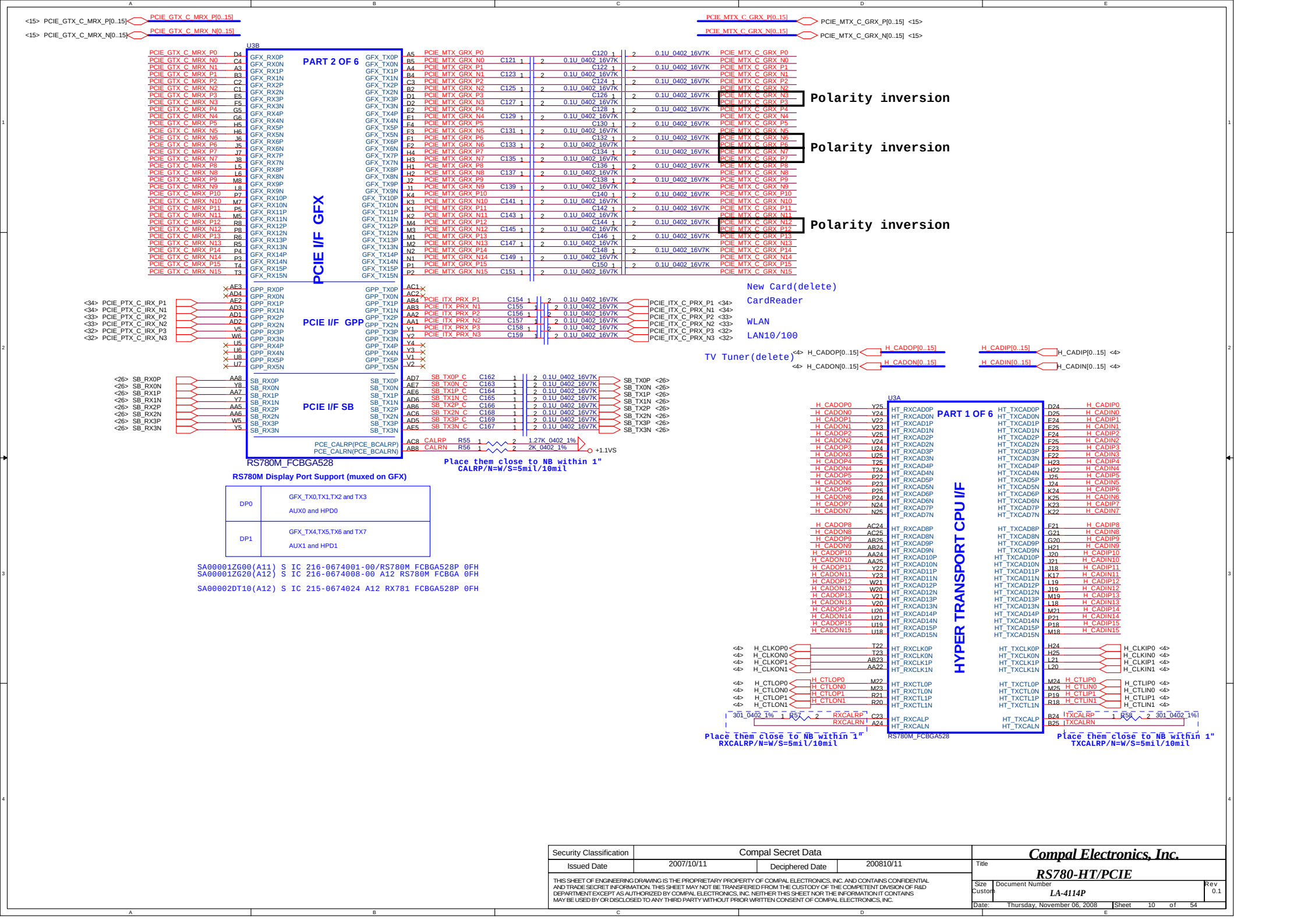

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

SA00001ZG00(A11) S IC 216-0674001-00/RS780M FCBGA528P 0FH
SA00001ZG20(A12) S IC 216-0674008-00 A12 RS780M FCBGA 0FH

SA00002DT10(A12) S IC 215-0674024 A12 RX781 FCBGA528P 0FH

Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **RS780-HT/PCIE**

Size	Document Number	Rev
Custom	LA-4114P	0.1

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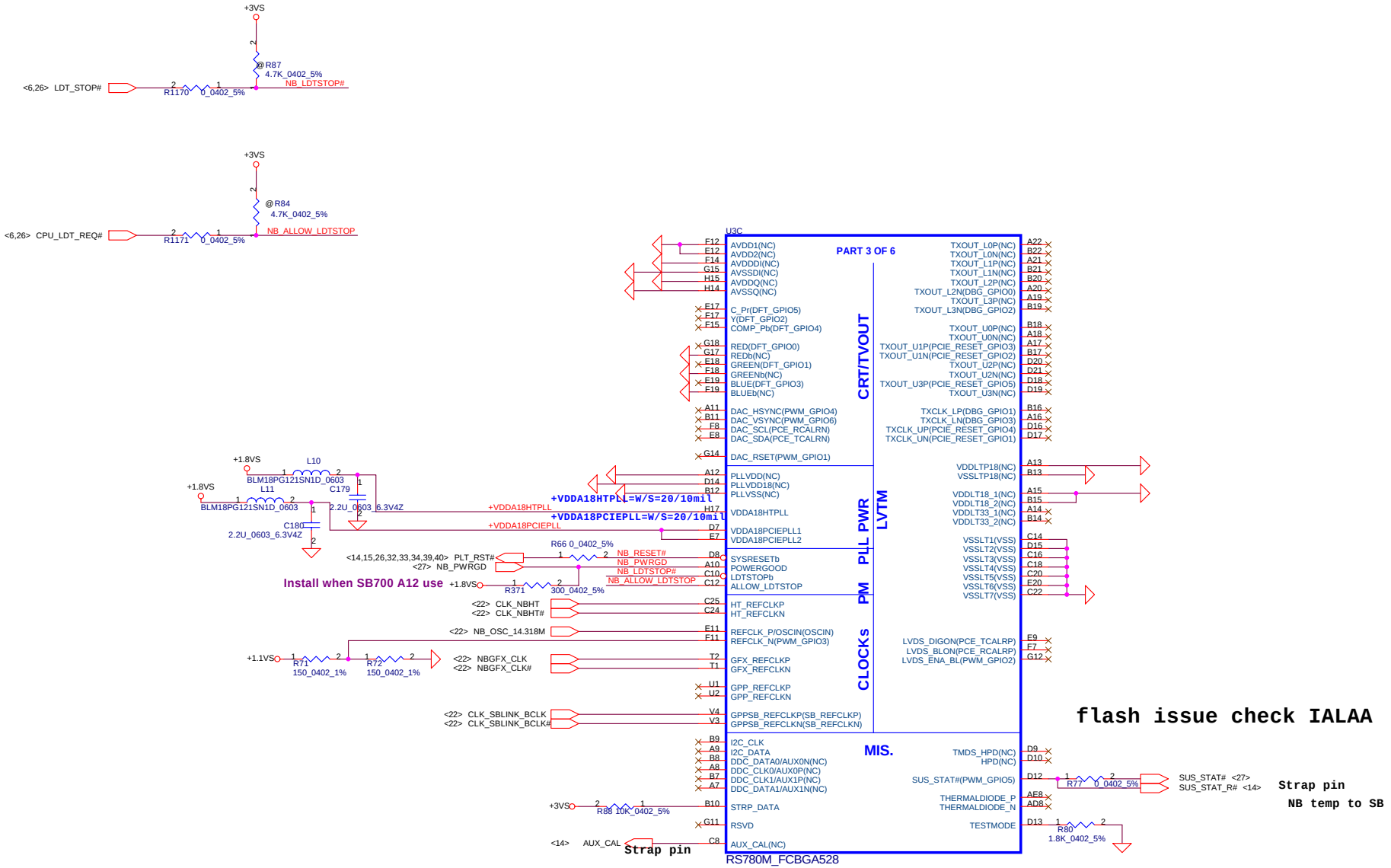

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title	RS780 VEDIO/CLK GEN		
Size: Custom	Document Number: LA-4114P		Rev: 0.1
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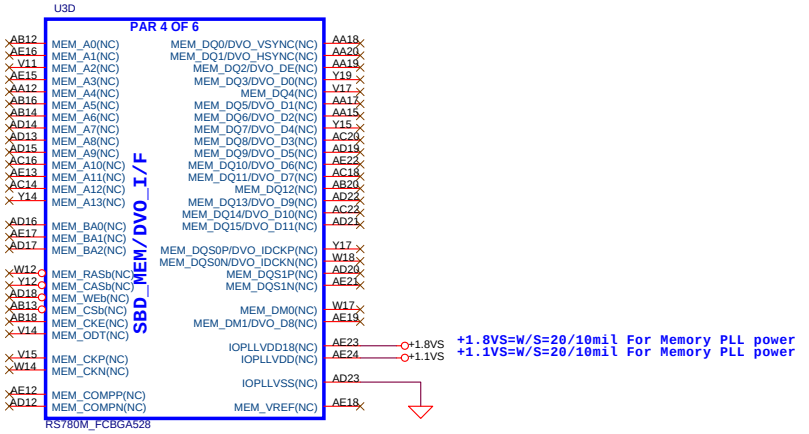

Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **RS780 Side-Port DDR2 SDRAM**

Size	Document Number	Rev
Custom	LA-4114P	0.1

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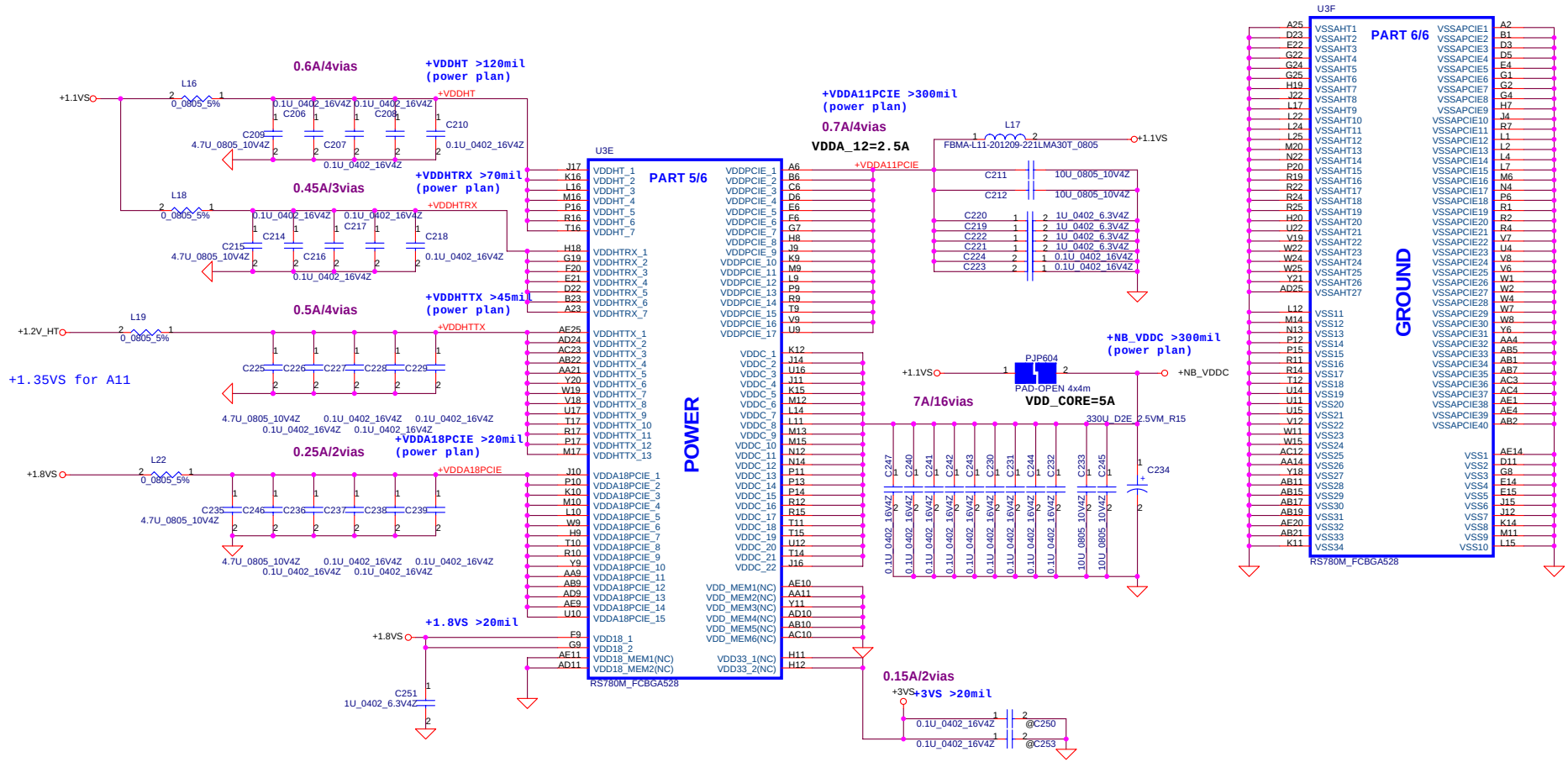

Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **RS780 PWR/GND**

Size	Document Number	Rev
Custom	LA-4114P	0.1

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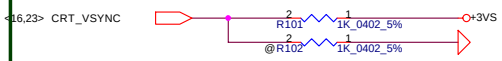
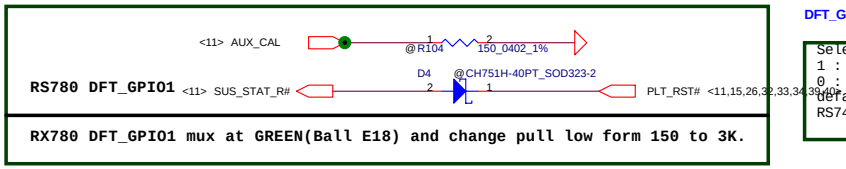
RS780 DFT_GPIO5 mux at CRT_VSYNC pull low to 1K



DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

```
Enables the Test Debug Bus using GPIO.
1 : Disable (RS740)  Enable (RX780, RS780)
0 : Enable (Rs740)   Disable (RX780, RS780)
PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#
```



RX780 DFT_GPIO1 mux at GREEN(Ball E18) and change pull low form 150 to 3K.

DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740/RX780: DFT_GPIO1  RS780:SUS_STAT
```

RS780 use HSYNC to enable SIDE PORT (internal pull high)

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

```
RX780: Enables the Test Debug Bus using PCIE bus
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable

RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)
1.  Disable (RS740/RS780)
0 : Enable (RS740/RS780)
```

Security Classification	Compal Secret Data		
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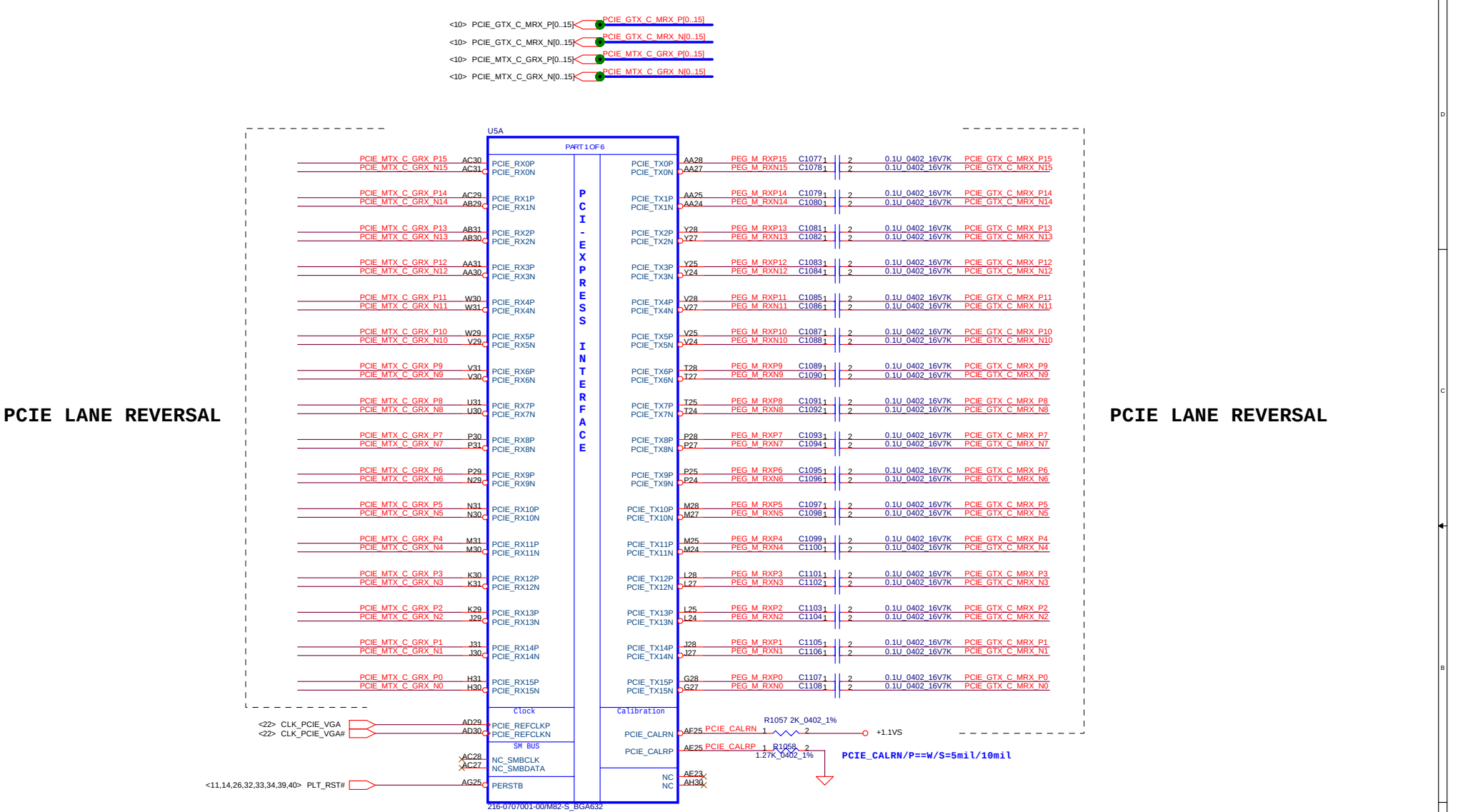
Compal Electronics, Inc.		
Title: RS780 STRAPS		
Size: Custom	Document Number: LA-4114P	Rev: 0.1
Date: Thursday, November 06, 2008	Sheet 14 of 54	



Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.		
Title: M82-S PCIE interface		
Size	Document Number: LA-4114P	Rev: 0.1
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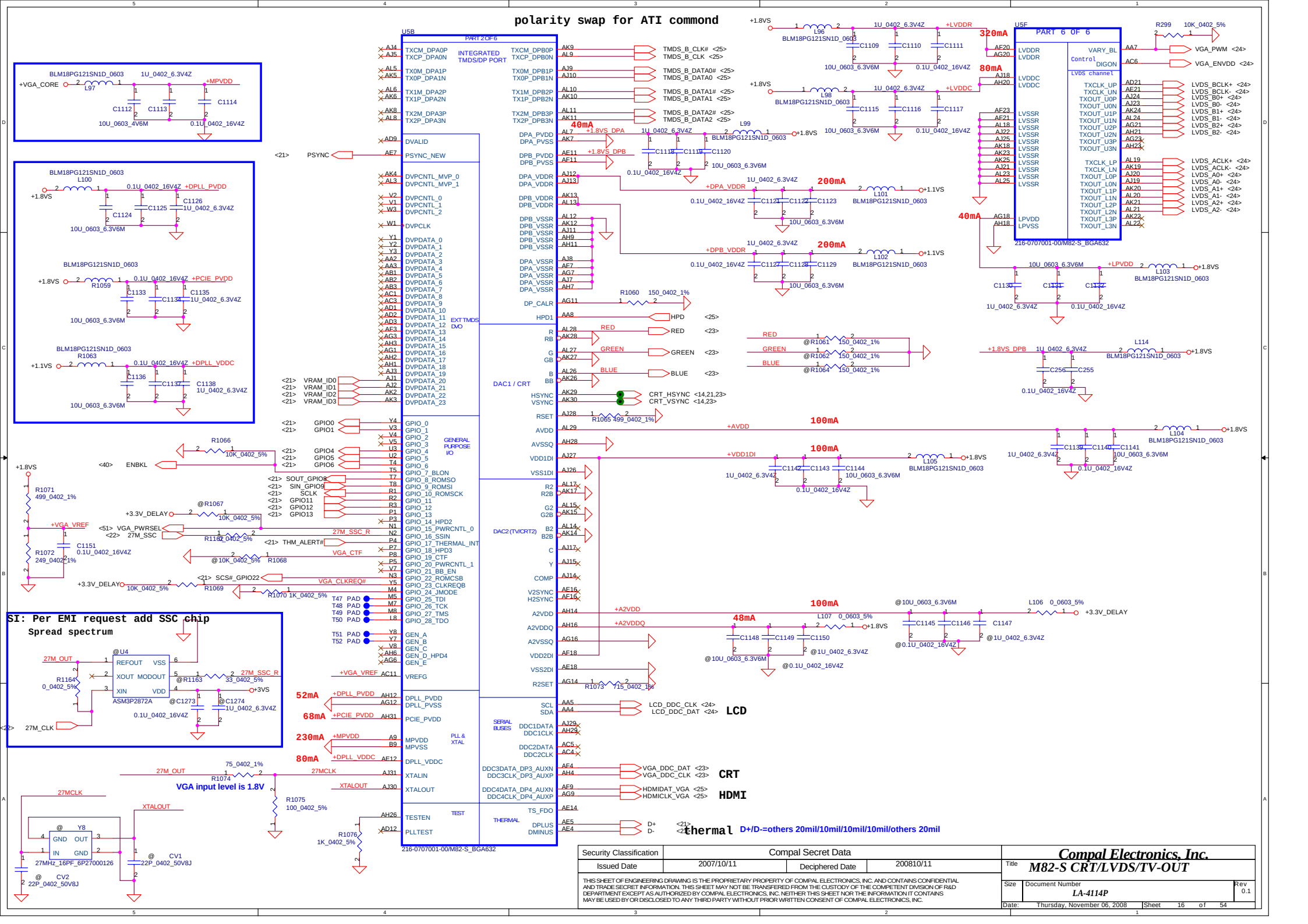
polarity swap for ATI commond



Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: *M82-S CRT/LVDS/TV-OUT*

Size	Document Number	Rev
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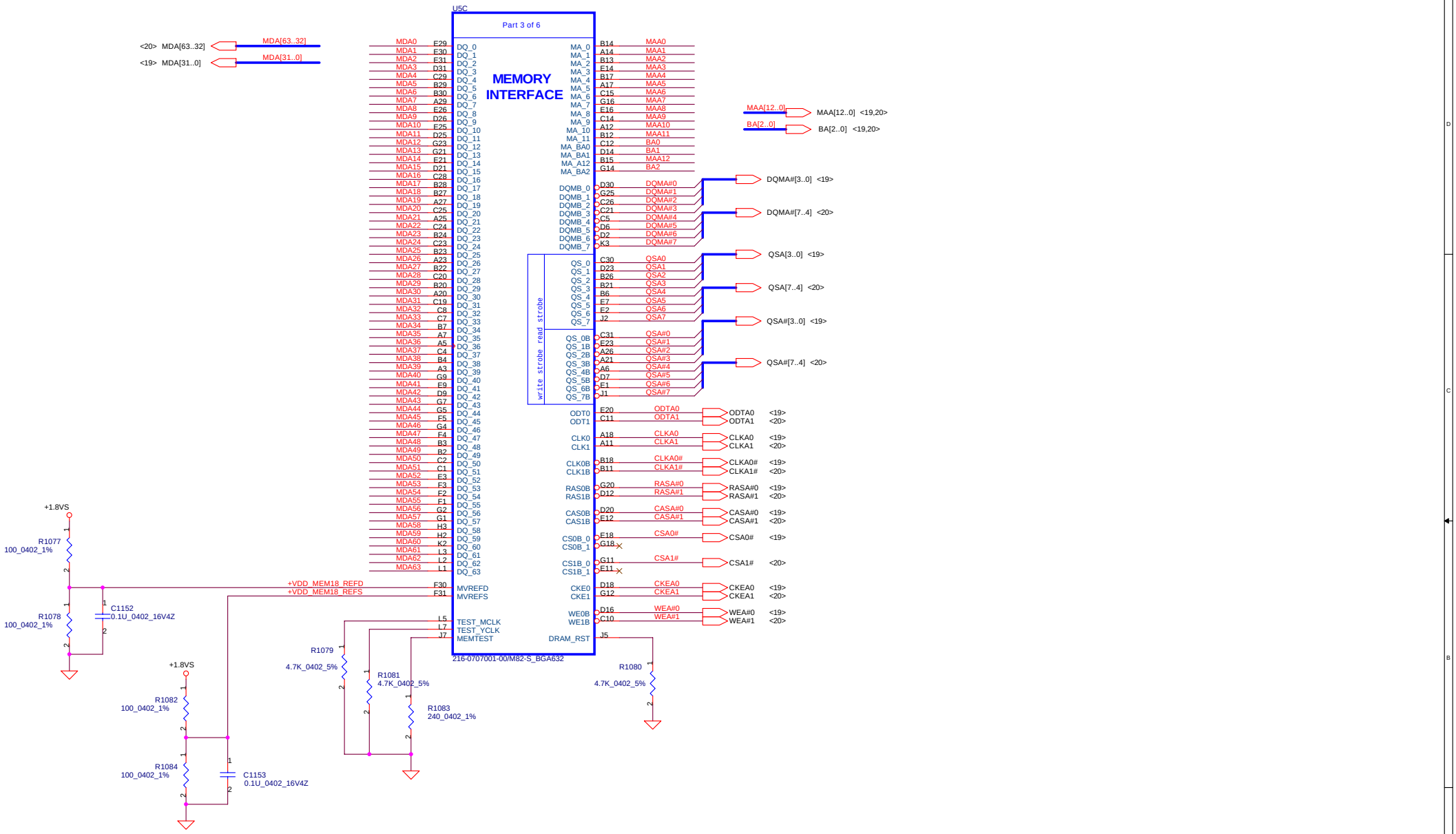

Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **M82-S MEM**

Size	Document Number	Rev
	LA-4114P	0.1

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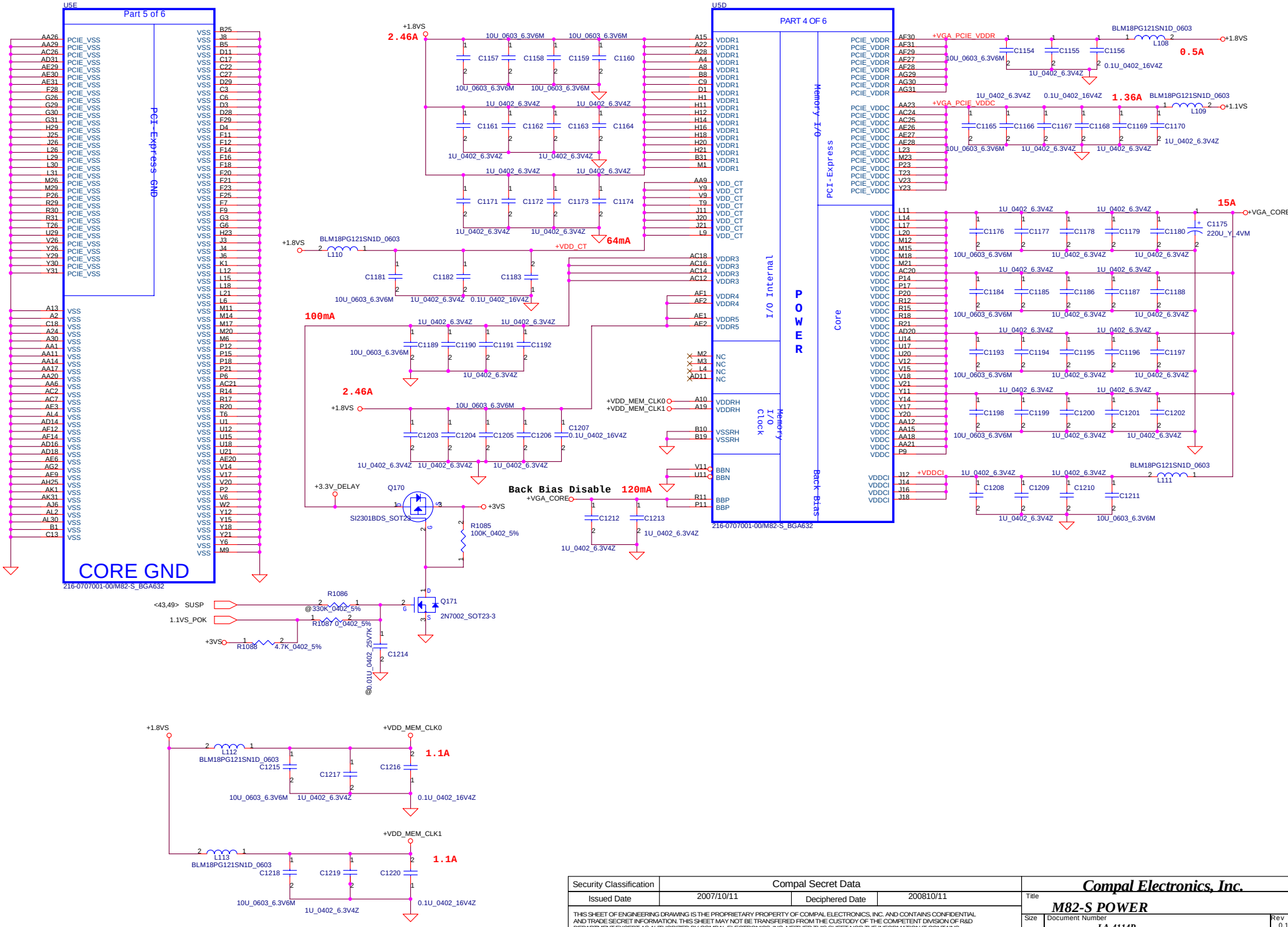

Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **M82-S POWER**

Size	Document Number	Rev
	LA-4114P	0.1

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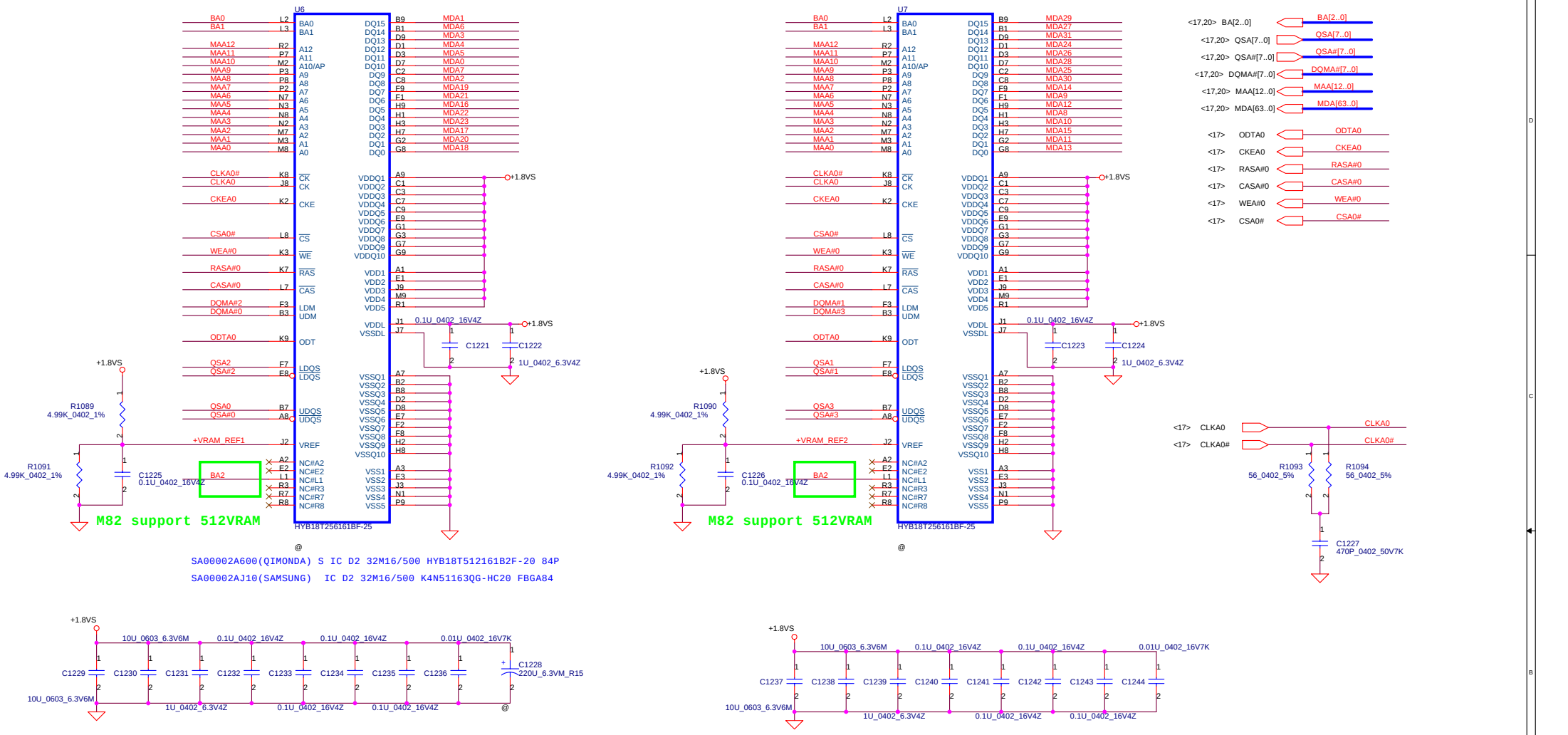

SA00002A600(QIMONDA) S IC D2 32M16/500 HYB18T512161B2F-20 84P

SA00002AJ10(SAMSUNG) IC D2 32M16/500 K4N51163QG-HC20 FBGA84

Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **M82-S VRAM**

Size	Document Number	Rev
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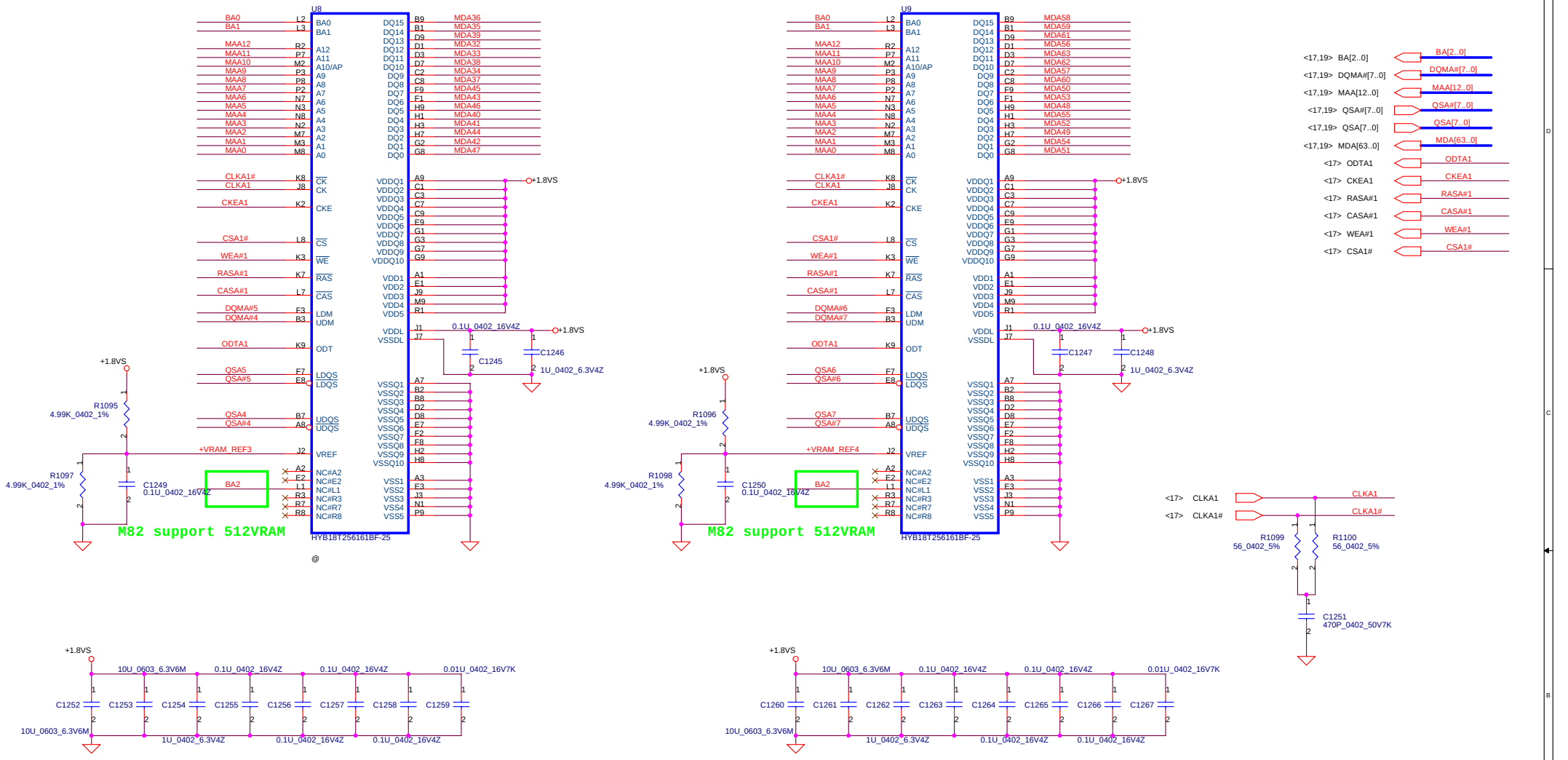


@

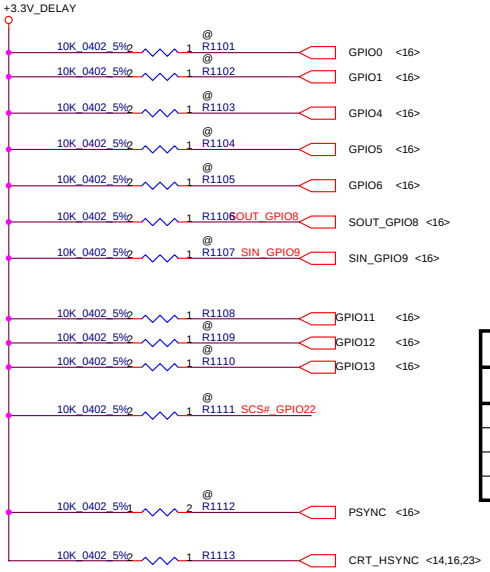
Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

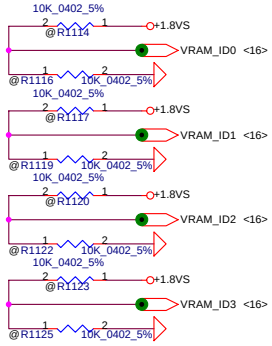
Compal Electronics, Inc.

Title: **M82-S VRAM**

Size	Document Number	Rev
	LA-4114P	0.1

Date: Thursday, November 06, 2008 Sheet 20 of 54





ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE

GPIO2 GPIO3 GPIO5 GPIO6 DVALID H2SYNC V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GENERICC GPIO21_BB_EN GPIO_28_TDO

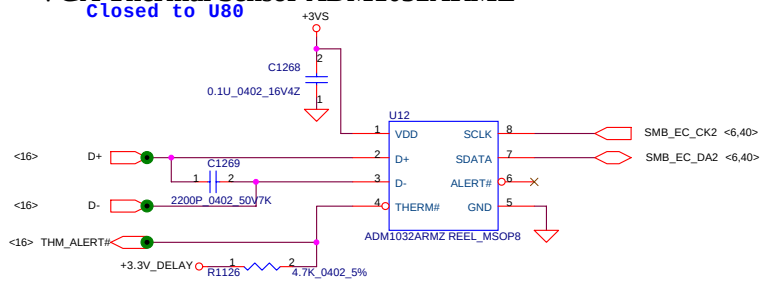
GPIO9 = 0 (BIOS_ROM_EN = 0)	
GPIO[13:11]	**MEMORY SIZE**
0 0 0	128MB
0 0 1	256MB
0 1 0	64MB
1 0 0	512MB

STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED M8X
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLES	0
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0
BIF_GEN2_EN_A	GPIO5	PCI-E 5.0GT/s or 2.5 GT/s select	0
DEBUG_I2C_ENABLE	GPIO6	Internal use only	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO(M8X)	1
ROMIDCFG[3:0]	GPIO [9,13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 1 0 1
BIOS_ROM EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	0
BIF_VGA_DIS	PSYNC	VGA ENABLED===0 is enable	0
BIF_HDMI_EN	HSYNC	HDMI ENABLE	1

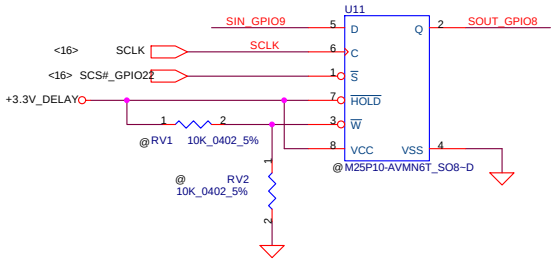
STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3,2,1,0
VRAM_ID[3:0]	DVPDATA (23,22,21,20)	M82M-XT	Rachman 1.2	512M(x4)	Samsung 64Mx16 1.8V	SA00002MD00	0 0 0 0
			Rachman 1.2	256M(X4)	Samsung 32Mx16 1.8V	SA00002AJ10	0 0 0 1
				512M(x4)	Hynix 64Mx16 1.8V		0 0 1 0
			Rachman 1.1	256M(X4)	Hynix 32Mx16 1.8V	SA00002DL00	0 0 1 1
			Rachman 1.1	256M(X4)	Qimonda 32Mx16 1.8V	SA00002A600	0 1 0 0
			Rachman 1.2	512M(x4)	Qimonda 64Mx16 1.8V	SA00002MF00	0 1 0 1

VGA Thermal Sensor ADM1032ARMZ

Closed to U80



FLASH ROM



Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **M82-S Filters / Strap**

Size	Document Number	Rev
	LA-4114P	0.1

Date: Friday, November 07, 2008 Sheet 21 of 54

+1.2V_HT >150mil

+VDDCLK_IO >15mil

+3VS >150mil

+3VS_CLK >15mil

EMI Caps for single end clock.

CLK_XTAL_IN/OUT=width /spacing/Others=10mil/10mil/20mil

	OSC_14M_NB
RS780	1.1V 158R/90.0R

NB

CPU

SB LINK

SB SRC

MiniCard_1(delete)

MiniCard_2

For ICS need to pull high.
For SLG is NC

CLKREQ_NCARD# , CLKREQ_LAN# , CLKREQ4 , CLKREQ_MCARD2#=width /spacing/Others=8mil/8mil/12mil

SLG8SP626VTR_QFN72_10x10

SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN(XA)
SA000025B10 S IC RTM880N-795-VB-GRT QFN 72P CLK GEN
SA00001ZV10 S IC ICS9LPRS476BKLFT MLF 72P CLK GEN

NB GFX

VGA chip(Dis)

Card Reader

LAN

New Card(delete)

SEL_SATA		
	1	configure as SATA output
	*	
	0	configure as normal SRC(SRC_6) output

* default

27M_SEL		
	1 *	configure as 27M and 27M_SS output
	0	configure as SRC_7 output

* default

Use voltage divider resistor R379 & R380 to pull low

NB_OSC_14.318M		
	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output

* default

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*

Security Classification	Compal Secret Data	
Issued Date	2007/10/11	Deciphered Date 200810/11

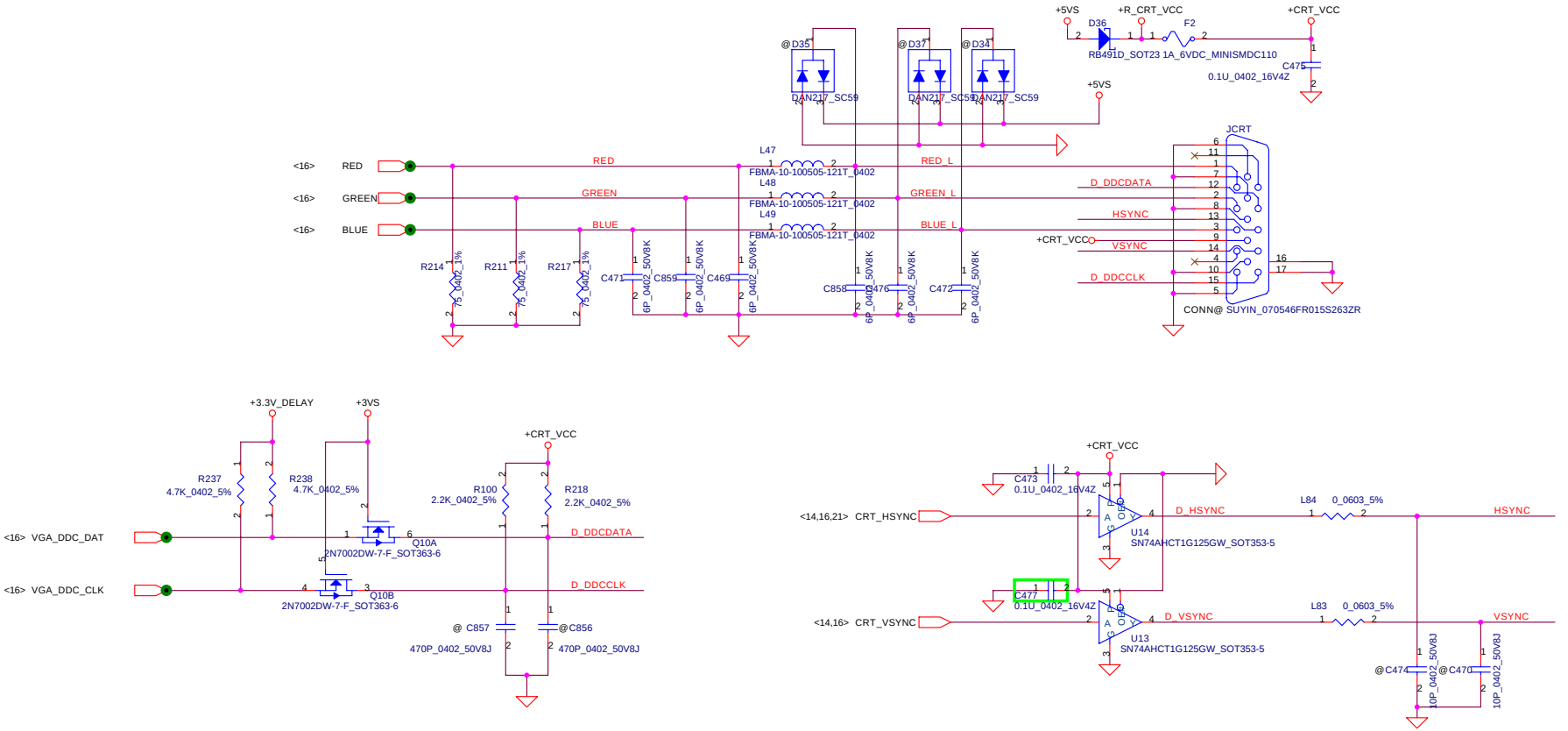
Compal Electronics, Inc.

Title: Clock generator

Size: Custom | Document Number: LA-4114P | Rev: 0.1

Date: Thursday, November 06, 2008 | Sheet 22 of 54

CRT CONNECTOR



Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

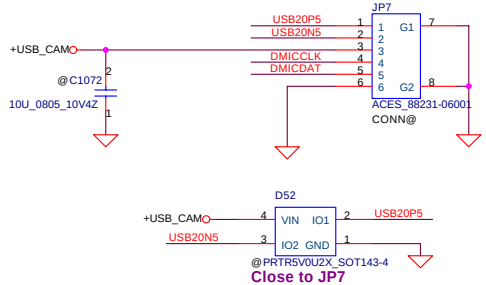
Compal Electronics, Inc.

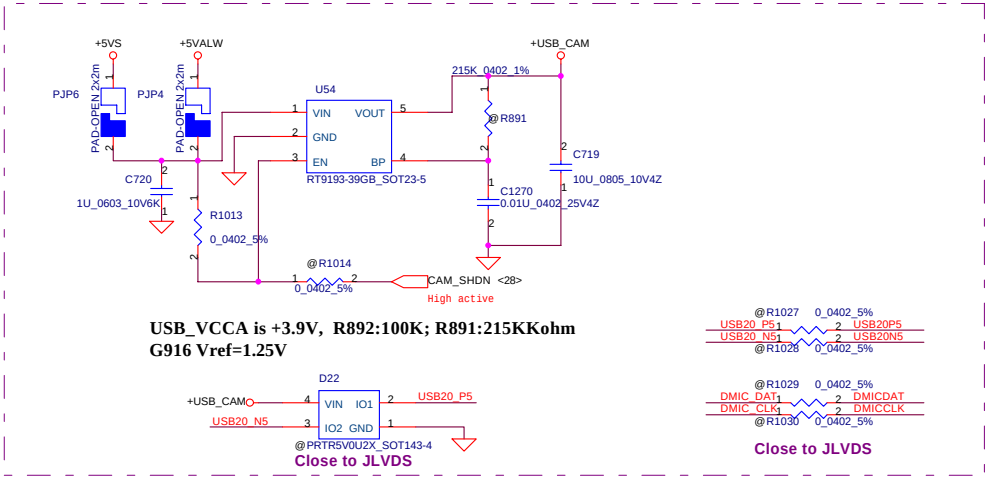
Title: **CRT Connector**

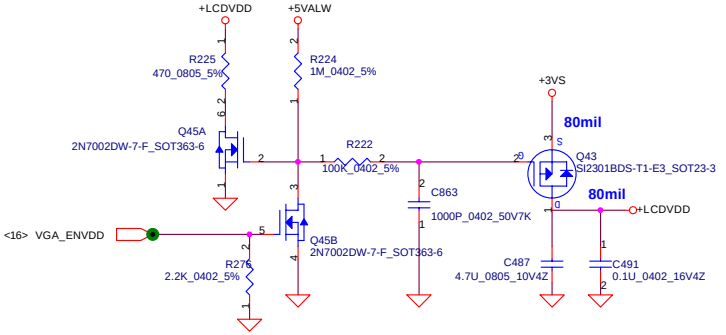
Size	Document Number	Rev
Custom	LA-4114P	0.1

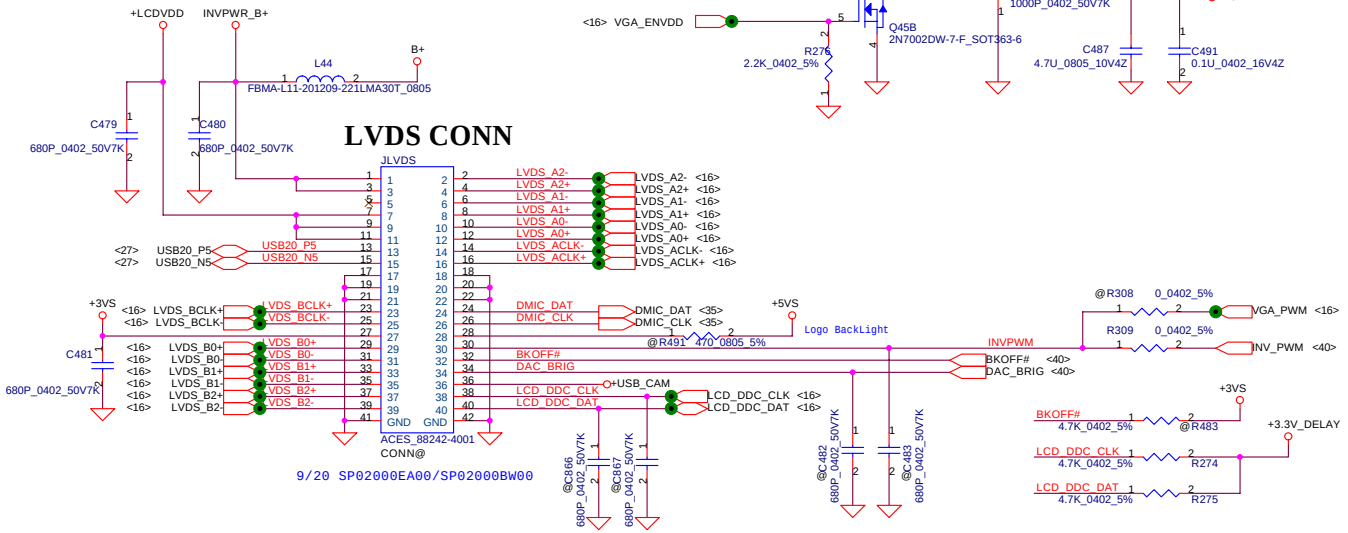
Date: Thursday, November 06, 2008 | Sheet 23 of 54

WebCam+Digital Mic









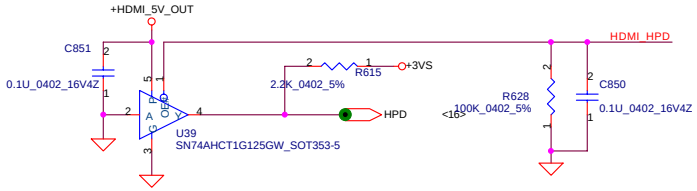
Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

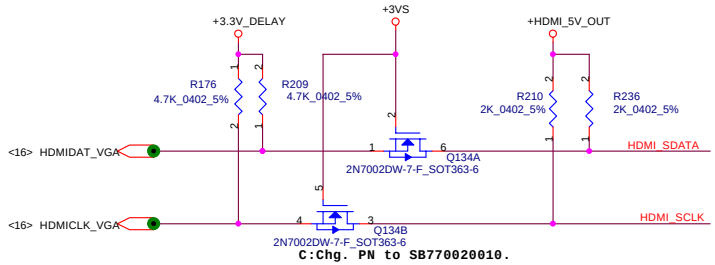
Compal Electronics, Inc.

Title: **LCD CONN. / WebCam**

Size	Document Number	Rev
Custom	LA-4114P	0.1

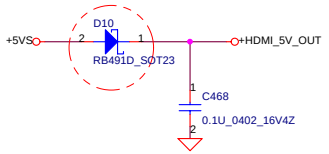
Date: Thursday, November 06, 2008 Sheet 24 of 54

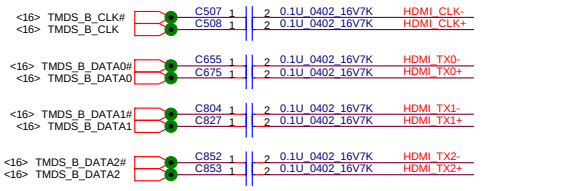


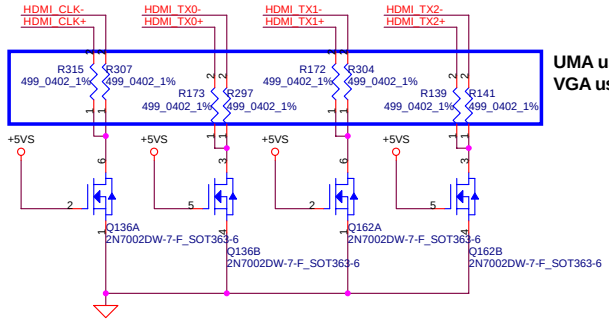


C:Chg. PN to SB770020010.

MP:Update D10 to meet HDMI.

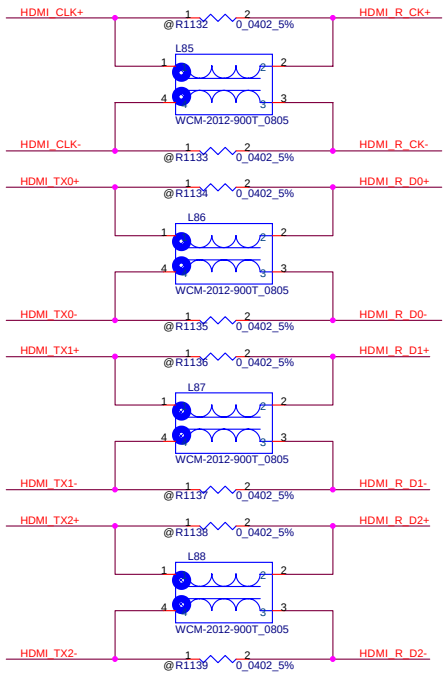




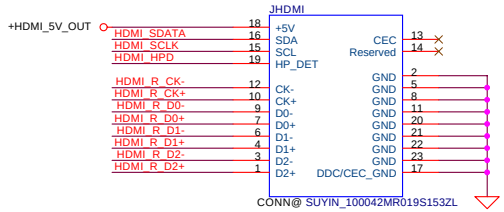


UMA use 750 ohm
VGA use 499 ohm

COMMON MODE CHOCK is SM070000K00 KING_WCM-2012-900T_4P



HDMI Connector



9/20 DC020709040

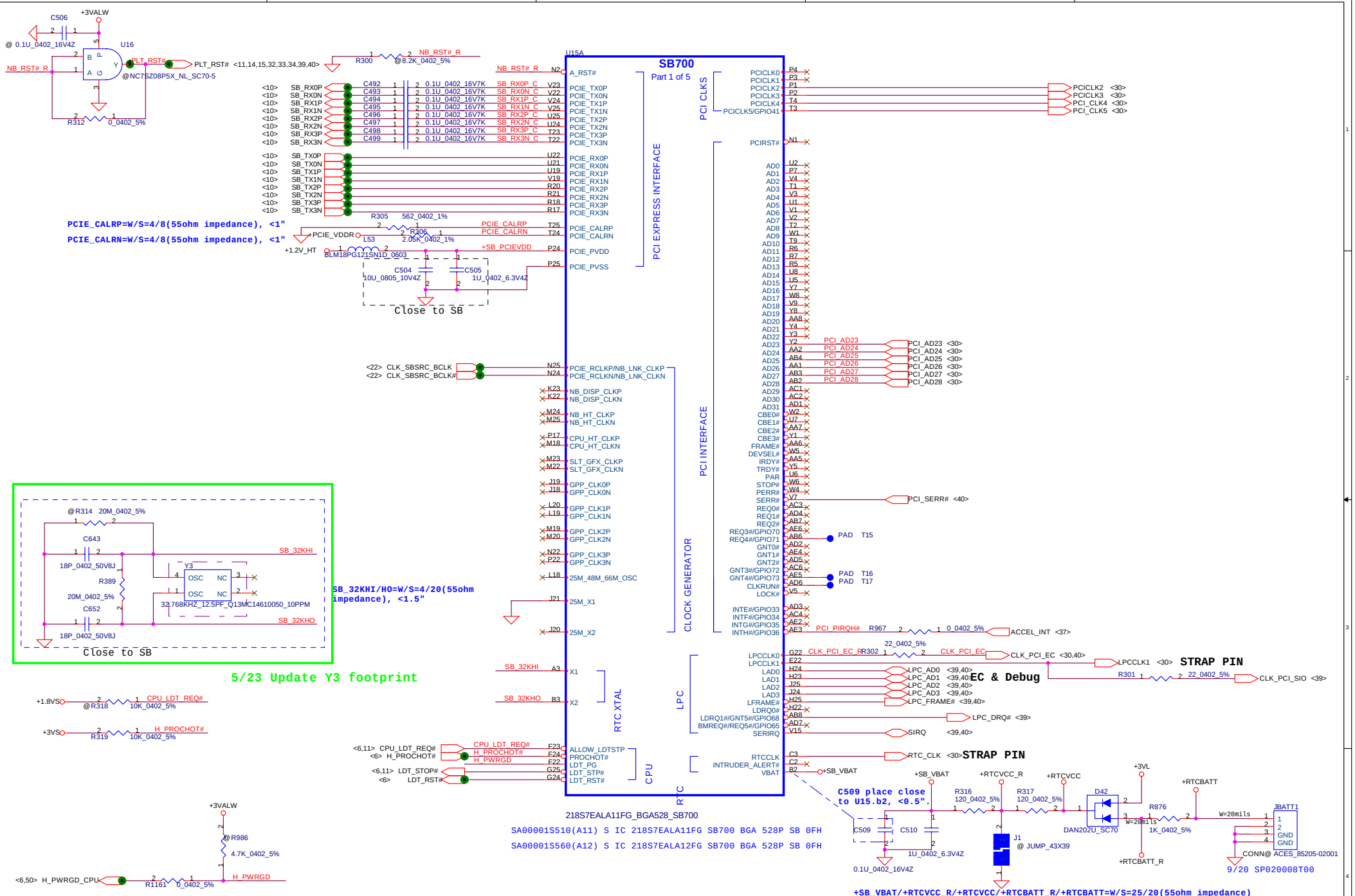
Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **HDMI**

Size	Document Number	Rev
Custom	LA-4114P	0.1

Date: Thursday, November 06, 2008 | Sheet 25 of 54



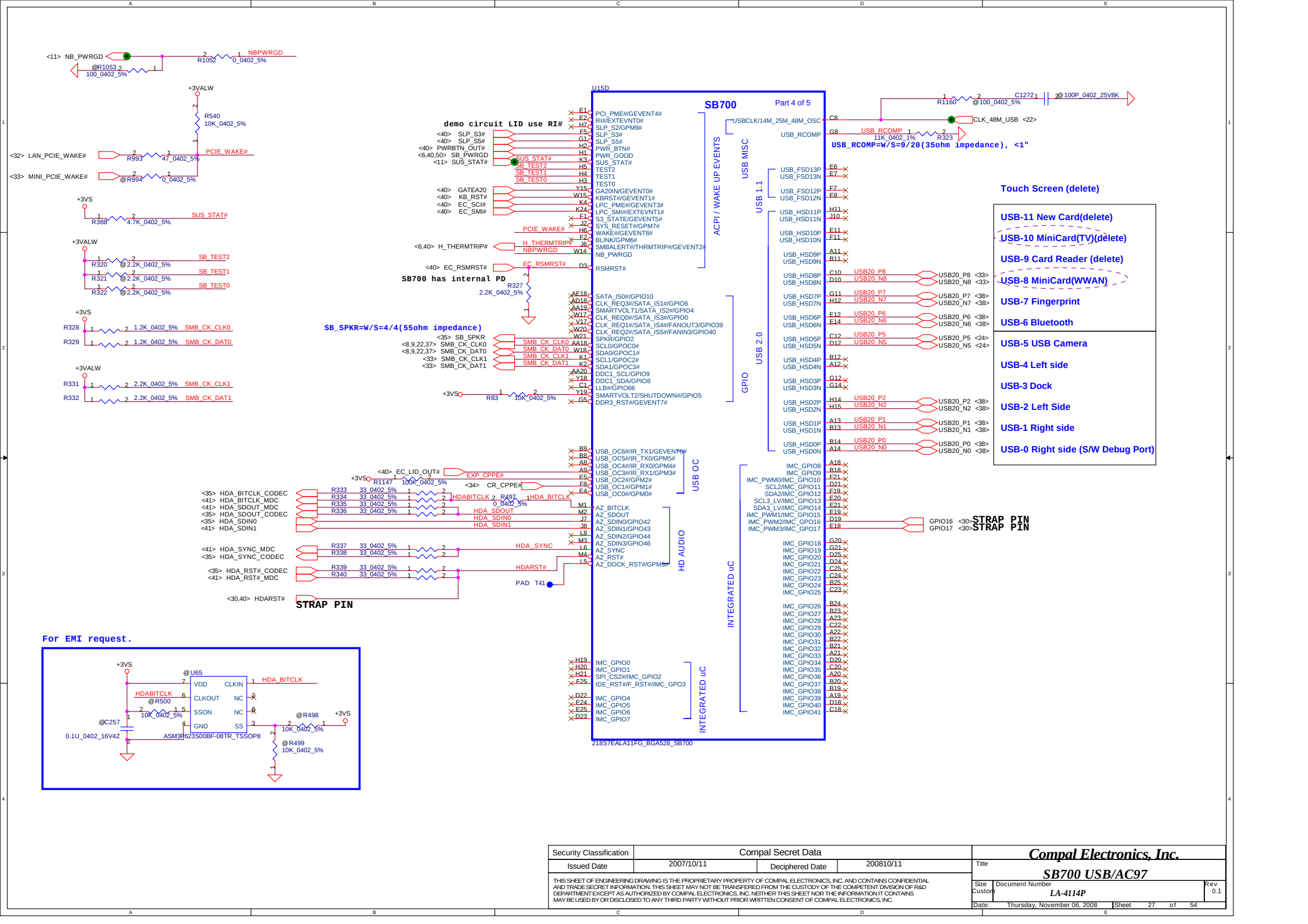
Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: SB700-PCIE/PCI/ACPI/LPC/RTC

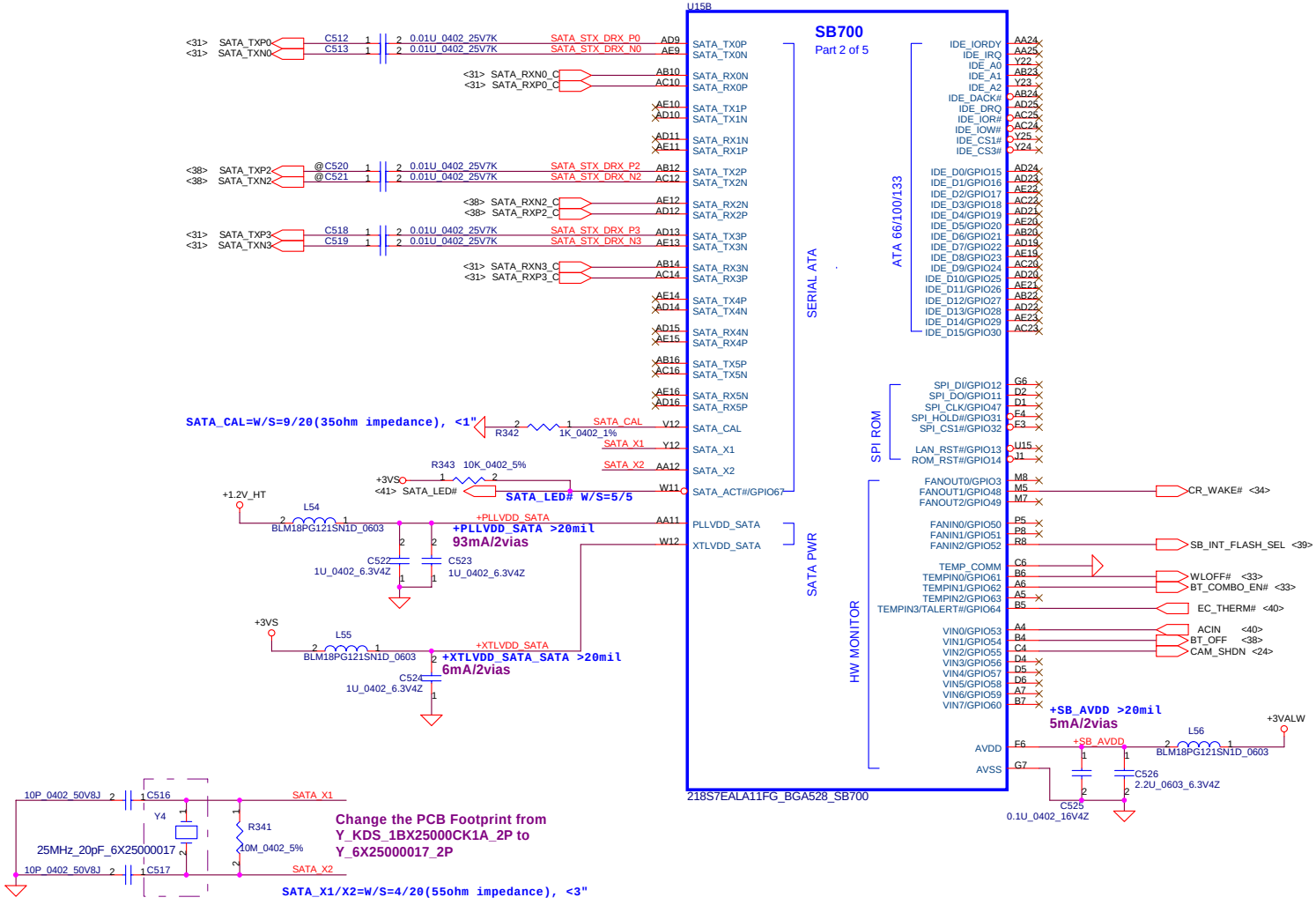
Size	Document Number	Rev
Custom	LA-4114P	0.1

Date: Monday, November 10, 2008 Sheet 26 of 54



Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.	
Title	SB700 USB/AC97
Size: Custom	Document Number: LA-4114P
Rev	0.1
Date: Thursday, November 06, 2008	Sheet 27 of 54



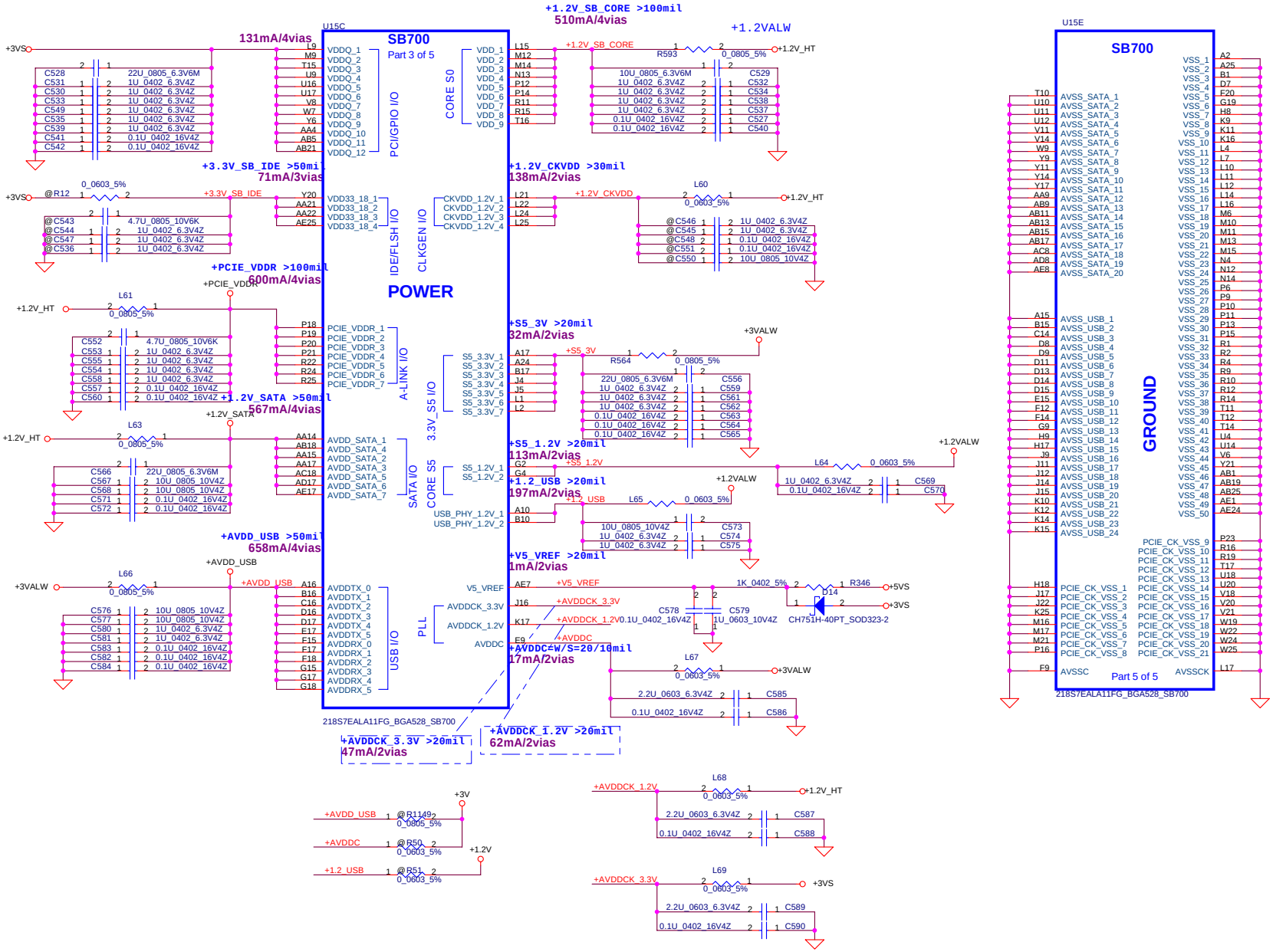
Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **SB700 SATA/IDE/SPI**

Size	Document Number	Rev
Custom	LA-4114P	0.1

Date: Thursday, November 06, 2008 | Sheet 28 of 54



Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **SB700 PWR/GND**

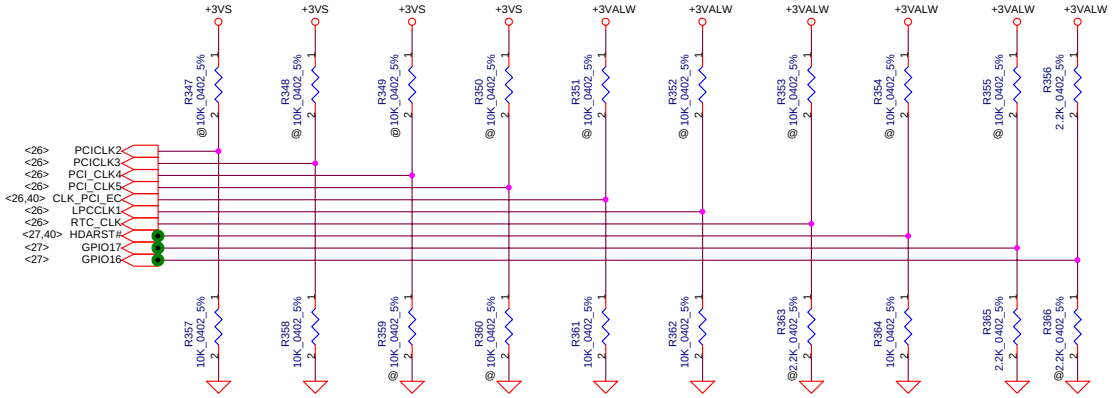
Size	Document Number	Rev
Custom	LA-4114P	0.1

Date: Thursday, November 06, 2008 | Sheet 29 of 54

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

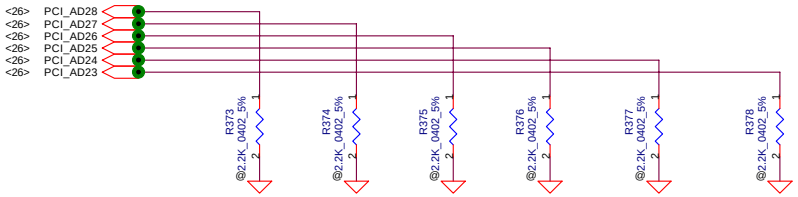
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	AZ_RST_CD#	LPC_CLK1	RTC_CLK	LPC_CLK0	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM



DEBUG STRAPS

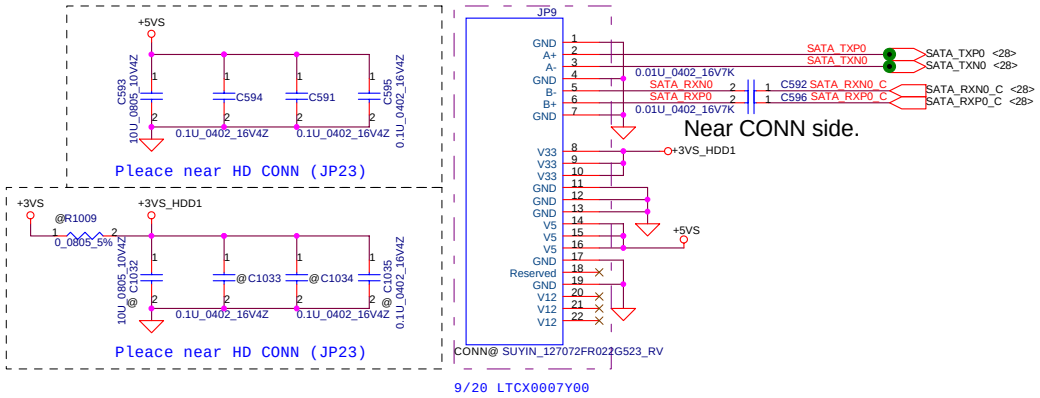
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



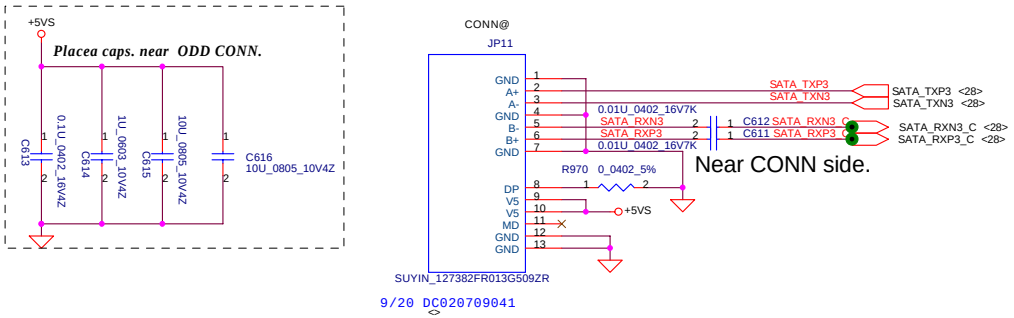
Compal Electronics, Inc.	
Title	SB700 STRAPS
Size: Custom	Document Number: LA-4114P
Rev	0.1
Date: Thursday, November 06, 2008	Sheet 30 of 54

HDD Connector



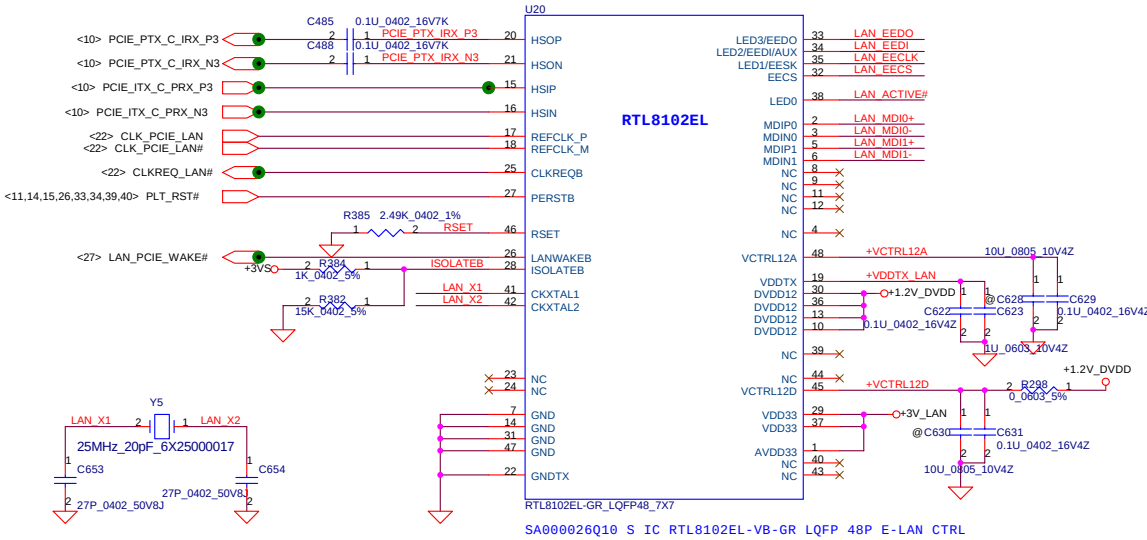
Multi-Bay Connector-option(deltet)

CD-ROM Connector

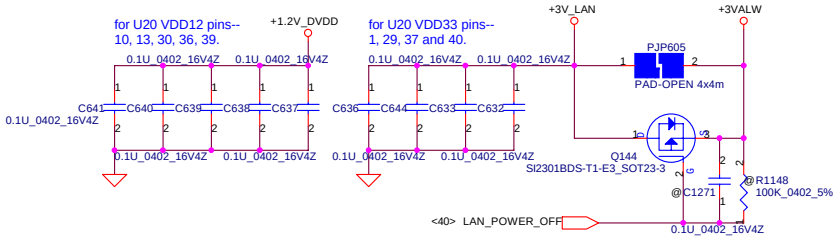


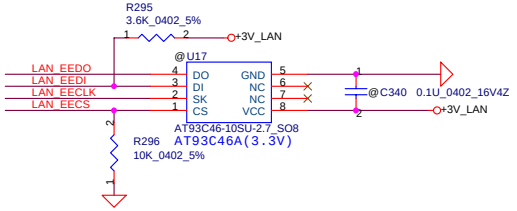
Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

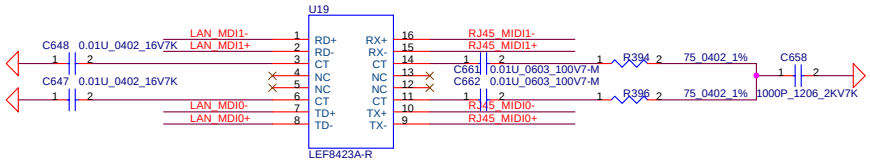
Compal Electronics, Inc.			
Title	HDD/CDROM		
Size: Custom	Document Number: LA-4114P		Rev: 0.1
Date: Thursday, November 06, 2008	Sheet 31 of 54		

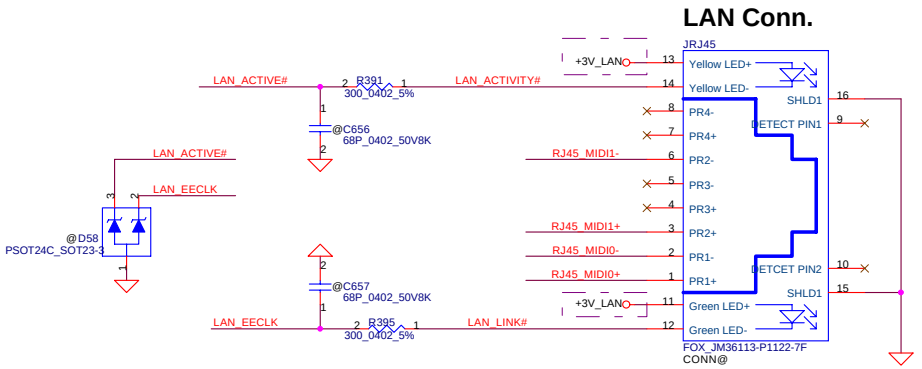


SA000026Q10 S IC RTL8102EL-VB-GR LQFP 48P E-LAN CTRL









Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

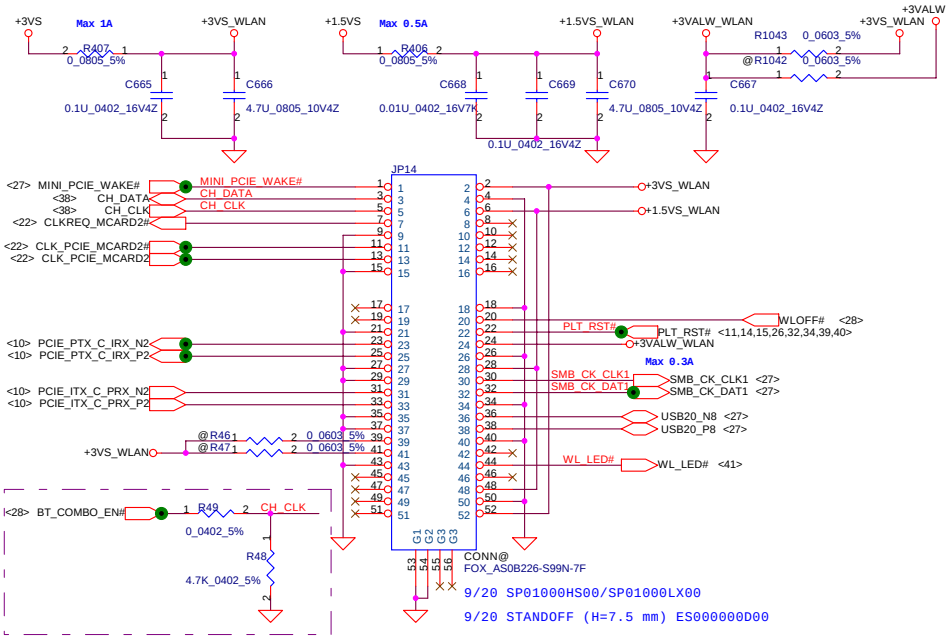
Compal Electronics, Inc.

Title: **RealTek_8102EL_10/100**

Size	Document Number	Rev
Custom	LA-4114P	0.1

Date: Thursday, November 06, 2008 | Sheet 32 of 54

Mini Card Slot 1---WLAN



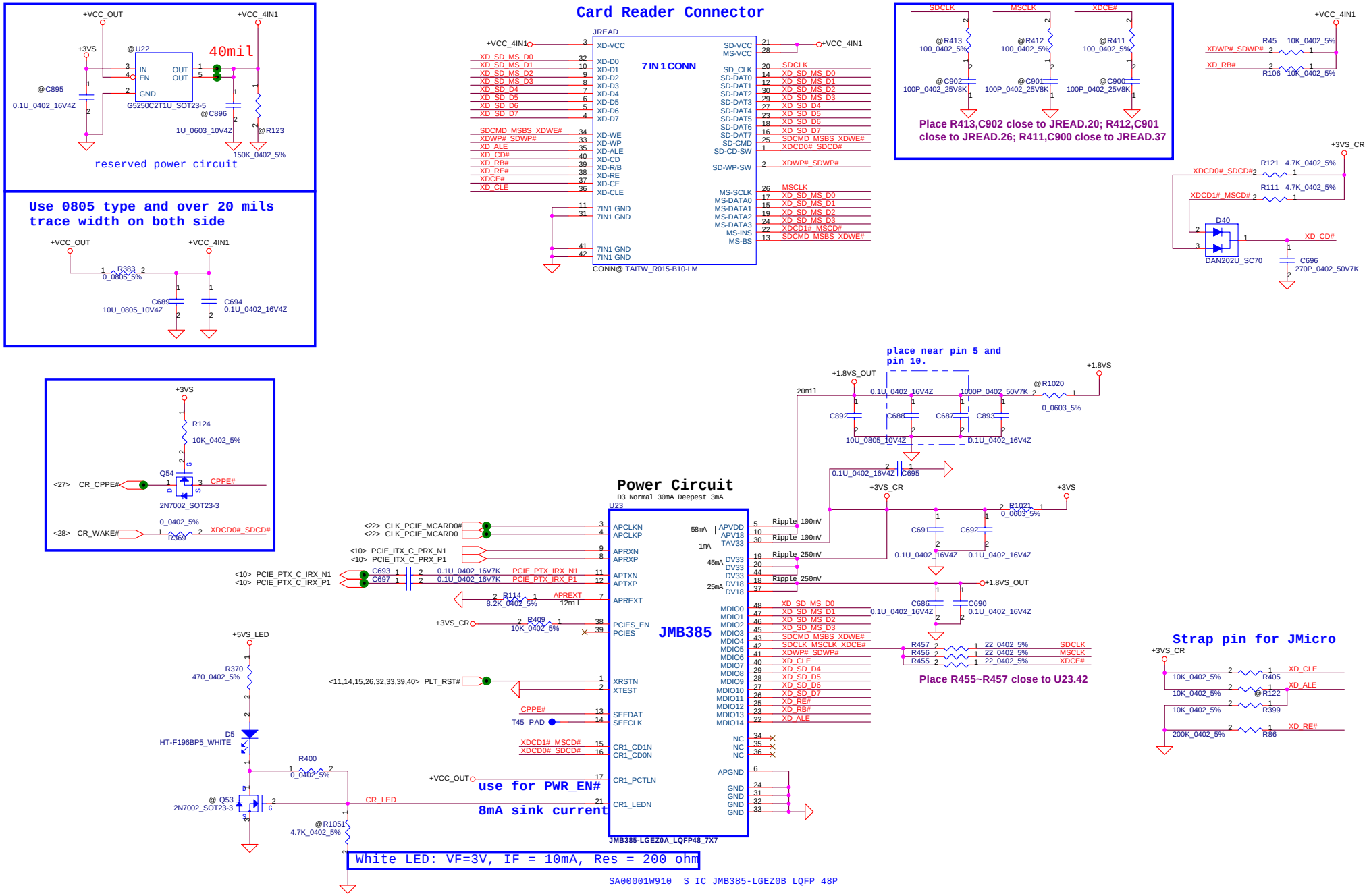
Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **WLAN**

Size	Document Number	Rev
Custom	LA-4114P	0.1

Date: Thursday, November 06, 2008 | Sheet 33 of 54



Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

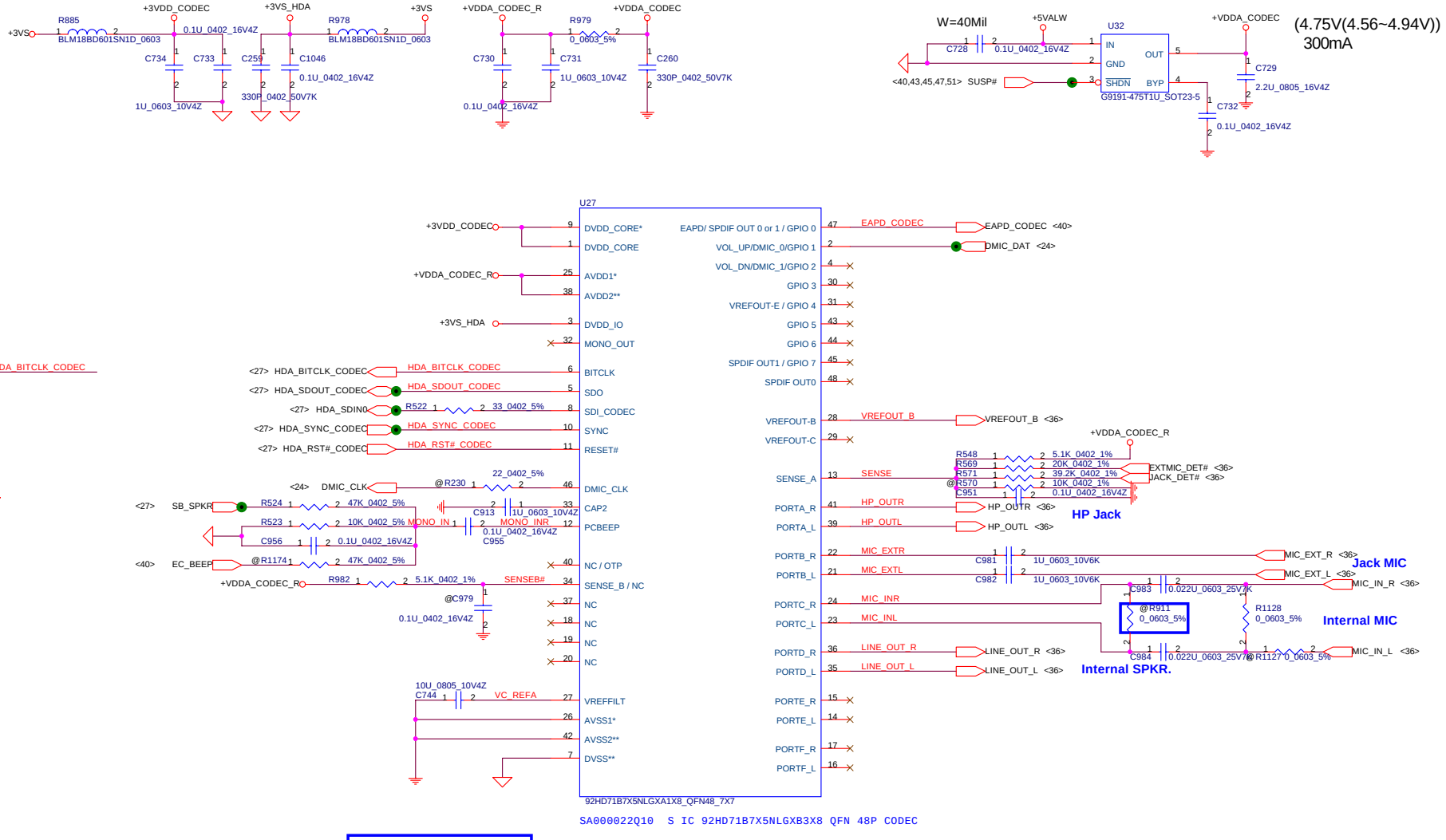
Compal Electronics, Inc.

Title: **PCI-E I/F Card Reader-JM385**

Size	Document Number	Rev
Custom	LA-4114P	0.1

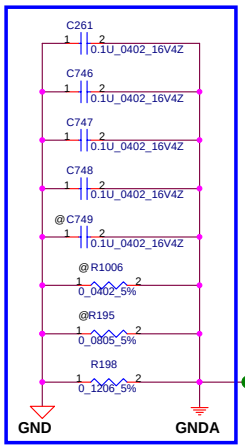
Date: Thursday, November 06, 2008 Sheet 34 of 54

CODEC POWER



SA000022Q10 S IC 92HD71B7X5NLGXB3X8 QFN 48P CODEC

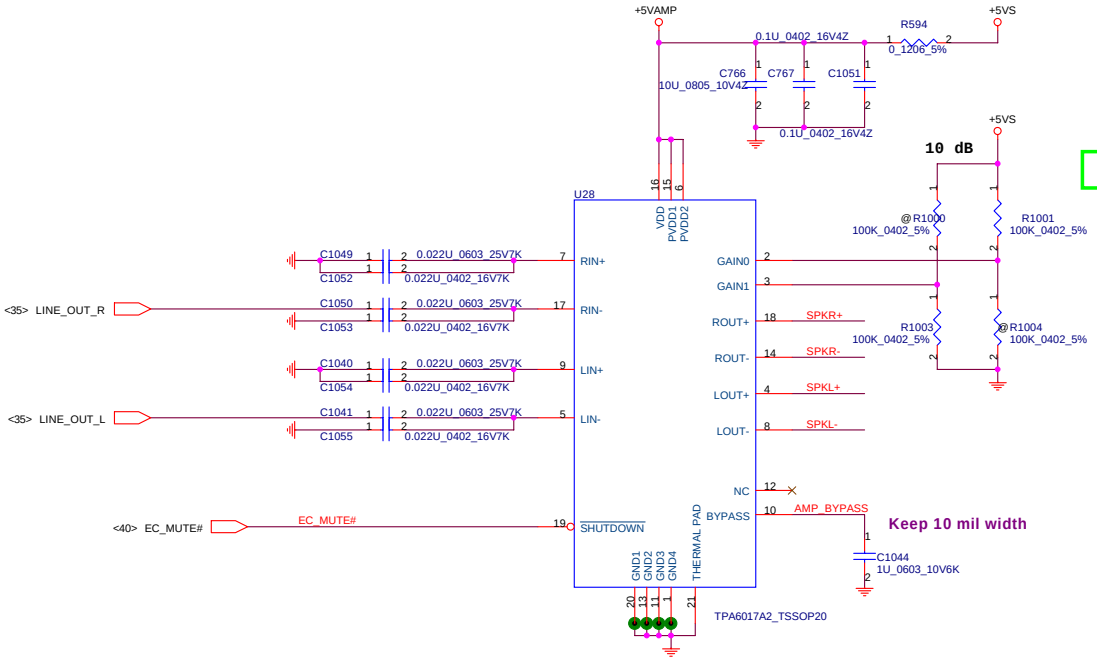
SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K



Use an 80mil to connection or place a 1206 resistor under CODEC with double vias.

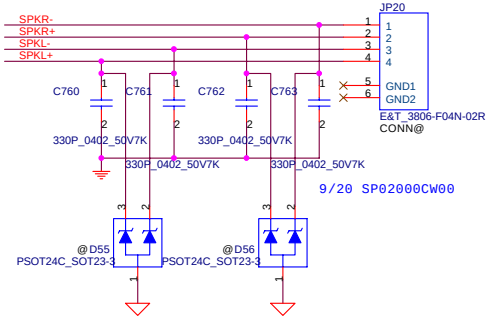
Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.	
Title	Audio Codec-IDT9271B7
Size: Custom	Document Number: LA-4114P
Rev	0.1
Date: Thursday, November 06, 2008	Sheet 35 of 54

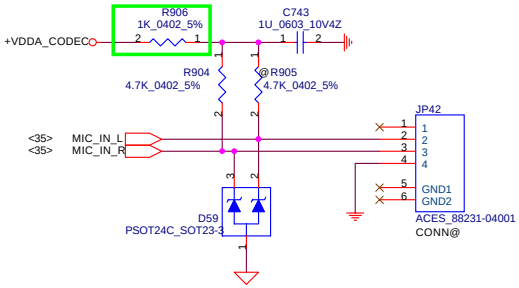


GAIN0	GAIN1	Av(inv)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

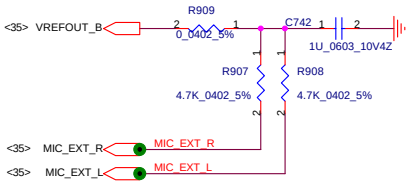
SPEAKER



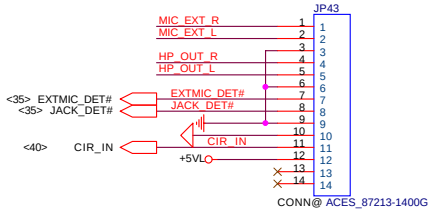
INTMIC IN

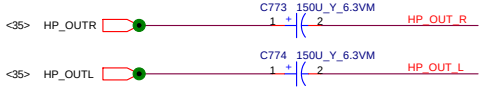


Audio/B & CIR



EXTMIC IN



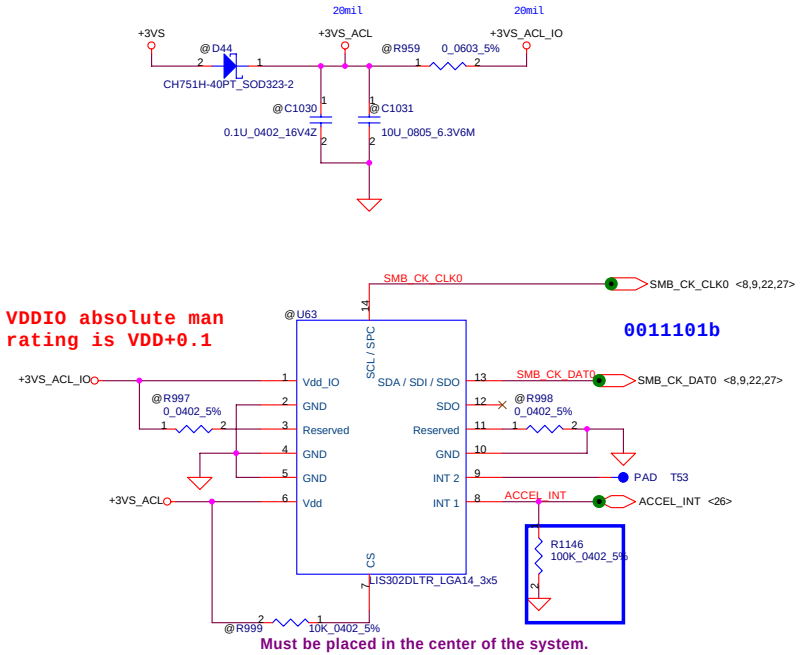


HP OUT For M/B

Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.			
Title: AMP & Audio Jack			
Size: Custom	Document Number: LA-4114P		Rev: 0.1
Date: Thursday, November 06, 2008	Sheet 36 of 54		

ACCELEROMETER



Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

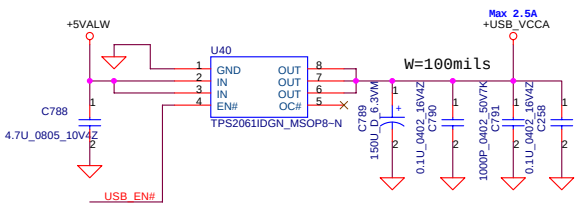
Compal Electronics, Inc.

Title: **Accelerometer**

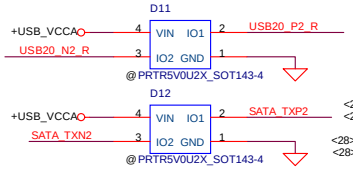
Size	Document Number	Rev
Custom	LA-4114P	0.1

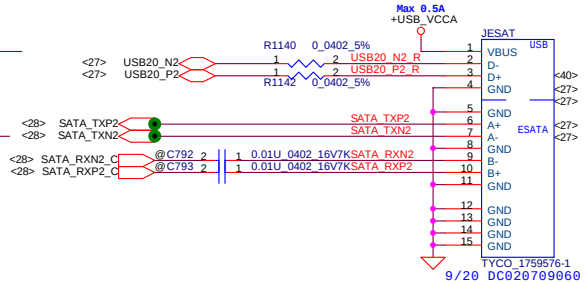
Date: Thursday, November 06, 2008 Sheet 37 of 54

Left side USB CONNECTOR

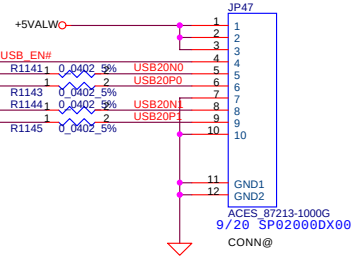


Left side ESATA5/USB2 combination Connector

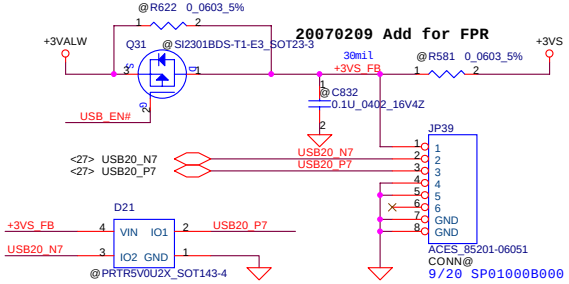




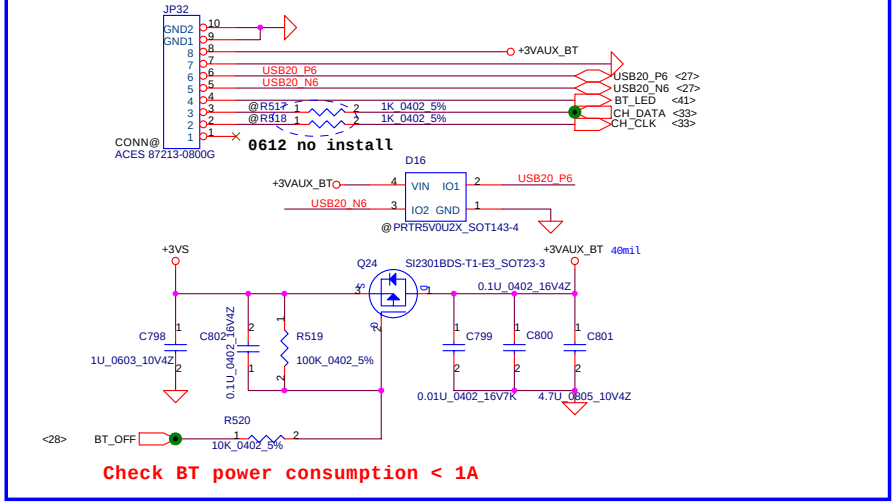
Right side USB 0&1 Board Conn



Finger printer



BT Connector

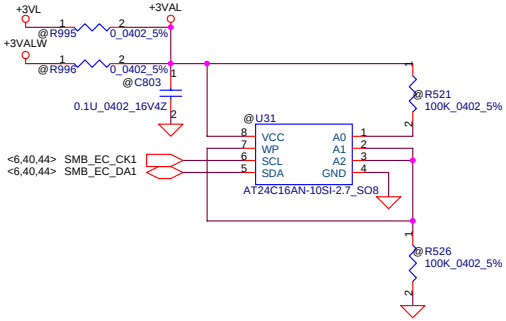


Finger printer

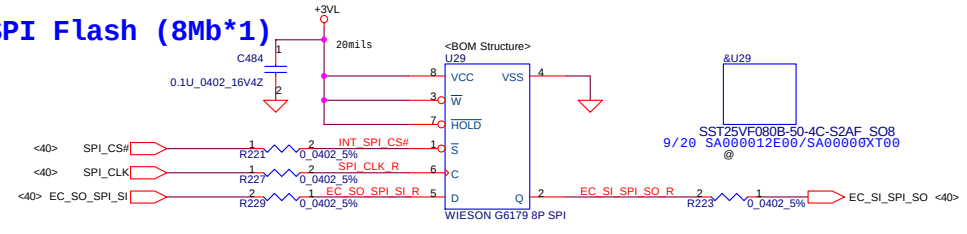
BT Connector

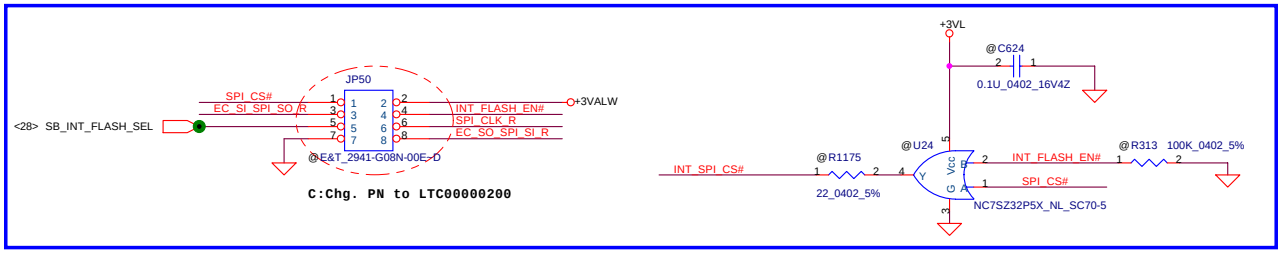
Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.			
Title	USB, BT, eSATA,FPR		
Size: Custom	Document Number: LA-4114P		Rev: 0.1
Date: Thursday, November 06, 2008	Sheet 38 of 54		

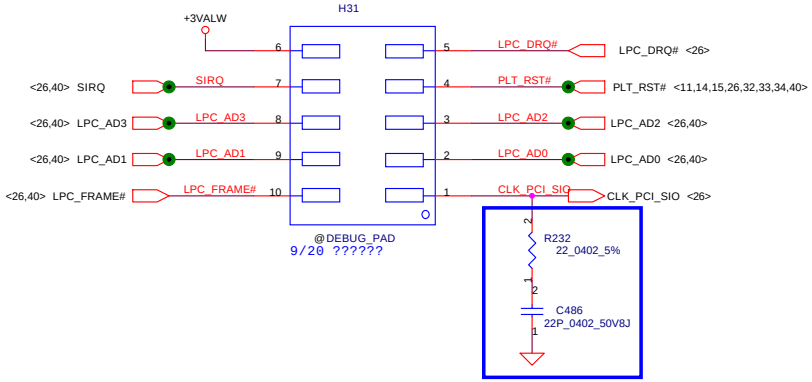


SPI Flash (8Mb*1)

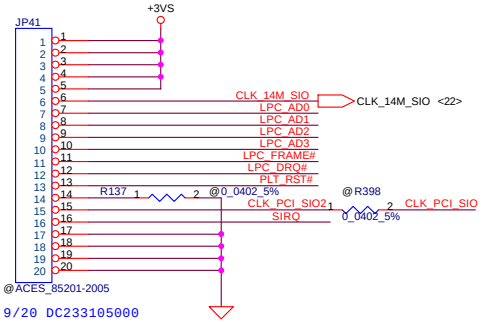




LPC Debug Port

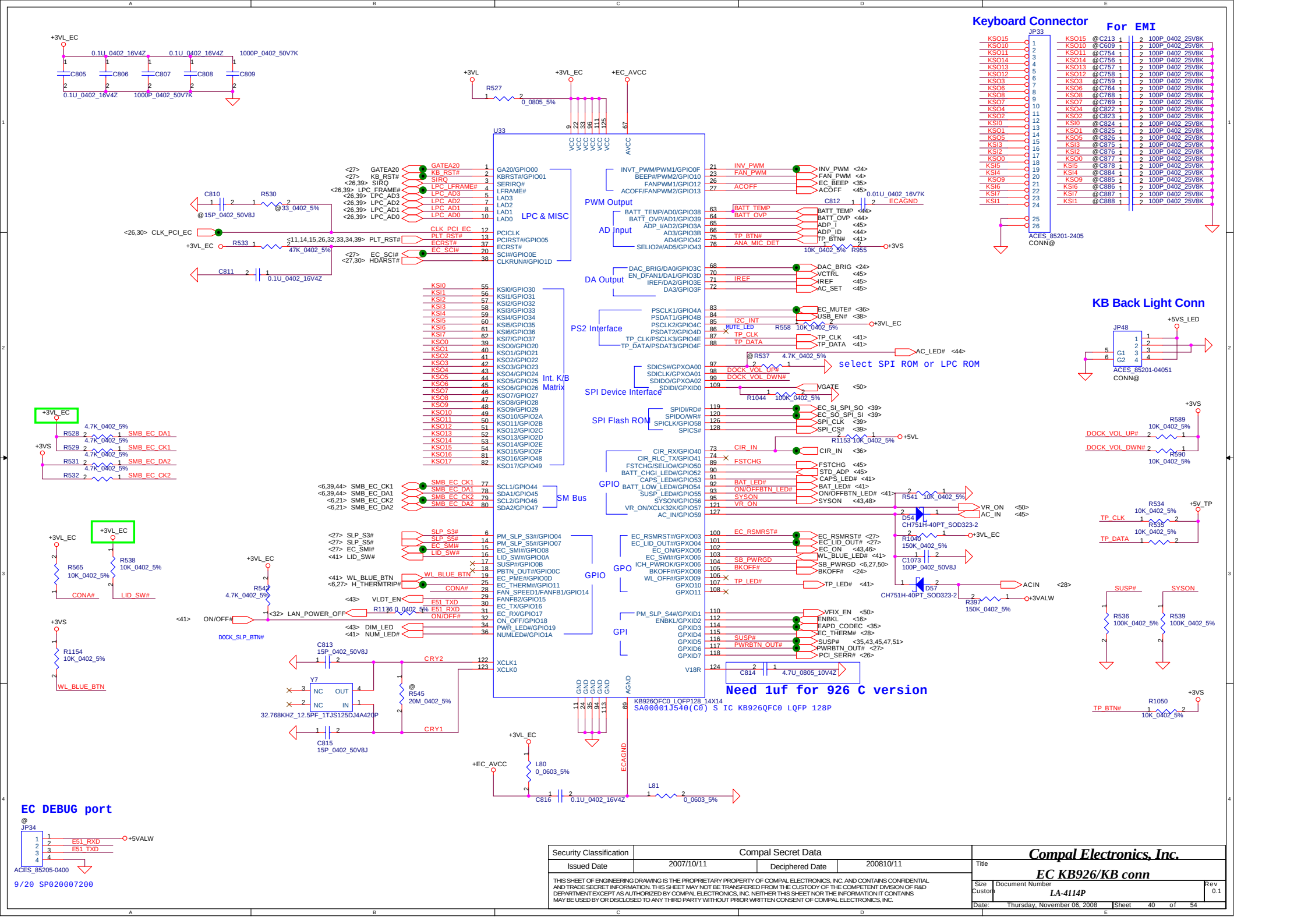


LPC Debug Port



Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.			
Title: BIOS ROM/Debug Tool			
Size: Custom	Document Number: LA-4114P		Rev: 0.1
Date: Thursday, November 06, 2008	Sheet 39 of 54		


Keyboard Connector
For EMI
JP33
ACES_85201-2405
CONN@
KB Back Light Conn
JP48
ACES_85201-04051
CONN@
select SPI ROM or LPC ROM
U33
KB926QFC0_LQFP128_14X14
SA00001J540(C0) S IC KB926QFC0 LQFP 128P
Need 1uf for 926 C version
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
EC DEBUG port
JP34
ACES_85205-0400
9/20 SP020007200
Security Classification
Compal Secret Data
Issued Date
2007/10/11
Deciphered Date
200810/11
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Compal Electronics, Inc.
Title
EC KB926/KB conn
Size
Custom
Document Number
LA-4114P
Rev
0.1
Date:
Thursday, November 06, 2008
Sheet
40
of
54

for debug only

BTN

TOP

@R1178 0_0603_5%

ON/OFF#

@SW3

SMT1-05_4P

ON/OFF Button Connector(delete)

TP ON/OFF

+3VALW

R1038 @10K_0402_5%

SW1 SMT1-05-A_4P

TP_BTN#

TP_BTN# <40>

Max 0.5A

+5VALW

R235 0_0603_5%

+5V_TP

@Q85 SI2301BDS-T1-E3_SOT23-3

<43,49> SYSON#

M/B TO TP/B

Max 0.5A

+5V_TP

TP_DATA

TP_CLK

C819 0.1U_0402_16V4Z

D31 PSOT24C_SOT23-3

JP37

TP_CLK

TP_DATA

TP_CLK <40>

TP_DATA <40>

ACES_85201-04051

CONN@

9/20 SP01000KC00/SP01E000900

@C820 100P_0402_50V8J

@C821 100P_0402_50V8J

MDC 1.5 Conn.

9/20 SP01000J100

9/20 STANDOFF (H= 5.0 mm) ES000000800

CONN@ JP25

GND1 IAC_SDATA_OUT GND2 IAC_SYNC IAC_SDATA_IN IAC_RESET#

RES0 RES1 3.3V GND3 GND4 IAC_BITCLK

<27> HDA_SDOUT_MDC

<27> HDA_SYNC_MDC

<27> HDA_SDIN1

<27> HDA_RST#_MDC

R495 33_0402_5%

HDA_SDIN1_MDC

+3VS

HDA_BITCLK_MDC <27>

@R496 10_0402_5%

ACES_88018-124G

Connector for MDC Rev1.5

C778 C779 C780 @4.7U_0805_10V4Z

1000P_0402_50V7K

0.1U_0402_16V4Z

@C777 10P_0402_50V8J

SWITCH BOARD.

+5VALW_LED

+5VS_LED

JP36

<40> ON/OFFBTN_LED#

ON/OFFBTN_LED#

<40> WL_BLUE_BTN

WL_BLUE_LED#

<40> NUM_LED#

<40> ON/OFF#

ON/OFF#

ACES_85201-1005N

CONN@

9/20 SP01000H400

HDD LED

+5VS

WHITE

+5VS_LED

R1177 10K_0402_5%

D46 HT-F196BP5_WHITE SC500004W00

R988 200_0402_5%

Q172B 2N7002DW-7-F_SOT363-6

<28> SATA_LED#

Q172A 2N7002DW-7-F_SOT363-6

TouchPAD ON/OFF LED

+5VS_LED

R983 200_0402_5%

R984 200_0402_5%

+5VS

AMBER WHITE

D45 HT-297UY5/BP5_YELLOW-WHITE

On (TP_LED#=L)-> White

Off (TP_LED#=H)-> Amber

R985 10K_0402_5%

Q153 2N7002_SOT23-3

TP_LED#

TP_LED# <40>

Reed switch BOARD.

+3VL

C262 0.1U_0402_16V4Z

JP40

<40> LID_SW#

C263 10P_0402_50V8J

ACES_85201-04051

CONN@

9/20 SP020020710

Battery Charge LED

WHITE

+5VALW_LED

<40> BAT_LED#

D50 HT-F196BP5_WHITE SC500004W00

R550 200_0402_5%

CAPS LOCK LED

WHITE

+5VS_LED

<40> CAPS_LED#

D30 HT-F196BP5_WHITE SC500004W00

R552 470_0402_5%

POWER LED

WHITE

+5VALW_LED

ON/OFFBTN_LED#

D27 HT-F196BP5_WHITE SC500004W00

R549 200_0402_5%

White LED: VF=3V, IF = 10mA, Res = 200 ohm

Amber LED: VF=1.8V, IF = 8mA, Res = 390 ohm

WLAN and BT LED inform pin to KBC

+5VS

+3VS

R989 10K_0402_5%

R1152 10K_0402_5%

<40> WL_BLUE_LED#

WL_BLUE_LED#

Q158A 2N7002DW-7-F_SOT363-6

WL_LED# <33>

Q158B 2N7002DW-7-F_SOT363-6

BT_LED <38>

R1025 100K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

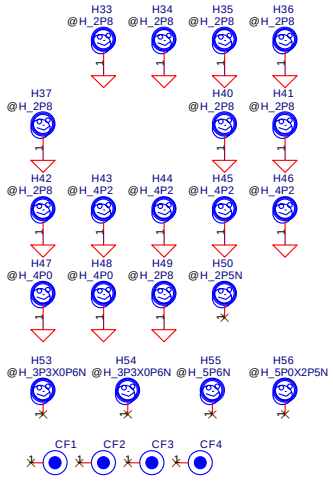
Compal Electronics, Inc.

Title: TP,MDC,ON/OFF,S/W,LED,Reed

Size: Custom | Document Number: LA-4114P | Rev: 0.1

Date: Thursday, November 06, 2008 | Sheet 41 of 54

H47, H48 -Stand off of MODEM on BOT Side



Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

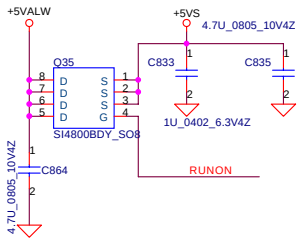
Compal Electronics, Inc.

Title: **SCREW HOLE**

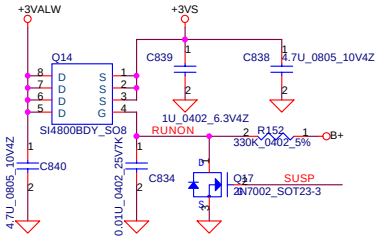
Size	Document Number	Rev
Custom	LA-4114P	0.1

Date: Thursday, November 06, 2008 Sheet 42 of 54

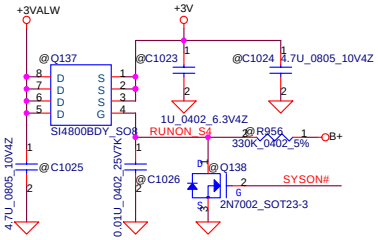
+5VALW TO +5VS



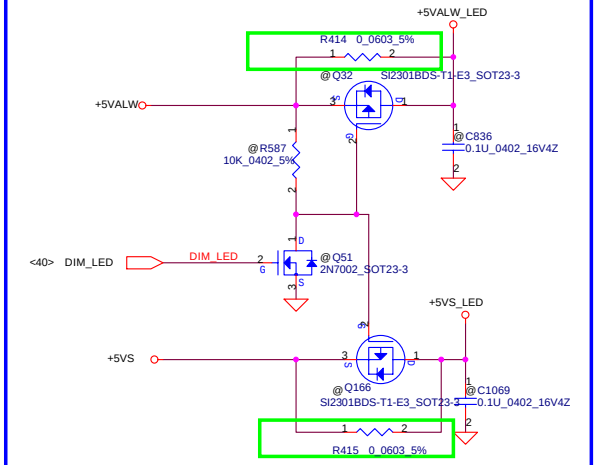
+3VALW TO +3VS



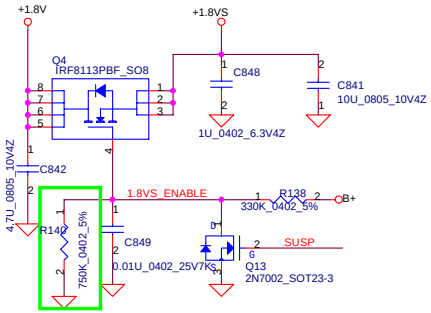
+3VALW TO +3V



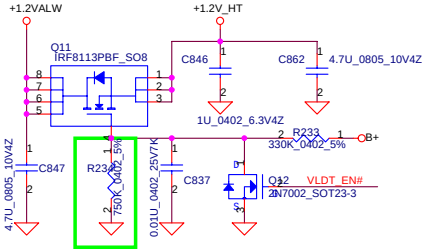
DIM LED



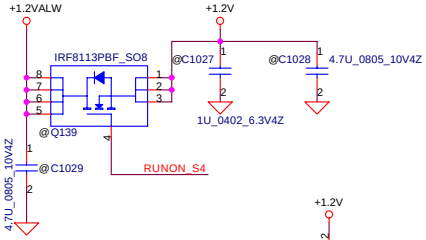
+1.8V TO +1.8VS

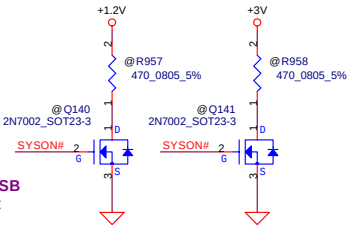


+1.2VALW TO +1.2V_HT

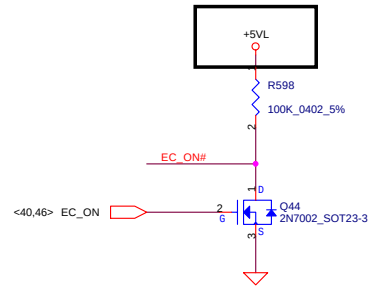


+1.2VALW TO +1.2V

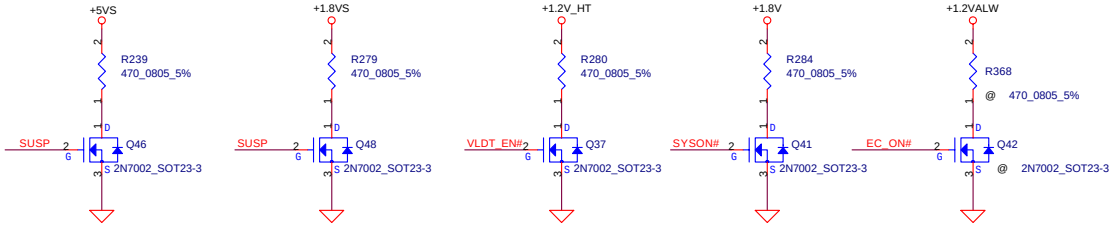


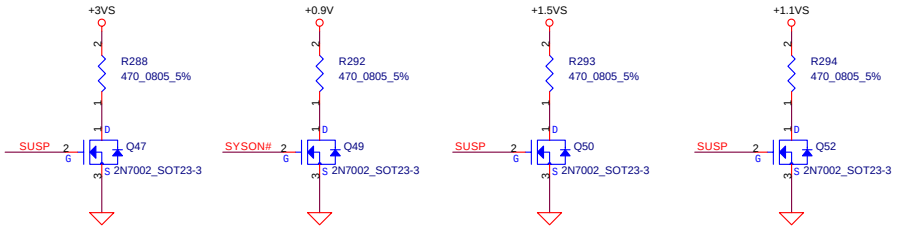


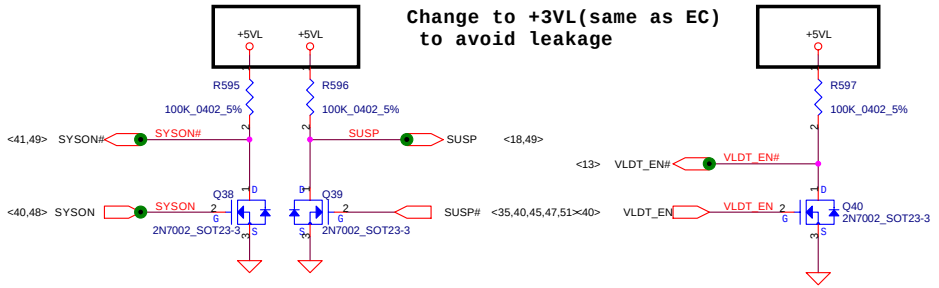
Reserve until SI-1 stage after SB USB PHY power saving report



Discharge circuit







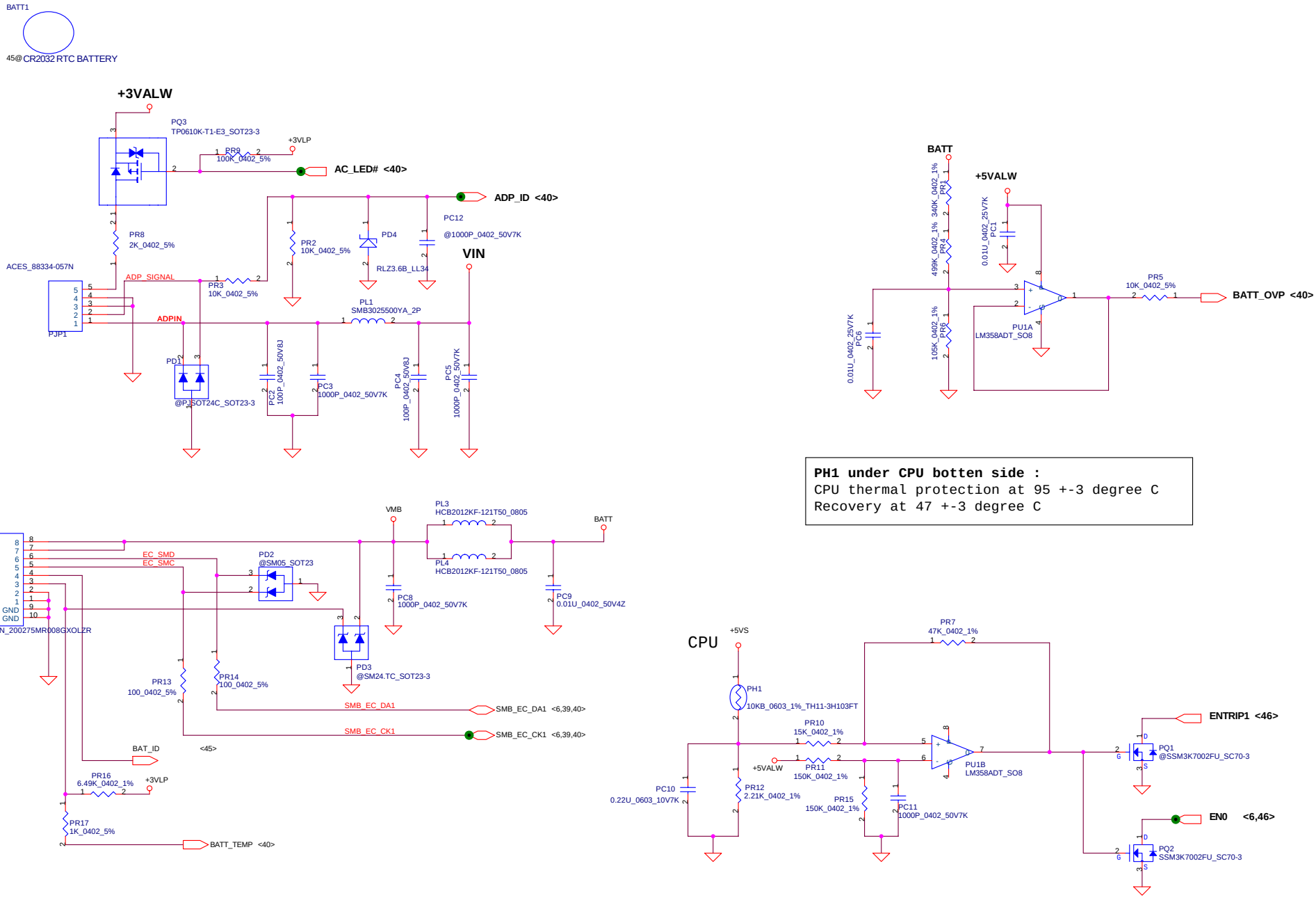
Security Classification	Compal Secret Data		
Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **DC/DC Circuits**

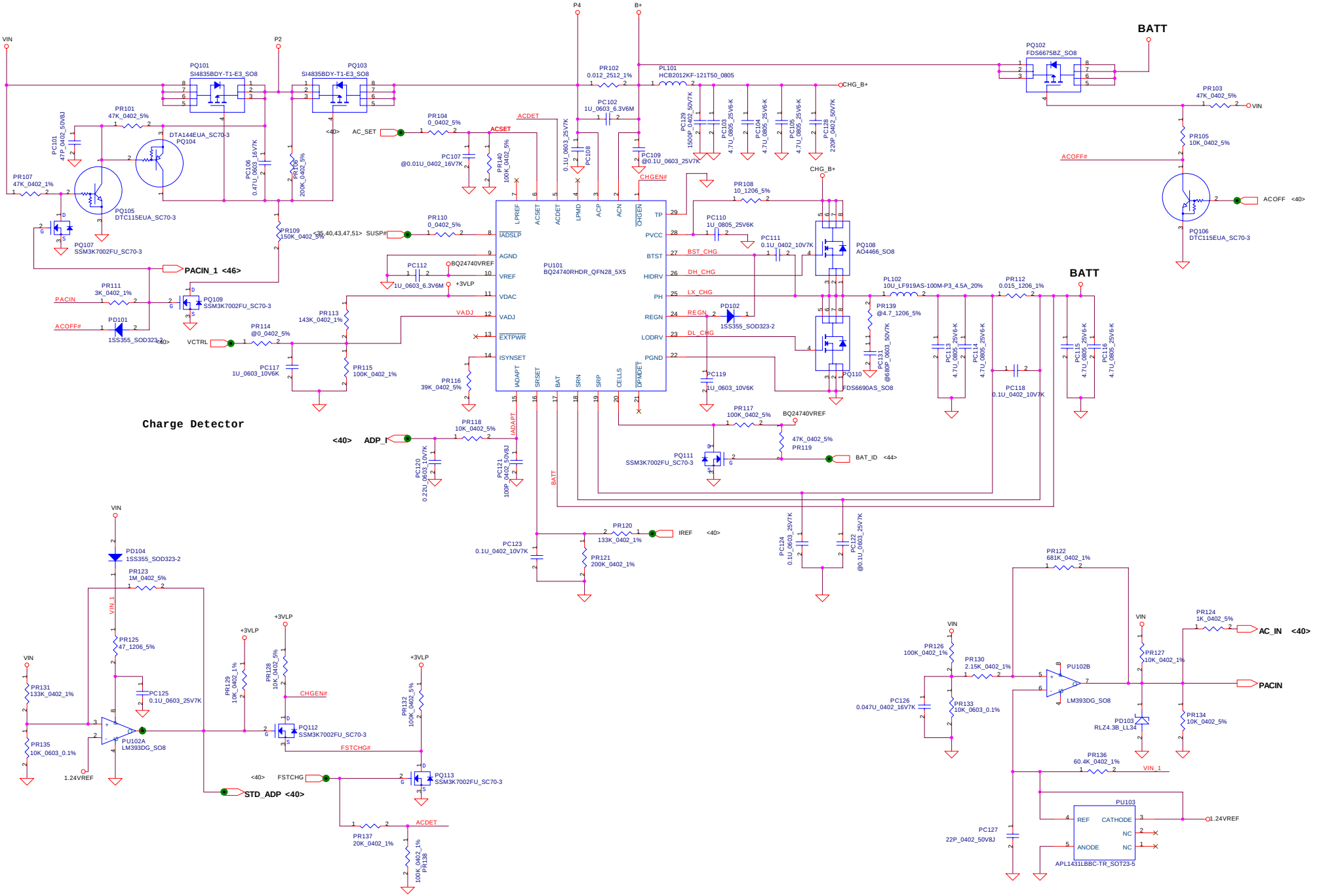
Size	Document Number	Rev
Custom	LA-4114P	0.1

Date: Thursday, November 06, 2008 Sheet 43 of 54



Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	200810/11

Compal Electronics, Inc.			
Title: DC Connector/CPU_OTP			
Size: Custom	Document Number: LA-4114P		Rev: 0.1
Date: Thursday, November 06, 2008	Sheet 44 of 53		



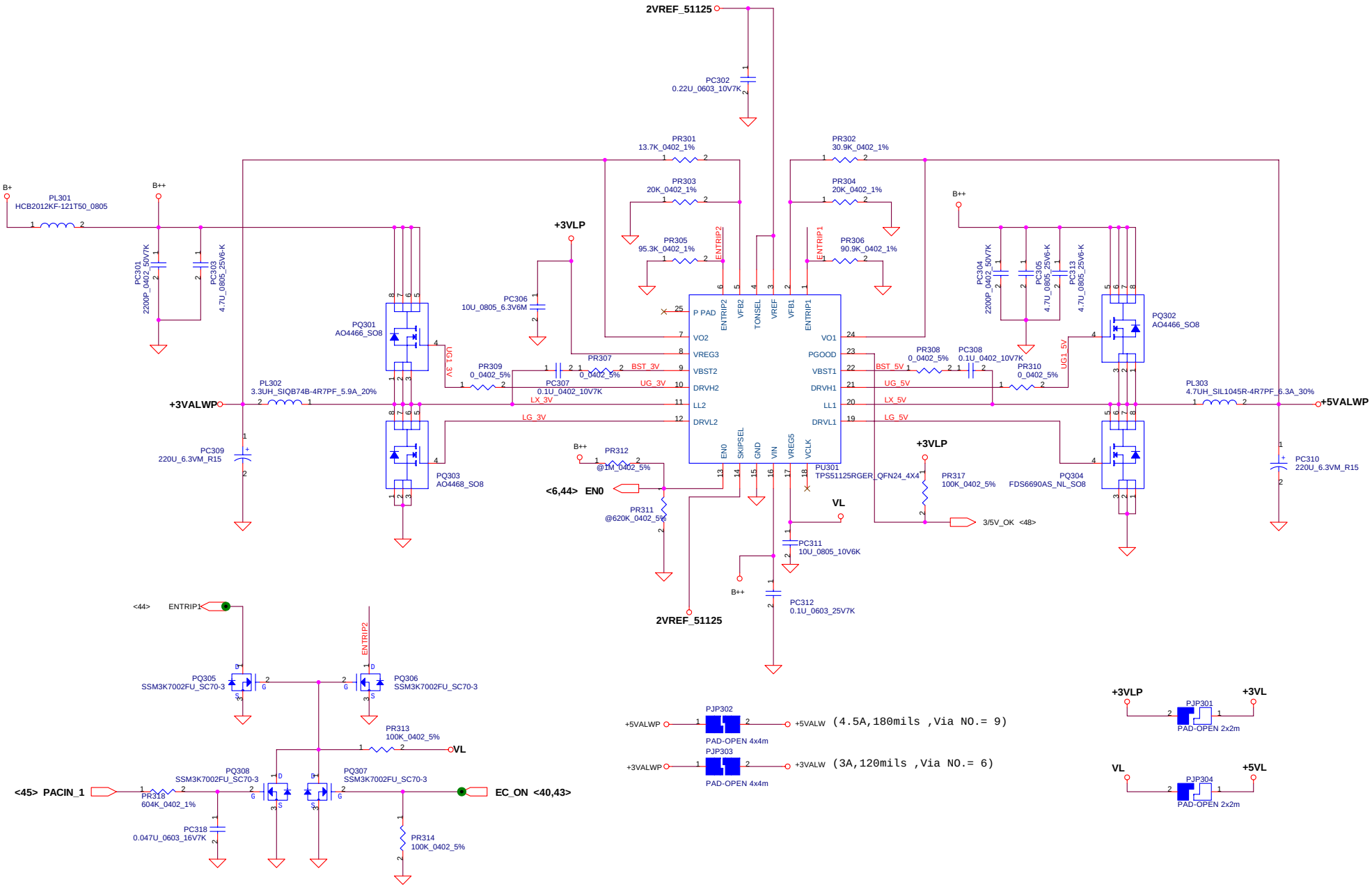
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **Charger**

Size	Document Number	Rev
	LA-4114P	0.1

Date: Thursday, November 06, 2008 | Sheet 45 of 53



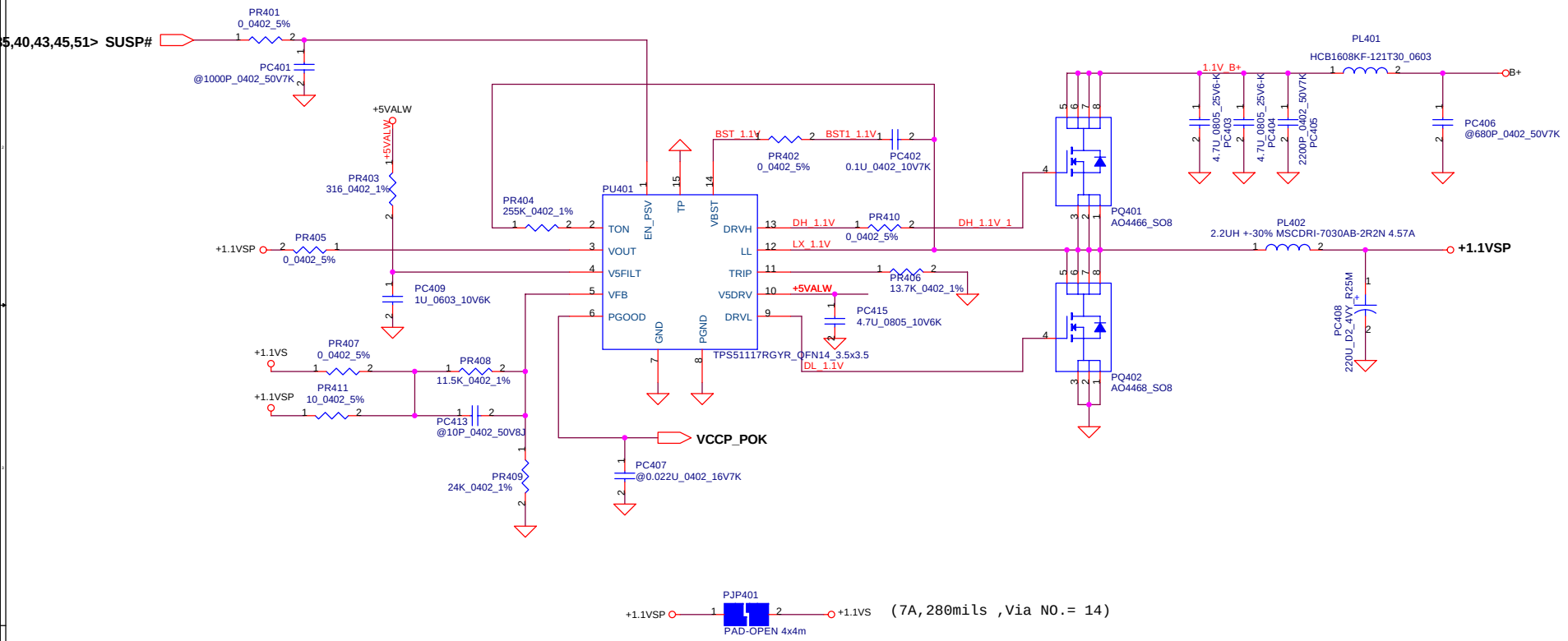
Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **3.3VALWP/5VALWP**

Size	Document Number	Rev
Custom	LA-4114P	0.1

Date: Thursday, November 06, 2008 | Sheet 46 of 53



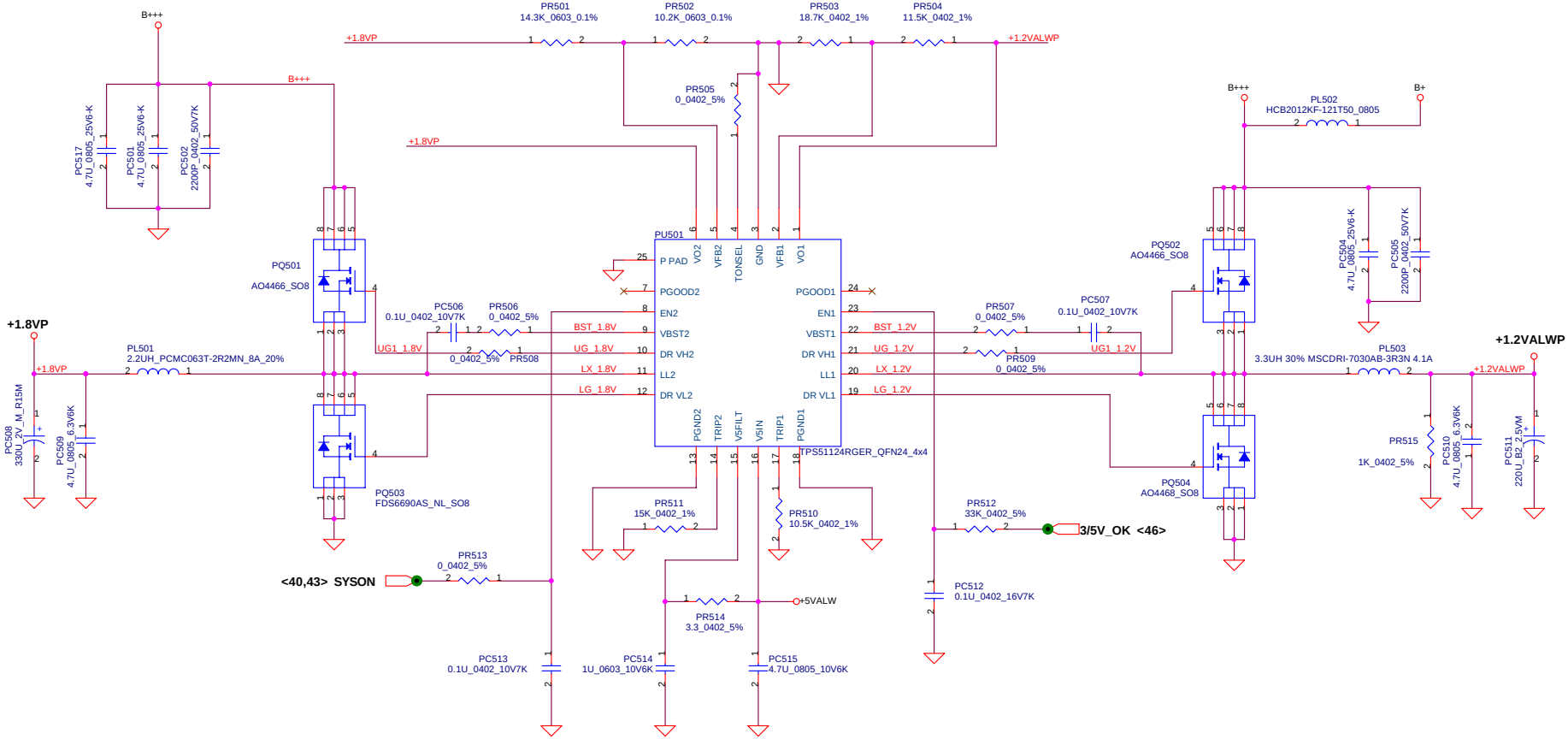
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **1.1VSP**

Size	Document Number	Rev
	LA-4114P	0.1

Date: Thursday, November 06, 2008 | Sheet 47 of 53



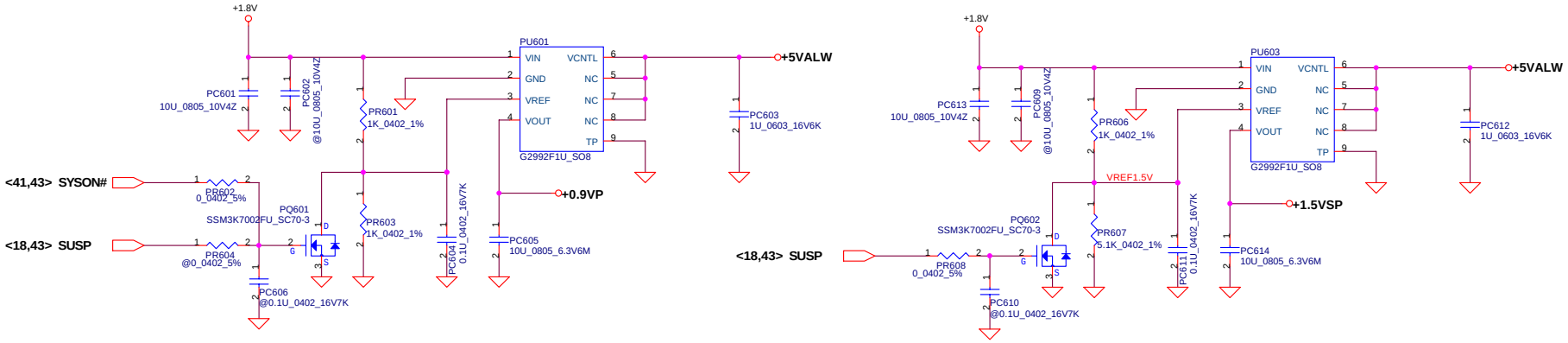
Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	200810/11

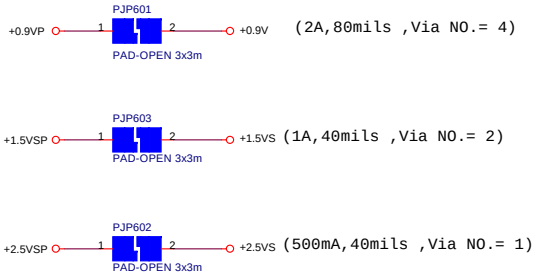
Compal Electronics, Inc.

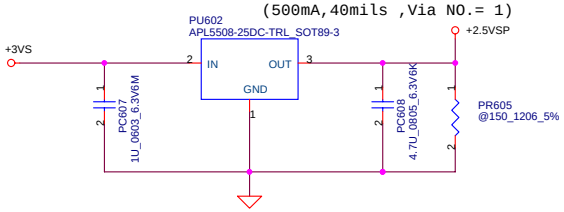
Title: **1.8VP/1.2VALWP**

Size	Document Number	Rev
Custom	LA-4114P	0.1

Date: Thursday, November 06, 2008 | Sheet 48 of 53







Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **0.9VSP/2.5VSP/1.5VSP**

Size	Document Number	Rev
Custom	LA-4114P	0.1

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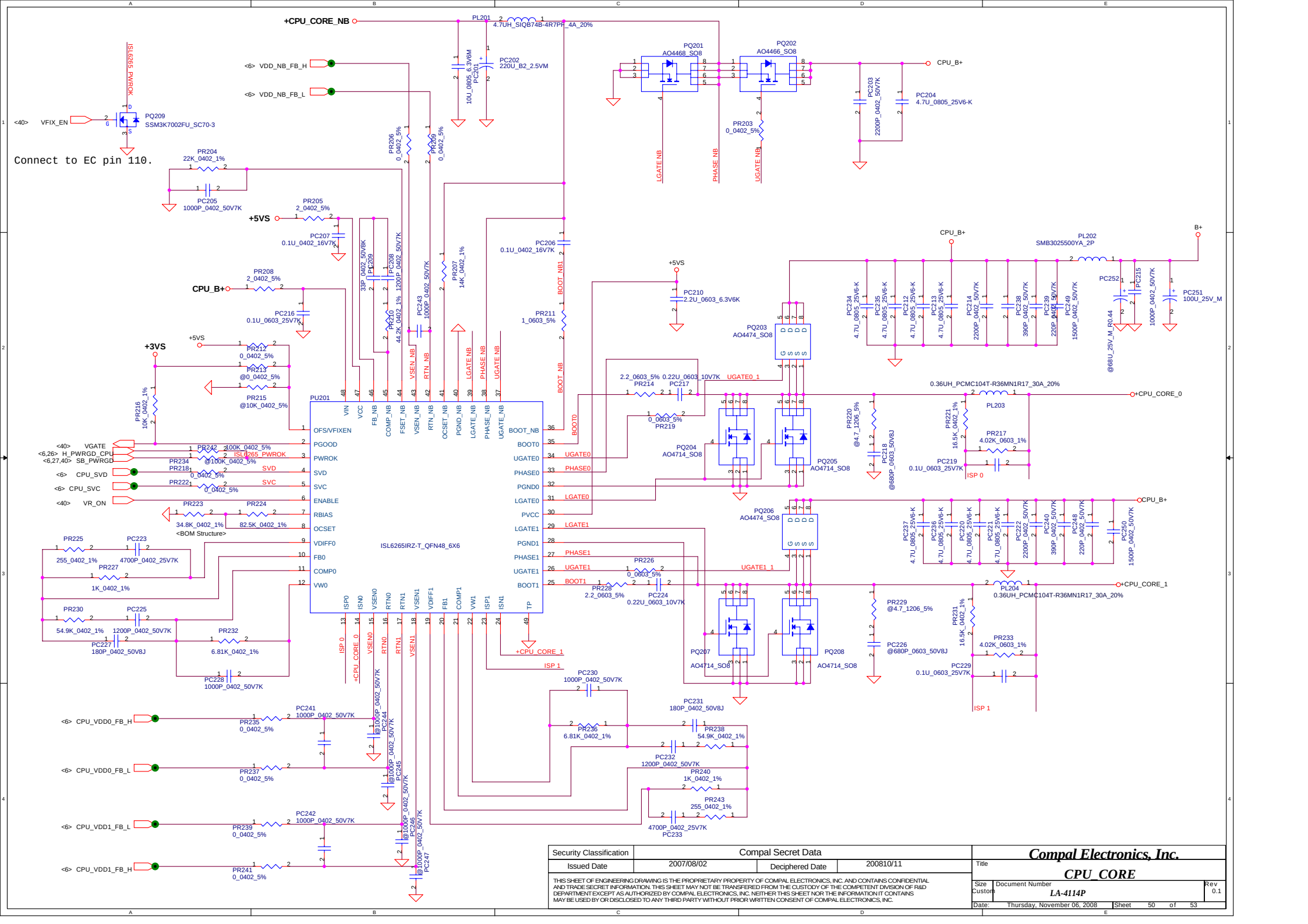

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	200810/11

Compal Electronics, Inc.

Title: **CPU_CORE**

Size	Document Number	Rev
Custom	LA-4114P	0.1

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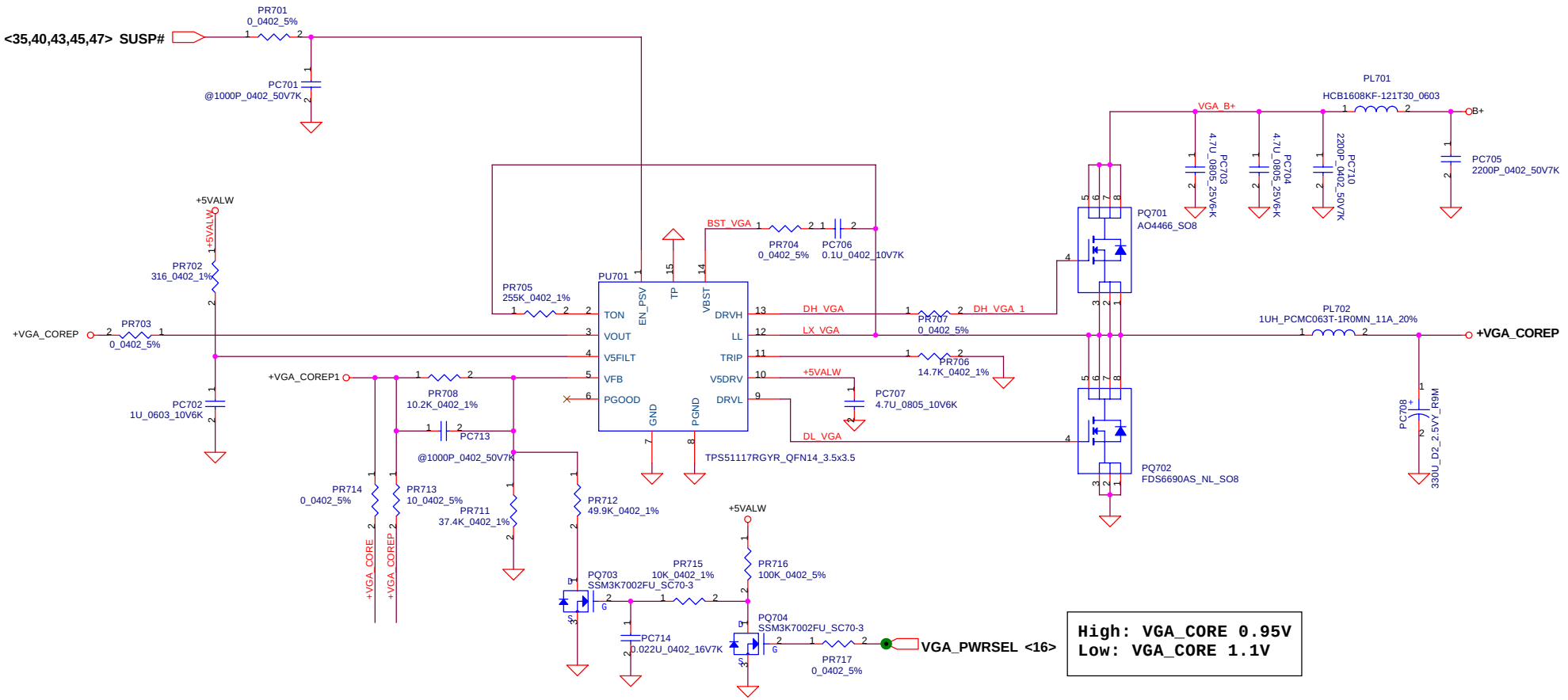

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Compal Electronics, Inc.

Title: VGA_CORE

Size | Document Number: LA-4114P | Rev: 0.1

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LA-4112P Rev0.1 -> 0.2 Product Improvement Record (P.I.R.)

BOM change list:

1. Stuff R41(220 Ohm), R26(300 Ohm), R28(300 Ohm). (Page 6)-* AMD recommand.
2. Stuff R1101(10K Ohm). (Page 21)-* Strenghen PCI-E swing to meet PCI-E spec.
3. Un-Stuff R1061,R1062,R1064/Change R214,R211,R217 from 150 -> 75 Ohm/C858,C476,C472 from 22p -> 6pF/Chagne L47,L48,L49 type (Page 16/25)-* Tune CRT(R/G/B) rising & falling skew time to meet SPEC.
4. Change C863 1000p -> 0.047uF. (Page 24)-* For LED Panel power up timing >0.5mSec.
5. Change C643,C652 18p -> 12pF. (Page 26)-* Tune RTC 32K Caps to meet HP SVTP spec.
6. Change R323 11.8K -> 11K Ohm. (Page 27)-* Tune the value to meet USB EE spec.
7. Change R356 10K -> 2.2K Ohm. (Page 30)-* ATI recommand.
8. Change C1040 10U -> 1UF. (Page 36)-* Reduce Power up "BOBO" noise.
9. Change Keyboard connecter type. (Page 40)-* For ME request.
10. Change Reed Switch Board connecter type. (Page 41)-* For ME request.
11. Un-stuff C9. (Page 4)-* Fixed Caps issue noise.
12. Change R371 10K -> 300 Ohm. (Page 10)-* ATI recommand.
13. Un-stuff L2,L4,L6,L9,L7/Stuff C170,C172,C175,C178,C176 0 Ohm. (Page 11)-* ATI RX781 changed recommand.
14. Un-stuff R1054/Stuff C252 0 Ohm. (Page 13)-* ATI RX781 changed recommand.
15. Un-stuff C250,C253. (Page 13)-* Follow 17" AMD circuit change.
16. Change C101,C102 1K->3K Ohm. (Page 14)-* ATI recommand.
17. Un-stuff R1067. (Page 16)-* Follow 17" AMD circuit circuit change.
18. Un-stuff R1155,R1157,R1159. (Page 28)-* Dont need to reserve it for UMA side port buffer strapping.

Circuit change list:

1. Del Q6, Q5 (Page 10)-* Dont need to reserve it.
2. Divide DPA_PDD & DPB_PVDD power.(Page 16)-* ATI recommand.
3. Del Q155 (Page 26)-* Dont need to reserve it.
4. Chagne PCICLK output source to LPCCLK1 output. (Page 26)-* Follow 17" AMD circuit change.
5. Add SSC circuit for AZ bus BIT CLK. (Page 27)-* EMI request.
6. Delete R1002,R1005. (Page 36)-* Dont need to reserve it for line out serial resistor from CODEC to AMP.
7. Modify JP20 speaker signals define. (Page 36)-* DB stage define error fix.
8. Chagne C802 position to +3VALW. (Page 38)-* DB stage +3VAUX_BT leakage fix.
9. Chagne U24 power source from +3VALW -> +3VL. (Page 39)-* Power souce need to be the same power source of SPI ROM.
10. Delete LPC debug port circuit. (Page 39)-* With BIOS discuss and delete it.
11. Add power requesting net "VFIX_EN". (Page 40)-* Power request.
12. Change JP36 pin7 GND -> NC. (Page 41)-* Follow Riply pin define.
13. Swap D45 T/P LED. (Page 41)-* DB Stage LED behavior error fix.
14. Add a signal AC_LED# of EC pin97 & VFIX_EN of EC pin110.. (Page 40)-* Power request.
15. Change AC_IN pull high from +3VALW to +3VL_EC. (Page 40)-* Power request.

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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	46	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF	
2	51	VGA_COREP	12/31	Compal	PWR request	Connect the PR715 and PC714 to PQ703 pin1	
3	51	VGA_COREP	12/31	Compal	EMI request	Change PC705 to 2220pF	
4	50	CPU_CORE	12/31	Compal	EMI request	Add PC238, PC239, PC240, PC248	
5	50	CPU_CORE	12/31	Compal	Vendor request	Change PR221 and PR231 to 16.6K_ohm Change PR217 and PR233 to 4.02K_ohm Change PR223 to 17.8K_ohm Change PR224 to 100K_ohm	
6	45	Charger	12/31	Compal	EMI request	add PC128	
7	45	Charger	01/04	Compal	PWR request	Change PQ102 to FDS6675BZ	
8	50	CPU_CORE	01/04	Compal	PWR request	Change PQ204, PQ205, PQ207, PQ208 to FDS6676AS Add PQ209 and PQ234 to fix CPU core voltage.	
9	44	DC Connector /CPU_OTP	01/09	Compal	AC LED change to KBC control	AC_LED connect to KBC pin 97	
10	51	VGA_COREP	02/27	Compal	Change VGA low voltage to 0.95V	Change PR712 to 49.9K_ohm and PR711 to 37.4K_ohm	
11	46	3.3VALWP/5VALWP	02/27	Compal	Change OTC shun down pin.	Change OTC shun down pin to PU301 pin13.	
12	50	CPU_CORE	03/03	Compal	EMI request	Add PC249, PC250	
13	45	Charger	03/03	Compal	EMI request	Add PC129	
14	50	CPU_CORE	03/03	Compal	HW request	Add H_PWRGD	
15	44	DC Connector /CPU_OTP	04/02	Compal	AC LED issue	Chaange AC_LED# pull high to +3VLP	
16	50	CPU_CORE	04/24	Compal	acoustic noise	Add PC251	
17	44	DC Connector /CPU_OTP	04/24	Compal	HW CPU thermal protection change to 95 +-3 degree C	Chaange PR12 to 2.21K_ohm	

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Title: Power Changed-List History-1			
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LA-4112P Rev0.2 -> 0.3 Product Improvement Record (P.I.R.)

Circuit change list:

1. Un-Stuff C18, Q127, Q129, R175, R814, C939 and change SMBus 2 -> SMBus 1. (Page 6)-* Follow 17" AMD circuit change.
2. Add signal H_PWRGD_CPU to option CPU core chip`s PWR OK. (Page 6)-* Follow AMD recommand power up sequence change.
3. Change signal name ENTRIP2 to EN0. (Page 6)-* For power team chagne request.
4. Un-Stuff C54. (Page 7)-* Follow 17" AMD circuit change.
5. AVDD1, AVDD2, AVDDI, AVDDQ, .PLVDD, PLVDD18, VDDLTP18, VDDLT18_1, VDDLT18_2 directly conecct to GND. (Page11)-* For RX781 change recommand.
6. VDD18_MEM1, VDD18_MEM_2 directly conecct to GND. (Page 13)-* For RX781 change recommand.
7. Change Bead L16, L22 to 0 ohm and Delete L20, L21 than use jumper to link the power. (Page 13)-* Follow 17" AMD circuit change.
8. Change R101, R102 3K -> 1K ohm. (Page 14)-* ATI recommand.
9. Add VGA_PWN to Panel. (Page 16/24)-* For panel power saving request.
10. Un-stuff R1101. (Page 21)-* For PCI-E EA request.
11. Add signal CLK_14M_SIO. (Page 22)-* For debug port requst.
12. Stuff C447. (Page 23)-* EMI/ESD recommand.
13. Add +5VS power for webcam`s LDO power option. (Page 24)-* Follow 17" AMD circuit change.
14. Change C863 0.047U -> 1000p. (Page 24)-* Fix panel power down waveform bounce.
15. Change Bead L61, L61 to 0 ohm. (Page 29)-* Follow 17" AMD circuit change.
16. Un-stuff R1148, C1271. (Page 32)-* Follow 17" AMD circuit change.
17. Modify JRJ45 layout footprint. (Page 32)-* For DFX request.
18. Add D58 ESD diode. (Page 32)-* EMI/ESD recommand.
19. Stuff R1043, Un-stuff R1042 (Page 33)-* Follow 17" AMD circuit change.
20. Add R399, R400 and un-stuff R122, R1051, Q53.(Page 34)-* Follow project common design.
21. Add C259, C260, C261 and stuff C746, C747,C748 and change C760, C761, C762, C763 100p -> 330p. (Page 35/36)-* EMI/ESD recommand.
22. Signal INTMIC_DET directly connect to AGND and Delete Q160, Q151, R951. (Page 35/36)-* OPP dont need the detect circuit.
23. Add C258. (Page 38)-* EMI/ESD recommand.
24. ME change JP32 and change Q24`s power +3VALW -> +3VS. (Page 38)-* Follow 17" AMD circuit change.
25. Add LPC debug port. (Page 39)-* For debug request.
26. Add D57, R397. (Page 40)-* Fix AC-IN chip power rail different issue.
27. Delete Q34, R645. (Page 41)-* Follow 17" AMD circuit change.
28. Add C262, C263. (Page 41)-* For Small/B design change.
29. Chagne C1175 type B2 ->Y. (Page 18)-* For fixed ME issue.
30. Add C264. (Page 22)-* For IDT request.
31. Add L85, L86, L87, L88. (Page 22)-* For EMI/ESD recommand.

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LA-4112P Rev0.3 -> 1.0 Product Improvement Record (P.I.R.)

Circuit change list:

1. Reserve R59, R60, R61.(Page 6)-* AMD suggest to reserve the pull high/down resistor of these test pin.
2. Add C477 0.1UF. (Page 23)-* For EMI recommand.
3. Change R906 from 0 ohm to 1k ohm. (Page 36)-* For reduce MIC background noise issue.
4. Change SMB DA1/CK1 pull high power rail from +3VALW to +3VL. (Page 40)-* EC recommand & follow Riply change list.
5. Add C819 0.1UF & D31 ESD diode. (Page 41)-* For EMI recommand.
6. Add R414 & R415 0 ohm. (Page 43)-* no support DIM function.
8. Add R140 & R234 750k ohm. (Page 43)-* Solve Rds on issue.

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