

Compal confidential

Schematics Document

Mobile Yonah uFCPGA with Intel Calistoga_GM/PM+ICH7-M core logic

2006-05-19

REV:0.1



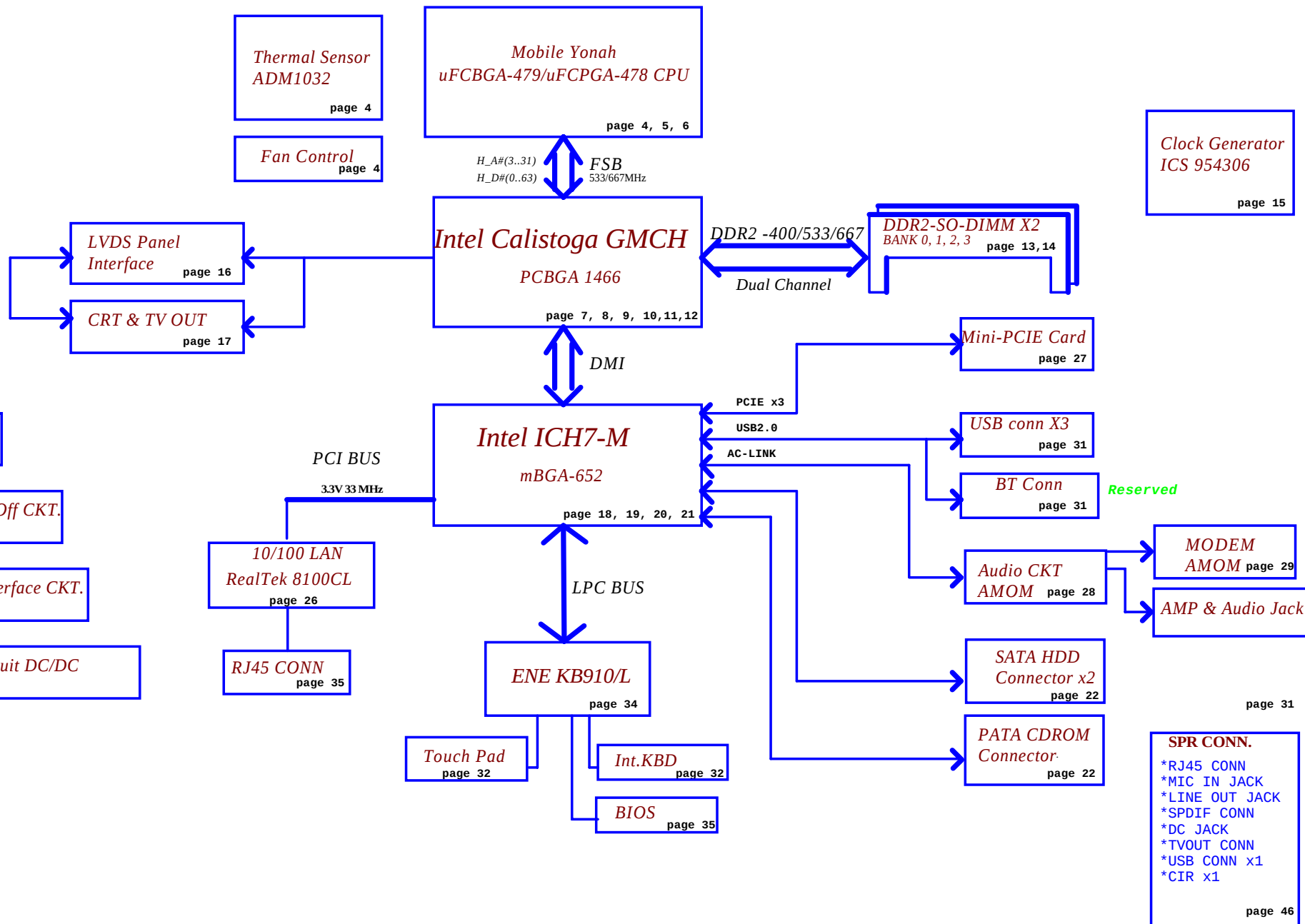
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Voltage Rails

power plane State	+B LD03 LD05	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.5VS +0.9VS +CPU_CORE +VCCP
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

0 MEANS ON
X MEANS OFF

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS & 1394	AD22	2	C,D,E,G
RealTek 8100CL	AD24	1	E

Load BOM check item

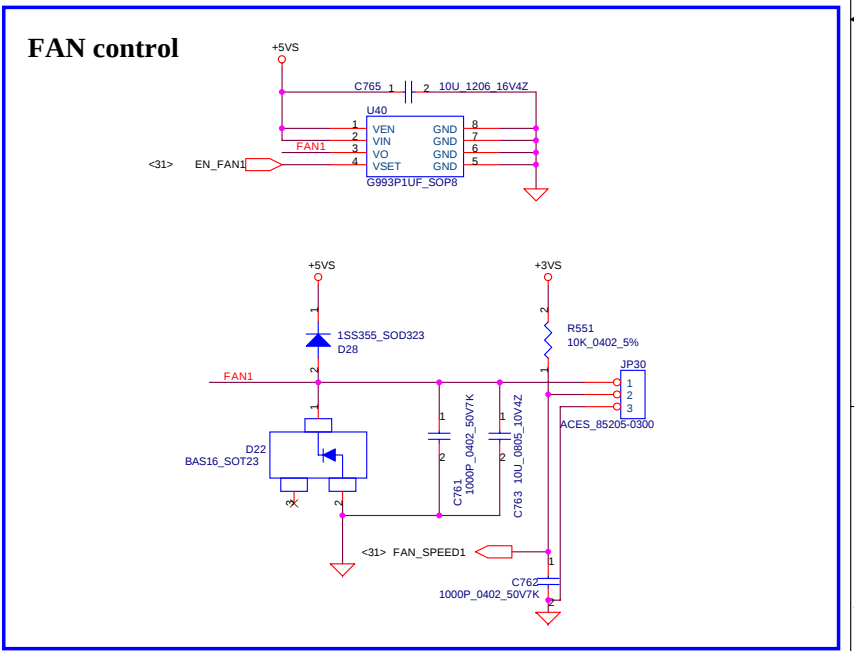
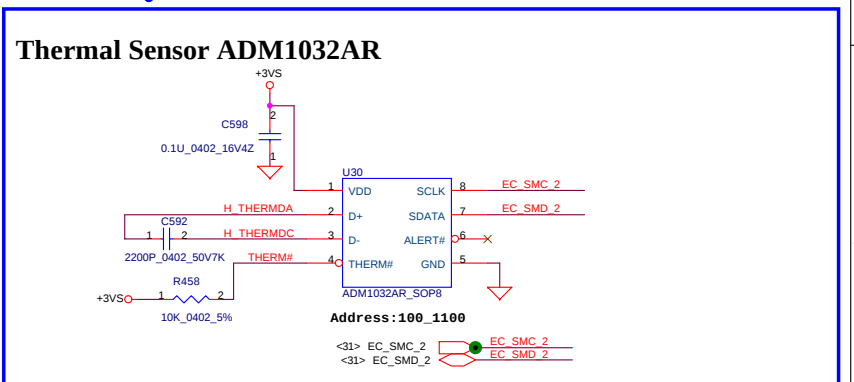
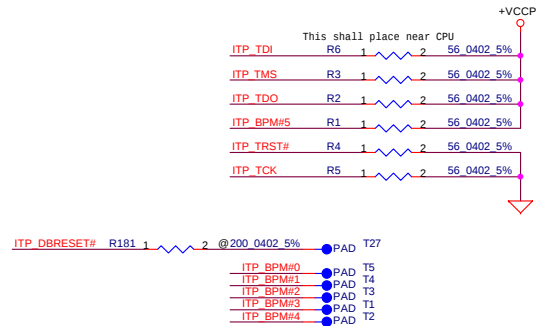
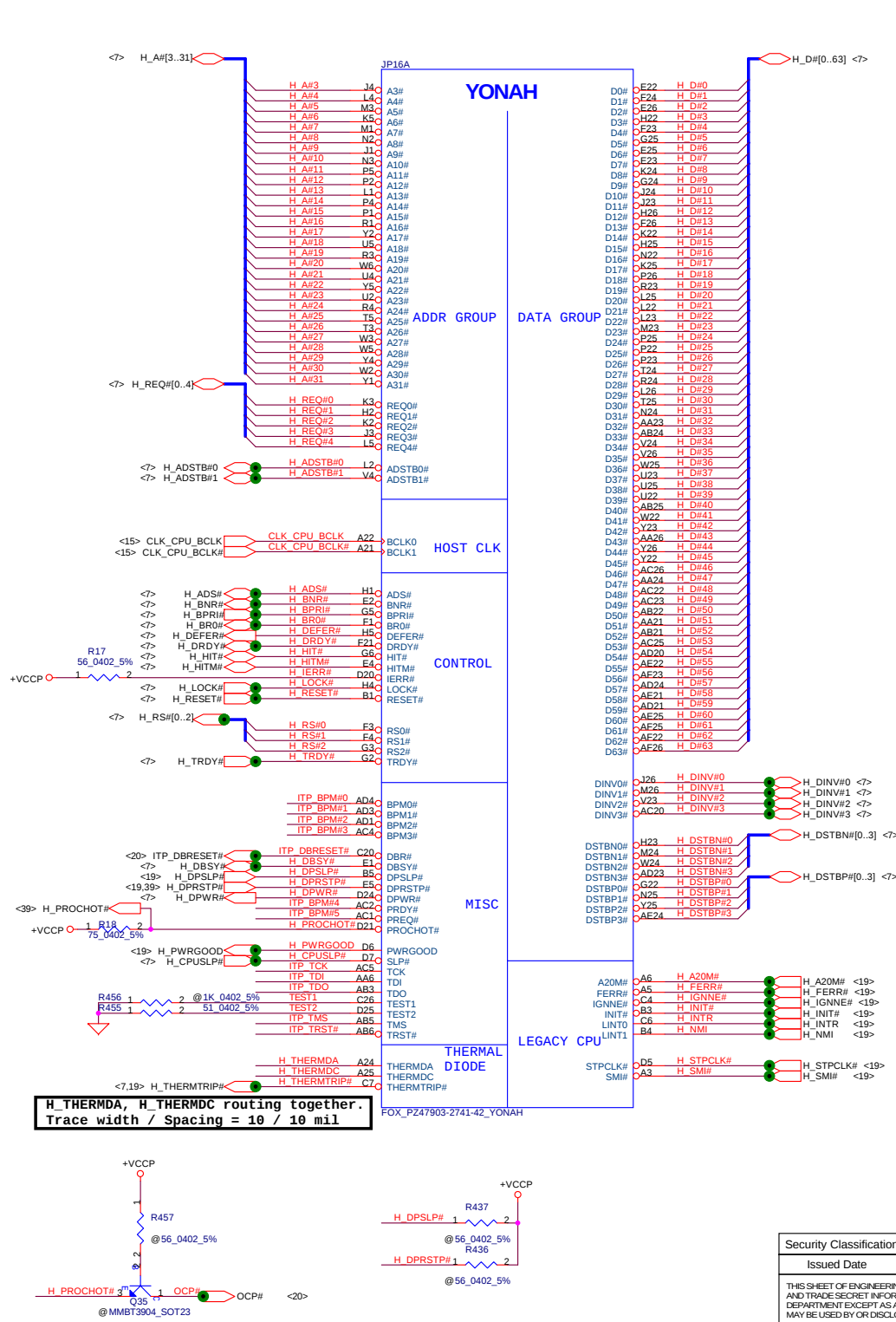
- 1.U31 GM/PM/GML part number
- 2.U6 ICH7 part number

BOM: 43144132L01 (GM)
43144132L02 (GML)

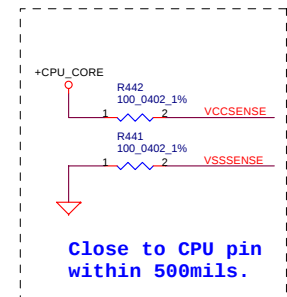
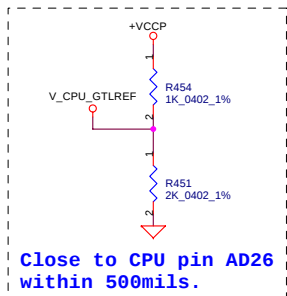
Jump-Short:

PJP4,PJP6,PJP7,PJP8,PJP10,PJP12,PJP14,PJP18,PJP19,PJP20,PJP25

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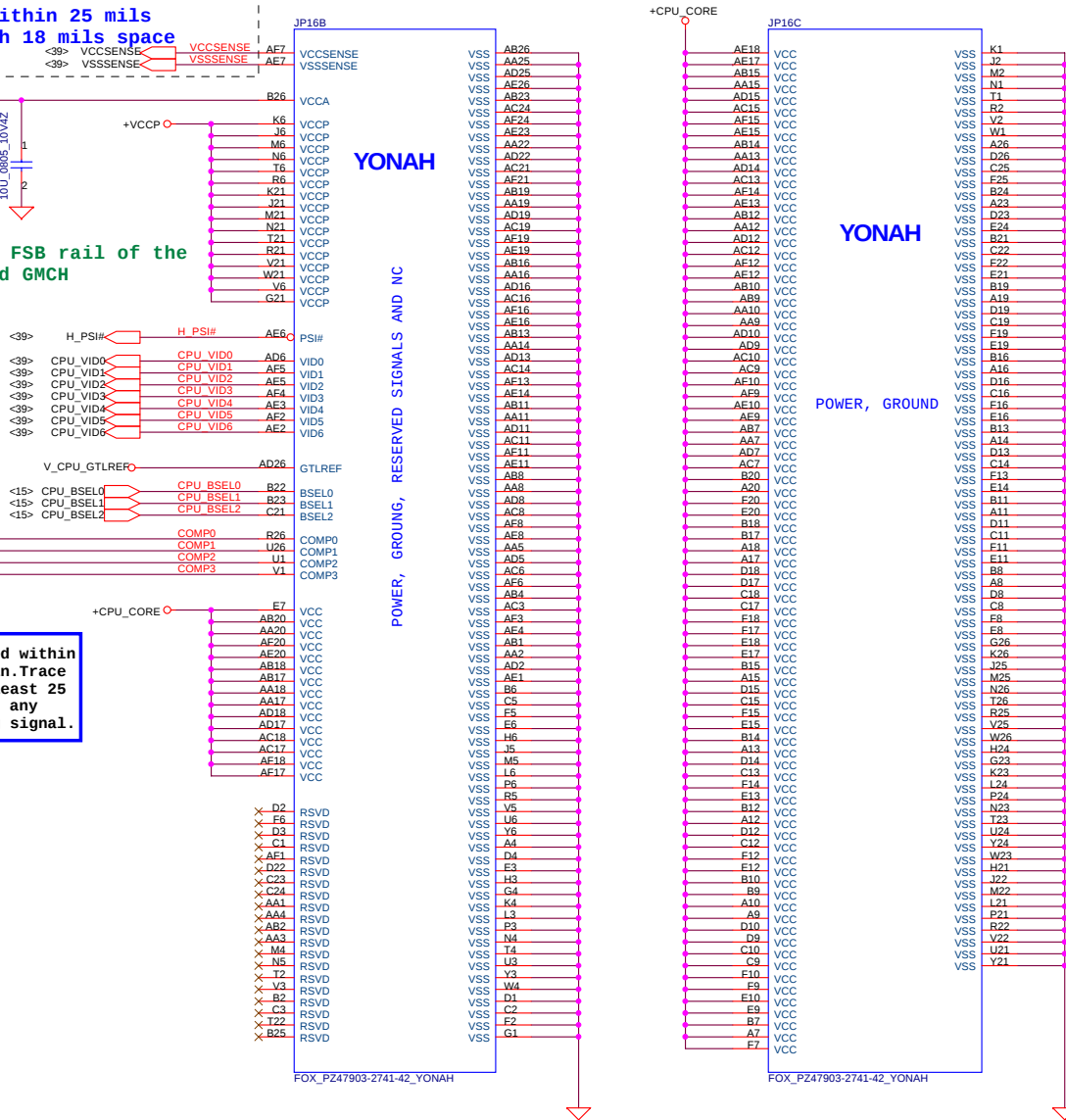
+1.5vs is a power source required by the PL clock generator on the processorsilicon

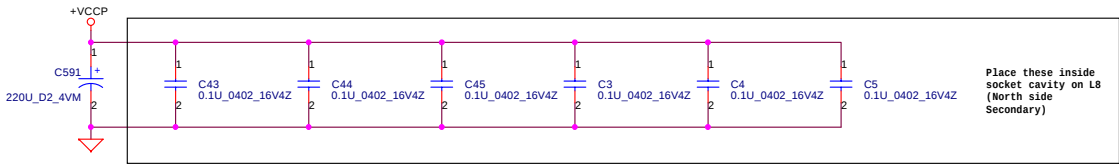
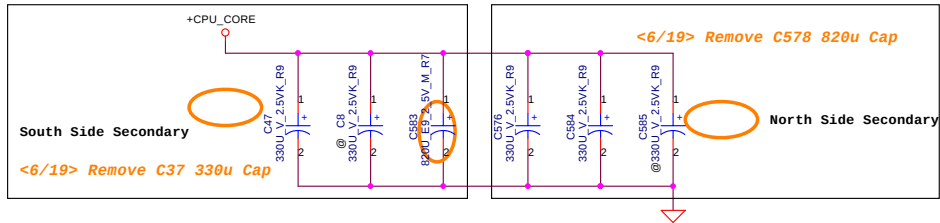
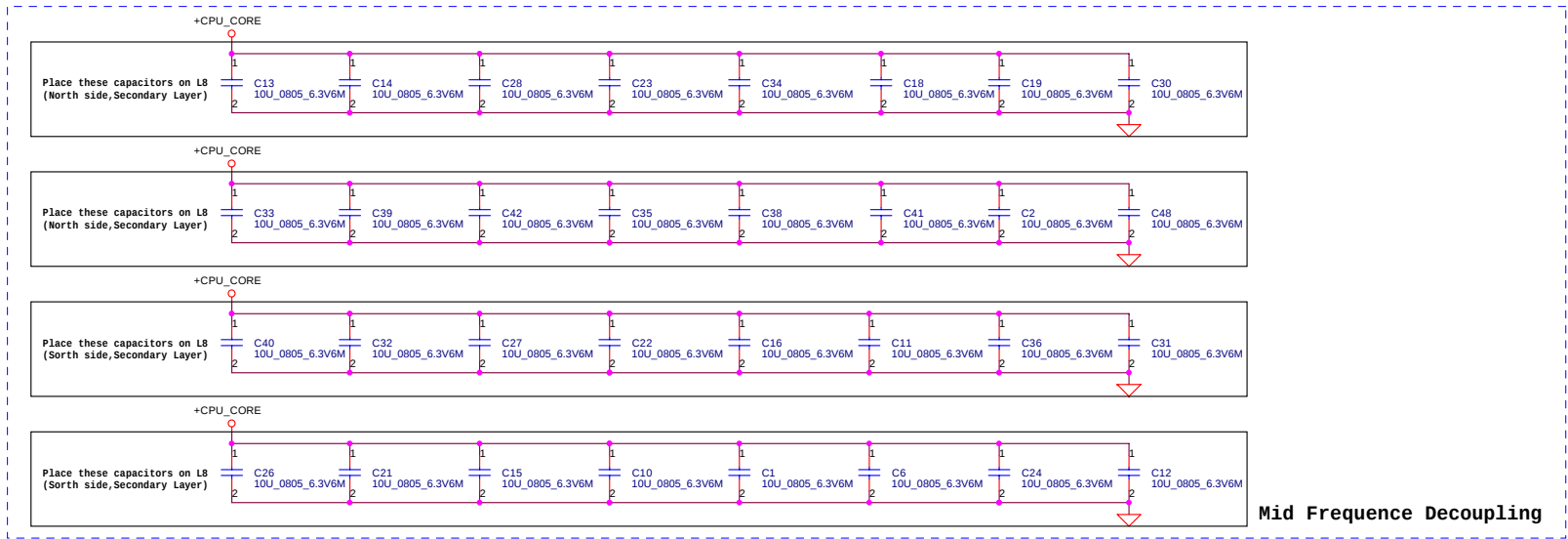
Length match within 25 mils
The trace width 18 mils space
7 mils

+VCCP is the FSB rail of the processor and GMCH

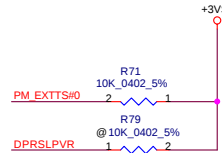
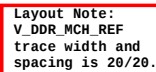
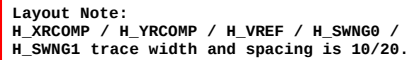
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal.

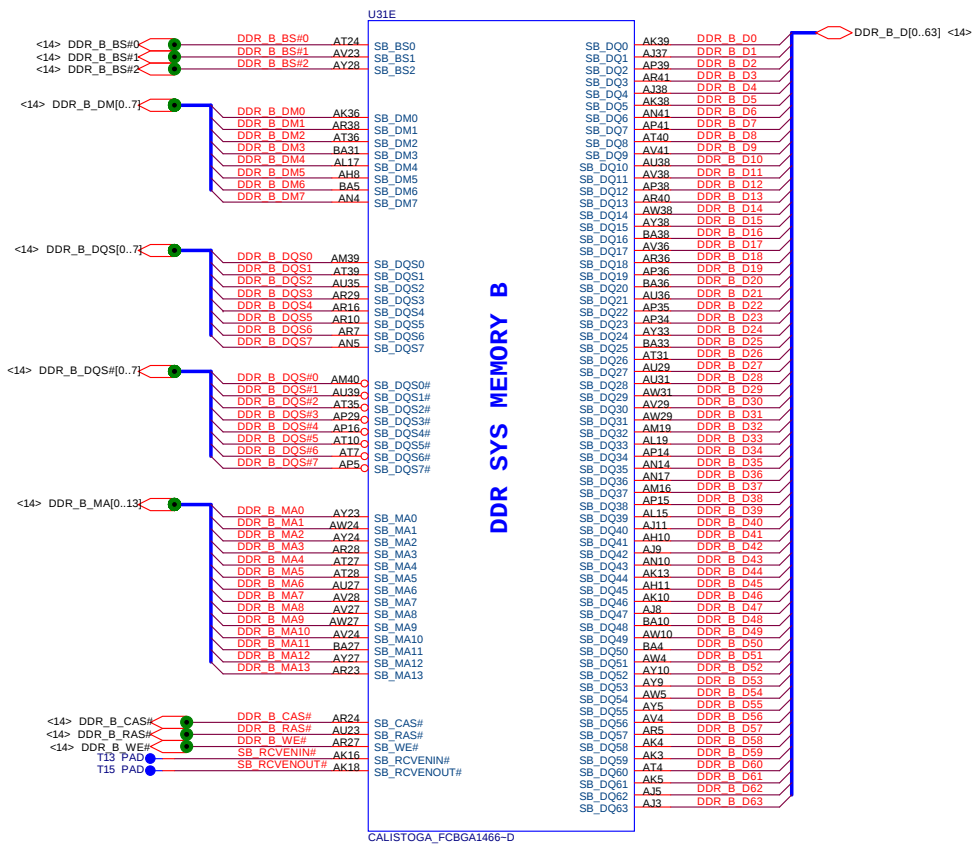
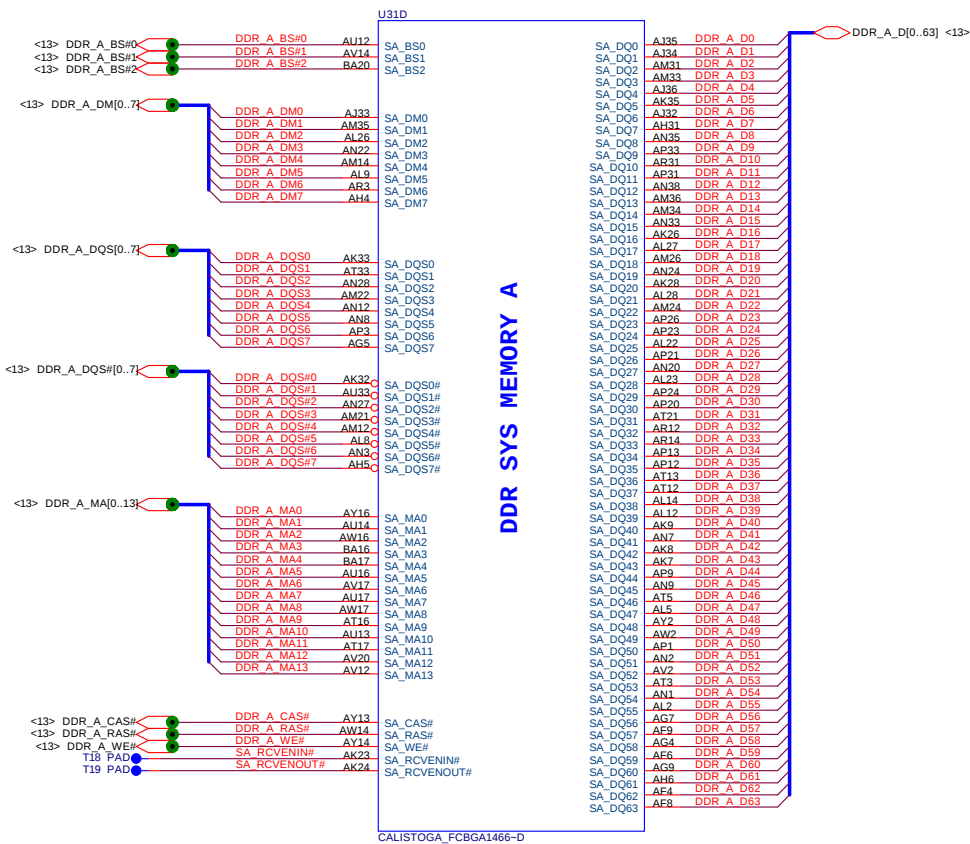




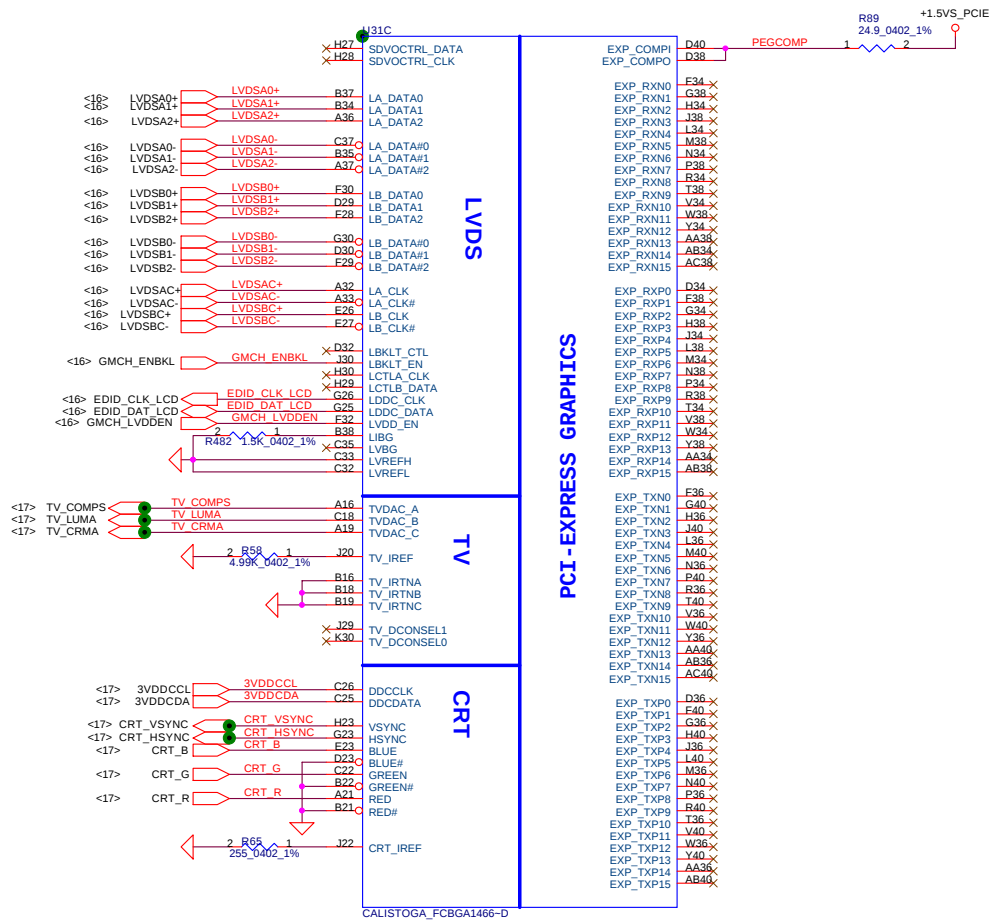
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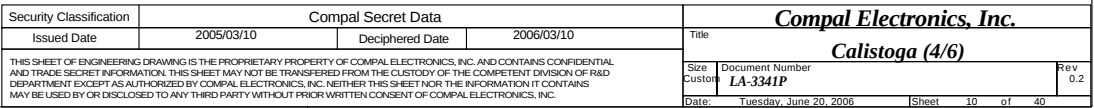
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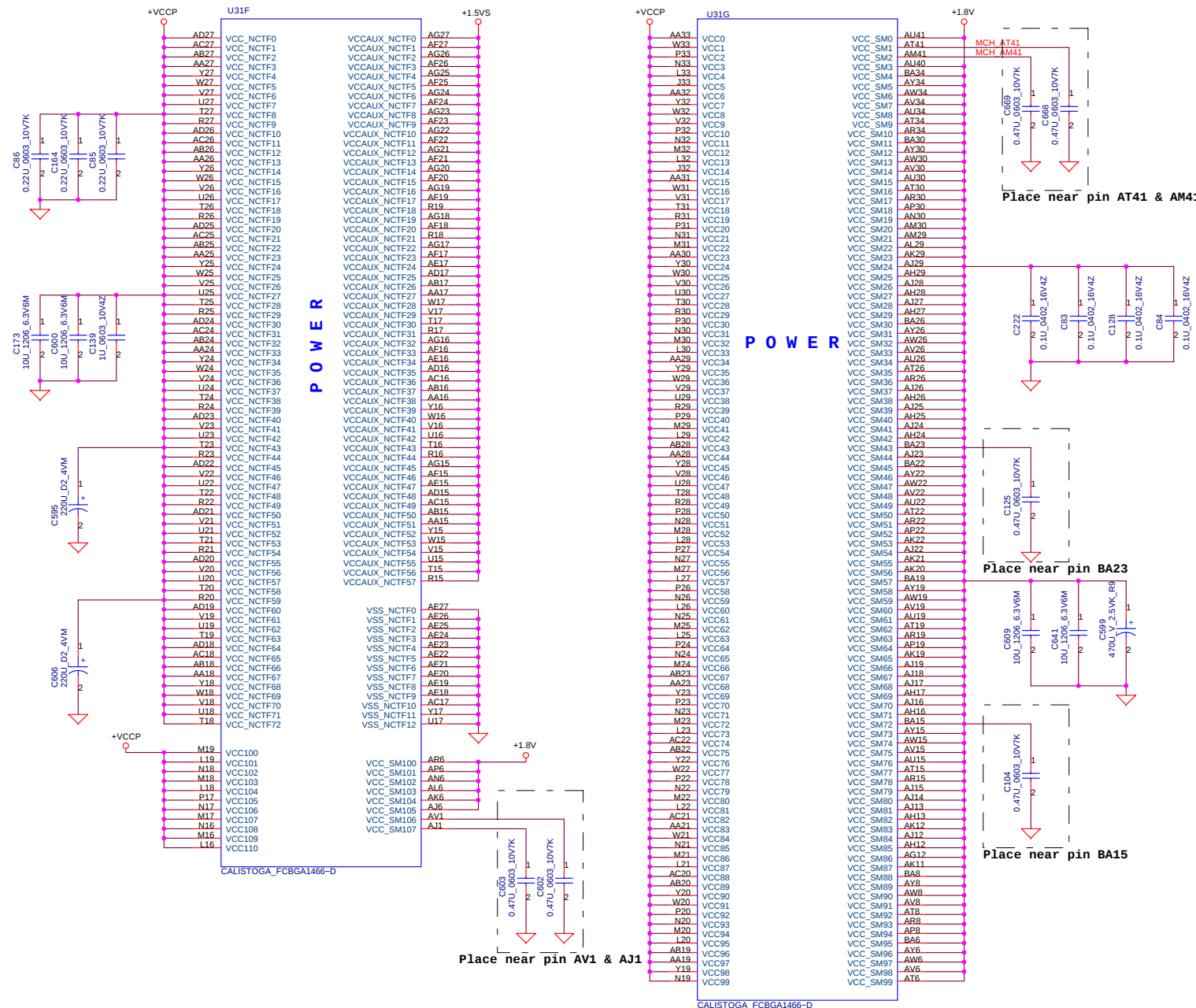
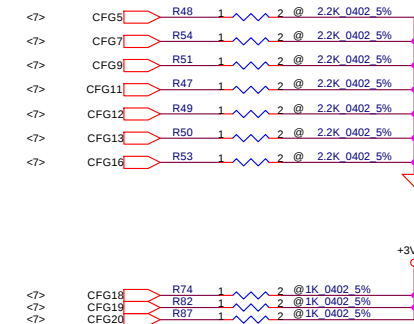
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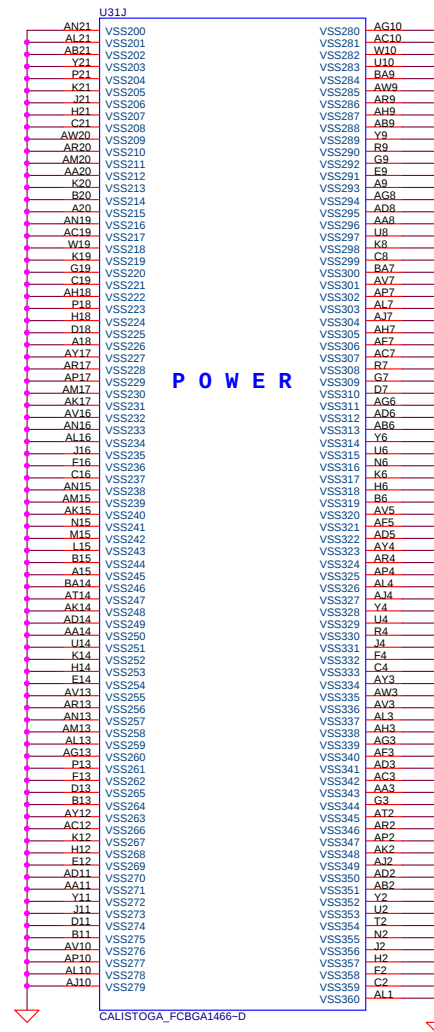
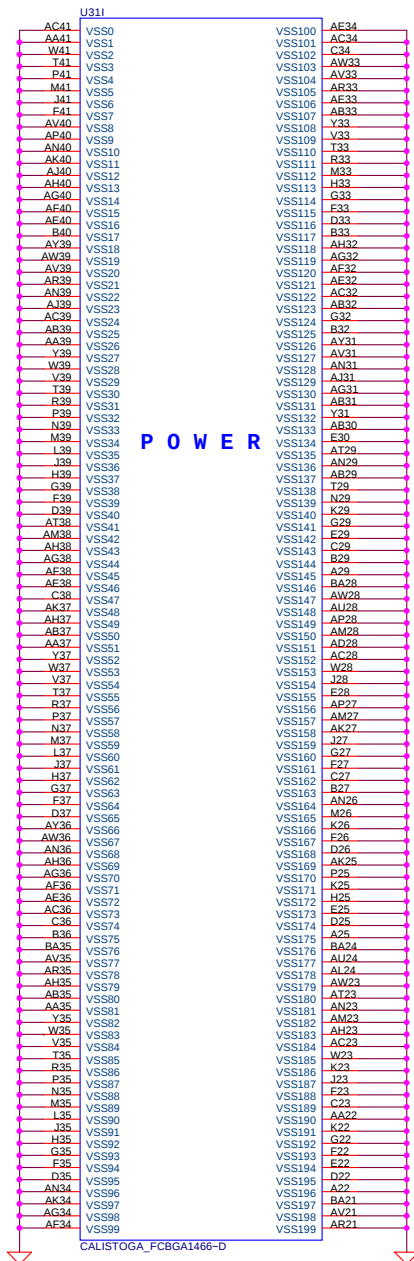
Strap Pin Table

CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

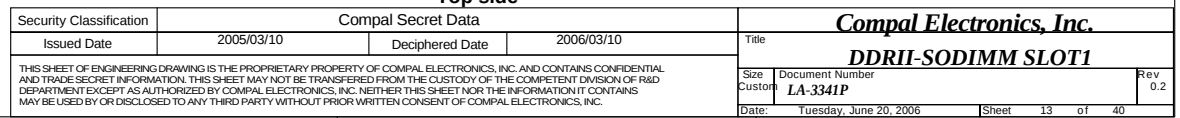
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V*(Default) 01 = 1.5V
CFG19	0 = No SDVO Device Present *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



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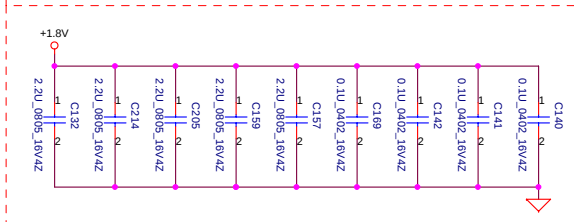


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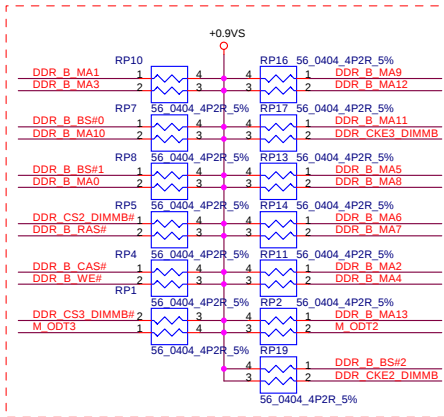
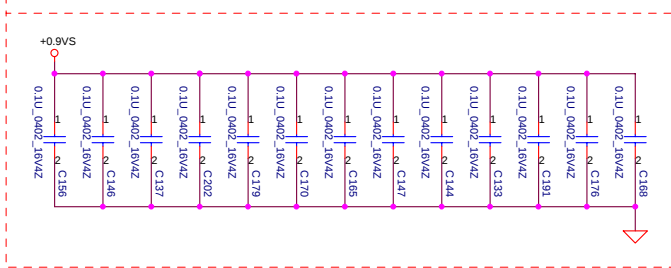


<> DDR_B_DQS#[0..7] <>
 <> DDR_B_D[0..63] <>
 <> DDR_B_DM[0..7] <>
 <> DDR_B_DQS[0..7] <>
 <> DDR_B_MA[0..13] <>

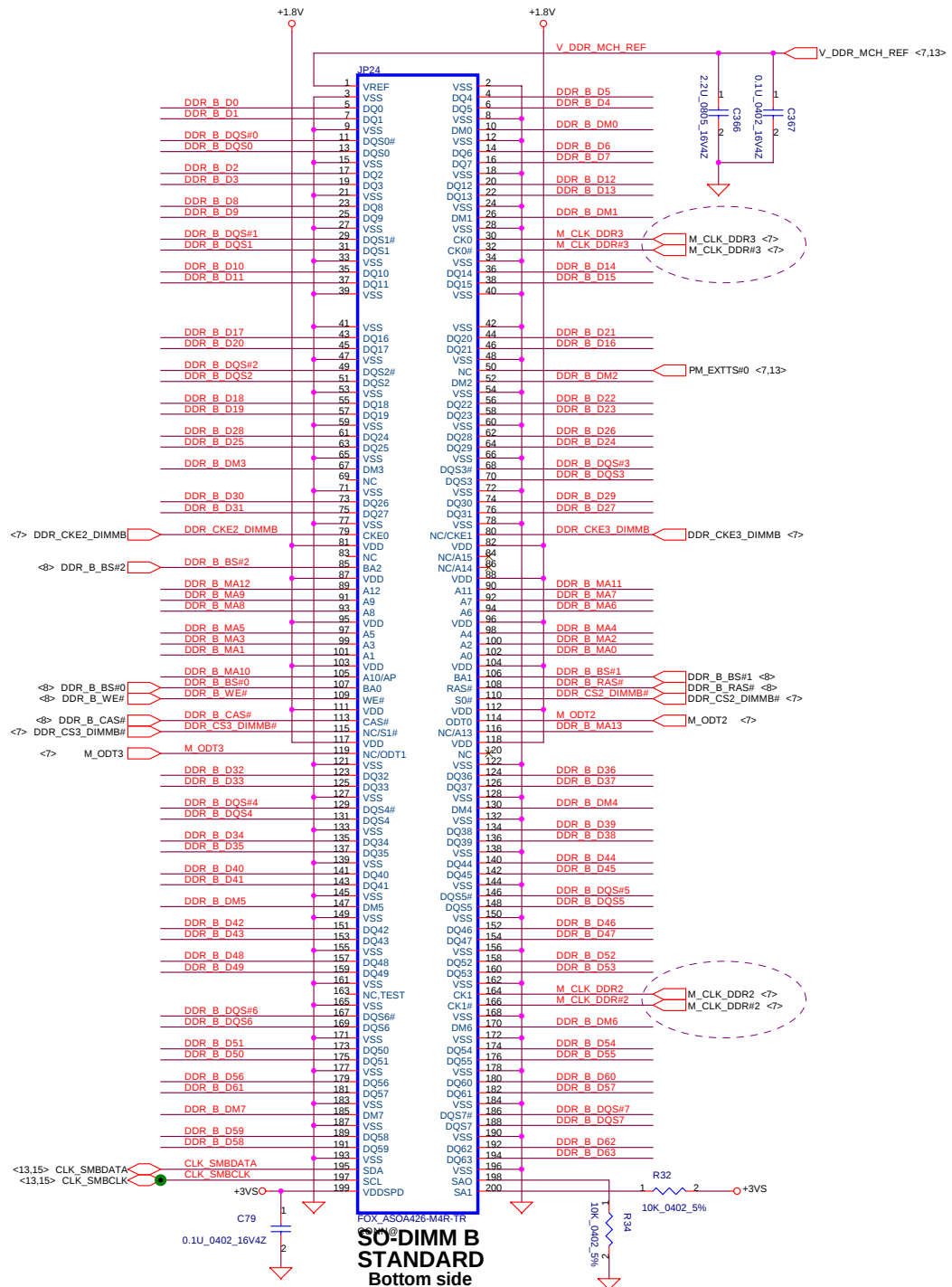
Layout Note:
 Place near JP42



Layout Note:
 Place one cap close to every 2 pullup resistors terminated to +0.9VS

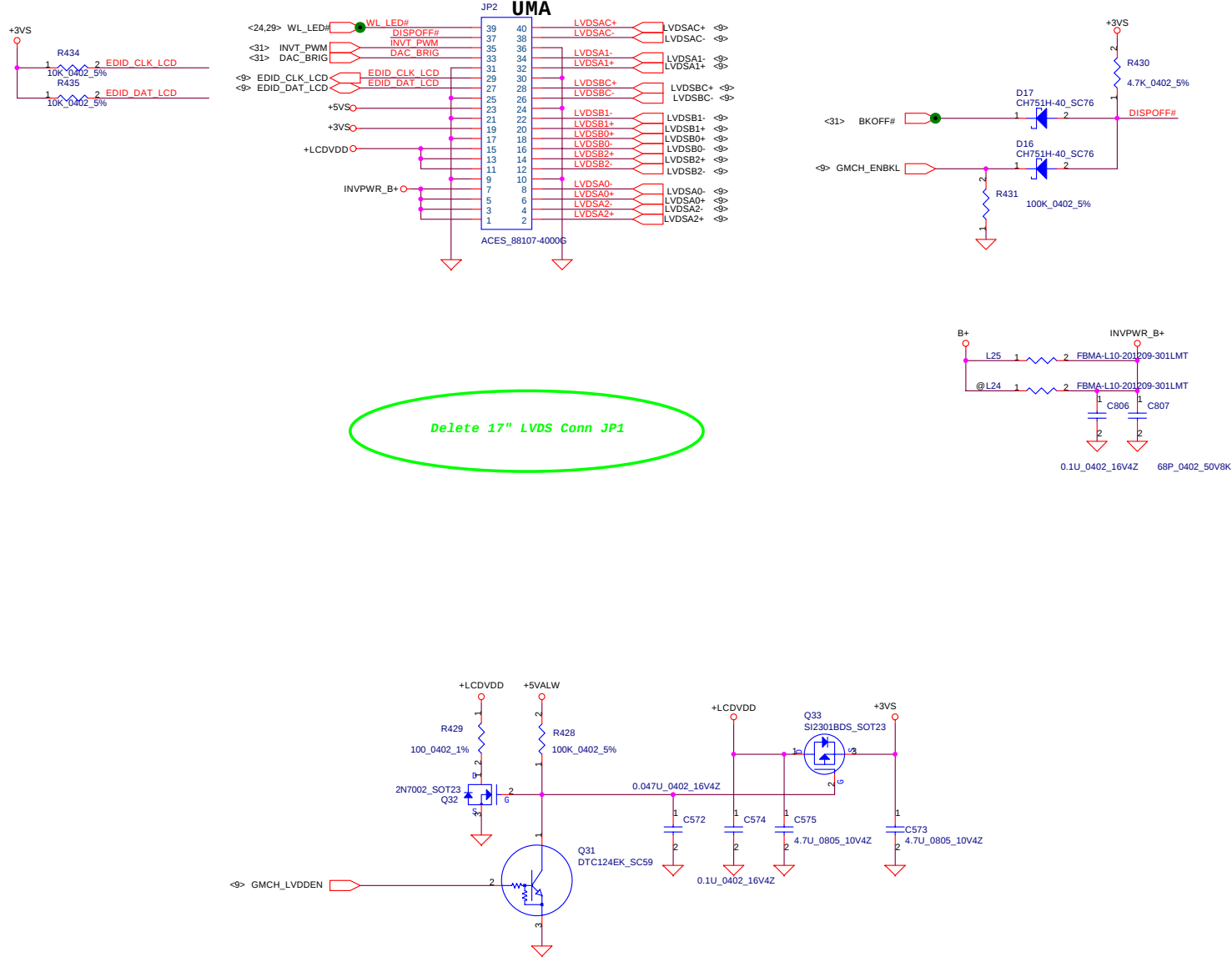


Layout Note:
 Place these resistor closely JP42, all trace length Max=1.5"

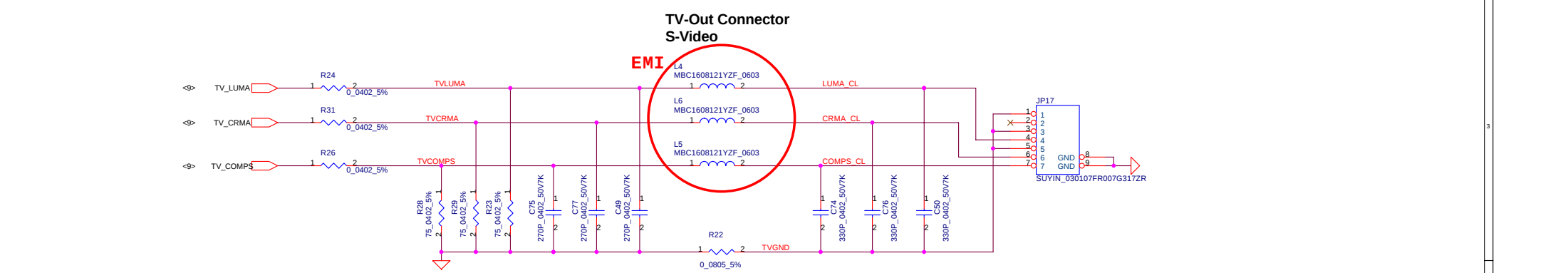
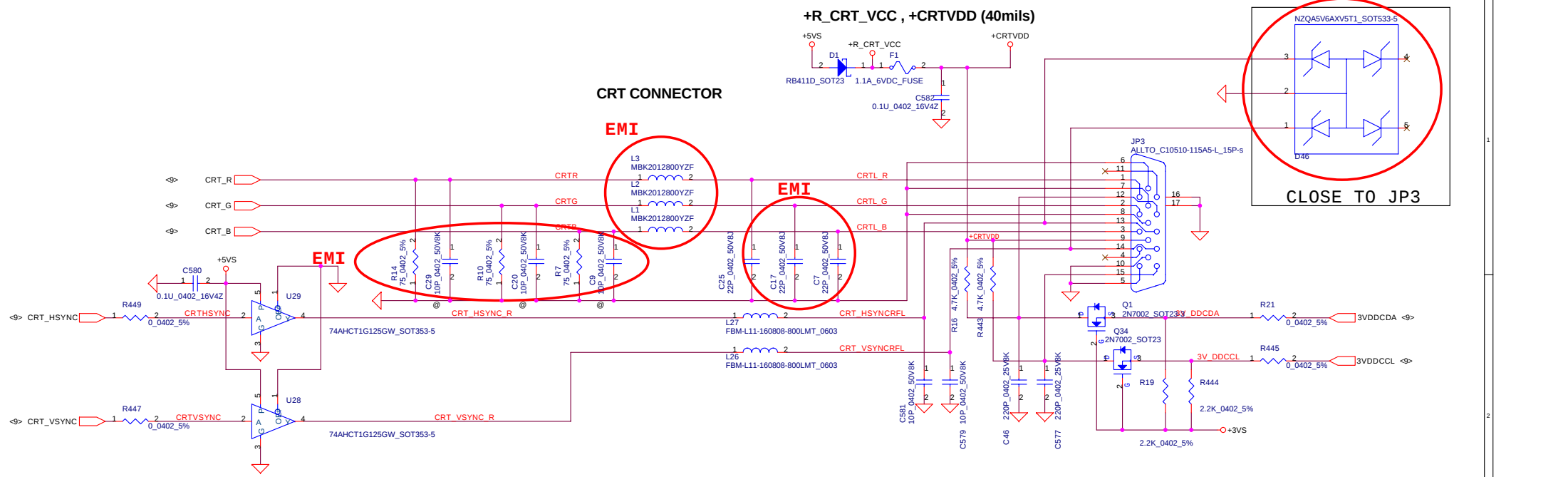


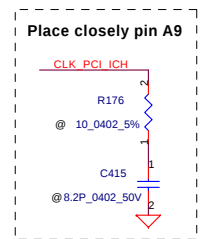
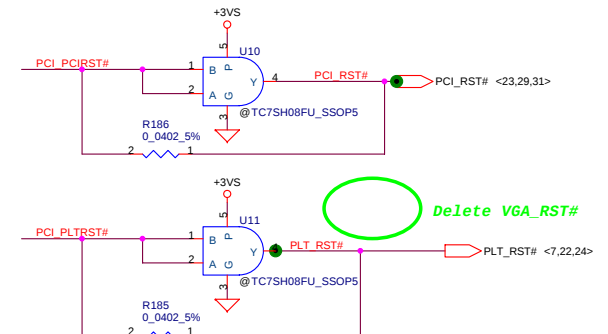
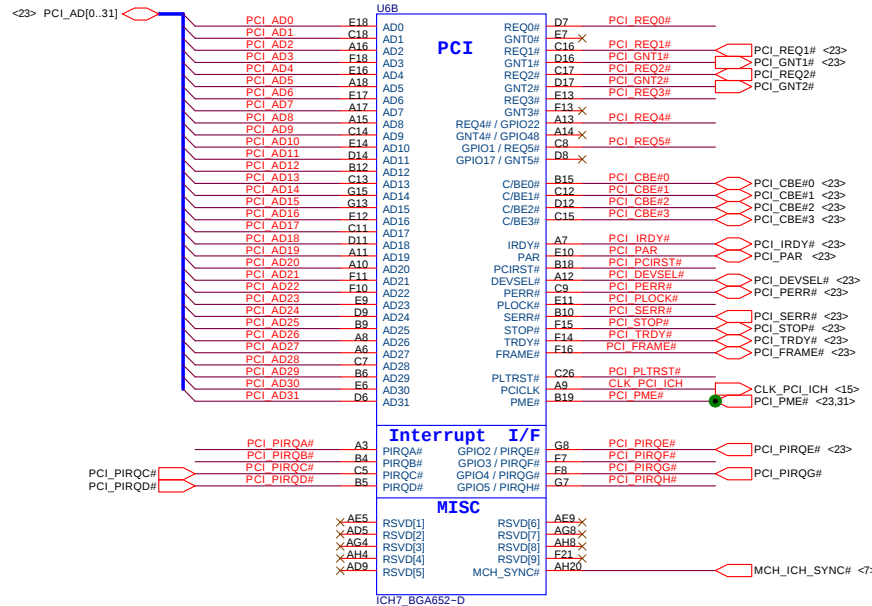
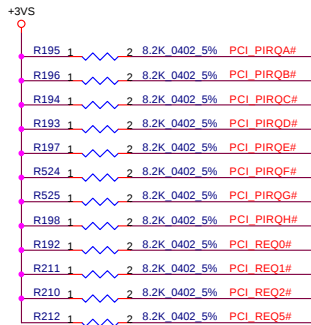
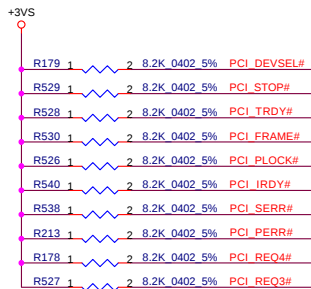
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LCD Panel & inverter Connector

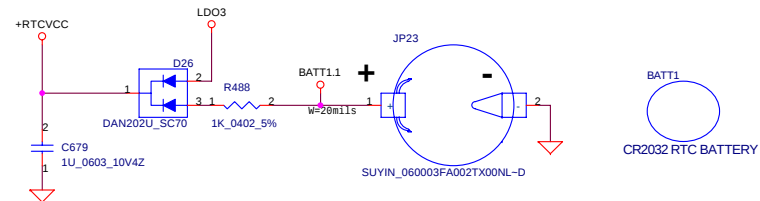


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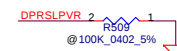




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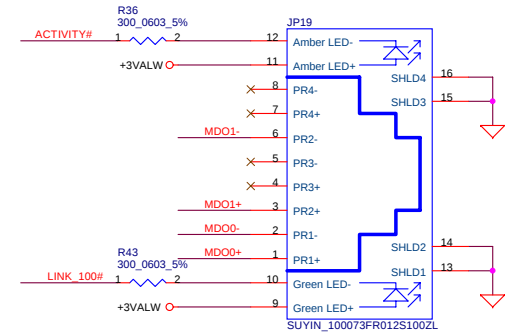
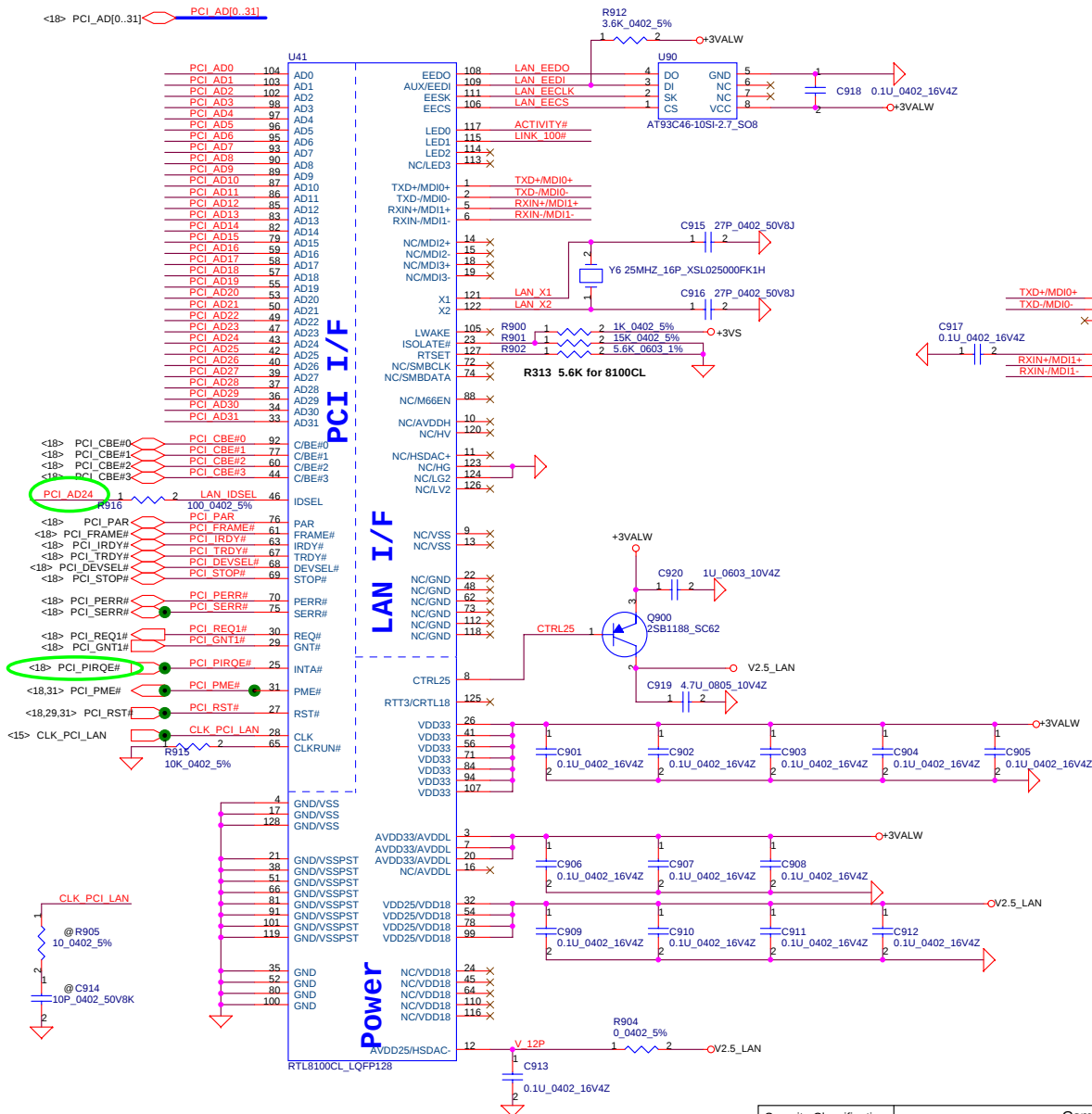


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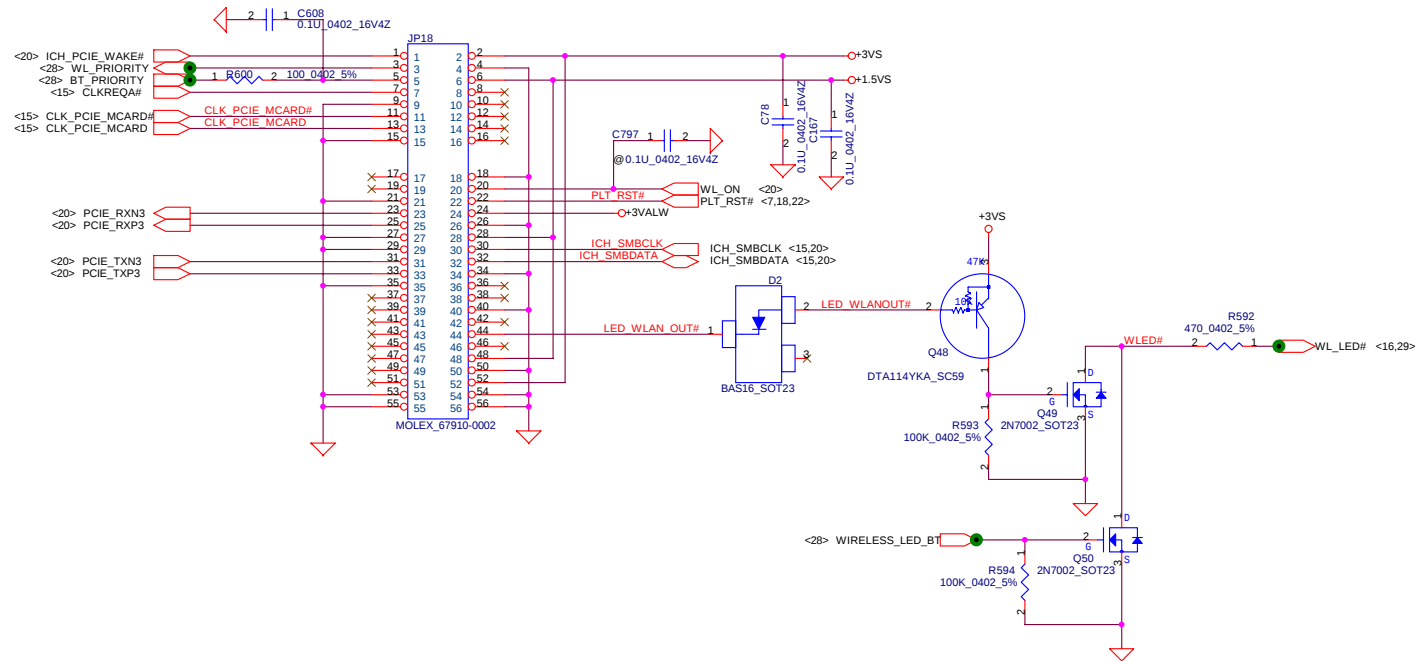
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Mini-Express Card(Slot 1-WLAN)



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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Mini Card	
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				Date	Tuesday, June 20, 2006
				Sheet	24 of 40
				Rev	0.2

<6/12> Remove PCM_SPK

For Layout:

Place decoupling caps near the power pins of SmartAMC device.

Delete CD traces

<6/12> Remove Docking line out

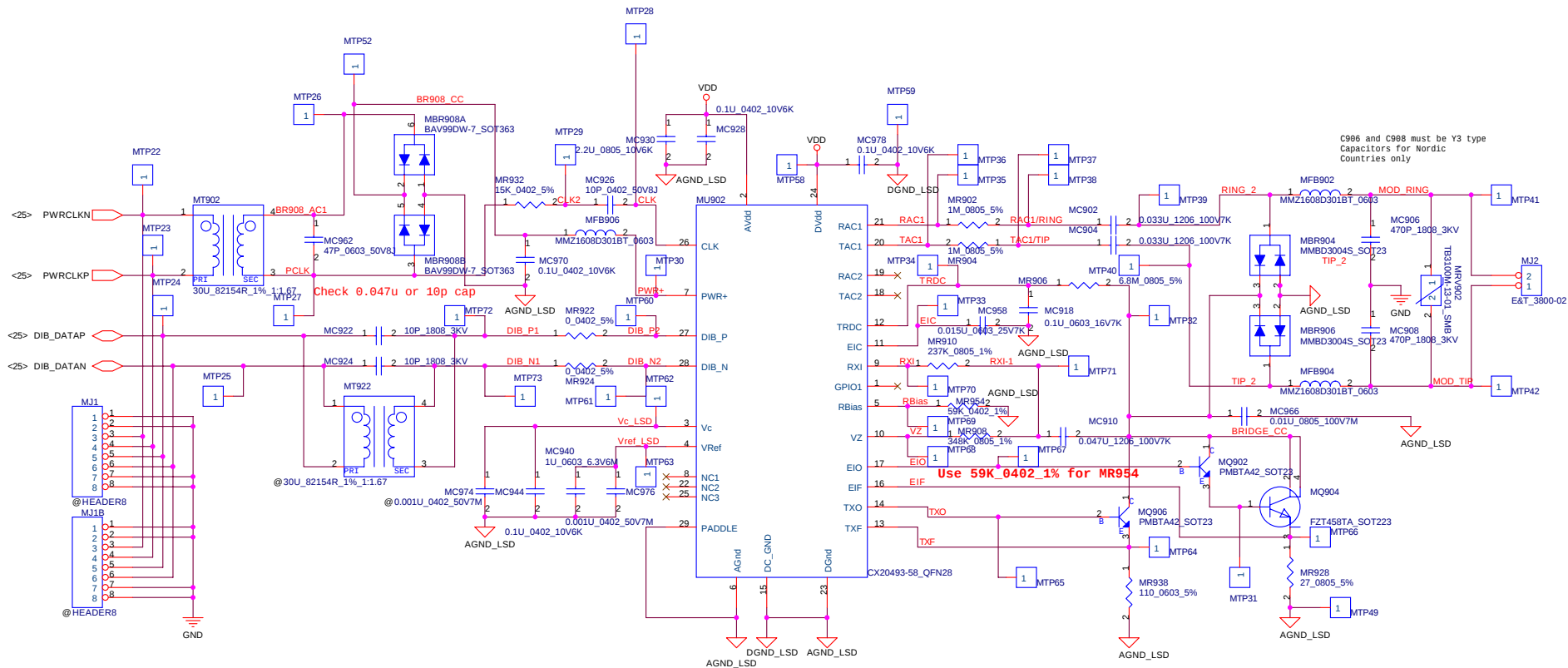
<6/12> Remove Docking MIC

<6/12> Remove JACK_DET from Docking

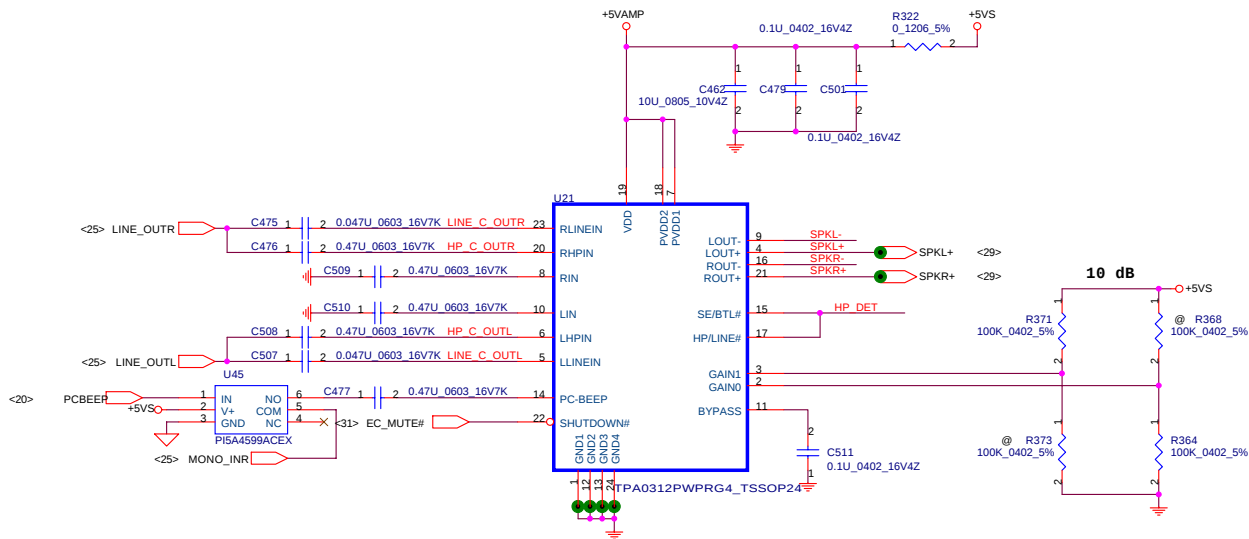
HP_DET#	JACK_DET#	PORT-A	PORT-B	EQ
0	0	ON	OFF	Disable
0	NC	ON	OFF	Disable
NC	0	OFF	ON	Disable
NC	NC	ON	OFF	Enable

MIC_DET	PORT-C	PORT-F
0	ON	OFF
NC	OFF	ON

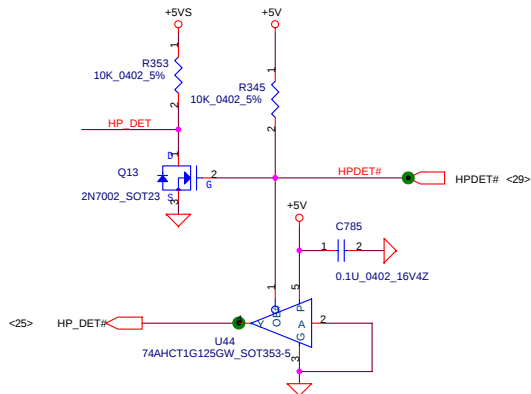
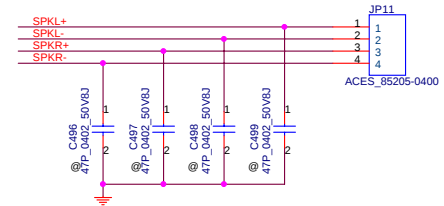
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title	AMOM_codec
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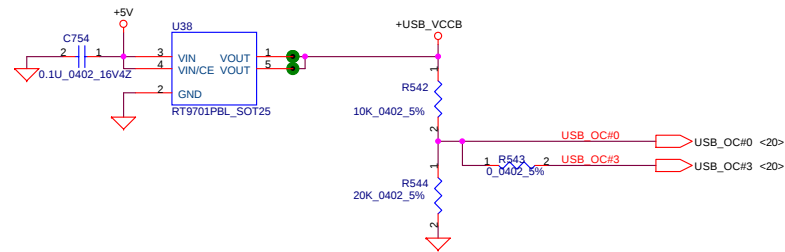
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title AMOM modem	
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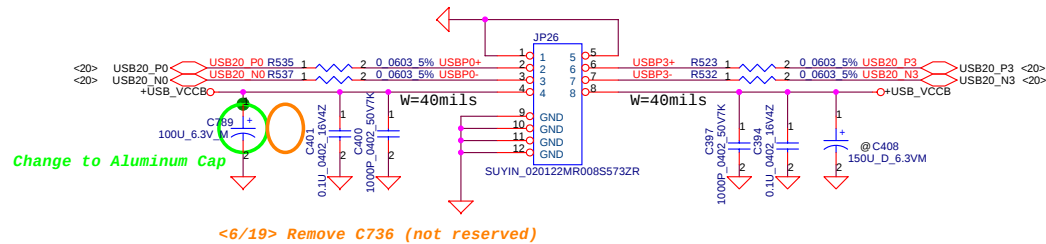
HEADPHONE OUT/LINE OUT			
GAIN0	GAIN1	SE/BTL#	Av(inv)
0	0	0	6 dB
0	1	0	* 10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB



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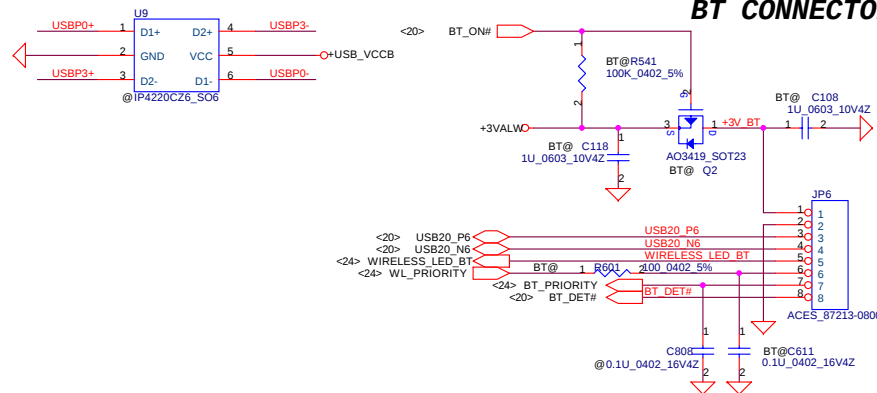


USB CONNECTOR (Left side)



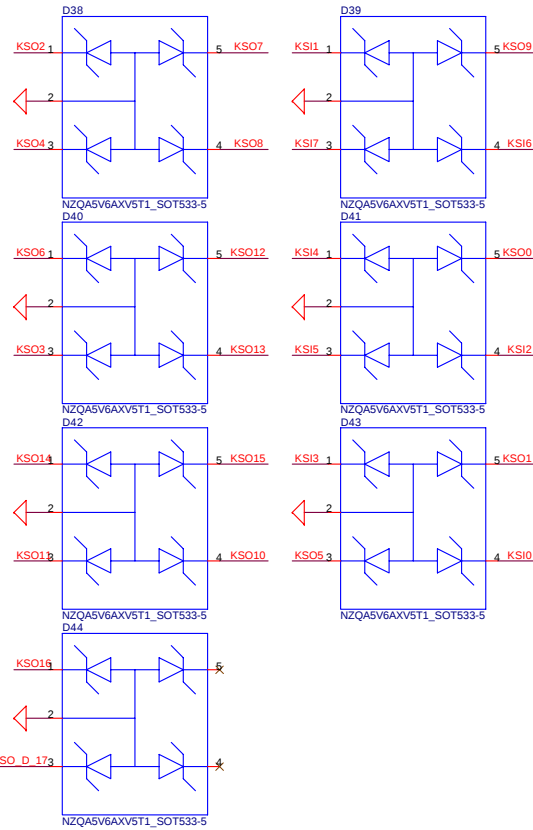
BT CONNECTOR

Reserve Bluetooth

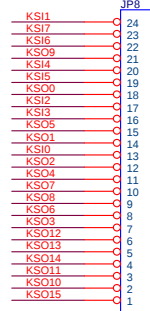


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KSI[0..7] <31>
KSO[0..16] <31>

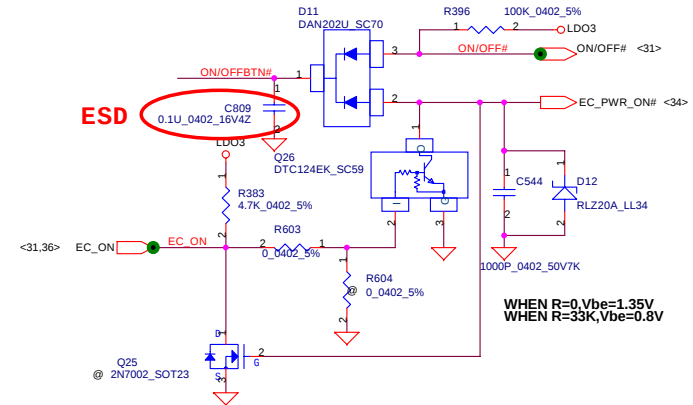


15.4 (TYPE "C" KB)

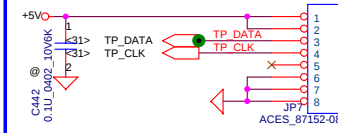


ACES_85201-2405

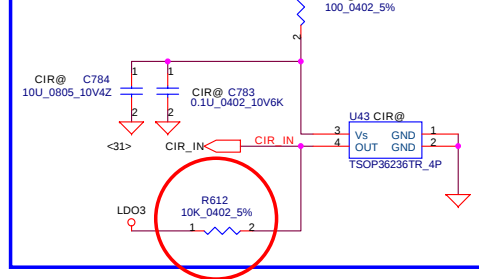
Power BTN



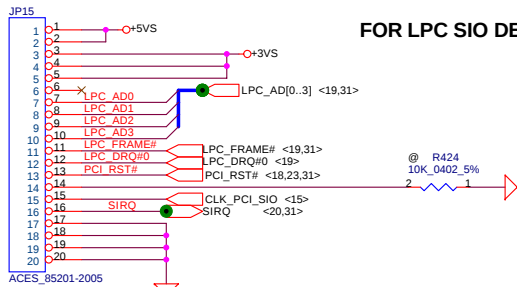
TP to MB CONN(15.4)



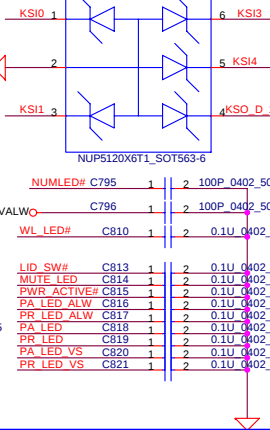
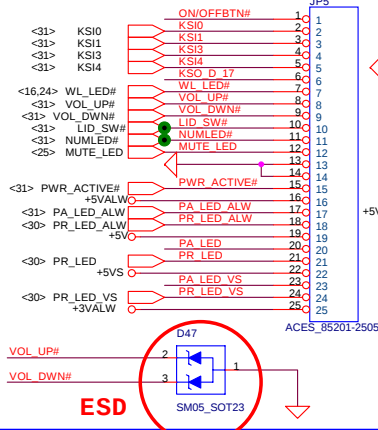
Consumer IR



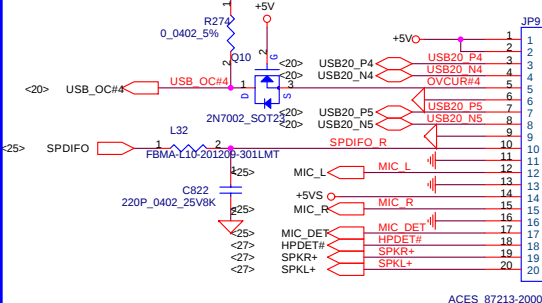
FOR LPC SIO DEBUG PORT



Switch board conn



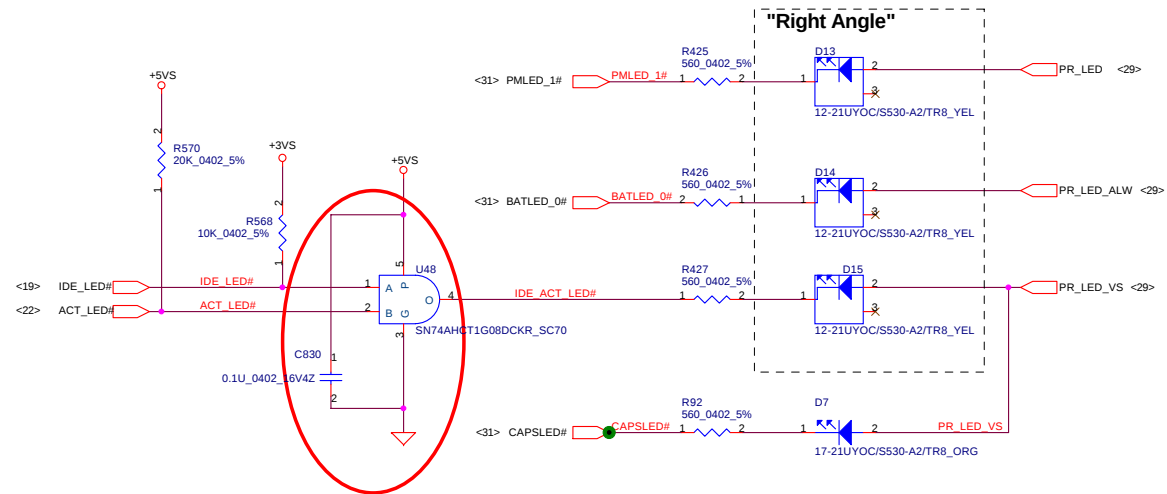
Audio board conn



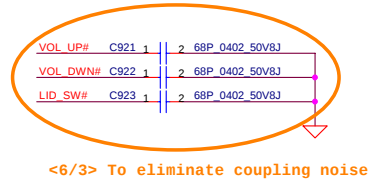
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Size	KB
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For PR

FOR POWER BUTTON BACKLIGHT SYSTEM POWER



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				Date:	Tuesday, June 20, 2006	Sheet 30 of 40



<6/3> To eliminate coupling noise

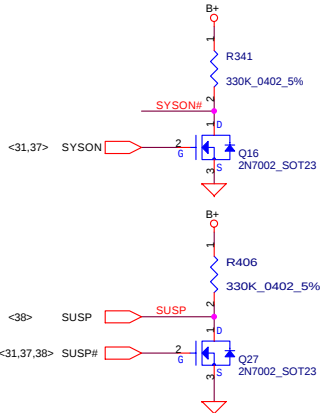
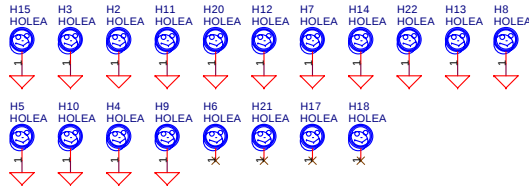
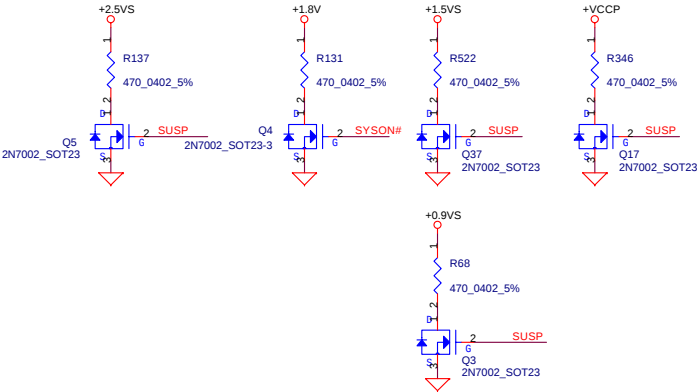
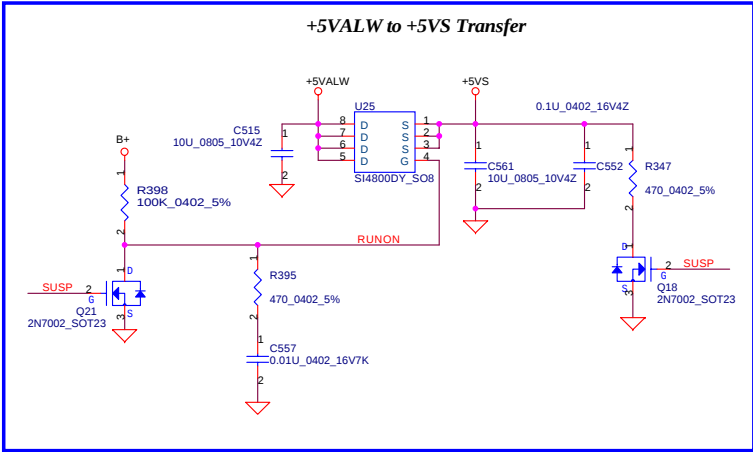
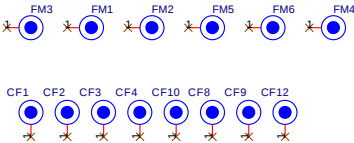
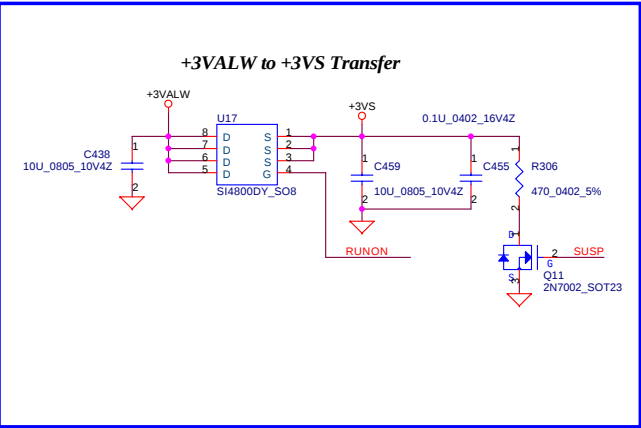
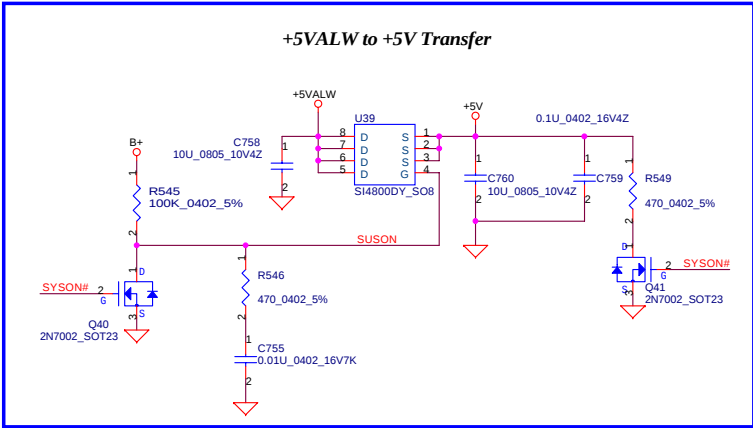
JP20

1	1
2	2
3	3
4	4

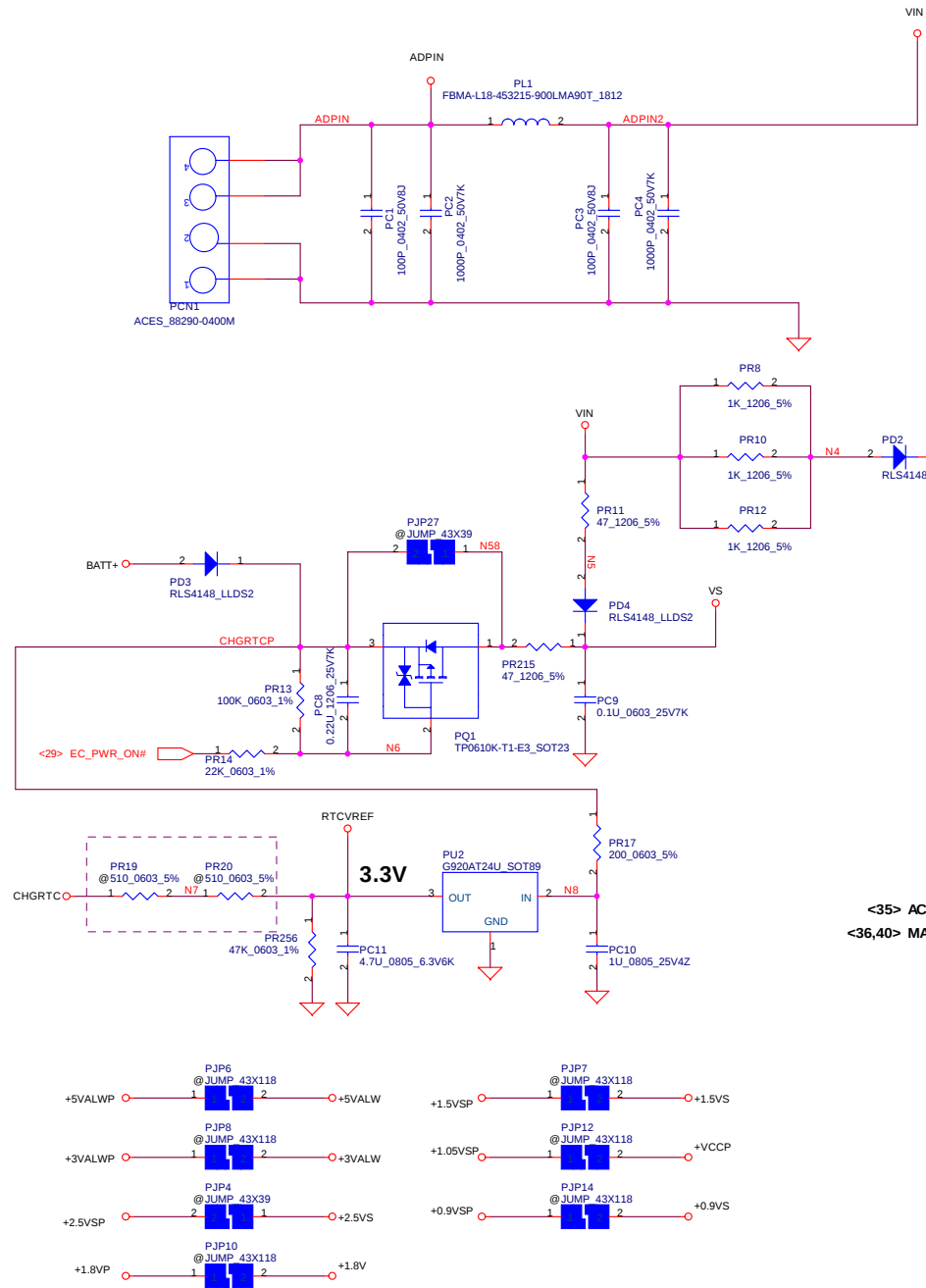
ACES 85205-0400

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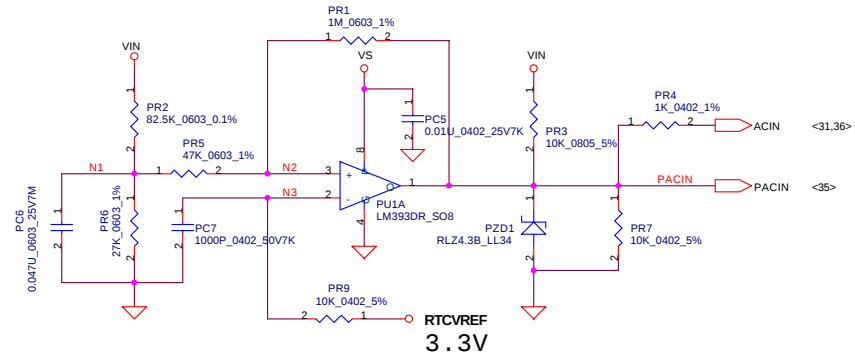
Security Classification				Compal Secret Data				Compal Electronics, Inc. BIOS & EC I/O Port			
Issued Date		2005/03/10		Deciphered Date		2006/03/10		Title		Rev	
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				Customer	LA-3341P
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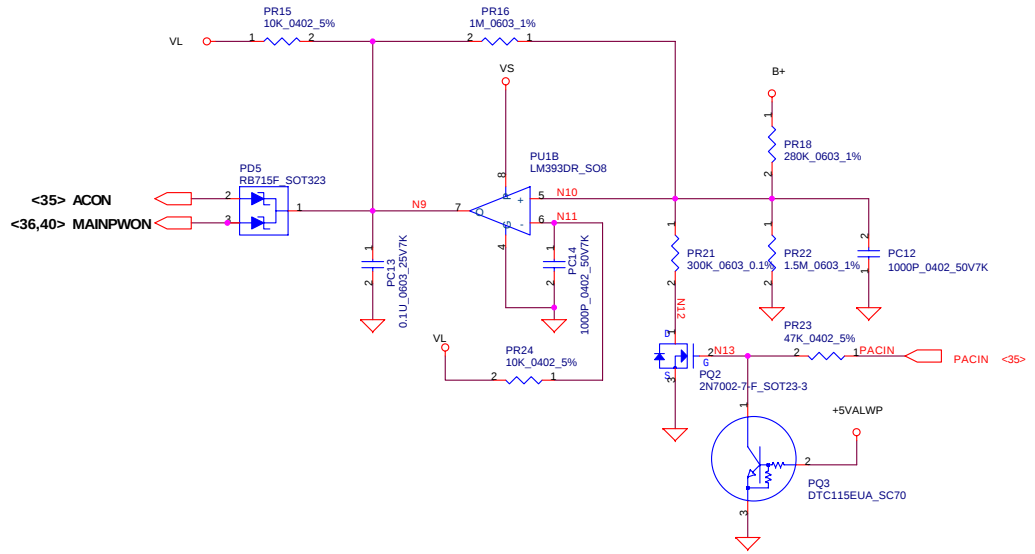


Vin Detector :			
14.698	14.285	13.879	
13.818	13.411	13.000	



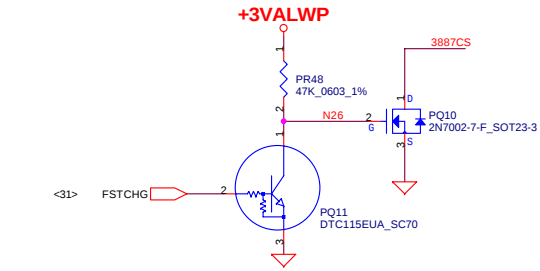
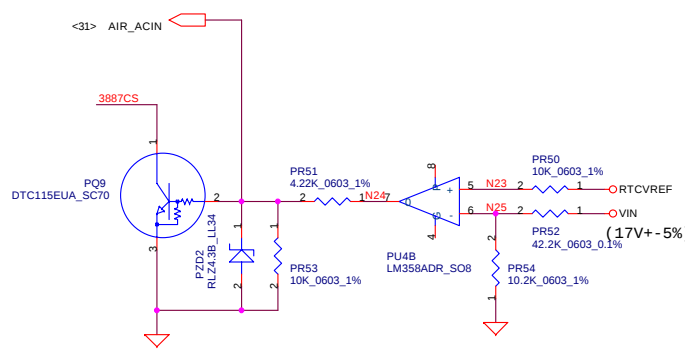
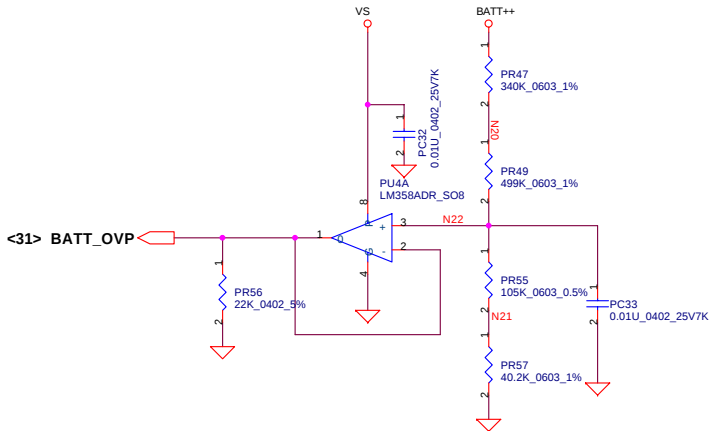
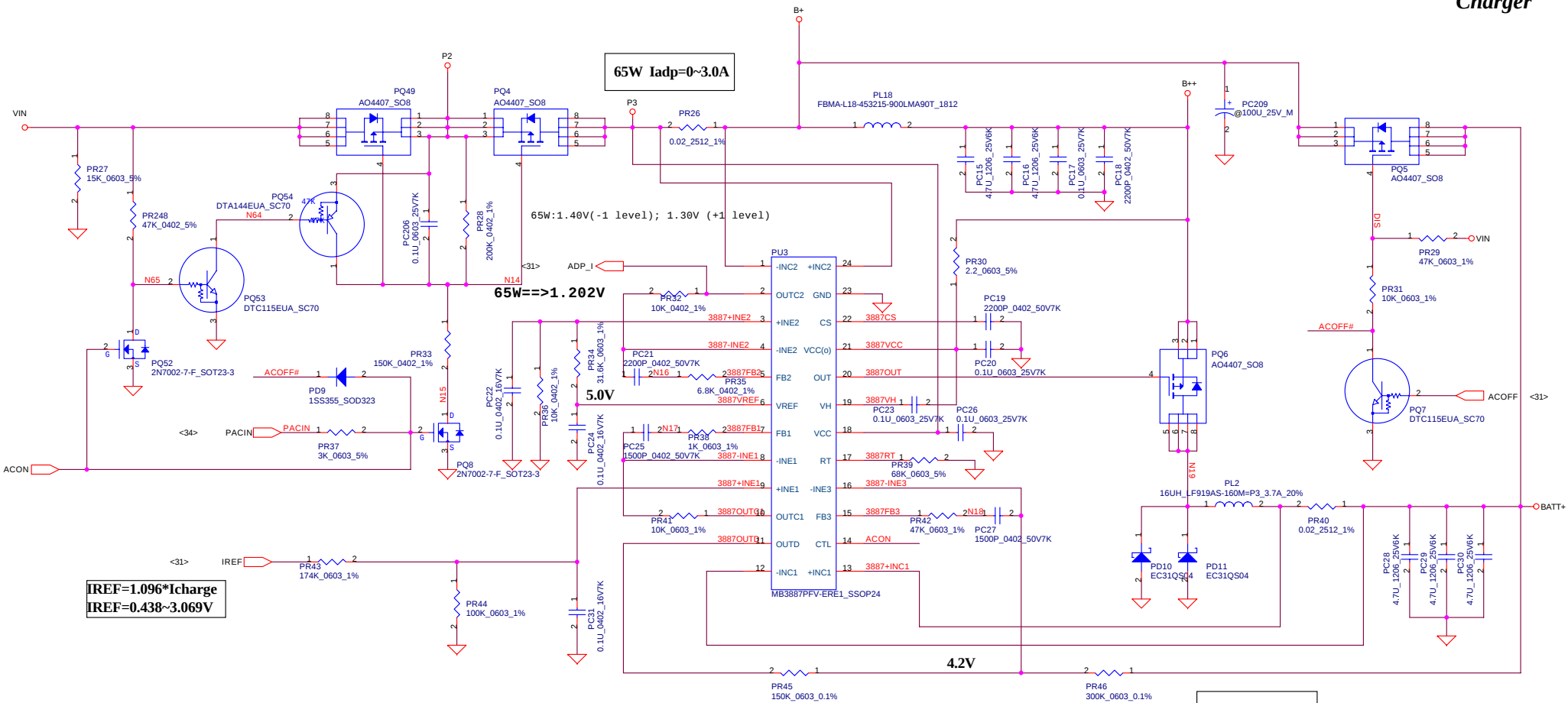
ACIN:			
Precharge detector			
12.384	12.000	11.624	
10.927	10.600	10.223	

BATT			
Precharge detector			
7.558	7.333	7.112	
6.108	5.933	5.704	



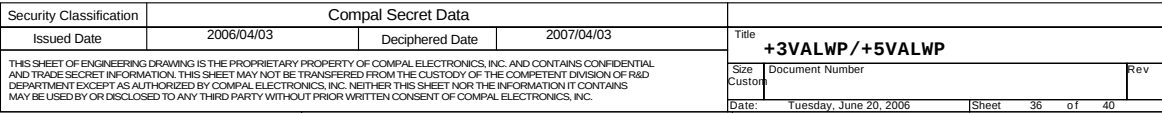
Security Classification		Compal Secret Data		Title		
Issued Date		2006/04/03	Deciphered Date	2007/04/03	Dectector / Precharge	
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				Customer		0.2
				Date:	Tuesday, June 20, 2006	Sheet

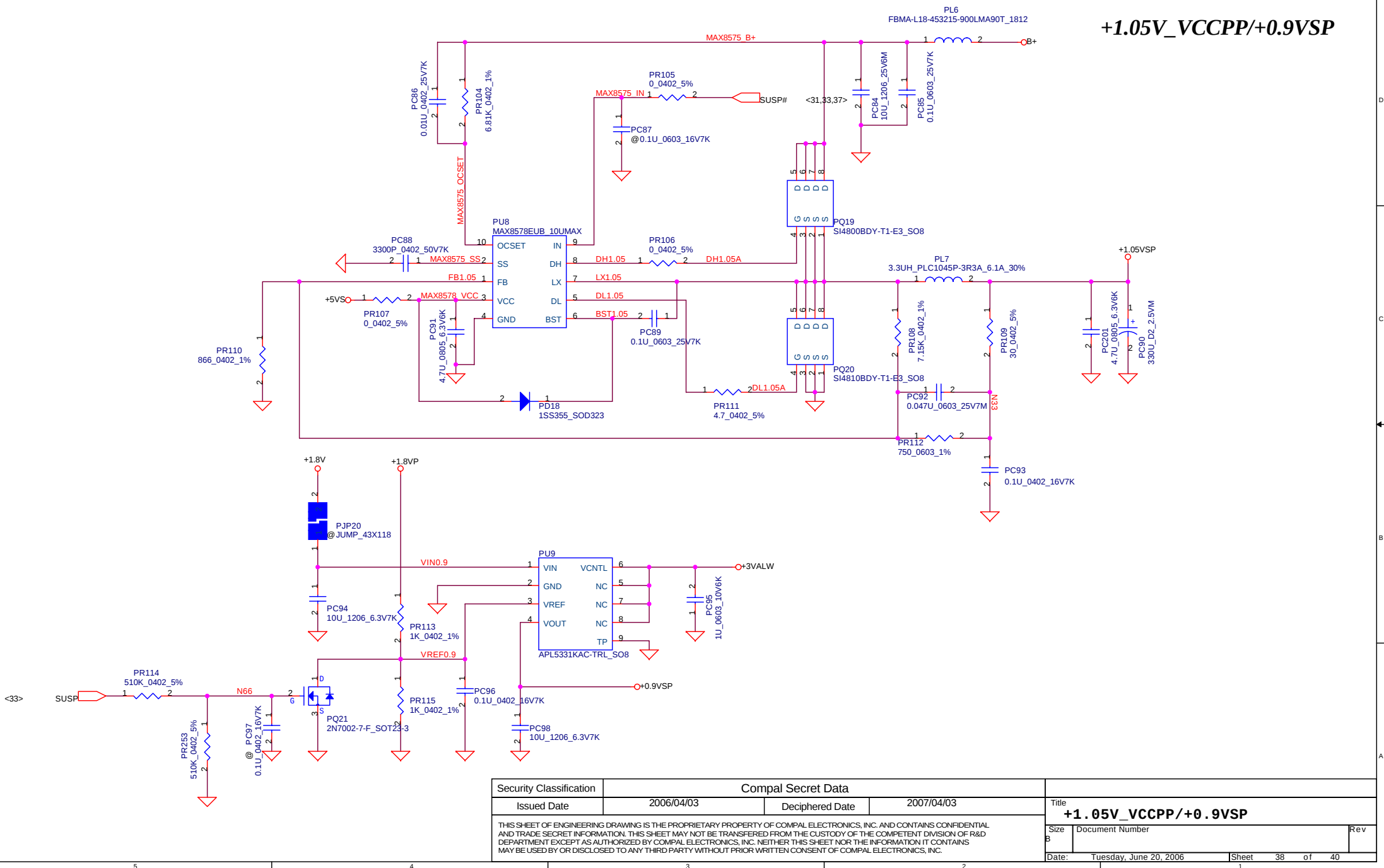
Charger

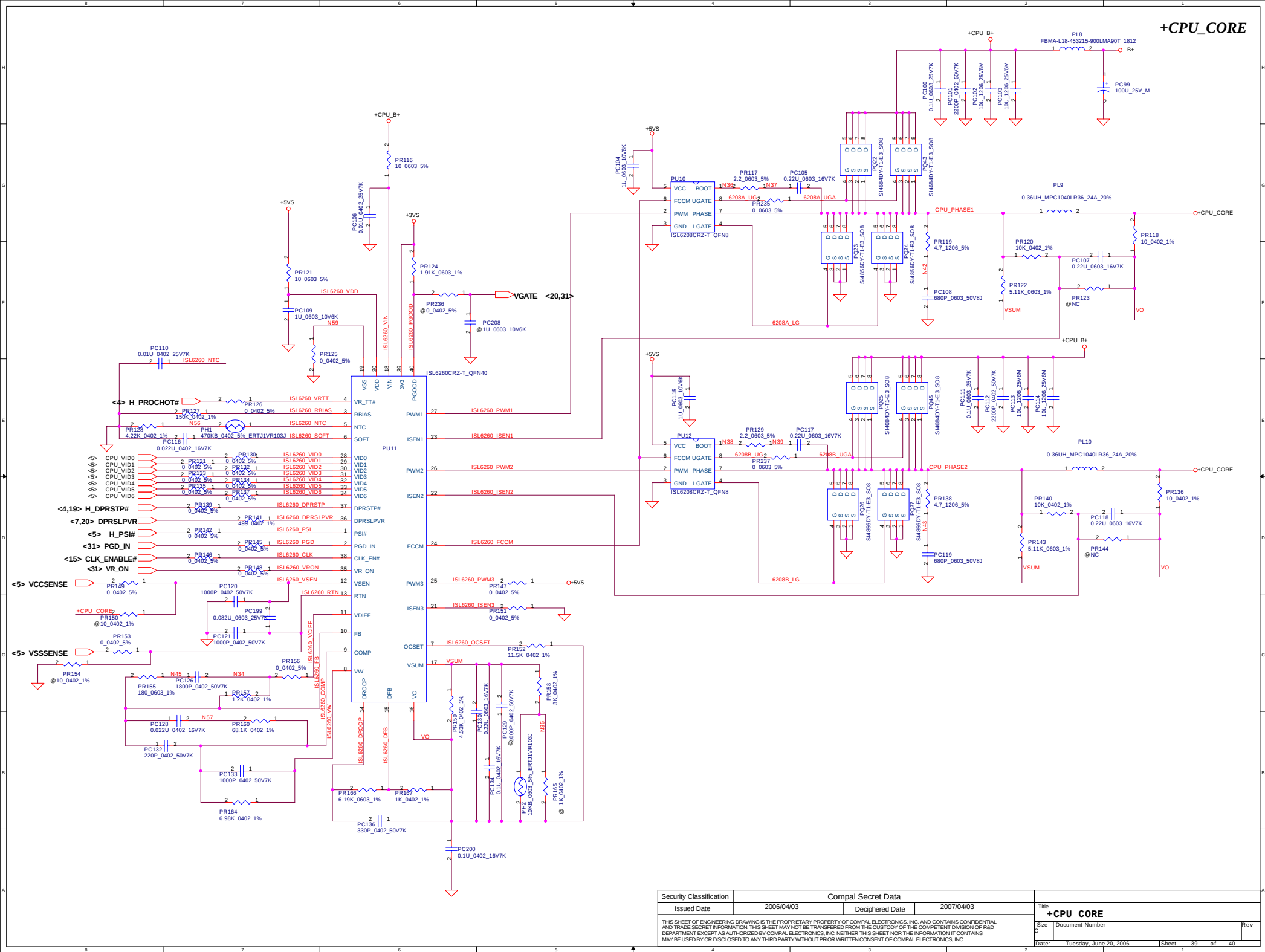


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				Date: Tuesday, June 20, 2006	Sheet 35 of 40

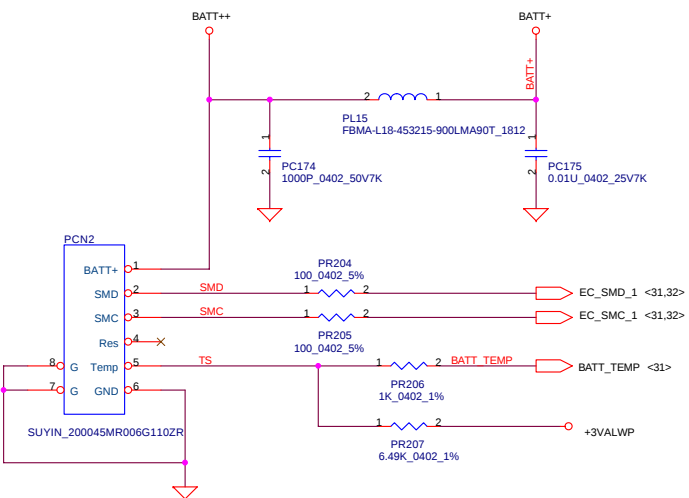
+3VALWP/+5VALWP



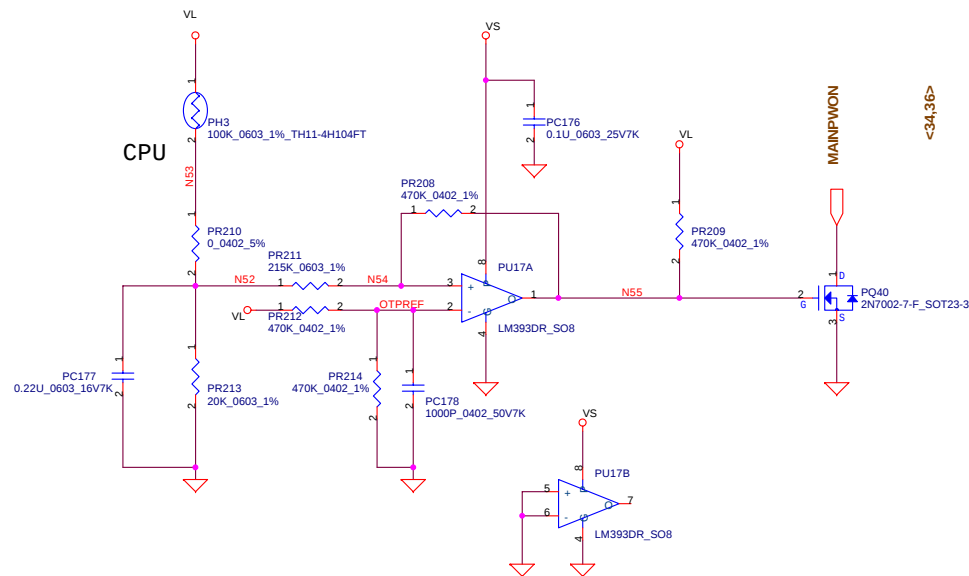




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PH1 under CPU botten side :
 CPU thermal protection at 90 +-3 degree C
 Recovery at 50 +-3 degree C



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								Size	Document Number	Rev
								Custom	Information	
Date:		Tuesday, June 20, 2006				Sheet		40 of 40		