SA1 BLOCK DIAGRAM

Merom / Crestline / ICH8-M

CPU THERMAL SENSOR +3.3V PG 3

CPU Merom (479 Micro-FCPGA) +1.5V +1.05V_VCCP +VCC_CORE PG 3,4

FSB 667/800 MHz

CPU CLK_ 200MHz
GMCH CLK_ 200MHz
DREFCLK_96MHz
PCIE MCH CLK_100MHz

X'TAL 14.318MHz

CLOCK GEN ICS9LPRS365/RTM875T-606 64pins +3.3V PG 2

DDRII-SODIMM1 DDRII-SODIMM2 +0.9V_DDR_VTT +1.8V_SUS +3.3V V_DDR_MCH_REF PG 12,13

DDRII 667 MHz

NORTH BRIDGE Crestline 965GM 1299 uFCBGA +1.05V_VCCP +1.8V_SUS +1.25V +3.3V V_DDR_MCH_REF PG 5~11

FOR Crestline (LCD/CRT/S-VIDEO)

LCD Panel VIN_BLIGHT LCDVCC +3.3V PG 18

FOR Crestline (LCD/CRT)

CRT port +5V +3.3V PG 20

SDVO

Chrontel Sil1392 PG 19

HDMI

HDMI port +3.3V +2.5V +1.8V PG 19

PCIE ICH CLK_100MHz
SATA ICH CLK_100MHz
PCIE LAN CLK_100MHz
PCIE MINICARD CLK_100MHz
PCIE NEW CARD CLK_100MHz

+3V_S5/+5V_S5 PG 40
CPU CORE POWER ISL6260C+ISL6208 PG 39
+1.5V PG 38
+1.25V & +1.05VCCP (ISL6236) PG 37
DDR2 +1.8V_SUS & +0.9V PG 36
D/D POWER +5_ALW & +3.3V_ALW PG 35
CHARGER MAX8724ETI+ PG 34
RUN POWER SW & DISCHARGE PG 33

Web Cam on LCD USB3 +5V PG 18

Bluetooth USB9 +5V_SUS PG 29

USB PORT X 3 USB0~2, +5V_SUS PG 28

USB 2.0

Fingerprint USB8 PG 29

ODD(fixed) +5V PG 27

PATA

Internal HDD +5V +3.3V PG 27

SATA

DMI LINK 4X PCI-E

X'TAL 32.768KHz

ICH8-M 652 BGA +1.5V +1.05V_VCCP +1.25V +3.3V +3.3V_ALW +3.3V_S5 +3.3V_SUS +3V_VCCLAN +5V +5V_ALW +5V_S5 VCCRTC_(1~4) PG 14~17

LPC

X'TAL 32.768KHz

IT8512E LQFP 128PIN +3.3V_ALW +3.3V +5V RTC_VCC PG 29

SWITCH BOARD +3.3V_ALW PG 31
FAN PG 3
Touchpad +5V PG 31
Keyboard +3.3V_ALW PG 31
SPI FLASH +3.3V_ALW PG 29

USB 2.0

PCI-E

Azalia

Azalia Codec STAC-9205 +AVDDA PG 23

MODEM CONN. (MDC) +3.3V_SUS PG 25

WIRE

RJ11/USB X 1 Board to board CONN. PG 25

AMP MAX 9789/TI** +5V_SPK_AMP PG 24

JACK HEADPHONE/SPDIF INT. DMIC INT. SPEAKERS PG 24

LAN(10/100) Realtek 8101E LAN_A1.8 LAN_A3.3 LAN_D1.5 LAN_E1.8 LANVCC PG 20,21

X'TAL 25MHz

RJ45 JACK PG 20

MINI-PCI-E Card X2 USB6~7 +3.3V_SUS +3.3V +1.5V PG 26

EXPRESS CARD (NEW CARD) USB5 3V_NEWCARD 3VAUX 1.5V_NEWCARD PG 32

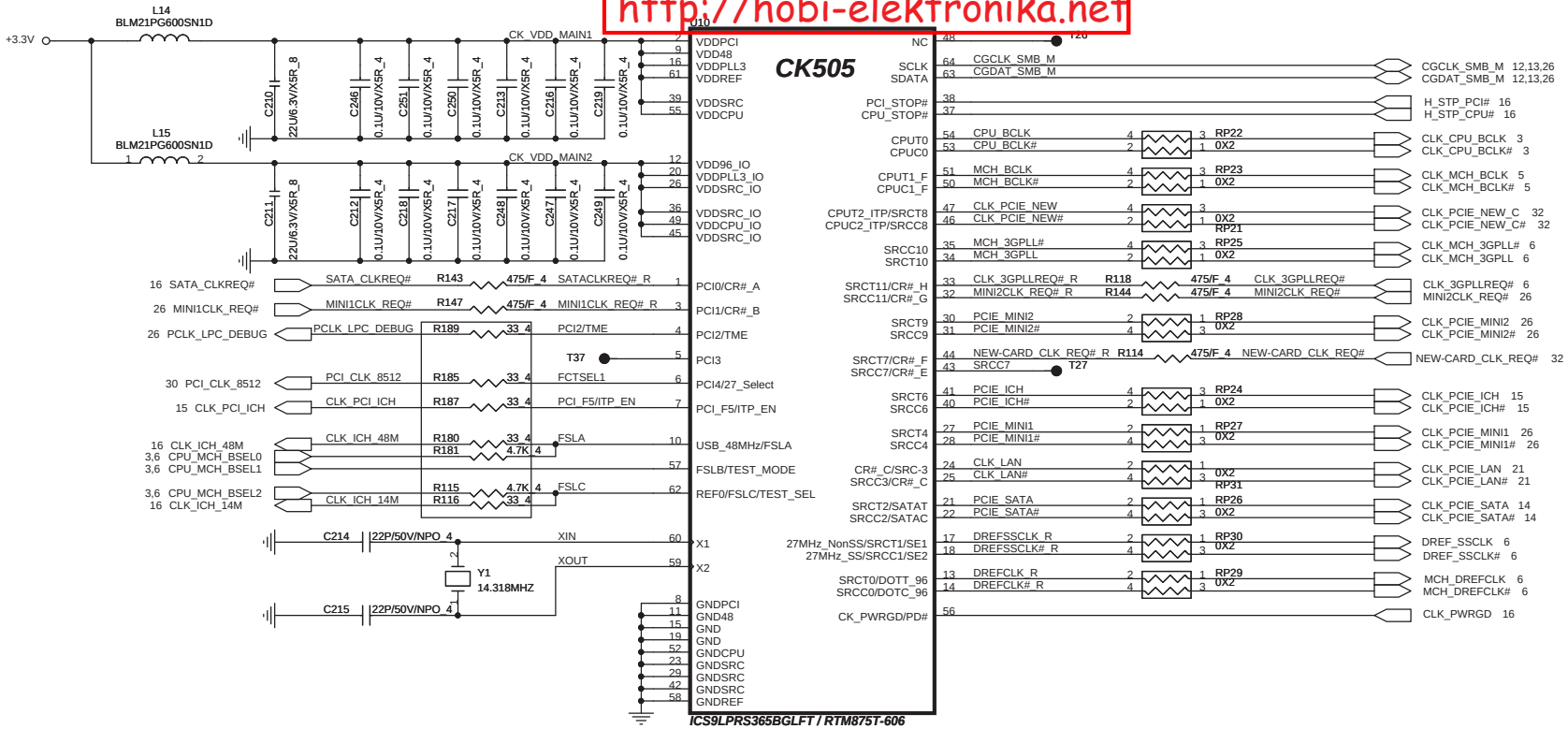
X'TAL 12MHz

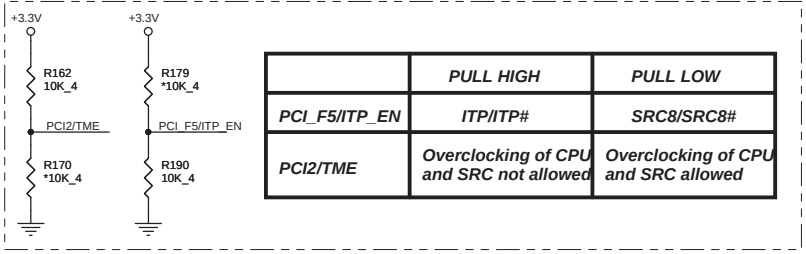
CARDREADER CONTROLLER Realtek RTS5158 USB4 +3.3V_SUS +5V_SUS PG 22

4 IN 1 SM/xD-Picture SD/MMC MS/MSPRO (CF) PG 22

PROJECT : SA1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	4A
Date: Friday, July 20, 2007	Sheet 1	of 43

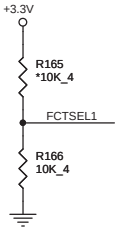


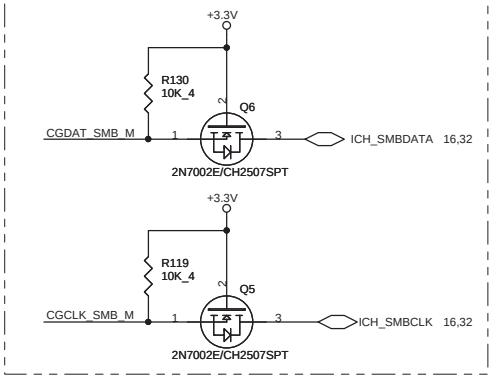


	PULL HIGH	PULL LOW
PCI_F5/ITP_EN	ITP/ITP#	SRC8/SRC8#
PCI2/TME	Overclocking of CPU and SRC not allowed	Overclocking of CPU and SRC allowed

GCLK_SEL = FCTSEL1

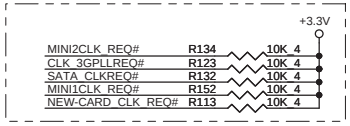
FCTSEL1 (PIN6)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96	DOT96#	SRC-1/LCDT_100	SRC-1#/LCDT_100
1 = External VGA	SRC-0	SRC-0#	27Mout-NSS	27Mout-SS

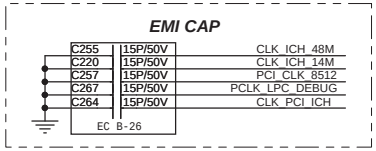




CPU Clock select

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100.00	100	33
0	0	1	133.33	100	33
0	1	1	166.66	100	33
0	1	0	200.00	100	33
0	0	0	266.66	100	33
1	0	0	333.33	100	33
1	1	0	400.00	100	33
1	1	1	200.00	100	33





PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	4A
Date: Thursday, July 26, 2007	Sheet 2	of 43

CPU Thermal monitor

03

CPU(HOST)

U22A

ADDR GROUP 0 · ADDR GROUP 1 · CONTROL · XDP/ITP SIGNALS · THERMAL · H CLK · RESERVED

Merom Ball-out Rev 1a

U22B

DATA GRP 0 · DATA GRP 1 · DATA GRP 2 · DATA GRP 3 · MISC

Merom Ball-out Rev 1a

<check list>
Default PU 56ohm if no use.Serial R NC
If connect to power side PU 75ohm.

Layout Note:
Place voltage divider within 0.5" of GTLREF pin

Layout Note:
Comp0,2 connect with Zo=27.4ohm,Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5".Trace should be at least 25 mils away from any other toggling signal.

Layout Note:
ICH_DPRSTP# need to daisy chain from ICH8 to IMVP6 to CPU.

Layout Note:
Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.

Layout Note:
Layout Note:Routing 10:10 mils and away from noise source with ground gard

Populate ITP700Flex for bringup

ITP700 layout guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	500 to 680 ohm ± 5%	GND	Place the pull-up near CPU
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	51 ohm ± 5%	VCCP	Place the pull-up near CPU
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.

PROJECT : SA1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU(1 of 2)/FAN/Thermal	4A
Date: Monday, July 23, 2007	Sheet 3 of 43	

CPU(Power)

All use 10U 4V(+-20%,X6S,0805)Pb-Free.

+VCC_CORE

C393 10U/4V/X6S_8 C394 10U/4V/X6S_8 C56 10U/4V/X6S_8 C406 10U/4V/X6S_8 C405 10U/4V/X6S_8

+VCC_CORE

C389 10U/4V/X6S_8 C391 10U/4V/X6S_8 C404 10U/4V/X6S_8 C407 10U/4V/X6S_8 C57 10U/4V/X6S_8

8 inside cavity, north side, secondary layer.

+VCC_CORE

C390 10U/4V/X6S_8 C26 10U/4V/X6S_8 C29 10U/4V/X6S_8 C28 10U/4V/X6S_8 C409 10U/4V/X6S_8

+VCC_CORE

C27 10U/4V/X6S_8 C30 10U/4V/X6S_8 C38 10U/4V/X6S_8 C55 10U/4V/X6S_8 C392 10U/4V/X6S_8

8 inside cavity, south side, secondary layer.

+VCC_CORE

C37 10U/4V/X6S_8 C44 10U/4V/X6S_8 C43 10U/4V/X6S_8 C24 10U/4V/X6S_8 C23 10U/4V/X6S_8 C25 10U/4V/X6S_8

6 inside cavity, north side, primary layer.

+VCC_CORE

C50 10U/4V/X6S_8 C51 10U/4V/X6S_8 C52 10U/4V/X6S_8 C53 10U/4V/X6S_8 C408 10U/4V/X6S_8 C54 10U/4V/X6S_8

6 inside cavity, south side, primary layer.

<REV.NO: 0.5/REF.NO.19343>
Ivcc Max 52A
Ivccp Max 6A(VCCP supply before Vcc stable)
Max 2A(VCCP supply after Vcc stable)
Ivcca Max 130mA

+VCC_CORE

U22C

A7	VCC[001]	VCC[068]	AB20	
A9	VCC[002]	VCC[069]	AB7	
A10	VCC[003]	VCC[070]	AC7	
A12	VCC[004]	VCC[071]	AC9	
A13	VCC[005]	VCC[072]	AC12	
A15	VCC[006]	VCC[073]	AC13	
A17	VCC[007]	VCC[074]	AC15	
A18	VCC[008]	VCC[075]	AC17	
A20	VCC[009]	VCC[076]	AC18	
B7	VCC[010]	VCC[077]	AD7	
B9	VCC[011]	VCC[078]	AD9	
B10	VCC[012]	VCC[079]	AD10	
B12	VCC[013]	VCC[080]	AD12	
B14	VCC[014]	VCC[081]	AD14	
B15	VCC[015]	VCC[082]	AD15	
B17	VCC[016]	VCC[083]	AD17	
B18	VCC[017]	VCC[084]	AD18	
B20	VCC[018]	VCC[085]	AE9	
C9	VCC[019]	VCC[086]	AE10	
C10	VCC[020]	VCC[087]	AE12	
C12	VCC[021]	VCC[088]	AE13	
C13	VCC[022]	VCC[089]	AE15	
C15	VCC[023]	VCC[090]	AE17	
C17	VCC[024]	VCC[091]	AE18	
C18	VCC[025]	VCC[092]	AE20	
D9	VCC[026]	VCC[093]	AE9	
D10	VCC[027]	VCC[094]	AE10	
D12	VCC[028]	VCC[095]	AE12	
D14	VCC[029]	VCC[096]	AE14	
D15	VCC[030]	VCC[097]	AE15	
D17	VCC[031]	VCC[098]	AE17	
D18	VCC[032]	VCC[099]	AE18	
E7	VCC[033]	VCC[100]	AE20	
E9	VCC[034]			
E10	VCC[035]	VCCP[01]	G21	
E12	VCC[036]	VCCP[02]	V6	
E13	VCC[037]	VCCP[03]	J6	
E15	VCC[038]	VCCP[04]	K6	
E17	VCC[039]	VCCP[05]	M6	
E18	VCC[040]	VCCP[06]	J21	
E20	VCC[041]	VCCP[07]	K21	
F7	VCC[042]	VCCP[08]	M21	
F9	VCC[043]	VCCP[09]	N21	
F10	VCC[044]	VCCP[10]	N6	
F12	VCC[045]	VCCP[11]	R21	
F14	VCC[046]	VCCP[12]	R6	
F15	VCC[047]	VCCP[13]	T21	
F17	VCC[048]	VCCP[14]	T6	
F18	VCC[049]	VCCP[15]	V21	
F20	VCC[050]	VCCP[16]	W21	
AA7	VCC[051]			
AA9	VCC[052]	VCCA[01]	B26	
AA10	VCC[053]	VCCA[02]	C26	
AA12	VCC[054]			
AA13	VCC[055]	VID[0]	AD6	VID0 39
AA15	VCC[056]	VID[1]	AE5	VID1 39
AA17	VCC[057]	VID[2]	AE5	VID2 39
AA18	VCC[058]	VID[3]	AE4	VID3 39
AA20	VCC[059]	VID[4]	AE3	VID4 39
AB9	VCC[060]	VID[5]	AE3	VID5 39
AC10	VCC[061]	VID[6]	AE2	VID6 39
AB10	VCC[062]			
AB12	VCC[063]			
AB14	VCC[064]	VCCSENSE	AF7	VCCSENSE 39
AB15	VCC[065]			
AB17	VCC[066]			
AB18	VCC[067]	VSSSENSE	AE7	VSSSENSE 39

Merom Ball-out Rev 1a

+1.05V_VCCP

C401 C397 C396 C398 C402 C400

0.1U/10V/X5R_4

Layout out:
Place these inside socket cavity on North side secondary.

+1.05V_VCCP

C388 330U/2V_7343

+1.5V

+VCC_CORE

C76 0.01U/16V/X7R_4

C73 10U/6.3V/X5R_8

R317 100/F_6

Layout Note:
Place C76,C73 near PIN B26.

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4ohms and length matched to within 25 mil. Place PU and PD within 2 inch of CPU.

R318 100/F_6

U22D

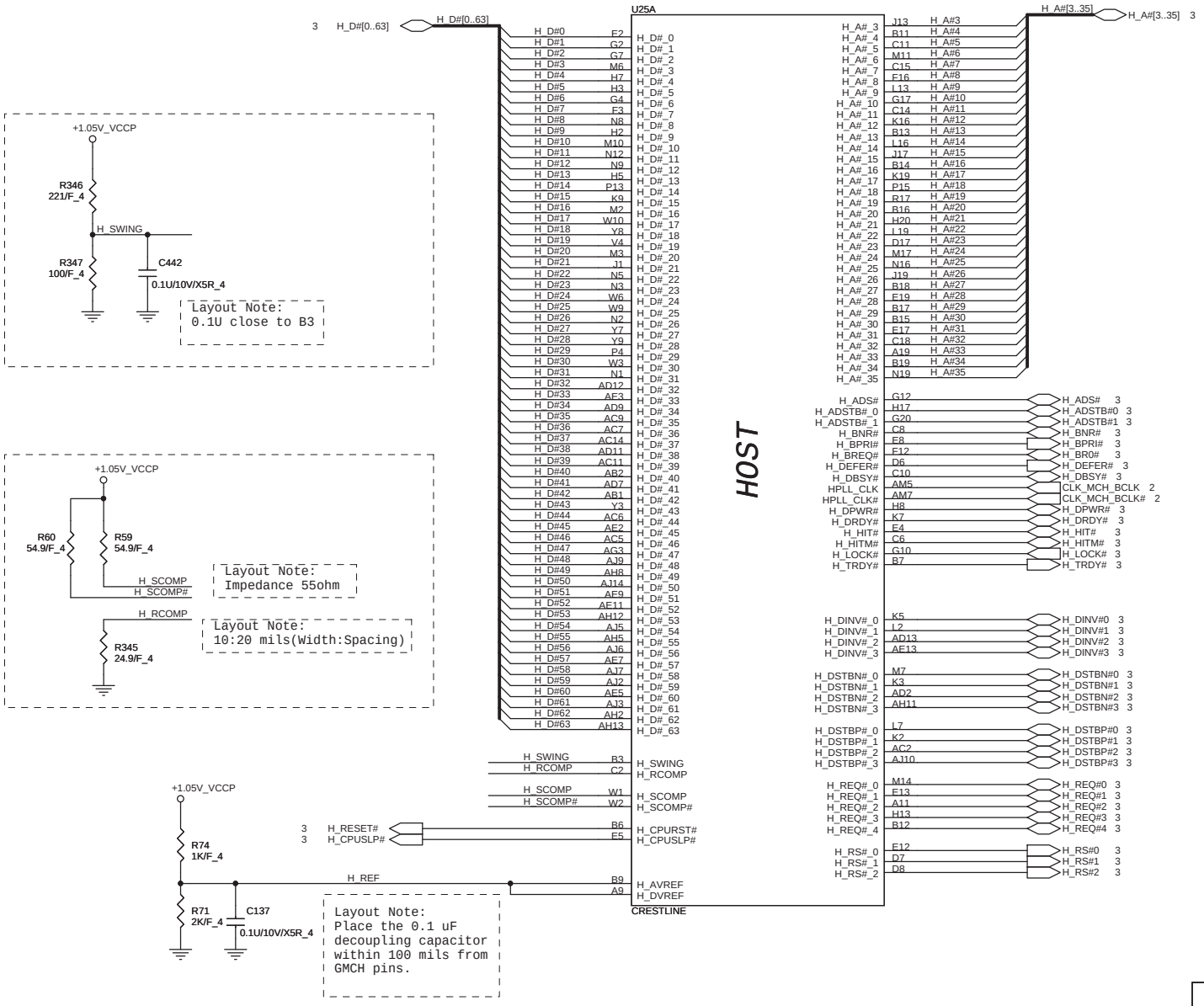
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
E24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC8
F19	VSS[049]	VSS[130]	AC11
F2	VSS[050]	VSS[131]	AC14
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
G26	VSS[056]	VSS[137]	AD5
H3	VSS[057]	VSS[138]	AD8
H6	VSS[058]	VSS[139]	AD11
H21	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE8
K23	VSS[067]	VSS[148]	AE11
K26	VSS[068]	VSS[149]	AE14
L3	VSS[069]	VSS[150]	AE16
L6	VSS[070]	VSS[151]	AE19
L21	VSS[071]	VSS[152]	AE23
L24	VSS[072]	VSS[153]	AE26
M2	VSS[073]	VSS[154]	A2
M5	VSS[074]	VSS[155]	AE6
M22	VSS[075]	VSS[156]	AE8
M25	VSS[076]	VSS[157]	AE11
N1	VSS[077]	VSS[158]	AE13
N4	VSS[078]	VSS[159]	AE16
N23	VSS[079]	VSS[160]	AE19
N26	VSS[080]	VSS[161]	AE21
P3	VSS[081]	VSS[162]	A25
		VSS[163]	AE25

Merom Ball-out Rev 1a

PROJECT : SA1

Quanta Computer Inc.

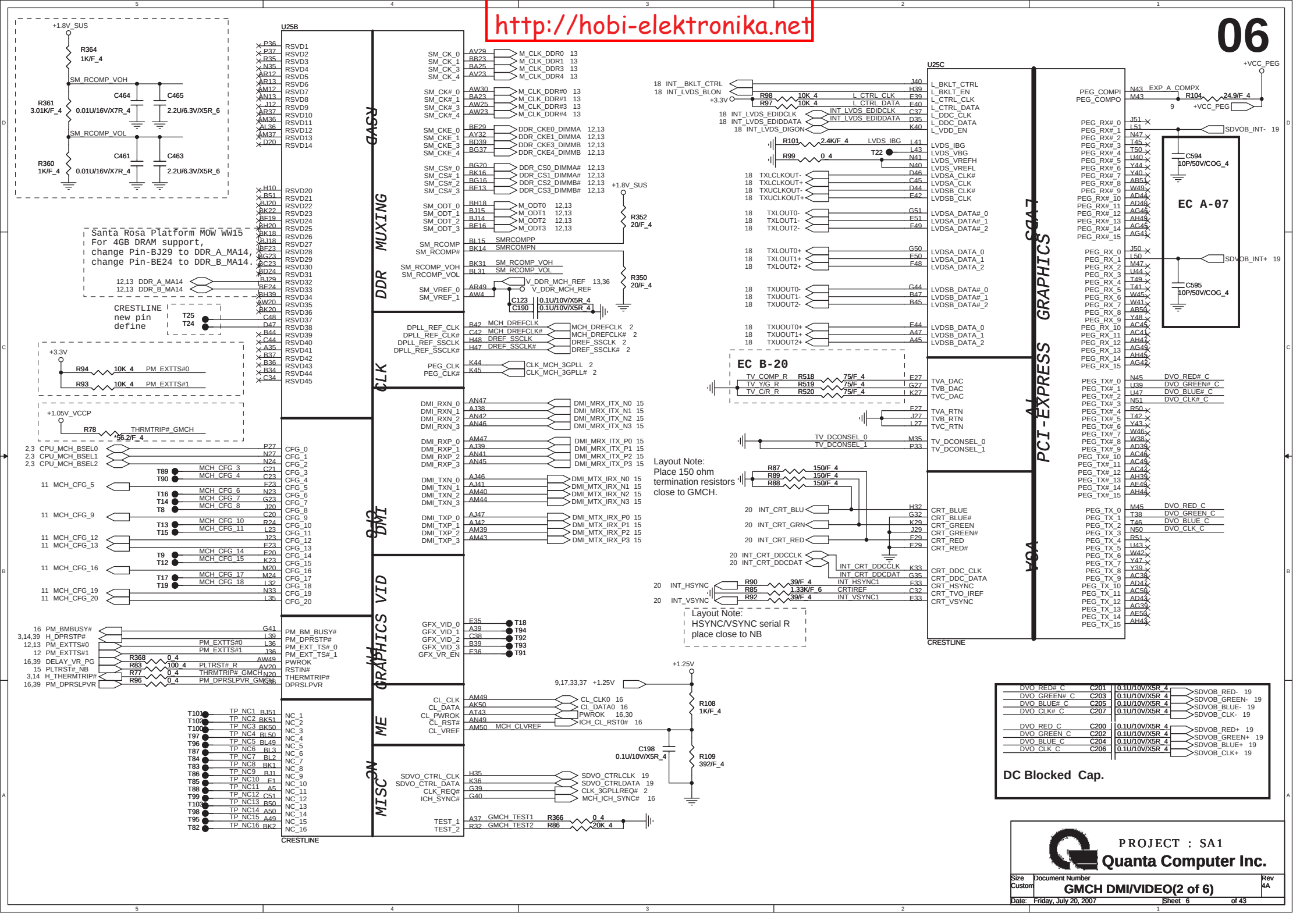
Size	Document Number	Rev
Custom	CPU(2 of 2)	4A
Date: Friday, July 20, 2007	Sheet 4	of 43

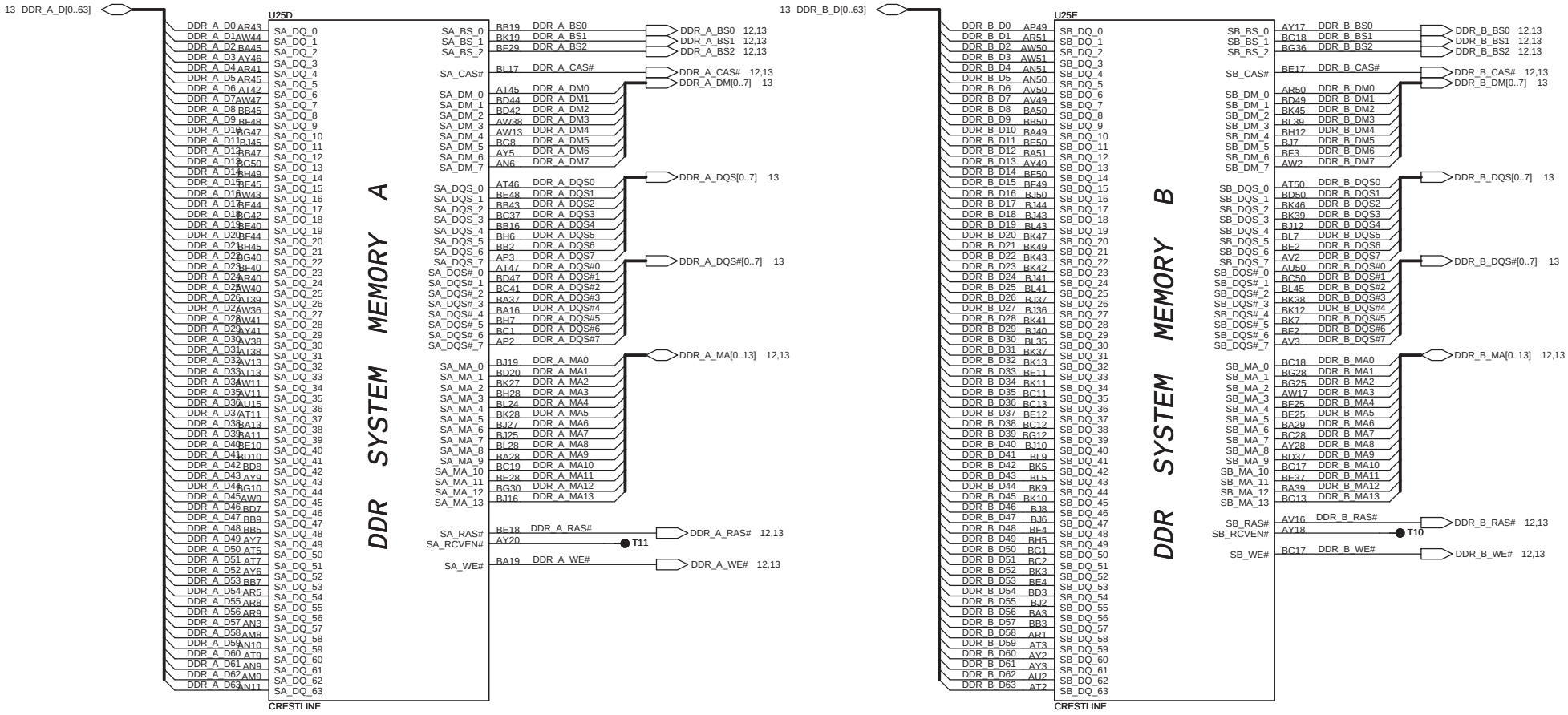


PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	GMCH HOST(1 of 6)	4A
Date: Friday, July 20, 2007	Sheet 5	of 43





PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	GMCH DDR/Strap(3 of 6)	4A
Date: Friday, July 20, 2007	Sheet 7 of 43	

GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

POWER

+1.05V_VCCP

U25G

VCC CORE: AT35 AT34 AH28 AC32 AC31 AK32 AJ31 AJ28 AH32 AH31 AH29 AF32 R30 → VCC_1 VCC_2 VCC_3 VCC_5 VCC_4 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13

+1.8V_SUS

IVCCSM supply current 1 channel 1.615A 2 channel 3.138A

0.1U/10V/X5R_4 C175; 330U/2.5V_7343 C483; 22U/4V/X6S_8 C171; 22U/4V/X6S_8 C172

Layout Note: Place C175 where LVDS and DDR2 taps.

VCC SM: AU32 AU33 AU35 AV33 AW33 AW35 AY35 BA32 BA33 BA35 BB33 BC32 BC33 BC35 BD32 BD35 BE32 BE33 BE35 BF33 BE34 BG32 BG33 BG35 BH32 BH34 BH35 BJ32 BJ33 BJ34 BK32 BK33 BK34 BK35 BL33 AU30 → VCC_SM_1 … VCC_SM_36

+1.05V_VCCP

VCC GFX: R20 T14 W13 W14 Y12 AA20 AA23 AA26 AA28 AB21 AB24 AB29 AC20 AC21 AC23 AC24 AC26 AC28 AC29 AD20 AD23 AD24 AD28 AE21 AE26 AA31 AH20 AH21 AH23 AH24 AH26 AD31 AJ20 AN14 → VCC_AXG_1 … VCC_AXG_34

CRESTLINE

VCC GFX NCTF: VCC_AXG_NCTF_1 … VCC_AXG_NCTF_83 → T17 T18 T19 T21 T22 T23 T25 U15 U16 U17 U19 U20 U21 U23 U26 V16 V17 V19 V20 V21 V23 V24 Y15 Y16 Y17 Y19 Y20 Y21 Y23 Y24 Y26 Y28 Y29 AA16 AA17 AB16 AB19 AC16 AC17 AC19 AD15 AD16 AD17 AE16 AE19 AH15 AH16 AH17 AH19 AJ16 AJ17 AJ19 AK16 AK19 AL16 AL17 AL19 AL20 AL21 AL23 AM15 AM16 AM19 AM20 AM21 AM23 AP15 AP16 AP17 AP19 AP20 AP21 AP23 AP24 AR20 AR21 AR23 AR24 AR26 V26 V28 V29 Y31

+1.05V_VCCP

Ivcc (External GFX 1.310 A, integrate 1.572 A)

330U/2V_7343 C84; 22U/4V/X6S_8 C96; 0.22U/6.3V/X5R_4 C163; 0.22U/6.3V/X5R_4 C154; C173 0.1U/10V/X5R_4

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity.

Ivcc_AXG Graphics core supply current 7.7A

C420 330U/2V_7343; C422 330U/2V_7343

Layout Note: 370 mils from edge.

C179 0.1U/10V/X5R_4; C178 0.1U/10V/X5R_4; C162 0.47U/10V/X7R_6; C148 1U/6.3V/X5R_6; C149 22U/4V/X6S_8; C99 10U/6.3V/X5R_8

Layout Note: Inside GMCH cavity for VCC_AXG.

Ivcc_AXM Controller supply current 540mA

Layout Note: Inside GMCH cavity for VCC_AXG.

+1.05V_VCCP 3,4,5,6,9,14,17,37

C177 0.1U/10V/X5R_4; C168 0.1U/10V/X5R_4; C161 0.1U/10V/X5R_4

C176 22U/4V/X6S_8; C155 0.22U/6.3V/X5R_4; C169 0.22U/6.3V/X5R_4

Layout Note: Place close to GMCH edge.

U25F

VCC NCTF: VCC_NCTF_1 … VCC_NCTF_50 → AB33 AB36 AB37 AC33 AC35 AC36 AD35 AD36 AF33 AF36 AH33 AH35 AH36 AH37 AJ33 AJ35 AK33 AK35 AK36 AK37 AD33 AJ36 AM35 AL33 AL35 AA33 AA35 AA36 AP35 AP36 AR35 AR36 Y32 Y33 Y35 Y36 Y37 T30 T34 T35 U29 U31 U32 U33 U35 U36 V32 V33 V36 V37

VSS NCTF: VSS_NCTF_1 … VSS_NCTF_21 → T27 T37 U24 U28 V31 V35 AA19 AB17 AB35 AD19 AD37 AF17 AF35 AK17 AM17 AM24 AP26 AP28 AR15 AR19 AR28

VSS SCB: VSS_SCB1 … VSS_SCB6 → A3 B2 C1 BL1 BL51 A51

VCC AXM NCTF: VCC_AXM_NCTF_1 … VCC_AXM_NCTF_19 → AL24 AL26 AL28 AM26 AM28 AM29 AM31 AM32 AM33 AP29 AP31 AP32 AP33 AL29 AL31 AL32 AR31 AR32 AR33

VCC AXM: VCC_AXM_1 … VCC_AXM_7 → AT33 AT31 AK29 AK24 AK23 AJ26 AJ23

+1.05V_VCCP

CRESTLINE

VCC SM LF: VCC_SM_LF1 … VCC_SM_LF7 → AW45 VCCSM_LF1; BC39 VCCSM_LF2; BE39 VCCSM_LF3; BD17 VCCSM_LF4; BD4 VCCSM_LF5; AW8 VCCSM_LF6; AT6 VCCSM_LF7

C131 0.1U/10V/X5R_4; C129 0.1U/10V/X5R_4; C127 0.22U/6.3V/X5R_4; C158 0.22U/6.3V/X5R_4; C181 0.47U/6.3V/X5R_4; C174 1U/6.3V/X5R_6; C187 1U/6.3V/X5R_6

+3.3V

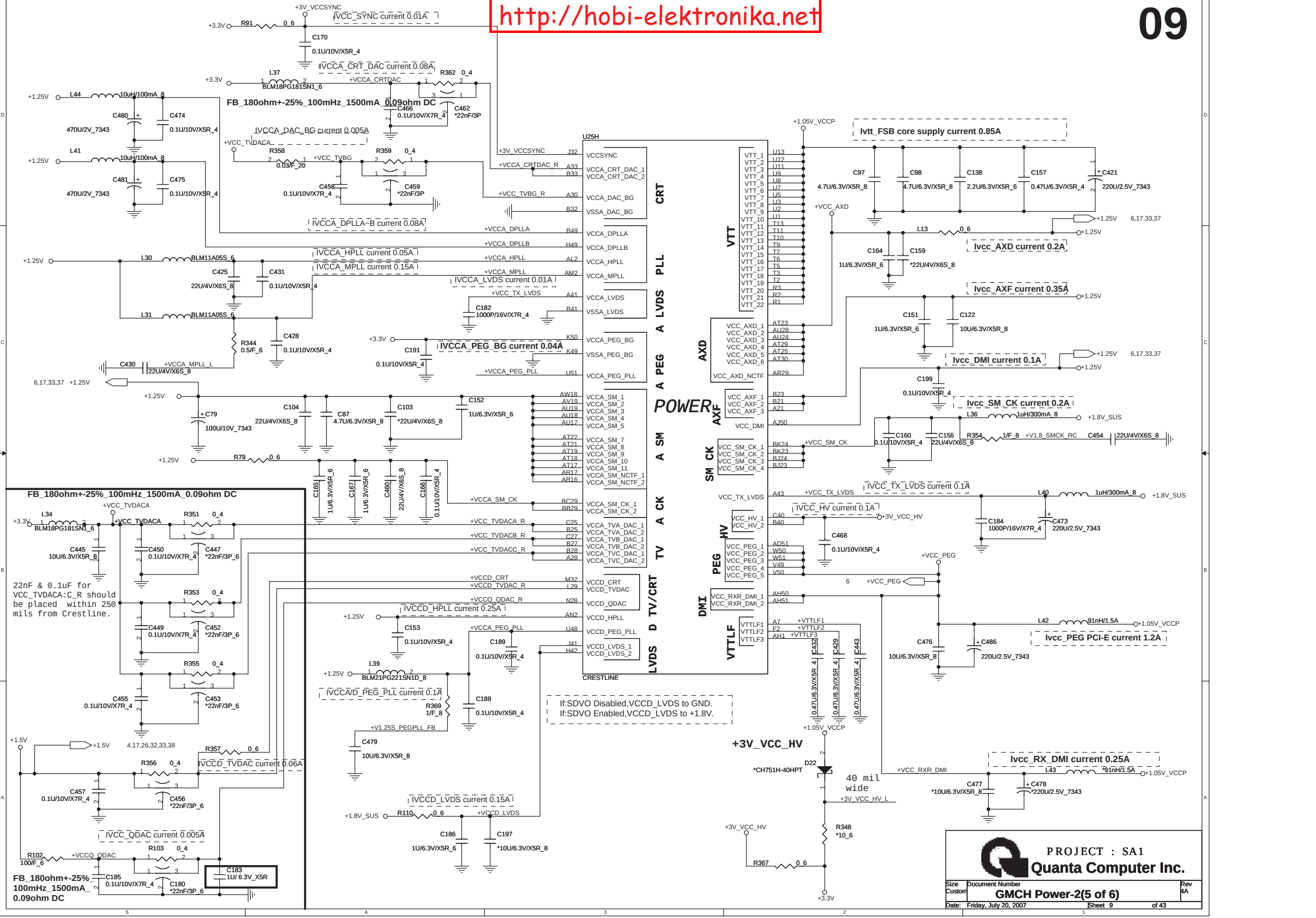
R349 10_6 +VCC_GMCH_L; D23 CH751H-40PT

PROJECT : SA1

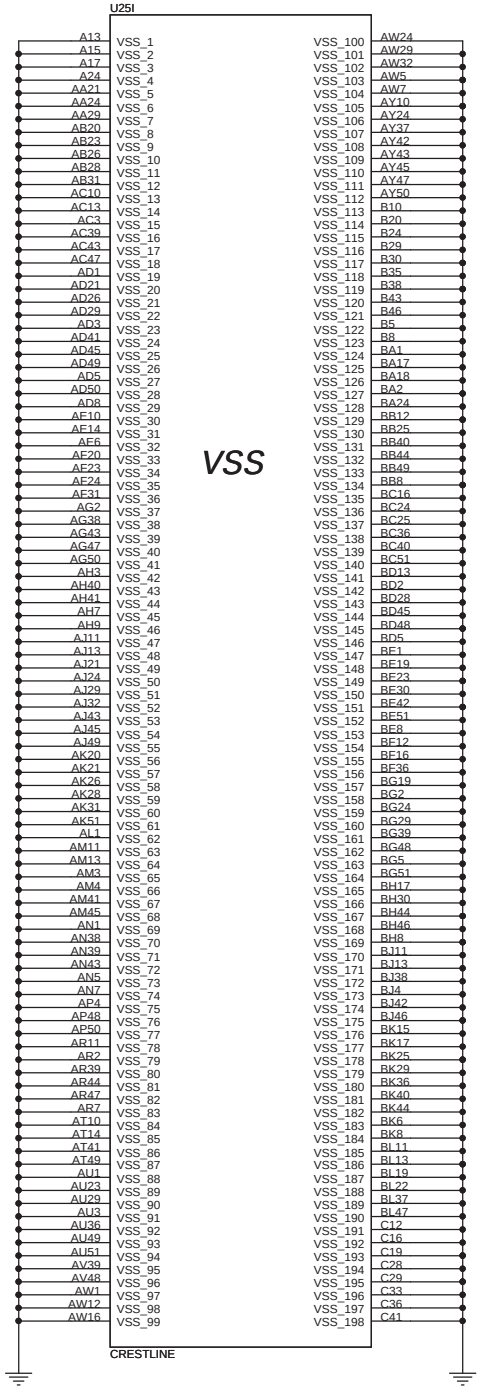
Quanta Computer Inc.

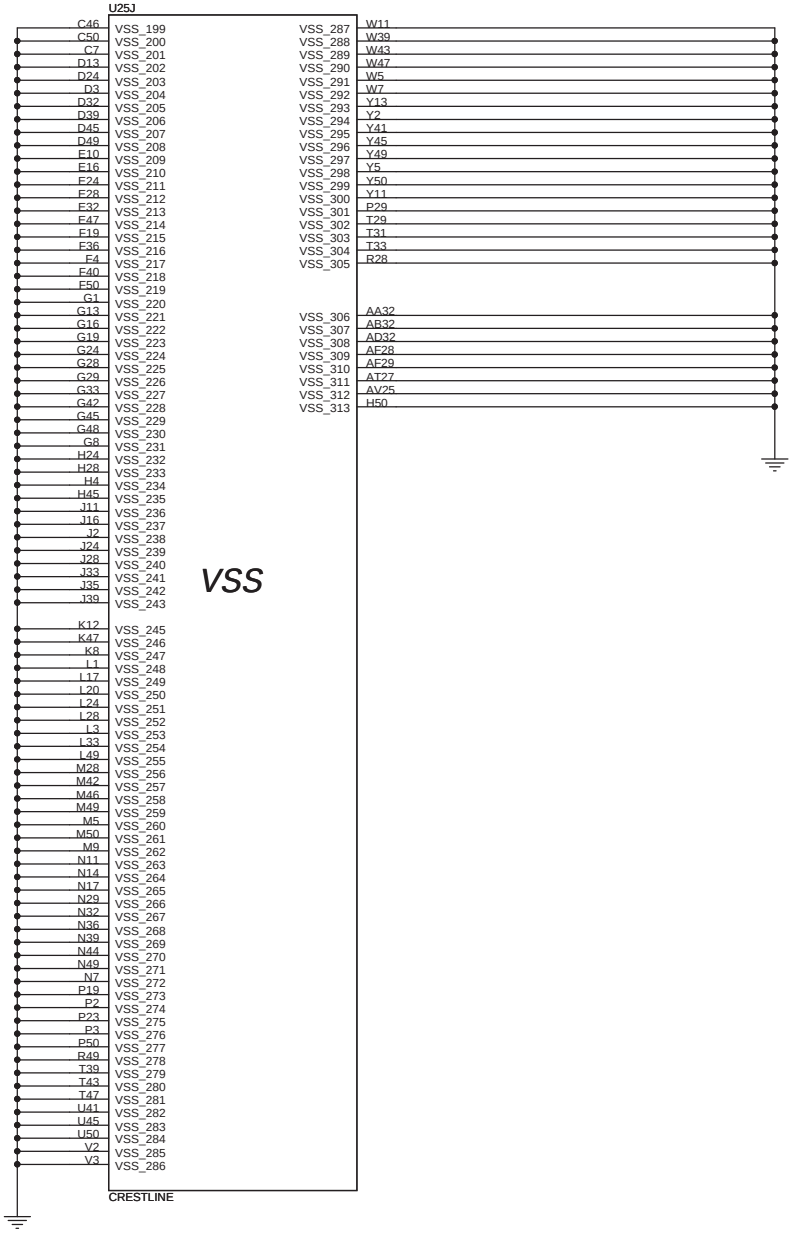
Size	Document Number	Rev
Custom	GMCH Power-1(4 of 6)	4A

Date: Friday, July 20, 2007 Sheet 8 of 43



	PROJECT : SA1		
	Quanta Computer Inc.		
Size: Custom	Document Number: GMCH Power-2(5 of 6)		Rev: 4A
Date: Friday, July 20, 2007	Sheet 9	of 43	





Size: Custom	Document Number: GMCH Power-3(6 of 6)	Rev: 4A
Date: Friday, July 20, 2007	Sheet 10 of 43	

PROJECT : SA1

Quanta Computer Inc.

Strap table

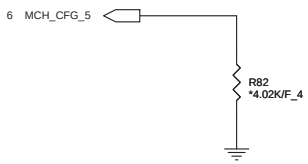
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	IntelR Management Engine Crypto strap	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. 1= Intel Management Engine Crypto TLS cipher suite with confidentiality (default).
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

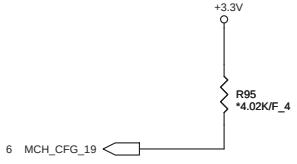
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



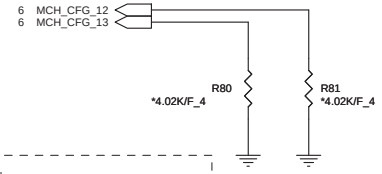
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane



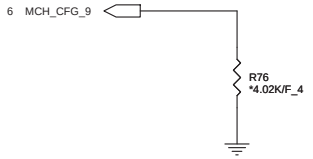
XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

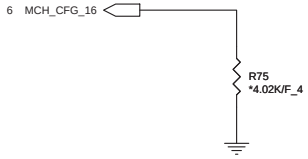


SDVO Present

Strap define at External DVI control page

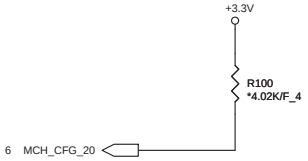
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port



Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minmize stub.

PROJECT : SA1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	GMCH Strap Table	4A
Date: Friday, July 20, 2007	Sheet 11 of 43	

DDRII A CHANNEL

Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

+0.9V_DDR_VTT

C139 C108 C89 C116 C133 C145 C142 C81 C92 C130 C91 C128 C141

0.1U/10V/X5R_4

DDRII B CHANNEL

+0.9V_DDR_VTT

C85 C150 C136 C143 C146 C120 C144 C86 C132 C80 C102 C112 C124

0.1U/10V/X5R_4

7,13 DDR_A_MA[0..13]

+0.9V_DDR_VTT

+0.9V_DDR_VTT 33,36

DDR_B_MA[0..13] 7,13

DDR_A_MA7 / DDR_A_MA11	RP17	56X2	RP16	56X2	DDR_B_MA11 / DDR_B_MA7
DDR_A_MA4 / DDR_A_MA6	RP15	56X2	RP13	56X2	DDR_B_MA6 / DDR_B_MA4
7,13 DDR_A_RAS# / 7,13 DDR_A_BS1	RP9	56X2	RP6	56X2	DDR_B_RAS# 7,13 / DDR_B_BS1 7,13
6,13 M_ODT0 / DDR_A_MA13	RP2	56X2	RP1	56X2	DDR_B_MA13 / M_ODT2 6,13
7,13 DDR_A_BS2 / DDR_A_MA12	RP20	56X2	RP10	56X2	DDR_B_MA3 / DDR_B_MA5
DDR_A_MA8 / DDR_A_MA9	RP18	56X2	RP19	56X2	DDR_B_MA9 / DDR_B_MA12
DDR_A_MA5 / DDR_A_MA3	RP12	56X2	RP14	56X2	DDR_B_MA1 / DDR_B_MA8
DDR_A_MA10 / DDR_A_BS0	RP7	56X2	RP5	56X2	DDR_B_MA10 / DDR_B_BS0 7,13
7,13 DDR_A_WE# / 7,13 DDR_A_CAS#	RP4	56X2	RP3	56X2	DDR_B_WE# 7,13 / DDR_B_CAS# 7,13
DDR_A_MA0 / DDR_A_MA2	RP11	56X2	RP8	56X2	DDR_B_MA2 / DDR_B_MA0

6,13 M_ODT1 / DDR_A_MA1	R57 56_4	R54 56_4	M_ODT3 6,13 / DDR_B_BS2 7,13
6,13 DDR_CS0_DIMMA#	R65 56_4	R68 56_4	DDR_CS2_DIMMB# 6,13
6,13 DDR_CS1_DIMMA#	R64 56_4	R62 56_4	DDR_CS3_DIMMB# 6,13
6,13 DDR_CKE0_DIMMA	R61 56_4	R58 56_4	DDR_CKE3_DIMMB 6,13
6,13 DDR_CKE1_DIMMA	R73 56_4	R72 56_4	DDR_CKE4_DIMMB 6,13
6,13 DDR_A_MA14	R69 56_4	R70 56_4	DDR_B_MA14 6,13
	R66 56_4	R67 56_4	

Please these resistor closely DIMMA,all trace length<750 mil.

Please these resistor closely DIMMB,all trace length<750 mil.

DDR2 Thermal Sensor SO-DIMM 0 & 1 — Uninstall

+3.3V

+3.3V 2,3,6,8,9,11,13,14,15,16,17,18,19,20,21,24,26,27,29,30,31,32,33

R33 *220_6

C59 *0.1U/10V/X5R_4

U4 *LM86CIMM

2,13,26 CGCLK_SMB_M	8	SCLK	
2,13,26 CGDAT_SMB_M	7	SDA	
6,13 PM_EXTTS#0	6	ALERT#	
6 PM_EXTTS#1	4	OVERT#	
	1	VCC	LM86_3V
	2	DXP	DDR_THERMDA
	3	DXN	
	5	GND	DDR_THERMDC

R34 *0_4

*MMBT3904_NL Q1

PROJECT : SA1

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Size	Document Number	Rev
Custom	DDR RES. ARRAY	4A

Date: Friday, July 20, 2007 Sheet 12 of 43

A is required to route to Top SoDIMM for AMT to function.This will need to change for M08

DDR2 Dual channel A/B CONN

PC4800 DDR2 SDRAM SO-DIMM (200P)

CN18 — DIMM1_9.2

CKE 0,1
CLOCK 0,1

SMbus address A0

CN19 — DIMM2_5.2

CKE 2,3
CLOCK 3,4

SMbus address A4

Place these Caps near So-Dimm1.

Place these Caps near So-Dimm2.

PROJECT : SA1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR SO-DIMM(200P)	4A
Date: Friday, July 20, 2007	Sheet 13 of 43	

RTC

+RTC_CELL
+3.3V_ALW
D3
CH501H-40PT
C256 1U/10V/X5R_6
VCCRTC_4
D4
CH501H-40PT
R164 20K_4
R211 1K_4
R158 1M/F_4
C261 1U/10V/X5R_6
RTC_CON.
CN22
+5V_ALW
VCCRTC_3
R209 *1.2K_4
VCCRTC_1
R210 *1K_4
VCCRTC_2
Q9 *MMBT3904_NL
R230 *4.7K_4
R229 *15K_4

SB Strap

+RTC_CELL
R150 332K/F_4
ICH_INTVRMEN
R137 *0_4

ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

+RTC_CELL
R172 332K/F_4
LAN100_SLP
R183 *0_4

ICH8M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)

ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

C244 18P/50V/COG_4
Y2 32.768KHZ
C253 18P/50V/COG_4
R149 10M_6

+3.3V_S5
R386 *10K_4
ENERGY_DET

U27A

ICH_RTCX1 AG25 RTCX1
ICH_RTCX2 AE24 RTCX2
RTCRST# AF23 RTCRST#
SM_INTRUDER# AD22 INTRUDER#
ICH_INTVRMEN AF25 INTVRMEN
LAN100_SLP AD21 LAN100_SLP

RTC

GLAN_CLK B24 GLAN_CLK
LAN_RSTSYNC D22 LAN_RSTSYNC
LAN_RXD0 C21 LAN_RXD0
LAN_RXD1 B21 LAN_RXD1
LAN_RXD2 C22 LAN_RXD2
LAN_TXD0 D21 LAN_TXD0
LAN_TXD1 E20 LAN_TXD1
LAN_TXD2 C20 LAN_TXD2
ENERGY_DET AH21 GLAN_DOCK#/GPIO13
GLAN_COMPI C25
GLAN_COMPO D25

LAN / GLAN

HDA_BIT_CLK AJ16
HDA_SYNC AJ15
HDA_RST# AE14
HDA_SDIN0 AJ17
HDA_SDIN1 AH17
HDA_SDIN2 AH15
HDA_SDIN3 AD13
HDA_SDOUT AE13
HDA_DOCK_EN#/GPIO33 AE10
HDA_DOCK_RST#/GPIO34 AG14

IHDA

SATALED# AE10
SATA0RXN AF6
SATA0RXP AF5
SATA0TXN AH5
SATA0TXP AH6
SATA1RXN AG3
SATA1RXP AG4
SATA1TXN AJ4
SATA1TXP AJ3
SATA2RXN AF2
SATA2RXP AF1
SATA2TXN AF4
SATA2TXP AF3
SATA_CLKN AB7
SATA_CLKP AC6
SATARBIAS# AG1
SATARBIAS AG2

SATA

FWH0/LAD0 E5
FWH1/LAD1 F5
FWH2/LAD2 G8
FWH3/LAD3 F6
FWH4/LFRAME# C4
LDRQ0# G9
LDRQ1#/GPIO23 E6
A20GATE AE13
A20M# AG26
DPRSTP# AF26
DPSLP# AE26
FERR# AD24
CPUPWRGD/GPIO49 AG29
IGNNE# AF27
INIT# AE24
INTR AC20
RCIN# AH14
NMI AD23
SMI# AG28
STPCLK# AA24
THRMTRIP# AE27
TP8 AA23

LPC

GATEA20
H_A20M#
H_DPRSTP#
H_DPSLP#
H_FERR#
H_PWRGOOD
H_IGNNE#
H_INIT#
H_INTR
RCIN#
H_NMI
H_SMI#
H_STPCLK#
H_THERMTRIP_R
ICH_TP8

CPU

IDE_DD0 V1
IDE_DD1 U2
IDE_DD2 V3
IDE_DD3 T1
IDE_DD4 V4
IDE_DD5 T5
IDE_DD6 AB2
IDE_DD7 T6
IDE_DD8 T3
IDE_DD9 R2
IDE_DD10 T4
IDE_DD11 V6
IDE_DD12 V5
IDE_DD13 U1
IDE_DD14 V2
IDE_DD15 U6
IDE_DA0 AA4
IDE_DA1 AA1
IDE_DA2 AB3
IDE_DCS1# Y6
IDE_DCS3# Y5
IDE_DIOR# W4
IDE_DIOW# W3
IDE_DDACK# Y2
IDE_IRQ Y3
IDE_IORDY Y1
IDE_DDREQ W5

IDE

ICH8M REV 1.0

+1.05V_VCCP
R127 *56.2/F_4
R139 *56.2/F_4
R157 56.2/F_4
H_DPSLP#
H_DPRSTP#
H_FERR#

+3.3V
+3.3V
R405 10K_4
R220 10K_4
RCIN#
GATEA20

+1.05V_VCCP
R124 56.2/F_4
H_THERMTRIP# 3,6

Layout Note:
Placement close SB L<2"
C599 Varistor_4

LDRQ#0 26
LDRQ#1
T73

R148 24.9/F_4 GLAN_COMP_SB
+1.5V_PCIE_ICH
15,17 +1.5V_PCIE_ICH

C589 10P/50V/COG_4
C82 10P/50V/COG_4
C272 10P/50V/COG_4
C271 10P/50V/COG_4

19 ICH_AZ_HDMI_BITCLK
25 ICH_AZ_MDC_BITCLK
24 ICH_AZ_CODEC_BITCLK
R50 33_4
R394 33_4
R392 33_4
ACZ_BIT_CLK

19 ICH_AZ_HDMI_SYNC
25 ICH_AZ_MDC_SYNC
24 ICH_AZ_CODEC_SYNC
R52 33_4
R397 33_4
R399 33_4
ACZ_SYNC
C590 10P/50V/COG_4

19 ICH_AZ_HDMI_RST#
25 ICH_AZ_MDC_RST#
24 ICH_AZ_CODEC_RST#
R45 33_4
R217 33_4
R215 33_4
ACZ_RST#
C591 10P/50V/COG_4

19 ICH_AZ_HDMI_SDOUT
25 ICH_AZ_MDC_SDOUT
24 ICH_AZ_CODEC_SDOUT
R40 33_4
R228 33_4
R232 33_4
ACZ_SDOUT
C592 10P/50V/COG_4

24 ICH_AZ_CODEC_SDIN0
25 ICH_AZ_MDC_SDIN1
19 ICH_AZ_HDMI_SDIN2
C593 10P/50V/COG_4

+3.3V
R206 10K_4
21 LAN_DISABLE#
GPIO34

31 SATA_LED#
27 SATA_RX0-
27 SATA_RX0+
SATA_TX0- C
SATA_TX0+ C

R253 10K_4
R258 10K_4
SATA1TXN
SATA1TXP
T136
T138

R434 10K_4
R435 10K_4
SATA2TXN
SATA2TXP
T75
T139

2 CLK_PCIE_SATA#
2 CLK_PCIE_SATA

R433 24.9/F_4 SATA_BIAS

Layout Note:
L<500mils

EC A-06

IDE_DD[0..15]
IDE_DD[0..15] 27

IDE_DA0 27
IDE_DA1 27
IDE_DA2 27
IDE_DCS1# 27
IDE_DCS3# 27
IDE_DIOR# 27
IDE_DIOW# 27
IDE_DDACK# 27
IDE_IRQ 27
IDE_IORDY 27
IDE_DDREQ 27

27 SATA_TX0-
27 SATA_TX0+
C294 3900P/25V/X7R_4 SATA_TX0-_C
C293 3900P/25V/X7R_4 SATA_TX0+_C

Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-8 M and cap on the "N" signal for same pair.

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

+3.3V
R207 *1K_4
ACZ_SDOUT
ICH_RSVD 16
R385 *1K_4

PROJECT : SA1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH8M HOST(1 of 4)	4A
Date: Friday, July 20, 2007	Sheet 14 of 43	

Place TX DC blocking caps close ICH8.

MiniCard-1 (WLAN)
MiniCard-2
Express Card (NEWCARD)

PCI-Express Direct Media Interface

SPI

USB

ICH8M REV 1.0

Layout Note:
DMI_IRCOMP_R<500mils

System
System
System
WEB CAM
CARDREADER
NEWCARD
MiniCard-1 (WLAN)
MiniCard-2(reserved)
FINGERPRINT CONNECTOR
BLUETOOTH

Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

ICH8 Boot BIOS select

Boot BIOS Strap

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

A16 SWAP Override strap

PCI_GNT3#	Low = A16 swap override enabled High = Default

SB-PCI

PCI

Interrupt I/F

Reserved for EMI. Place resister and cap close to ICH.

PCI Pullups

PROJECT : SA1
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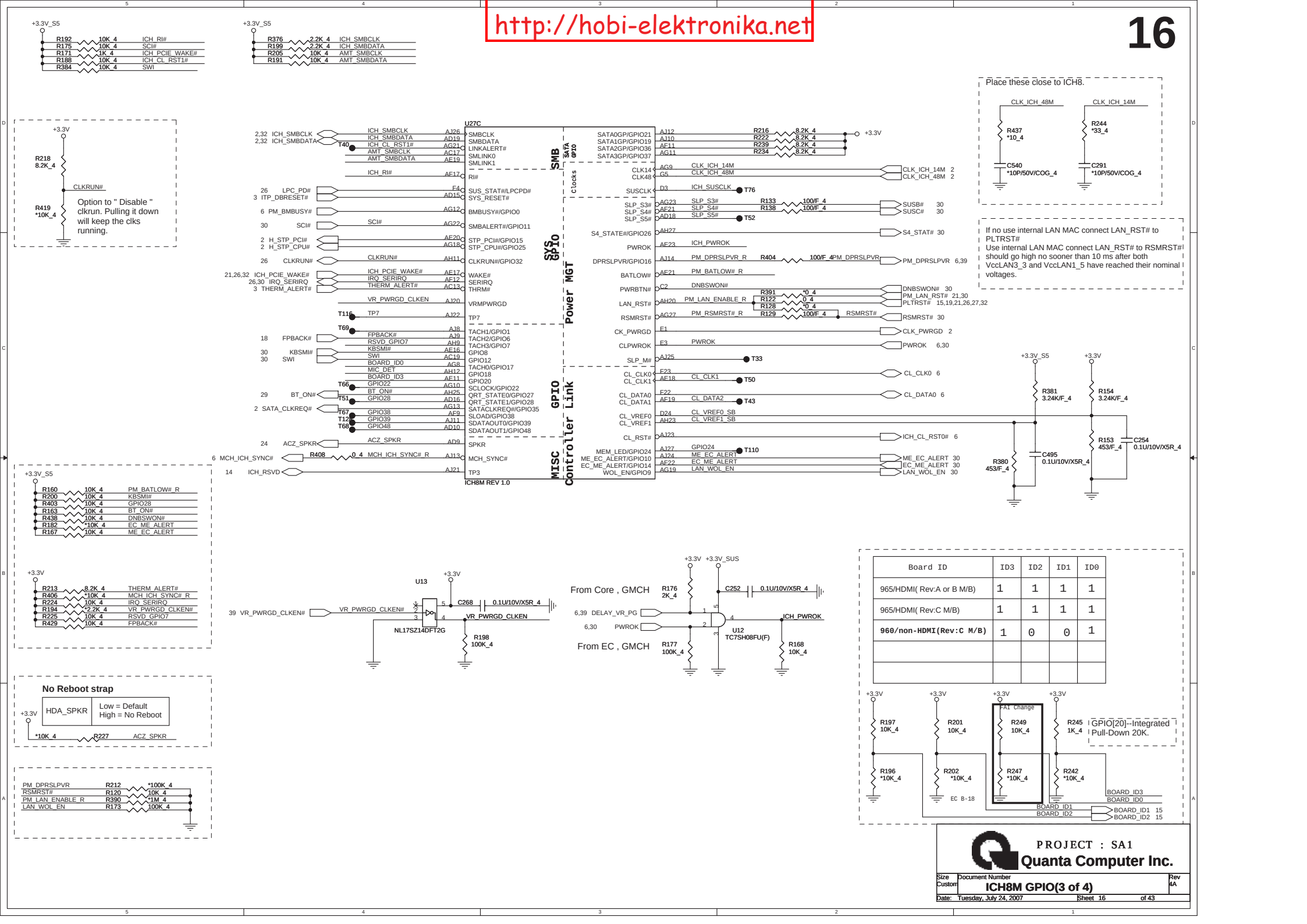
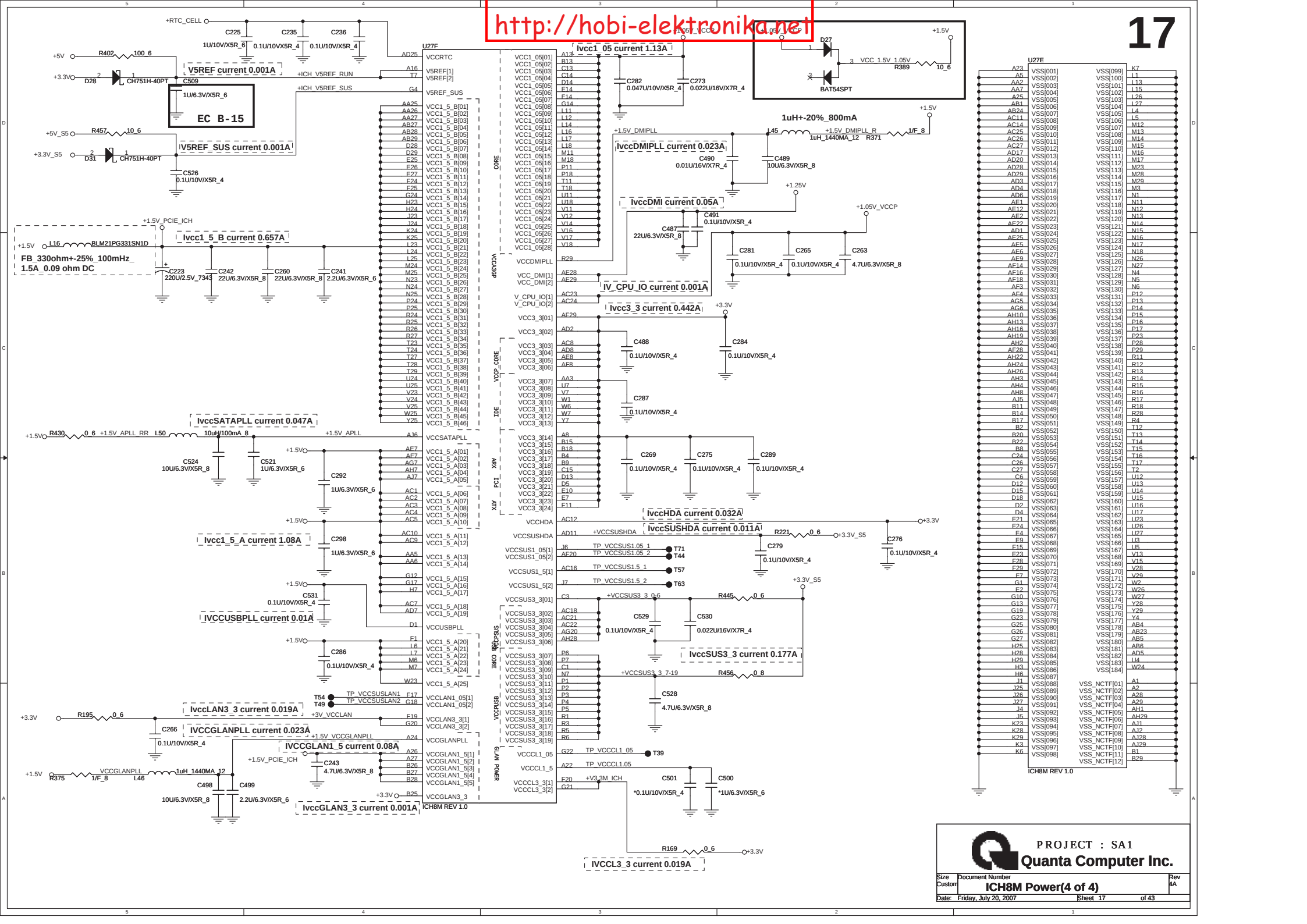
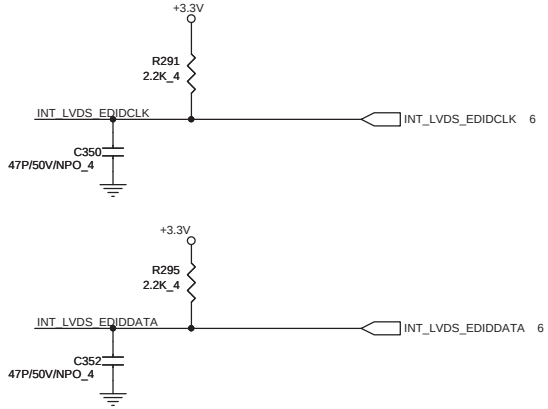
ICH8M PCIE(2 of 4)

Size: Custom | Rev: 4A
Date: Friday, July 20, 2007 | Sheet 15 of 43

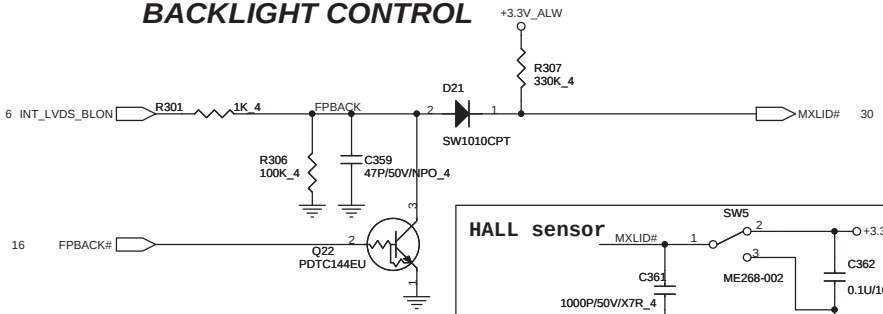


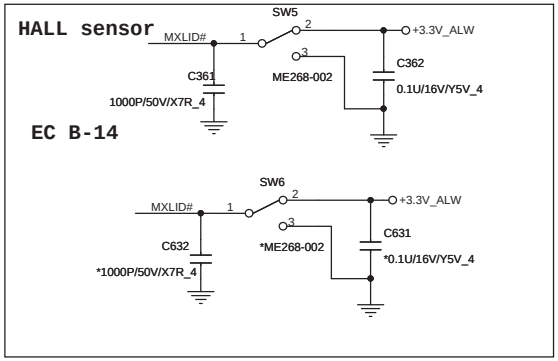


PROJECT : SA1	Quanta Computer Inc.
Size: Custom	Document Number: ICH8M Power(4 of 4)
Rev: 4A	
Date: Friday, July 20, 2007	Sheet 17 of 43

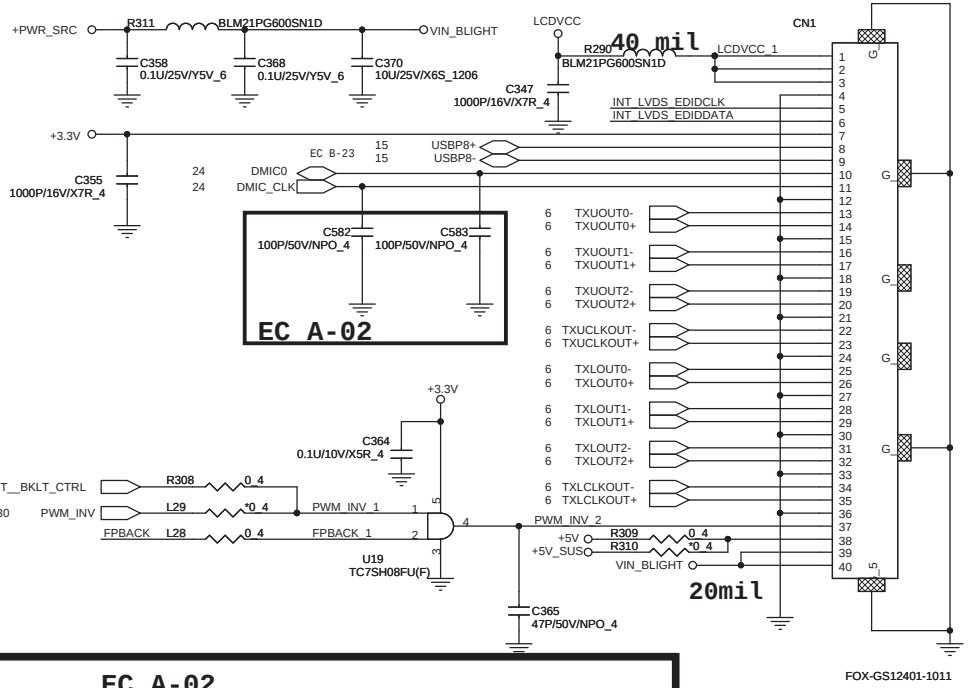


BACKLIGHT CONTROL



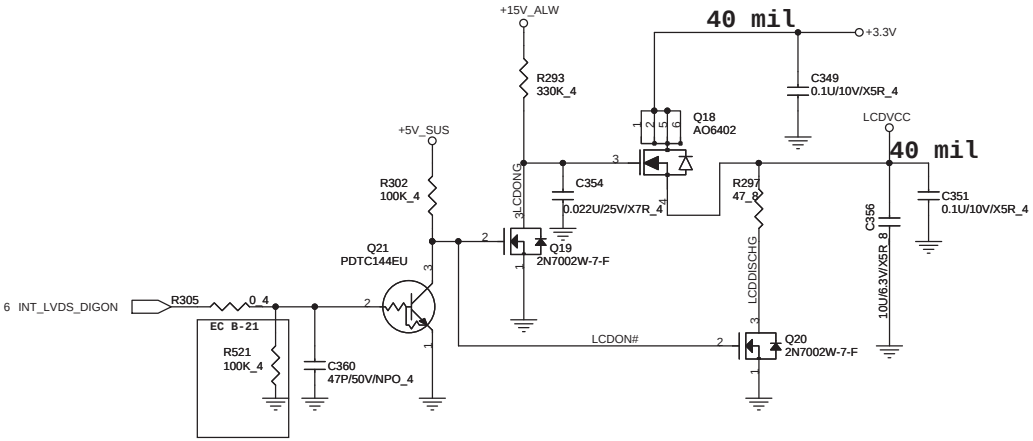


LCD CONNECTOR(Include WEB CAM function)



TO PANEAL

PANEL VCC CONTROL



PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LVDS/LCD CONN/LID/WEB CAM	4A
Date: Friday, July 20, 2007	Sheet 18	of 43

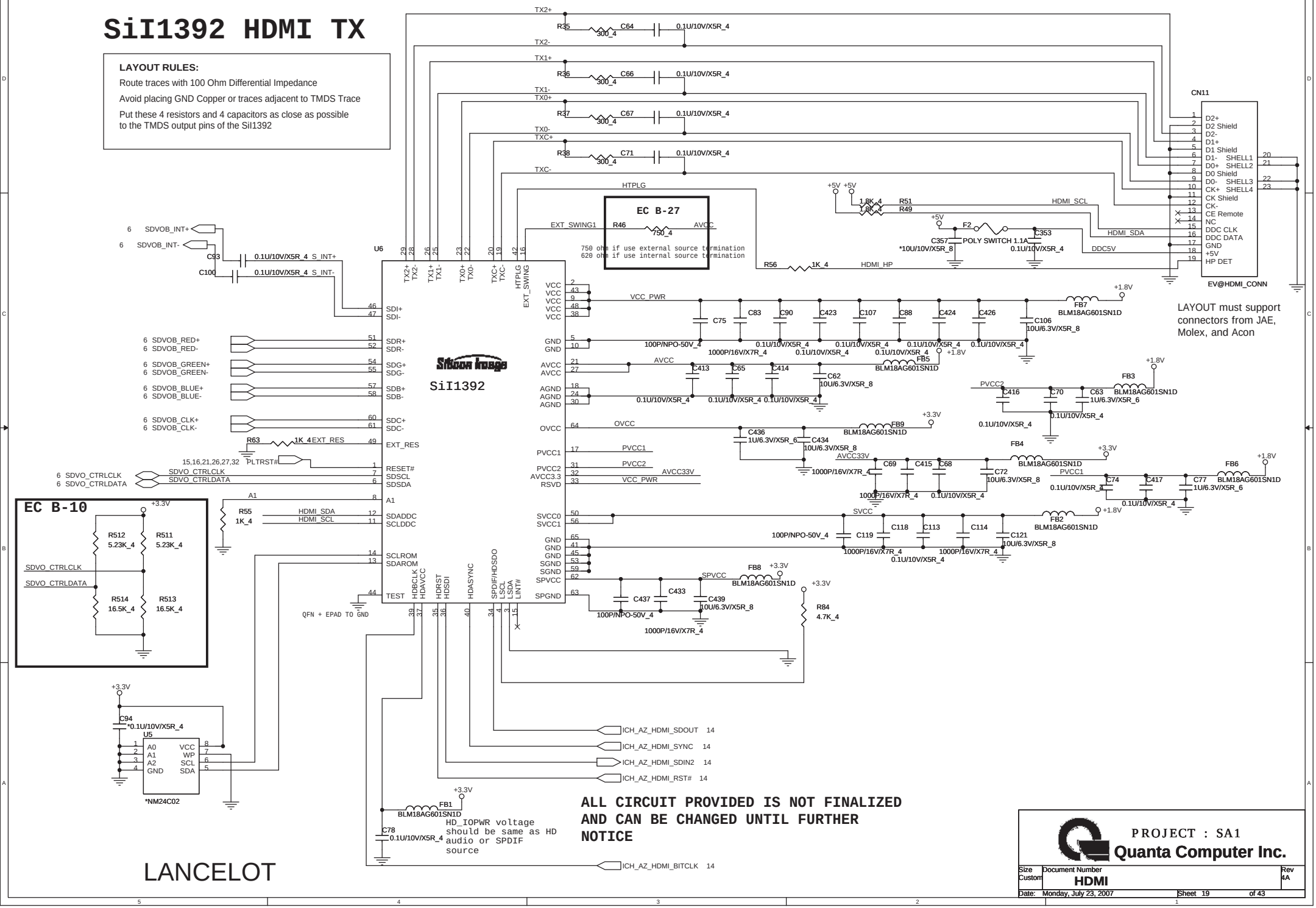
SiI1392 HDMI TX

LAYOUT RULES:

Route traces with 100 Ohm Differential Impedance

Avoid placing GND Copper or traces adjacent to TMDS Trace

Put these 4 resistors and 4 capacitors as close as possible to the TMDS output pins of the Sil1392



LANCELOT

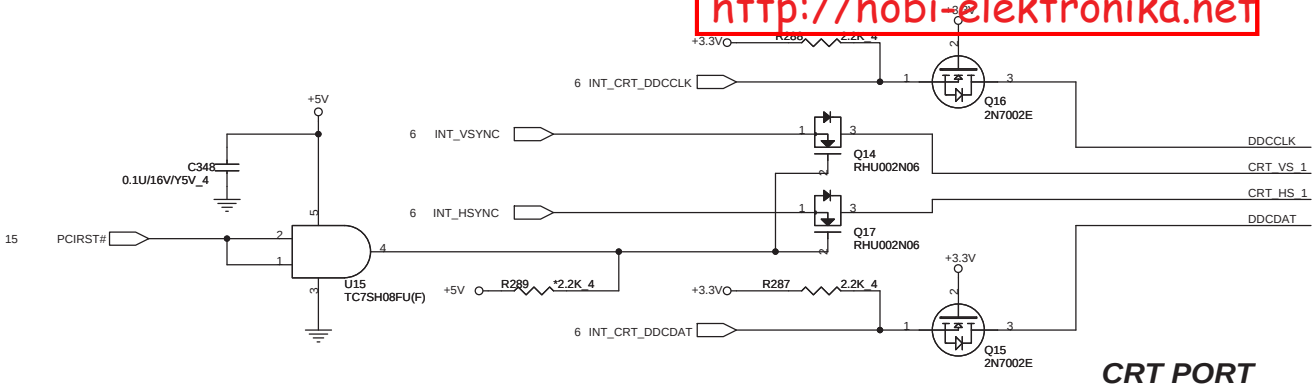
PROJECT : SA1

Quanta Computer Inc.

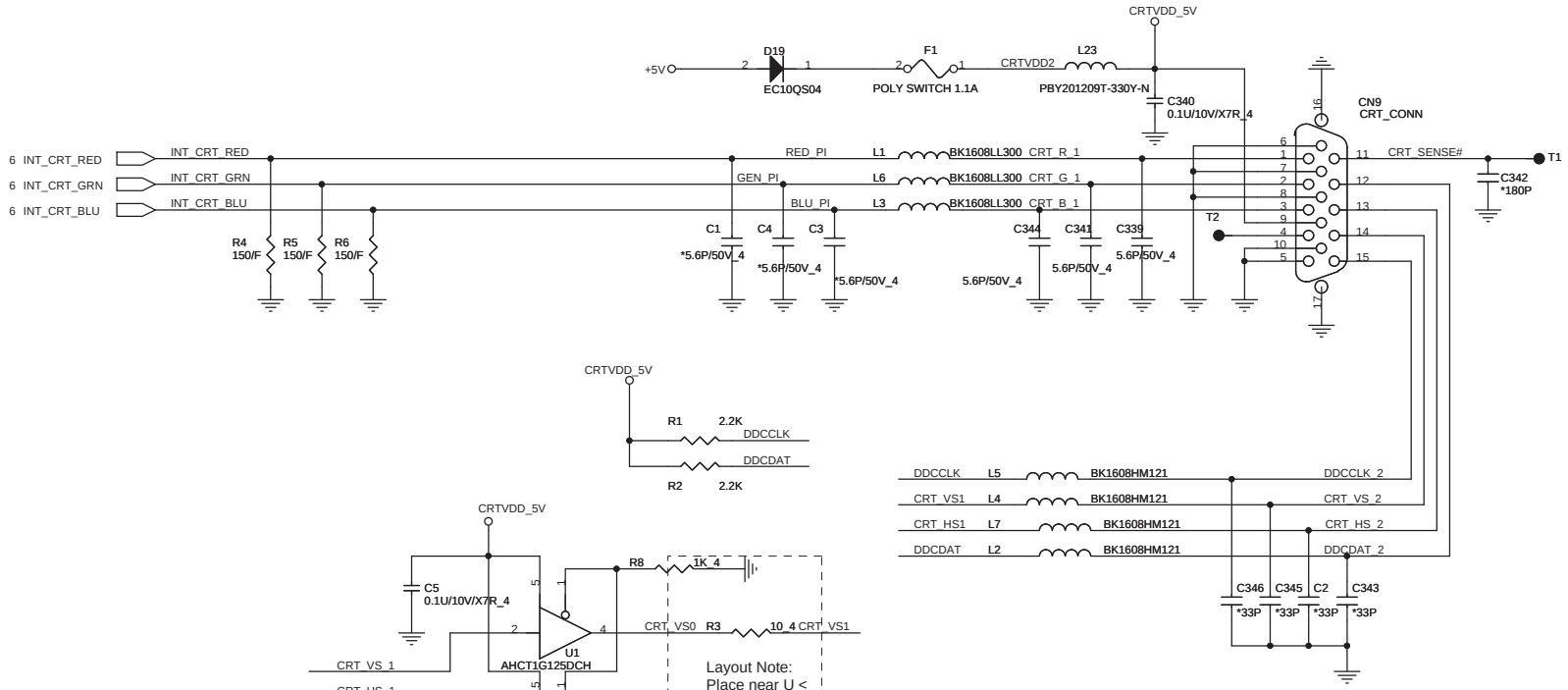
Size	Document Number	Rev
Custom	HDMI	4A

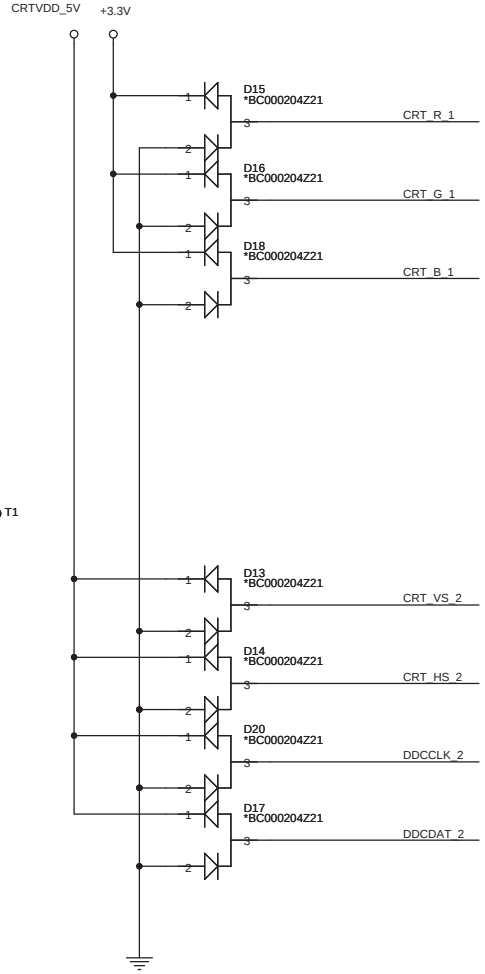
Date: Monday, July 23, 2007 Sheet 19 of 43

ESD PORTECTION



CRT PORT





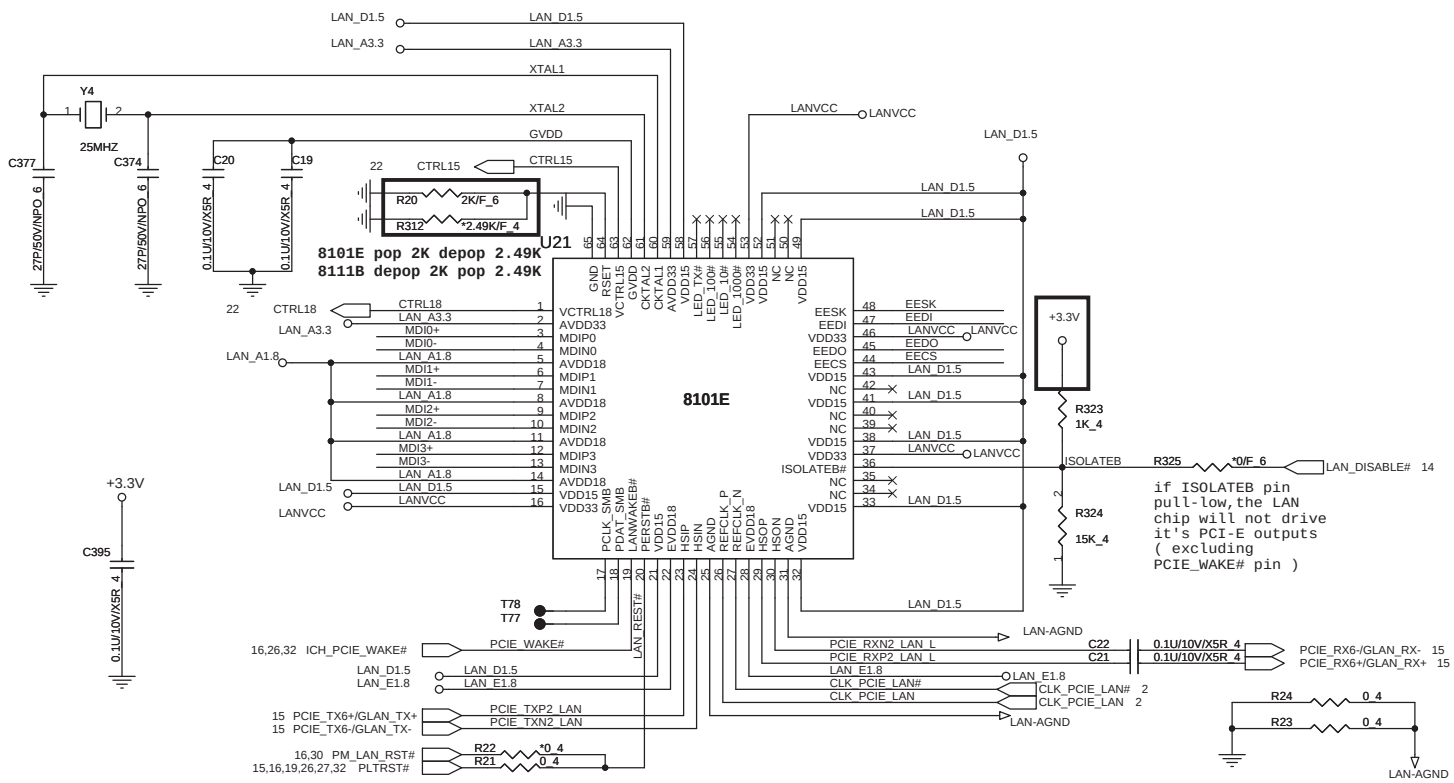
PROJECT : SA1

Quanta Computer Inc.

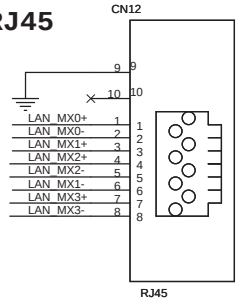
Size	Document Number	Rev
Custom	CRT PORT	4A

Date: Monday, July 23, 2007 Sheet 20 of 43

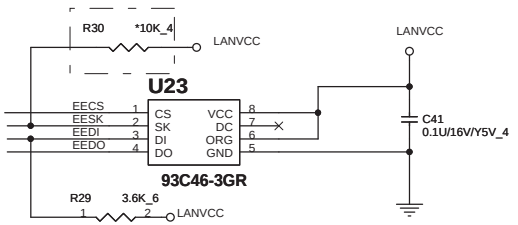
E : Stuffed for 8101E(10/100)

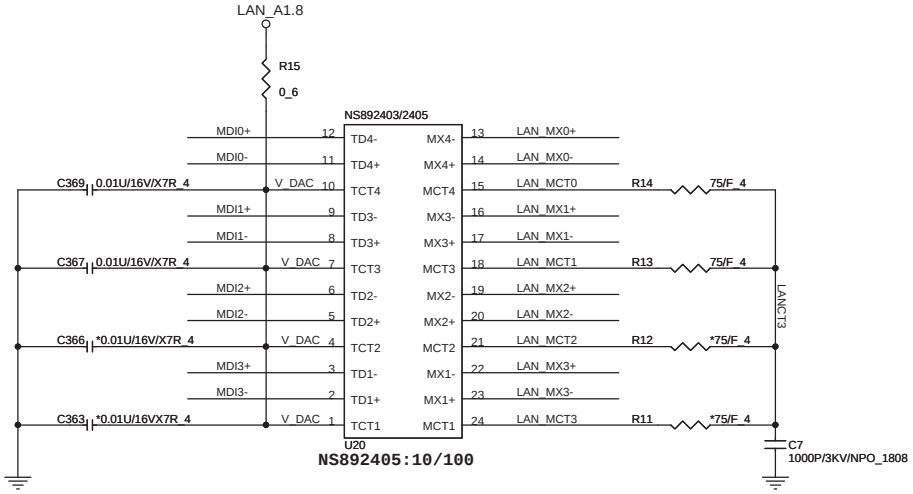


RJ45

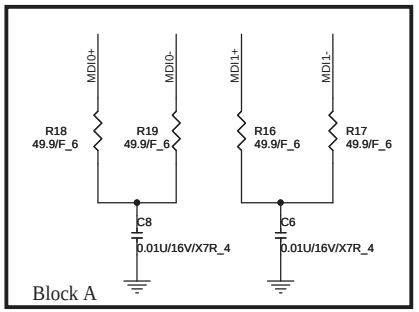


for 93C56 used. NC if 93C46 is used.





BLOCK A is only for RTL8101E application.



	10/100M	1G
R14 R15 R16 R17	ASM	NoASM

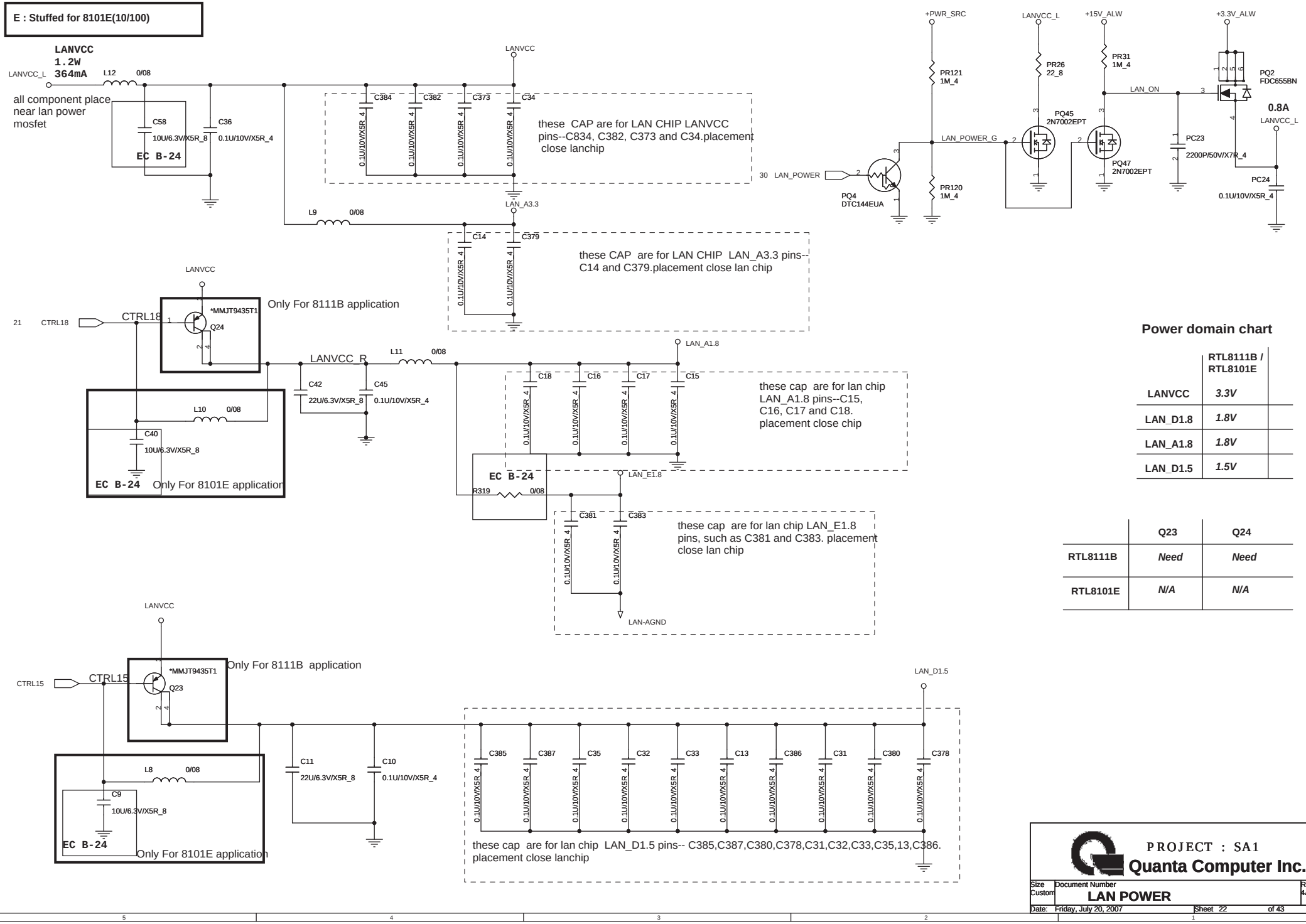
PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN-REALTEK 8101E	4A
Date: Monday, July 23, 2007	Sheet 21	of 43

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)



Power domain chart

	RTL8111B / RTL8101E
LANVCC	*3.3V*
LAN_D1.8	*1.8V*
LAN_A1.8	*1.8V*
LAN_D1.5	*1.5V*

	Q23	Q24
RTL8111B	*Need*	*Need*
RTL8101E	*N/A*	*N/A*

PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN POWER	4A
Date: Friday, July 20, 2007	Sheet 22	of 43

Note:

	SD/MMC	MS	XD
SP0			
SP1	SD_WP		XD_CD#
SP2			
SP3	SD_CD#		
SP4			XD_D4
SP5		MS_BS	XD_D5
SP6	SD_DAT1	MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

U14

Realtek RTS5158

EC A-05

7 IN1 CARD-READER (PUSH-PUSH)

Support SD/MS/xD/SM/RS-MMC/MMC/miniSD Cards

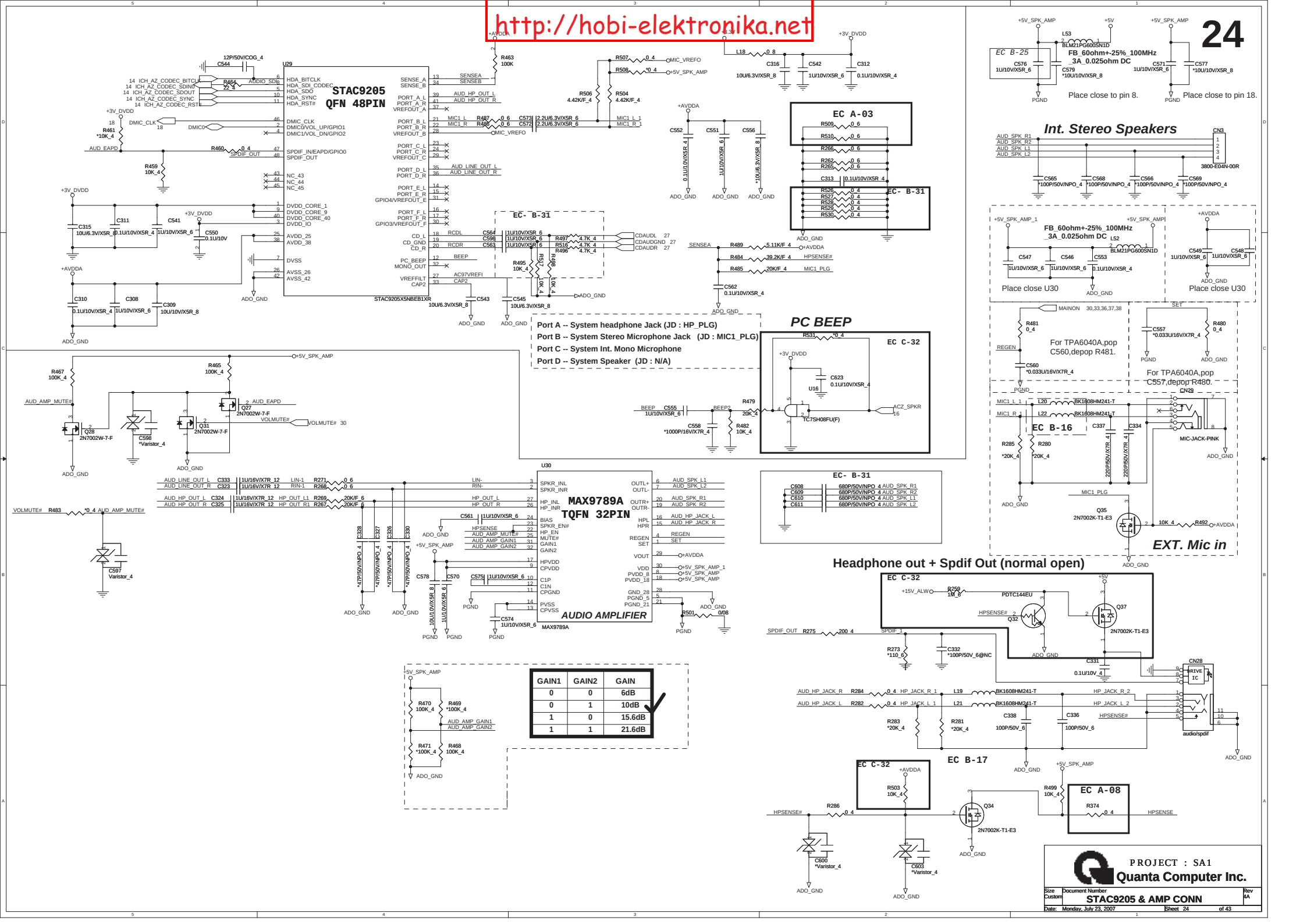
CN8

R015-212-LM

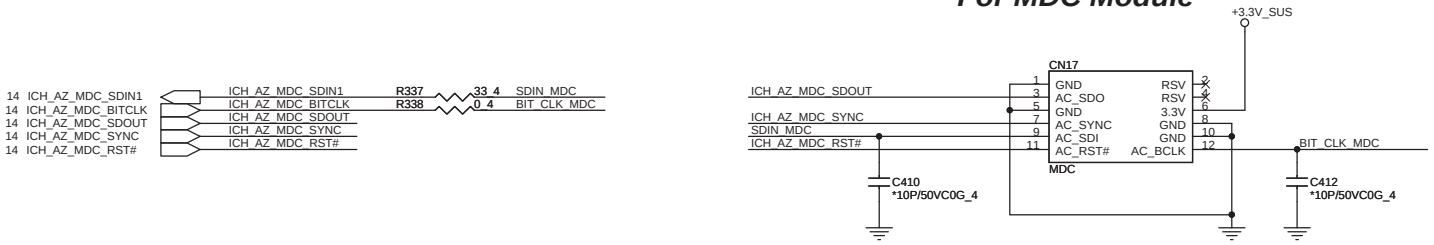
PROJECT : SA1

Quanta Computer Inc.

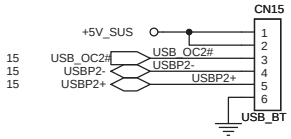
Size	Document Number	Rev
Custom	RTS5158 CONTROLLER	4A
Date: Friday, July 20, 2007	Sheet 23	of 43



For MDC Module



TO RJ11/USB PORT



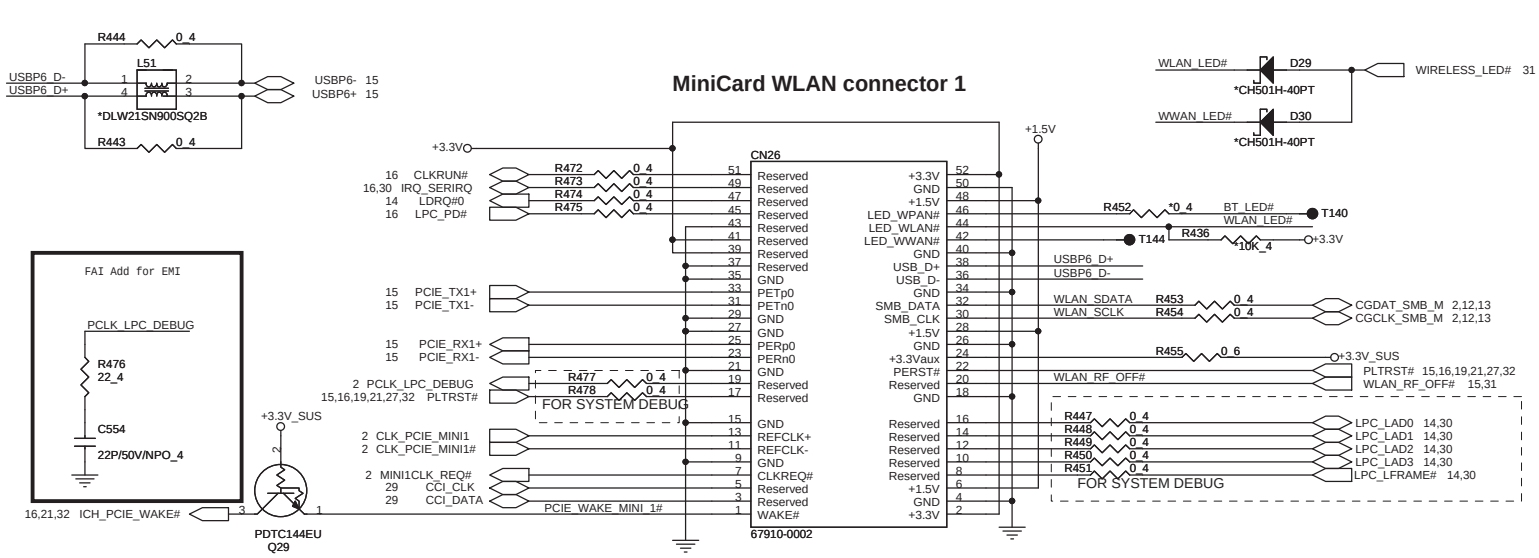
PROJECT : SA1

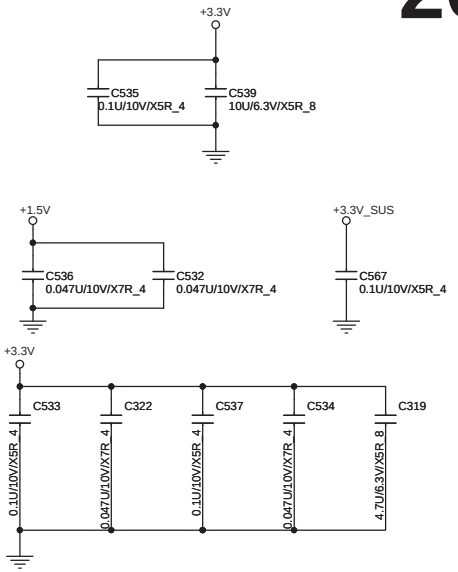
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MODEM(MDC)	4A

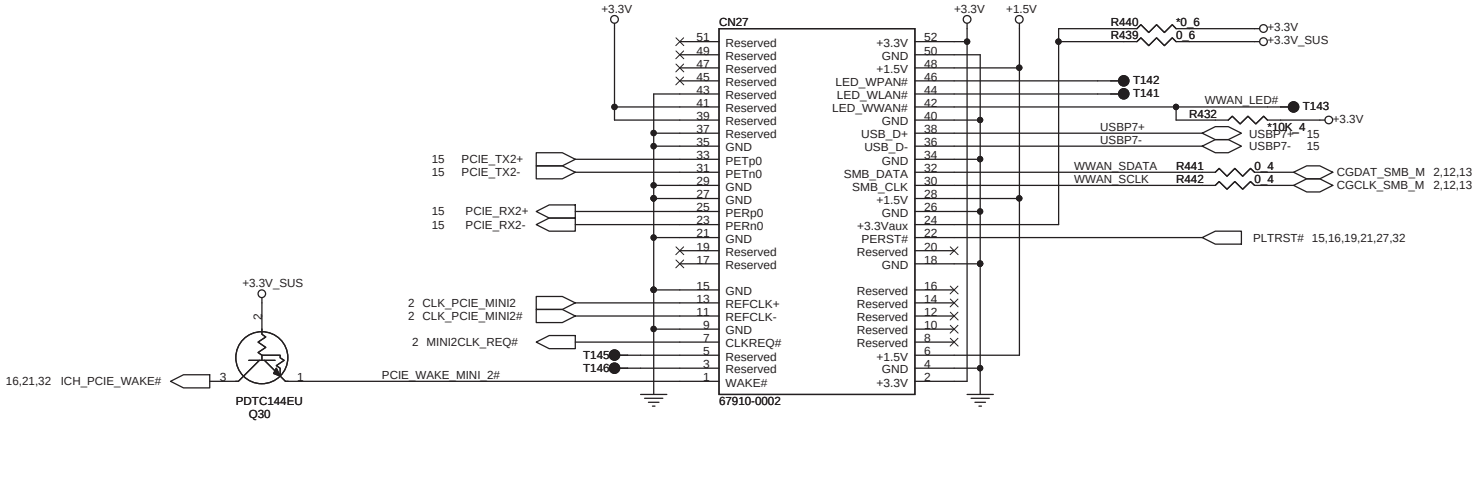
Date: Friday, July 20, 2007 Sheet 25 of 43

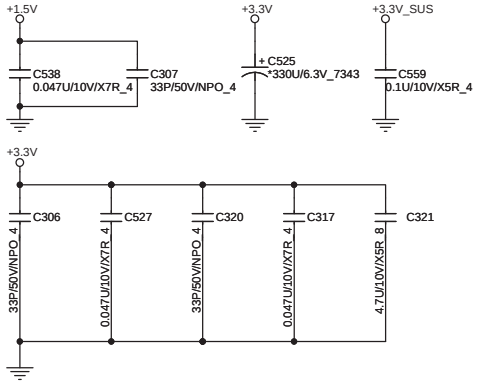
MiniCard WLAN connector 1





MiniCard connector 2





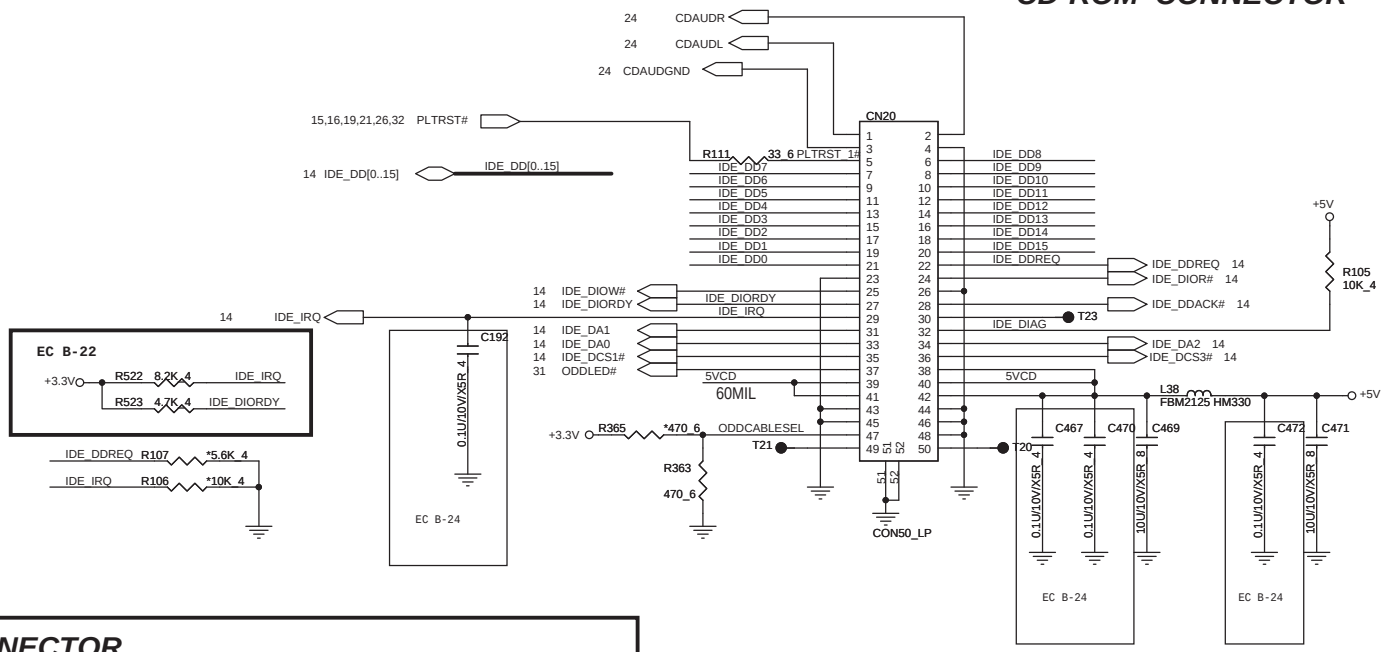
PROJECT : SA1

Quanta Computer Inc.

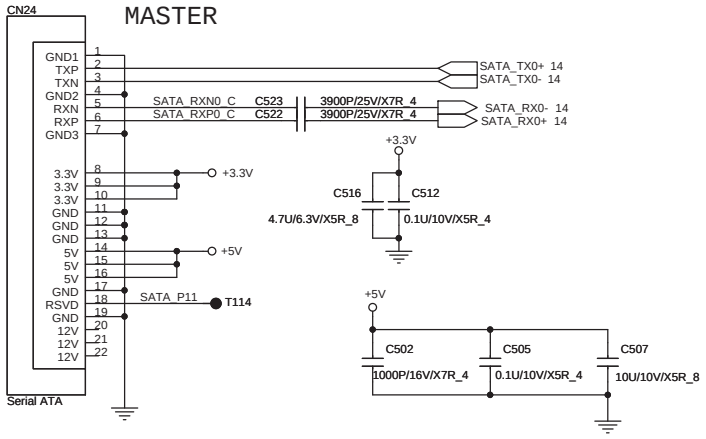
Size	Document Number	Rev
Custom	MiniCard connector	4A
Date: Monday, July 23, 2007	Sheet 26	of 43

For fix ODD

CD-ROM CONNECTOR



SATA CONNECTOR

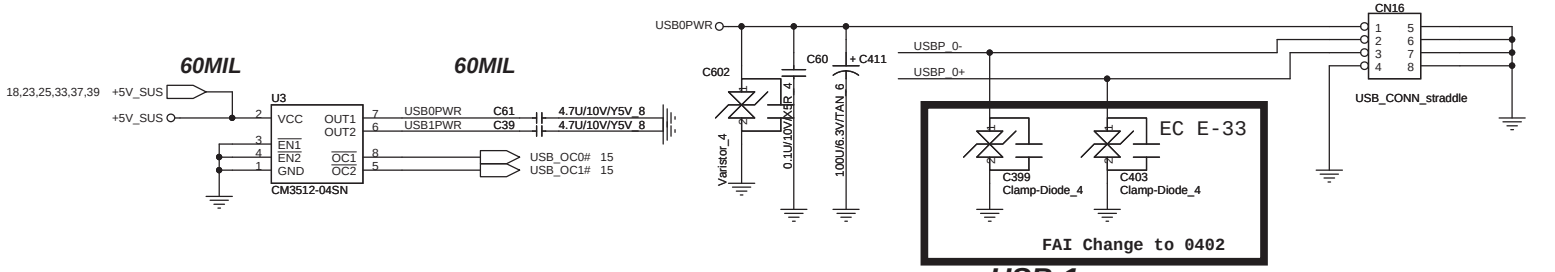


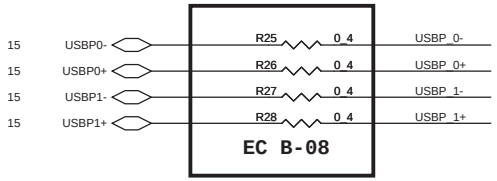
PROJECT : SA1

Quanta Computer Inc.

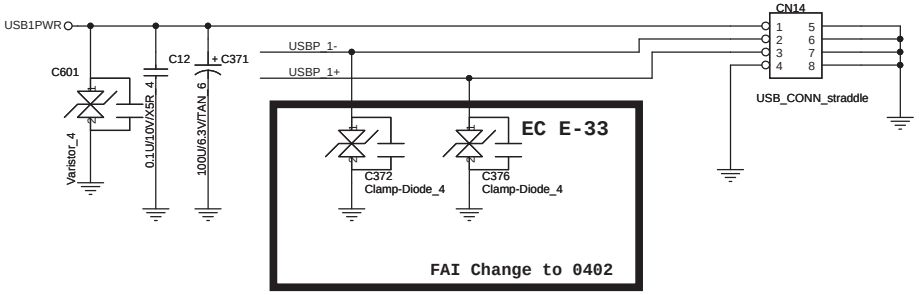
Size	Document Number	Rev
Custom	SATA HDD,ODD,USB	4A
Date: Monday, July 23, 2007	Sheet 27	of 43

USB-0



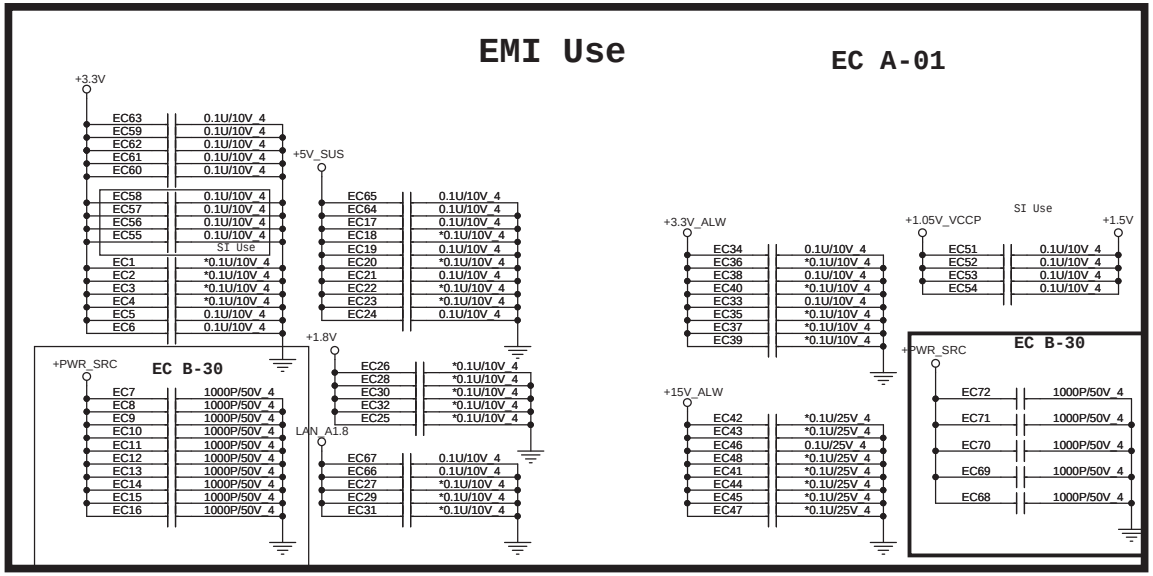


USB-1



EMI Use

EC A-01

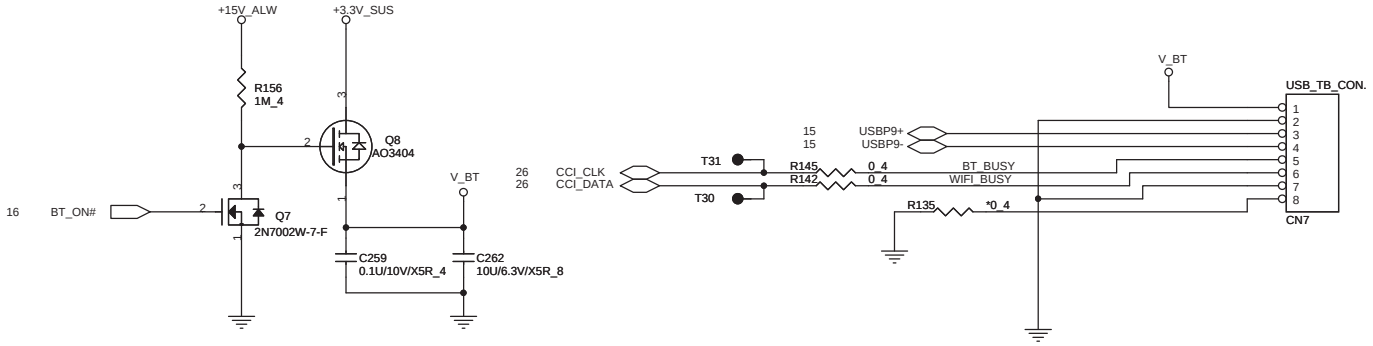


PROJECT : SA1

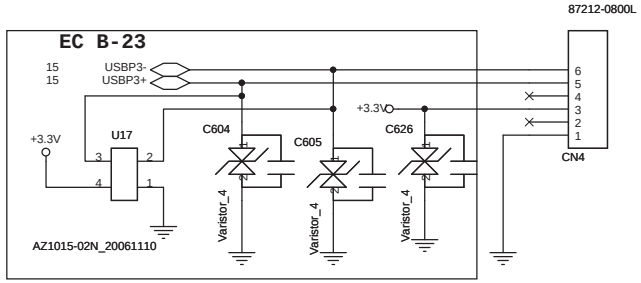
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB PORT	4A
Date: Monday, July 23, 2007	Sheet 28	of 43

BLUETOOTH CONNECTOR



FINGERPRINT CONNECTOR



PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLUETOOTH	4A

Date: Tuesday, July 24, 2007 Sheet 29 of 43

IT8512

POWER SWITCH

RF ON/OFF SLIDE SWITCH

8Mbit (1M Byte), SPI

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

TMKBC Function	
High	Enable
Low	Disable

R3444	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC" minimum trace width 12mils.

Layout Note:
Place R428,R416,R420 within 500 mils from SPI Flash.

Please reserve this connector for serial debug port & KBS download usage.

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

EC B-13

EC B-11

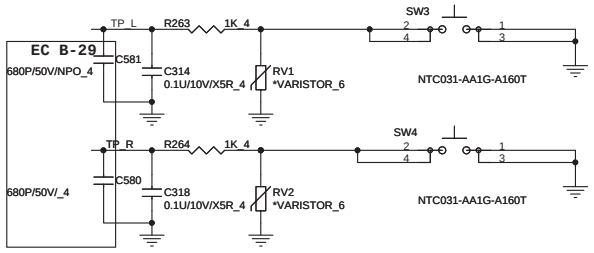
(For PLL Power)

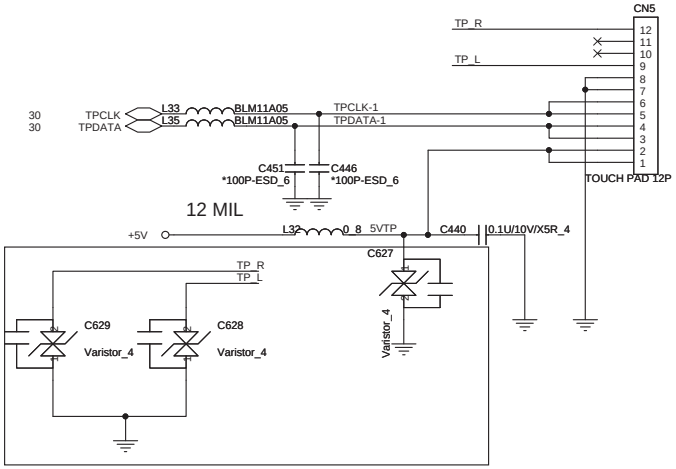
Place close to EC,

PROJECT : SA1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBC-IT8512	4A
Date: Monday, July 23, 2007	Sheet 30	of 43

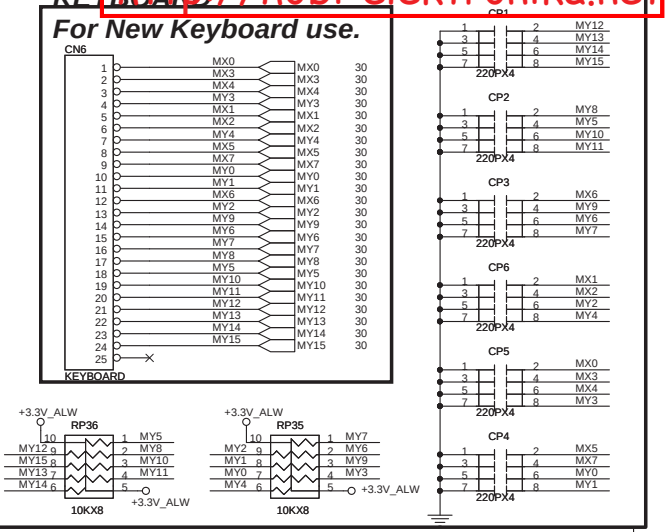
TOUCHPAD SWITCH CONN



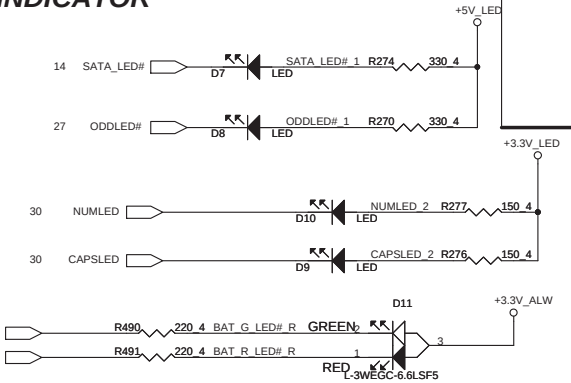


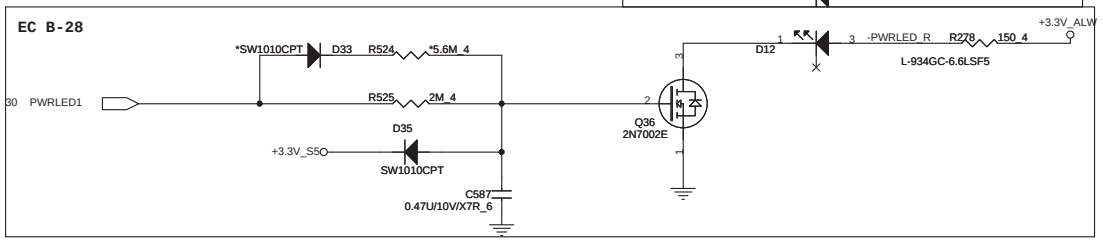
KEYBOARD

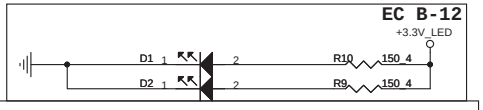
For New Keyboard use.

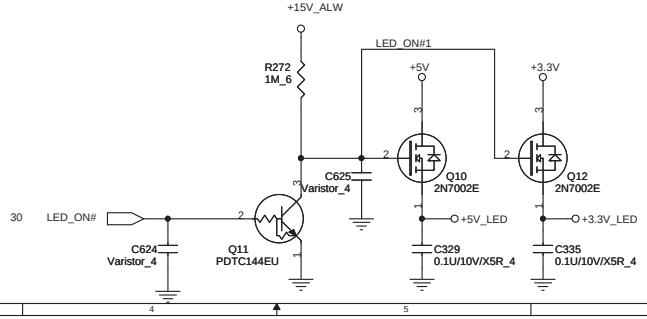


LED INDICATOR

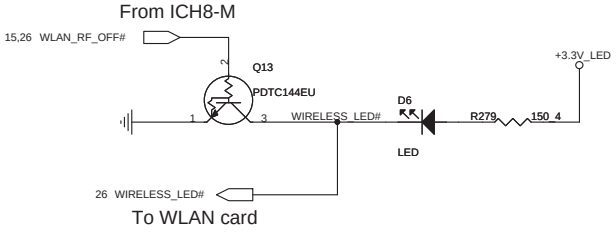


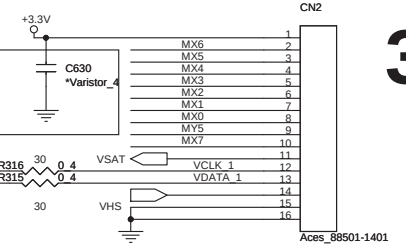


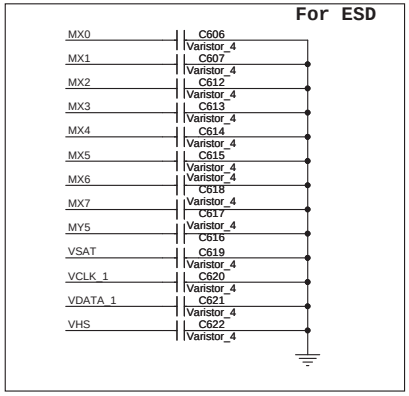




WIRELESS LED







SWITCH/Volume cintral BOARD

PROJECT : SA1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TP/KB/LED/SW. BOARD	4A
Date: Monday, July 23, 2007	Sheet 31	of 43

NEWCARD

15 USBP5-
15 USBP5+
R462 1 2 0_4 USBCONP5-
R458 1 2 0_4 USBCONP5+

+3.3V
CPUSB# R141 10K_4
CPPE# R140 10K_4
2231_SHDN# R121 10K_4
2231_STBY# R117 10K_4

1.35A need 60 mil

3V_NEWCARD

CN23

USBCONP5-
USBCONP5+
CPUSB#
2,16 ICH_SMBCLK
2,16 ICH_SMBDATA
0.75A need 30~40 mil
1.5V_NEWCARD
16,21,26 ICH_PCIE_WAKE#
3VAUX
PERST#
2 NEW-CARD_CLK_REQ#
R241 1 2 0_4 CLK_NEW_OE#
CPPE#
2 CLK_PCIE_NEW_C#
2 CLK_PCIE_NEW_C
15 PCIE_RXN3
15 PCIE_RXP3
15 PCIE_TXN3
15 PCIE_TXP3

1	GND4		
2	USB_D-		
3	USB_D+		
4	CPUSB#		
5	RESERVED2		
6	RESERVED1		
7	SMB_CLK		
8	SMB_DATA		
9	+1.5V2		
10	+1.5V1		
11	WAKE#		
12	+3.3VAUX		
13	PERST#		
14	+3.3V2		
15	+3.3V1		
16	CLKREQ#		
17	CPPE#		
18	REFCLK-		
19	REFCLK+		
20	GND3		
21	PERn0		
22	PERp0		
23	GND2	SHIELD4	30
24	PETn0	SHIELD3	29
25	PETp0	SHIELD2	28
26	GND1	SHIELD1	27

331-1CX43201-ZG-X2_NEW_CARD

U9

+3.3V_SUS
3VAUX
2231_STBY# 1
17 AUXIN
15 AUXOUT
CP_RST# 6
CPPE# 10
CPUSB# 9
PERST# 8
2231_SHDN# 20
RCLKEN 18
OC# 19
7

STBY# 3.3VIN 2 +3.3V
AUXIN 3.3VIN 4
SYSRST# 1.5VIN 12 +1.5V
CPPE# 1.5VIN 14
CPUSB#
PERST# 3.3VOUT 3 3V_NEWCARD **1.35A need 60 mil**
SHDN# 3.3VOUT 5
RCLKEN
OC# 1.5VOUT 11 1.5V_NEWCARD
GND 1.5VOUT 13 **0.75A need 30~40 mil**

R5538

T29 *PAD
T28 *PAD
R131 *10K_4
R125 *0_4

+3.3V_SUS
C224 0.1U/10V/X5R_4
15,16,19,21,26,27 PLTRST#
U8 TC7SH08FU(F)
CP_RST#

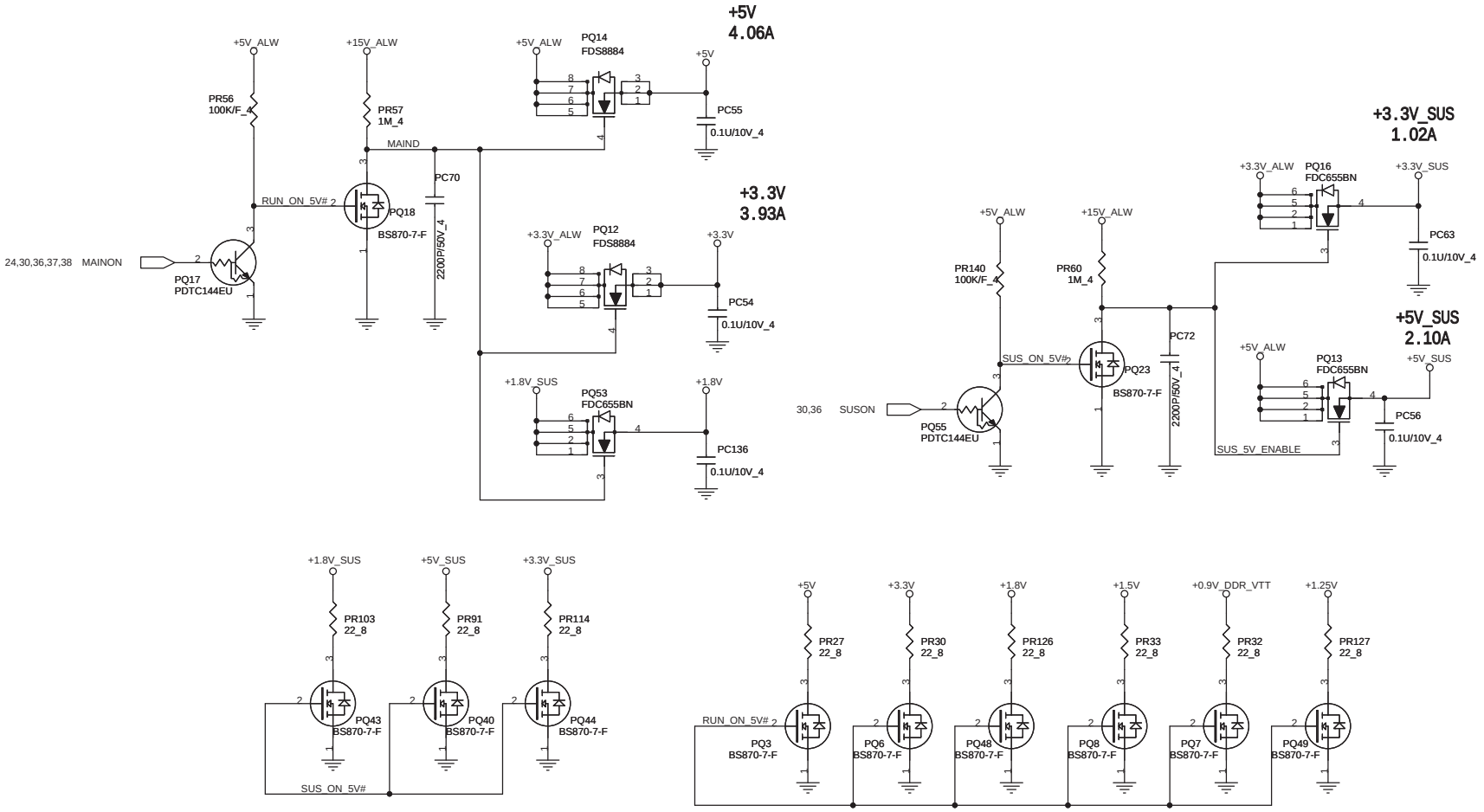
3V_NEWCARD
3VAUX
1.5V_NEWCARD

C221 0.1U/10V/X5R_4
C222 0.1U/10V/X5R_4
C240 0.1U/10V/X5R_4
C239 0.1U/10V/X5R_4
C238 0.1U/10V/X5R_4
C237 0.1U/10V/X5R_4

EC B-24

PROJECT : SA1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD	4A
Date: Monday, July 23, 2007	Sheet 32	of 43

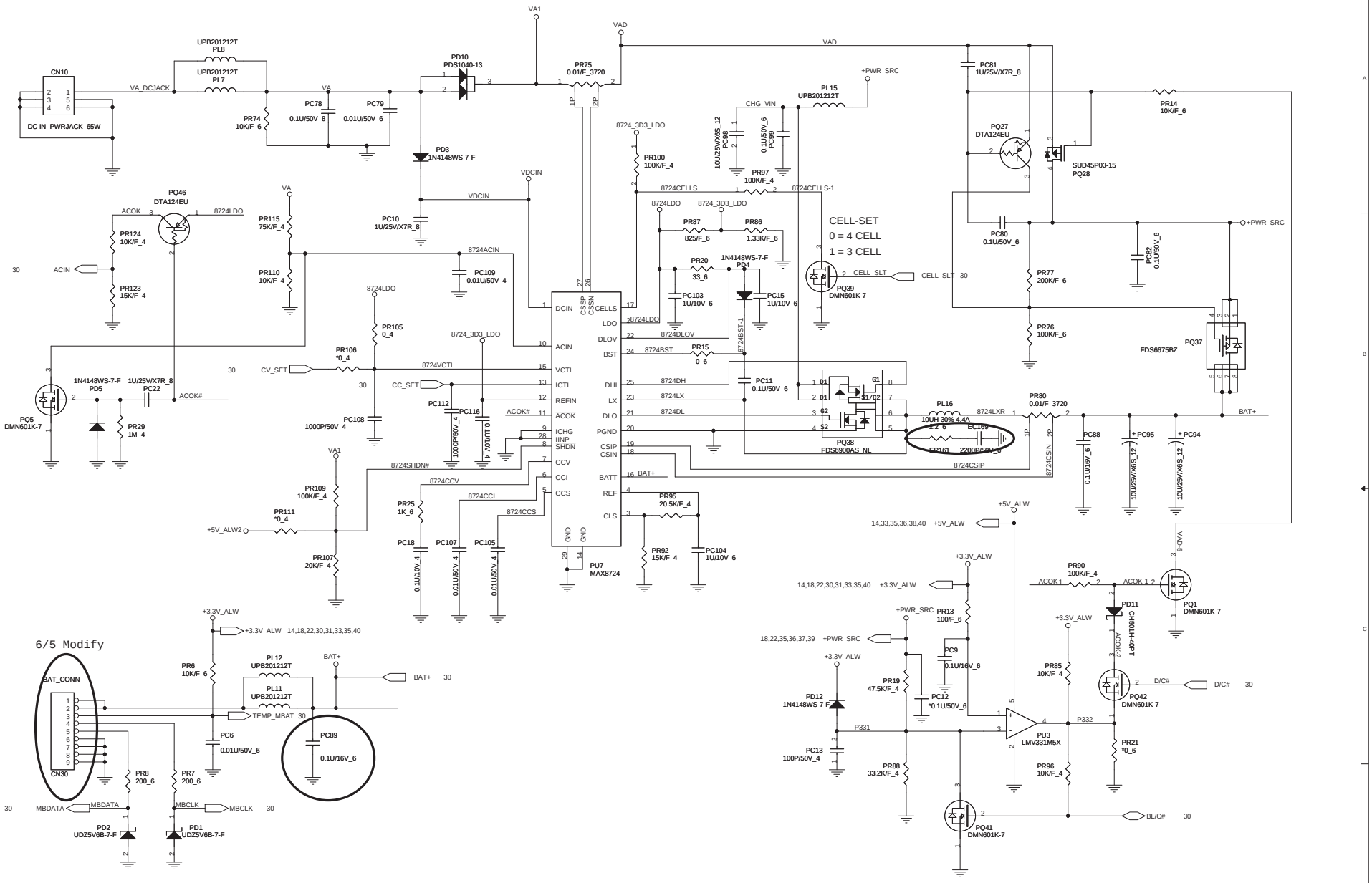


PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	RUN POWER SW & DISCHARGE	4A

Date: Monday, July 23, 2007 Sheet 33 of 43

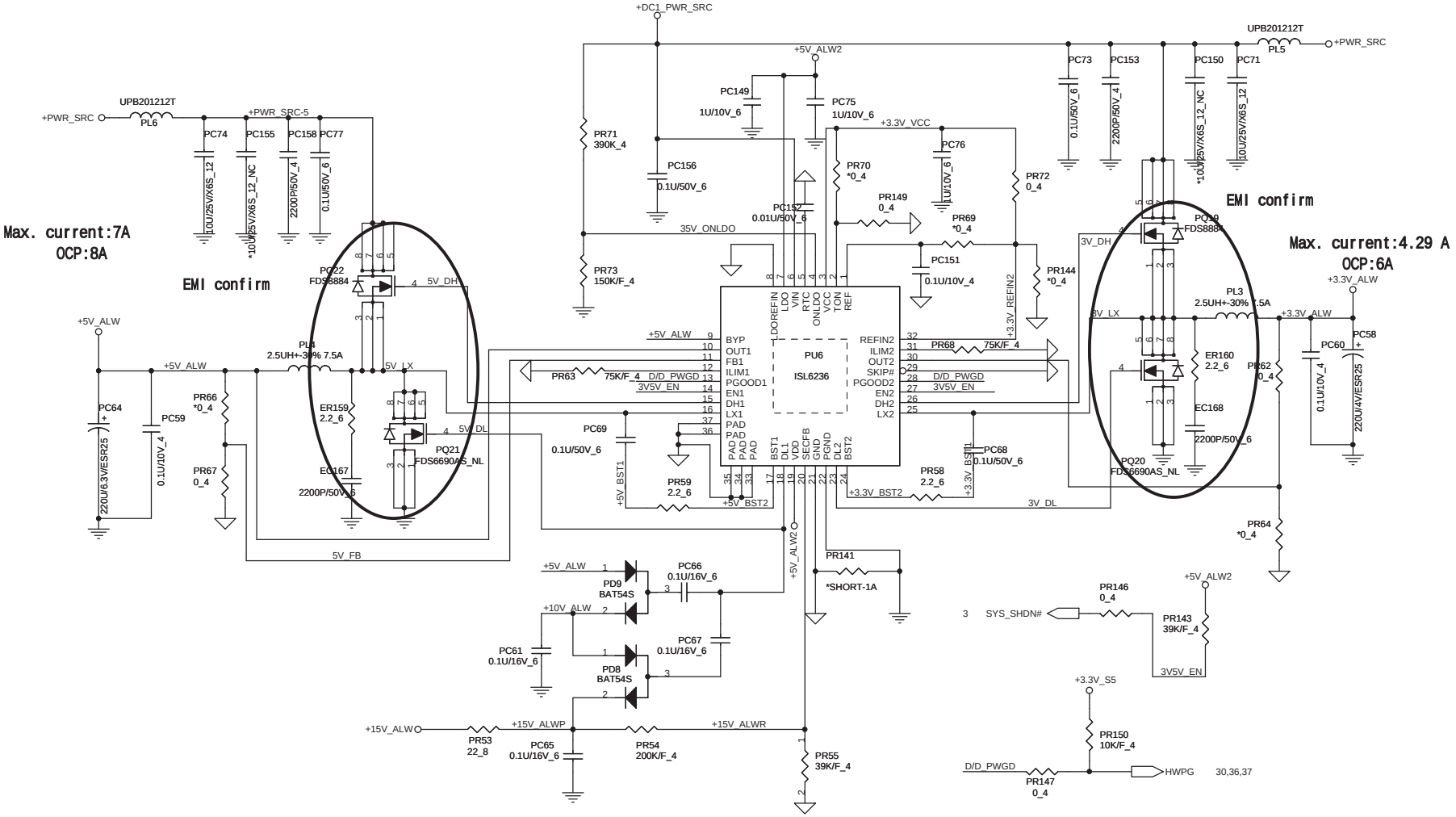


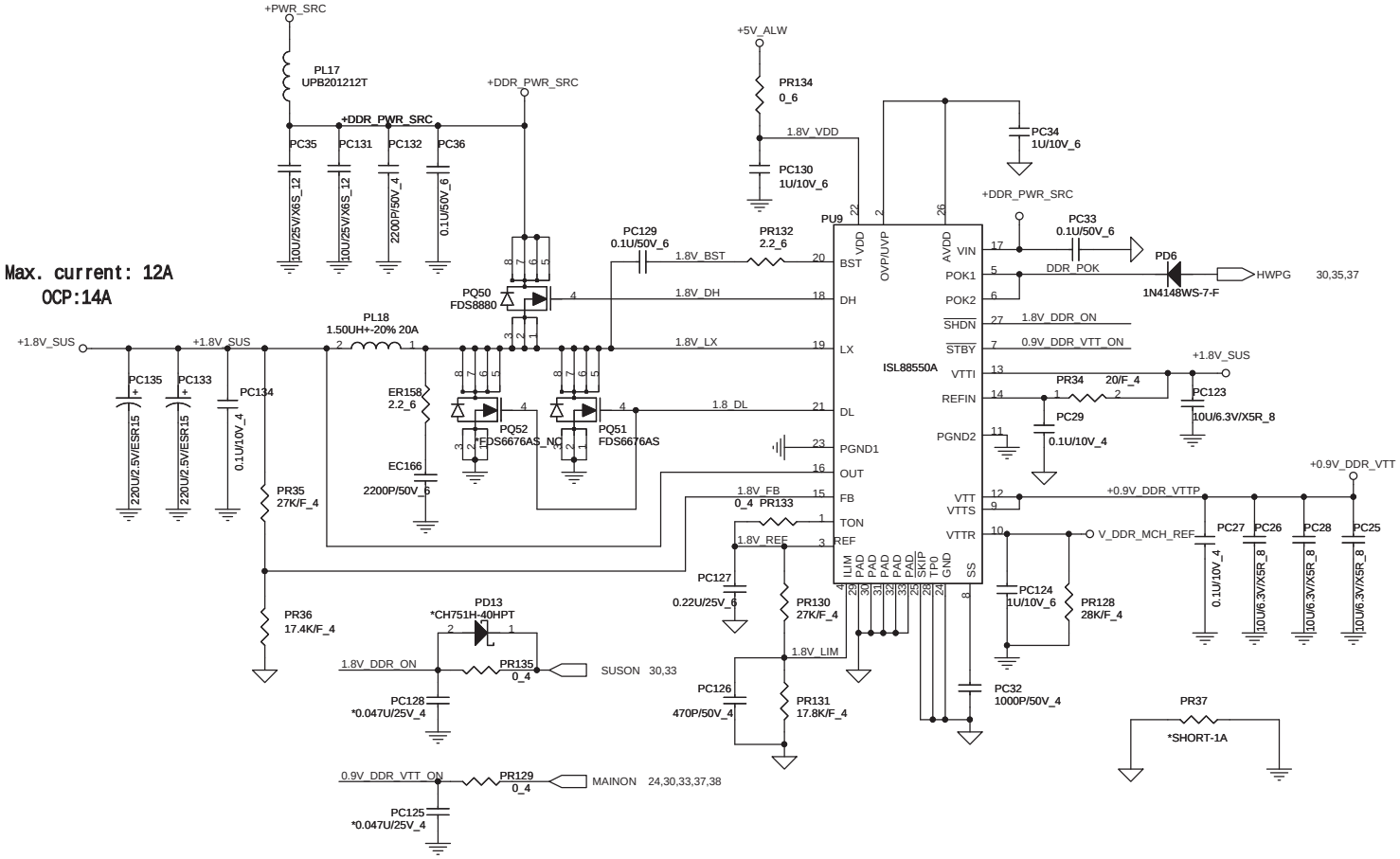
PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHARGER	4A

Date: Friday, July 20, 2007 Sheet 34 of 43

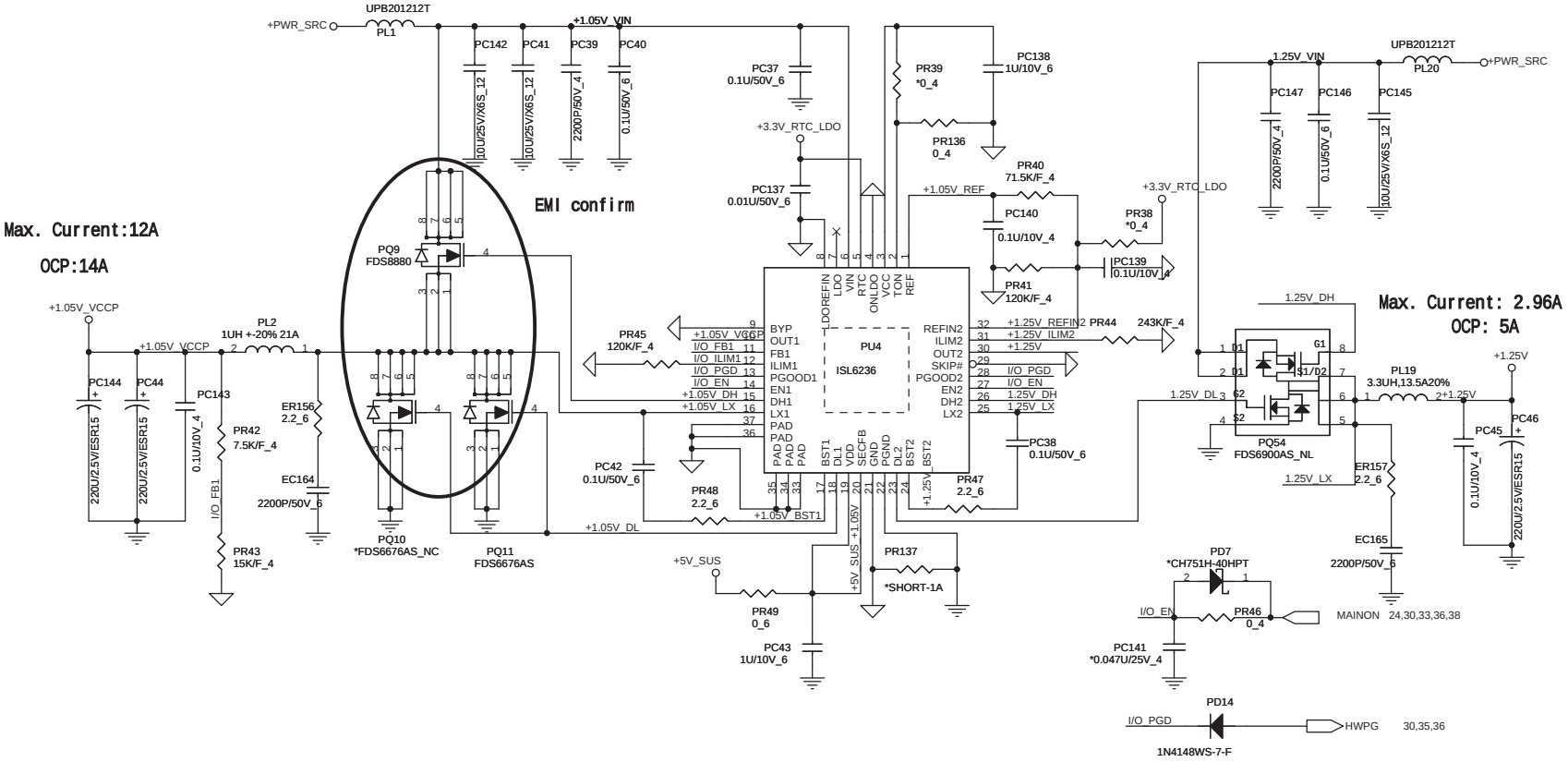




PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.8V_SUS & +0.9V_DDR_VTT	4A
Date: Friday, July 20, 2007	Sheet 36 of 43	

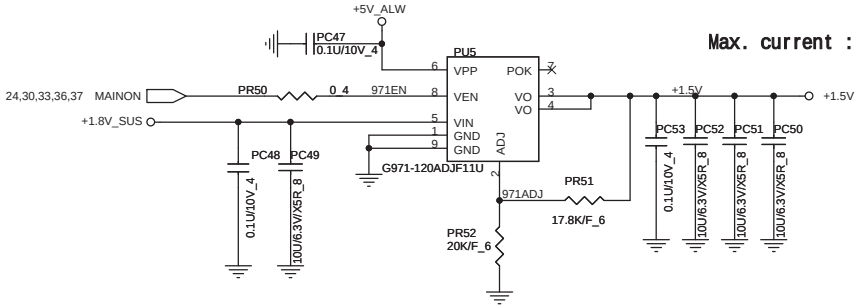


PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.25V & +1.05VCCP	4A

Date: Friday, July 20, 2007 Sheet 37 of 43



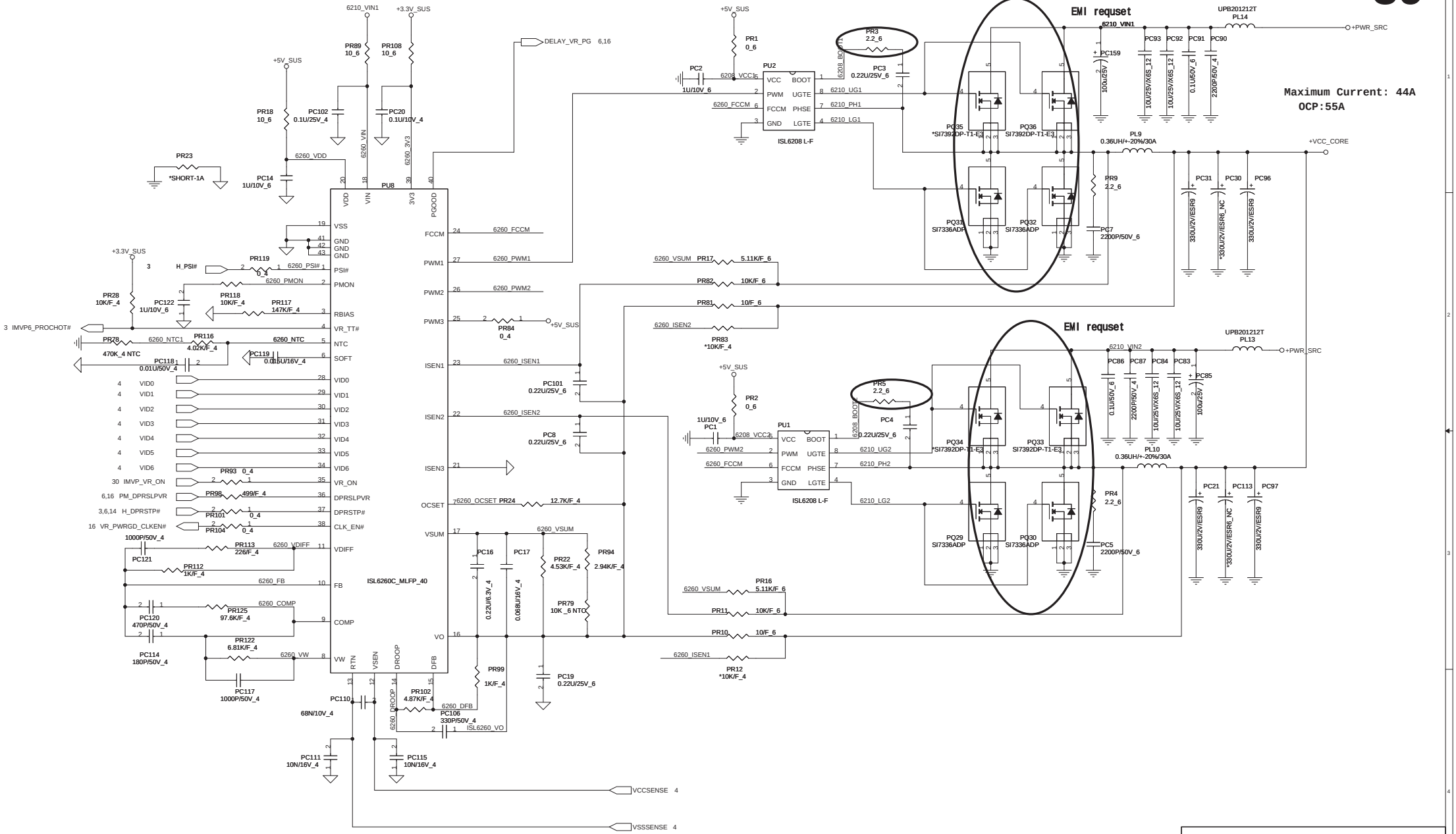
Max. current : 2.76A

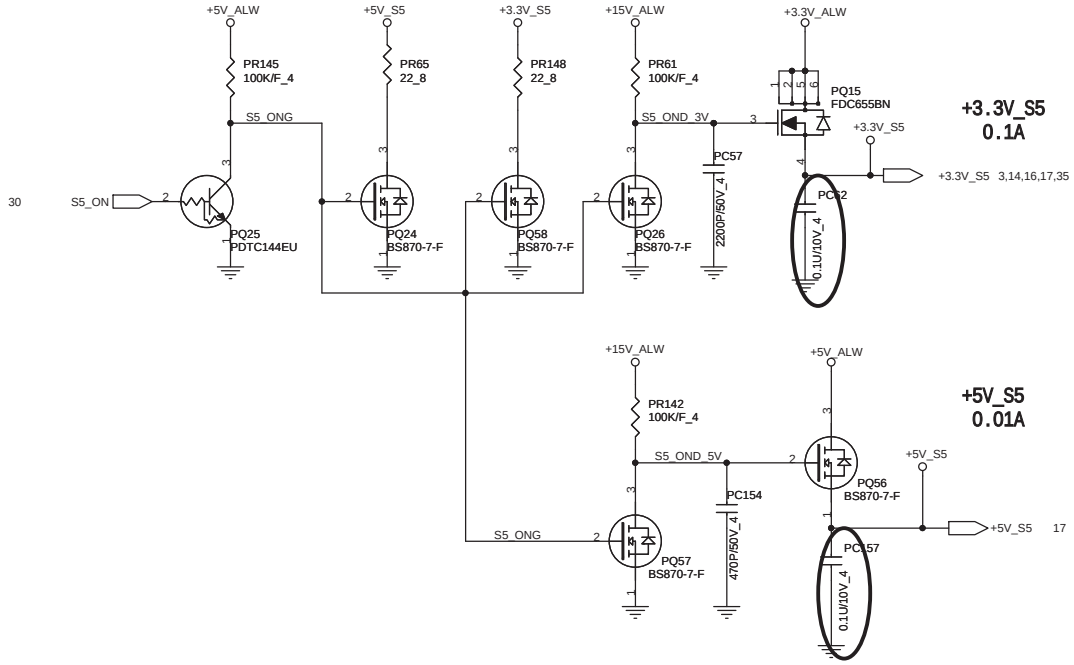
Vout =0.8(1+R1/R2) = 0.8(1+17.8K/20K) = 1.512V

PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.5V	4A
Date: Friday, July 20, 2007	Sheet 38	of 43

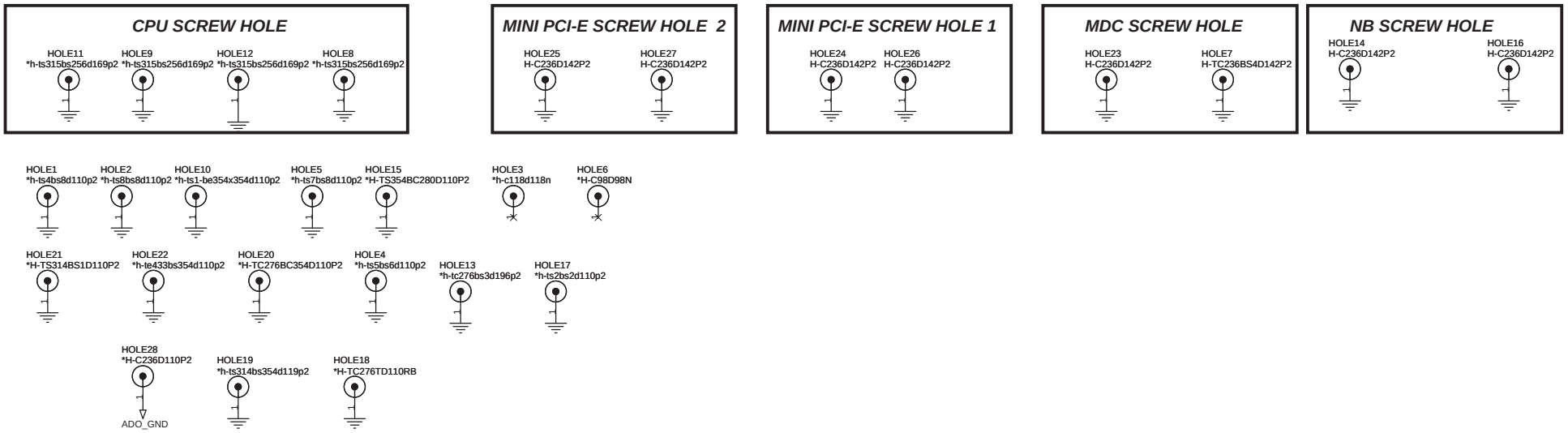




PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	+3V_S5/+5V_S5	4A
Date: Friday, July 20, 2007	Sheet 40	of 43



PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	EMI PAD & Hole	4A
Date: Friday, July 20, 2007	Sheet 41 of 43	

EC A-01 /28 Add EMI EC1~EC52 for EMI use

EC A-02 /18 Add EMI EC49, EC50,C582,C583 for EMI use.

EC A-03 /24 Add EMI R509,R510 for EMI use.

EC A-04 /21 CN12 Pin9 and Pin10 connect to GND

EC A-05 /23 Change All SP0~SP19 0 ohm to 33 Ohm

EC A-06 /14 Add EMI request C589~C593

EC A-07 /6 Add EMI request C594~C595

EC A-08 /24 Add R374 0 Ohm for Audio SPDIF Detec.

EC B-09 /28 Remove EB2 for EMI.
EC B-10 /19 Add R511~R514 for Fix SDVO issue
EC B-11 /30 Mount R372 R373 R379 for Volume Contral.
EC B-12 /31 Cgange D1 and D2 connect to +3.3V_LED for S3 S4 off.
EC B-13 /30 Add VHS 10K Pull-high for Wake up.
EC B-14 /18 Chnage to HALL sensor SW5, Del SW6 C588 C587.
EC B-15 /17 Change C509 from 0.1U to 1U for Loss of ODD on Vista.
EC B-16 /24 Change L20 L22 some L19 BK1608HM241-T.
EC B-17 /24 Change R503 connect to +AVDDA
EC B-18 /16 M/B ID change to 1101.
EC B-19 /24 Add R516 R517 C596 for IDT request.
EC B-20 /6 Add R518 R519 R520 to meet Intel Check list.
EC B-21 /18 Add R521 100K for meet Intel checklist.
EC B-22 /27 Add R522 R523 for ODD Pull-high
EC B-23 /18/29 Change USB3 and USB8 for S3 as mouse attach usb port near by RJ11 with FPR.
EC B-24 change C467,C470,C472,C192,C221,C222,C237,C238,C239,C240 from 0603 to 0402, and C9 C40 C58 to 10U.
EC B-25 /24 Add C576 for THD+ pass.
EC B-26 /2 Change C257,C264,C267 to 15P for meet Clock test Pass.
EC B-27 /19 Change R42 to 750 for meet HDMI .
EC B-28 /31 LED schematic follow MA8
EC B-29 /19 EMI request from 100P to 680P.
EC B-30 /23 change C301 C302 to 15P.
EC B-31 /24 EMI request Add C608~C611 R526~R530.
EC C-32 /24 Add U16 for Audio noise and SPDF issue.

EC E-33 Chnage USB C399,C403,C372,C376 Varistor to 0402 for Cost down.