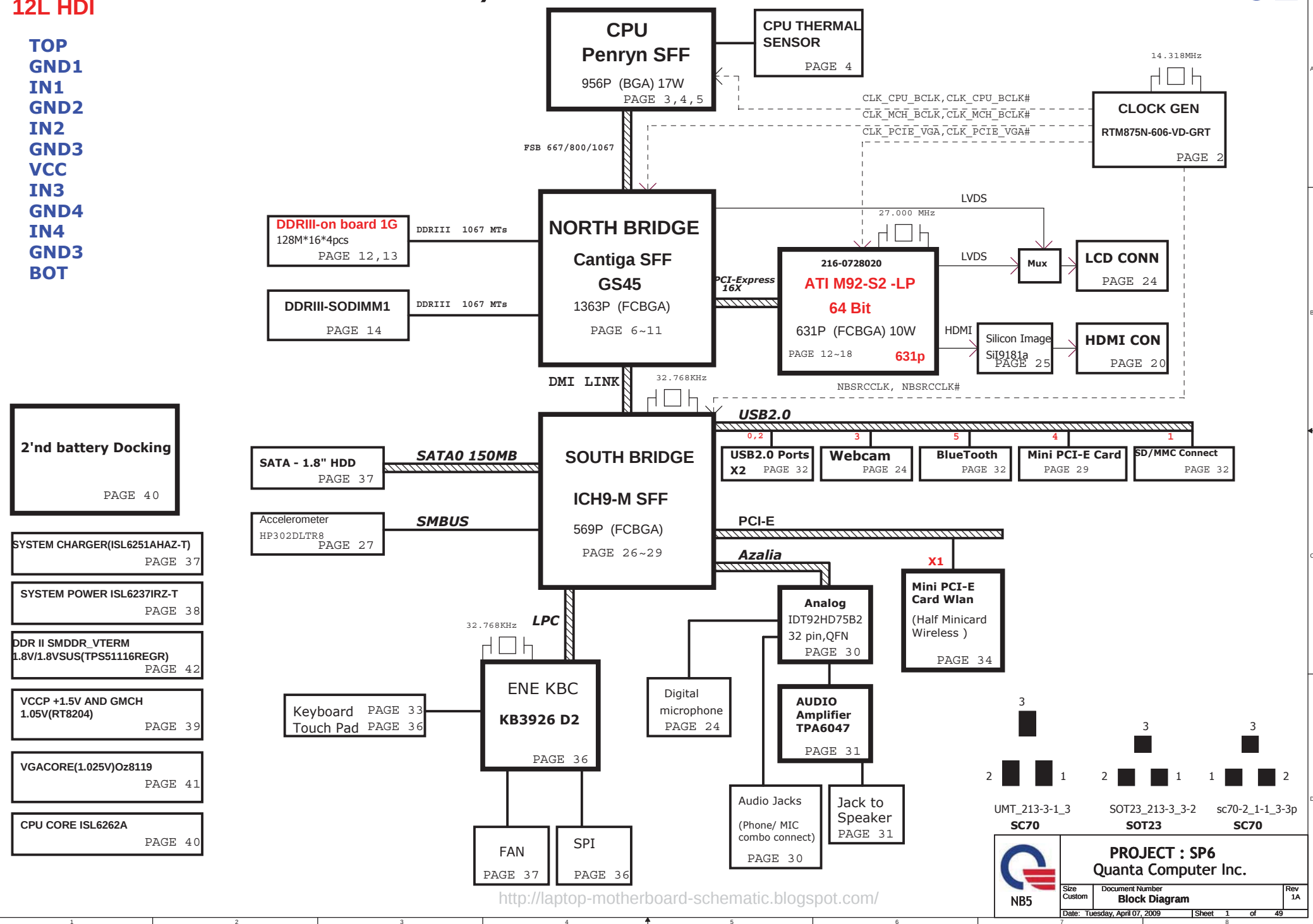
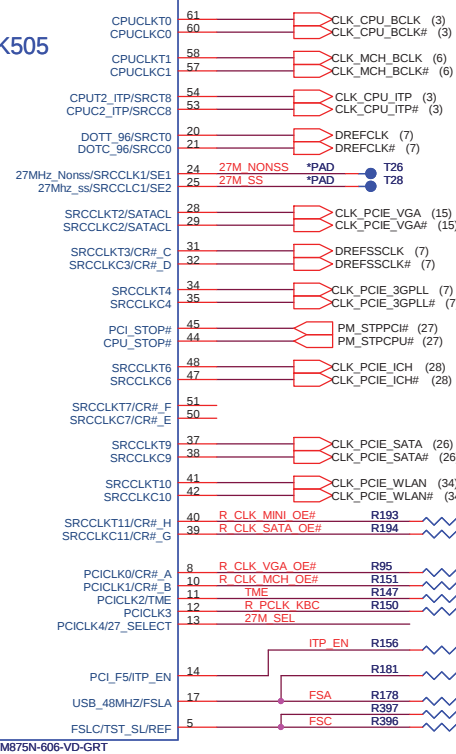
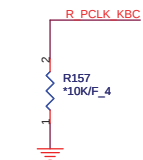
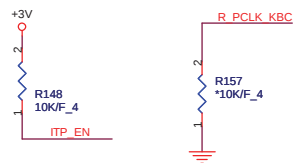
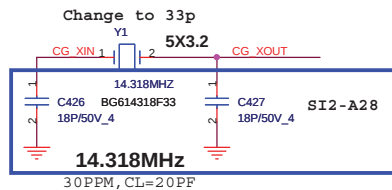
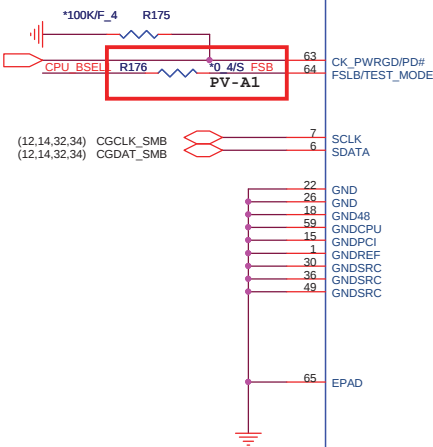
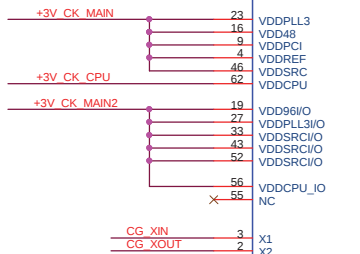


# Bond, SP6 BLOCK DIAGRAM



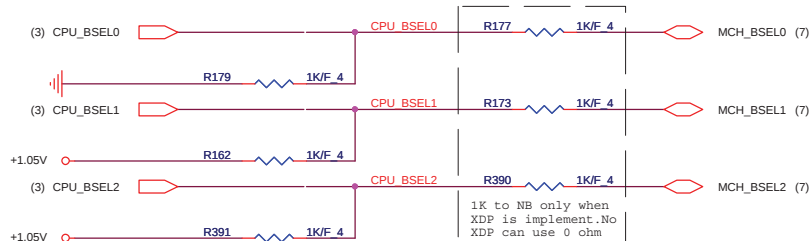


The diagram shows four clock signals (CLK) connected to a 3V power supply. The signals are labeled as follows:

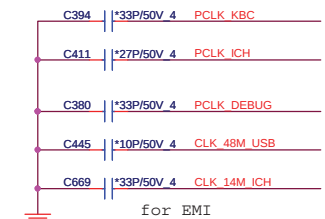
- CLK MCH OE# (R392) 2 1 10K/F 4
- CLK MINI OE# (R196) 2 1 10K/F 4
- CLK VGA OE# (R94) 2 1 10K/F 4
- CLK SATA OE# (R371) 10K/F 4

|                   |             |
|-------------------|-------------|
| RTM875N-606-VD-GR | AL000875000 |
| SLG8SP513VTR      | AL8SP513000 |

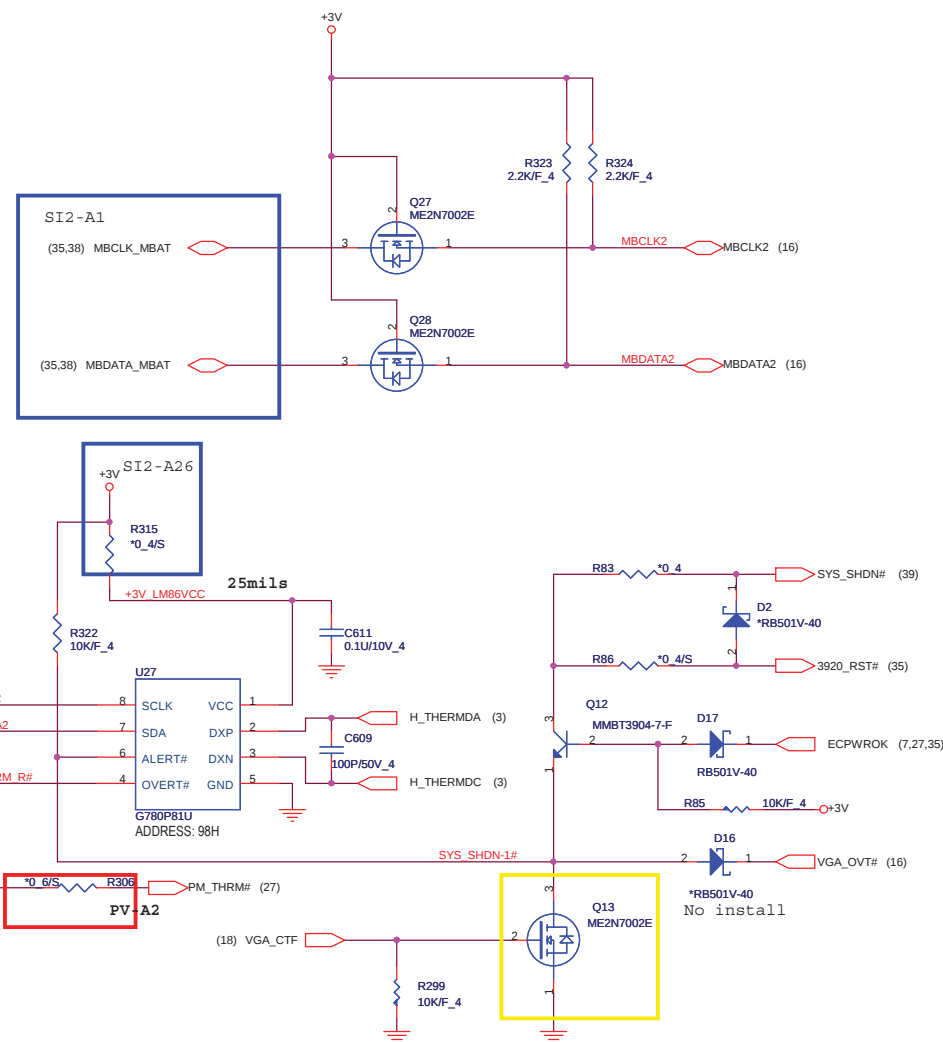
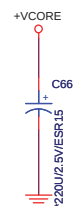
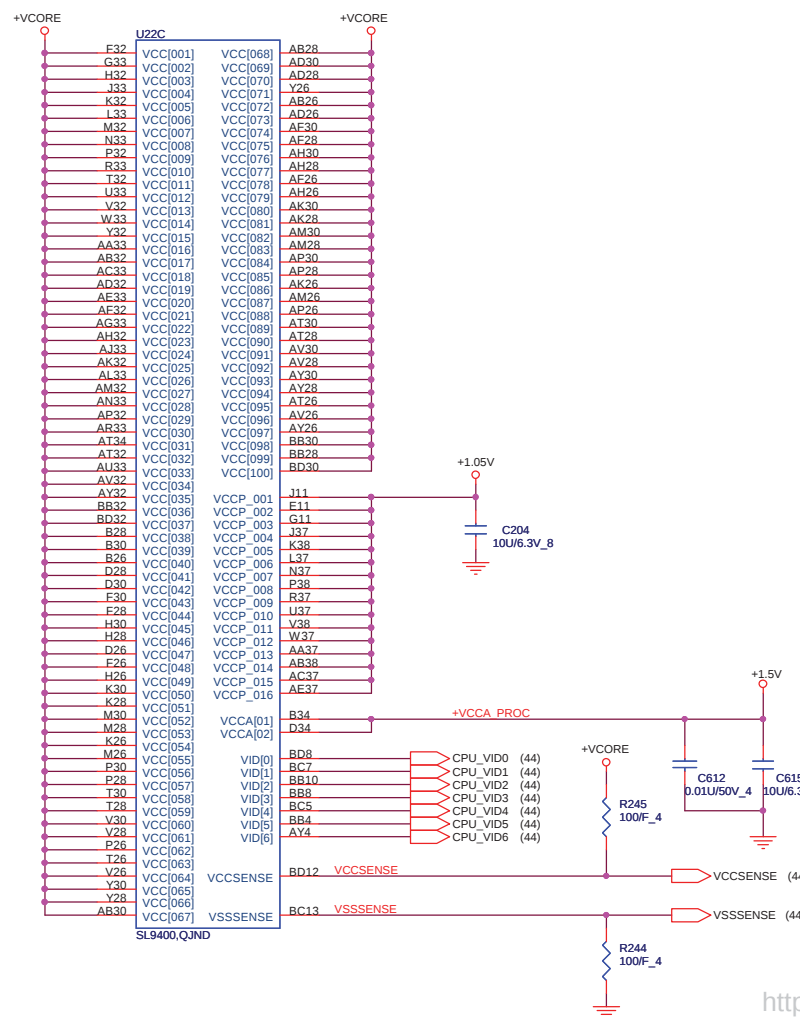
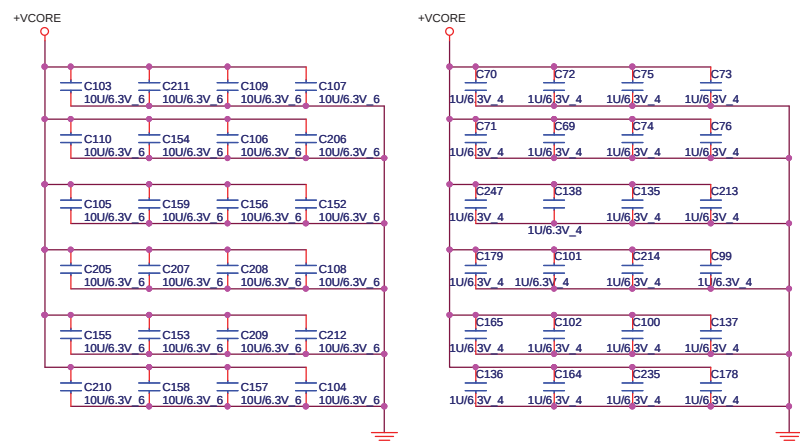
|                     |        |        |                |                |
|---------------------|--------|--------|----------------|----------------|
| 27M_SEL<br>PIN13    | PIN20  | PIN21  | PIN24          | PIN25          |
| 0=UMA               | DOT96T | DOT96C | SRCT1/LCDT_100 | SRCT1/LCDT_100 |
| 1 = External<br>VGA | SRCT0  | SRCC0  | 27Mout-NSS     | 27Mout-SS      |

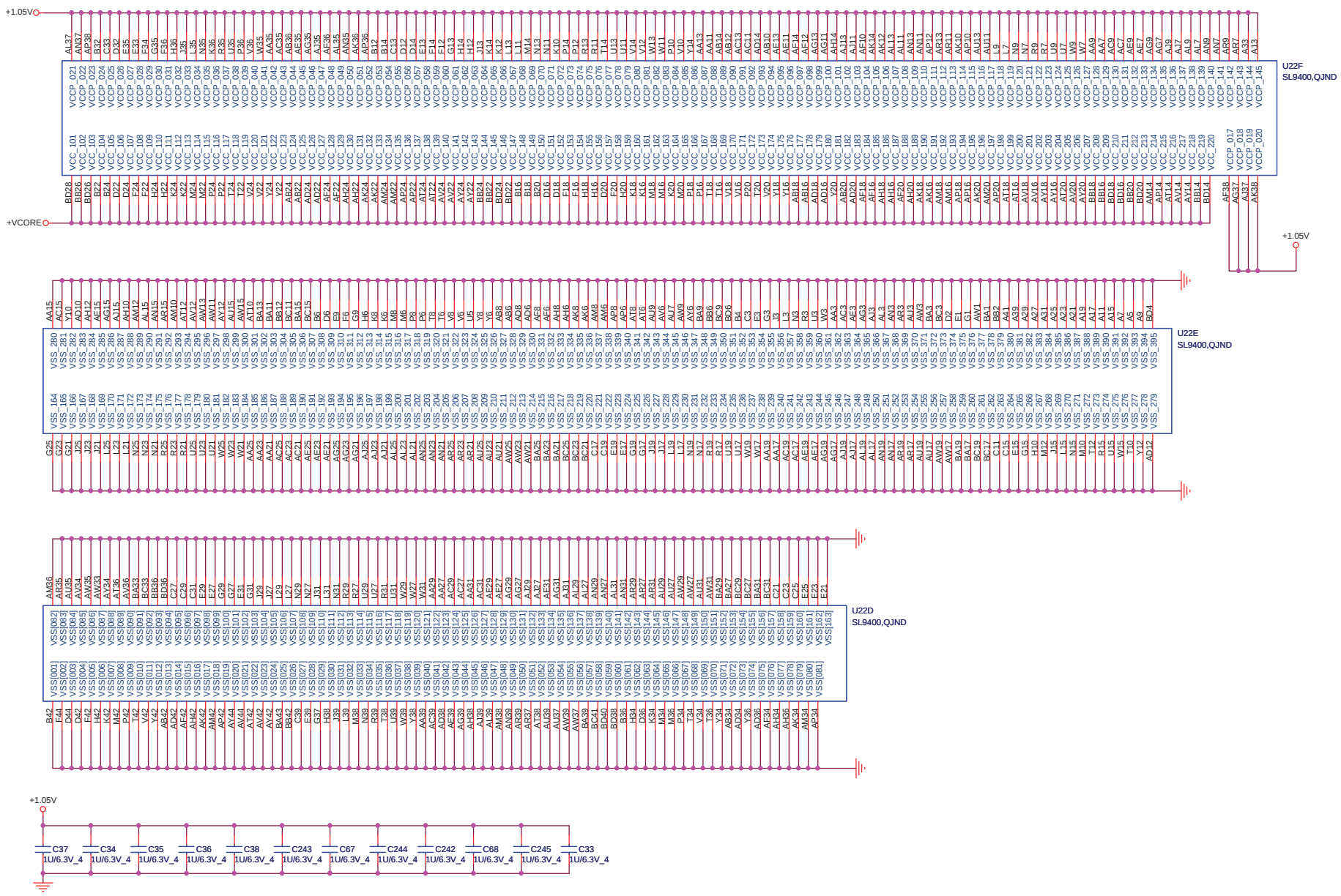


|    | FSC | FSB | FSA | CPU  | SRC | PC |
|----|-----|-----|-----|------|-----|----|
| 1) | 1   | 0   | 1   | 100  | 100 | 33 |
|    | 0   | 0   | 1   | 133  | 100 | 33 |
|    | 0   | 1   | 1   | 166  | 100 | 33 |
| 7) | 0   | 1   | 0   | 200  | 100 | 33 |
|    | 0   | 0   | 0   | 266  | 100 | 33 |
|    | 1   | 0   | 0   | 333  | 100 | 33 |
| 7) | 1   | 1   | 0   | 400  | 100 | 33 |
|    | 1   | 1   | 1   | RSVD | 100 | 33 |







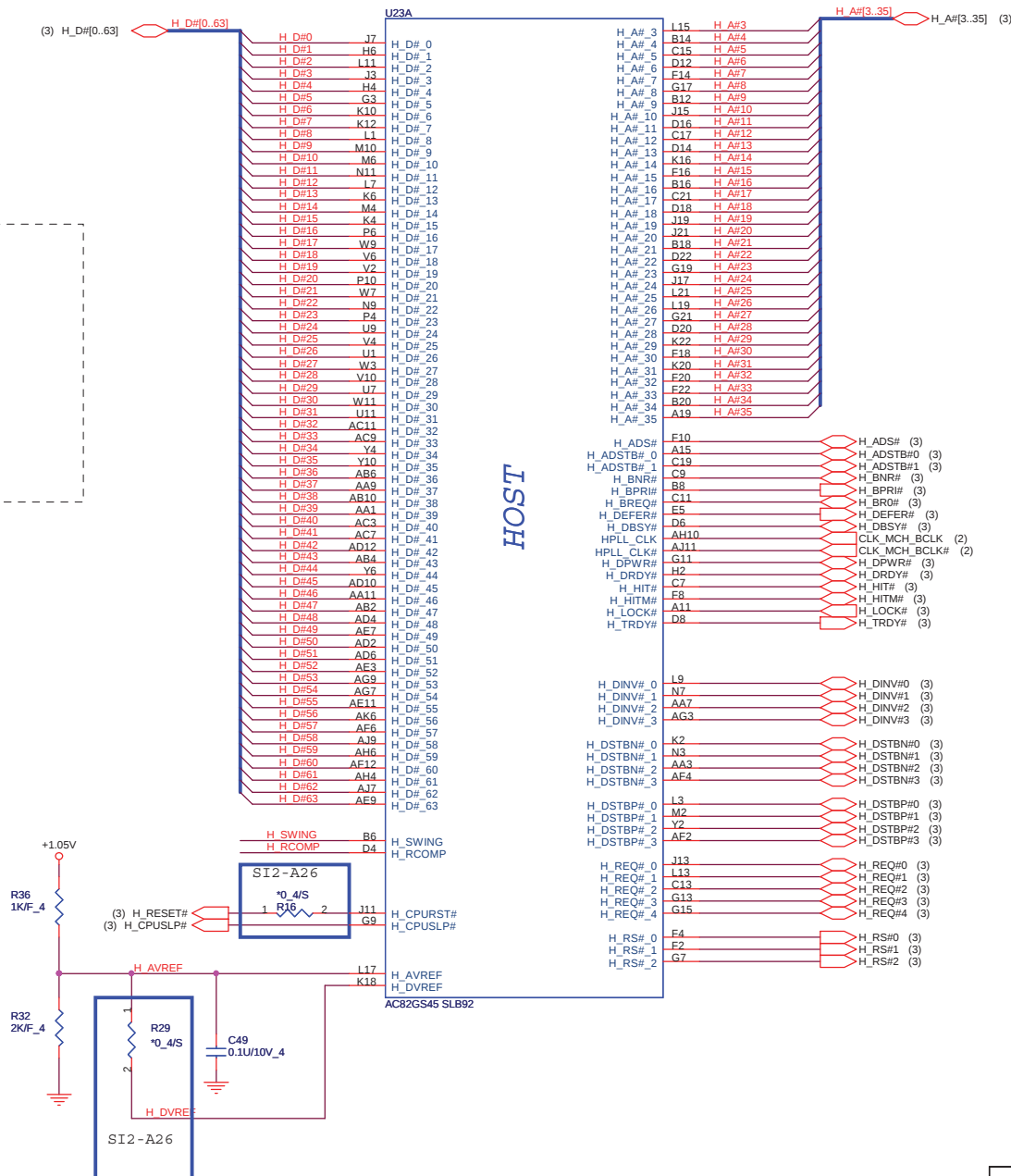
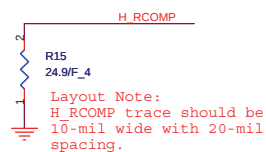
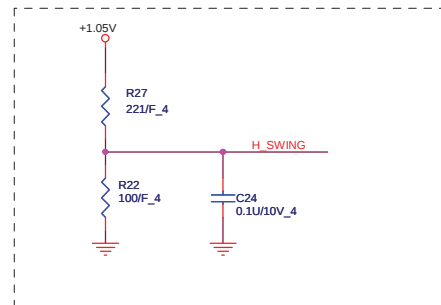


05

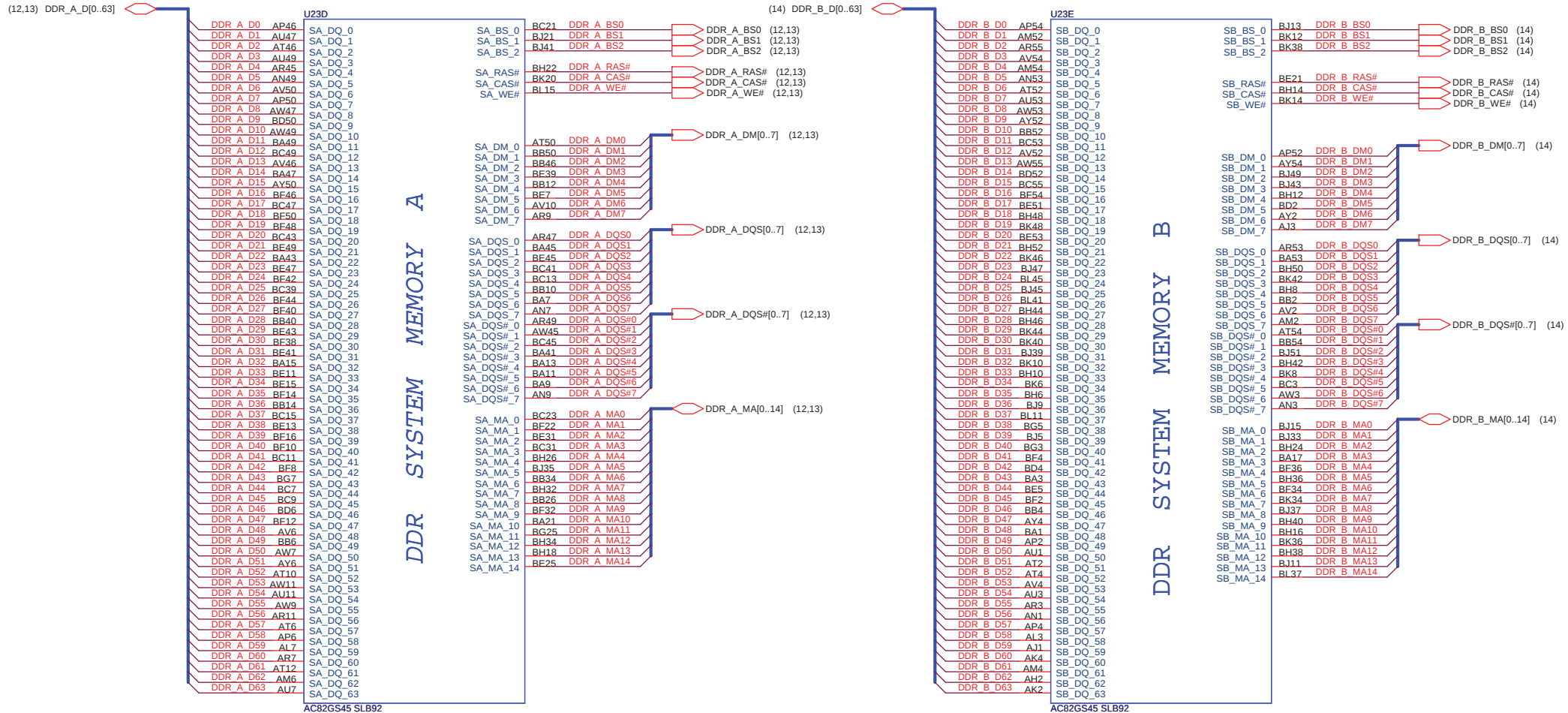


PROJECT : SP6  
Quanta Computer Inc.

|                               |                               |           |
|-------------------------------|-------------------------------|-----------|
| Size<br>Custom                | Document Number<br>Penryn 3/3 | Rev<br>1A |
| Date: Tuesday, April 07, 2009 | Sheet 5 of 49                 |           |



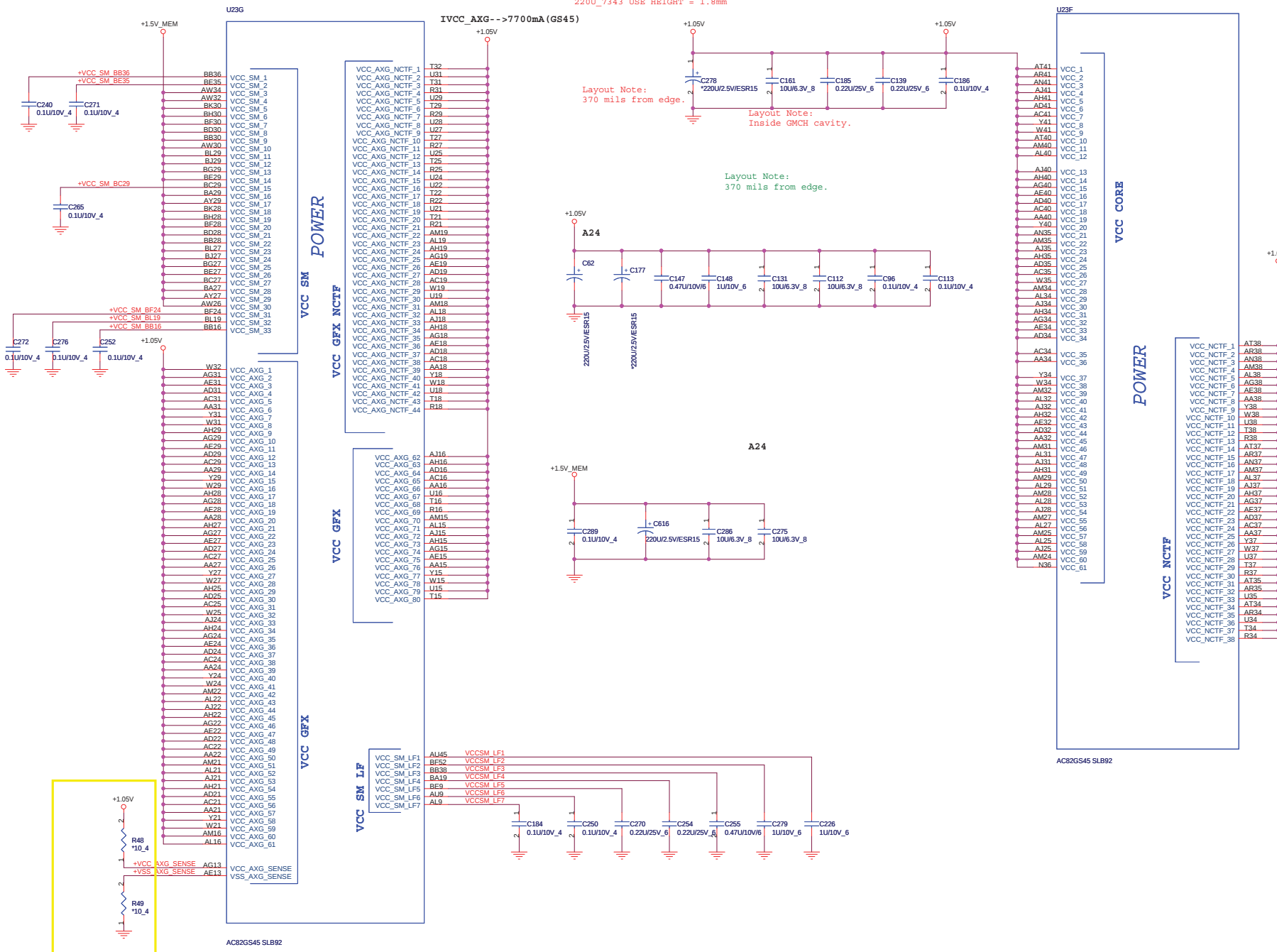




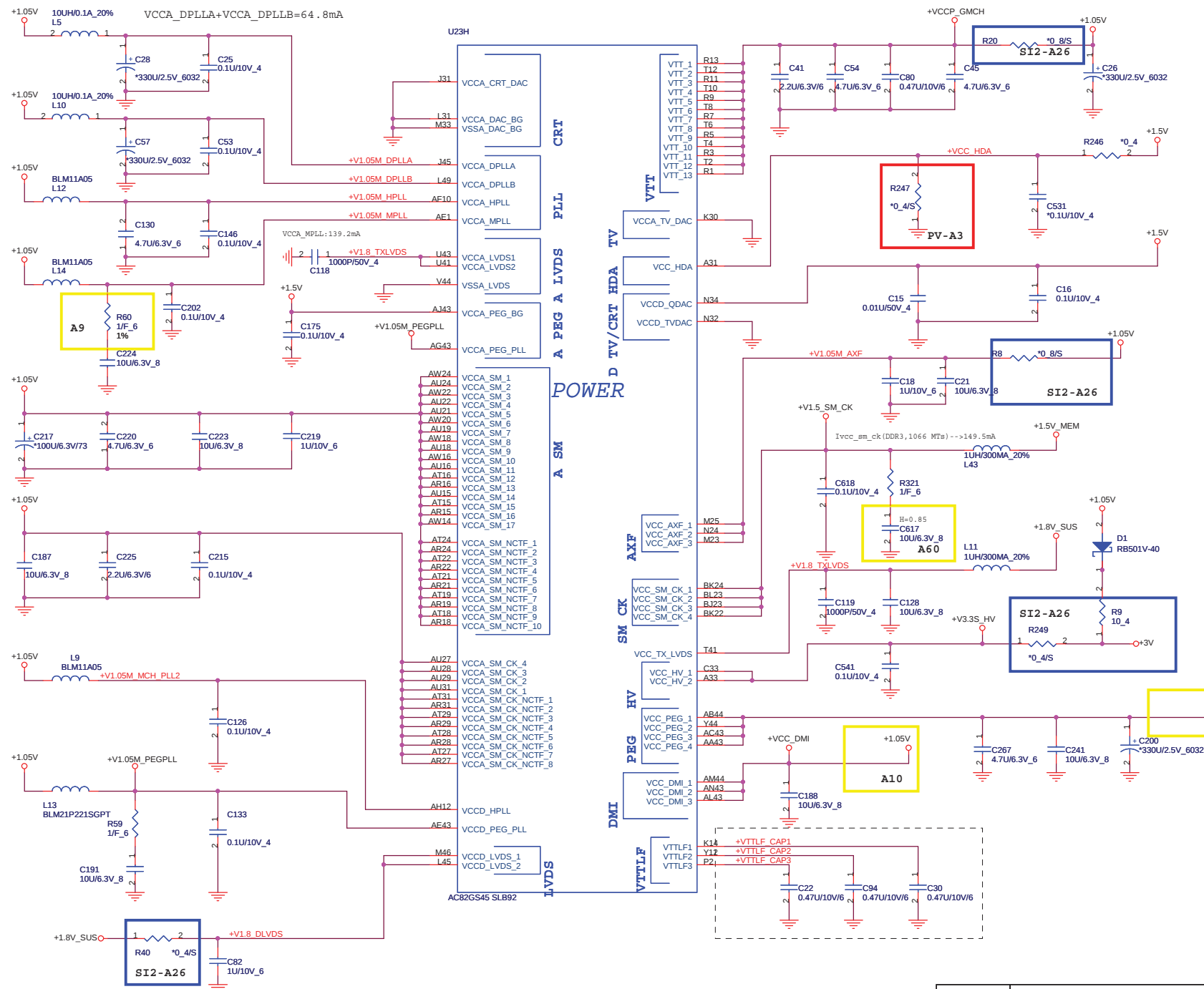
|                                                                                              |                                                     |                                            |           |  |
|----------------------------------------------------------------------------------------------|-----------------------------------------------------|--------------------------------------------|-----------|--|
| <br>NB5 | <b>PROJECT : SP6</b><br><b>Quanta Computer Inc.</b> |                                            | Rev<br>1A |  |
|                                                                                              | Size<br>Custom                                      | Document Number<br>Cantiga (DDR interface) |           |  |
|                                                                                              | Date: Tuesday, April 07, 2009                       | Sheet 8 of 49                              |           |  |

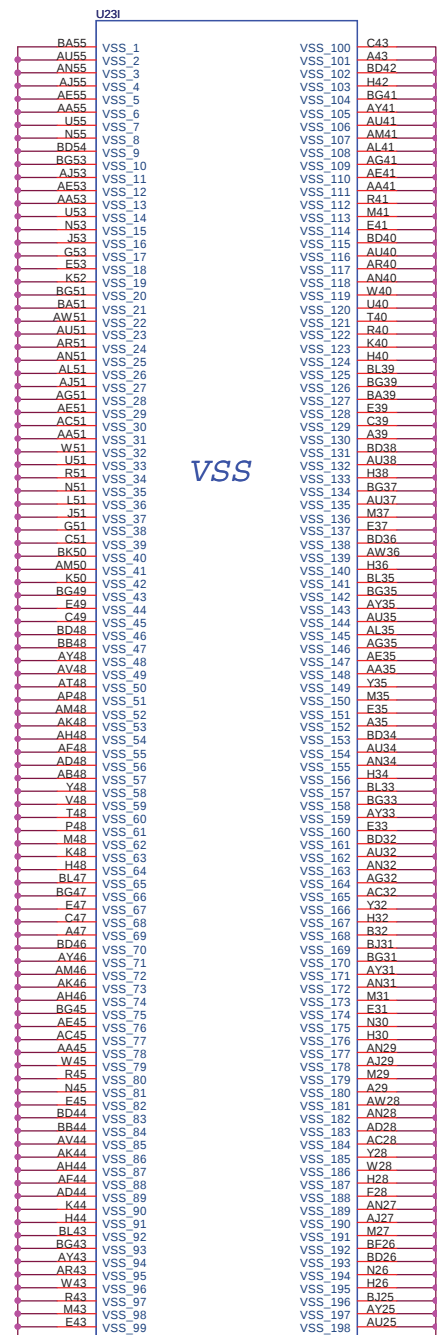
Ivcc sm (DDR3,1.5V,1066MTs) -->4140mA

220U\_7343 USE HEIGHT = 1.8mm

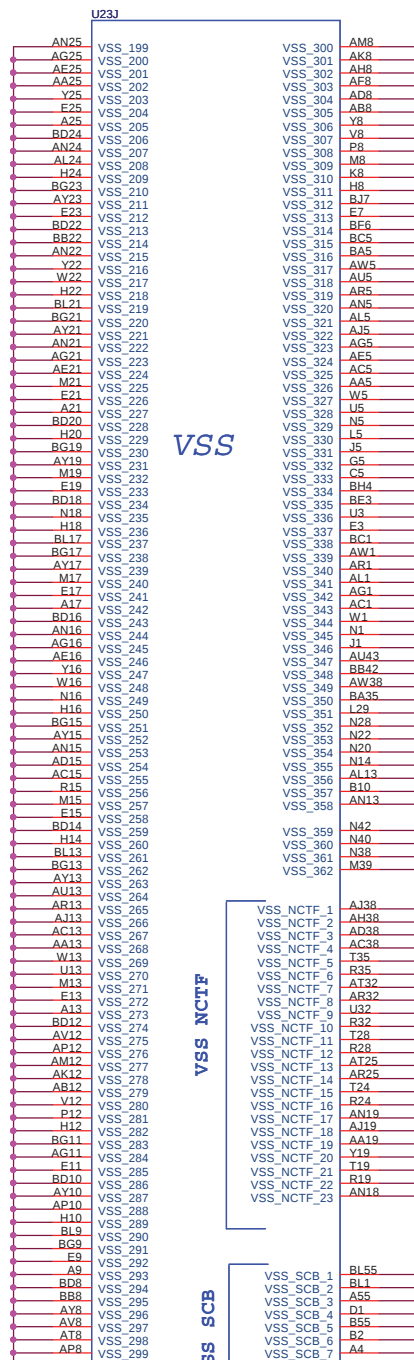


render standby feature is not implemented can be left





AC82GS45 SLB92

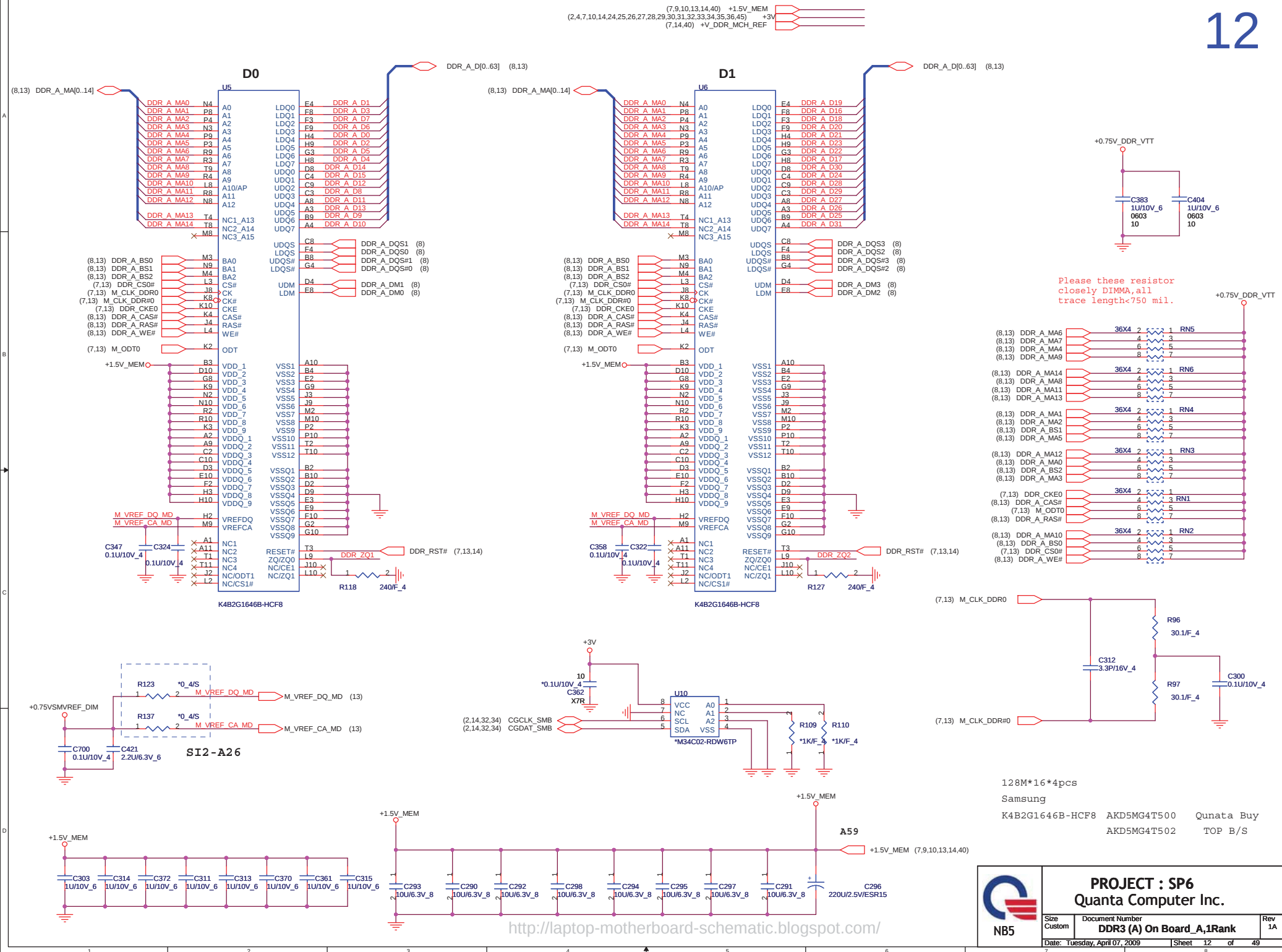


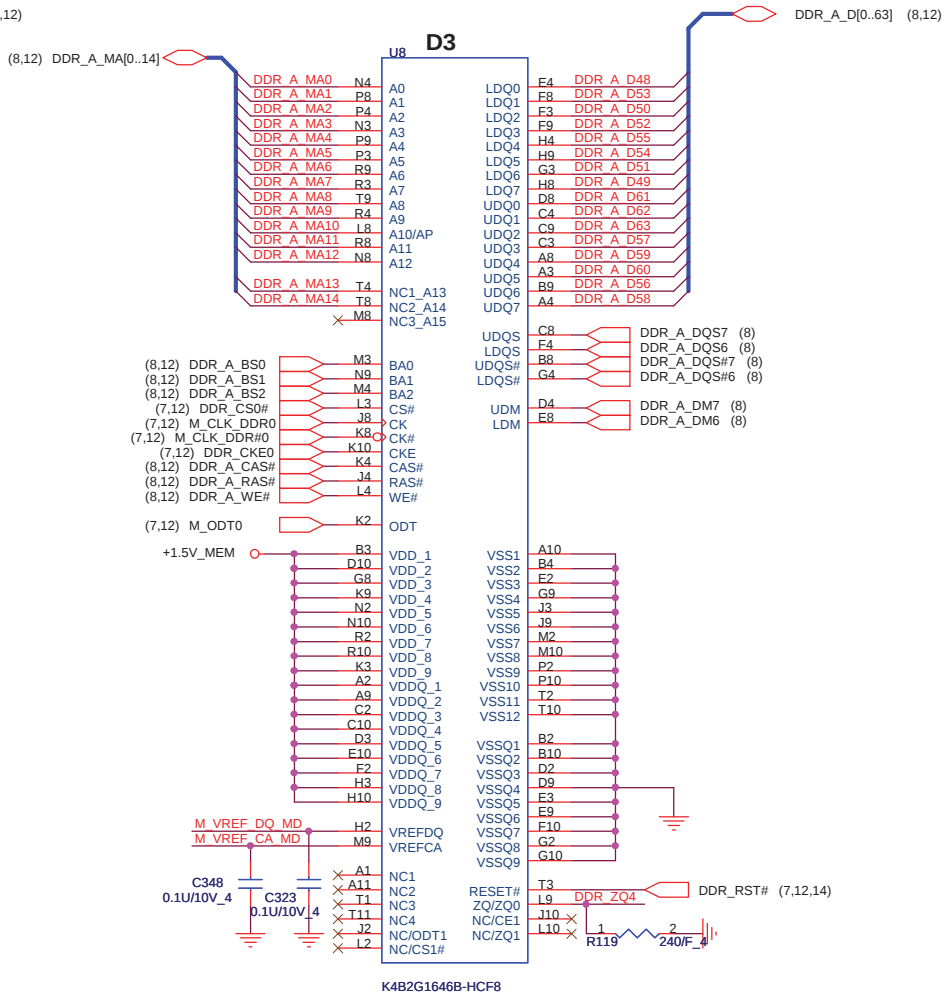
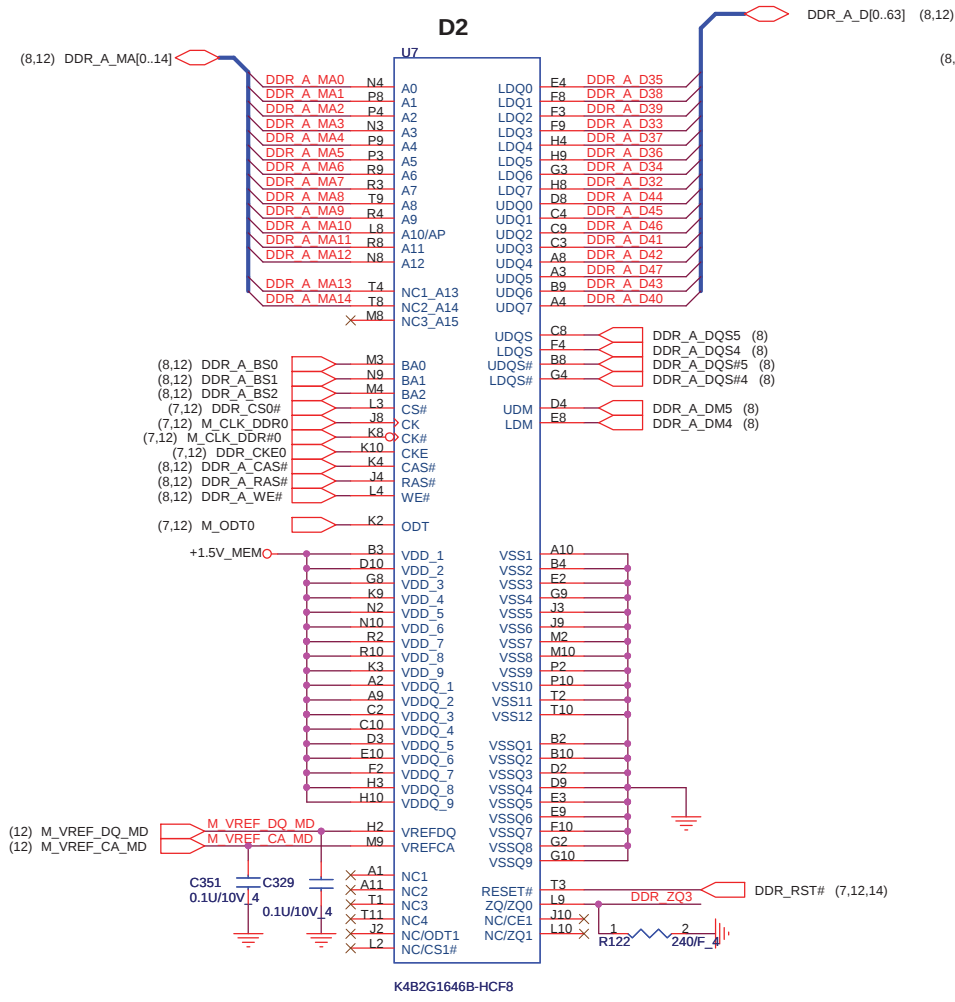
AC82GS45 SLB92



PROJECT : SP6  
Quanta Computer Inc.

|                               |                                  |        |
|-------------------------------|----------------------------------|--------|
| Size Custom                   | Document Number<br>Cantiga (Vss) | Rev 1A |
| Date: Tuesday, April 07, 2009 | Sheet 11 of 49                   |        |

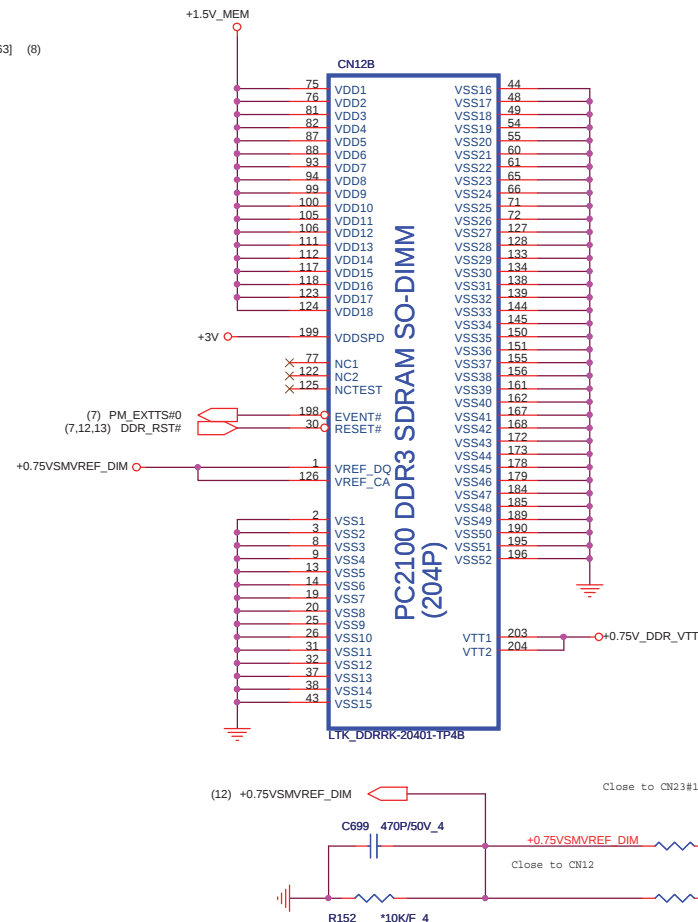
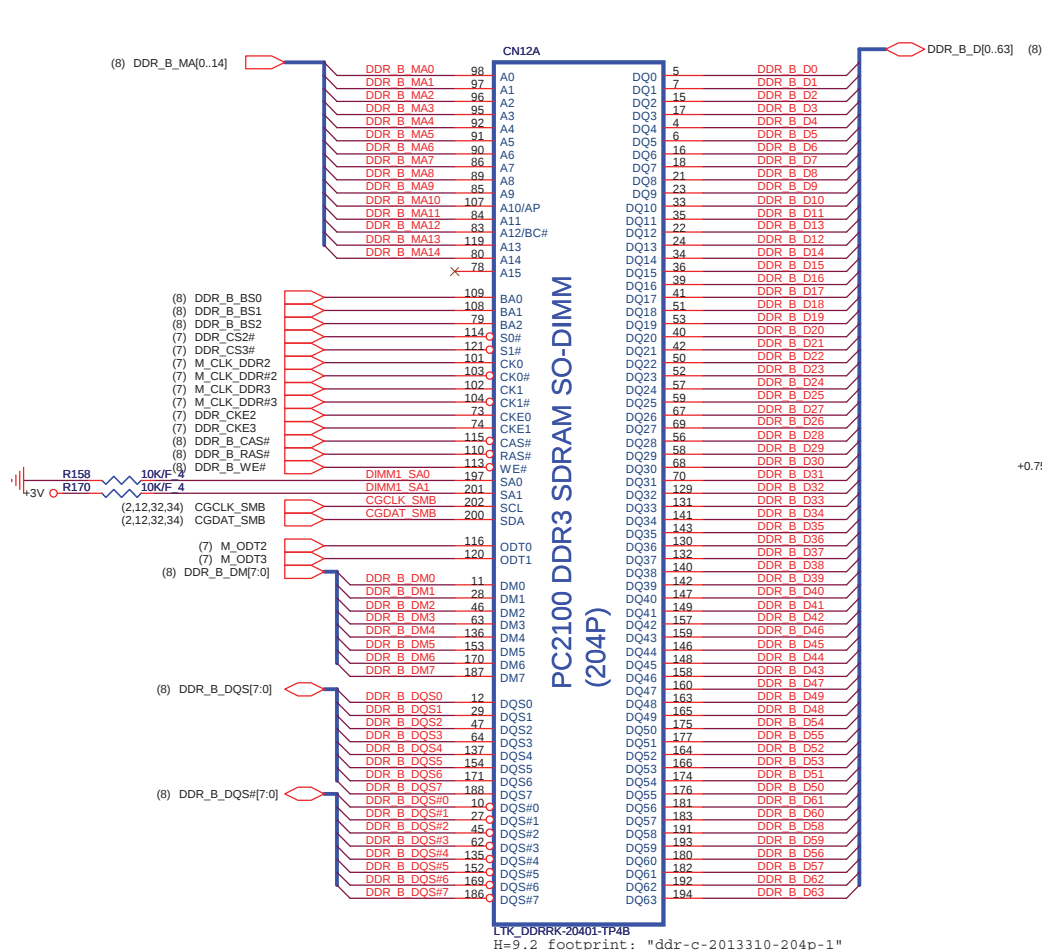




|                                                                                       |                 |          |                                                     |        |
|---------------------------------------------------------------------------------------|-----------------|----------|-----------------------------------------------------|--------|
|  |                 |          | <b>PROJECT : SP6</b><br><b>Quanta Computer Inc.</b> |        |
| Size B                                                                                | Document Number |          |                                                     | Rev 1A |
| <b>DDR3 (A) On Board_B,1Rank</b>                                                      |                 |          |                                                     |        |
| Date: Tuesday, April 07, 2009                                                         |                 | Sheet 13 | of 49                                               |        |

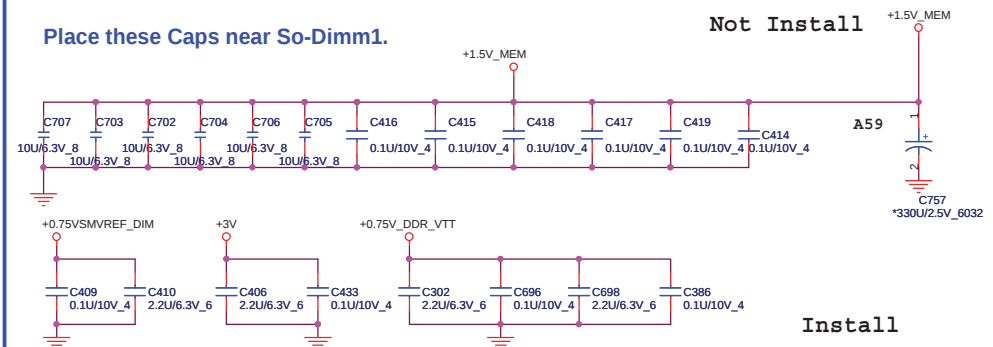
0922--&gt;CN23 update library to DDR-AS0A62X-U4RN-7F-204P type

(7,9,10,12,13,40) +1.5V\_MEM  
(2,4,7,10,12,24,25,26,27,28,29,30,31,32,33,34,35,36,45) +3V  
(12,40) +0.75V\_DDR\_VTT  
(12,40) +0.75V\_DDR\_VTT



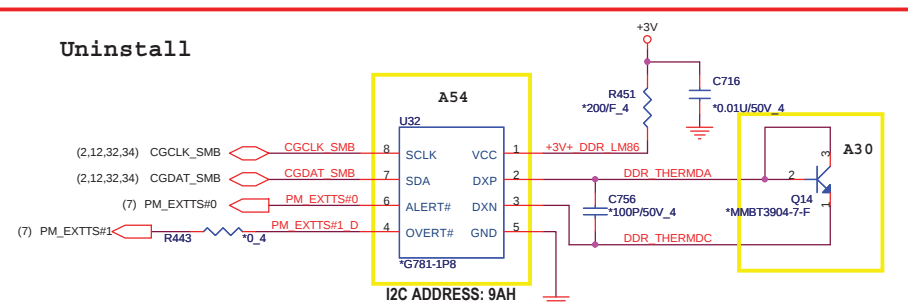
Place these Caps near So-Dimm1.

Not Install



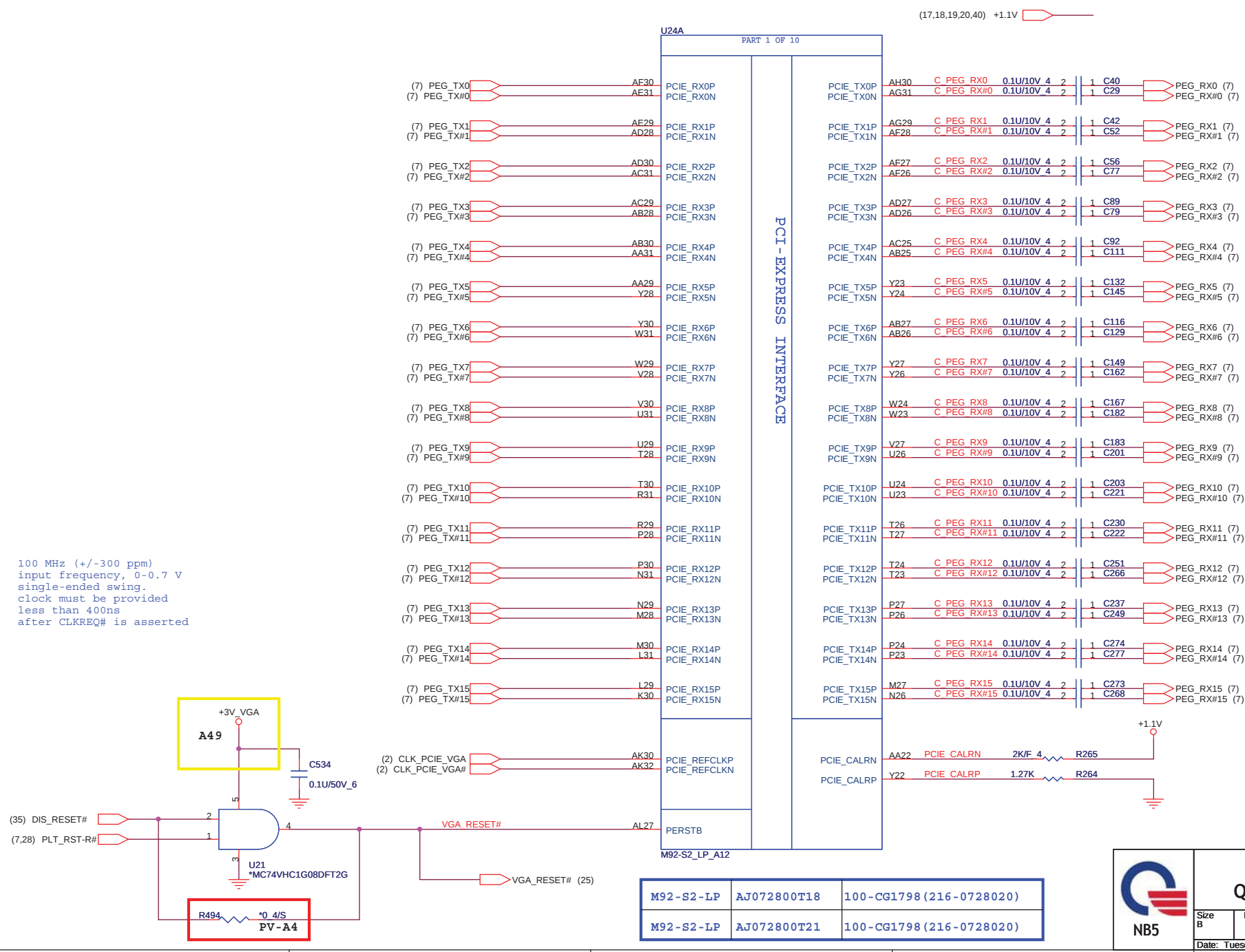
Install

Uninstall



PROJECT : SP6  
Quanta Computer Inc.

Size Custom Document Number  
DDR3 Connect  
Date: Tuesday, April 07, 2009 Sheet 14 of 49



100 MHz (+/-300 ppm)  
input frequency, 0-0.7 V  
single-ended swing.  
clock must be provided  
less than 400ns  
after CLKREQ# is asserted

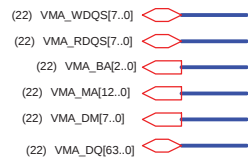
|           |             |                          |
|-----------|-------------|--------------------------|
| M92-S2-LP | AJ072800T18 | 100-CG1798 (216-0728020) |
| M92-S2-LP | AJ072800T21 | 100-CG1798 (216-0728020) |

**PROJECT : SP6**  
**Quanta Computer Inc.**

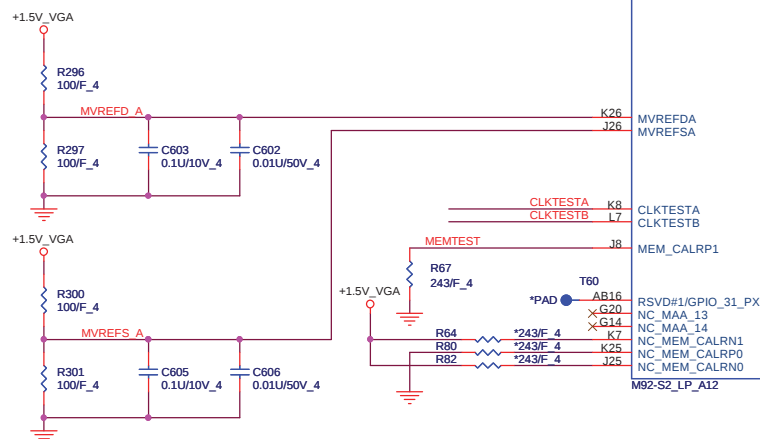
|        |                                              |        |
|--------|----------------------------------------------|--------|
| Size B | Document Number<br><b>M92 PCIe interface</b> | Rev 1A |
|--------|----------------------------------------------|--------|

Date: Tuesday, April 07, 2009 Sheet 15 of 49

# MEMORY INTERFACE



| DIVIDER RESISTORS | DDR3 |
|-------------------|------|
| MVREF TO 1.5V     | 100R |
| MVREF TO GND      | 100R |

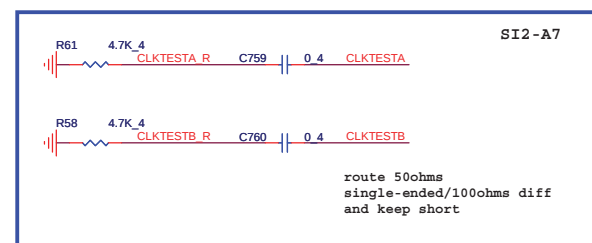
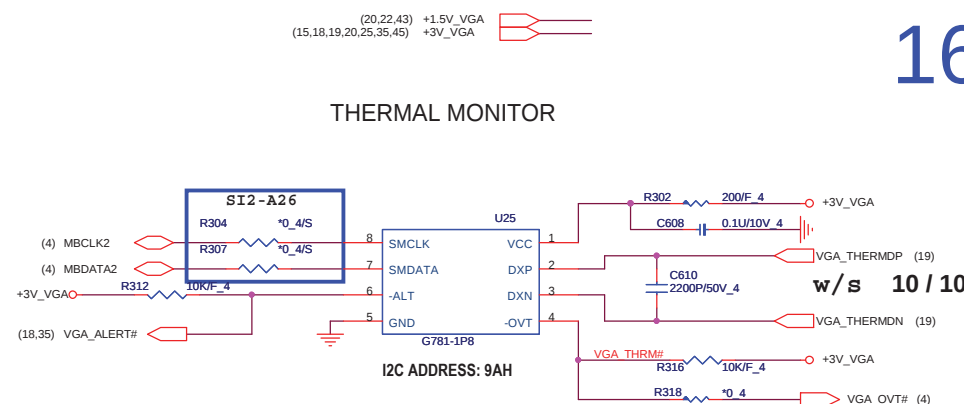


U24C PART 3 OF 10

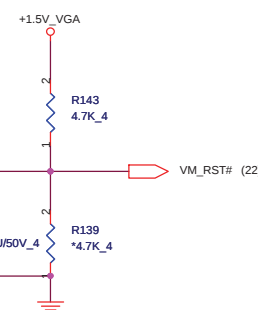
## MEMORY INTERFACE



## THERMAL MONITOR



For DDR3

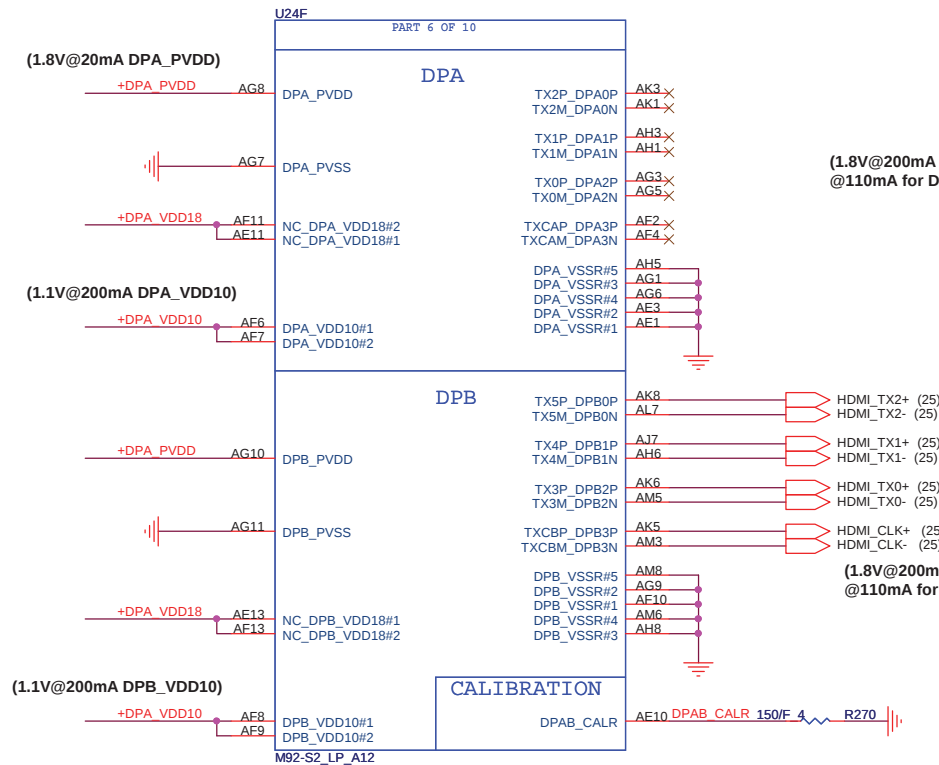


16

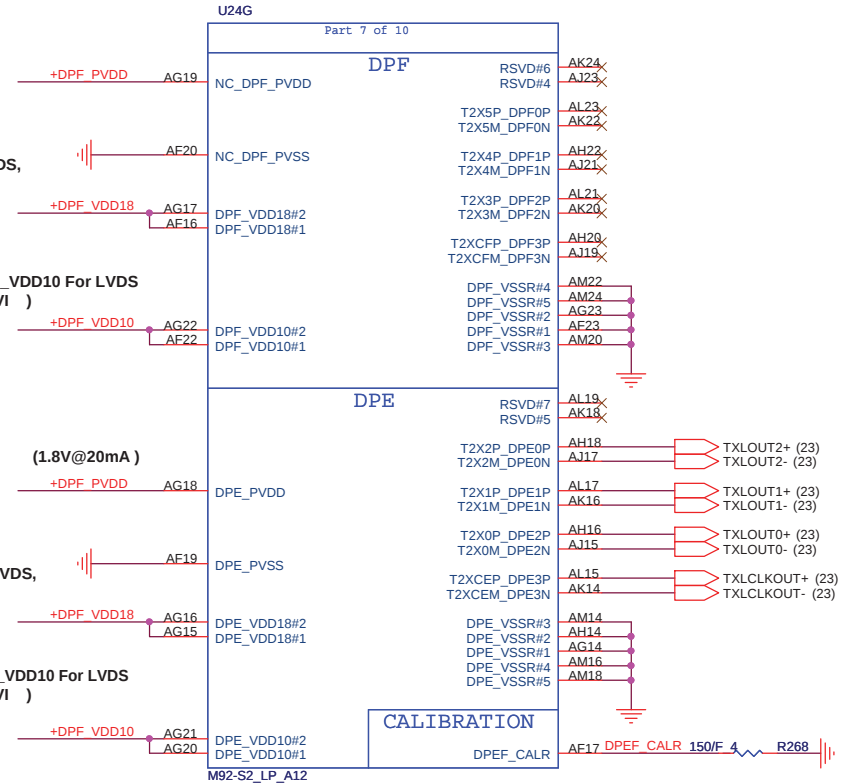
## TMDP(HDMI) INTERFACE

(15,18,19,20,40) +1.1V

## LVDS INTERFACE



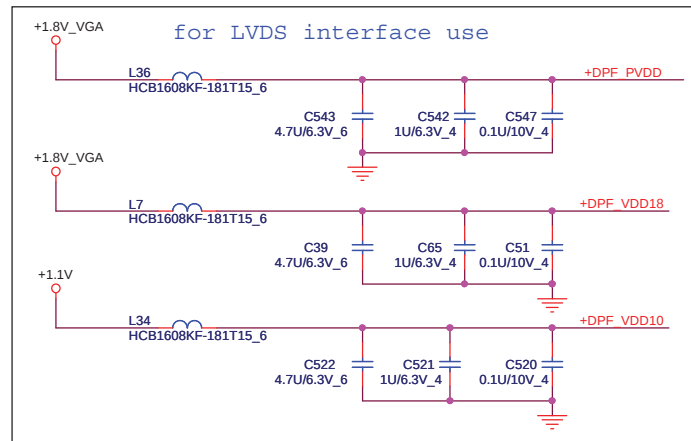
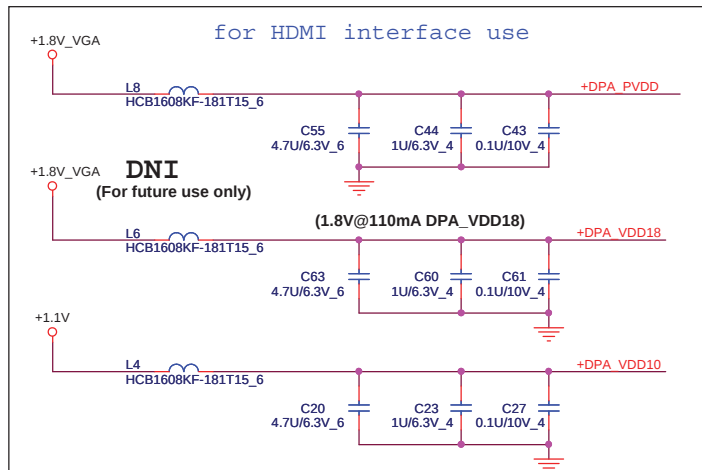
(1.1V@100mA DPF\_VDD10 For LVDS  
@170mA for DP/DVI )



(1.8V@20mA )

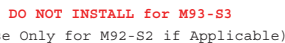
(1.8V@200mA DPE\_VDD18 for LVDS,  
@110mA for DP/DVI)

(1.1V@100mA DPE\_VDD10 For LVDS  
@170mA for DP/DVI )

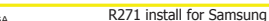


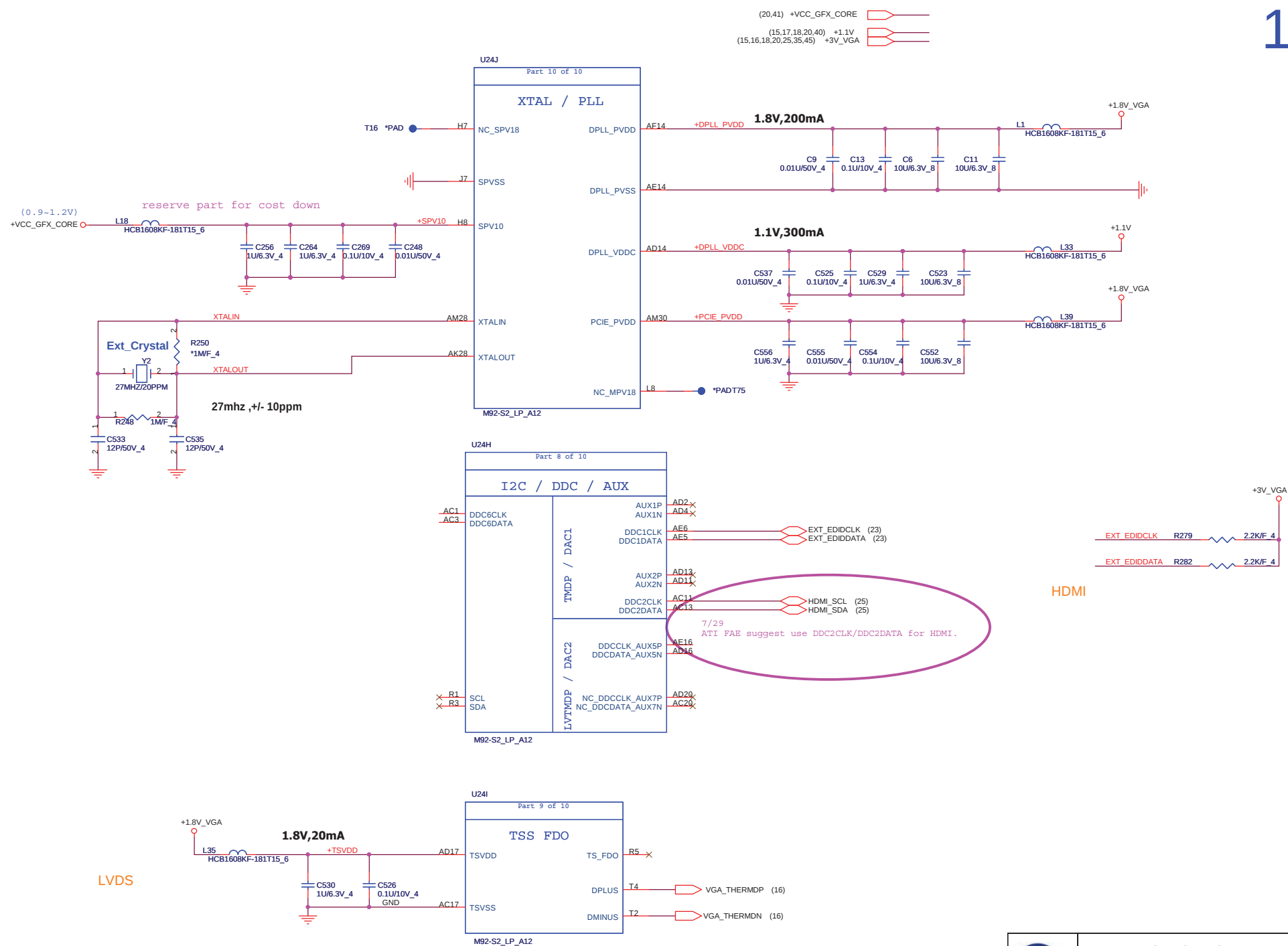
**PROJECT : SP6**  
Quanta Computer Inc.

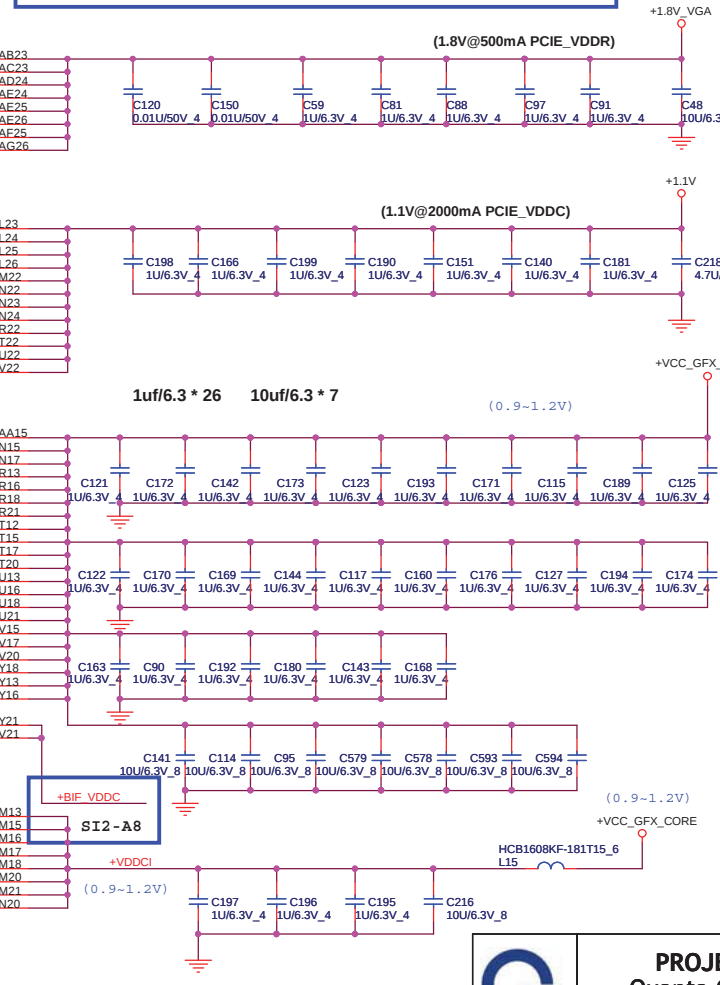
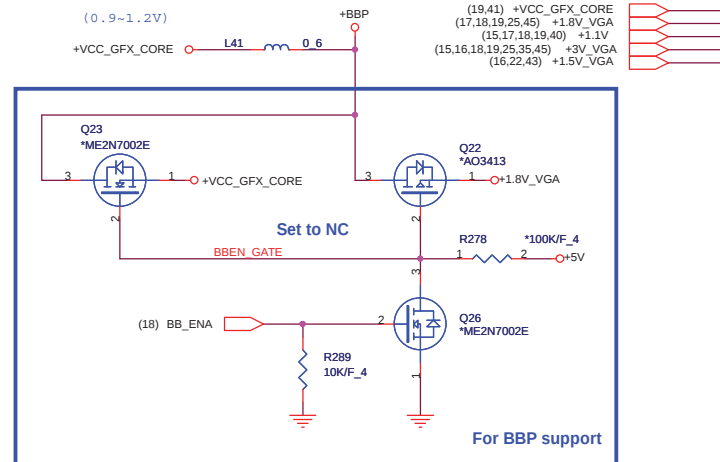
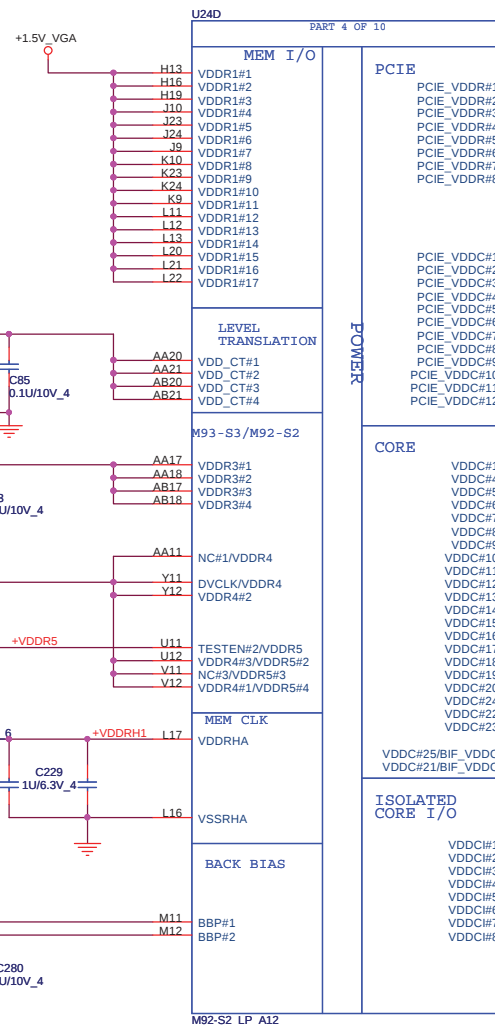
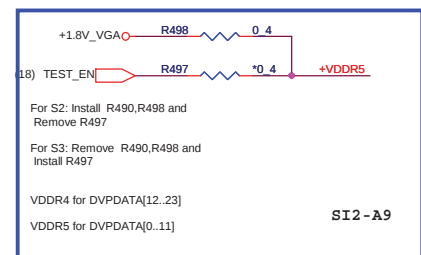
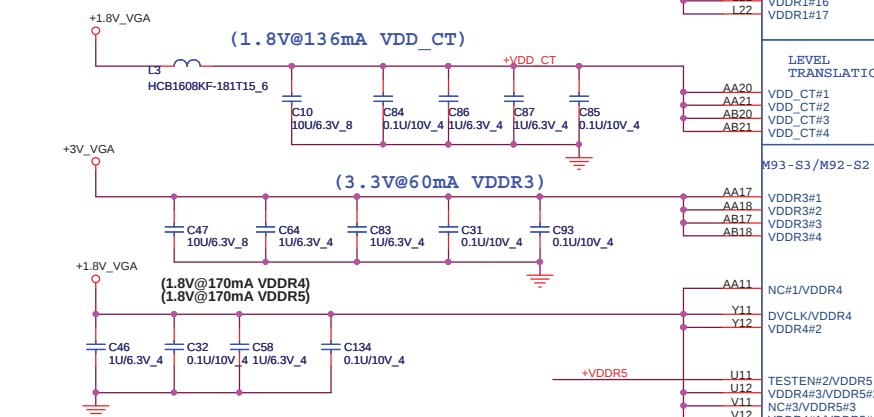
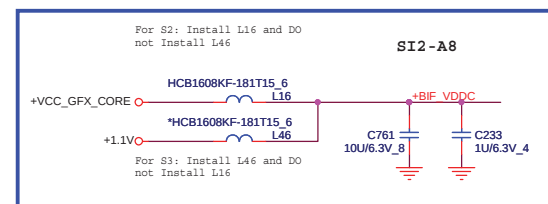
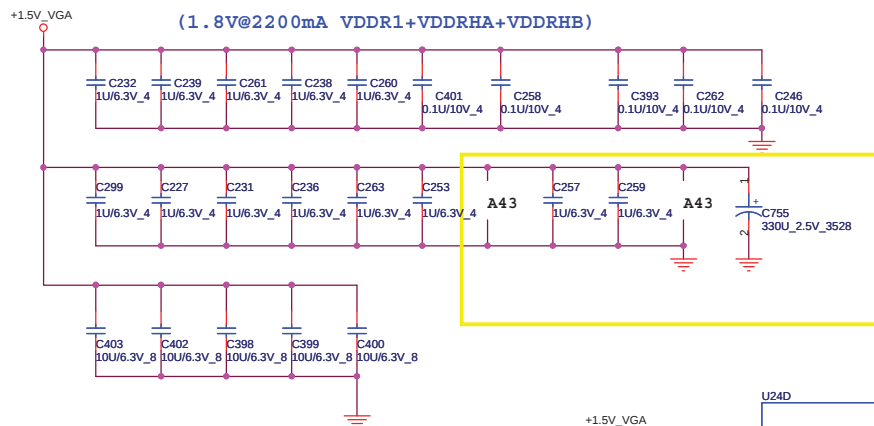
|                               |                                                   |                |
|-------------------------------|---------------------------------------------------|----------------|
| Size<br>B                     | Document Number<br><b>M92 HDMI/LVDS interface</b> | Rev<br>1A      |
| Date: Tuesday, April 07, 2009 |                                                   | Sheet 17 of 49 |

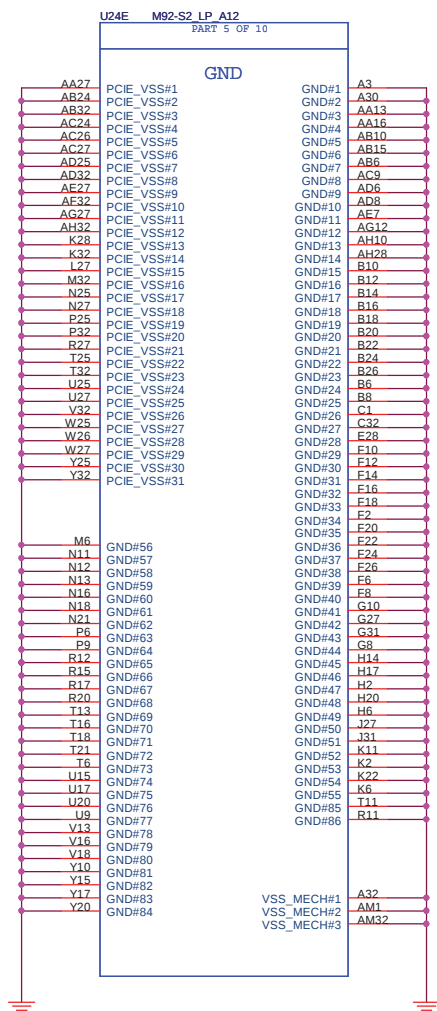
DefaultDefaultDefault

spectrum chip  
in order to  
reasons.









## Power up

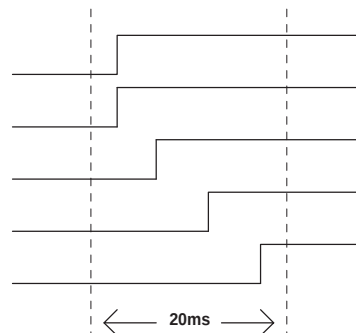
BBP/N=VDDC=VSS=3.3V

+1.1V VDDC=0.9~1.2V

DDR3(+1.5V)

VDD\_CT=1.8V

VDDR3=3.3V



## Power down

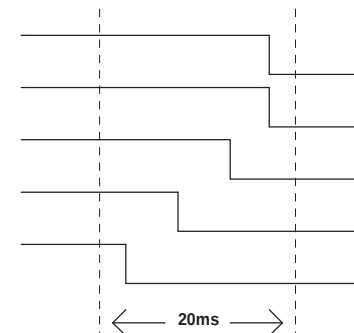
BBP/N=VDDC=VSS=3.3V

+1.1V VDDC=0.9~1.2V

DDR3(+1.5V)

VDD\_CT=1.8V

VDDR3=3.3V



## CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

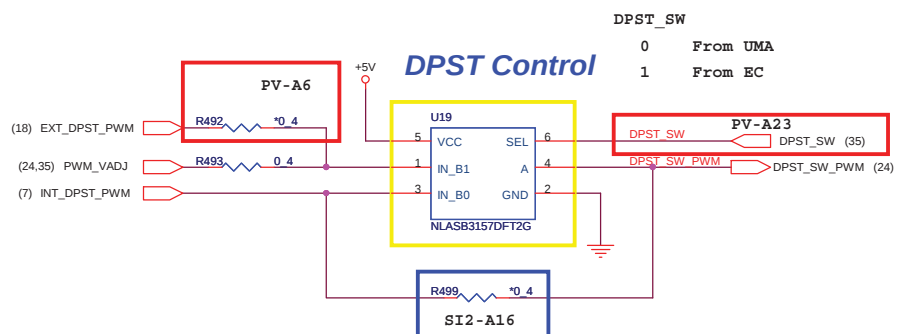
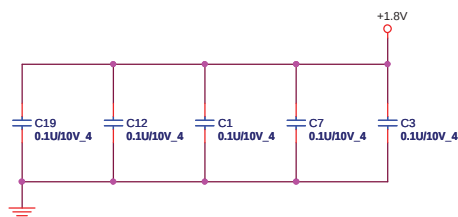
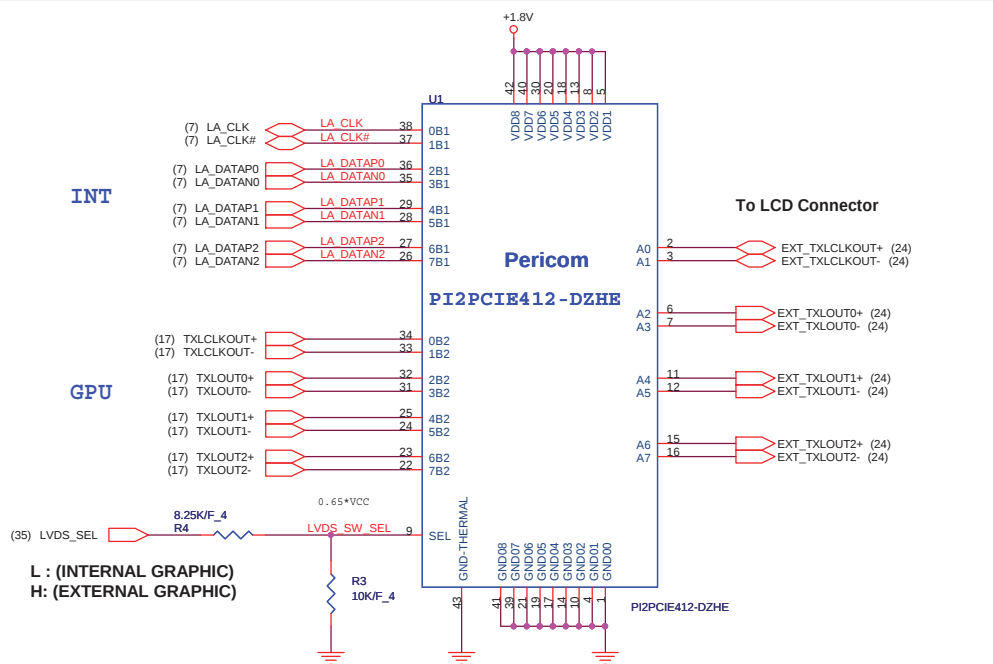
RECOMMENDED SETTINGS  
0= DO NOT INSTALL RESISTOR  
1= INSTALL 10K RESISTOR  
X= DESIGN DEPENDANT  
NA= NOT APPLICABLE

| STRAPS               | PIN            | DESCRIPTION OF DEFAULT SETTINGS                                                                                                                                                 |       |
|----------------------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| TX_PWRS_ENB          | GPIO0          | PCIE FULL TX OUTPUT SWING                                                                                                                                                       | X     |
| TX_DEEMPH_EN         | GPIO1          | PCIE TRANSMITTER DE-EMPHASIS ENABLED                                                                                                                                            | X     |
| BIF_GEN2_EN_A        | GPIO2          | PCIE GEN2 ENABLED                                                                                                                                                               | X     |
| RSVD                 | GPIO8          |                                                                                                                                                                                 | 0     |
| BIF_VGA_DIS          | GPIO9          | VGA ENABLED                                                                                                                                                                     | 0     |
| RSVD                 | GPIO21         |                                                                                                                                                                                 | 0     |
| BIOS_ROM_EN          | GPIO_22_ROMCSB | ENABLE EXTERNAL BIOS ROM                                                                                                                                                        | X     |
| ROMIDCFG(2:0)        | GPIO[13:11]    | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT                                                                                                                                  | X X X |
| VIP_DEVICE_STRAP_ENA | V2SYNC         | IGNORE VIP DEVICE STRAPS                                                                                                                                                        | X     |
| RSVD                 | GENERICC       |                                                                                                                                                                                 | 0     |
| AUD[1]               | HSYNC          |                                                                                                                                                                                 | 0     |
| AUD[0]               | VSYN           | AUD[1] AUD[0]<br>0 0 No audio function<br>0 1 Audio for DisplayPort and HDMI if dongle is detected<br>1 0 Audio for DisplayPort only<br>1 1 Audio for both DisplayPort and HDMI | X X   |

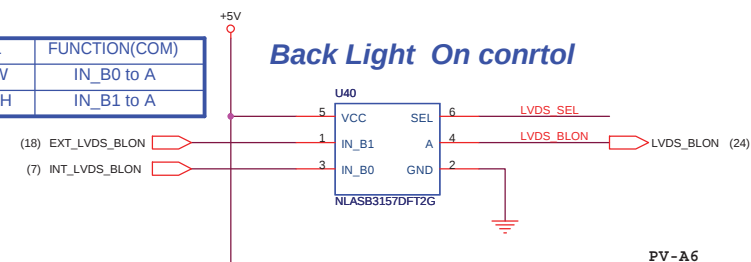


INT

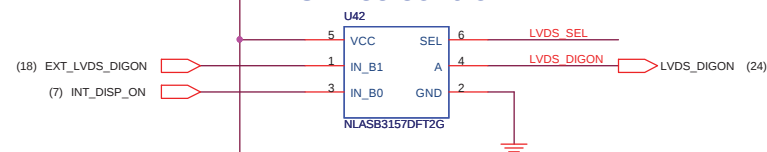
GPU



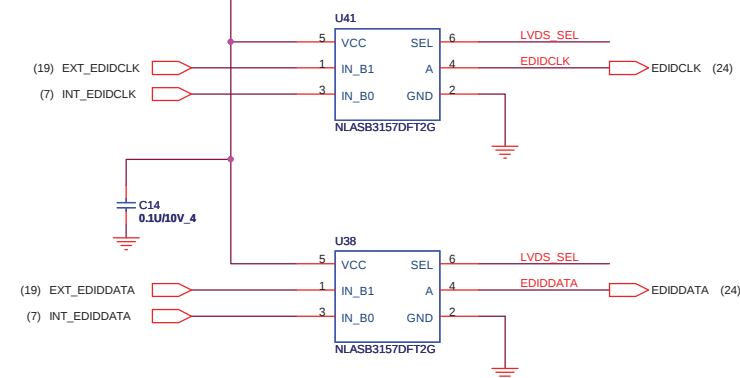
### Back Light On control



### LCDVcc control

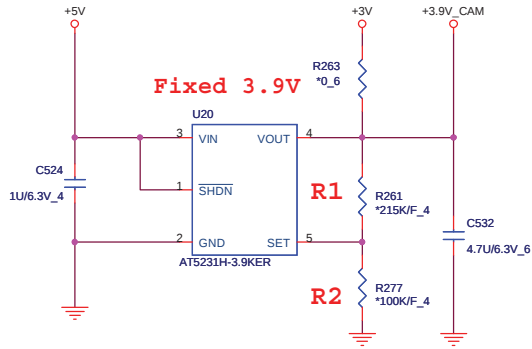


### LCD EDID(CLK/DATA) control

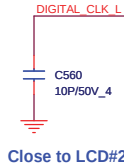


# USB CAMERA /DIGITAL MIC CONNECT

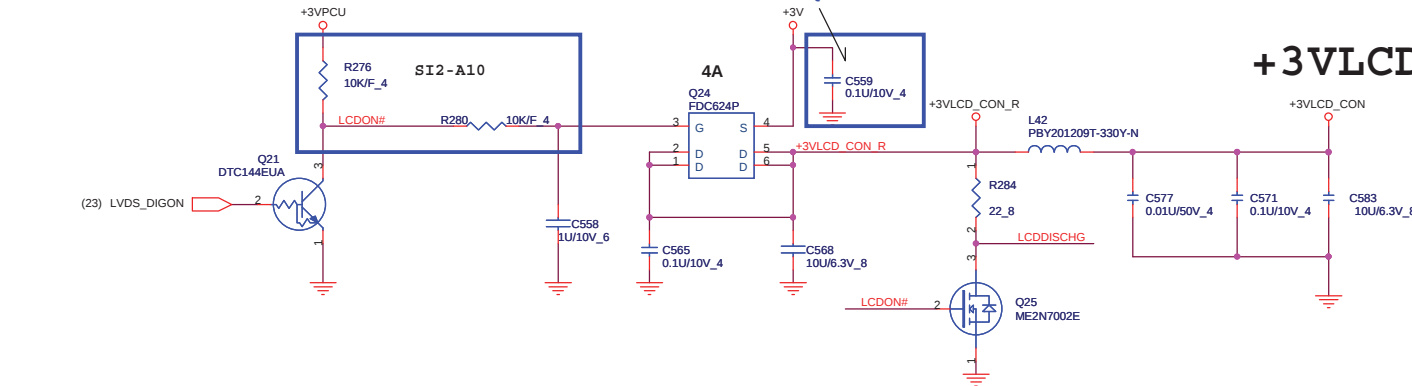
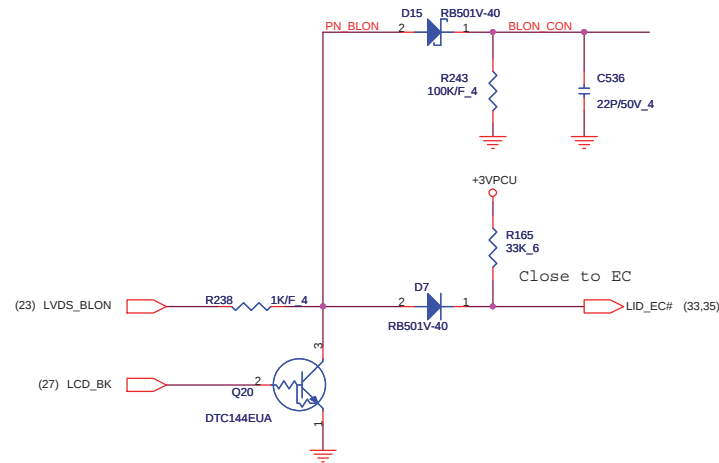
$$V_{out}=1.25(1+R1/R2)$$



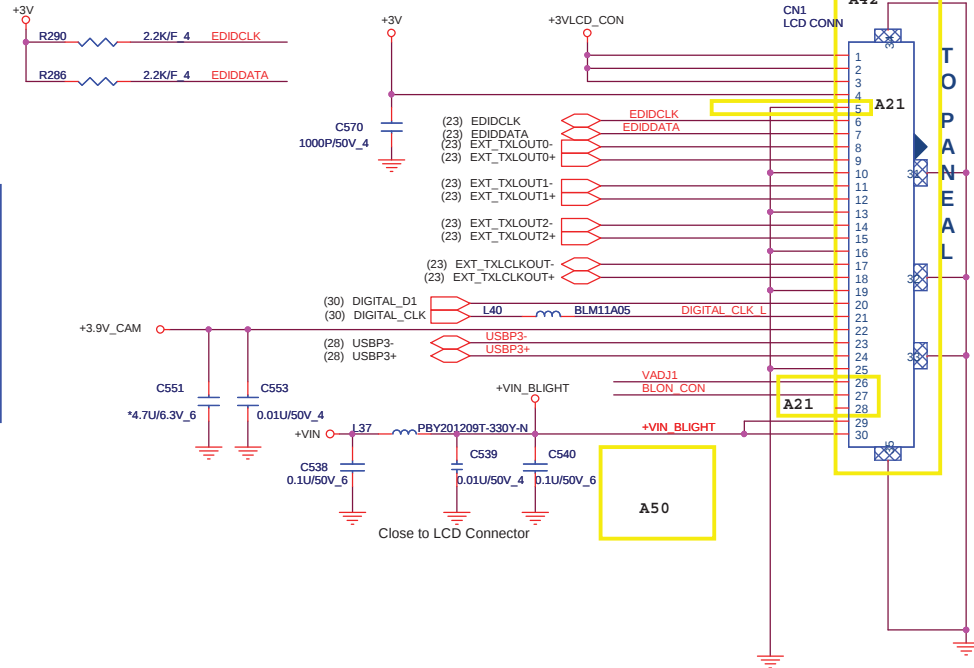
Add for EMI solution



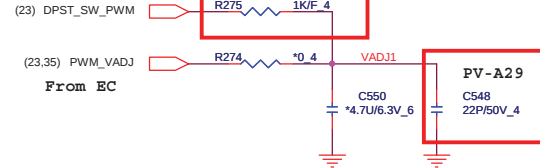
Close to LCD#21



(2,4,7,10,12,14,25,26,27,28,29,30,31,32,33,34,35,36,45)  
(20,23,25,29,31,36,45)  
(37,39,40,41,42,43,44,45)  
(26,32,33,35,37,38,39,43,44,45)

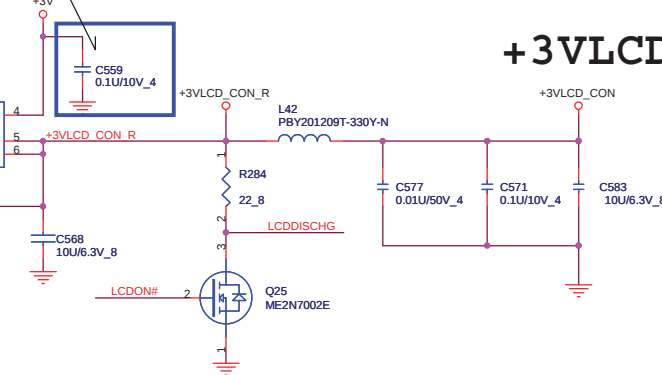


From Switch



+3VLCD

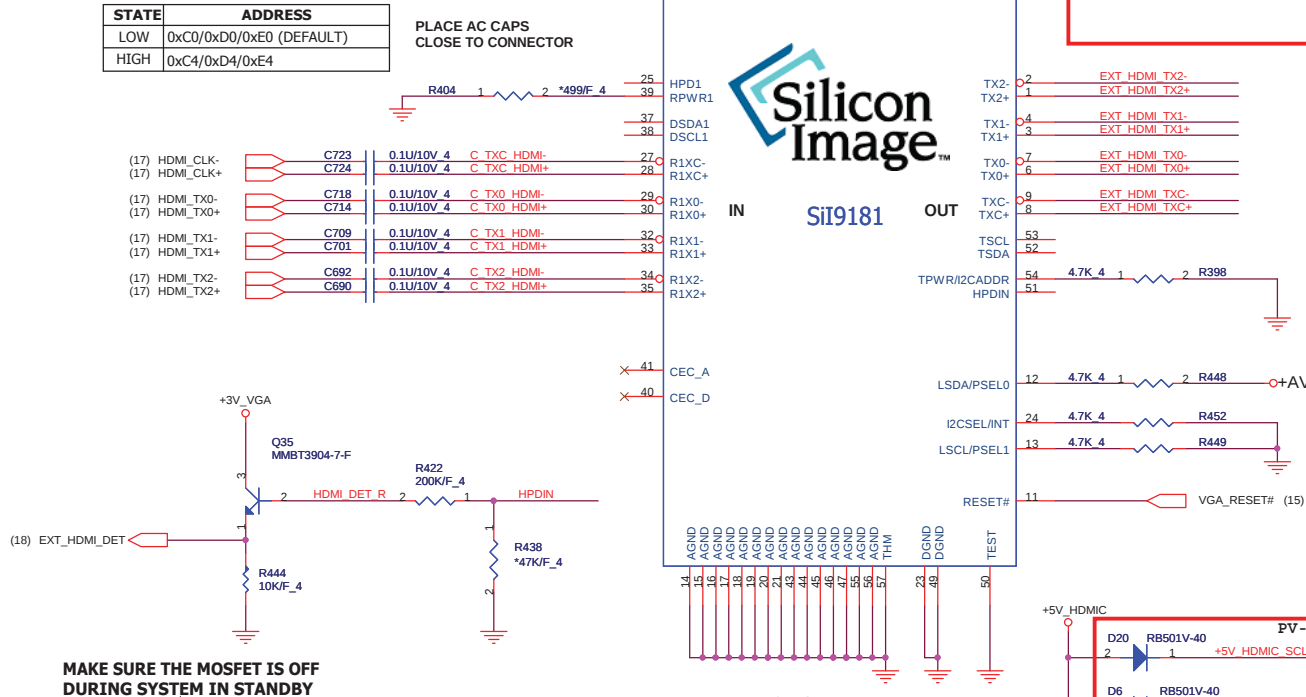
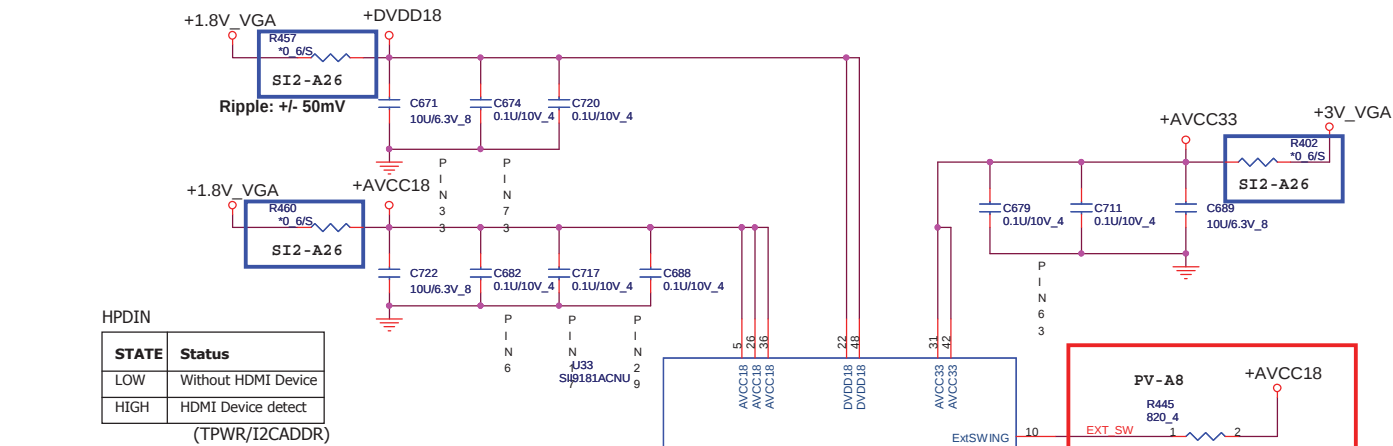
Close to Q24#4



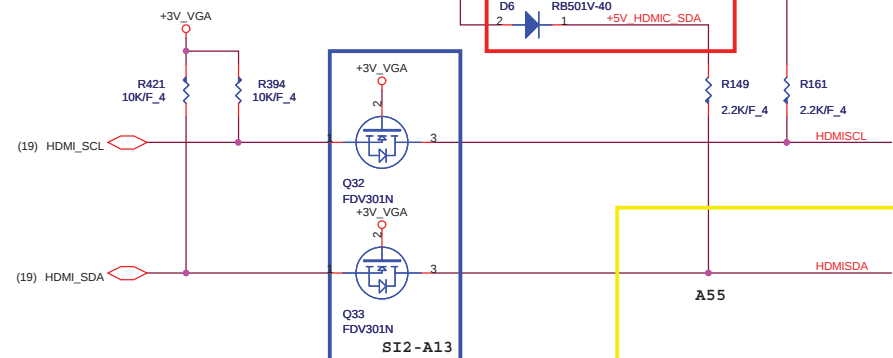
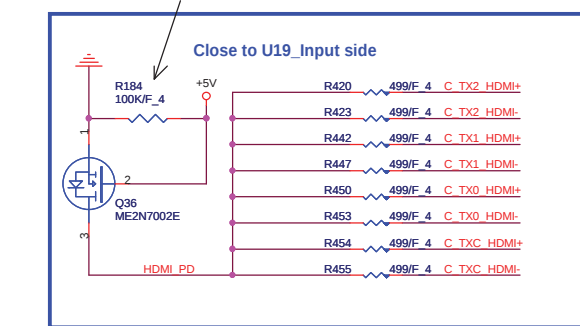
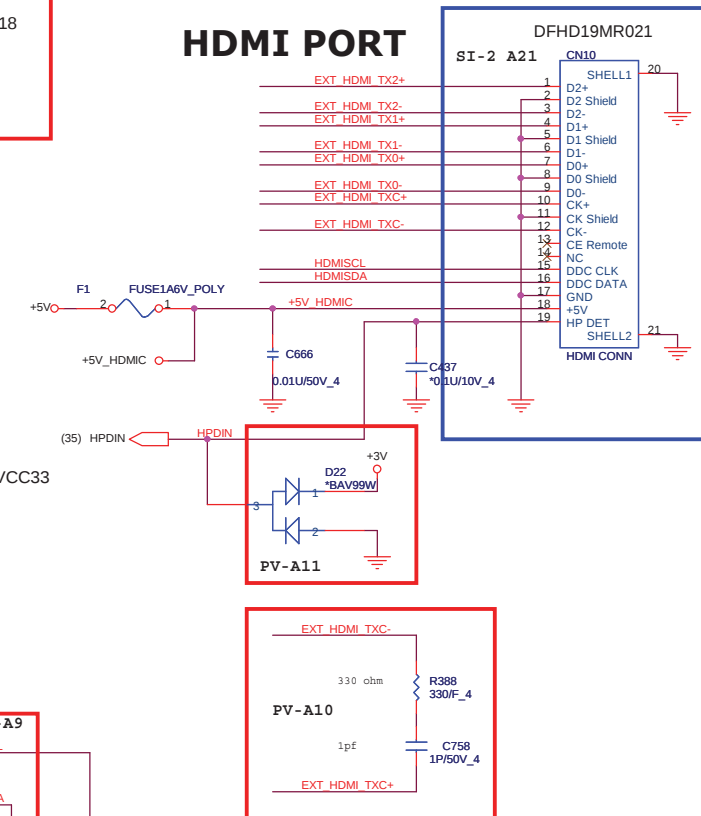
PROJECT : SP6  
Quanta Computer Inc.

| Size                          | Document Number         | Rev |
|-------------------------------|-------------------------|-----|
| Custom                        | LVDS/Camera/Digital MIC | 1A  |
| Date: Tuesday, April 07, 2009 | Sheet 24 of 49          |     |

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## HDMI PORT



PROJECT : SP6  
Quanta Computer Inc.



## XOR Chain Entrance Strap

ICH9-M LAN100\_SLP Strap  
(Internal VR for  
VccLAN1\_05 and  
VccCL1.05)

|            |                                                                  |
|------------|------------------------------------------------------------------|
| LAN100_SLP | Low = Internal VR disabled<br>High = Internal VR enable(Default) |
|------------|------------------------------------------------------------------|

| ICH_TP3 | HDA_SDOUT | Description                |
|---------|-----------|----------------------------|
| 0       | 0         | RSVD                       |
| 0       | 1         | Enter XOR Chain            |
| 1       | 0         | Normal operation(Default)  |
| 1       | 1         | Set PCIe port config bit 1 |

|       |           |          |
|-------|-----------|----------|
| STRAP | PCI_GNT0# | SPI_CS#1 |
|-------|-----------|----------|

| SPI | PCI | LPC |
|-----|-----|-----|
| 0   | 1   | 1   |
| 1   | 0   | 0   |
| 1   | 1   | 1   |

\*1K/F 4 R120 GNT0# (28)

\*1K/F 4 R376 ICH\_SPI\_CS1# R (28)

|           |                                                 |
|-----------|-------------------------------------------------|
| PCI_GNT#3 | Low = A16 swap override enabled<br>Hi = Default |
|-----------|-------------------------------------------------|

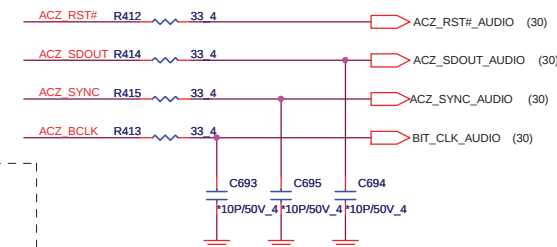
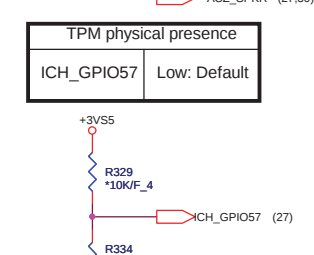
\*1K/F 4 R112 GNT3# (28)

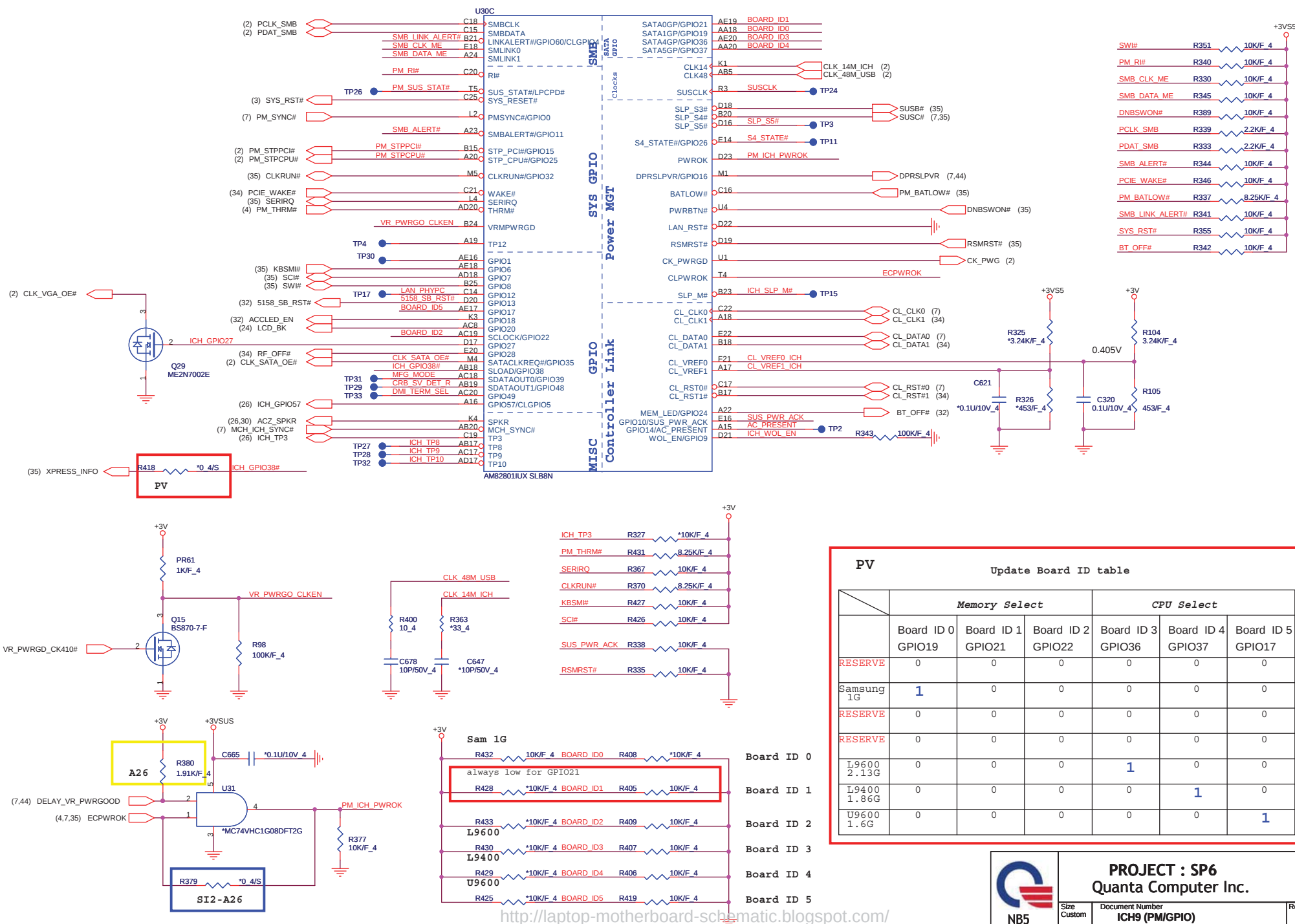
|          |                               |
|----------|-------------------------------|
| ACZ_SPKR | Low: Default<br>Hi: No reboot |
|----------|-------------------------------|

+3V

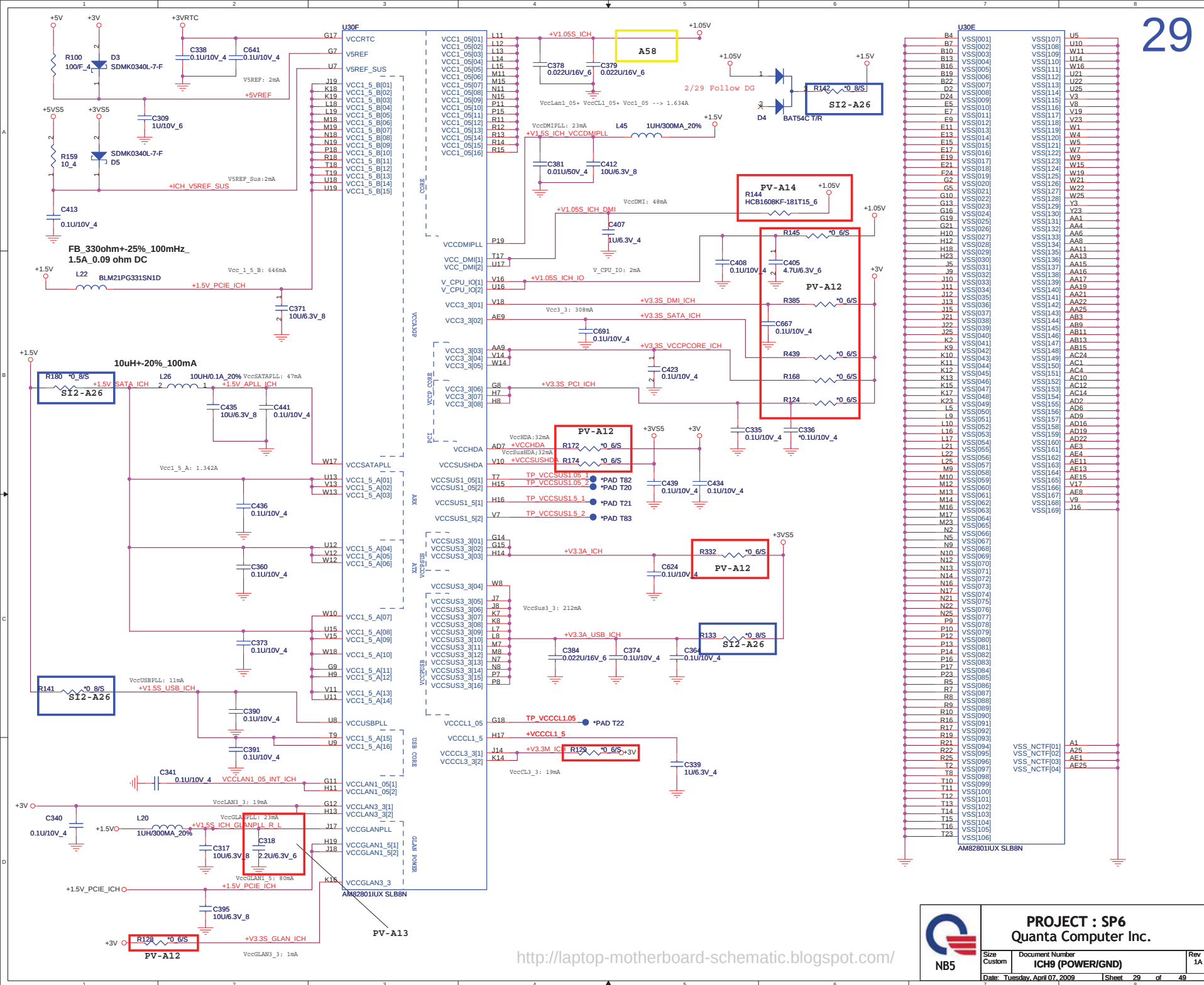
|            |              |
|------------|--------------|
| ICH_GPIO57 | Low: Default |
|------------|--------------|

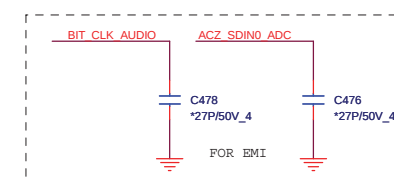
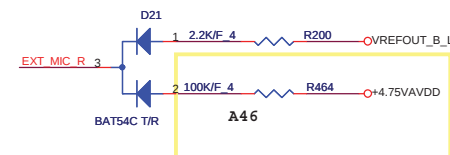
+3VS5



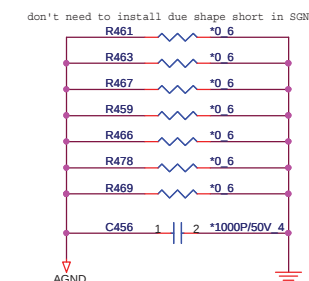




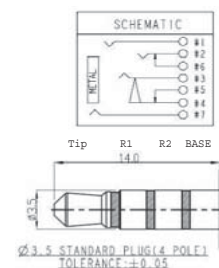
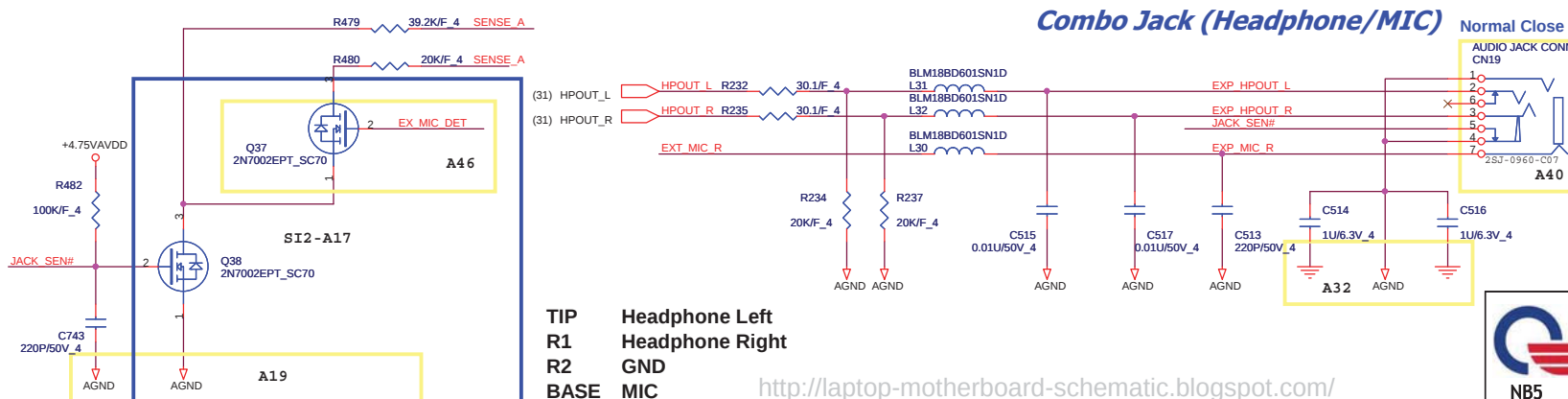




SA\_A# -->Headphone out  
SA\_B# -->EXT MIC

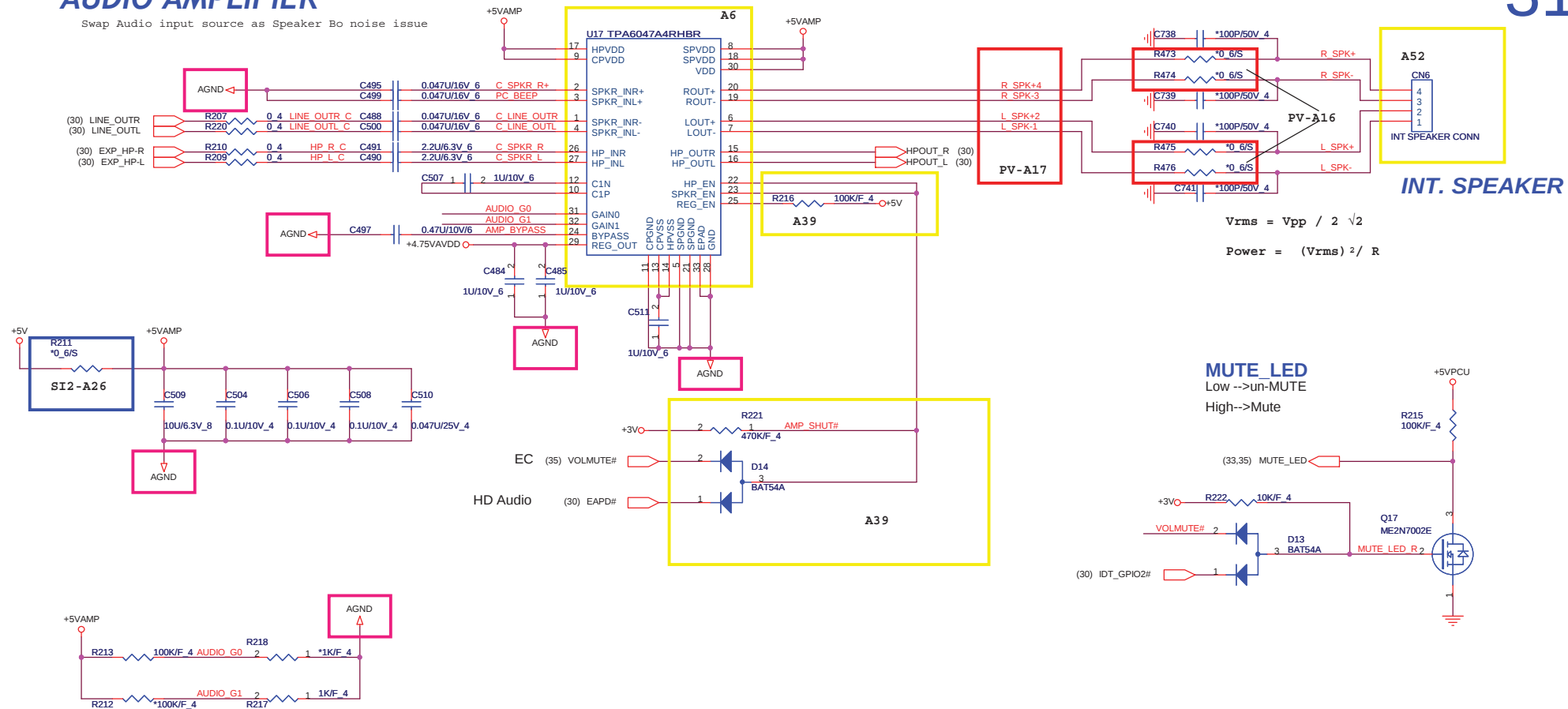


|              |           |            |
|--------------|-----------|------------|
| Normal Close |           |            |
| <b>SI-1</b>  | JACK_SEN# | EX_MIC_DET |
| None         | Low       | HIGH       |
| Normal HP    | HIGH      | Low        |
| HP+MIC       | HIGH      | HIGH       |



# AUDIO AMPLIFIER

Swap Audio input source as Speaker Bo noise issue



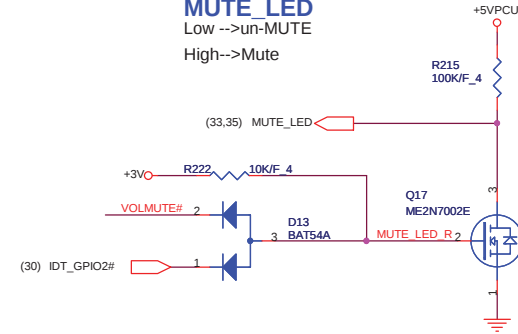
31

INT. SPEAKER

$$V_{rms} = V_{pp} / 2 \sqrt{2}$$

$$Power = (V_{rms})^2 / R$$

MUTE\_LED  
Low --> un-MUTE  
High --> Mute

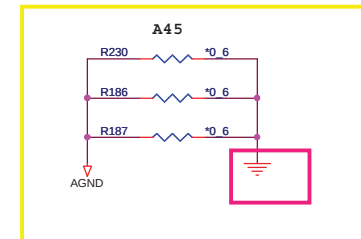


6047A2 Gain Table

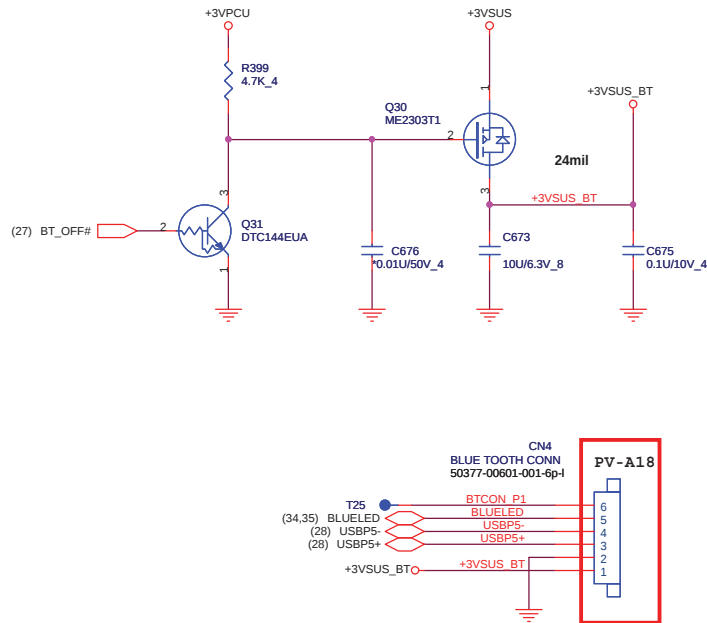
| GAIN0 | GAIN1 | AV     | RIN |
|-------|-------|--------|-----|
| 0     | 0     | 6dB    | 90K |
| 0     | 1     | 10dB   | 70K |
| 1     | 0     | 15.6dB | 45K |
| 1     | 1     | 21.6dB | 25K |

PIN23 SPKR\_EN

TPA6047A4 High enable

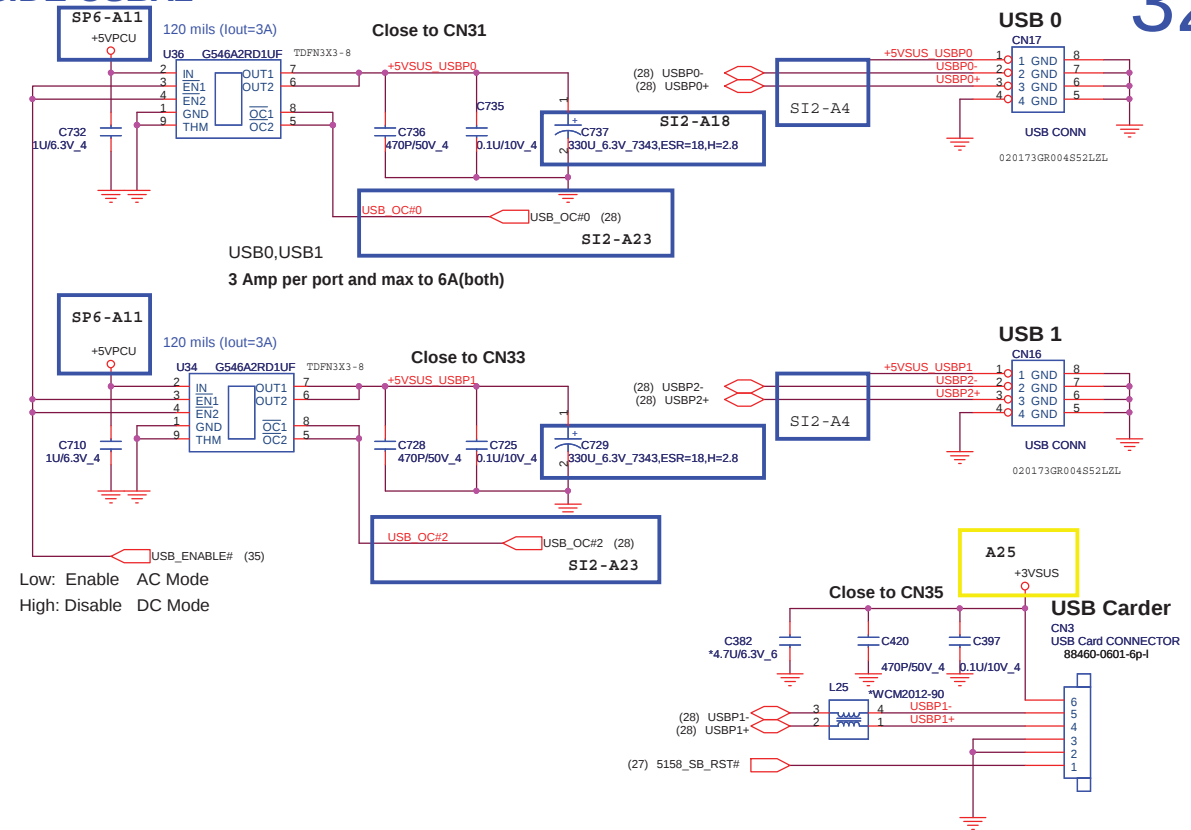


## BLUETOOTH



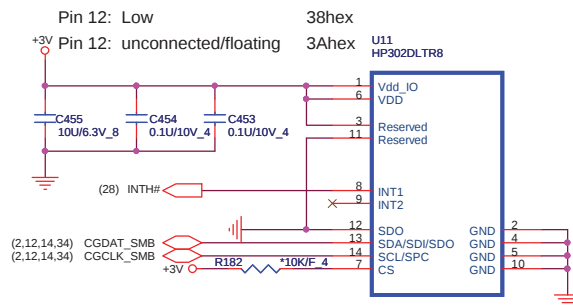
Change CN4 layout footprint to 50377-00601-001-6p-1

## LEFT SIDE USBX2



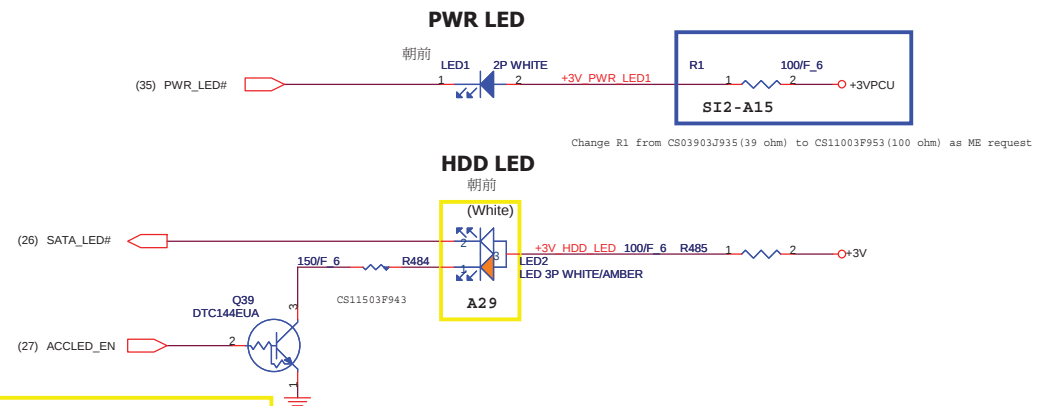
## Accelerometer Sensor

SGT-LIS302DLTR interrupt pin default is low / active Hi, BIOS need to programming 22h to change status from active Hi to low



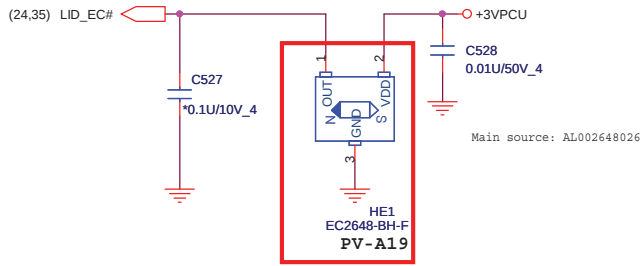
Change R181 to no stuff as internal pull high

## LED

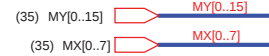
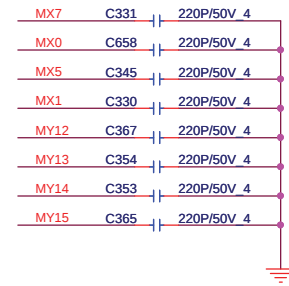
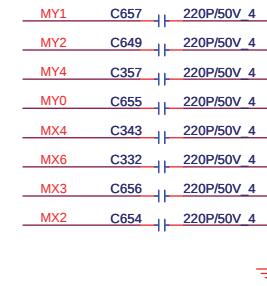
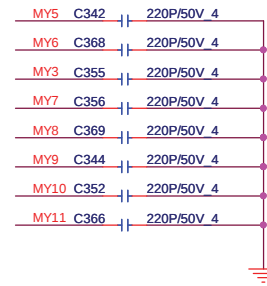
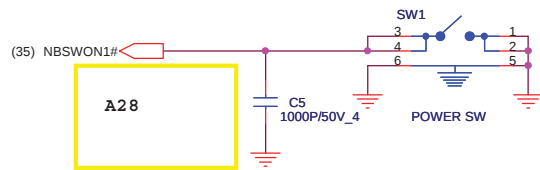


use a single 80 mil copper fill between digital ground and audio ground. None of the 0 ohm resistors should be used.

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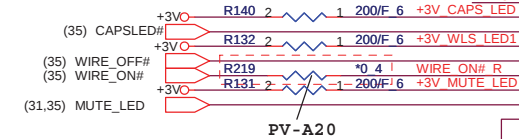
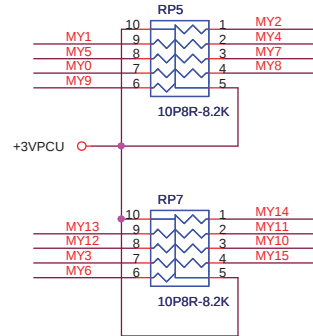


POWER SW

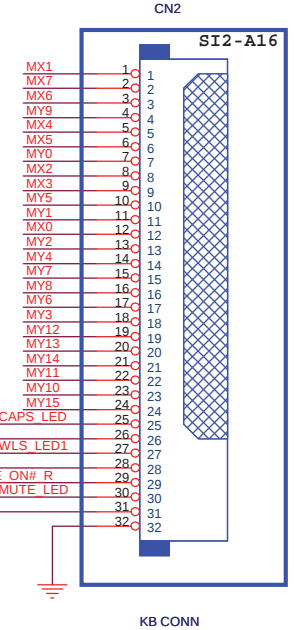


Modify CN2 footprint from bl137-32r1-tand-32p-1 to 196033-32041-32p-1

## KEYBOARD PULL-UP



PV-A20



KB CONN

|               |        |      |
|---------------|--------|------|
| Caps Lock LED | 2 Pins | 30mA |
| Wireless LED  | 3 pins |      |
| MUTE LED      | 2 Pins |      |
| Charge LED    | 3 pins |      |

Pin 32

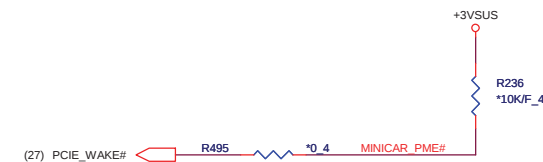
Pin 1

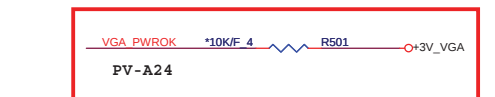
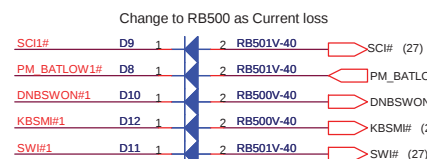


**PROJECT : SP6**  
**Quanta Computer Inc.**

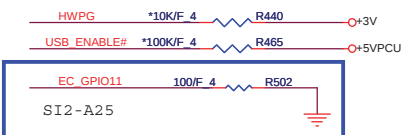
| Size B                        | Document Number | Rev       |
|-------------------------------|-----------------|-----------|
|                               | <b>KB/CAP</b>   | <b>1A</b> |
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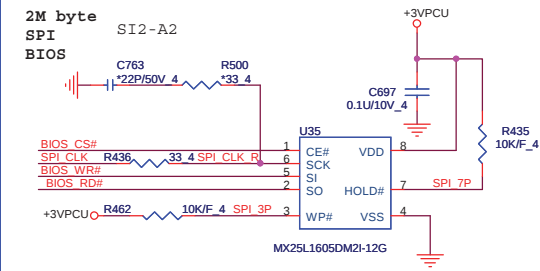




## 36



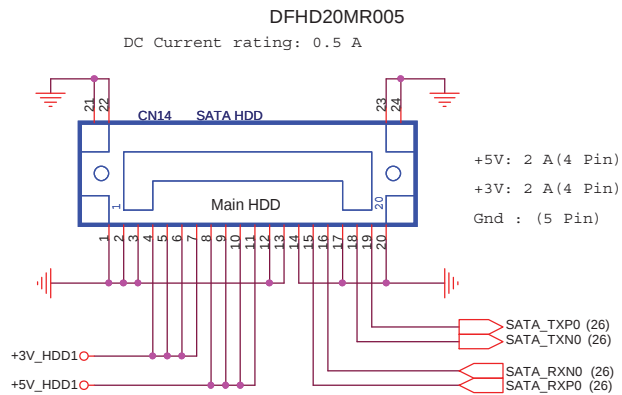
\_\_\_\_\_



Delete T10 and tie pin 117 from Lan for DSM

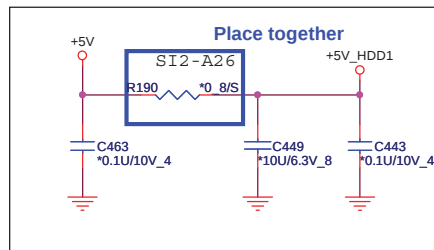
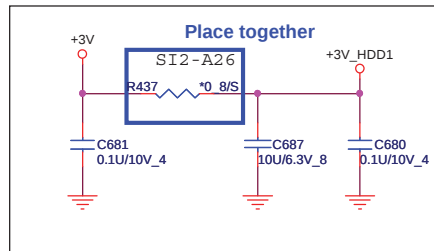
Sheet 35 of 4

## SATA 1.8" HDD CONNECTOR



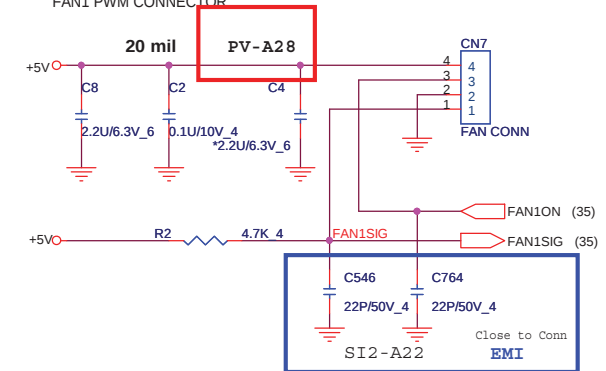
Modify 固定孔 Size as SMT request

GS12201-1011-9F-20P-L-QT6



### Master FAN

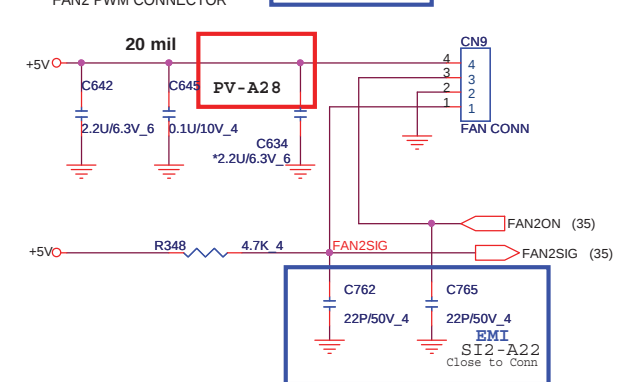
FAN1 PWM CONNECTOR



PWM signal

### Slave FAN

FAN2 PWM CONNECTOR

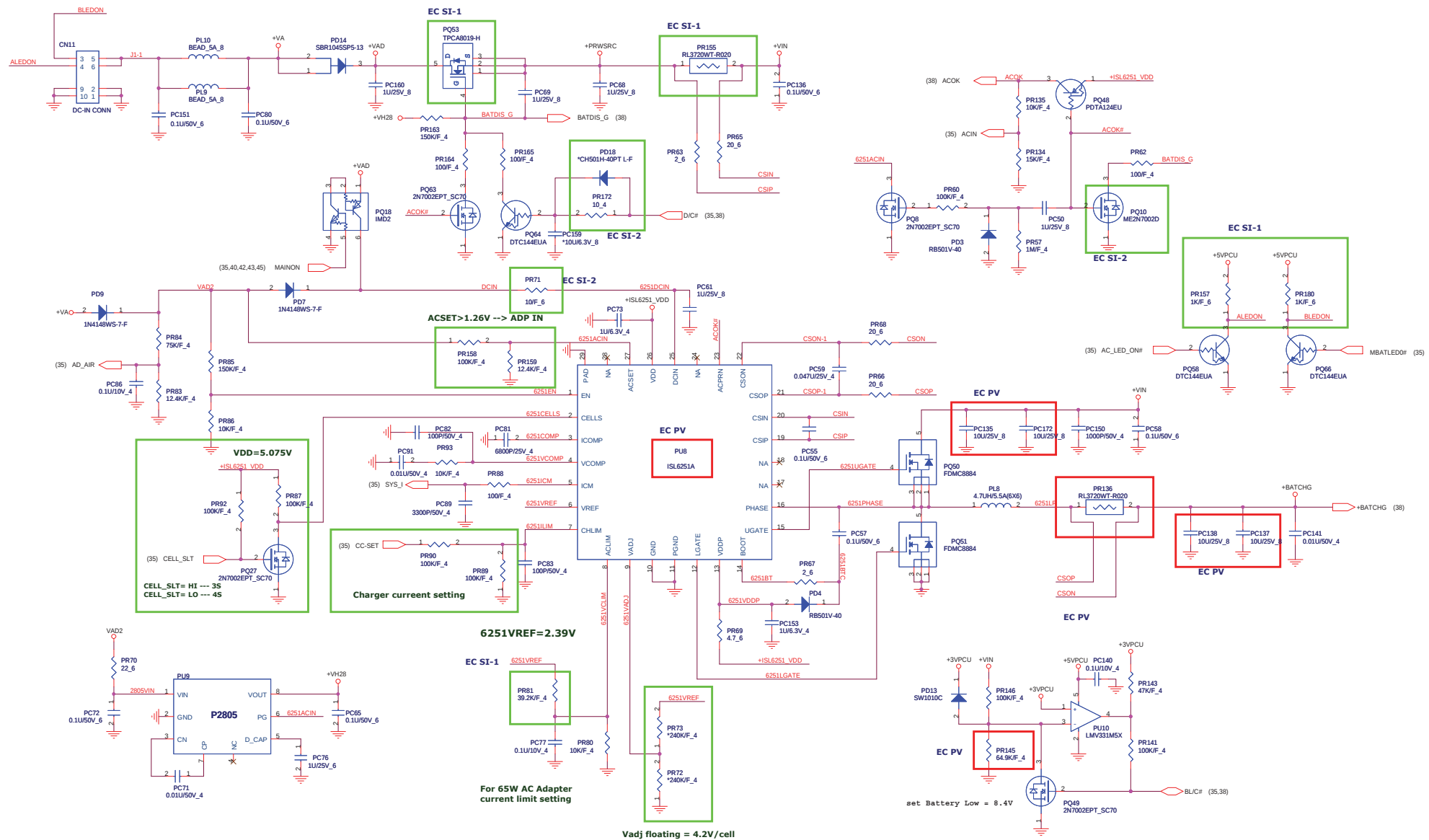


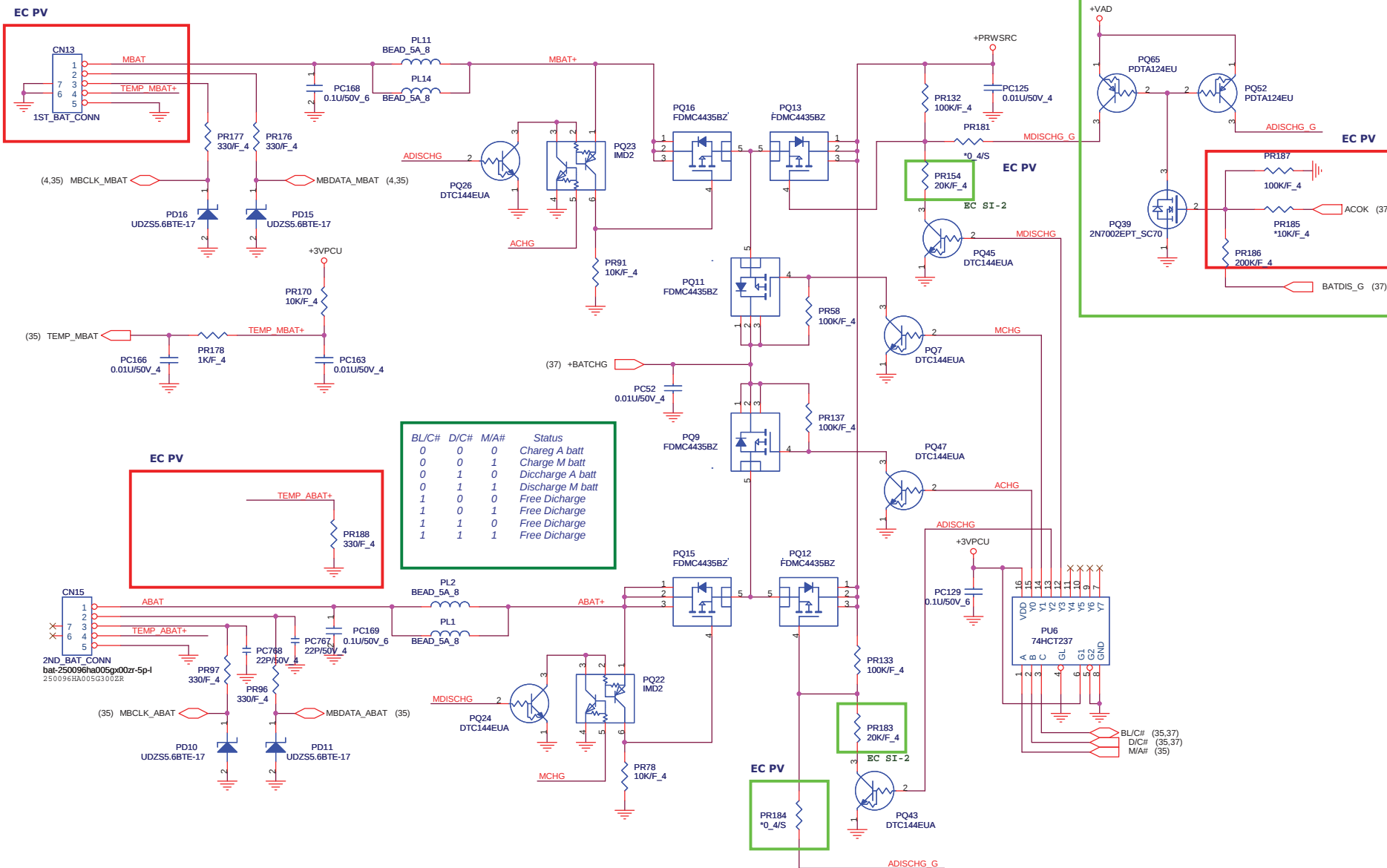
PWM signal



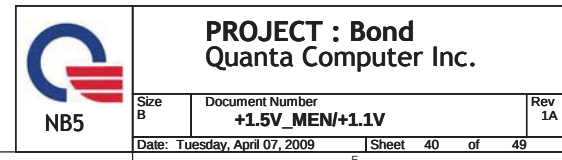
PROJECT : SP6  
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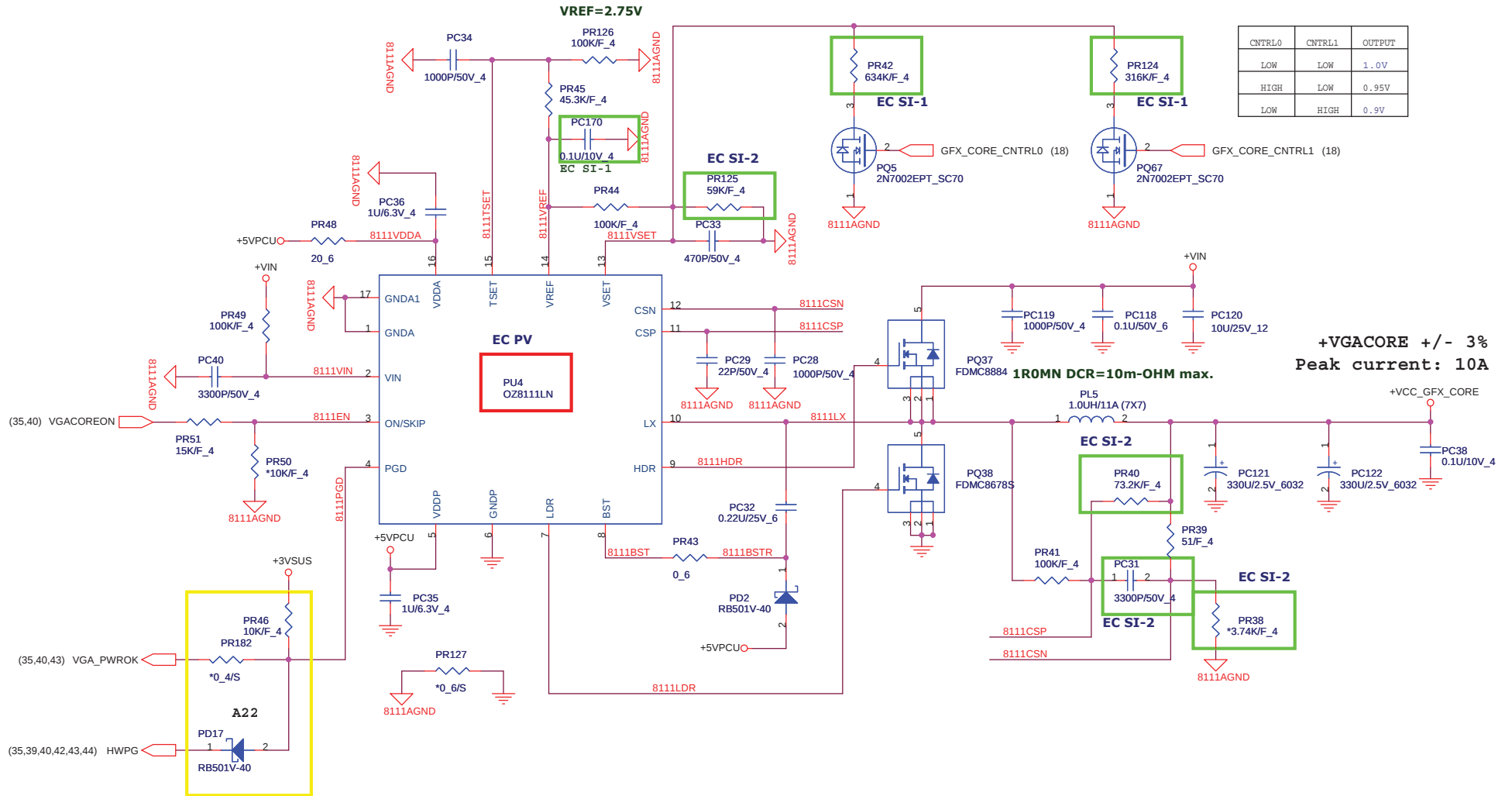
| Size B                        | Document Number | Rev |
|-------------------------------|-----------------|-----|
|                               | Fan1 and Fan2   | 1A  |
| Date: Tuesday, April 07, 2009 | Sheet 36 of 49  |     |





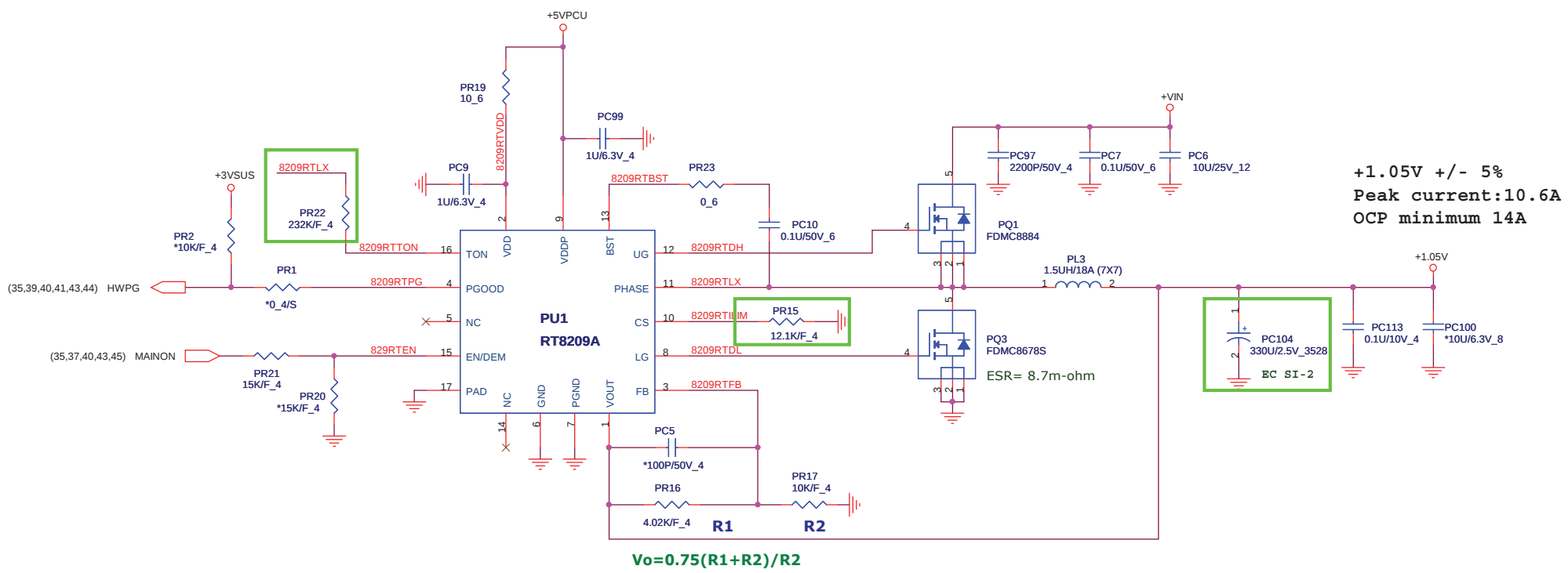






**PROJECT : Bond  
Quanta Computer Inc.**

| Size<br>B                     | Document Number<br>VGACORE | Rev<br>1A |
|-------------------------------|----------------------------|-----------|
| Date: Tuesday, April 07, 2009 | Sheet 41 of 49             |           |

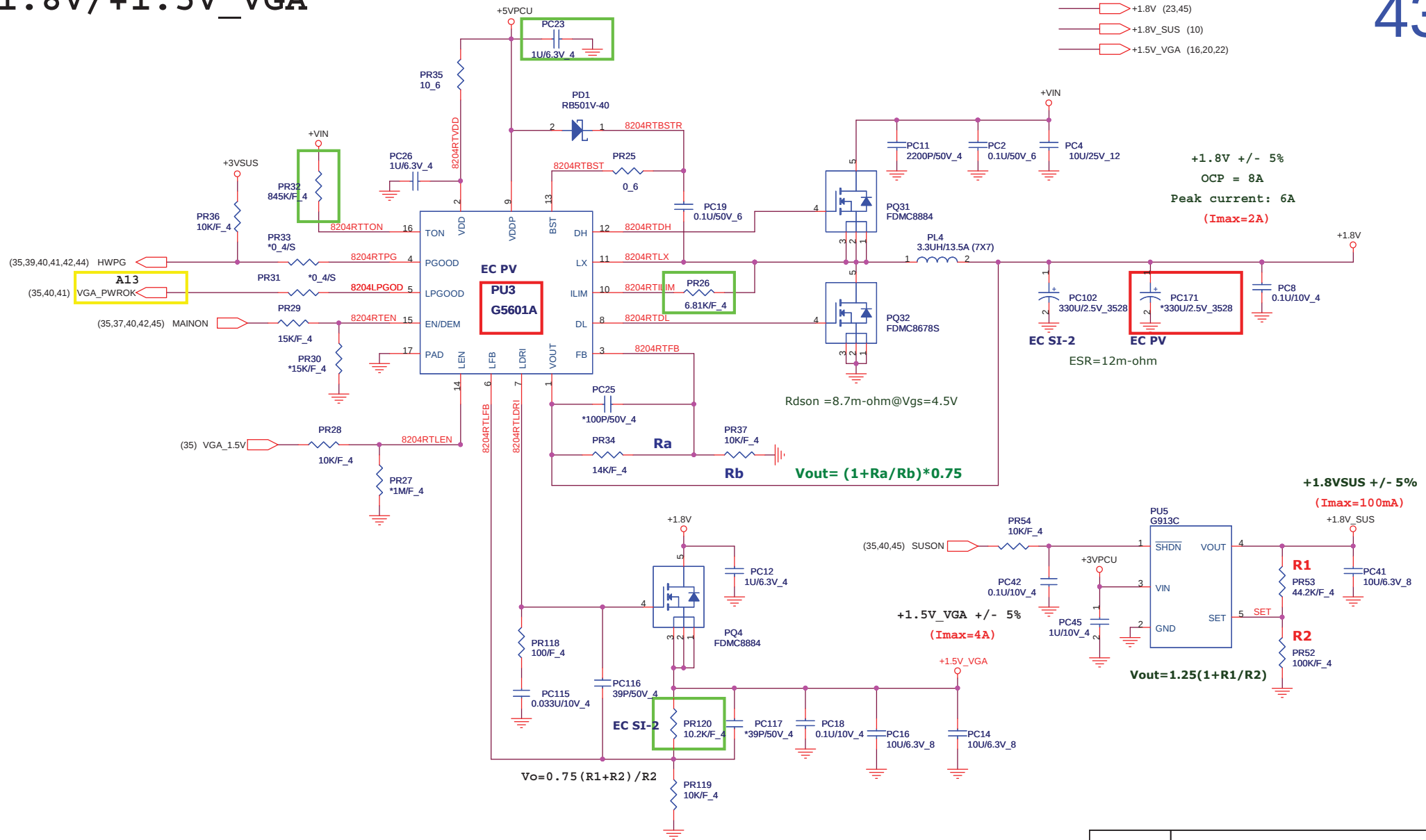


**PROJECT : Bond**  
**Quanta Computer Inc.**

|                               |                                        |        |
|-------------------------------|----------------------------------------|--------|
| Size B                        | Document Number<br><b>+1.05V/+1.5V</b> | Rev 1A |
| Date: Tuesday, April 07, 2009 | Sheet 42 of 49                         |        |

# +1.8V/+1.5V\_VGA

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| Size                          | Document Number | Rev |
|-------------------------------|-----------------|-----|
| B                             | +1.05V/+1.5V    | 1A  |
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