EVEREST-M

WS BULID

2010.01.04

INVENTEC

TITLE EVEREST-M
COVER PAGE

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

CHANGE by Frank Hu DATE Tue Jan 04 11:08:28 2011 SHEET 1 of 97

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EDP
3D PANEL
15.6 WXGA LED

MUX
PERICOM

eDP

eDP

IVY BRIDGE
QC 45W OR DC 35W
VT & TXT
SOCKET-RPGA989
37.5 X 37.5 X 5 mm

DUAL CHANNEL

DDR3@1.5/0.75V
(1600MHZ)
204-PIN SODIMM X2
MAX MEMORY 8GB X2

VRAM*4(64Mb*32)
TOTAL:1GB GDDR5

AMD

PEGX16

FDI

DMI 2.0

JTAG

60-PIN CPU XDP
(TEST ONLY)

HDR
HDMI 1.4

HDMI

ATI WHISTLER XT
35W
29MM X 29MM

JTAG

60-PIN PCH XDP
(TEST ONLY)

HDR
VGA

R

RGB

JTAG

LS

HDR
RJ-11ME JTAG
(TEST ONLY)

R

RGB

HDR(DONGLE)
HDMI 1.4

HDR
DISPLAYPORT 1.1
(TEST ONLY)

DP

PCH

COUGAR POINT
TDP 3.9W
25 X 25 X 2.3 mm

HDA

AUDIO CODEC
REALTEK
ALC269Q_VC

INTERNAL MIC IN

EXT MIC IN

HEADPHONE/LINEOUT

HDR
LVDS
(TEST ONLY)

LVDS

SPI

SPI FLASH 8MB
WINB_W25Q64BVSSIG

RJ45

Gbe Phy
(100/1000)
LEWISVILLE
INTEL 82579LM_BAM271

PCIE_6

USB_0 RESERVE FOR USB3.0
USB_2 RESERVE FOR USB3.0
USB_1 eSATA PORT
USB_5 Minicard WLAN
USB_10 Webcam
USB_12 Bluetooth
USB_13 Minicard 3G

USB 2.0

SIM CARD
CONNECTOR

PCIE_3: WIFI
PCIE_4: 3G/mSATA

PCIE

USB 3.0
TI_TUSB7320

PCIE_1

SATA

SATA3_0: SSD
SATA3_1: HDD
SATA2_2: ZERO POWER ODD
SATA2_3: eSATA
SATA2_4: mSATA

USB3.0

CONN A

CONN B

CARD READER
RTS5209

PCIE_2

LPC

TPM V1.2
SLB9635TT1.2_FW3.17

EC WINDBOND
NPCE791LA0DX

SPI

SPI Flash 1MB
WINB_W25Q80BVSSIG

KEYBOARD

TOUCH PAD

BATTERY CHARGER &
DC/DC & IMVP 7

LI-ION BATTERY
6-Cell

INVENTEC

TITLE: EVEREST-M
BLOCK DIAGRAM

SIZE	CODE	DOC.NUMBER	REV
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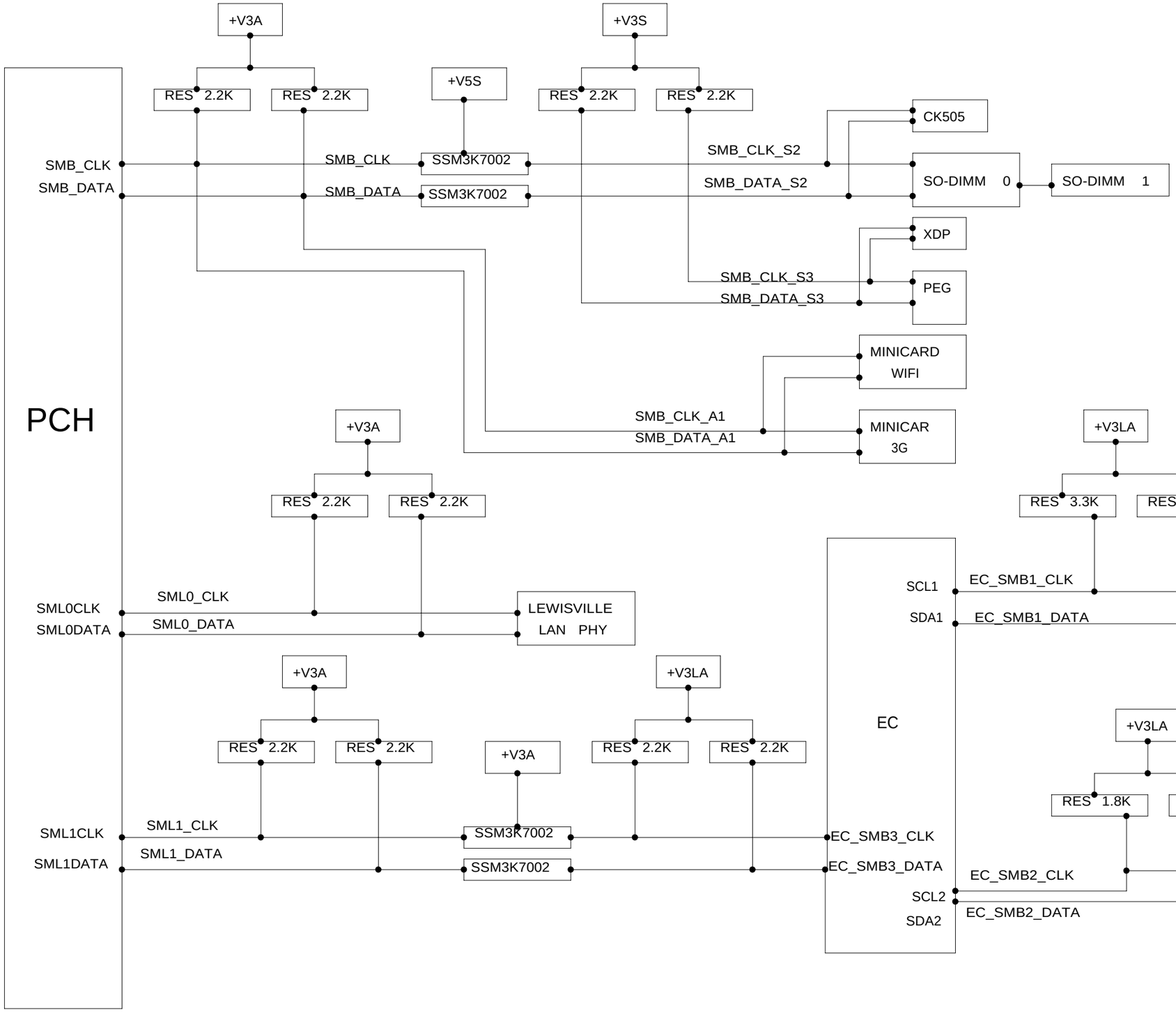


PCIE	
1	USB3.0_TUSB7320
2	CardReader_RTS5209
3	WLAN
4	MINICARD3G
5	NC
6	LAN
7	NC
8	NC

SATA	
0	SSD
1	HDD
2	ODD
3	eSATA
4	mSATA
5	NC

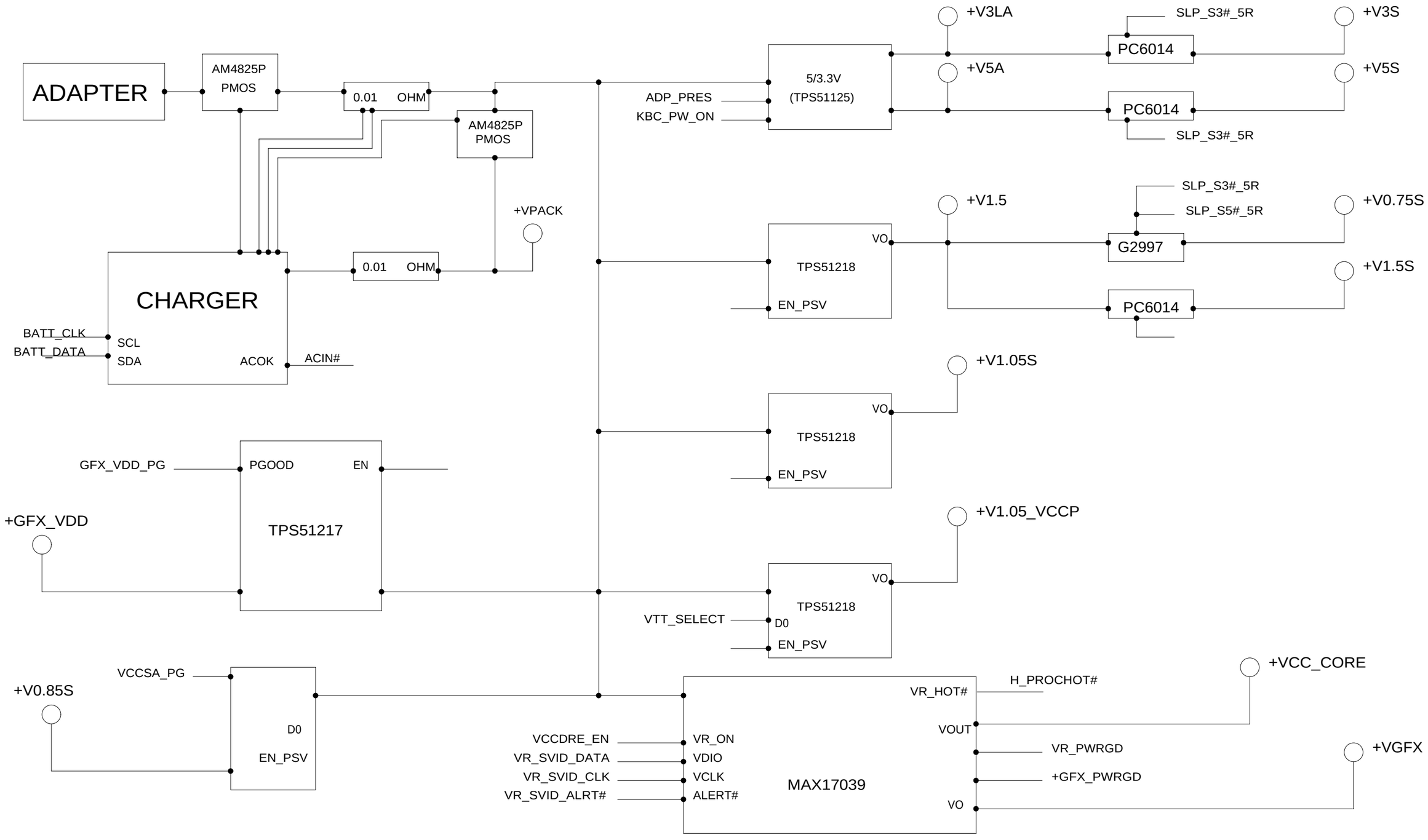
USB	
0	Reserve for USB3.0
1	eSATA
2	Reserve for USB3.0
3	NC
4	NC
5	MINICARD WLAN
6	NC
7	NC
8	NC
9	NC
10	WEBCAM
11	NC
12	BLUE TOOTH
13	MINICARD 3G

INVENTEC

TITLE: EVEREST-M
SMB DIAGRAM

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

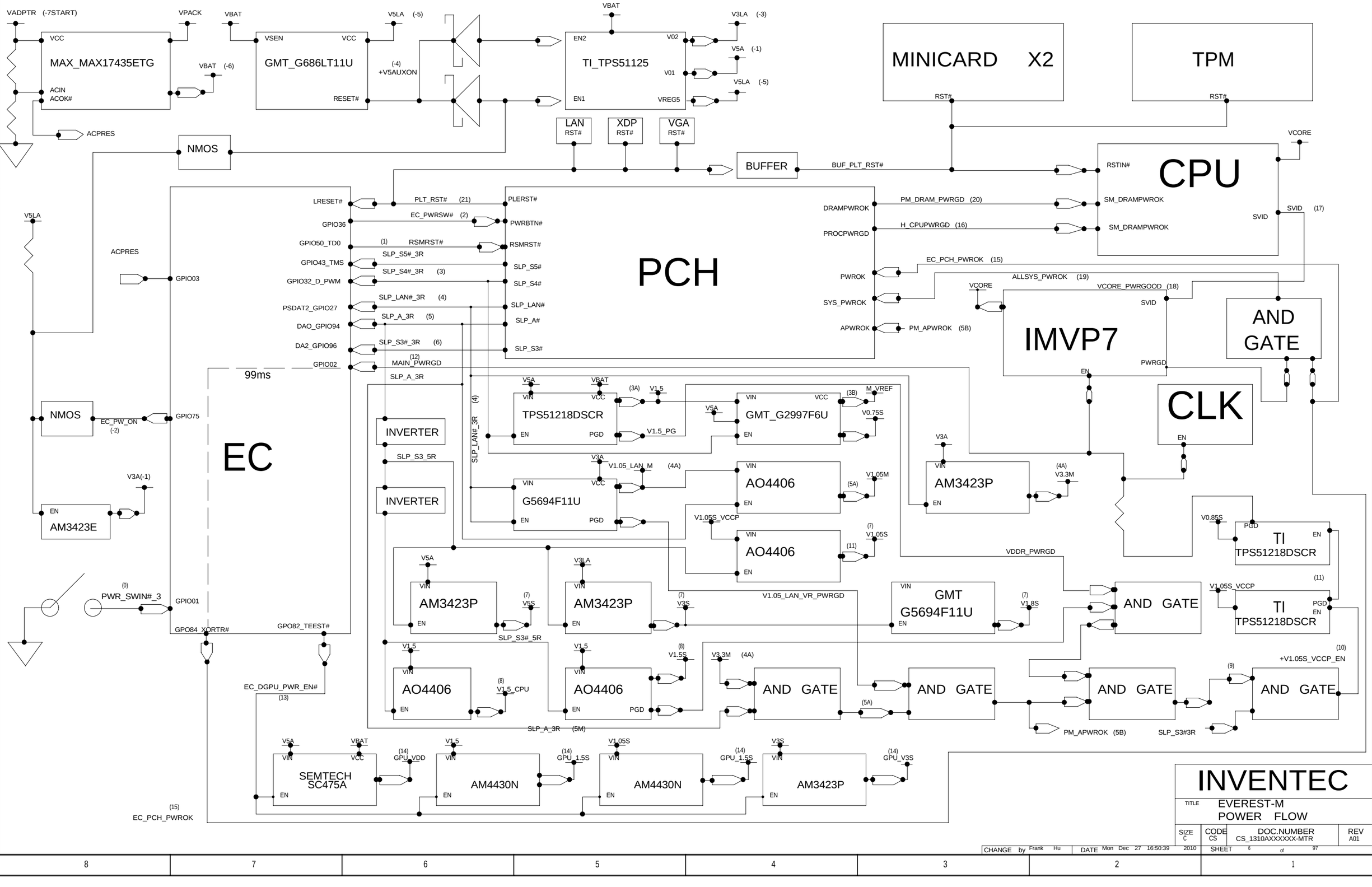
CHANGE by Frank Hu DATE Mon Dec 27 16:50:16 2010 SHEET 4 of 97



INVENTEC

TITLE	EVEREST-M POWER SEQUENCE BLOCK		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Mon Dec 27 16:50:27 2010	SHEET 5 of 97	

EVEREST PWROWSEQUENCE



TITLE	EVEREST-M POWER FLOW
SIZE	C
CODE	CS
DOC.NUMBER	CS_1310AXXXXXX-MTR
REV	A01
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INVENTEC

FIX1 FIX_MASK
FIX2 FIX_MASK
FIX3 FIX_MASK
FIX4 FIX_MASK
FIX5 FIX_MASK
FIX6 FIX_MASK
FIX7 FIX_MASK
FIX8 FIX_MASK

CPU

S1 SCREW330_600_800_1P
S10 SCREW330_600_800_1P
S18 SCREW330_600_800_1P
S22 SCREW330_600_800_1P

MB

S24 SCREW300_700_1P
S4 SCREW300_1000_1P
S3 SCREW300_1000_1P
S12 SCREW300_1000_1P
S20 SCREW300_1000_1P
S23 SCREW300_1000_1P
S25 SCREW500_1000_1P
S26 SCREW300_1000_1P

MINI CARD

S14 SCREW120_500_0_1P

FAN

S7 SCREW120_0_500_1P
S16 SCREW120_0_500_1P

PCH

S17 SCREW120_0_500_1P
S27 SCREW120_0_500_1P

GPU

S9 SCREW320_500_400_1P
S11 SCREW320_500_400_1P
S19 SCREW320_500_400_1P
S33 SCREW320_500_400_1P

INVENTEC

TITLE EVEREST-M
PCB SCREW

SIZE	CODE	DOC.NUMBER	REV
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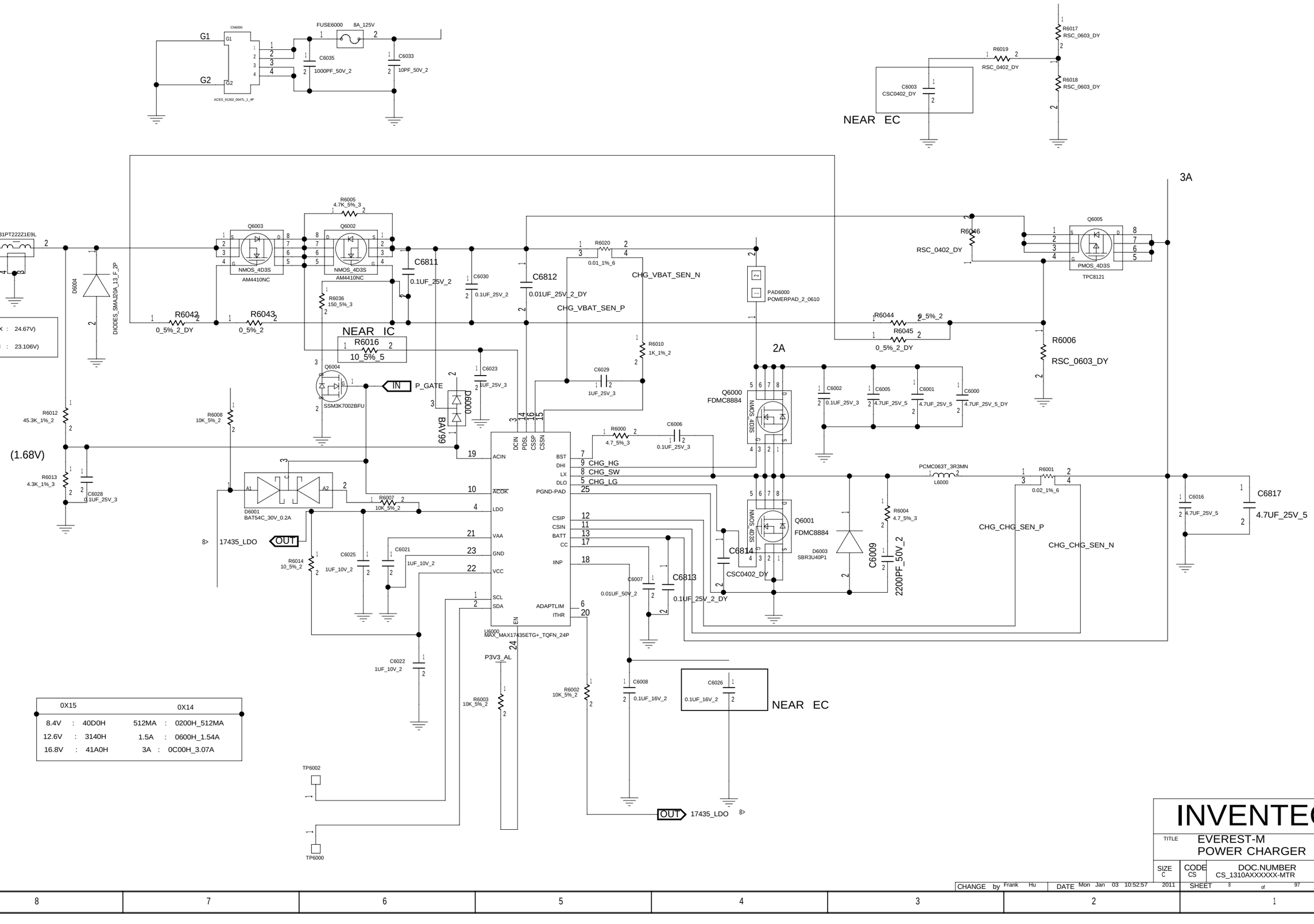
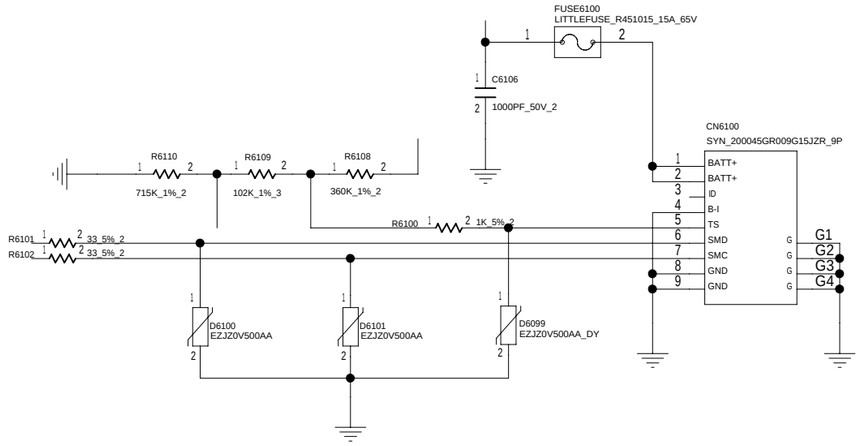
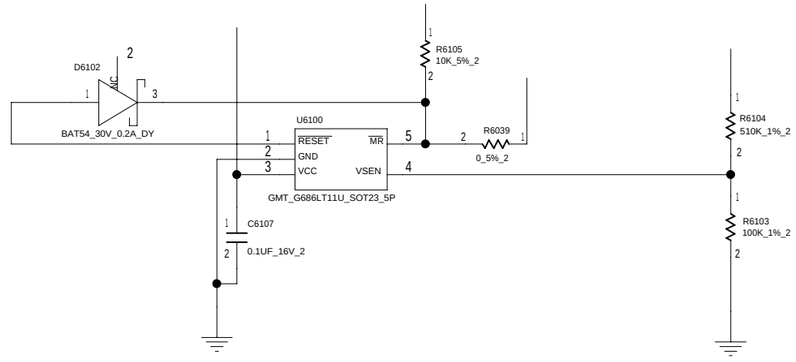
CHANGE by Frank Hu DATE Fri Dec 31 10:16:56 2010 SHEET 7 of 97



INVENTEC

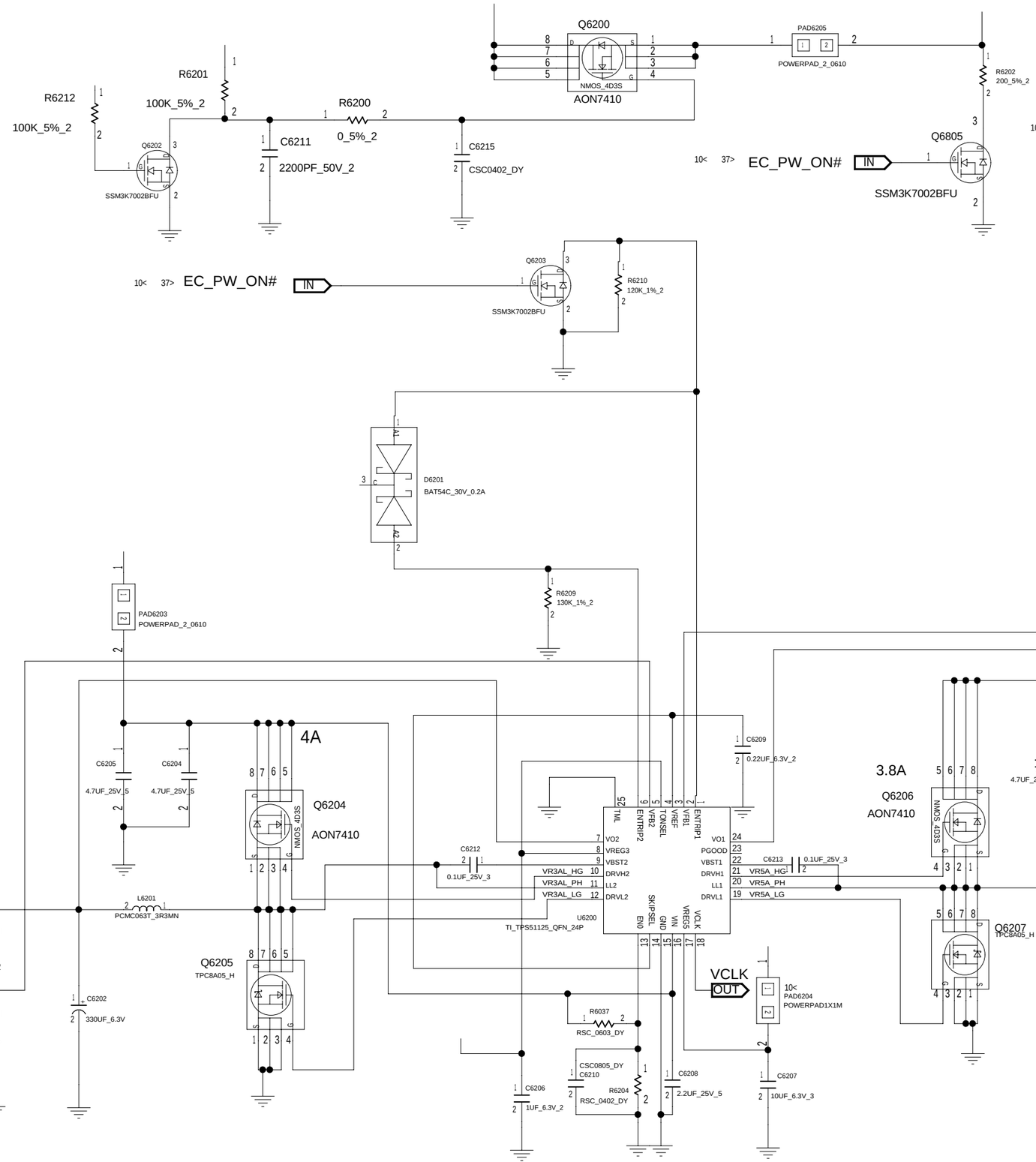
TITLE	EVEREST-M POWER CHARGER		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Mon Jan 03 10:52:57 2011	SHEET 8 of 97	





INVENTEC

TITLE	EVEREST-M POWER BATTERY		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Mon Jan 03 10:53:36 2011	SHEET 9 of 97	



INVENTEC

TITLE	EVEREST-M POWER +3A/+5A
SIZE C	CODE CS
DOC.NUMBER	CS_1310AXXXXXX-MTR
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CHANGE by	Frank Hu
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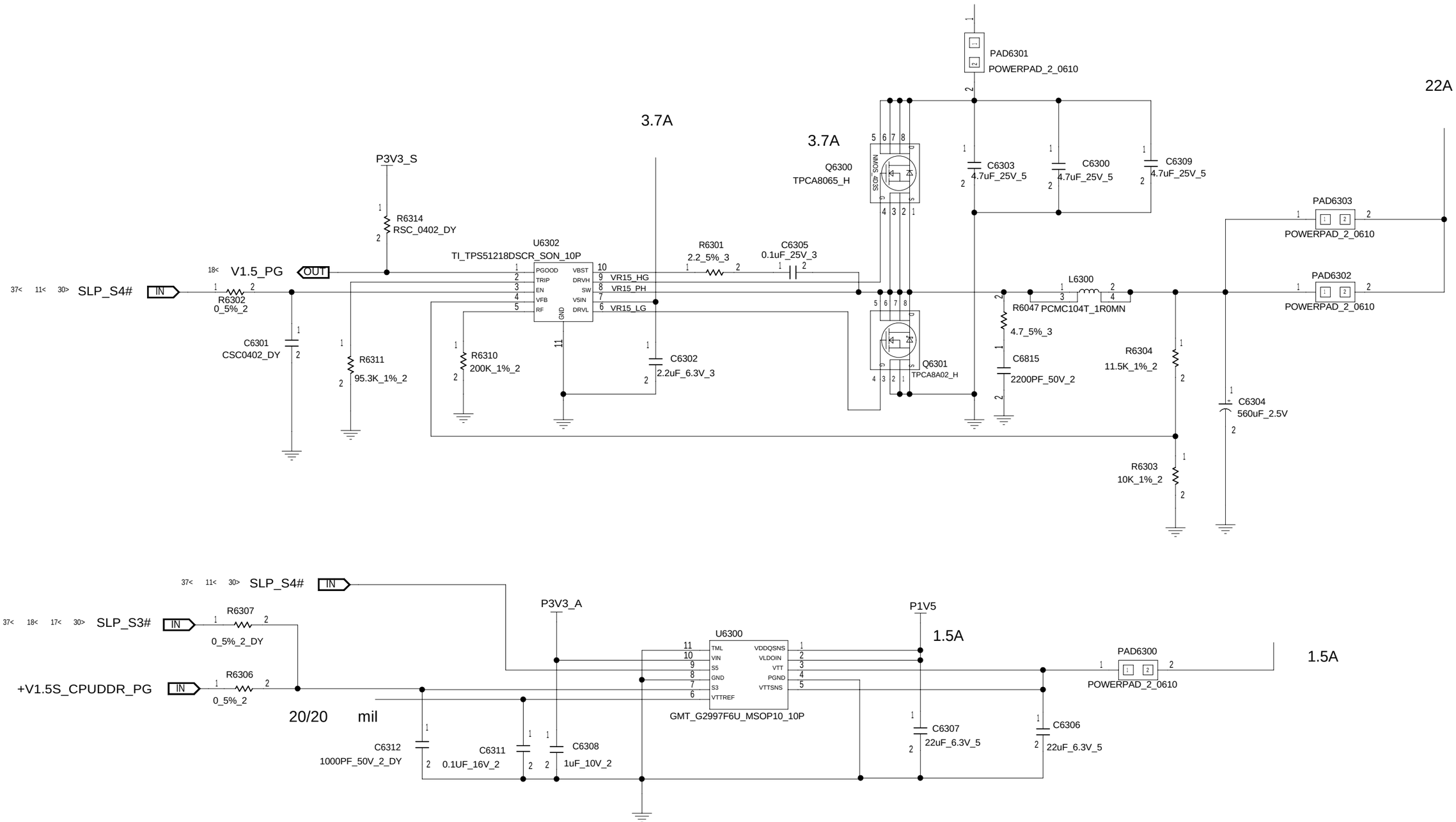
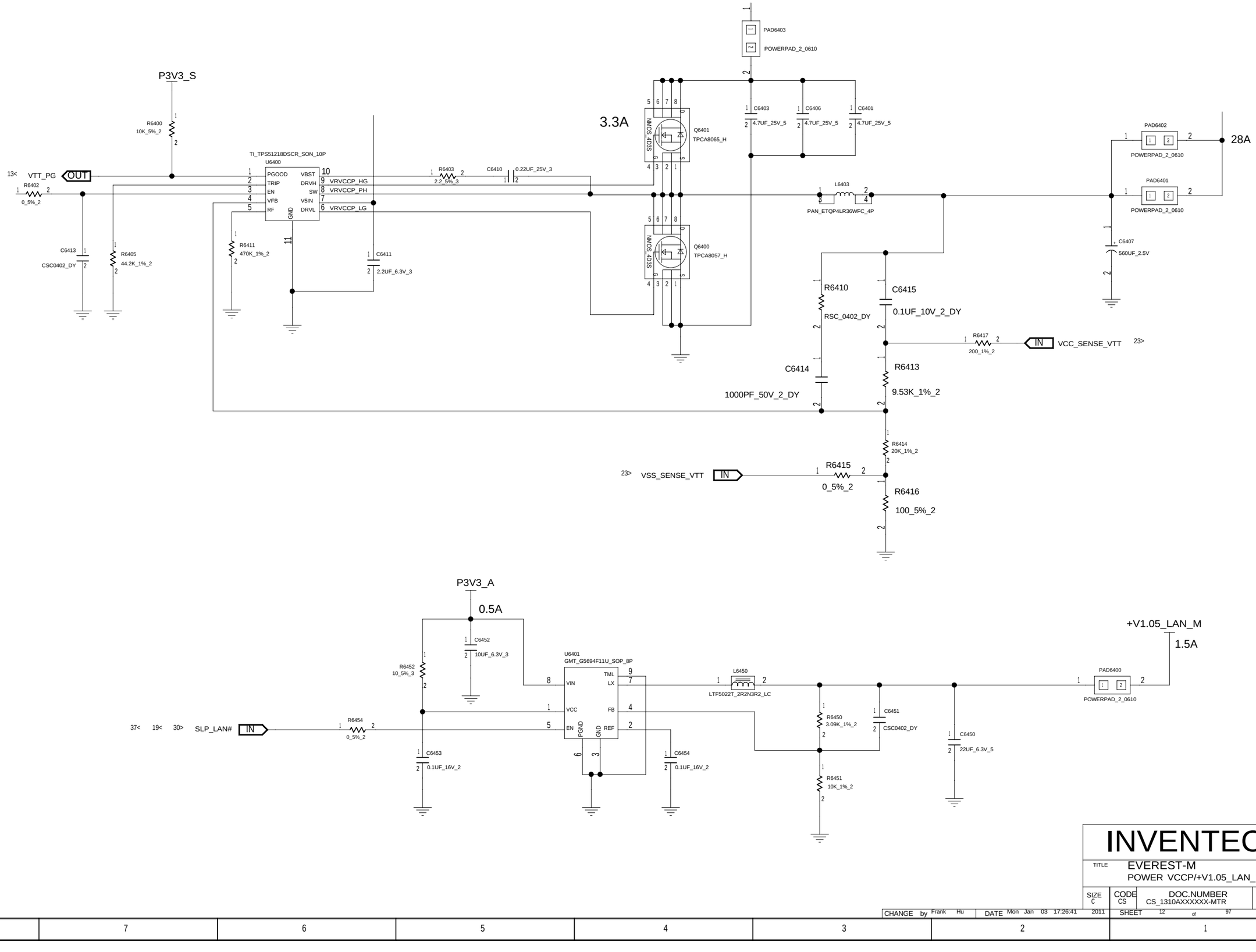
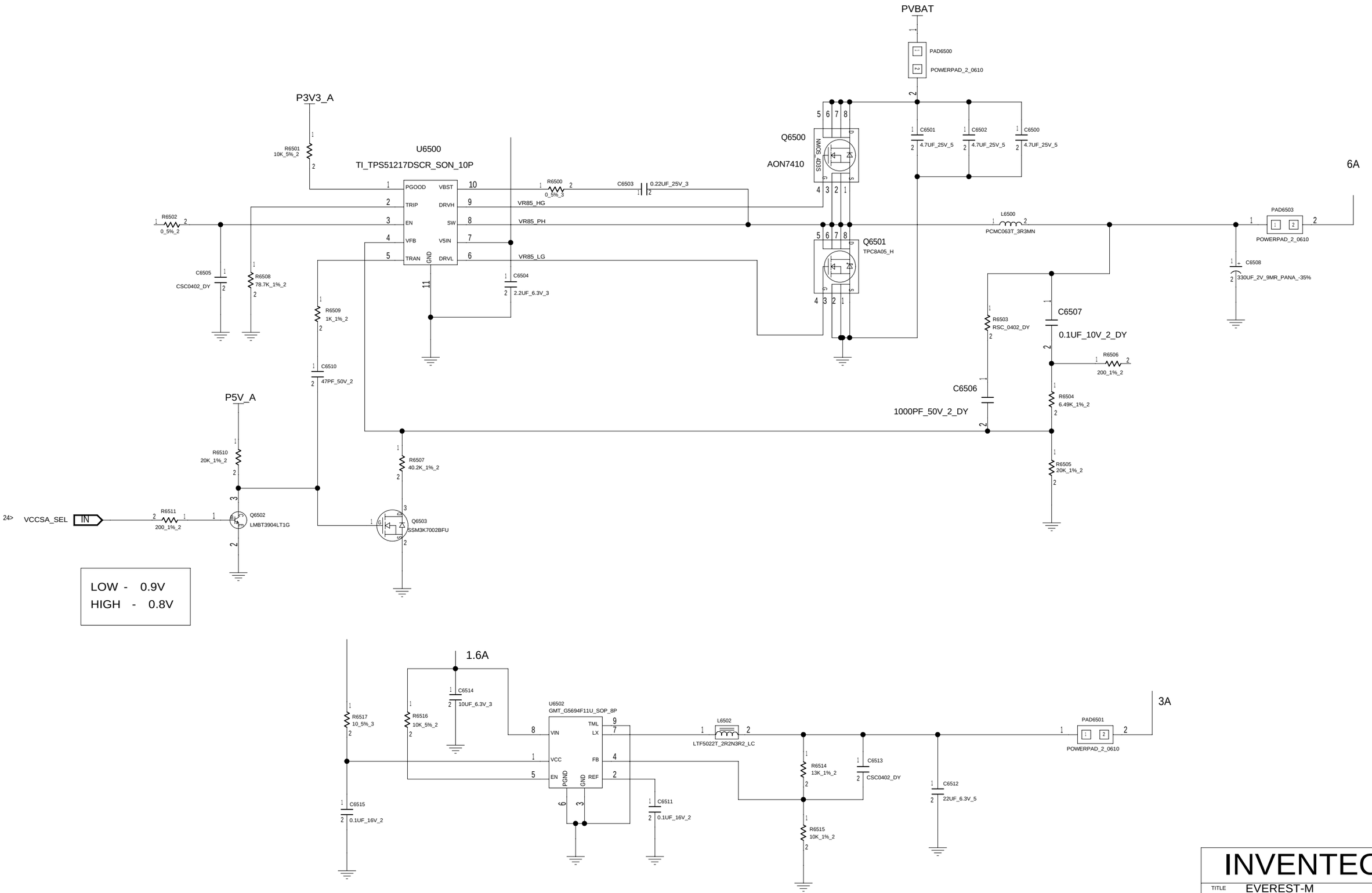


INVENTEC			
TITLE	EVEREST-M POWER +V1.5/+V0.75S		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Mon Jan 03 17:25:55 2011	SHEET 11 of 97	



INVENTEC

TITLE	EVEREST-M POWER VCCP/+V1.05_LAN_M		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Mon Jan 03 17:26:41 2011	SHEET 12 of 97	



TITLE	EVEREST-M POWER +V0.85S/+V1.8S		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
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INVENTEC

FOLLOW BERLIN 10RG

+VBAT_CPU P3V3_A P5V_A

R6622 178K_1%_2
R6620 0_5%_2
R6624 4.87K_1%_2

IN TONA 14<
IN IMAXA 14<
IN IMONA 14<
IN CCVA 14<
IN VBOOTA 14<
IN SRA 14<
IN THERMA 14<

R6621 20.5K_1%_2
C6615 470PF_50V_2
R6619 0_5%_2
R6618 115K_1%_2
R6626 100K_5%_2

IN VSSSENSE 23> 14<

PVBAT

10A

PAD6600
POWERPAD_2_0610

+VBAT_CPU

C6601 C6600 C6602 C6603 C6604 C6605 C6606 C6607
4.7UF_25V_5

P5V_A

U6602
MAX_MAX8791GTA+_TQFN_8P

14< PH3_PWM IN
14< PH3_SKIP# IN

PWM SKIP VDD DH BST LX DL GND PAD

IN VRCPU_HG3 15<
IN CPU_BST3 15<
IN VRCPU_PH3 15<
IN VRCPU_LG3 15<

C6619 1UF_6.3V_2

PVAXG

C6609 1000PF_50V_2
R6603 10_1%_2
R6604 100_1%_2 CATCH R

14< FBB OUT
R6605 9.53K_1%_2

14< GNDSB OUT

R6601 10_1%_2
C6608 1000PF_50V_2
R6602 100_1%_2 CATCH R

P5V_A

C6618 2.2UF_6.3V_2

VRCPU_HG2 VRCPU_LG2 VRCPU_LG1 VRCPU_HG1 VRCPU_PH1 PH3_PWM PH3_SKIP# CCVA IMONA GNDSA FBA
CPU_BST2 CPU_BST1

P3V3_S

R6611 2K_5%_2
R6610 2K_5%_2

15< VRCPU_PH2 IN

DH2 BST2 DLA2 VDDA DLA1 BST1 DHA1 LXA1 PWM_OUT DRSKIP CCVA IMONA GNDSA FBA

LXA2 VRA_READY VRB_READY CSPA1 CSNA1 CSNA2 CSPA2 CSPA3 CSNA3 IMAXA IMAXB TMAX VR_HOT# AGND

VBOOTB VBOOTA CCI2 CCI1 SRA SRB THERMA THERMB N.C. FBB GNDSB IMONB CCVB LXB GND

IN VBOOTB 14<
IN VBOOTA
IN SRA 14<
IN SRB 14<
IN THERMA 14<
IN THERMB 14<
IN FBB 14>
IN GNDSB 14>
IN IMONB 14<
IN CCVB 14<
IN VRAXG_PH1 15<

C6610 470PF_50V_2
IN VCCSENSE 23> 14<
C6611 470PF_50V_2
TP6600

P5V_A

14< IMAXA IN
14< IMAXB IN

R6623 10K_5%_2
R6038 0_5%_2

U6600
MAX_MAX17039GTN+_TQFN_56P

ALERT# VDIO VCLK VCC TONA TONB CSPB CSNB VR_ENABLE DLG VDDB DLB BSTB DHB

TONA 14<
TONB 14<

VRAXG_LG1 15<
GPU_BST1 15<
VRAXG_HG1 15<

TP6601

P5V_A P5V_A

C6616 2.2UF_6.3V_2
C6617 2.2UF_6.3V_2

FOLLOW BERLIN 10RG

+VBAT_CPU P3V3_A P5V_A

R6617 178K_1%_2
R6608 0_5%_2
R6625 4.87K_1%_2

IN TONB 14<
IN IMAXB 14<
IN IMONB 14<
IN CCVB 14<
IN VBOOTB 14<
IN SRB 14<
IN THERMB 14<

R6609 20.5K_1%_2
C6612 470PF_50V_2
R6607 0_5%_2
R6606 115K_1%_2
R6627 100K_5%_2

IN VSSAXG_SENSE 24> 14<

C6614 1000PF_50V_2
R6616 5.1K_1%_2
R6614 10_1%_2

14< FBA IN
14< GNDSA IN

R6612 10_1%_2
C6613 1000PF_50V_2

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INVENTEC

TITLE: EVEREST-M POWER VCORE

SIZE	CODE	DOC.NUMBER	REV
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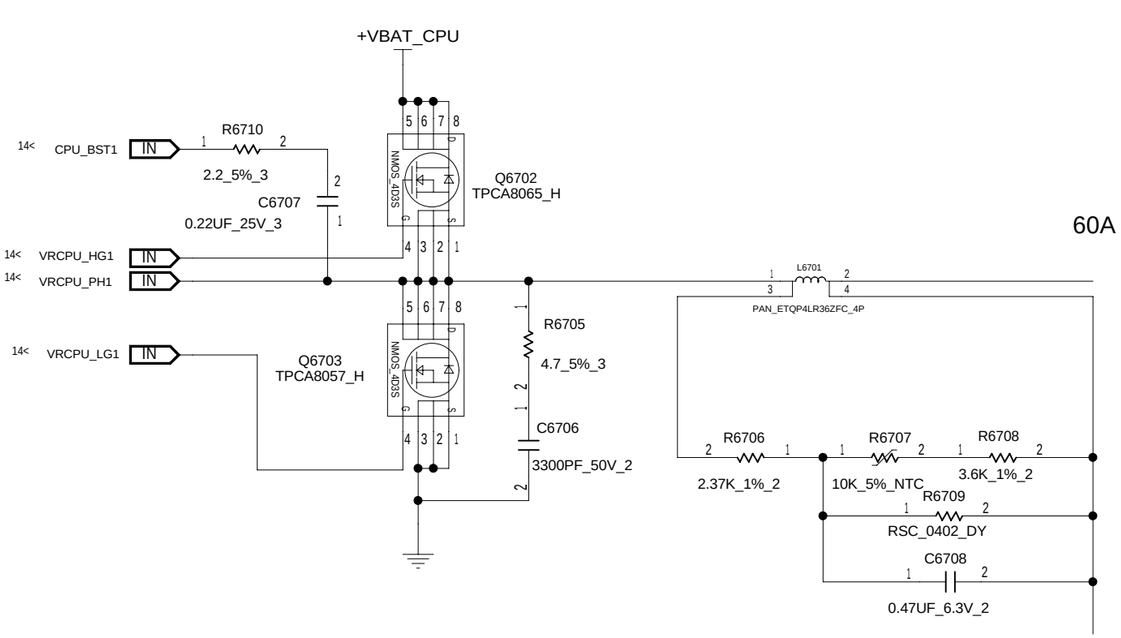
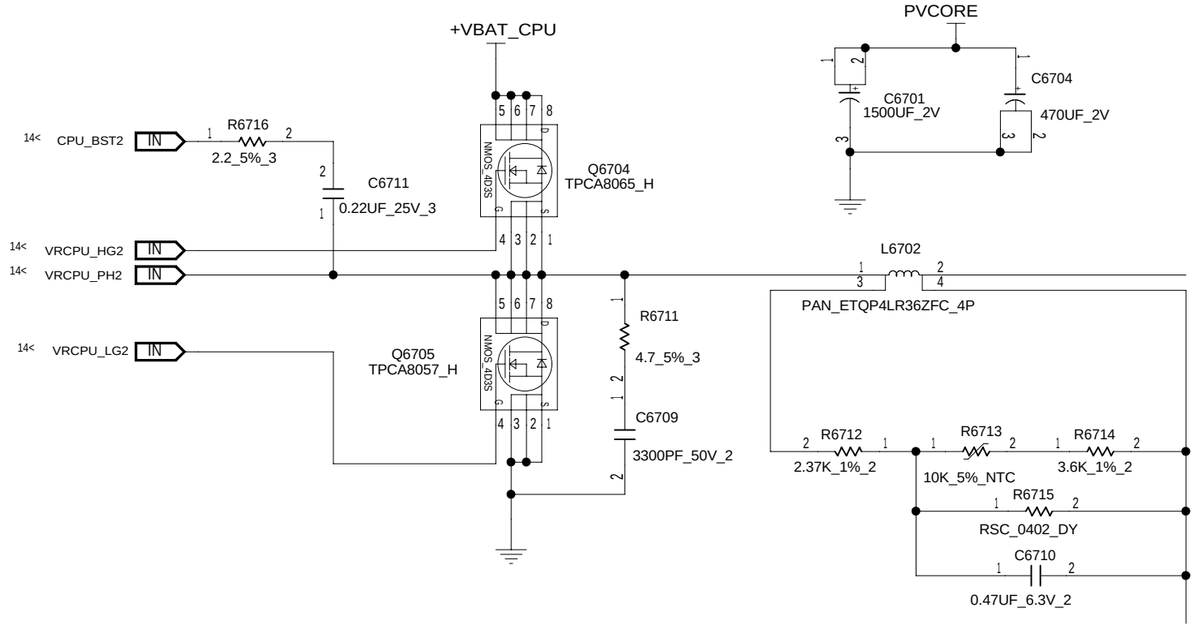
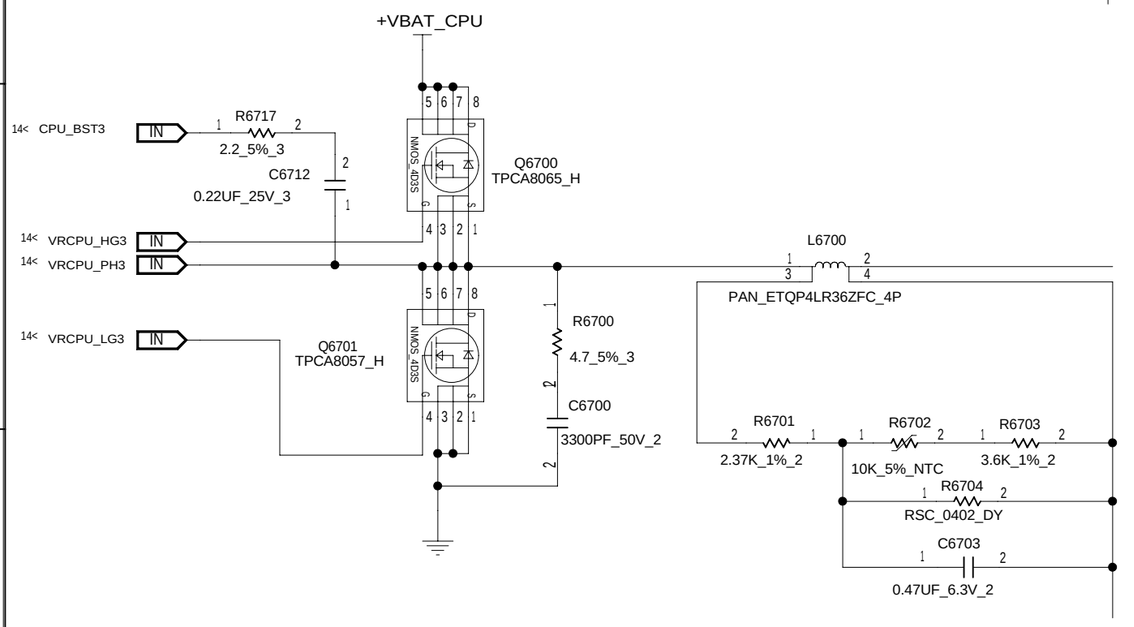
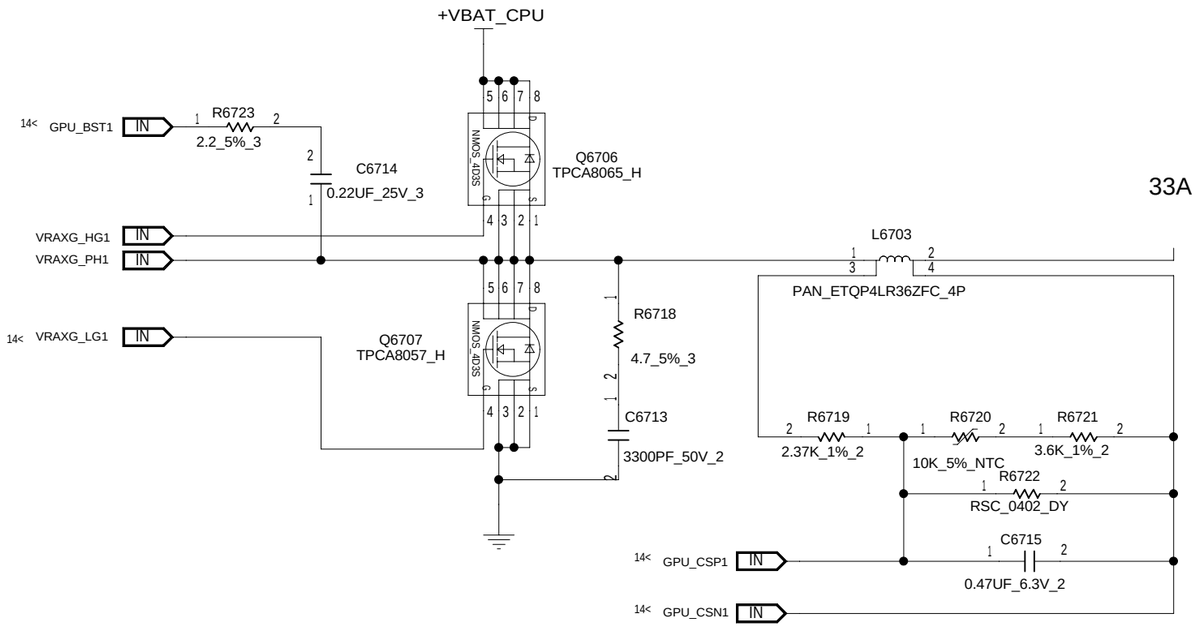


60A





33A



INVENTEC

TITLE	EVEREST-M POWER VCORE		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
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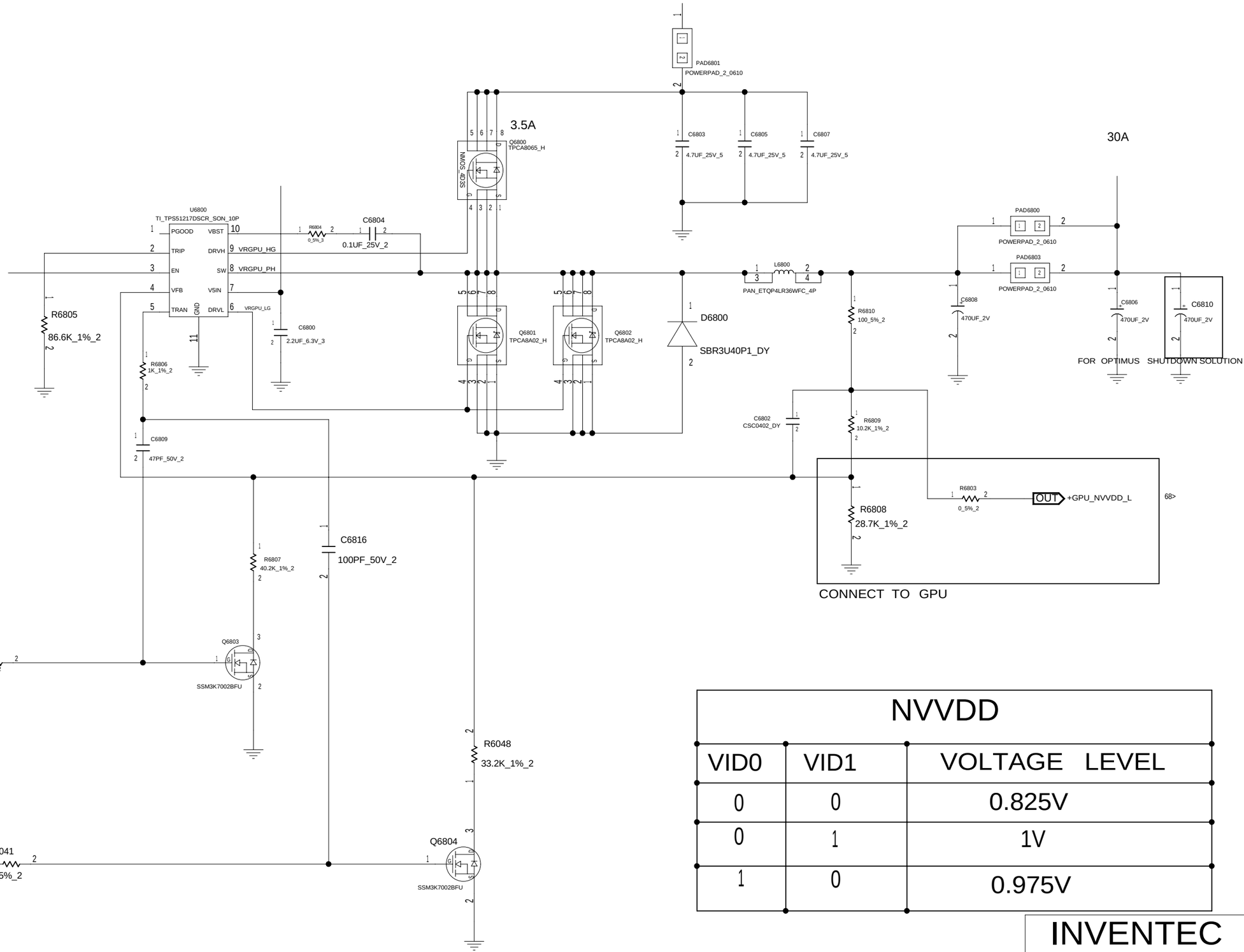

NVVDD

VID0	VID1	VOLTAGE LEVEL
0	0	0.825V
0	1	1V
1	0	0.975V

INVENTEC

TITLE: EVEREST-M
POWER GPU NVVDD

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

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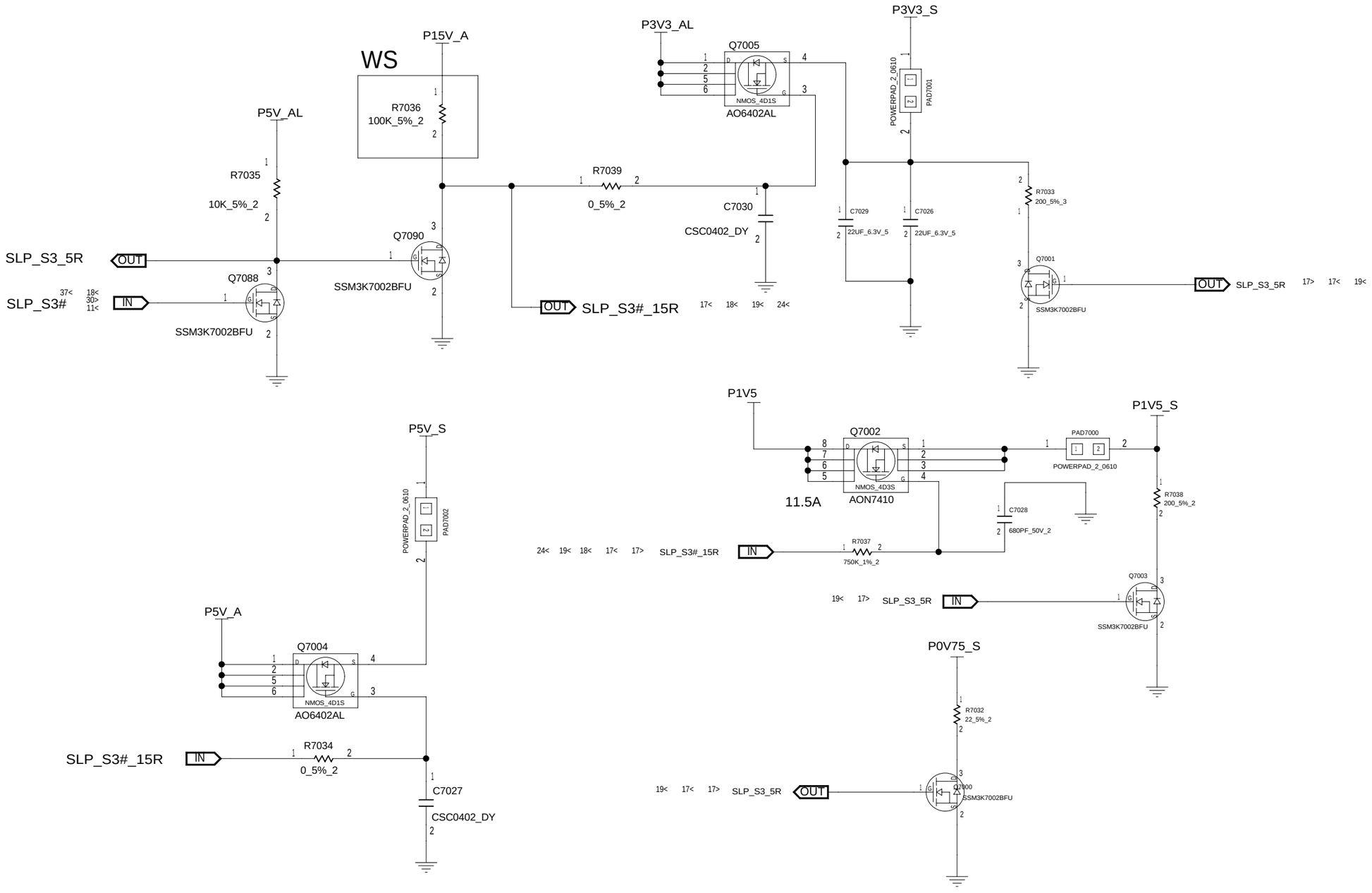

INVENTEC

TITLE	EVEREST-M POWER +V3S/+V5S/+V1.5S		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
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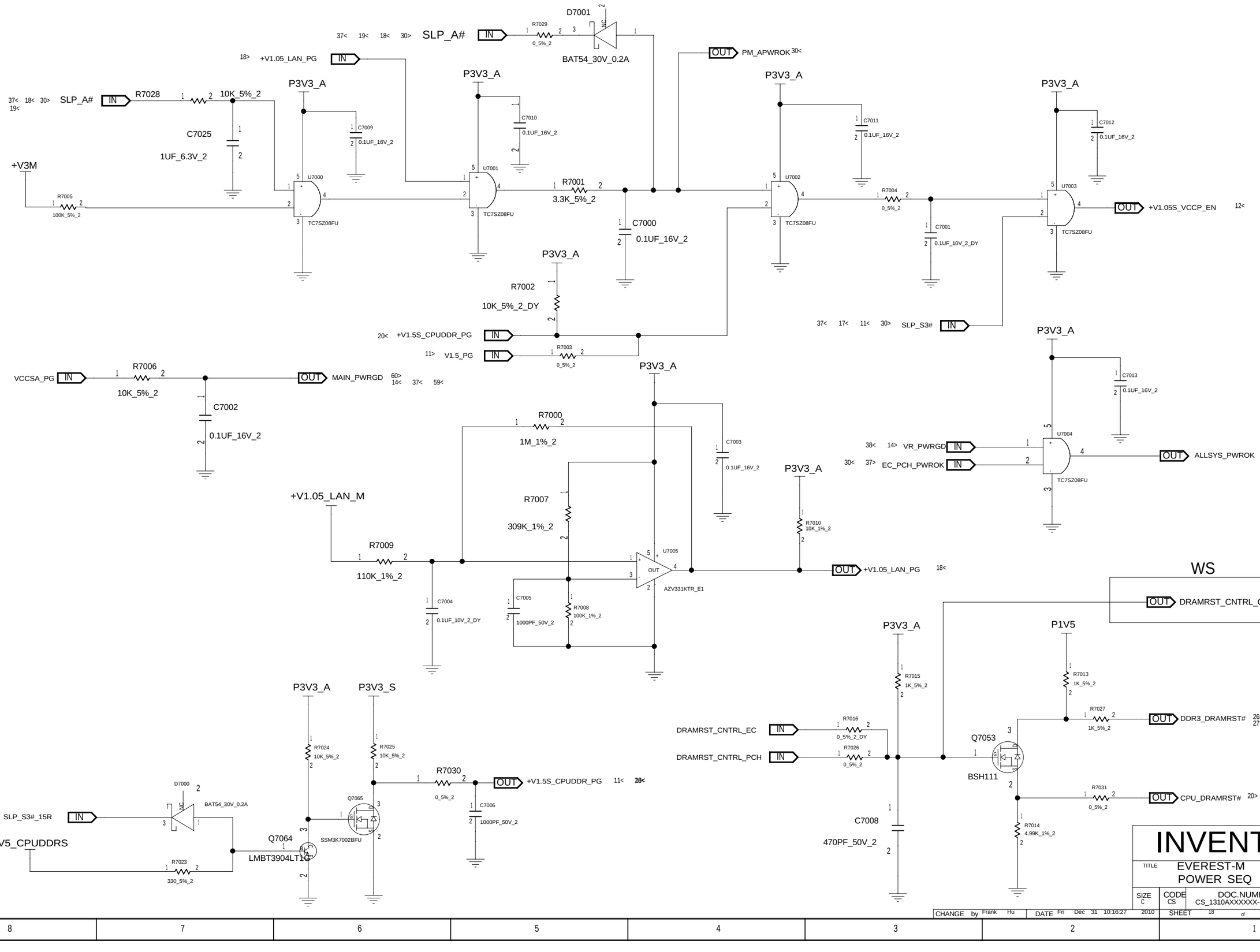
D7001
37< 19< 18< 30> SLP_A#
IN
R7029
0_5%_2
BAT54_30V_0.2A
OUT PM_APWROK 30<
18> +V1.05_LAN_PG
IN
P3V3_A
37< 18< 30> 19< SLP_A#
IN
R7028
10K_5%_2
C7025
1UF_6.3V_2
C7009
0.1UF_16V_2
+V3M
R7005
100K_5%_2
U7000
TC7SZ08FU
C7010
0.1UF_16V_2
U7001
R7001
3.3K_5%_2
C7000
0.1UF_16V_2
C7011
0.1UF_16V_2
U7002
R7004
0_5%_2
C7001
0.1UF_10V_2_DY
C7012
0.1UF_16V_2
U7003
OUT +V1.05S_VCCP_EN 12<
37< 17< 11< 30> SLP_S3#
IN
R7002
10K_5%_2_DY
20< +V1.5S_CPUDDR_PG
11> V1.5_PG
R7003
0_5%_2
VCCSA_PG
IN
R7006
10K_5%_2
OUT MAIN_PWRGD 60> 14< 37< 59<
C7002
0.1UF_16V_2
R7000
1M_1%_2
C7003
0.1UF_16V_2
+V1.05_LAN_M
R7009
110K_1%_2
R7007
309K_1%_2
C7004
0.1UF_10V_2_DY
C7005
1000PF_50V_2
R7008
100K_1%_2
U7005
AZV331KTR_E1
R7010
10K_1%_2
OUT +V1.05_LAN_PG 18<
C7013
0.1UF_16V_2
U7004
38< 14> VR_PWRGD
IN
30< 37> EC_PCH_PWROK
IN
OUT ALLSYS_PWROK
TC7SZ08FU
WS
OUT DRAMRST_CNTRL_CPU
P3V3_S
D7000
BAT54_30V_0.2A
19< 17< 17< 24< SLP_S3#_15R
IN
P1V5_CPUDDRS
Q7064
LMBT3904LT1G
R7023
330_5%_2
R7024
10K_5%_2
R7025
10K_5%_2
Q7065
SSM3K7002BFU
R7030
0_5%_2
OUT +V1.5S_CPUDDR_PG 11< 20<
C7006
1000PF_50V_2
P1V5
R7015
1K_5%_2
DRAMRST_CNTRL_EC
IN
DRAMRST_CNTRL_PCH
IN
R7016
0_5%_2_DY
R7026
0_5%_2
Q7053
BSH111
C7008
470PF_50V_2
R7013
1K_5%_2
R7027
1K_5%_2
OUT DDR3_DRAMRST# 26> 27>
R7031
0_5%_2
OUT CPU_DRAMRST# 20>
R7014
4.99K_1%_2
INVENTEC
TITLE EVEREST-M
POWER SEQ
SIZE C
CODE CS
DOC.NUMBER CS_1310AXXXXXX-MTR
REV A01
CHANGE by Frank Hu
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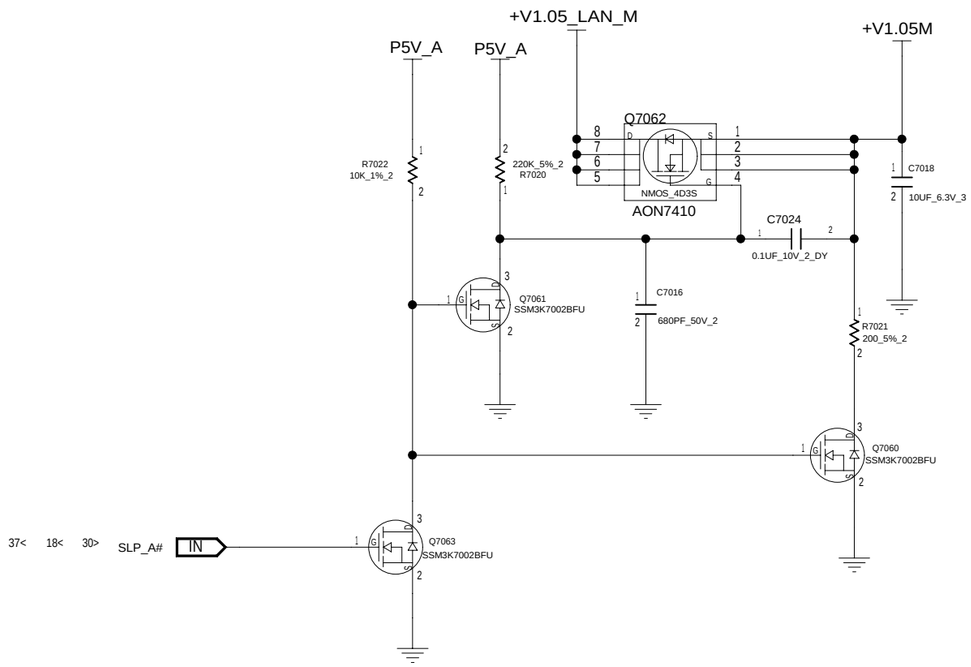

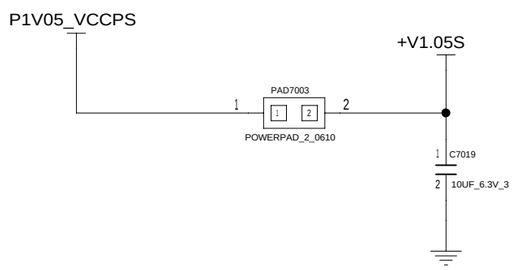

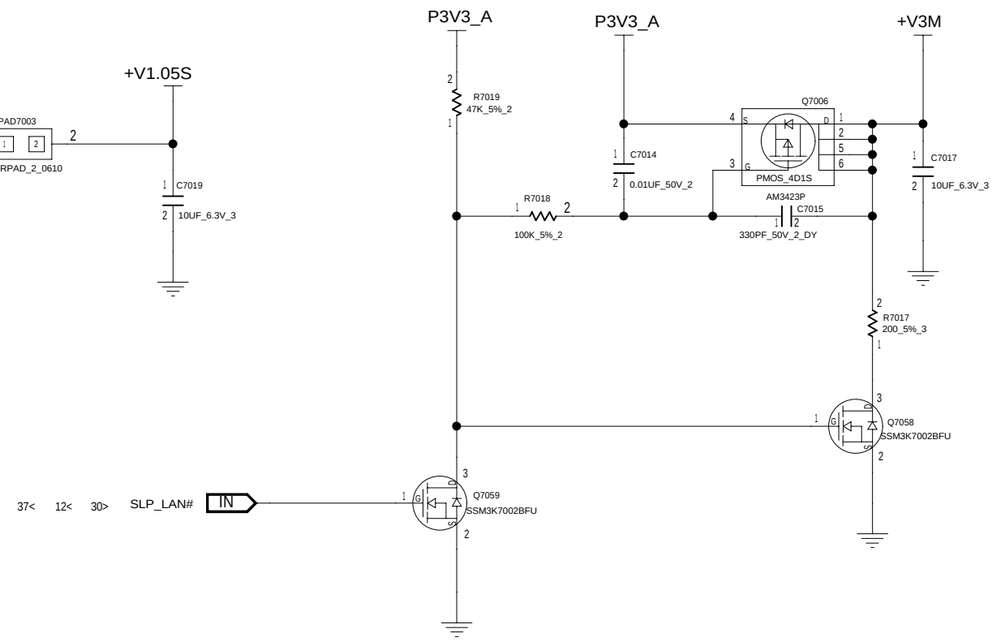

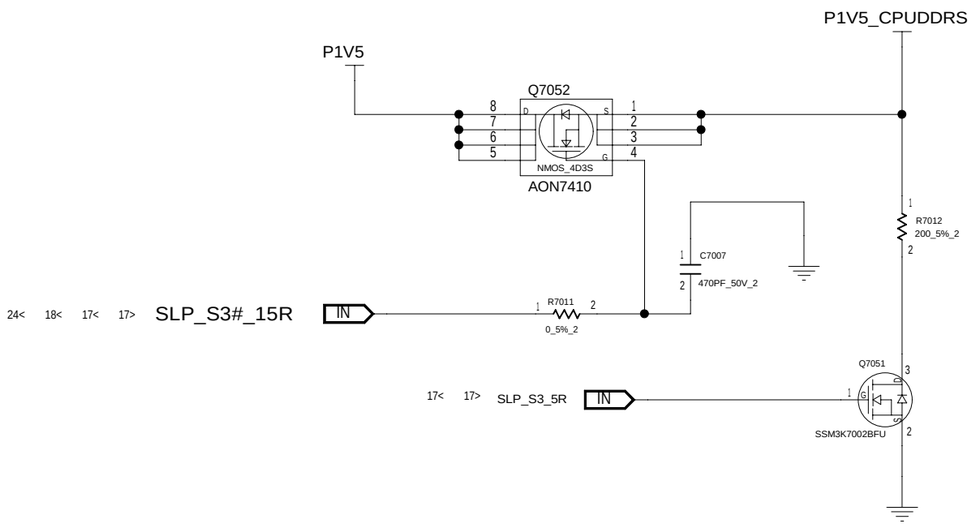

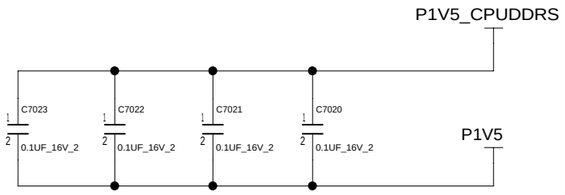

INVENTEC

TITLE: EVEREST-M
POWER SEQ

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

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REMOVE CLKOUT_DMI_CLKGEN_DP
CLKOUT_DMI_CLKGEN_DN

WS

CN4500

MISC

THERMAL

PWR MANAGEMENT

CLOCKS

MISC DDR3

JTAG & BPM

P1V8_S
R4537 2.2K_5%_2
Place close to CPT and NVRAM connector
20> H_SNB_IVB# OUT
R4538 4.7K_5%_2
OUT NV_CLE 32>

DMI&FDI TerminationVoltage
NV_CLE
Set toVss when LOW (Default)
Set toVcc when HIGH

P1V05_VCCPS
R4510 62_5%_2
14> H_PROCHOT# OUT
C4504 47PF_50V_2

20> H_SNB_IVB# OUT C26 PROC_SELECT#
TP4500 AN34 SKTOCC#
R4517 0_5%_2_DY H_CATERR#_R AL33 CATERR#
37<> 33> H_PECI OUT R4516 43_5%_2 H_PECI_R AN33 PECI
R4536 56_5%_2 H_PROCHOT#_R AL32 PROCHOT#
33< PM_THRMTRIP# OUT R4535 0_5%_2 PM_THRMTRIP#_R AN32 THERMTRIP#

P3V3_A
R4512 100K_5%_2_DY
R4511 200_5%_2
U4502 NXP_74AHC1G09GV_SOT753_5P
P3V3_A
C4570 0.1UF_16V_2

P1V5_CPUDDRS
R4532 200_5%_2
R4513 39_5%_2
Q4500 SSM3K7002BFU
SLP_S3_5R IN

LOW_IN C6/C7
30<> H_PM_SYNC BI R4534 0_5%_2 H_PM_SYNC_R AM34 PM_SYNC
60> 33> H_CPUPWRGD IN R4533 0_5%_2 H_CPUPWRGD_R AP33 UNCOREPWRGOOD
18> 30> PM_DRAM_PWRGD IN
18< +V1.5S_CPUDDR_PG IN
R4500 130_1%_2 PM_DRAM_PWRGD_R V8 SM_DRAMPWROK
20> BUF_PLT_RST#_CPU IN AR33 RESET#

FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER

CLKOUT_DMI_PCH_R_DP
BCLK A28 R4542 0_5%_2 IN CLK_DMI_PCH_DP 29>
BCLK# A27 R4541 0_5%_2 IN CLK_DMI_PCH_DN 29>
CLKOUT_DMI_PCH_R_DN

CLK_DP_PCH_CPU_R_DP
DPLL_REF_CLK A16 R4531 0_5%_2 IN CLK_DP_PCH_CPU_DP 29>
DPLL_REF_CLK# A15 R4530 0_5%_2 IN CLK_DP_PCH_CPU_DN 29>
CLK_DP_PCH_CPU_R_DN

SM_DRAMRST# R8 OUT CPU_DRAMRST# 18>

SM_RCOMP[0] AK1 SM_RCOMP0 R4507 140_1%_2
SM_RCOMP[1] A5 SM_RCOMP1 R4506 25.5_1%_2
SM_RCOMP[2] A4 SM_RCOMP2 R4505 200_1%_2

PRDY# AP29 OUT H_PRDY# 60<
PREQ# AP27 IN H_PREQ# 60> 20<
TCK AR26 IN H_TCK 60<> 60> 20<
TMS AR27 IN H_TMS 60<> 60> 20<
TRST# AP30 IN H_TRST# 60> 20<
TDI AR28 IN H_TDI 60> 20<
TDO AP26 OUT H_TDO 60<> 60<

DBR# AL35 SYS_RESET#_R R4529 0_5%_2 OUT SYS_RESET# 60> 30<

BPM#[0] AT28 OUT H_BPM0_XDP# 60<
BPM#[1] AR29 OUT H_BPM1_XDP# 60<
BPM#[2] AR30 OUT H_BPM2_XDP# 60<
BPM#[3] AT30 OUT H_BPM3_XDP# 60<
BPM#[4] AP32 OUT H_BPM4_XDP# 60<
BPM#[5] AR31 OUT H_BPM5_XDP# 60<
BPM#[6] AT31 OUT H_BPM6_XDP# 60<
BPM#[7] AR32 OUT H_BPM7_XDP# 60<

P3V3_S
C4559 0.1UF_16V_2
P1V05_VCCPS
R4558 75_5_%_2
U4501 TSB_TC7SZ07FU_SSOP_5P
56< 55< 32<> 43< BUF_PLT_RST# IN
R4509 43_5%_2 OUT BUF_PLT_RST#_CPU 20<
R4508 0_5%_2_DY

H_CPUPWRGD_R IN
R4557 10K_5%_2

P1V05_VCCPS
20< 60> 60<> H_TMS IN R4556 51_5%_2
20< 60> H_TDI IN R4555 51_5%_2
20< 60> H_PREQ# IN R4552 51_5%_2_DY
20< 60> 60<> H_TCK IN R4554 51_5%_2
20< 60> H_TRST# IN R4553 51_5%_2

INVENTEC

TITLE	EVEREST-M CPU 1		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
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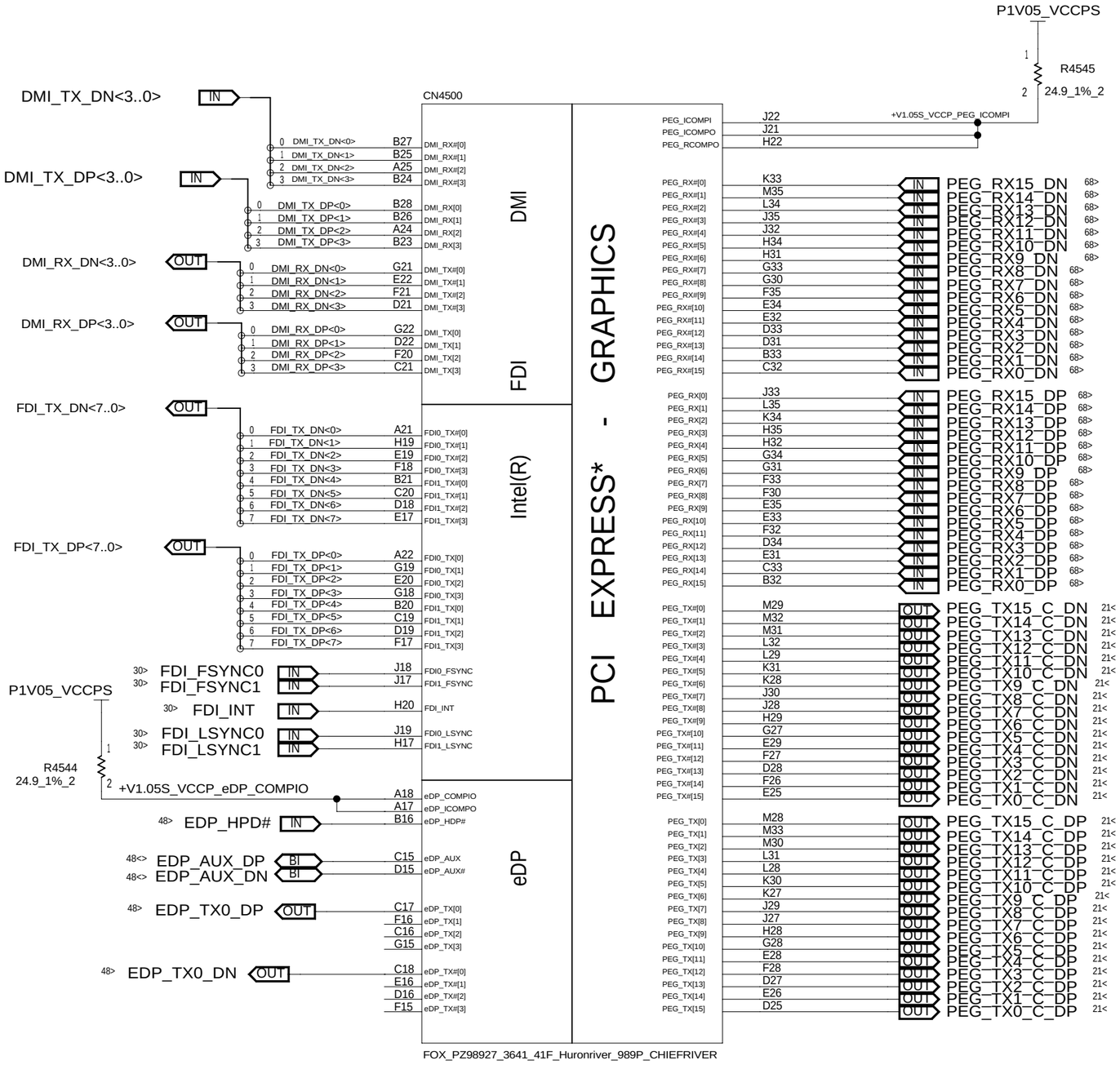

FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER

CLOSE to CPU

PEG_TX15_C_DN	C4546	0.1UF_6.3V_1	PEG_TX15_DN	68<
PEG_TX14_C_DN	C4545	0.1UF_6.3V_1	PEG_TX14_DN	68<
PEG_TX13_C_DN	C4544	0.1UF_6.3V_1	PEG_TX13_DN	68<
PEG_TX12_C_DN	C4543	0.1UF_6.3V_1	PEG_TX12_DN	68<
PEG_TX11_C_DN	C4542	0.1UF_6.3V_1	PEG_TX11_DN	68<
PEG_TX10_C_DN	C4541	0.1UF_6.3V_1	PEG_TX10_DN	68<
PEG_TX9_C_DN	C4540	0.1UF_6.3V_1	PEG_TX9_DN	68<
PEG_TX8_C_DN	C4539	0.1UF_6.3V_1	PEG_TX8_DN	68<
PEG_TX7_C_DN	C4538	0.1UF_6.3V_1	PEG_TX7_DN	68<
PEG_TX6_C_DN	C4537	0.1UF_6.3V_1	PEG_TX6_DN	68<
PEG_TX5_C_DN	C4536	0.1UF_6.3V_1	PEG_TX5_DN	68<
PEG_TX4_C_DN	C4535	0.1UF_6.3V_1	PEG_TX4_DN	68<
PEG_TX3_C_DN	C4534	0.1UF_6.3V_1	PEG_TX3_DN	68<
PEG_TX2_C_DN	C4533	0.1UF_6.3V_1	PEG_TX2_DN	68<
PEG_TX1_C_DN	C4532	0.1UF_6.3V_1	PEG_TX1_DN	68<
PEG_TX0_C_DN	C4531	0.1UF_6.3V_1	PEG_TX0_DN	68<

PEG_TX15_C_DP	C4530	0.1UF_6.3V_1	PEG_TX15_DP	68<
PEG_TX14_C_DP	C4529	0.1UF_6.3V_1	PEG_TX14_DP	68<
PEG_TX13_C_DP	C4528	0.1UF_6.3V_1	PEG_TX13_DP	68<
PEG_TX12_C_DP	C4527	0.1UF_6.3V_1	PEG_TX12_DP	68<
PEG_TX11_C_DP	C4526	0.1UF_6.3V_1	PEG_TX11_DP	68<
PEG_TX10_C_DP	C4525	0.1UF_6.3V_1	PEG_TX10_DP	68<
PEG_TX9_C_DP	C4524	0.1UF_6.3V_1	PEG_TX9_DP	68<
PEG_TX8_C_DP	C4523	0.1UF_6.3V_1	PEG_TX8_DP	68<
PEG_TX7_C_DP	C4522	0.1UF_6.3V_1	PEG_TX7_DP	68<
PEG_TX6_C_DP	C4521	0.1UF_6.3V_1	PEG_TX6_DP	68<
PEG_TX5_C_DP	C4520	0.1UF_6.3V_1	PEG_TX5_DP	68<
PEG_TX4_C_DP	C4519	0.1UF_6.3V_1	PEG_TX4_DP	68<
PEG_TX3_C_DP	C4518	0.1UF_6.3V_1	PEG_TX3_DP	68<
PEG_TX2_C_DP	C4517	0.1UF_6.3V_1	PEG_TX2_DP	68<
PEG_TX1_C_DP	C4516	0.1UF_6.3V_1	PEG_TX1_DP	68<
PEG_TX0_C_DP	C4515	0.1UF_6.3V_1	PEG_TX0_DP	68<

INVENTEC

TITLE	EVEREST-M CPU 2		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
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SOCKET,CPU,989P,TIN,3.0MM,STR,SMD,TR

CN4500

DDR SYSTEM MEMORY A

M_A_DQ<63..0> BI

0	M_A_DQ<0>	C5	SA_DQ[0]
1	M_A_DQ<1>	D5	SA_DQ[1]
2	M_A_DQ<2>	D3	SA_DQ[2]
3	M_A_DQ<3>	D2	SA_DQ[3]
4	M_A_DQ<4>	D6	SA_DQ[4]
5	M_A_DQ<5>	C6	SA_DQ[5]
6	M_A_DQ<6>	C2	SA_DQ[6]
7	M_A_DQ<7>	C3	SA_DQ[7]
8	M_A_DQ<8>	F10	SA_DQ[8]
9	M_A_DQ<9>	F8	SA_DQ[9]
10	M_A_DQ<10>	G10	SA_DQ[10]
11	M_A_DQ<11>	G9	SA_DQ[11]
12	M_A_DQ<12>	F9	SA_DQ[12]
13	M_A_DQ<13>	F7	SA_DQ[13]
14	M_A_DQ<14>	G8	SA_DQ[14]
15	M_A_DQ<15>	G7	SA_DQ[15]
16	M_A_DQ<16>	K4	SA_DQ[16]
17	M_A_DQ<17>	K5	SA_DQ[17]
18	M_A_DQ<18>	K1	SA_DQ[18]
19	M_A_DQ<19>	J1	SA_DQ[19]
20	M_A_DQ<20>	J5	SA_DQ[20]
21	M_A_DQ<21>	J4	SA_DQ[21]
22	M_A_DQ<22>	J2	SA_DQ[22]
23	M_A_DQ<23>	K2	SA_DQ[23]
24	M_A_DQ<24>	M8	SA_DQ[24]
25	M_A_DQ<25>	N10	SA_DQ[25]
26	M_A_DQ<26>	N8	SA_DQ[26]
27	M_A_DQ<27>	N7	SA_DQ[27]
28	M_A_DQ<28>	M10	SA_DQ[28]
29	M_A_DQ<29>	M9	SA_DQ[29]
30	M_A_DQ<30>	N9	SA_DQ[30]
31	M_A_DQ<31>	M7	SA_DQ[31]
32	M_A_DQ<32>	AG6	SA_DQ[32]
33	M_A_DQ<33>	AG5	SA_DQ[33]
34	M_A_DQ<34>	AK6	SA_DQ[34]
35	M_A_DQ<35>	AK5	SA_DQ[35]
36	M_A_DQ<36>	AH5	SA_DQ[36]
37	M_A_DQ<37>	AH6	SA_DQ[37]
38	M_A_DQ<38>	AJ5	SA_DQ[38]
39	M_A_DQ<39>	AJ6	SA_DQ[39]
40	M_A_DQ<40>	AJ8	SA_DQ[40]
41	M_A_DQ<41>	AK8	SA_DQ[41]
42	M_A_DQ<42>	AJ9	SA_DQ[42]
43	M_A_DQ<43>	AK9	SA_DQ[43]
44	M_A_DQ<44>	AH8	SA_DQ[44]
45	M_A_DQ<45>	AH9	SA_DQ[45]
46	M_A_DQ<46>	AL9	SA_DQ[46]
47	M_A_DQ<47>	AL8	SA_DQ[47]
48	M_A_DQ<48>	AP11	SA_DQ[48]
49	M_A_DQ<49>	AN11	SA_DQ[49]
50	M_A_DQ<50>	AL12	SA_DQ[50]
51	M_A_DQ<51>	AM12	SA_DQ[51]
52	M_A_DQ<52>	AM11	SA_DQ[52]
53	M_A_DQ<53>	AL11	SA_DQ[53]
54	M_A_DQ<54>	AP12	SA_DQ[54]
55	M_A_DQ<55>	AN12	SA_DQ[55]
56	M_A_DQ<56>	AJ14	SA_DQ[56]
57	M_A_DQ<57>	AH14	SA_DQ[57]
58	M_A_DQ<58>	AL15	SA_DQ[58]
59	M_A_DQ<59>	AK15	SA_DQ[59]
60	M_A_DQ<60>	AL14	SA_DQ[60]
61	M_A_DQ<61>	AK14	SA_DQ[61]
62	M_A_DQ<62>	AJ15	SA_DQ[62]
63	M_A_DQ<63>	AH15	SA_DQ[63]

SA_CLK[0]	AB6	OUT	M_CLK_DDR0_DP 26<
SA_CLK#[0]	AA6	OUT	M_CLK_DDR0_DN 26<
SA_CKE[0]	V9	OUT	M_CKE0 26<
SA_CLK[1]	AA5	OUT	M_CLK_DDR1_DP 26<
SA_CLK#[1]	AB5	OUT	M_CLK_DDR1_DN 26<
SA_CKE[1]	V10	OUT	M_CKE1 26<
RSVD_TP[1]	AB4		
RSVD_TP[2]	AA4		
RSVD_TP[3]	W9		
RSVD_TP[4]	AB3		
RSVD_TP[5]	AA3		
RSVD_TP[6]	W10		
SA_CS#[0]	AK3	OUT	M_CS#0 26<
SA_CS#[1]	AL3	OUT	M_CS#1 26<
RSVD_TP[7]	AG1		
RSVD_TP[8]	AH1		
SA_ODT[0]	AH3	OUT	M_ODT0 26<
SA_ODT[1]	AG3	OUT	M_ODT1 26<
RSVD_TP[9]	AG2		
RSVD_TP[10]	AH2		

M_A_DQS_DN<7..0> BI

SA_DQS#[0]	C4	M_A_DQS_DN<0>	0
SA_DQS#[1]	G6	M_A_DQS_DN<1>	1
SA_DQS#[2]	J3	M_A_DQS_DN<2>	2
SA_DQS#[3]	M6	M_A_DQS_DN<3>	3
SA_DQS#[4]	AL6	M_A_DQS_DN<4>	4
SA_DQS#[5]	AM8	M_A_DQS_DN<5>	5
SA_DQS#[6]	AR12	M_A_DQS_DN<6>	6
SA_DQS#[7]	AM15	M_A_DQS_DN<7>	7

M_A_DQS_DP<7..0> BI

SA_DQS[0]	D4	M_A_DQS_DP<0>	0
SA_DQS[1]	F6	M_A_DQS_DP<1>	1
SA_DQS[2]	K3	M_A_DQS_DP<2>	2
SA_DQS[3]	N6	M_A_DQS_DP<3>	3
SA_DQS[4]	AL5	M_A_DQS_DP<4>	4
SA_DQS[5]	AM9	M_A_DQS_DP<5>	5
SA_DQS[6]	AR11	M_A_DQS_DP<6>	6
SA_DQS[7]	AM14	M_A_DQS_DP<7>	7

M_A_A<15..0> OUT

SA_MA[0]	AD10	M_A_A<0>	0
SA_MA[1]	W1	M_A_A<1>	1
SA_MA[2]	W2	M_A_A<2>	2
SA_MA[3]	W7	M_A_A<3>	3
SA_MA[4]	V3	M_A_A<4>	4
SA_MA[5]	V2	M_A_A<5>	5
SA_MA[6]	W3	M_A_A<6>	6
SA_MA[7]	W6	M_A_A<7>	7
SA_MA[8]	V1	M_A_A<8>	8
SA_MA[9]	W5	M_A_A<9>	9
SA_MA[10]	AD8	M_A_A<10>	10
SA_MA[11]	V4	M_A_A<11>	11
SA_MA[12]	W4	M_A_A<12>	12
SA_MA[13]	AF8	M_A_A<13>	13
SA_MA[14]	V5	M_A_A<14>	14
SA_MA[15]	V7	M_A_A<15>	15

26<	M_A_BS0 OUT	AE10	SA_BS[0]
26<	M_A_BS1 OUT	AF10	SA_BS[1]
26<	M_A_BS2 OUT	V6	SA_BS[2]
26<	M_A_CAS# OUT	AE8	SA_CAS#
26<	M_A_RAS# OUT	AD9	SA_RAS#
26<	M_A_WE# OUT	AF9	SA_WE#

FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER

27<> M_B_DQ<63..0> BI

CN4500

DDR SYSTEM MEMORY B

0	M_B_DQ<0>	C9	SB_DQ[0]
1	M_B_DQ<1>	A7	SB_DQ[1]
2	M_B_DQ<2>	D10	SB_DQ[2]
3	M_B_DQ<3>	C8	SB_DQ[3]
4	M_B_DQ<4>	A9	SB_DQ[4]
5	M_B_DQ<5>	A8	SB_DQ[5]
6	M_B_DQ<6>	D9	SB_DQ[6]
7	M_B_DQ<7>	D8	SB_DQ[7]
8	M_B_DQ<8>	G4	SB_DQ[8]
9	M_B_DQ<9>	F4	SB_DQ[9]
10	M_B_DQ<10>	F1	SB_DQ[10]
11	M_B_DQ<11>	G1	SB_DQ[11]
12	M_B_DQ<12>	G5	SB_DQ[12]
13	M_B_DQ<13>	F5	SB_DQ[13]
14	M_B_DQ<14>	F2	SB_DQ[14]
15	M_B_DQ<15>	G2	SB_DQ[15]
16	M_B_DQ<16>	J7	SB_DQ[16]
17	M_B_DQ<17>	J8	SB_DQ[17]
18	M_B_DQ<18>	K10	SB_DQ[18]
19	M_B_DQ<19>	K9	SB_DQ[19]
20	M_B_DQ<20>	J9	SB_DQ[20]
21	M_B_DQ<21>	J10	SB_DQ[21]
22	M_B_DQ<22>	K8	SB_DQ[22]
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24	M_B_DQ<24>	M5	SB_DQ[24]
25	M_B_DQ<25>	N4	SB_DQ[25]
26	M_B_DQ<26>	N2	SB_DQ[26]
27	M_B_DQ<27>	N1	SB_DQ[27]
28	M_B_DQ<28>	M4	SB_DQ[28]
29	M_B_DQ<29>	N5	SB_DQ[29]
30	M_B_DQ<30>	M2	SB_DQ[30]
31	M_B_DQ<31>	M1	SB_DQ[31]
32	M_B_DQ<32>	AM5	SB_DQ[32]
33	M_B_DQ<33>	AM6	SB_DQ[33]
34	M_B_DQ<34>	AR3	SB_DQ[34]
35	M_B_DQ<35>	AP3	SB_DQ[35]
36	M_B_DQ<36>	AN3	SB_DQ[36]
37	M_B_DQ<37>	AN2	SB_DQ[37]
38	M_B_DQ<38>	AN1	SB_DQ[38]
39	M_B_DQ<39>	AP2	SB_DQ[39]
40	M_B_DQ<40>	AP5	SB_DQ[40]
41	M_B_DQ<41>	AN9	SB_DQ[41]
42	M_B_DQ<42>	AT5	SB_DQ[42]
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44	M_B_DQ<44>	AP6	SB_DQ[44]
45	M_B_DQ<45>	AN8	SB_DQ[45]
46	M_B_DQ<46>	AR6	SB_DQ[46]
47	M_B_DQ<47>	AR5	SB_DQ[47]
48	M_B_DQ<48>	AR9	SB_DQ[48]
49	M_B_DQ<49>	AJ11	SB_DQ[49]
50	M_B_DQ<50>	AT8	SB_DQ[50]
51	M_B_DQ<51>	AT9	SB_DQ[51]
52	M_B_DQ<52>	AH11	SB_DQ[52]
53	M_B_DQ<53>	AR8	SB_DQ[53]
54	M_B_DQ<54>	AJ12	SB_DQ[54]
55	M_B_DQ<55>	AH12	SB_DQ[55]
56	M_B_DQ<56>	AT11	SB_DQ[56]
57	M_B_DQ<57>	AN14	SB_DQ[57]
58	M_B_DQ<58>	AR14	SB_DQ[58]
59	M_B_DQ<59>	AT14	SB_DQ[59]
60	M_B_DQ<60>	AT12	SB_DQ[60]
61	M_B_DQ<61>	AN15	SB_DQ[61]
62	M_B_DQ<62>	AR15	SB_DQ[62]
63	M_B_DQ<63>	AT15	SB_DQ[63]

SB_CLK[0]	AE2	OUT	M_CLK_DDR2_DP 27<
SB_CLK#[0]	AD2	OUT	M_CLK_DDR2_DN 27<
SB_CKE[0]	R9	OUT	M_CKE2 27<
SB_CLK[1]	AE1	OUT	M_CLK_DDR3_DP 27<
SB_CLK#[1]	AD1	OUT	M_CLK_DDR3_DN 27<
SB_CKE[1]	R10	OUT	M_CKE3 27<
RSVD_TP[11]	AB2		
RSVD_TP[12]	AA2		
RSVD_TP[13]	T9		
RSVD_TP[14]	AA1		
RSVD_TP[15]	AB1		
RSVD_TP[16]	T10		
SB_CS#[0]	AD3	OUT	M_CS#2 27<
SB_CS#[1]	AE3	OUT	M_CS#3 27<
RSVD_TP[17]	AD6		
RSVD_TP[18]	AE6		
SB_ODT[0]	AE4	OUT	M_ODT2 27<
SB_ODT[1]	AD4	OUT	M_ODT3 27<
RSVD_TP[19]	AD5		
RSVD_TP[20]	AE5		

M_B_DQS_DN<7..0> BI

SB_DQS#[0]	D7	M_B_DQS_DN<0>	0
SB_DQS#[1]	F3	M_B_DQS_DN<1>	1
SB_DQS#[2]	K6	M_B_DQS_DN<2>	2
SB_DQS#[3]	N3	M_B_DQS_DN<3>	3
SB_DQS#[4]	AN5	M_B_DQS_DN<4>	4
SB_DQS#[5]	AP9	M_B_DQS_DN<5>	5
SB_DQS#[6]	AK12	M_B_DQS_DN<6>	6
SB_DQS#[7]	AP15	M_B_DQS_DN<7>	7

M_B_DQS_DP<7..0> BI

SB_DQS[0]	C7	M_B_DQS_DP<0>	0
SB_DQS[1]	G3	M_B_DQS_DP<1>	1
SB_DQS[2]	J6	M_B_DQS_DP<2>	2
SB_DQS[3]	M3	M_B_DQS_DP<3>	3
SB_DQS[4]	AN6	M_B_DQS_DP<4>	4
SB_DQS[5]	AP8	M_B_DQS_DP<5>	5
SB_DQS[6]	AK11	M_B_DQS_DP<6>	6
SB_DQS[7]	AP14	M_B_DQS_DP<7>	7

M_B_A<15..0> OUT 27<>

SB_MA[0]	AA8	M_B_A<0>	0
SB_MA[1]	T7	M_B_A<1>	1
SB_MA[2]	R7	M_B_A<2>	2
SB_MA[3]	T6	M_B_A<3>	3
SB_MA[4]	T2	M_B_A<4>	4
SB_MA[5]	T4	M_B_A<5>	5
SB_MA[6]	T3	M_B_A<6>	6
SB_MA[7]	R2	M_B_A<7>	7
SB_MA[8]	T5	M_B_A<8>	8
SB_MA[9]	R3	M_B_A<9>	9
SB_MA[10]	AB7	M_B_A<10>	10
SB_MA[11]	R1	M_B_A<11>	11
SB_MA[12]	T1	M_B_A<12>	12
SB_MA[13]	AB10	M_B_A<13>	13
SB_MA[14]	R5	M_B_A<14>	14
SB_MA[15]	R4	M_B_A<15>	15

27<	M_B_BS0 OUT	AA9	SB_BS[0]
27<	M_B_BS1 OUT	AA7	SB_BS[1]
27<	M_B_BS2 OUT	R6	SB_BS[2]
27<	M_B_CAS# OUT	AA10	SB_CAS#
27<	M_B_RAS# OUT	AB8	SB_RAS#
27<	M_B_WE# OUT	AB9	SB_WE#

FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER

INVENTEC

TITLE EVEREST-M
CPU 3 DRAM

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

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POWER

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

CN4500

PVCORE

C4580 10uF_6.3V_3 — C4579 10uF_6.3V_3

C4584 10uF_6.3V_3 — C4583 10uF_6.3V_3 — C4582 10uF_6.3V_3 — C4581 10uF_6.3V_3

C4586 10uF_6.3V_3 — C4587 10uF_6.3V_3 — C4594 10uF_6.3V_3 — C4585 10uF_6.3V_3

C4578 22uF_6.3V_5 — C4577 22uF_6.3V_5 — C4593 22uF_6.3V_5 — C4592 22uF_6.3V_5

C4591 22uF_6.3V_5 — C4590 22uF_6.3V_5 — C4589 22uF_6.3V_5 — C4588 22uF_6.3V_5

C4574 22uF_6.3V_5 — C4573 22uF_6.3V_5 — C4572 22uF_6.3V_5 — C4571 22uF_6.3V_5

C4564 22uF_6.3V_5 — C4565 22uF_6.3V_5 — C4576 22uF_6.3V_5 — C4575 22uF_6.3V_5

CN4500		CN4500		CN4500	
AG35	VCC1	AD35	VCC21	AC35	VCC31
AG34	VCC2	AD34	VCC22	AC34	VCC32
AG33	VCC3	AD33	VCC23	AC33	VCC33
AG32	VCC4	AD32	VCC24	AC32	VCC34
AG31	VCC5	AD31	VCC25	AC31	VCC35
AG30	VCC6	AD30	VCC26	AC30	VCC36
AG29	VCC7	AD29	VCC27	AC29	VCC37
AG28	VCC8	AD28	VCC28	AC28	VCC38
AG27	VCC9	AD27	VCC29	AC27	VCC39
AG26	VCC10	AD26	VCC30	AC26	VCC40
AF35	VCC11	AC35	VCC31	AA35	VCC41
AF34	VCC12	AC34	VCC32	AA34	VCC42
AF33	VCC13	AC33	VCC33	AA33	VCC43
AF32	VCC14	AC32	VCC34	AA32	VCC44
AF31	VCC15	AC31	VCC35	AA31	VCC45
AF30	VCC16	AC30	VCC36	AA30	VCC46
AF29	VCC17	AC29	VCC37	AA29	VCC47
AF28	VCC18	AC28	VCC38	AA28	VCC48
AF27	VCC19	AC27	VCC39	AA27	VCC49
AF26	VCC20	AC26	VCC40	AA26	VCC50

CN4500		CN4500		CN4500	
Y35	VCC51	V35	VCC61	R35	VCC81
Y34	VCC52	V34	VCC62	R34	VCC82
Y33	VCC53	V33	VCC63	R32	VCC84
Y32	VCC54	V32	VCC64	R31	VCC85
Y31	VCC55	V31	VCC65	R30	VCC86
Y30	VCC56	V30	VCC66	R29	VCC87
Y29	VCC57	V29	VCC67	R28	VCC88
Y28	VCC58	V28	VCC68	R27	VCC89
Y27	VCC59	V27	VCC69	R26	VCC90
Y26	VCC60	V26	VCC70	P35	VCC91
V35	VCC61	U35	VCC71	P34	VCC92
V34	VCC62	U34	VCC72	P33	VCC93
V33	VCC63	U33	VCC73	P32	VCC94
V32	VCC64	U32	VCC74	P31	VCC95
V31	VCC65	U31	VCC75	P30	VCC96
V30	VCC66	U30	VCC76	P29	VCC97
V29	VCC67	U29	VCC77	P28	VCC98
V28	VCC68	U28	VCC78	P27	VCC99
V27	VCC69	U27	VCC79	P26	VCC100
V26	VCC70	U26	VCC80		

FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER

P1V05_VCCPS

C4569 470UF_2V — C4599 22uF_6.3V_5 — C4596 22uF_6.3V_5 — C4598 22uF_6.3V_5 — C4597 22uF_6.3V_5 — C4557 22uF_6.3V_5 — C4503 22uF_6.3V_5 — C4558 22uF_6.3V_5

C4563 22uF_6.3V_5 — C4560 22uF_6.3V_5 — C4562 22uF_6.3V_5 — C4561 22uF_6.3V_5 — C4566 22uF_6.3V_5

VCCIO		VCCIO		VCCIO	
VCCIO1	AH13	VCCIO14	H11	VCCIO27	D14
VCCIO2	AH10	VCCIO15	G14	VCCIO28	D13
VCCIO3	AG10	VCCIO16	G13	VCCIO29	D12
VCCIO4	AC10	VCCIO17	G12	VCCIO30	D11
VCCIO5	Y10	VCCIO18	F14	VCCIO31	C14
VCCIO6	U10	VCCIO19	F13	VCCIO32	C13
VCCIO7	P10	VCCIO20	F12	VCCIO33	C12
VCCIO8	L10	VCCIO21	F11	VCCIO34	C11
VCCIO9	J14	VCCIO22	E14	VCCIO35	B14
VCCIO10	J13	VCCIO23	E12	VCCIO36	B12
VCCIO11	J12	VCCIO24		VCCIO37	A14
VCCIO12	J11	VCCIO25	E11	VCCIO38	A13
VCCIO13	H14	VCCIO26	D14	VCCIO39	A12
				VCCIO40	A11

VCCIO40 J23 — +V1.05S_VCCP_VCCIO40 — R4528 0_5%_2

20mil

P1V05_VCCPS

CLOSE TO POWER IC

R4525 130_1%_2 — R4548 54.9_1%_2 — R4547 75_1%_2 — R4546 130_1%_2

VIDALERT#	AJ29	H_CPU_SVIDALRT#	R4551	43_1%_2	OUT VR_SVID_ALRT# 14<
VIDSCLK	AJ30	H_CPU_SVIDCLK	R4549	0_5%_2	OUT VR_SVID_CLK 14<
VIDSOUT	AJ28	H_CPU_SVIDDAT	R4550	0_5%_2	OUT VR_SVID_DATA 14<>

PVCORE

R4504 100_1%_2

R4527 0_5%_2 — OUT VCCSENSE 14<

R4526 0_5%_2 — OUT VSSSENSE 14<

R4503 100_1%_2

P1V05_VCCPS

WS

VCC_SENSE	AJ35	VCCSENSE_R	R4502 10_1%_2	OUT VCC_SENSE_VTT
VSS_SENSE	AJ34	VSSSENSE_R	R4501 10_1%_2	OUT VSS_SENSE_VTT
VCCIO_SENSE	B10			
VSS_SENSE_VCCIO	A10			

INVENTEC

TITLE EVEREST-M
CPU 4 POWER

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

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WS

Function	xxVccSA_Select[1] [[CPU PIN# C24 VID0 of VR]]	xxVccSA_Select[0] [[CPU PIN# C22 VID1 of VR]]	VCCSA VR Vout
SNB HIGH	0	0	0.90V
IVB HIGH	0	1	0.725V
SNB LOW	1	0	0.80V
IVB LOW	1	1	0.675V

P0V75_VREF_M

20/20 mil

Q4501 NMOS_4D1S AO6402AL

20/20 mil

P0V75_VREF_M_H

C4595 470pF_50V_2

R4523 100K_5%_2

SLP_S3#_15R IN

R4524 0_5%_2

PVAXG

C4509 C4510 C4511 C4512 C4513 C4514 22uF_6.3V_5

C4600 C4601 C4602 C4603 C4507 C4508 22uF_6.3V_5

C4604 22uF_6.3V_5_DY C4605 22uF_6.3V_5_DY

WS

C4506 470UF_2V C4505 470UF_2V

CN4500

POWER

AT24	VAXG1	LINES	SENSE
AT23	VAXG2		
AT21	VAXG3		
AT20	VAXG4		
AT18	VAXG5		
AT17	VAXG6		
AR24	VAXG7		
AR23	VAXG8		
AR21	VAXG9		
AR20	VAXG10		
AR18	VAXG11		
AR17	VAXG12		
AP24	VAXG13		
AP23	VAXG14		
AP21	VAXG15		
AP20	VAXG16		
AP18	VAXG17		
AP17	VAXG18		
AN24	VAXG19		
AN23	VAXG20		
AN21	VAXG21		
AN20	VAXG22		
AN18	VAXG23		
AN17	VAXG24		
AM24	VAXG25		
AM23	VAXG26		
AM21	VAXG27		
AM20	VAXG28		
AM18	VAXG29		
AM17	VAXG30		
AL24	VAXG31		
AL23	VAXG32		
AL21	VAXG33		
AL20	VAXG34		
AL18	VAXG35		
AL17	VAXG36		
AK24	VAXG37		
AK23	VAXG38		
AK21	VAXG39		
AK20	VAXG40		
AK18	VAXG41		
AK17	VAXG42		
AJ24	VAXG43		
AJ23	VAXG44		
AJ21	VAXG45		
AJ20	VAXG46		
AJ18	VAXG47		
AJ17	VAXG48		
AH24	VAXG49		
AH23	VAXG50		
AH21	VAXG51		
AH20	VAXG52		
AH18	VAXG53		
AH17	VAXG54		

GRAPHICS RAILS DDR3 -1.5V

SA RAIL

1.8V RAIL

MISC

VAXG_SENSE AK35 OUT VAXG_SENSE 14<

VSSAXG_SENSE AK34 OUT VSSAXG_SENSE 14<

20/20 mil

P0V75_VREF_M_H CPU_CHA_VREFDQ CPU_CHB_VREFDQ

SM_VREF AL1

SA_DIMM_VREFDQ B4

SB_DIMM_VREFDQ D1

WS

P1V5_CPUDDRS

6A

VDDQ1 AF7, VDDQ2 AF4, VDDQ3 AF1, VDDQ4 AC7, VDDQ5 AC4, VDDQ6 AC1, VDDQ7 Y7, VDDQ8 Y4, VDDQ9 Y1, VDDQ10 U7, VDDQ11 U4, VDDQ12 U1, VDDQ13 P7, VDDQ14 P4, VDDQ15 P1

C4554 C4556 C4555 C4553 C4552 C4551 10uF_6.3V_3

C4568 220UF_2.5V

P0V85_S

VCCSA1 M27, VCCSA2 M26, VCCSA3 L26, VCCSA4 J26, VCCSA5 J25, VCCSA6 J24, VCCSA7 H26, VCCSA8 H25

C4502 C4501 C4500 10uF_6.3V_3

C4567 220UF_2.5V

P1V8_S

L4500 FBM_11_160808_181A15T

1.1A

VCCPLL B6 VCCPLL1, A6 VCCPLL2, A2 VCCPLL3

C4547 22uF_6.3V_5 C4549 1uF_6.3V_2 C4548 1uF_6.3V_2 C4550 10uF_6.3V_3

VCCSA_SENSE H23 OUT VCCSA_SENSE WS

VCCSA_VID[0] C22

VCCSA_VID[1] C24 OUT VCCSA_SEL 13<

VCCIO_SEL A19

R4543 10K_5%_2

R4559 0_5%_2_DY WS

FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER

INVENTEC

TITLE EVEREST-M
CPU 5 POWER

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

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CN4500

VSS

AT35	VSS1	VSS81	AJ22
AT32	VSS2	VSS82	AJ19
AT29	VSS3	VSS83	AJ16
AT27	VSS4	VSS84	AJ13
AT25	VSS5	VSS85	AJ10
AT22	VSS6	VSS86	AJ7
AT19	VSS7	VSS87	AJ4
AT16	VSS8	VSS88	AJ3
AT13	VSS9	VSS89	AJ2
AT10	VSS10	VSS90	AJ1
AT7	VSS11	VSS91	AH35
AT4	VSS12	VSS92	AH34
AT3	VSS13	VSS93	AH32
AR25	VSS14	VSS94	AH30
AR22	VSS15	VSS95	AH29
AR19	VSS16	VSS96	AH28
AR16	VSS17		
AR13	VSS18	VSS98	AH25
AR10	VSS19	VSS99	AH22
AR7	VSS20	VSS100	AH19
AR4	VSS21	VSS101	AH16
AR2	VSS22	VSS102	AH7
AP34	VSS23	VSS103	AH4
AP31	VSS24	VSS104	AG9
AP28	VSS25	VSS105	AG8
AP25	VSS26	VSS106	AG4
AP22	VSS27	VSS107	AF6
AP19	VSS28	VSS108	AF5
AP16	VSS29	VSS109	AF3
AP13	VSS30	VSS110	AF2
AP10	VSS31	VSS111	AE35
AP7	VSS32	VSS112	AE34
AP4	VSS33	VSS113	AE33
AP1	VSS34	VSS114	AE32
AN30	VSS35	VSS115	AE31
AN27	VSS36	VSS116	AE30
AN25	VSS37	VSS117	AE29
AN22	VSS38	VSS118	AE28
AN19	VSS39	VSS119	AE27
AN16	VSS40	VSS120	AE26
AN13	VSS41	VSS121	AE9
AN10	VSS42	VSS122	AD7
AN7	VSS43	VSS123	AC9
AN4	VSS44	VSS124	AC8
AM29	VSS45	VSS125	AC6
AM25	VSS46	VSS126	AC5
AM22	VSS47	VSS127	AC3
AM19	VSS48	VSS128	AC2
AM16	VSS49	VSS129	AB35
AM13	VSS50	VSS130	AB34
AM10	VSS51	VSS131	AB33
AM7	VSS52	VSS132	AB32
AM4	VSS53	VSS133	AB31
AM3	VSS54	VSS134	AB30
AM2	VSS55	VSS135	AB29
AM1	VSS56	VSS136	AB28
AL34	VSS57	VSS137	AB27
AL31	VSS58	VSS138	AB26
AL28	VSS59	VSS139	Y9
AL25	VSS60	VSS140	Y8
AL22	VSS61	VSS141	Y6
AL19	VSS62	VSS142	Y5
AL16	VSS63	VSS143	Y3
AL13	VSS64	VSS144	Y2
AL10	VSS65	VSS145	W35
AL7	VSS66	VSS146	W34
AL4	VSS67	VSS147	W33
AL2	VSS68	VSS148	W32
AK33	VSS69	VSS149	W31
AK30	VSS70	VSS150	W30
AK27	VSS71	VSS151	W29
AK25	VSS72	VSS152	W28
AK22	VSS73	VSS153	W27
AK19	VSS74	VSS154	W26
AK16	VSS75	VSS155	U9
AK13	VSS76	VSS156	U8
AK10	VSS77	VSS157	U6
AK7	VSS78	VSS158	U5
AK4	VSS79	VSS159	U3
AJ25	VSS80	VSS160	U2

FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER

CN4500

VSS

T35	VSS161	VSS234	F22
T34	VSS162	VSS235	F19
T33	VSS163	VSS236	E30
T32	VSS164	VSS237	E27
T31	VSS165	VSS238	E24
T30	VSS166	VSS239	E21
T29	VSS167	VSS240	E18
T28	VSS168	VSS241	E15
T27	VSS169	VSS242	E13
T26	VSS170	VSS243	E10
P9	VSS171	VSS244	E9
P8	VSS172	VSS245	E8
P6	VSS173	VSS246	E7
P5	VSS174	VSS247	E6
P3	VSS175	VSS248	E5
P2	VSS176	VSS249	E4
N35	VSS177	VSS250	E3
N34	VSS178	VSS251	E2
N33	VSS179	VSS252	E1
N32	VSS180	VSS253	D35
N31	VSS181	VSS254	D32
N30	VSS182	VSS255	D29
N29	VSS183	VSS256	D26
N28	VSS184	VSS257	D20
N27	VSS185	VSS258	D17
N26	VSS186	VSS259	C34
M34	VSS187	VSS260	C31
L33	VSS188	VSS261	C28
L30	VSS189	VSS262	C27
L27	VSS190	VSS263	C25
L9	VSS191	VSS264	C23
L8	VSS192	VSS265	C10
L6	VSS193	VSS266	C1
L5	VSS194	VSS267	B22
L4	VSS195	VSS268	B19
L3	VSS196	VSS269	B17
L2	VSS197	VSS270	B15
L1	VSS198	VSS271	B13
K35	VSS199	VSS272	B11
K32	VSS200	VSS273	B9
K29	VSS201	VSS274	B8
K26	VSS202	VSS275	B7
J34	VSS203	VSS276	B5
J31	VSS204	VSS277	B3
H33	VSS205	VSS278	B2
H30	VSS206	VSS279	A35
H27	VSS207	VSS280	A32
H24	VSS208	VSS281	A29
H21	VSS209	VSS282	A26
H18	VSS210	VSS283	A23
H15	VSS211	VSS284	A20
H13	VSS212	VSS285	A3
H10	VSS213		
H9	VSS214		
H8	VSS215		
H7	VSS216		
H6	VSS217		
H5	VSS218		
H4	VSS219		
H3	VSS220		
H2	VSS221		
H1	VSS222		
G35	VSS223		
G32	VSS224		
G29	VSS225		
G26	VSS226		
G23	VSS227		
G20	VSS228		
G17	VSS229		
G11	VSS230		
F34	VSS231		
F31	VSS232		
F29	VSS233		

FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER

CN4500

RESERVED

		CFG<0>	OUT	AK28	CFG[0]
		CFG<1>	OUT	AK29	CFG[1]
60<	25<	CFG<2>	OUT	AL26	CFG[2]
		CFG<3>	OUT	AL27	CFG[3]
60<	25<	CFG<4>	OUT	AK26	CFG[4]
60<	25<	CFG<5>	OUT	AL29	CFG[5]
60<	25<	CFG<6>	OUT	AL30	CFG[6]
60<	25<	CFG<7>	OUT	AM31	CFG[7]
		CFG<8>	OUT	AM32	CFG[8]
		CFG<9>	OUT	AM30	CFG[9]
		CFG<10>	OUT	AM28	CFG[10]
		CFG<11>	OUT	AM26	CFG[11]
		CFG<12>	OUT	AN28	CFG[12]
		CFG<13>	OUT	AN31	CFG[13]
		CFG<14>	OUT	AN26	CFG[14]
		CFG<15>	OUT	AM27	CFG[15]
		CFG<16>	OUT	AK31	CFG[16]
		CFG<17>	OUT	AN29	CFG[17]

AJ31	VAXG_VAL_SENSE	RSVD28	L7
AH31	VSSAXG_VAL_SENSE	RSVD29	AG7
AJ33	VCC_VAL_SENSE	RSVD30	AE7
AH33	VSS_VAL_SENSE	RSVD31	AK2
		RSVD32	W8
AJ26	RSVD5	RSVD33	AT26
		RSVD34	AM33
		RSVD35	AJ27
		VCC_DIE_SENSE	AH27
		VSS_DIE_SENSE	AH26
		RSVD37	T8
		RSVD38	J16
		RSVD39	H16
		RSVD40	G16
		RSVD_NCTF1	AR35
		RSVD_NCTF2	AT34
		RSVD_NCTF3	AT33
		RSVD_NCTF4	AP35
		RSVD_NCTF5	AR34
		RSVD_NCTF6	B34
		RSVD_NCTF7	A33
		RSVD_NCTF8	A34
		RSVD_NCTF9	B35
		RSVD_NCTF10	C35
F25	RSVD8		
F24	RSVD9		
F23	RSVD10		
D24	RSVD11	RSVD51	AJ32
G25	RSVD12	RSVD52	AK32
G24	RSVD13		
E23	RSVD14		
D23	RSVD15		
C30	RSVD16		
A31	RSVD17		
B30	RSVD18		
B29	RSVD19		
D30	RSVD20	BCLK_ITP	AN35
B31	RSVD21	BCLK_ITP#	AM35
A30	RSVD22		
C29	RSVD23		
J20	RSVD24		
B18	RSVD25	RSVD_NCTF11	AT2
		RSVD_NCTF12	AT1
		RSVD_NCTF13	AR1
J15	RSVD27		
		KEY	B1

IN CLK_XDP_CLKGEN_DP
IN CLK_XDP_CLKGEN_DN

FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER

PEG Static Lane Reversal

CFG(2)	1: (Default) Normal operation 0: Lane Reversed

LOW eDP ENABLE

CFG(4)	1: (Default) eDP Disabled 0: eDP Enabled

PEG Defer Training

CFG(7)	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

PCIE Port Bifurcation Straps

CFG[6:5]	11: (Default) x16 - Device 1 function 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled 00: x8, x4, x4 - Device 1 function 1 and 2 enabled

PEG Static Lan Reversal	CFG<2>	IN	R4522 1	2 1K_1%_2
LOW eDP ENABLE	CFG<4>	IN	R4521 1	2 1K_1%_2
60< 25>	CFG<5>	IN	R4520 1	2 1K_1%_2_DY
PCIE Port Bifurcation	CFG<6>	IN	R4519 1	2 1K_1%_2_DY
PEG Defer Training	CFG<7>	IN	R4518 1	2 1K_1%_2_DY

STRAP PIN

INVENTEC

TITLE: EVEREST-M
CPU 6 GND

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

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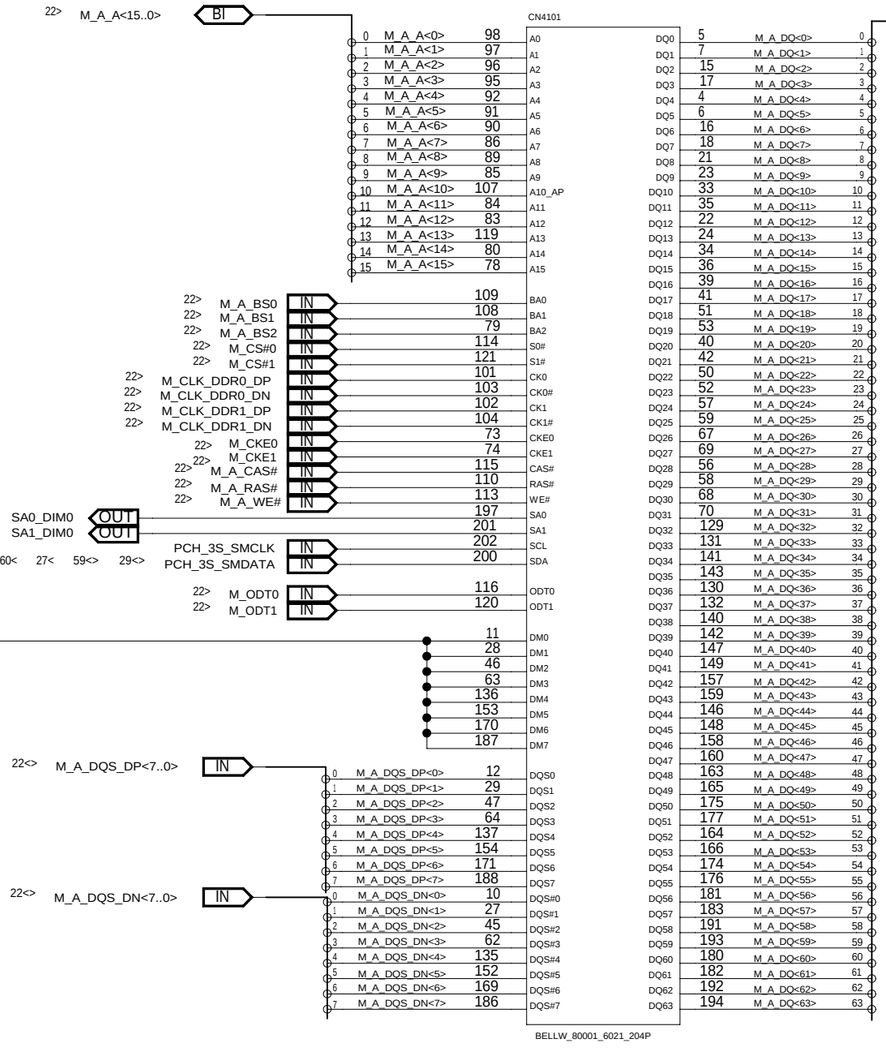
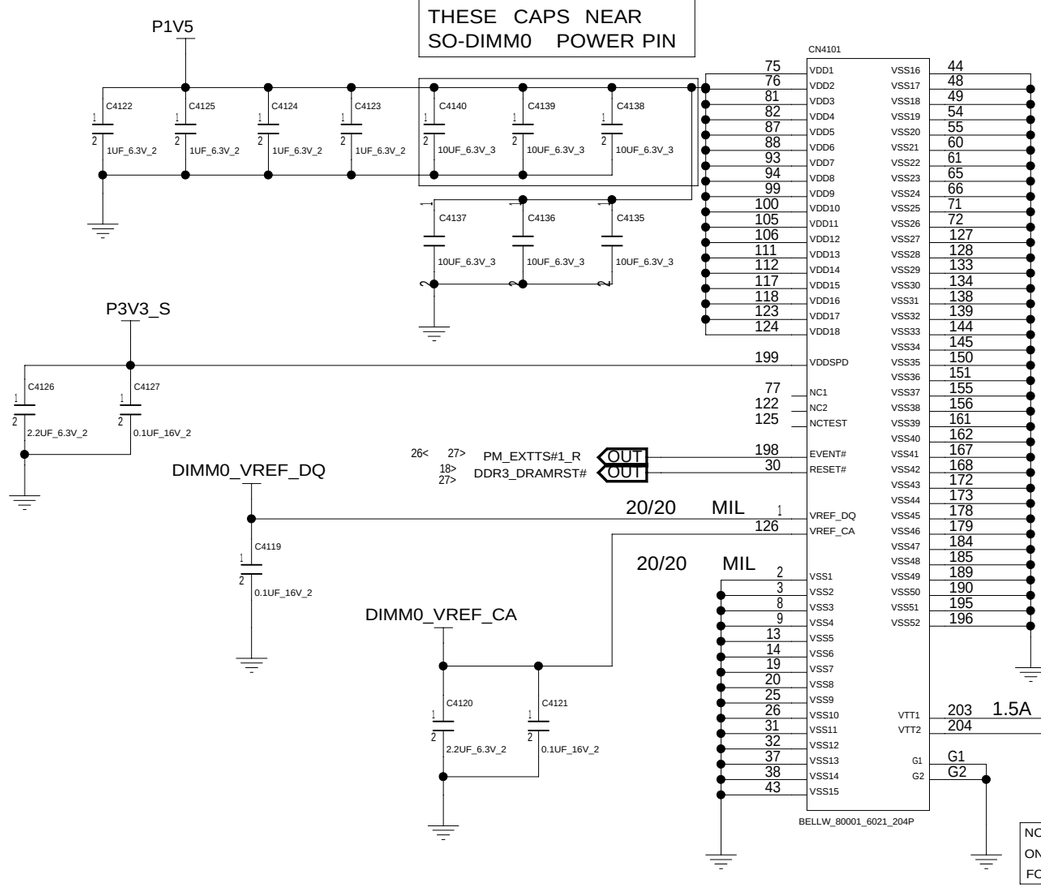
CHA





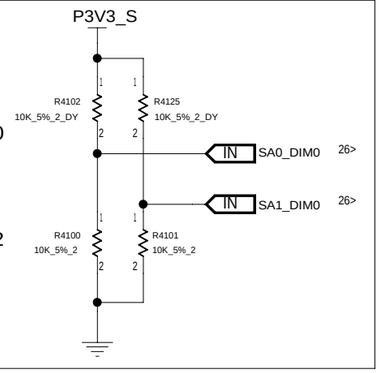
PLACE THESE CAPS CLOSE TO VTT1 AND VTT2

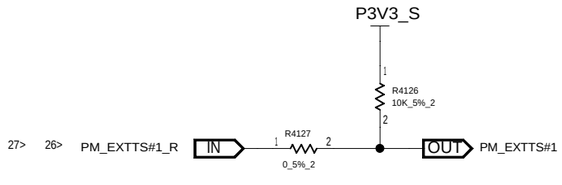
WS
REMOVE 1UF CAP 1PCS

NOTE:

IF SA0_DIM0=0 , SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0XA0
SO-DIMMA TS ADDRESS IS 0X30

IF SA0_DIM0=1 , SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0XA2
SO-DIMMA TS ADDRESS IS 0X32





INVENTEC

TITLE EVEREST-M
DDR3 DIMM0

SIZE C | CODE CS | DOC.NUMBER CS_1310AXXXXXX-MTR | REV A01

CHANGE by Frank Hu | DATE Fri Dec 31 10:17:00 2010 | SHEET 26 of 97

CHB

22> M_B_A<15..0> BI

CN4100

0	M_B_A<0>	98	A0		
1	M_B_A<1>	97	A1		
2	M_B_A<2>	96	A2		
3	M_B_A<3>	95	A3		
4	M_B_A<4>	92	A4		
5	M_B_A<5>	91	A5		
6	M_B_A<6>	90	A6		
7	M_B_A<7>	86	A7		
8	M_B_A<8>	89	A8		
9	M_B_A<9>	85	A9		
10	M_B_A<10>	107	A10_AP		
11	M_B_A<11>	84	A11		
12	M_B_A<12>	83	A12		
13	M_B_A<13>	119	A13		
14	M_B_A<14>	80	A14		
15	M_B_A<15>	78	A15		

22> M_B_BS0	IN	109	BA0		
22> M_B_BS1	IN	108	BA1		
22> M_B_BS2	IN	79	BA2		
22> M_CS#2	IN	114	S0#		
22> M_CS#3	IN	121	S1#		
22> M_CLK_DDR2_DP	IN	101	CK0		
22> M_CLK_DDR2_DN	IN	103	CK0#		
22> M_CLK_DDR3_DP	IN	102	CK1		
22> M_CLK_DDR3_DN	IN	104	CK1#		
22> M_CKE2	IN	73	CKE0		
22> M_CKE3	IN	74	CKE1		
22> M_B_CAS#	IN	115	CAS#		
22> M_B_RAS#	IN	110	RAS#		
22> M_B_WE#	IN	113	WE#		
27< SA0_DIM1	OUT	197	SA0		
27< SA1_DIM1	OUT	201	SA1		
PCH_3S_SMCLK	IN	202	SCL		
60< 26< 59<> 29<> PCH_3S_SMDATA	IN	200	SDA		
22> M_ODT2	IN	116	ODT0		
22> M_ODT3	IN	120	ODT1		
		11	DM0		
		28	DM1		
		46	DM2		
		63	DM3		
		136	DM4		
		153	DM5		
		170	DM6		
		187	DM7		

22<> M_B_DQS_DP<7..0>	IN	0 M_B_DQS_DP<0>	12	DQS0	
		1 M_B_DQS_DP<1>	29	DQS1	
		2 M_B_DQS_DP<2>	47	DQS2	
		3 M_B_DQS_DP<3>	64	DQS3	
		4 M_B_DQS_DP<4>	137	DQS4	
		5 M_B_DQS_DP<5>	154	DQS5	
		6 M_B_DQS_DP<6>	171	DQS6	
		7 M_B_DQS_DP<7>	188	DQS7	
22<> M_B_DQS_DN<7..0>	IN	0 M_B_DQS_DN<0>	10	DQS#0	
		1 M_B_DQS_DN<1>	27	DQS#1	
		2 M_B_DQS_DN<2>	45	DQS#2	
		3 M_B_DQS_DN<3>	62	DQS#3	
		4 M_B_DQS_DN<4>	135	DQS#4	
		5 M_B_DQS_DN<5>	152	DQS#5	
		6 M_B_DQS_DN<6>	169	DQS#6	
		7 M_B_DQS_DN<7>	186	DQS#7	

		5	M_B_DQ<0>	0	DQ0
		7	M_B_DQ<1>	1	DQ1
		15	M_B_DQ<2>	2	DQ2
		17	M_B_DQ<3>	3	DQ3
		4	M_B_DQ<4>	4	DQ4
		6	M_B_DQ<5>	5	DQ5
		16	M_B_DQ<6>	6	DQ6
		18	M_B_DQ<7>	7	DQ7
		21	M_B_DQ<8>	8	DQ8
		23	M_B_DQ<9>	9	DQ9
		33	M_B_DQ<10>	10	DQ10
		35	M_B_DQ<11>	11	DQ11
		22	M_B_DQ<12>	12	DQ12
		24	M_B_DQ<13>	13	DQ13
		34	M_B_DQ<14>	14	DQ14
		36	M_B_DQ<15>	15	DQ15
		39	M_B_DQ<16>	16	DQ16
		41	M_B_DQ<17>	17	DQ17
		51	M_B_DQ<18>	18	DQ18
		53	M_B_DQ<19>	19	DQ19
		40	M_B_DQ<20>	20	DQ20
		42	M_B_DQ<21>	21	DQ21
		50	M_B_DQ<22>	22	DQ22
		52	M_B_DQ<23>	23	DQ23
		57	M_B_DQ<24>	24	DQ24
		59	M_B_DQ<25>	25	DQ25
		67	M_B_DQ<26>	26	DQ26
		69	M_B_DQ<27>	27	DQ27
		56	M_B_DQ<28>	28	DQ28
		58	M_B_DQ<29>	29	DQ29
		68	M_B_DQ<30>	30	DQ30
		70	M_B_DQ<31>	31	DQ31
		129	M_B_DQ<32>	32	DQ32
		131	M_B_DQ<33>	33	DQ33
		141	M_B_DQ<34>	34	DQ34
		143	M_B_DQ<35>	35	DQ35
		130	M_B_DQ<36>	36	DQ36
		132	M_B_DQ<37>	37	DQ37
		140	M_B_DQ<38>	38	DQ38
		142	M_B_DQ<39>	39	DQ39
		147	M_B_DQ<40>	40	DQ40
		149	M_B_DQ<41>	41	DQ41
		157	M_B_DQ<42>	42	DQ42
		159	M_B_DQ<43>	43	DQ43
		146	M_B_DQ<44>	44	DQ44
		148	M_B_DQ<45>	45	DQ45
		158	M_B_DQ<46>	46	DQ46
		160	M_B_DQ<47>	47	DQ47
		163	M_B_DQ<48>	48	DQ48
		165	M_B_DQ<49>	49	DQ49
		175	M_B_DQ<50>	50	DQ50
		177	M_B_DQ<51>	51	DQ51
		164	M_B_DQ<52>	52	DQ52
		166	M_B_DQ<53>	53	DQ53
		174	M_B_DQ<54>	54	DQ54
		176	M_B_DQ<55>	55	DQ55
		181	M_B_DQ<56>	56	DQ56
		183	M_B_DQ<57>	57	DQ57
		191	M_B_DQ<58>	58	DQ58
		193	M_B_DQ<59>	59	DQ59
		180	M_B_DQ<60>	60	DQ60
		182	M_B_DQ<61>	61	DQ61
		192	M_B_DQ<62>	62	DQ62
		194	M_B_DQ<63>	63	DQ63

BELLW_80001_2021_204P

BI M_B_DQ<63..0> 22<>

LAYOUT NOTE: PLACE THESE CAPS NEAR SO-DIMM0 POWER PIN

P1V5

C4112 C4115 C4114 C4113 1UF_6.3V_2

C4134 C4133 C4132 C4131 C4130 C4129 10UF_6.3V_3

P3V3_S

C4116 2.2UF_6.3V_2

C4117 0.1UF_16V_2

WS

REMOVE CPU_CHB_VREFDQ

DIMM1_VREF_DQ

C4104 0.1UF_16V_2

CN4100

75	VDD1		VSS16	44	
76	VDD2		VSS17	48	
81	VDD3		VSS18	49	
82	VDD4		VSS19	54	
87	VDD5		VSS20	55	
88	VDD6		VSS21	60	
93	VDD7		VSS22	61	
94	VDD8		VSS23	65	
99	VDD9		VSS24	66	
100	VDD10		VSS25	71	
105	VDD11		VSS26	72	
106	VDD12		VSS27	127	
111	VDD13		VSS28	128	
112	VDD14		VSS29	133	
117	VDD15		VSS30	134	
118	VDD16		VSS31	138	
123	VDD17		VSS32	139	
124	VDD18		VSS33	144	
199	VDDSPD		VSS34	145	
77	NC1		VSS35	150	
122	NC2		VSS36	151	
125	NCTEST		VSS37	155	
198	EVENT#		VSS38	156	
30	RESET#		VSS39	161	
			VSS40	162	
			VSS41	167	
			VSS42	168	
			VSS43	172	
			VSS44	173	
			VSS45	178	
			VSS46	179	
			VSS47	184	
			VSS48	185	
			VSS49	189	
			VSS50	190	
			VSS51	195	
			VSS52	196	
126	VREF_DQ				
	VREF_CA				
2	VSS1				
3	VSS2				
8	VSS3				
9	VSS4				
13	VSS5				
14	VSS6				
19	VSS7				
20	VSS8				
25	VSS9				
26	VSS10		VTT1	203	
31	VSS11		VTT2	204	
32	VSS12				
37	VSS13		G1	G1	
38	VSS14		G2	G2	
43	VSS15				

BELLW_80001_2021_204P

PM_EXTTS#1_R OUT
DDR3_DRAMRST# OUT

20/20 MIL

DIMM1_VREF_CA

C4105 C4106 2.2UF_6.3V_2 0.1UF_16V_2

PLACE THESE CAPS CLOSE TO VTT1 AND VTT2

P0V75_S

1.5A

G1 G2

C4108 C4107 C4102 C4101 1UF_6.3V_2

NOTE:
SO-DIMMB SPD ADDRESS IS 0XA4
SO-DIMMB TS ADDRESS IS 0X34

P3V3_S

R4104 10K_5%_2 R4124 10K_5%_2_DY

SA1_DIM1 27> IN SA0_DIM1 27>

R4123 10K_5%_2_DY R4103 10K_5%_2

PLACE THESE CAPS CLOSE TO VTT1 AND VTT2

20/20 MIL

WS

CPU_CHA_VREFDQ

R4114 0_5%_2_DY

Q4100 NMOS_4D1S AO6402AL

R4128 1K_5%_2_DY

DRAMRST_CNTRL_CPU IN

DIMM0_VREF_DQ

R4115 R4111 0_5%_2

P1V5

R4118 R4117 1K_1%_2

P1V5_CPUDDRS

R4129 1K_5%_2_DY

C4118 0.1UF_16V_2

R4130 1K_5%_2_DY

C4103 0.1UF_16V_2

P1V5

R4122 R4121 1K_1%_2

DIMM1_VREF_DQ

R4119 R4110 R4141 0_5%_2

R4120 0_5%_2_DY

Q4101 NMOS_4D1S AO6402AL

CPU_CHB_VREFDQ

R4131 1K_5%_2_DY

IN DRAMRST_CNTRL_CPU

R4142 R4143 R4144 0_5%_2_DY

P0V75_VREF_M

DIMM0_VREF_CA

P1V5

R4132 1K_5%_2_DY

R4136 R4137 0_5%_2

R4133 1K_5%_2_DY

C4141 0.1UF_16V_2

R4105 0_5%_2_DY

R4138 R4139 R4140 R4112 0_5%_2

R4116 0_5%_2_DY

DIMM1_VREF_CA

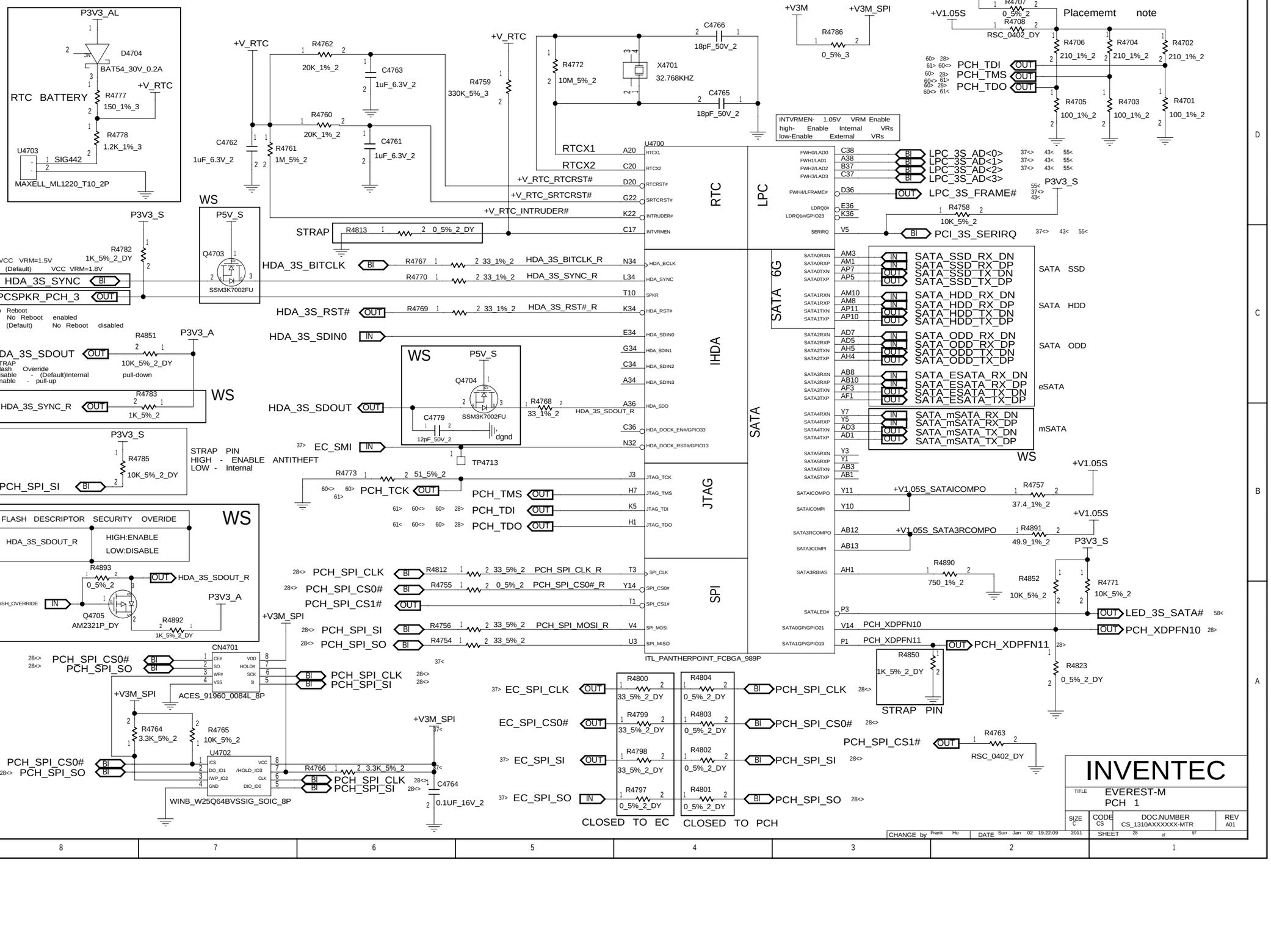
P1V5

R4134 R4135 1K_5%_2_DY

C4142 0.1UF_16V_2

INVENTEC

TITLE	EVEREST-M DDR3 DIMM1		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:16:30 2010	SHEET 27 of 97	


P3V3_AL
D4704
BAT54_30V_0.2A
RTC BATTERY
+V_RTC
R4777
150_1%_3
R4778
1.2K_1%_3
U4703
SIG442
MAXELL_ML1220_T10_2P
R4762
20K_1%_2
C4763
1uF_6.3V_2
R4760
20K_1%_2
C4762
1uF_6.3V_2
R4761
1M_5%_2
C4761
1uF_6.3V_2
R4759
330K_5%_3
R4772
10M_5%_2
X4701
32.768KHZ
C4766
18pF_50V_2
C4765
18pF_50V_2
+V3M
+V3M_SPI
R4786
0_5%_3
P3V3_A
+V1.05S
Placememt note
R4707
0_5%_2
R4708
RSC_0402_DY
R4706
210_1%_2
R4704
210_1%_2
R4702
210_1%_2
R4705
100_1%_2
R4703
100_1%_2
R4701
100_1%_2
PCH_TDI
PCH_TMS
PCH_TDO
INTVRMEN- 1.05V VRM Enable
high- Enable Internal VRs
low-Enable External VRs
U4700
RTCX1
RTCX2
+V_RTC_RTCRST#
+V_RTC_SRTCRST#
+V_RTC_INTRUDER#
STRAP
R4813
0_5%_2_DY
RTC
LPC
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
SERIRQ
LPC_3S_AD<0>
LPC_3S_AD<1>
LPC_3S_AD<2>
LPC_3S_AD<3>
LPC_3S_FRAME#
PCI_3S_SERIRQ
P3V3_S
R4758
10K_5%_2
WS
P5V_S
Q4703
SSM3K7002FU
P3V3_S
R4782
1K_5%_2_DY
H-VCC VRM=1.5V
L- (Default) VCC VRM=1.8V
HDA_3S_SYNC
PCSPKR_PCH_3
No Reboot
1: No Reboot enabled
0: (Default) No Reboot disabled
HDA_3S_BITCLK
HDA_3S_BITCLK_R
HDA_3S_SYNC_R
HDA_3S_RST#
HDA_3S_RST#_R
HDA_3S_SDIN0
HDA_3S_SDOUT
HDA_3S_SDOUT_R
EC_SMI
TP4713
IHDA
SATA
SATA 6G
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA_SSD_RX_DN
SATA_SSD_RX_DP
SATA_SSD_TX_DN
SATA_SSD_TX_DP
SATA SSD
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA_HDD_RX_DN
SATA_HDD_RX_DP
SATA_HDD_TX_DN
SATA_HDD_TX_DP
SATA HDD
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_ODD_RX_DN
SATA_ODD_RX_DP
SATA_ODD_TX_DN
SATA_ODD_TX_DP
SATA ODD
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA_ESATA_RX_DN
SATA_ESATA_RX_DP
SATA_ESATA_TX_DN
SATA_ESATA_TX_DP
eSATA
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA_mSATA_RX_DN
SATA_mSATA_RX_DP
SATA_mSATA_TX_DN
SATA_mSATA_TX_DP
mSATA
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
+V1.05S_SATAICOMPO
+V1.05S_SATA3RCOMPO
SATAICOMPO
SATAICOMPI
SATA3RCOMPO
SATA3COMPI
SATA3RBIAS
R4757
37.4_1%_2
R4891
49.9_1%_2
R4890
750_1%_2
R4852
10K_5%_2
R4771
10K_5%_2
SATALED#
SATA0GP/GPIO21
SATA1GP/GPIO19
LED_3S_SATA#
PCH_XDPFN10
PCH_XDPFN11
R4850
1K_5%_2_DY
STRAP PIN
R4823
0_5%_2_DY
JTAG
R4773
51_5%_2
PCH_TCK
PCH_TMS
PCH_TDI
PCH_TDO
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
SPI
PCH_SPI_CLK
PCH_SPI_CS0#
PCH_SPI_CS1#
PCH_SPI_SI
PCH_SPI_SO
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
ITL_PANTHERPOINT_FCBGA_989P
R4812
33_5%_2
PCH_SPI_CLK_R
R4755
0_5%_2
PCH_SPI_CS0#_R
R4756
33_5%_2
PCH_SPI_MOSI_R
R4754
33_5%_2
R4800
33_5%_2_DY
R4804
0_5%_2_DY
R4799
33_5%_2_DY
R4803
0_5%_2_DY
R4798
33_5%_2_DY
R4802
0_5%_2_DY
R4797
0_5%_2_DY
R4801
0_5%_2_DY
EC_SPI_CLK
EC_SPI_CS0#
EC_SPI_SI
EC_SPI_SO
CLOSED TO EC
CLOSED TO PCH
R4763
RSC_0402_DY
R4785
10K_5%_2_DY
PCH_SPI_SI
STRAP PIN
HIGH - ENABLE ANTITHEFT
LOW - Internal
FLASH DESCRIPTOR SECURITY OVERIDE
HDA_3S_SDOUT_R
HIGH:ENABLE
LOW:DISABLE
R4893
0_5%_2
FLASH_OVERRIDE
Q4705
AM2321P_DY
R4892
1K_5%_2_DY
R4851
10K_5%_2_DY
STRAP
Flash Override
Disable - (Default)Internal pull-down
Enable - pull-up
R4783
1K_5%_2
CN4701
ACES_91960_0084L_8P
U4702
WINB_W25Q64BVSSIG_SOIC_8P
R4764
3.3K_5%_2
R4765
10K_5%_2
R4766
3.3K_5%_2
C4764
0.1UF_16V_2
C4779
12pF_50V_2
R4768
33_1%_2
dgnd
+V3M_SPI
Distance between the PCH and cap on the "P" signal should be identical distance between the PCH and cap on the "N" signal for same pair
INVENTEC
TITLE
EVEREST-M
PCH 1
SIZE C
CODE CS
DOC.NUMBER CS_1310AXXXXXX-MTR
REV A01
CHANGE by Frank Hu
DATE Sun Jan 02 19:22:09 2011
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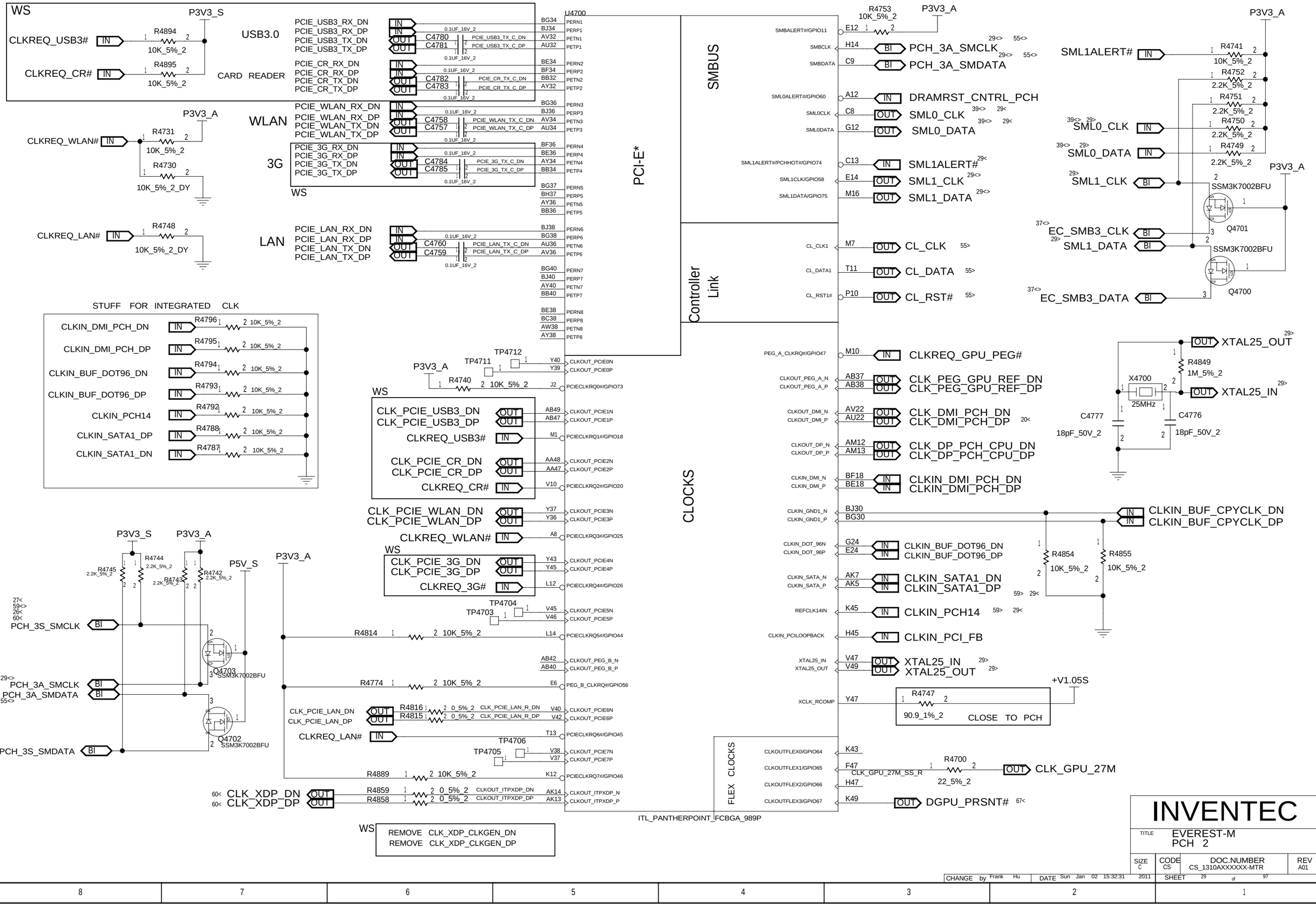
WS
P3V3_S
CLKREQ_USB3#
R4894
10K_5%_2
CLKREQ_CR#
R4895
10K_5%_2
USB3.0
CARD READER
PCIE_USB3_RX_DN
PCIE_USB3_RX_DP
PCIE_USB3_TX_DN
PCIE_USB3_TX_DP
C4780
C4781
0.1UF_16V_2
PCIE_CR_RX_DN
PCIE_CR_RX_DP
PCIE_CR_TX_DN
PCIE_CR_TX_DP
C4782
C4783
P3V3_A
CLKREQ_WLAN#
R4731
10K_5%_2
R4730
10K_5%_2_DY
WLAN
PCIE_WLAN_RX_DN
PCIE_WLAN_RX_DP
PCIE_WLAN_TX_DN
PCIE_WLAN_TX_DP
C4758
C4757
3G
PCIE_3G_RX_DN
PCIE_3G_RX_DP
PCIE_3G_TX_DN
PCIE_3G_TX_DP
C4784
C4785
WS
CLKREQ_LAN#
R4748
10K_5%_2_DY
LAN
PCIE_LAN_RX_DN
PCIE_LAN_RX_DP
PCIE_LAN_TX_DN
PCIE_LAN_TX_DP
C4760
C4759
U4700
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6
PERP6
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
PCI-E*
SMBUS
SMBALERT#/GPIO11
R4753
10K_5%_2
SMBCLK
SMBDATA
PCH_3A_SMCLK
PCH_3A_SMDATA
SML0ALERT#/GPIO60
DRAMRST_CNTRL_PCH
SML0CLK
SML0_CLK
SML0DATA
SML0_DATA
SML1ALERT#/PCHHOT#/GPIO74
SML1ALERT#
SML1CLK/GPIO58
SML1_CLK
SML1DATA/GPIO75
SML1_DATA
Controller Link
CL_CLK1
CL_CLK
CL_DATA1
CL_DATA
CL_RST1#
CL_RST#
SML1ALERT#
R4741
10K_5%_2
R4752
2.2K_5%_2
R4751
2.2K_5%_2
R4750
2.2K_5%_2
R4749
2.2K_5%_2
SML0_CLK
SML0_DATA
SML1_CLK
SSM3K7002BFU
Q4701
EC_SMB3_CLK
SML1_DATA
Q4700
EC_SMB3_DATA
STUFF FOR INTEGRATED CLK
CLKIN_DMI_PCH_DN
CLKIN_DMI_PCH_DP
CLKIN_BUF_DOT96_DN
CLKIN_BUF_DOT96_DP
CLKIN_PCH14
CLKIN_SATA1_DP
CLKIN_SATA1_DN
R4796
R4795
R4794
R4793
R4792
R4788
R4787
10K_5%_2
TP4712
TP4711
P3V3_A
R4740
10K_5%_2
CLKOUT_PCIE0N
CLKOUT_PCIE0P
PCIECLKRQ0#/GPIO73
WS
CLK_PCIE_USB3_DN
CLK_PCIE_USB3_DP
CLKREQ_USB3#
CLK_PCIE_CR_DN
CLK_PCIE_CR_DP
CLKREQ_CR#
CLK_PCIE_WLAN_DN
CLK_PCIE_WLAN_DP
CLKREQ_WLAN#
WS
CLK_PCIE_3G_DN
CLK_PCIE_3G_DP
CLKREQ_3G#
CLKOUT_PCIE1N
CLKOUT_PCIE1P
PCIECLKRQ1#/GPIO18
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2#/GPIO20
CLKOUT_PCIE3N
CLKOUT_PCIE3P
PCIECLKRQ3#/GPIO25
CLKOUT_PCIE4N
CLKOUT_PCIE4P
PCIECLKRQ4#/GPIO26
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5#/GPIO44
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PEG_B_CLKRQ#/GPIO56
CLKOUT_PCIE6N
CLKOUT_PCIE6P
PCIECLKRQ6#/GPIO45
CLKOUT_PCIE7N
CLKOUT_PCIE7P
PCIECLKRQ7#/GPIO46
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND1_N
CLKIN_GND1_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLOCKS
PEG_A_CLKRQ#/GPIO47
CLKREQ_GPU_PEG#
CLK_PEG_GPU_REF_DN
CLK_PEG_GPU_REF_DP
CLK_DMI_PCH_DN
CLK_DMI_PCH_DP
CLK_DP_PCH_CPU_DN
CLK_DP_PCH_CPU_DP
CLKIN_DMI_PCH_DN
CLKIN_DMI_PCH_DP
CLKIN_BUF_CPYCLK_DN
CLKIN_BUF_CPYCLK_DP
CLKIN_BUF_DOT96_DN
CLKIN_BUF_DOT96_DP
CLKIN_SATA1_DN
CLKIN_SATA1_DP
CLKIN_PCH14
CLKIN_PCI_FB
XTAL25_IN
XTAL25_OUT
R4854
10K_5%_2
R4855
10K_5%_2
R4747
90.9_1%_2
CLOSE TO PCH
+V1.05S
FLEX CLOCKS
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
CLK_GPU_27M_SS_R
R4700
22_5%_2
CLK_GPU_27M
DGPU_PRSNT#
ITL_PANTHERPOINT_FCBGA_989P
X4700
25MHz
C4777
18pF_50V_2
C4776
18pF_50V_2
R4849
1M_5%_2
XTAL25_OUT
XTAL25_IN
P3V5_S
P3V3_A
R4744
R4745
R4743
R4742
2.2K_5%_2
PCH_3S_SMCLK
PCH_3A_SMCLK
PCH_3A_SMDATA
PCH_3S_SMDATA
Q4703
Q4702
SSM3K7002BFU
R4814
R4774
R4889
R4859
R4858
CLK_XDP_DN
CLK_XDP_DP
CLKOUT_ITPXDP_DN
CLKOUT_ITPXDP_P
TP4704
TP4703
TP4706
TP4705
R4816
R4815
CLK_PCIE_LAN_R_DN
CLK_PCIE_LAN_R_DP
CLK_PCIE_LAN_DN
CLK_PCIE_LAN_DP
CLKREQ_LAN#
WS
REMOVE CLK_XDP_CLKGEN_DN
REMOVE CLK_XDP_CLKGEN_DP
INVENTEC
TITLE
EVEREST-M
PCH 2
SIZE C
CODE CS
DOC.NUMBER CS_1310AXXXXXX-MTR
REV A01
CHANGE by Frank Hu
DATE Sun Jan 02 15:32:31 2011
SHEET 29 of 97

DSWVRMEN - Deep S4/S5 Well On-Die Voltage Regulator Enable

high-Enabled(Default)
low-Disabled

U4700

DMI

FDI

STRAP PIN

+V_RTC
R4885 330K_5%_2
R4884 330K_5%_2_DY

DMI_RX_DN<0> BC24 DMI0RXN
DMI_RX_DN<1> BE20 DMI1RXN
DMI_RX_DN<2> BG18 DMI2RXN
DMI_RX_DN<3> BG20 DMI3RXN

DMI_RX_DP<0> BE24 DMI0RXP
DMI_RX_DP<1> BC20 DMI1RXP
DMI_RX_DP<2> BJ18 DMI2RXP
DMI_RX_DP<3> BJ20 DMI3RXP

DMI_TX_DN<0> AW24 DMI0TXN
DMI_TX_DN<1> AW20 DMI1TXN
DMI_TX_DN<2> BB18 DMI2TXN
DMI_TX_DN<3> AV18 DMI3TXN

DMI_TX_DP<0> AY24 DMI0TXP
DMI_TX_DP<1> AY20 DMI1TXP
DMI_TX_DP<2> AY18 DMI2TXP
DMI_TX_DP<3> AU18 DMI3TXP

+V1.05S
R4739 49.9_1%_2

BJ24 DMI_ZCOMP
BG25 DMI_IRCOMP
R4888 750_1%_2
BH21 DMI2RBIAS

FDI_RXN0 BJ14 FDI_TX_DN<0>
FDI_RXN1 AY14 FDI_TX_DN<1>
FDI_RXN2 BE14 FDI_TX_DN<2>
FDI_RXN3 BH13 FDI_TX_DN<3>
FDI_RXN4 BC12 FDI_TX_DN<4>
FDI_RXN5 BJ12 FDI_TX_DN<5>
FDI_RXN6 BG10 FDI_TX_DN<6>
FDI_RXN7 BG9 FDI_TX_DN<7>

FDI_RXP0 BG14 FDI_TX_DP<0>
FDI_RXP1 BB14 FDI_TX_DP<1>
FDI_RXP2 BF14 FDI_TX_DP<2>
FDI_RXP3 BG13 FDI_TX_DP<3>
FDI_RXP4 BE12 FDI_TX_DP<4>
FDI_RXP5 BG12 FDI_TX_DP<5>
FDI_RXP6 BJ10 FDI_TX_DP<6>
FDI_RXP7 BH9 FDI_TX_DP<7>

FDI_INT AW16 FDI_INT
FDI_FSYNC0 AV12 FDI_FSYNC0
FDI_FSYNC1 BC10 FDI_FSYNC1
FDI_LSYNC0 AV14 FDI_LSYNC0
FDI_LSYNC1 BB10 FDI_LSYNC1

DSWVRMEN A18

P3V3_S
R4734 10K_5%_2

EC SUSACK#_EC IN R4887 0_5%_2_DY SUSACK#_R C12 SUSACK#

SYS_RESET# IN K3 SYS_RESET#

R4847 0_5%_2
SUS_PWR_ACK_R IN OUT SUSACK#_R

CLOSE TO IC
ALLSYS_PWROK IN C4778 0.1UF_10V_2_DY P12 SYS_PWROK
EC_PCH_PWROK IN C4769 0.1UF_10V_2_DY L22 PWROK
PM_APWROK IN C4768 0.1UF_10V_2_DY L10 APWROK
PM_DRAM_PWRGD OUT B13 DRAMPWROK

P3V3_A
R4738 10K_5%_2
D4702 BAT54_30V_0.2A
EC_PWRSW# IN R4846 0_5%_2 E20 PWRBTN#
XDP_PWRSW# IN

RSMRST# IN R4886 0_5%_2 RSMRST#_R C21 RSMRST#
SUS_PWR_ACK OUT R4848 0_5%_2 SUS_PWR_ACK_R K16 SUSWARN#/SUSPWRDNACK/GPIO30

ACPRESENT IN H20 ACPRESENT/GPIO31
E10 BATLOW#/GPIO72
PM_RI# IN A10 RI#

D4703 BAT54_30V_0.2A
LOW_BAT#_3 IN

P3V3_A
R4732 8.2K_5%_2
ISOLATION

ITL_PANTHERPOINT_FCBGA_989P

Power Management

DPWROK E22 R4883 0_5%_2 IN RSMRST#_R
C4767 CLOSE TO IC 0.1UF_10V_2_DY
WAKE# B9 IN PCIE_WAKE# 55<> 30<
CLKRUN#/GPIO32 N3 BI PCI_3S_CLKRUN# 37<> 30< 43<
SUS_STAT#/GPIO61 G8 OUT SUS_STAT# 37>
SUSCLK/GPIO62 N14 OUT FM_32KHZ 37<
SLP_S5#/GPIO63 D10 OUT SLP_S5# 37>
SLP_S4# H4 OUT SLP_S4# 11< 37<
SLP_S3# F4 OUT SLP_S3# 11< 17< 18< 37<
SLP_A# G10 OUT SLP_A# 18< 19< 37<
SLP_SUS# G16 OUT SLP_SUS# 37<
PMSYNCH AP14 BI H_PM_SYNC 20<>
SLP_LAN#/GPIO29 K14 OUT SLP_LAN# 30> 12< 19< 37<

P3V3_A
ACPRESENT IN R4776 10K_5%_2
SUS_PWR_ACK IN R4735 10K_5%_2
PM_RI# IN R4736 10K_5%_2
PCIE_WAKE# IN R4775 10K_5%_2
SLP_LAN# OUT R4824 10K_5%_2_DY

P3V3_S
PCI_3S_CLKRUN# IN R4733 8.2K_5%_2

INVENTEC

TITLE EVEREST-M
PCH 3

SIZE C | CODE CS | DOC.NUMBER CS_1310AXXXXXX-MTR | REV A01

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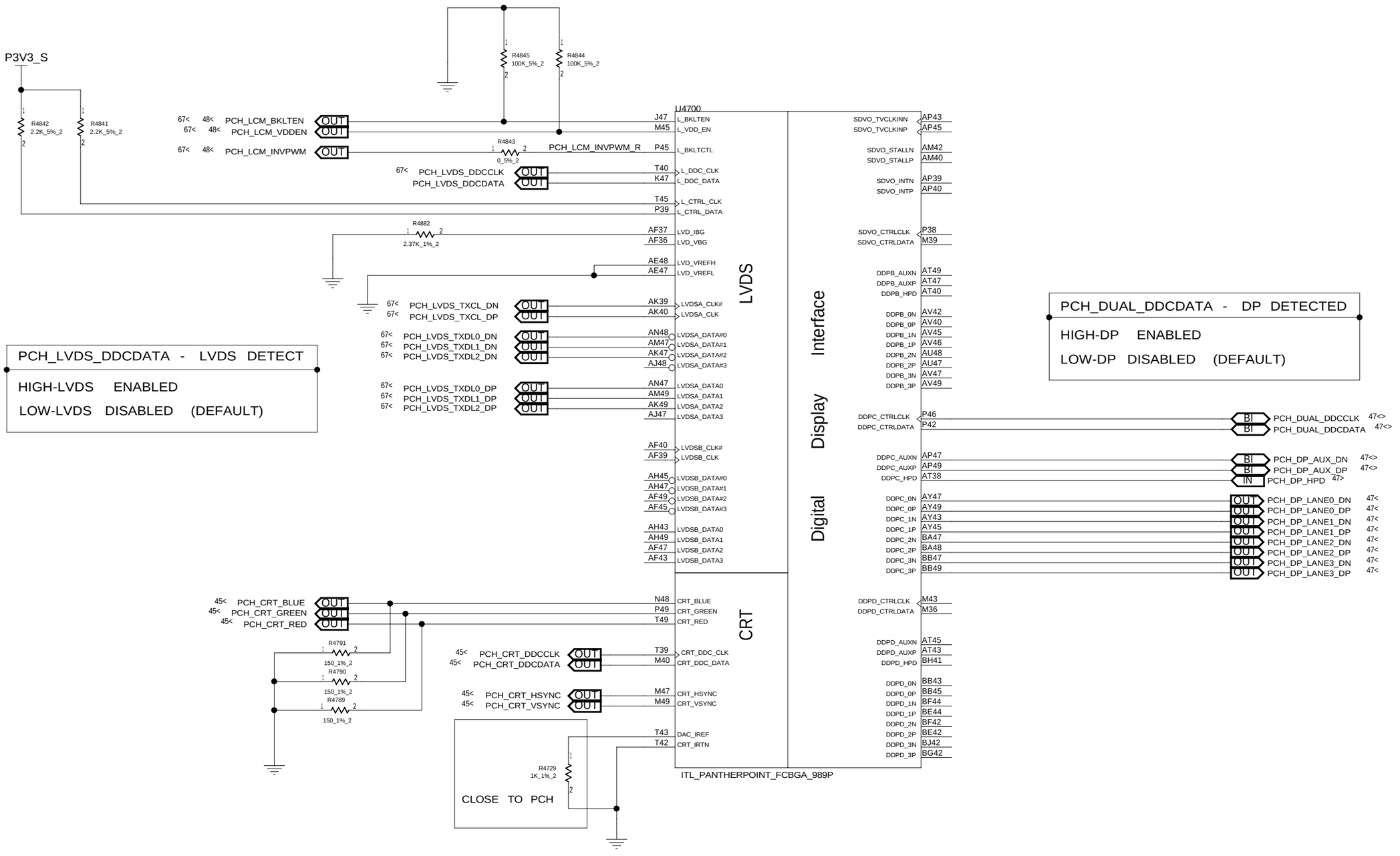

INVENTEC

TITLE EVEREST-M
PCH 4 AXG

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

CHANGE by Frank Hu DATE Sat Jan 01 18:30:03 2011 SHEET 31 of 97

GPIO51	GPIO19	BOOT BIOS
BBS_BIT1	BBS_BIT0	DESTINATION
0	1	RESERVED(NAND)
1	0	-
1	1	SPI (DEFAULT)
0	0	LPC

P3V3_S

R4711 8.2K_5%_2 — BI — PCI_3S_INTA# 32<>
R4725 8.2K_5%_2 — BI — PCI_3S_INTB# 32<>
R4724 8.2K_5%_2 — BI — PCI_3S_INTC# 32<>
R4723 8.2K_5%_2 — BI — PCI_3S_INTD# 32<>
R4722 10K_5%_2_DY — IN — RUNSCI0# 33> 37>

R4721 10K_5%_2_DY — BI — PCI_3S_INTG# 32<>
R4720 10K_5%_2_DY — BI — PCI_3S_INTH# 32<>
R4719 10K_5%_2 — IN — DGPU_HOLD_RST# 32> 37>
R4718 10K_5%_2_DY — IN — EC_DGPU_PWR_EN# 37> 67<
R4717 10K_5%_2 — IN — DGPU_SELECT# 32> 67<
R4818 10K_5%_2 — IN — SATA_ODD_DA# 32<> 50>
R4780 10K_5%_2 — IN — DGPU_PWR_EN# 32> 37<

P3V3_S

R4878 10K_5%_2
54> 32<> BTMDL# — BI
R4877 1K_5%_2_DY

BBS STRAP
BBS_BIT1
STP_A16OVR
R4728 1K_5%_2_DY
R4716 1K_5%_2_DY

STP_A16OVR	LOW=A16 SWAP OVERRIDE
TOP-BLOCK SWAP OVERRIDE	HIGH=DEFAULT

P3V3_A

68< 60< 39< 37< PLT_RST# — BI

C4772 0.1UF_16V_2
U4701 TC7SZ08FU
BUF_PLT_RST# — BI
R4727 100K_5%_2

Routed with 90 ohms impedance
Total length no longer than 11 inches

WS

USB3_P1_RX_DN	BI	BE28 USB3RN1
USB3_P3_RX_DN	BI	BC30 USB3RN2
USB3_P1_RX_DP	BI	BE32 USB3RN3
USB3_P3_RX_DP	BI	BJ32 USB3RN4
USB3_P1_TX_DN	BI	BC28 USB3RP1
USB3_P3_TX_DN	BI	BE30 USB3RP2
USB3_P1_TX_DP	BI	BF32 USB3RP3
USB3_P3_TX_DP	BI	BG32 USB3RP4
		AV26 USB3TN1
		BB26 USB3TN2
		AU28 USB3TN3
		AY30 USB3TN4
		AU26 USB3TP1
		AY26 USB3TP2
		AV28 USB3TP3
		AW30 USB3TP4

32<> PCI_3S_INTA# — BI — K40 PIRQA#
32<> PCI_3S_INTB# — BI — K38 PIRQB#
32<> PCI_3S_INTC# — BI — H38 PIRQC#
32<> PCI_3S_INTD# — BI — G38 PIRQD#

32< 37> DGPU_HOLD_RST# — OUT — C46 REQ1#/GPIO50
67< 32< DGPU_SELECT# — OUT — C44 REQ2#/GPIO52
37< 32< DGPU_PWR_EN# — OUT — E40 REQ3#/GPIO54

D47 GNT1#/GPIO51
DGPU_PWM_SELECT# — OUT — R4821 0_5%_2 — DGPU_PWM_SELECT#_R — E42 GNT2#/GPIO53
F46 GNT3#/GPIO55

54> 32<> BTMDL# — BI — G42 PIRQE#/GPIO2
32< 50> SATA_ODD_DA# — BI — G40 PIRQF#/GPIO3
32<> PCI_3S_INTG# — BI — C42 PIRQG#/GPIO4
32<> PCI_3S_INTH# — BI — D44 PIRQH#/GPIO5

P3V3_A
R4714 10K_5%_2_DY — +V3A_PME# — K10 PME#

C6 PLTRST#

37<> CLK_PCI_EC — OUT — R4881 22_5%_2 — CLK_PCI_EC_R — H49 CLKOUT_PCI0
43< CLK_PCI_TPM — OUT — R4879 22_5%_2 — CLK_PCI_TPM_R — H43 CLKOUT_PCI1
29< CLKIN_PCI_FB — OUT — R4880 22_5%_2 — CLK_PCI_FB_R — J48 CLKOUT_PCI2
55< CLK_PCI_DEBUG — OUT — TP4702 — R4715 22_5%_2 — CLK_PCI_DEBUG_R — K42 CLKOUT_PCI3 — H40 CLKOUT_PCI4

PCI

U4700

RSVD

BG26	TP1	
BJ26	TP2	
BH25	TP3	
BJ16	TP4	
BG16	TP5	
AH38	TP6	
AH37	TP7	
AK43	TP8	
AK45	TP9	
C18	TP10	
N30	TP11	
H3	TP12	
AH12	TP13	
AM4	TP14	
AM5	TP15	
Y13	TP16	
K24	TP17	
L24	TP18	
AB46	TP19	
AB45	TP20	
B21	TP21	
M20	TP22	
AY16	TP23	
BG46	TP24	

NVRAM

RSVD1	AY7
RSVD2	AV7
RSVD3	AU3
RSVD4	BG4
RSVD5	AT10
RSVD6	BC8
RSVD7	AU2
RSVD8	AT4
RSVD9	AT3
RSVD10	AT1
RSVD11	AY3
RSVD12	AT5
RSVD13	AV3
RSVD14	AV1
RSVD15	BB1
RSVD16	BA3
RSVD17	BB5
RSVD18	BB3
RSVD19	BB7
RSVD20	BE8
RSVD21	BD4
RSVD22	BF6
RSVD23	AV5
RSVD24	AV10
RSVD25	AT8
RSVD26	AY5
RSVD27	BA2
RSVD28	AT12
RSVD29	BF3

ITL_PANTHERPOINT_FCBGA_989P

DEBUG PORT

WS

USBP0N	C24	BI USB_P0_DN	RESERVE FOR USB3.0
USBP0P	A24	BI USB_P0_DP	
USBP1N	C25	BI USB_P1_DN	eSATA
USBP1P	B25	BI USB_P1_DP	
USBP2N	C26	BI USB_P2_DN	RESERVE FOR USB3.0
USBP2P	A26	BI USB_P2_DP	
USBP3N	K28		
USBP3P	H28		
USBP4N	E28		
USBP4P	D28		
USBP5N	C28	BI USB_P5_DN	WLAN
USBP5P	A28	BI USB_P5_DP	
USBP6N	C29		
USBP6P	B29		
USBP7N	N28		
USBP7P	M28		
USBP8N	L30		
USBP8P	K30		
USBP9N	G30		
USBP9P	E30	TP4714 — TP4715	
USBP10N	C30	BI USB_P10_DN	WEBCAM
USBP10P	A30	BI USB_P10_DP	
USBP11N	L32		
USBP11P	K32		
USBP12N	G32	BI USB_P12_DN	BT
USBP12P	E32	BI USB_P12_DP	
USBP13N	C32	BI USB_P13_DN	3G
USBP13P	A32	BI USB_P13_DP	

USB

USBRBIAS# C33 — R4726 22.6_1%_3 — CLOSE TO PCH
USBRBIAS B33

P3V3_A
R4817 10K_5%_2_DY
R4896 10K_5%_2_DY

OC0#/GPIO59	A14	R4839 0_5%_2	IN USB_OC#_0 RESERVE FOR USB3.0
OC1#/GPIO40	K20	R4840 0_5%_2	IN USB_OC#_1 FOR eSATA
OC2#/GPIO41	B17	R4838 10K_5%_2	IN USB_OC#_2 RESERVE FOR USB3.0
OC3#/GPIO42	C16	R4837 10K_5%_2	
OC4#/GPIO43	L16	R4836 10K_5%_2	
OC5#/GPIO9	A16	R4835 10K_5%_2	
OC6#/GPIO10	D14	R4834 10K_5%_2	
OC7#/GPIO14	C14	R4833 0_5%_2	IN SMC_WAKE_SCI#

IN PCH_XDPFN0
IN PCH_XDPFN1
IN PCH_XDPFN2
IN PCH_XDPFN3
IN PCH_XDPFN4
IN PCH_XDPFN5
IN PCH_XDPFN6
IN PCH_XDPFN7

P3V3_A
R4832 10K_5%_2
SMC_WAKE_SCI# — OUT

INVENTEC

TITLE: EVEREST-M
PCH 5 USB

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

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P3V3_A

R4831 2 1K_5%_2 OUT HOST_ALERT#1

STRAP PIN

HOST_ALERT#1 - TLS CONFIDENTIALITY

LOW - (DEFAULT) INTEL ME CRYPTO TRANSPORT LAYER SECURITY(TLS) CIPHER SUITE WITH NO CONFIDENTIALITY

HIGH - INTEL ME CRYPTO TLS CIPHER SUITE WITH CONFIDENTIALITY

STRAP PIN

INTEGRATED CLOCKING

P3V3_A

R4779 10K_5%_2_DY

R4820 2 1K_5%_2 OUT ICC_EN# 33> 59<

LOW - (DEFAULT) ENABLE INTEGRATED CLK

HIGH - DISABLE INTEGRATED CLK

P3V3_S

R4870 10K_5%_2 OUT BIOS_REC 33> 33<

R4864 10K_5%_2 OUT MFG_MODE 33> 33<

R4862 10K_5%_2_DY IN TEST_DET 33> 33<

R4830 200K_1%_2 OUT SATA_ODD_PRSNT# 33> 50>

R4826 10K_5%_2_DY OUT GFX_CRB_DET 33>

R4825 10K_5%_2 OUT CRIT_TEMP_REP# 33> 37>

R4861 10K_5%_2 IN TEST_DET 33> 33<

R4865 10K_5%_2_DY IN MFG_MODE 33>

R4873 10K_5%_2_DY IN BIOS_REC 33>

R4827 100K_5%_2 OUT GFX_CRB_DET 33>

P3V3_S STRAP PIN

R4828 1K_5%_2_DY OUT FDI_OVRVLTG 33>

R4829 10K_5%_2

FDI_OVRVLTG

LOW- TX,RXTERMINATED TO SAME VOLTAGE

(DC COUPLING MODE) DEFAULT

R4781 10K_5%_2_DY IN PCH_XDPFN8 33>

STRAP

PCH_XDPFN8 - ON DIE PLL VOLTAGE REGULATOR

HIGH-ENABLED (DEFAULT)

LOW-DISABLED

P3V3_S

P3V3_S

P3V3_A

P3V3_S

P3V3_S

U4700

R4876 10K_5%_2 PCH_XDPFN17 T7 BMBUSY#/GPIO0

R4872 10K_5%_2 A42 TACH1/GPIO1

R4871 10K_5%_2 DGPU_HPD_INTR#_R H36 TACH2/GPIO6

32< 37> RUNSCI0# OUT E38 TACH3/GPIO7

59< 33> ICC_EN# OUT R4819 0_5%_2 ICC_EN#_R C10 GPIO8

39<> LAN_PHY_PWR OUT C4 LAN_PHY_PWR_CTRL/GPIO12

33> HOST_ALERT#1 OUT R4875 0_5%_2 PCH_XDPFN16 G2 GPIO15

R4874 10K_5%_2 PCH_XDPFN14 U2 SATA4GP/GPIO16

67< 16> DGPU_PWROK BI D40 TACH0/GPIO17

1:DEFAULT/0:ENABLE 33> 33> BIOS_REC OUT T5 SCLOCK/GPIO22

R4869 10K_5%_2 E8 GPIO24

R4784 10K_5%_2 E16 GPIO27

33< PCH_XDPFN8 OUT P8 GPIO28

R4811 10K_5%_2 K1 STP_PCI#/GPIO34

R4868 10K_5%_2 PCH_XDPFN9 K4 GPIO35

50> 33> SATA_ODD_PRSNT# OUT R4867 0_5%_2 PCH_XDPFN12 V8 SATA2GP/GPIO36

33> FDI_OVRVLTG OUT R4866 0_5%_2 PCH_XDPFN13 M5 SATA3GP/GPIO37

33< 33> MFG_MODE OUT N2 SLOAD/GPIO38

33> GFX_CRB_DET OUT M3 SDATAOUT0/GPIO39

V13 SDATAOUT1/GPIO48

37> 33> CRIT_TEMP_REP# OUT R4863 0_5%_2 PCH_XDPFN15 V3 SATA5GP/GPIO49/TEMP_ALERT#

33< TEST_DET OUT D6 GPIO57

GPIO

TACH4/GPIO68 C40 OUT SATA_ODD_PWREN 50<

TACH5/GPIO69 B41 R4860 2.5K_1%_1/16W

TACH6/GPIO70 C41

TACH7/GPIO71 A40

A20GATE P4 IN EC_3S_A20GATE 37<

PECI AU16 PCH_PECI R4853 0_5%_2_DY OUT H_PECI 20> 37<>

RCIN# P5 IN KBRST# 37>

PROCPWRGD AY11 OUT H_CPUPWRGD 60> 20<

THRMTRIP# AY10 THRMTRIP#_R

INIT3_3V# T14

DF_TVS AY1

TS_VSS1 AH8

TS_VSS2 AK11

TS_VSS3 AH10

TS_VSS4 AK10

NC_1 P37

WS

FOLLOW EDS1.0

CPU/MISC

P1V05_VCCPS

R4713 56_5%_2_DY

R4712 390_5%_2

IN PM_THRMTRIP# 20> 38<

BOTH THESE SHOULD BE CLOSE TO PCH

OUT NV_CLE 20>

WS

NCTF

A4 VSS_NCTF_1

A44 VSS_NCTF_2

A45 VSS_NCTF_3

A46 VSS_NCTF_4

A5 VSS_NCTF_5

A6 VSS_NCTF_6

B3 VSS_NCTF_7

B47 VSS_NCTF_8

BD1 VSS_NCTF_9

BD49 VSS_NCTF_10

BE1 VSS_NCTF_11

BE49 VSS_NCTF_12

BF1 VSS_NCTF_13

BF49 VSS_NCTF_14

VSS_NCTF_15 BG2

VSS_NCTF_16 BG48

VSS_NCTF_17 BH3

VSS_NCTF_18 BH47

VSS_NCTF_19 BJ4

VSS_NCTF_20 BJ44

VSS_NCTF_21 BJ45

VSS_NCTF_22 BJ46

VSS_NCTF_23 BJ5

VSS_NCTF_24 BJ6

VSS_NCTF_25 C2

VSS_NCTF_26 C48

VSS_NCTF_27 D1

VSS_NCTF_28 D49

VSS_NCTF_29 E1

VSS_NCTF_30 E49

VSS_NCTF_31 F1

VSS_NCTF_32 F49

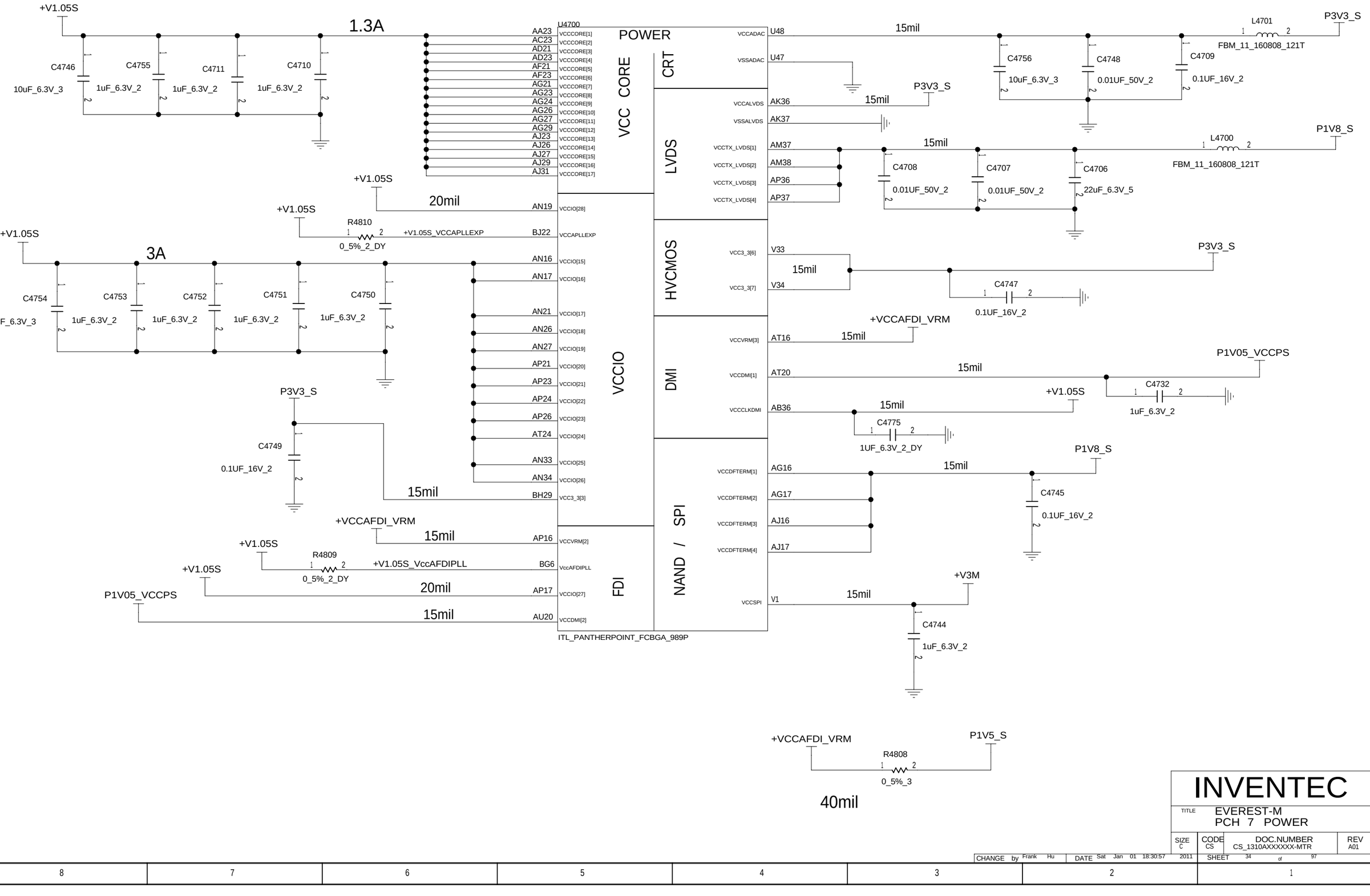
ITL_PANTHERPOINT_FCBGA_989P

INVENTEC

TITLE EVEREST-M
PCH 6 MISC

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

CHANGE by Frank Hu DATE Sun Jan 02 17:58:29 2011 SHEET 33 of 97

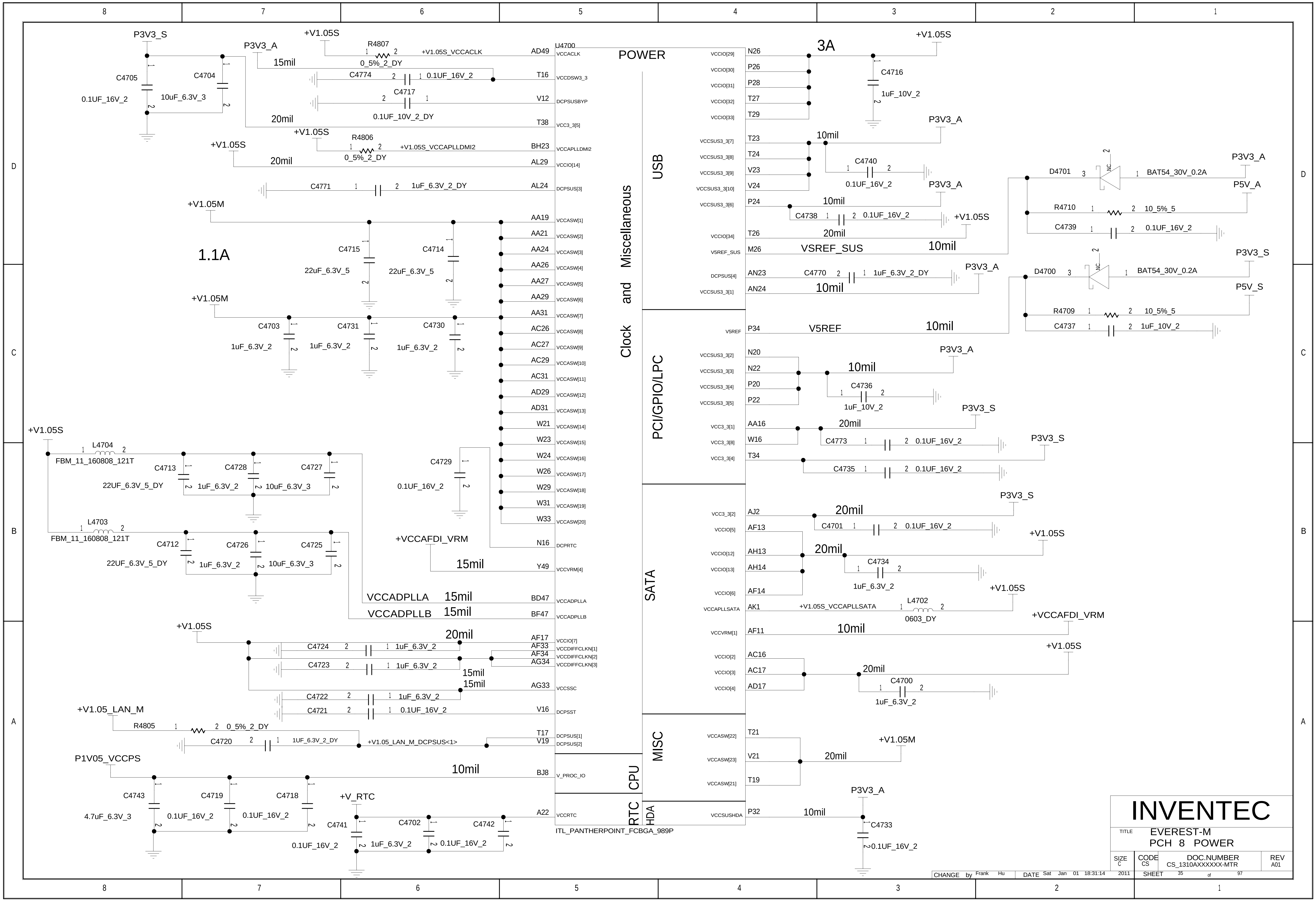


INVENTEC

TITLE: EVEREST-M
PCH 7 POWER

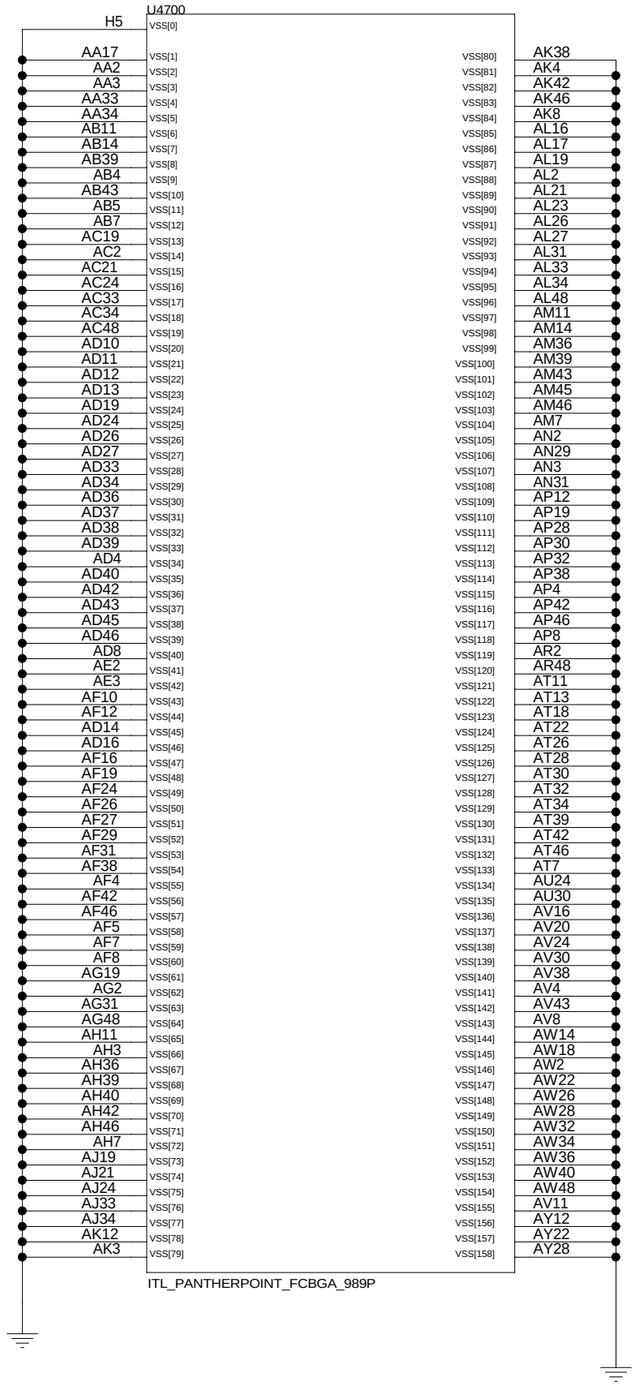
SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

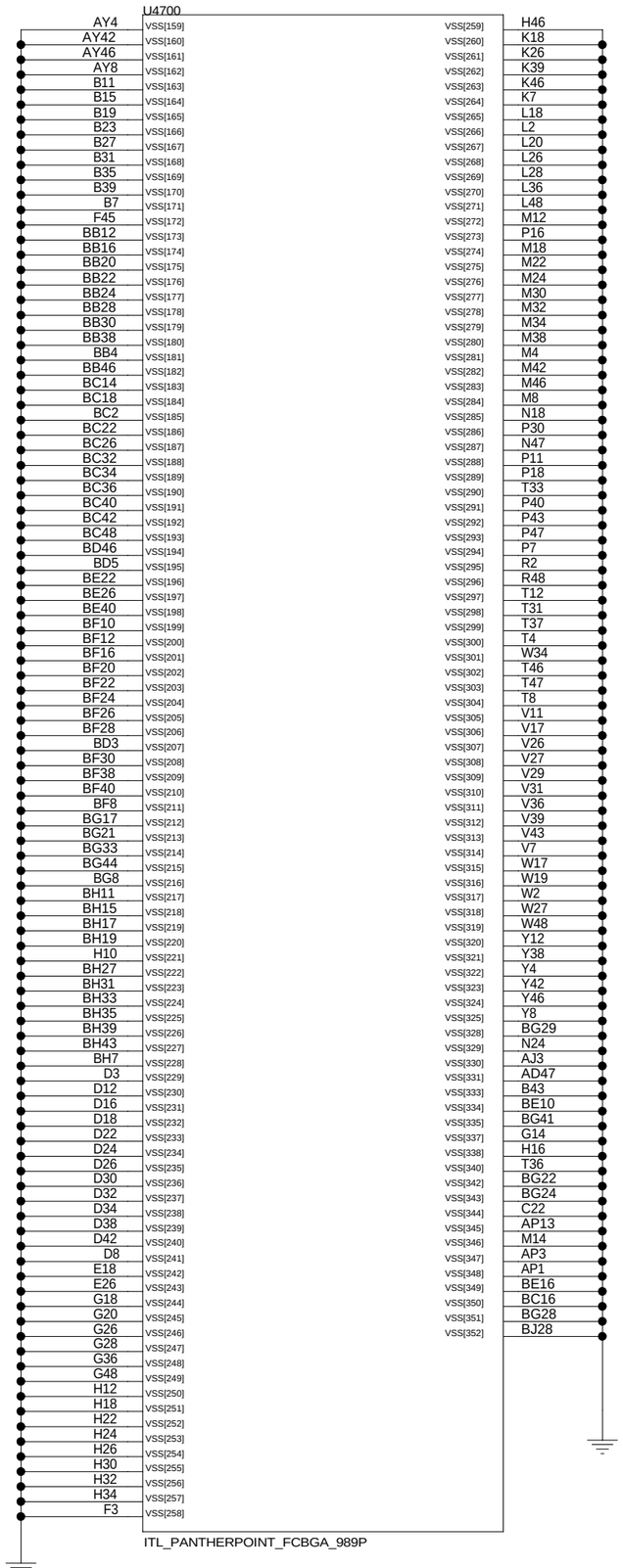
CHANGE by Frank Hu DATE Sat Jan 01 18:30:57 2011 SHEET 34 of 97



INVENTEC

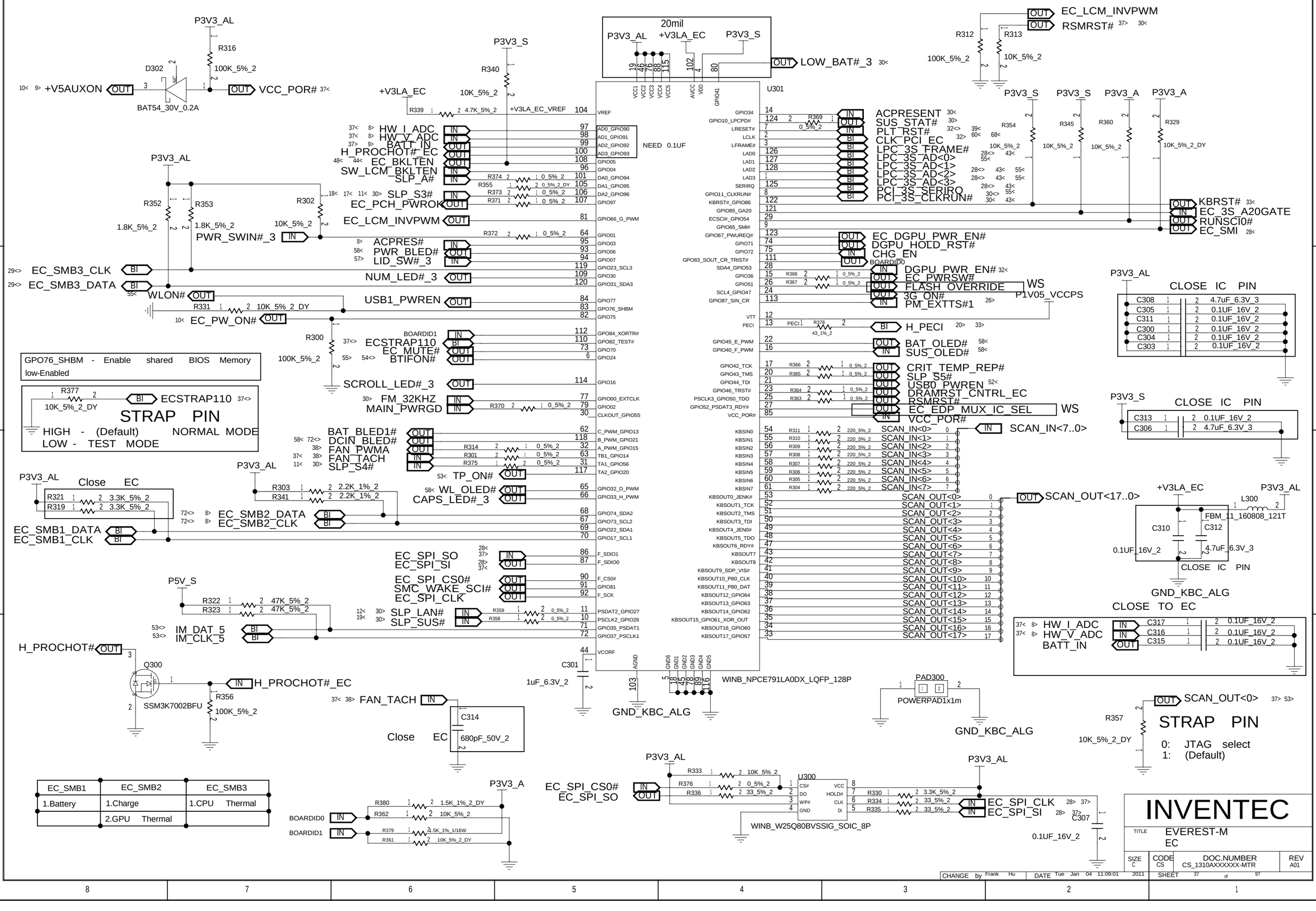
TITLE	EVEREST-M PCH 8 POWER
SIZE	C
CODE	CS
DOC.NUMBER	CS_1310AXXXXXX-MTR
REV	A01
CHANGE by	Frank Hu
DATE	Sat Jan 01 18:31:14 2011
SHEET	35 of 97

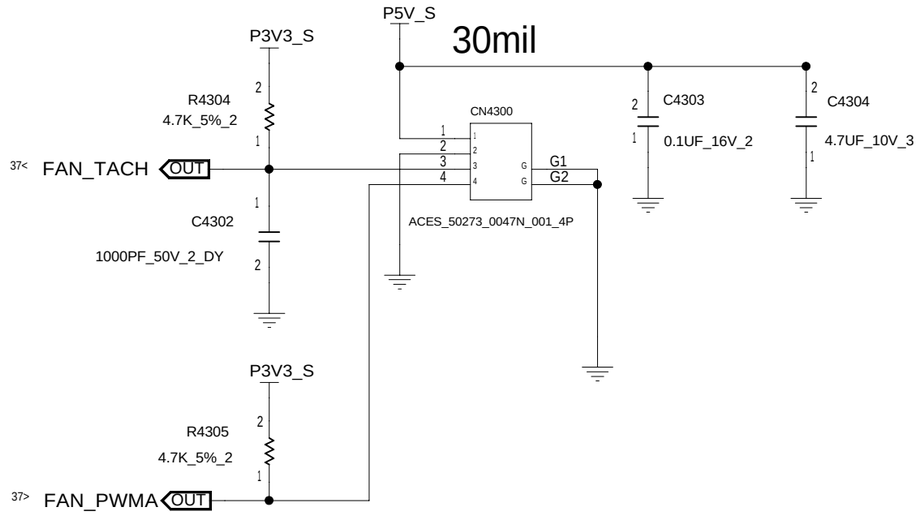


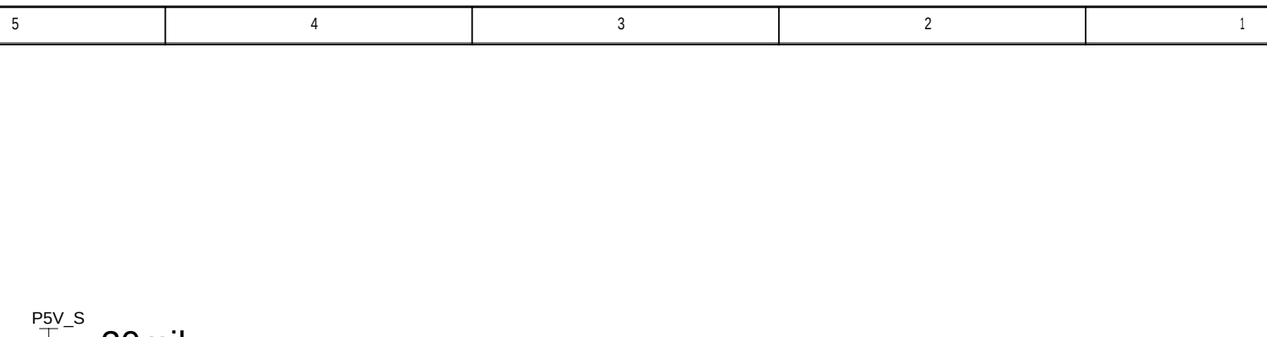


INVENTEC

TITLE	EVEREST-M PCH 9 GND		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Sun Jan 02 18:04:06 2011	SHEET 36 of 97	


P3V3_AL
R316
100K_5%_2
D302
BAT54_30V_0.2A
+V5AUXON
VCC_POR#
P3V3_S
R340
10K_5%_2
+V3LA_EC
R339 4.7K_5%_2
+V3LA_EC_VREF
20mil
P3V3_AL +V3LA_EC P3V3_S
LOW_BAT#_3
U301
NEED 0.1UF
HW_I_ADC
HW_V_ADC
BATT_IN
H_PROCHOT#_EC
EC_BKLTEN
SW_LCM_BKLTEN
SLP_A#
SLP_S3#
EC_PCH_PWROK
EC_LCM_INVPWM
PWR_SWIN#_3
ACPRES#
PWR_BLED#
LID_SW#_3
NUM_LED#_3
USB1_PWREN
EC_PW_ON#
WLON#
EC_SMB3_CLK
EC_SMB3_DATA
R352 1.8K_5%_2
R353 1.8K_5%_2
R302 10K_5%_2
R331 10K_5%_2_DY
ECSTRAP110
EC_MUTE#
BTIFON#
SCROLL_LED#_3
FM_32KHZ
MAIN_PWRGD
R300 100K_5%_2
BOARDID1
GPO76_SHBM - Enable shared BIOS Memory low-Enabled
R377 10K_5%_2_DY
STRAP PIN
HIGH - (Default) NORMAL MODE
LOW - TEST MODE
BAT_BLED1#
DCIN_BLED#
FAN_PWMA
FAN_TACH
SLP_S4#
R314 0_5%_2
R301 0_5%_2
R375 0_5%_2
TP_ON#
WL_OLED#
CAPS_LED#_3
P3V3_AL
R303 2.2K_1%_2
R341 2.2K_1%_2
EC_SMB2_DATA
EC_SMB2_CLK
EC_SMB1_DATA
EC_SMB1_CLK
Close EC
R321 3.3K_5%_2
R319 3.3K_5%_2
EC_SPI_SO
EC_SPI_SI
EC_SPI_CS0#
SMC_WAKE_SCI#
EC_SPI_CLK
P5V_S
R322 47K_5%_2
R323 47K_5%_2
SLP_LAN#
SLP_SUS#
R359 0_5%_2
R358 0_5%_2
IM_DAT_5
IM_CLK_5
H_PROCHOT#
Q300
SSM3K7002BFU
R356 100K_5%_2
H_PROCHOT#_EC
FAN_TACH
C314 680pF_50V_2
Close EC
C301 1uF_6.3V_2
GND_KBC_ALG
WINB_NPCE791LA0DX_LQFP_128P
PAD300
POWERPAD1x1m
GND_KBC_ALG
R312 100K_5%_2
R313 10K_5%_2
EC_LCM_INVPWM
RSMRST#
ACPRESENT
SUS_STAT#
PLT_RST#
CLK_PCI_EC
LPC_3S_FRAME#
LPC_3S_AD<0>
LPC_3S_AD<1>
LPC_3S_AD<2>
LPC_3S_AD<3>
PCI_3S_SERIRQ
PCI_3S_CLKRUN#
R369 0_5%_2
R354 10K_5%_2
R345 10K_5%_2
R360 10K_5%_2
R329 10K_5%_2_DY
P3V3_S
P3V3_A
KBRST#
EC_3S_A20GATE
RUNSCI0#
EC_SMI
EC_DGPU_PWR_EN#
DGPU_HOLD_RST#
CHG_EN
BOARDID0
DGPU_PWR_EN#
EC_PWRSW#
FLASH_OVERRIDE
3G_ON#
PM_EXTTS#1
WS
P1V05_VCCPS
H_PECI
BAT_OLED#
SUS_OLED#
CRIT_TEMP_REP#
SLP_S5#
USB0_PWREN
DRAMRST_CNTRL_EC
RSMRST#
EC_EDP_MUX_IC_SEL
VCC_POR#
SCAN_IN<0>
SCAN_IN<1>
SCAN_IN<2>
SCAN_IN<3>
SCAN_IN<4>
SCAN_IN<5>
SCAN_IN<6>
SCAN_IN<7>
SCAN_IN<7..0>
SCAN_OUT<0>
SCAN_OUT<1>
SCAN_OUT<2>
SCAN_OUT<3>
SCAN_OUT<4>
SCAN_OUT<5>
SCAN_OUT<6>
SCAN_OUT<7>
SCAN_OUT<8>
SCAN_OUT<9>
SCAN_OUT<10>
SCAN_OUT<11>
SCAN_OUT<12>
SCAN_OUT<13>
SCAN_OUT<14>
SCAN_OUT<15>
SCAN_OUT<16>
SCAN_OUT<17>
SCAN_OUT<17..0>
P3V3_AL
CLOSE IC PIN
C308 4.7uF_6.3V_3
C305 0.1UF_16V_2
C311 0.1UF_16V_2
C300 0.1UF_16V_2
C304 0.1UF_16V_2
C303 0.1UF_16V_2
P3V3_S
CLOSE IC PIN
C313 0.1UF_16V_2
C306 4.7uF_6.3V_3
+V3LA_EC
P3V3_AL
L300 FBM_11_160808_121T
C310 0.1UF_16V_2
C312 4.7uF_6.3V_3
CLOSE IC PIN
GND_KBC_ALG
CLOSE TO EC
HW_I_ADC
HW_V_ADC
BATT_IN
C317 0.1UF_16V_2
C316 0.1UF_16V_2
C315 0.1UF_16V_2
SCAN_OUT<0>
STRAP PIN
0: JTAG select
1: (Default)
R357 10K_5%_2_DY
EC_SMB1 | EC_SMB2 | EC_SMB3
1.Battery | 1.Charge | 1.CPU Thermal
2.GPU Thermal
P3V3_A
R380 1.5K_1%_2_DY
R362 10K_5%_2
R379 2.5K_1%_1/16W
R361 10K_5%_2_DY
BOARDID0
BOARDID1
EC_SPI_CS0#
EC_SPI_SO
P3V3_AL
R333 10K_5%_2
R376 0_5%_2
R336 33_5%_2
U300
WINB_W25Q80BVSSIG_SOIC_8P
R330 3.3K_5%_2
R334 33_5%_2
R335 33_5%_2
EC_SPI_CLK
EC_SPI_SI
C307 0.1UF_16V_2
INVENTEC
TITLE EVEREST-M EC
SIZE C
CODE CS
DOC.NUMBER CS_1310AXXXXXX-MTR
REV A01
CHANGE by Frank Hu
DATE Tue Jan 04 11:09:01 2011
SHEET 37 of 97





GM Thermal shutdown at 80.8℃ +/-3℃ from 60℃ to 100℃
PM Thermal shutdown at 86℃ +/-3℃ from 60℃ to 100℃
RSET=0.0012*T2-0.9308*T+96.147
Hysteresis is 30C

INVENTEC

TITLE EVEREST-M
FAN & THERMAL

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

CHANGE by Frank Hu DATE Fri Dec 31 10:16:37 2010 SHEET 38 of 97

30MIL

+V3M

+V3M_LAN

R415 0_5%_5

C416 0.1UF_16V_2

C414 0.1UF_16V_2

C415 22UF_6.3V_5 0805

C413 0.1UF_16V_2

+V3M_LAN

R417 10K_5%_2_DY

R416 10K_5%_2_DY

BI LAN_JTAG_TMS 39<>

BI LAN_JTAG_TCK 39<>

R412 0_5%_2

X400 25MHZ

OUT LAN_X1 39<

OUT LAN_X2 39<

C411 33PF_50V_2

C412 33PF_50V_2

P3V3_A

R411 10K_5%_2

U400

29< CLKREQ_LAN# OUT
68< 60< 37< 32<> PLT_RST# IN

R410 0_5%_2 CLKREQ_LAN#_R 48 CLK_REQ_N
R418 0_5%_2 PLT_RST#_R 36 PE_RST_N

29> CLK_PCIE_LAN_DP IN 44 PE_CLKP
29> CLK_PCIE_LAN_DN IN 45 PE_CLKN

29< PCIE_LAN_RX_DP OUT
29< PCIE_LAN_RX_DN OUT

C404 0.1UF_16V_2 PCIE_LAN_RX_C_DP 38 PETp
C403 0.1UF_16V_2 PCIE_LAN_RX_C_DN 39 PETn

29> PCIE_LAN_TX_DP IN 41 PERp
29> PCIE_LAN_TX_DN IN 42 PERn

PCI-E

29< 29> SML0_CLK BI
29< 29> SML0_DATA BI

R408 0_5%_2 SMB_CLK_LAN 28 SMB_CLK
R409 0_5%_2 SMB_DATA_LAN 31 SMB_DATA

SMB

+V3M_LAN

LAN_ENABLE 3 LAN_DISABLE_N

R407 10K_5%_2

33> LAN_PHY_PWR BI R405 0_5%_2

R406 0_5%_2_DY

40< LED_R3S_LANACT# BI 26 LED0
LED_R3S_LANLINK# BI 27 LED1
TP400 25 LED2

LED

TP402 TP401 32 JTAG_TDI
34 JTAG_TDO
39<> LAN_JTAG_TMS BI 33 JTAG_TMS
39<> LAN_JTAG_TCK BI 35 JTAG_TCK

JTAG

39> LAN_X1 IN 9 XTAL_OUT
39> LAN_X2 IN 10 XTAL_IN

30 TEST_EN
12 RBIAS

R404 1K_5%_2
R403 3.01K_1%_2

ITL_LEWISVILLE_PQFN_48P

MDI

MDI_PLUS0 13 BI LAN_TRD0_DP 40<
MDI_MINUS0 14 BI LAN_TRD0_DN 40<
MDI_PLUS1 17 BI LAN_TRD1_DP 40<
MDI_MINUS1 18 BI LAN_TRD1_DN 40<
MDI_PLUS2 20 BI LAN_TRD2_DP 40<
MDI_MINUS2 21 BI LAN_TRD2_DN 40<
MDI_PLUS3 23 BI LAN_TRD3_DP 40<
MDI_MINUS3 24 BI LAN_TRD3_DN 40<

+V3M_LAN

RSVD_NC 6 +V3M_LAN_RSVD_NC R414 0_5%_2_DY
RSVD_VCC3P3_1 1 +V3M_LAN_RSVD_VCC3P3_1 R401 4.7K_5%_2
RSVD_VCC3P3_2 2 +V3M_LAN_RSVD_VCC3P3_2 R400 4.7K_5%_2
VDD3P3_IN 5

15MIL

VDD3P3_OUT 4

R413 0_5%_2

C400 1UF_10V_2

VDD3P3_15 15
VDD3P3_19 19
VDD3P3_29 29

+V1.05_LAN

VDD1P0_47 47
VDD1P0_46 46
VDD1P0_37 37

15MIL

VDD1P0_43 43

15MIL

VDD1P0_11 11

VDD1P0_40 40
VDD1P0_22 22
VDD1P0_16 16
VDD1P0_8 8

15MIL

+V1.05_LAN_CTRL_1P0

CTRL_1P0 7 L400 0603_DY 4.7UH

VSS_EPAD 49

C401 22UF_6.3V_5

C402 0.1UF_16V_2

+V1.05_LAN

R402 0_5%_5

+V1.05_LAN_M

15MIL

+V3M_LAN

15MIL

INVENTEC			
TITLE	EVEREST-M LAN		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:16:38 2010	SHEET 39 of 97	

LED_R3S_LANACT# IN R477 1 2 RSC_0603_DY

+V3M_LAN

R478 1 2 RSC_0603_DY

R476 1 2 RSC_0603_DY IN LED_R3S_LANLINK#

R475 1 2 RSC_0603_DY

WS

LAN_TRD3_CN_DP IN
LAN_TRD3_CN_DN IN
LAN_TRD2_CN_DP IN
LAN_TRD1_CN_DP IN
LAN_TRD1_CN_DN IN
LAN_TRD2_CN_DN IN
LAN_TRD0_CN_DP IN
LAN_TRD0_CN_DN IN

JACK470

1 TX+
2 TX-
3 RX+
4 P4
5 P5
6 RX-
7 P7
8 P8
G G1
G G2
G G3
G G4

SYN_100073HR008G13CZL_8P

+V3M_LAN

R472 1 2 0_5%_2_DY

WS

LAN_TRD3_DN IN
LAN_TRD3_DP IN
LAN_TRD2_DN IN
LAN_TRD2_DP IN
LAN_TRD1_DN IN
LAN_TRD1_DP IN
LAN_TRD0_DN IN
LAN_TRD0_DP IN

+V3M_LAN_TRANSFORMER

U470

1 TCT1 MCT1 24
3 TD1- MX1- 22
2 TD1+ MX1+ 23
4 TCT2 MCT2 21
6 TD2- MX2- 19
5 TD2+ MX2+ 20
7 TCT3 MCT3 18
9 TD3- MX3- 16
8 TD3+ MX3+ 17
10 TCT4 MCT4 15
12 TD4- MX4- 13
11 TD4+ MX4+ 14

BOTH_GST5009_SOP_24P

OUT LAN_TRD0_CN_DN 40<
OUT LAN_TRD0_CN_DP 40<
OUT LAN_TRD1_CN_DN 40<
OUT LAN_TRD1_CN_DP 40<
OUT LAN_TRD2_CN_DN 40<
OUT LAN_TRD2_CN_DP 40<
OUT LAN_TRD3_CN_DN 40<
OUT LAN_TRD3_CN_DP 40<

C409 1 2 0.1UF_16V_2
C408 1 2 0.1UF_16V_2
C407 1 2 0.1UF_16V_2
C406 1 2 0.1UF_16V_2
C405 1 2 1UF_6.3V_2

R473 1 2 75_5%_3
R474 1 2 75_5%_3
R470 1 2 75_5%_3
R471 1 2 75_5%_3

C410 1 2 1000PF_2000V_6

8152 OPEN

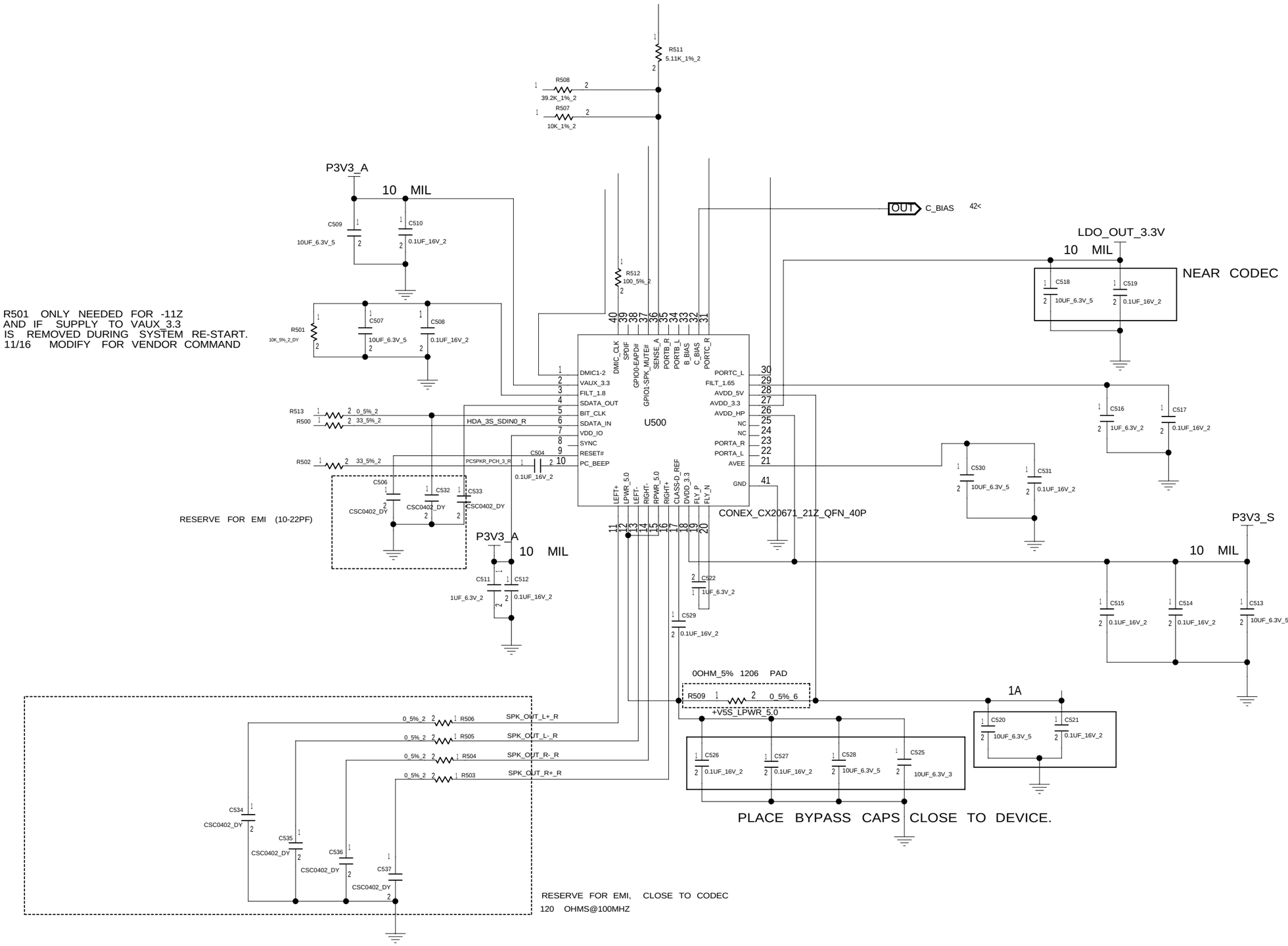
INVENTEC

TITLE EVEREST-M
RJ45 & TRANSFORMER

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

CHANGE by Frank Hu DATE Tue Jan 04 00:15:14 2011 SHEET 40 of 97

R501 ONLY NEEDED FOR -11Z
AND IF SUPPLY TO VAUX_3.3
IS REMOVED DURING SYSTEM RE-START.
11/16 MODIFY FOR VENDOR COMMAND



PORT CONFIGURATION

PORT A:	HEADPHONE JACK
PORT B:	INTERNAL MIC
PORT C:	MICROPHONE JACK

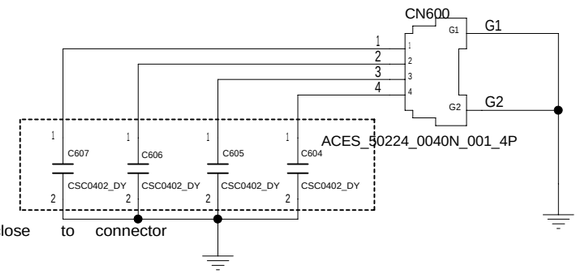
INVENTEC

TITLE: EVEREST-M AUDIO CODEC

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

CHANGE by Frank Hu DATE Sun Jan 02 13:16:19 2011 SHEET 41 of 97

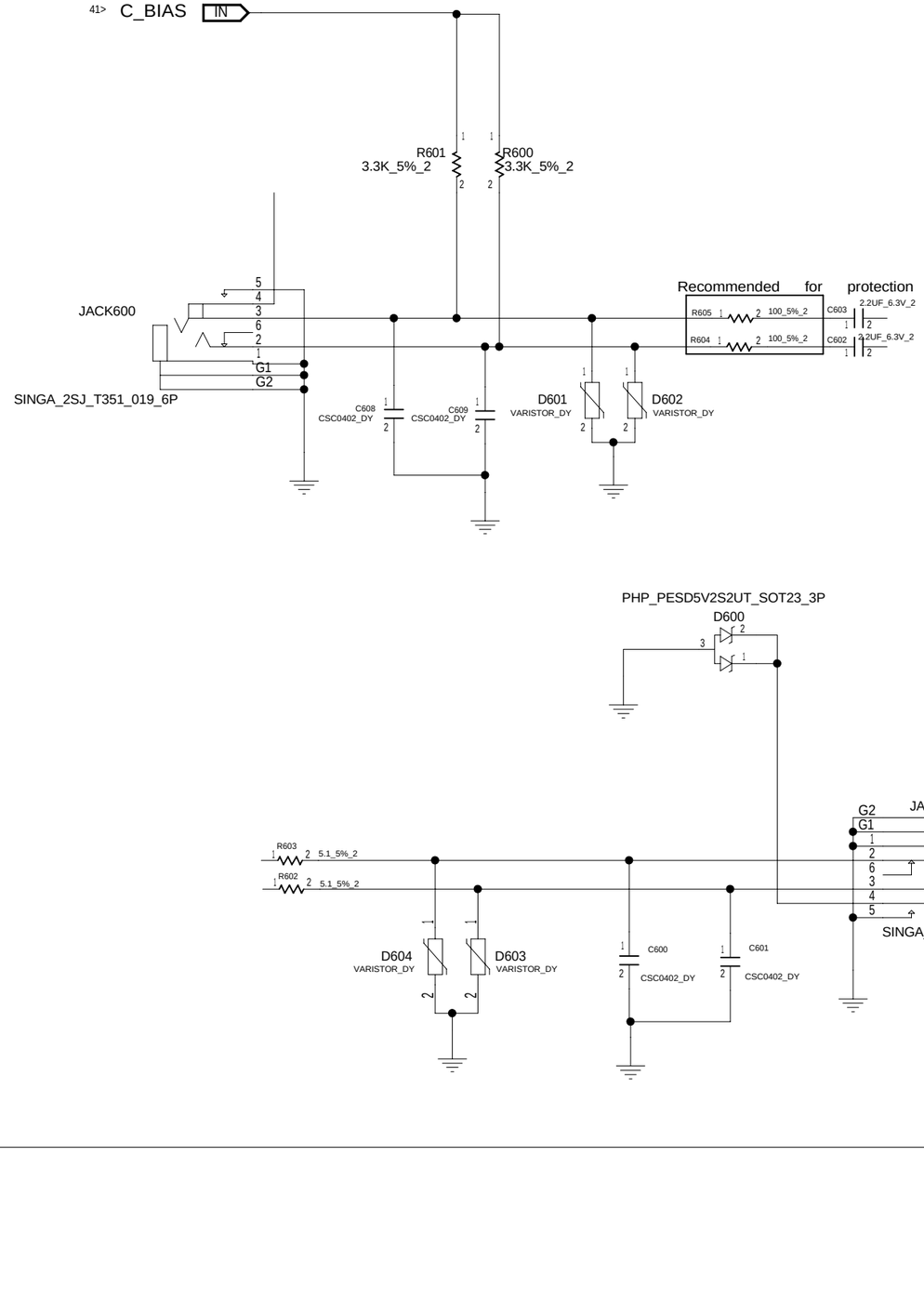
INTERNAL SPEAKERS



Reserve for EMI, place close to connector

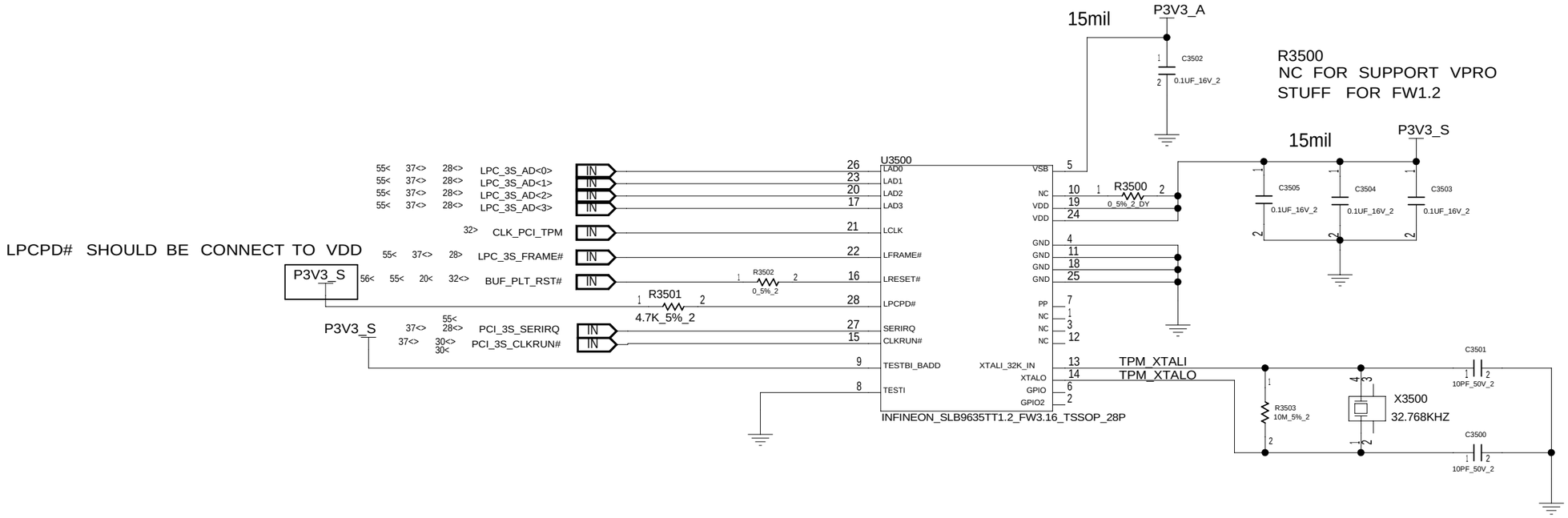
AUDIO JACKS

PORT C
EXTENAL MICROPHONE



INVENTEC

TITLE: EVEREST-M AUDIO AMP			
SIZE: C	CODE: CS	DOC.NUMBER: CS_1310AXXXXXX-MTR	REV: A01
CHANGE by: Frank Hu	DATE: Sun Jan 02 13:17:10 2011	SHEET: 42 of 97	



TPM1.2

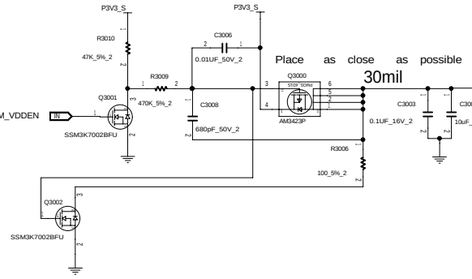
FW VERSION	P/N
1.02	6019B0101801
3.16	6019B0761601 (SUPPORT VPRO)

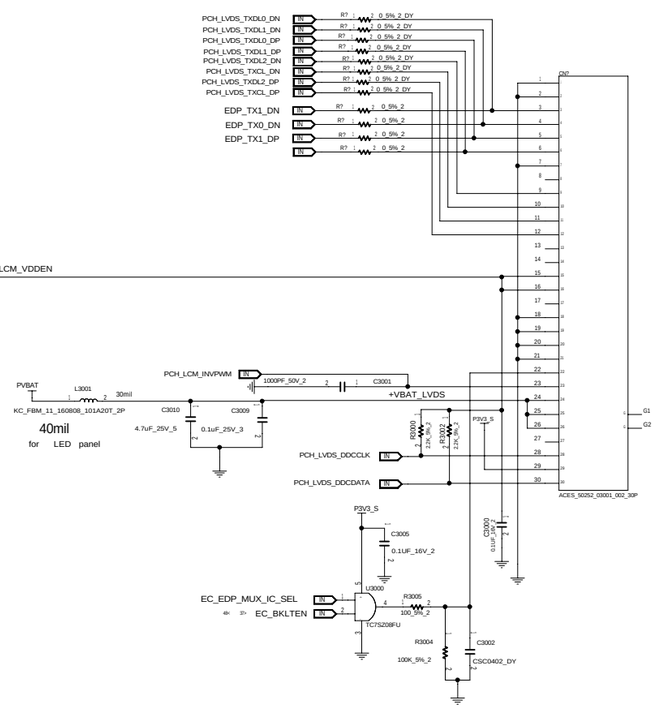
INVENTEC

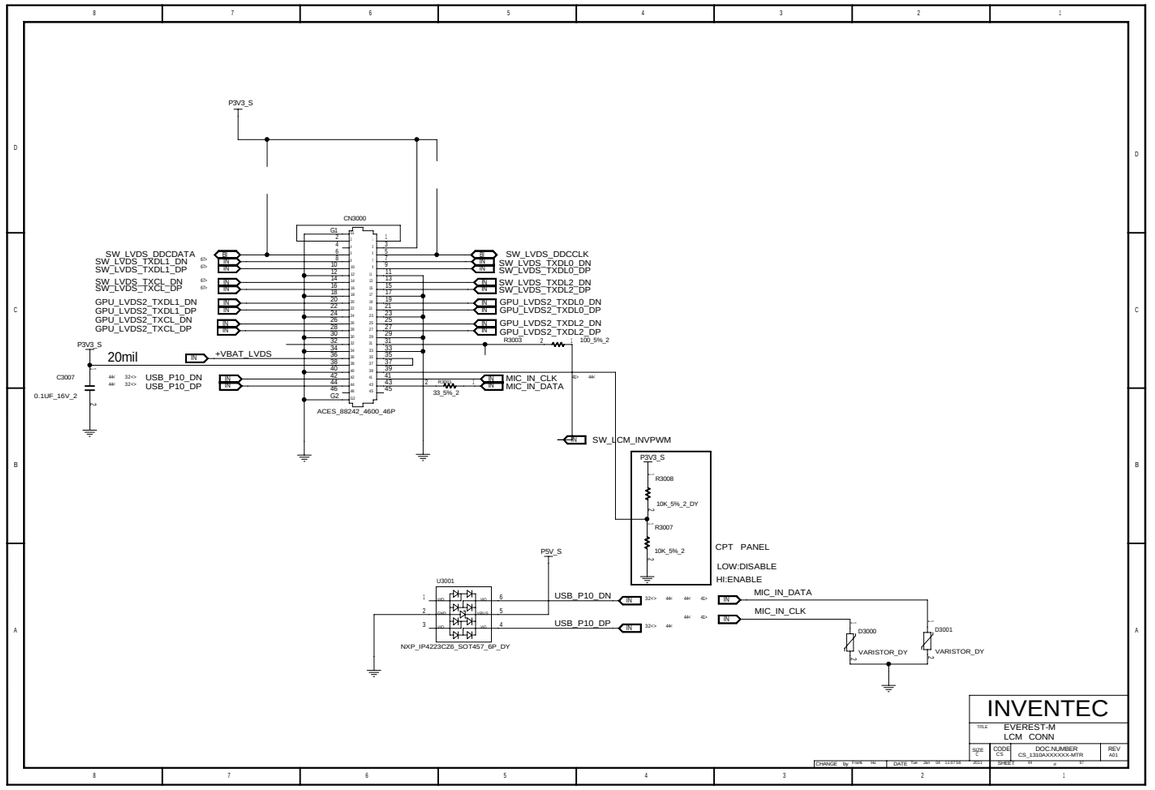
TITLE: EVEREST-M TPM

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

CHANGE by Frank Hu DATE Fri Dec 31 10:16:39 2010 SHEET 43 of 97





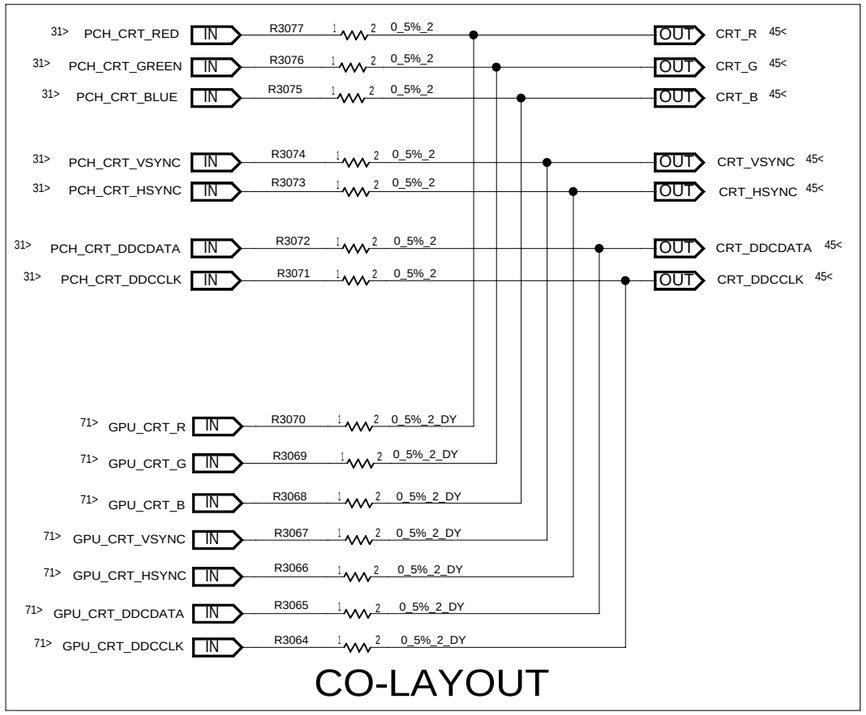


INVENTEC

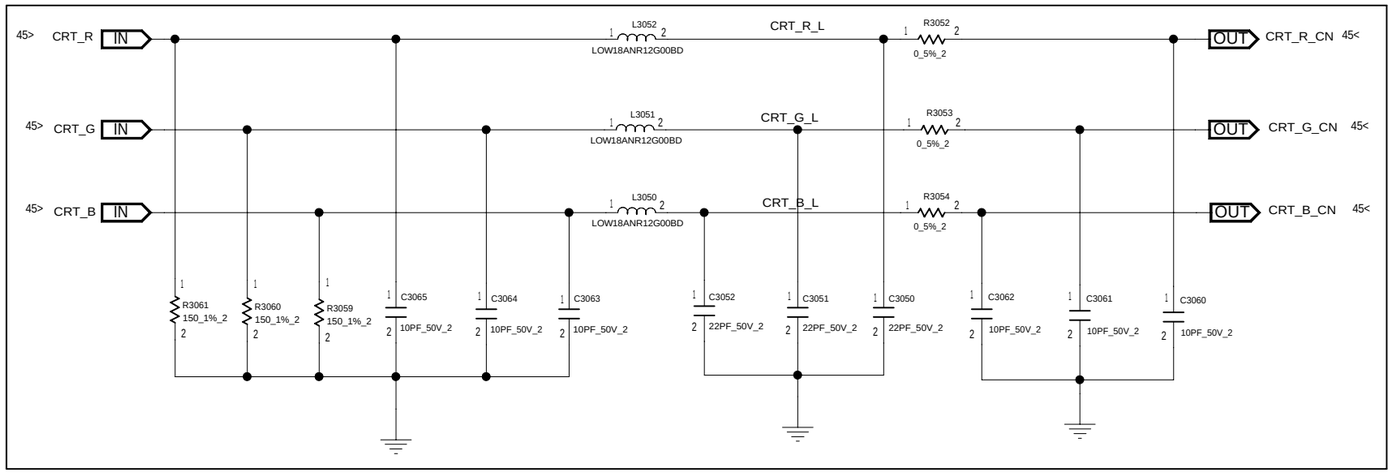
TITLE: EVEREST-M LCM CONN

SIZE	CODE	DOC NUMBER	REV
C	CS	CS_13GMXXXXXX-MTR	A01

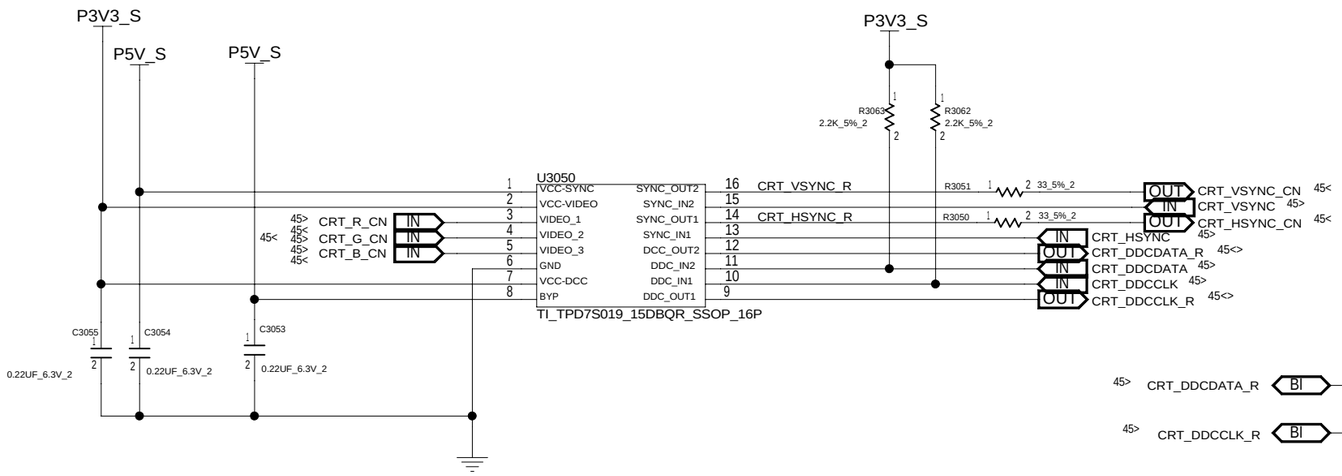
CHANGE By Date: DATE: SHEET

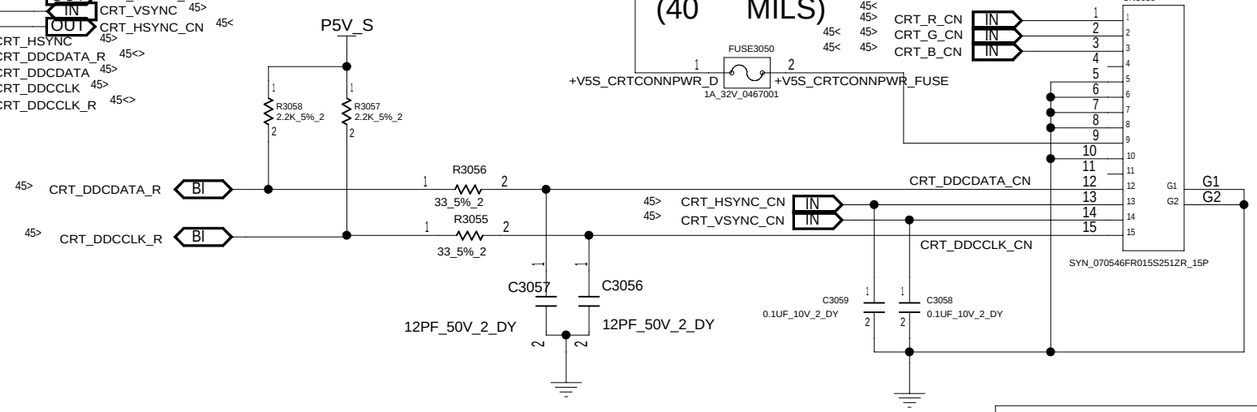


CO-LAYOUT



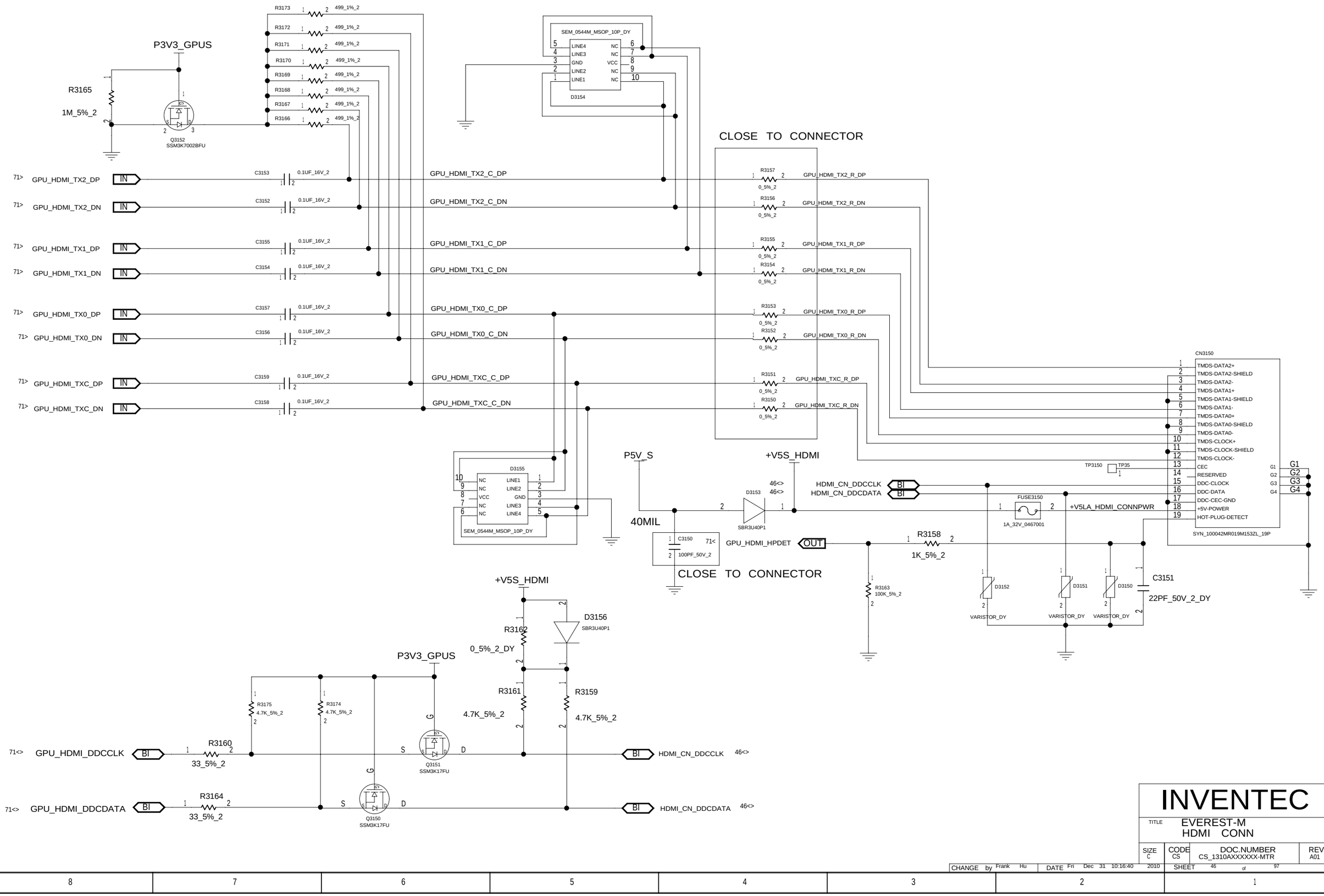
FOLLOW INTEL DESIGN GUIDE





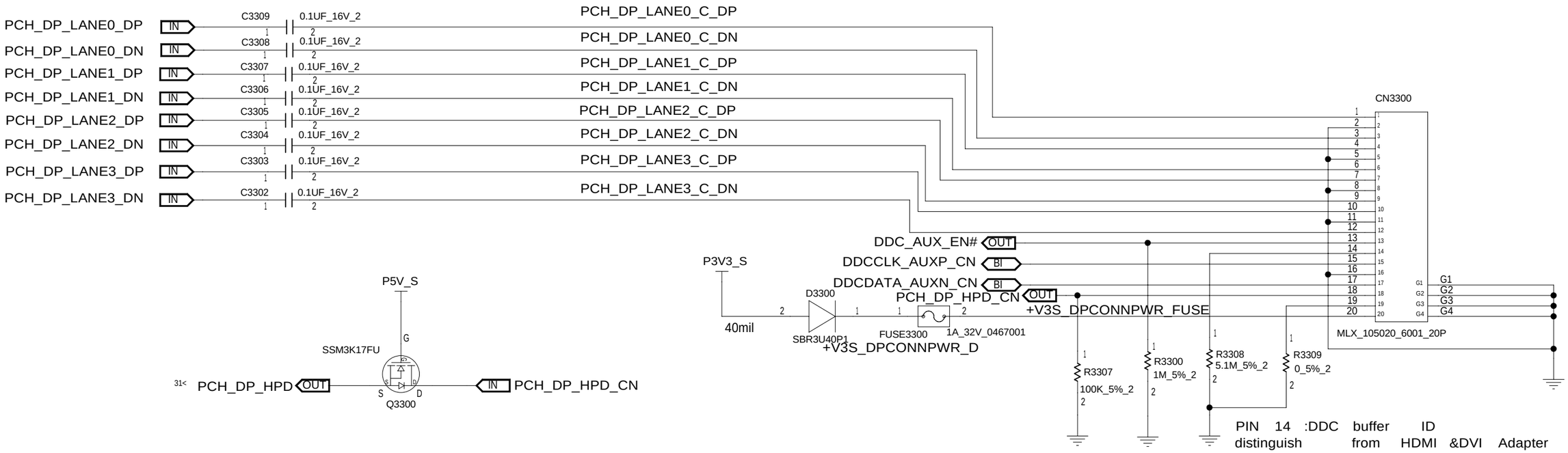
INVENTEC

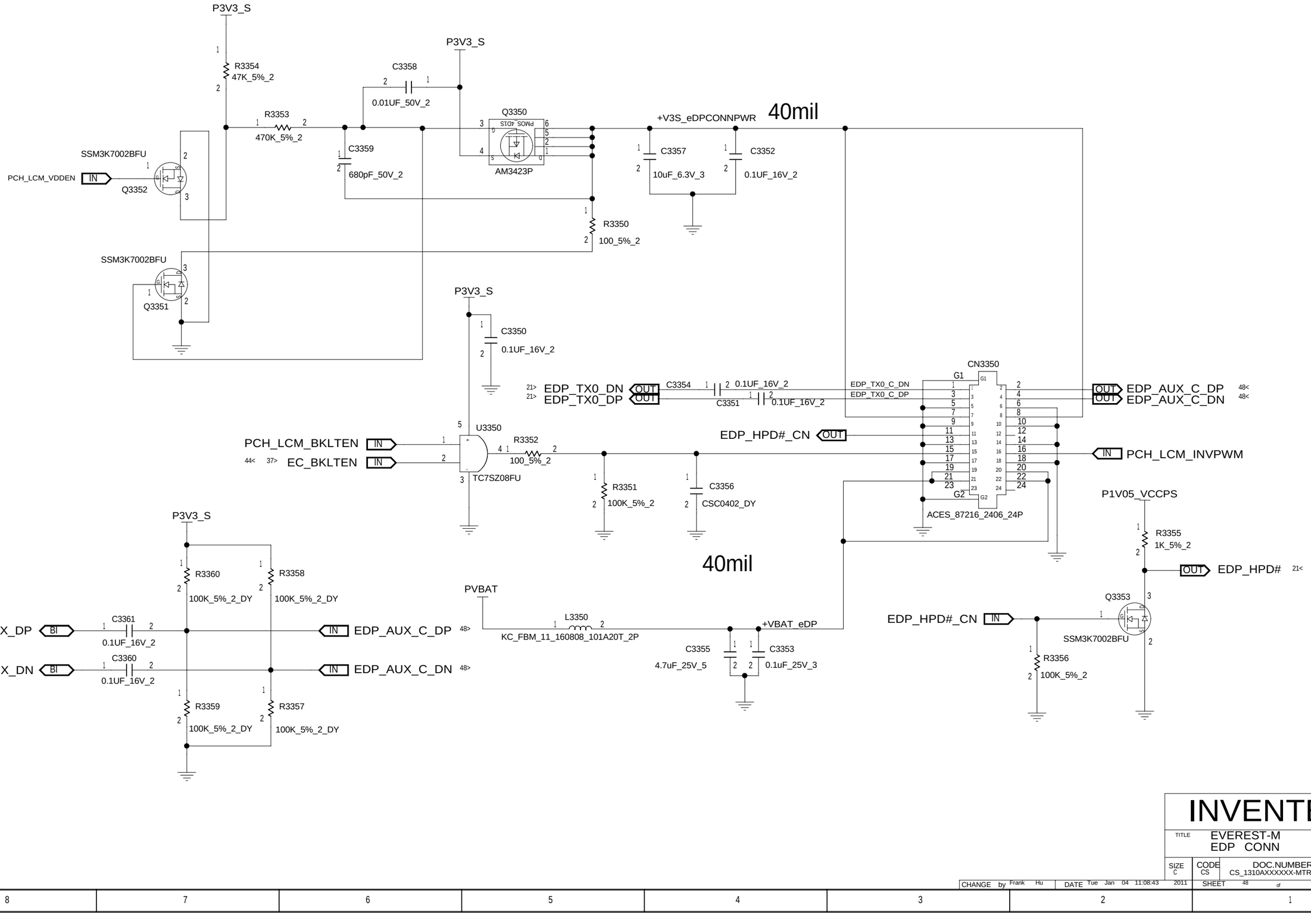
TITLE	EVEREST-M CRT CONN		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:17:01 2010	SHEET 45 of 97	



INVENTEC

TITLE	EVEREST-M HDMI CONN		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:16:40 2010	SHEET 46 of 97	

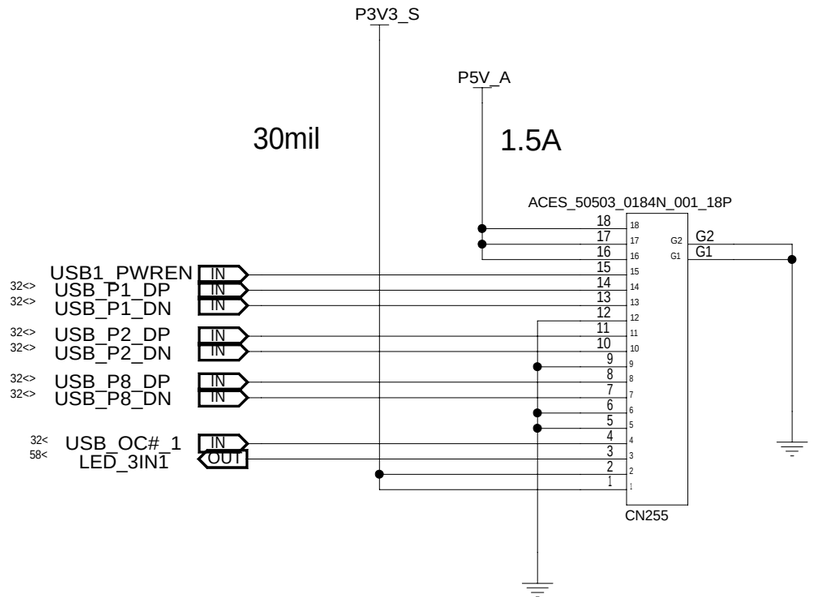

PCH_DP_LANE0_DP
PCH_DP_LANE0_DN
PCH_DP_LANE1_DP
PCH_DP_LANE1_DN
PCH_DP_LANE2_DP
PCH_DP_LANE2_DN
PCH_DP_LANE3_DP
PCH_DP_LANE3_DN
C3309 C3308 C3307 C3306 C3305 C3304 C3303 C3302
0.1UF_16V_2
PCH_DP_LANE0_C_DP
PCH_DP_LANE0_C_DN
PCH_DP_LANE1_C_DP
PCH_DP_LANE1_C_DN
PCH_DP_LANE2_C_DP
PCH_DP_LANE2_C_DN
PCH_DP_LANE3_C_DP
PCH_DP_LANE3_C_DN
CN3300
MLX_105020_6001_20P
DDC_AUX_EN#
DDCCLK_AUXP_CN
DDCDATA_AUXN_CN
PCH_DP_HPD_CN
+V3S_DPCONNPWR_FUSE
P3V3_S
40mil
D3300
SBR3U40P1
+V3S_DPCONNPWR_D
FUSE3300
1A_32V_0467001
R3307 100K_5%_2
R3300 1M_5%_2
R3308 5.1M_5%_2
R3309 0_5%_2
PIN 14 :DDC buffer ID distinguish from HDMI &DVI Adapter
P5V_S
SSM3K17FU
Q3300
PCH_DP_HPD
PCH_DP_AUX_DP
PCH_DP_AUX_C_DP
C3301
Q3301
PCH_DP_AUX_M_DP
Q3307
PCH_DP_AUX_DN
PCH_DP_AUX_C_DN
C3300
Q3310
PCH_DP_AUX_M_DN
Q3306
R3301 2.2K_5%_2
PCH_DUAL_DDCCLK
Q3309
PCH_DUAL_DDCCLK_M
Q3305
R3303 100K_5%_2
R3304 2.2K_5%_2
PCH_DUAL_DDCDATA
Q3308
PCH_DUAL_DDCDATA_M
Q3304
R3302 100K_5%_2
R3306 10K_5%_2
R3305 10K_5%_2
Q3303
Q3302
SSM3K7002BFU
PCH Dual-mode
INVENTEC
TITLE EVEREST-M DP CONN
SIZE C
CODE CS
DOC.NUMBER CS_1310AXXXXXX-MTR
REV A01
CHANGE by Frank Hu
DATE Fri Dec 31 10:16:41 2010
SHEET 47 of 97



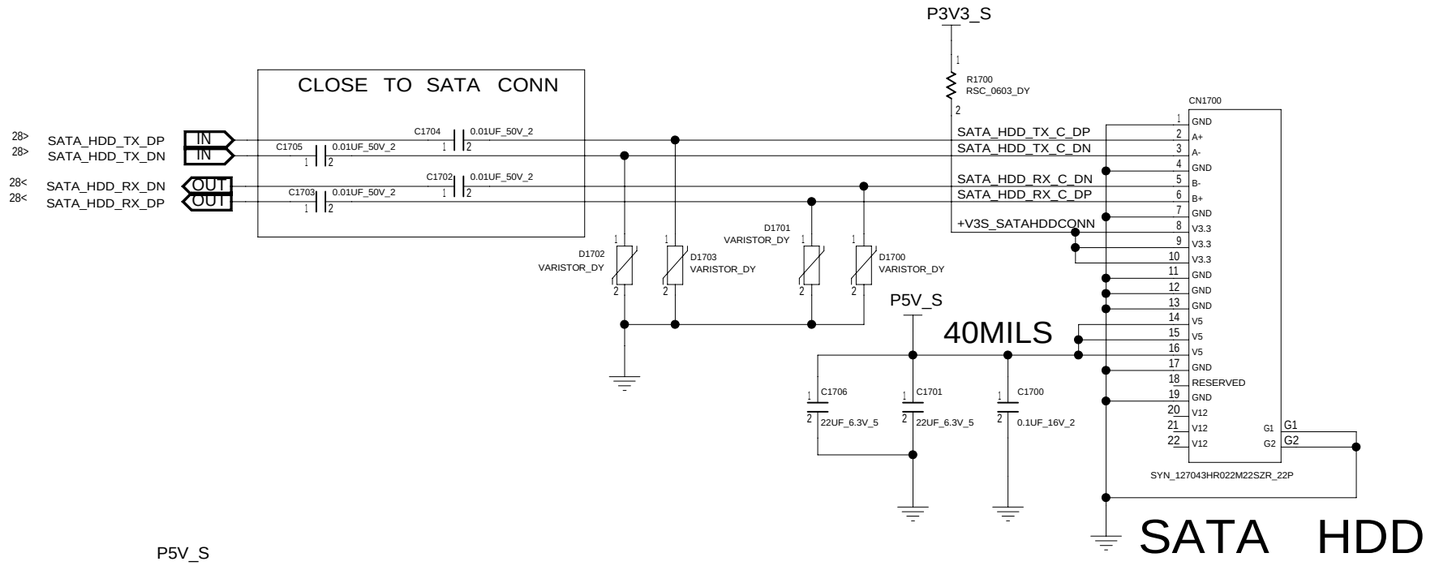
INVENTEC

TITLE	EVEREST-M EDP CONN			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR		REV A01
CHANGE by Frank Hu	DATE Tue Jan 04 11:08:43 2011	SHEET 48 of 97		

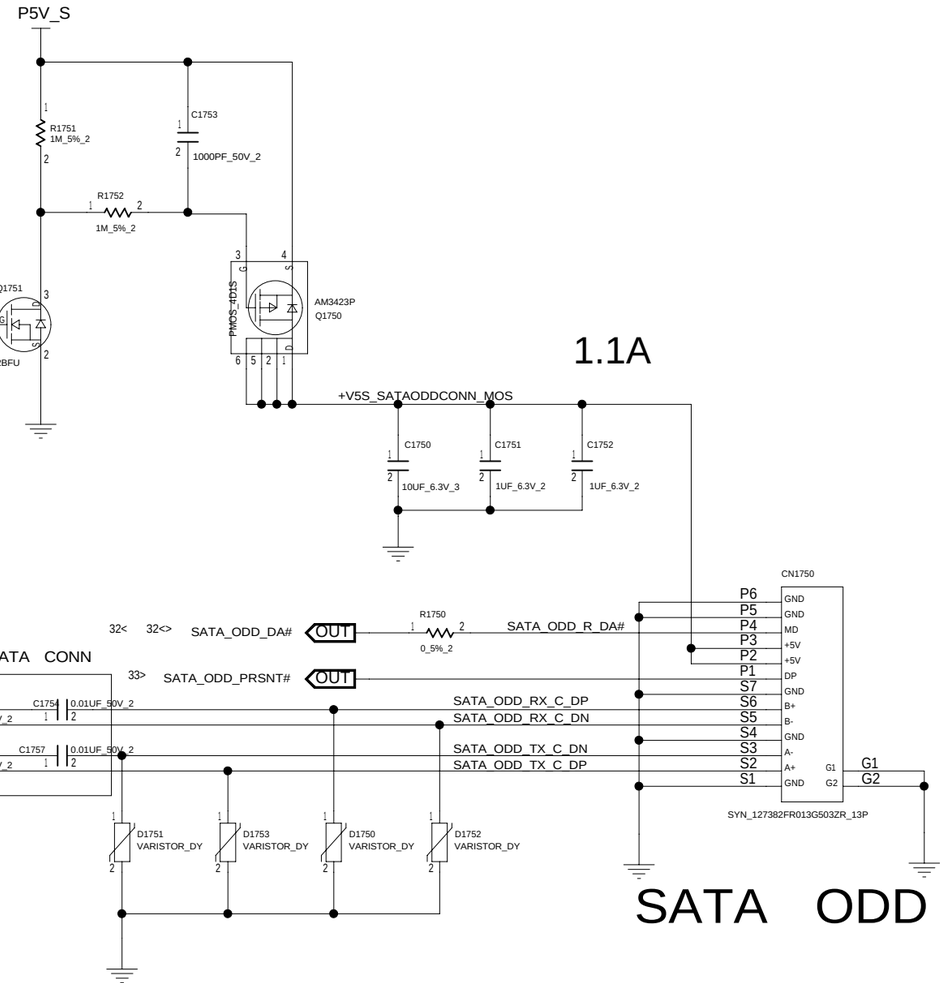
CARDREADER/USB CONNECTOR



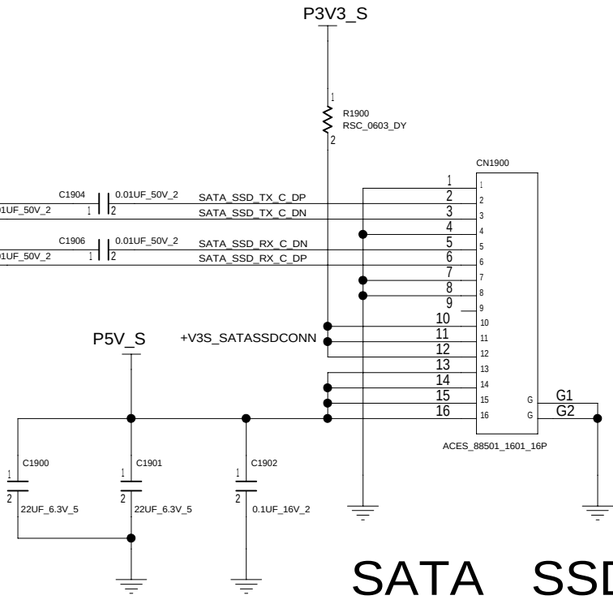
INVENTEC			
TITLE	EVEREST-M DB CONN USB & CARDREADER		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:17:02 2010	SHEET 49 of 97	



SATA HDD



SATA ODD

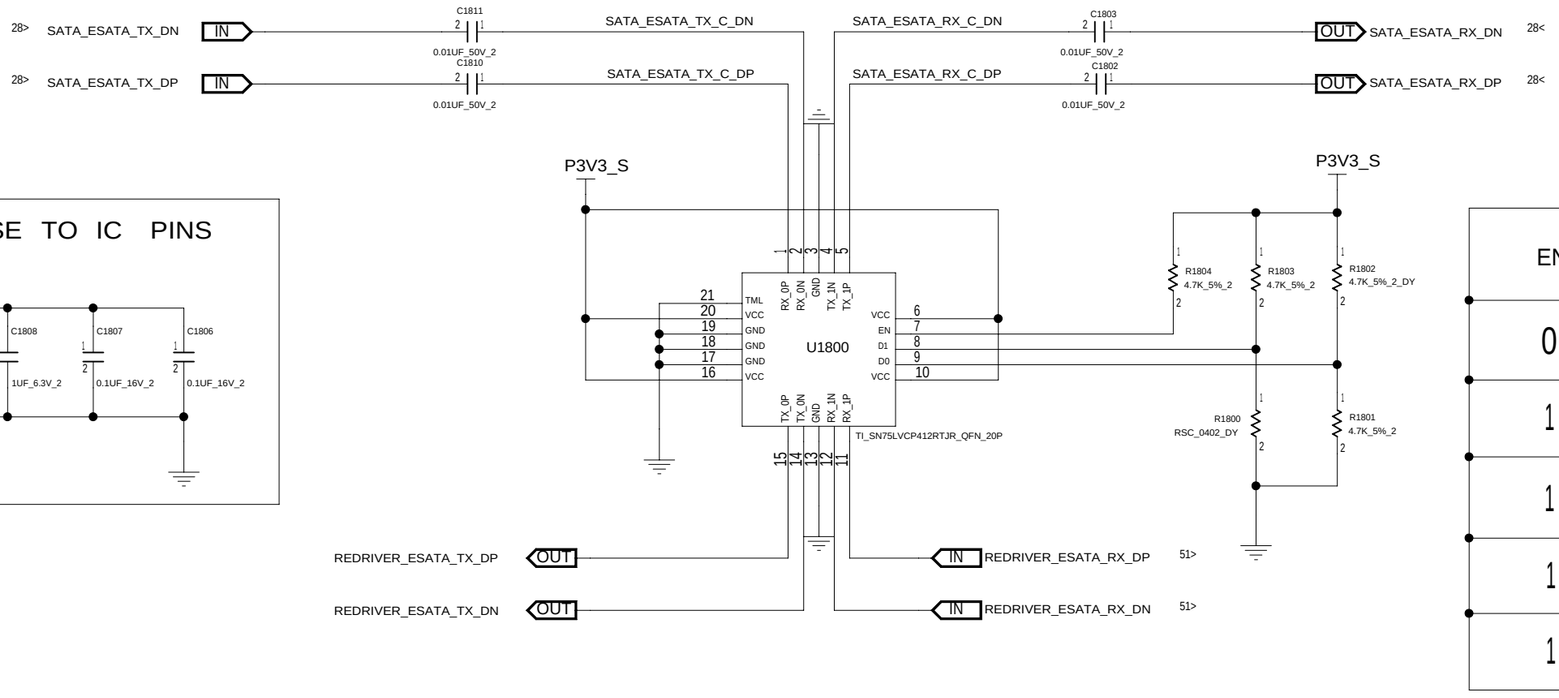


SATA SSD

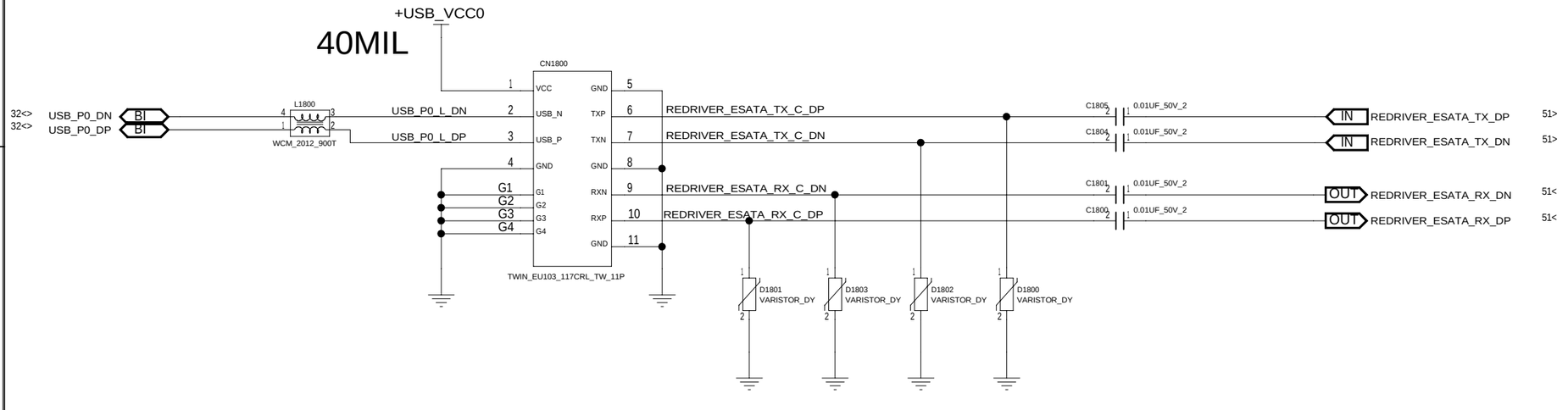
INVENTEC

TITLE	EVEREST-M SATA HDD/SSD & ODD CONN		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Sun Jan 02 18:54:06 2011	SHEET 50 of 97	

E-SATA

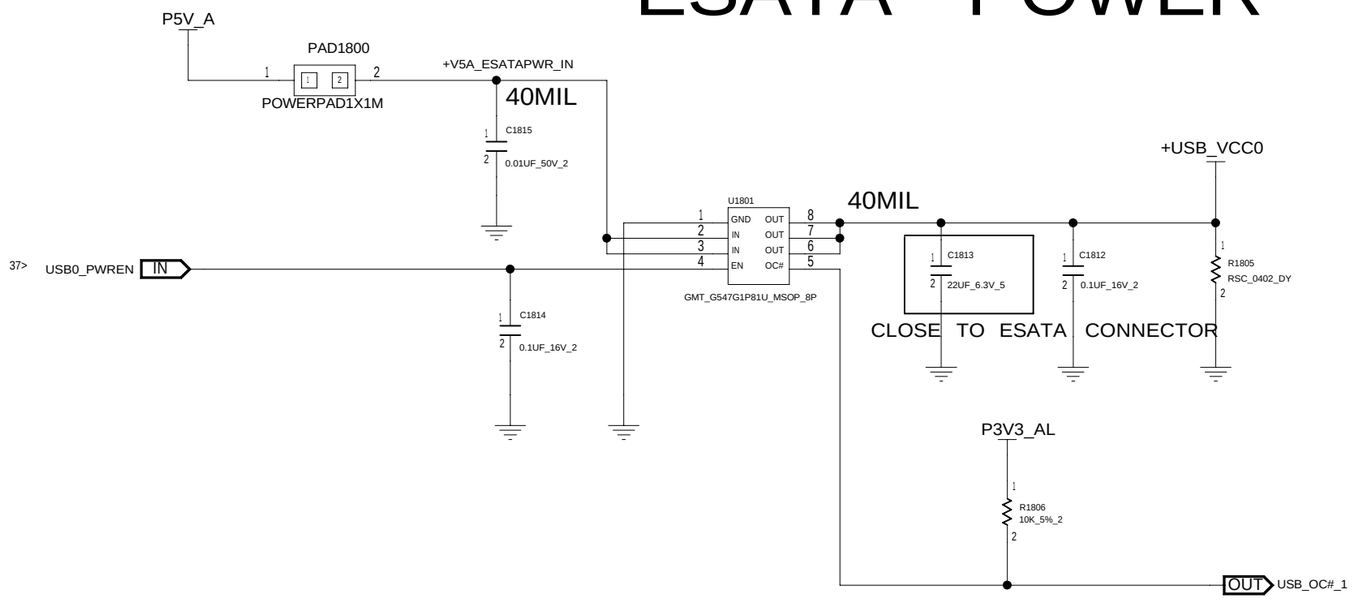


EN	D0	D1	FUNCTION
0	X	X	STANDBY
1	0	0	DEFAULT
1	1	0	CH0->5DB
1	0	1	CH1->5DB
1	1	1	CH0,1->5DB



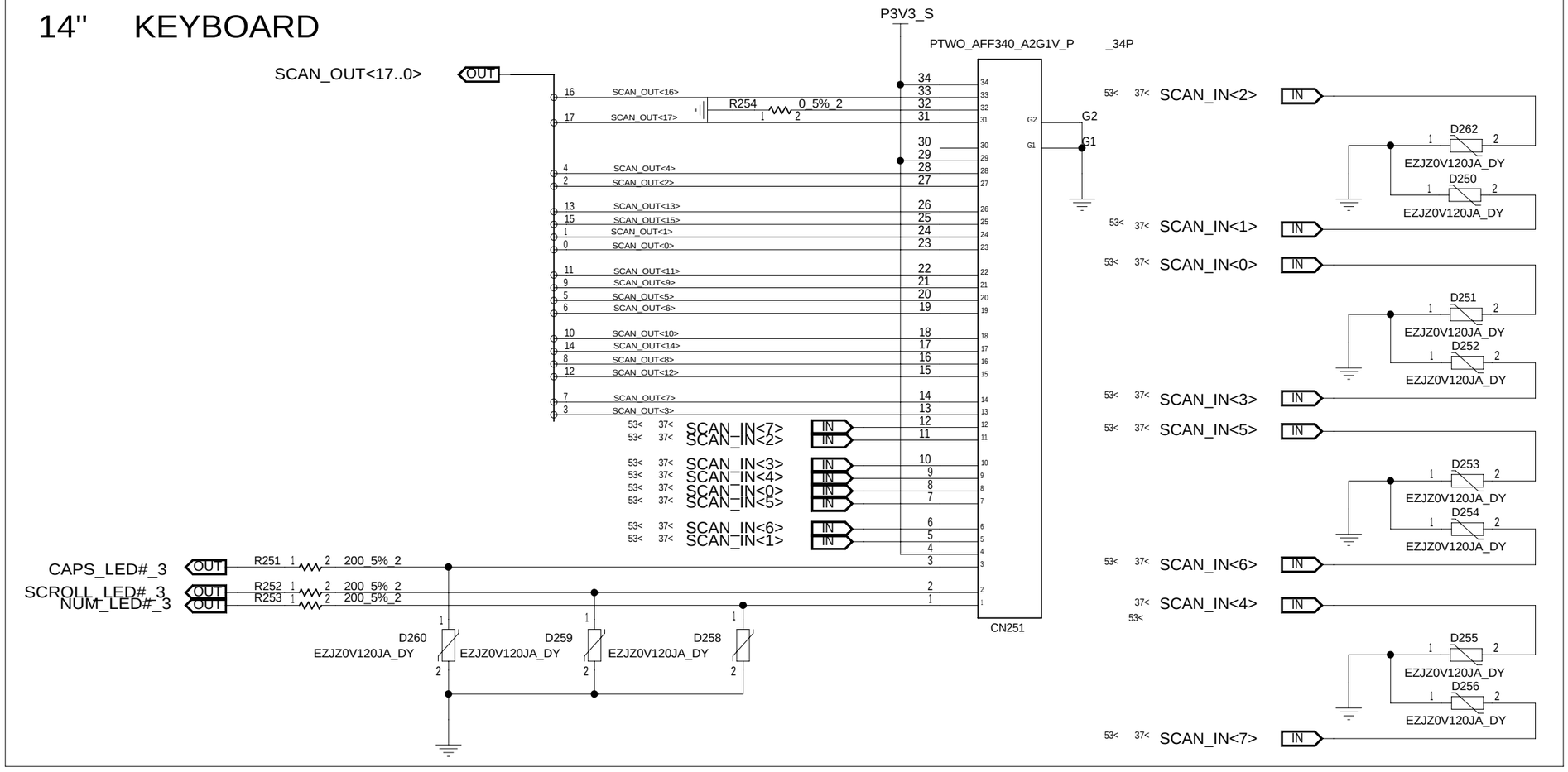
INVENTEC			
TITLE	EVEREST-M E-SATA CONN		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:16:42 2010	SHEET 51 of 97	

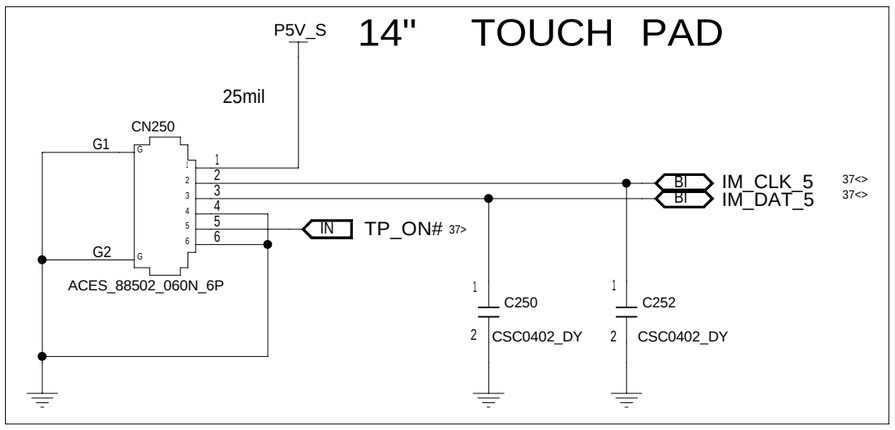
ESATA POWER

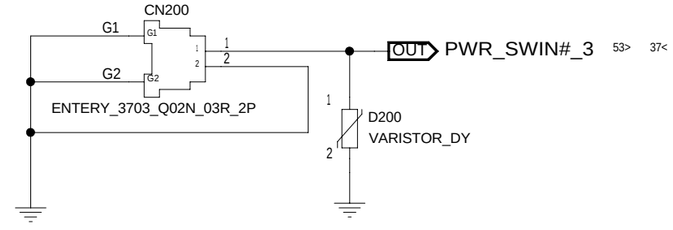


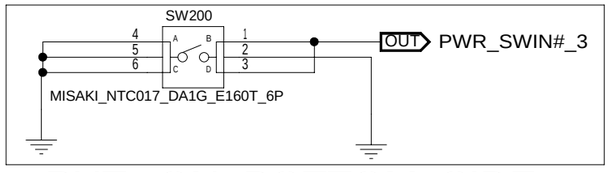
INVENTEC			
TITLE	EVEREST-M USB CONN		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Sun Jan 02 18:04:58 2011	SHEET 52 of 97	

14" KEYBOARD







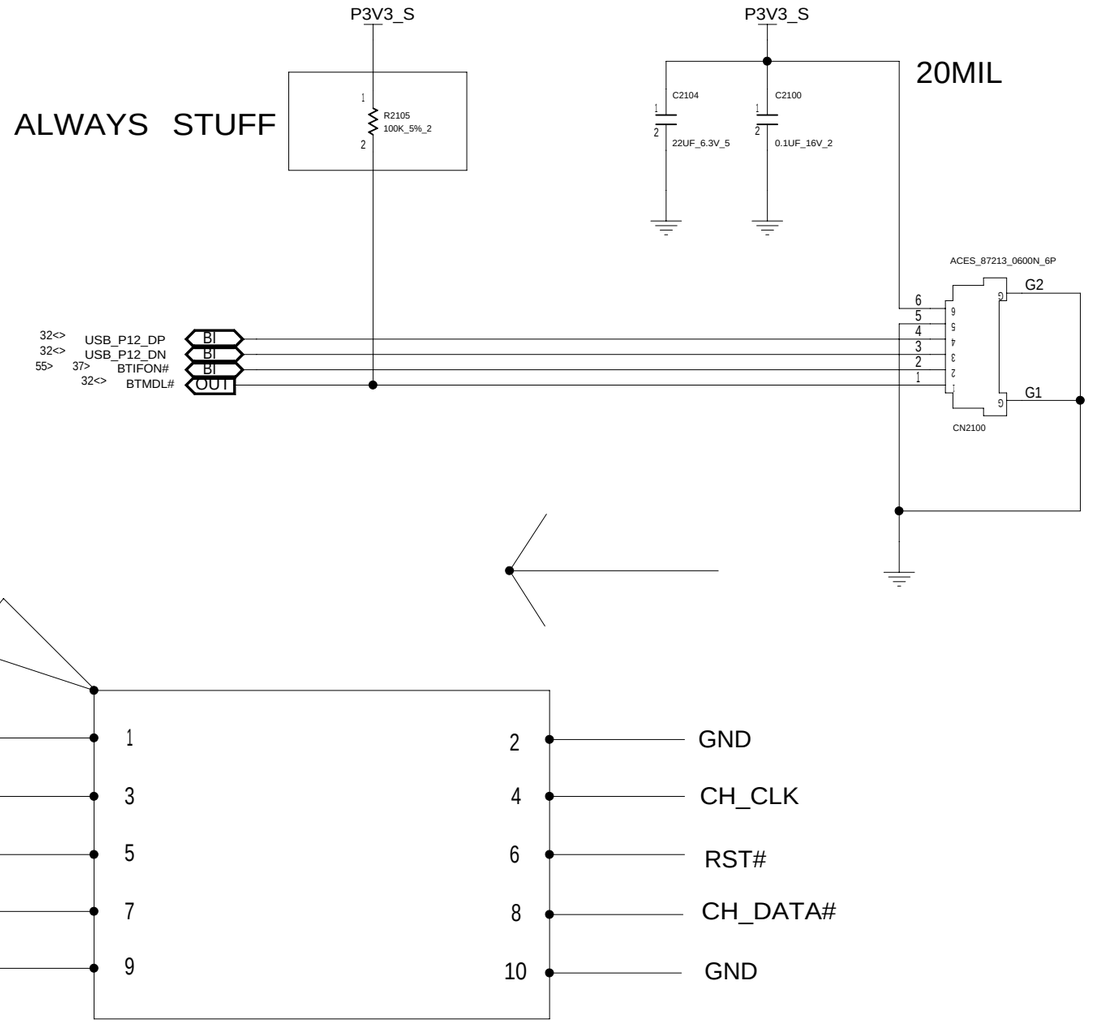


PUT ON BOTTOM SIDE

INVENTEC

TITLE	EVEREST-M K/B & TP/B CONN		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:16:43 2010	SHEET 53 of 97	

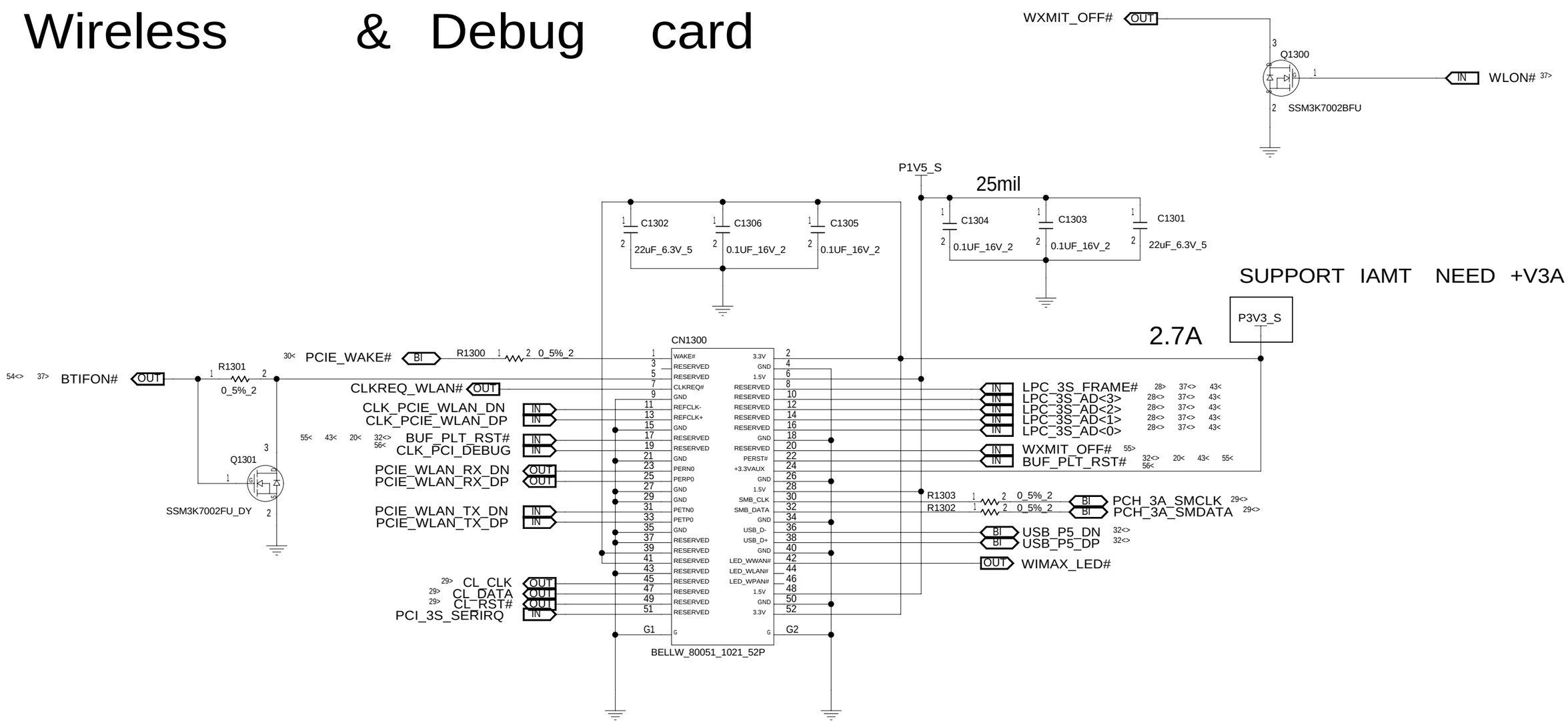
BLUETOOTH



INVENTEC

TITLE	EVEREST-M BLUETOOTH CONN		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:17:02 2010	SHEET 54 of 97	

Wireless & Debug card



MINI CARD 1

Note:	Peak(max)mA	Normal(max)mA
3.3V	2,750mA	1,100mA
1.5V	500mA	375mA

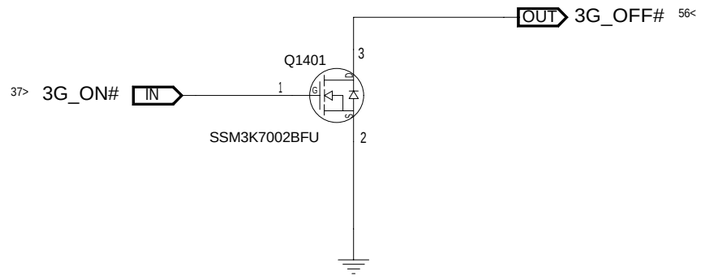
INVENTEC

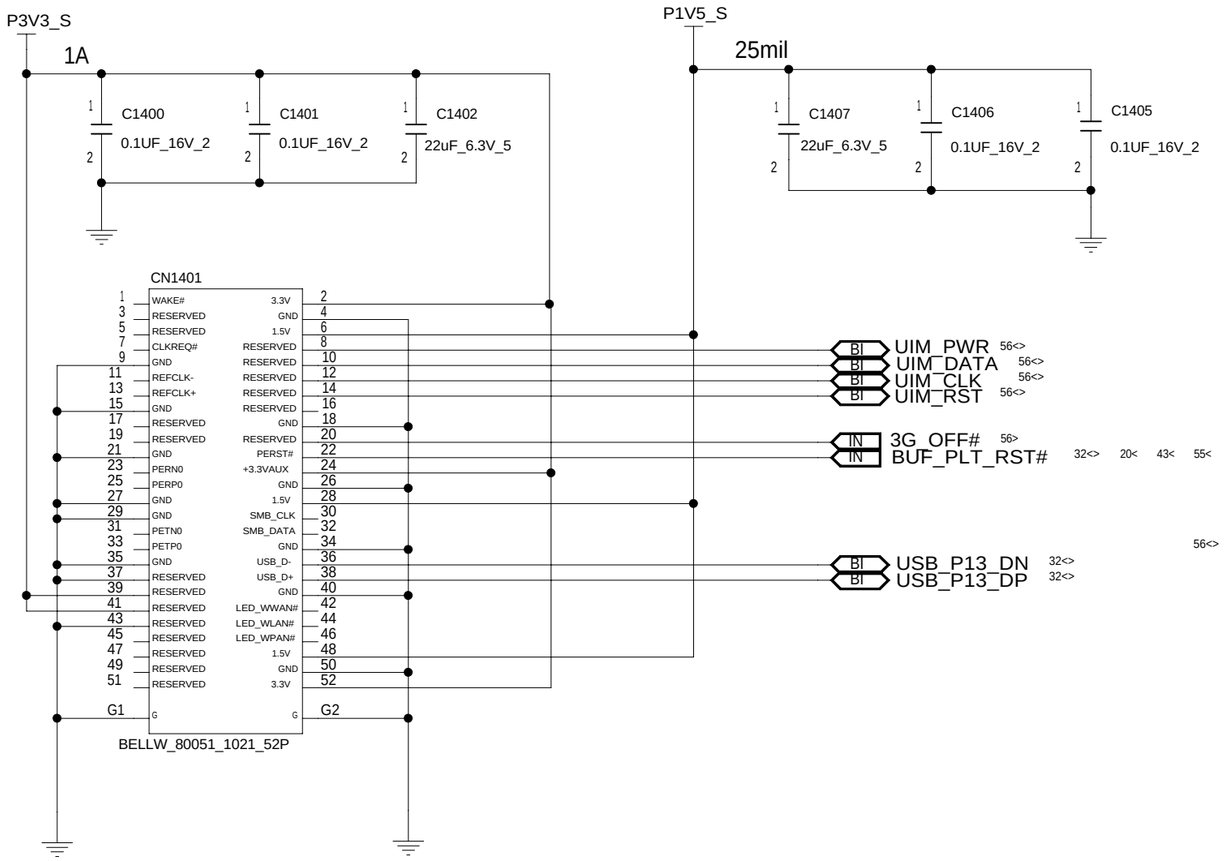
TITLE EVEREST-M
MINI1 WLAN/DEBUG CARD

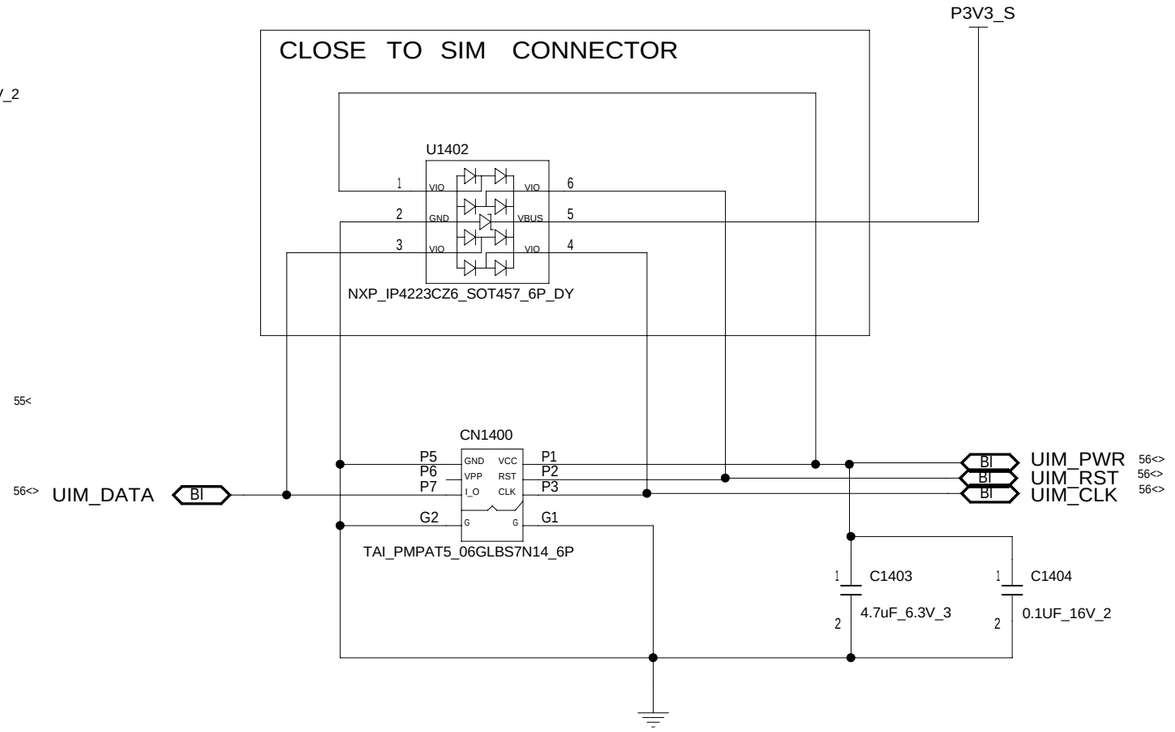
SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

CHANGE by Frank Hu DATE Fri Dec 31 10:16:43 2010 SHEET 55 of 97

3G/GPS



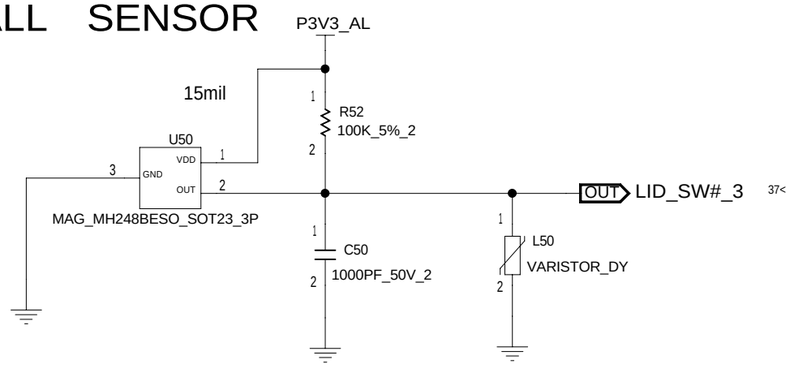




MINI CARD 2

INVENTEC			
TITLE	EVEREST-M MINI2 3G		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:17:03 2010	SHEET 56 of 97	

HALL SENSOR

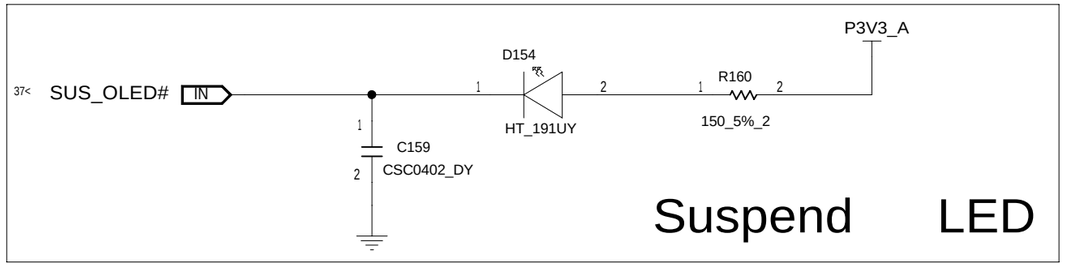


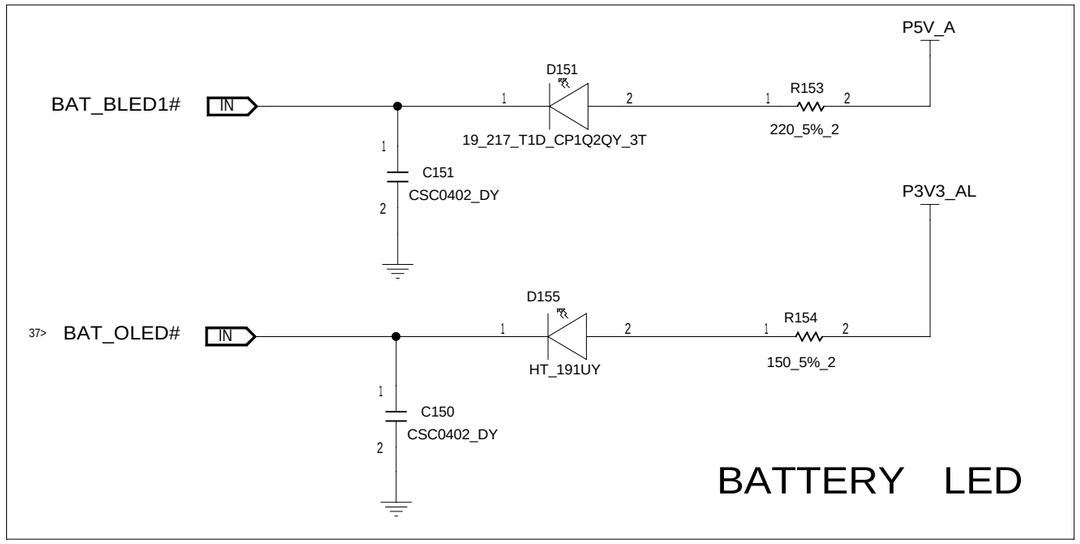
INVENTEC

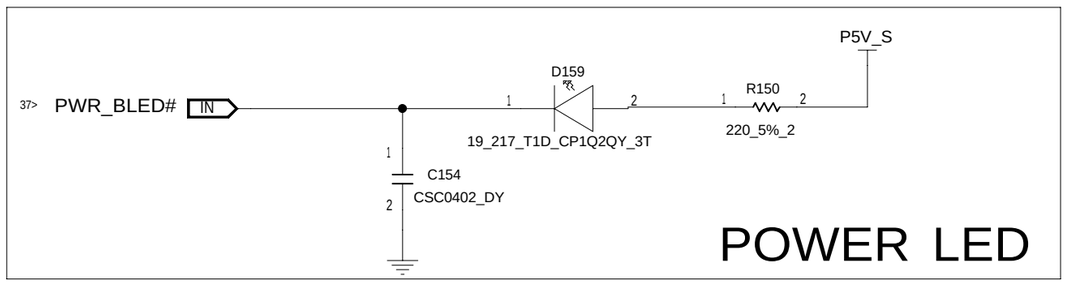
TITLE EVEREST-M
HALL SENSOR

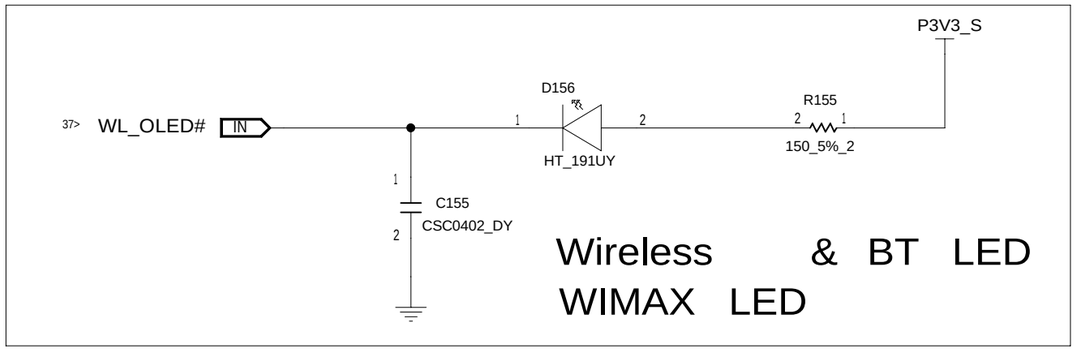
SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

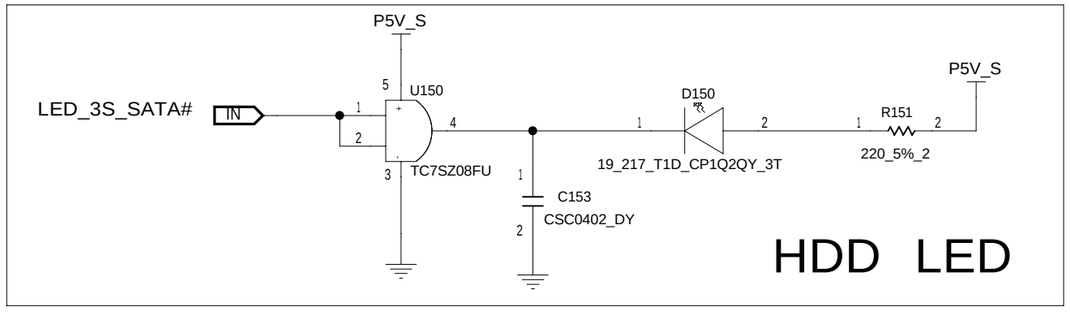
CHANGE by Frank Hu DATE Fri Dec 31 10:17:03 2010 SHEET 57 of 97

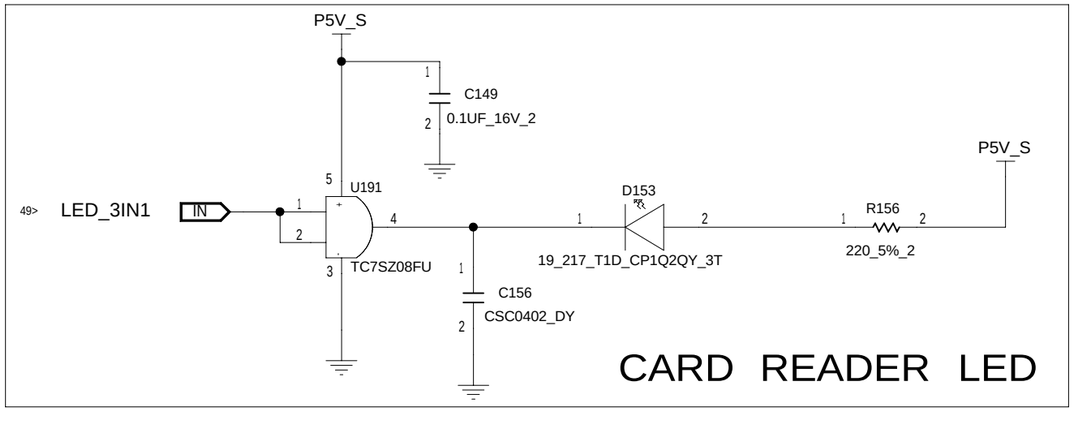


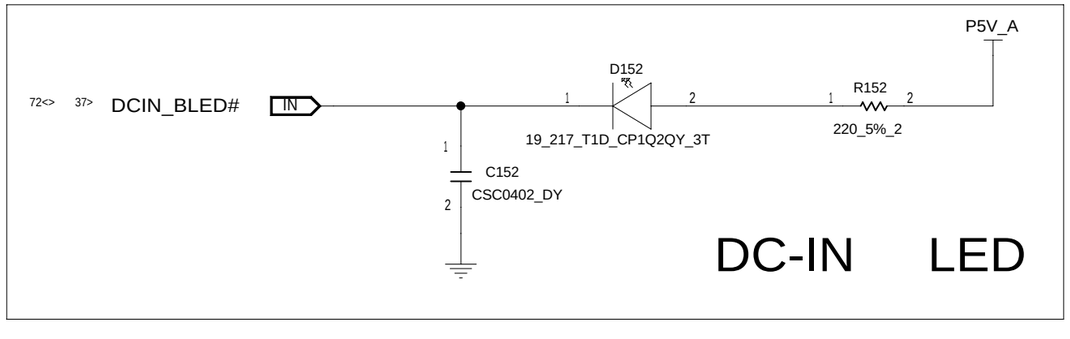






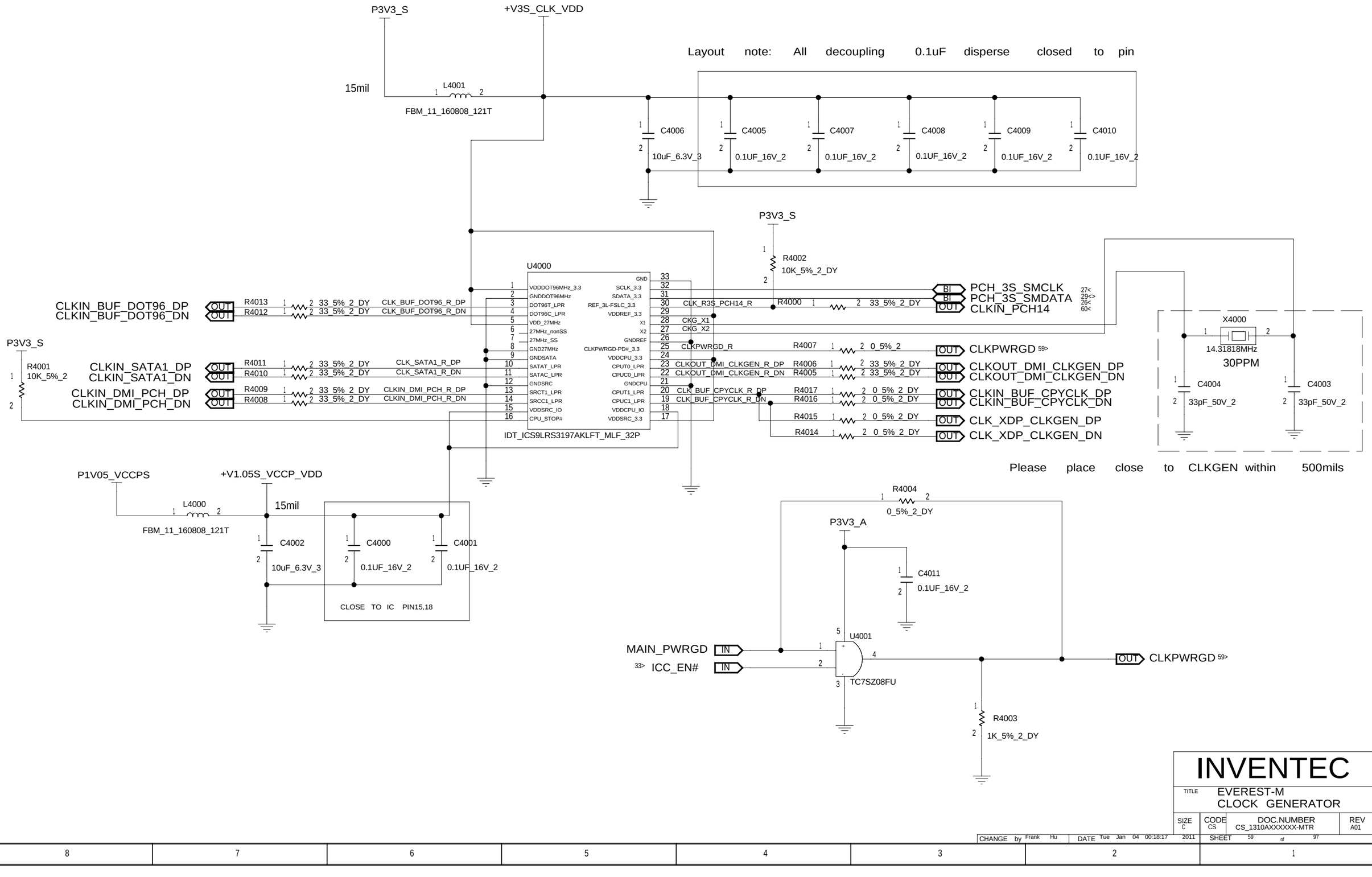






INVENTEC

TITLE	EVEREST-M LED		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:16:44 2010	SHEET 58 of 97	


P3V3_S
+V3S_CLK_VDD
15mil
L4001
FBM_11_160808_121T
Layout note: All decoupling 0.1uF disperse closed to pin
C4006
10uF_6.3V_3
C4005
C4007
C4008
C4009
C4010
0.1UF_16V_2
P3V3_S
R4002
10K_5%_2_DY
U4000
IDT_ICS9LRS3197AKLFT_MLF_32P
CLKIN_BUF_DOT96_DP
CLKIN_BUF_DOT96_DN
R4013
R4012
33_5%_2_DY
CLK_BUF_DOT96_R_DP
CLK_BUF_DOT96_R_DN
CLKIN_SATA1_DP
CLKIN_SATA1_DN
R4011
R4010
CLK_SATA1_R_DP
CLK_SATA1_R_DN
CLKIN_DMI_PCH_DP
CLKIN_DMI_PCH_DN
R4009
R4008
CLKIN_DMI_PCH_R_DP
CLKIN_DMI_PCH_R_DN
R4001
10K_5%_2
CLK_R3S_PCH14_R
R4000
PCH_3S_SMCLK
PCH_3S_SMDATA
CLKIN_PCH14
CKG_X1
CKG_X2
CLKPWRGD_R
R4007
0_5%_2
CLKPWRGD
CLKOUT_DMI_CLKGEN_R_DP
CLKOUT_DMI_CLKGEN_R_DN
R4006
R4005
CLKOUT_DMI_CLKGEN_DP
CLKOUT_DMI_CLKGEN_DN
CLK_BUF_CPYCLK_R_DP
CLK_BUF_CPYCLK_R_DN
R4017
R4016
CLKIN_BUF_CPYCLK_DP
CLKIN_BUF_CPYCLK_DN
R4015
R4014
CLK_XDP_CLKGEN_DP
CLK_XDP_CLKGEN_DN
X4000
14.31818MHz
30PPM
C4004
C4003
33pF_50V_2
Please place close to CLKGEN within 500mils
P1V05_VCCPS
+V1.05S_VCCP_VDD
L4000
FBM_11_160808_121T
15mil
C4002
C4000
C4001
10uF_6.3V_3
0.1UF_16V_2
CLOSE TO IC PIN15,18
R4004
0_5%_2_DY
P3V3_A
C4011
MAIN_PWRGD
ICC_EN#
U4001
TC7SZ08FU
R4003
1K_5%_2_DY
INVENTEC
TITLE
EVEREST-M
CLOCK GENERATOR
SIZE C
CODE CS
DOC.NUMBER CS_1310AXXXXXX-MTR
REV A01
CHANGE by Frank Hu
DATE Tue Jan 04 00:18:17 2011
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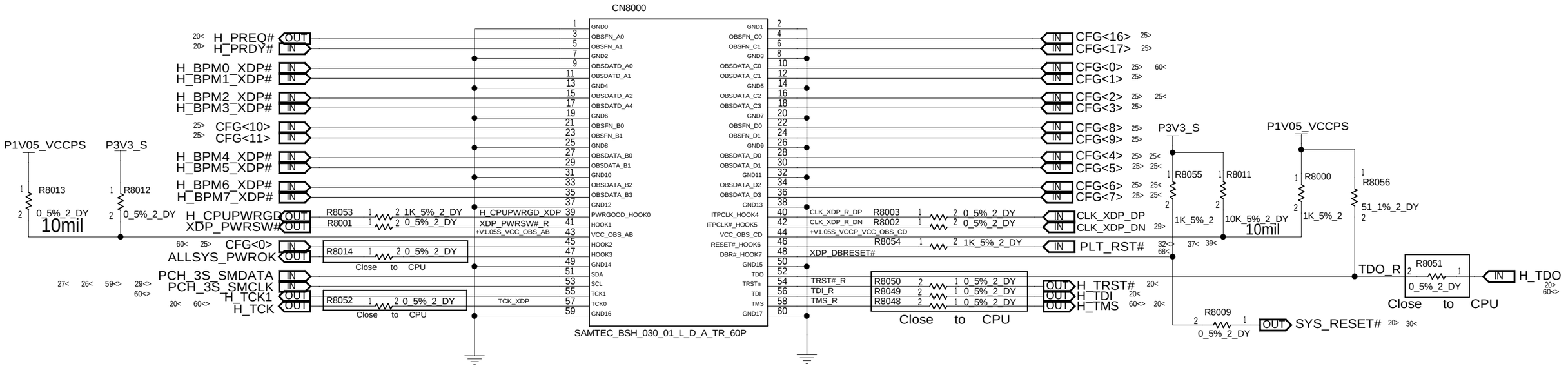
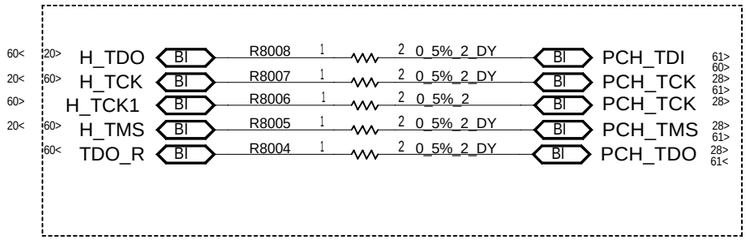
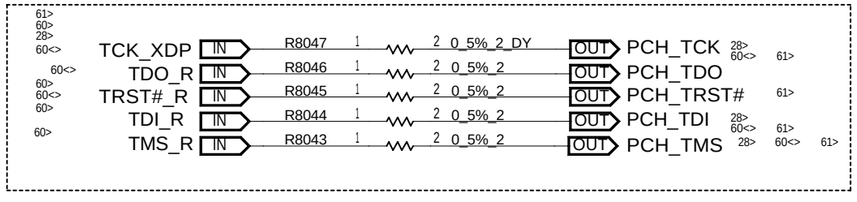


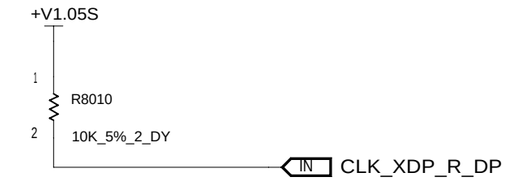
XDP CONNECTOR

SERIES

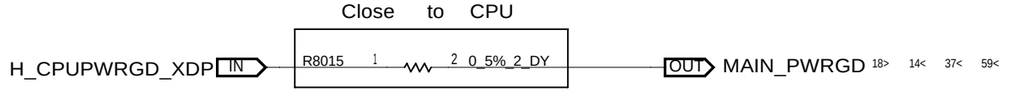


PCH ONLY

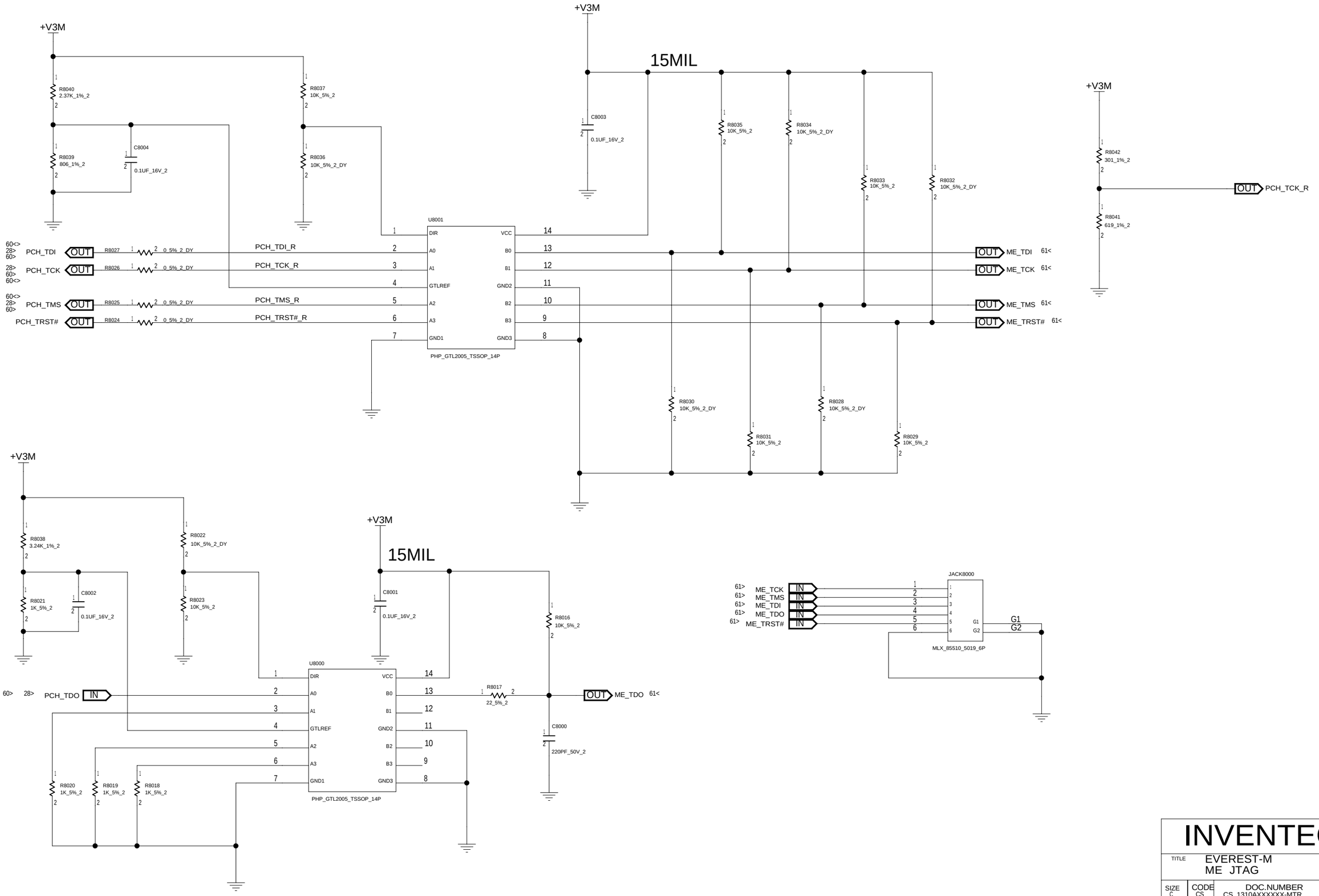




Close to CPU



INVENTEC			
TITLE	EVEREST-M XDP		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:16:45 2010	SHEET 60 of 97	



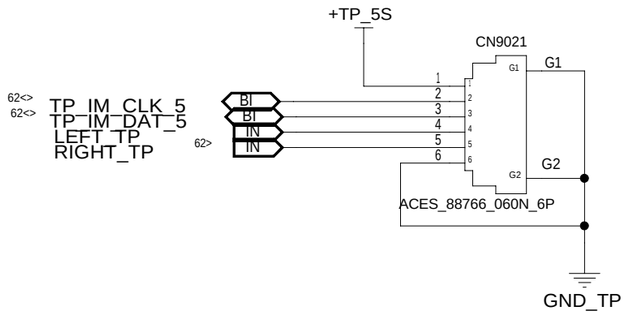
TITLE	EVEREST-M ME JTAG		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:16:46 2010	SHEET 61 of 97	

INVENTEC

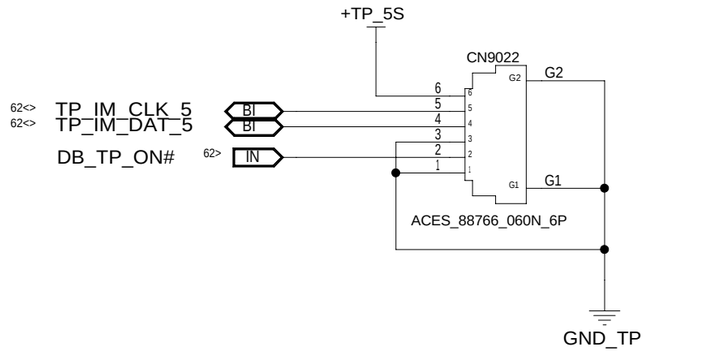
PICK BUTTON BOARD

(FOR - TOUCHPAD MODULE, TOUCHPAD SWITCH BOARD, FINGERPRINT MODULE)

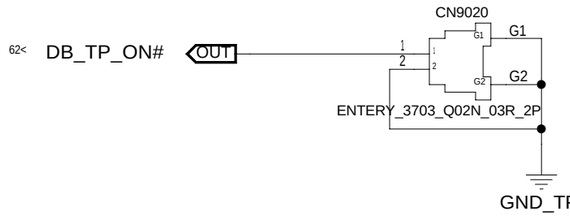
CONNECT TO TOUCHPAD MODULE

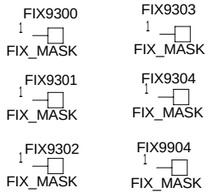


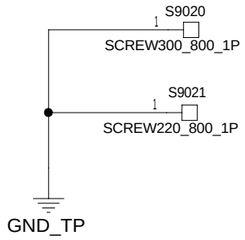
CONNECT TO MAINBOARD'S TP CONNECTOR

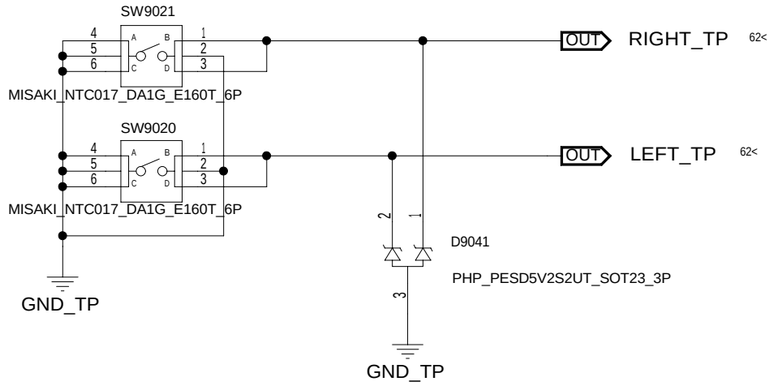


CONNECT TO TOUCHPAD SWITCH BOARD



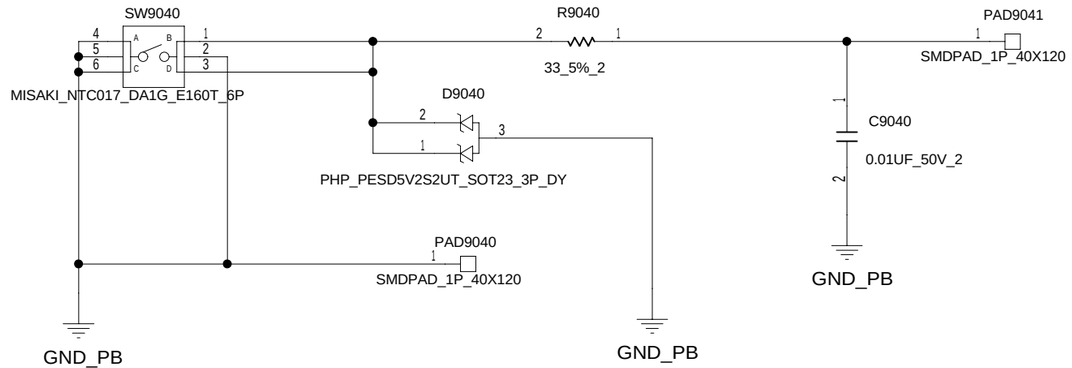


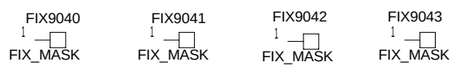


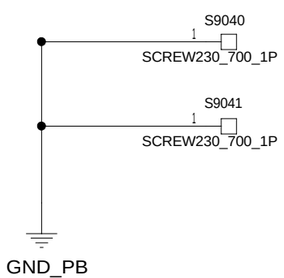


INVENTEC			
TITLE	EVEREST-M PICK BUTTON BOARD		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:17:03 2010	SHEET 62 of 97	

TOUCHPAD SWITCH BOARD



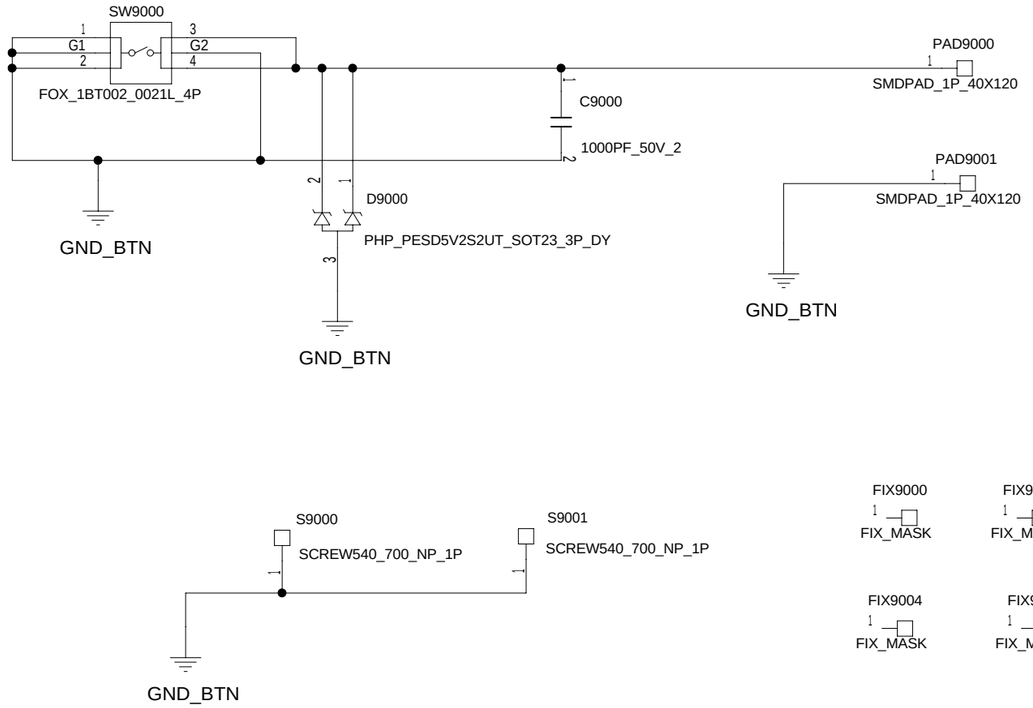




INVENTEC

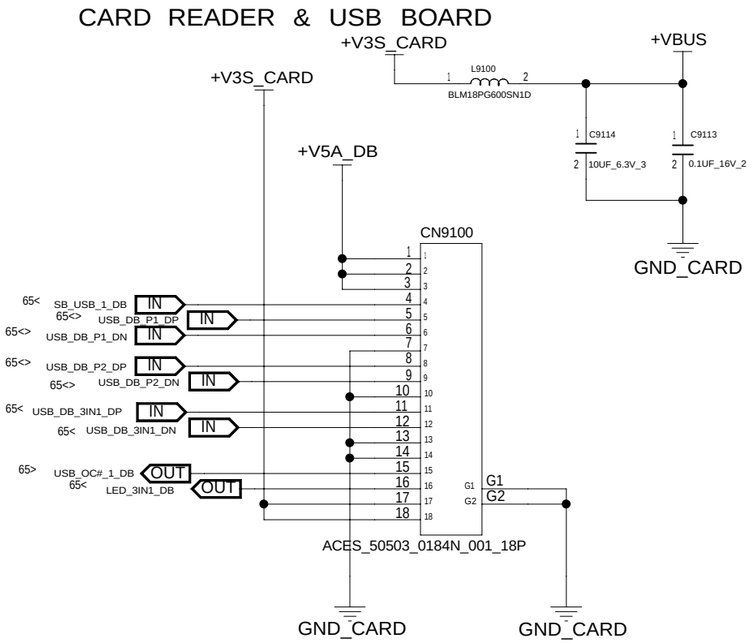
TITLE	EVEREST-M TOUCH PAD SW BOARD		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:16:46 2010	SHEET 63 of 97	

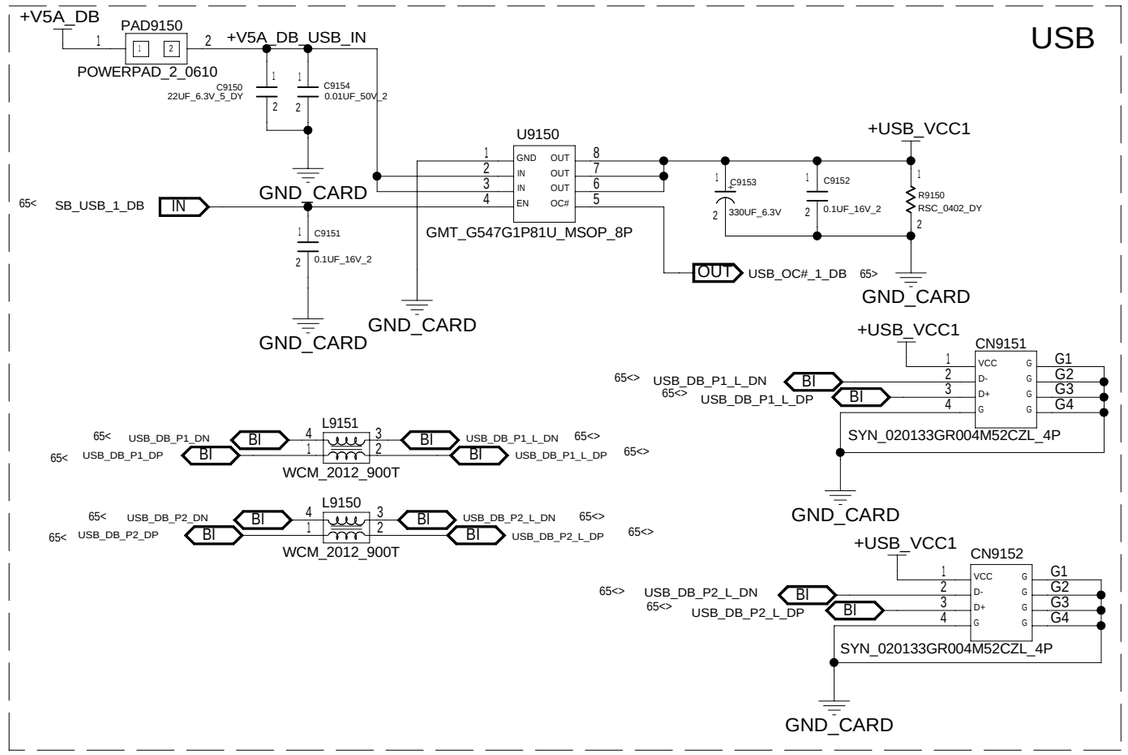
POWER BUTTON

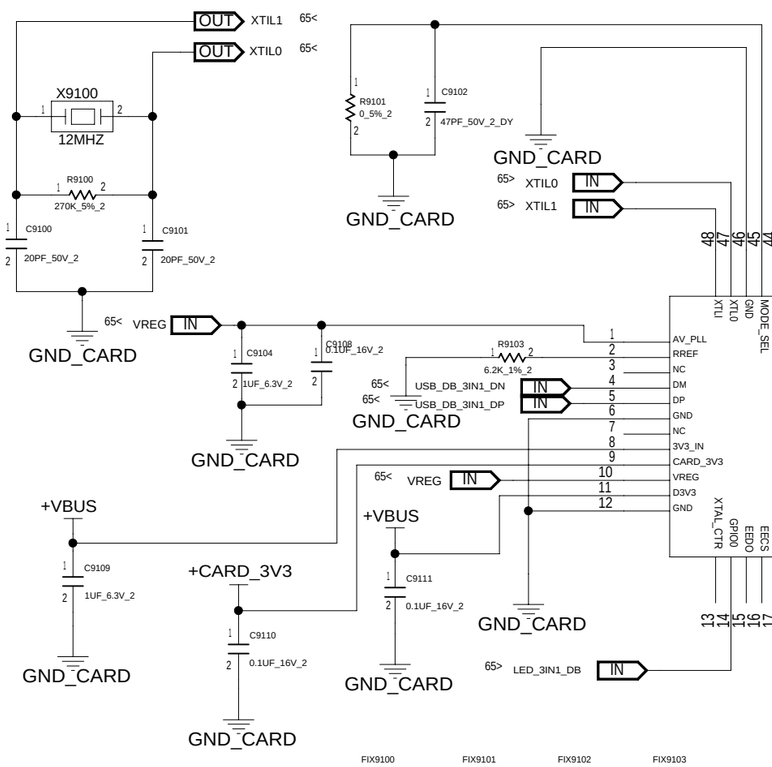


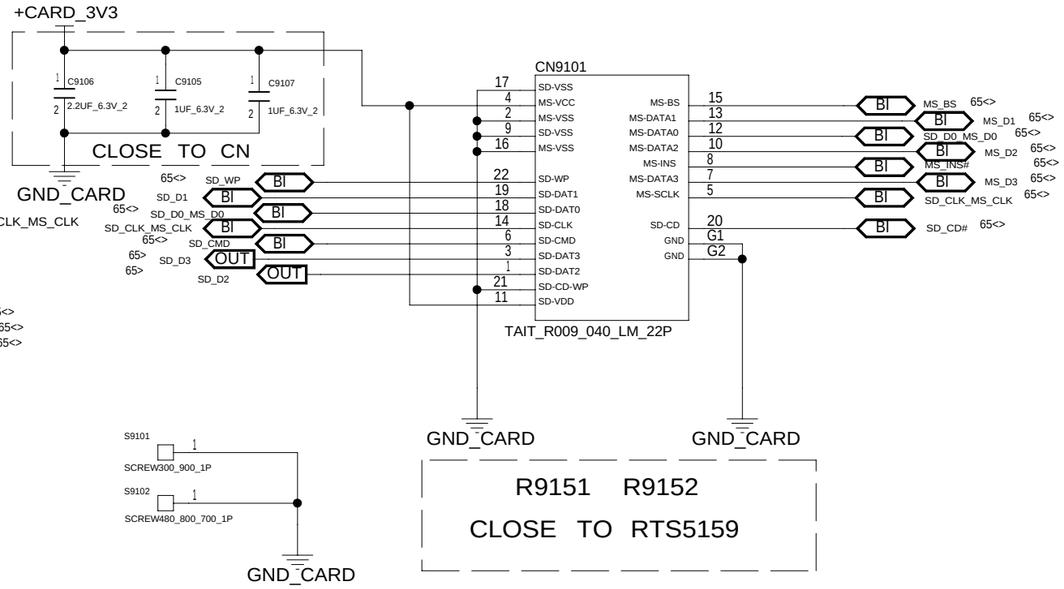
INVENTEC				
TITLE	EVEREST-M POWER BUTTON BOARD			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR		REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:16:46 2010	SHEET 64 of 97		

CARD READER & USB BOARD



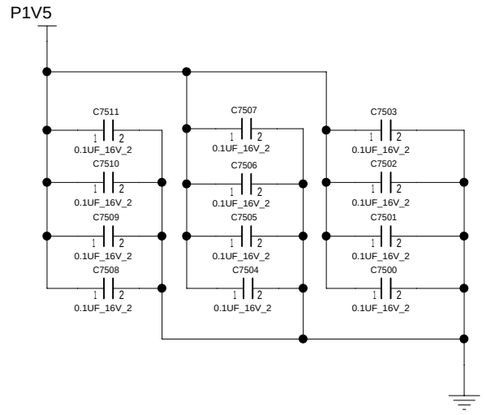






INVENTEC			
TITLE	EVEREST-M CARDREADER & USB BOARD		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:16:47 2010	SHEET 65 of 97	

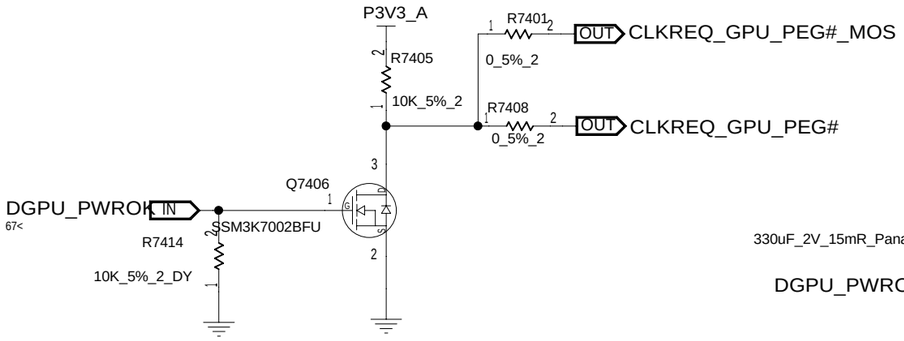
EMI

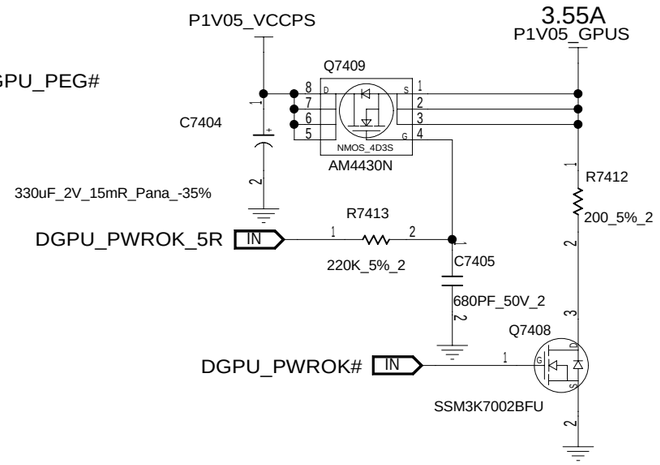


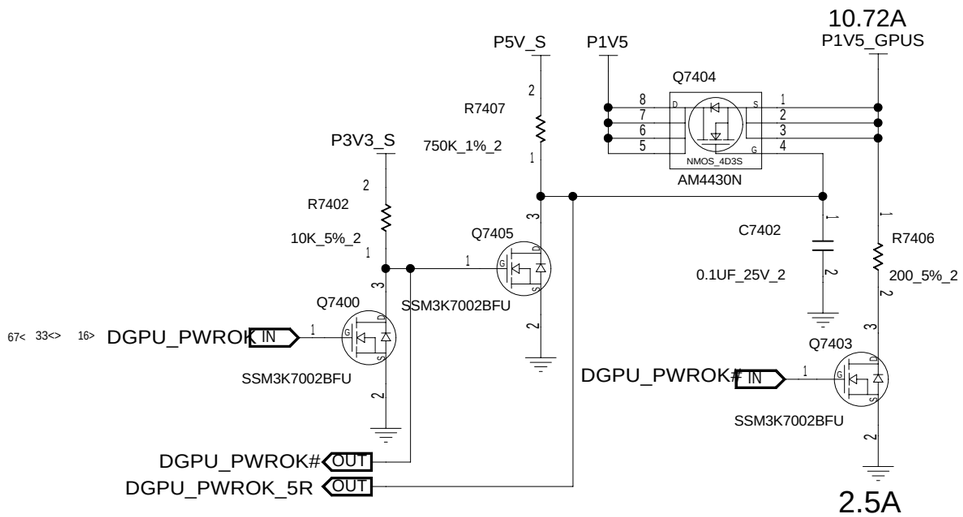
INVENTEC

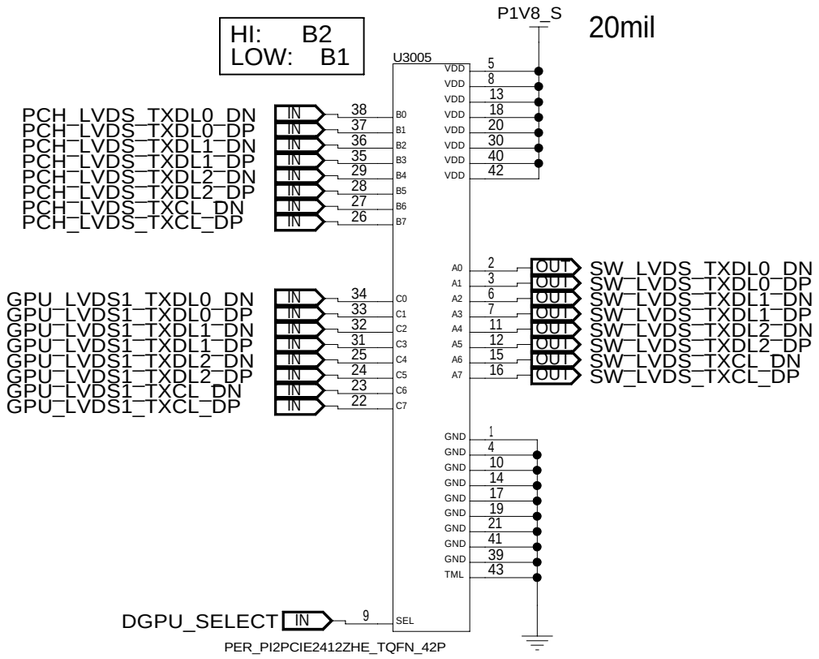
TITLE	EVEREST-M EMI		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01

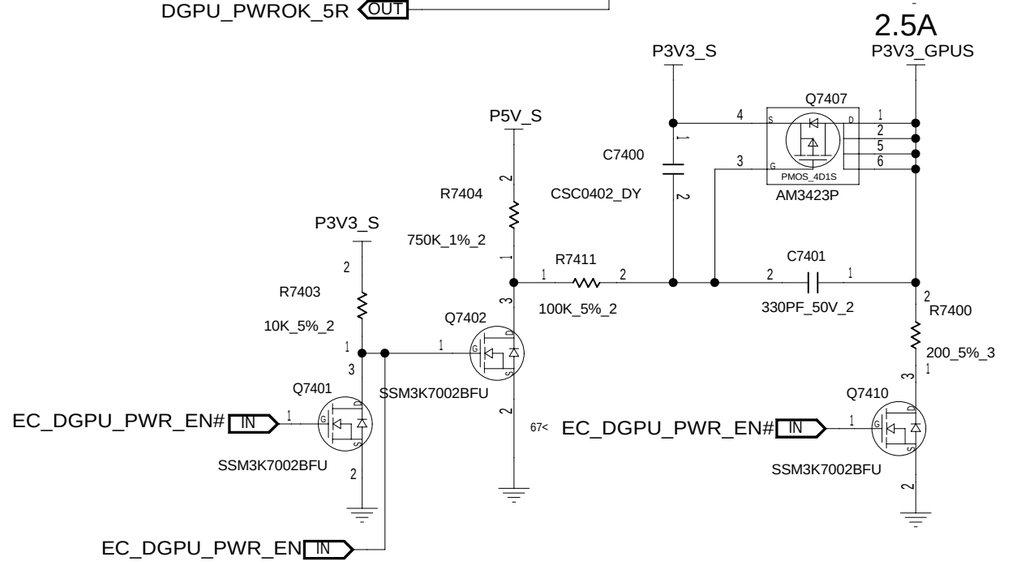
CHANGE by Frank Hu DATE Fri Dec 31 10:17:04 2010 SHEET 66 of 97

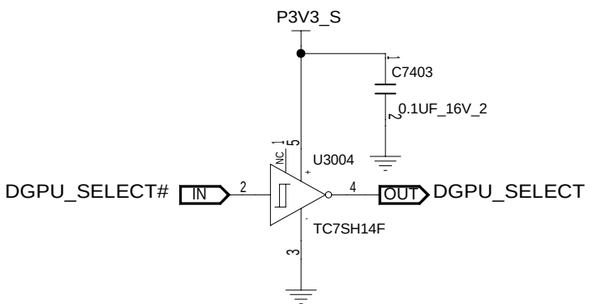


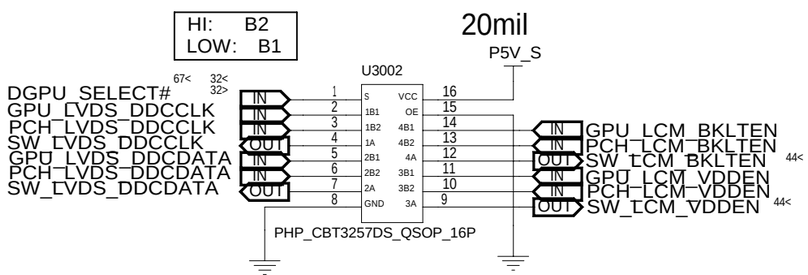


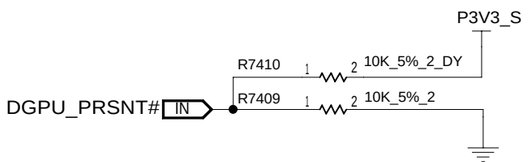


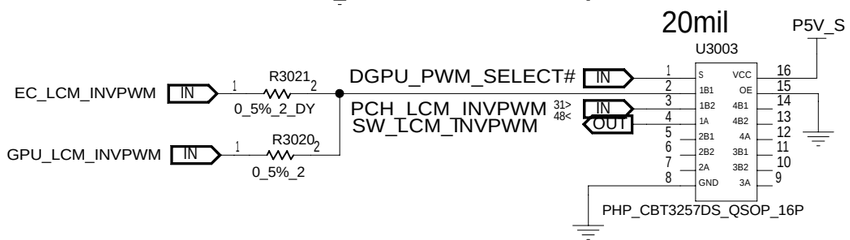












	DURING RESET	AFTER RESET	
DGPU_PRSNT#			0 : ADDIN CARD PRESENT 1 : ADDIN CARD NOT PLUGGED IN
DGPU_PWR_EN#	HIGH	HIGH	0 : DGPU POWER SWITCH TURNED ON 1 : POWER SWITCH TURNED OFF
DGPU_PWROK			0 : DGPU POWER IS NOT STABLE. 1 : DGPU POWER IS STABLE
DGPU_HOLD_RST#	LOW	LOW	0 : KEEP DGPU IN RESET 1 : RESET IS RELEASED
DGPU_SELECT#	HIGH	HIGH	0 : DISPLAY SWITCH ENABLED FOR DGPU 1 : DISPLAY SWITCH ENABLED FOR IGPU
DGPU_PWM_SELECT#			0 : PWM SIGNAL FROM EC 1 : PWM SIGNAL FROM PCH

INVENTEC

TITLE: EVEREST-M
GPU SW / POWER

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX-MTR	A01

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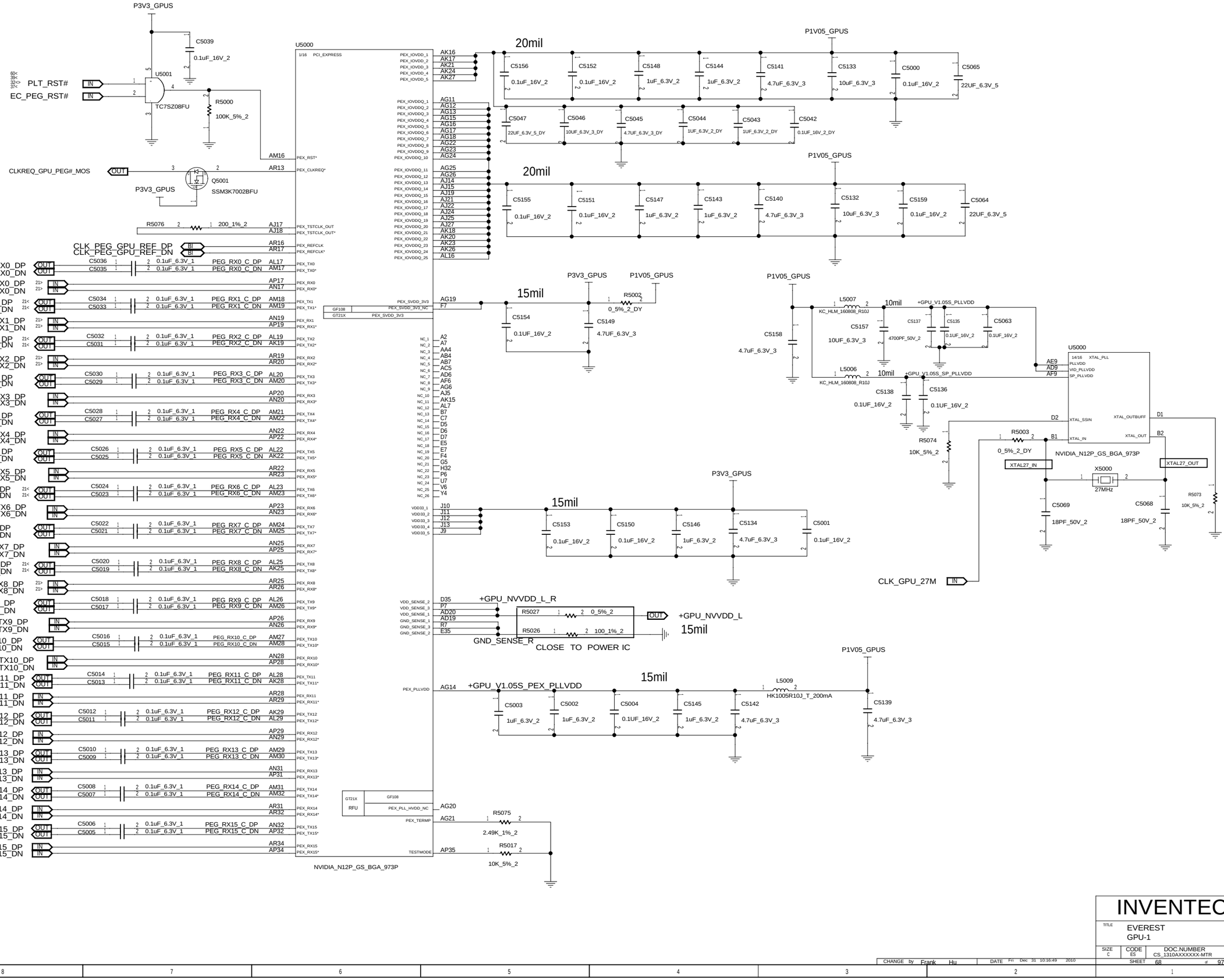
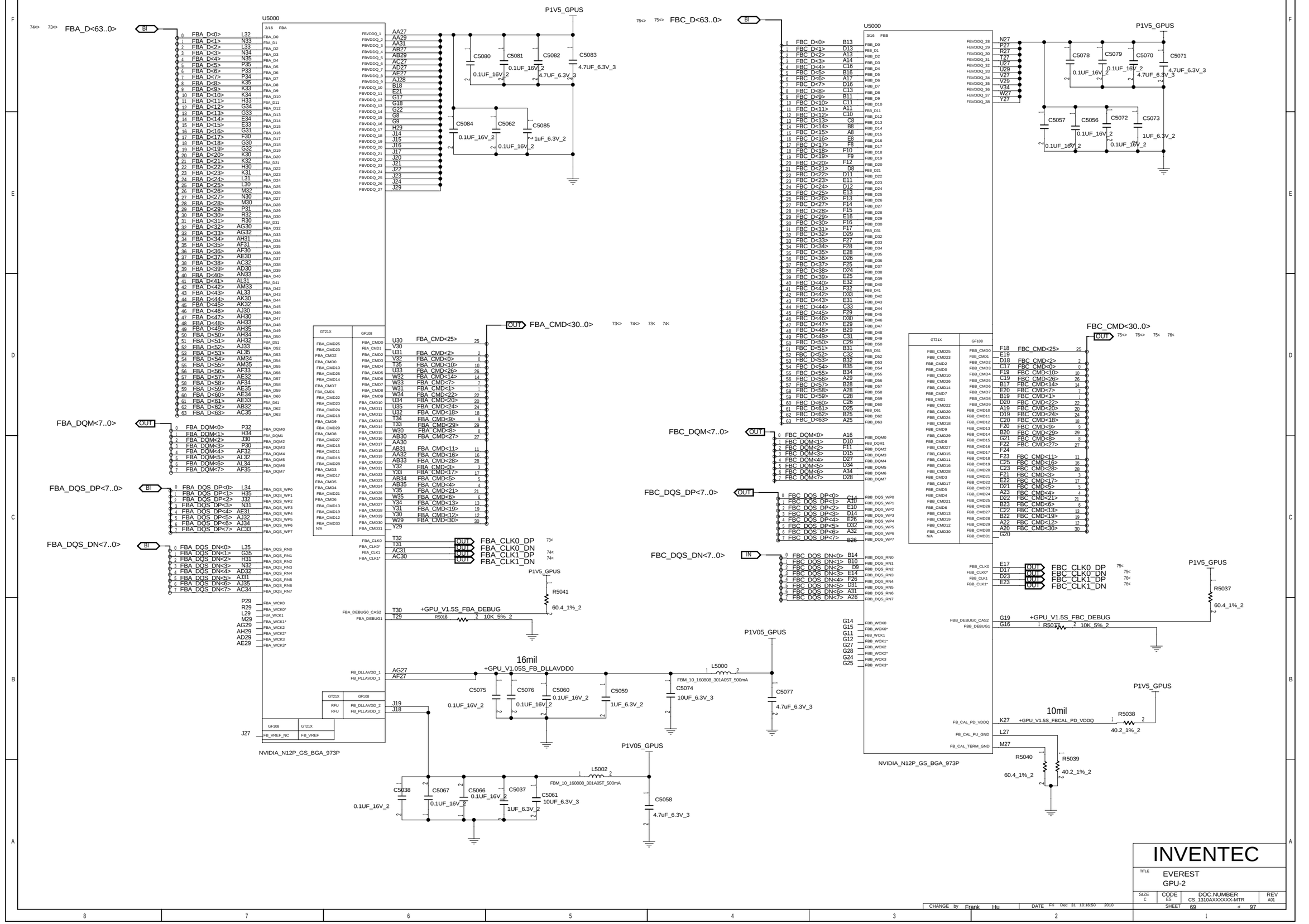


INVENTEC

TITLE	EVEREST GPU-1		
SIZE C	CODE ES	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:16:49 2010	SHEET 68 of 97	



CHANGE by	Frank Hu
DATE	Fri Dec 31 10:16:50 2010

INVENTEC

TITLE	
	EVEREST
	GPU-2

SIZE	CODE	DOC.NUMBER	REV
C	ES	CS_1310AXXXXXX-MTR	A01

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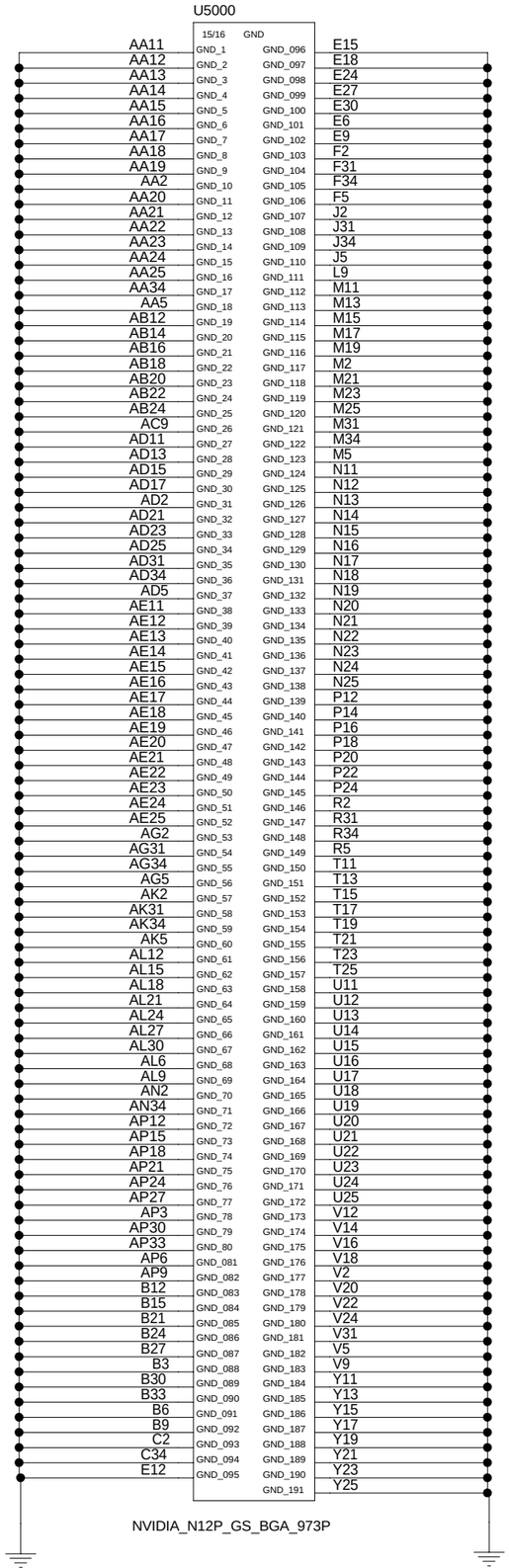
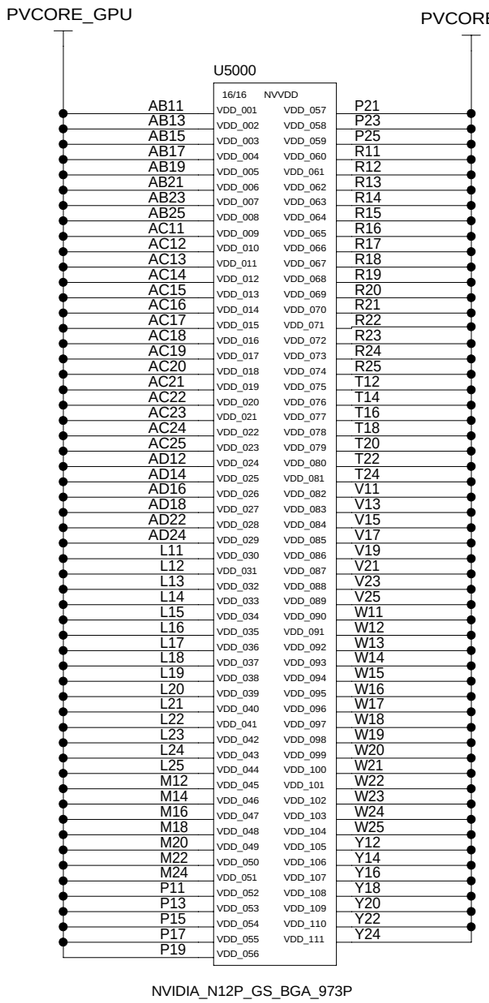
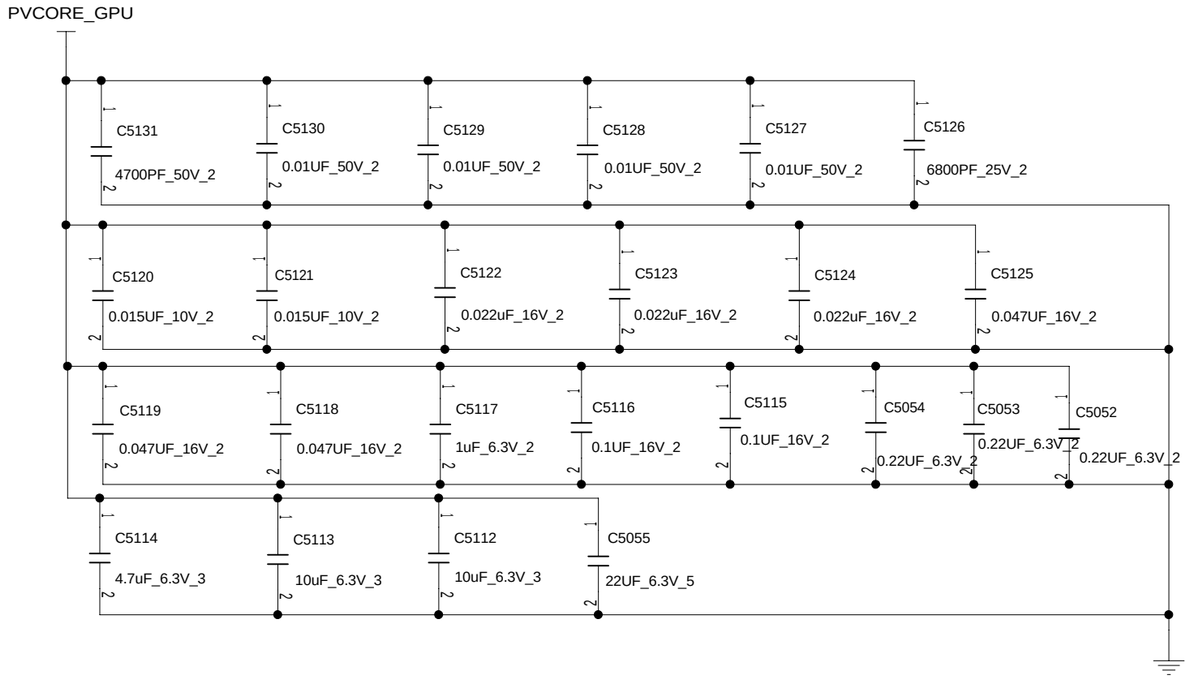
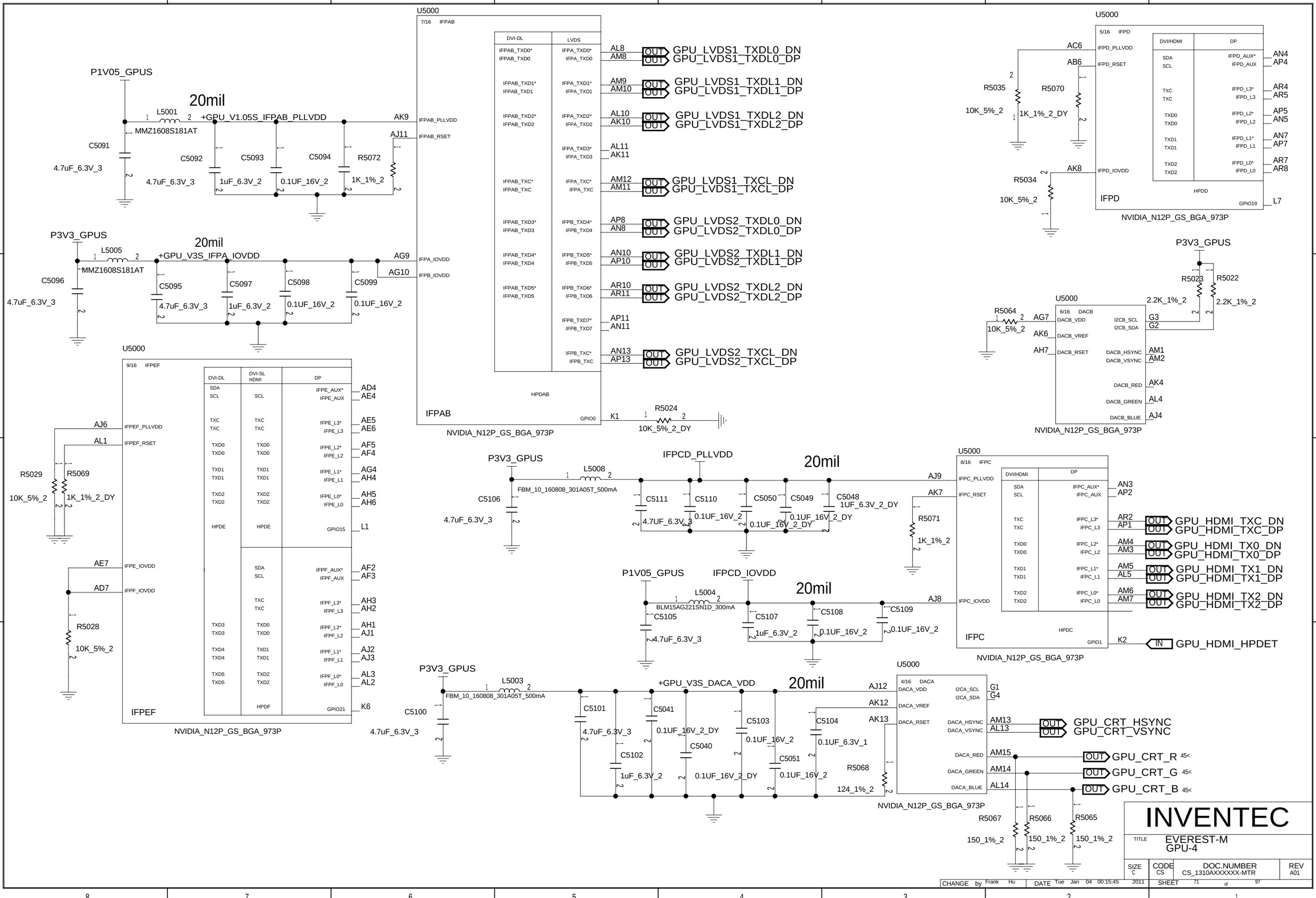






INVENTEC			
TITLE	EVEREST-M GPU-3		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:17:04 2010	SHEET 70 of 97	


U5000
7/16 IFPAB
DVI-DL
LVDS
IFPAB_TXD0*
IFPAB_TXD0
IFPA_TXD0*
IFPA_TXD0
AL8
AM8
GPU_LVDS1_TXDL0_DN
GPU_LVDS1_TXDL0_DP
IFPAB_TXD1*
IFPAB_TXD1
IFPA_TXD1*
IFPA_TXD1
AM9
AM10
GPU_LVDS1_TXDL1_DN
GPU_LVDS1_TXDL1_DP
IFPAB_TXD2*
IFPAB_TXD2
IFPA_TXD2*
IFPA_TXD2
AL10
AK10
GPU_LVDS1_TXDL2_DN
GPU_LVDS1_TXDL2_DP
IFPA_TXD3*
IFPA_TXD3
AL11
AK11
IFPAB_TXC*
IFPAB_TXC
IFPA_TXC*
IFPA_TXC
AM12
AM11
GPU_LVDS1_TXCL_DN
GPU_LVDS1_TXCL_DP
IFPAB_TXD3*
IFPAB_TXD3
IFPB_TXD4*
IFPB_TXD4
AP8
AN8
GPU_LVDS2_TXDL0_DN
GPU_LVDS2_TXDL0_DP
IFPAB_TXD4*
IFPAB_TXD4
IFPB_TXD5*
IFPB_TXD5
AN10
AP10
GPU_LVDS2_TXDL1_DN
GPU_LVDS2_TXDL1_DP
IFPAB_TXD5*
IFPAB_TXD5
IFPB_TXD6*
IFPB_TXD6
AR10
AR11
GPU_LVDS2_TXDL2_DN
GPU_LVDS2_TXDL2_DP
IFPB_TXD7*
IFPB_TXD7
AP11
AN11
IFPB_TXC*
IFPB_TXC
AN13
AP13
GPU_LVDS2_TXCL_DN
GPU_LVDS2_TXCL_DP
HPDAB
IFPAB
GPIO0
K1
R5024
10K_5%_2_DY
NVIDIA_N12P_GS_BGA_973P
P1V05_GPUS
20mil
L5001
+GPU_V1.05S_IFPAB_PLLVDD
AK9
IFPAB_PLLVDD
MMZ1608S181AT
AJ11
IFPAB_RSET
C5091
4.7uF_6.3V_3
C5092
4.7uF_6.3V_3
C5093
1uF_6.3V_2
C5094
0.1UF_16V_2
R5072
1K_1%_2
P3V3_GPUS
20mil
L5005
+GPU_V3S_IFPA_IOVDD
AG9
IFPA_IOVDD
AG10
IFPB_IOVDD
MMZ1608S181AT
C5096
4.7uF_6.3V_3
C5095
4.7uF_6.3V_3
C5097
1uF_6.3V_2
C5098
0.1UF_16V_2
C5099
0.1UF_16V_2
U5000
9/16 IFPEF
DVI-DL
DVI-SL HDMI
DP
SDA
SCL
IFPE_AUX*
IFPE_AUX
AD4
AE4
TXC
TXD0
TXD1
TXD2
IFPE_L3*
IFPE_L3
IFPE_L2*
IFPE_L2
IFPE_L1*
IFPE_L1
IFPE_L0*
IFPE_L0
AE5
AE6
AF5
AF4
AG4
AH4
AH5
AH6
HPDE
GPIO15
L1
IFPEF_PLLVDD
IFPEF_RSET
AJ6
AL1
R5029
10K_5%_2
R5069
1K_1%_2_DY
IFPE_IOVDD
AE7
IFPF_IOVDD
AD7
R5028
10K_5%_2
IFPF_AUX*
IFPF_AUX
AF2
AF3
IFPF_L3*
IFPF_L3
AH3
AH2
IFPF_L2*
IFPF_L2
AH1
AJ1
IFPF_L1*
IFPF_L1
AJ2
AJ3
IFPF_L0*
IFPF_L0
AL3
AL2
TXD3
TXD4
TXD5
HPDF
GPIO21
K6
IFPEF
NVIDIA_N12P_GS_BGA_973P
U5000
5/16 IFPD
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DP
IFPD_PLLVDD
AC6
IFPD_RSET
AB6
R5035
10K_5%_2
R5070
1K_1%_2_DY
IFPD_IOVDD
AK8
R5034
10K_5%_2
IFPD_AUX*
IFPD_AUX
AN4
AP4
IFPD_L3*
IFPD_L3
AR4
AR5
IFPD_L2*
IFPD_L2
AP5
AN5
IFPD_L1*
IFPD_L1
AN7
AP7
IFPD_L0*
IFPD_L0
AR7
AR8
HPDD
IFPD
GPIO19
L7
NVIDIA_N12P_GS_BGA_973P
P3V3_GPUS
R5023
R5022
2.2K_1%_2
2.2K_1%_2
U5000
6/16 DACB
R5064
10K_5%_2
AG7
DACB_VDD
I2CB_SCL
I2CB_SDA
G3
G2
AK6
DACB_VREF
AH7
DACB_RSET
DACB_HSYNC
DACB_VSYNC
AM1
AM2
DACB_RED
AK4
DACB_GREEN
AL4
DACB_BLUE
AJ4
NVIDIA_N12P_GS_BGA_973P
P3V3_GPUS
L5008
FBM_10_160808_301A05T_500mA
C5106
4.7uF_6.3V_3
IFPCD_PLLVDD
20mil
C5111
4.7uF_6.3V_3
C5110
0.1UF_16V_2
C5050
0.1UF_16V_2_DY
C5049
0.1UF_16V_2_DY
C5048
1UF_6.3V_2_DY
AJ9
AK7
R5071
1K_1%_2
U5000
8/16 IFPC
DVI/HDMI
DP
IFPC_PLLVDD
IFPC_RSET
SDA
SCL
IFPC_AUX*
IFPC_AUX
AN3
AP2
TXC
TXD0
TXD1
TXD2
IFPC_L3*
IFPC_L3
IFPC_L2*
IFPC_L2
IFPC_L1*
IFPC_L1
IFPC_L0*
IFPC_L0
AR2
AP1
AM4
AM3
AM5
AL5
AM6
AM7
GPU_HDMI_TXC_DN
GPU_HDMI_TXC_DP
GPU_HDMI_TX0_DN
GPU_HDMI_TX0_DP
GPU_HDMI_TX1_DN
GPU_HDMI_TX1_DP
GPU_HDMI_TX2_DN
GPU_HDMI_TX2_DP
HPDC
IFPC
GPIO1
K2
IN
GPU_HDMI_HPDET
NVIDIA_N12P_GS_BGA_973P
P1V05_GPUS
IFPCD_IOVDD
20mil
L5004
BLM15AG221SN1D_300mA
C5105
4.7uF_6.3V_3
C5107
1uF_6.3V_2
C5108
0.1UF_16V_2
C5109
0.1UF_16V_2
AJ8
P3V3_GPUS
L5003
FBM_10_160808_301A05T_500mA
C5100
4.7uF_6.3V_3
+GPU_V3S_DACA_VDD
20mil
C5101
4.7uF_6.3V_3
C5102
1uF_6.3V_2
C5041
0.1UF_16V_2_DY
C5040
0.1UF_16V_2_DY
C5103
0.1UF_16V_2
C5051
0.1UF_16V_2
C5104
0.1UF_6.3V_1
R5068
124_1%_2
U5000
4/16 DACA
AJ12
AK12
AK13
DACA_VDD
DACA_VREF
DACA_RSET
I2CA_SCL
I2CA_SDA
G1
G4
DACA_HSYNC
DACA_VSYNC
AM13
AL13
GPU_CRT_HSYNC
GPU_CRT_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
AM15
AM14
AL14
GPU_CRT_R
GPU_CRT_G
GPU_CRT_B
NVIDIA_N12P_GS_BGA_973P
R5067
150_1%_2
R5066
150_1%_2
R5065
150_1%_2
INVENTEC
TITLE
EVEREST-M
GPU-4
SIZE
C
CODE
CS
DOC.NUMBER
CS_1310AXXXXXX-MTR
REV
A01
CHANGE by Frank Hu
DATE Tue Jan 04 00:15:45 2011
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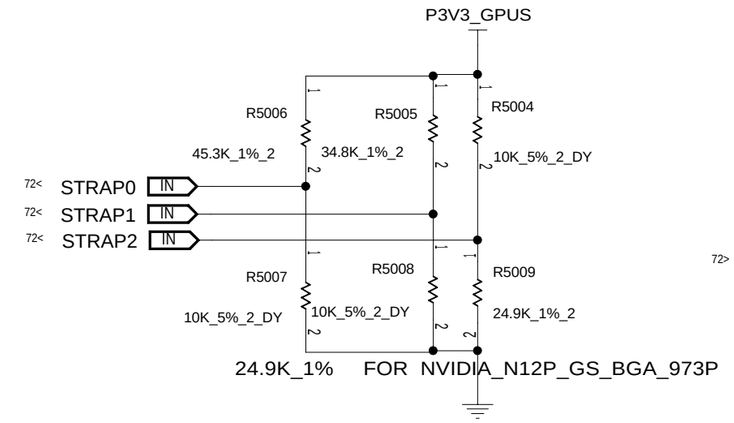
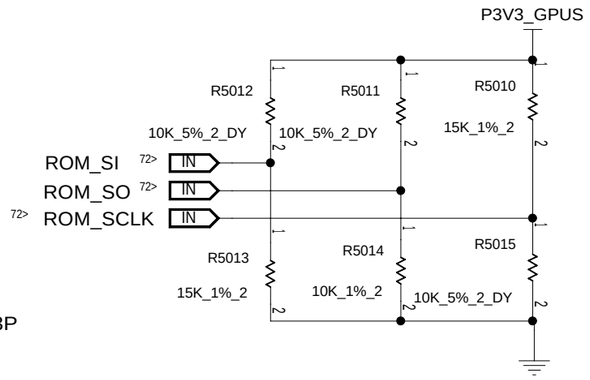
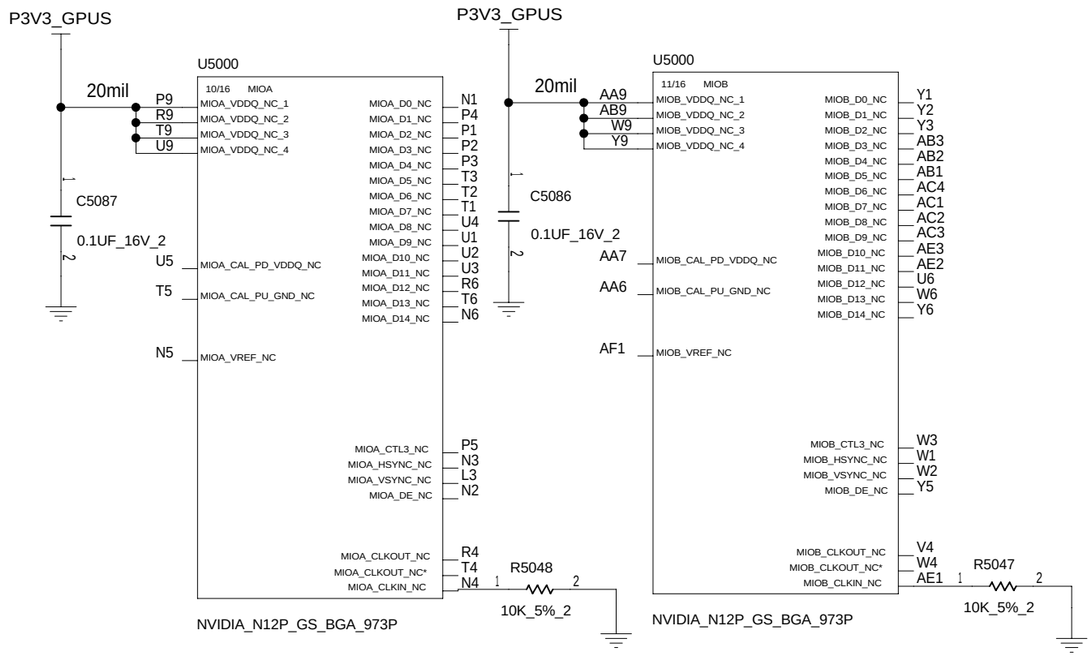
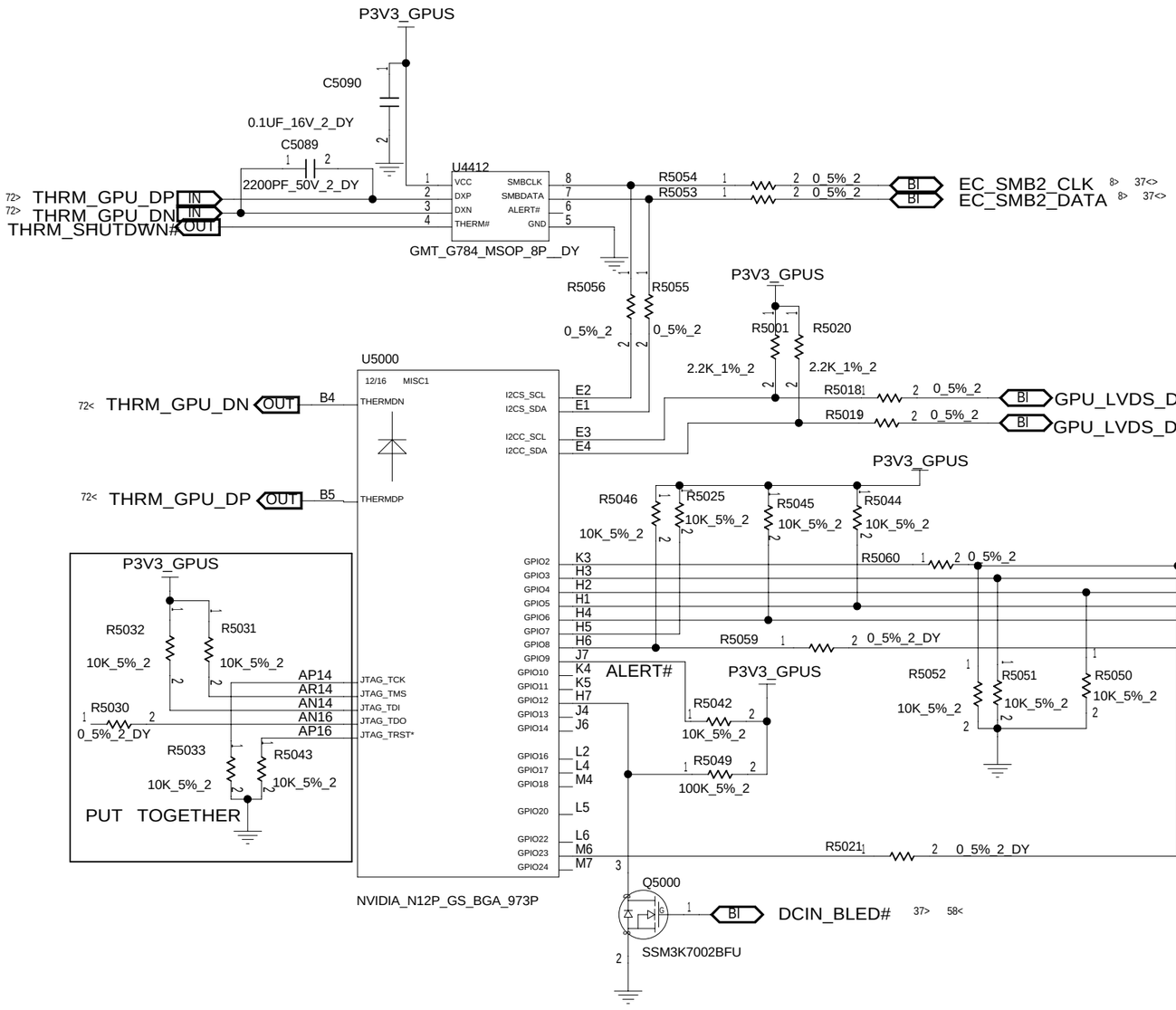
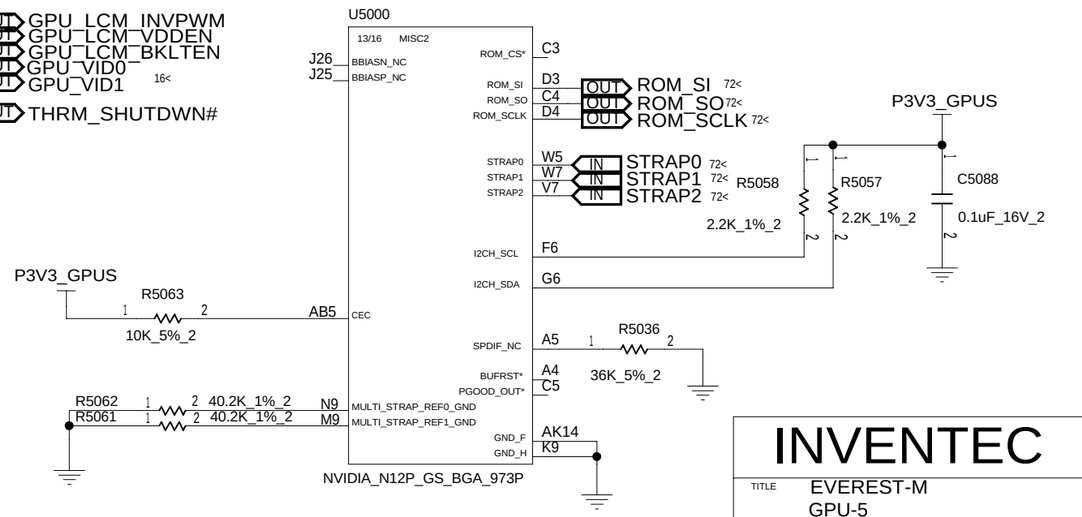




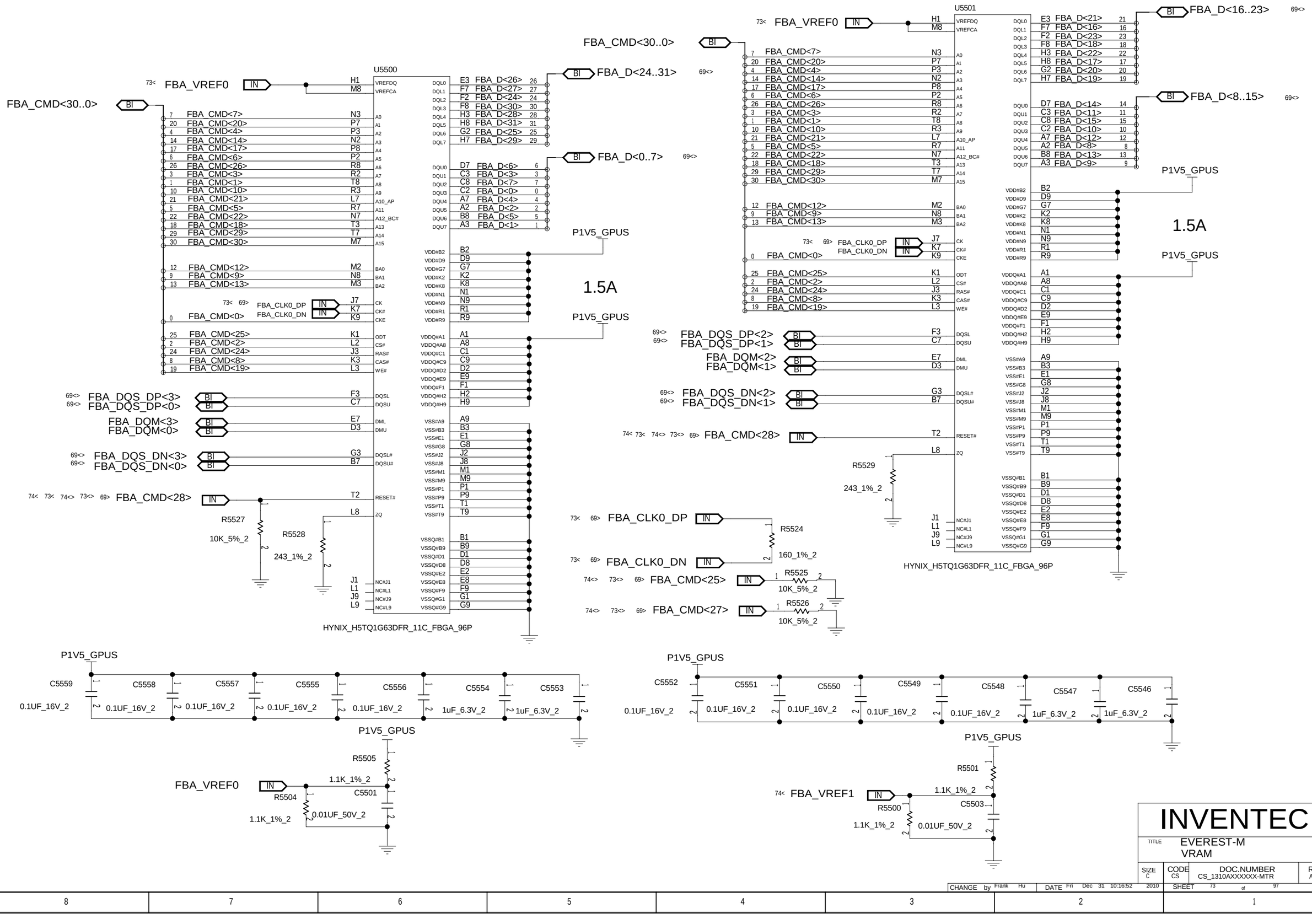






INVENTEC

TITLE	EVEREST-M GPU-5		
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXXX-MTR	REV A01
CHANGE by Frank Hu	DATE Fri Dec 31 10:16:52 2010	SHEET 72 of 97	


U5500
U5501
FBA_VREF0
FBA_CMD<30..0>
FBA_D<24..31>
FBA_D<0..7>
FBA_D<16..23>
FBA_D<8..15>
P1V5_GPUS
1.5A
FBA_CLK0_DP
FBA_CLK0_DN
FBA_DQS_DP<3>
FBA_DQS_DP<0>
FBA_DQM<3>
FBA_DQM<0>
FBA_DQS_DN<3>
FBA_DQS_DN<0>
FBA_DQS_DP<2>
FBA_DQS_DP<1>
FBA_DQM<2>
FBA_DQM<1>
FBA_DQS_DN<2>
FBA_DQS_DN<1>
FBA_CMD<28>
FBA_CMD<25>
FBA_CMD<27>
R5527 10K_5%_2
R5528 243_1%_2
R5524 160_1%_2
R5525 10K_5%_2
R5526 10K_5%_2
R5529 243_1%_2
HYNIX_H5TQ1G63DFR_11C_FBGA_96P
C5559 C5558 C5557 C5555 C5556 C5554 C5553
C5552 C5551 C5550 C5549 C5548 C5547 C5546
0.1UF_16V_2
1uF_6.3V_2
R5505 1.1K_1%_2
R5504 1.1K_1%_2
C5501 0.01UF_50V_2
R5501 1.1K_1%_2
R5500 1.1K_1%_2
C5503 0.01UF_50V_2
FBA_VREF1
INVENTEC
TITLE EVEREST-M VRAM
SIZE C
CODE CS
DOC.NUMBER CS_1310AXXXXXX-MTR
REV A01
CHANGE by Frank Hu
DATE Fri Dec 31 10:16:52 2010
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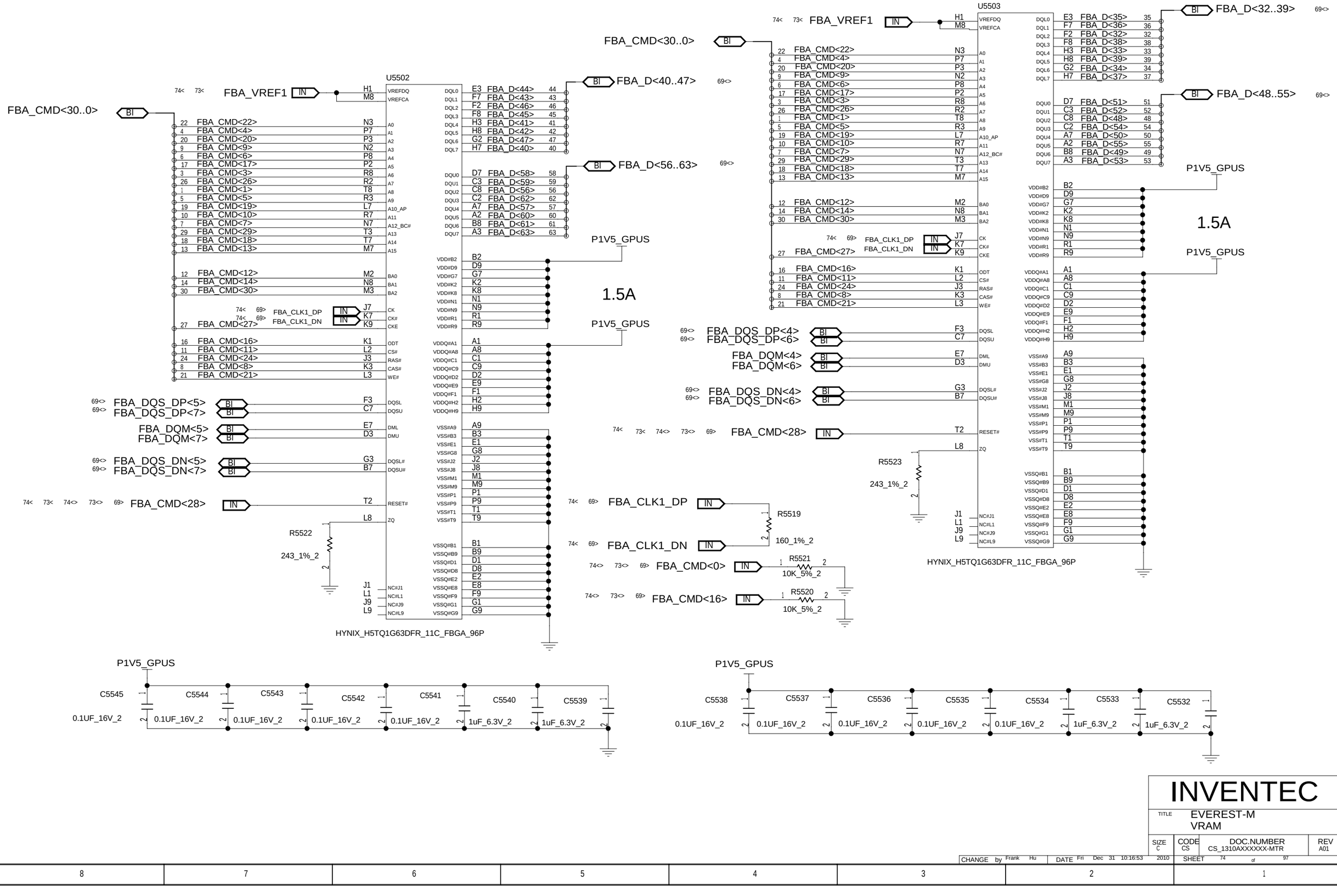
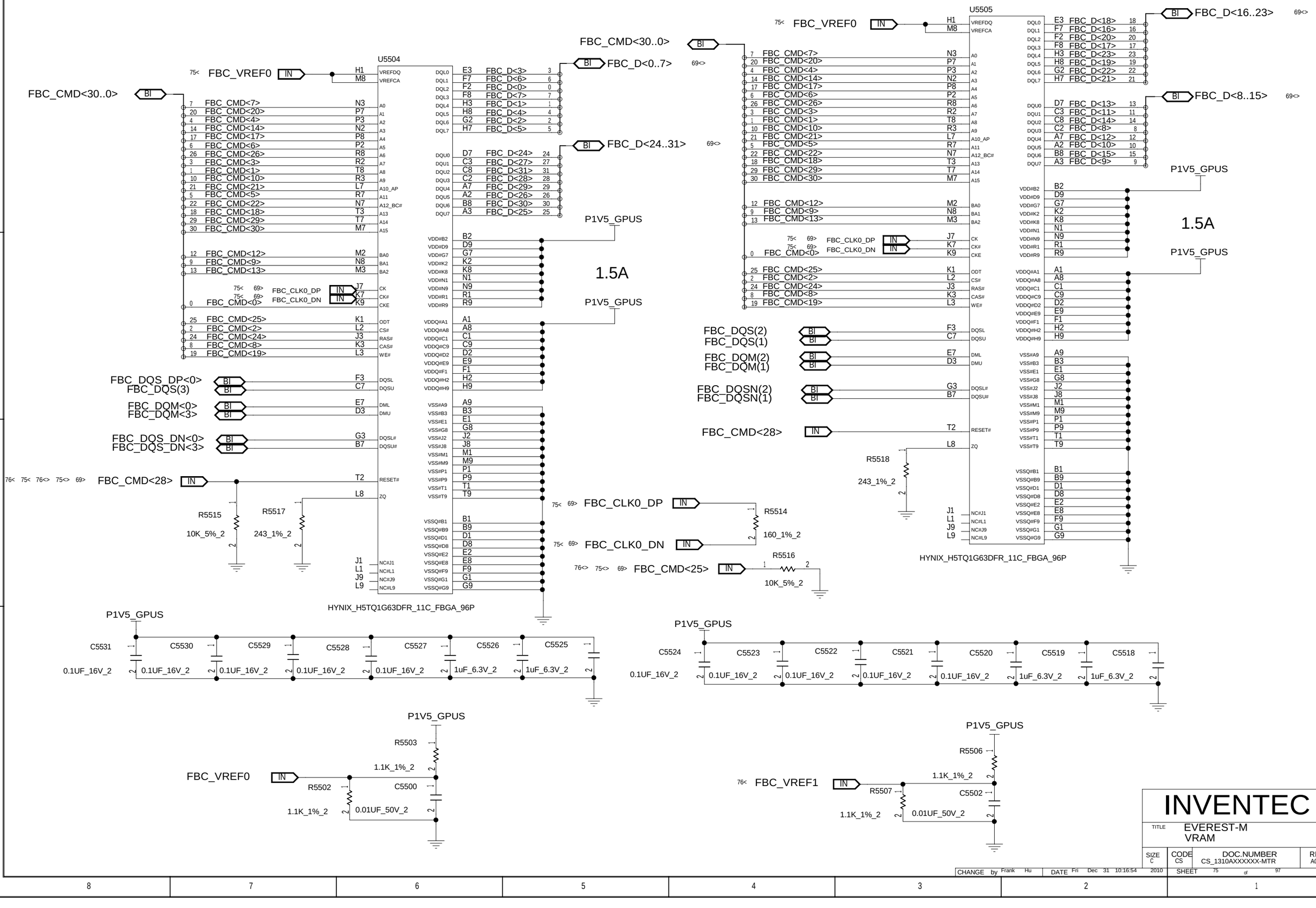


TITLE	EVEREST-M VRAM
SIZE	C
CODE	CS
DOC.NUMBER	CS_1310AXXXXXX-MTR
REV	A01
CHANGE by	Frank Hu
DATE	Fri Dec 31 10:16:53 2010
SHEET	74 of 97



TITLE	EVEREST-M VRAM
SIZE	C
CODE	CS
DOC.NUMBER	CS_1310AXXXXXX-MTR
REV	A01
CHANGE by	Frank Hu
DATE	Fri Dec 31 10:16:54 2010
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INVENTEC

FUSE6000
65W-75W 8A(6036A0003401)
90W 10A(6036A0002901)
120W 12A(6036A0006001)

PVADPTR
CN6000
ACES_91302_0047L_1_4P
C6035 1000PF_50V_2
FUSE6000 8A_125V
C6033 10PF_50V_2
L6001 NFE31PT222Z1E9L
PVBAT
R6017 RSC_0603_DY
R6019 33K_5%_2_DY
R6018 RSC_0603_DY
HW_V_ADC OUT
C6003 0.1uF_16V_2_DY
R6000 4.7K_5%_3
R6005 RSC_0603_DY
Q6003 AM4410NC
Q6002 AM4410NC
R6020 0.01_1%_6
C6025 CSC0805_DY
R6002 RSC_1206_DY
R6003 RSC_1206_DY
C6010 2200pF_50V_2
C6007 0.1UF_25V_3
R6023 1M_5%_3
D6000 DIODES_BAV99
C6013 0.1UF_25V_3
C6014 0.1UF_25V_3
C6012 0.1UF_16V_2
PVADPTR
D6001 BAT54C_30V_0.2A
C6018 68UF_25V
PVBAT
PAD6000 POWERPAD_2_0610
Q6005 TPCA8065_H
PVPACK
C6024 0.1uF_25V_3
P3V3_AL
R6008 10K_5%_3
R6006 4.02K_1%_3
R6007 4.02K_1%_3
R6012 20.5K_1%_2
WS
ACPRES# OUT
Active Low
R6015 10_5%_5
Q6000 AON7410
C6002 470pF_50V_2
C6005 4.7UF_25V_5
C6001 4.7UF_25V_5
C6000 CSC0805_DY
U6000 TI_BQ24725RGRR_QFN_20P
C6015 1UF_25V_3
VRCHARGER_HG
VRCHARGER_PH
C6006 0.047uF_16V_2
L6000 PCMC063T_4R7MN
R6001 0.01_1%_6
C6022 0.1UF_16V_2
HW_I_ADC OUT
R6013 3.3K_1%_3
C6028 CSC0603_DY
C6026 CSC0402_DY
C6008 100pF_50V_2
C6029 CSC0402_DY
C6027 CSC0402_DY
EC_SMB2_DATA OUT
EC_SMB2_CLK OUT
D6002 BAT54C_30V_0.2A
C6017 1UF_10V_2
Q6001 AON7410
D6003 SBR3U40P1_DY
R6004 2.2_5%_3
C6009 0.0015uF_50V_2
C6020 0.1UF_25V_3
C6021 0.1UF_25V_3
C6016 4.7UF_25V_5
C6019 4.7UF_25V_5
C6023 CSC0805_DY
C6004 4.7UF_25V_5
VRCHARGER_LG
P3V3_AL
R6014 110K_1%_2
R6021 10K_5%_3_DY
Q6004 SSM3K7002FU_DY
WS
CHG_EN IN
Active High
R6011 30.1K_1%_2
C6011 0.1UF_16V_2
R6009 10_1%_2
R6010 6.98_1%_2
R6016 4.02K_1%_3

INVENTEC
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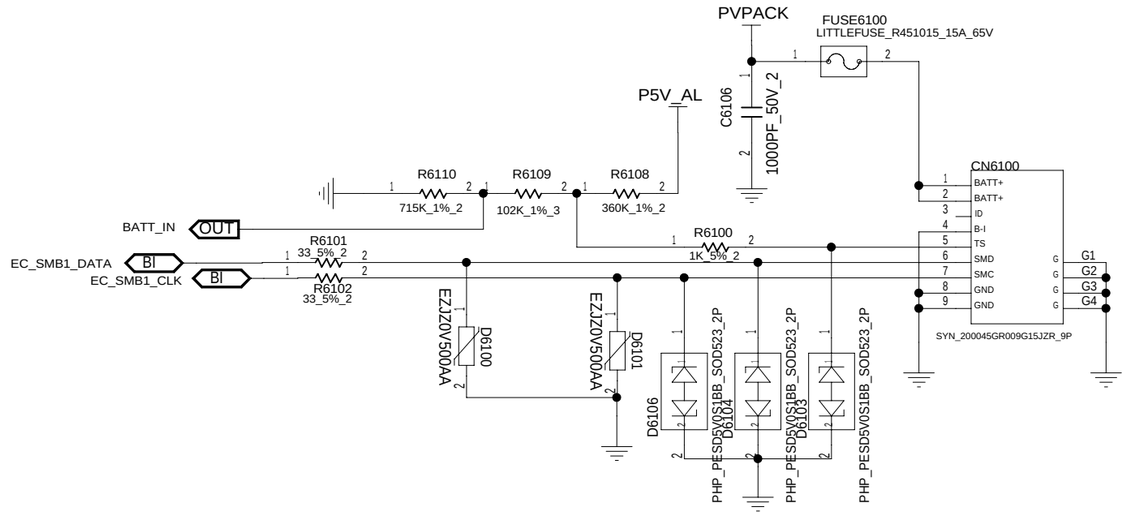
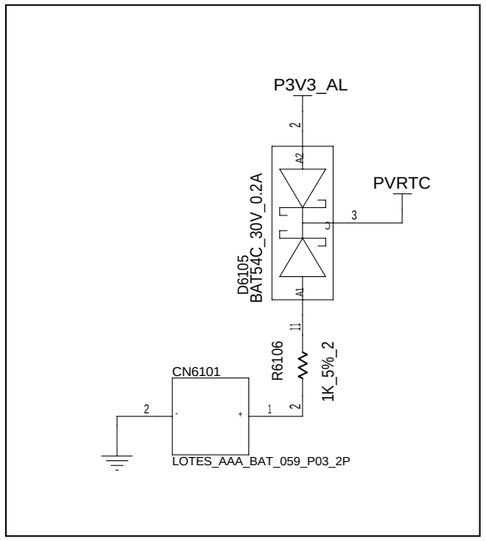
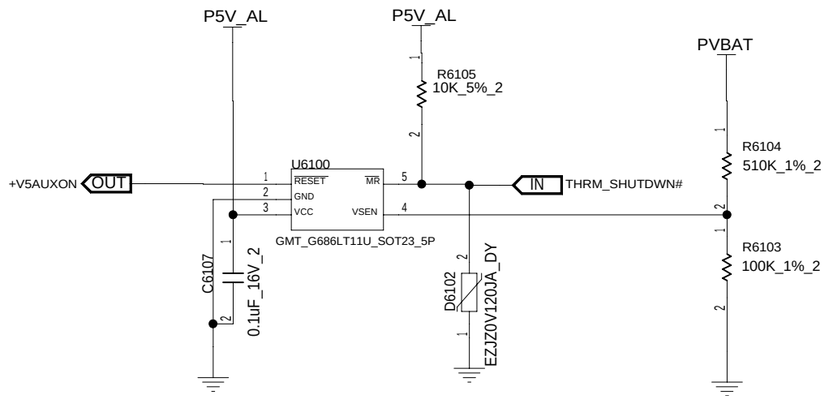


REMOVE ?





INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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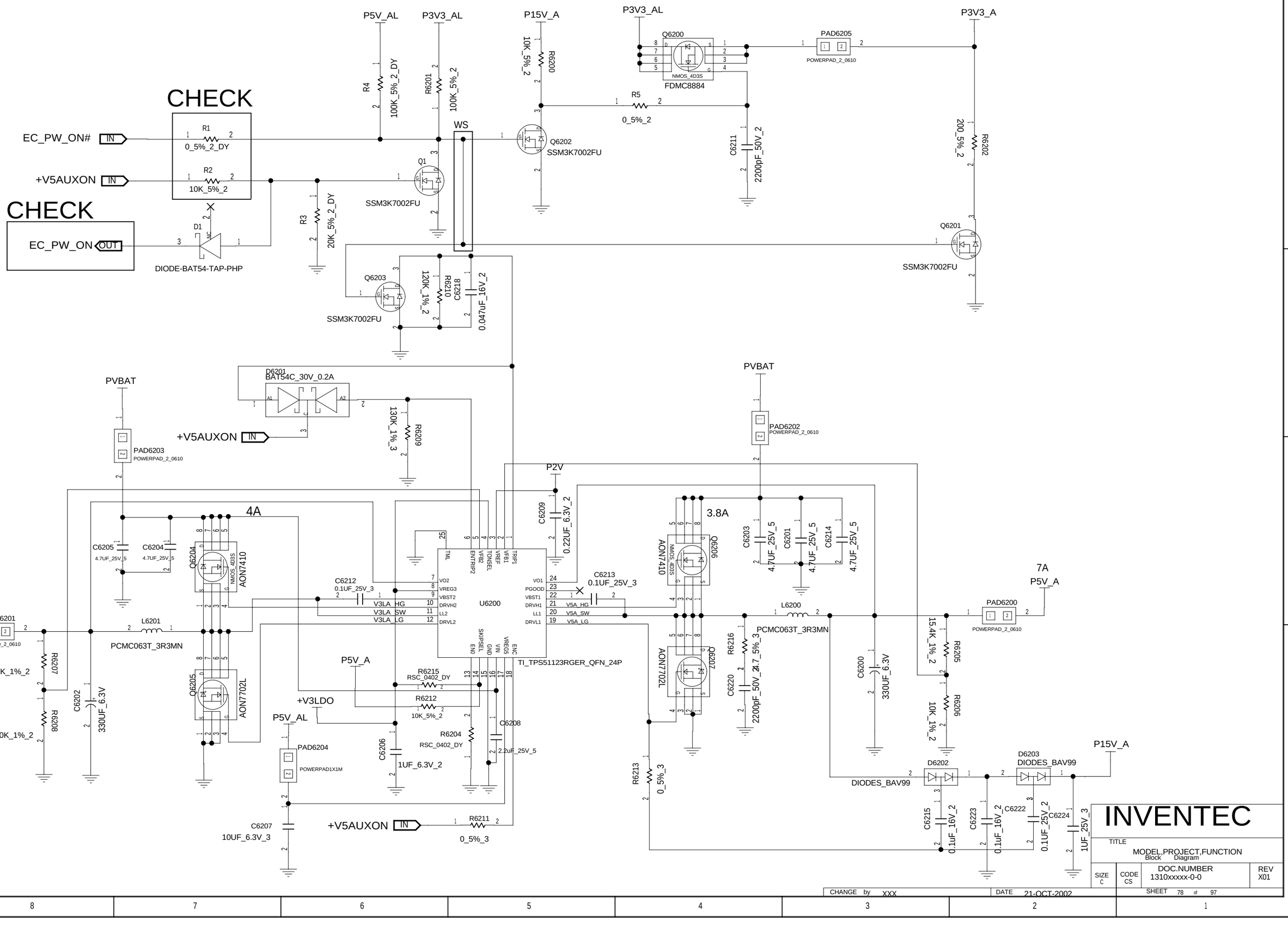
P5V_AL
P3V3_AL
P15V_A
P3V3_AL
P3V3_A
Q6200
NMOS_4D3S
FDMC8884
PAD6205
POWERPAD_2_0610
R4
100K_5%_2_DY
R6201
100K_5%_2
10K_5%_2
R6200
R5
0_5%_2
C6211
2200pF_50V_2
200_5%_2
R6202
CHECK
EC_PW_ON#
IN
R1
0_5%_2_DY
+V5AUXON
R2
10K_5%_2
WS
Q6202
SSM3K7002FU
Q1
SSM3K7002FU
CHECK
EC_PW_ON
OUT
D1
DIODE-BAT54-TAP-PHP
R3
20K_5%_2_DY
Q6201
SSM3K7002FU
Q6203
SSM3K7002FU
120K_1%_2
R6210
C6218
0.047uF_16V_2
PVBAT
D6201
BAT54C_30V_0.2A
+V5AUXON
IN
130K_1%_3
R6209
PAD6203
POWERPAD_2_0610
PVBAT
PAD6202
POWERPAD_2_0610
P2V
C6209
0.22UF_6.3V_2
4A
3.8A
C6205
4.7UF_25V_5
C6204
4.7UF_25V_5
Q6204
AON7410
Q6206
AON7410
C6203
4.7UF_25V_5
C6201
4.7UF_25V_5
C6214
4.7UF_25V_5
10A
P3V3_AL
PAD6201
POWERPAD_2_0610
L6201
PCMC063T_3R3MN
C6212
0.1UF_25V_3
C6213
0.1UF_25V_3
U6200
TI_TPS51123RGER_QFN_24P
7A
P5V_A
PAD6200
POWERPAD_2_0610
L6200
PCMC063T_3R3MN
R6207
6.8K_1%_2
R6208
10K_1%_2
C6202
330UF_6.3V
Q6205
AON7702L
Q6207
AON7702L
R6216
1.7_5%_3
C6220
2200pF_50V_2
C6200
330UF_6.3V
15.4K_1%_2
R6205
10K_1%_2
R6206
P5V_A
R6215
RSC_0402_DY
R6212
10K_5%_2
+V3LDO
P5V_AL
PAD6204
POWERPAD1X1M
C6206
1UF_6.3V_2
R6204
RSC_0402_DY
C6208
2.2uF_25V_5
R6213
0_5%_3
P15V_A
D6202
DIODES_BAV99
D6203
DIODES_BAV99
DIODES_BAV99
C6215
0.1uF_16V_2
C6223
0.1uF_16V_2
C6222
0.1UF_25V_2
C6224
1UF_25V_3
C6207
10UF_6.3V_3
+V5AUXON
IN
R6211
0_5%_3
V3LA_HG
V3LA_SW
V3LA_LG
V5A_HG
V5A_SW
V5A_LG
INVENTEC
TITLE
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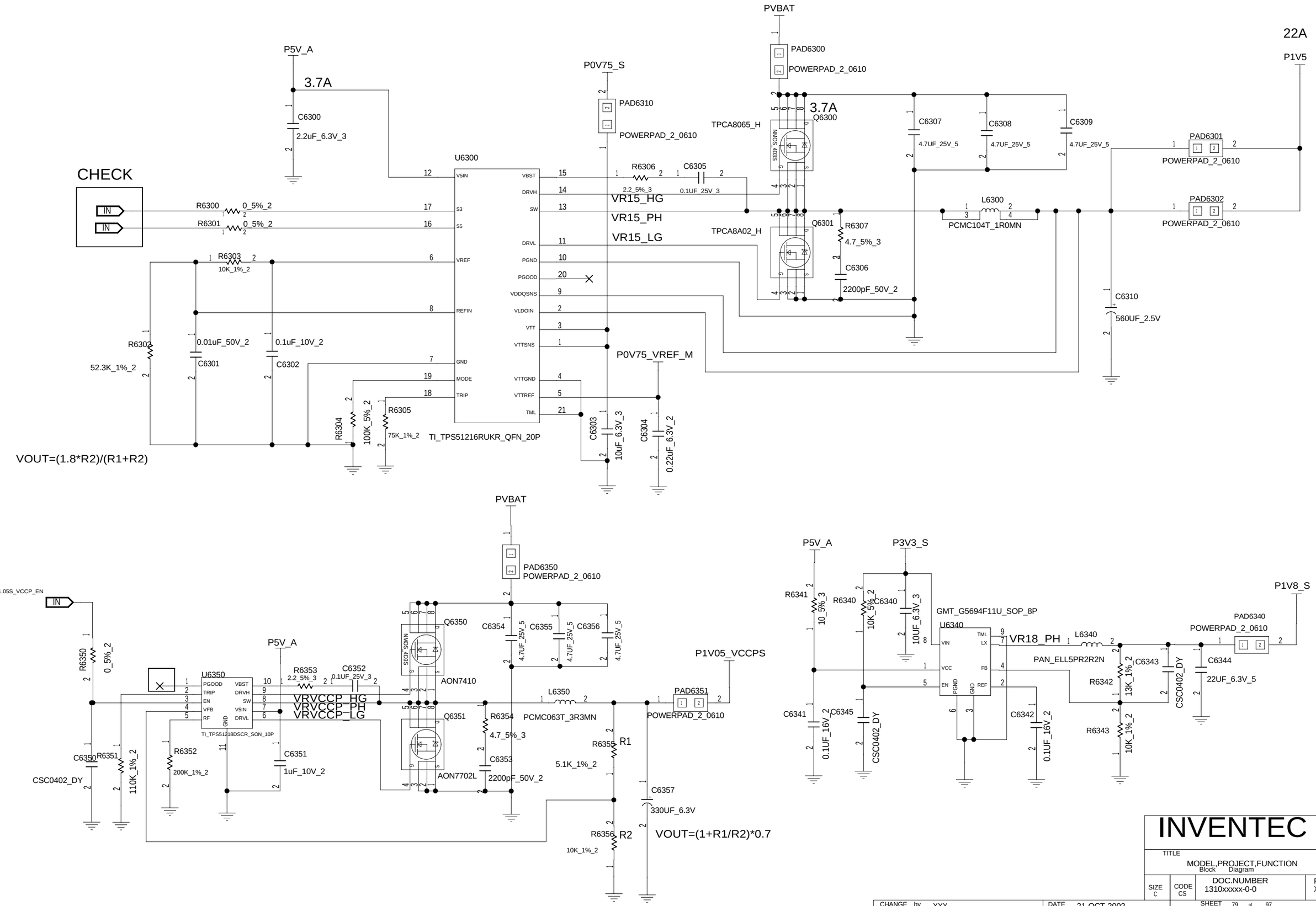
PVBAT
22A
P1V5
P5V_A
3.7A
C6300
2.2uF_6.3V_3
P0V75_S
PAD6310
POWERPAD_2_0610
PAD6300
POWERPAD_2_0610
TPCA8065_H
Q6300
3.7A
C6307
C6308
C6309
4.7UF_25V_5
PAD6301
POWERPAD_2_0610
CHECK
IN
IN
R6300
0_5%_2
R6301
0_5%_2
U6300
VSIN
S3
S5
VREF
REFIN
GND
MODE
TRIP
VBST
DRVH
SW
DRVL
PGOOD
VDDQSNS
VLDOIN
VTT
VTTSNS
VTTGND
VTTREF
TML
R6306
2.2_5%_3
C6305
0.1UF_25V_3
VR15_HG
VR15_PH
VR15_LG
TPCA8A02_H
Q6301
R6307
4.7_5%_3
C6306
2200pF_50V_2
L6300
PCMC104T_1R0MN
PAD6302
POWERPAD_2_0610
C6310
560UF_2.5V
R6303
10K_1%_2
R6302
52.3K_1%_2
0.01uF_50V_2
C6301
0.1uF_10V_2
C6302
R6304
100K_5%_2
R6305
75K_1%_2
TI_TPS51216RUKR_QFN_20P
P0V75_VREF_M
C6303
10uF_6.3V_3
C6304
0.22uF_6.3V_2
VOUT=(1.8*R2)/(R1+R2)
PVBAT
PAD6350
POWERPAD_2_0610
+V1.05S_VCCP_EN
IN
R6350
0_5%_2
P5V_A
U6350
PGOOD
TRIP
EN
VFB
RF
VBST
DRVH
SW
VSIN
DRVL
GND
TI_TPS51218DSCR_SON_10P
R6353
2.2_5%_3
C6352
0.1UF_25V_3
VRVCCP_HG
VRVCCP_PH
VRVCCP_LG
Q6350
AON7410
Q6351
AON7702L
C6354
C6355
C6356
4.7UF_25V_5
L6350
PCMC063T_3R3MN
R6354
4.7_5%_3
C6353
2200pF_50V_2
P1V05_VCCPS
PAD6351
POWERPAD_2_0610
R6355
R1
5.1K_1%_2
C6357
330UF_6.3V
R6356
R2
10K_1%_2
VOUT=(1+R1/R2)*0.7
C6350
CSC0402_DY
R6351
110K_1%_2
R6352
200K_1%_2
C6351
1uF_10V_2
P5V_A
P3V3_S
R6341
10_5%_3
R6340
10K_5%_2
C6340
10UF_6.3V_3
GMT_G5694F11U_SOP_8P
U6340
VIN
VCC
EN
TML
LX
FB
PGND
GND
REF
VR18_PH
L6340
PAN_ELL5PR2R2N
R6342
13K_1%_2
C6343
CSC0402_DY
C6344
22UF_6.3V_5
PAD6340
POWERPAD_2_0610
P1V8_S
C6341
0.1UF_16V_2
C6345
CSC0402_DY
C6342
0.1UF_16V_2
R6343
10K_1%_2
INVENTEC
TITLE
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Block Diagram
SIZE C
CODE CS
DOC.NUMBER 1310xxxxx-0-0
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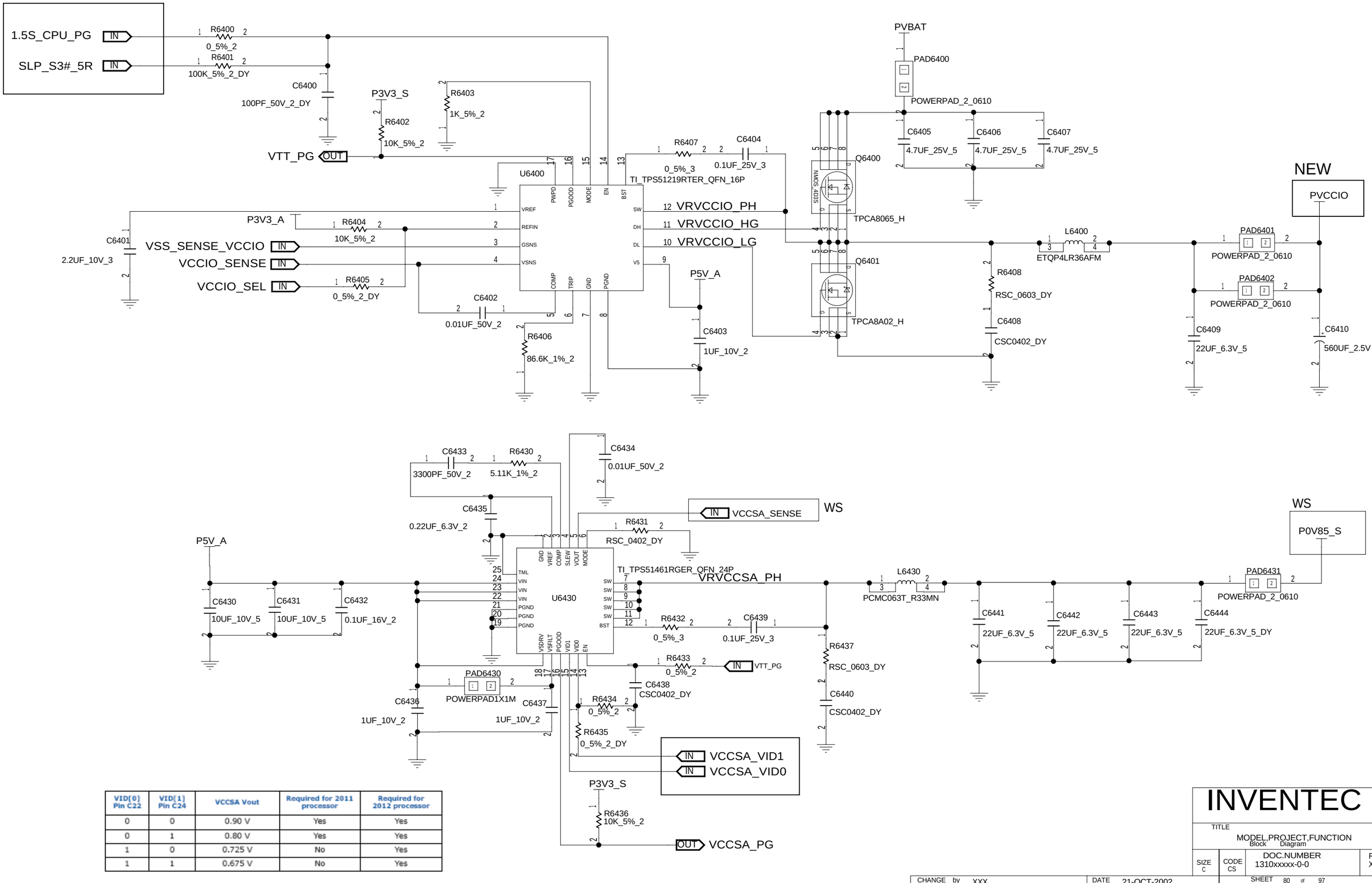

VID[0] Pin C22	VID[1] Pin C24	VCCSA Vout	Required for 2011 processor	Required for 2012 processor
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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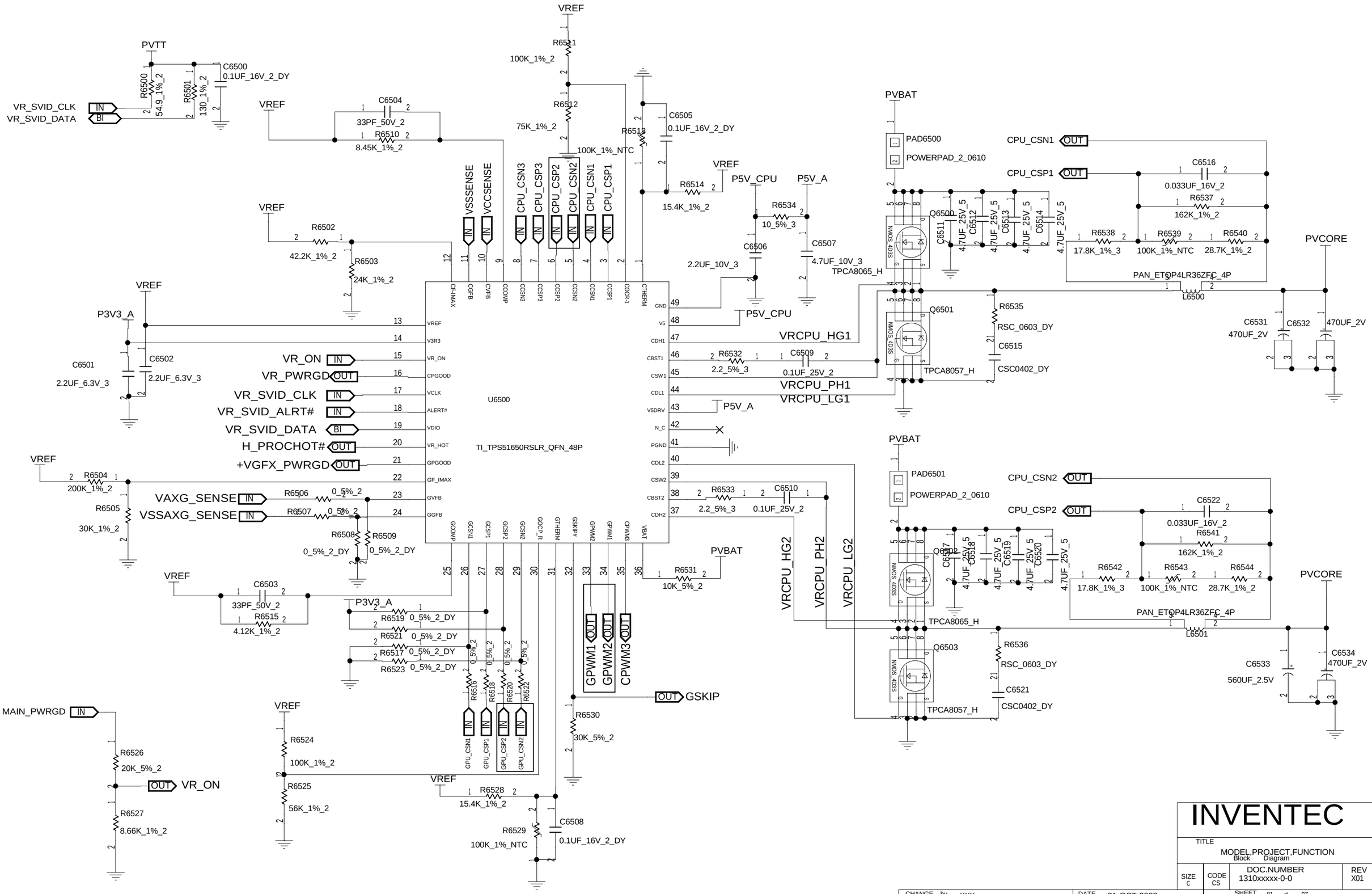
U6500
TI_TPS51650RSLR_QFN_48P
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE C
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
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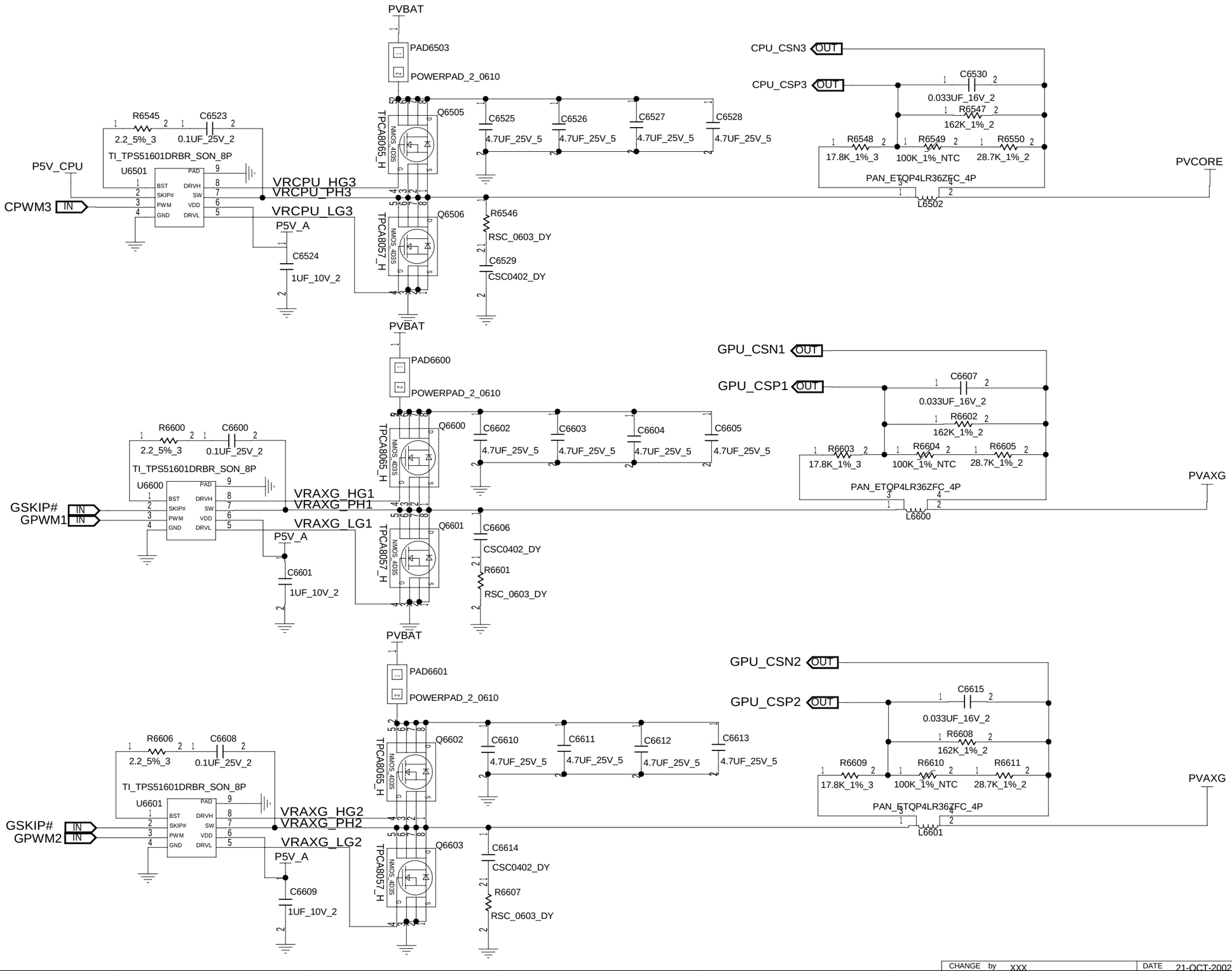

INVENTEC			
TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE C	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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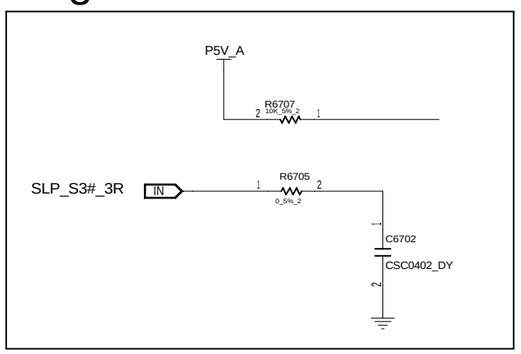
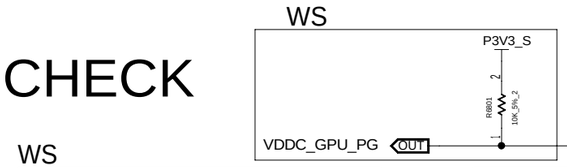
Original Sch

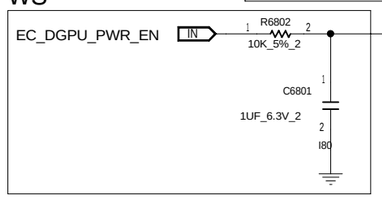


CHECK

WS



WS



CHECK

WS

CHECK

WS

WS

VID1	VID0	+VDDC_GPU
POW_SW1	POW_SW0	PCORE_GPU
0	0	1.05V
0	1	1.00V
1	0	0.90V

For XT

VID1	VID0	+VDDC_GPU
POW_SW1	POW_SW0	PCORE_GPU
0	1	1.00V
1	0	0.90V

For PRO

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
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SIZE	CODE	DOC.NUMBER	REV
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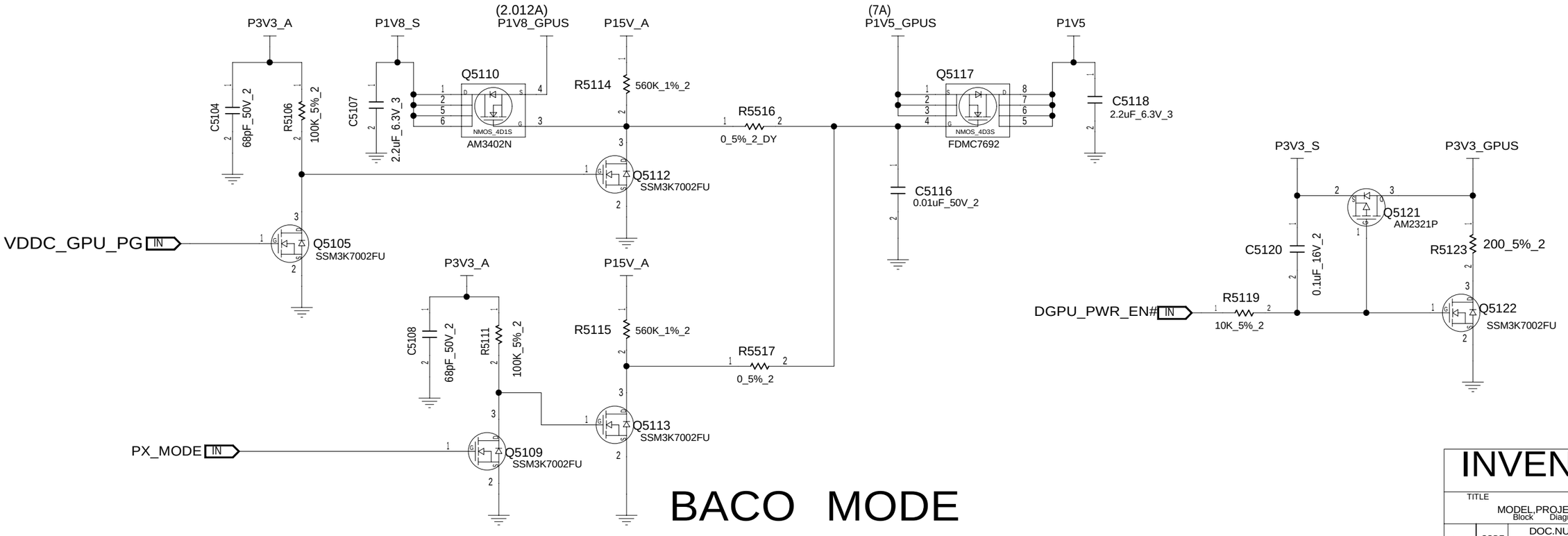
GPU
Whistler

CONFIGURATION STRAPS: Pin-Based Straps

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS
TX_PWRS_ENB	GPIO_0	Full Tx output swing=1 (Default) 50% Tx output swing=0
TX_DEEMPH_EN	GPIO_1	Tx De-emphasis enabled=1 (Default) Tx De-emphasis disabled=0
RESERVED	GPIO_2	Advertises the PCIe device as 2.5 GT/s capable at power on=0 Advertises the PCIe device as 5.0 GT/s capable at power on=1 (ASIC Internal pull down, and PCB Default is 0)
RESERVED	GPIO_8	Must be low during reset PCB default is left unconnected
RESERVED	GPIO_21	Must be low during reset (PCB default is 0) Voltage control signal for the memory-voltage regulator.
BIF_VGA DIS	GPIO_9	VGA controller capacity enabled=0 (Default) VGA controller capacity disabled=1
BIOS_ROM_EN	GPIO_22	Disable the external BIOS ROM device=0 (Default) Enable the external BIOS ROM device=1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO_13 GPIO_12 GPIO_11	If GPIO_22 = 0, then CONFIG [2:0] defines the primary memory-aperture size. Default is 0 0 1
AUD[0] AUD[1]	HSYNC VSYNC	AUD [1:0]: 0 0 = No audio function 0 1 = Audio for DisplayPort only 1 0 = Audio for DisplayPort and HDMI, if dongle is detected 1 1 = Audio for both DisplayPort and HDMI. (Default is 1 1)
RESERVED	GENLK_CLK	Must be low during reset PCB default is left unconnected



BACO MODE

INVENTEC

TITLE: MODEL.PROJECT.FUNCTION
Block Diagram

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WHISTLER XT TDP: 30~35 W
WHISTLER PRO TDP: 20~25 W

U5124

PCI EXPRESS INTERFACE

PEG_TX0_DP	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PEG_RX0_C_DP
PEG_TX0_DN	Y37	PCIE_RX0N	PCIE_TX0N	Y32	PEG_RX0_C_DN
PEG_TX1_DP	Y35	PCIE_RX1P	PCIE_TX1P	W33	PEG_RX1_C_DP
PEG_TX1_DN	W36	PCIE_RX1N	PCIE_TX1N	W32	PEG_RX1_C_DN
PEG_TX2_DP	W38	PCIE_RX2P	PCIE_TX2P	U33	PEG_RX2_C_DP
PEG_TX2_DN	V37	PCIE_RX2N	PCIE_TX2N	U32	PEG_RX2_C_DN
PEG_TX3_DP	V35	PCIE_RX3P	PCIE_TX3P	U30	PEG_RX3_C_DP
PEG_TX3_DN	U36	PCIE_RX3N	PCIE_TX3N	U29	PEG_RX3_C_DN
PEG_TX4_DP	U38	PCIE_RX4P	PCIE_TX4P	T33	PEG_RX4_C_DP
PEG_TX4_DN	T37	PCIE_RX4N	PCIE_TX4N	T32	PEG_RX4_C_DN
PEG_TX5_DP	T35	PCIE_RX5P	PCIE_TX5P	T30	PEG_RX5_C_DP
PEG_TX5_DN	R36	PCIE_RX5N	PCIE_TX5N	T29	PEG_RX5_C_DN
PEG_TX6_DP	R38	PCIE_RX6P	PCIE_TX6P	P33	PEG_RX6_C_DP
PEG_TX6_DN	P37	PCIE_RX6N	PCIE_TX6N	P32	PEG_RX6_C_DN
PEG_TX7_DP	P35	PCIE_RX7P	PCIE_TX7P	P30	PEG_RX7_C_DP
PEG_TX7_DN	N36	PCIE_RX7N	PCIE_TX7N	P29	PEG_RX7_C_DN
PEG_TX8_DP	N38	PCIE_RX8P	PCIE_TX8P	N33	PEG_RX8_C_DP
PEG_TX8_DN	M37	PCIE_RX8N	PCIE_TX8N	N32	PEG_RX8_C_DN
PEG_TX9_DP	M35	PCIE_RX9P	PCIE_TX9P	N30	PEG_RX9_C_DP
PEG_TX9_DN	L36	PCIE_RX9N	PCIE_TX9N	N29	PEG_RX9_C_DN
PEG_TX10_DP	L38	PCIE_RX10P	PCIE_TX10P	L33	PEG_RX10_C_DP
PEG_TX10_DN	K37	PCIE_RX10N	PCIE_TX10N	L32	PEG_RX10_C_DN
PEG_TX11_DP	K35	PCIE_RX11P	PCIE_TX11P	L30	PEG_RX11_C_DP
PEG_TX11_DN	J36	PCIE_RX11N	PCIE_TX11N	L29	PEG_RX11_C_DN
PEG_TX12_DP	J38	PCIE_RX12P	PCIE_TX12P	K33	PEG_RX12_C_DP
PEG_TX12_DN	H37	PCIE_RX12N	PCIE_TX12N	K32	PEG_RX12_C_DN
PEG_TX13_DP	H35	PCIE_RX13P	PCIE_TX13P	J33	PEG_RX13_C_DP
PEG_TX13_DN	G36	PCIE_RX13N	PCIE_TX13N	J32	PEG_RX13_C_DN
PEG_TX14_DP	G38	PCIE_RX14P	PCIE_TX14P	K30	PEG_RX14_C_DP
PEG_TX14_DN	F37	PCIE_RX14N	PCIE_TX14N	K29	PEG_RX14_C_DN
PEG_TX15_DP	F35	PCIE_RX15P	PCIE_TX15P	H33	PEG_RX15_C_DP
PEG_TX15_DN	E37	PCIE_RX15N	PCIE_TX15N	H32	PEG_RX15_C_DN

CLOCK

CLK_PEG_GPU_REF_DP	AB35	PCIE_REFCLKP
CLK_PEG_GPU_REF_DN	AA36	PCIE_REFCLKN

CALIBRATION

PCIE_CALRP	Y30	R5126 1.27K_1%_2
PCIE_CALRN	Y29	2K_1%_2 R5127

PWRGOOD	AH16	R5003 10K_5%_2
PERSTB	AA30	

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CLOSE TO GPU

PEG_RX0_C_DP	C5128	0.1UF_16V_2
PEG_RX0_C_DN	C5129	0.1UF_16V_2
PEG_RX1_C_DP	C5130	0.1UF_16V_2
PEG_RX1_C_DN	C5131	0.1UF_16V_2
PEG_RX2_C_DP	C5132	0.1UF_16V_2
PEG_RX2_C_DN	C5133	0.1UF_16V_2
PEG_RX3_C_DP	C5134	0.1UF_16V_2
PEG_RX3_C_DN	C5135	0.1UF_16V_2
PEG_RX4_C_DP	C5136	0.1UF_16V_2
PEG_RX4_C_DN	C5137	0.1UF_16V_2
PEG_RX5_C_DP	C5138	0.1UF_16V_2
PEG_RX5_C_DN	C5139	0.1UF_16V_2
PEG_RX6_C_DP	C5140	0.1UF_16V_2
PEG_RX6_C_DN	C5141	0.1UF_16V_2
PEG_RX7_C_DP	C5142	0.1UF_16V_2
PEG_RX7_C_DN	C5143	0.1UF_16V_2
PEG_RX8_C_DP	C5144	0.1UF_16V_2
PEG_RX8_C_DN	C5145	0.1UF_16V_2
PEG_RX9_C_DP	C5146	0.1UF_16V_2
PEG_RX9_C_DN	C5147	0.1UF_16V_2
PEG_RX10_C_DP	C5148	0.1UF_16V_2
PEG_RX10_C_DN	C5149	0.1UF_16V_2
PEG_RX11_C_DP	C5150	0.1UF_16V_2
PEG_RX11_C_DN	C5151	0.1UF_16V_2
PEG_RX12_C_DP	C5004	0.1UF_16V_2
PEG_RX12_C_DN	C5005	0.1UF_16V_2
PEG_RX13_C_DP	C5152	0.1UF_16V_2
PEG_RX13_C_DN	C5153	0.1UF_16V_2
PEG_RX14_C_DP	C5154	0.1UF_16V_2
PEG_RX14_C_DN	C5155	0.1UF_16V_2
PEG_RX15_C_DP	C5156	0.1UF_16V_2
PEG_RX15_C_DN	C5157	0.1UF_16V_2

PEG_RX0_DP	PEG_RX0_DN
PEG_RX1_DP	PEG_RX1_DN
PEG_RX2_DP	PEG_RX2_DN
PEG_RX3_DP	PEG_RX3_DN
PEG_RX4_DP	PEG_RX4_DN
PEG_RX5_DP	PEG_RX5_DN
PEG_RX6_DP	PEG_RX6_DN
PEG_RX7_DP	PEG_RX7_DN
PEG_RX8_DP	PEG_RX8_DN
PEG_RX9_DP	PEG_RX9_DN
PEG_RX10_DP	PEG_RX10_DN
PEG_RX11_DP	PEG_RX11_DN
PEG_RX12_DP	PEG_RX12_DN
PEG_RX13_DP	PEG_RX13_DN
PEG_RX14_DP	PEG_RX14_DN
PEG_RX15_DP	PEG_RX15_DN

P1V0_GPU

P3V3_S

C5000 0.1UF_16V_2

U5001 TC7SZ08FU

DGPU_HOLD_RST# (IN)

PLT_RST# (IN)

PEG_PLT_RST#

R5125 100K_5%_2

R5002 0_5%_2_DY

GEN2:
PCI EXPRESS BUS:TRANSMITTED/RECEIVER
UP TO 5.0-GT/S BIT RATE.

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 85 of 97

IF GPU_GPIO22 = 0, THEN GPIO[13:11] DEFINES THE PRIMARY MEMORY APERTURE SIZE			
GPU_GPIO13	GPU_GPIO12	GPU_GPIO11	MEMORY APERTURE SIZE
0	0	1	256 MB (DEFAULT)
0	0	0	128 MB
0	1	0	64 MB
0	1	1	32 MB

MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	Vendor (GDDR5)
0	0	1	1	HYNIX (1GB)
0	0	0	1	SAMSUNG (1GB)

VID1	VID0	+VDDC_GPU
POW_SW1	POW_SW0	PCORE_GPU
0	0	1.05V
0	1	1.00V
1	0	0.90V

For XT

VID1	VID0	+VDDC_GPU
POW_SW1	POW_SW0	PCORE_GPU
0	1	1.00V
1	0	0.90V

For PRO

P3V3_GPUS

R5167 10K_5%_2 OUT GPU_GPIO0
R5168 10K_5%_2 OUT GPU_GPIO1
R5019 10K_5%_2_DY OUT GPU_GPIO2
R5169 10K_5%_2 IN GPU_THERM_INT# [ALERT]
R5170 10K_5%_2_DY OUT GPU_GPIO22
R5171 10K_5%_2 OUT GPU_GPIO11
R5172 10K_5%_2_DY OUT GPU_GPIO12
R5173 10K_5%_2_DY OUT GPU_GPIO13
R5174 10K_5%_2_DY OUT GPU_GPIO23
R5175 10K_5%_2_DY OUT GPU_GPIO9
R5176 10K_5%_2_DY OUT GPU_GPIO5
R5177 10K_5%_2 OUT GPU_CRT_HSYNC
R5178 10K_5%_2 OUT GPU_CRT_VSYNC
HDMI&DP Audio
R5179 10K_5%_2_DY OUT GPU_GPIO21

R5158 10K_5%_2 IN GPU_GPIO19
R5159 10K_5%_2 IN GPU_LCM_BKLTEN
R5161 10K_5%_2 IN POW_SW0
R5163 10K_5%_2 IN POW_SW1

SWING: 1.8V

CLK_GPU_27M IN R5009 0_5%_2_DY
X5015 27MHZ_12PF XTAL_4PIN
C5011 15PF_50V_2
C5166 15PF_50V_2
R5016 1M_5%_2
U5017 ICS_ICLK X2 VDD_100M VDD_27M GPU_XOIN2_100M 100M GPU_XOIN_27M 27M S0 S1 GND_PLL GND_27M TML
IDT_6V40088_DFN_10P
R5022 33_5%_2 OUT GPU_XOIN2_100M_R
R5023 33_5%_2 OUT GPU_XOIN_27M_R

P3V3_GPUS
FBM_11_160808_121T L5007 3.3V,0.05A
C5006 10UF_6.3V_3
C5161 0.1UF_16V_2
C5163 0.1UF_16V_2
R5010 0_5%_2
R5012 0_5%_2
32 KHZ SPREAD SPECTRUM MODULATION

SWING: 3.3V

P3V3_GPUS
R5160 10K_5%_2_DY
R5162 10K_5%_2_DY
R5164 10K_5%_2_DY
R5165 10K_5% TP24
OUT GPU_JTAG_TDO
OUT GPU_JTAG_TDI
OUT GPU_JTAG_TRSTB
OUT GPU_JTAG_TMS
OUT GPU_JTAG_TCK
R5008 10K_5%_2
JTAG MODE

P3V3_GPUS
C5013 0.1UF_16V_2
C5014 2200PF_50V_3
U5018 VCC DXP DXN THERM# SMBCLK SMBDATA ALERT# GND
GMT_G784_MSOP_8P
THRM_GPU_DP IN
THRM_GPU_DN IN
THRM_SHUTDWN# OUT
R5020 0_5%_2_DY BI GPU_THM_CLK
R5021 0_5%_2_DY BI GPU_THM_DAT
BI EC_SMB2_CLK
BI EC_SMB2_DATA

P1V8_GPUS
R5029 10K_5%_2_DY
R5030 10K_5%_2_DY
R5187 10K_5%_2
R5191 10K_5%_2
MEM_ID0 MEM_ID1 MEM_ID2 MEM_ID3

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MUTI GFX
DVPCNTL_MVP_0 AR8
DVPCNTL_MVP_1 AU8
DVPCNTL_0 AP8
DVPCNTL_1 AW8
DVPCNTL_2 AR3
DVPCLK AR1
DVPDATA_0 AU1
DVPDATA_1 AU3
DVPDATA_2 AW3
DVPDATA_3 AP6
DVPDATA_4 AW5
DVPDATA_5 AU5
DVPDATA_6 AR6
DVPDATA_7 AW6
DVPDATA_8 AU6
DVPDATA_9 AT7
DVPDATA_10 AV7
DVPDATA_11 AN7
DVPDATA_12 AV9
DVPDATA_13 AT9
DVPDATA_14 AR10
DVPDATA_15 AW10
DVPDATA_16 AU10
DVPDATA_17 AP10
DVPDATA_18 AV11
DVPDATA_19 AT11
DVPDATA_20 AR12
DVPDATA_21 AW12
DVPDATA_22 AU12
DVPDATA_23 AP12
SWAPLOCKA AJ21
SWAPLOCKB AK21

I2C
TP5189 TP24 AK26 SCL
TP5190 TP24 AJ26 SDA

GENERAL PURPOSE I/O
GPU_GPIO0 OUT AH20 GPIO_0
GPU_GPIO1 OUT AH18 GPIO_1
GPU_GPIO2 OUT AN16 GPIO_2
GPU_THM_DAT BI AH23 GPIO_3_SMBDATA
GPU_THM_CLK BI AJ23 GPIO_4_SMBCLK
GPU_GPIO5 IN AH17 GPIO_5_AC_BATT
GPU_LCM_BKLTEN OUT AJ17 GPIO_6
AK17 GPIO_7_BLON
AJ13 GPIO_8_ROMSO
GPU_GPIO9 IN AH15 GPIO_9_ROMSI
AJ16 GPIO_10_ROMSCK
GPU_GPIO11 IN AK16 GPIO_11
GPU_GPIO12 IN AL16 GPIO_12
GPU_GPIO13 IN AM16 GPIO_13
GPU_EDP_HPD IN AM14 GPIO_14_HPD2
POW_SW0 OUT AM13 GPIO_15_PWRCNTL_0
AK14 GPIO_16
GPU_THERM_INT# OUT AG30 GPIO_17_THERMAL_INT
AN14 GPIO_18_HPD3
GPU_GPIO19 OUT AM17 GPIO_19_CTF
POW_SW1 OUT AL13 GPIO_20_PWRCNTL_1
GPU_GPIO21 IN AJ14 GPIO_21_BB_EN
GPU_GPIO22 IN AK13 GPIO_22_ROMCSB
GPU_GPIO23 IN AN13 GPIO_23_CLKREQB
GPU_JTAG_TRSTB IN AM23 JTAG_TRSTB
GPU_JTAG_TDI IN AN23 JTAG_TDI
GPU_JTAG_TCK IN AK23 JTAG_TCK
GPU_JTAG_TMS IN AL24 JTAG_TMS
GPU_JTAG_TDO IN AM24 JTAG_TDO
TP5035 TP24 AJ19 GENERICA
AK19 GENERICB
TP5036 TP24 AJ20 GENERICC
AK20 GENERICD
AJ24 GENERICE_HPD4
AH26 GENERICF_HPD5
AH24 GENERICG_HPD6

GPU_HDMI_HPD1 IN AK24 HPD1

P1V8_GPUS
R5185 499_1%_2
C5033 0.1UF_16V_2
R5034 249_1%_2 CLOSE TO GPU AH13 VREFG

P1V8_GPUS
L5181 FBM_11_160808_121T I=0.075A
C5183 10UF_6.3V_3
C5184 1UF_6.3V_2
C5028 0.1UF_16V_2
DPLL_PVDD AM32
DPLL_PVSS AN32

P1V0_GPU
L5180 FBM_11_160808_121T I=0.125A
C5026 10UF_6.3V_3
C5182 1UF_6.3V_2
C5027 0.1UF_16V_2
DPLL_VDDC AN31 DPLL_VDDC
PLL/CLOCK
TP5031 TP24 AV33 XTALIN
TP5032 TP24 AU34 XTALOUT

P1V8_GPUS
R5024 10K_5%_2_DY
R5025 10K_5%_2_DY
GPU_TS_FDO IN
MLPS option for future ASIC
GPU_XOIN_27M_R IN AW34 XO_IN
GPU_XOIN2_100M_R IN AW35 XO_IN2

THERMAL
THRM_GPU_DP OUT AF29 DPLUS
THRM_GPU_DN OUT AG29 DMINUS
GPU_TS_FDO OUT AK32 TS_FDO
AL31 TS_A/NC

P1V8_GPUS
L5186 FBM_11_160808_121T I=0.005A
TSVDD
C5188 10UF_6.3V_3
C5192 1UF_6.3V_2
C5193 0.1UF_16V_2
TSVDD AJ32
TSVSS AJ33

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DPA
TXCAP_DPA3P AU24 GPU_HDMI_TXC_DP
TXCAM_DPA3N AV23 GPU_HDMI_TXC_DN
TX0P_DPA2P AT25 GPU_HDMI_TX0_DP
TX0M_DPA2N AR24 GPU_HDMI_TX0_DN
TX1P_DPA1P AU26 GPU_HDMI_TX1_DP
TX1M_DPA1N AV25 GPU_HDMI_TX1_DN
TX2P_DPA0P AT27 GPU_HDMI_TX2_DP
TX2M_DPA0N AR26 GPU_HDMI_TX2_DN
HDMI

DPB
TXCBP_DPB3P AR30
TXCBM_DPB3N AT29
TX3P_DPB2P AV31
TX3M_DPB2N AU30
TX4P_DPB1P AR32 GPU_EDP_TX1_DP
TX4M_DPB1N AT31 GPU_EDP_TX1_DN
TX5P_DPB0P AT33 GPU_EDP_TX0_DP
TX5M_DPB0N AU32 GPU_EDP_TX0_DN
EDP
DUAL CHANNEL FOR 3D FUNCTION

DPC
TXCCP_DPC3P AU14
TXCCM_DPC3N AV13
TX0P_DPC2P AT15
TX0M_DPC2N AR14
TX1P_DPC1P AU16
TX1M_DPC1N AV15
TX2P_DPC0P AT17
TX2M_DPC0N AR16

DPD
TXCDP_DPD3P AU20
TXCDM_DPD3N AT19
TX3P_DPD2P AT21
TX3M_DPD2N AR20
TX4P_DPD1P AU22
TX4M_DPD1N AV21
TX5P_DPD0P AT23
TX5M_DPD0N AR22

CLOSE TO GPU
R5194 150_1%_2
R5196 150_1%_2
R5197 150_1%_2

DAC1
R AD39 GPU_CRT_R
RB AD37
G AE36 GPU_CRT_G
GB AD35
B AF37 GPU_CRT_B
BB AE38
HSYNC AC36 GPU_CRT_HSYNC
VSYNC AC38 GPU_CRT_VSYNC
CRT
RSET AB34 R5195 499_1%_2 Away from noisy GND area.

AVDD AD34 AVDD I=0.07A L5042 P1V8_GPUS
AVSSQ AE34
FBM_11_160808_121T
C5198 10UF_6.3V_3
C5200 0.1UF_16V_2
C5204 1UF_6.3V_2
Away from noisy GND area.
VDD1DI AC33 VDD1D1 I=0.045A L5207 P1V8_GPUS
VSS1DI AC34
FBM_11_160808_121T
C5199 10UF_6.3V_3
C5201 0.1UF_16V_2
C5205 1UF_6.3V_2

R2/NC AC30
R2B/NC AC31 OUT GPU_PS1
G2/NC AD30
G2B/NC AD31 R5037 0_5%_2_DY
B2/NC AF30
B2B/NC AF31 R5038 0_5%_2_DY
C/NC AC32
Y/NC AD32
COMP/NC AF32

DAC2
H2SYNC/GENLK_CLK AD29
V2SYNC/GENLK_VSYNC AC29
1.8V,0.1A
VDD2DI/NC AG31 OUT GPU_PS2
VSS2DI/NC AG32 R5039 0_5%_2_DY P3V3_GPUS
A2VDD/NC AG33 R5040 0_5%_3_DY 3.3V,0.13A
A2VDDQ/NC AD33 OUT GPU_PS3
A2VSSQ/TSVSSQ AF33
R2SET/NC AA29 R5041 715_1%_2_DY Away from noisy GND area.

DDC/AUX
DDC1CLK AM26 BI GPU_HDMI_DDCCLK
DDC1DATA AN26 BI GPU_HDMI_DDCDATA
AUX1P AM27
AUX1N AL27
DDC2CLK AM19
DDC2DATA AL19
AUX2P AN20 BI GPU_EDP_AUX_DP
AUX2N AM20 BI GPU_EDP_AUX_DN
DDCCLK_AUX3P AL30
DDCDATA_AUX3N AM30
DDCCLK_AUX4P AL29
DDCDATA_AUX4N AM29
DDCCLK_AUX5P AN21 BI GPU_CRT_DDCCLK
DDCDATA_AUX5N AM21 BI GPU_CRT_DDCDATA
DDC6CLK AJ30
DDC6DATA AJ31
DDCCLK_AUX7P AK30
DDCDATA_AUX7N AK29

P1V8_GPUS
R5202 10K_5%_2_DY
R5208 0_5%_3_DY
R5211 10K_5%_2_DY
GPU_PS1 IN
GPU_PS2 IN
GPU_PS3 IN
R5203 10K_5%_2_DY
C5206 0.1UF_16V_2_DY
R5209 10K_5%_2_DY
C5210 0.1UF_16V_2_DY
R5212 10K_5%_2_DY
C5213 0.1UF_16V_2_DY

FUTURE ASIC
GPU Multi Level Pin Straps feature

INVENTEC
TITLE MODEL,PROJECT,FUNCTION Block Diagram
SIZE C CODE CS DOC.NUMBER CS_1310AXXXXXX_MTR REV A01
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CHANNEL A

U5124

VM_A0_ADA<31..0>

0	VM_A0_ADA<0>	C37
1	VM_A0_ADA<1>	C35
2	VM_A0_ADA<2>	A35
3	VM_A0_ADA<3>	E34
4	VM_A0_ADA<4>	G32
5	VM_A0_ADA<5>	D33
6	VM_A0_ADA<6>	F32
7	VM_A0_ADA<7>	E32
8	VM_A0_ADA<8>	D31
9	VM_A0_ADA<9>	F30
10	VM_A0_ADA<10>	C30
11	VM_A0_ADA<11>	A30
12	VM_A0_ADA<12>	F28
13	VM_A0_ADA<13>	C28
14	VM_A0_ADA<14>	A28
15	VM_A0_ADA<15>	E28
16	VM_A0_ADA<16>	D27
17	VM_A0_ADA<17>	F26
18	VM_A0_ADA<18>	C26
19	VM_A0_ADA<19>	A26
20	VM_A0_ADA<20>	F24
21	VM_A0_ADA<21>	C24
22	VM_A0_ADA<22>	A24
23	VM_A0_ADA<23>	E24
24	VM_A0_ADA<24>	C22
25	VM_A0_ADA<25>	A22
26	VM_A0_ADA<26>	F22
27	VM_A0_ADA<27>	D21
28	VM_A0_ADA<28>	A20
29	VM_A0_ADA<29>	F20
30	VM_A0_ADA<30>	D19
31	VM_A0_ADA<31>	E18

VM_A1_ADA<31..0>

0	VM_A1_ADA<0>	C18
1	VM_A1_ADA<1>	A18
2	VM_A1_ADA<2>	F18
3	VM_A1_ADA<3>	D17
4	VM_A1_ADA<4>	A16
5	VM_A1_ADA<5>	F16
6	VM_A1_ADA<6>	D15
7	VM_A1_ADA<7>	E14
8	VM_A1_ADA<8>	F14
9	VM_A1_ADA<9>	D13
10	VM_A1_ADA<10>	F12
11	VM_A1_ADA<11>	A12
12	VM_A1_ADA<12>	D11
13	VM_A1_ADA<13>	F10
14	VM_A1_ADA<14>	A10
15	VM_A1_ADA<15>	C10
16	VM_A1_ADA<16>	G13
17	VM_A1_ADA<17>	H13
18	VM_A1_ADA<18>	J13
19	VM_A1_ADA<19>	H11
20	VM_A1_ADA<20>	G10
21	VM_A1_ADA<21>	G8
22	VM_A1_ADA<22>	K9
23	VM_A1_ADA<23>	K10
24	VM_A1_ADA<24>	G9
25	VM_A1_ADA<25>	A8
26	VM_A1_ADA<26>	C8
27	VM_A1_ADA<27>	E8
28	VM_A1_ADA<28>	A6
29	VM_A1_ADA<29>	C6
30	VM_A1_ADA<30>	E6
31	VM_A1_ADA<31>	A5

DDR2 GDDR3/GDDR5 DDR3

DQA0_0/DQA_0 … DQA0_7/DQA_7 DQA0_8/DQA_8 … DQA0_15/DQA_15 DQA0_16/DQA_16 … DQA0_23/DQA_23 DQA0_24/DQA_24 … DQA0_31/DQA_31

DQA1_0/DQA_32 … DQA1_7/DQA_39 DQA1_8/DQA_40 … DQA1_15/DQA_47 DQA1_16/DQA_48 … DQA1_23/DQA_55 DQA1_24/DQA_56 … DQA1_31/DQA_63

MEMORY INTERFACE A

MVREFDA L18
MVREFSA L20

MEM_CALRN0 L27
MEM_CALRN1 N12
MEM_CALRN2 AG12

MEM_CALRP1 M12
MEM_CALRP0 M27
MEM_CALRP2 AH12

DDR2 GDDR5/GDDR3 DDR3

MAA0_0/MAA_0	G24	VM_A0_AA<0>
MAA0_1/MAA_1	J23	VM_A0_AA<1>
MAA0_2/MAA_2	H24	VM_A0_AA<2>
MAA0_3/MAA_3	J24	VM_A0_AA<3>
MAA0_4/MAA_4	H26	VM_A0_AA<4>
MAA0_5/MAA_5	J26	VM_A0_AA<5>
MAA0_6/MAA_6	H21	VM_A0_AA<6>
MAA0_7/MAA_7	G21	VM_A0_AA<7>
MAA1_0/MAA_8	H19	VM_A1_AA<0>
MAA1_1/MAA_9	H20	VM_A1_AA<1>
MAA1_2/MAA_10	L13	VM_A1_AA<2>
MAA1_3/MAA_11	G16	VM_A1_AA<3>
MAA1_4/MAA_12	J16	VM_A1_AA<4>
MAA1_5/MAA_13_BA2	H16	VM_A1_AA<5>
MAA1_6/MAA_14_BA0	J17	VM_A1_AA<6>
MAA1_7/MAA_A15_BA1	H17	VM_A1_AA<7>

VM_A0_AA<7..0>

VM_A1_AA<7..0>

WCKA0_0/DQMA_0	A32
WCKA0B_0/DQMA_1	C32
WCKA0_1/DQMA_2	D23
WCKA0B_1/DQMA_3	E22
WCKA1_0/DQMA_4	C14
WCKA1B_0/DQMA_5	A14
WCKA1_1/DQMA_6	E10
WCKA1B_1/DQMA_7	D9

VM_WCKA0_0_DP
VM_WCKA0_0_DN
VM_WCKA0_1_DP
VM_WCKA0_1_DN
VM_WCKA1_0_DP
VM_WCKA1_0_DN
VM_WCKA1_1_DP
VM_WCKA1_1_DN

GDDR5/DDR2/GDDR3

EDCA0_0/QSA_0/RDQSA_0	C34
EDCA0_1/QSA_1/RDQSA_1	D29
EDCA0_2/QSA_2/RDQSA_2	D25
EDCA0_3/QSA_3/RDQSA_3	E20
EDCA1_0/QSA_4/RDQSA_4	E16
EDCA1_1/QSA_5/RDQSA_5	E12
EDCA1_2/QSA_6/RDQSA_6	J10
EDCA1_3/QSA_7/RDQSA_7	D7

VM_EDCA0_0
VM_EDCA0_1
VM_EDCA0_2
VM_EDCA0_3
VM_EDCA1_0
VM_EDCA1_1
VM_EDCA1_2
VM_EDCA1_3

DDBIA0_0/QSA_0B/WDQSA_0	A34
DDBIA0_1/QSA_1B/WDQSA_1	E30
DDBIA0_2/QSA_2B/WDQSA_2	E26
DDBIA0_3/QSA_3B/WDQSA_3	C20
DDBIA1_0/QSA_4B/WDQSA_4	C16
DDBIA1_1/QSA_5B/WDQSA_5	C12
DDBIA1_2/QSA_6B/WDQSA_6	J11
DDBIA1_3/QSA_7B/WDQSA_7	F8

VM_DDBIA0_0
VM_DDBIA0_1
VM_DDBIA0_2
VM_DDBIA0_3
VM_DDBIA1_0
VM_DDBIA1_1
VM_DDBIA1_2
VM_DDBIA1_3

ADBIA0/ODTA0	J21
ADBIA1/ODTA1	G19

VM_ADBIA0
VM_ADBIA1

CLKA0	H27
CLKA0B	G27
CLKA1	J14
CLKA1B	H14
RASA0B	K23
RASA1B	K19
CASA0B	K20
CASA1B	K17
CSA0B_0	K24
CSA0B_1	K27
CSA1B_0	M13
CSA1B_1	K16
CKEA0	K21
CKEA1	J20
WEA0B	K26
WEA1B	L15

DDR_A_CLKA0_DP
DDR_A_CLKA0_DN
DDR_A_CLKA1_DP
DDR_A_CLKA1_DN
DDR_A_RASA0#
DDR_A_RASA1#
DDR_A_CASA0#
DDR_A_CASA1#
DDR_A_CSA0#_0
DDR_A_CSA1#_0
DDR_A_CKEA0
DDR_A_CKEA1
DDR_A_WEA0#
DDR_A_WEA1#

GDDR5

MAA0_8	H23
MAA1_8	J19

VM_A0_AA<8>
VM_A1_AA<8>

AMD_216_0810_001_FCBGA_962P

P1V5_GPUS

R5043 40.2_1%_2

MVREFDA_GPU

R5214 100_1%_2 C5216 0.1UF_16V_2

R & CAPS CLOSE TO GPU

P1V5_GPUS

R5044 40.2_1%_2

MVREFSA_GPU

R5215 100_1%_2 C5217 0.1UF_16V_2

R & CAPS CLOSE TO GPU

P1V5_GPUS

R5045 243_1%_2
R5218 243_1%_2
R5219 243_1%_2
R5220 243_1%_2
R5221 243_1%_2
R5222 243_1%_2

INVENTEC

TITLE: MODEL PRODUCTION FUNCTION

Block Diagram

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0 CS_1310AXXXXXX-MTR	X01 A01

CHANGE by XXX BEN LEE DATE February 22, 2010

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CHANNEL B

U5124

VM_B0_ADA<31..0> → BI

0	VM_B0_ADA<0>	C5
1	VM_B0_ADA<1>	C3
2	VM_B0_ADA<2>	E3
3	VM_B0_ADA<3>	E1
4	VM_B0_ADA<4>	F1
5	VM_B0_ADA<5>	F3
6	VM_B0_ADA<6>	F5
7	VM_B0_ADA<7>	G4
8	VM_B0_ADA<8>	H5
9	VM_B0_ADA<9>	H6
10	VM_B0_ADA<10>	J4
11	VM_B0_ADA<11>	K6
12	VM_B0_ADA<12>	K5
13	VM_B0_ADA<13>	L4
14	VM_B0_ADA<14>	M6
15	VM_B0_ADA<15>	M1
16	VM_B0_ADA<16>	M3
17	VM_B0_ADA<17>	M5
18	VM_B0_ADA<18>	N4
19	VM_B0_ADA<19>	P6
20	VM_B0_ADA<20>	P5
21	VM_B0_ADA<21>	R4
22	VM_B0_ADA<22>	T6
23	VM_B0_ADA<23>	T1
24	VM_B0_ADA<24>	U4
25	VM_B0_ADA<25>	V6
26	VM_B0_ADA<26>	V1
27	VM_B0_ADA<27>	V3
28	VM_B0_ADA<28>	Y6
29	VM_B0_ADA<29>	Y1
30	VM_B0_ADA<30>	Y3
31	VM_B0_ADA<31>	Y5

VM_B1_ADA<31..0> → BI

0	VM_B1_ADA<0>	AA4
1	VM_B1_ADA<1>	AB6
2	VM_B1_ADA<2>	AB1
3	VM_B1_ADA<3>	AB3
4	VM_B1_ADA<4>	AD6
5	VM_B1_ADA<5>	AD1
6	VM_B1_ADA<6>	AD3
7	VM_B1_ADA<7>	AD5
8	VM_B1_ADA<8>	AF1
9	VM_B1_ADA<9>	AF3
10	VM_B1_ADA<10>	AF6
11	VM_B1_ADA<11>	AG4
12	VM_B1_ADA<12>	AH5
13	VM_B1_ADA<13>	AH6
14	VM_B1_ADA<14>	AJ4
15	VM_B1_ADA<15>	AK3
16	VM_B1_ADA<16>	AF8
17	VM_B1_ADA<17>	AF9
18	VM_B1_ADA<18>	AG8
19	VM_B1_ADA<19>	AG7
20	VM_B1_ADA<20>	AK9
21	VM_B1_ADA<21>	AL7
22	VM_B1_ADA<22>	AM8
23	VM_B1_ADA<23>	AM7
24	VM_B1_ADA<24>	AK1
25	VM_B1_ADA<25>	AL4
26	VM_B1_ADA<26>	AM6
27	VM_B1_ADA<27>	AM1
28	VM_B1_ADA<28>	AN4
29	VM_B1_ADA<29>	AP3
30	VM_B1_ADA<30>	AP1
31	VM_B1_ADA<31>	AP5

DDR2 GDDR3/GDDR5 DDR3 — MEMORY INTERFACE B

DQB0_0/DQB_0 … DQB0_7/DQB_7 … DQB0_8/DQB_8 … DQB0_9/DQB_9 … DQB0_10/DQB_10 … DQB0_11/DQB_11 … DQB0_12/DQB_12 … DQB0_13/DQB_13 … DQB0_14/DQB_14 … DQB0_15/DQB_15 … DQB0_16/DQB_16 … DQB0_17/DQB_17 … DQB0_18/DQB_18 … DQB0_19/DQB_19 … DQB0_20/DQB_20 … DQB0_21/DQB_21 … DQB0_22/DQB_22 … DQB0_23/DQB_23 … DQB0_24/DQB_24 … DQB0_25/DQB_25 … DQB0_26/DQB_26 … DQB0_27/DQB_27 … DQB0_28/DQB_28 … DQB0_29/DQB_29 … DQB0_30/DQB_30 … DQB0_31/DQB_31

DQB1_0/DQB_32 … DQB1_1/DQB_33 … DQB1_2/DQB_34 … DQB1_3/DQB_35 … DQB1_4/DQB_36 … DQB1_5/DQB_37 … DQB1_6/DQB_38 … DQB1_7/DQB_39 … DQB1_8/DQB_40 … DQB1_9/DQB_41 … DQB1_10/DQB_42 … DQB1_11/DQB_43 … DQB1_12/DQB_44 … DQB1_13/DQB_45 … DQB1_14/DQB_46 … DQB1_15/DQB_47 … DQB1_16/DQB_48 … DQB1_17/DQB_49 … DQB1_18/DQB_50 … DQB1_19/DQB_51 … DQB1_20/DQB_52 … DQB1_21/DQB_53 … DQB1_22/DQB_54 … DQB1_23/DQB_55 … DQB1_24/DQB_56 … DQB1_25/DQB_57 … DQB1_26/DQB_58 … DQB1_27/DQB_59 … DQB1_28/DQB_60 … DQB1_29/DQB_61 … DQB1_30/DQB_62 … DQB1_31/DQB_63

MVREFDB ← Y12
MVREFSB ← AA12
TESTEN ← AD28
CLKTESTA ← AK10
CLKTESTB ← AL10

DDR2 GDDR5/GDDR3 DDR3

MAB0_0/MAB_0	P8	VM_B0_AA<0>
MAB0_1/MAB_1	T9	VM_B0_AA<1>
MAB0_2/MAB_2	P9	VM_B0_AA<2>
MAB0_3/MAB_3	N7	VM_B0_AA<3>
MAB0_4/MAB_4	N8	VM_B0_AA<4>
MAB0_5/MAB_5	N9	VM_B0_AA<5>
MAB0_6/MAB_6	U9	VM_B0_AA<6>
MAB0_7/MAB_7	U8	VM_B0_AA<7>
MAB1_0/MAB_8	Y9	VM_B1_AA<0>
MAB1_1/MAB_9	W9	VM_B1_AA<1>
MAB1_2/MAB_10	AC8	VM_B1_AA<2>
MAB1_3/MAB_11	AC9	VM_B1_AA<3>
MAB1_4/MAB_12	AA7	VM_B1_AA<4>
MAB1_5/BA2	AA8	VM_B1_AA<5>
MAB1_6/BA0	Y8	VM_B1_AA<6>
MAB1_7/BA1	AA9	VM_B1_AA<7>

VM_B0_AA<7..0> → BI
VM_B1_AA<7..0> → BI

WCKB0_0/DQMB_0	H3	VM_WCKB0_0_DP
WCKB0B_0/DQMB_1	H1	VM_WCKB0_0_DN
WCKB0_1/DQMB_2	T3	VM_WCKB0_1_DP
WCKB0B_1/DQMB_3	T5	VM_WCKB0_1_DN
WCKB1_0/DQMB_4	AE4	VM_WCKB1_0_DP
WCKB1B_0/DQMB_5	AF5	VM_WCKB1_0_DN
WCKB1_1/DQMB_6	AK6	VM_WCKB1_1_DP
WCKB1B_1/DQMB_7	AK5	VM_WCKB1_1_DN

GDDR5/DDR2/GDDR3

EDCB0_0/QSB_0/RDQSB_0	F6	VM_EDCB0_0
EDCB0_1/QSB_1/RDQSB_1	K3	VM_EDCB0_1
EDCB0_2/QSB_2/RDQSB_2	P3	VM_EDCB0_2
EDCB0_3/QSB_3/RDQSB_3	V5	VM_EDCB0_3
EDCB1_0/QSB_4/RDQSB_4	AB5	VM_EDCB1_0
EDCB1_1/QSB_5/RDQSB_5	AH1	VM_EDCB1_1
EDCB1_2/QSB_6/RDQSB_6	AJ9	VM_EDCB1_2
EDCB1_3/QSB_7/RDQSB_7	AM5	VM_EDCB1_3

DDBIB0_0/QSB_0B/WDQSB_0	G7	VM_DDBIB0_0
DDBIB0_1/QSB_1B/WDQSB_1	K1	VM_DDBIB0_1
DDBIB0_2/QSB_2B/WDQSB_2	P1	VM_DDBIB0_2
DDBIB0_3/QSB_3B/WDQSB_3	W4	VM_DDBIB0_3
DDBIB1_0/QSB_4B/WDQSB_4	AC4	VM_DDBIB1_0
DDBIB1_1/QSB_5B/WDQSB_5	AH3	VM_DDBIB1_1
DDBIB1_2/QSB_6B/WDQSB_6	AJ8	VM_DDBIB1_2
DDBIB1_3/QSB_7B/WDQSB_7	AM3	VM_DDBIB1_3

ADBIB0/ODTB0	T7	VM_ADBIB0
ADBIB1/ODTB1	W7	VM_ADBIB1

CLKB0	L9	DDR_B_CLKB0_DP
CLKB0B	L8	DDR_B_CLKB0_DN
CLKB1	AD8	DDR_B_CLKB1_DP
CLKB1B	AD7	DDR_B_CLKB1_DN
RASB0B	T10	DDR_B_RASB0#
RASB1B	Y10	DDR_B_RASB1#
CASB0B	W10	DDR_B_CASB0#
CASB1B	AA10	DDR_B_CASB1#
CSB0B_0	P10	DDR_B_CSB0#_0
CSB0B_1	L10	
CSB1B_0	AD10	DDR_B_CSB1#_0
CSB1B_1	AC10	
CKEB0	U10	DDR_B_CKEB0
CKEB1	AA11	DDR_B_CKEB1
WEB0B	N10	DDR_B_WEB0#
WEB1B	AB11	DDR_B_WEB1#

GDDR5

MAB0_8	T8	VM_B0_AA<8>
MAB1_8	W8	VM_B1_AA<8>
DRAM_RST	AH11	VM_RESET_R1

VM_RESET_R1 — R5053 10_1%_2 — VM_RESET_R2 — R5055 51_1%_2 → OUT VM_RESET
VM_RESET_R2 — R5052 5K_1%_2 — C5054 120PF_50V_2

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P1V5_GPUS — R5046 40.2_1%_2 — MVREFDB_GPU — R5223 100_1%_2 — C5225 0.1UF_16V_2

R & CAPS CLOSE TO GPU

P1V5_GPUS — R5047 40.2_1%_2 — MVREFSB_GPU — R5224 100_1%_2 — C5226 0.1UF_16V_2

R & CAPS CLOSE TO GPU

GPU_TESTEN — P3V3_GPUS — R5048 10K_5%_2_DY — R5049 5.11K_1%_2

C5227 0.1UF_16V_2_DY — R5050 51_1%_2_DY
C5228 0.1UF_16V_2_DY — R5051 51_1%_2_DY

DEBUG ONLY

JTAG SIGNAL STUFF OPTION

SIGNALS	NORMAL MODE	JTAG MODE
GPU_TESTEN	0	1

PLACE ALL THESE COMPONENTS VERY CLOSE TO GPU (WITHIN 25MM) AND KEEP ALL COMPONENT CLOSE TO EACH OTHER. (WITHIN 5MM) EXCEPT RSER2

INVENTEC

TITLE: MODEL PRODUCTION FUNCTION (Module Block Diagram)

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0 CS_1310AXXXXXX-MTR	X01 A01

CHANGE by XXX BEN LEE DATE February 22, 2010 (Draft-2002)

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GPU POWER

U5124

P1V5_GPUS

GDDR5 900MHZ,1.5V,2.3A(PEAK)

C5234 C5237 C5240 C5246 C5247 C5251 C5253 C5258 C5265 C5270 1UF_6.3V_2

C5229 C5232 C5236 C5239 C5241 C5244 0.1UF_16V_2

C5248 C5252 C5254 C5259 C5266 C5271 10UF_6.3V_3

STITCHING CAPS OPTION FOR MEM SIGNALS
THAT HAVE A CHANGE OF REFERENCE PLANE
VOLTAGE.ADD STITCHING CAPS WHEN REQUIRED,
ONE CAP PER THREE SIGNALS

MEM I/O

AC7 AD11 AF7 AG10 AJ7 AK8 AL9 G11 G14 G17 G20 G23 G26 G29 H10 J7 J9 K11 K13 K8 L12 L16 L21 L23 L26 L7 M11 N11 P7 R11 U11 U7 Y11 Y7
VDDR1#1 VDDR1#2 VDDR1#3 VDDR1#4 VDDR1#5 VDDR1#6 VDDR1#7 VDDR1#8 VDDR1#9 VDDR1#10 VDDR1#11 VDDR1#12 VDDR1#13 VDDR1#14 VDDR1#15 VDDR1#16 VDDR1#17 VDDR1#18 VDDR1#19 VDDR1#20 VDDR1#21 VDDR1#22 VDDR1#23 VDDR1#24 VDDR1#25 VDDR1#26 VDDR1#27 VDDR1#28 VDDR1#29 VDDR1#30 VDDR1#31 VDDR1#32 VDDR1#33 VDDR1#34

LEVEL TRANSLATION

P1V8_GPUS

L5249 FBM_11_160808_121T

1.8V,0.017A

C5255 C5261 10UF_6.3V_3 C5059 0.1UF_16V_2 C5272 1UF_6.3V_2

VDD_CT

AF26 AF27 AG26 AG27
VDD_CT#1 VDD_CT#2 VDD_CT#3 VDD_CT#4

P3V3_GPUS

3.3V,0.06A

C5256 C5262 10UF_6.3V_3 C5268 C5273 1UF_6.3V_2

I/O

AF23 AF24 AG23 AG24
VDDR3#1 VDDR3#2 VDDR3#3 VDDR3#4

P1V8_GPUS

L5230 FBM_11_160808_121T

PCIE_PVDD

1.8V,0.04A

C5231 10UF_6.3V_3 C5235 1UF_6.3V_2 C5056 0.1UF_16V_2

P1V8_GPUS

L5250 FBM_11_160808_121T

1.8V,0.17A

VDDR4

Follow GDDR3 ORB

C5263 10UF_6.3V_3 C5269 1UF_6.3V_2 C5274 1UF_6.3V_2

AF13 AF15 AG13 AG15
VDDR4#4 VDDR4#5 VDDR4#7 VDDR4#8

AD12 AF11 AF12 AG11
VDDR4#1 VDDR4#2 VDDR4#3 VDDR4#6

P1V8_GPUS

L5233 FBM_11_160808_121T

1.8V,0.05A

C5238 10UF_6.3V_3 C5242 1UF_6.3V_2 C5245 0.1UF_16V_2

P1V8_GPUS

L5057 FBM_11_160808_121T

1.8V,0.15A

MVP18

C5257 10UF_6.3V_3 C5058 1UF_6.3V_2 C5264 1UF_6.3V_2 C5060 0.1UF_16V_2 C5276 0.1UF_16V_2

M20 M21 NC_VDDRHA NC_VSSRHA
V12 U12 NC_VDDRHB NC_VSSRHB

PLL

H7 H8 MPV18#1 MPV18#2

P1V0_GPU

L5243 FBM_11_160808_121T

1.0V,0.1A

SPV18

C5260 10UF_6.3V_3 C5267 1UF_6.3V_2 C5275 0.1UF_16V_2

AM10 AN9 AN10 SPV18 SPV10 SPVSS

VOLTAGE SENESE

AF28 AG28 AH29 FB_VDDC FB_VDDCI FB_GND

VOLTAGE SENESE
WAITING POWER DESIGN

PCIE

PCIE_VDDR#1 AA31
PCIE_VDDR#2 AA32
PCIE_VDDR#3 AA33
PCIE_VDDR#4 AA34
PCIE_VDDR#5 V28
PCIE_VDDR#6 W29
PCIE_VDDR#7 W30
PCIE_VDDR#8 Y31
PCIE_VDDR/PCIE_PVDD AB37

PCIE_PVDD

1.8V,0.04A

PCIE_VDDC#1 G30
PCIE_VDDC#2 G31
PCIE_VDDC#3 H29
PCIE_VDDC#4 H30
PCIE_VDDC#5 J29
PCIE_VDDC#6 J30
PCIE_VDDC#7 L28
PCIE_VDDC#8 M28
PCIE_VDDC#9 N28
PCIE_VDDC#10 R28
PCIE_VDDC#11 T28
PCIE_VDDC#12 U28

CORE

VDDC#1 AA15
VDDC#2 AA17
VDDC#3 AA20
VDDC#4 AA22
VDDC#5 AA24
VDDC#6 AA27
VDDC#7 AB16
VDDC#8 AB18
VDDC#9 AB21
VDDC#10 AB23
VDDC#11 AB26
VDDC#12 AB28
VDDC#13 AC17
VDDC#14 AC20
VDDC#15 AC22
VDDC#16 AC24
VDDC#17 AC27
VDDC#18 AD18
VDDC#19 AD21
VDDC#20 AD23
VDDC#21 AD26
VDDC#22 AF17
VDDC#23 AF20
VDDC#24 AF22
VDDC#25 AG16
VDDC#26 AG18
VDDC#27 AG21
VDDC#28 AH22
VDDC#29 AH27
VDDC#30 AH28
VDDC#31 M26
VDDC#32 N24
VDDC/BIF_VDDC#33 N27
VDDC#34 R18
VDDC#35 R21
VDDC#36 R23
VDDC#37 R26
VDDC#38 T17
VDDC#39 T20
VDDC#40 T22
VDDC#41 T24
VDDC/BIF_VDDC#42 T27
VDDC#43 U16
VDDC#44 U18
VDDC#45 U21
VDDC#46 U23
VDDC#47 U26
VDDC#48 V17
VDDC#49 V20
VDDC#50 V22
VDDC#51 V24
VDDC#52 V27
VDDC#53 Y16
VDDC#54 Y18
VDDC#55 Y21
VDDC#56 Y23
VDDC#57 Y26
VDDC#58 Y28

POWER

ISOLATED CORE I/O

VDDCI#1 AA13
VDDCI#2 AB13
VDDCI#3 AC12
VDDCI#4 AC15
VDDCI#5 AD13
VDDCI#6 AD16
VDDCI#7 M15
VDDCI#8 M16
VDDCI#9 M18
VDDCI#10 M23
VDDCI#11 N13
VDDCI#12 N15
VDDCI#13 N17
VDDCI#14 N20
VDDCI#15 N22
VDDCI#16 R12
VDDCI#17 R13
VDDCI#18 R16
VDDCI#19 T12
VDDCI#20 T15
VDDCI#21 V15
VDDCI#22 Y13

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P1V8_GPUS

1.8V,0.44A

PCIE_VDDR

L5336 BLM18PG600SN1D

C5063 0.1UF_16V_2 C5297 0.1UF_16V_2 C5065 1UF_6.3V_2 C5316 1UF_6.3V_2 C5066 1UF_6.3V_2 C5334 10UF_6.3V_3

P1V0_GPU

1.0V,1.1A

C5062 C5064 C5298 C5304 C5310 C5318 C5328 C5335 1UF_6.3V_2 10UF_6.3V_3

PVCORE_GPU

VDDC+VDDCI=43.3A(PEAK)

C5282 C5288 C5293 C5300 C5305 C5312 C5319 C5324 C5330 C5338 1UF_6.3V_2

C5283 C5289 C5294 C5301 C5306 C5313 C5320 C5325 C5331 C5339 1UF_6.3V_2

C5284 C5290 C5295 C5302 C5307 C5314 C5321 C5326 C5332 C5337 1UF_6.3V_2

C5061 C5291 C5296 C5303 C5308 C5315 C5322 C5327 C5333 C5340 10UF_6.3V_3

BIF_VDDC

BIF_VDDC IS SEPARATE CORE
POWER FOR THE PCIE BUS LOGIC.

C5281 C5287 1UF_6.3V_2

PVCORE_GPU

VDDC+VDDCI=43.3A(PEAK)

C5277 C5279 C5285 C5292 C5299 C5309 C5311 C5317 C5323 C5329 1UF_6.3V_2

C5278 C5280 C5286 10UF_6.3V_3

INVENTEC

TITLE MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310_0XXXXX_M1R	X01

CHANGE by XXX JEN LEE DATE February 22, 2010 21:04:12002

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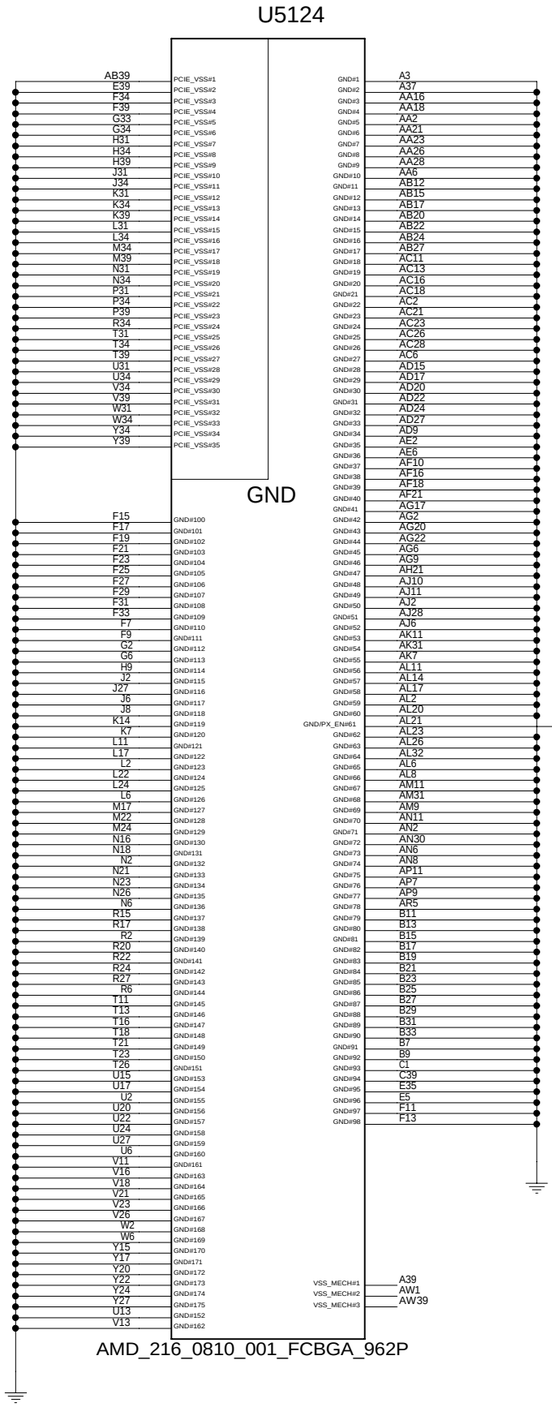
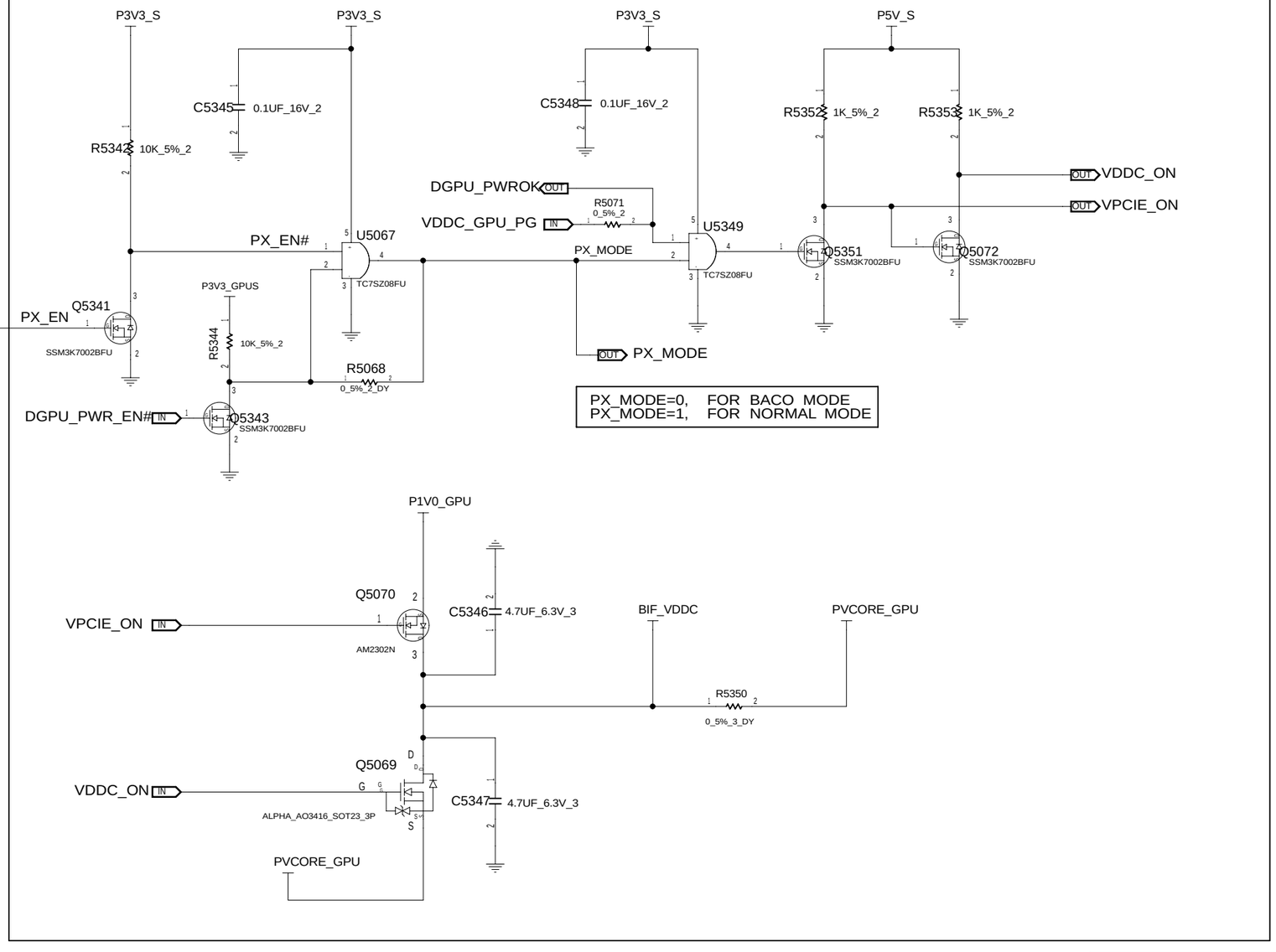
BACO





INVENTEC

TITLE: MODEL PROJECT FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXXX_MTR	XB1

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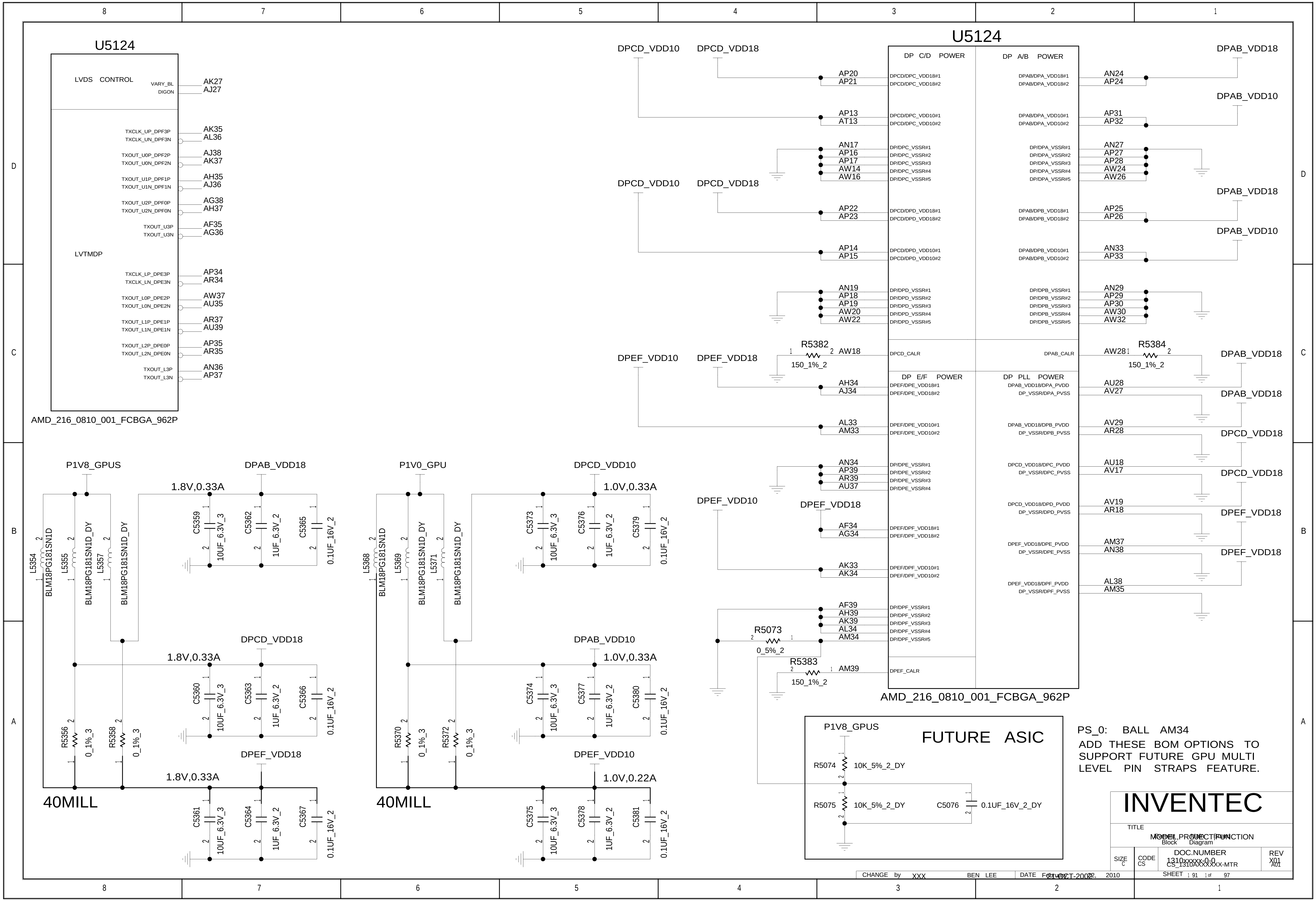
CHANGE by CHEN LEE DATE February 22, 2010


U5124
LVDS CONTROL
VARY_BL AK27
DIGON AJ27
LVTMDP
TXCLK_UP_DPF3P AK35
TXCLK_UN_DPF3N AL36
TXOUT_U0P_DPF2P AJ38
TXOUT_U0N_DPF2N AK37
TXOUT_U1P_DPF1P AH35
TXOUT_U1N_DPF1N AJ36
TXOUT_U2P_DPF0P AG38
TXOUT_U2N_DPF0N AH37
TXOUT_U3P AF35
TXOUT_U3N AG36
TXCLK_LP_DPE3P AP34
TXCLK_LN_DPE3N AR34
TXOUT_L0P_DPE2P AW37
TXOUT_L0N_DPE2N AU35
TXOUT_L1P_DPE1P AR37
TXOUT_L1N_DPE1N AU39
TXOUT_L2P_DPE0P AP35
TXOUT_L2N_DPE0N AR35
TXOUT_L3P AN36
TXOUT_L3N AP37
AMD_216_0810_001_FCBGA_962P
U5124
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
DPCD_VDD10
DPCD_VDD18
DPAB_VDD18
DPAB_VDD10
DPEF_VDD10
DPEF_VDD18
R5382 150_1%_2
R5384 150_1%_2
R5073 0_5%_2
R5383 150_1%_2
DPCD_CALR
DPAB_CALR
DPEF_CALR
AMD_216_0810_001_FCBGA_962P
P1V8_GPUS
P1V0_GPU
1.8V,0.33A
1.0V,0.33A
1.0V,0.22A
BLM18PG181SN1D
BLM18PG181SN1D_DY
10UF_6.3V_3
1UF_6.3V_2
0.1UF_16V_2
0_1%_3
40MILL
FUTURE ASIC
R5074 10K_5%_2_DY
R5075 10K_5%_2_DY
C5076 0.1UF_16V_2_DY
PS_0: BALL AM34
ADD THESE BOM OPTIONS TO SUPPORT FUTURE GPU MULTI LEVEL PIN STRAPS FEATURE.
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
DOC.NUMBER
1310xxxx-0-0
CS_1310XXXXXXX-MTR
SIZE C
CODE CS
REV X01
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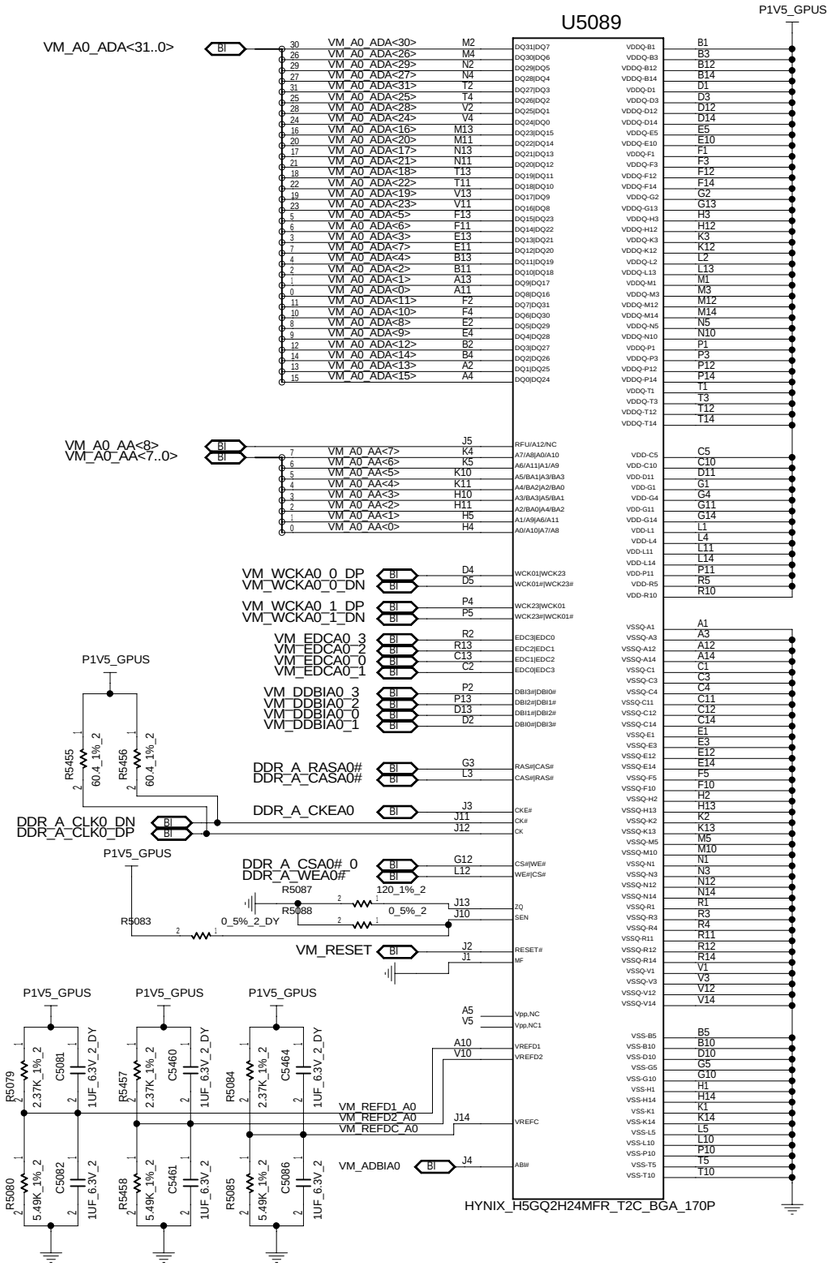
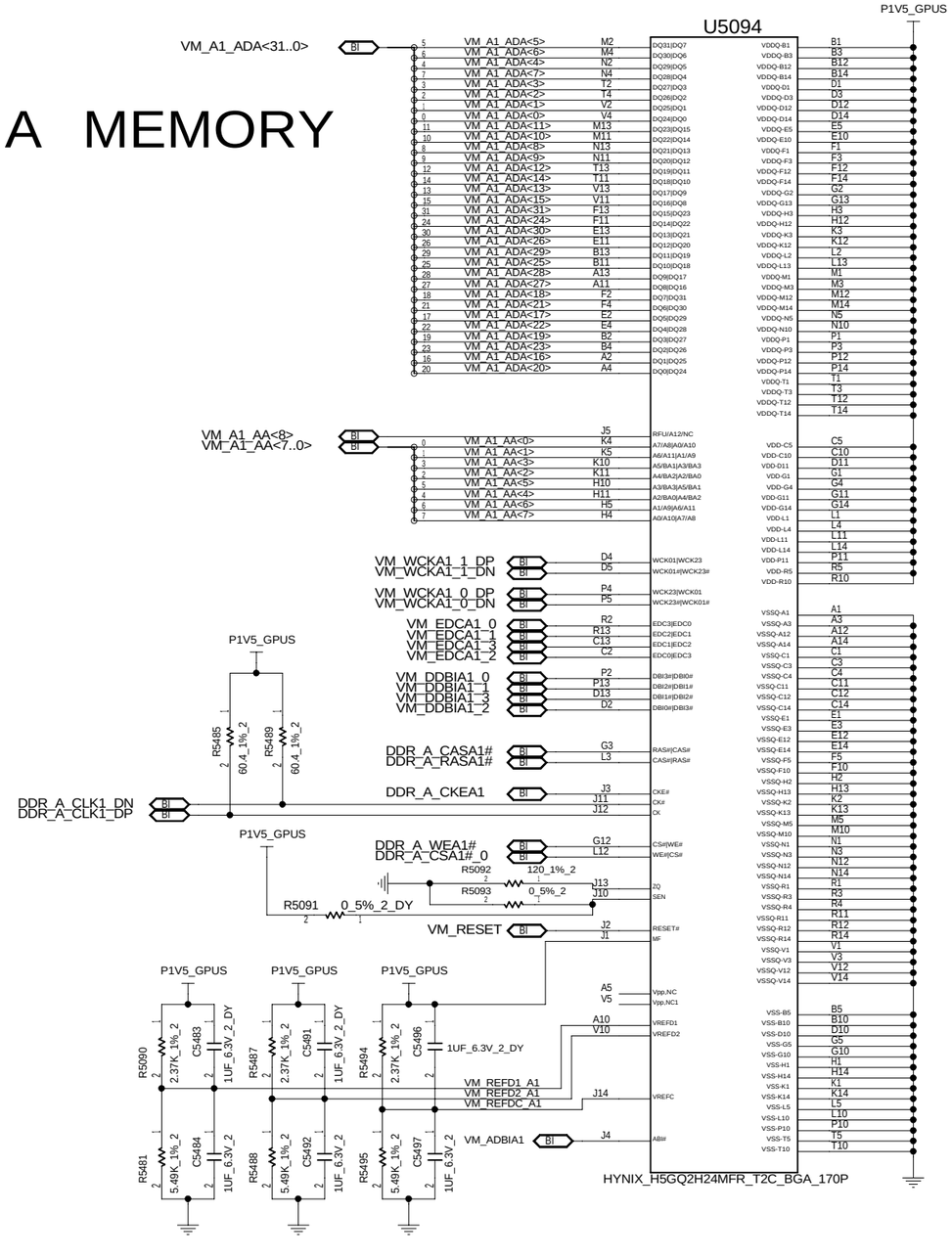
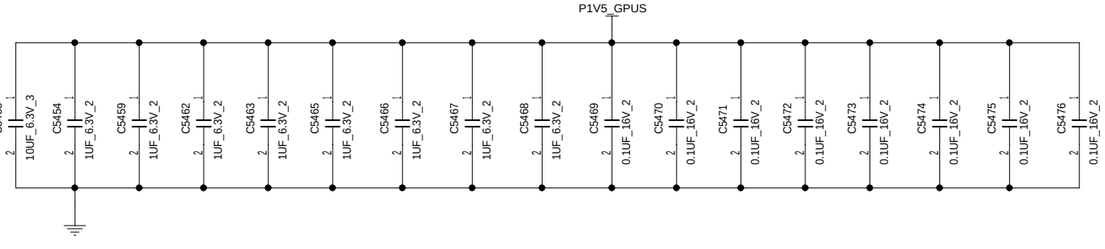
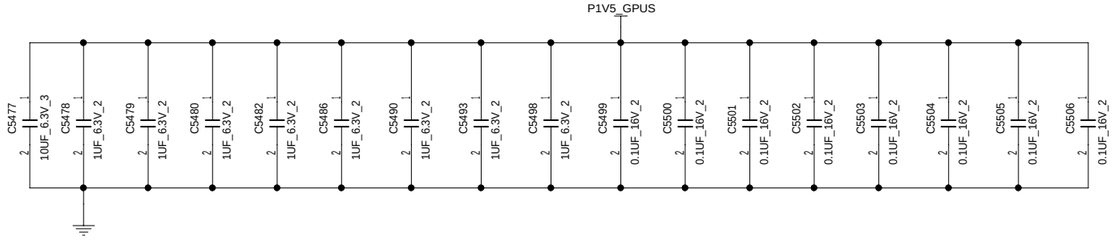
CHANGE by XXX
BEN LEE
DATE 21-OCT-2002
2010

GDDR5
CHANNEL A MEMORY









INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310_XXXXXXXX_MTR	XXX

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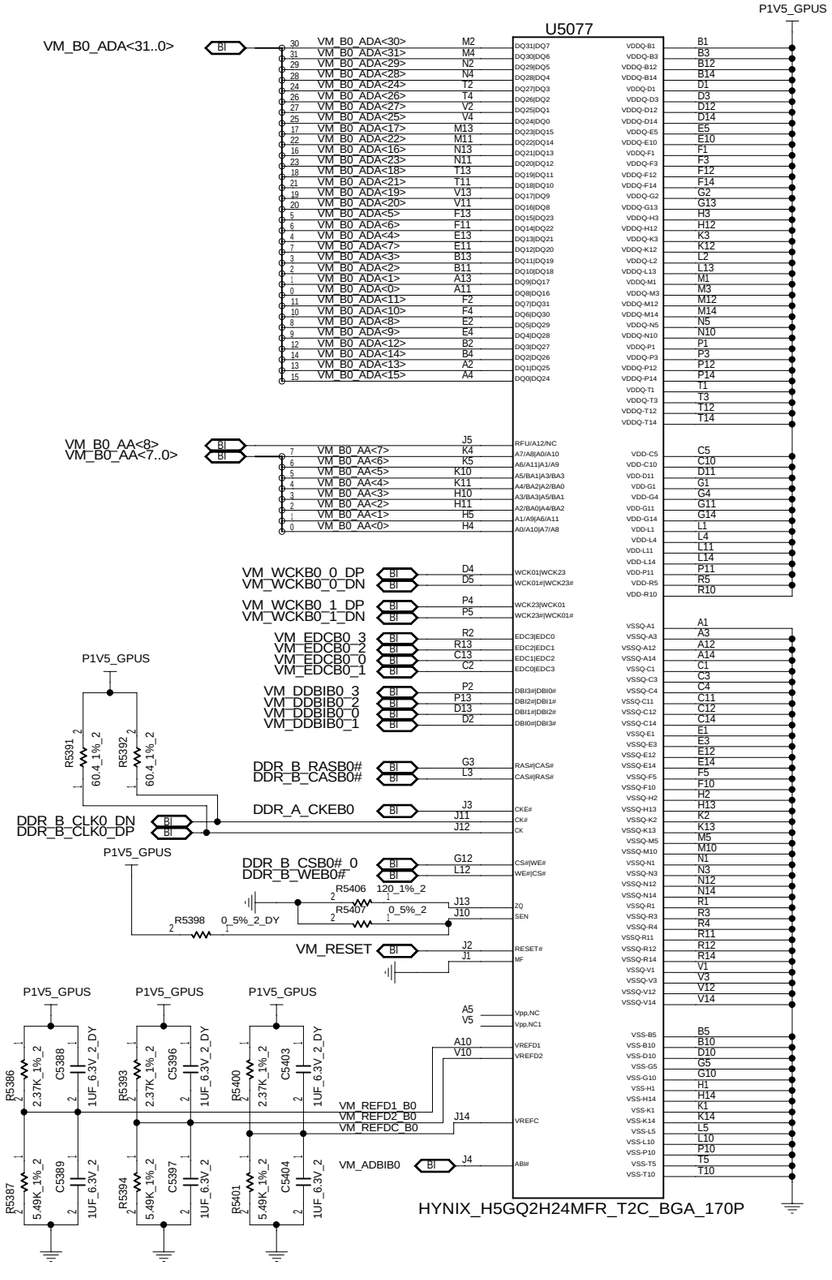
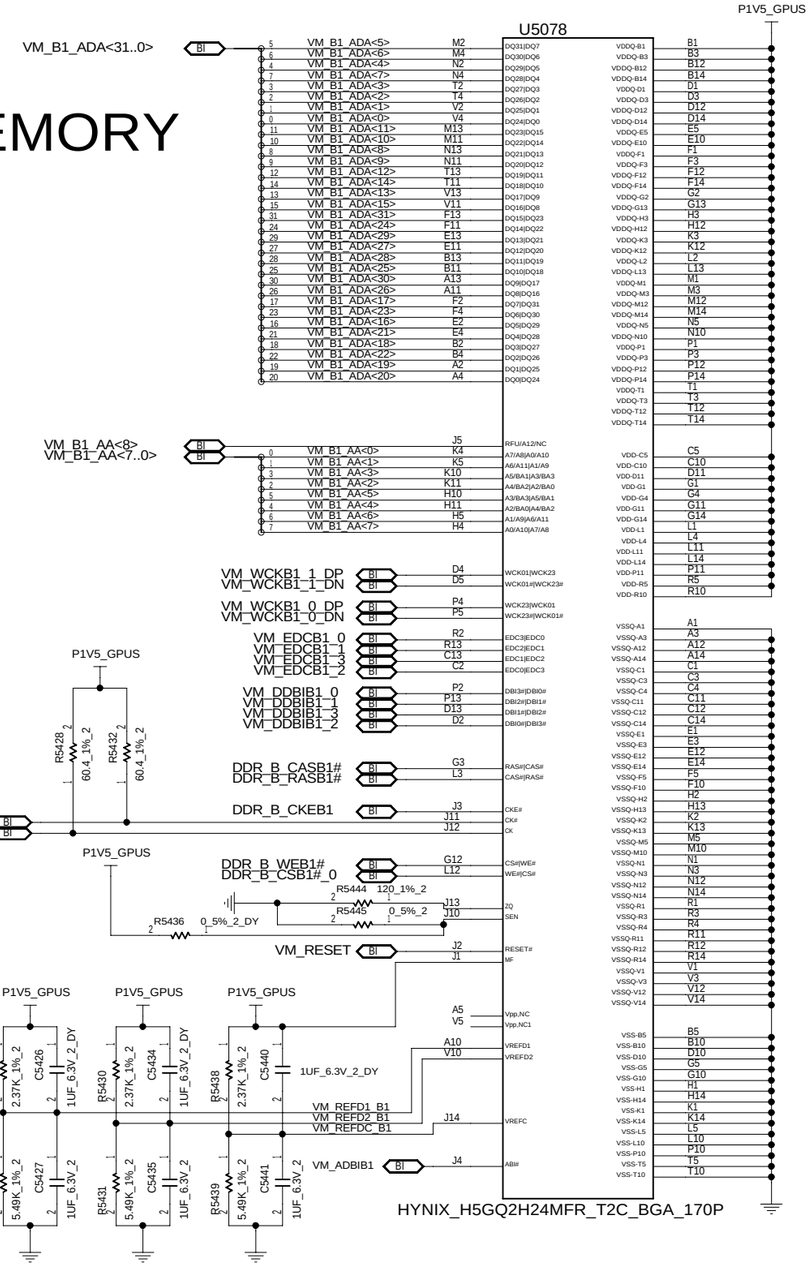
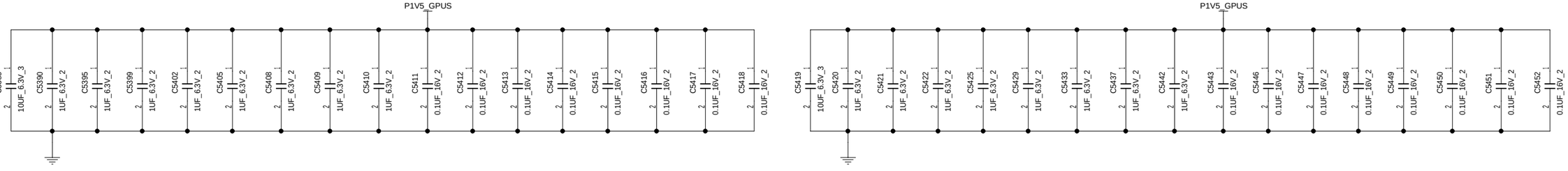
CHANGE by	DATE
XXX_KEN_LEE	February 22, 2010

GDDR5
CHANNEL B MEMORY







INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310_XXXXXXXX_MTR	XX

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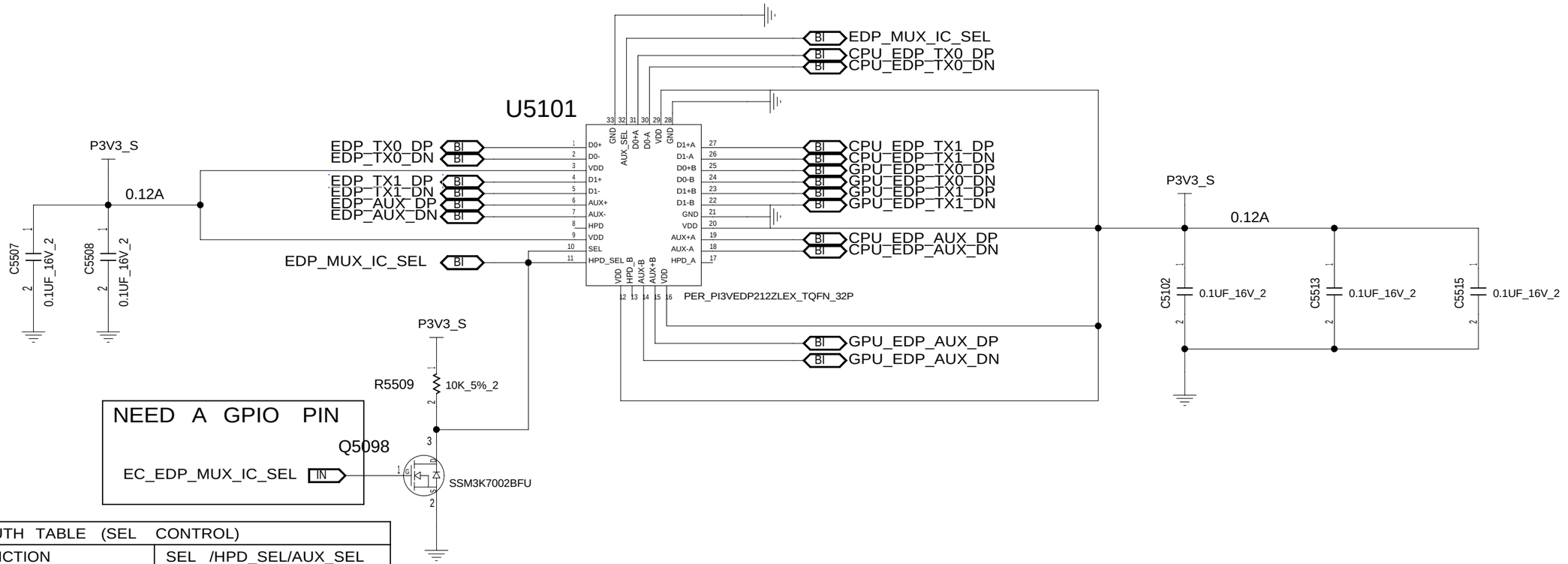
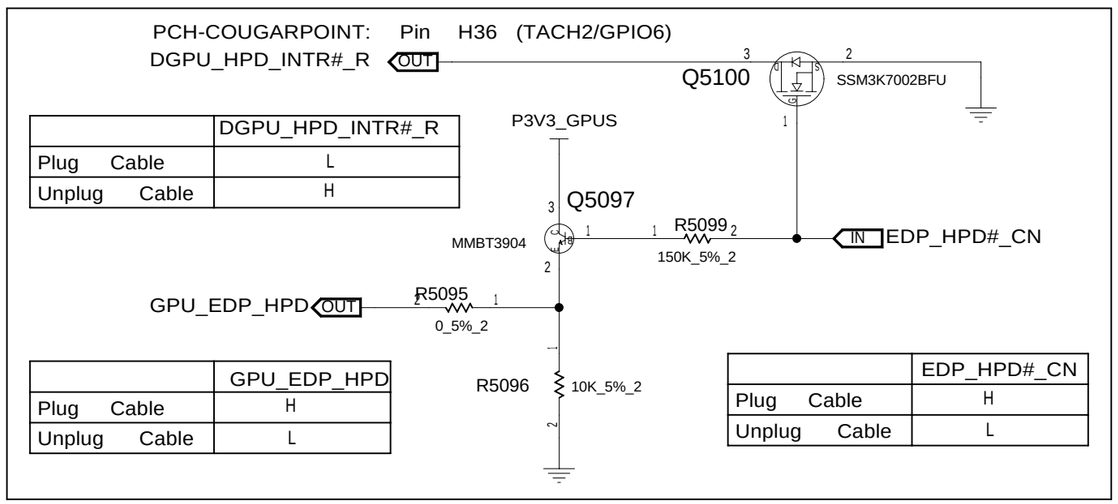
CHANGE by	DATE
XXXX_LEE	February 22, 2010



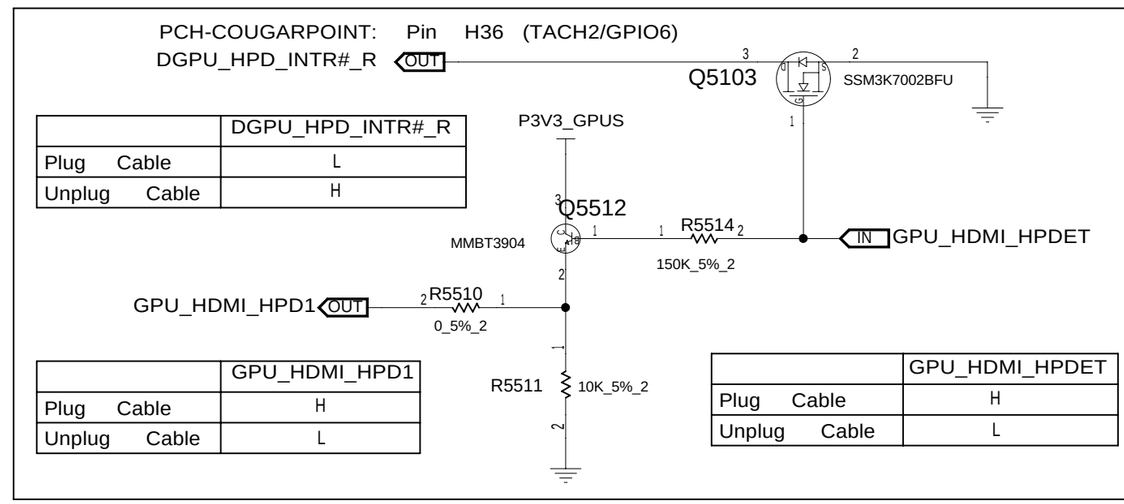
TRUTH TABLE (SEL CONTROL)		
FUNCTION	SEL /HPD_SEL/AUX_SEL	
PORT A IS ACTIVE	L	(CPU)
PORT B IS ACTIVE	H	(GPU)



	DGPU_HPD_INTR#_R
Plug Cable	L
Unplug Cable	H

	GPU_EDP_HPD
Plug Cable	H
Unplug Cable	L

	EDP_HPD#_CN
Plug Cable	H
Unplug Cable	L



	DGPU_HPD_INTR#_R
Plug Cable	L
Unplug Cable	H

	GPU_HDMI_HPD1
Plug Cable	H
Unplug Cable	L

	GPU_HDMI_HPDET
Plug Cable	H
Unplug Cable	L

INVENTEC

TITLE: MODEL PRODUCTION FUNCTION

Block Diagram

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0 CS_1310AXXXXXX-MTR	X01 A01

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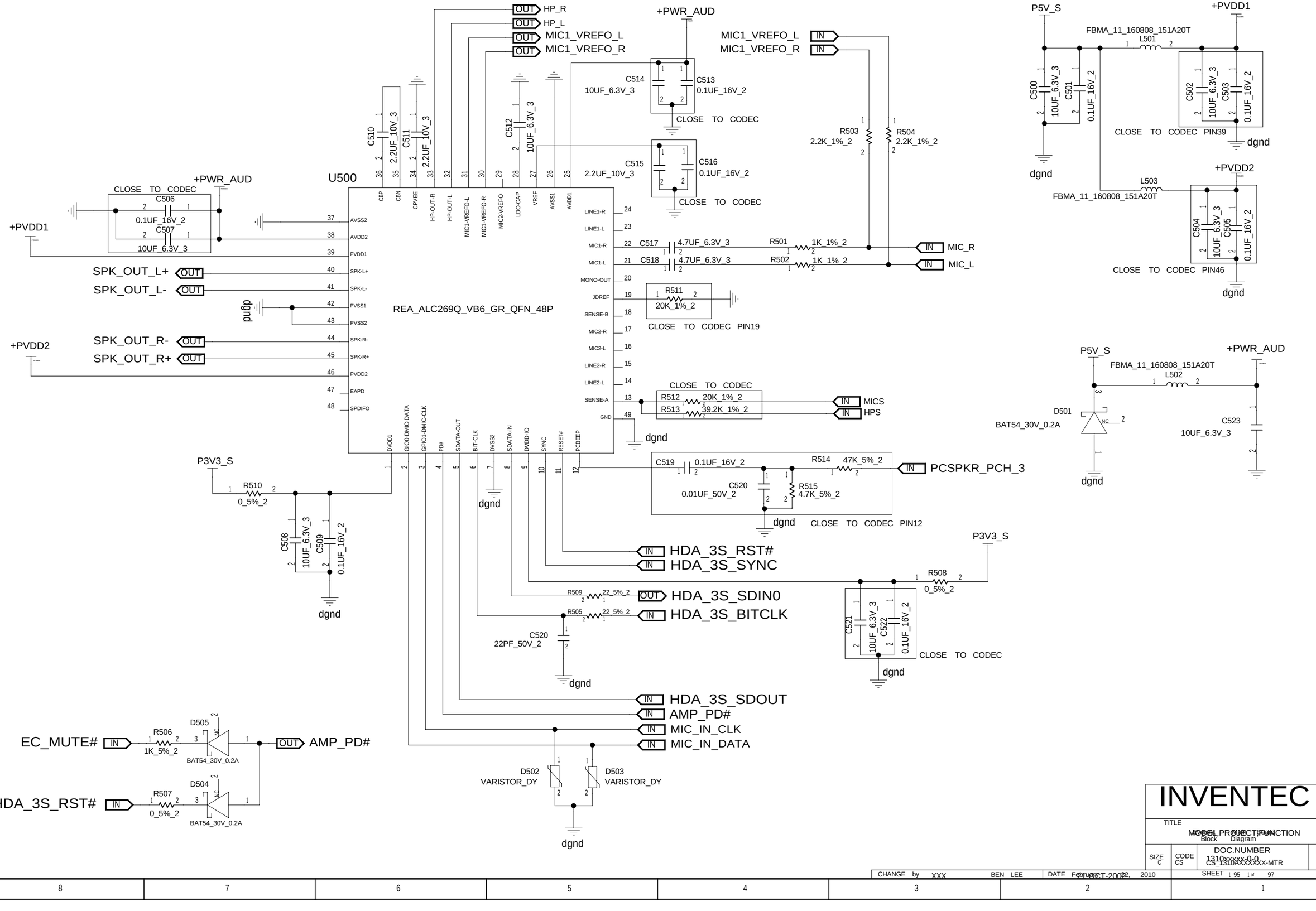
U500
REA_ALC269Q_VB6_GR_QFN_48P
+PWR_AUD
+PVDD1
+PVDD2
P3V3_S
P5V_S
dgnd
HP_R
HP_L
MIC1_VREFO_L
MIC1_VREFO_R
SPK_OUT_L+
SPK_OUT_L-
SPK_OUT_R-
SPK_OUT_R+
MIC_R
MIC_L
MICS
HPS
PCSPKR_PCH_3
HDA_3S_RST#
HDA_3S_SYNC
HDA_3S_SDIN0
HDA_3S_BITCLK
HDA_3S_SDOUT
AMP_PD#
MIC_IN_CLK
MIC_IN_DATA
EC_MUTE#
CLOSE TO CODEC
CLOSE TO CODEC PIN39
CLOSE TO CODEC PIN46
CLOSE TO CODEC PIN19
CLOSE TO CODEC PIN12
FBMA_11_160808_151A20T
BAT54_30V_0.2A
VARISTOR_DY
INVENTEC
TITLE
MODEL PRODUCT FUNCTION
Block Diagram
SIZE C
CODE CS
DOC.NUMBER 1310xxxxx-0-0
CS_1310AXXXXXX-MTR
REV X01 A01
CHANGE by XXX BEN LEE
DATE February 22, 2010
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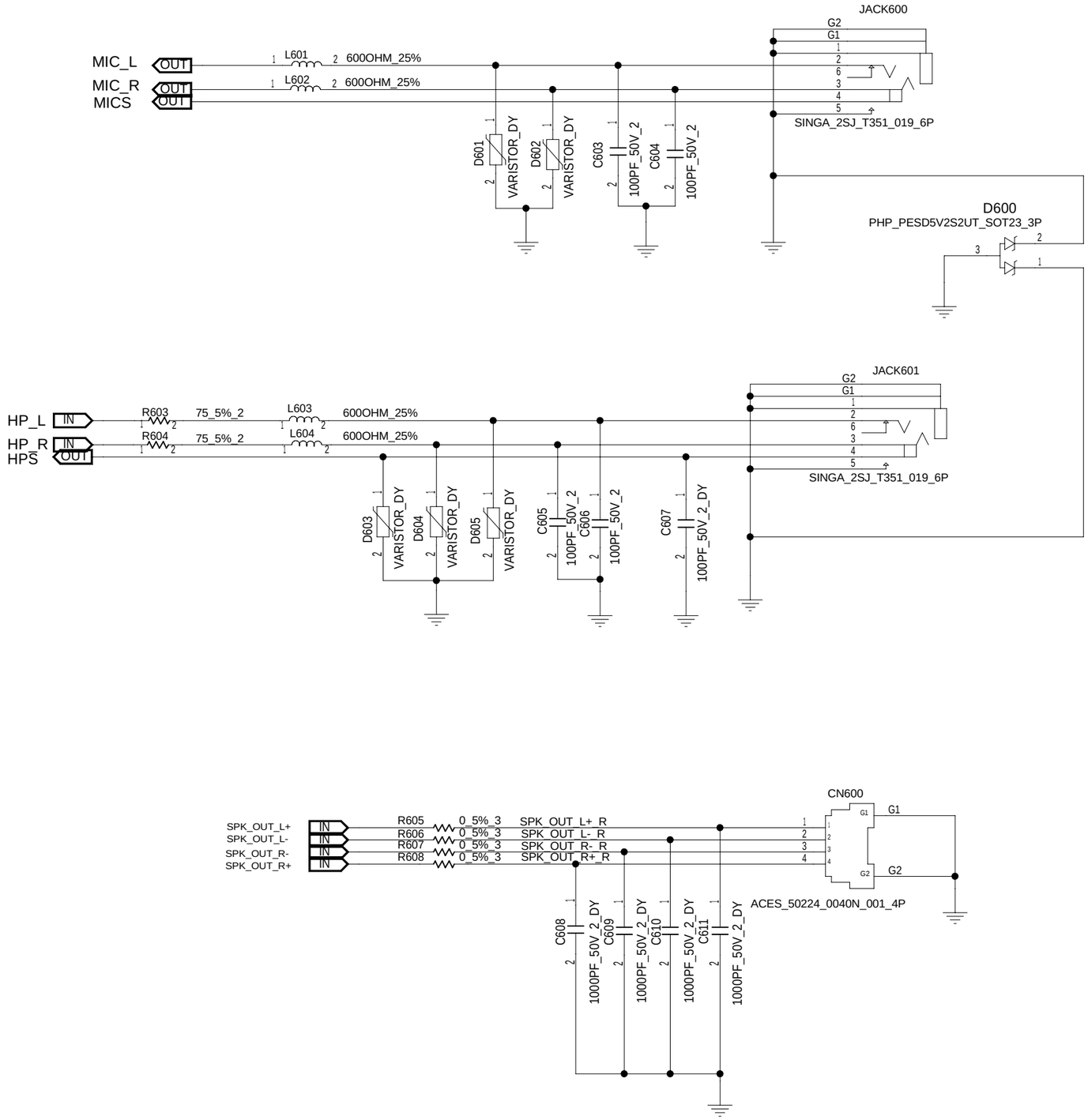

TITLE	MODEL PRODUCTION FUNCTION Block Diagram	
SIZE C	CODE CS	DOC.NUMBER 1310xxxxx-0-0 CS_1310AXXXXXX-MTR
		REV X01 A01
CHANGE by XXX BEN LEE	DATE February 22, 2010	SHEET 1 96 1 of 97

INVENTEC

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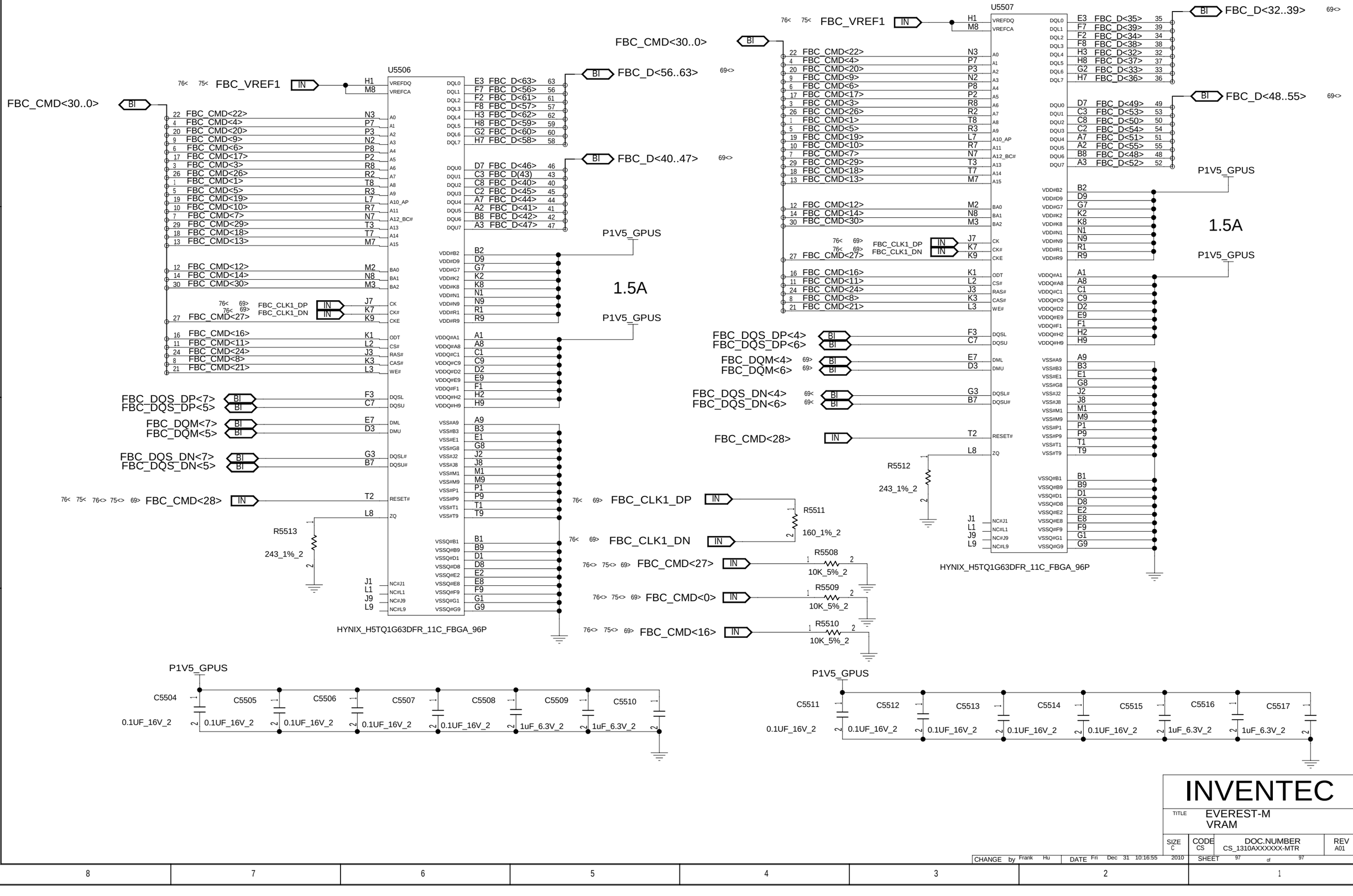
U5506
U5507
FBC_CMD<30..0>
FBC_VREF1
FBC_D<56..63>
FBC_D<40..47>
FBC_D<32..39>
FBC_D<48..55>
FBC_CLK1_DP
FBC_CLK1_DN
FBC_DQS_DP<7>
FBC_DQS_DP<5>
FBC_DQM<7>
FBC_DQM<5>
FBC_DQS_DN<7>
FBC_DQS_DN<5>
FBC_CMD<28>
FBC_DQS_DP<4>
FBC_DQS_DP<6>
FBC_DQM<4>
FBC_DQM<6>
FBC_DQS_DN<4>
FBC_DQS_DN<6>
P1V5_GPUS
1.5A
R5511
160_1%_2
R5512
243_1%_2
R5513
243_1%_2
R5508
10K_5%_2
R5509
10K_5%_2
R5510
10K_5%_2
HYNIX_H5TQ1G63DFR_11C_FBGA_96P
C5504
C5505
C5506
C5507
C5508
C5509
C5510
C5511
C5512
C5513
C5514
C5515
C5516
C5517
0.1UF_16V_2
1uF_6.3V_2
INVENTEC
TITLE
EVEREST-M
VRAM
SIZE
C
CODE
CS
DOC.NUMBER
CS_1310AXXXXXX-MTR
REV
A01
CHANGE by Frank Hu
DATE Fri Dec 31 10:16:55 2010
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