

Compal Confidential

Schematics Document

AUBURNDALE with Intel
IBEX PEAK-M core logic

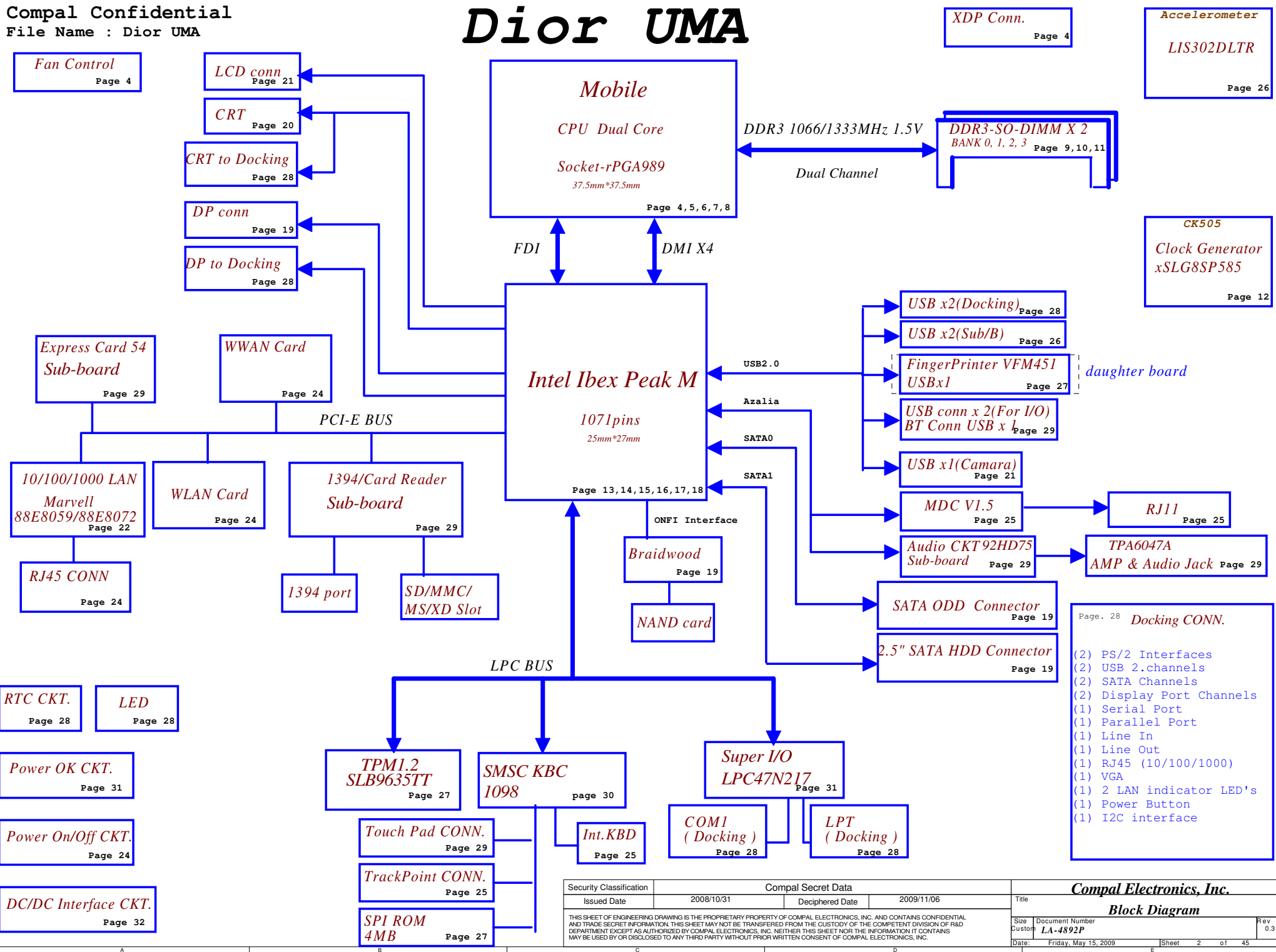
Dior UMA

2009-05-16

REV: 0.3

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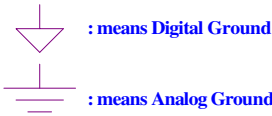


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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B +3VL	+5VALW +3VALW	+1.5V +0.75V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +1.05VS +1.8VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

Symbol Note :



Install below 43 level BOM structure for ver. 0.2

8072@ : Install for 8072 NIC controller

Install below 45 level BOM structure for ver. 0.2

45@ : means just put it in the BOM of 45 level.

Reserve below BOM structure for ver. 0.2

@ : means just reserve , no build

CONN@ : means ME part.

8059@ : Install for 8059 NIC controller

SMBUS Control Table

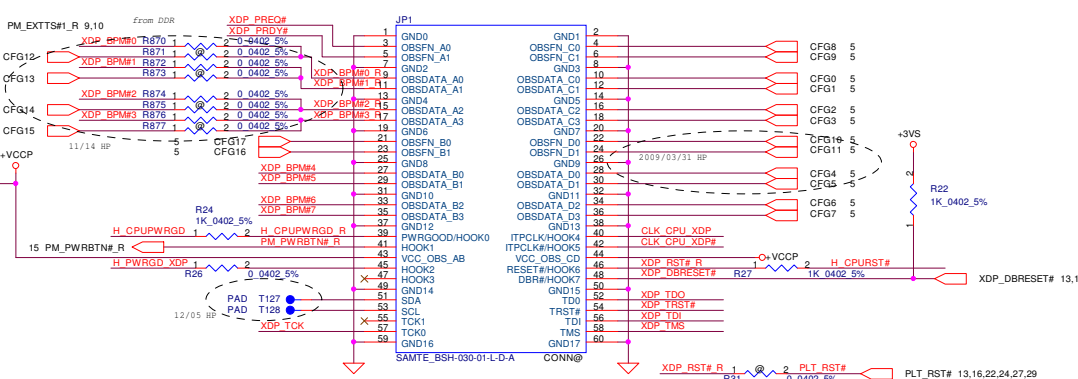
	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	V	X	V
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	X

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The diagram illustrates the timing relationships for the JCPU18, categorized into four functional blocks:

- CLOCKS:** Shows the timing of clock signals (COMP3, COMP2, COMP1, COMP0) and their relationship to the SKTOCC# and CATERR# signals. It also includes the timing for the H_PECI_ISO and H_PROCHOT#_D signals.
- THERMAL:** Displays the timing for thermal management signals, including H_THERMTRIP#_R, H_CUPURST#, H_PM_SYNC, and H_CUPWGRD.
- PMR MANAGEMENT:** Details the timing for power management signals, such as VCCPWGOOD, VDDPWGOOD, VTTWPGOOD, and H_PWRGD_XDP.
- JTAG & BPM:** Shows the timing for JTAG and BPM signals, including PLT_RST#, RSTN#, and various clock signals like CLK_CPU, CLK_EXP, CLK_CPU_BCLK, and CLK_CPU_BCLK#.

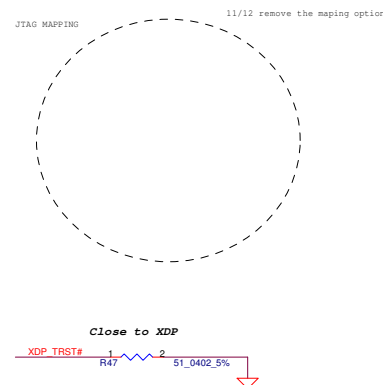
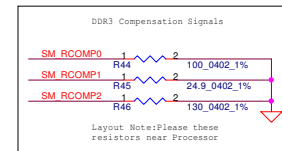
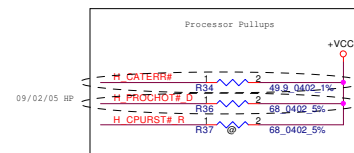
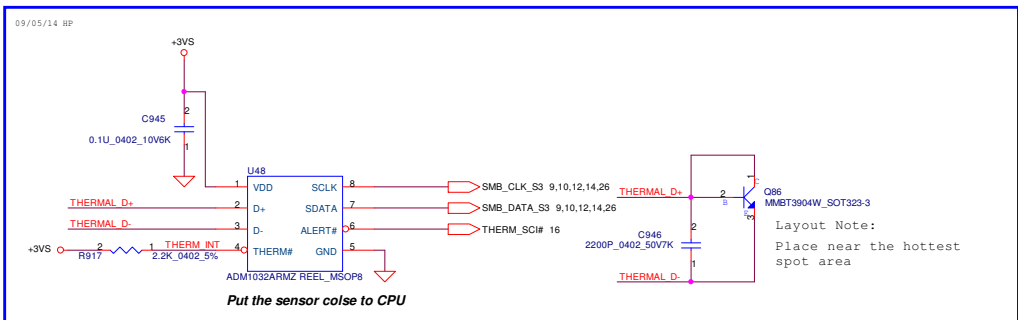
The diagram includes numerous signal transitions and delays, with specific values provided for each signal. For example, the H_PECI_ISO signal has a delay of 0.0402 5%, and the H_PROCHOT#_D signal has a delay of 0.0402 5%. The H_THERMTRIP#_R signal has a delay of 0.0402 5%. The H_CUPURST# signal has a delay of 0.0402 5%. The H_PM_SYNC signal has a delay of 0.0402 5%. The H_CUPWGRD signal has a delay of 0.0402 5%. The VCCPWGOOD signal has a delay of 0.0402 5%. The VDDPWGOOD signal has a delay of 0.0402 5%. The VTTWPGOOD signal has a delay of 0.0402 5%. The H_PWRGD_XDP signal has a delay of 0.0402 5%. The PLT_RST# signal has a delay of 0.0402 5%. The RSTN# signal has a delay of 0.0402 5%. The CLK_CPU signal has a delay of 0.0402 5%. The CLK_EXP signal has a delay of 0.0402 5%. The CLK_CPU_BCLK signal has a delay of 0.0402 5%. The CLK_CPU_BCLK# signal has a delay of 0.0402 5%.



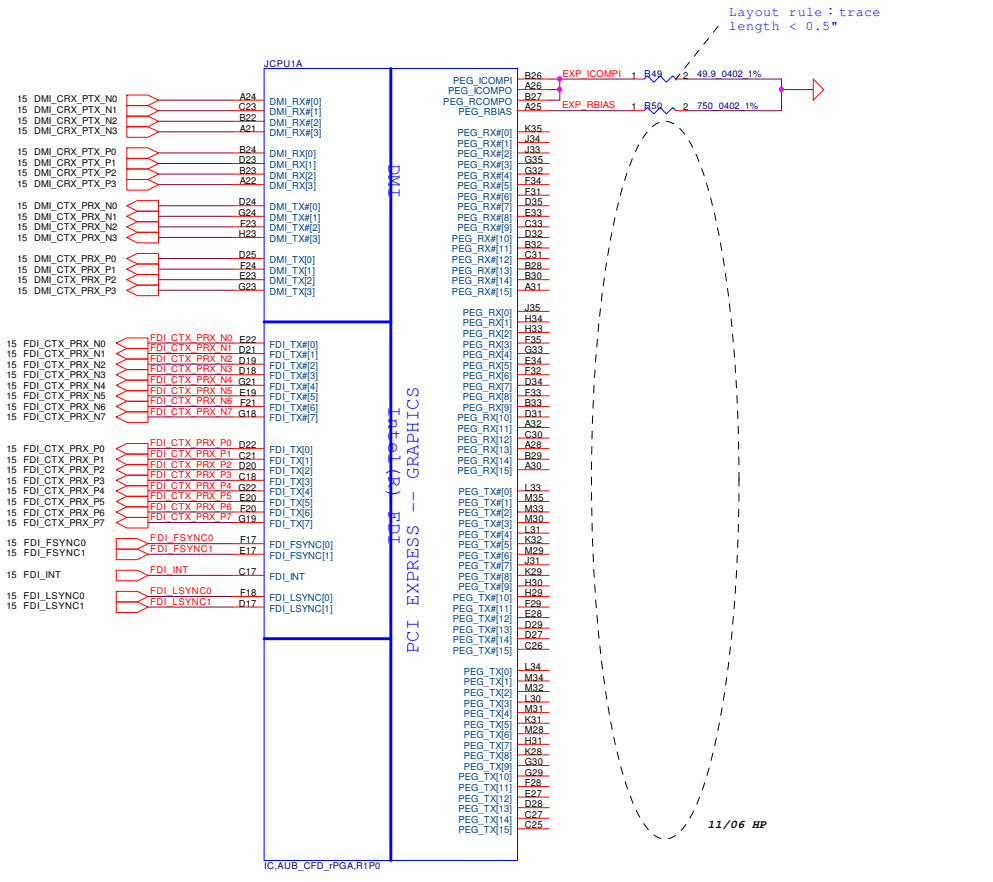
PWM Fan Control circuit

The schematic diagram illustrates a PWM Fan Control circuit. Key components and their connections are as follows:

- Control Signal:** A +3VS signal is connected to a resistor (R965, 10K_0402_5%), which then connects to the base of a MOSFET (Q98, MMBT3904W_SOT323-3).
- MOSFET Driver:** The MOSFET (Q98) is used to drive the fan (FAN_PWM). Its gate is connected to the +3VS signal through R965. The drain is connected to a +5VS supply through a resistor (R42, 22_0402_5%) and a capacitor (C2, 0.1u_0402_10V6K). The source is connected to ground.
- Temperature Sensor:** A temperature sensor (Q98, MMBT3904W_SOT323-3) is connected to a +VCC signal. Its output is connected to the +3VS signal line.
- Connector:** A connector (JF2, ACES_85204-03001) is shown on the right, with pins 1, 2, 3, 4, and 5 connected to various signals.



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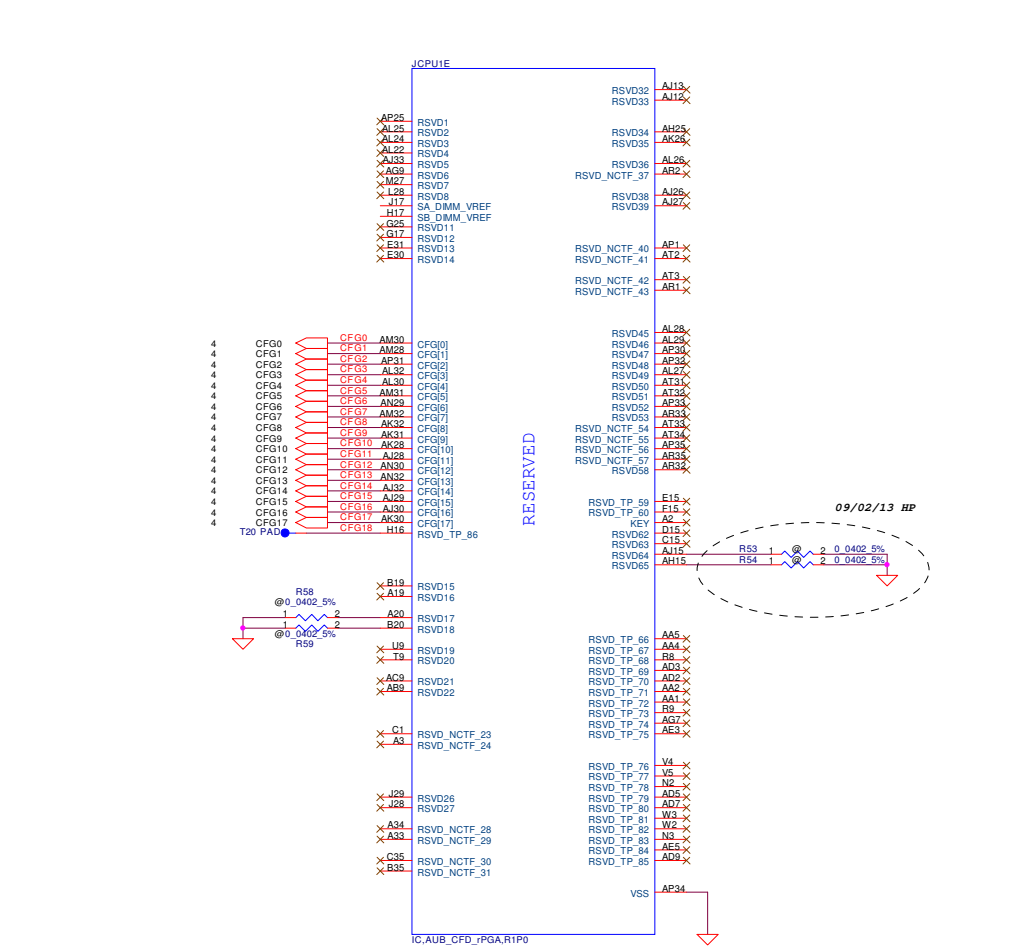
CFG Straps for PROCESSOR

CFG0
R60 @ 5.01K_0402_1%
PCI-Express Configuration Select
CFG0: 1: Single F80
0: Riser/Configuration enabled
Not applicable for Clocksfield Processor

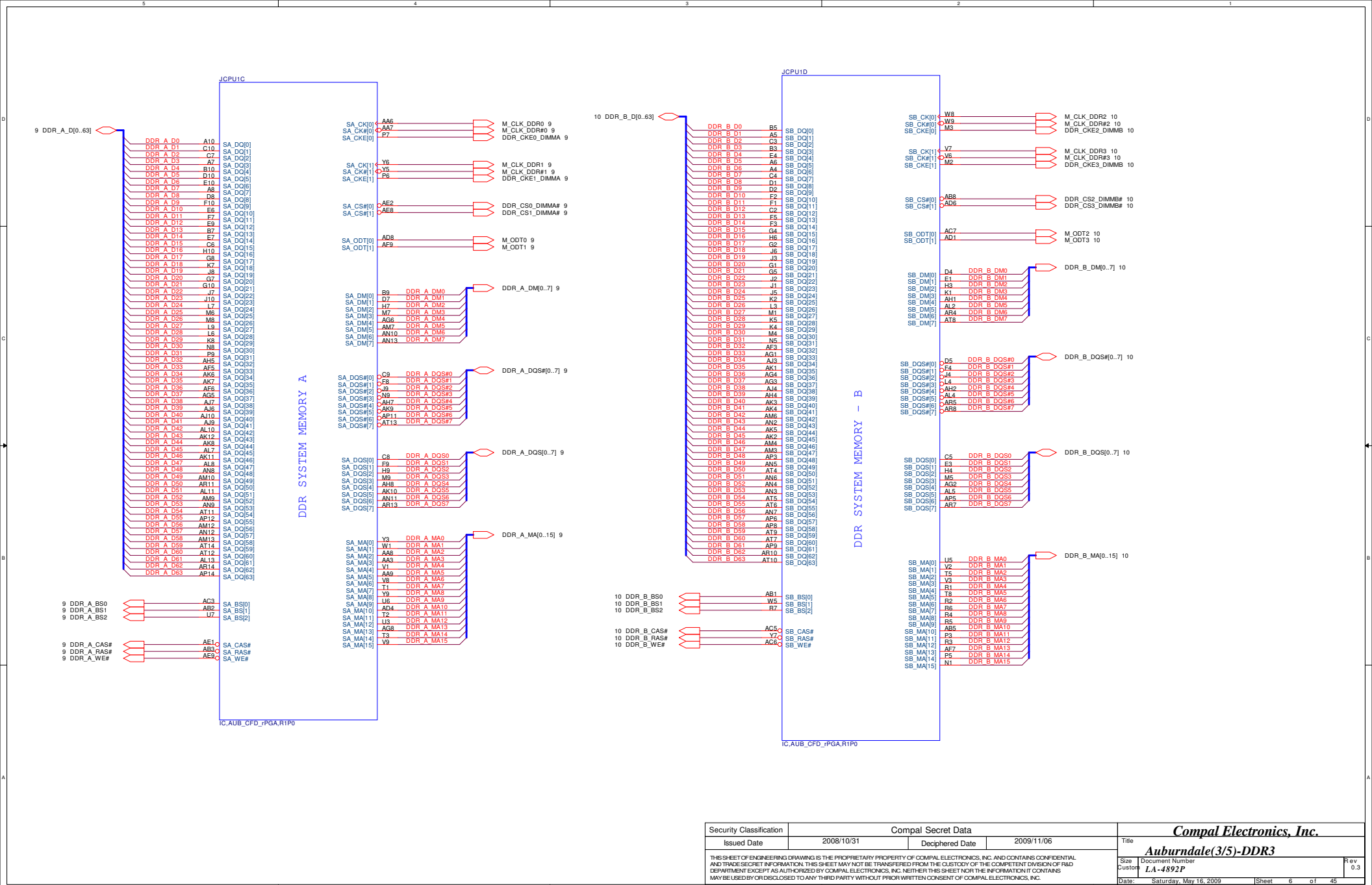
CFG3
R62 @ 5.01K_0402_1%
CFG3-PCI Express Static Lane Reversal
CFG3: 1: Normal Operation
0: Lane Numbers Reversed
15 -> 0, 14 -> 13,

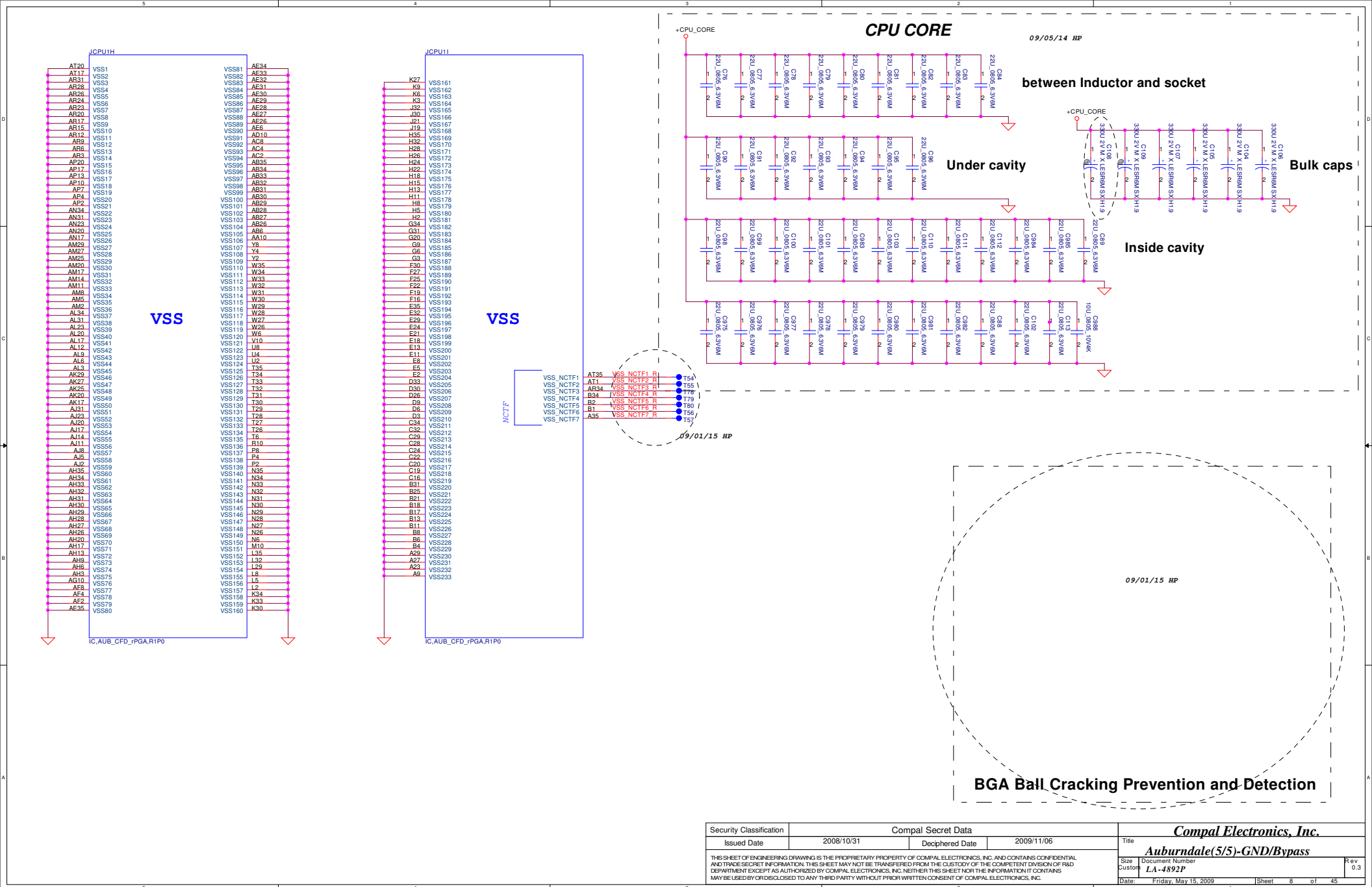
CFG4
R63 @ 5.01K_0402_1%
CFG4-Display Port Presence
CFG4: 1: Disabled; No Physical Display Port attached to Embedded Display Port
0: Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7
R61 @ 5.01K_0402_1%
Only temporary for early CPD samples (rPGA/BGA)
No needed by MoW41.



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DDR3 SO-DIMM A

TOP SLOT

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DDR3 SO-DIMM A

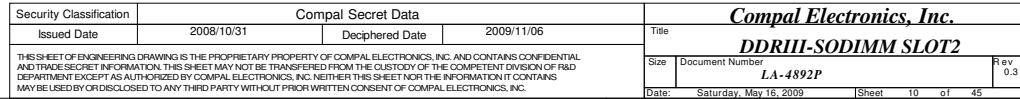
TOP SLOT

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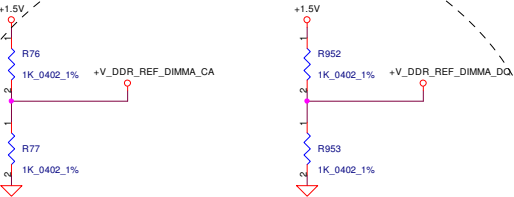
DDR3 SO-DIMM A

TOP SLOT

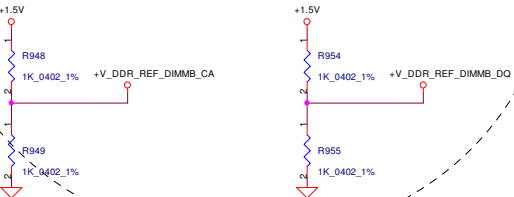
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09/04/03 Auburndale/Arrandale only supports M1 change Vref to +V_DDR_CPU_REF



09/04/23 HP



11/20 Auburndale does not require to support M2 for VrefDQ, HP

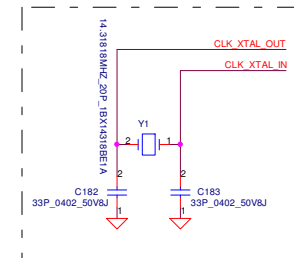
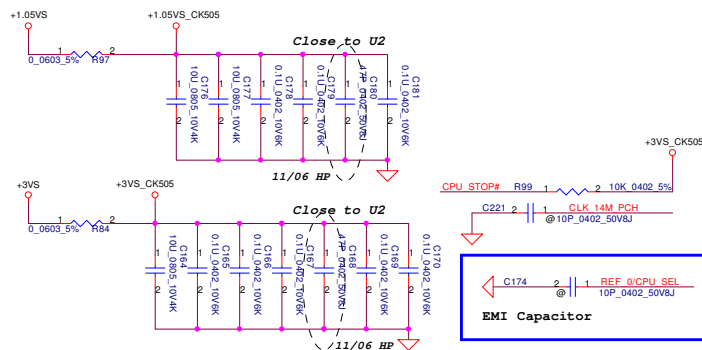
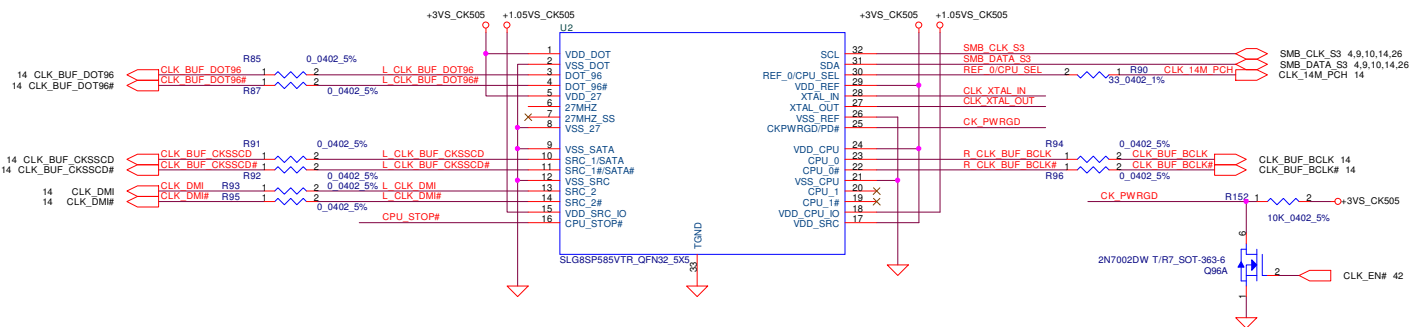
11/20 HP

09/03/31 Auburndale/Arrandale only supports M1, HP

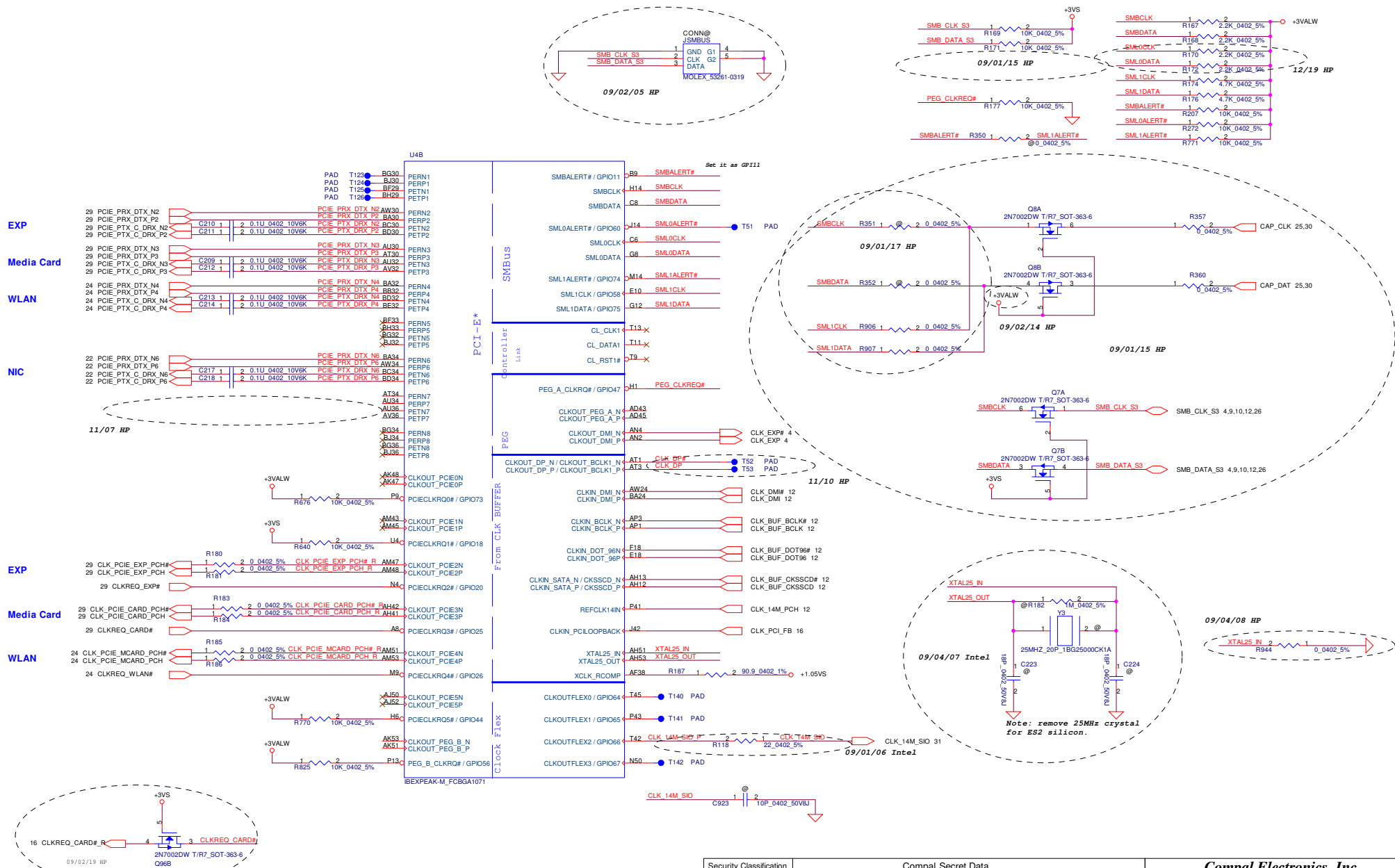
11/20 HP

09/03/31 Auburndale/Arrandale only supports M1, HP

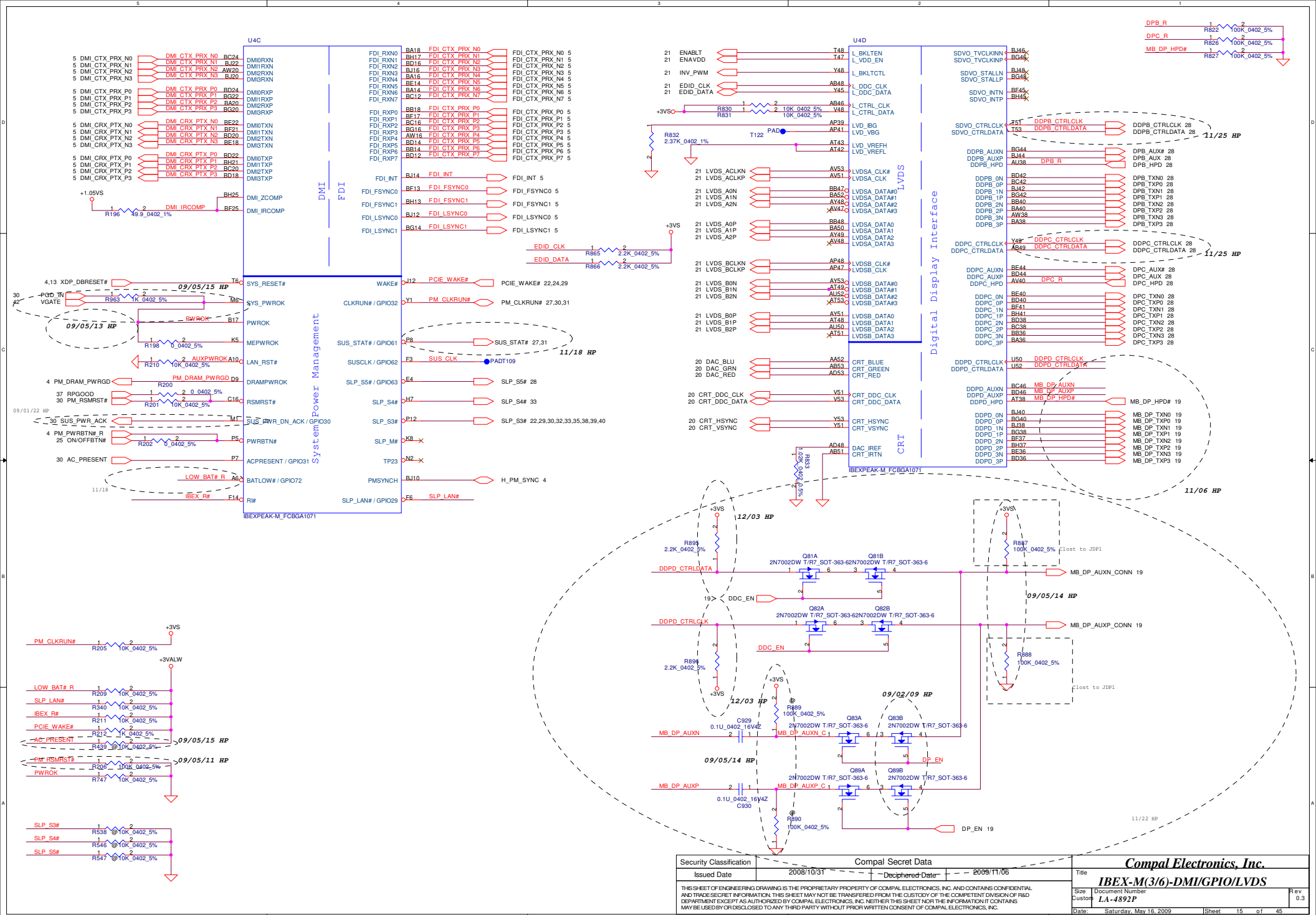
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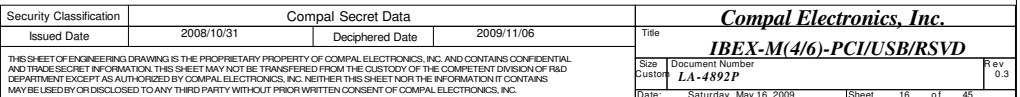


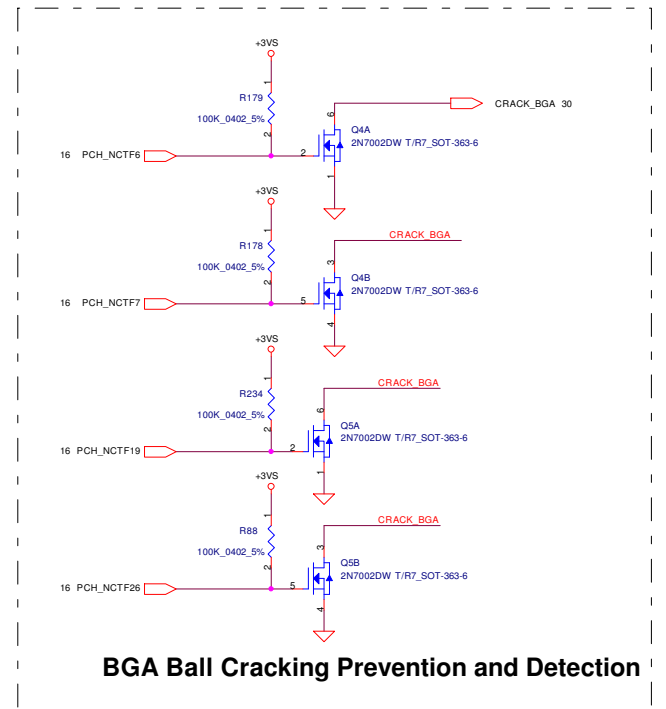
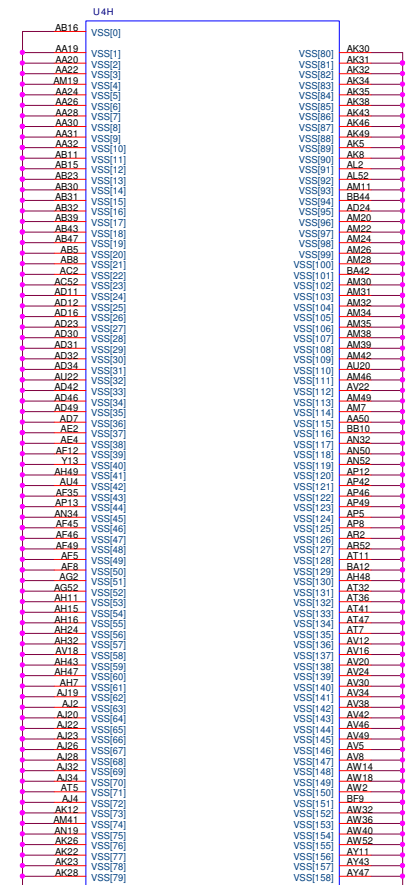
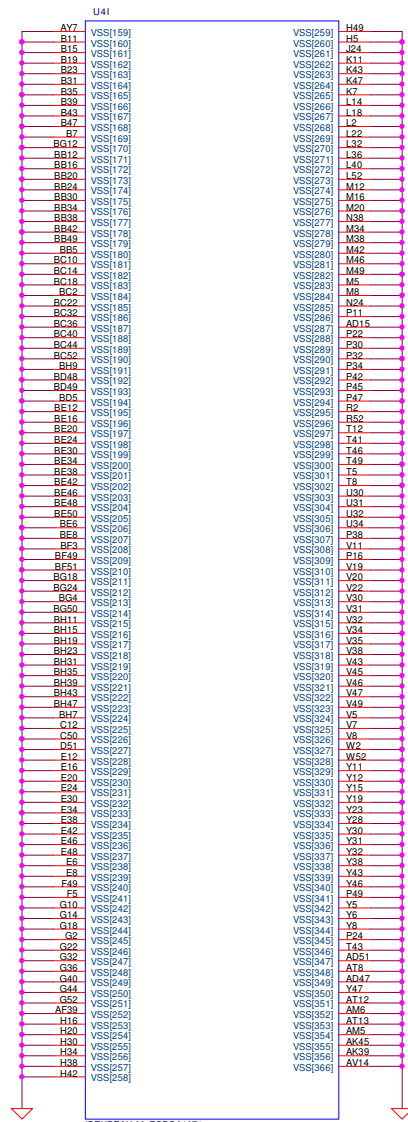
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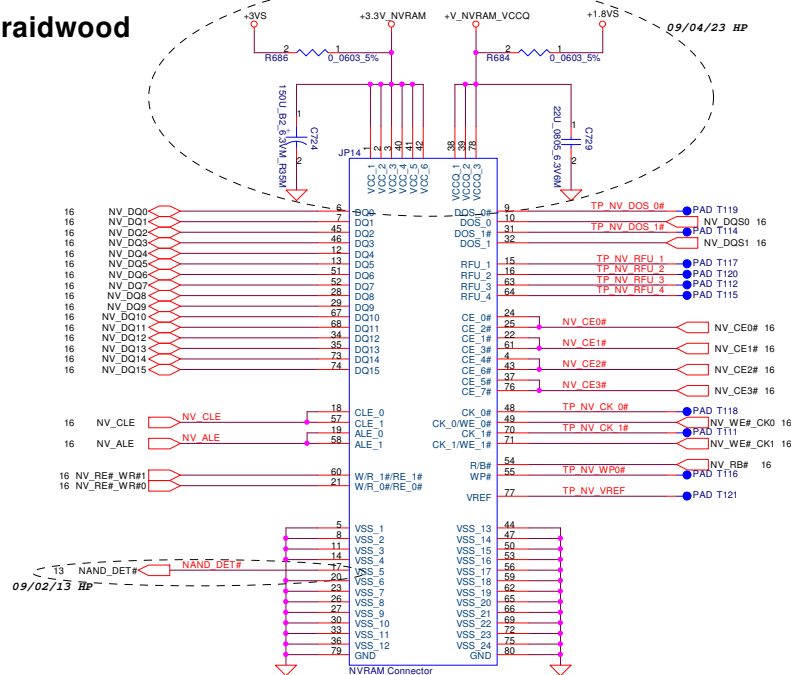




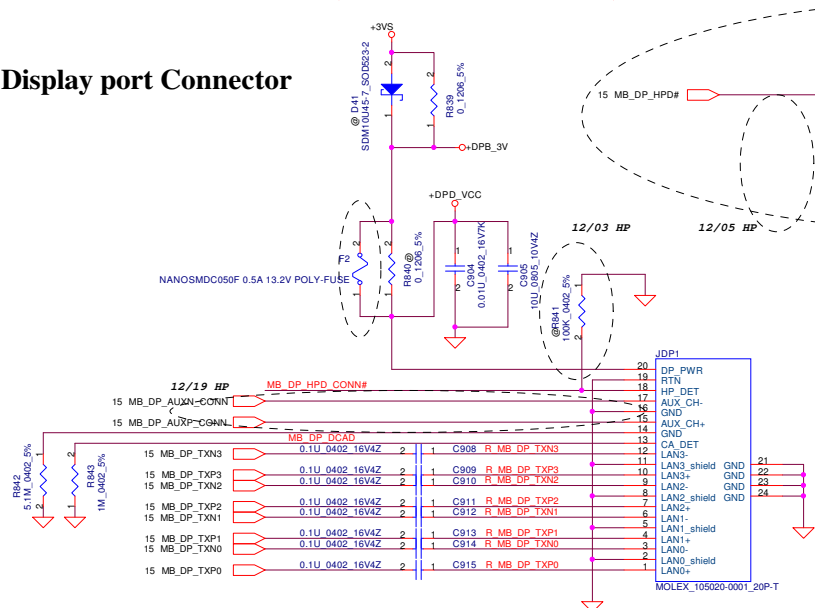
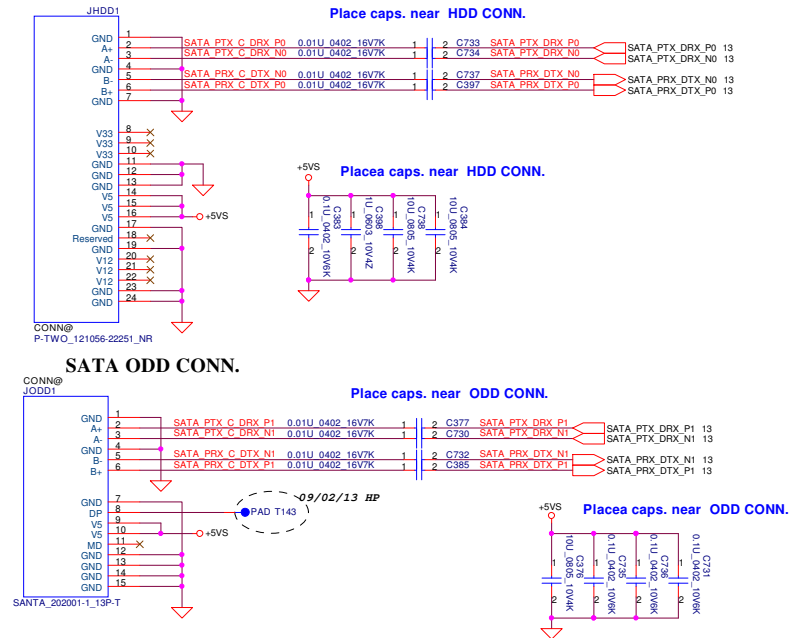


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Braidwood

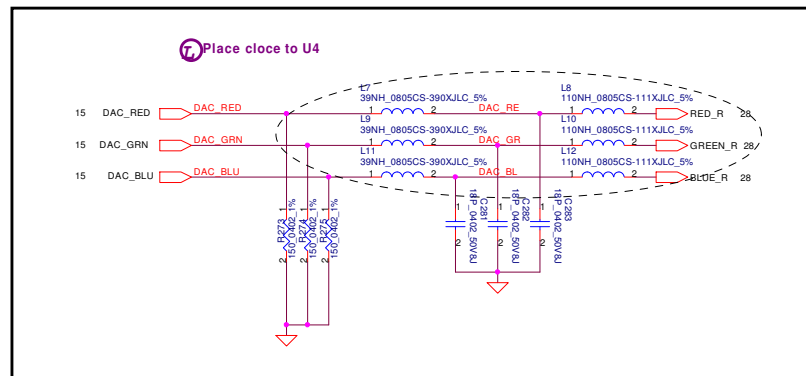
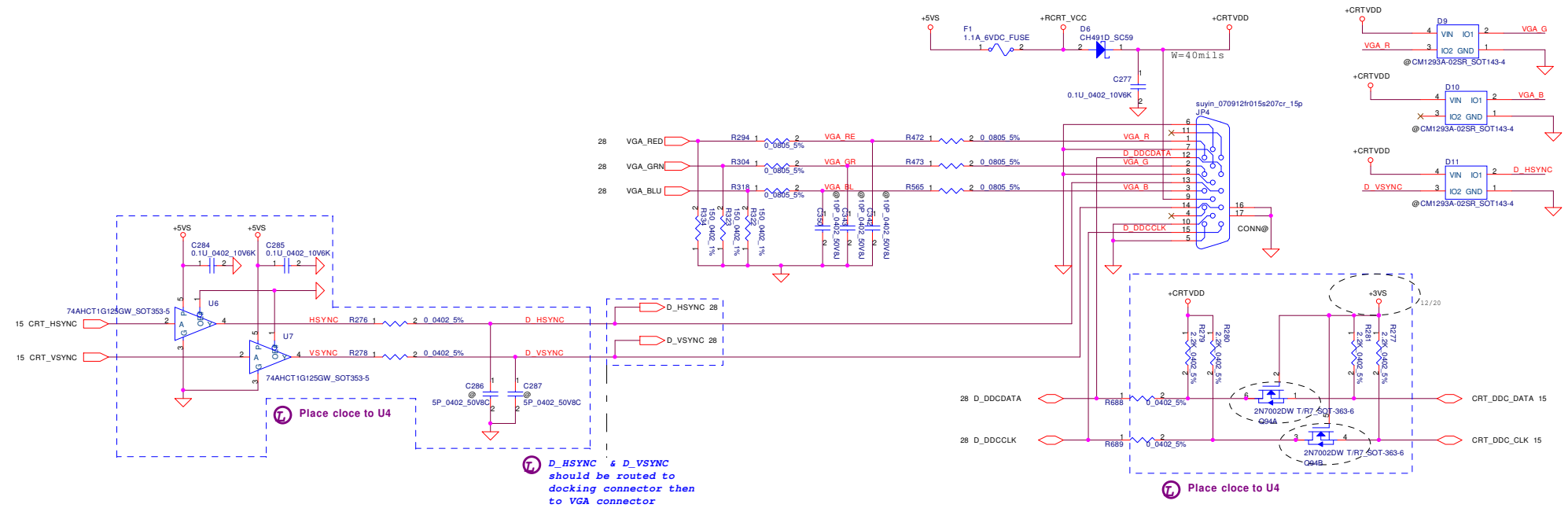


Display port Connector

**SATA HDD CONN.**

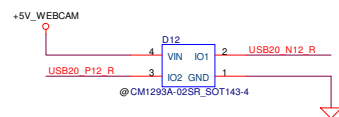
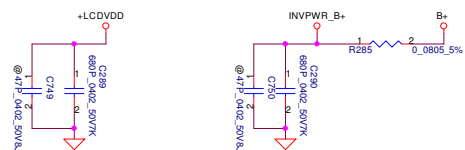
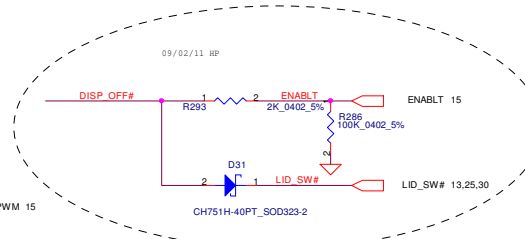
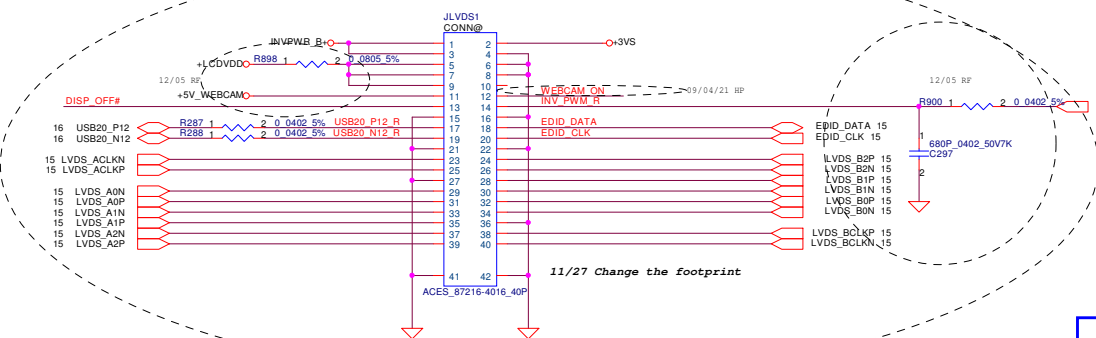
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CRT Connector

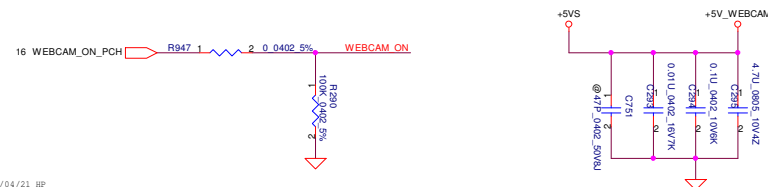


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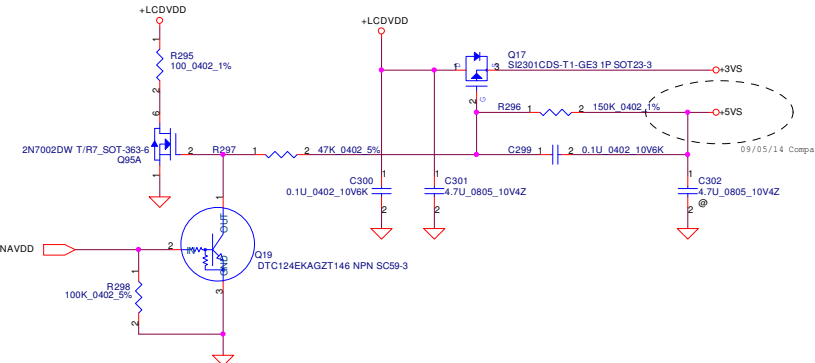
LCD/PANEL BD. CONN.



Webcam POWER CIRCUIT



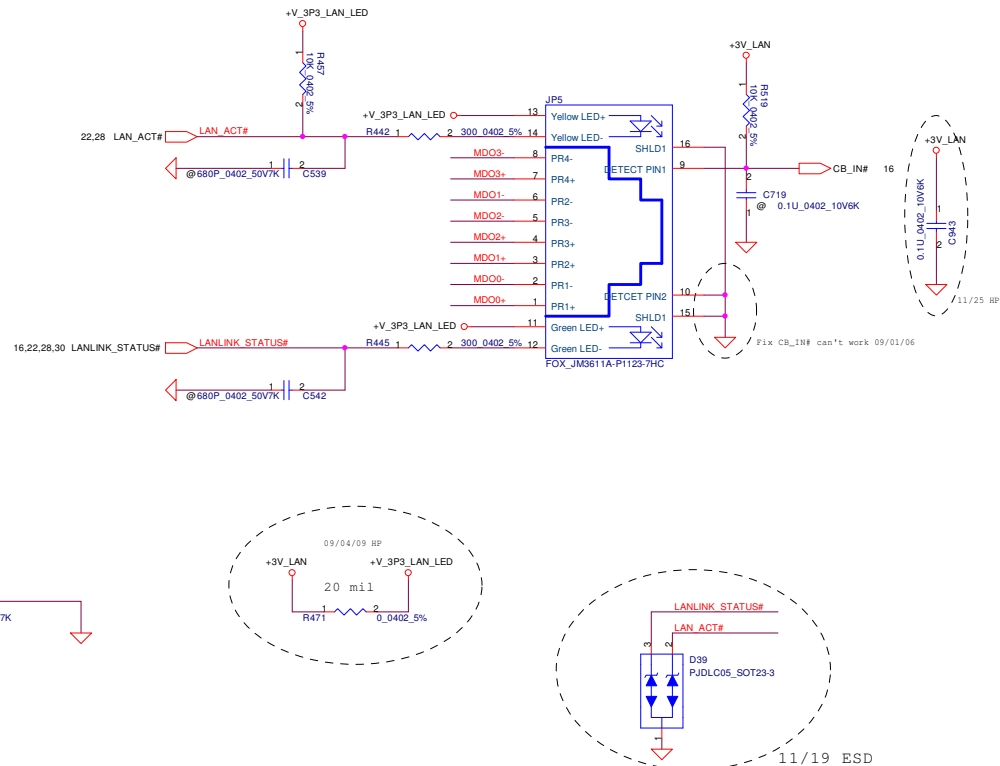
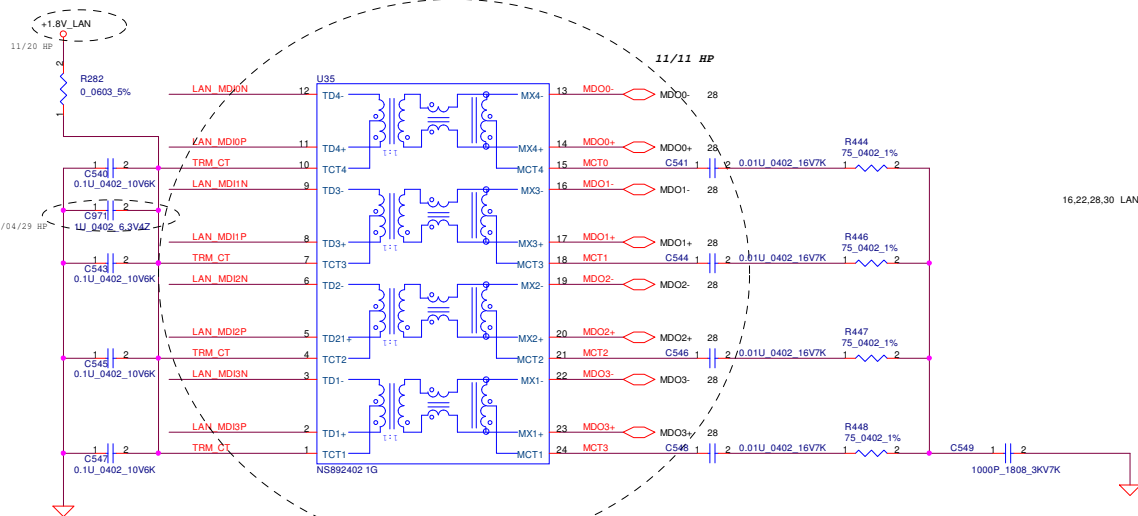
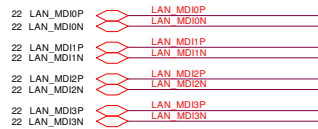
LCD POWER CIRCUIT



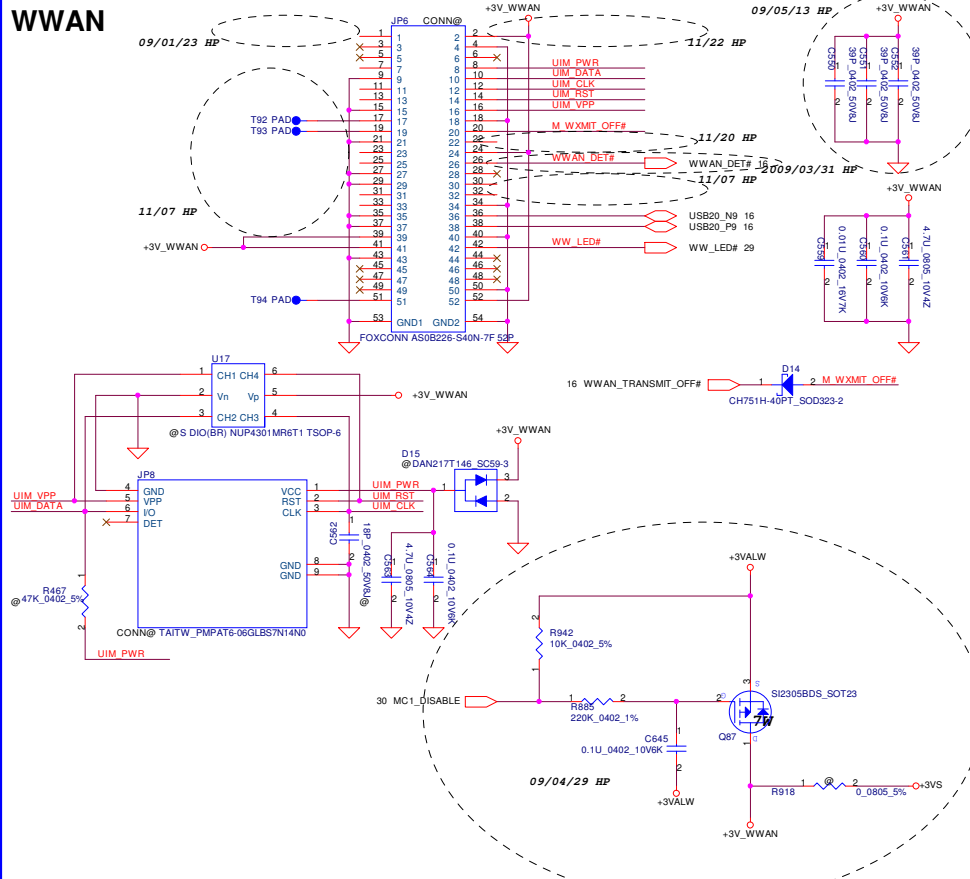
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				Date:	Saturday, May 16, 2009
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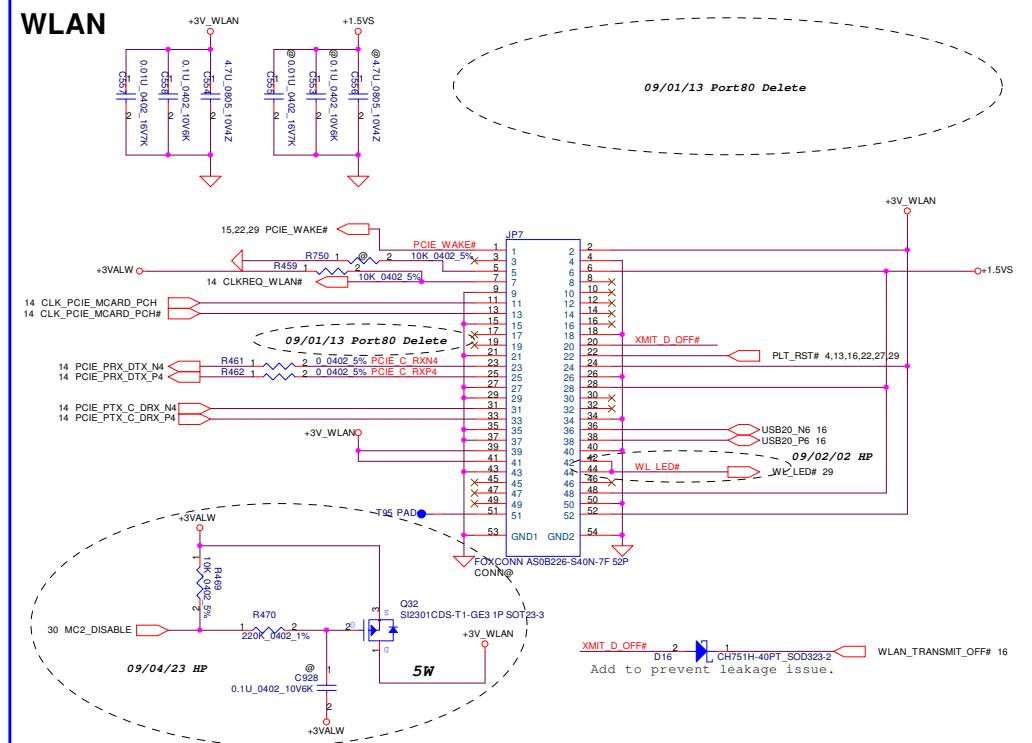
LCD CONN & O-Switch & GPIO Ext.



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WWAN

WLAN



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				Date:	Saturday, May 16, 2009	Sheet 24 of 45

[illegible][illegible][illegible]

INT_KBD_CONN.

30 KSI0[0..13] KSI00..13

20 KSI[0..7] KSI00..7

Pinout Table:

Pin	Signal	Pin	Signal
1	KSI011	31	KSI04
2	KSI00	32	KSI07
3	KSI02	33	KSI06
4	KSI05	34	KSI010
5	KSI D 14	35	KSI01
6	KSI D 8	36	KSI D 5
7	KSI D 10	37	KSI D 6
8	KSI D 0	38	KSI D 1
9	KSI D 4	39	KSI D 2
10	KSI D 15	40	KSI D 3
11	KSI D 17	41	KSI D 4
12	KSI D 13	42	KSI D 5
13	KSI D 16	43	KSI D 6
14	KSI D 12	44	KSI D 7
15	KSI D 18	45	KSI D 8
16	KSI D 19	46	KSI D 9
17	KSI D 1	47	KSI D 10
18	KSI D 2	48	KSI D 11
19	KSI D 3	49	KSI D 12
20	KSI D 4	50	KSI D 13
21	KSI03	51	KSI09
22	KSI08	52	KSI08
23	KSI07	53	KSI05
24	KSI06	54	KSI02
25	KSI010	55	KSI01
26	KSI01	56	KSI04
27	KSI02	57	KSI07
28	KSI03	58	KSI06
29	KSI04	59	KSI09
30	KSI05	60	KSI08

Internal Components:

- CP1, CP2, CP3, CP4, CP5, CP6, CP7: 100P_1206_8P4C_50V8K capacitors.
- CS01, CS02, CS03, CS04, CS05, CS06, CS07, CS08, CS09, CS10, CS11, CS12, CS13, CS14, CS15, CS16, CS17, CS18, CS19, CS20, CS21, CS22, CS23, CS24, CS25, CS26, CS27, CS28, CS29, CS30, CS31, CS32, CS33, CS34, CS35, CS36, CS37, CS38, CS39, CS40, CS41, CS42, CS43, CS44, CS45, CS46, CS47, CS48, CS49, CS50, CS51, CS52, CS53, CS54, CS55, CS56, CS57, CS58, CS59, CS60: 100P_1206_8P4C_50V8K capacitors.
- C756: 100P_0402_50VBV capacitor.

Connector Details:

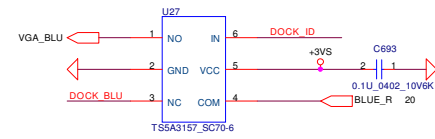
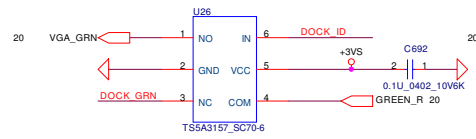
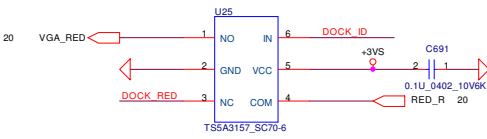
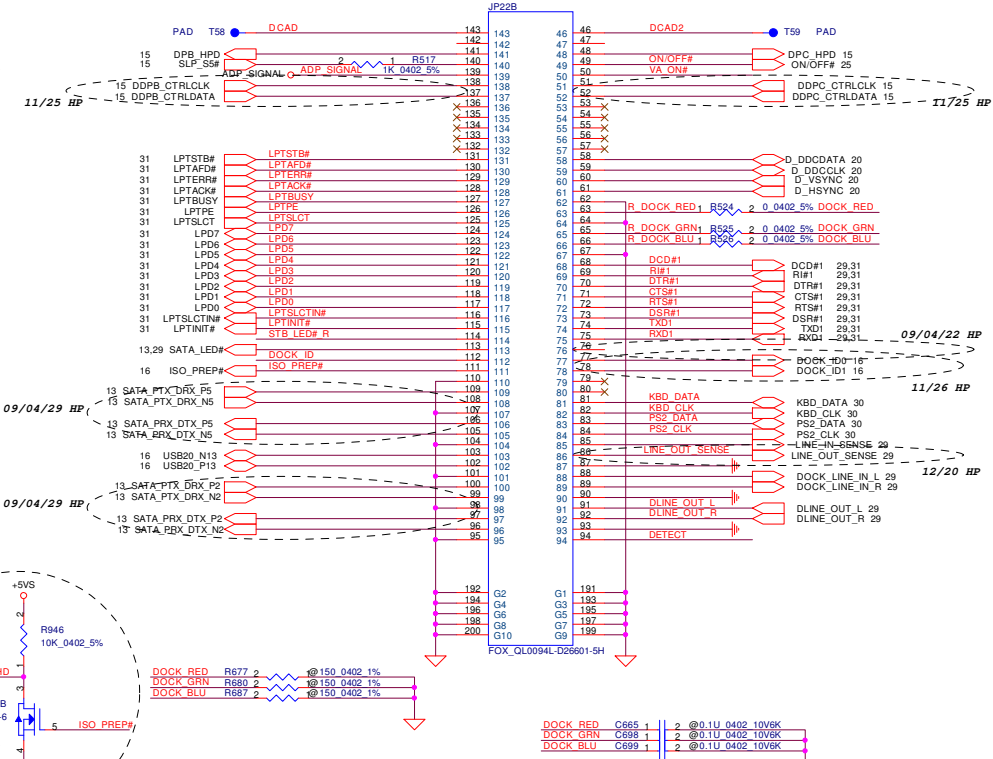
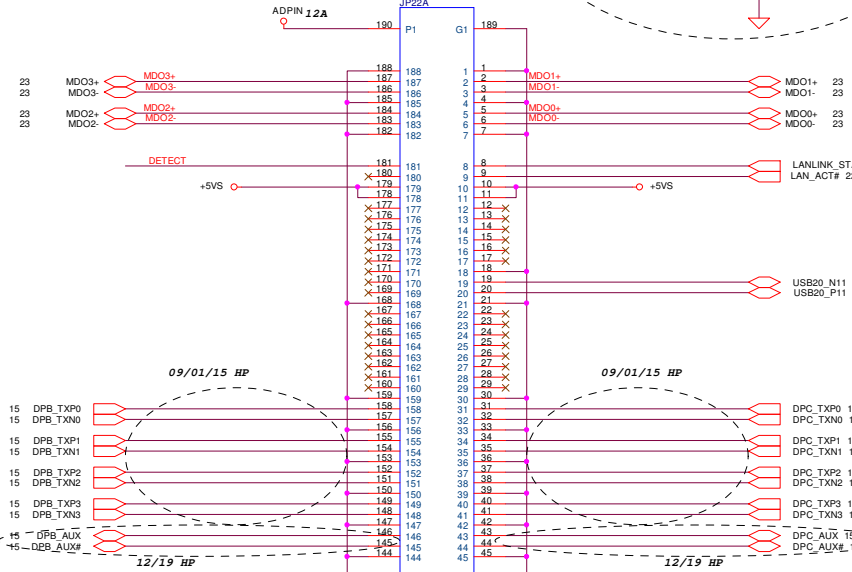
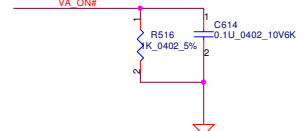
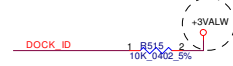
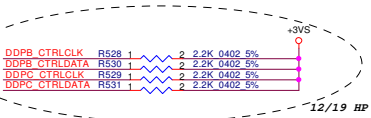
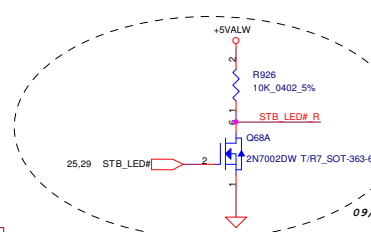
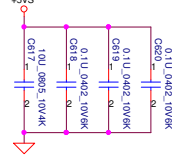
- CONN@ HIKOSE FHT2HP-305-SV 55 30P
- 11/11 HP

TrackPoint CONN.

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				Size	Document Number	Rev
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Date: Saturday, May 16, 2009				Sheet	25	of 45

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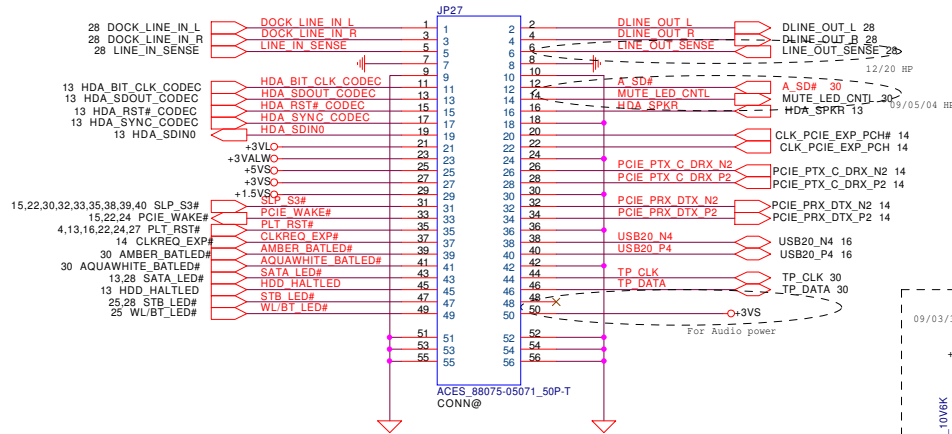
DOCKING CONNECTOR



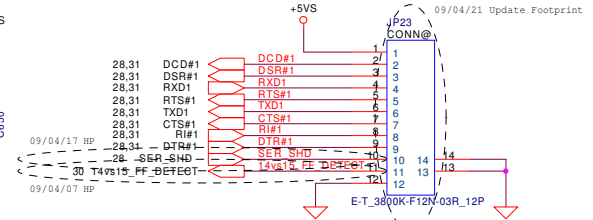
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L	ON	OFF
H	OFF	ON

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			Size	Document Number
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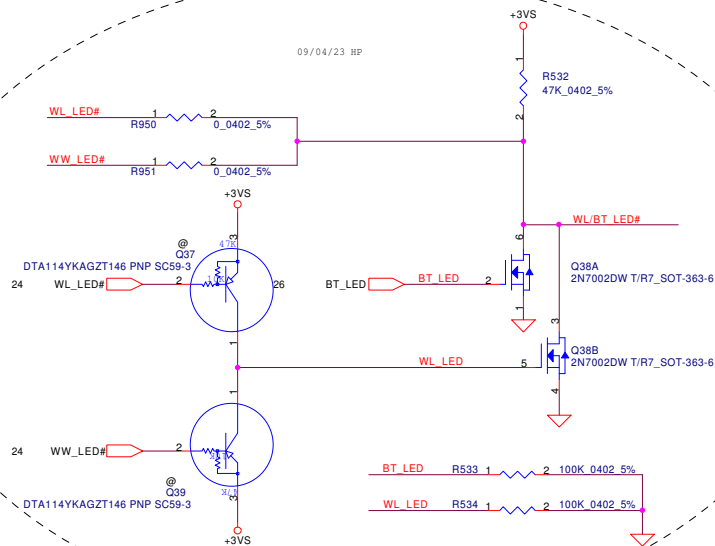
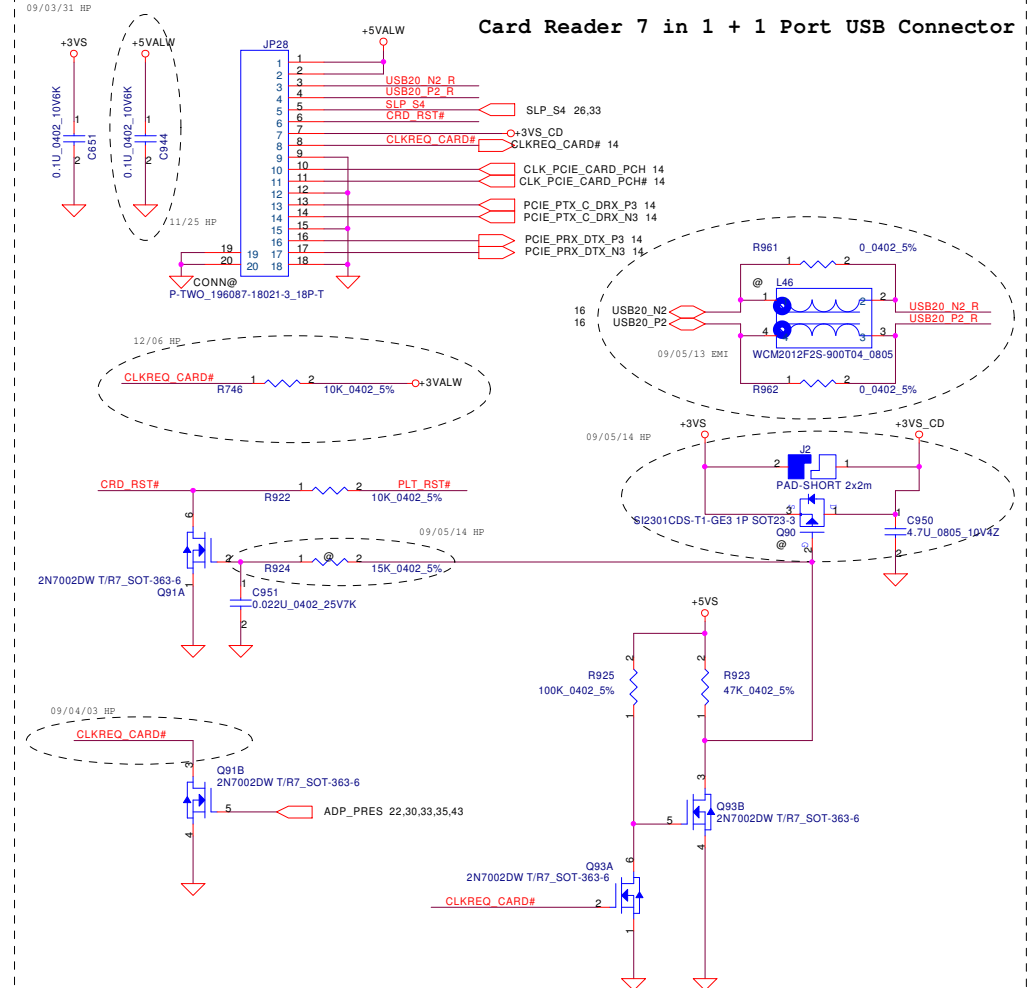
Audio/Express Card/TP/LEDs Connector



Serial Port CONN



Card Reader 7 in 1 + 1 Port USB Connector



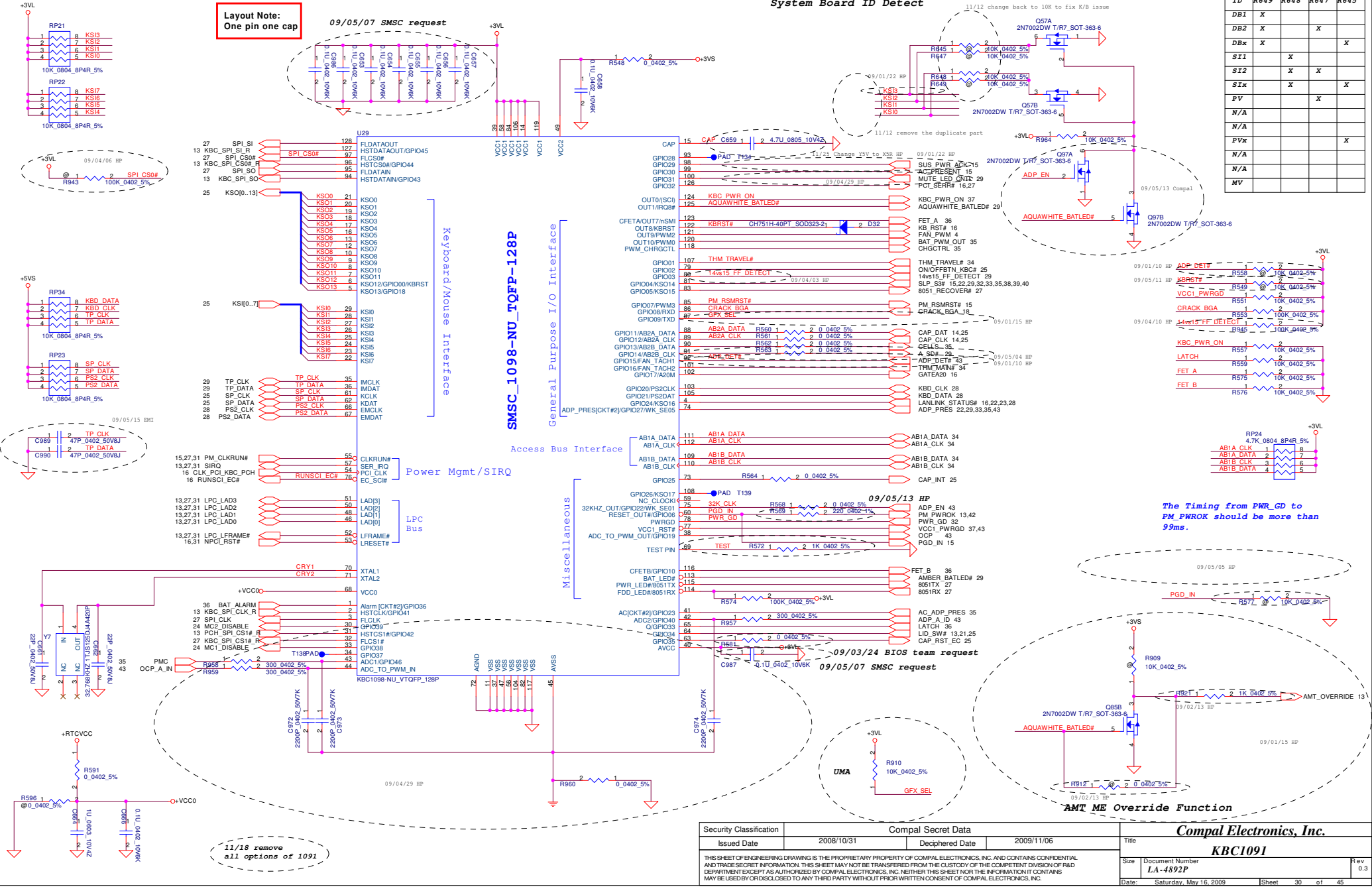
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Layout Note:
One pin one cap

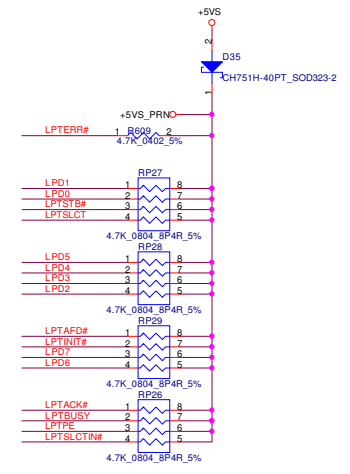
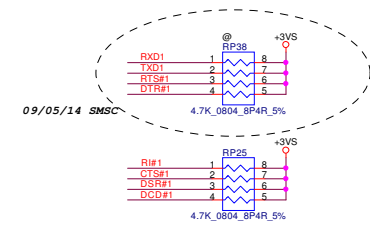
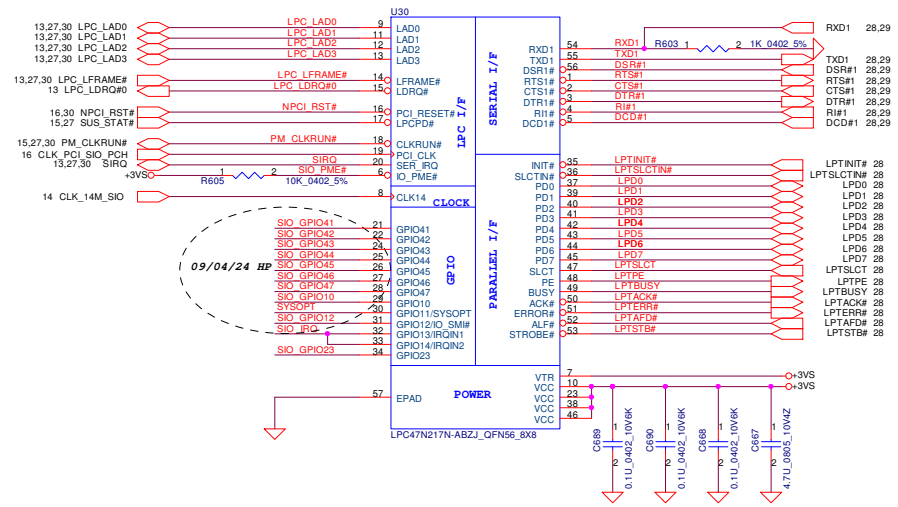
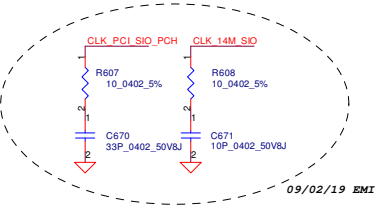
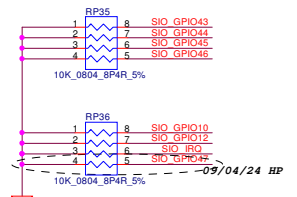
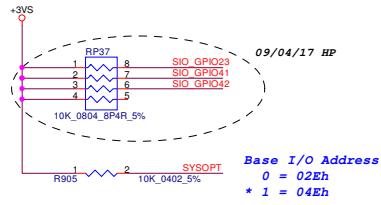
09/05/07 SMSC request

System Board ID Detect

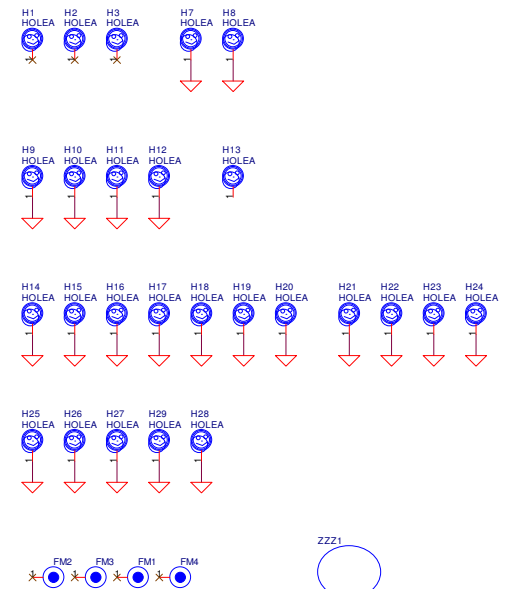
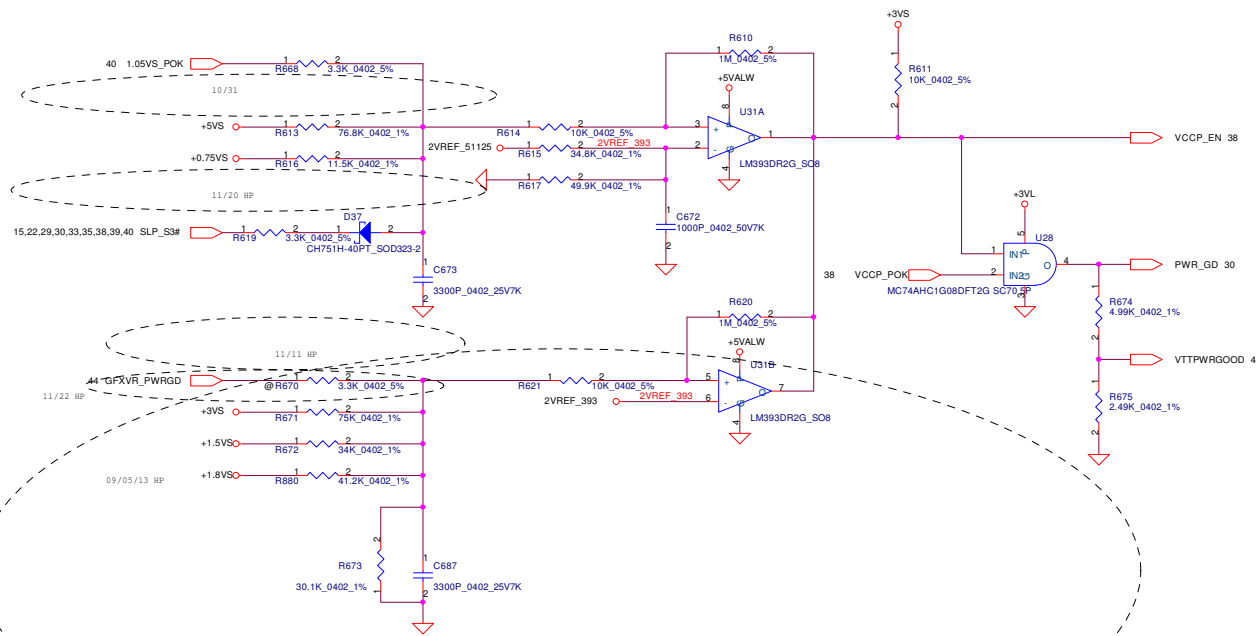
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SIx		X		X
PV			X	
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N/A				
PVx				X
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MV				



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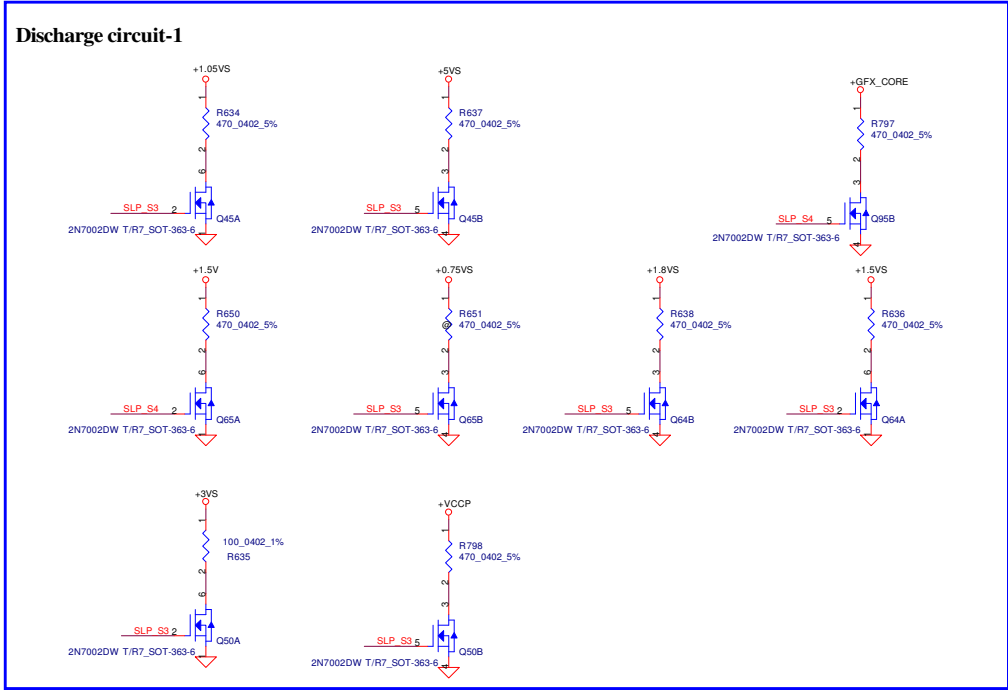
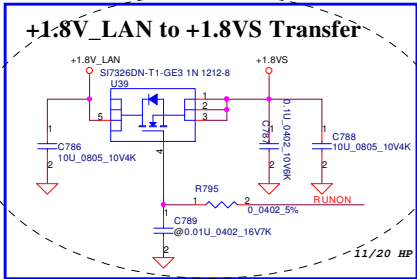
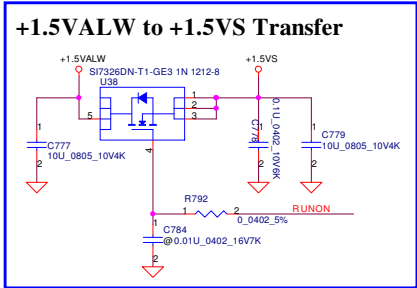
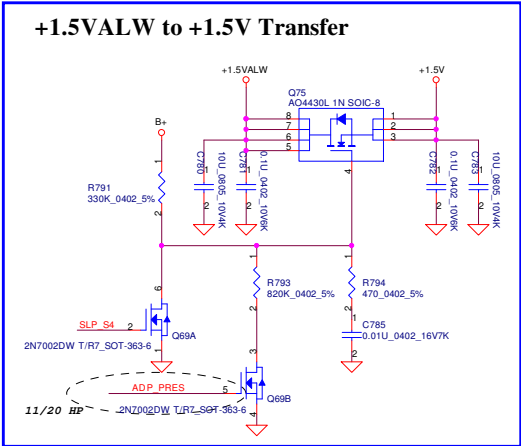
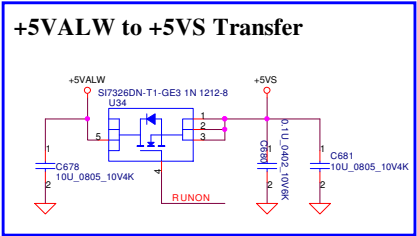
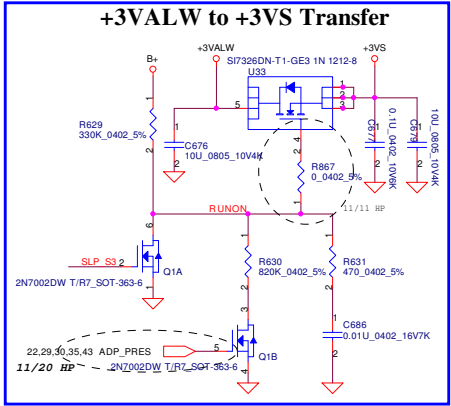


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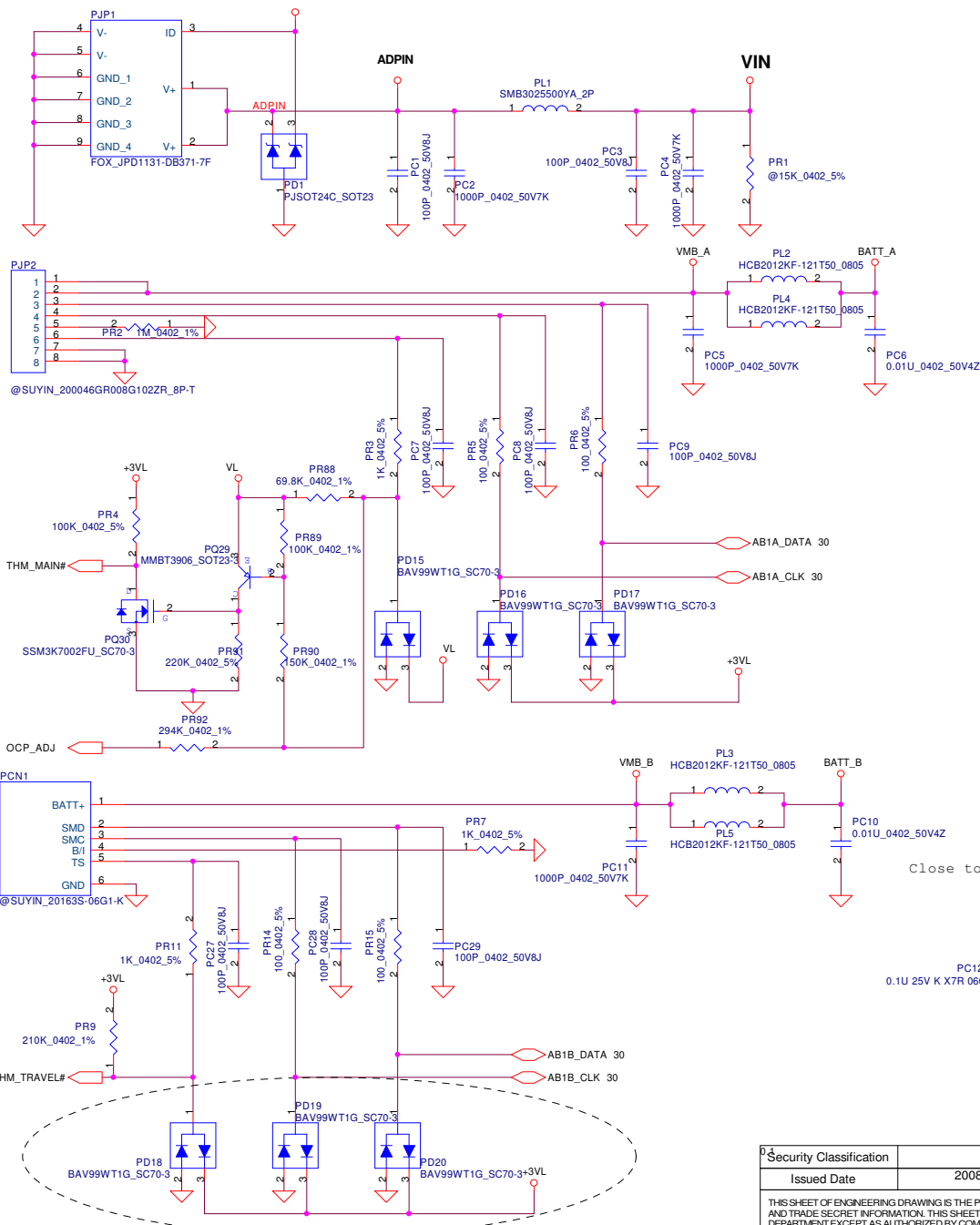
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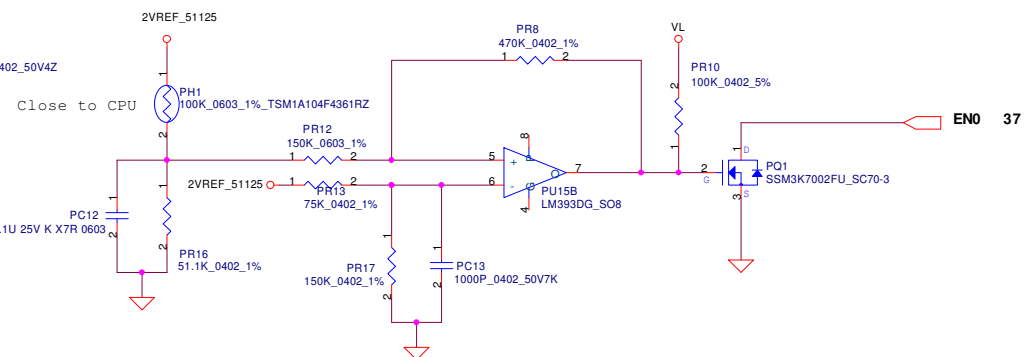


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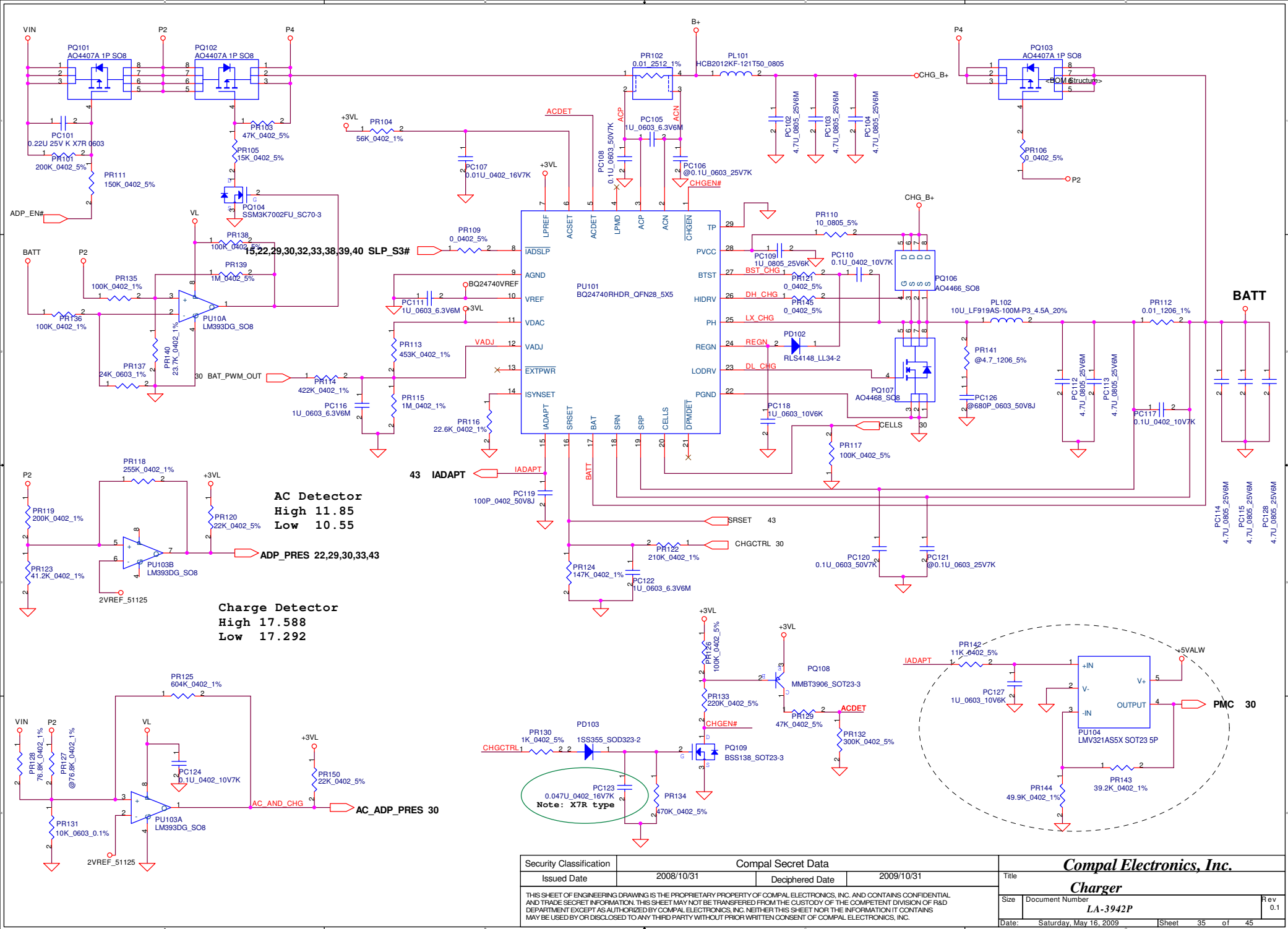
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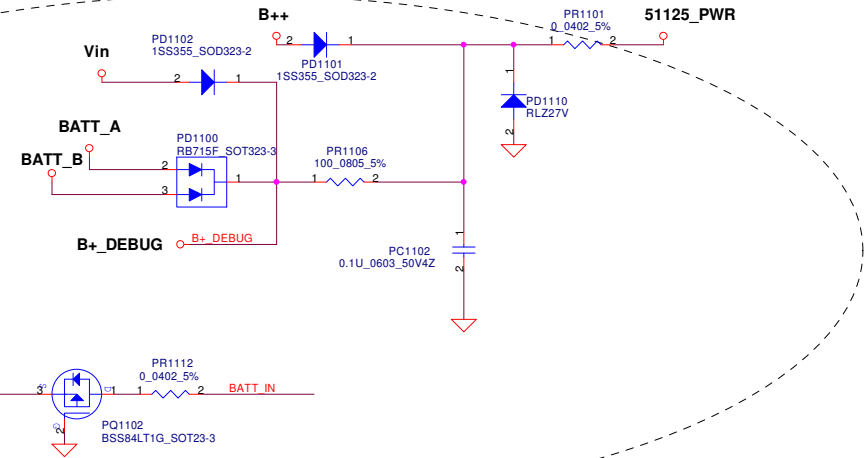
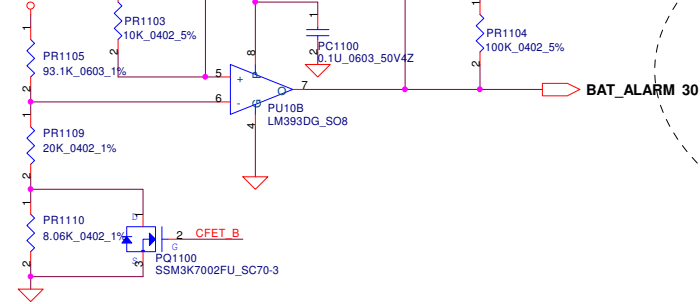
PH1 under CPU bottom side :
CPU thermal protection at 90 +/-3 degree C
(Need to be checked)



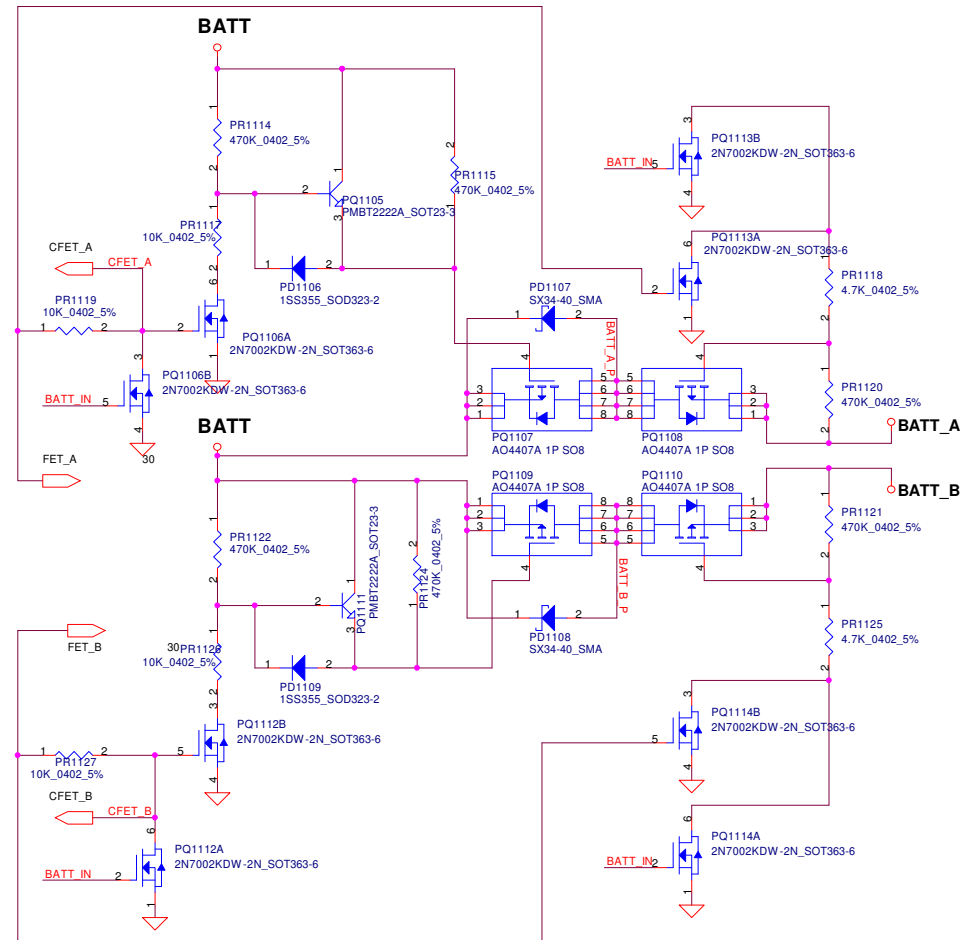
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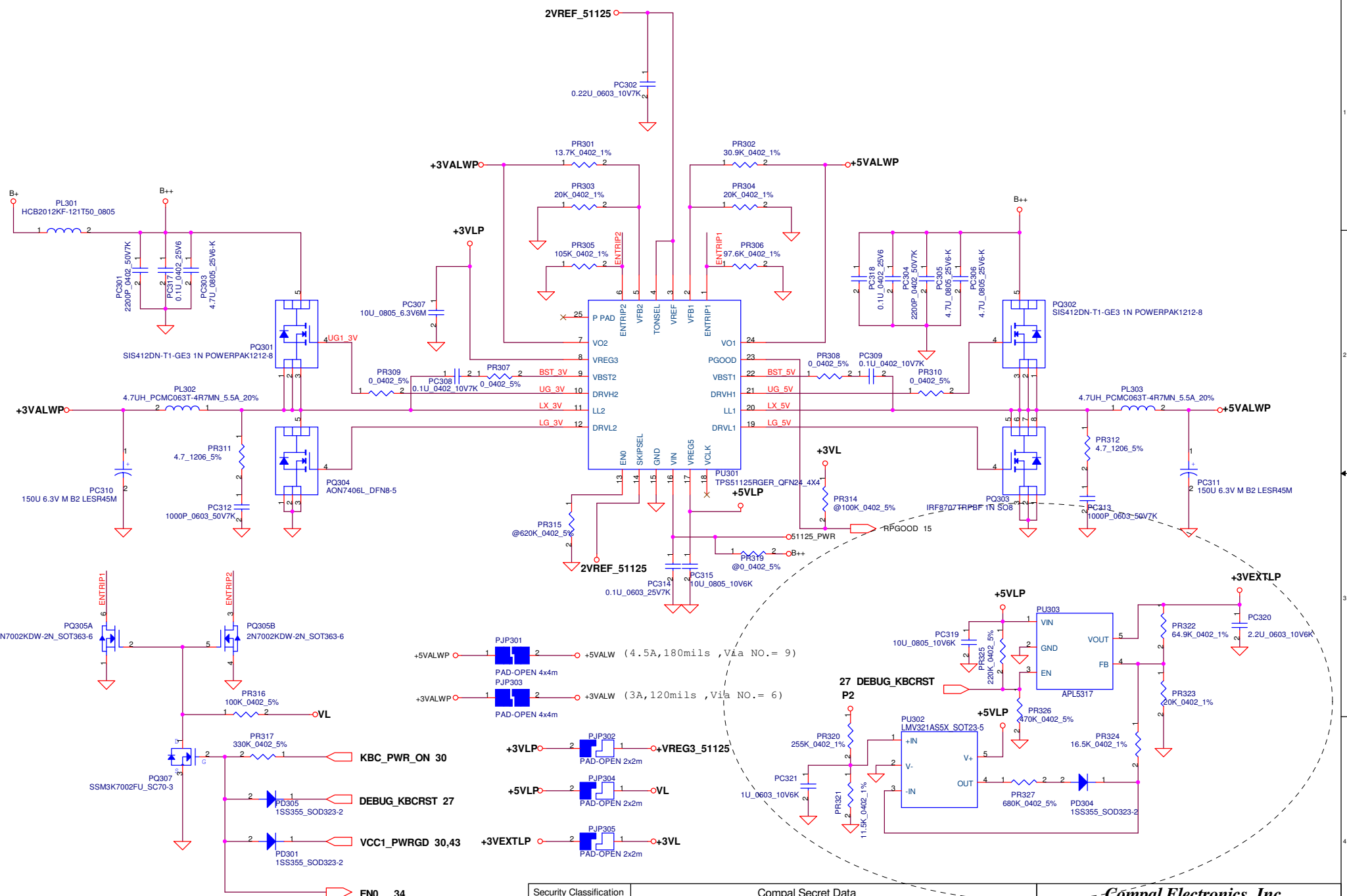


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				Date:	Saturday, May 16, 2009
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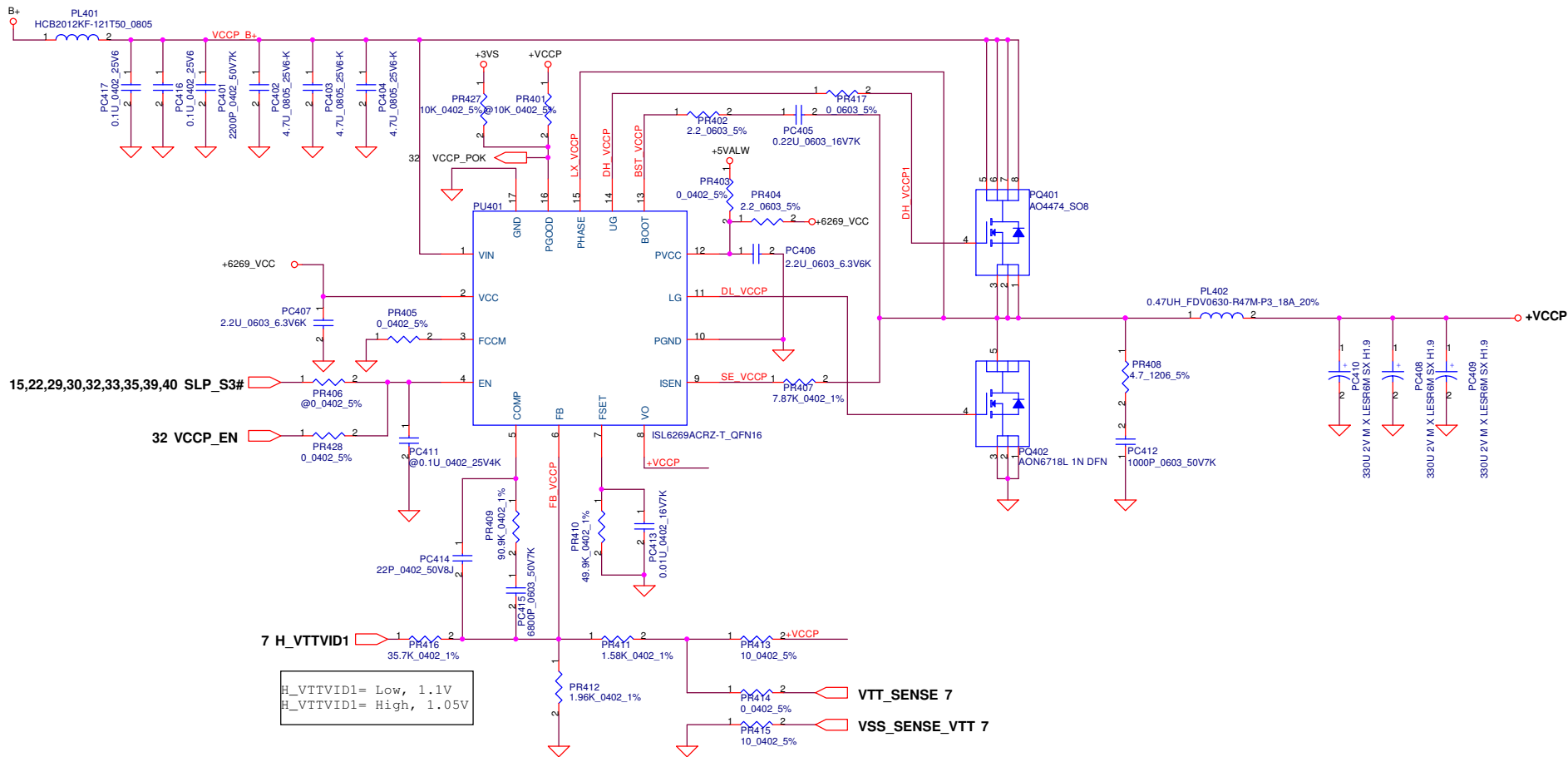
Battery selector

Rev

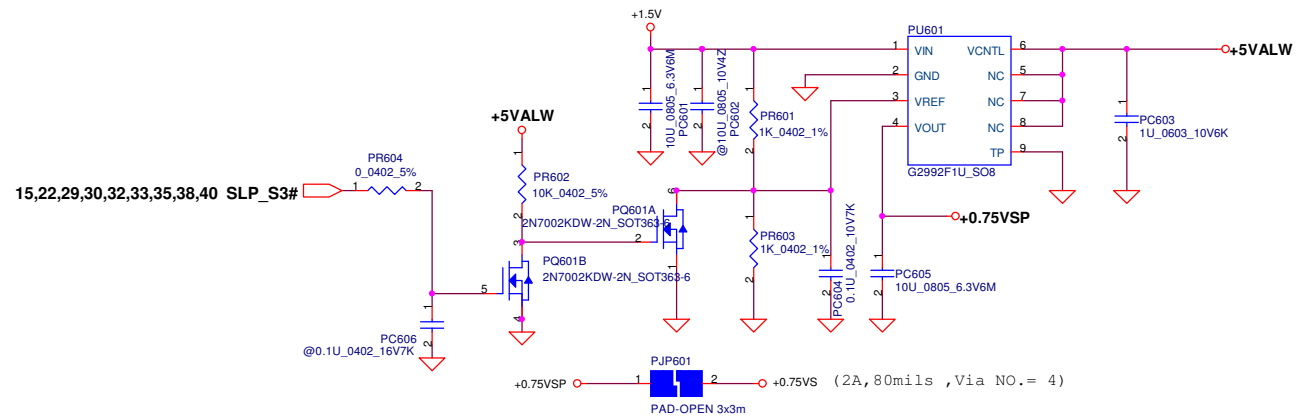


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				Saturday, May 16, 2009	0.1
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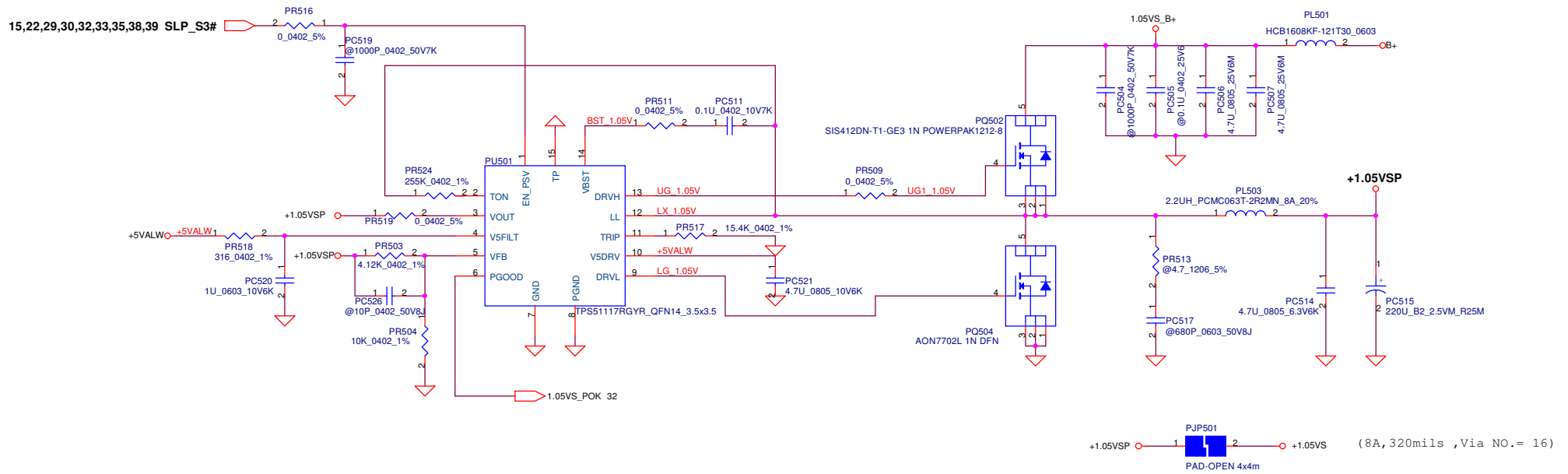
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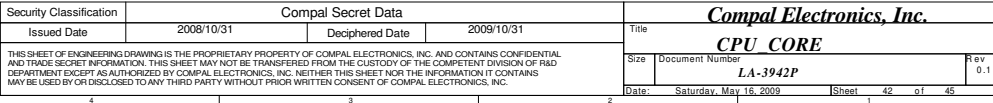
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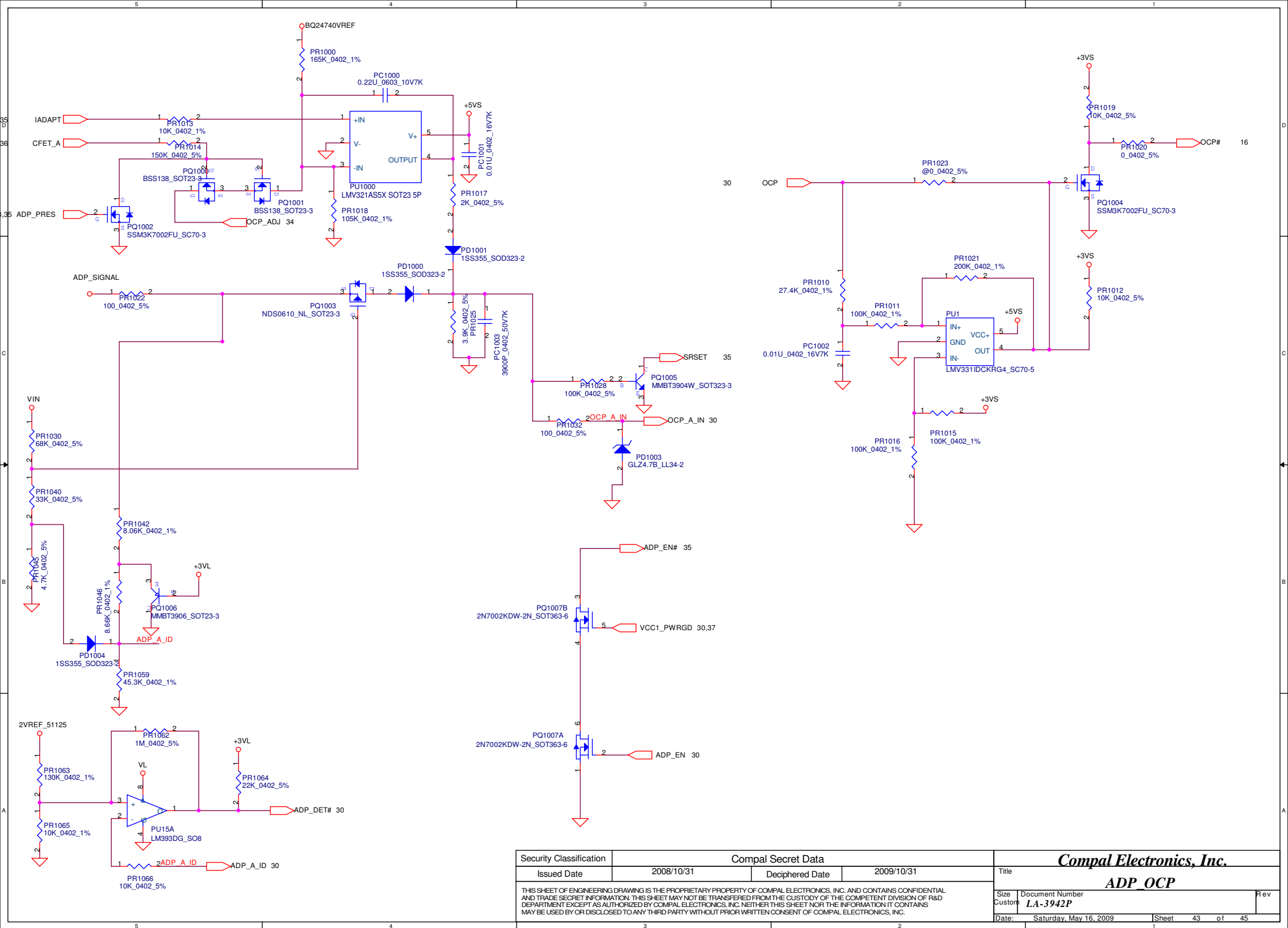


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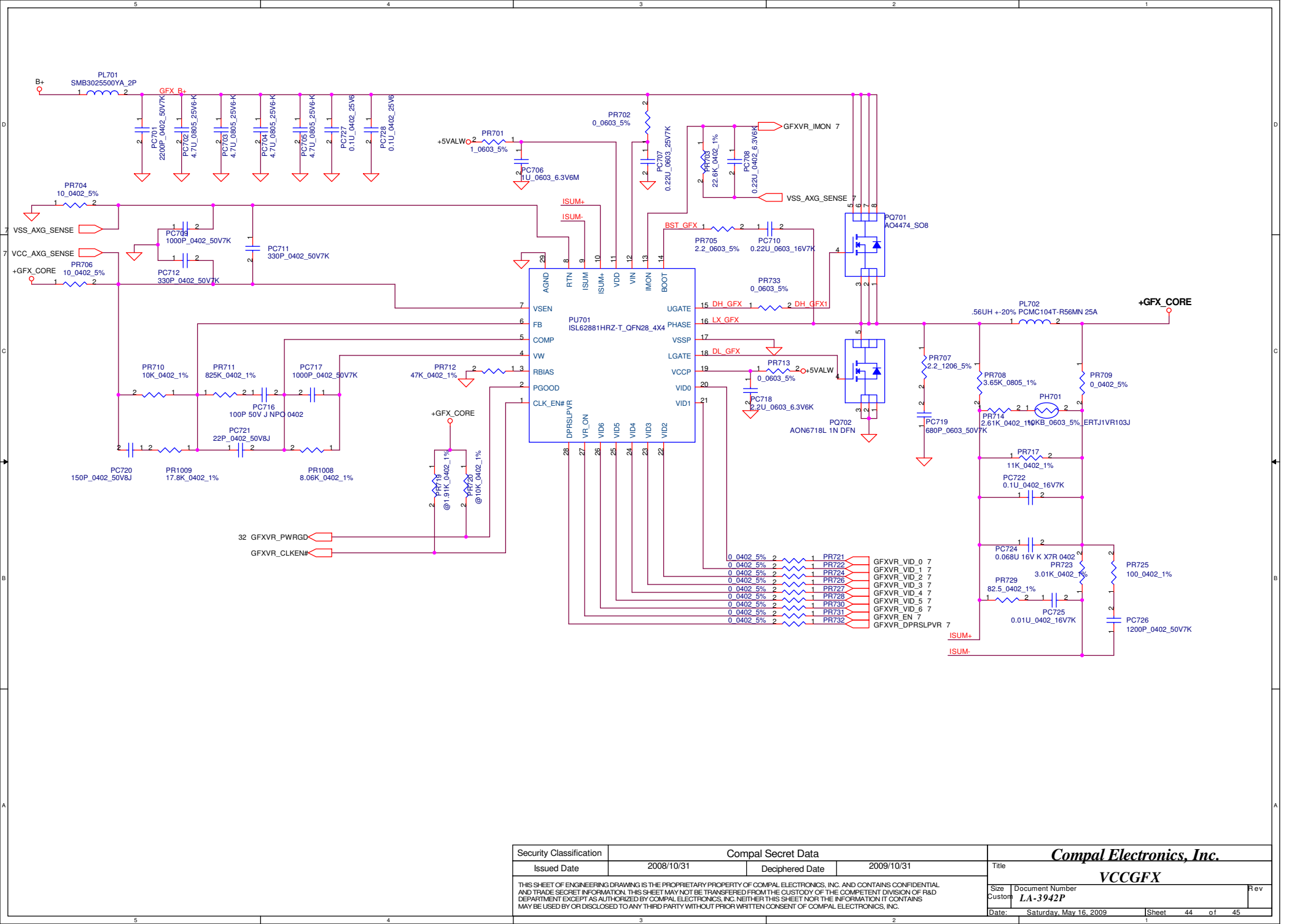


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