Huron Block Diagram

Project code: 91.4V301.001
PCB P/N : 07205
REVISION : SD

CLK GEN.
IDTCV125PAG 71.00125.A0W
RTM865T-433 71.00865.B0W
3

Mobile CPU
Yonah 478
Celeron M
62.10079.001 4, 5

FSB 400/533/667MHz

G792 20

TV Out 14
CRT 14
LCD 13
DVI 42

DDR2 533/667 MHz 13,14
533/667MHz

DDR2 533/667 MHz 13,14
533/667MHz

Calistoga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CALIS.00U 6,7,8,9,10

VGA Borad 26

DMI 100MHz

ICH7M
4 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
2 SATA
1 PATA 66/100
8 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
71.ICH7M.00U 15,16,17,18

Line In
MIC In 29
INT.MIC
INT.SPKR 29
Line Out (SPDIF)
SUBWF 29

Codec ALC268 28
AZALIA

OP AMP G1431Q 29
OP AMP G1412 29
OP AMP G1442 29

PCI BUS

OZ129 1394 CardReader 24
1394 CONN 25

Cardreader BD
PCB P/N:07517
MS/MS Pro/xD/ MMC/SD 5 in 1
MODEM Card 25
RJ11

AZALIA

PCI Express

Giga LAN 22
BCM5787MKMLG
TXFM 23
RJ45 23

New card 27
P2231NFC1 28

Mini Card
Kedron a/b/g/n 27

LPC BUS

KBC
Winbond
WPC8768L 30
SPI I/F
BIOS
W25X80-VSS 32

Touch Pad 31
INT. KB 31

USB

MINI USB
BlueTooth 22

HDD 20
SATA

CDROM 20
PATA

USB BD
PCB : 07521 21

USB 2 Port 21

CAMERA 13

MEDIA BD
56.41004.031 31

PWM BD
PCB : 07520 31

LAUNCH BD
PCB : 07519 31

e-Key BD
PCB : 07518 31

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC TPS51120 37	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5

SYSTEM DC/DC TPS51124 38	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D05V_S0

TPS51100 40	
1D8V_S3	DDR_VREF

APL5308 40	
3D3V_S0	2D5V_S0

APL5912 39	
1D8V_S3	1D5V_S0

Intersil CHARGER MAX8731 41	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6262 35	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 48A

Volvi

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Title: BLOCK DIAGRAM
Size: A3 | Document Number: HURON | Rev: SD
Date: Monday, March 12, 2007 | Sheet 1 of 44

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

RTM865T-433 100Mhz/LCDCLK Spread and Frequency Selection Table

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	0.8% Down
0	0	0	1	1.0% Down
0	0	1	0	1.25% Down
0	0	1	1	1.50% Down
0	1	0	0	1.75% Down
0	1	0	1	2.0% Down
0	1	1	0	2.5% Down
0	1	1	1	3.0% Down
1	0	0	0	+-0.3% Center
1	0	0	1	+-0.4% Center
1	0	1	0	+-0.5% Center
1	0	1	1	+-0.6% Center
1	1	0	0	+-0.8% Center
1	1	0	1	+-1.0% Center
1	1	1	0	+-1.25% Center
1	1	1	1	+-1.5% Center

PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
OZ129TZ	AD22	A→G	REQ0# ->REQ0#

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	MINICARD
5	BlueTooth
6	CCD
7	NewCard

Calistoga Strapping Signals and Configuration

EDS 17050 0.71

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

<Core Design>

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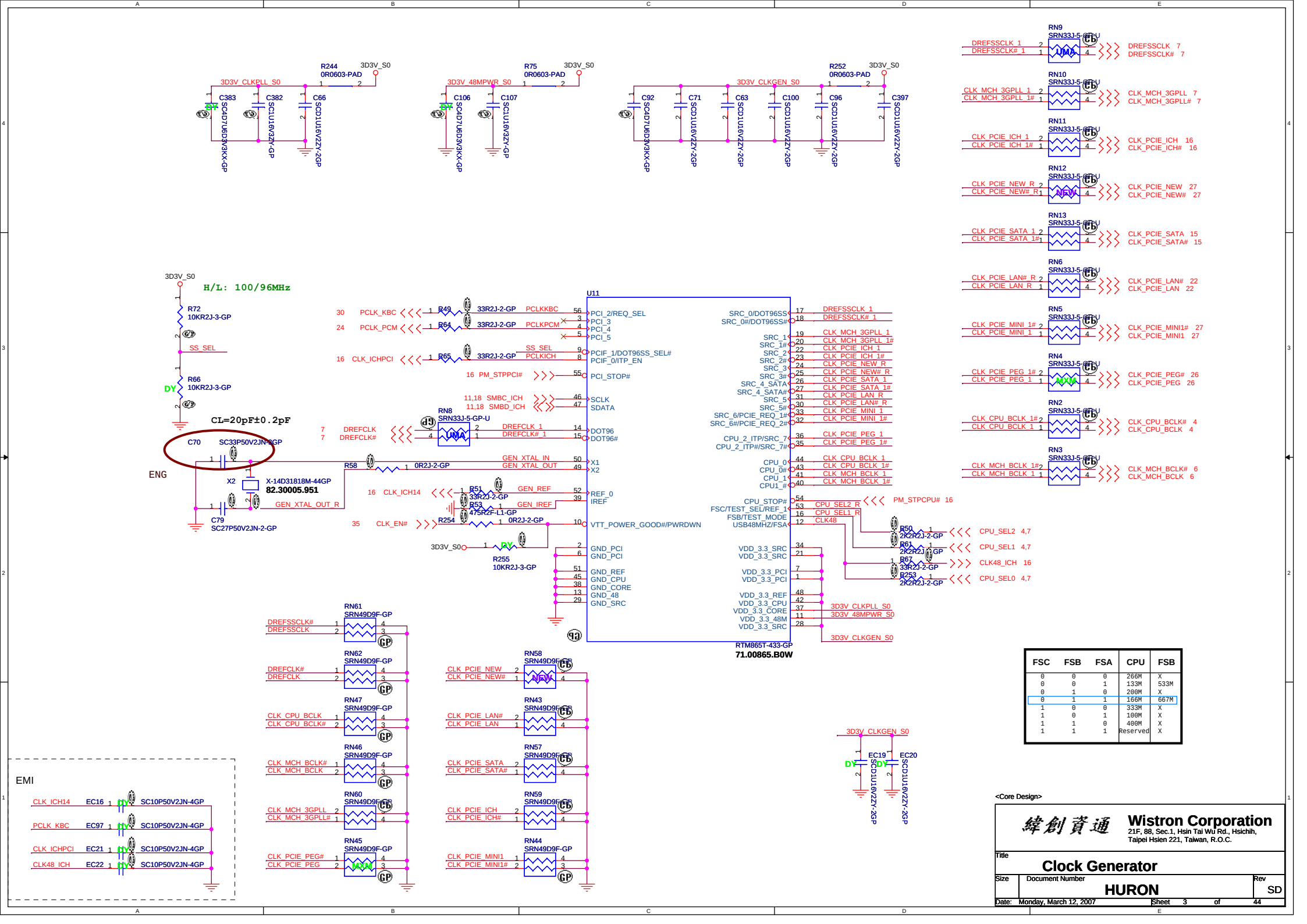
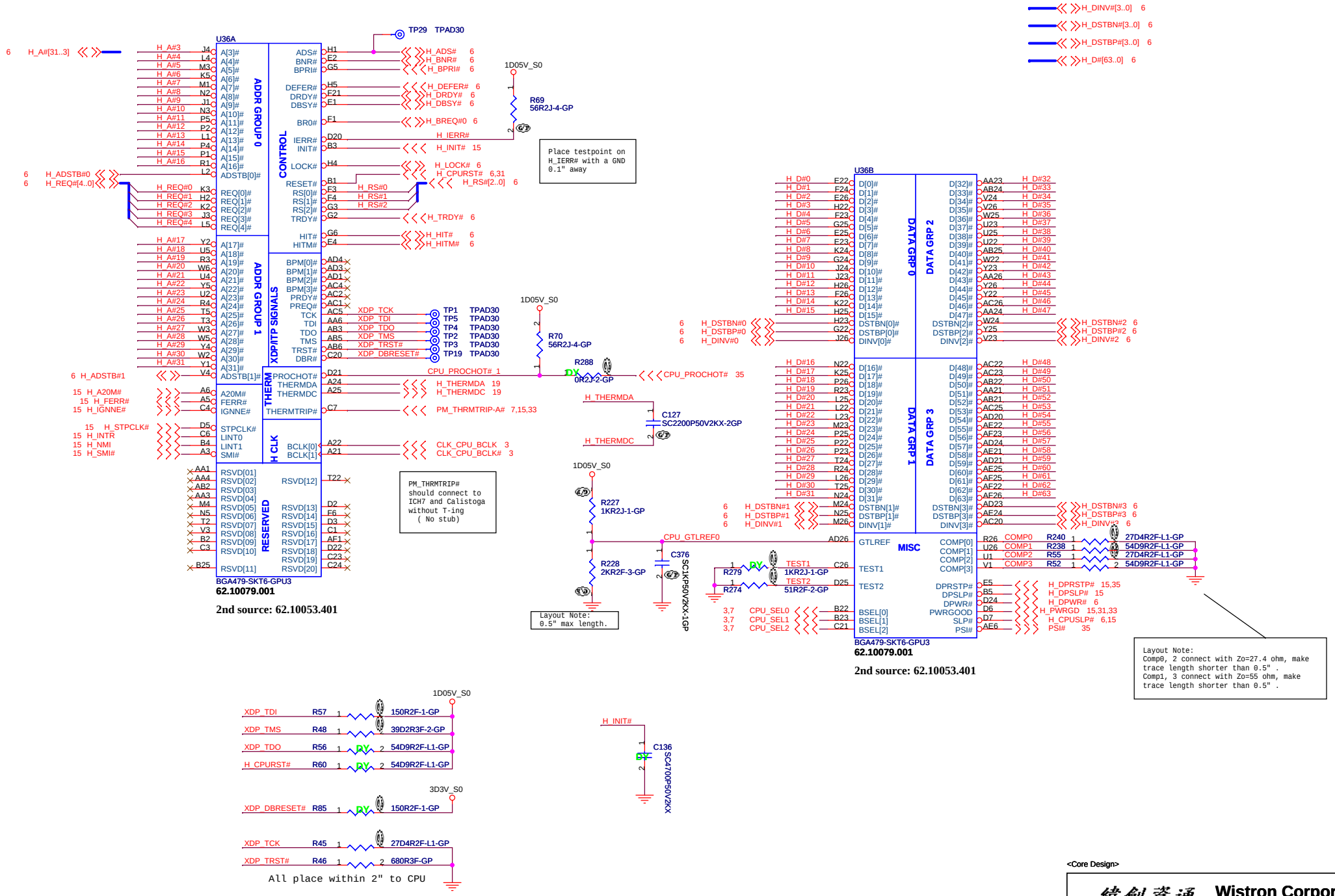
Title: Reference

Size | Document Number: HURON | Rev: SD

Date: Monday, March 12, 2007 | Sheet 2 of 44


3D3V_S0
H/L: 100/96MHz
R72 10KR2J-3-GP
SS_SEL
R66 10KR2J-3-GP
CL=20pF±0.2pF
C70 SC33P50V2JN-4GP
ENG
X2 X-14D31818M-44GP 82.30005.951
C79 SC27P50V2JN-2-GP
R58 0R2J-2-GP
GEN_XTAL_OUT_R
U11
RTM865T-433-GP
71.00865.B0W
PCLK_KBC
PCLK_PCM
CLK_ICHPCI
PM_STPPCI#
SMBC_ICH
SMBD_ICH
DREFCLK
DREFCLK#
CLK_ICH14
CLK_EN#
GEN_XTAL_IN
GEN_XTAL_OUT
GEN_REF
GEN_IREF
VTT_POWER_GOOD#/PWRDWN
PM_STPCPU#
CPU_SEL2
CPU_SEL1
CLK48
CLK48_ICH
CPU_SEL0
3D3V_CLKPLL_S0
3D3V_48MPWR_S0
3D3V_CLKGEN_S0
R244 0R0603-PAD
R75 0R0603-PAD
R252 0R0603-PAD
C383 C382 C66
C106 C107
C92 C71 C63 C100 C96 C397
RN9 RN10 RN11 RN12 RN13 RN6 RN5 RN4 RN2 RN3
DREFSSCLK_1 DREFSSCLK# 1
CLK_MCH_3GPLL_1 CLK_MCH_3GPLL_1#
CLK_PCIE_ICH_1 CLK_PCIE_ICH_1#
CLK_PCIE_NEW_R CLK_PCIE_NEW# R
CLK_PCIE_SATA_1 CLK_PCIE_SATA_1#
CLK_PCIE_LAN# R CLK_PCIE_LAN R
CLK_PCIE_MINI_1# CLK_PCIE_MINI_1
CLK_PCIE_PEG_1# CLK_PCIE_PEG_1
CLK_CPU_BCLK_1# CLK_CPU_BCLK_1
CLK_MCH_BCLK_1# CLK_MCH_BCLK_1
RN61 RN62 RN47 RN46 RN60 RN45
RN58 RN43 RN57 RN59 RN44
EMI
CLK_ICH14 EC16 SC10P50V2JN-4GP
PCLK_KBC EC97 SC10P50V2JN-4GP
CLK_ICHPCI EC21 SC10P50V2JN-4GP
CLK48_ICH EC22 SC10P50V2JN-4GP
EC19 EC20 SCD1U16V2ZY-2GP
FSC FSB FSA CPU FSB
0 0 0 266M X
0 0 1 133M 533M
0 1 0 200M X
0 1 1 166M 667M
1 0 0 333M X
1 0 1 100M X
1 1 0 400M X
1 1 1 Reserved X
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator
Size
Document Number
HURON
Rev
SD
Date: Monday, March 12, 2007
Sheet 3 of 44



<Core Design>

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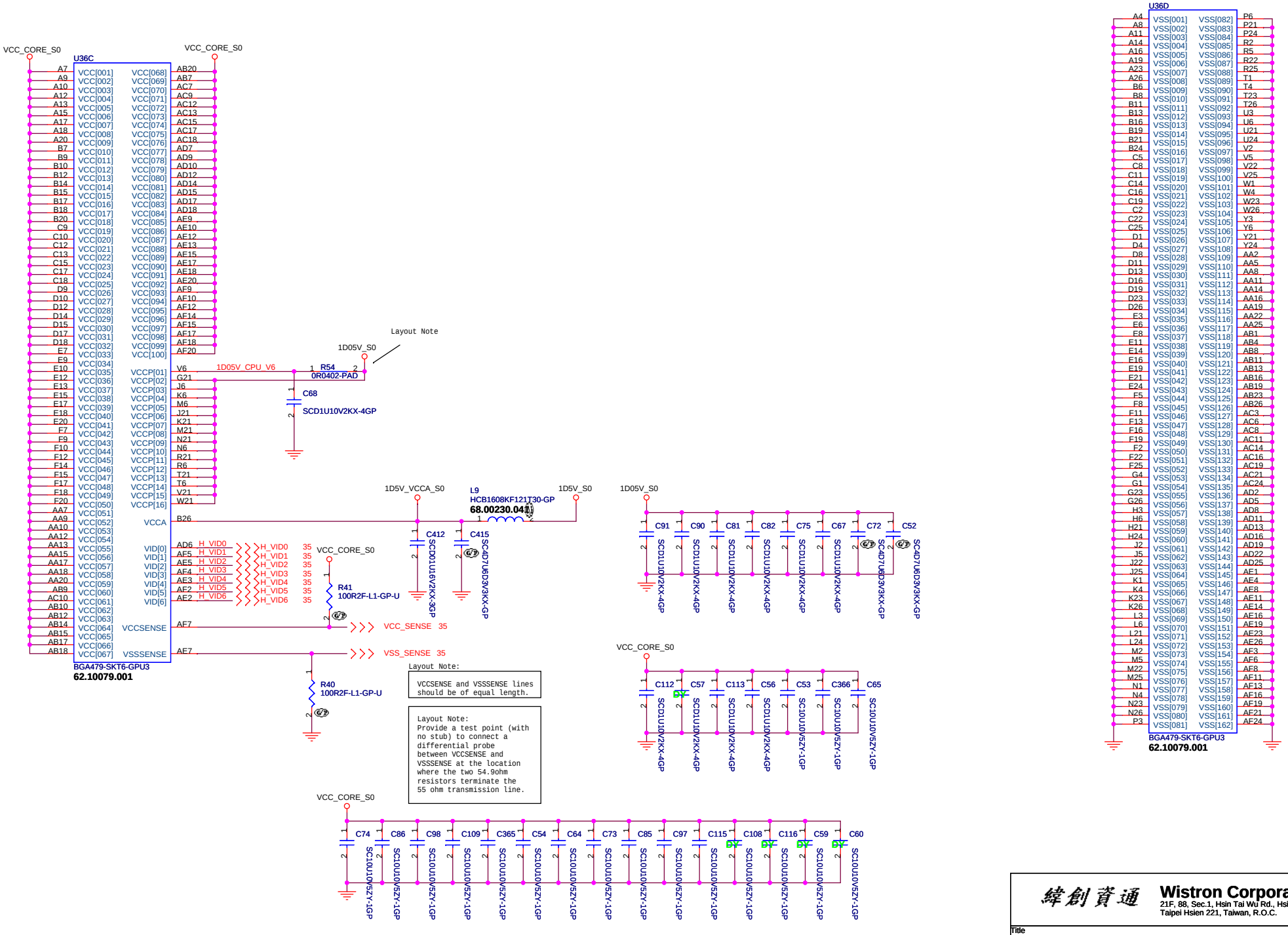
Title: CPU (1 of 2)

Size | Document Number: HURON | Rev: SD

Date: Monday, March 12, 2007 | Sheet 4 of 44



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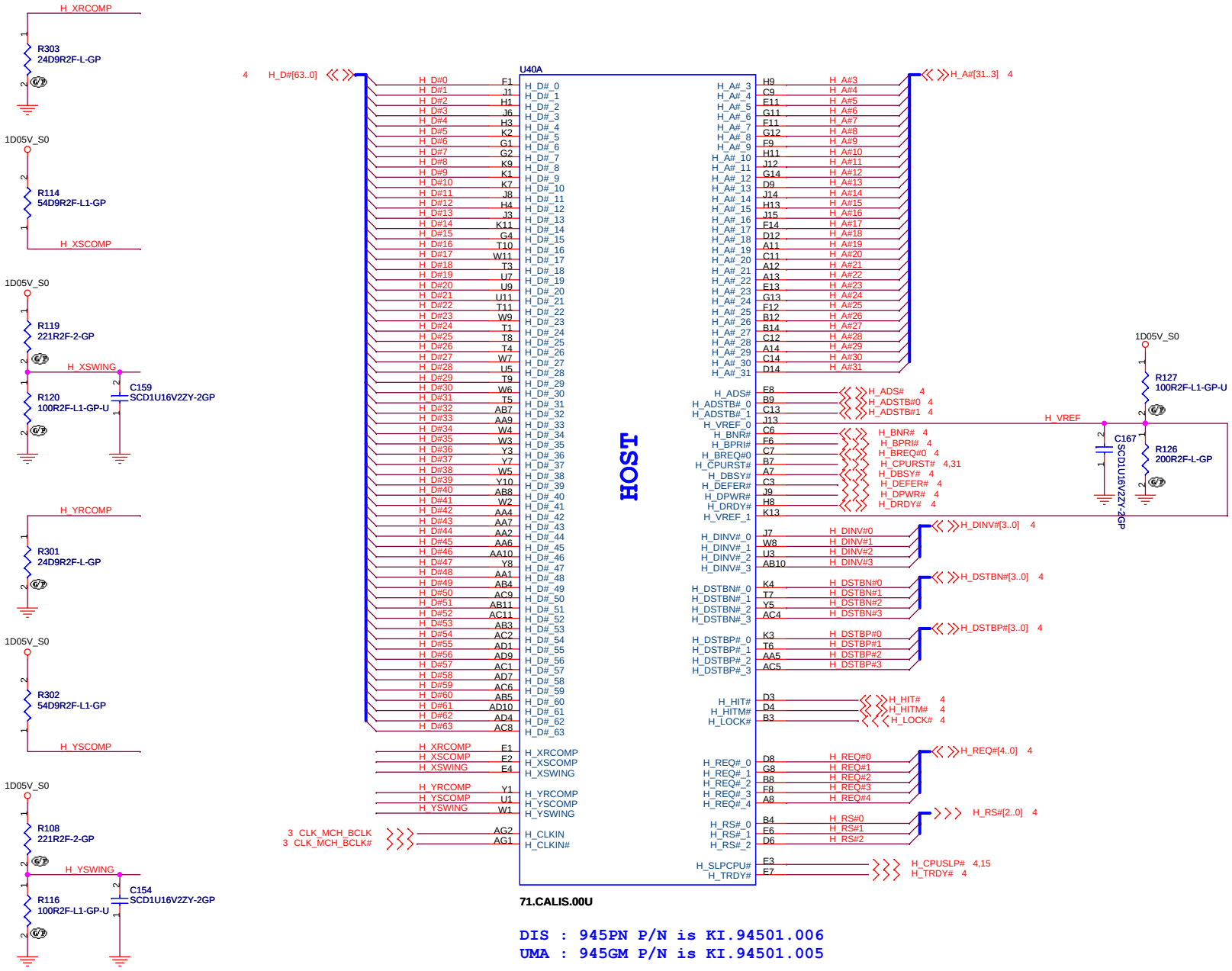
Title	CPU (2 of 2)
Size	Document Number: HURON — Rev: SD
Date: Monday, March 12, 2007	Sheet 5 of 44



Place them near to the chip (< 0.5")

<Core Design>

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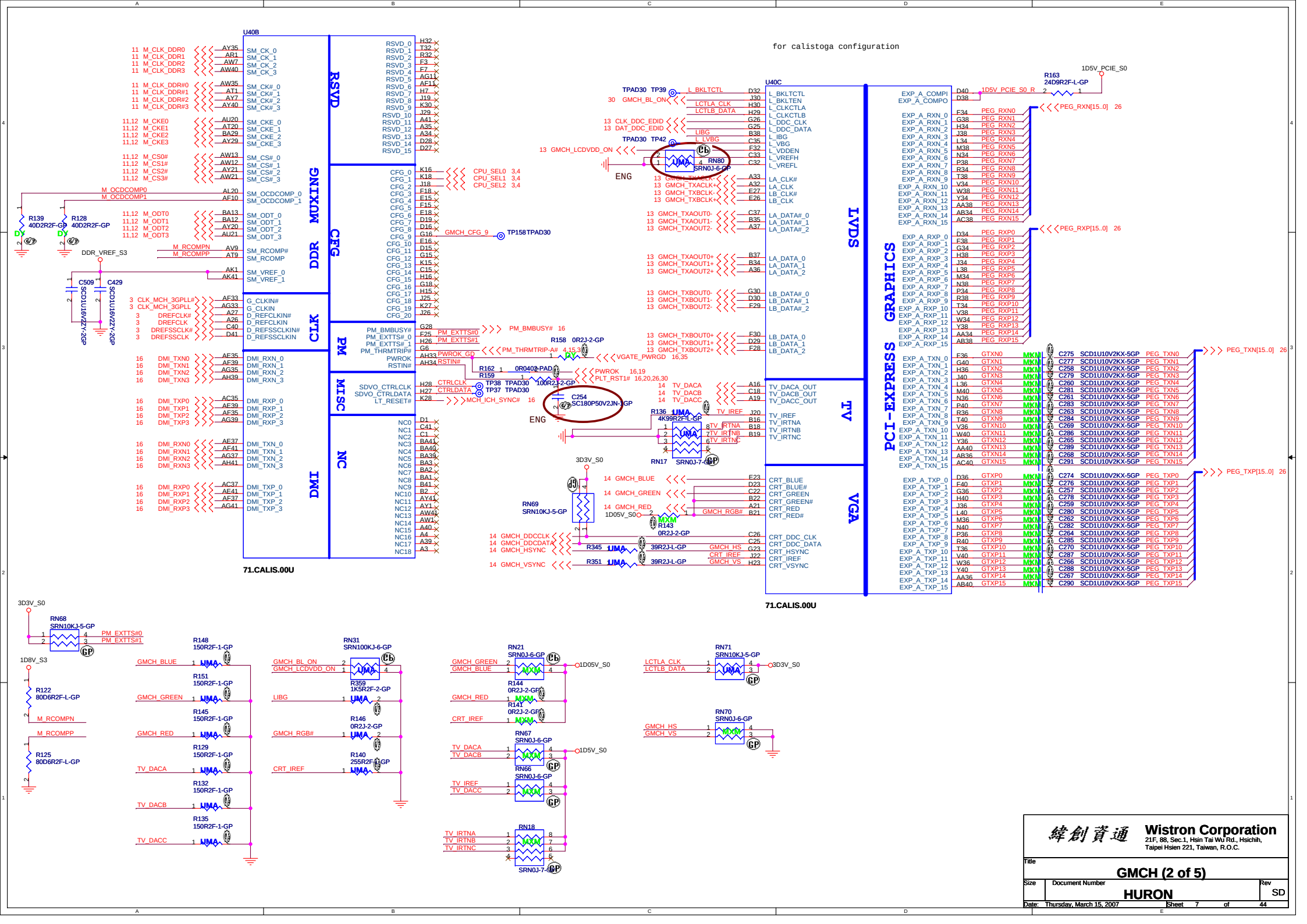
Title: **GMCH (1 of 5)**

Size | Document Number: **HURON** | Rev: SD

Date: Monday, March 12, 2007 | Sheet 6 of 44


for calistoga configuration
U40B
U40C
SM_CK_0
SM_CK_1
SM_CK_2
SM_CK_3
SM_CK#_0
SM_CK#_1
SM_CK#_2
SM_CK#_3
SM_CKE_0
SM_CKE_1
SM_CKE_2
SM_CKE_3
SM_CS#_0
SM_CS#_1
SM_CS#_2
SM_CS#_3
SM_OCDCOMP_0
SM_OCDCOMP_1
SM_ODT_0
SM_ODT_1
SM_ODT_2
SM_ODT_3
SM_RCOMP#
SM_RCOMP
SM_VREF_0
SM_VREF_1
DDR MUXING
CFG
CLK
PM
MISC
NC
DMI
RSVD
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
71.CALIS.00U
71.CALIS.00U
Wistron Corporation
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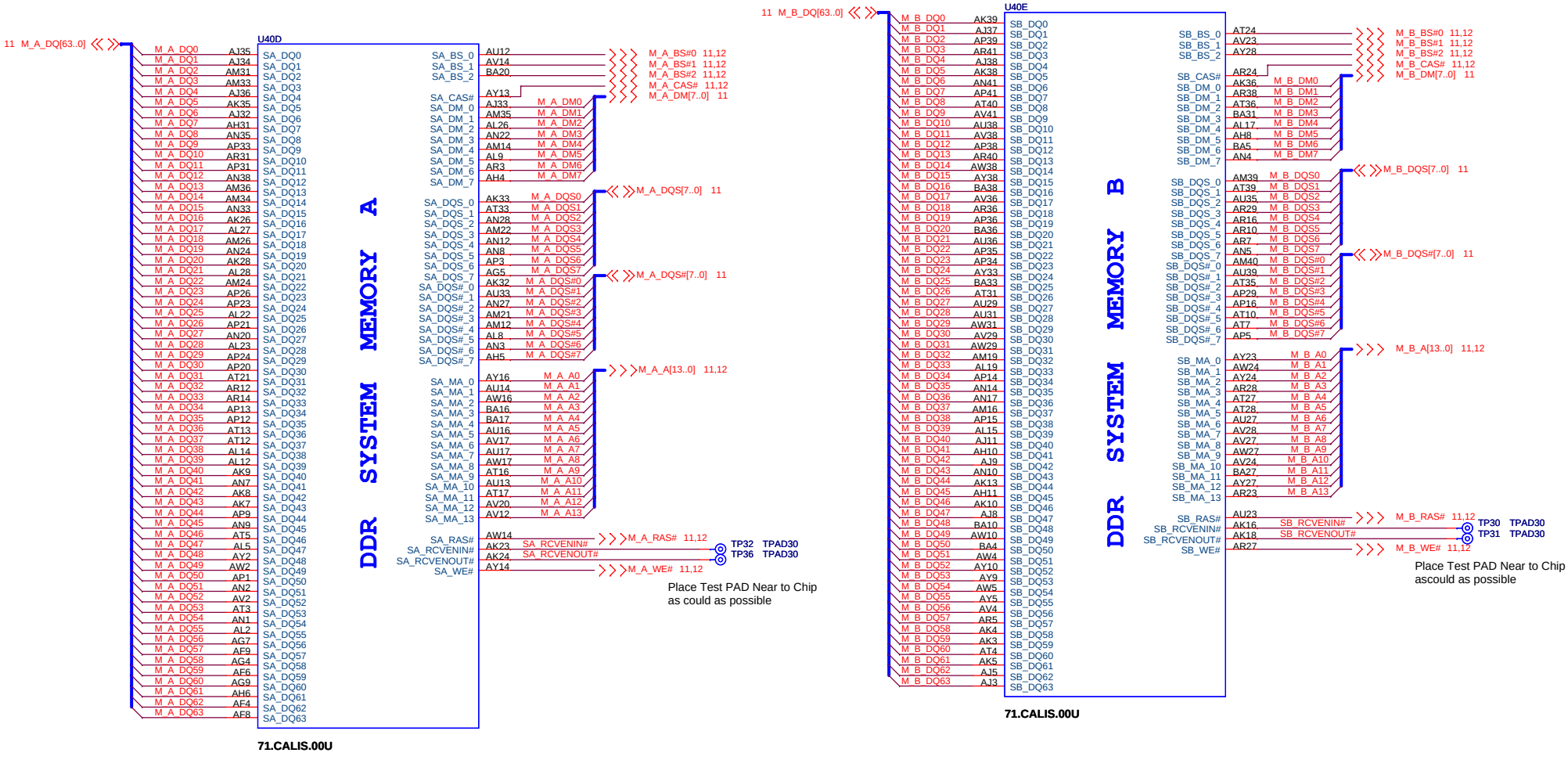
Taipei Hsien 221, Taiwan, R.O.C.
GMCH (2 of 5)
HURON
SD
Thursday, March 15, 2007
Sheet 7 of 44



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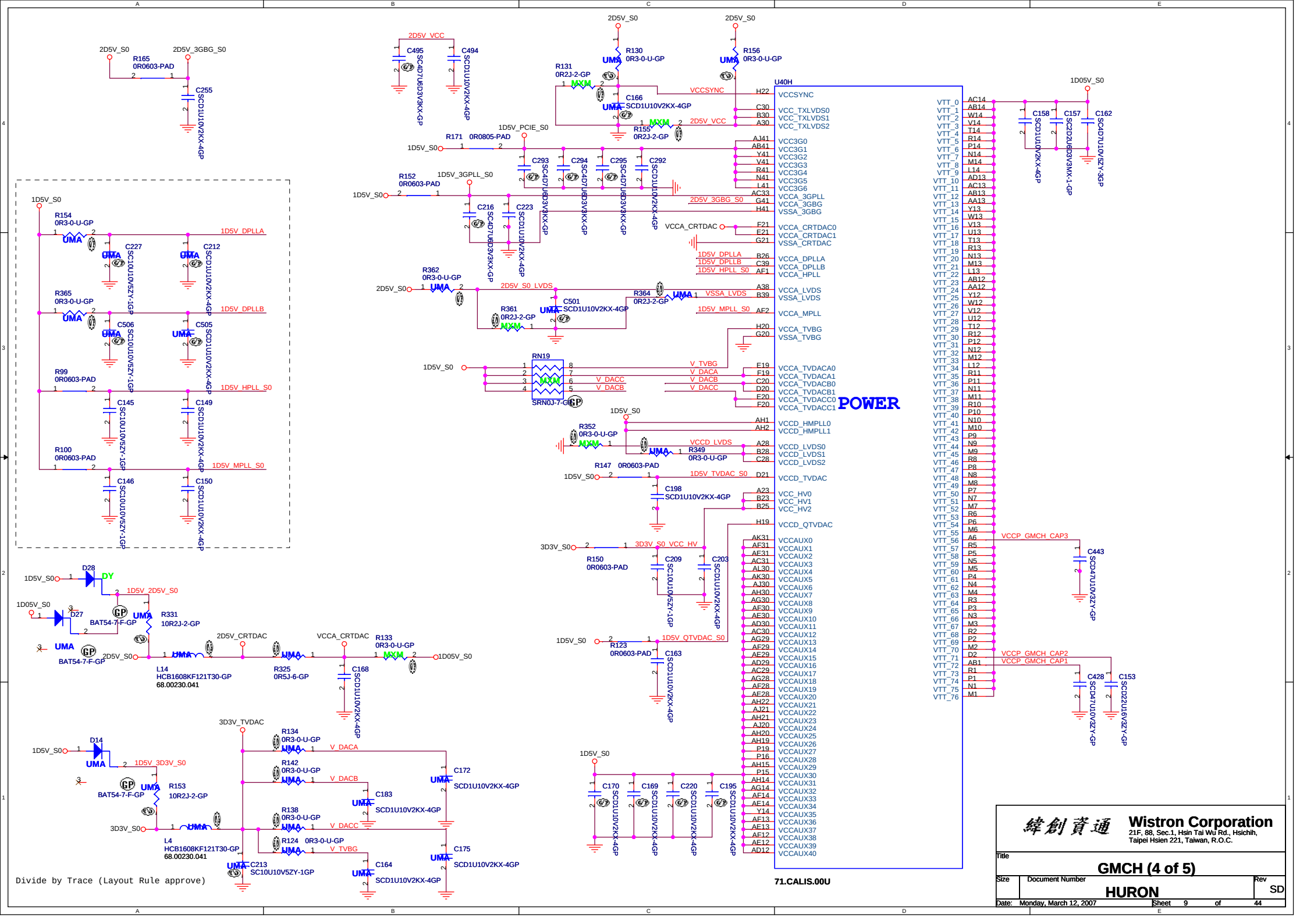
Title: **GMCH (3 of 5)**

Size	Document Number	Rev
	HURON	SD

Date: Monday, March 12, 2007 Sheet 8 of 44


POWER
U40H
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_LVDS
VSSA_LVDS
VCCA_MPLL
VCCA_TVBG
VSSA_TVBG
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
VCC_HV0
VCC_HV1
VCC_HV2
VCCD_QTVDAC
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
VCCAUX16
VCCAUX17
VCCAUX18
VCCAUX19
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VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
VTT_0
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VTT_69
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VTT_71
VTT_72
VTT_73
VTT_74
VTT_75
VTT_76
VCCP_GMCH_CAP3
VCCP_GMCH_CAP2
VCCP_GMCH_CAP1
71.CALIS.00U
Divide by Trace (Layout Rule approve)
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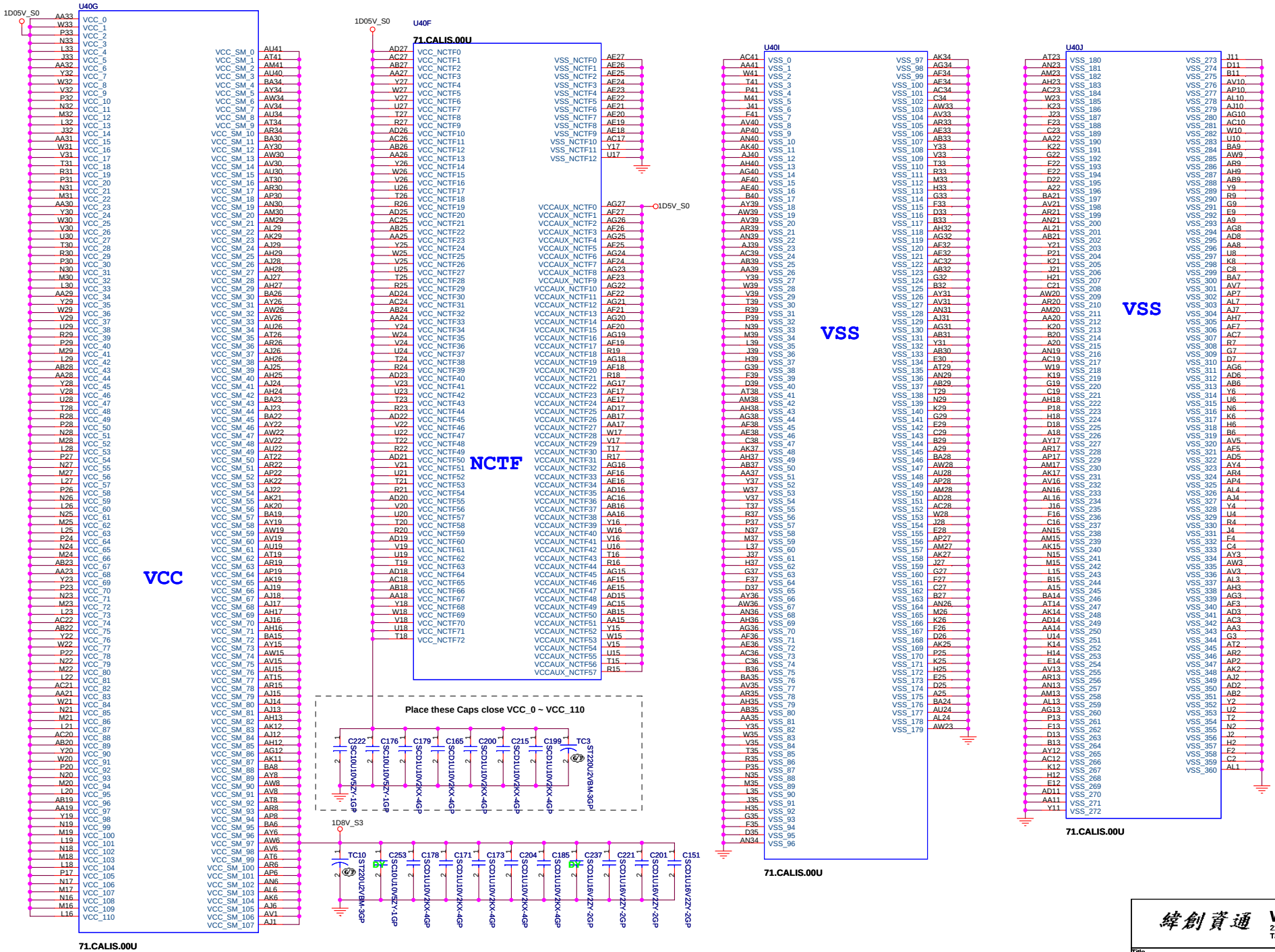
Title
GMCH (4 of 5)
Size
Document Number
HURON
Rev
SD
Date: Monday, March 12, 2007
Sheet 9 of 44



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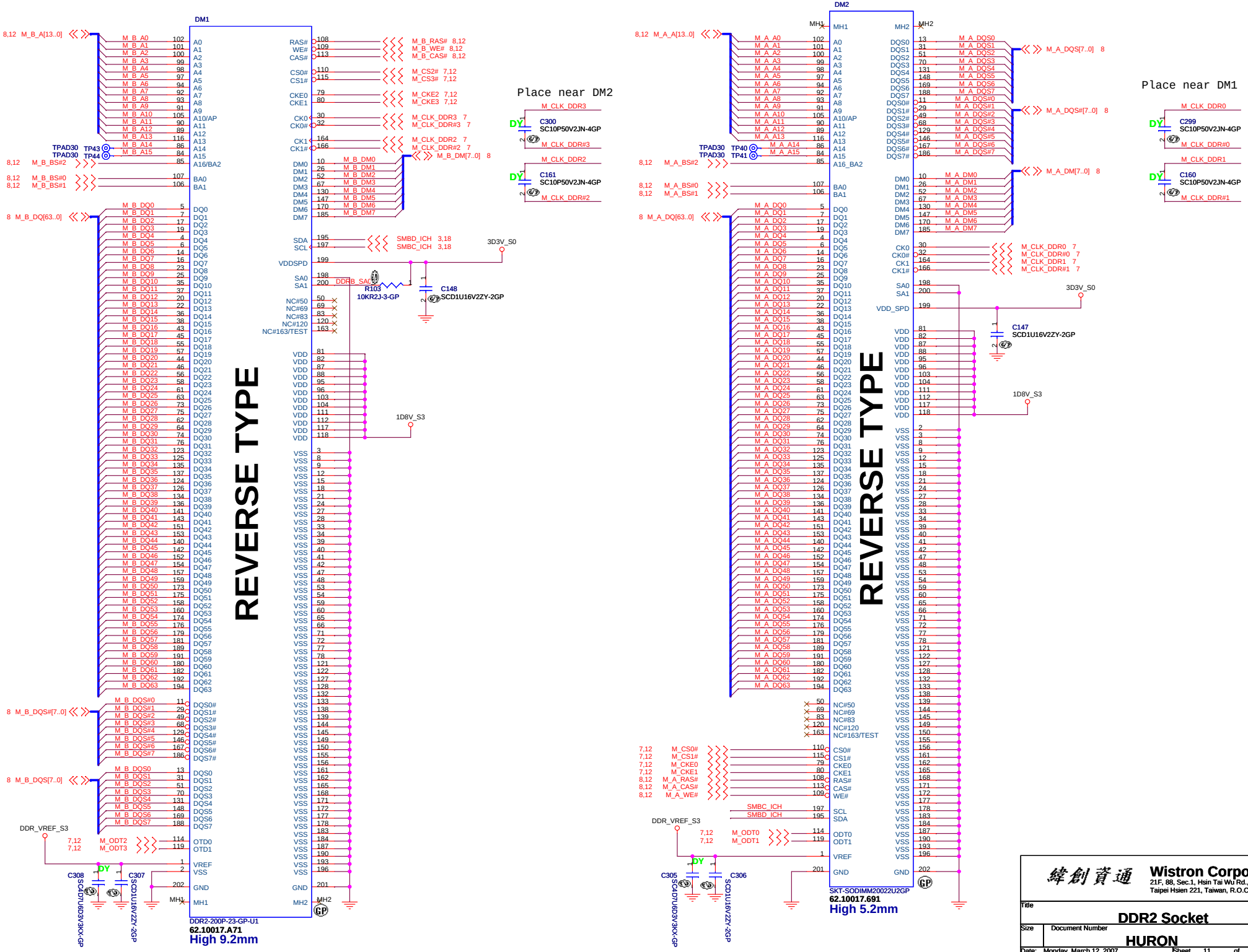
Title: GMCH (5 of 5)	
Size	Document Number: HURON
Rev: SD	
Date: Monday, March 12, 2007	Sheet 10 of 44



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Title: DDR2 Socket

Size | Document Number: HURON | Rev: SD

Date: Monday, March 12, 2007 | Sheet 11 of 44

PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

RN34 — SRN56J-5-GP
- M_A_A12
- M_CKE0 7,11
- M_A_BS#2 8,11

RN30 — SRN56J-5-GP
- M_B_A9
- M_B_A8
- M_B_A3
- M_B_A5

RN35 — SRN56J-5-GP
- M_CKE2 7,11
- M_B_BS#2 8,11
- M_B_A12

RN26 — SRN56J-5-GP
- M_B_A10
- M_B_BS#0 8,11
- M_B_A0

RN24 — SRN56J-5-GP
- M_B_A13
- M_ODT2 7,11
- M_ODT3 7,11
- M_B_RAS# 8,11

RN28 — SRN56J-5-GP
- M_B_BS#1 8,11
- M_B_A2
- M_B_A1
- M_B_A4

RN33 — SRN56J-5-GP
- M_B_A6
- M_B_A7
- M_B_A11
- M_CKE3 7,11

RN22 — SRN56J-5-GP
- M_B_CAS# 8,11
- M_CS3# 7,11
- M_B_WE# 8,11
- M_CS2# 7,11

RN23 — SRN56J-5-GP
- M_A_A13
- M_ODT0 7,11
- M_CS0# 7,11
- M_A_RAS# 8,11

RN27 — SRN56J-5-GP
- M_A_BS#1 8,11
- M_A_A0
- M_A_A2
- M_A_A4

RN20 — SRN56J-5-GP
- M_A_CAS# 8,11
- M_CS1# 7,11
- M_ODT1 7,11

RN29 — SRN56J-5-GP
- M_A_A9
- M_A_A8
- M_A_A5
- M_A_A1

RN32 — SRN56J-5-GP
- M_A_A6
- M_A_A7
- M_A_A11
- M_CKE1 7,11

RN25 — SRN56J-5-GP
- M_A_A3
- M_A_A10
- M_A_WE# 8,11
- M_A_BS#0 8,11

M_A_A[13..0] ⟷ M_A_A[13..0] 8,11

M_B_A[13..0] ⟷ M_B_A[13..0] 8,11

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

C190 C174 C243 C235 C214 C191 C236 C238 C188 C245 C205 — SCD1U16V2ZY-2GP (DY)

C233 C226 C249 C244 C187 C232 C234 C206 C182 C218 C197 — SCD1U16V2ZY-2GP (DY)

Place these Caps near DM1

1D8V_S3

C177 C207 C242 C239 C180 — SC2D2U6D3V3MX-1-GP

C189 C219 C194 C228 — SCD1U16V2ZY-2GP (DY)

Place these Caps near DM2

1D8V_S3

C181 C184 C241 C240 C250 — SC2D2U6D3V3MX-1-GP

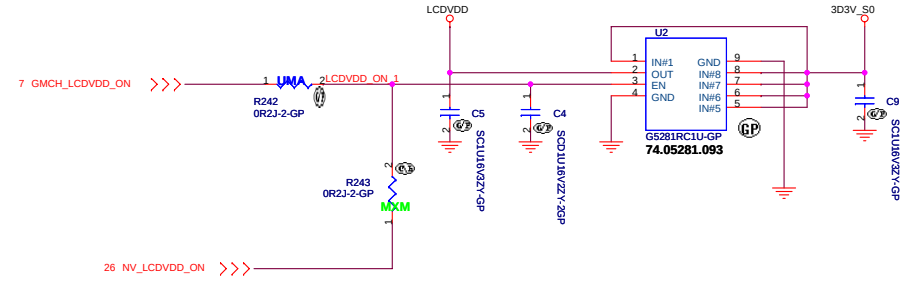
C231 C217 C208 C192 — SCD1U16V2ZY-2GP (DY)

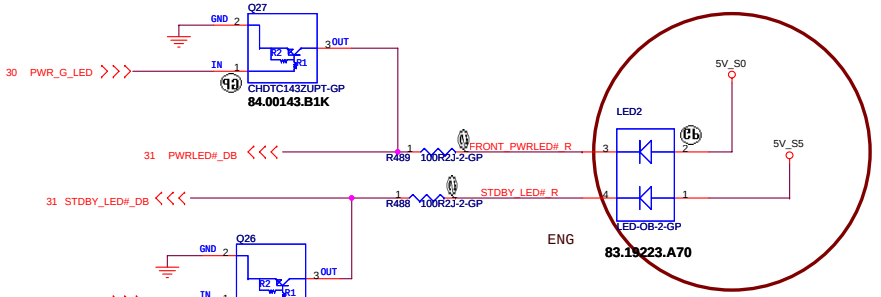
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

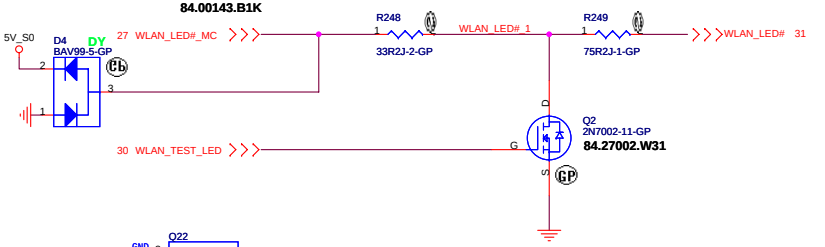
Title: **DDR2 Termination Resistor**

Size | Document Number: **HURON** | Rev: SD

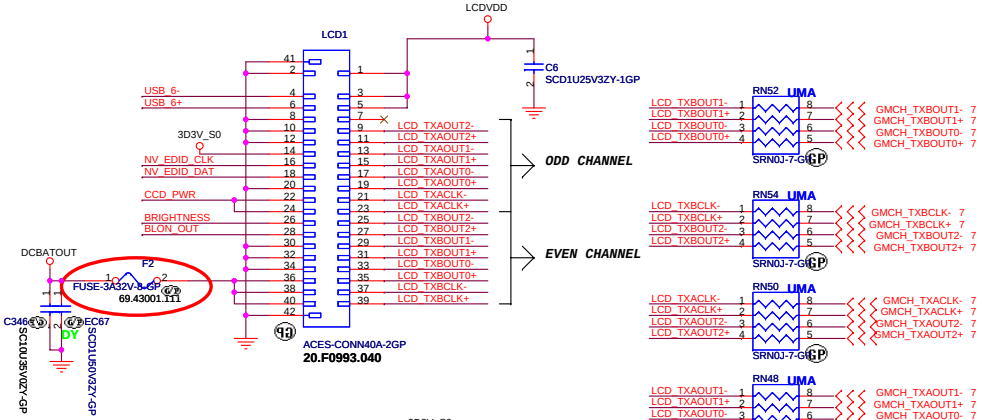
Date: Monday, March 12, 2007 | Sheet 12 of 44

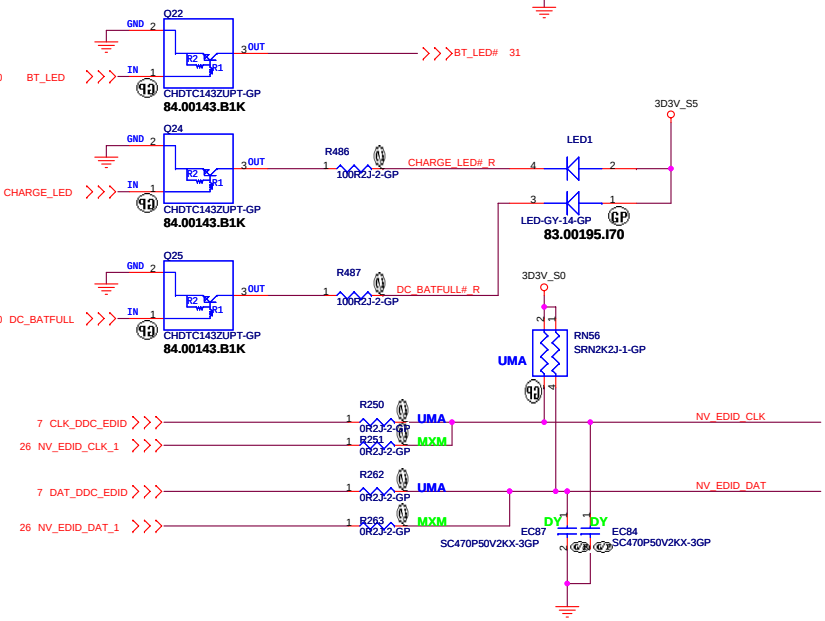


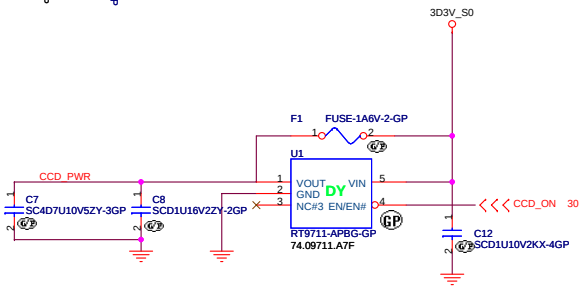


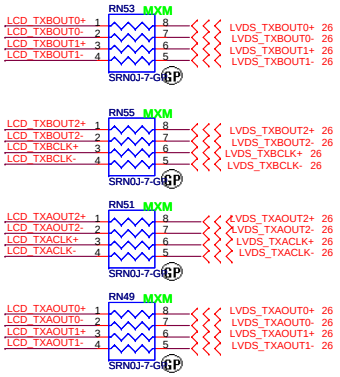


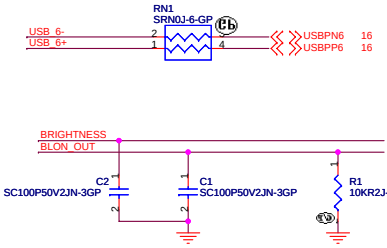
LCD/INVERTER CONN

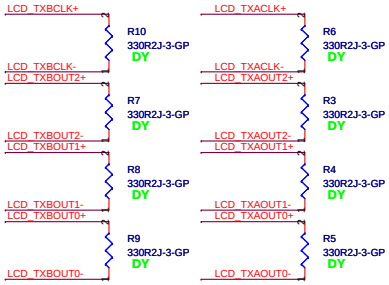












<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD CONN & LED**

Size	Document Number	Rev
	HURON	SD

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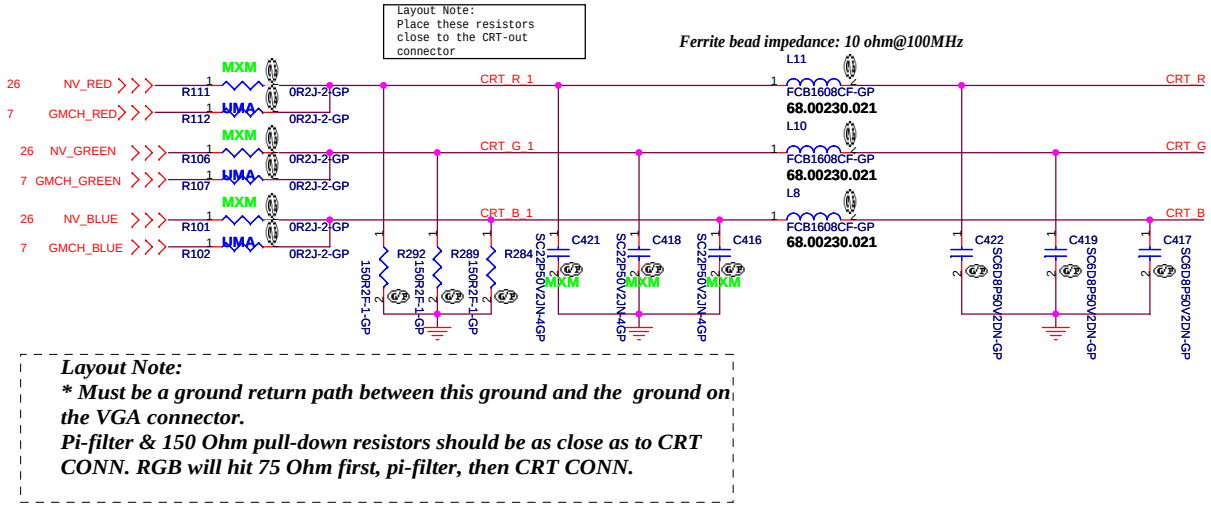
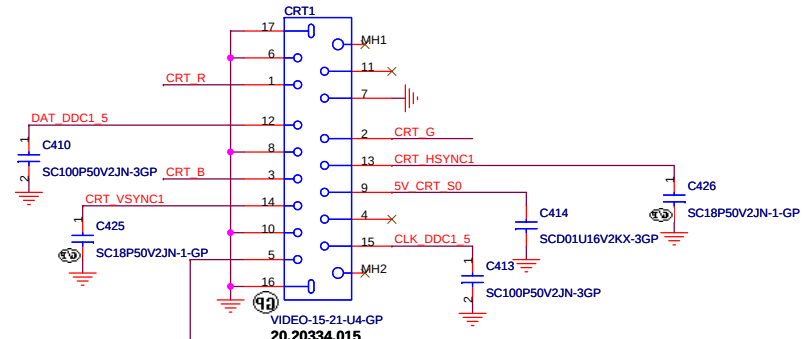
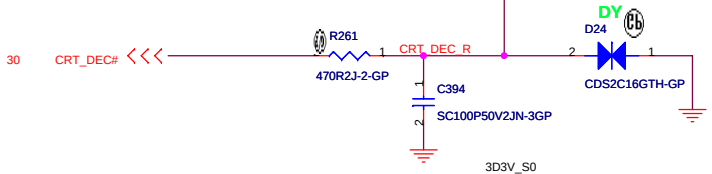
CRT I/F & CONNECTOR

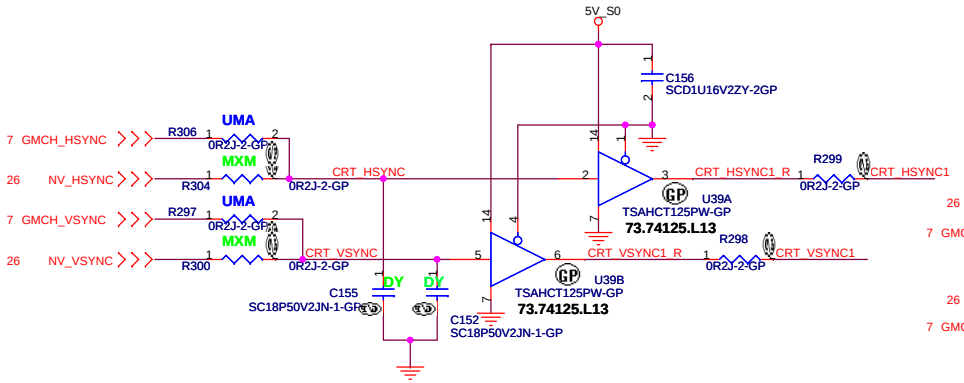


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

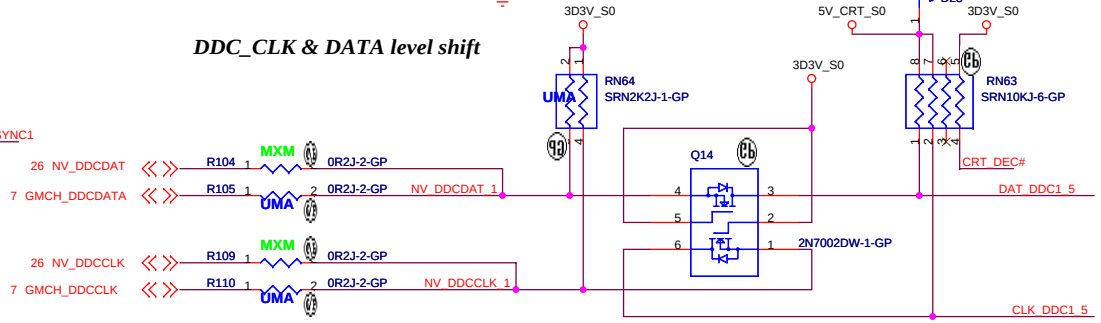




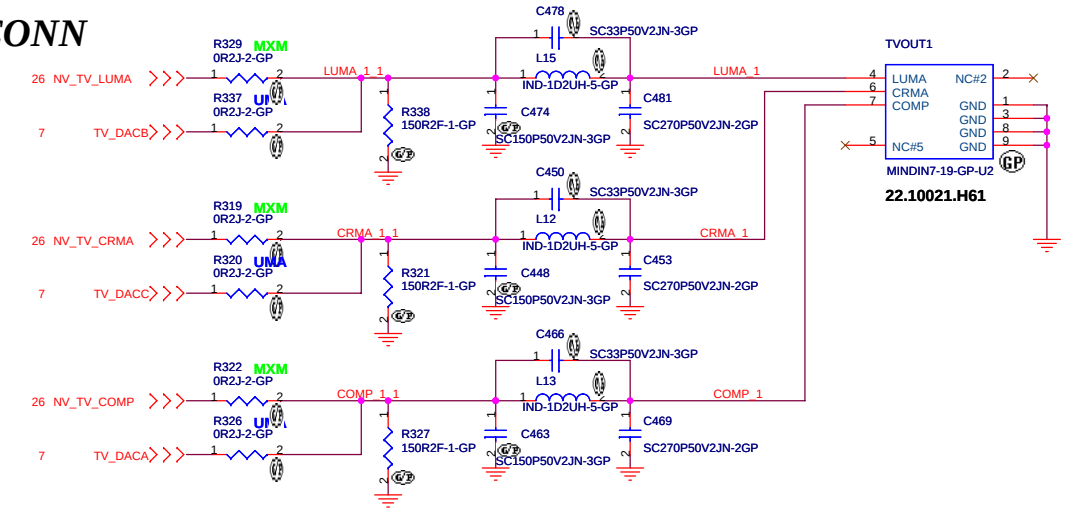
Hsync & Vsync level shift



DDC_CLK & DATA level shift



TV CONN



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Title: **CRT/TV Connector**

Size | Document Number: **HURON** | Rev: SD

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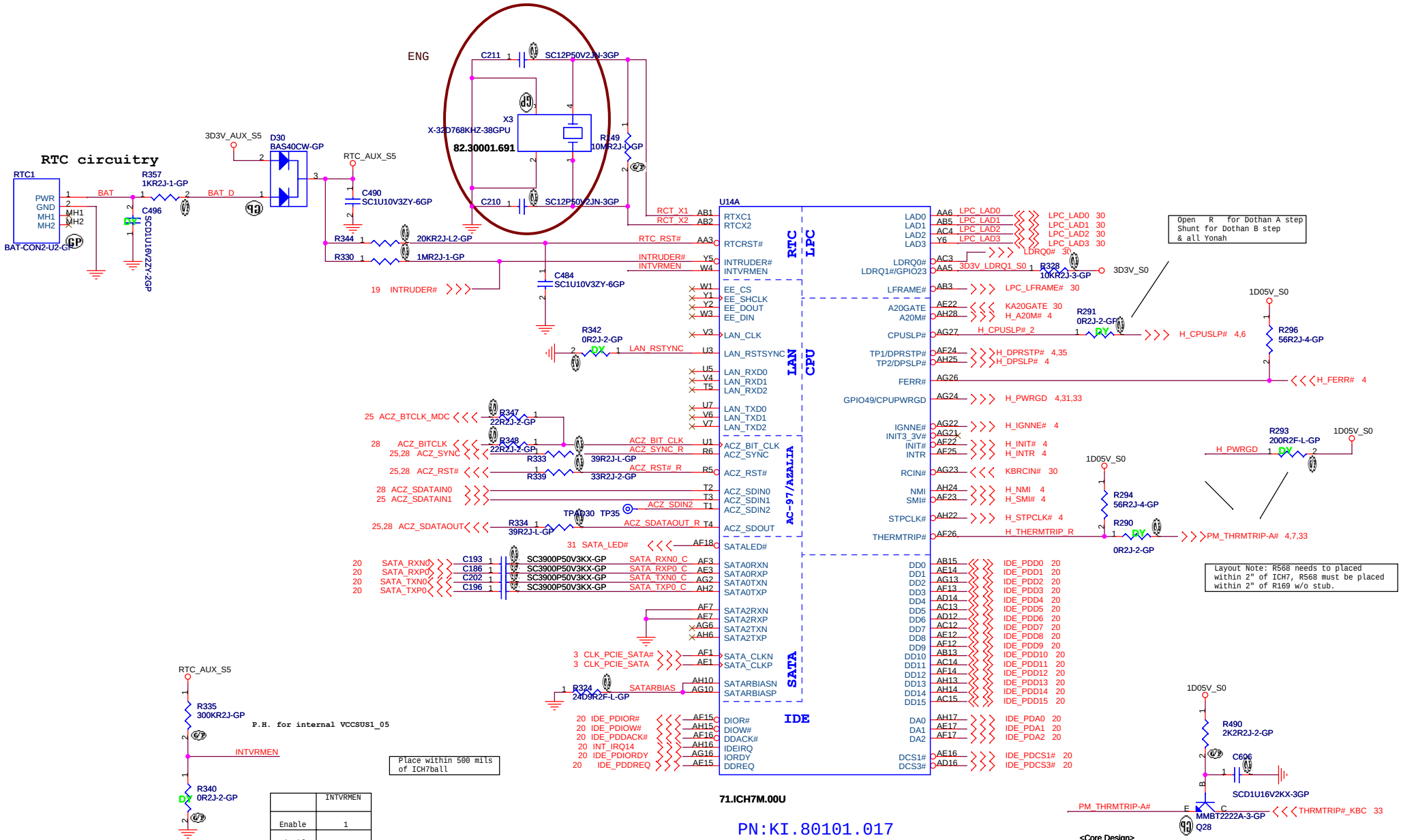
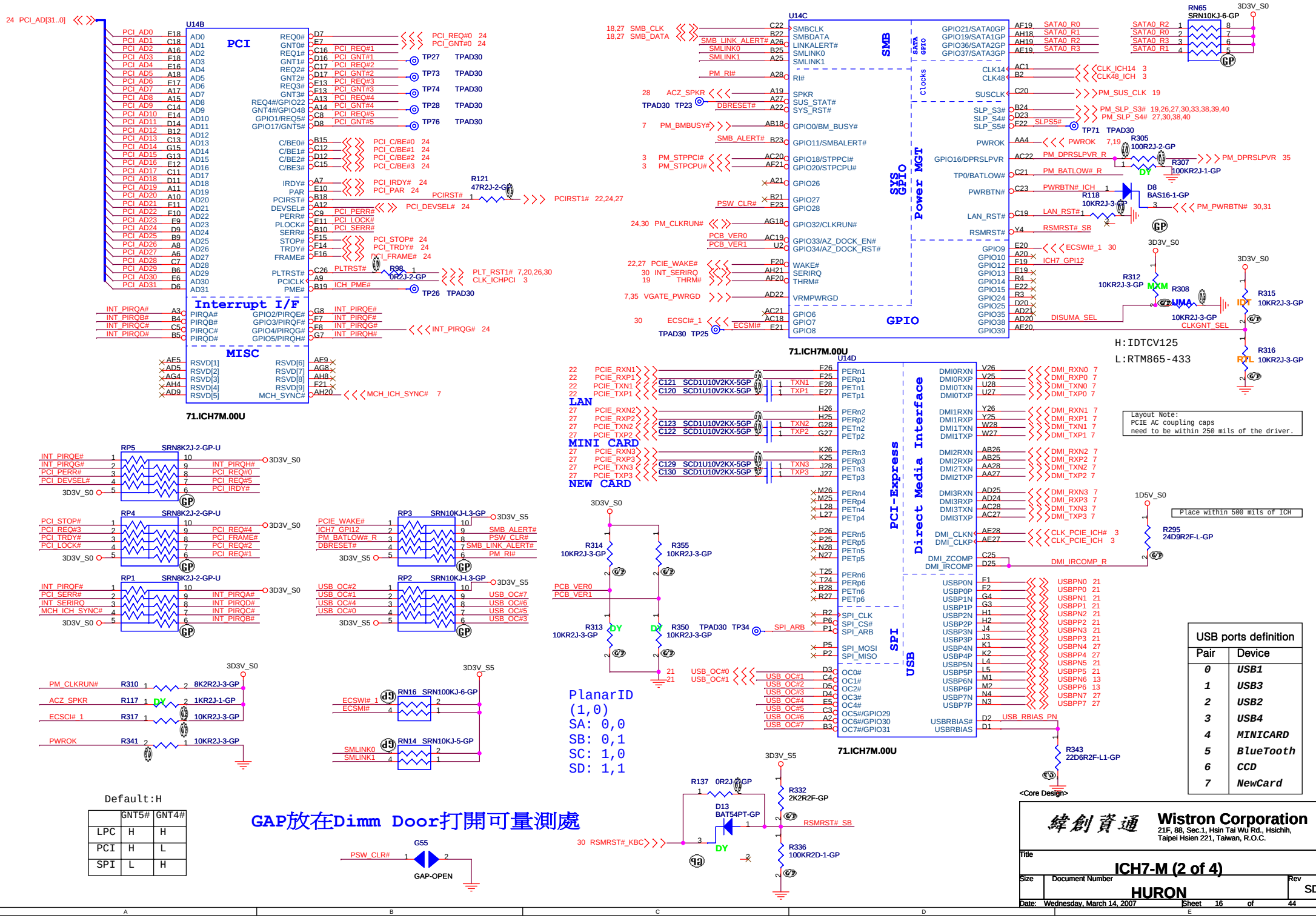

RTC circuitry
ENG
RTC1
BAT-CON2-U2-GP
R357 1KR2J-1-GP
C496 SCD1U16V2ZY-2GP
D30 BAS40CW-GP
3D3V_AUX_S5
RTC_AUX_S5
C490 SC1U10V3ZY-6GP
C211 SC12P50V2JN-3GP
C210 SC12P50V2JN-3GP
X3 X-32D768KHZ-38GPU
82.30001.691
R149 10MR2J-L-GP
R344 20KR2J-L2-GP
R330 1MR2J-1-GP
C484 SC1U10V3ZY-6GP
R342 0R2J-2-GP
U14A
RTC
LPC
LAN
CPU
AC-97/AZALIA
IDE
SATA
RTCRST#
INTRUDER#
INTVRMEN
EE_CS
EE_SHCLK
EE_DOUT
EE_DIN
LAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
ACZ_BIT_CLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDOUT
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIASN
SATARBIASP
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
LAD0
LAD1
LAD2
LAD3
LDRQ0#
LDRQ1#/GPIO23
LFRAME#
A20GATE
A20M#
CPUSLP#
TP1/DPRSTP#
TP2/DPSLP#
FERR#
GPIO49/CPUPWRGD
IGNNE#
INIT3_3V#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THERMTRIP#
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
R328 10KR2J-3-GP
R291 0R2J-2-GP
R296 56R2J-4-GP
R293 200R2F-L-GP
R294 56R2J-4-GP
R290 0R2J-2-GP
R347 22R2J-2-GP
R348 22R2J-2-GP
R333 39R2J-L-GP
R339 33R2J-2-GP
R334 39R2J-L-GP
TP0930
TP35
C193 SC3900P50V3KX-GP
C186 SC3900P50V3KX-GP
C202 SC3900P50V3KX-GP
C196 SC3900P50V3KX-GP
R324 24D9R2F-L-GP
R335 300KR2J-GP
R340 0R2J-2-GP
R490 2K2R2J-2-GP
C606 SCD1U16V2KX-3GP
MMBT2222A-3-GP
Q28
P.H. for internal VCCSUS1_05
Place within 500 mils of ICH7ball
Open R for Dothan A step
Shunt for Dothan B step
& all Yonah
Layout Note: R568 needs to placed within 2" of ICH7, R568 must be placed within 2" of R169 w/o stub.
Placement Note:
Diatance between the ICH-7 M and cap on the "P" signal should be identical distance between the ICH-7 M and cap on the "N" signal for same pair.
INTVRMEN
Enable 1
Disable 0
71.ICH7M.00U
PN:KI.80101.017
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (1 of 4)
Size
Document Number
HURON
Rev
SD
Date: Monday, March 12, 2007
Sheet 15 of 44


U14B
PCI
Interrupt I/F
MISC
71.ICH7M.00U
U14C
SMB
SYS GPIO
Power MGT
GPIO
71.ICH7M.00U
U14D
LAN
MINI CARD
NEW CARD
PCI-Express
Direct Media Interface
SPI
USB
71.ICH7M.00U
H:IDTCV125
L:RTM865-433
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
USB ports definition
Pair | Device
0 USB1
1 USB3
2 USB2
3 USB4
4 MINICARD
5 BlueTooth
6 CCD
7 NewCard
PlanarID
(1,0)
SA: 0,0
SB: 0,1
SC: 1,0
SD: 1,1
Default:H
GNT5# GNT4#
LPC H H
PCI H L
SPI L H
GAP放在Dimm Door打開可量測處
GAP-OPEN
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (2 of 4)
Size
Document Number
HURON
Rev
SD
Date: Wednesday, March 14, 2007
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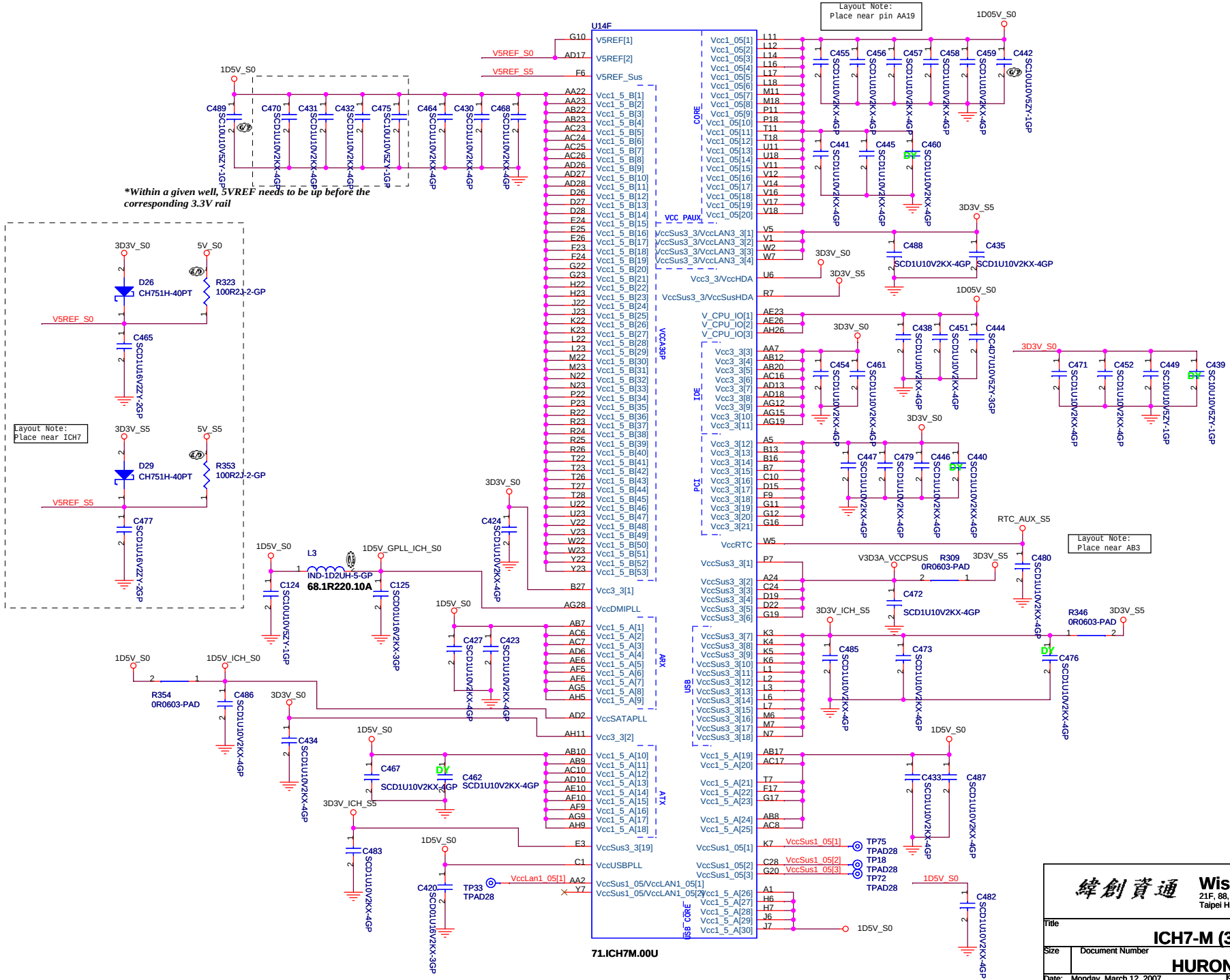
U14F
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near pin AA19
Layout Note: Place near ICH7
Layout Note: Place near AB3
71.ICH7M.00U
Wistron Corporation
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Title
ICH7-M (3 of 4)
Size
Document Number
HURON
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SD
Date: Monday, March 12, 2007
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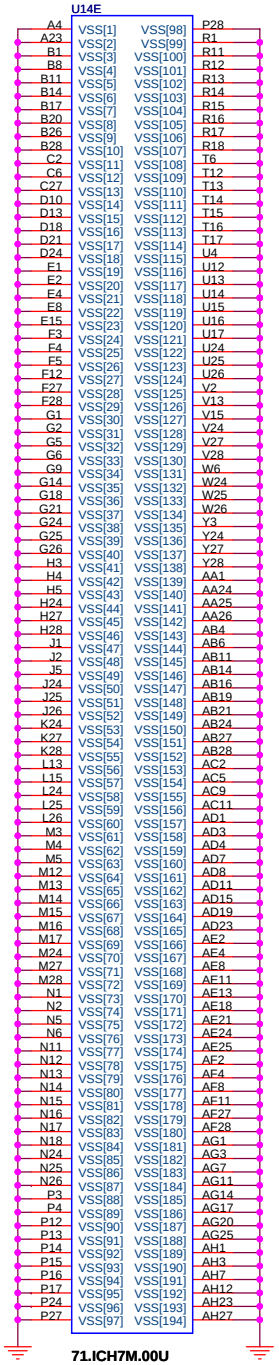

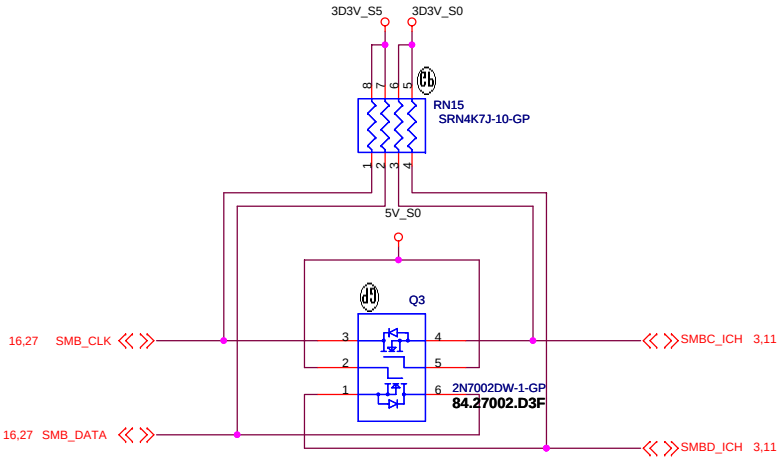

Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH7-M (4 of 4)**

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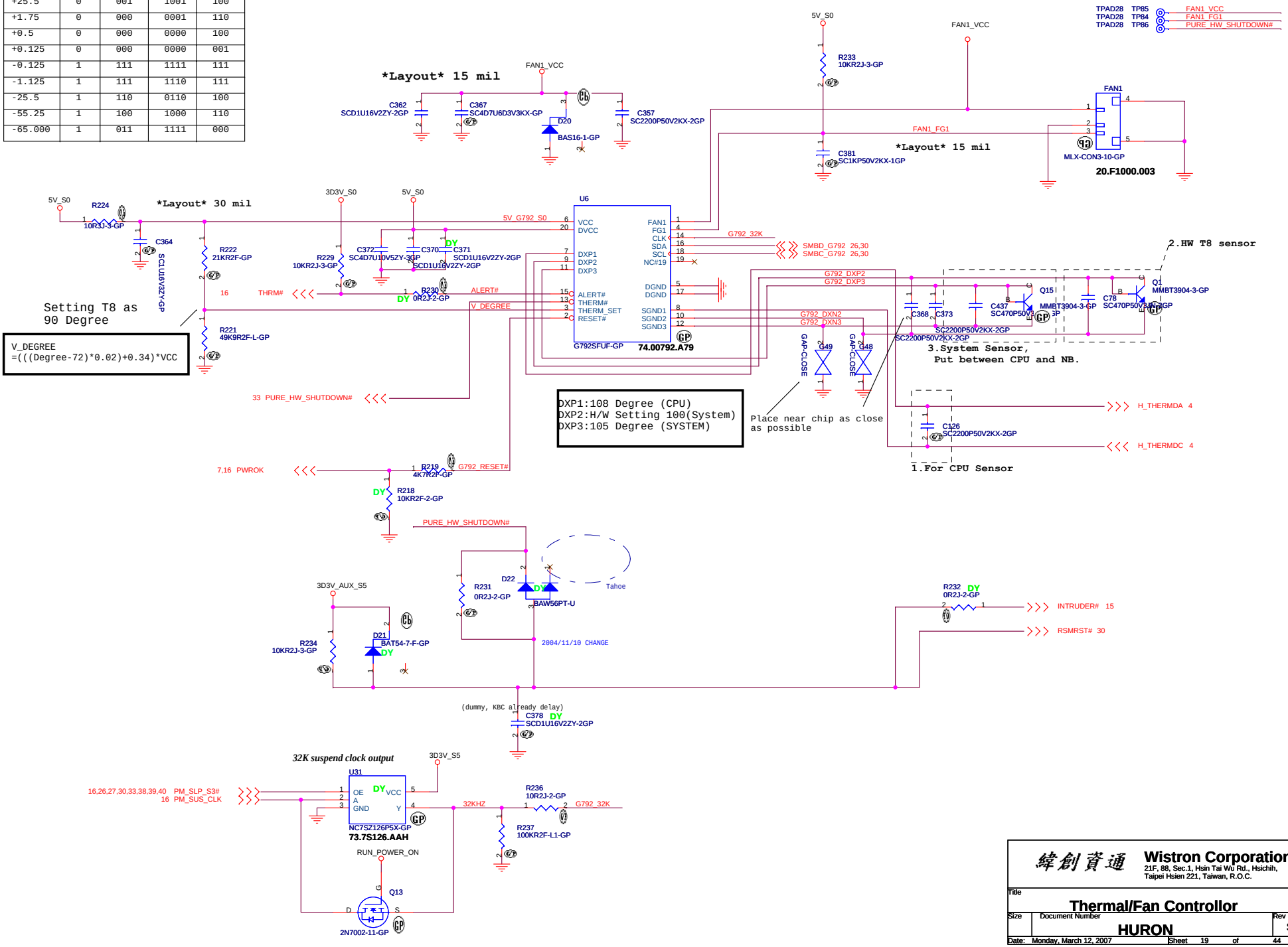
TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



緯創資通 **Wistron Corporation**
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Title: **Thermal/Fan Controllor**

Size	Document Number	Rev
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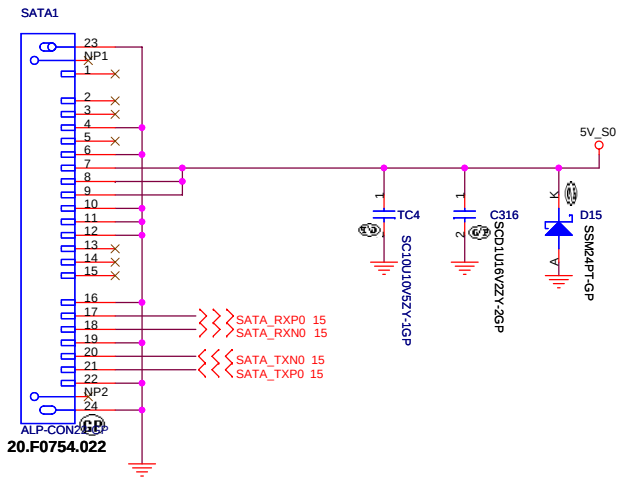
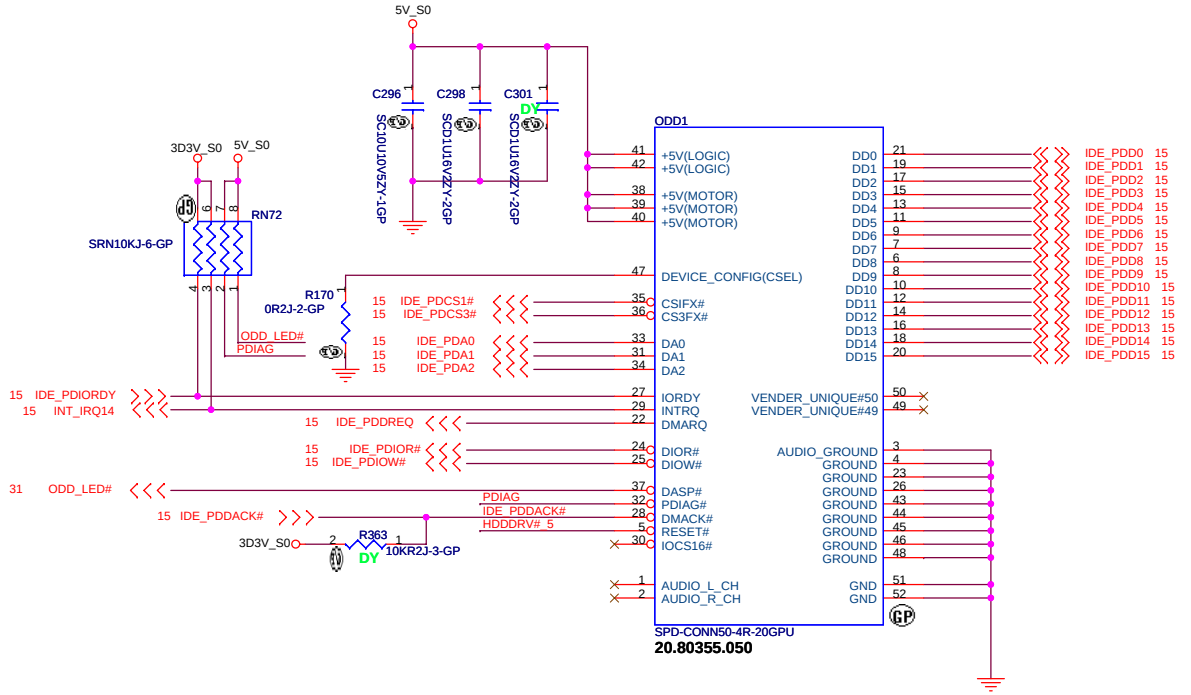
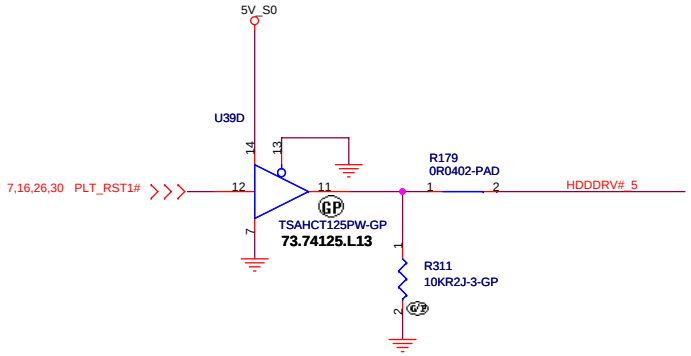
SATA HD Connector



ODD Connector





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD and CDROM

Size	Document Number	Rev
	HURON	SD

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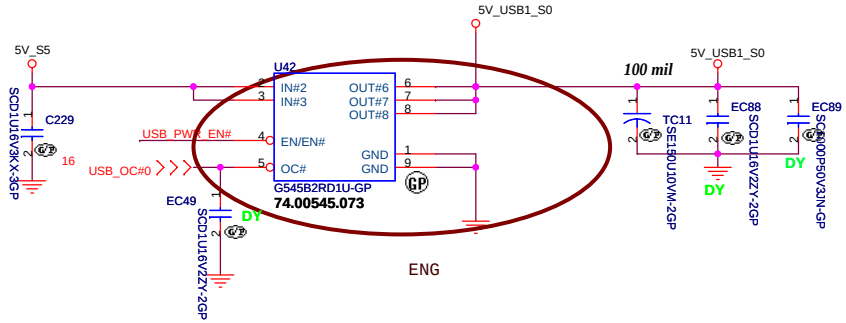
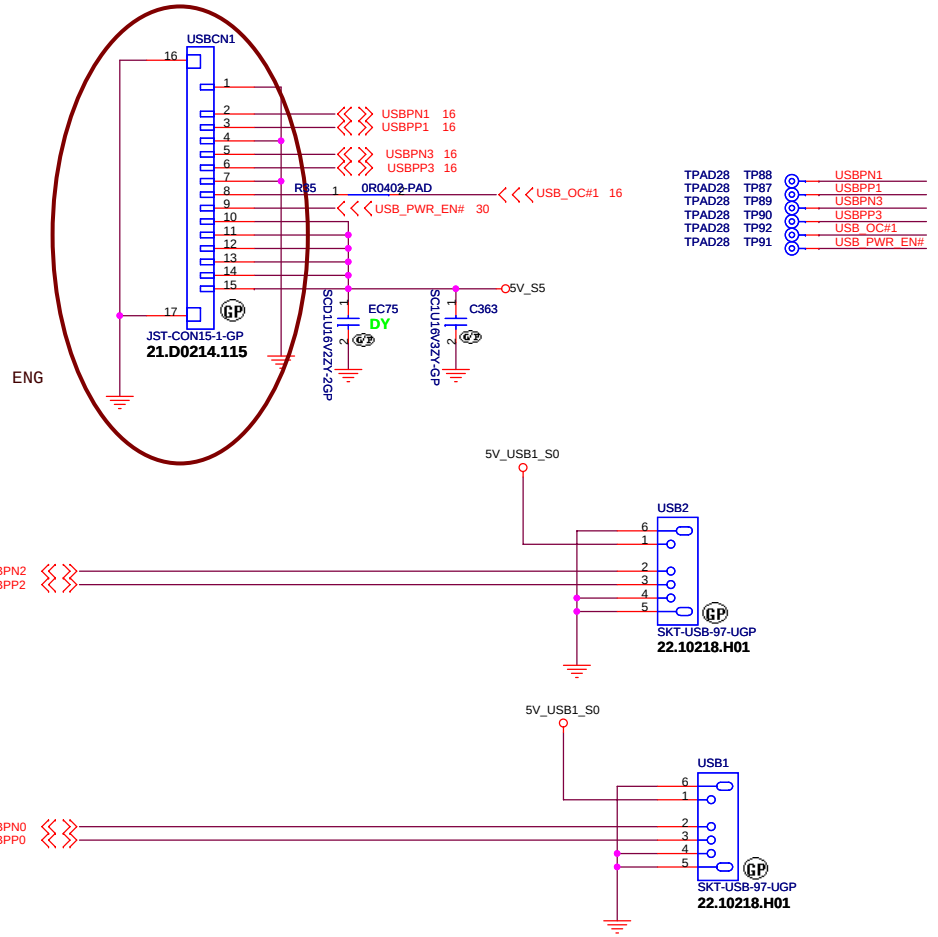
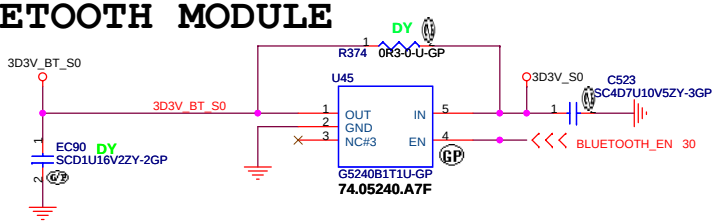
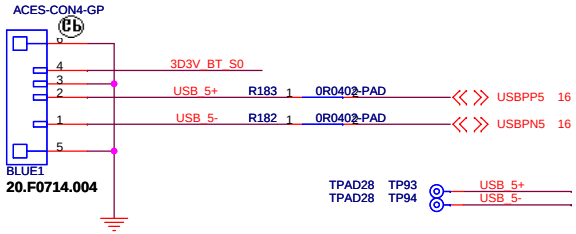




BLUETOOTH MODULE

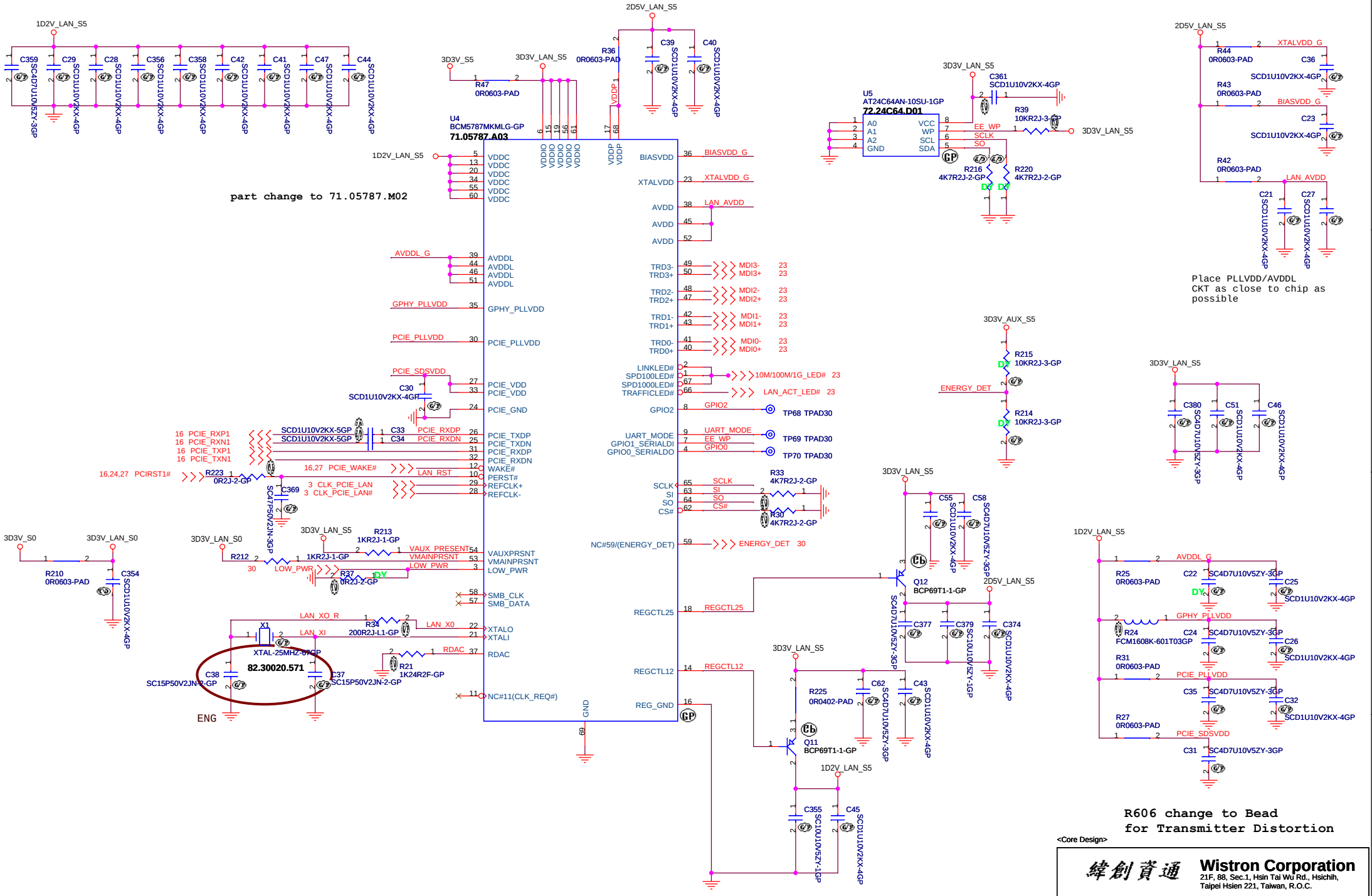


EC21 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB / BLUETOOTH		
Size	Document Number: HURON	Rev: SD
Date: Tuesday, March 13, 2007	Sheet 21 of 44	


part change to 71.05787.M02
U4
BCM5787MKMLG-GP
71.05787.A03
U5
AT24C64AN-10SU-1GP
72.24C64.D01
82.30020.571
ENG
Place PLLVDD/AVDDL
CKT as close to chip as
possible
R606 change to Bead
for Transmitter Distortion
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN BCM5787
Size
A3
Document Number
HURON
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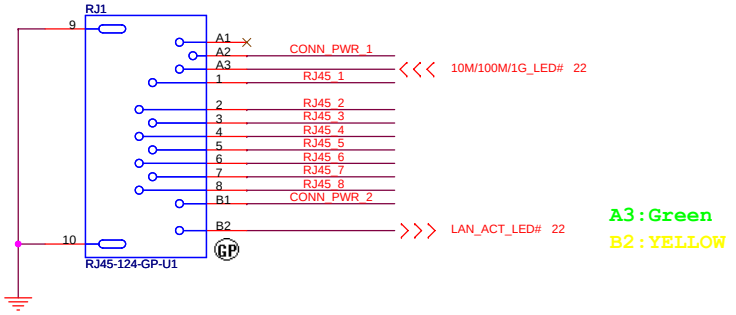
LAN Connector

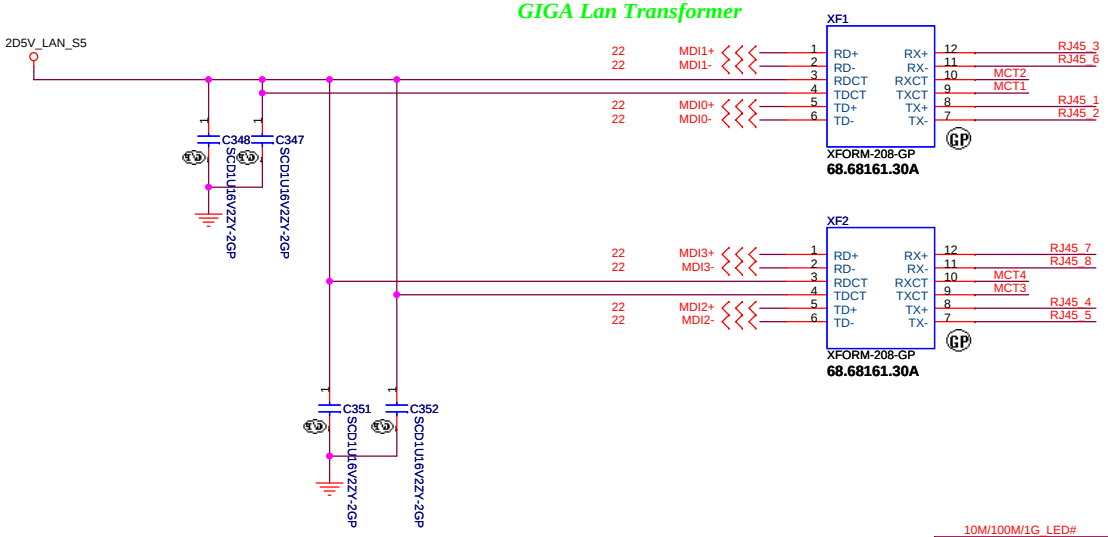
Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.

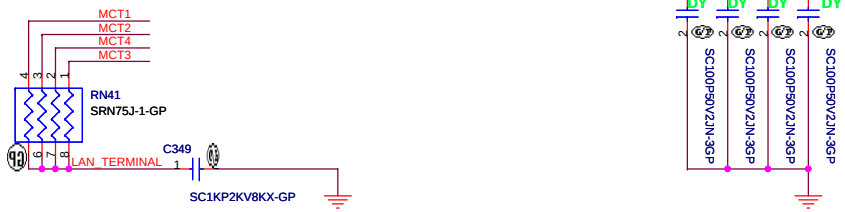
GIGA Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

<Core Design>

緯創資通 Wistron Corporation
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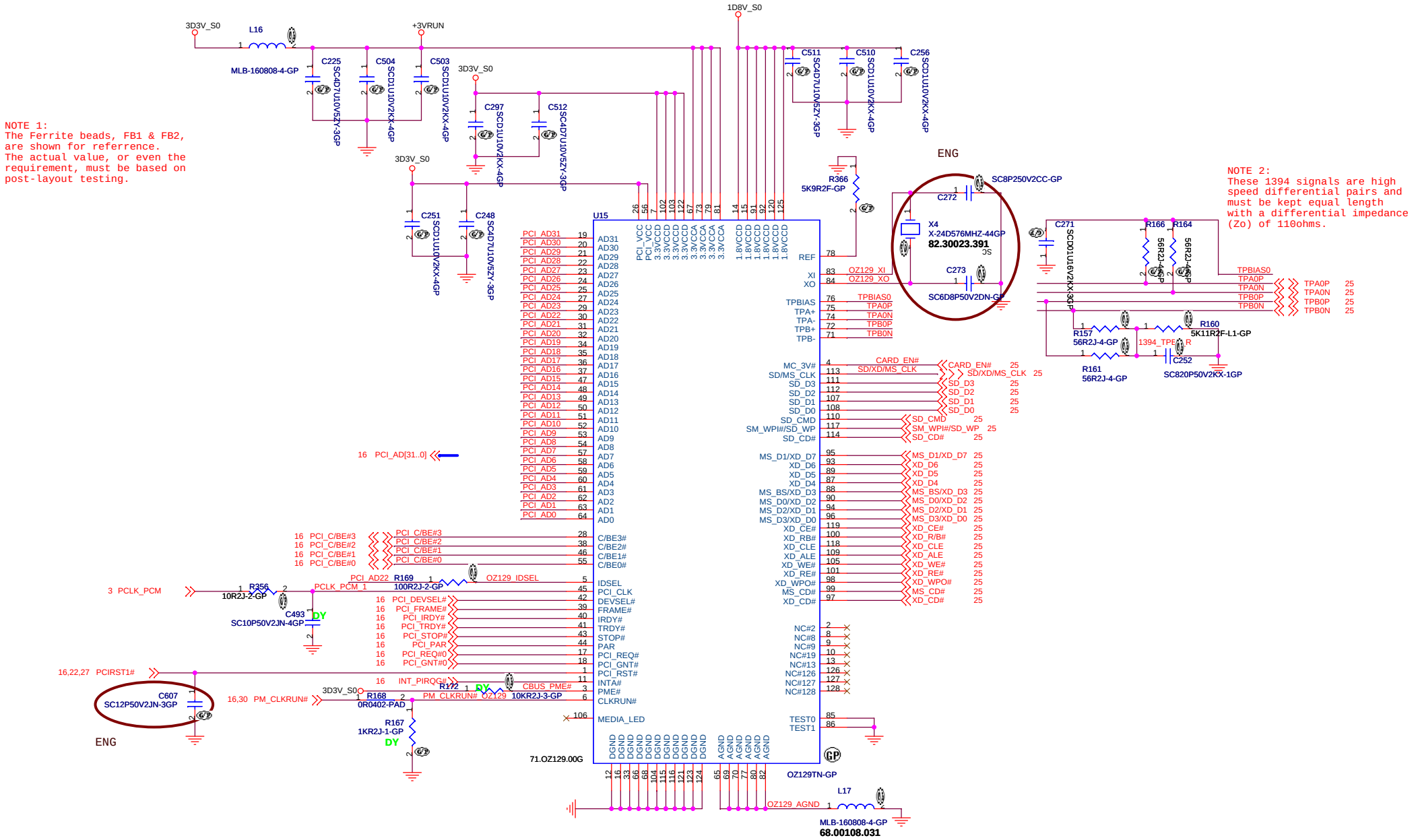
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector
Size: A3 | Document Number: HURON | Rev: SD
Date: Monday, March 19, 2007 | Sheet 23 of 44



<Core Design>
緯創資通
Wistron Corporation
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Title: OZ129T

Size | Document Number: HURON | Rev: SD

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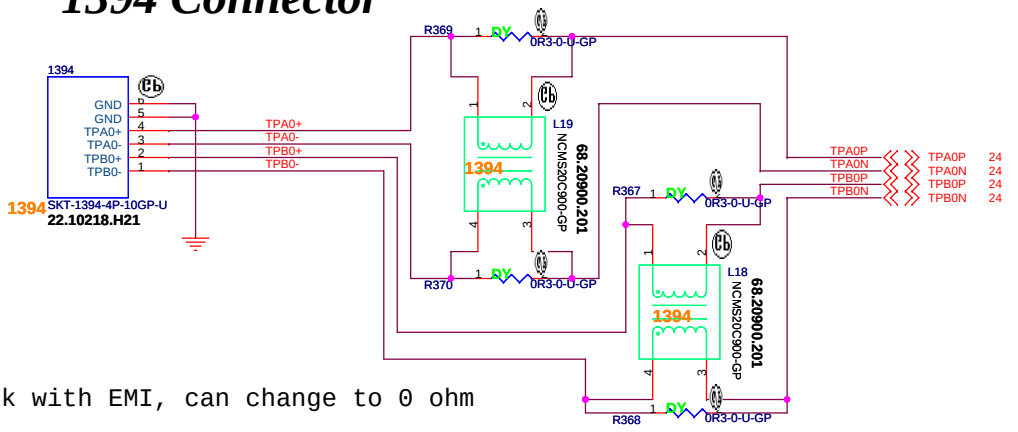
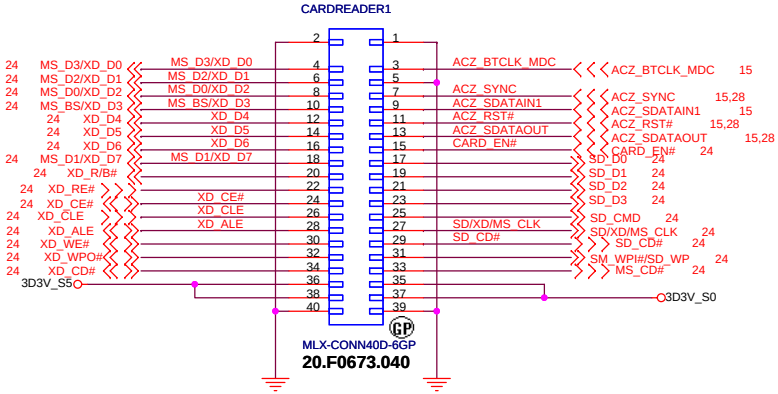
1394 Connector



check with EMI, can change to 0 ohm



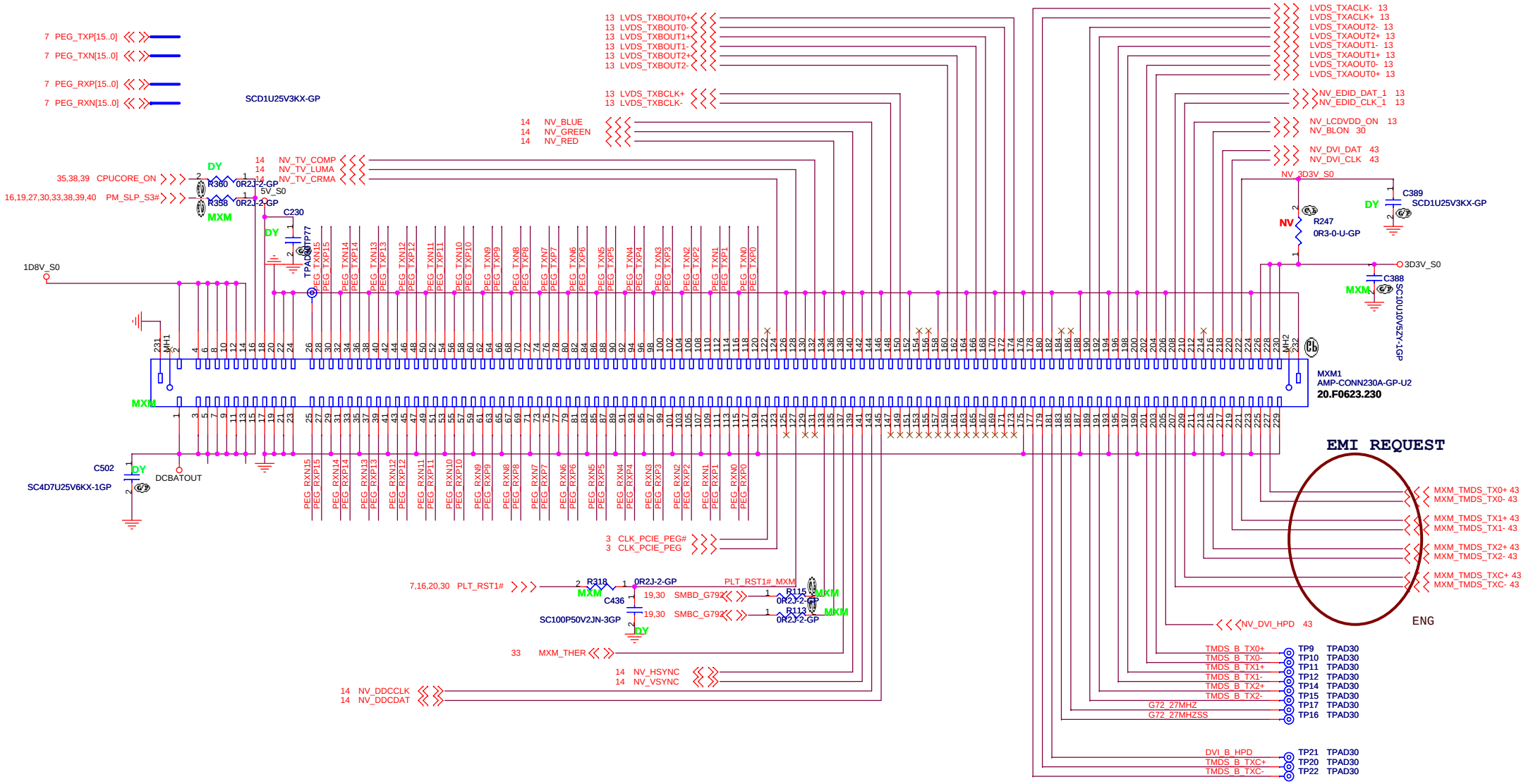
CONN on Bottom side

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**1394 / CARD READER BD**
Size	Document Number: **HURON** — Rev: SD
Date: Tuesday, March 13, 2007	Sheet 25 of 44

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector



<Core Design>

緯創資通 Wistron Corporation
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Title: Graphic MXM CONN

Size	Document Number	Rev
A3	HURON	SD

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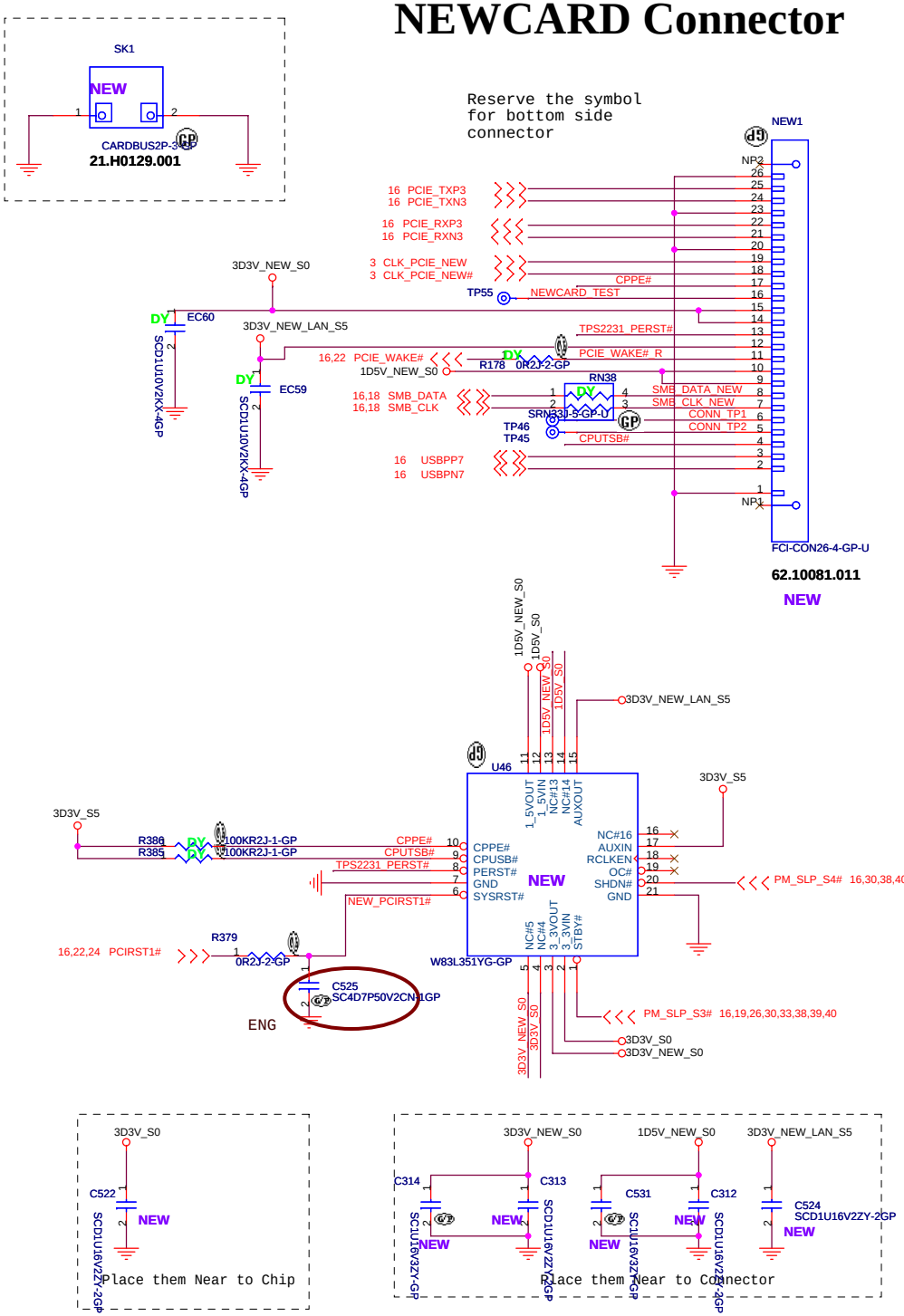
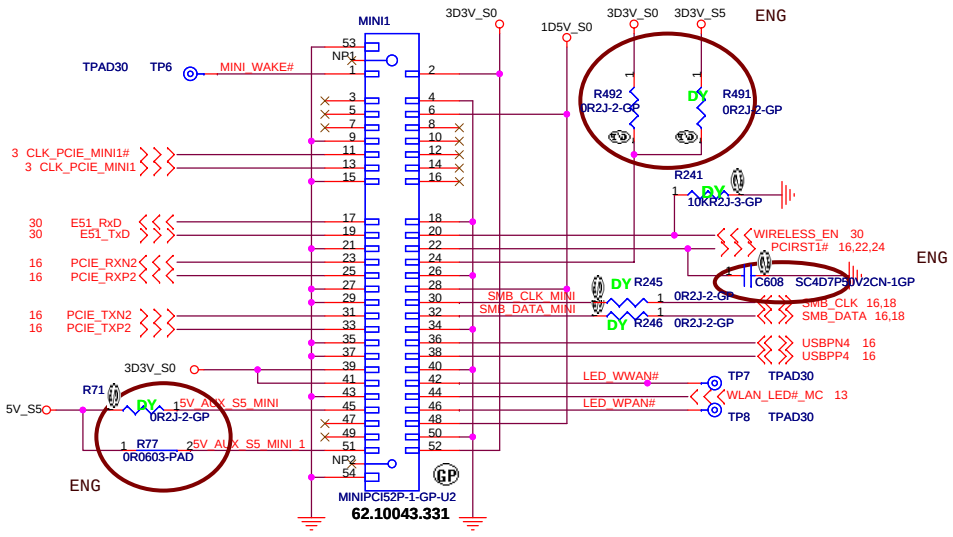
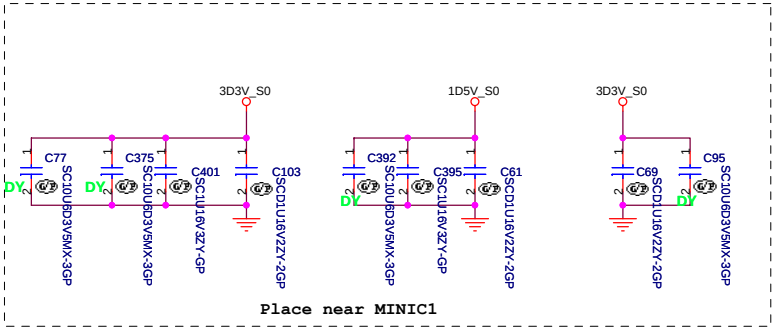
NEWCARD Connector



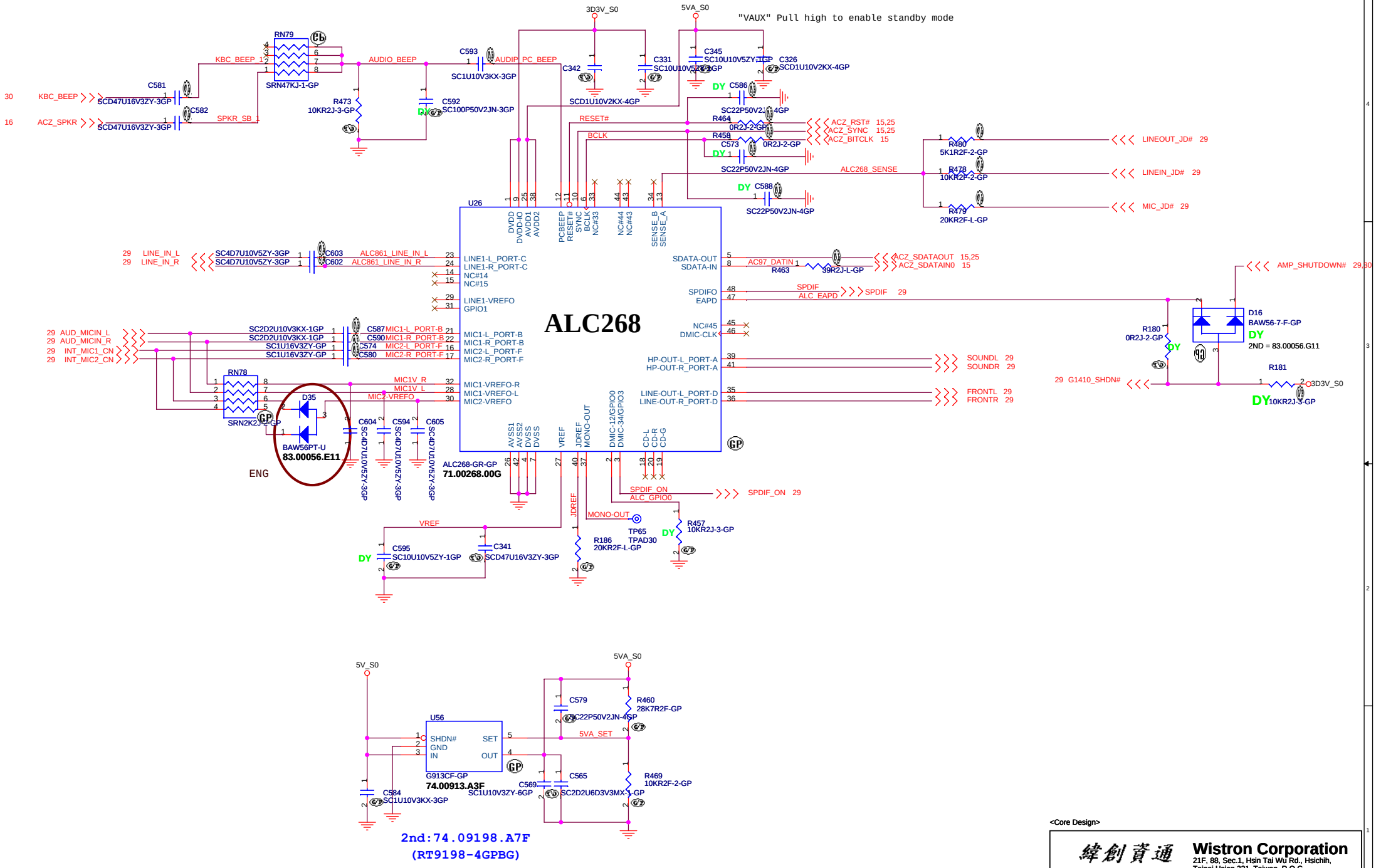
Mini Card Connector





<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD / NEW CARD		
Size	Document Number: HUR0N	Rev: SD
Date: Wednesday, March 14, 2007	Sheet 27 of 44	


"VAUX" Pull high to enable standby mode
ALC268
U26
ALC268-GR-GP
71.00268.00G
RN79
SRN47KJ-1-GP
RN78
SRN2K2J-1-GP
D35
BAW56PT-U
83.00056.E11
ENG
U56
G913CF-GP
74.00913.A3F
2nd:74.09198.A7F
(RT9198-4GPBG)
D16
BAW56-7-F-GP
2ND = 83.00056.G11
<Core Design>
Wistron Corporation
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Title
AZALIA CODEC - ALC268
Size
Document Number
HURON
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SD
Date: Wednesday, March 14, 2007
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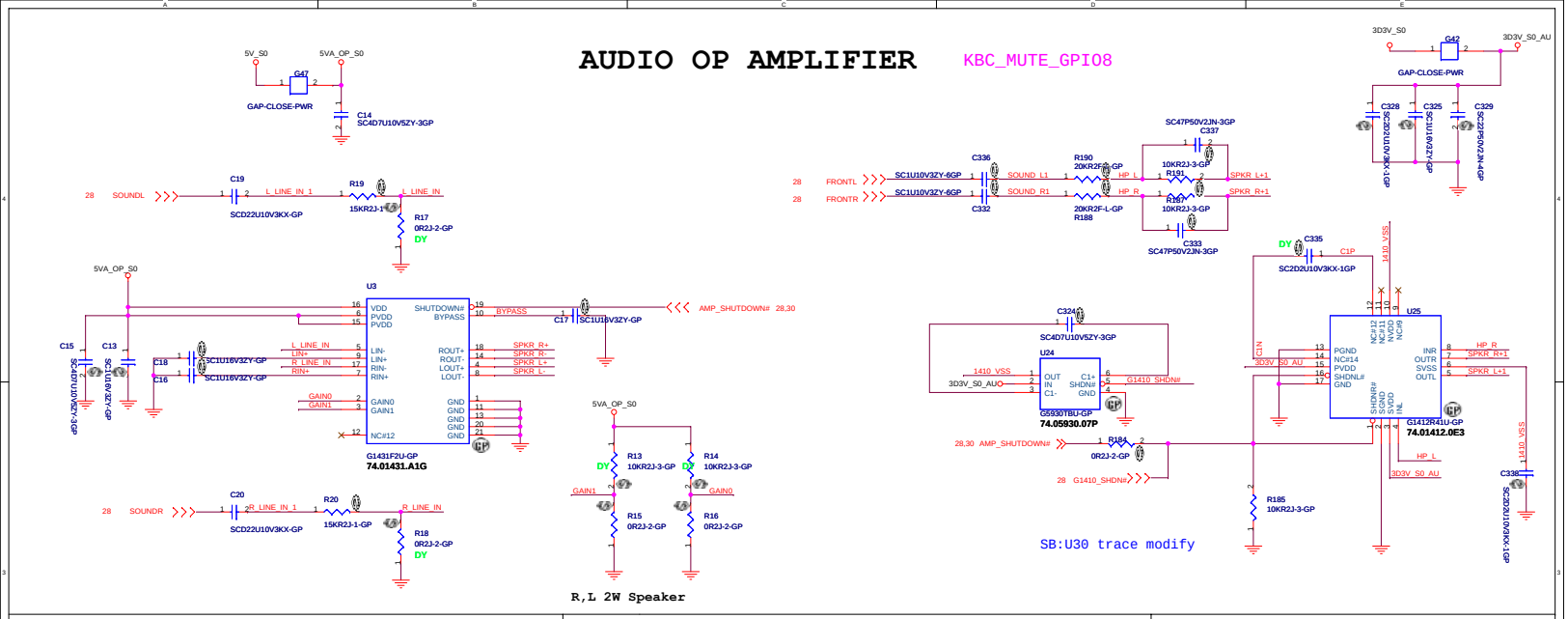
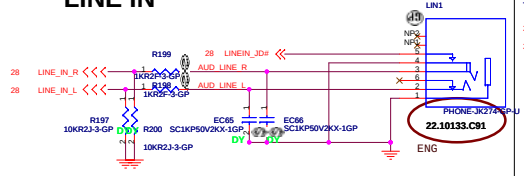
AUDIO OP AMPLIFIER

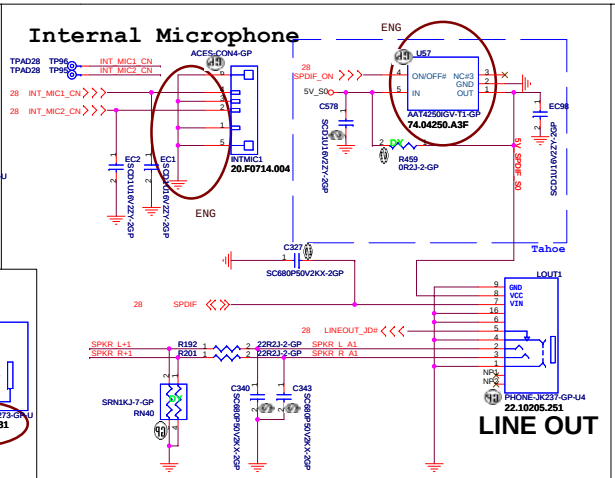
KBC_MUTE_GPIO8



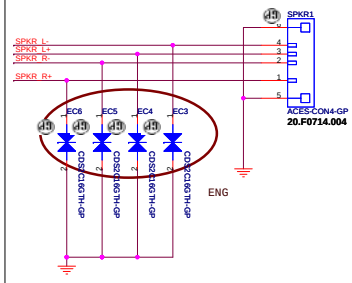
LINE IN



Internal Microphone

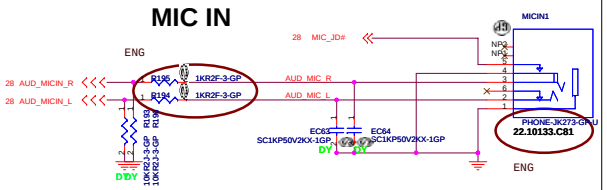


Internal Speaker

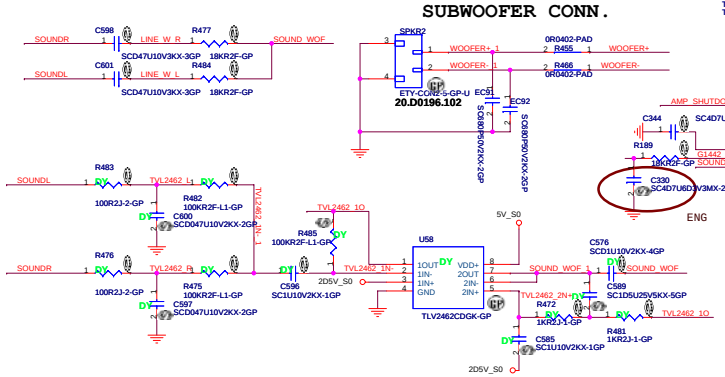


LINE OUT

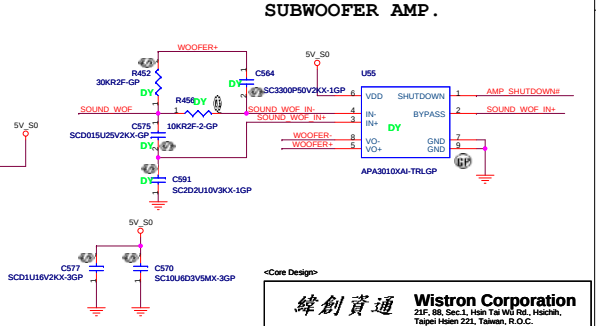
MIC IN



SUBWOOFER CONN.

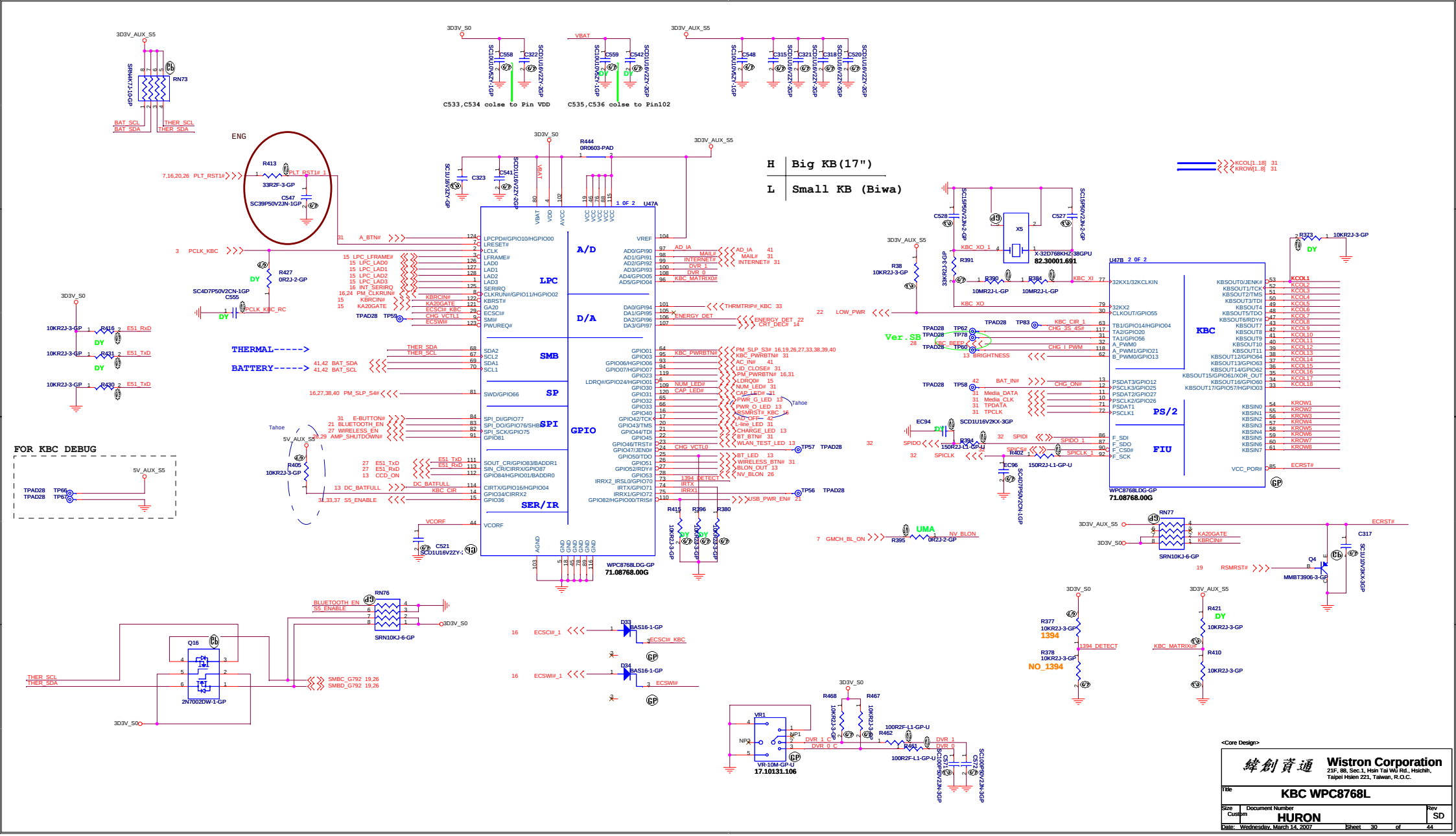


SUBWOOFER AMP.



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO AMP AND JACK		
Size	Document Number: HURON	Rev: SD
Date: Thursday, March 15, 2007	Sheet 29 of 44	


ENG
H | Big KB(17")
L | Small KB (Biwa)
C533,C534 colse to Pin VDD
C535,C536 colse to Pin102
FOR KBC DEBUG
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
THERMAL----->
BATTERY----->
WPC8768LDG-GP
71.08768.00G
KBC
PS/2
FIU
Ver.SB
UMA
NO_1394
2N7002DW-1-GP
VR-10M-GP-U
17.10131.106
Wistron Corporation
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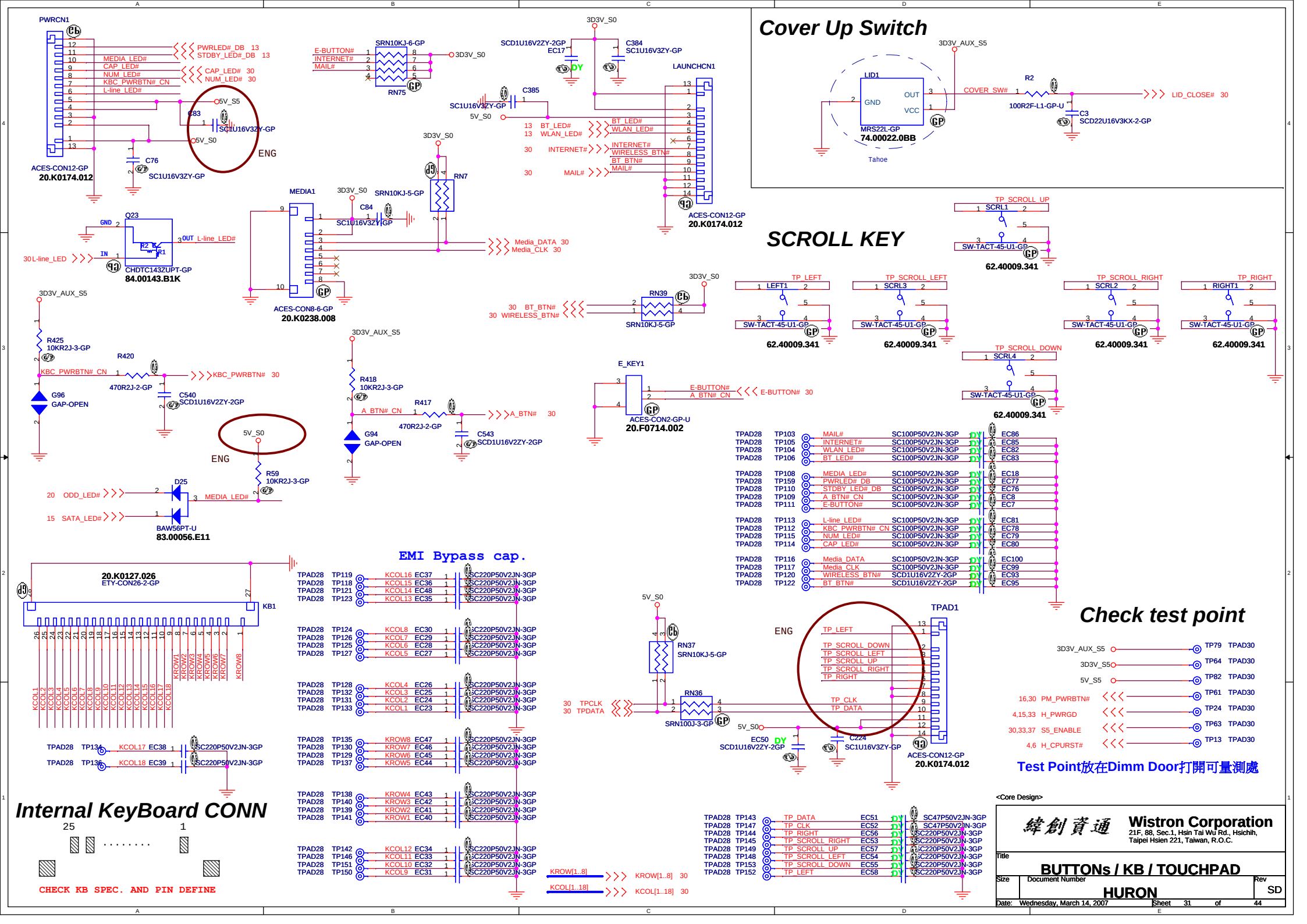
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L
HURON
Wednesday, March 14, 2007


Cover Up Switch
SCROLL KEY
Check test point
EMI Bypass cap.
Internal KeyBoard CONN
Test Point放在Dimm Door打開可量測處
CHECK KB SPEC. AND PIN DEFINE
PWRCN1
ACES-CON12-GP
20.K0174.012
SRN10KJ-6-GP
RN75
LAUNCHCN1
ACES-CON12-GP
20.K0174.012
LID1
MRS22L-GP
74.00022.0BB
Tahoe
MEDIA1
ACES-CON8-6-GP
20.K0238.008
Q23
CHDTC143ZUPT-GP
84.00143.B1K
SRN10KJ-5-GP
RN7
RN39
SRN10KJ-5-GP
E_KEY1
ACES-CON2-GP-U
20.F0714.002
62.40009.341
D25
BAW56PT-U
83.00056.E11
20.K0127.026
ETY-CON26-2-GP
KB1
RN37
SRN10KJ-5-GP
RN36
SRN100J-3-GP
TPAD1
ACES-CON12-GP
20.K0174.012
3D3V_S0
3D3V_AUX_S5
5V_S0
5V_S5
ENG
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
BUTTONs / KB / TOUCHPAD
HURON
Size
Document Number
Rev
SD
Date: Wednesday, March 14, 2007
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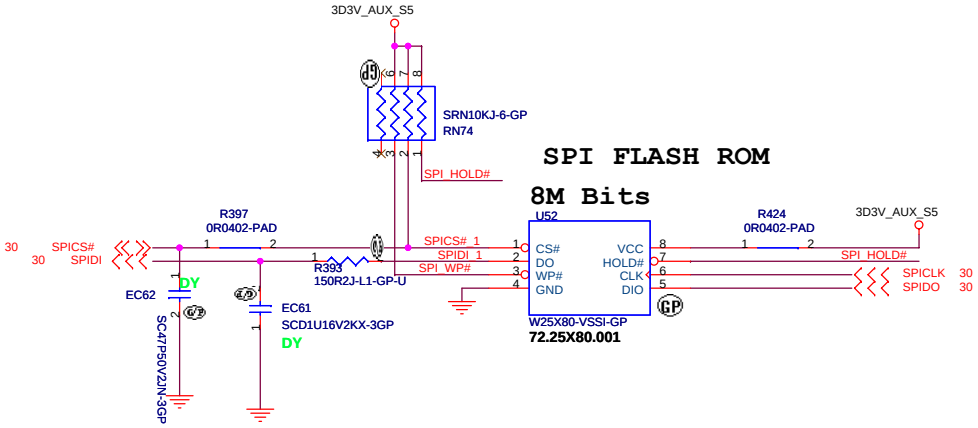

<Core Design>

緯創資通 **Wistron Corporation**
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Title: **BIOS**

Size	Document Number	Rev
A3	HURON	SD

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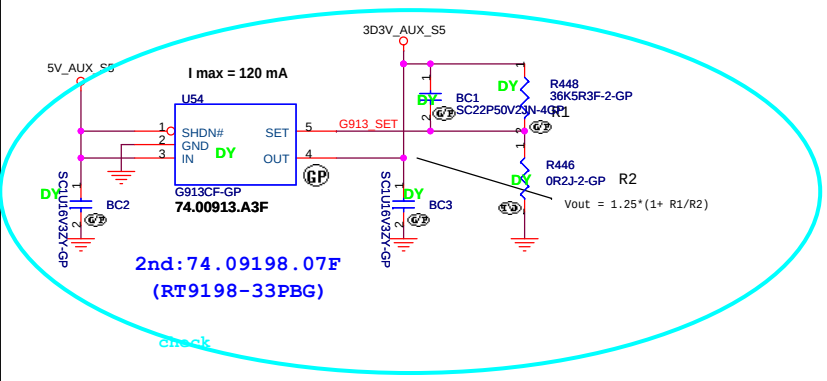
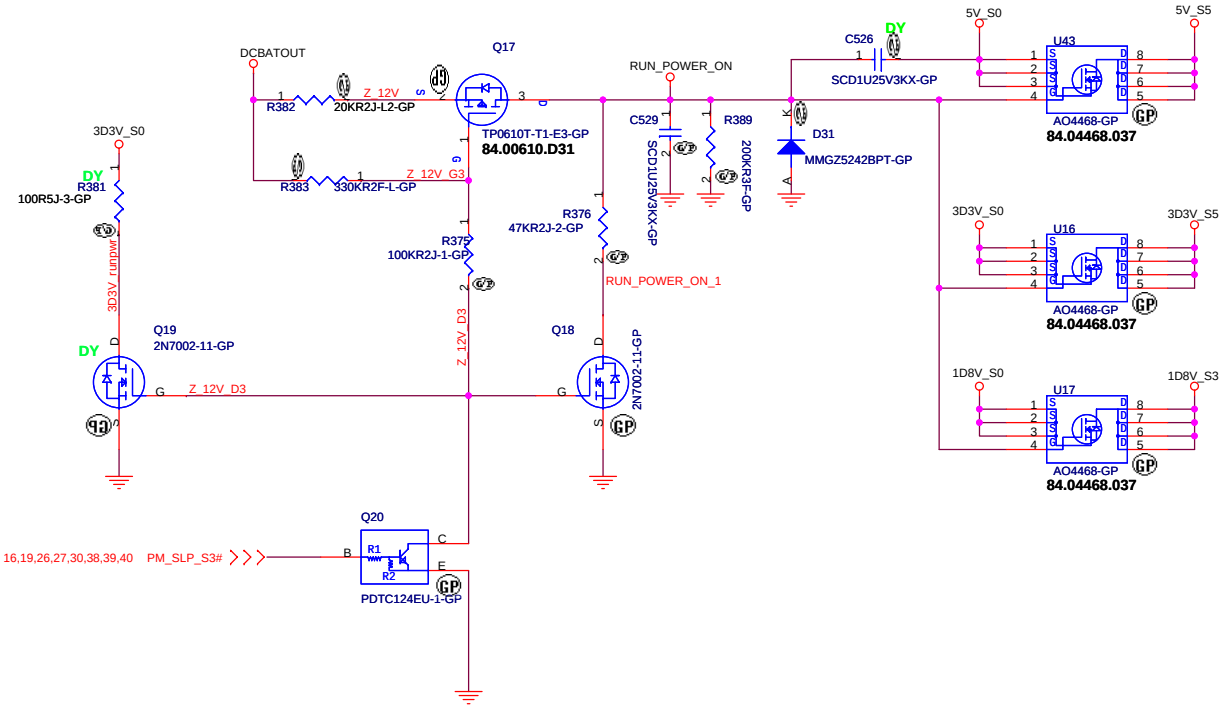
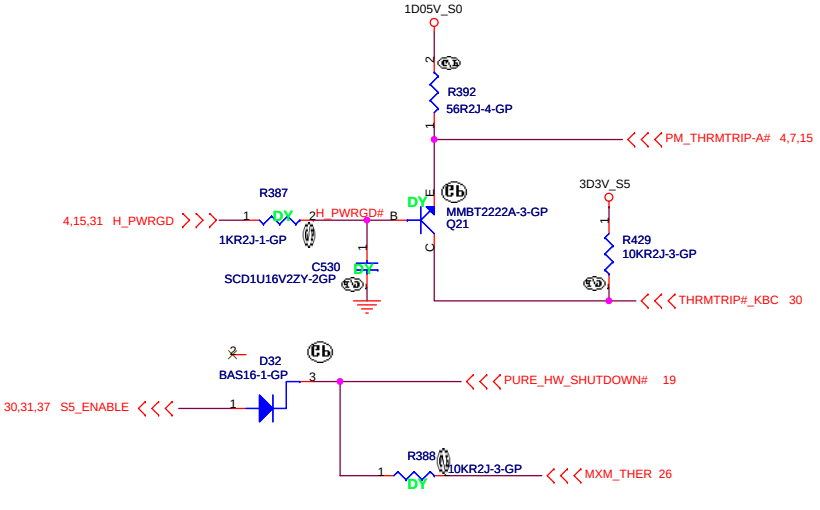
Aux Power 3D3V_AUX_S5



Run Power





<Core Design>

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Title: RUN POWER

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	HURON	SD

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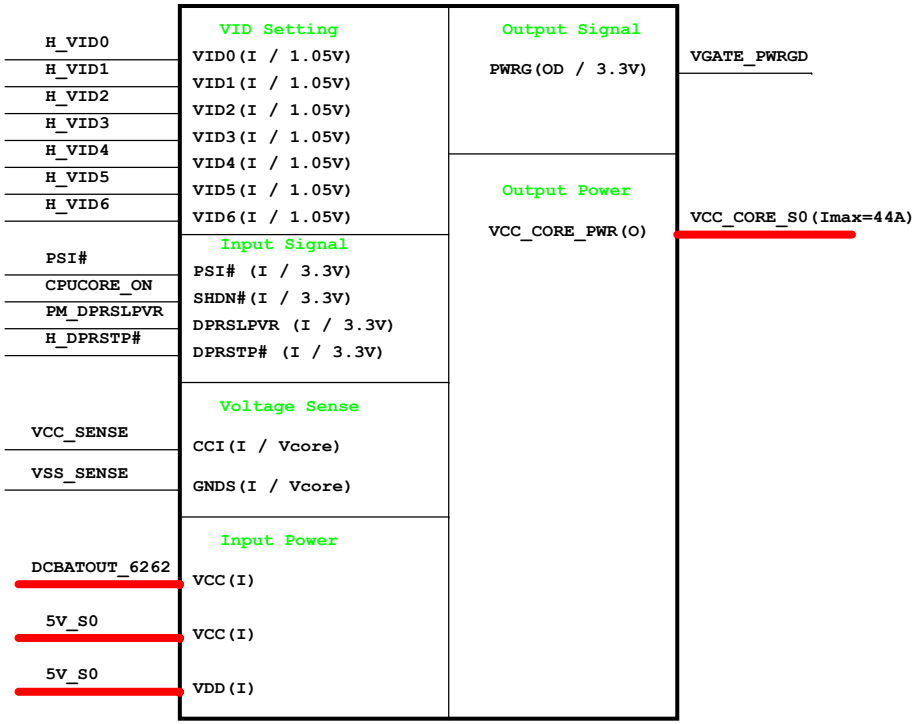
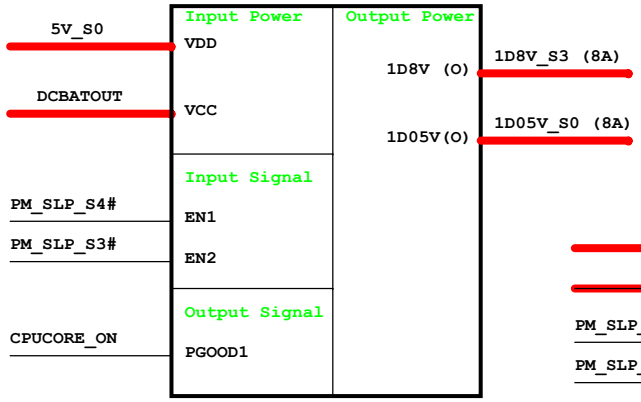
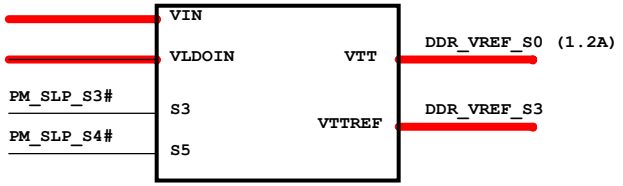
CPU_CORE
ISL6262



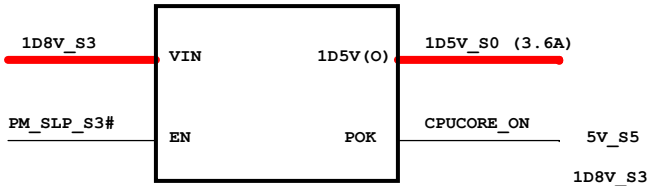
TPS51124
1D8V_S3 / 1D05V_S0



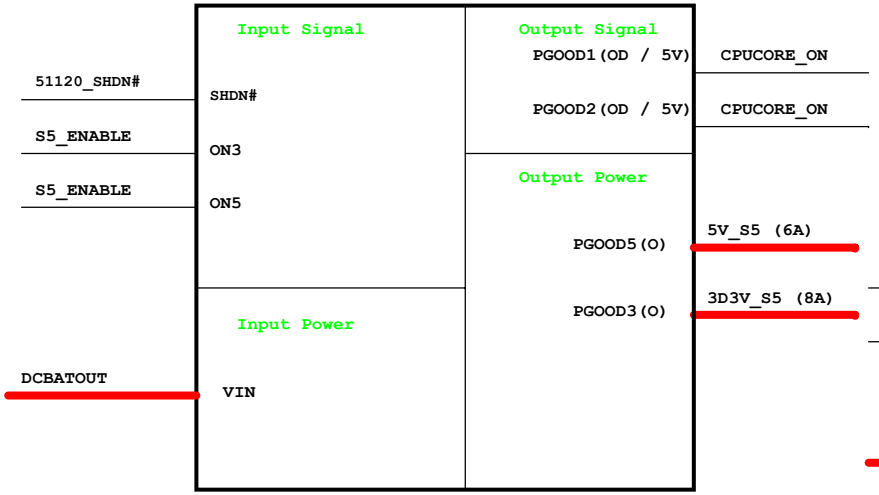
TPS51100
DDR_VREF_S0



APl5912
1D5V_S0

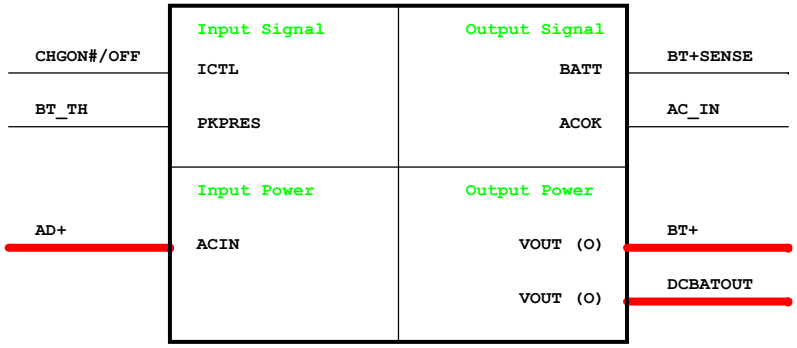


TPS51120
5V_S5 / 3D3V_S5



APL5308
2D5V_S0

Charger MAX8731A



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size	Document Number	Rev
A3	Huron	SD

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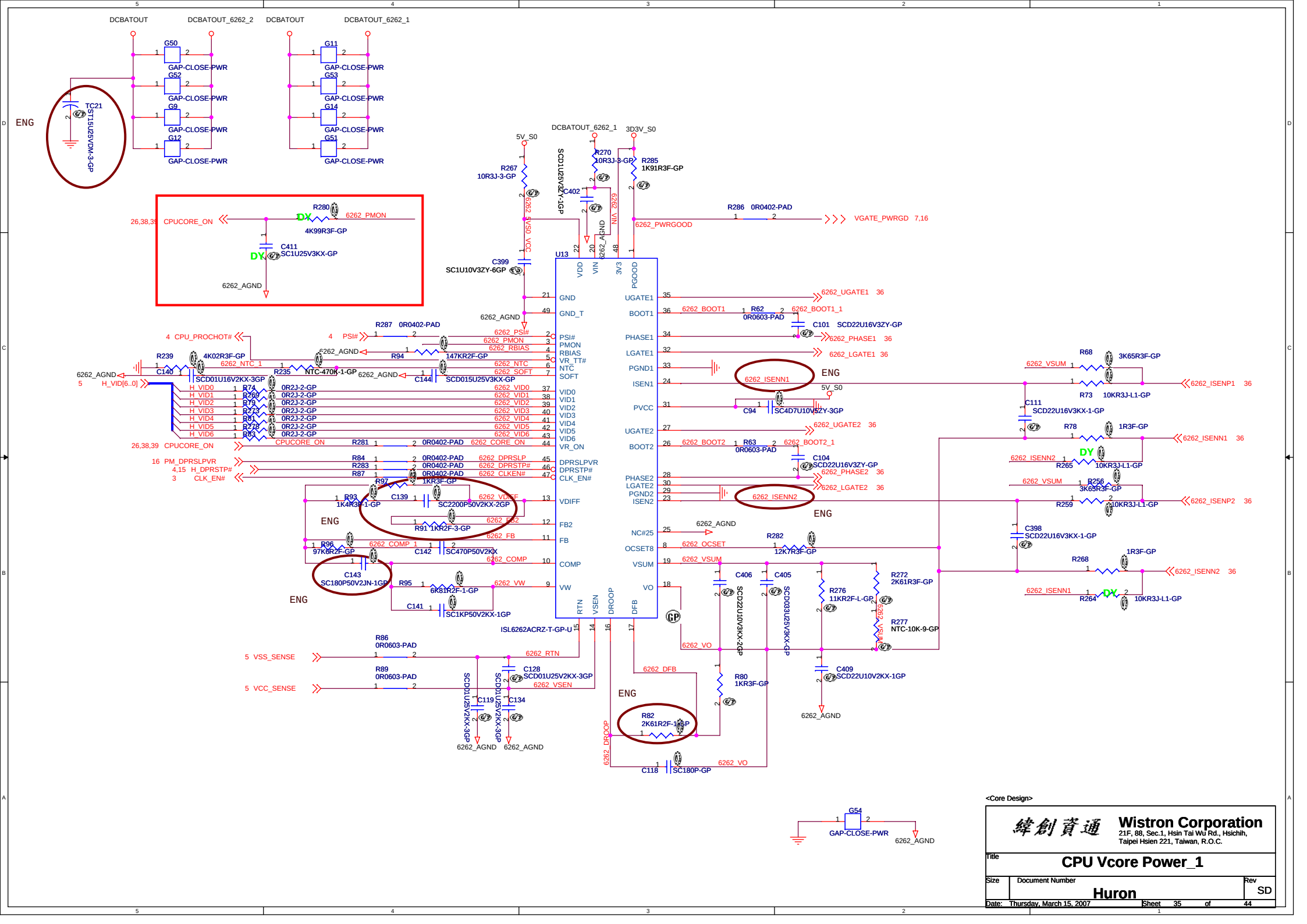
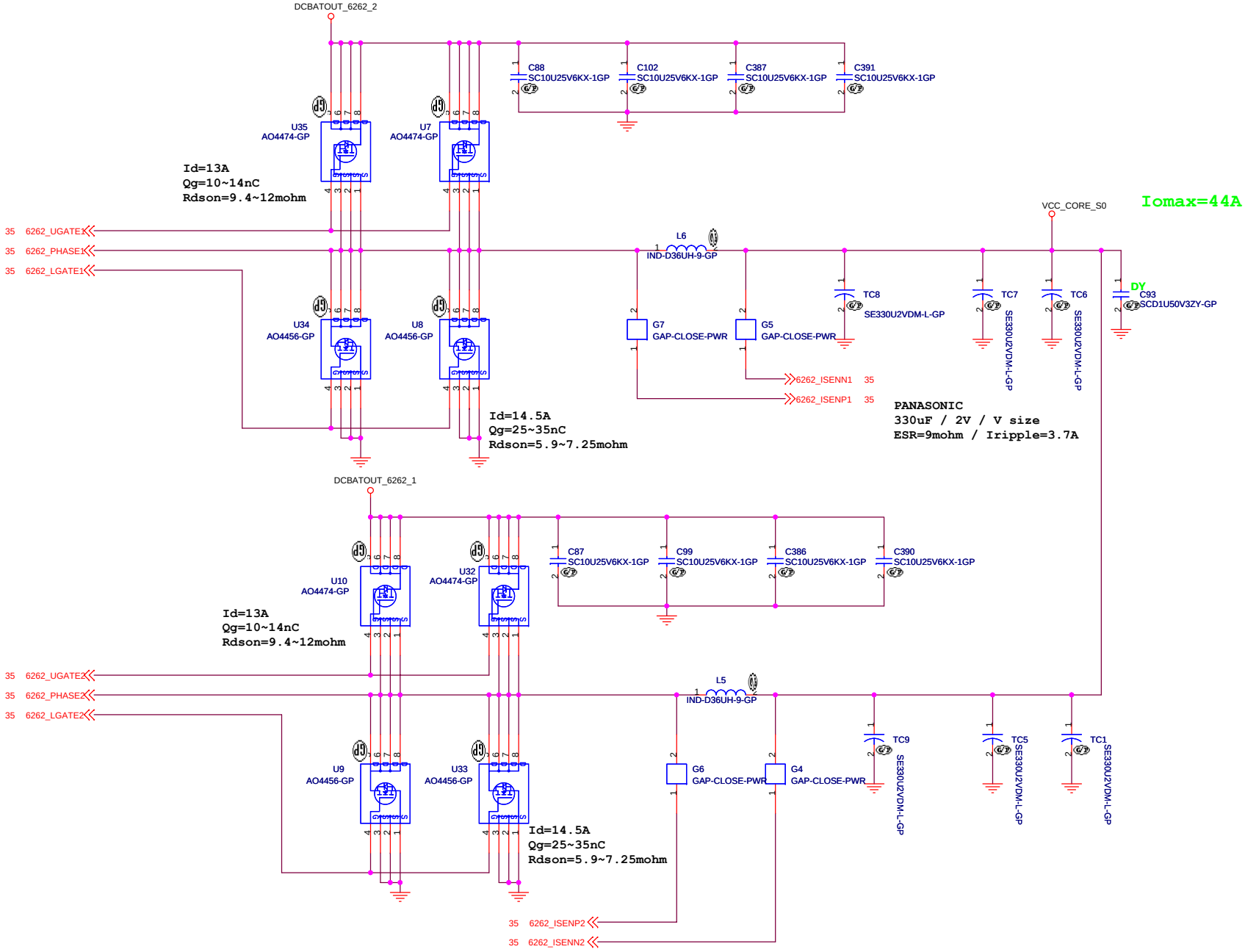


<Core Design>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU Vcore Power_1
Size	Document Number: Huron — Rev: SD
Date: Thursday, March 15, 2007	Sheet 35 of 44



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU Vcore Power_2**

Size | Document Number: **Huron** | Rev: SD

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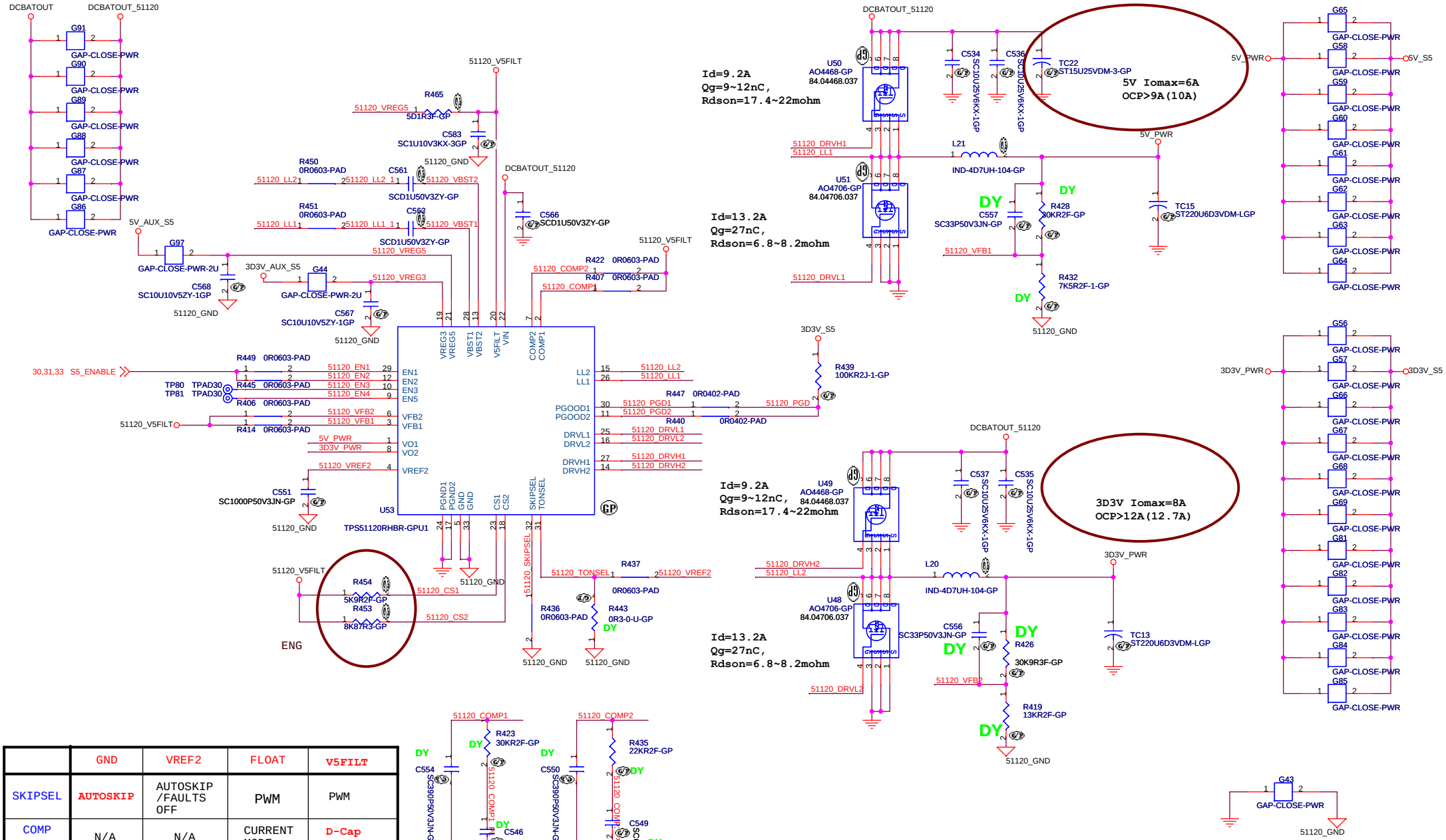

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	Switcher OFF	not use	Swithchr ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Core Design>

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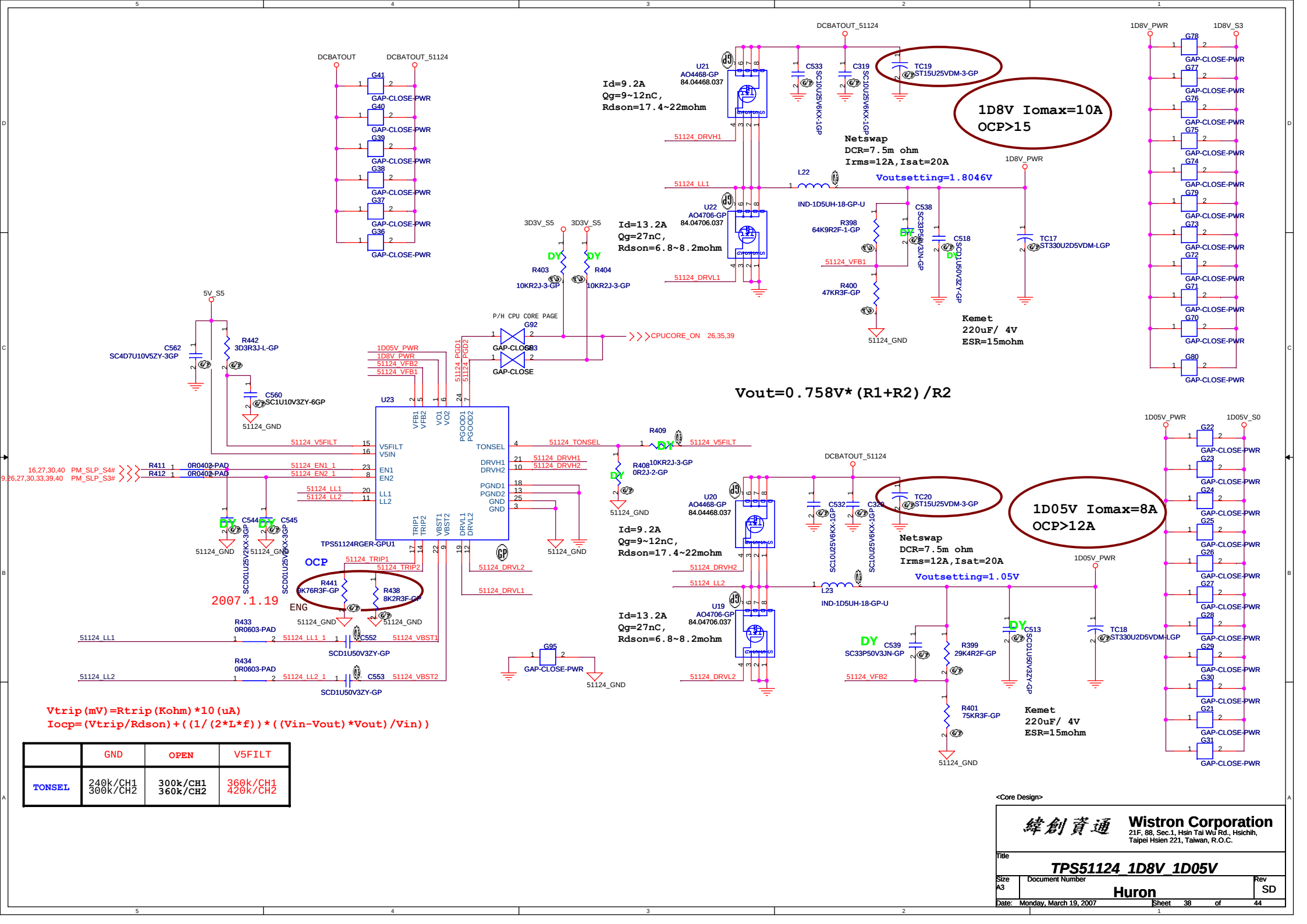
Taipei Hsien 221, Taiwan, R.O.C.

Title: 3D3V_S5 & 5V_S5
Size: Document Number: Huron
Rev: SD
Date: Thursday, March 15, 2007 Sheet 37 of 44



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

<Core Design>

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Title: TPS51124_1D8V_1D05V

Size: A3 | Document Number: Huron | Rev: SD

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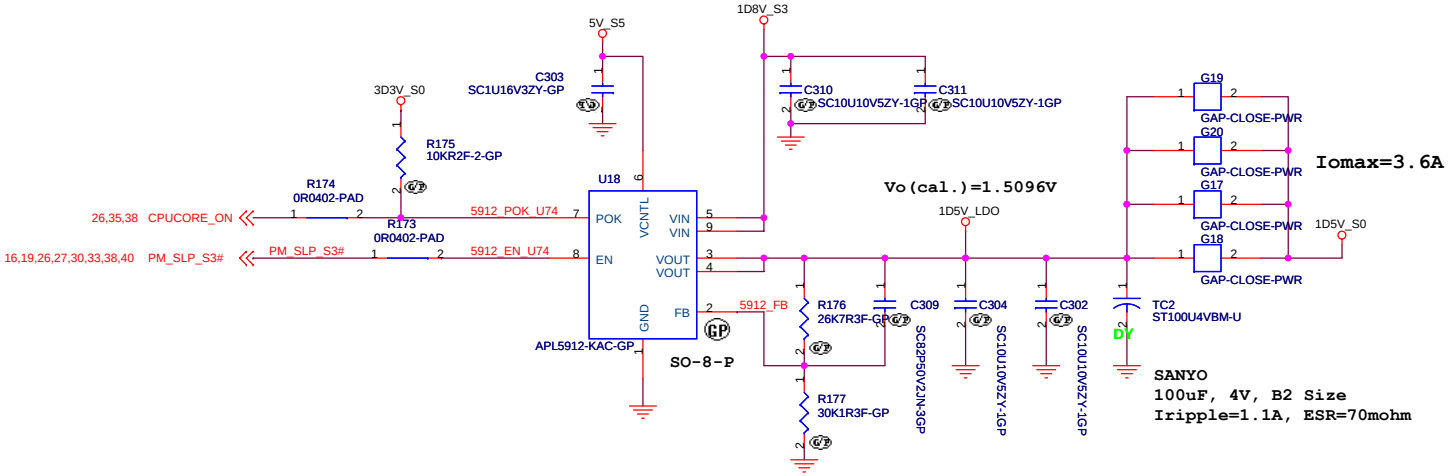
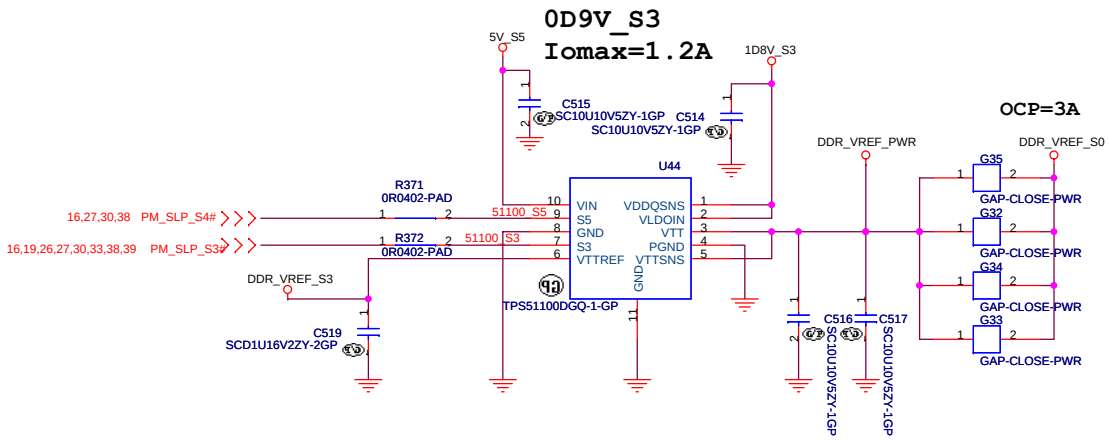
1D5V_S0
Iomax=3.6A

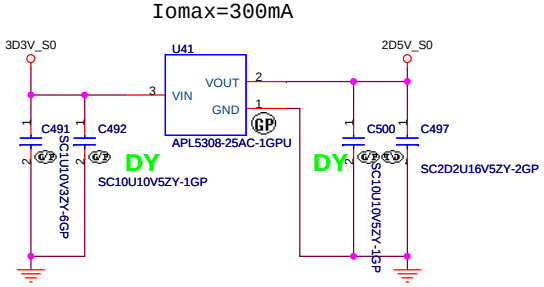


Vo=0.8*(1+(R1/R2))

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: APL5912_1D5V		
Size: A3	Document Number: Huron	Rev: SD
Date: Wednesday, March 14, 2007	Sheet 39 of 44	





<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 0D9V/2D5V		
Size: A3	Document Number: Huron	Rev: SD
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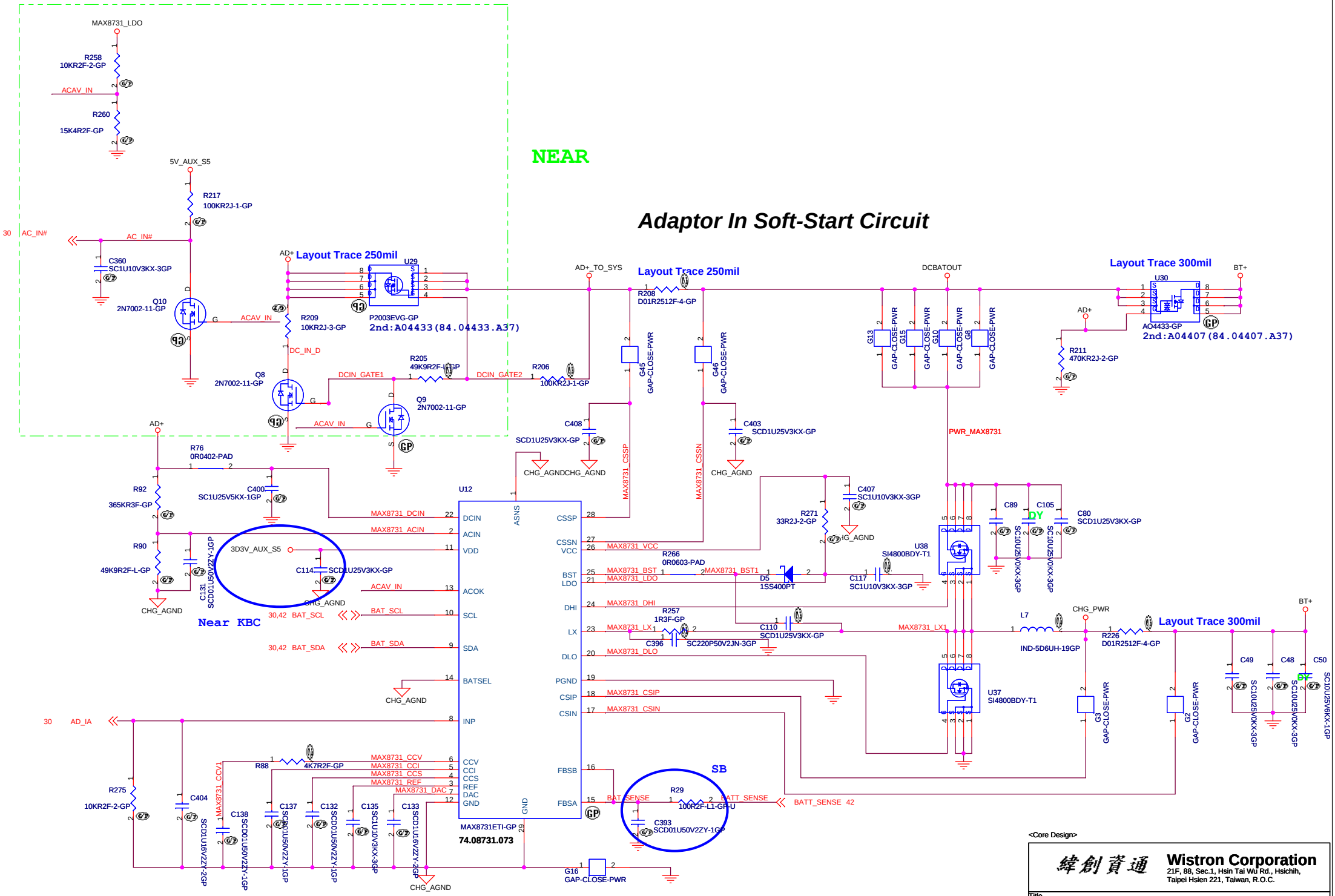

Need Check MAXIM Sming Use MAX8731 or MAX8731A

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER MAX8731

Size: A3 | Document Number: HURON | Rev: SD

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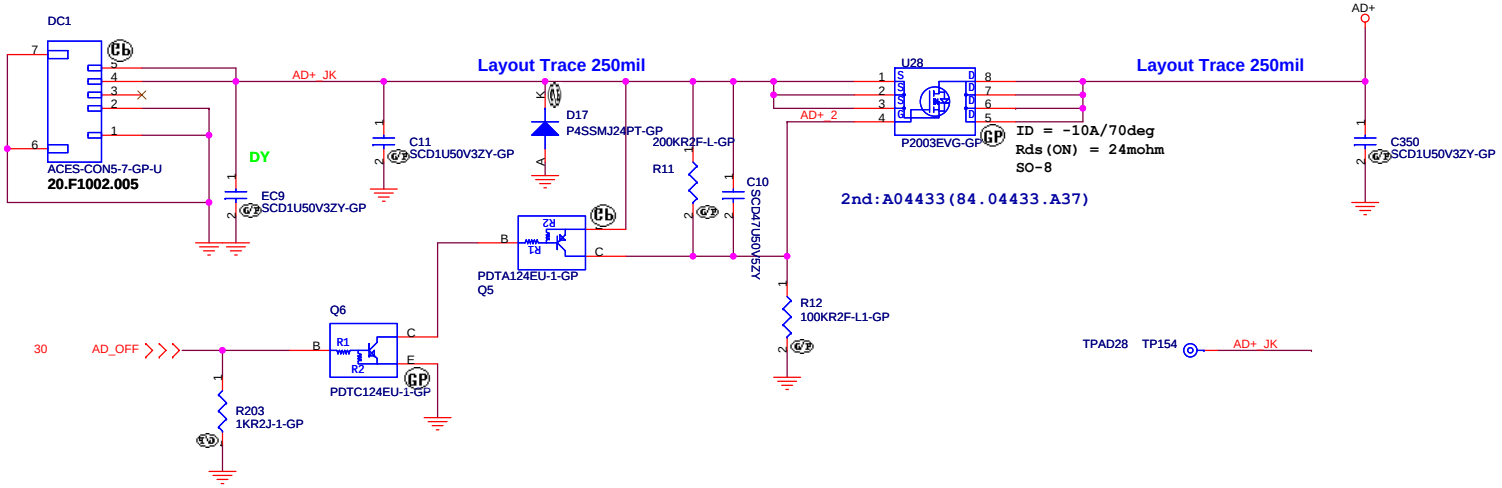
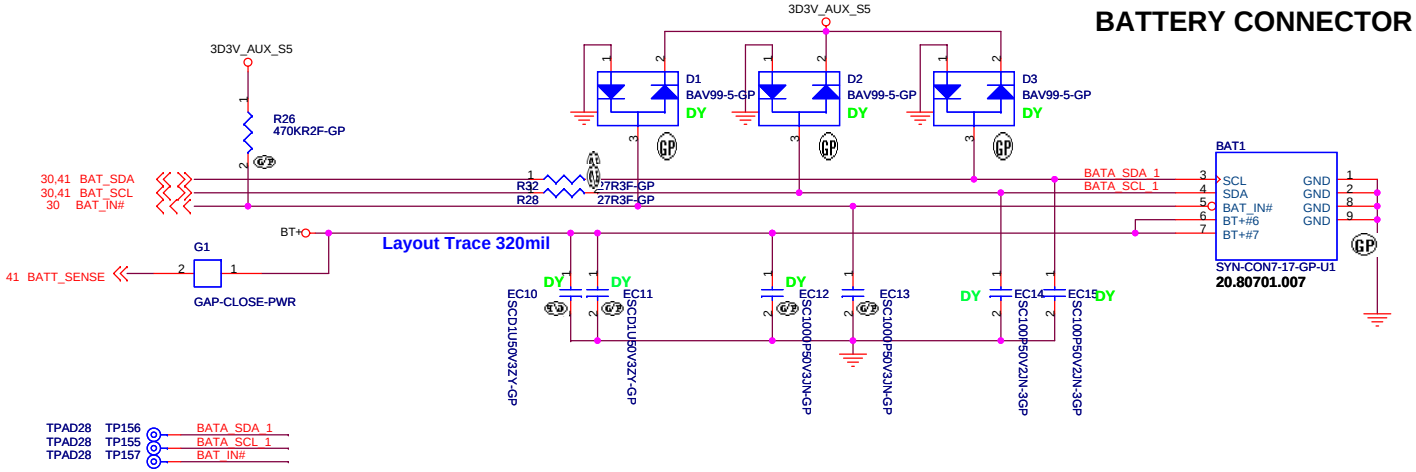
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

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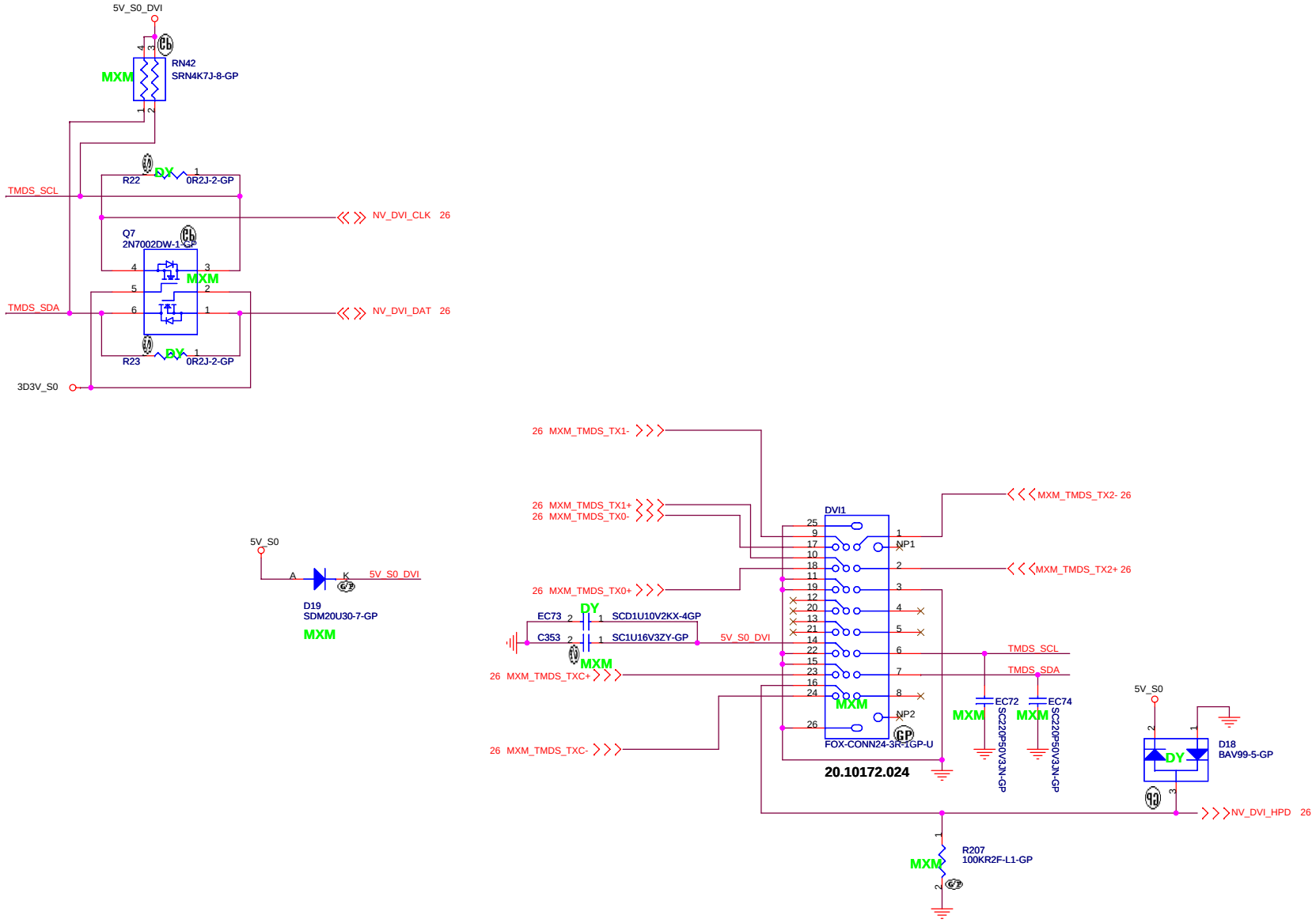
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size A3	Document Number HURON	Rev SD
Date: Monday, March 12, 2007	Sheet 42 of 44	



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DVI CONNECTOR**

Size	Document Number	Rev
A3	HURON	SD

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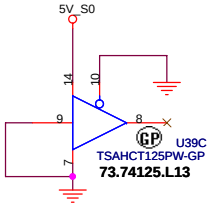
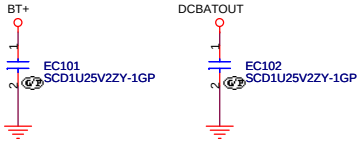
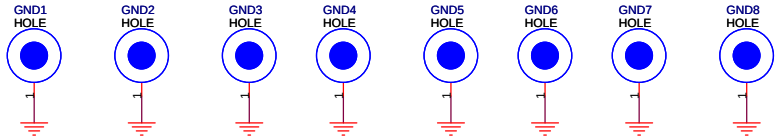
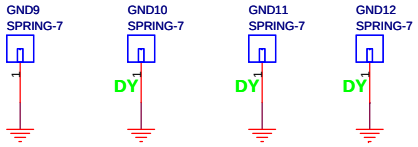




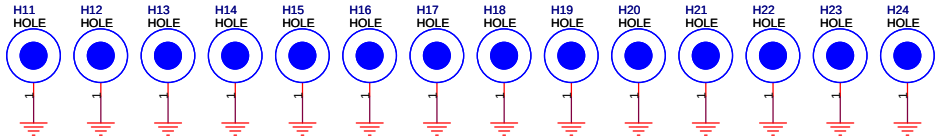


Spring



MXM H1 H2 **CPU** H4 H5 H6 **NB** H3 H7 **MINICard** H8 H9 **BD to BD** H10

34.4T902.001 34.4T901.001 34.4T901.001 34.4G502.001 34.4G501.001



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **EMI/Spring/Boss**

Size | Document Number: **HURON** | Rev: SD

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