TUCANA Block Diagram

PROJECT CODE : 91.4KK01.001
PCB P/N : 48.4KK01.0SB
REVISION : S0201-SB

Clock Generator
ICS9LVS3197BKLFT 3

Thermal Sensor
GMT G787 37

DDRIII 800 Slot 0 21 — DDRIII Channel A
DDRIII 800 Slot 1 22 — DDRIII Channel B

Intel CPU
SFF
4,5,..,10,11

FDIx8 / DMIx4

INTEL
PCH
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
6 SATA ports
8 PCIE ports
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE
12,13,...,19,20

Int MIC
Line Out
MIC In
SPKR 1.5W
Codec Realtek ALC269 31~33 — AZALIA

LVDS — LCD 23
RGB — CRT 24
PCIe — HDMI 25

USB
9 — CAMERA 23
0,1,4 — USB Port x 3 28
12 — Blue Tooth 27
2 — Cardreader Realtek RTS5186 34 — MS Pro Duo /SD(SDHC) 34
8 — Mini 1 Card WLAN/ WIMAX 35

PCIe
1 — Giga LAN Atheros AR8131M 29 — TXFM 30 — RJ45 30

HDD 26 — 0 — SATA
Flash ROM 4MB 39 — SPI

LPC
KBC Winbond NPCE781L 38 — SPI — Flash ROM 128KB 39
LPC DEBUG CONN. 39
Touch Pad 40
INT. KB 38

PCB STACKUP

TOP		L1
VCC		L2
S		L3
S		L4
GND		L5
BOTTOM		L6

SMbus ADDRESS

DIMM 1	1010 000x b
DIMM 2	1010 001x b
CLK GEN	1110 001x b
Thermal Sensor	0101 110x b
CHARGER	0001 001x b
BATTERY	0001 110x b

SYSTEM DC/DC RT8223 47

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(5A) 5V_AUX_S5 3D3V_AUX_S5

RT8209 49

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(20A)

RT8209 48

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(9.4A)

RT9026 51

INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 1.2A

CHARGER BQ24751 52

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC ADP3211 46

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 27A

GFX Core ADP3211 50

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 11A

DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
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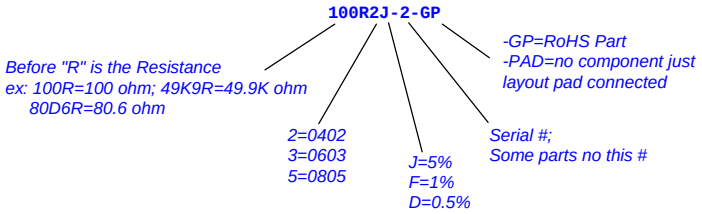
PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

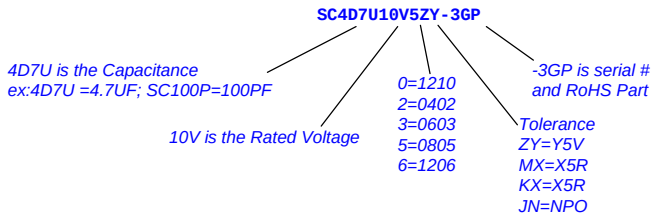
Processor Strapping

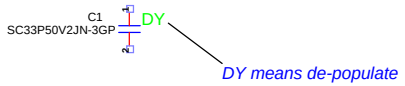
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

Resistor



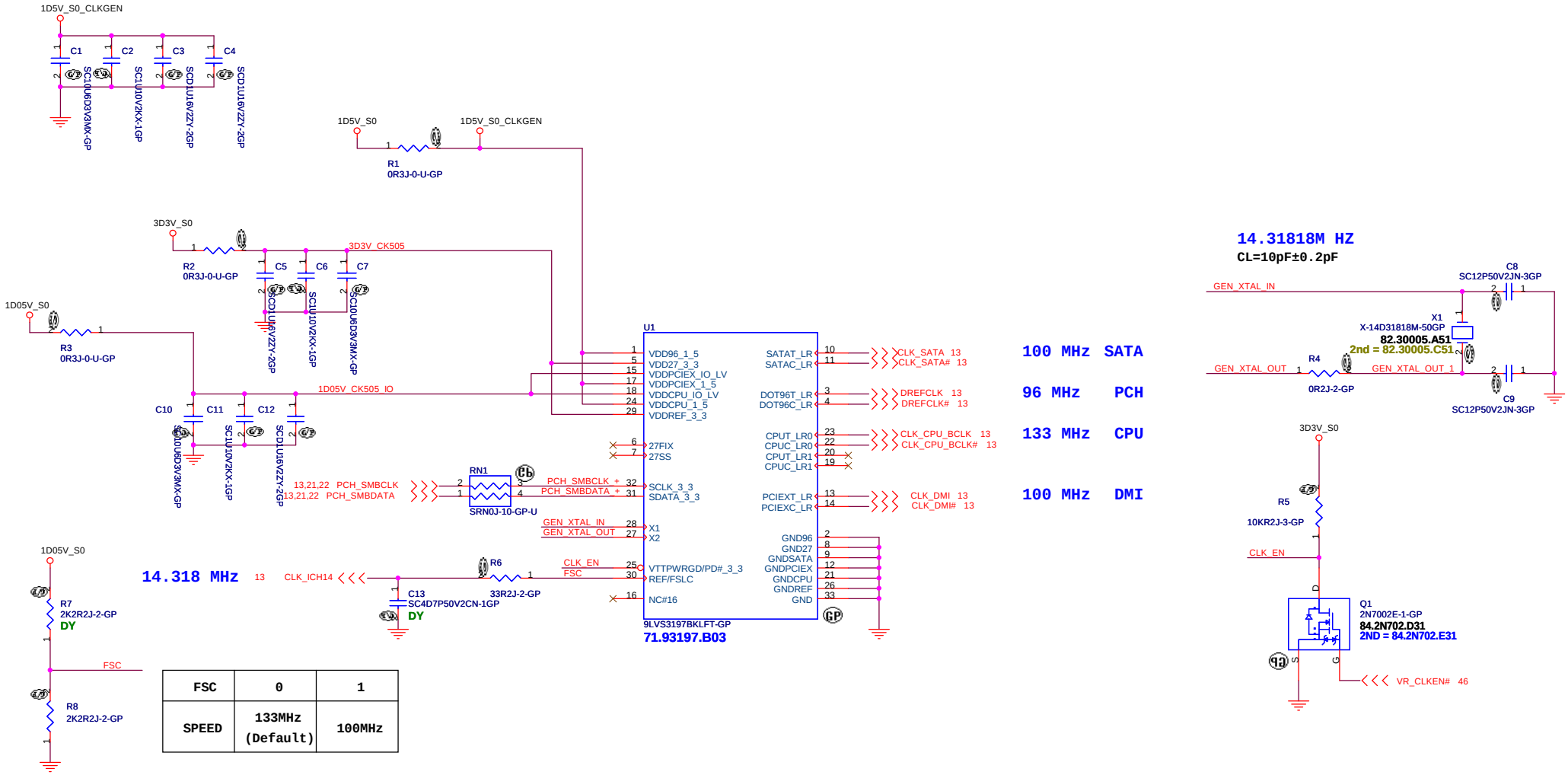
Capacitor





DVT 1ST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **Reference**	
Size: A3	Document Number: **TUCANA** Rev: **SB**
Date: Wednesday, July 07, 2010	Sheet 2 of 56



FSC	0	1
SPEED	133MHz (Default)	100MHz

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator

Size	Document Number	Rev
A3	TUCANA	SB

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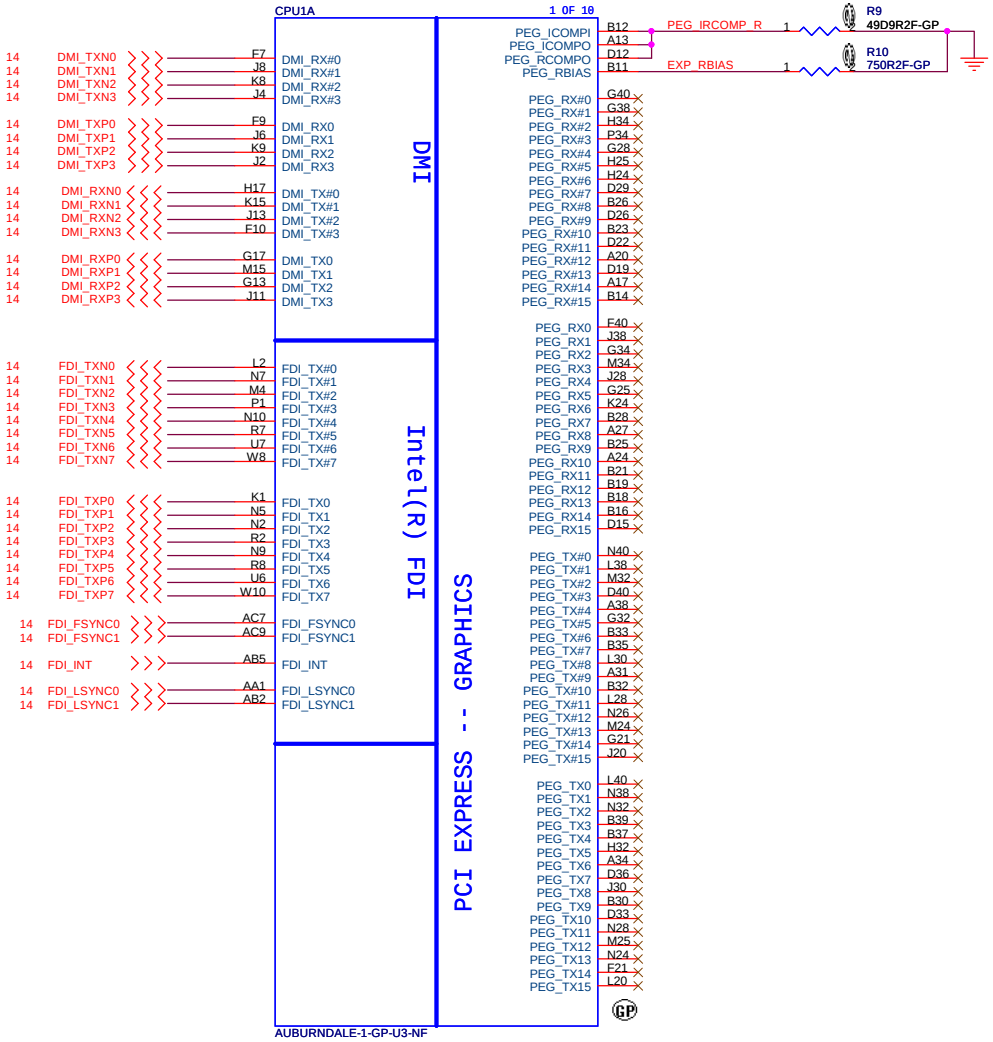


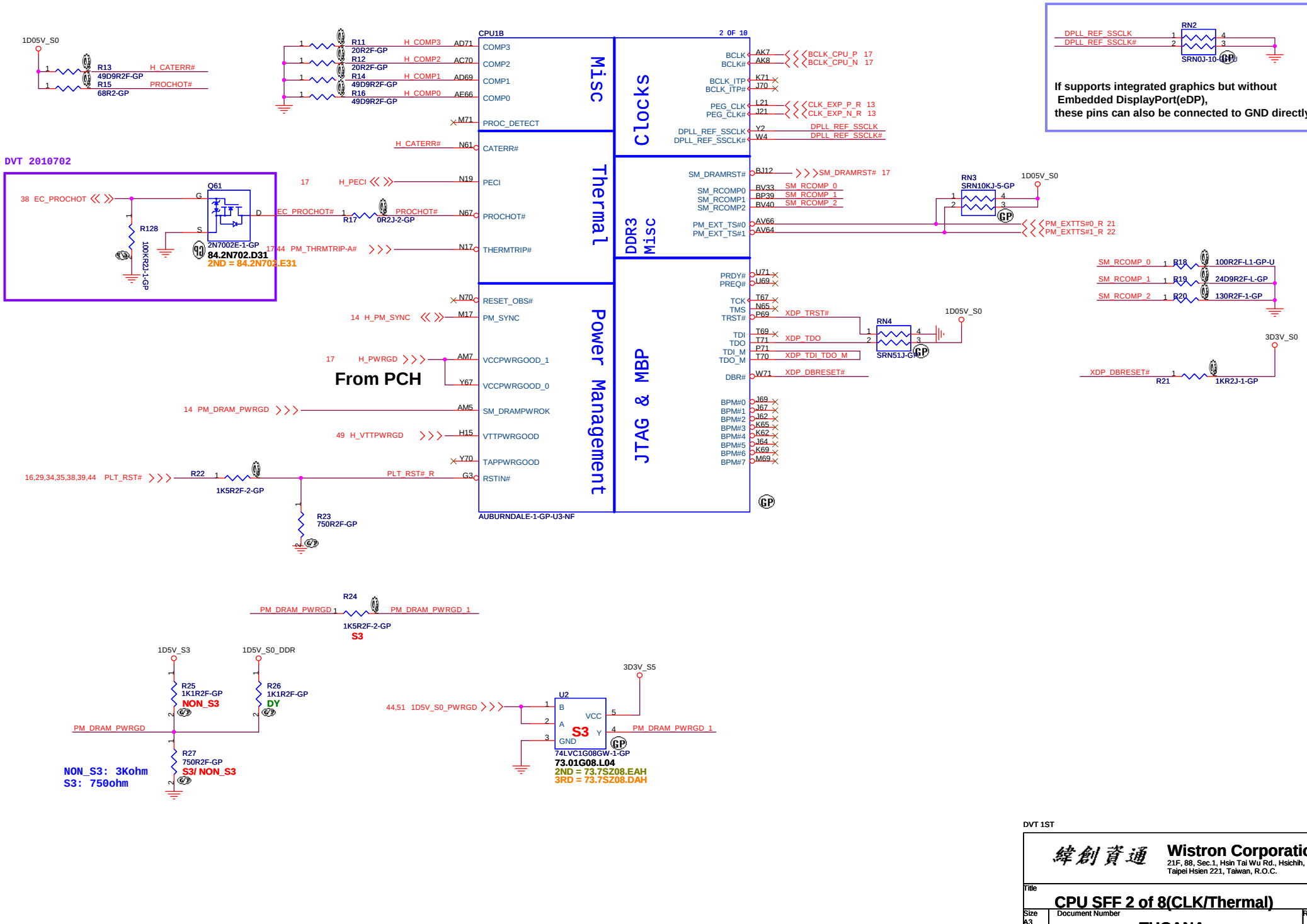
DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU SFF 1 of 8(DMI/FDI/PEG)**

Size	Document Number	Rev
A3	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 4 of 56


1D05V_S0
R13 49D9R2F-GP
R15 68R2-GP
H_CATERR#
PROCHOT#
R11 20R2F-GP
R12 20R2F-GP
R14 49D9R2F-GP
R16 49D9R2F-GP
H_COMP3
H_COMP2
H_COMP1
H_COMP0
CPU1B
2 OF 10
COMP3
COMP2
COMP1
COMP0
PROC_DETECT
CATERR#
PECI
PROCHOT#
THERMTRIP#
RESET_OBS#
PM_SYNC
VCCPWRGOOD_1
VCCPWRGOOD_0
SM_DRAMPWROK
VTTPWRGOOD
TAPPWRGOOD
RSTIN#
Misc
Thermal
Power Management
Clocks
DDR3 Misc
JTAG & MBP
BCLK
BCLK#
BCLK_ITP
BCLK_ITP#
PEG_CLK
PEG_CLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
SM_DRAMRST#
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
PM_EXT_TS#0
PM_EXT_TS#1
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
TDI_M
TDO_M
DBR#
BPM#0
BPM#1
BPM#2
BPM#3
BPM#4
BPM#5
BPM#6
BPM#7
AUBURNDALE-1-GP-U3-NF
From PCH
DVT 2010702
Q61
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
R128 100KR2J-1-GP
R17 0R2J-2-GP
EC_PROCHOT
EC_PROCHOT#
H_PECI
PM_THRMTRIP-A#
H_PM_SYNC
H_PWRGD
PM_DRAM_PWRGD
H_VTTPWRGD
PLT_RST#
PLT_RST# R
R22 1K5R2F-2-GP
R23 750R2F-GP
R24 1K5R2F-2-GP
S3
PM_DRAM_PWRGD_1
1D5V_S3
1D5V_S0_DDR
R25 1K1R2F-GP
NON_S3
R26 1K1R2F-GP
DY
R27 750R2F-GP
S3/ NON_S3
NON_S3: 3Kohm
S3: 750ohm
44,51 1D5V_S0_PWRGD
3D3V_S5
U2
74LVC1G08GW-1-GP
73.01G08.L04
2ND = 73.7SZ08.EAH
3RD = 73.7SZ08.DAH
RN3 SRN10KJ-5-GP
RN4 SRN51J-GP
SM_RCOMP_0
SM_RCOMP_1
SM_RCOMP_2
R18 100R2F-L1-GP-U
R19 24D9R2F-L-GP
R20 130R2F-1-GP
XDP_TRST#
XDP_TDO
XDP_TDI_TDO_M
XDP_DBRESET#
R21 1KR2J-1-GP
3D3V_S0
RN2
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
SRN0J-10-GP
If supports integrated graphics but without Embedded DisplayPort(eDP), these pins can also be connected to GND directly.
DVT 1ST
Wistron Corporation
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Title
CPU SFF 2 of 8(CLK/Thermal)
Size A3
Document Number
TUCANA
Rev SB
Date: Wednesday, July 07, 2010
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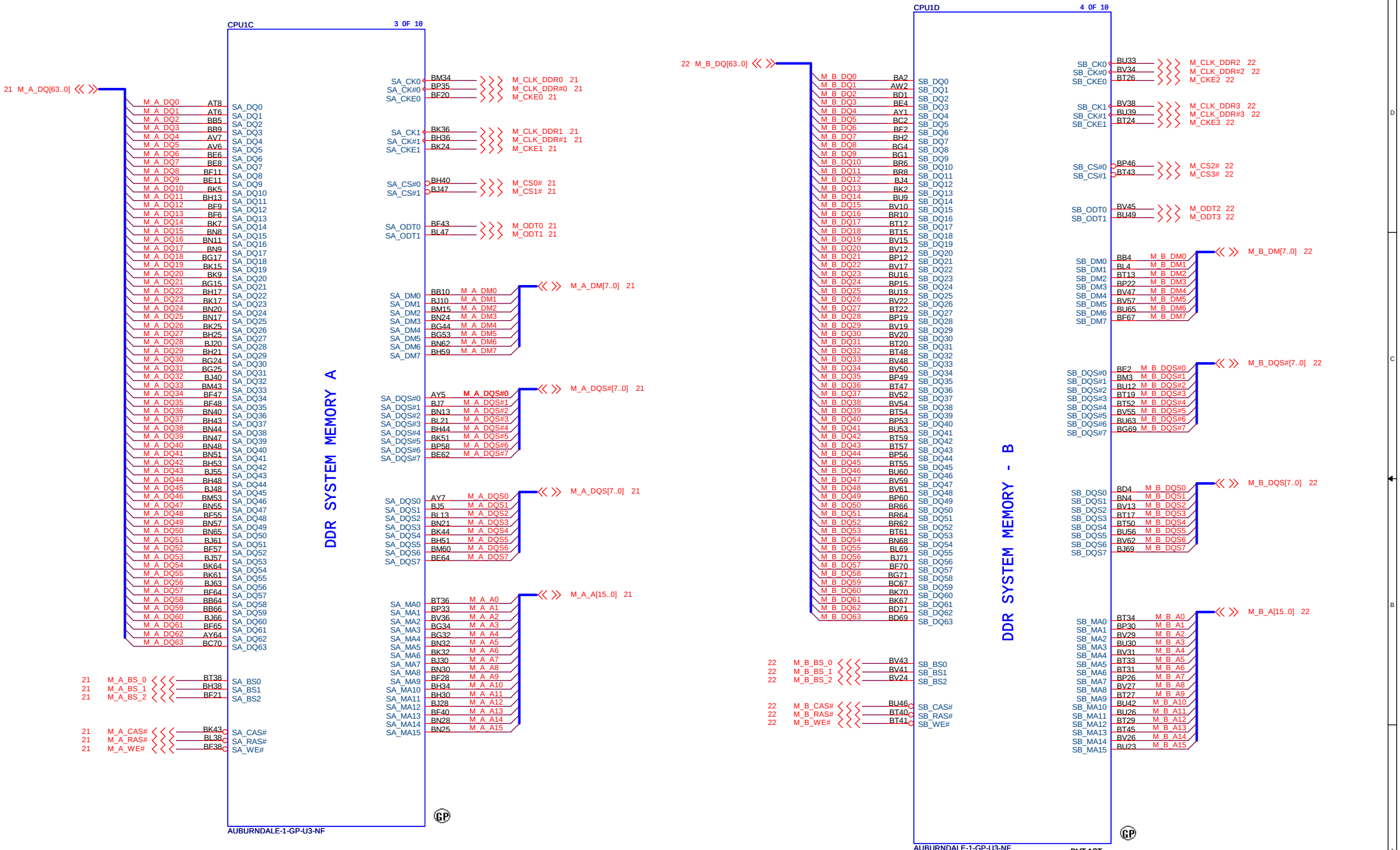
CPU1C
3 OF 10
DDR SYSTEM MEMORY A
AUBURNDALE-1-GP-U3-NF
21 M_A_DQ[63..0]
M_A_DQ0 AT8 SA_DQ0
M_A_DQ1 AT6 SA_DQ1
M_A_DQ2 BB5 SA_DQ2
M_A_DQ3 BB9 SA_DQ3
M_A_DQ4 AV7 SA_DQ4
M_A_DQ5 AV6 SA_DQ5
M_A_DQ6 BE6 SA_DQ6
M_A_DQ7 BE8 SA_DQ7
M_A_DQ8 BF11 SA_DQ8
M_A_DQ9 BE11 SA_DQ9
M_A_DQ10 BK5 SA_DQ10
M_A_DQ11 BH13 SA_DQ11
M_A_DQ12 BF9 SA_DQ12
M_A_DQ13 BF6 SA_DQ13
M_A_DQ14 BK7 SA_DQ14
M_A_DQ15 BN8 SA_DQ15
M_A_DQ16 BN11 SA_DQ16
M_A_DQ17 BN9 SA_DQ17
M_A_DQ18 BG17 SA_DQ18
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M_A_DQ21 BG15 SA_DQ21
M_A_DQ22 BH17 SA_DQ22
M_A_DQ23 BK17 SA_DQ23
M_A_DQ24 BN20 SA_DQ24
M_A_DQ25 BN17 SA_DQ25
M_A_DQ26 BK25 SA_DQ26
M_A_DQ27 BH25 SA_DQ27
M_A_DQ28 BJ20 SA_DQ28
M_A_DQ29 BH21 SA_DQ29
M_A_DQ30 BG24 SA_DQ30
M_A_DQ31 BG25 SA_DQ31
M_A_DQ32 BJ40 SA_DQ32
M_A_DQ33 BM43 SA_DQ33
M_A_DQ34 BF47 SA_DQ34
M_A_DQ35 BF48 SA_DQ35
M_A_DQ36 BN40 SA_DQ36
M_A_DQ37 BH43 SA_DQ37
M_A_DQ38 BN44 SA_DQ38
M_A_DQ39 BN47 SA_DQ39
M_A_DQ40 BN48 SA_DQ40
M_A_DQ41 BN51 SA_DQ41
M_A_DQ42 BH53 SA_DQ42
M_A_DQ43 BJ55 SA_DQ43
M_A_DQ44 BH48 SA_DQ44
M_A_DQ45 BJ48 SA_DQ45
M_A_DQ46 BM53 SA_DQ46
M_A_DQ47 BN55 SA_DQ47
M_A_DQ48 BF55 SA_DQ48
M_A_DQ49 BN57 SA_DQ49
M_A_DQ50 BN65 SA_DQ50
M_A_DQ51 BJ61 SA_DQ51
M_A_DQ52 BF57 SA_DQ52
M_A_DQ53 BJ57 SA_DQ53
M_A_DQ54 BK64 SA_DQ54
M_A_DQ55 BK61 SA_DQ55
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M_A_DQ57 BF64 SA_DQ57
M_A_DQ58 BB64 SA_DQ58
M_A_DQ59 BB66 SA_DQ59
M_A_DQ60 BJ66 SA_DQ60
M_A_DQ61 BF65 SA_DQ61
M_A_DQ62 AY64 SA_DQ62
M_A_DQ63 BC70 SA_DQ63
21 M_A_BS_0 BT38 SA_BS0
21 M_A_BS_1 BH38 SA_BS1
21 M_A_BS_2 BF21 SA_BS2
21 M_A_CAS# BK43 SA_CAS#
21 M_A_RAS# BL38 SA_RAS#
21 M_A_WE# BF38 SA_WE#
SA_CK0 BM34 M_CLK_DDR0 21
SA_CK#0 BP35 M_CLK_DDR#0 21
SA_CKE0 BF20 M_CKE0 21
SA_CK1 BK36 M_CLK_DDR1 21
SA_CK#1 BH36 M_CLK_DDR#1 21
SA_CKE1 BK24 M_CKE1 21
SA_CS#0 BH40 M_CS0# 21
SA_CS#1 BJ47 M_CS1# 21
SA_ODT0 BF43 M_ODT0 21
SA_ODT1 BL47 M_ODT1 21
SA_DM0 BB10 M_A_DM0
SA_DM1 BJ10 M_A_DM1
SA_DM2 BM15 M_A_DM2
SA_DM3 BN24 M_A_DM3
SA_DM4 BG44 M_A_DM4
SA_DM5 BG53 M_A_DM5
SA_DM6 BN62 M_A_DM6
SA_DM7 BH59 M_A_DM7
M_A_DM[7..0] 21
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SA_DQS#4 BH44 M_A_DQS#4
SA_DQS#5 BK51 M_A_DQS#5
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SA_DQS7 BE64 M_A_DQS7
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SA_MA1 BP33 M_A_A1
SA_MA2 BV36 M_A_A2
SA_MA3 BG34 M_A_A3
SA_MA4 BG32 M_A_A4
SA_MA5 BN32 M_A_A5
SA_MA6 BK32 M_A_A6
SA_MA7 BJ30 M_A_A7
SA_MA8 BN30 M_A_A8
SA_MA9 BF28 M_A_A9
SA_MA10 BH34 M_A_A10
SA_MA11 BH30 M_A_A11
SA_MA12 BJ28 M_A_A12
SA_MA13 BF40 M_A_A13
SA_MA14 BN28 M_A_A14
SA_MA15 BN25 M_A_A15
M_A_A[15..0] 21
CPU1D
4 OF 10
DDR SYSTEM MEMORY - B
AUBURNDALE-1-GP-U3-NF
22 M_B_DQ[63..0]
M_B_DQ0 BA2 SB_DQ0
M_B_DQ1 AW2 SB_DQ1
M_B_DQ2 BD1 SB_DQ2
M_B_DQ3 BE4 SB_DQ3
M_B_DQ4 AY1 SB_DQ4
M_B_DQ5 BC2 SB_DQ5
M_B_DQ6 BF2 SB_DQ6
M_B_DQ7 BH2 SB_DQ7
M_B_DQ8 BG4 SB_DQ8
M_B_DQ9 BG1 SB_DQ9
M_B_DQ10 BR6 SB_DQ10
M_B_DQ11 BR8 SB_DQ11
M_B_DQ12 BJ4 SB_DQ12
M_B_DQ13 BK2 SB_DQ13
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M_B_DQ30 BV20 SB_DQ30
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M_B_DQ59 BC67 SB_DQ59
M_B_DQ60 BK70 SB_DQ60
M_B_DQ61 BK67 SB_DQ61
M_B_DQ62 BD71 SB_DQ62
M_B_DQ63 BD69 SB_DQ63
22 M_B_BS_0 BV43 SB_BS0
22 M_B_BS_1 BV41 SB_BS1
22 M_B_BS_2 BV24 SB_BS2
22 M_B_CAS# BU46 SB_CAS#
22 M_B_RAS# BT40 SB_RAS#
22 M_B_WE# BT41 SB_WE#
SB_CK0 BU33 M_CLK_DDR2 22
SB_CK#0 BV34 M_CLK_DDR#2 22
SB_CKE0 BT26 M_CKE2 22
SB_CK1 BV38 M_CLK_DDR3 22
SB_CK#1 BU39 M_CLK_DDR#3 22
SB_CKE1 BT24 M_CKE3 22
SB_CS#0 BP46 M_CS2# 22
SB_CS#1 BT43 M_CS3# 22
SB_ODT0 BV45 M_ODT2 22
SB_ODT1 BU49 M_ODT3 22
SB_DM0 BB4 M_B_DM0
SB_DM1 BL4 M_B_DM1
SB_DM2 BT13 M_B_DM2
SB_DM3 BP22 M_B_DM3
SB_DM4 BV47 M_B_DM4
SB_DM5 BV57 M_B_DM5
SB_DM6 BU65 M_B_DM6
SB_DM7 BF67 M_B_DM7
M_B_DM[7..0] 22
SB_DQS#0 BE2 M_B_DQS#0
SB_DQS#1 BM3 M_B_DQS#1
SB_DQS#2 BU12 M_B_DQS#2
SB_DQS#3 BT19 M_B_DQS#3
SB_DQS#4 BT52 M_B_DQS#4
SB_DQS#5 BV55 M_B_DQS#5
SB_DQS#6 BU63 M_B_DQS#6
SB_DQS#7 BG69 M_B_DQS#7
M_B_DQS#[7..0] 22
SB_DQS0 BD4 M_B_DQS0
SB_DQS1 BN4 M_B_DQS1
SB_DQS2 BV13 M_B_DQS2
SB_DQS3 BT17 M_B_DQS3
SB_DQS4 BT50 M_B_DQS4
SB_DQS5 BU56 M_B_DQS5
SB_DQS6 BV62 M_B_DQS6
SB_DQS7 BJ69 M_B_DQS7
M_B_DQS[7..0] 22
SB_MA0 BT34 M_B_A0
SB_MA1 BP30 M_B_A1
SB_MA2 BV29 M_B_A2
SB_MA3 BU30 M_B_A3
SB_MA4 BV31 M_B_A4
SB_MA5 BT33 M_B_A5
SB_MA6 BT31 M_B_A6
SB_MA7 BP26 M_B_A7
SB_MA8 BV27 M_B_A8
SB_MA9 BT27 M_B_A9
SB_MA10 BU42 M_B_A10
SB_MA11 BU26 M_B_A11
SB_MA12 BT29 M_B_A12
SB_MA13 BT45 M_B_A13
SB_MA14 BV26 M_B_A14
SB_MA15 BU23 M_B_A15
M_B_A[15..0] 22
DVT 1ST
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU SFF 3 of 8(DDR)
Size A3
Document Number
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Date: Wednesday, July 07, 2010
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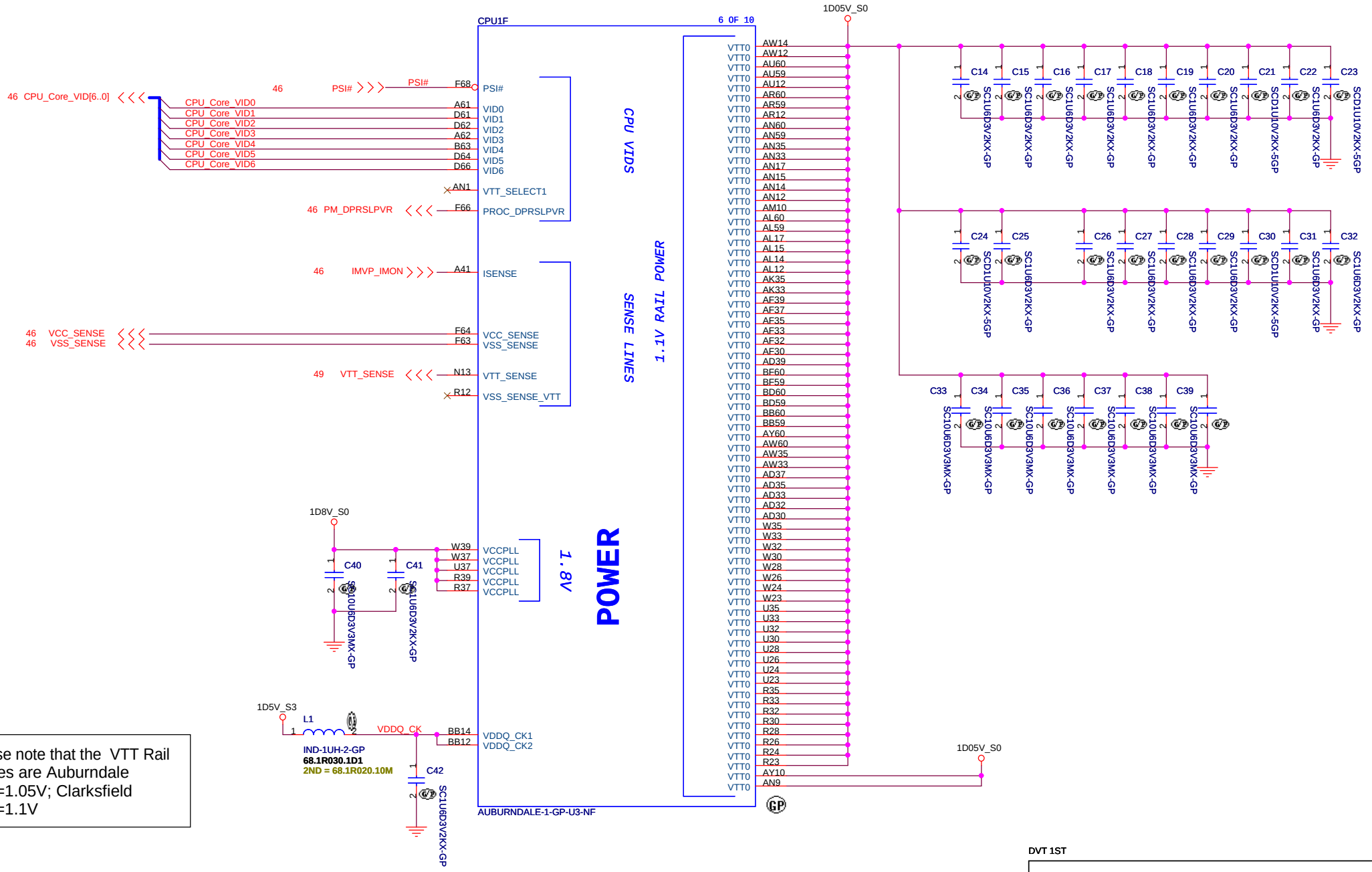
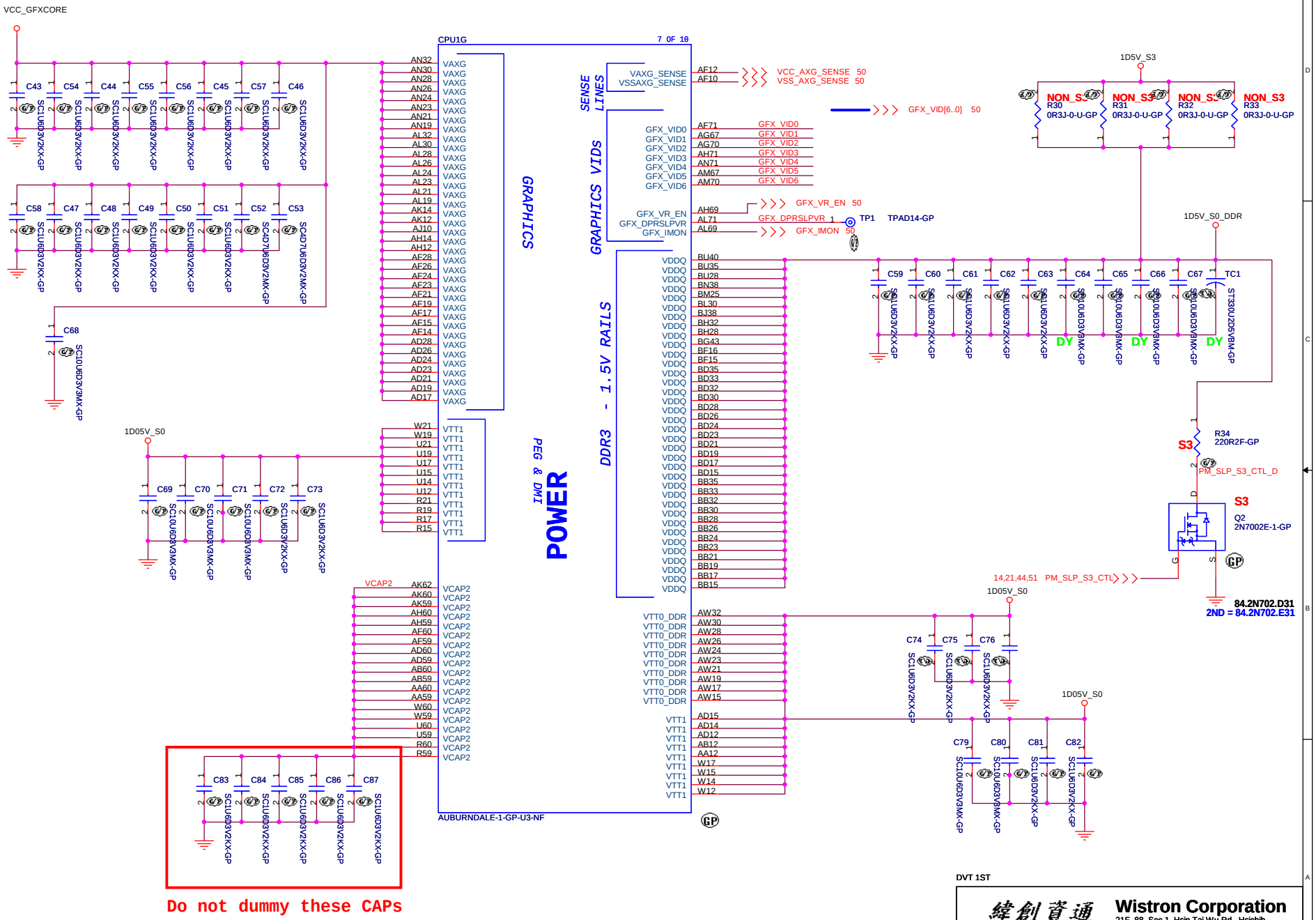


Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

DVT 1ST

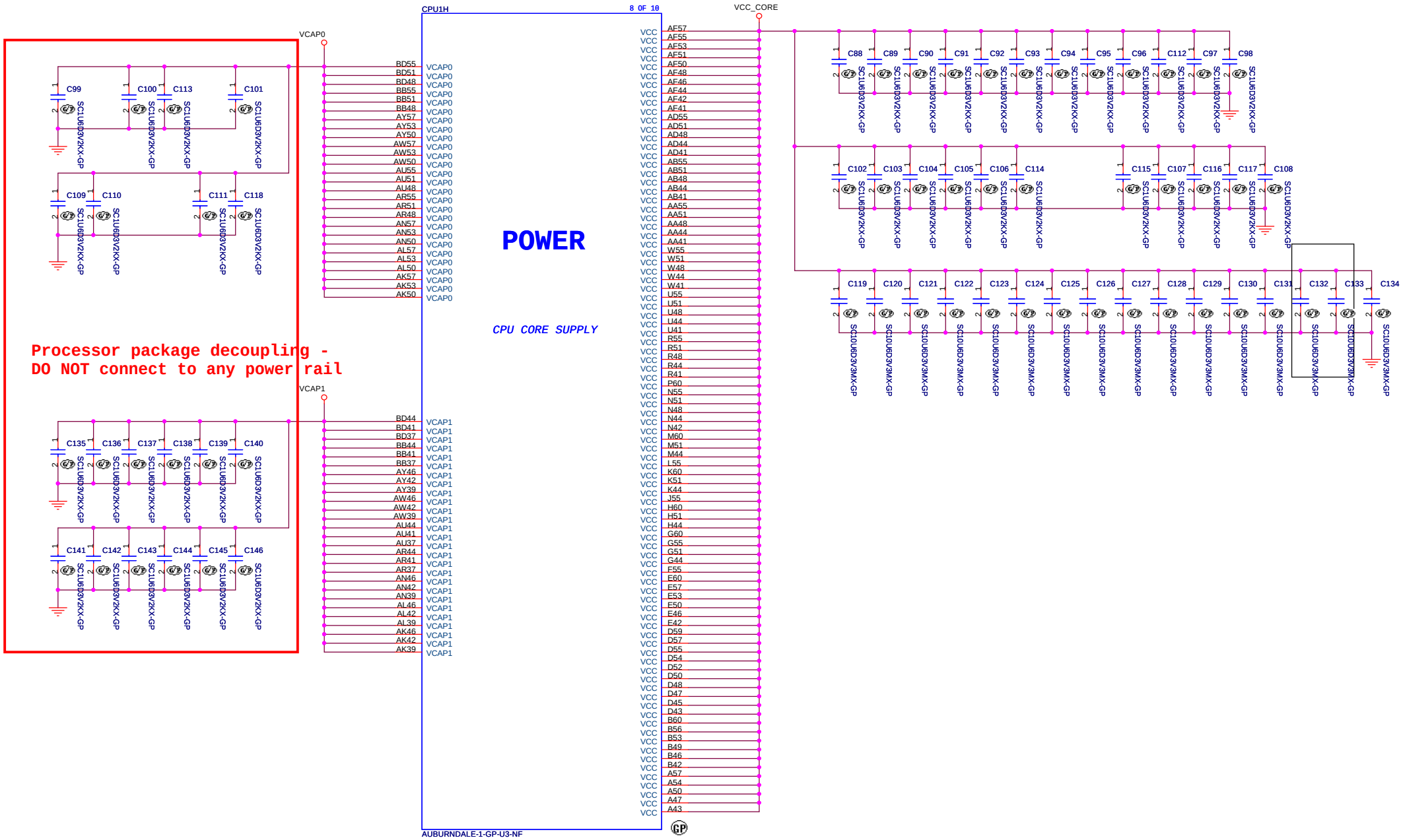
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU SFF 4 of 8(POWER/VTT)		
Size: Custom	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 7 of 56	



DVT 1ST

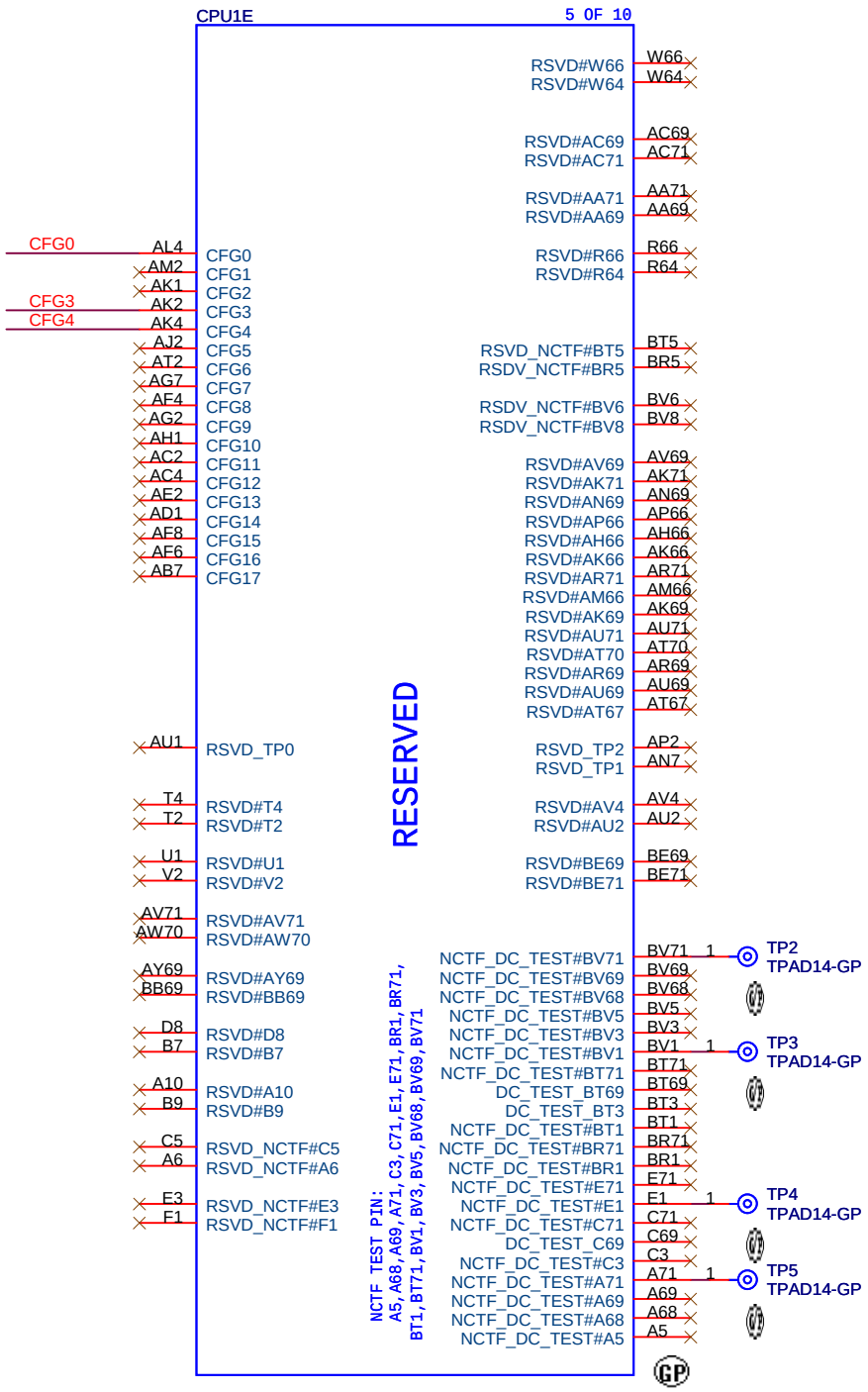
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

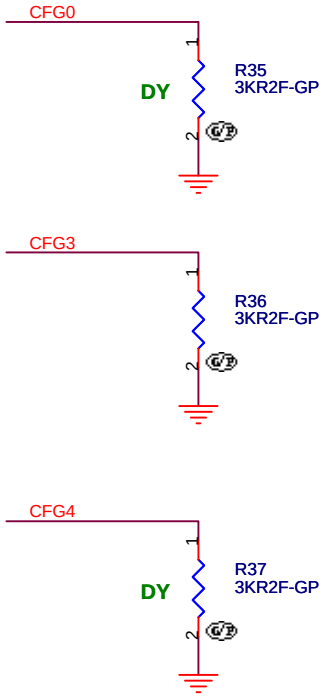
Title	CPU SFF 5 of 8(PWR/DDR/GFX/)	
Size A3	Document Number TUCANA	Rev SB
Date: Wednesday, July 07, 2010	Sheet 8 of 56	



DVT 1ST

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CPU SFF 6 of 8(CPUCORE)**	
Size A3	Document Number **TUCANA**	Rev **SB**
Date: Wednesday, July 07, 2010	Sheet 9 of 56	





PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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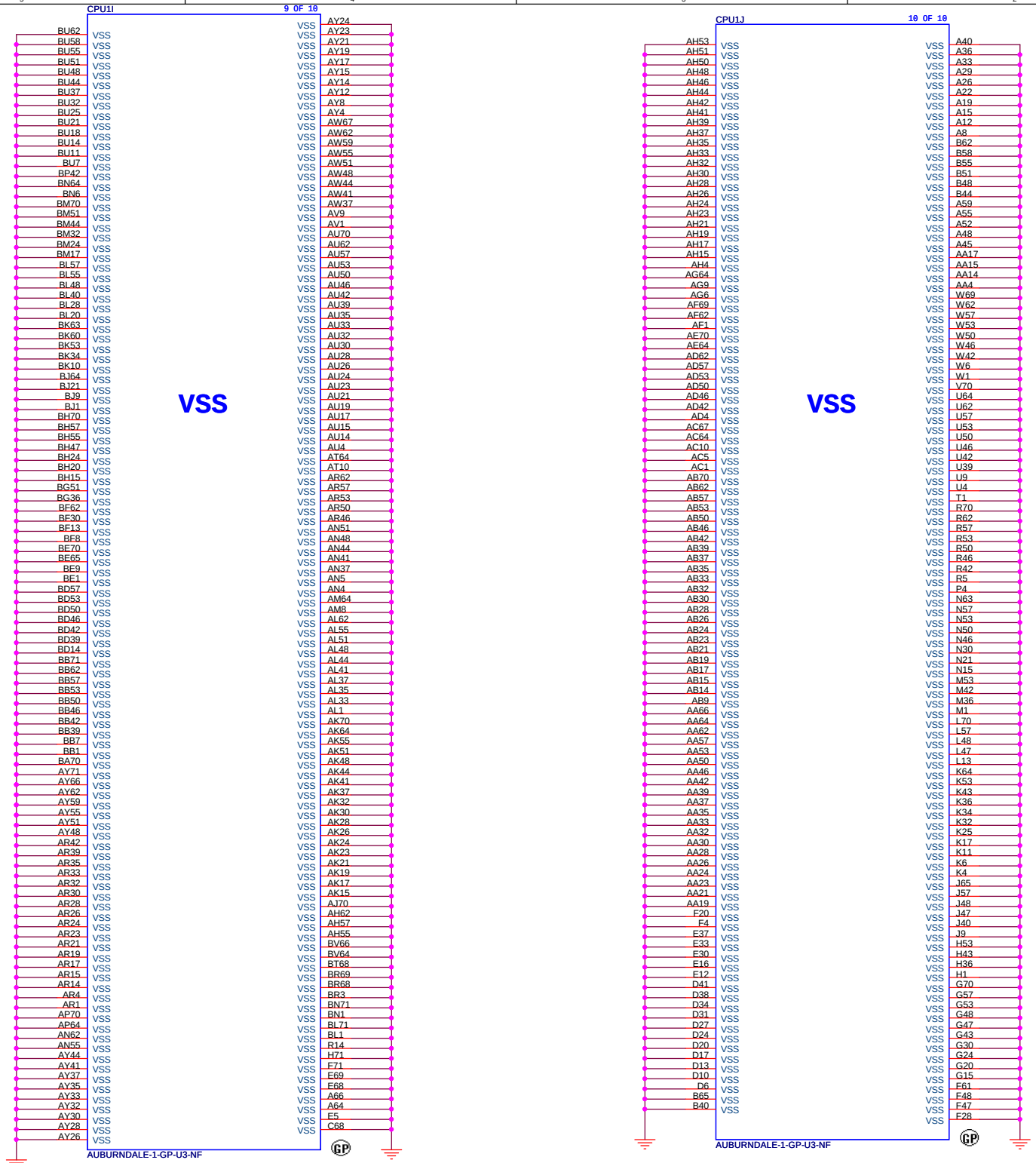
Title: **CPU SFF 7 of 8(RESERVED)**

Size	Document Number	Rev
A4	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 10 of 56



DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU SFF 8 of 8(VSS)		
Size A3	Document Number TUCANA		Rev SB
Date: Wednesday, July 07, 2010	Sheet 11 of 56		

integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

RTC_X1
RTC_X2
R39 10MR2J-L-GP
R41 0R2J-2-GP
RTC_X2_1
X2 X-32D768KHZ-34GPU 82.30001.661
C147 SC5P50V2CN-2GP
C148 SC5P50V2CN-2GP

RTC_AUX_S5
R38 330KR2J-L-GP
INTVRMEN
SM_INTRUDER#
R40 1MR2J-1-GP

RN6 SRN33J-7-GP
31,32 ACZ_RST#
31 ACZ_BITCLK
31 ACZ_SYNC
31 ACZ_SDATAOUT
ACZ_RST#_1
ACZ_BIT_CLK_1
ACZ_SYNC_1
ACZ_SDATAOUT_1

ACZ_BIT_CLK_1
PCH_SPI_CLK
EC1 DY SC22P50V2JN-4GP
EC2 DY SC22P50V2JN-4GP

PCH_JTAG_TCK
R48 51R2F-2-GP

RN7 SRN0J-7-GP
39 PCH_SPI_CS#0
39 PCH_SPI_MOSI
39 PCH_SPI_CLK
SPI_CS#0_R
SPI_MOSI_R
SPI_CLK_R

1D8V_S0 1D5V_S0
R52 DY 10KR2J-3-GP
R53 DY 10KR2J-3-GP
R54 DY 10KR2J-3-GP
ACZ_SYNC_1

If reserve 1.5/1.8V option for VCCVRM.Not Power plan change only.
Please refer figure2.HDA_SYNC will be strap to define VCCVRM is 1.5 or 1.8V source.
Means need have Pull high/low resistor to option,
P/H voltage base on HAD Link is 1.5V or 3.3V(Figure 3).

RTC_AUX_S5
RN5 SRN20KJ-GP
ICH_RTCRST#
SRTCRST#
SM_INTRUDER#
INTVRMEN
C149 SC1U10V2KX-1GP
G1 GAP-OPEN
C150 SC1U10V2KX-1GP

PCH1A 1 OF 10

RTC_X1	B13	RTCX1	
RTC_X2	D13	RTCX2	
ICH_RTCRST#	C14	RTCRST#	RTC
SRTCRST#	D17	SRTCRST#	RTC
SM_INTRUDER#	A16	INTRUDER#	RTC
INTVRMEN	A14	INTVRMEN	RTC
ACZ_BIT_CLK_1	A30	HDA_BCLK	IHDA
ACZ_SYNC_1	D29	HDA_SYNC	IHDA
31 ACZ_SPKR	P1	SPKR	IHDA
ACZ_RST#_1	C30	HDA_RST#	IHDA
31 ACZ_SDATAIN0	G30	HDA_SDIN0	IHDA
	F30	HDA_SDIN1	IHDA
	E32	HDA_SDIN2	IHDA
	F32	HDA_SDIN3	IHDA
ACZ_SDATAOUT_1	B29	HDA_SDO	IHDA
38 ME_UNLOCK#	H32	HDA_DOCK_EN#/GPIO33	SATA
	J30	HDA_DOCK_RST#/GPIO13	SATA
PCH_JTAG_TCK	M3	JTAG_TCK	JTAG
PCH_JTAG_TMS	K3	JTAG_TMS	JTAG
PCH_JTAG_TDI	K1	JTAG_TDI	JTAG
PCH_JTAG_TDO	J2	JTAG_TDO	JTAG
PCH_JTAG_TRST#	J4	TRST#	JTAG
SPI_CLK_R	BA2	SPI_CLK	SPI
SPI_CS#0_R	AV3	SPI_CS0#	SPI
	AY3	SPI_CS1#	SPI
SPI_MOSI_R	AY1	SPI_MOSI	SPI
39 SPI_MISO_R	AV1	SPI_MISO	SPI

IBEXPEAK-M-GP-NF

When unused all JTAG pins may be NC
TPAD14-GP TP6
R47 100KR2J-1-GP
R49 DY 0R2J-2-GP
R51 DY 0R2J-2-GP

FWH0/LAD0	D33	LPC_LAD0_1 R42	LPC_LAD0 38,39
FWH1/LAD1	B33	LPC_LAD1_1 R43	LPC_LAD1 38,39
FWH2/LAD2	C32	LPC_LAD2_1 R44	LPC_LAD2 38,39
FWH3/LAD3	A32	LPC_LAD3_1 R45	LPC_LAD3 38,39
FWH4/LFRAME#	C34	LPC_LFRAME#_1 R46	LPC_LFRAME# 38,39
LDRQ0#	A34		
LDRQ1#/GPIO23	F34		
SERIRQ	AB9		INT_SERIRQ 38

HDD

SATA0RXN	AK7	SATA_RXN0 26
SATA0RXP	AK6	SATA_RXP0 26
SATA0TXN	AK11	SATA_TXN0 26
SATA0TXP	AK9	SATA_TXP0 26
SATA1RXN	AH6	
SATA1RXP	AH5	
SATA1TXN	AH9	
SATA1TXP	AH8	
SATA2RXN	AF11	
SATA2RXP	AF9	
SATA2TXN	AF7	
SATA2TXP	AF6	
SATA3RXN	AH3	
SATA3RXP	AH1	
SATA3TXN	AF3	
SATA3TXP	AF1	
SATA4RXN	AD9	
SATA4RXP	AD8	
SATA4TXN	AD6	
SATA4TXP	AD5	
SATA5RXN	AD3	
SATA5RXP	AD1	
SATA5TXN	AB3	
SATA5TXP	AB1	
SATAICOMPO	AF16	SATAICOMP R50 37D4R2F-GP 1D05V_S0
SATAICOMPI	AF15	
SATALED#	T3	HDD_LED# 13,43
SATA0GP/GPIO21	Y9	SATA_DET#0_R
SATA1GP/GPIO19	V1	SATA_DET#1_R 17

SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"

3D3V_S0
RN8 SRN10KJ-5-GP
SATA_DET#0_R
INT_SERIRQ

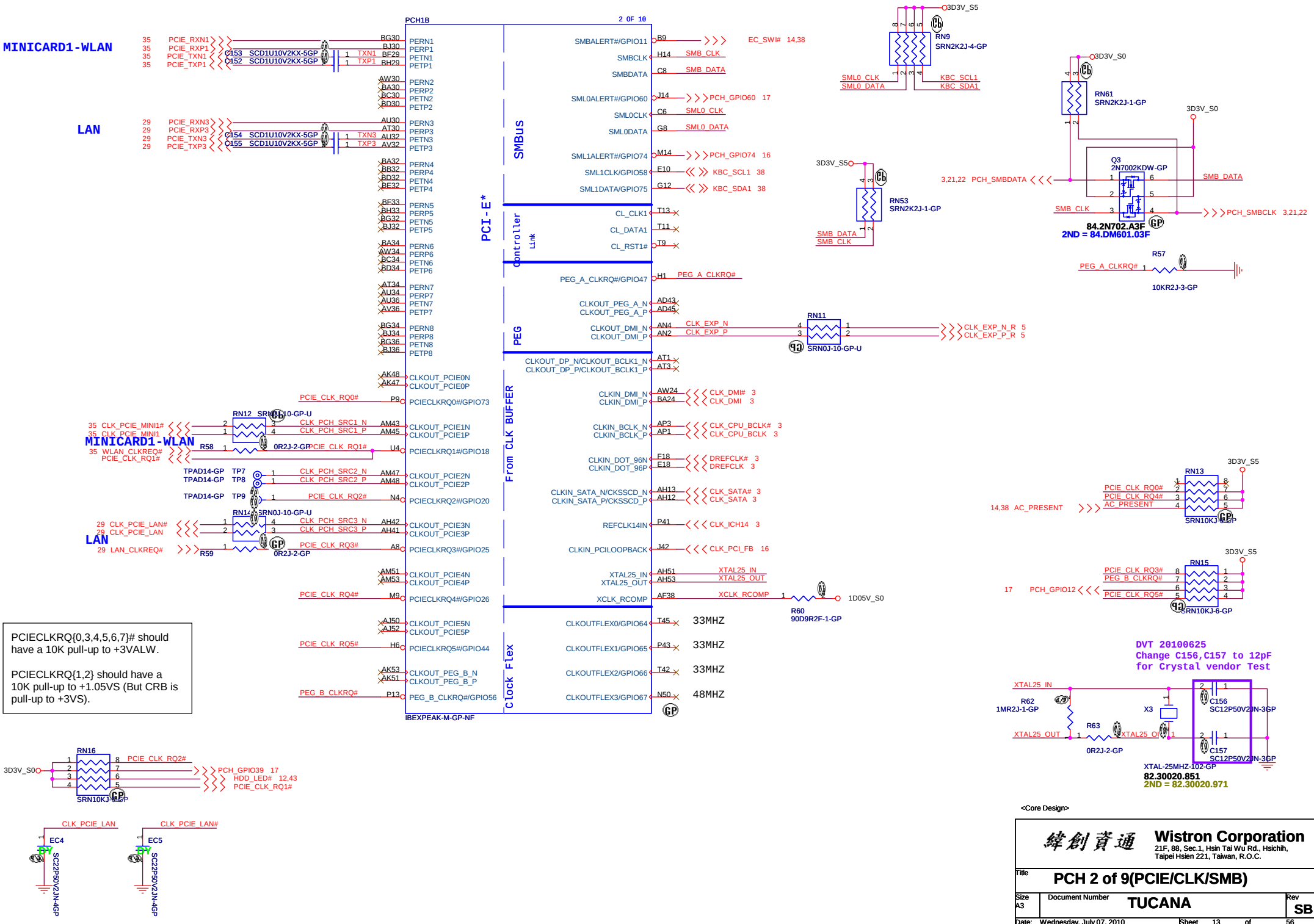
DVT 20100630
RTC_AUX_S5
3D3V_AUX_S5
C151 SC1U10V2KX-1GP
D1 BAT54GP-GP-U
83.R2003.I81
2ND = 83.BAT54.D81

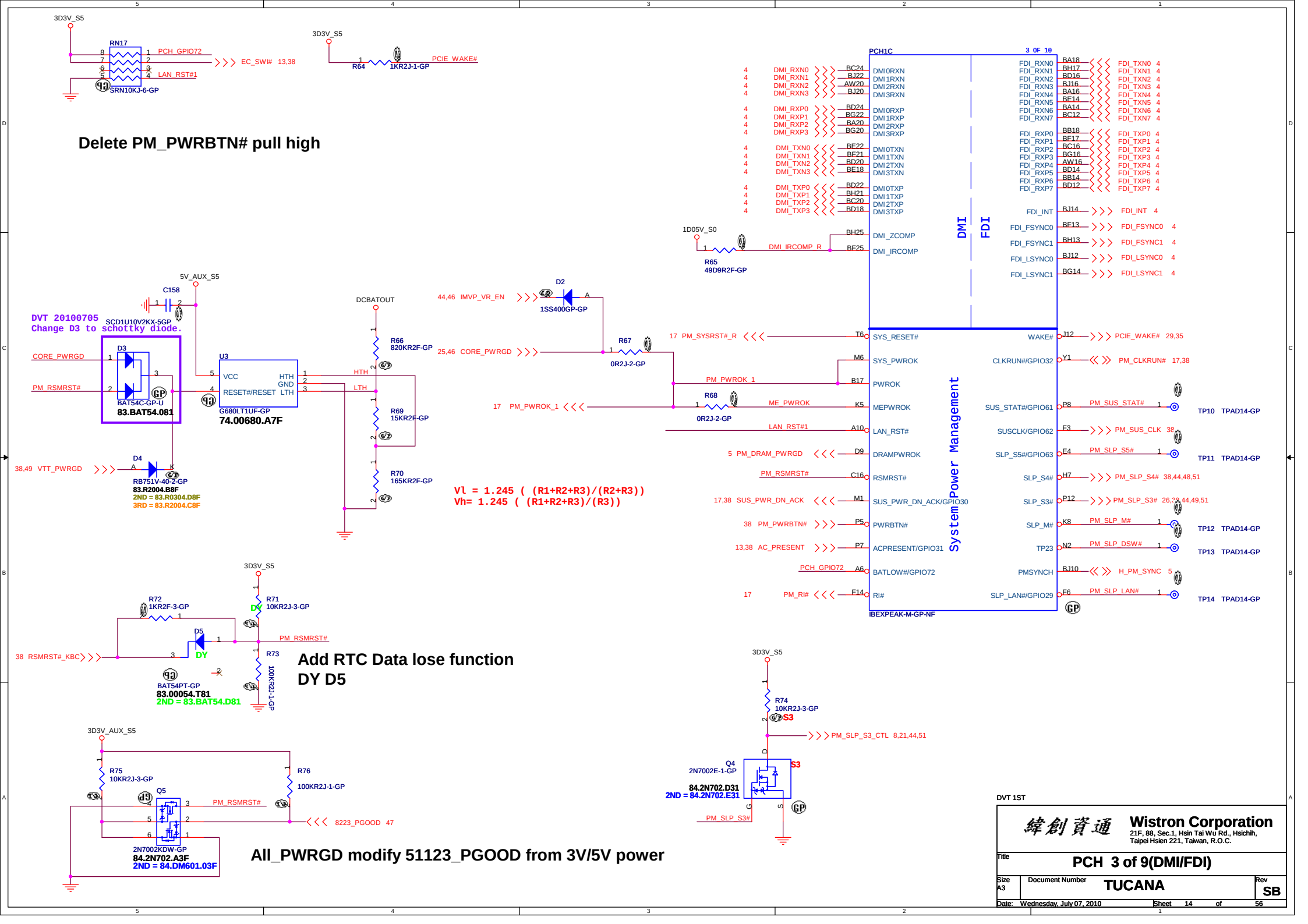
RTC CONN
RTC_AUX_S5
R55 510R2J-1-GP
RTC_BAT
R56 510R2J-1-GP
RTC_BAT_R
RTC1 ACES-CON2-11-GP
20.F0772.002
2ND = 20.F1729.002

DVT 1ST

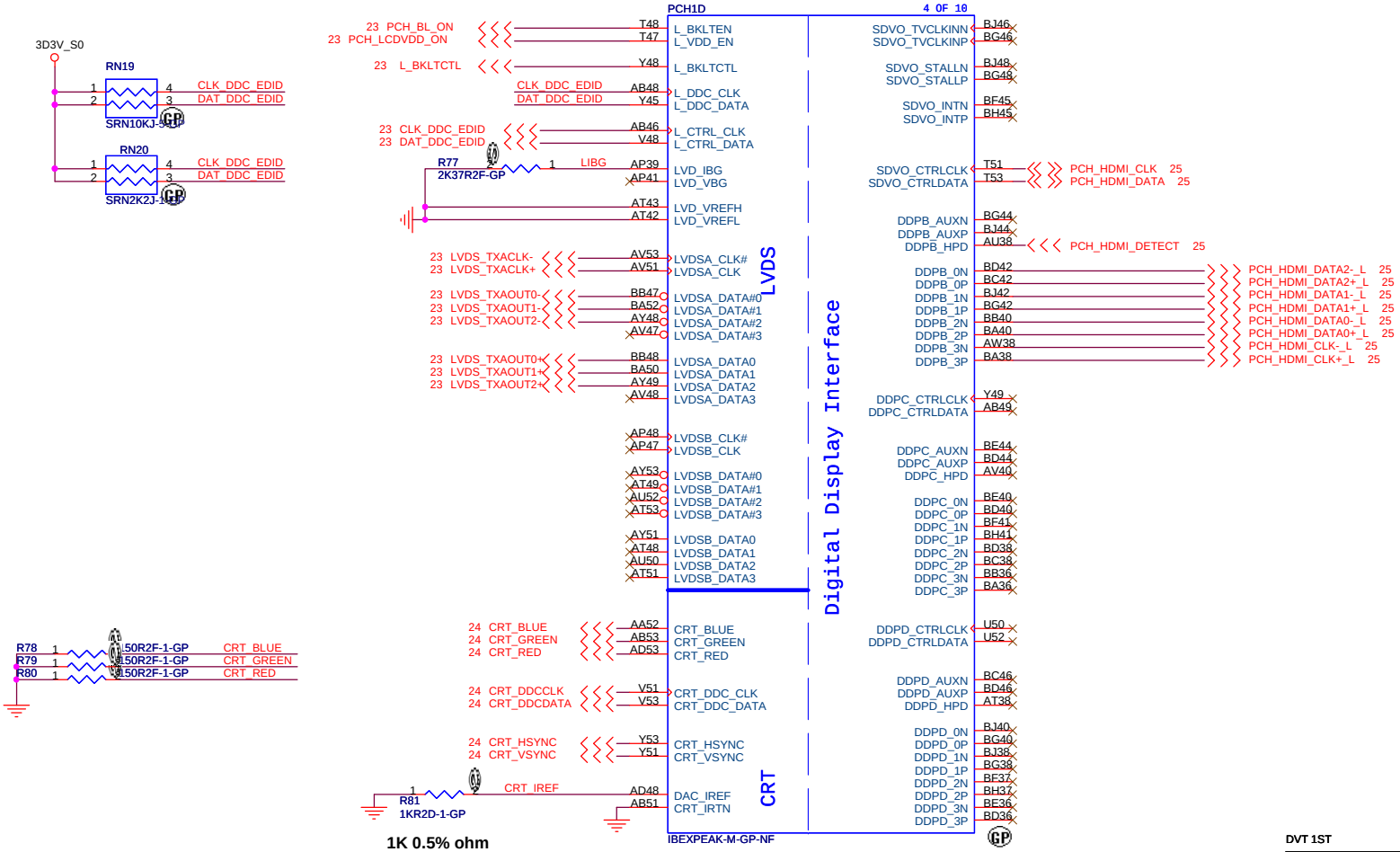
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH 1 of 9(SATA/RTC/HDA)
Size: A3 | Document Number: TUCANA | Rev: SB
Date: Wednesday, July 07, 2010 | Sheet 12 of 56


MINICARD1-WLAN
LAN
PCH1B
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M-GP-NF
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
DVT 20100625
Change C156,C157 to 12pF
for Crystal vendor Test
XTAL-25MHZ-102-GP
82.30020.851
2ND = 82.30020.971
84.2N702.A3F
2ND = 84.DM601.03F
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH 2 of 9(PCIE/CLK/SMB)
Size A3
Document Number
TUCANA
Rev SB
Date: Wednesday, July 07, 2010
Sheet 13 of 56


3D3V_S5
RN17
PCH_GPIO72
EC_SW# 13,38
LAN_RST#1
SRN10KJ-6-GP
3D3V_S5
R64
1KR2J-1-GP
PCIE_WAKE#
Delete PM_PWRBTN# pull high
PCH1C
3 OF 10
DMI0RXN
DMI1RXN
DMI2RXN
DMI3RXN
DMI0RXP
DMI1RXP
DMI2RXP
DMI3RXP
DMI0TXN
DMI1TXN
DMI2TXN
DMI3TXN
DMI0TXP
DMI1TXP
DMI2TXP
DMI3TXP
DMI_ZCOMP
DMI_IRCOMP
DMI
FDI
FDI_RXN0
FDI_RXN1
FDI_RXN2
FDI_RXN3
FDI_RXN4
FDI_RXN5
FDI_RXN6
FDI_RXN7
FDI_RXP0
FDI_RXP1
FDI_RXP2
FDI_RXP3
FDI_RXP4
FDI_RXP5
FDI_RXP6
FDI_RXP7
FDI_TXN0
FDI_TXN1
FDI_TXN2
FDI_TXN3
FDI_TXN4
FDI_TXN5
FDI_TXN6
FDI_TXN7
FDI_TXP0
FDI_TXP1
FDI_TXP2
FDI_TXP3
FDI_TXP4
FDI_TXP5
FDI_TXP6
FDI_TXP7
FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1
1D05V_S0
DMI_IRCOMP_R
R65
49D9R2F-GP
5V_AUX_S5
C158
SCD1U10V2KX-5GP
DVT 20100705
Change D3 to schottky diode.
D3
CORE_PWRGD
PM_RSMRST#
BAT54C-GP-U
83.BAT54.081
U3
VCC
RESET#/RESET
HTH
GND
LTH
G680LT1UF-GP
74.00680.A7F
DCBATOUT
R66
820KR2F-GP
R69
15KR2F-GP
R70
165KR2F-GP
HTH
LTH
D4
38,49 VTT_PWRGD
RB751V-40-2-GP
83.R2004.B8F
2ND = 83.R0304.D8F
3RD = 83.R2004.C8F
D2
44,46 IMVP_VR_EN
1SS400GP-GP
R67
25,46 CORE_PWRGD
0R2J-2-GP
17 PM_SYSRST#_R
PM_PWROK_1
17 PM_PWROK_1
R68
ME_PWROK
0R2J-2-GP
LAN_RST#1
5 PM_DRAM_PWRGD
PM_RSMRST#
17,38 SUS_PWR_DN_ACK
38 PM_PWRBTN#
13,38 AC_PRESENT
PCH_GPIO72
17 PM_RI#
SYS_RESET#
SYS_PWROK
PWROK
MEPWROK
LAN_RST#
DRAMPWROK
RSMRST#
SUS_PWR_DN_ACK/GPIO30
PWRBTN#
ACPRESENT/GPIO31
BATLOW#/GPIO72
RI#
IBEXPEAK-M-GP-NF
System Power Management
WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_M#
TP23
PMSYNCH
SLP_LAN#/GPIO29
PCIE_WAKE# 29,35
PM_CLKRUN# 17,38
PM_SUS_STAT#
TP10 TPAD14-GP
PM_SUS_CLK 38
PM_SLP_S5#
TP11 TPAD14-GP
PM_SLP_S4# 38,44,48,51
PM_SLP_S3# 26,38,44,49,51
PM_SLP_M#
TP12 TPAD14-GP
PM_SLP_DSW#
TP13 TPAD14-GP
H_PM_SYNC 5
PM_SLP_LAN#
TP14 TPAD14-GP
Vl = 1.245 ((R1+R2+R3)/(R2+R3))
Vh= 1.245 ((R1+R2+R3)/(R3))
3D3V_S5
R72
1KR2F-3-GP
R71
10KR2J-3-GP
DY
D5
PM_RSMRST#
38 RSMRST#_KBC
R73
100KR2J-1-GP
BAT54PT-GP
83.00054.T81
2ND = 83.BAT54.D81
Add RTC Data lose function
DY D5
3D3V_S5
R74
10KR2J-3-GP
S3
PM_SLP_S3_CTL 8,21,44,51
Q4
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
PM_SLP_S3#
3D3V_AUX_S5
R75
10KR2J-3-GP
R76
100KR2J-1-GP
Q5
PM_RSMRST#
8223_PGOOD 47
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
All_PWRGD modify 51123_PGOOD from 3V/5V power
DVT 1ST
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH 3 of 9(DMI/FDI)
Size
A3
Document Number
TUCANA
Rev
SB
Date: Wednesday, July 07, 2010
Sheet 14 of 56

Panel backlight enable control for LVDS -
used to gate power into the backlight circuit



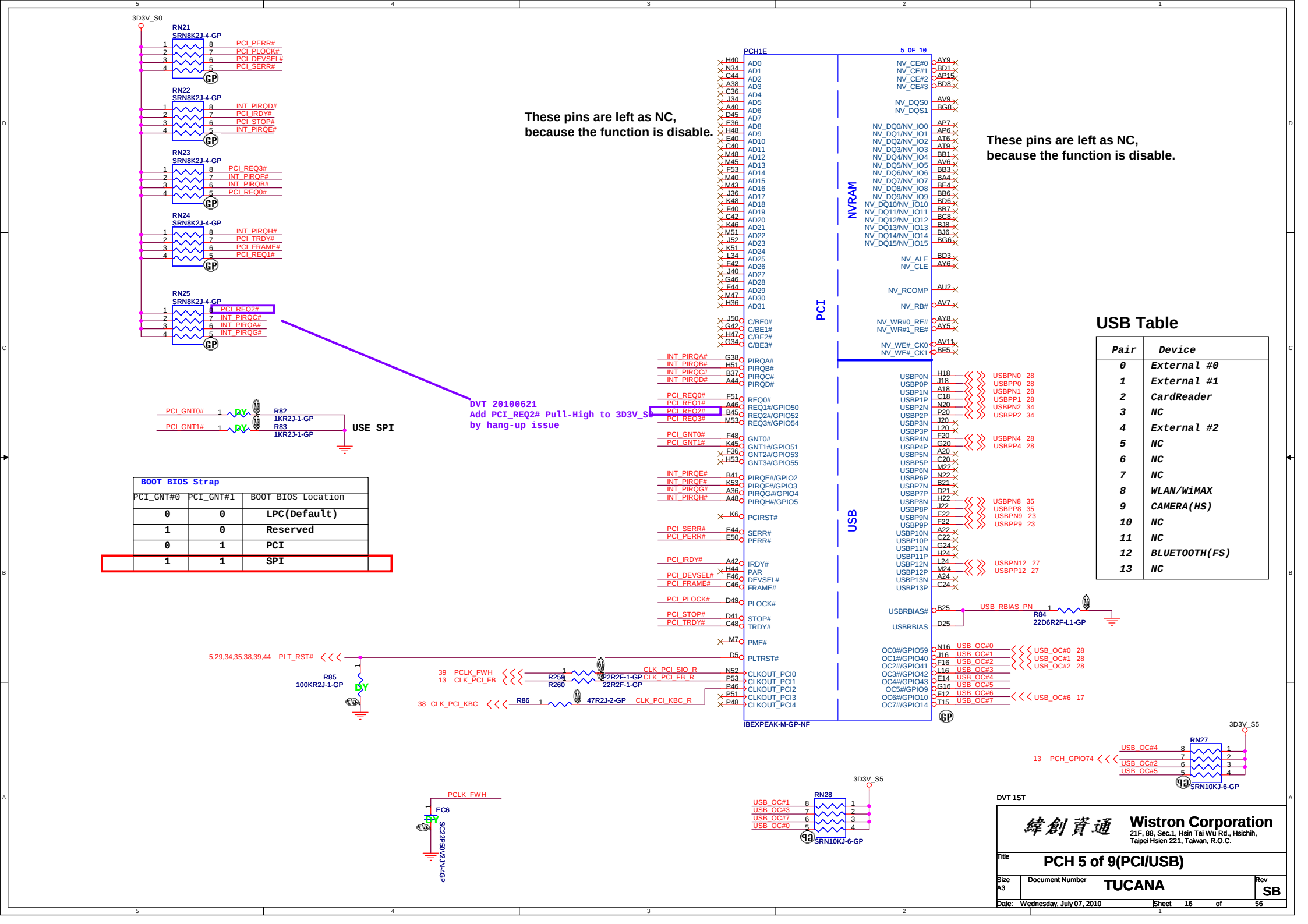
DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH 4 of 9(LVDS/CRT/DP)

Size: Custom | Document Number: TUCANA | Rev: SB

Date: Wednesday, July 07, 2010 | Sheet 15 of 56



USB Table

Pair	Device
0	External #0
1	External #1
2	CardReader
3	NC
4	External #2
5	NC
6	NC
7	NC
8	WLAN/WiMAX
9	CAMERA(HS)
10	NC
11	NC
12	BLUETOOTH(FS)
13	NC

DVT 1ST

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH 5 of 9(PCI/USB)

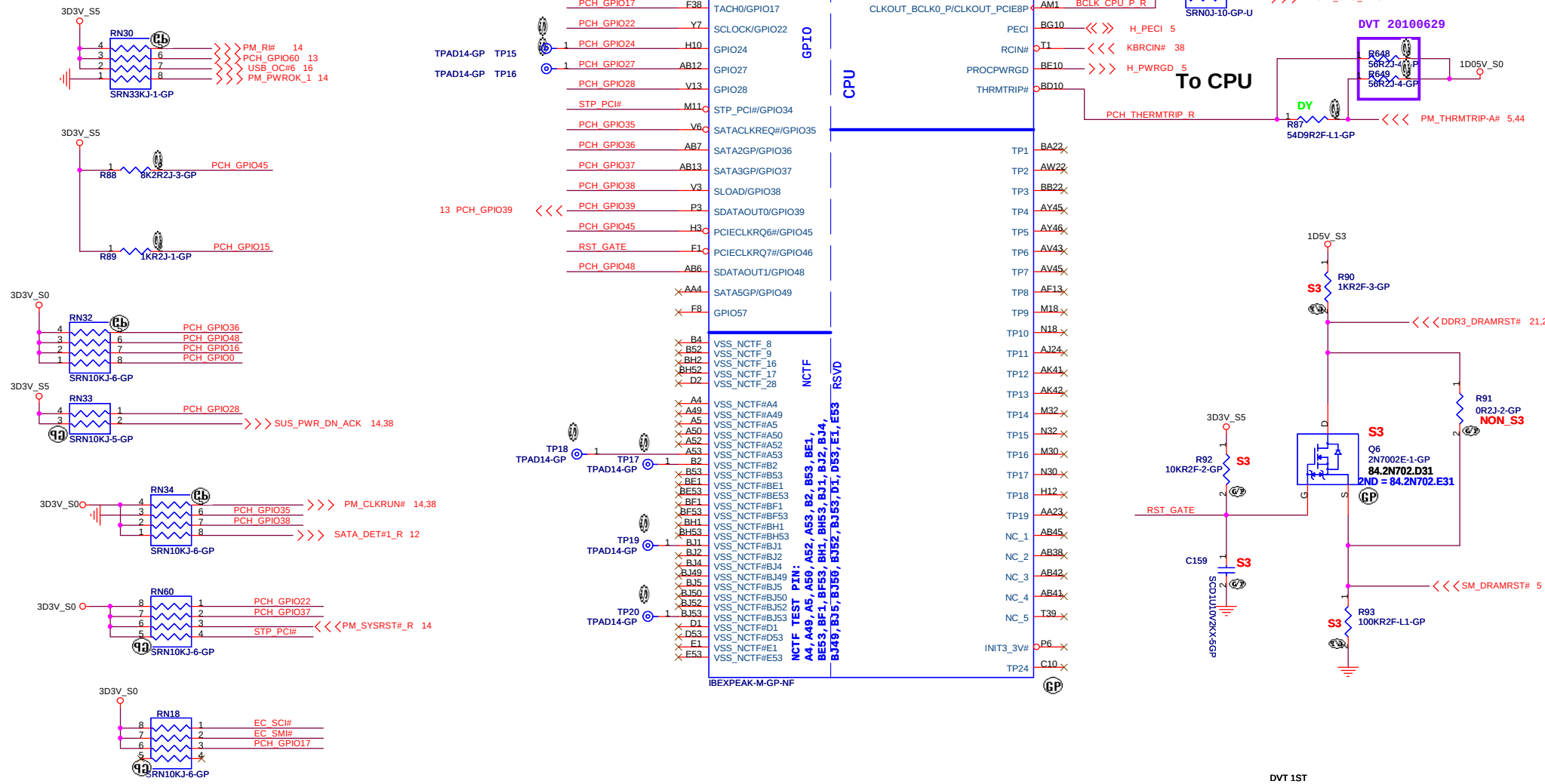
Size: A3 | Document Number: TUCANA | Rev: SB

Date: Wednesday, July 07, 2010 | Sheet 16 of 56

GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

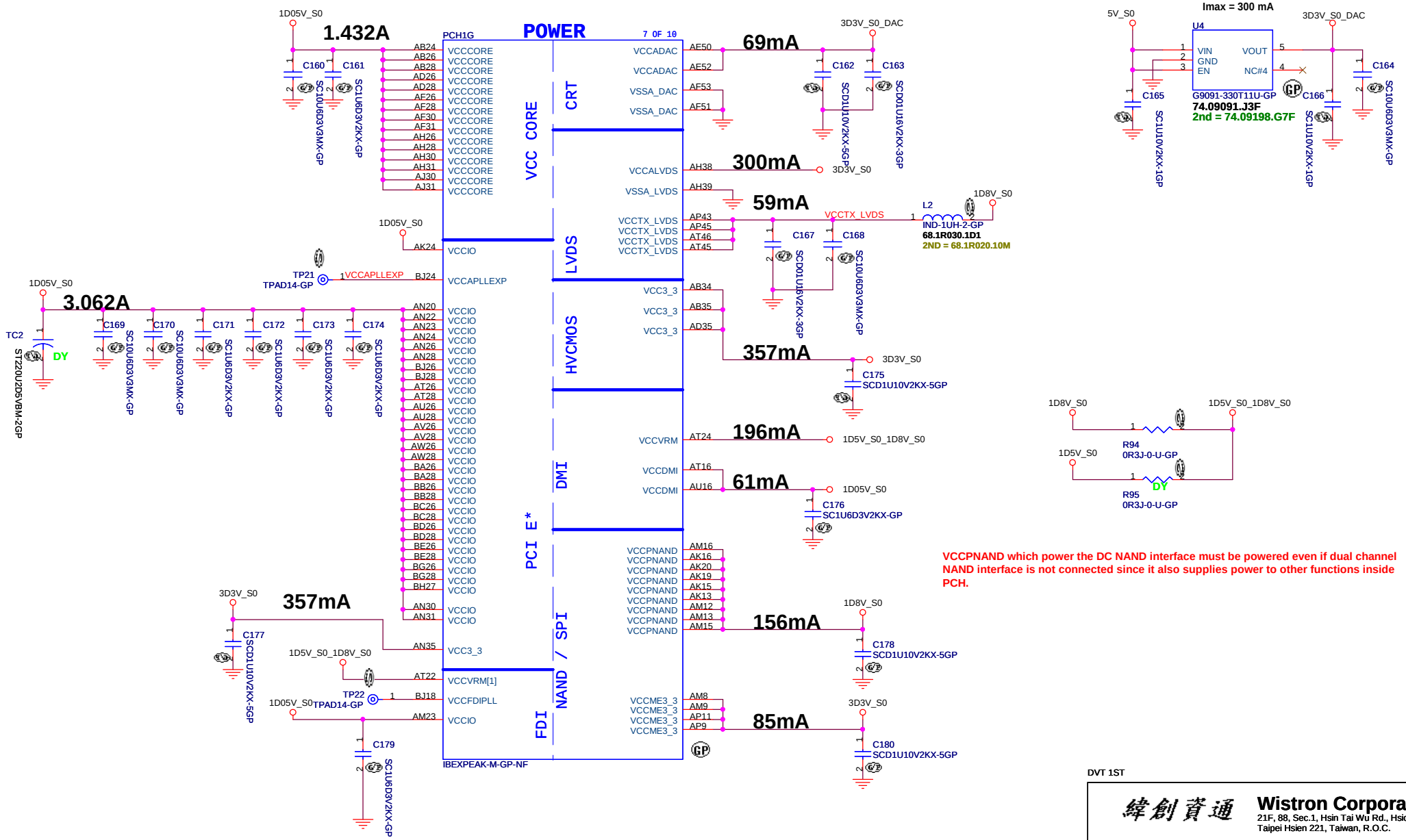
GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

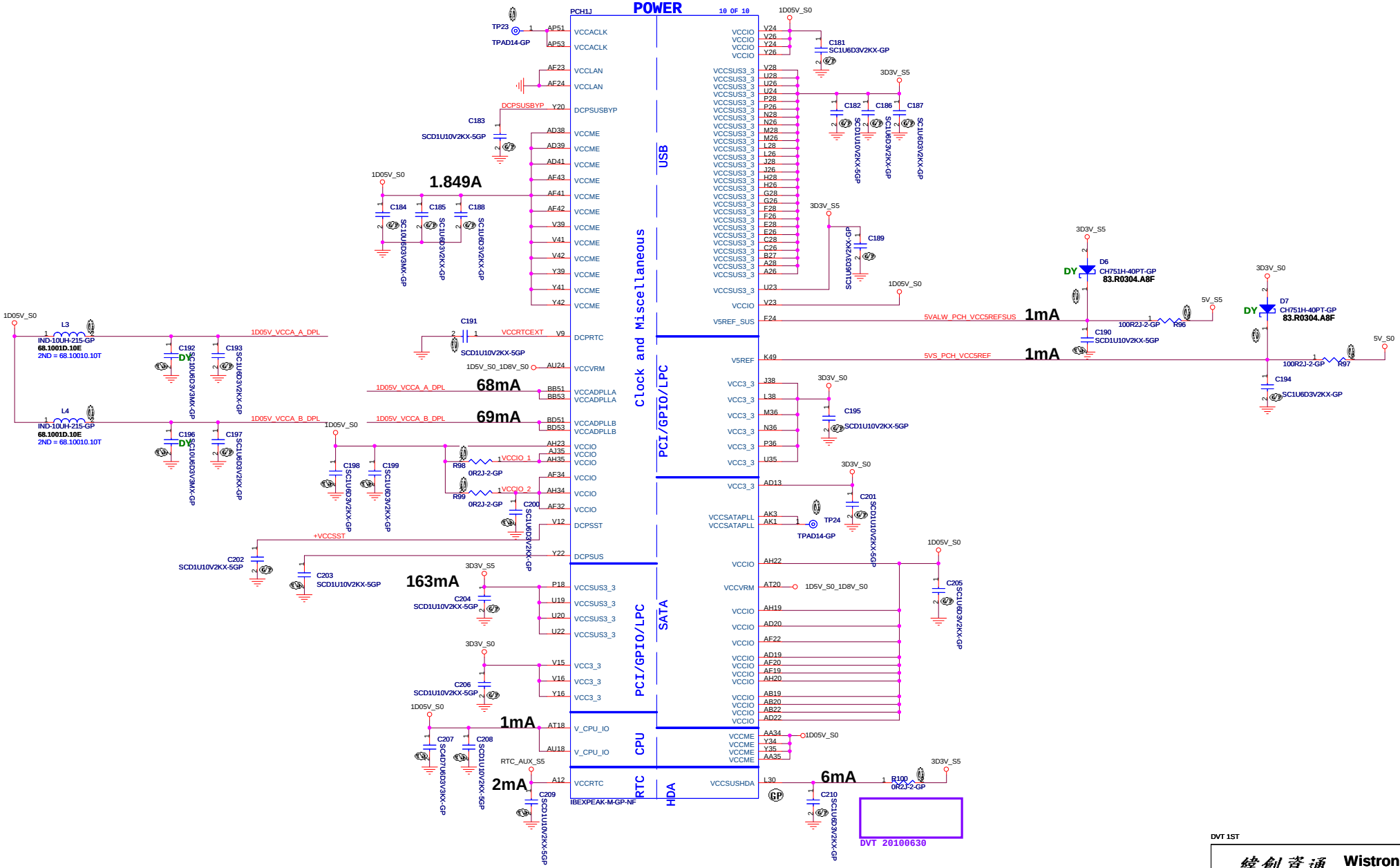
GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.



DVT 1ST

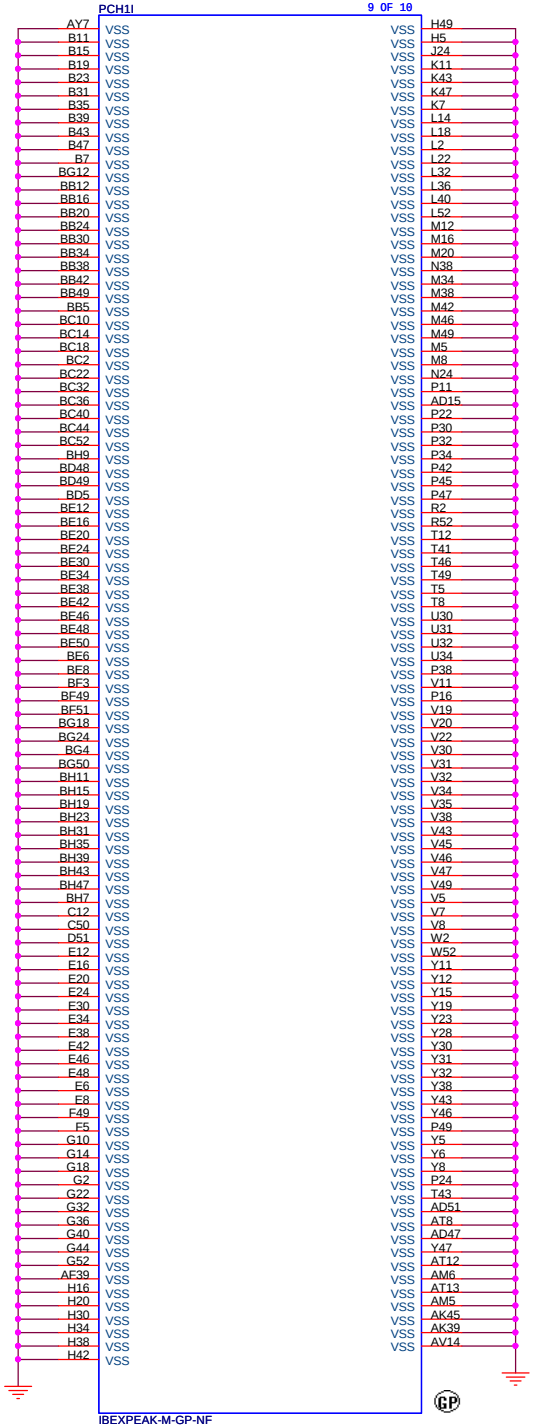
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH 6 of 9(GPIO/RSVD)		
Size: A3	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 17 of 56	

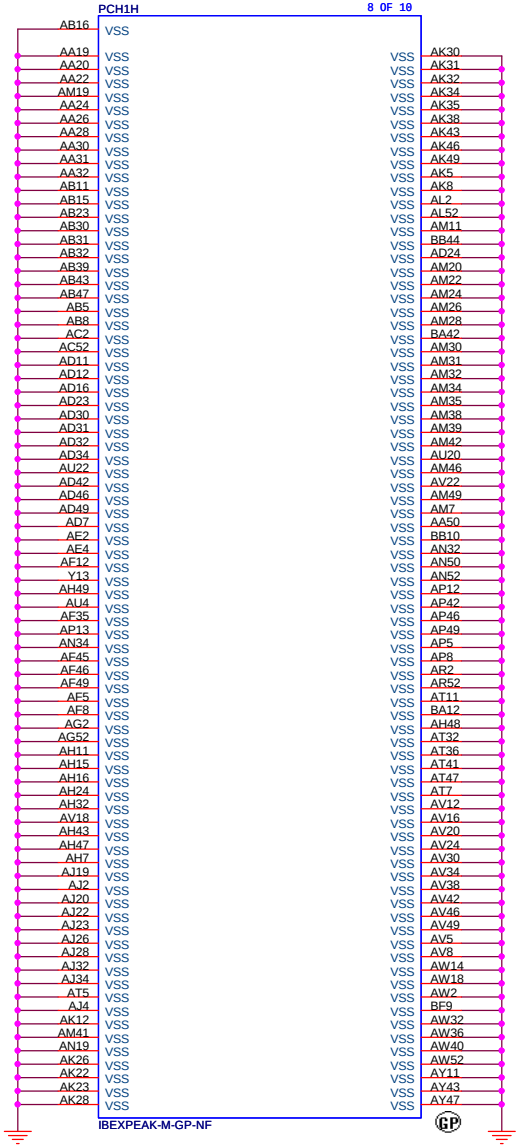

POWER
PCH1G
7 OF 10
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
1.432A
3.062A
357mA
69mA
300mA
59mA
357mA
196mA
61mA
156mA
85mA
1D05V_S0
3D3V_S0
3D3V_S0_DAC
1D8V_S0
1D05V_S0_1D8V_S0
5V_S0
Imax = 300 mA
U4
G9091-330T11U-GP
74.09091.J3F
2nd = 74.09198.G7F
L2
IND-1UH-2-GP
68.1R030.1D1
2ND = 68.1R020.10M
R94
R95
0R3J-0-U-GP
TC2
ST220U2D5VBM-2GP
TP21
TP22
TPAD14-GP
IBEXPEAK-M-GP-NF
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.
DVT 1ST
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH 7 of 9(PWR/VCORE/LVDS)
Size
Custom
Document Number
TUCANA
Rev
SB
Date: Wednesday, July 07, 2010
Sheet 18 of 56



DVT 1ST

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCH 8 of 9(PWR\SATA\USB)	
Size: Custom	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 19 of 56	





DVT 1ST

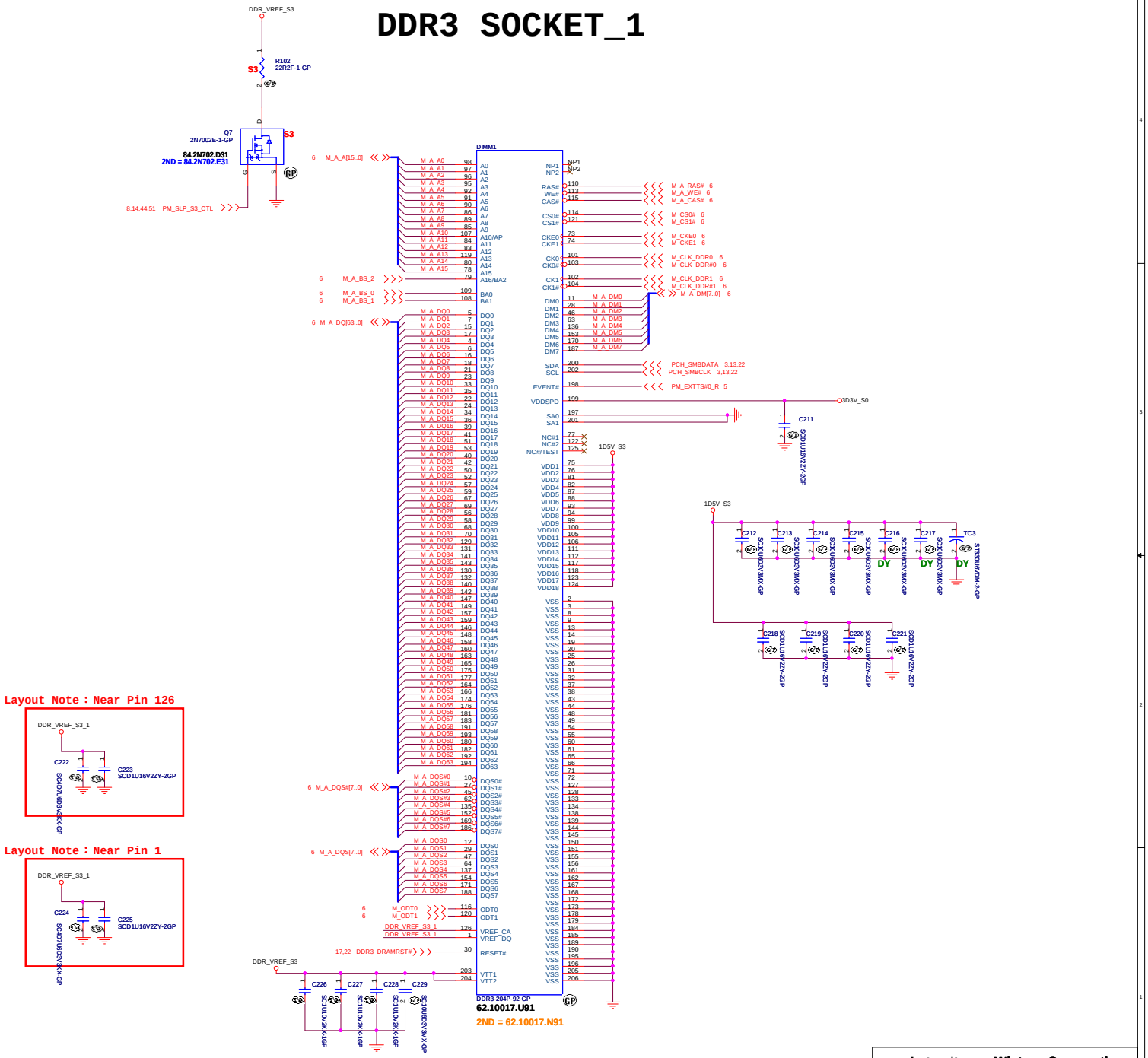
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH 9 of 9(VSS)**

Size	Document Number	Rev
A3	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 20 of 56

DDR3 SOCKET_1



Layout Note : Near Pin 126

Layout Note : Near Pin 1

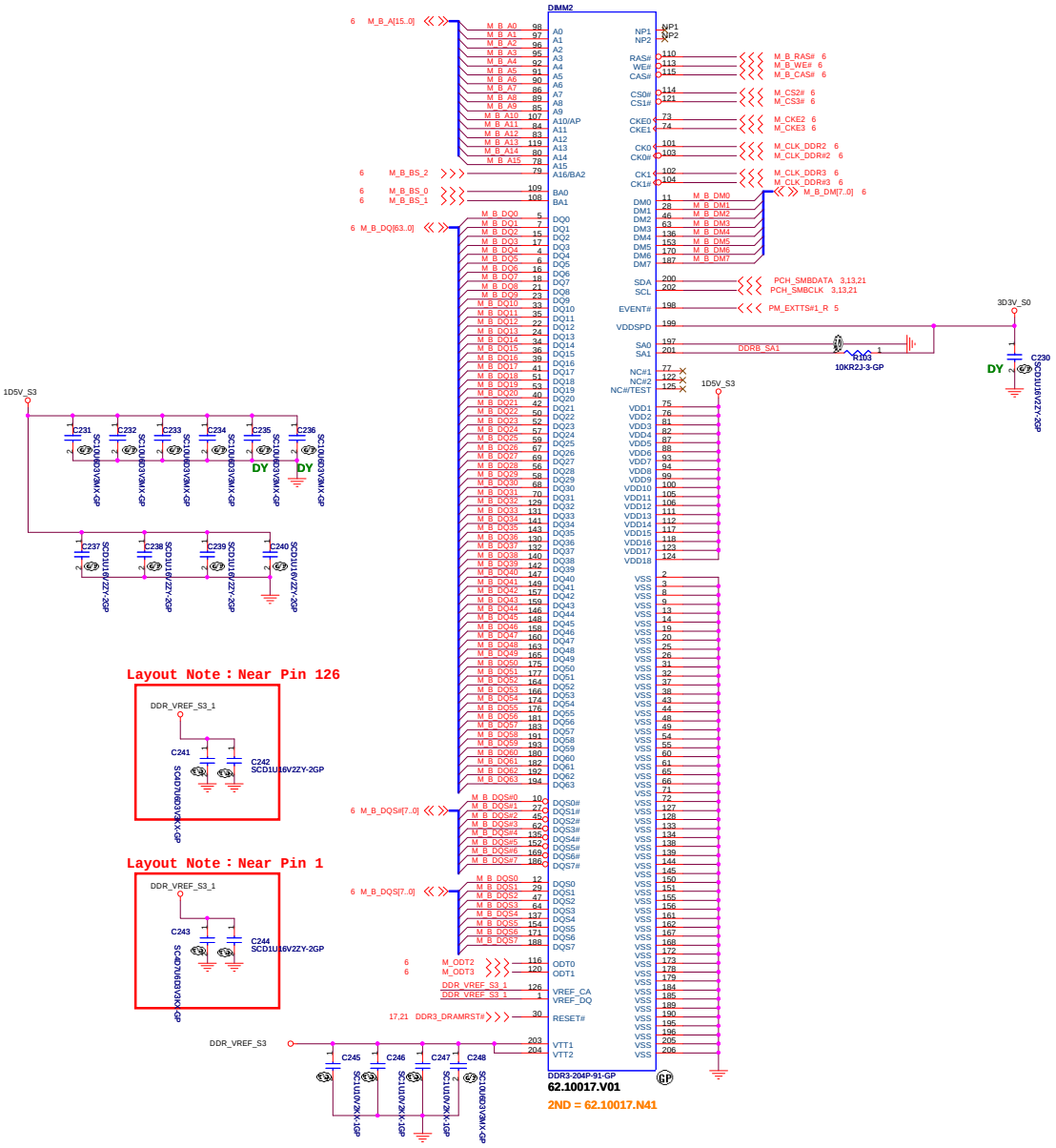
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3 Socket1***

Size	Document Number	Rev
	TUCANA	SB

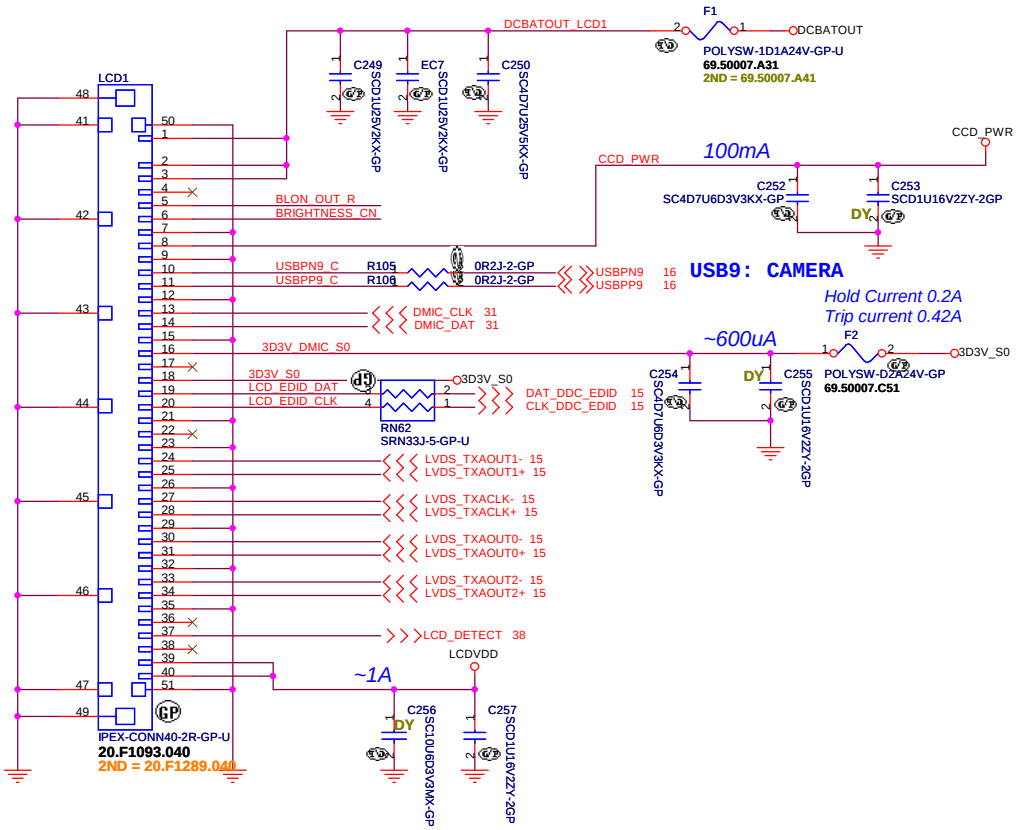
Date: Wednesday, July 07, 2010 Sheet 21 of 56

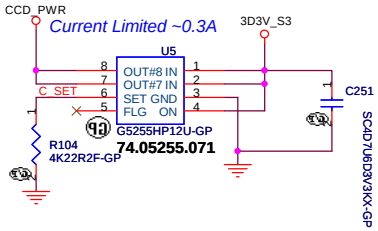
DDR3 SOCKET_2

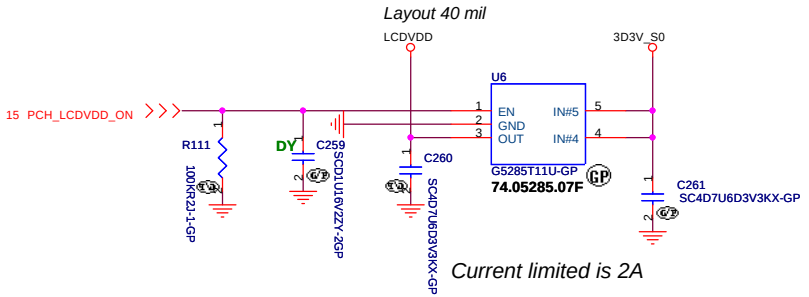


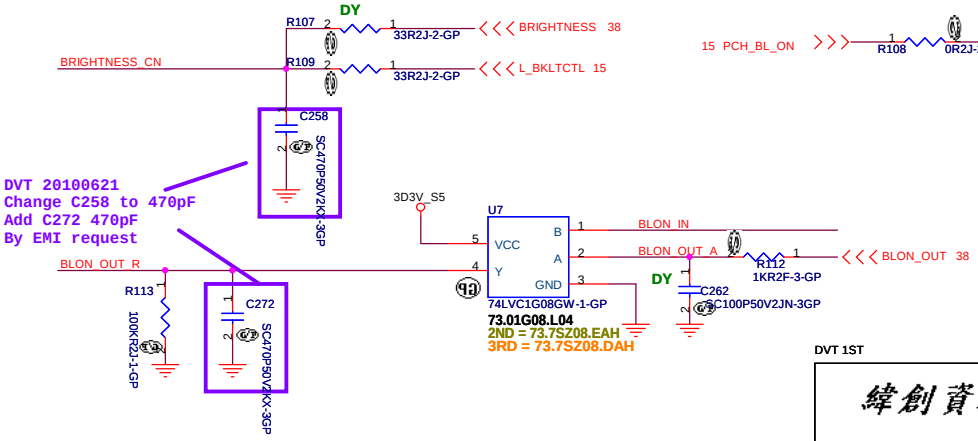
Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: DDR3 Socket2			
Size	Document Number	Rev	
	TUCANA	SB	
Date: Wednesday, July 07, 2010	Sheet 22 of 56		

LCD/CCD CONN









DVT 1ST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD CONN		
Size	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 23 of 56	

Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 40 ohm@100MHz

15 CRT_RED
15 CRT_GREEN
15 CRT_BLUE

CRT_RED
CRT_GREEN
CRT_BLUE

L5 SBK160808T-4[illegible]Y-N-GP
68.00119.241
2ND = 68.00909.151

L6 SBK160808T-4[illegible]Y-N-GP
68.00119.241
2ND = 68.00909.151

L7 SBK160808T-4[illegible]Y-N-GP
68.00119.241
2ND = 68.00909.151

CRT_R
CRT_G
CRT_B

R116 150R2F-1-GP
R117 150R2F-1-GP
R118 150R2F-1-GP

C264 SC5P50V2CN-2GP
C265 SC5P50V2CN-2GP
C266 SC5P50V2CN-2GP
C267 SC5P50V2CN-2GP
C268 SC5P50V2CN-2GP
C269 SC5P50V2CN-2GP

3D3V_S0
5V_S0
5V_CRT_S0

C263 SCD1U16V2ZY-2GP

U8
VCC_SYNC
VCC_VIDEO
VCC_DDC
VIDEO_1
VIDEO_2
VIDEO_3
BYP
DDC_IN1
DDC_IN2
DDC_OUT1
DDC_OUT2
SYNC_IN1
SYNC_IN2
SYNC_OUT1
SYNC_OUT2
GND
CM2009-02QR-GP
83.02009.BA0

C270 SC22U10V2KX-1GP

R114 2K7R2J-GP
R115 2K7R2J-GP

CLK_DDC1_5
DAT_DDC1_5

CRT_DDCCLK 15
CRT_DDCDATA 15
CRT_HSYNC 15
CRT_VSYNC 15

CRT_HSYNC1_R
CRT_VSYNC1_R
CRT_HSYNC1
CRT_VSYNC1

RN35 SRN33J-5-GP-U

DVT 20100621
Change R114,R115,R119,R120 to 2.7K ohm for CRT VEVS report

CRT_DDCCLK
CRT_DDCDATA
R119 2K7R2J-GP
R120 2K7R2J-GP

EC122 SCD01U50V2KX-1GP
EC123 SCD01U50V2KX-1GP

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR

6 1 7 2 8 3 9 4 10 5

EC8 SCD1U16V2ZY-2GP
EC9 SCD1U16V2ZY-2GP

CRT1
NC#4
NC#11
GND
GND
GND
GND
GND
GND
GND
GND
VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
D-SUB-15-76-GP
20.20891.015
2ND = 20.20886.015

~300mA

D8 CH551H-30PT-GP
83.R5003.C8F
2ND = 83.5R003.08F
3RD = 83.R5003.H8H

F6 POLYSW-40A60V-GP
69.44002.001

DVT 20100601
Change F6 to 69.44002.001, for Cadiz use

C273 SCD01U50V2KX-1GP

C274 DY SC18P50V2JN-1-GP
C275 DY SC18P50V2JN-1-GP
C276 DY SC18P50V2JN-1-GP
C277 DY SC18P50V2JN-1-GP

DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT CONN
Size: | Document Number: TUCANA | Rev: SB
Date: Wednesday, July 07, 2010 | Sheet 24 of 56

DVT 20100611
Change C283,C364 to 1uF
Change C282,C285 to 1KpF
for EMI request

3D3V_S0

C284 SCD1U16V2ZY-2GP
C285 SC1KP50V2KX-1GP
C286 SCD1U16V2ZY-2GP
C364 SC1U6D3V2KX-GP
C280 SCD1U16V2ZY-2GP
C281 SCD1U16V2ZY-2GP
C282 SC1KP50V2KX-1GP
C283 SC1U6D3V2KX-GP

VCC x8, NC#35, NC#34

15 PCH_HDMI_DATA0-_L
15 PCH_HDMI_DATA0+_L
C290 SCD1U10V2KX-5GP
C291 SCD1U10V2KX-5GP
HDMI_DATA0- 38
HDMI_DATA0+ 39
IN_D1-
IN_D1+

15 PCH_HDMI_CLK-_L
15 PCH_HDMI_CLK+_L
C288 SCD1U10V2KX-5GP
C289 SCD1U10V2KX-5GP
HDMI_CLK- 41
HDMI_CLK+ 42
IN_D2-
IN_D2+

15 PCH_HDMI_DATA1-_L
15 PCH_HDMI_DATA1+_L
C292 SCD1U10V2KX-5GP
C293 SCD1U10V2KX-5GP
HDMI_DATA1- 44
HDMI_DATA1+ 45
IN_D3-
IN_D3+

15 PCH_HDMI_DATA2-_L
15 PCH_HDMI_DATA2+_L
C294 SCD1U10V2KX-5GP
C295 SCD1U10V2KX-5GP
HDMI_DATA2- 47
HDMI_DATA2+ 48
IN_D4-
IN_D4+

OUT_D1- 23 HDMI_TX0-
OUT_D1+ 22 HDMI_TX0+
OUT_D2- 20 HDMI_TXC-
OUT_D2+ 19 HDMI_TXC+
OUT_D3- 17 HDMI_TX1-
OUT_D3+ 16 HDMI_TX1+
OUT_D4- 14 HDMI_TX2-
OUT_D4+ 13 HDMI_TX2+

Recommended Equalization: [PC1,PC0]=01, 4dB
3D3V_S0
R122 4K7R2J-2-GP DY
R121 5K1R2F-2-GP
R493 499R2F-2-GP
PC0 3
PC1 4
REXT_HDMI 6
RT_EN# 10
P8101_OE# 25
DDC_EN_PS8101 32
REXT
RT_EN#
OE#
DDC_EN

SDA 8
SCL 9
HPD 7
PCH_HDMI_DATA 15
PCH_HDMI_CLK 15
PCH_HDMI_DETECT 15
R123 100KR2J-1-GP

HPD_SINK 30 HDMI_HPD
SDA_SINK 29 TMDS_SDA
SCL_SINK 28 TMDS_SCL

GND x9

U73
PS8101-GP
71.P8101.003

HDMI in : Hi
HDMI out : Low

HDMI1
HDMI_TX2+_R
HDMI_TX2-_R
HDMI_TX1+_R
HDMI_TX1-_R
HDMI_TX0+_R
HDMI_TX0-_R
HDMI_TXC+_R
HDMI_TXC-_R
HDMI_A_CEC
TMDS_SCL
TMDS_SDA
HDMI_5V_S0_1_R
HDMI_HPD
NP1
NP2
SKT-HDMI25P-1-GP
22.10296.461

TP25 TPAD14-GP

3D3V_S0
R124 20KR2J-L2-GP
P8101_OE#
Q12 2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31

DVT 20100630
Change Q12 to 84.2N702.D31
(ESD Protected 1.0KV)

DVT 20100517
change 2nd source to 69.4R500.151

5V_S0
F4 FUSE-D5A6V-2-GP
69.4R500.141
2ND = 69.4R500.151
HDMI_5V_S0_1
Q59 AO3413-GP
84.03413.A31
2ND = 84.02130.031
HDMI_5V_S0_1_R
R620 10KR2J-3-GP
R621 10KR2J-3-GP
C278 SCD1U10V2KX-4GP
C279 SC1KP50V2KX-1GP
Q60 2N7002E-1-GP
84.2N702.D31
2nd = 84.2N702.E31
14,46 CORE_PWRGD

HDMI_5V_S0_1_R
D9 CH551H-30PT-GP
83.R5003.C8F
2ND = 83.5R003.08F
3RD = 83.R5003.H8H
RN36 SRN2K2J-1-GP
TMDS_SCL
TMDS_SDA

3D3V_S0
RN51 SRN2K2J-1-GP
PCH_HDMI_DATA
PCH_HDMI_CLK

3D3V_S0
R127 4K7R2J-2-GP PC0
R126 4K7R2J-2-GP DDC_EN_PS8101
R125 4K7R2J-2-GP RT_EN#

U9
HDMI_TX2-_R
HDMI_TX2+_R
R182 0R2J-2-GP
R215 0R2J-2-GP
HDMI_TX2-
HDMI_TX2+
FILTER-4P-14-GP
69.10118.051
2nd = 68.01210.20C
R614 200R2J-L1-GP

U11
HDMI_TX0-_R
HDMI_TX0+_R
R183 0R2J-2-GP
R222 0R2J-2-GP
HDMI_TX0-
HDMI_TX0+
FILTER-4P-14-GP
69.10118.051
2nd = 68.01210.20C
R615 200R2J-L1-GP

DVT 20100611
Change R614~R617 to 200R ohm
By EMI request

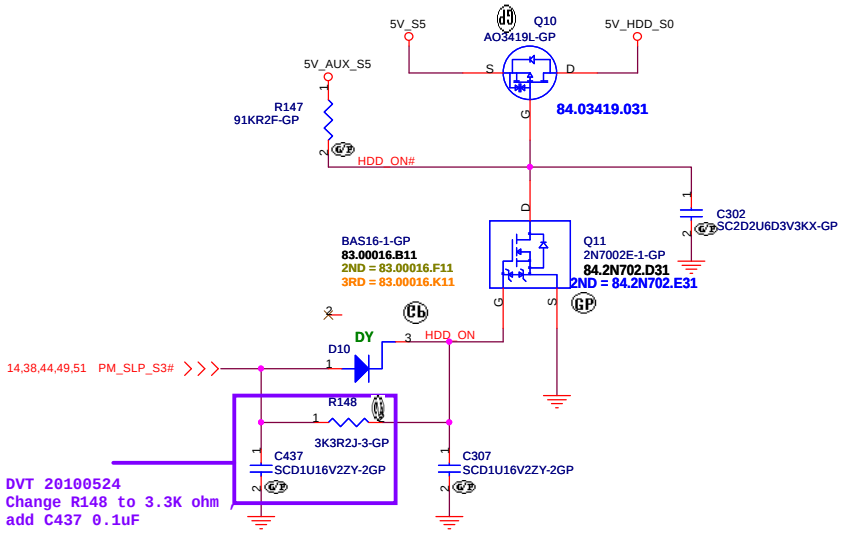
U10
HDMI_TX1-_R
HDMI_TX1+_R
R185 0R2J-2-GP
R223 0R2J-2-GP
HDMI_TX1-
HDMI_TX1+
FILTER-4P-14-GP
69.10118.051
2nd = 68.01210.20C
R616 200R2J-L1-GP

U12
HDMI_TXC-_R
HDMI_TXC+_R
R186 0R2J-2-GP
R241 0R2J-2-GP
HDMI_TXC-
HDMI_TXC+
FILTER-4P-14-GP
69.10118.051
2nd = 68.01210.20C
R617 200R2J-L1-GP

DVT 1ST

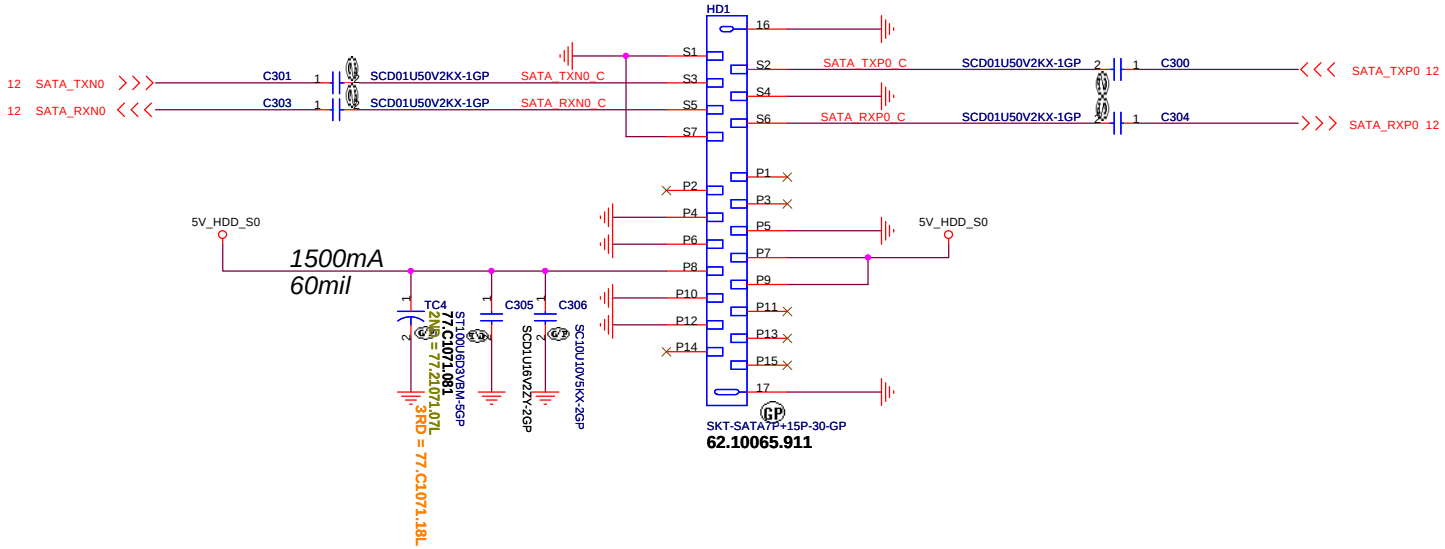
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI CONN
Size: | Document Number: TUCANA | Rev: SB
Date: Wednesday, July 07, 2010 | Sheet 25 of 56



Delay HDD power off timing for 400ms after SATA controller shut down. Control the C307 and R148 to finally tune delay timing between 500ms and 400ms.

SSD SATA Connector



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD Connector

Size	Document Number	Rev
	TUCANA	SB

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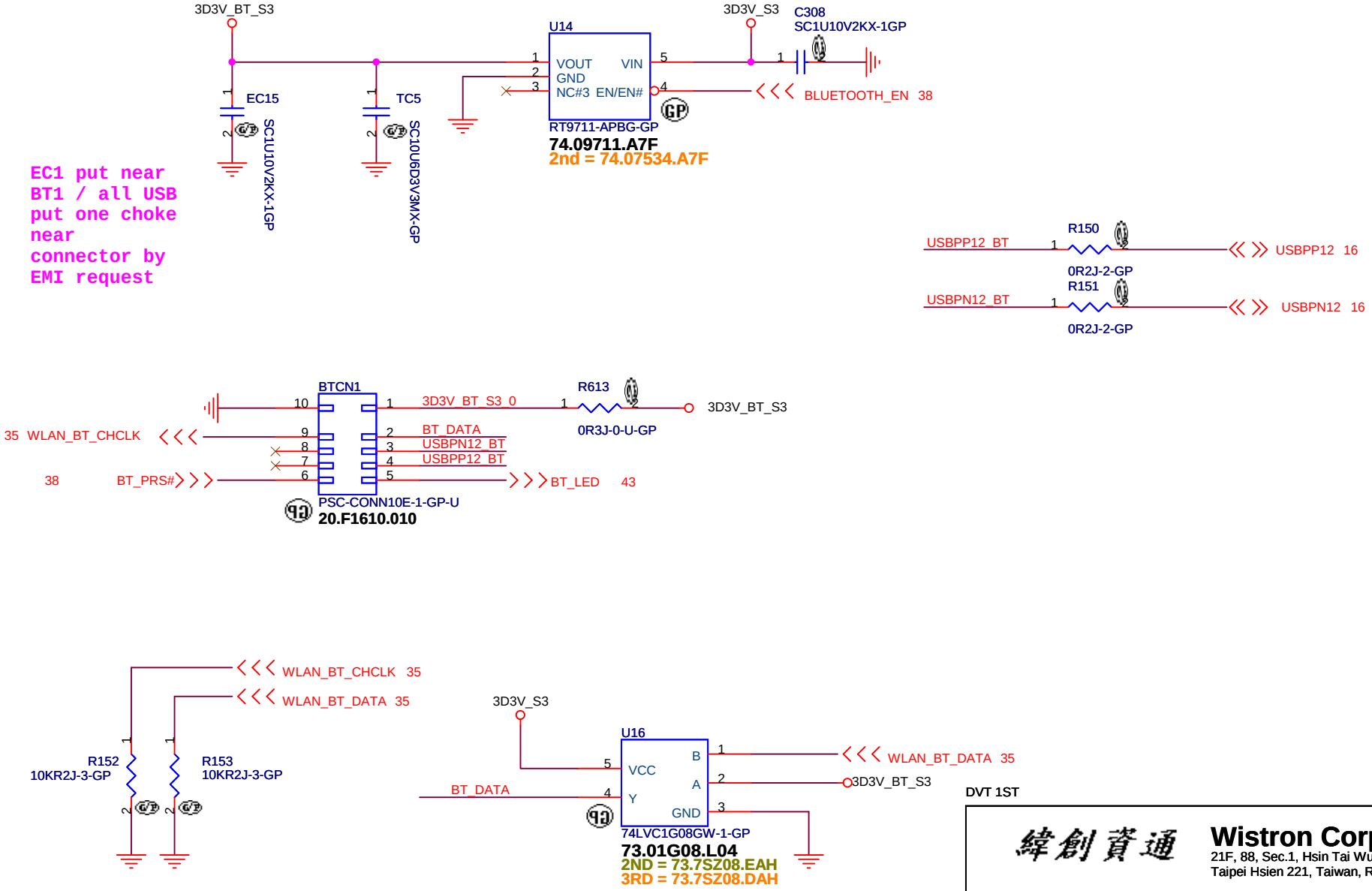
Bluetooth



DVT 1ST

緯創資通 **Wistron Corporation**
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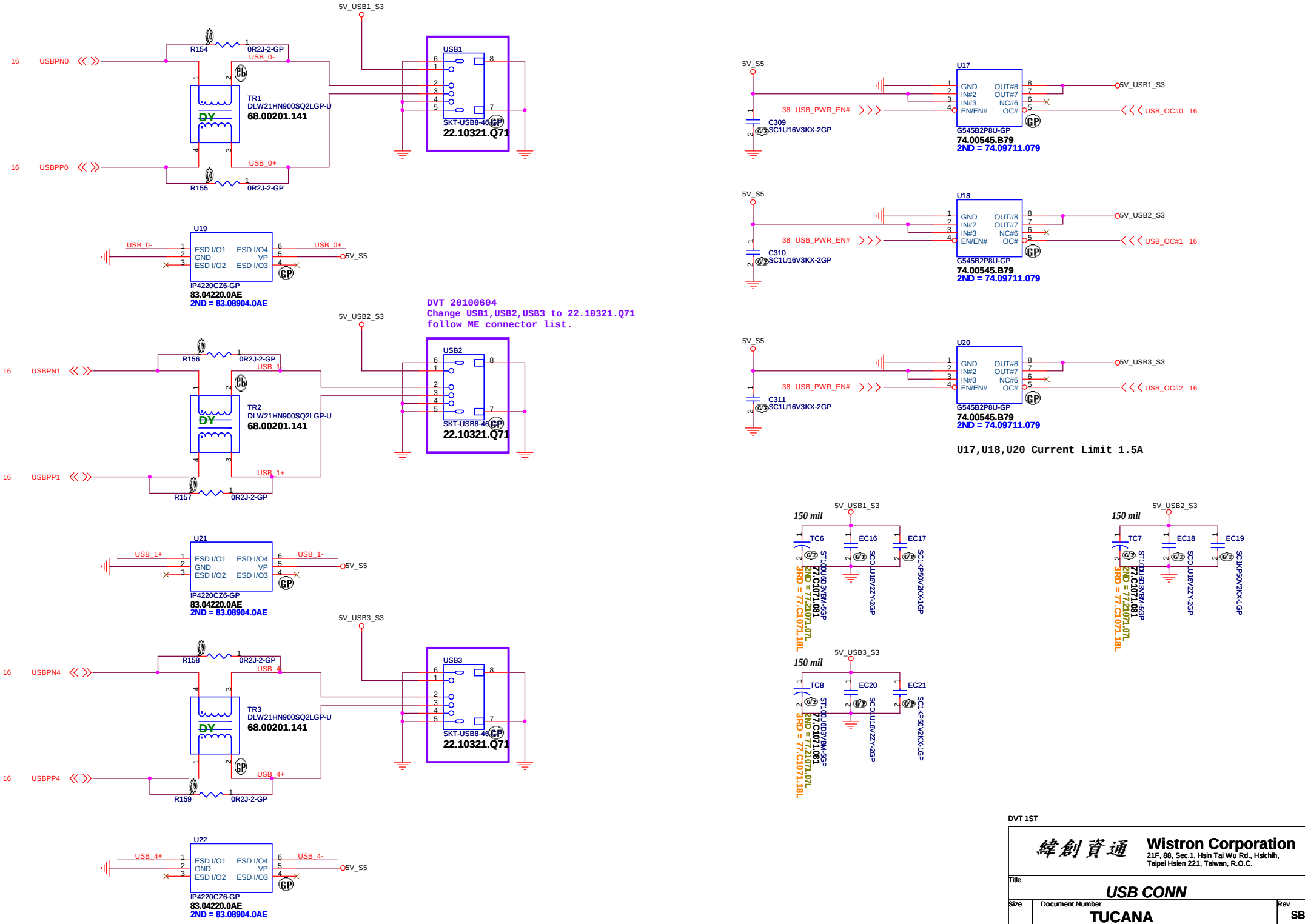
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Bluetooth***	
Size	Document Number **TUCANA**	Rev **SB**
Date: Wednesday, July 07, 2010	Sheet 27 of 56	



DVT 1ST

緯創資通 **Wistron Corporation**
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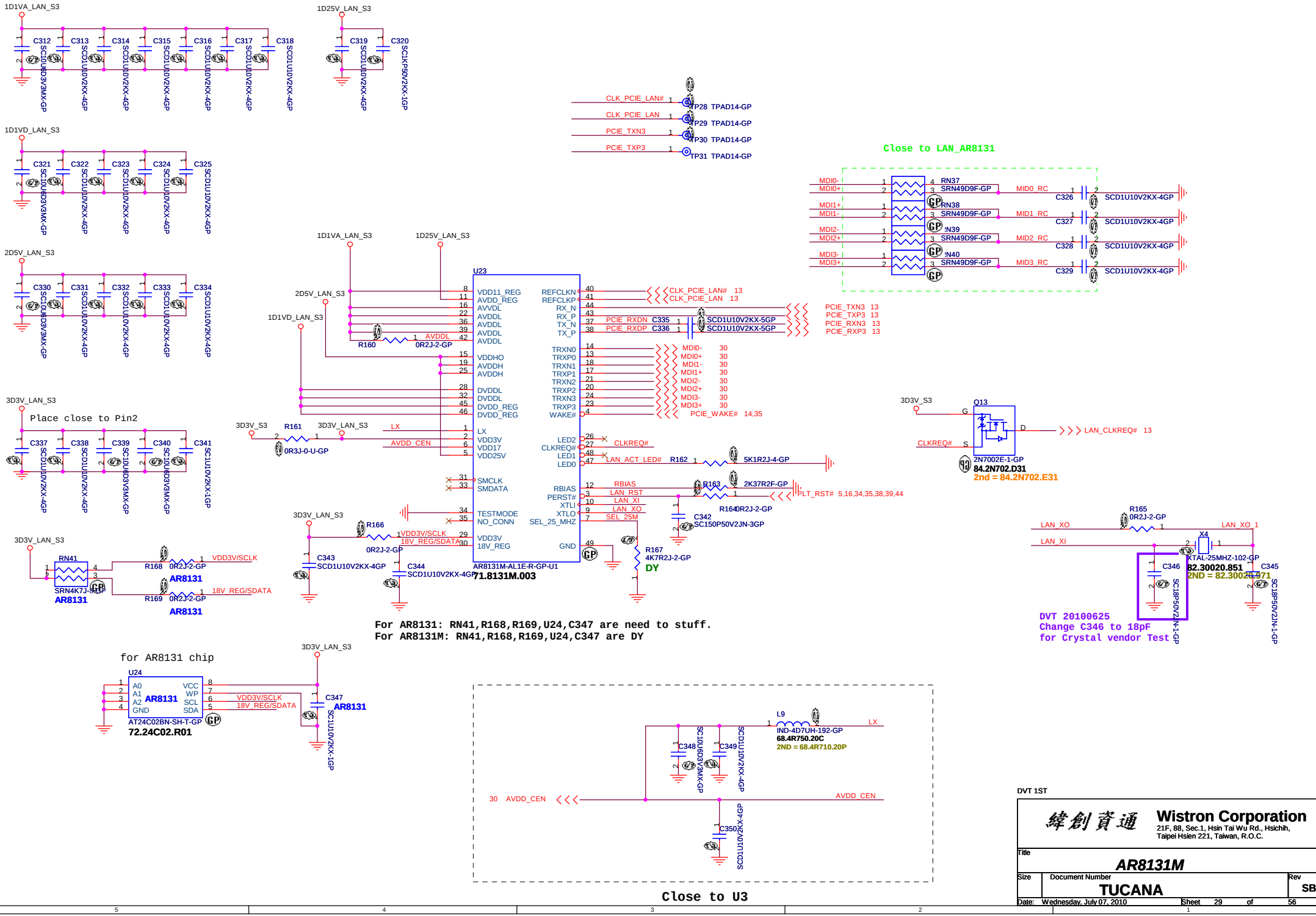
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB CONN**

Size	Document Number	Rev
	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 28 of 56



DVT 1ST

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AR8131M**

Size	Document Number	Rev
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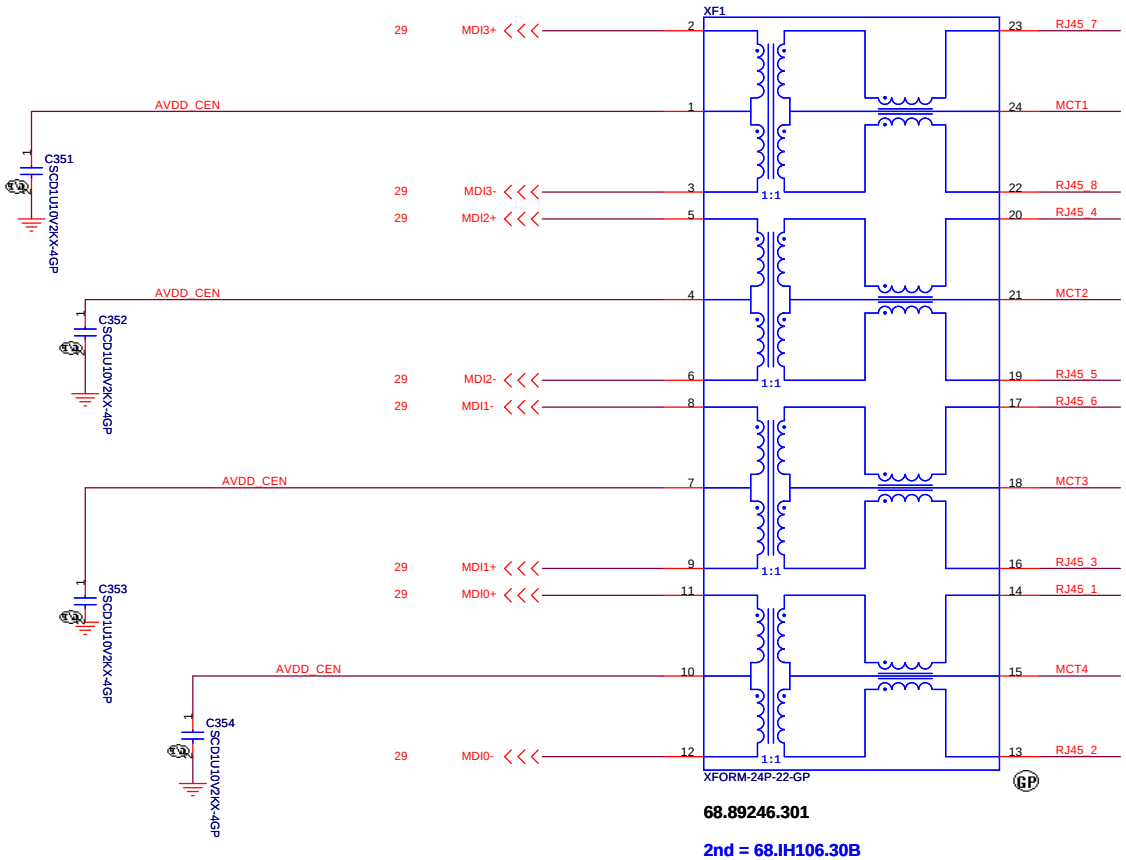
Date: Wednesday, July 07, 2010 Sheet 29 of 56

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

LAN Transformer

AVDD_CEN 29

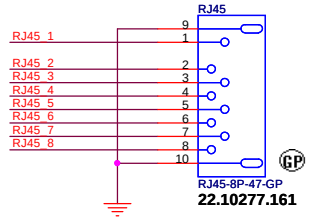
GIGA Lan Transformer



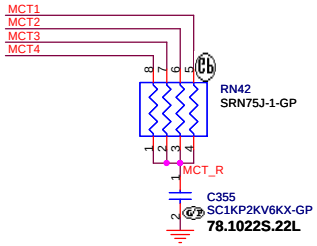
68.89246.301

2nd = 68.IH106.30B

LAN Connector



22.10277.161

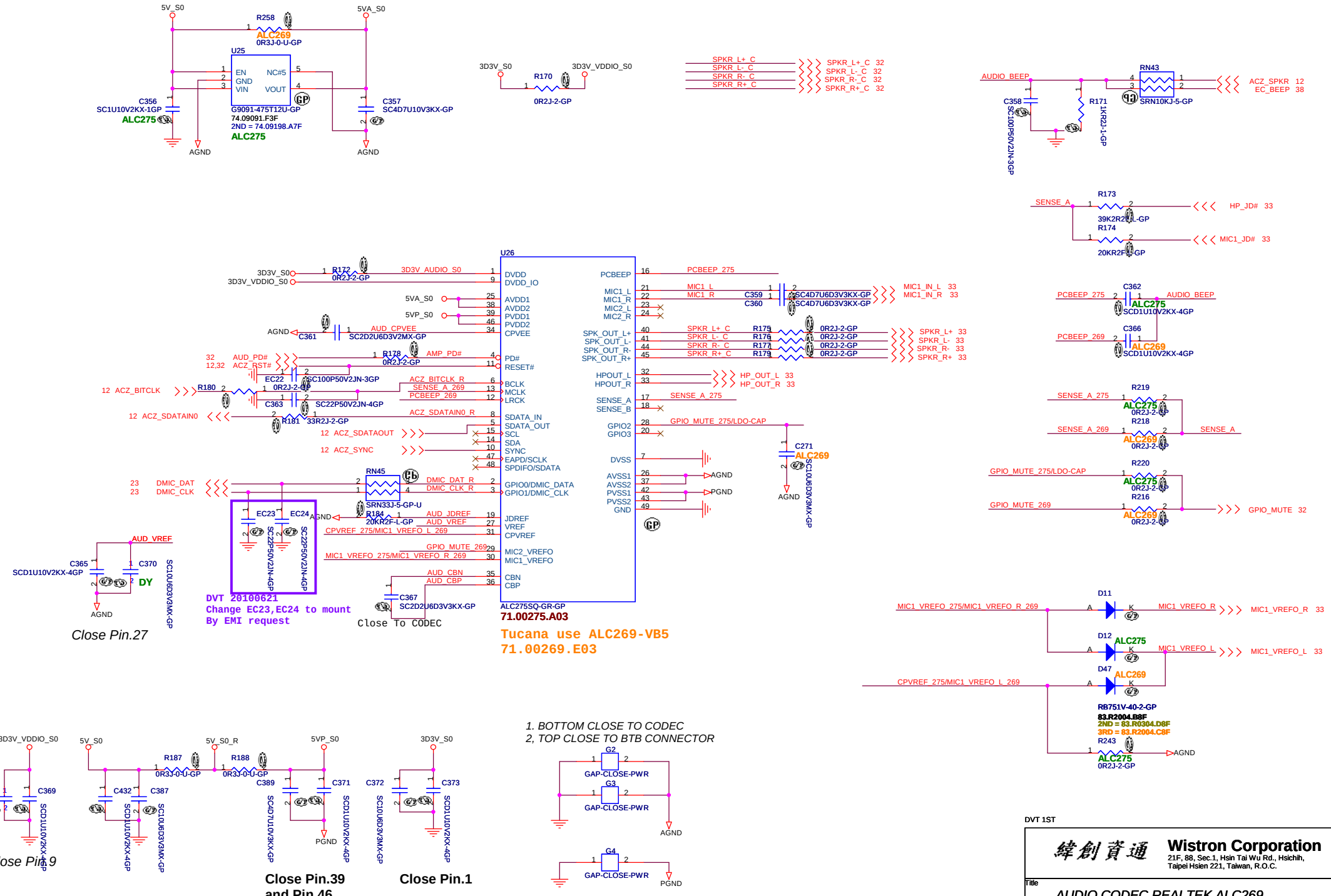


78.1022S.22L

DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**LAN CONN**	
Size	Document Number **TUCANA**	Rev **SB**
Date: Wednesday, July 07, 2010	Sheet 30 of 56	



DVT 1ST

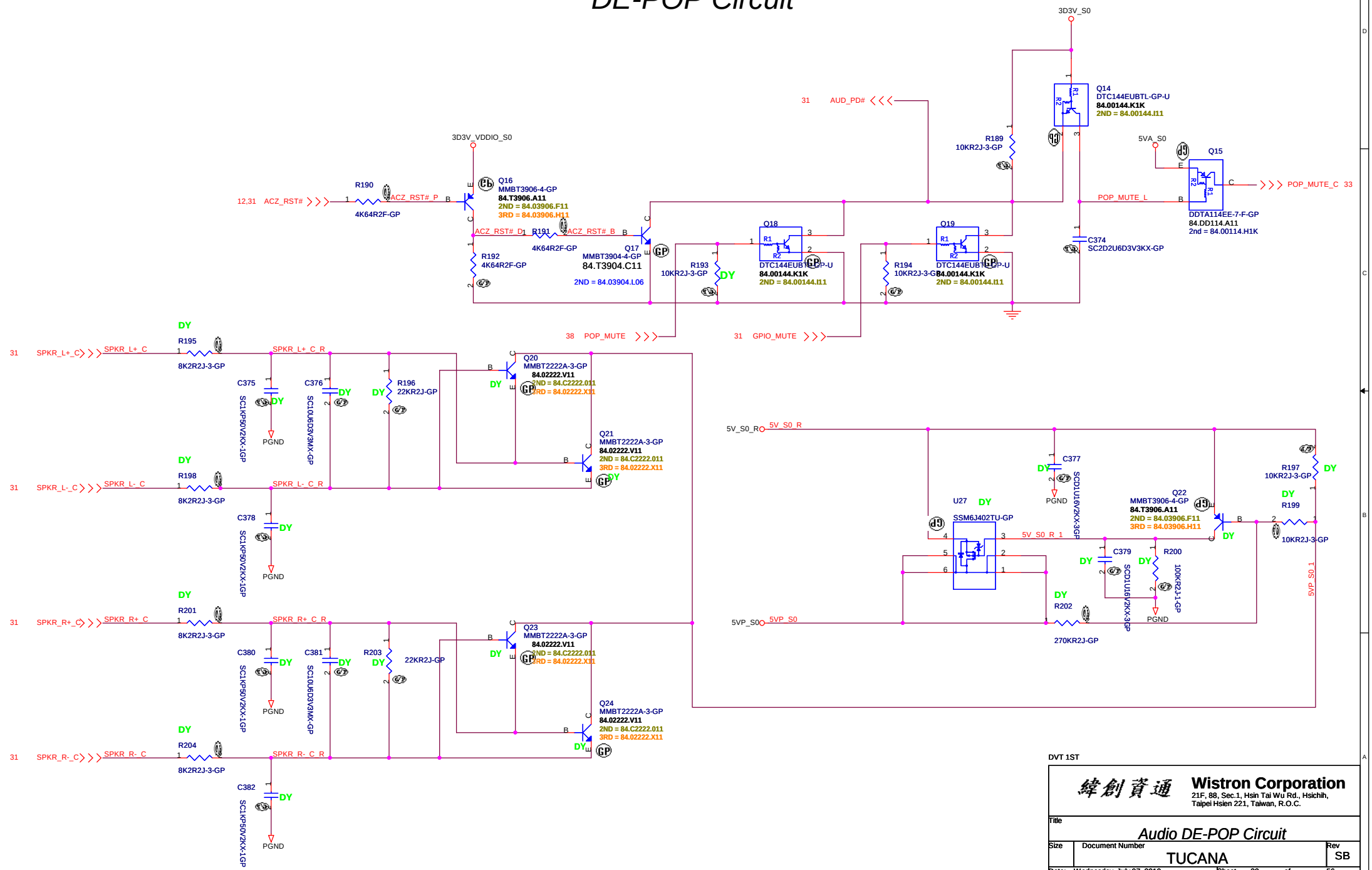
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO CODEC REALTEK ALC269*

Size	Document Number	Rev
	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 31 of 56

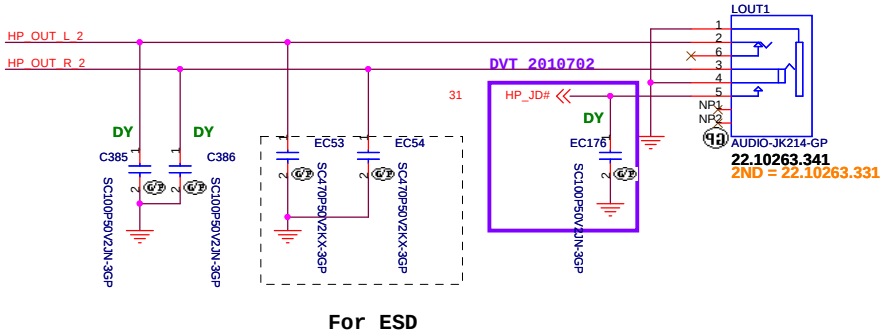
DE-POP Circuit



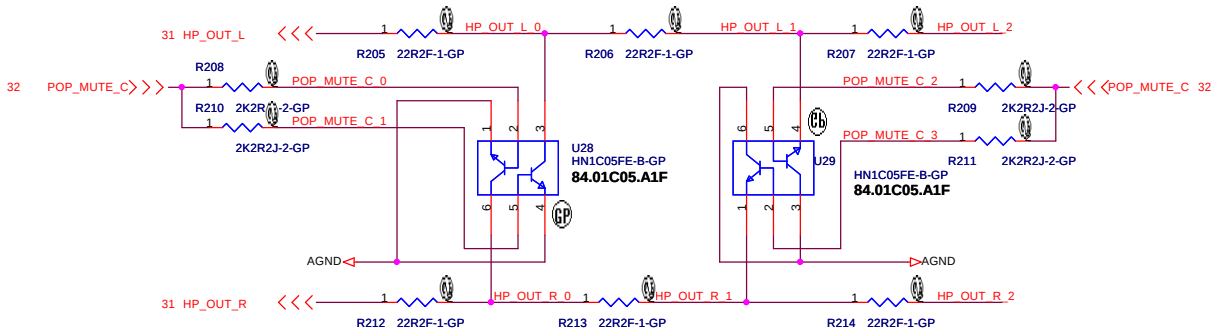
DVT 1ST

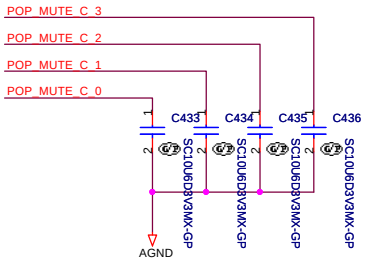
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Audio DE-POP Circuit		
Size	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 32 of 56	

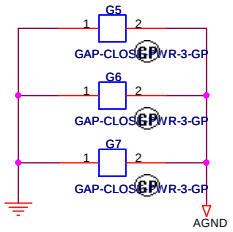
LINE OUT



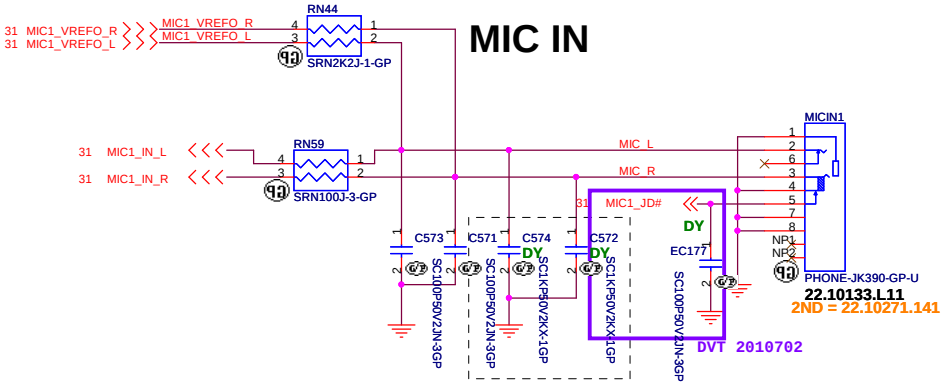
For ESD





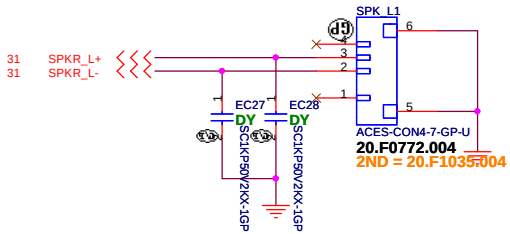


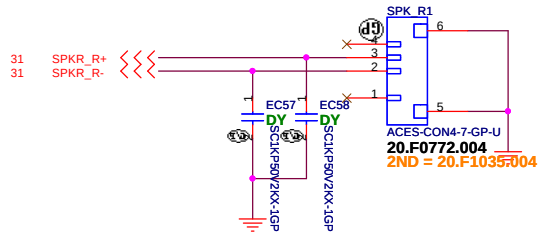
MIC IN



For ESD

Internal Speaker CONN





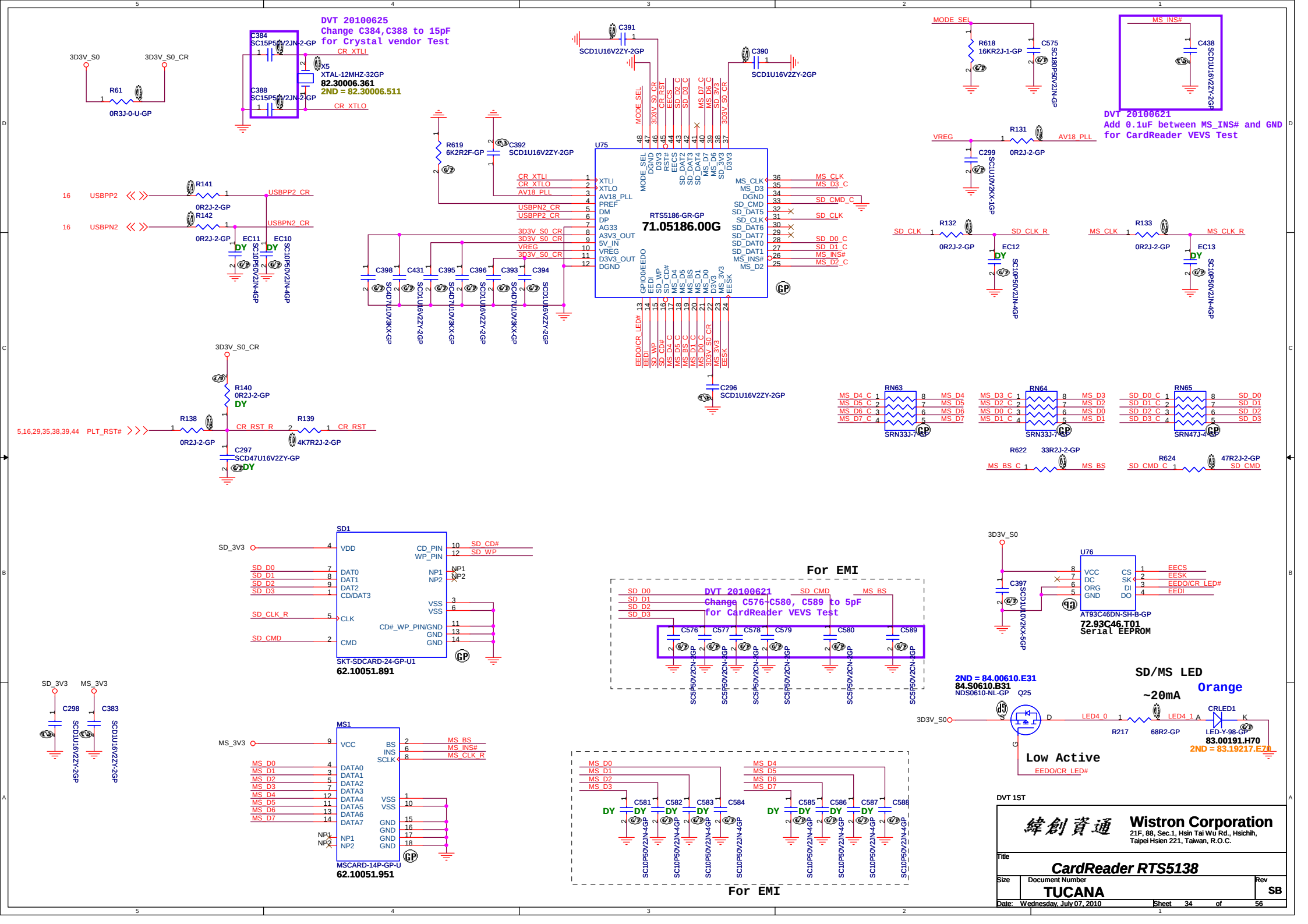
DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack & Speaker

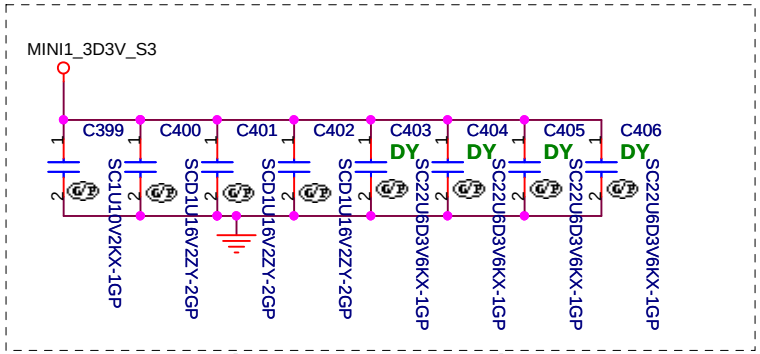
Size	Document Number	Rev
	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 33 of 56


DVT 20100625
Change C384,C388 to 15pF
for Crystal vendor Test
C384
SC15P50V2JN-2-GP
C388
SC15P50V2JN-2-GP
X5
XTAL-12MHZ-32GP
82.30006.361
2ND = 82.30006.511
3D3V_S0
3D3V_S0_CR
R61
0R3J-0-U-GP
CR_XTLI
CR_XTLO
C391
SCD1U16V2ZY-2GP
C390
SCD1U16V2ZY-2GP
R619
6K2R2F-GP
C392
SCD1U16V2ZY-2GP
U75
RTS5186-GR-GP
71.05186.00G
MODE_SEL
3D3V_S0_CR
CR_RST
EECS
SD_D2_C
SD_D3_C
MS_D7_C
MS_D6_C
SD_3V3
3D3V_S0_CR
XTLI
XTLO
AV18_PLL
PREF
DM
DP
AG33
A3V3_OUT
5V_IN
VREG
D3V3_OUT
DGND
MS_CLK
MS_D3
DGND
SD_CMD
SD_DAT5
SD_CLK
SD_DAT6
SD_DAT7
SD_DAT0
SD_DAT1
MS_INS#
MS_D2
GPIO0/EEDO
EEDI
SD_WP
SD_CD#
MS_D4
MS_D5
MS_BS
MS_D1
MS_D0
D3V3
MS_3V3
EESK
EEDO/CR_LED#
EEDI
SD_WP
SD_CD#
MS_D4_C
MS_D5_C
MS_BS_C
MS_D1_C
MS_D0_C
3D3V_S0_CR
MS_3V3
EESK
C296
SCD1U16V2ZY-2GP
USBPP2
USBPN2
R141
R142
0R2J-2-GP
USBPP2_CR
USBPN2_CR
EC11
EC10
SC10P50V2JN-4GP
C398
C431
C395
C396
C393
C394
SC4D7U10V3KX-GP
SCD1U16V2ZY-2GP
3D3V_S0_CR
VREG
MODE_SEL
R618
16KR2J-1-GP
C575
SC18P50V2JN-GP
MS_INS#
C438
SCD1U16V2ZY-2GP
DVT 20100621
Add 0.1uF between MS_INS# and GND
for CardReader VEVS Test
VREG
R131
0R2J-2-GP
AV18_PLL
C299
SC1U10V2KX-1GP
SD_CLK
R132
SD_CLK_R
EC12
MS_CLK
R133
MS_CLK_R
EC13
SC10P50V2JN-4GP
3D3V_S0_CR
R140
0R2J-2-GP
DY
5,16,29,35,38,39,44
PLT_RST#
R138
CR_RST_R
R139
CR_RST
4K7R2J-2-GP
C297
SCD47U16V2ZY-GP
RN63
SRN33J-7-GP
MS_D4_C
MS_D5_C
MS_D6_C
MS_D7_C
MS_D4
MS_D5
MS_D6
MS_D7
RN64
SRN33J-7-GP
MS_D3_C
MS_D2_C
MS_D0_C
MS_D1_C
MS_D3
MS_D2
MS_D0
MS_D1
RN65
SRN47J-4-GP
SD_D0_C
SD_D1_C
SD_D2_C
SD_D3_C
SD_D0
SD_D1
SD_D2
SD_D3
R622
33R2J-2-GP
MS_BS_C
MS_BS
R624
47R2J-2-GP
SD_CMD_C
SD_CMD
SD1
SKT-SDCARD-24-GP-U1
62.10051.891
SD_3V3
VDD
CD_PIN
WP_PIN
SD_D0
SD_D1
SD_D2
SD_D3
DAT0
DAT1
DAT2
CD/DAT3
SD_CLK_R
CLK
SD_CMD
CMD
NP1
NP2
VSS
VSS
CD#_WP_PIN/GND
GND
GND
SD_CD#
SD_WP
For EMI
DVT 20100621
Change C576-C580, C589 to 5pF
for CardReader VEVS Test
SD_CMD
MS_BS
C576
C577
C578
C579
C580
C589
SC5P50V2CN-4GP
U76
AT93C46DN-SH-B-GP
72.93C46.T01
Serial EEPROM
VCC
DC
ORG
GND
CS
SK
DI
DO
EECS
EESK
EEDO/CR_LED#
EEDI
C397
SCD1U10V2KX-5GP
SD_3V3
MS_3V3
C298
C383
SCD1U16V2ZY-2GP
MS1
MSCARD-14P-GP-U
62.10051.951
MS_3V3
VCC
BS
INS
SCLK
MS_BS
MS_INS#
MS_CLK_R
MS_D0
MS_D1
MS_D2
MS_D3
MS_D4
MS_D5
MS_D6
MS_D7
DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
VSS
VSS
GND
GND
GND
GND
NP1
NP2
NP1
NP2
For EMI
C581
C582
C583
C584
C585
C586
C587
C588
2ND = 84.00610.E31
84.S0610.B31
NDS0610-NL-GP
Q25
3D3V_S0
LED4_0
LED4_1
R217
68R2-GP
CRLED1
LED-Y-98-GP
83.00191.H70
2ND = 83.19217.E70
SD/MS LED
Orange
~20mA
Low Active
EEDO/CR_LED#
DVT 1ST
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CardReader RTS5138
Size
Document Number
TUCANA
Rev
SB
Date: Wednesday, July 07, 2010
Sheet 34 of 56

Mini Card Connector(WLAN)

WLAN_EN:
Low: disable the radio
High: enable the radio



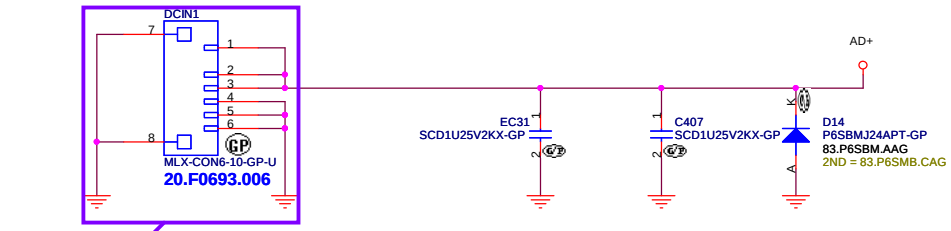
C50,C68 bypass MINI1 pin2
C51,C69 bypass MINI1 pin39
C52,C70 bypass MINI1 pin41
C53,C71 bypass MINI1 pin52
Place near MINI1

DVT 1ST

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI CARD CONN***	
Size	Document Number **TUCANA**	Rev **SB**
Date: Wednesday, July 07, 2010	Sheet 35 of 56	

DC IN Connector

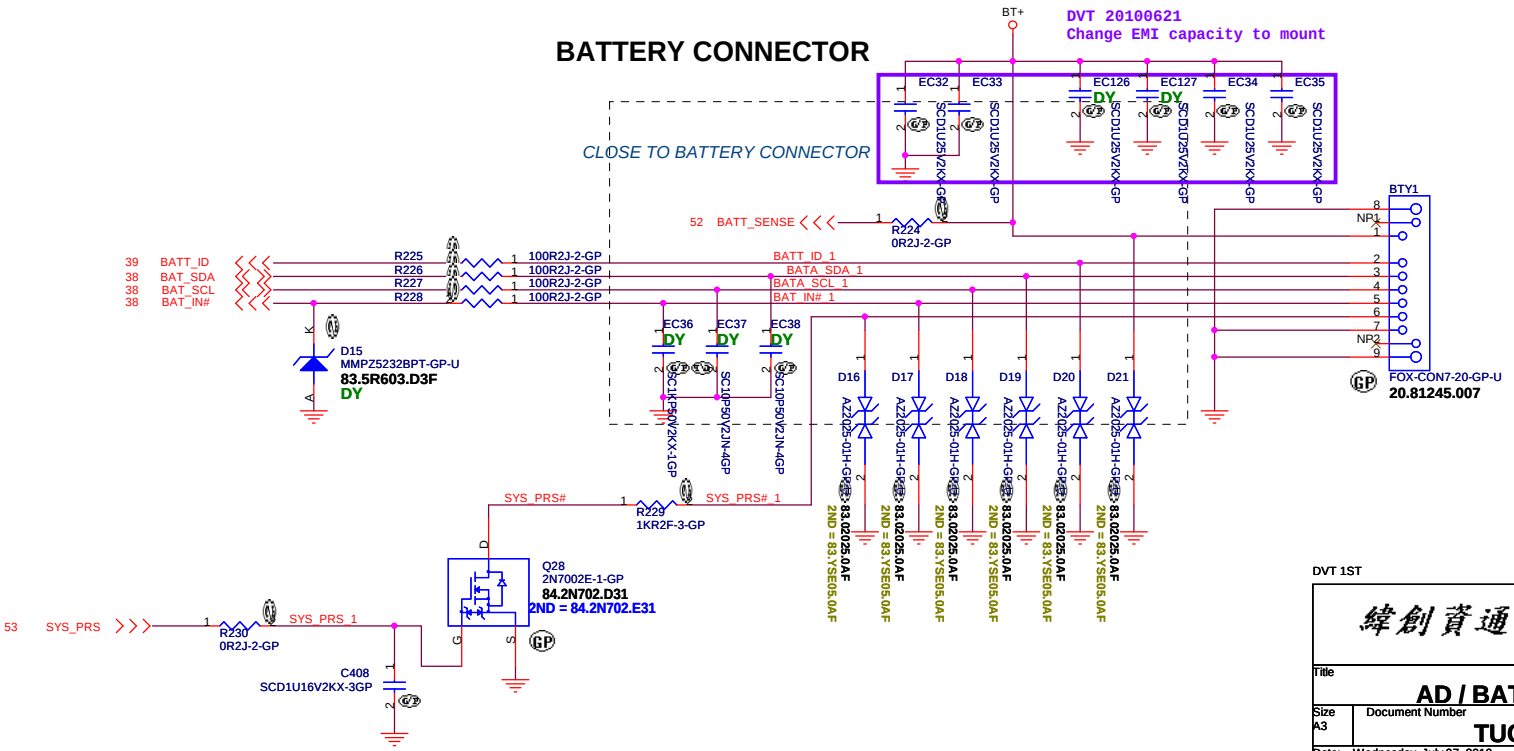
1 pin 1A



DVT 20100610
Change DCIN1 to 20.F0693.006
(follow connector list)

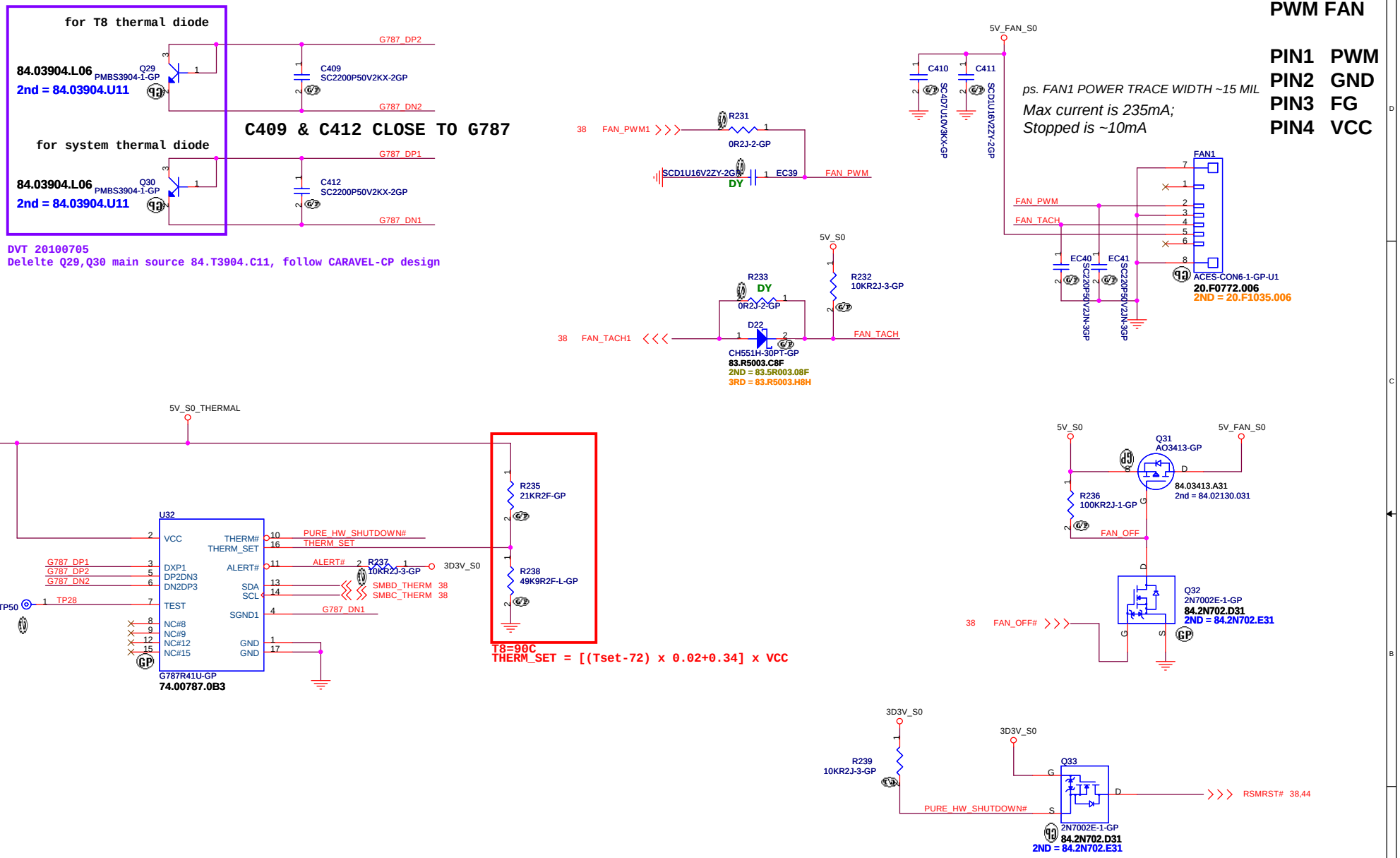
Adaptor in to generate DCBATOUT

BATTERY CONNECTOR



DVT 1ST

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**AD / BATT CONN**
Size A3	Document Number **TUCANA** Rev SB
Date: Wednesday, July 07, 2010	Sheet 36 of 56



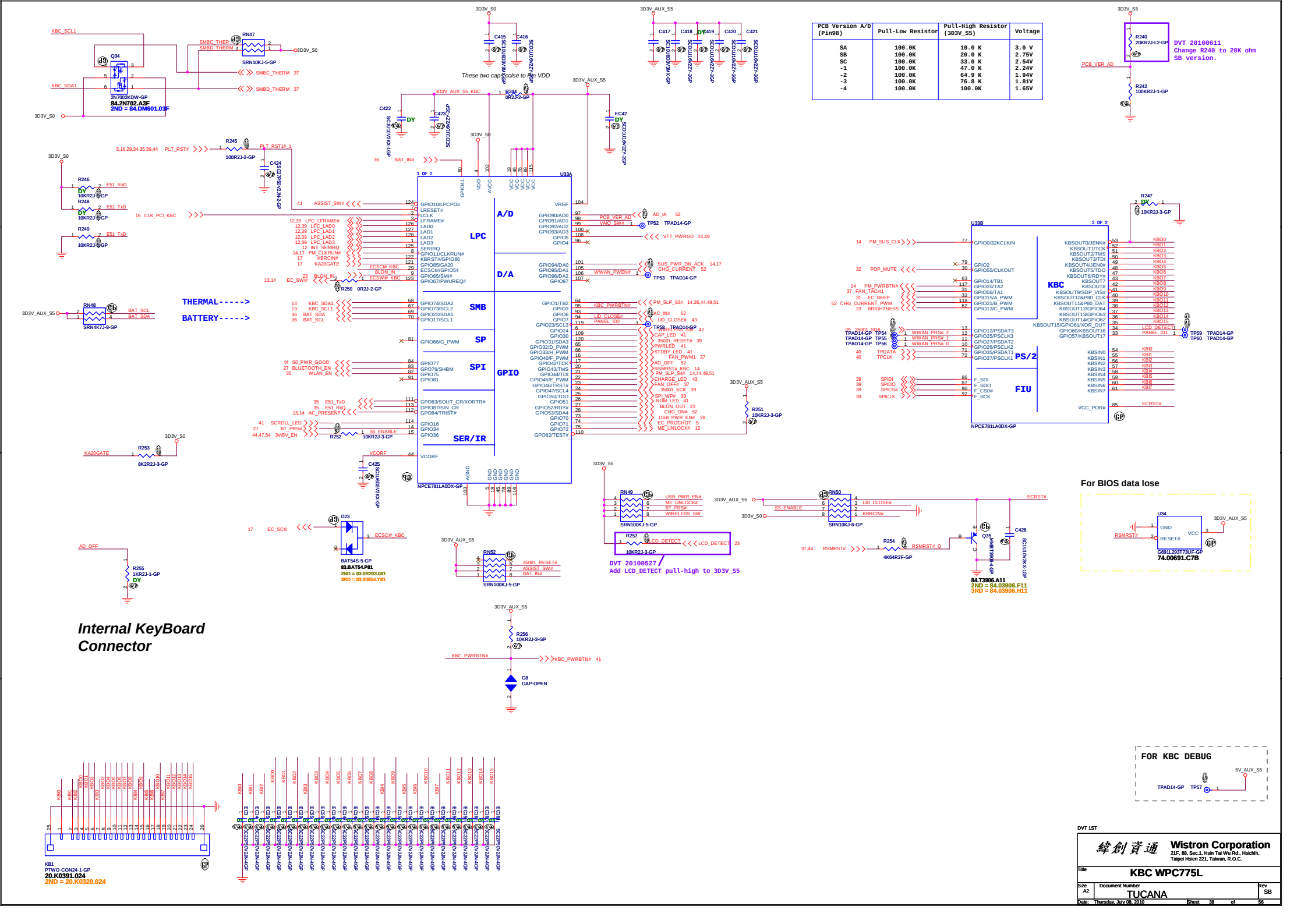
DVT 1ST

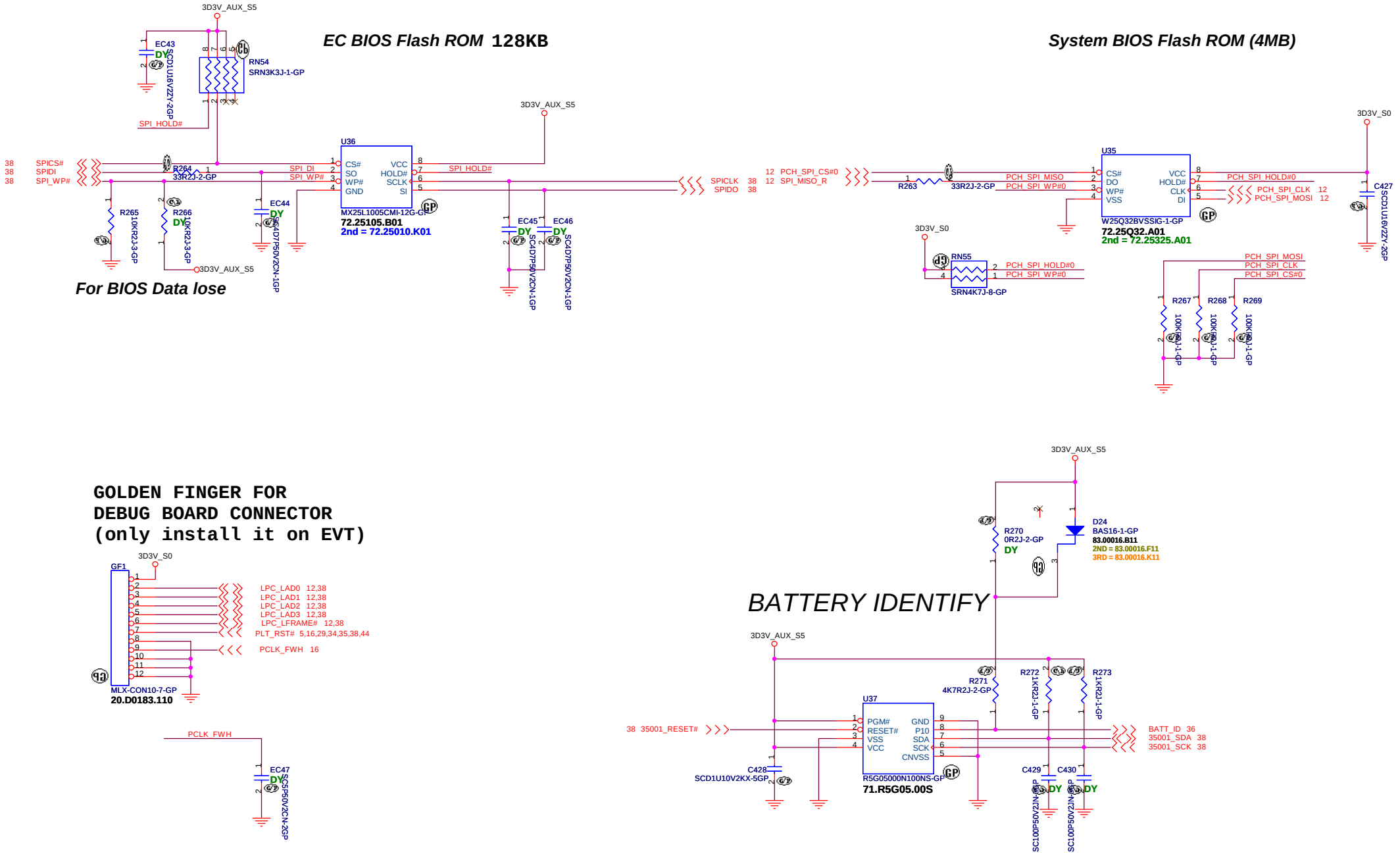
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor***

Size	Document Number	Rev
	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 37 of 56


PCB Version A/D (Pin98)
Pull-Low Resistor
Pull-High Resistor (3D3V_S5)
Voltage
SA 100.0K 10.0 K 3.0 V
SB 100.0K 20.0 K 2.75V
SC 100.0K 33.0 K 2.54V
-1 100.0K 47.0 K 2.24V
-2 100.0K 64.9 K 1.94V
-3 100.0K 76.8 K 1.81V
-4 100.0K 100.0K 1.65V
DVT 20100611
Change R240 to 20K ohm
SB version.
These two caps close to Pin VDD
THERMAL----->
BATTERY----->
A/D
D/A
SMB
SP
SPI
SER/IR
LPC
GPIO
KBC
PS/2
FIU
U33A
U33B
NPCE781LA0DX-GP
DVT 20100527
Add LCD_DETECT pull-high to 3D3V_S5
For BIOS data lose
Internal KeyBoard Connector
FOR KBC DEBUG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC775L
TUCANA
Thursday, July 08, 2010



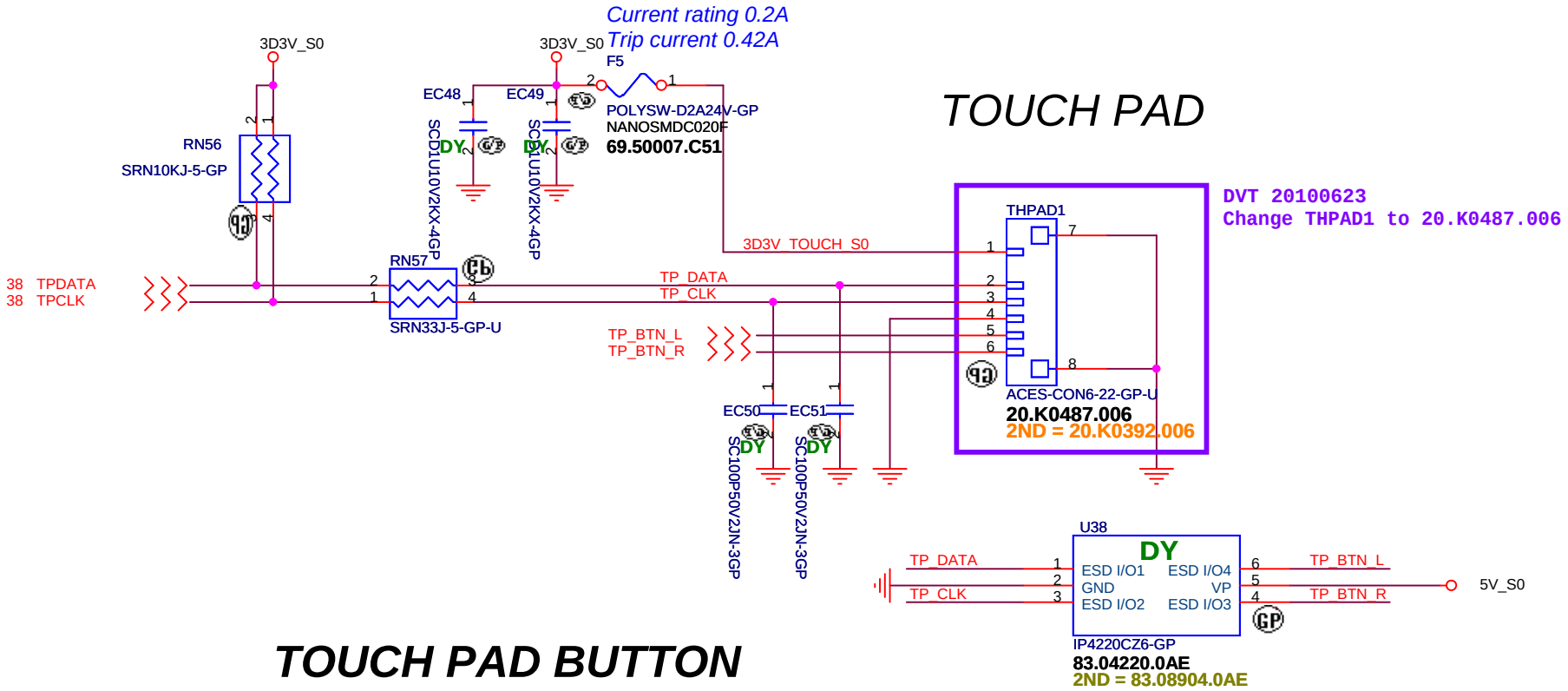
DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS & SW/C & BAT ID**

Size	Document Number	Rev
	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 39 of 56



DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TouchPad**

Size	Document Number	Rev
A4	TUCANA	SB

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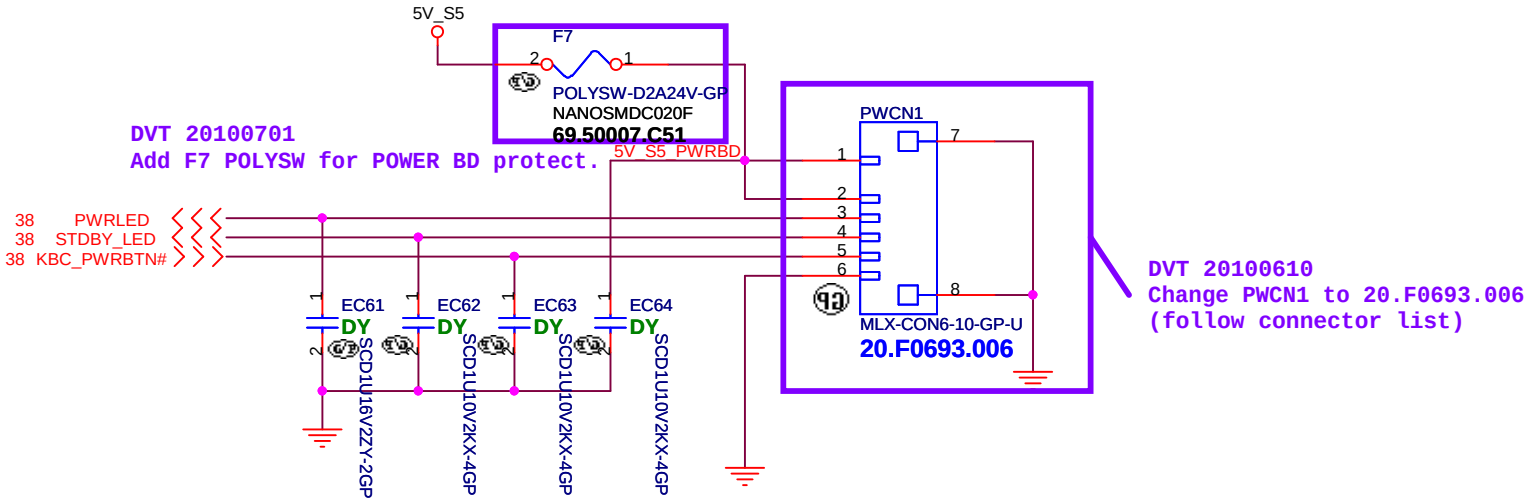
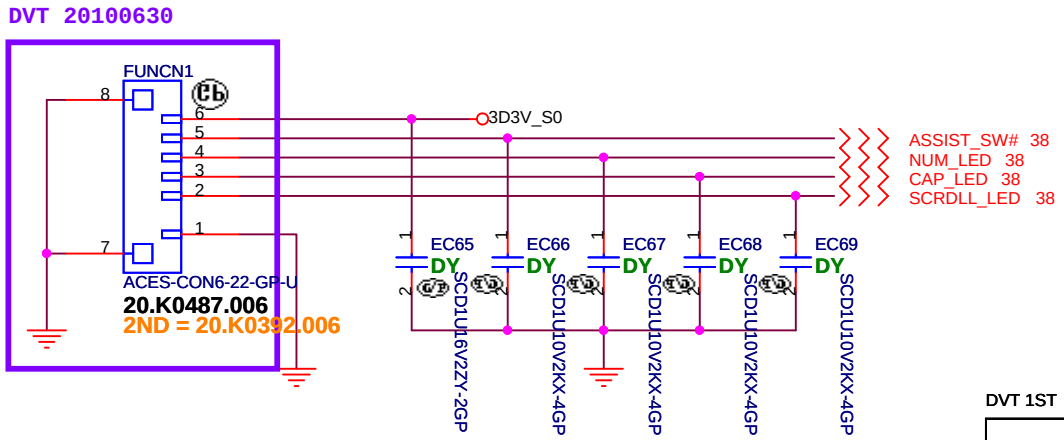
POWER BUTTON BD CONN



FUNCTION BD CONN



DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**FUNCTION BD & POWER BD**	
Size	Document Number **TUCANA**	Rev **SB**
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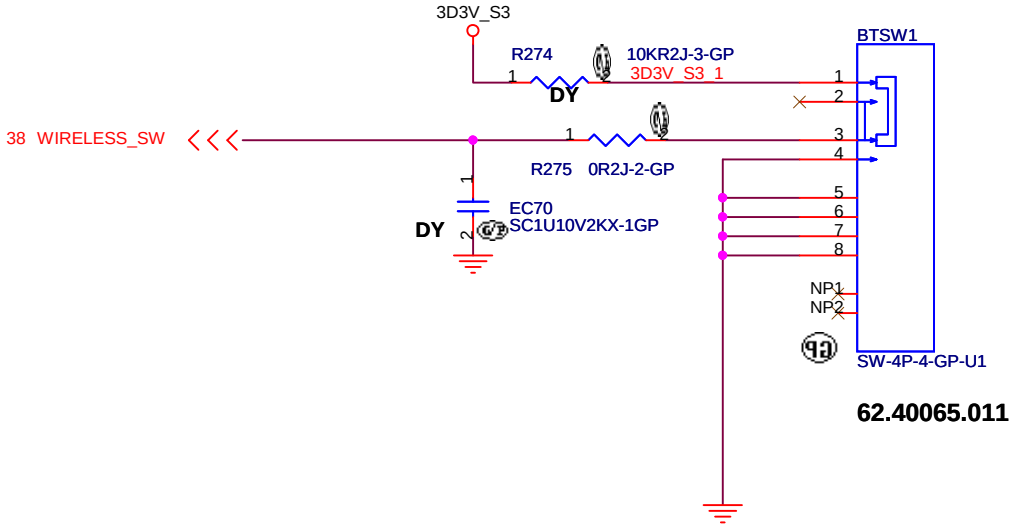
WLAN SWITCH



DVT 1ST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Switch*		
Size	Document Number: TUCANA	Rev: SB
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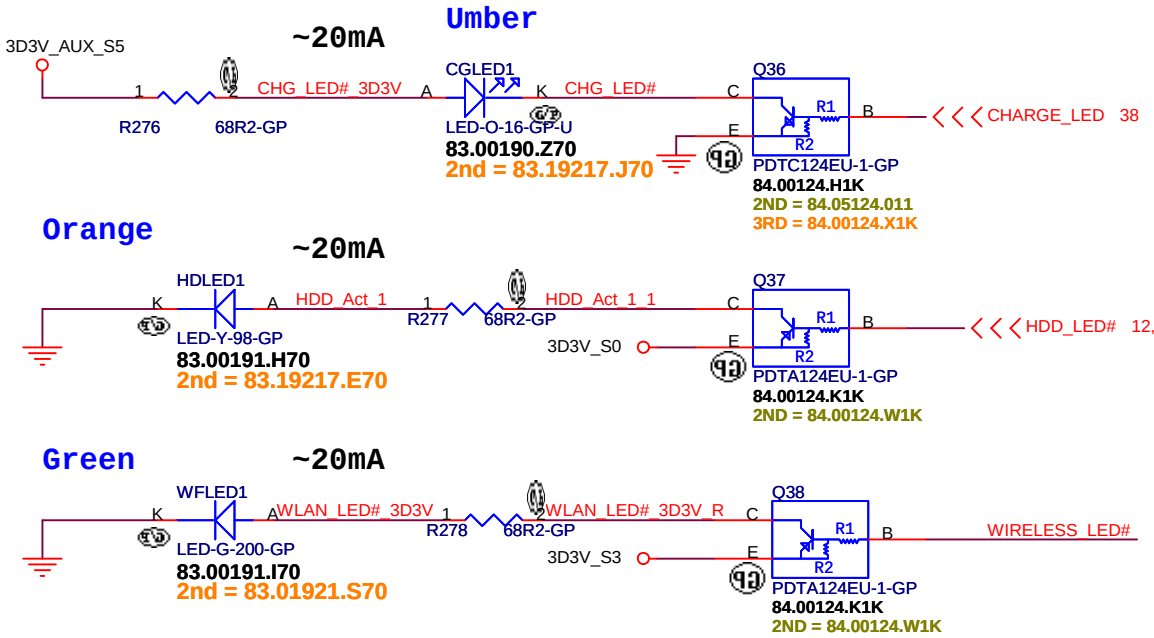
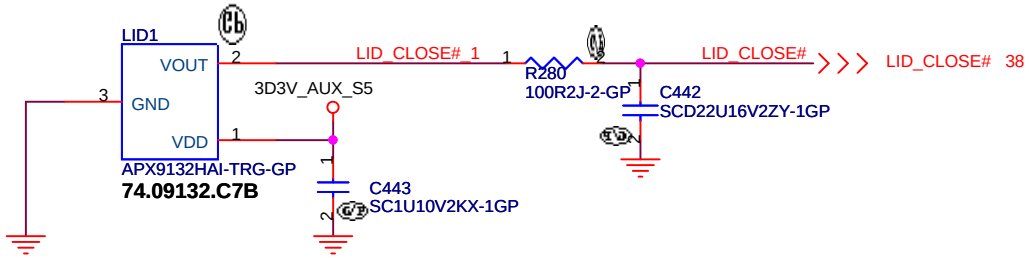
LED



active	High	Low
WWAN(W_DISABLE#)	ON	OFF
WLAN(WLAN_LED#)	OFF	ON
Bluetooth(BT_LED)	ON	OFF

Cover Up Switch



Common wireless SW(mechanical)	ON							
WLAN SW(software)	ON	OFF	ON	OFF	ON	OFF	ON	OFF
WWAN SW(software)	ON	ON	OFF	OFF	ON	ON	OFF	OFF
Bluetooth SW(software)	ON	ON	ON	ON	OFF	OFF	OFF	OFF
LED	TURN ON							OFF

DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Lid Switch & LED***

Size	Document Number	Rev
	TUCANA	SB

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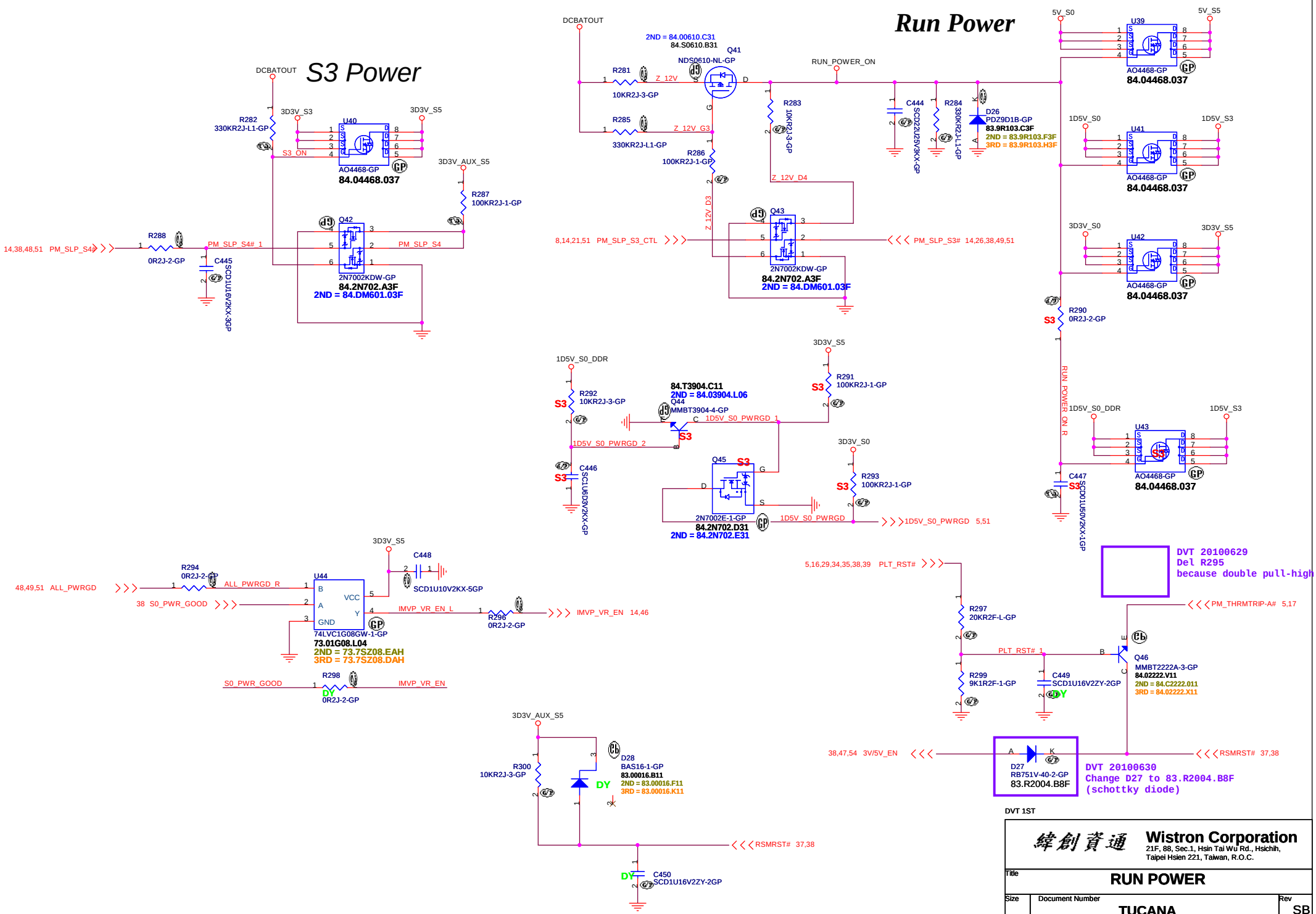

DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RUN POWER	
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CPU_CORE
ADP3211

VID0
VID1
VID2
VID3
VID4
VID5
VID6

CPUCORE_ON

VCC_SENSE
VSS_SENSE

DCBATOUT_6261A
5V_S0
3D3V_S0

VID Setting	Output Signal
VID0(I / 3.3V)	PGOOD
VID1(I / 3.3V)	
VID2(I / 3.3V)	
VID3(I / 3.3V)	Output Power
VID4(I / 3.3V)	VCC_CORE_PWR(O)
VID5(I / 3.3V)	
VID6(I / 3.3V)	
Input Signal	
EN (I / 3.3V)	
Voltage Sense	
VSEN(I / Vcore)	
RGND(I / Vcore)	
Input Power	
VCC(I)	
VCC(I)	
VCC(I)	

VR_PWROK
VCC_CORE(Imax=27A)

RT8209 1D05V_S0

DCBATOUT_8202_1D05V
ALL_PWRGD

VIN	1D5V(O)
EN	PGOOD

1D05V_S0 (20A)
CPUCORE_ON

RT8209 1D5V_S3

DCBATOUT_8202_1D5V
PM_SLP_S4#

VIN	1D5V(O)
EN	PGOOD

1D5V_S3 (9.4A)
S3_PWRGD

GFX_CORE/ VGA_CORE
ADP3211

VID0
VID1
VID2
VID3
VID4

5V_S0
DCBATOUT_3211

GFXVR_EN

VCC_AXG_SENSE
VSS_AXG_SENSE

VID Setting	Output Signal
VID0(I / 3.3V)	PGOOD
VID1(I / 3.3V)	
VID2(I / 3.3V)	
VID3(I / 3.3V)	
VID4(I / 3.3V)	
Input Power	Output Power
VDD	
VIN	VGFXCORE (O)
Input Signal	
VR_ON	
Voltage Sense	
VSEN(I / Vcore)	
RGND(I / Vcore)	

CPUCORE_ON
VCC_GFXCORE(11A)

RT9026 0D75V_S0

5V_S5
1D5V_S3
PM_SLP_S3#
PM_SLP_S4#

VIN	
VLDOIN	VTT
S3	VTTREF
S5	

0D75V_S3 (1.2A)
0D75V_S3_1

RT8015 1D8V_S0

3D3V_S5
PM_SLP_S3#

VDD	VTT
EN	

1D8V_S0 (1.577A)

5V/3D3V
RT8223

DCBATOUT_51123
S5_ENABLE
ALW_PWRGD_3V_5V

Input Power	Output Power
VIN	5V(O)
Input Signal	3D3V(O)
EN0	5V(O)
Output Signal	3D3V(O)
PGOOD	

5V_S5 (6A)
3D3V_S5 (5A)
5V_AUX_S5
3D3V_AUX_S5

Charger BQ24751

CHG_ON#
AD+

Input Signal	Output Signal
CHGEN#	ACGOOD#
	SRSET
	BAT
Input Power	Output Power
ACDET	VOUT (O)
	VOUT (O)

AC_IN#
CHG_CURRENT
BATT_SENSE
BT+
DCBATOUT

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal	Output Signal
(I)	(O)
Input Power	Output Power
VCC(I)	VCC(O)
VCC(I)	

AD_IN#
AD+

DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Sequence Logic**

Size	Document Number	Rev
A3	TUCANA	SB

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DVT 20100701
Change OPEN-GAP to CLOSE-GAP

DVT 20100623

DVT 20100623

DVT 20100623

Id=24A
Qg=11nC
Rdson=9.6~13.4mohm

Id=50A
Qg=46nC
Rdson=2.3~3.6mohm

Mag. 0.36uH
DCR=1.05~1.2mohm
Idc=30A, Isat=60A

Iomax=27A
OCP>40.5A

Panasonic 330uF
2V, ESR=9mohm

64.64915.6DL

Intel support POC (power on current).

DVT 1ST

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADP3211 CPU CORE

Size: | Document Number: TUCANA | Rev: SB

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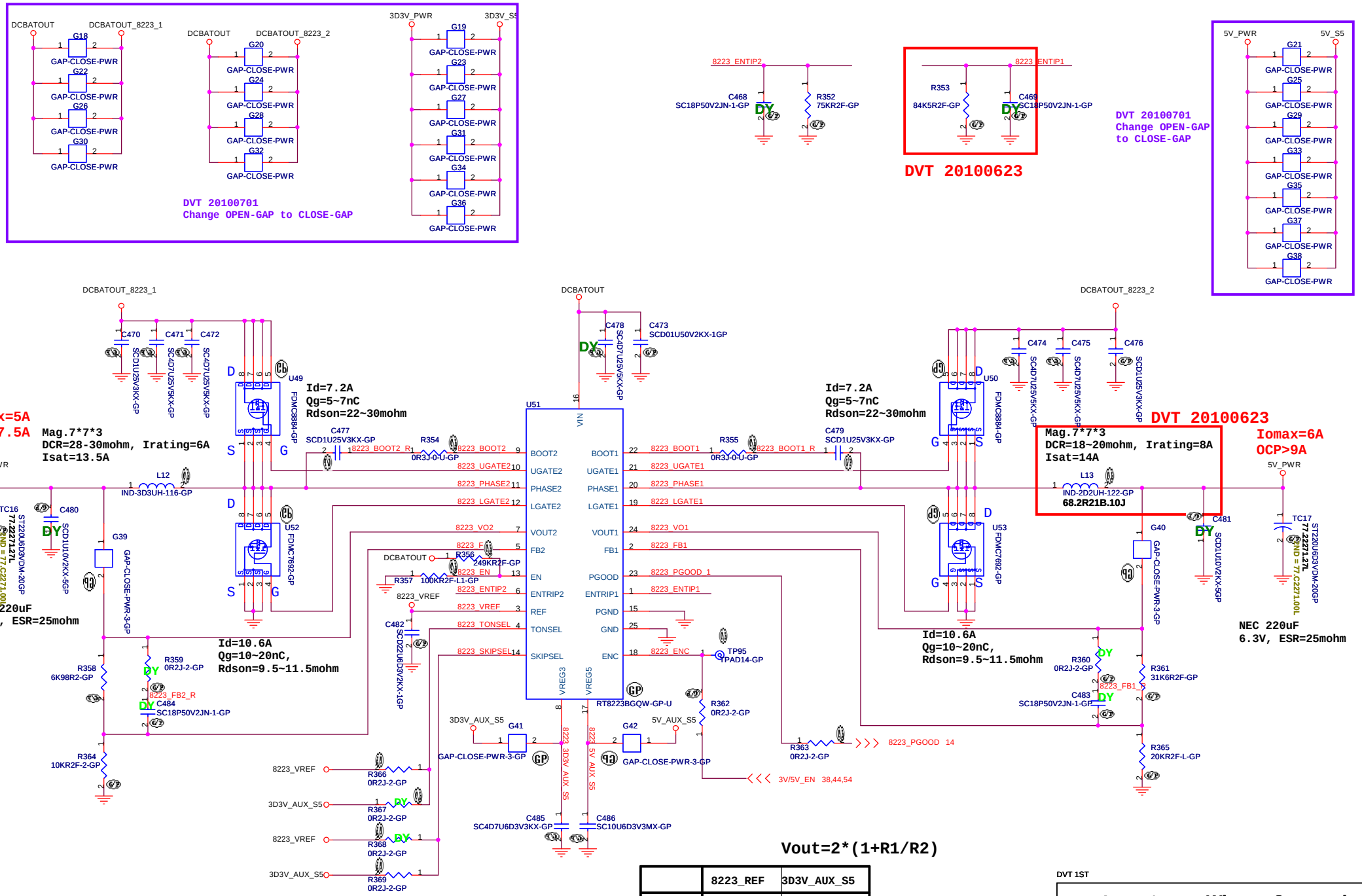

	8223_REF	3D3V_AUX_S5
SKIPSEL	PWM	00A AUTOSKIP
TONSEL	245k/CH1 305k/CH2	300k/CH1 375k/CH2

DVT 1ST

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223_5V/3D3V

Size	Document Number	Rev
	TUCANA	SA

Date: Wednesday, July 07, 2010 Sheet 47 of 56

RT8209 for 1D5V

DVT 20100701
Change OPEN-GAP to
CLOSE-GAP

DCBATOUT DCBATOUT_8209_1D5V
G47 GAP-CLOSE-PWR
G49 GAP-CLOSE-PWR
G51 GAP-CLOSE-PWR
G53 GAP-CLOSE-PWR
TC28 DY ST15U25VDM-1-GP
77.21561.00L
2ND = 77.C1561.03L

DVT 20100701
Change OPEN-GAP to
CLOSE-GAP

1D5V_PWR 1D5V_S3
G43 GAP-CLOSE-PWR
G44 GAP-CLOSE-PWR
G45 GAP-CLOSE-PWR
G46 GAP-CLOSE-PWR
G48 GAP-CLOSE-PWR
G50 GAP-CLOSE-PWR
G52 GAP-CLOSE-PWR
G54 GAP-CLOSE-PWR
G55 GAP-CLOSE-PWR
G56 GAP-CLOSE-PWR

5V_S5
C487 SC1U10V2KX-1GP
R370 2D2R3-1-U-GP
8209_1D5_V5FILT
C491 SC1U10V2KX-1GP
R371 0R3J-0-U-GP
8209_1D5_PHASE_1
C492 SCD1U25V3KX-GP
R372 0R3J-0-U-GP
8209_1D5_UGATE_R

U55
VDD
VDDP
FB
BOOT
UGATE
LGATE
PHASE
VOUT
PGOOD
GND
PGND
EN/DEM
TON
CS
NC#15
RT8209EGQW-GP
8209_1D5_UGATE
8209_1D5_LGATE
8209_1D5_PHASE
8209_1D5_PGOOD
8209_1D5_FB
8209_1D5_BOOT
8209_1D5_EN
8209_1D5_TON
8209_1D5_CS

14,38,44,51 PM_SLP_S4#
R374 0R2J-2-GP
R376 100KR2F-L1-GP
C495 DY SCD1U10V2KX-5GP
R373 249KR2F-GP
R377 7K5R2F-1-GP
DVT 20100623

1D5V_PWR
3D3V_S0
R378 10KR2F-2-GP
R379 0R2J-2-GP
ALL_PWRGD 44,49,51

DCBATOUT_8209_1D5V
U54 SI7686DP-T1-GE3-GP
84.07686.A37
Id=14.3A
Qg=9.2~14nC
Rdson=11~14mohm
C488 SC4D7U25V5KX-GP
C489 SC4D7U25V5KX-GP
C490 SCD1U25V3KX-GP

L14 IND-1UH-93-GP
68.1R01B.10J
Mag. 1.0uH
DCR=2.9~3.3mohm
Idc=18A, Isat=36A
Iomax=9.4A
OCP>14.1A
20100401

U56 SIR460DP-T1-GE3-GP
84.00460.037
20100331

R375 31K6R2F-GP
R380 30KR2F-GP
8209_1D5_FB
C493 DY SC33P50V2JN-3GP
C494 SCD1U10V2KX-5GP
TC18 ST330U2D5VBM-1-GP
80.3371V.A2L
2ND = 77.2371.31L
Panasonic 220uF
2V, ESR=9mohm

Id=19.4A
Qg=16.8~25.5nC,
Rdson=4.9~6.1mohm
20100331

Vout=0.75*(1+R1/R2)

DVT 1ST

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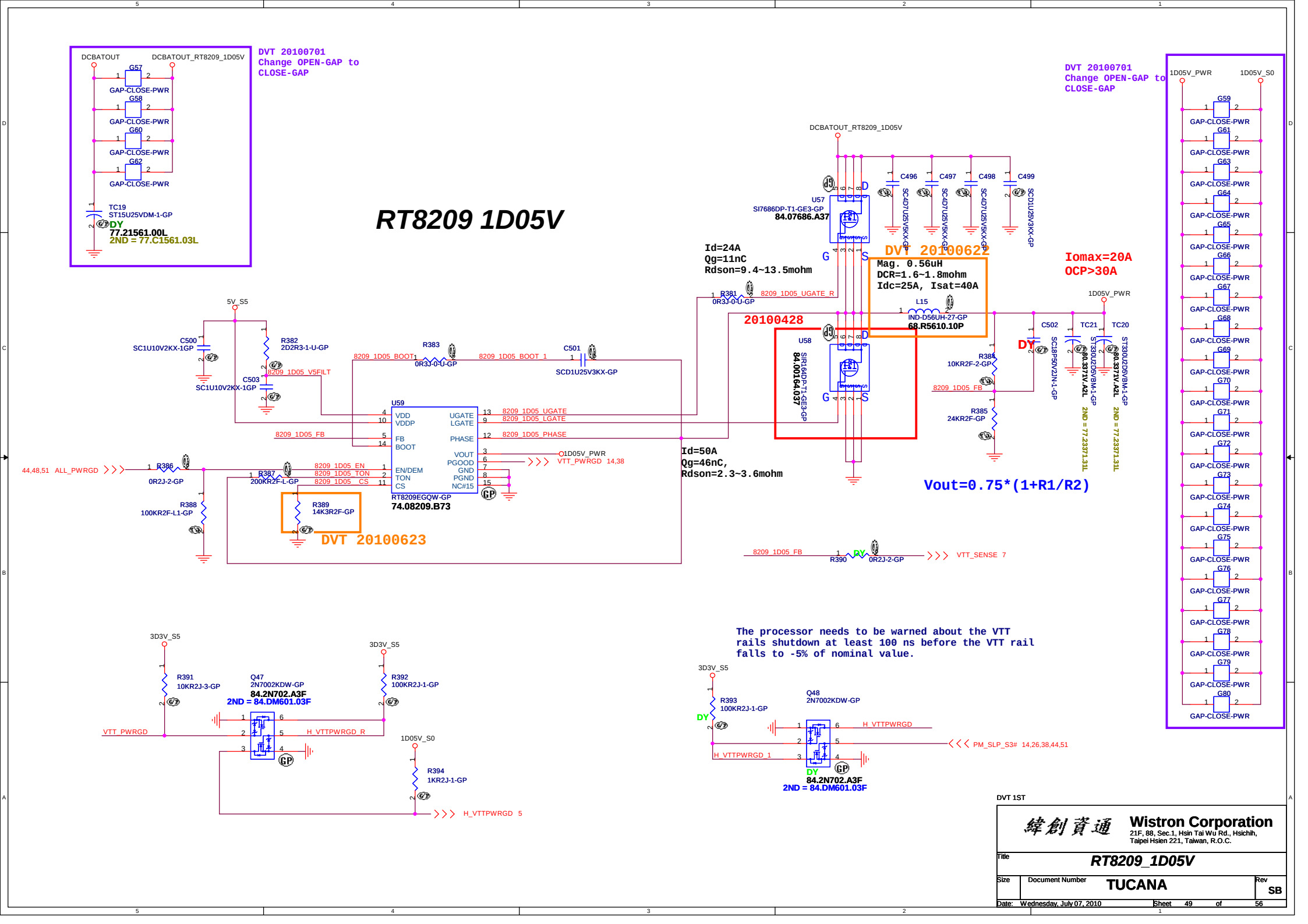
DCBATOUT
DCBATOUT_RT8209_1D05V
G57
GAP-CLOSE-PWR
G58
GAP-CLOSE-PWR
G60
GAP-CLOSE-PWR
G62
GAP-CLOSE-PWR
TC19
ST15U25VDM-1-GP
DY
77.21561.00L
2ND = 77.C1561.03L
DVT 20100701
Change OPEN-GAP to
CLOSE-GAP
RT8209 1D05V
DVT 20100701
Change OPEN-GAP to
CLOSE-GAP
1D05V_PWR
1D05V_S0
G59
G61
G63
G64
G65
G66
G67
G68
G69
G70
G71
G72
G73
G74
G75
G76
G77
G78
G79
G80
DCBATOUT_RT8209_1D05V
U57
SI7686DP-T1-GE3-GP
84.07686.A37
C496
C497
C498
C499
SC4D7U25V5KX-GP
SCD1U25V3KX-GP
Id=24A
Qg=11nC
Rdson=9.4~13.5mohm
DVT 20100622
Mag. 0.56uH
DCR=1.6~1.8mohm
Idc=25A, Isat=40A
Iomax=20A
OCP>30A
20100428
R381
0R3J-0-U-GP
8209_1D05_UGATE_R
L15
IND-D56UH-27-GP
68.R5610.10P
1D05V_PWR
5V_S5
C500
SC1U10V2KX-1GP
C503
SC1U10V2KX-1GP
R382
2D2R3-1-U-GP
8209_1D05_V5FILT
R383
0R3J-0-U-GP
8209_1D05_BOOT
8209_1D05_BOOT_1
C501
SCD1U25V3KX-GP
U59
VDD
VDDP
FB
BOOT
EN/DEM
TON
CS
UGATE
LGATE
PHASE
VOUT
PGOOD
GND
PGND
NC#15
RT8209EGQW-GP
74.08209.B73
8209_1D05_UGATE
8209_1D05_LGATE
8209_1D05_PHASE
8209_1D05_FB
8209_1D05_EN
8209_1D05_TON
8209_1D05_CS
1D05V_PWR
VTT_PWRGD 14,38
44,48,51 ALL_PWRGD
R386
0R2J-2-GP
R387
200KR2F-L-GP
R388
100KR2F-L1-GP
R389
14K3R2F-GP
DVT 20100623
U58
SIR164DP-T1-GE3-GP
84.00164.037
Id=50A
Qg=46nC,
Rdson=2.3~3.6mohm
R384
10KR2F-2-GP
R385
24KR2F-GP
C502
SC18P50V2JN-1-GP
DY
TC21
TC20
ST330U2D5VBM-1-GP
80.337V1.A2L
2ND = 77.23371.31L
Vout=0.75*(1+R1/R2)
8209_1D05_FB
R390
DY
0R2J-2-GP
VTT_SENSE 7
3D3V_S5
R391
10KR2J-3-GP
Q47
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
R392
100KR2J-1-GP
VTT_PWRGD
H_VTTPWRGD_R
1D05V_S0
R394
1KR2J-1-GP
H_VTTPWRGD 5
The processor needs to be warned about the VTT
rails shutdown at least 100 ns before the VTT rail
falls to -5% of nominal value.
3D3V_S5
R393
100KR2J-1-GP
DY
Q48
2N7002KDW-GP
H_VTTPWRGD
H_VTTPWRGD_1
PM_SLP_S3# 14,26,38,44,51
DY
84.2N702.A3F
2ND = 84.DM601.03F
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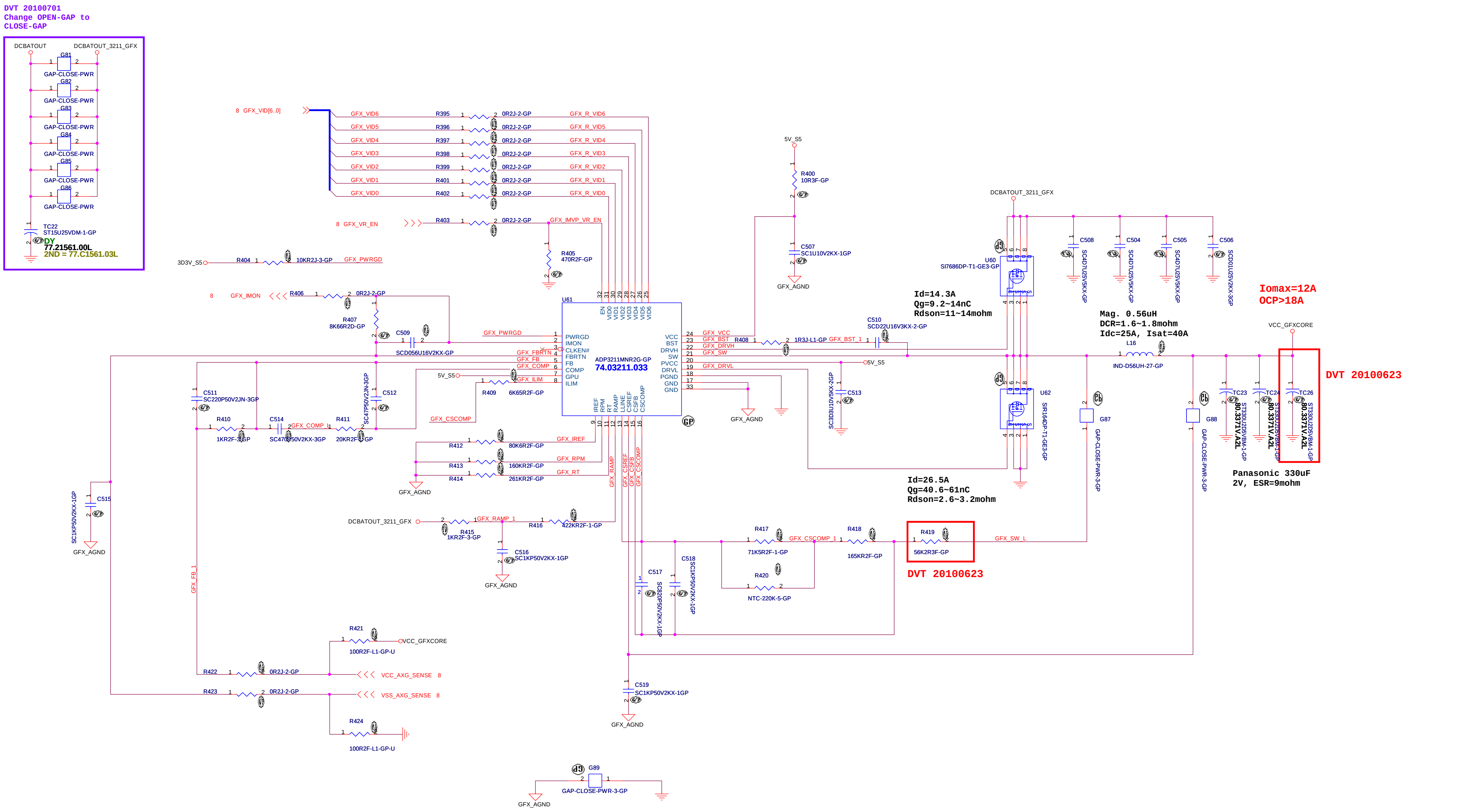

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Title			
ADP3211_GFX_CORE			
Size: A2	Document Number: TUCANA		Rev: SB
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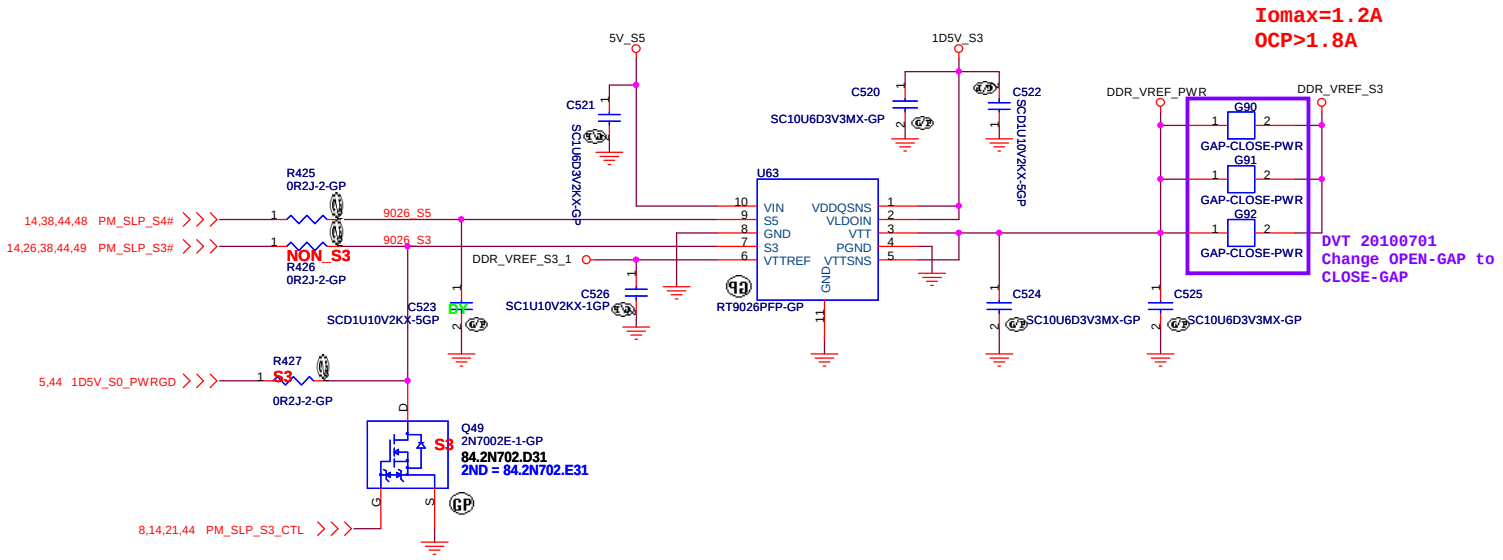
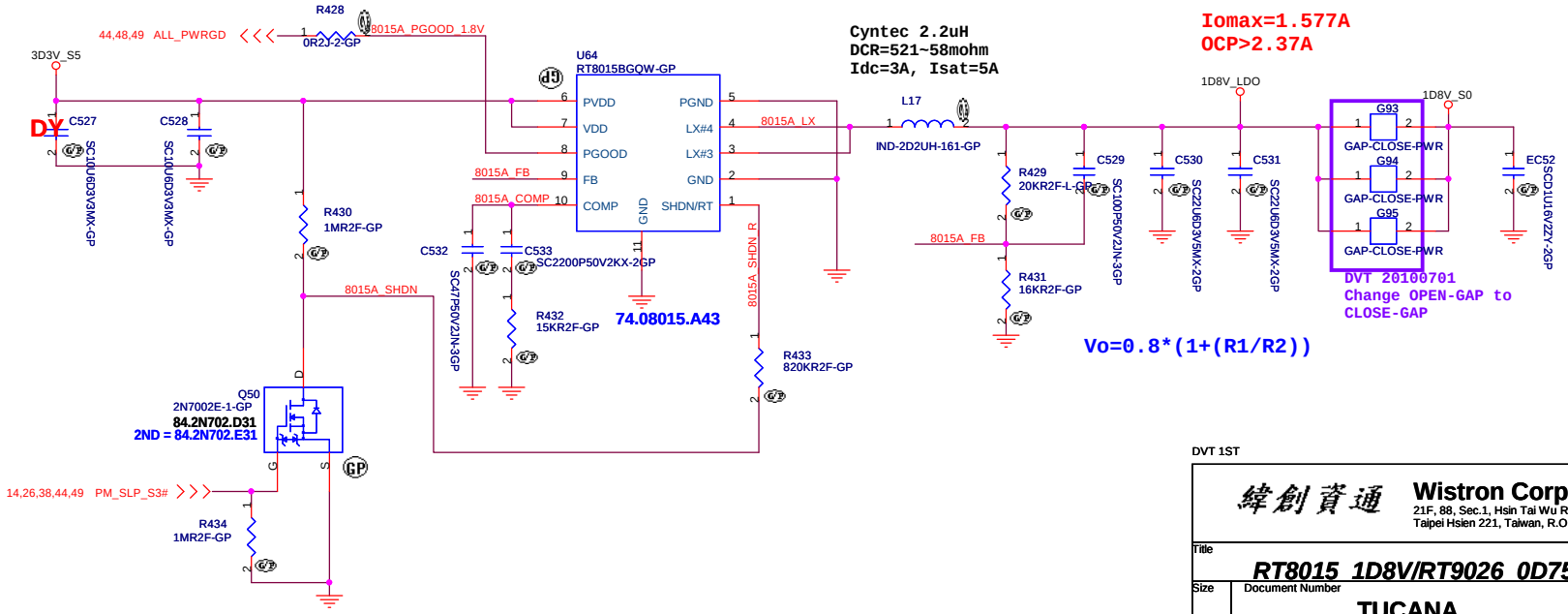
RT9026 for 0D75V_S3



RT8015 for 1D8V_S0



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Title: ***RT8015_1D8V/RT9026_0D75***

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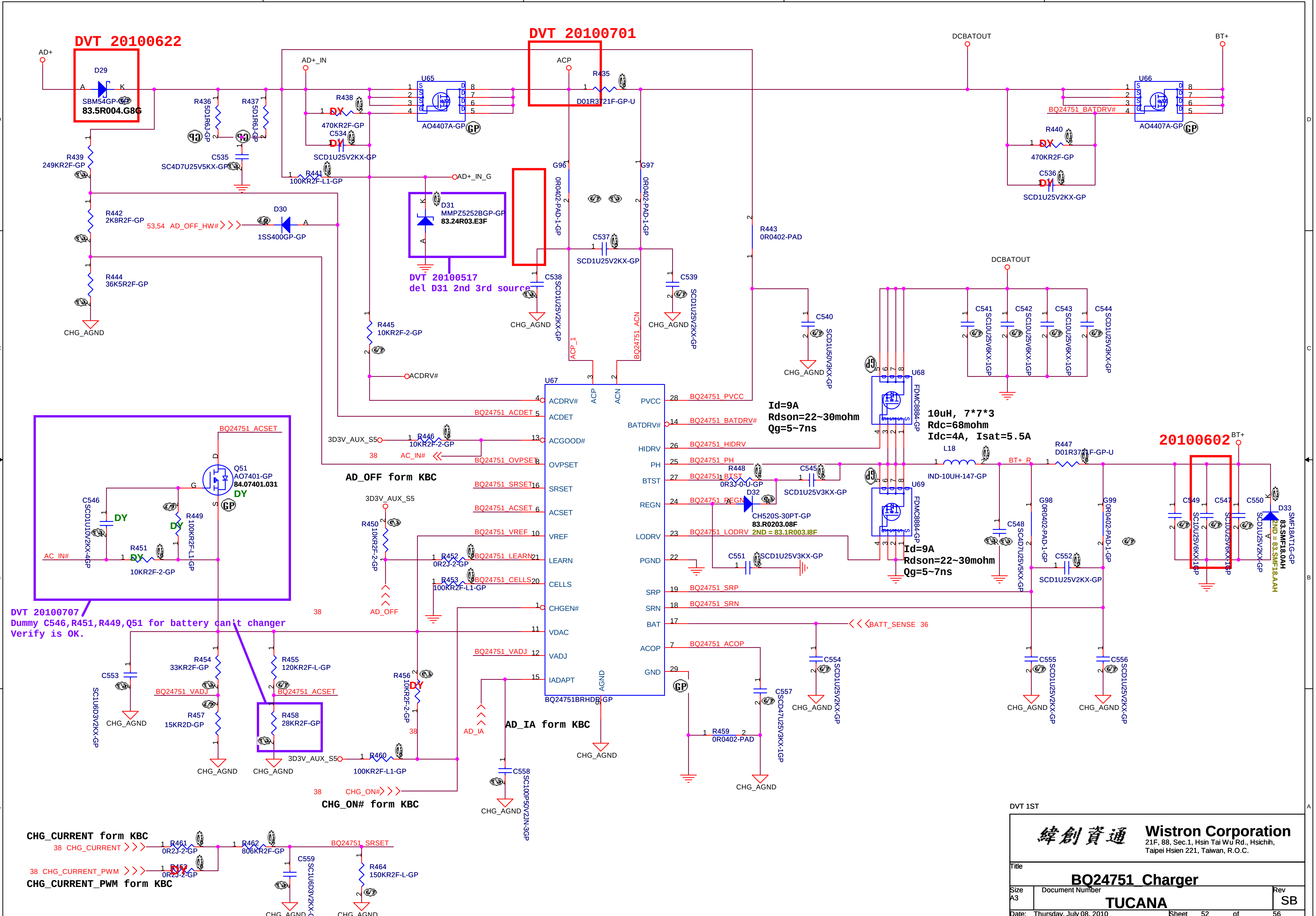

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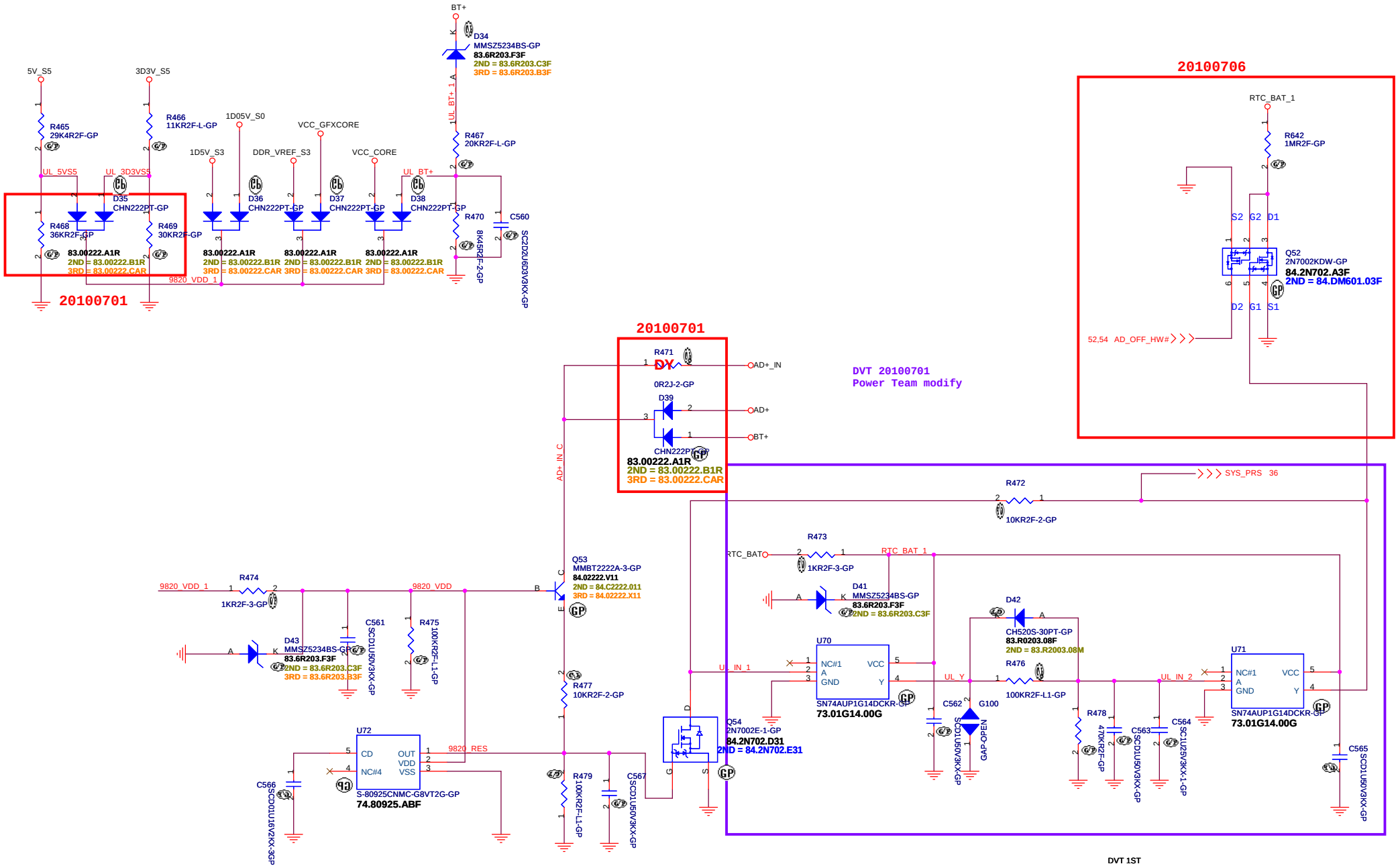
Title	BQ24751_Charger	
Size A3	Document Number TUCANA	Rev SB
Date: Thursday, July 08, 2010	Sheet 52 of 56	



DVT 1ST

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Taipei Hsien 221, Taiwan, R.O.C.

Title: UL circuit

Size: A3 | Document Number: TUCANA | Rev: SB

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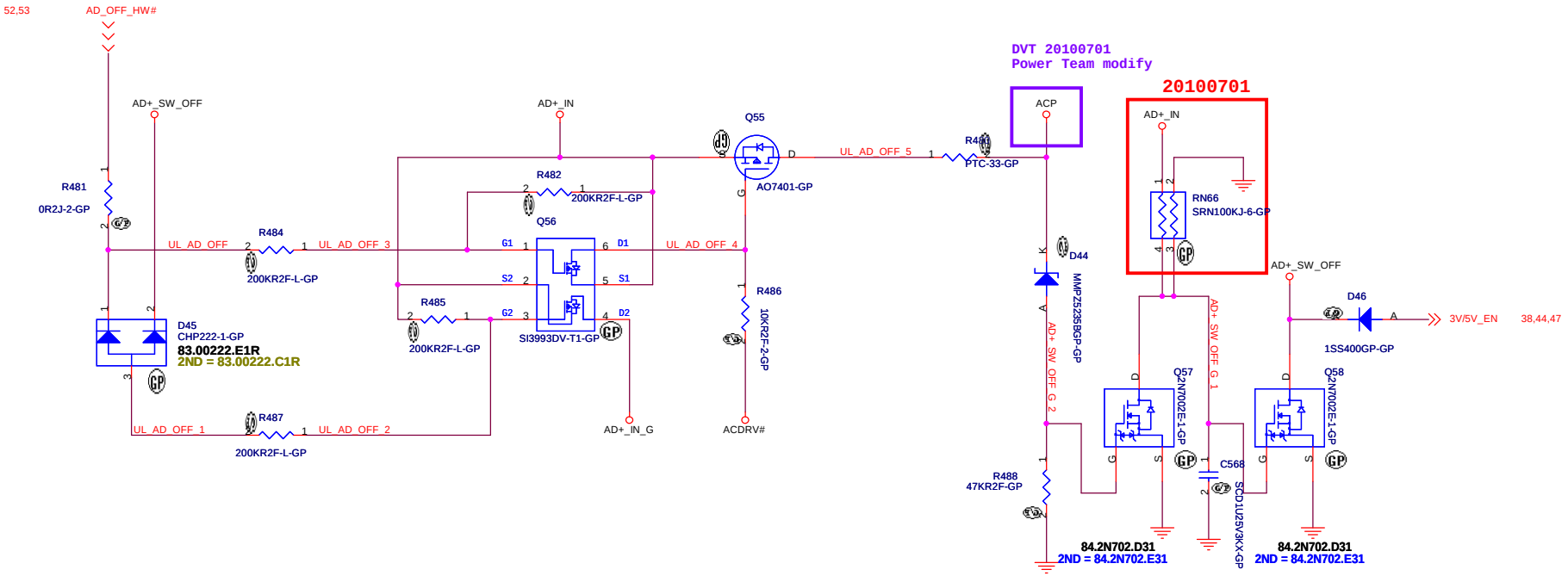

DVT 1ST

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Title: UVP Protect

Size: A3 | Document Number: TUCANA | Rev: SB

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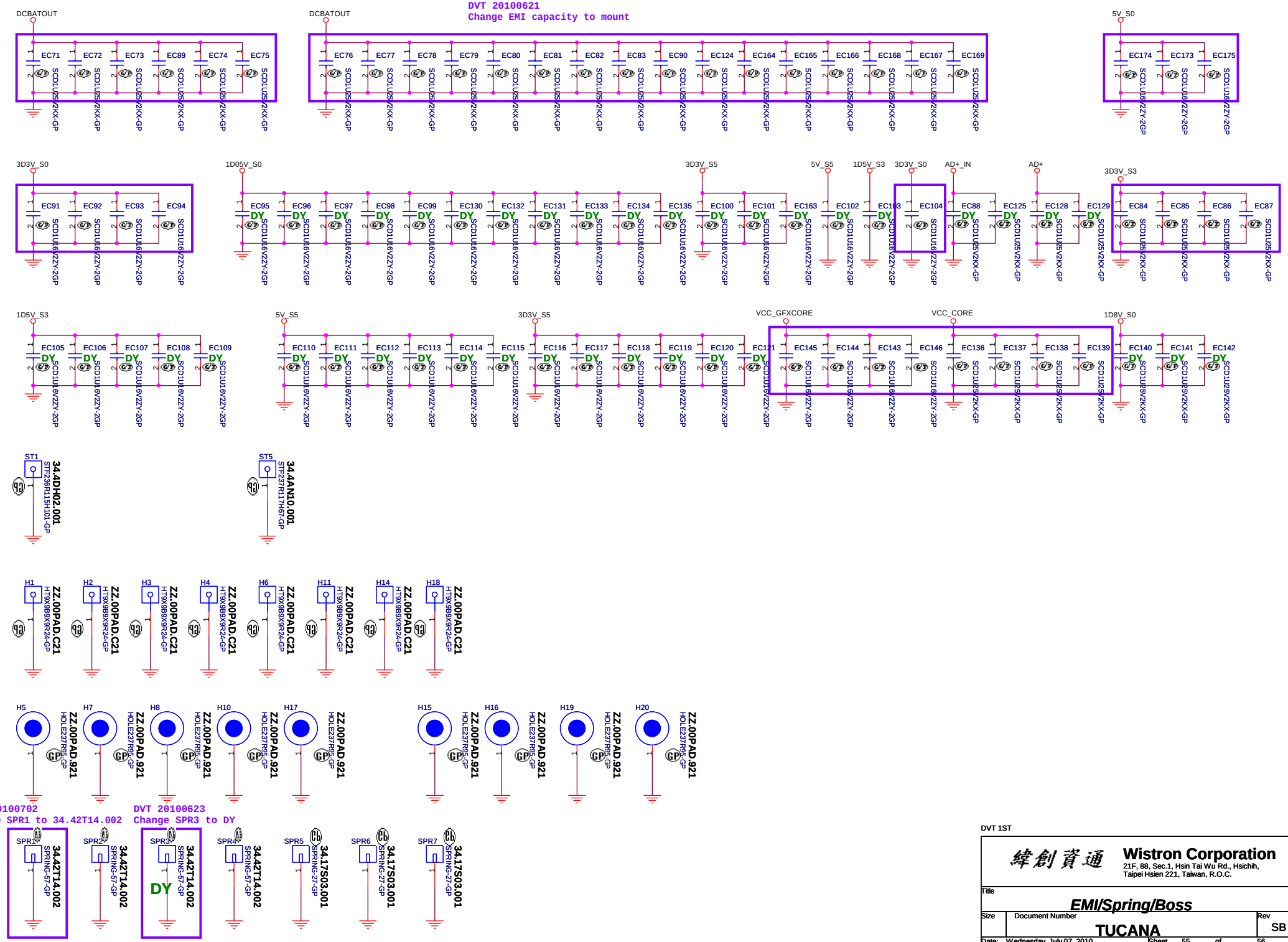
DVT 20100621
Change EMI capacity to mount
DCBATOUT
DCBATOUT
5V_S0
EC71 EC72 EC73 EC89 EC74 EC75
EC76 EC77 EC78 EC79 EC80 EC81 EC82 EC83 EC90 EC124 EC164 EC165 EC166 EC168 EC167 EC169
EC174 EC173 EC175
SCD1U25V2KX-GP
SCD1U16V2ZY-2GP
3D3V_S0
1D05V_S0
3D3V_S5
5V_S5
1D5V_S3
3D3V_S0
AD+_IN
AD+
3D3V_S3
EC91 EC92 EC93 EC94
EC95 EC96 EC97 EC98 EC99 EC130 EC132 EC131 EC133 EC134 EC135
EC100 EC101 EC163
EC102
EC103
EC104
EC88 EC125
EC128 EC129
EC84 EC85 EC86 EC87
SCD1U16V2ZY-2GP
SCD1U25V2KX-GP
1D5V_S3
5V_S5
3D3V_S5
VCC_GFXCORE
VCC_CORE
1D8V_S0
EC105 EC106 EC107 EC108 EC109
EC110 EC111 EC112 EC113 EC114 EC115
EC116 EC117 EC118 EC119 EC120 EC121
EC145 EC144 EC143 EC146
EC136 EC137 EC138 EC139
EC140 EC141 EC142
SCD1U16V2ZY-2GP
SCD1U25V2KX-GP
ST1
34.4DH02.001
STF236FR115H101-GP
ST5
34.4AN10.001
STF237FR117H67-GP
H1 H2 H3 H4 H6 H11 H14 H18
ZZ.00PAD.C21
HT9X9B9X9R24-GP
H5 H7 H8 H10 H17 H15 H16 H19 H20
ZZ.00PAD.921
HOLE237R95-GP
DVT 20100702
Change SPR1 to 34.42T14.002
DVT 20100623
Change SPR3 to DY
SPR1 SPR2 SPR3 SPR4
34.42T14.002
SPRING-57-GP
DY
SPR5 SPR6 SPR7
34.17S03.001
SPRING-27-GP
DVT 1ST
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Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
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EVT

2010/5/17	P.52[BQ24751_Charger]	Del D31 2nd 3rd source
2010/5/17	P.25[HDMI CONN_PS8101]	Change 2nd source to 69.4R500.151
2010/5/24	P.26[HDD Connector]	Change R148 to 3.3K ohm ,add C437 for PM_SLP_S3# Delay
2010/5/27	P.38[KBC_NPCE781L / KB]	Add LCD_DETECT pull-high to 3D3V_S5
2010/5/31	P.52[BQ24751_Charger]	Mount C546,R451,R449,Q51 for battery can't Changer
2010/6/1	P.24[CRT CONN]	Change F6 to 69.44002.001, for Cadiz use
2010/6/4	P.33[Audio Jack]	Change MICIN1 to 20.10133.L11 , follow connector list
	P.28[USB]	Change USB1,USB2,USB3 connector to 22.10321.Q71 [follow ME connector list]
2010/6/10	P.36[AD / BATT CONN]	Change DCIN1 to 20.F0693.006 (follow connector list)
	P.41[FUNCTION BD & POWER BD]	Change PWCN1 to 20.F0693.006 (follow connector list)
2010/6/11	P.41[FUNCTION BD & POWER BD]	Del FUNCN2 connector by ME request
	P.38[KBC_NPCE781L / KB]	Change R240 to 20K ohm SB version.
	P.25[HDMI CONN_PS8101]	Change R614~R617 to 200R2J , Set mount. [for EMI request]
	P.25[HDMI CONN_PS8101]	Change C283,C364 to 1uF [for EMI request]
	P.25[HDMI CONN_PS8101]	Change C282,C285 to 1KpF [for EMI request]
2010/6/21	P.16[PCH (5 of 9)-PCI/USB]	Add PCI_REQ2# Pull-High to 3D3V_S0 by hang-up issue
	P.31[Audio Codec ALC269]	Change EC23,EC24 to mount [for EMI request]
	P.55[EMI/Spring/Boss]	Change DCBATOUT capacity to mount (EC71~83,EC89,EC90,EC124,EC164~169) [for EMI request]
		Change 5V_S0 capacity to mount (EC173~EC175) [for EMI request]
		Change 3D3V_S0 capacity to mount (EC91~94,EC104) [for EMI request]
		Change 3D3V_S3 capacity to mount (EC84~87) [for EMI request]
		Change VCC_GFXCORE capacity to mount (EC142~146) [for EMI request]
		Change VCC_CORE capacity to mount (EC136~139) [for EMI request]
	P.36[AD / BATT CONN]	Change BT+ capacity to mount (EC32~35) [for EMI request]
	P.23[LCD CONN]	Change C258 to 470pF (BRIGHTNESS_CN) [for EMI request]
		Add C272 between BLON_OUT_R and Gnd [for EMI request]
	P.34[CardReader RTS5186]	Change C576~580,C589 to 5pF [CardReader VEVS test]
		Add 0.1uF between MS_INS# and GND [CardReader VEVS test]
	P.24[CRT CONN]	Change R114,R115,R119,R120 to 2.7K ohm [CRT VEVS report]
2010/6/22	P.53[UL CIRCUIT]	UL Circuit modify. [Prevent the RTC_BAT keep protecting.]
2010/6/23	P.40[TouchPad]	Change THPAD1 to 20.K0487.006 [Follow ME connector list]
	P.55[EMI/Spring/Boss]	Change SPR3 to DY [for EMI request]
	P.53[UL CIRCUIT]	Add D42(83.00400.D1F), D41(83.00400.D1F) components. [Reduce the RTC_BAT discharge]
		connect R467 pin1 to D41 and D42 pin k. [Reduce the RTC_BAT discharge]
		connect D42 pin A to AD+_in. [Reduce the RTC_BAT discharge]
		connect D41 pin A to ACP_UVP [Reduce the RTC_BAT discharge]
	P.46[ADP3211_CPU CORE]	Change U45 to 84.08030.037 [Improve High side Vgs induce voltage]
		Change U47 to 84.08028.037 [Improve High side Vgs induce voltage]
		Change U48 to 84.08028.037 [Improve High side Vgs induce voltage]
		add these statements. [follow Power Team design]
		Change R316 to 7.87K ohm (old use 7.32K ohm) [Tune CPU Imon value]
		Change C465 to 680pF (old use 560pF) [Tune CPU load line value]
	P.47[RT8223_5V/3D3V]	Change R353 to 84.5K ohm (old use 97.6K ohm) [Adjust OCP value]
		Change L13 to 2.2uH (old use 3.3uH) [IC needs highter sensing voltage to detect it.]
	P.48[RT8209_1D5V]	Change R377 to 7.5K ohm (old use 11.5K ohm) [Adjust OCP value]
	P.49[RT8209_1D05V]	Change R389 to 14.3K ohm (old use 10.2K ohm) [Adjust OCP value]
		Change L15 to 0.56uH (old use 0.45uH) [Reduce the output ripple voltage]
	P.50[ADP3211_GFX_CORE]	Change R419 to 56.2K ohm (old use 53.6K ohm) [Tune GFX load line value]
		Change TC26 to mount.(old Dummy) [Improve under-shoot voltage phenomenon]
2010/6/25	P.13[PCH (2 of 9)-PCIE/CLK/SMB]	Change C156,C157 to 12pF [for Crystal vendor Test]
	P.29[LAN AR8131M]	Change C346 to 18pF [for Crystal vendor Test]
	P.34[CardReader RTS5186]	Change C384,C388 to 15pF [for Crystal vendor Test]
2010/6/29	P.17[PCH (6 of 9)-GPIO/RSVD]	Change RN31 to R648,R649 (56 ohm) for pull-high 1.05V_S0
		Del R295 , because double pull-high
2010/6/30	P.41[FUNCTION BD & POWER BD]	Change pin define of the FUNCN1 connector [follow the way of FFC folder for ME]
	P.19[PCH (8 of 9)-PWR\SATA\USB]	Del R101 , only use 3D3V_S5
	P.12[PCH (1 of 9)-SATA/RTC/HDA]	Change D1 to 83.R2003.I81 (SCHOTTKY DIODE)
	P.25[HDMI CONN_PS8101]	Change Q12 to 84.2N702.D31 (ESD Protected 1.0KV)
	P.44[RUN POWER]	Change D27 to 83.R2004.B8F (schottky diode)
2010/7/1	P.46[ADP3211_CPU CORE]	Change OPEN-GAP to CLOSE-GAP (G9~14)
	P.47[RT8223_5V/3D3V]	Change OPEN-GAP to CLOSE-GAP (G18,G22,G26,G30,G20,G24,G28,G32)
		Change OPEN-GAP to CLOSE-GAP (G19,G23,G27,G31,G34,G36)
		Change OPEN-GAP to CLOSE-GAP (G21,G25,G29,G33,G35,G37,G38)
	P.48[RT8209_1D5V]	Change OPEN-GAP to CLOSE-GAP (G47,G49,G51,G53)
		Change OPEN-GAP to CLOSE-GAP (G43~46,G48,G50,G52,G54~56)
	P.49[RT8209_1D05V]	Change OPEN-GAP to CLOSE-GAP (G57,G58,G60,G62)
		Change OPEN-GAP to CLOSE-GAP (G59,G61,G63~80)
	P.50[ADP3211_GFX_CORE]	Change OPEN-GAP to CLOSE-GAP (G81~86)
	P.51[RT8015_1D8V/ RT9026_0D75]	Change OPEN-GAP to CLOSE-GAP (G90~95)
	P.41[FUNCTION BD & POWER BD]	Add F7 POLYSW for POWER BD 5V_S5 protect.
	P.54[UVP Protect]	Delete R483 and add RN66. (RN66 part number is 66.10436.04L)
		Connect AD+_IN to RN66 pin 1.
		Connect RN66 pin2 to GND.
		Connect RN66 pin3 and pin4 to AD+_SW_OFF_G_1
	P.53[UL CIRCUIT]	Change R468 part number to the 64.36025.6DL
		Change R469 to the part number 64.30025.6DL
		Cummy R471 and mount D39.
		Delete D40 and RN58.
		Add R642. (Part number is 64.10045.6DL)
		Connect R642 pin 1 to RTC_BAT.
		Connect R642 pin2 to Q52 pin 2 and pin3.
	P.52[BQ24751_Charger]	Connect ACP to R435 pin 1.
	P.27[Bluetooth]	UPDATE BTCN1 PCB LAYOUT (REMOVE THE NPTH)
2010/7/2	P.38[KBC_NPCE781L / KB]	Rename H_PROCHOT# to EC_PROCHOT
	P.5[CPU SFF(2 of 8)-CLK/Thermal]	Add R128 for EC_PROCHOT pull-low to Gnd
	P.5[CPU SFF(2 of 8)-CLK/Thermal]	Add Q61 for EC_PROCHOT to PROCHOT#
	P.33[Audio Jack]	Add EC176 for HP_JD# to GND , Set Dummy for ESD.
		Add EC177 for MIC1_JD# to GND , Set Dummy for ESD.
	P.55[EMI/Spring/Boss]	Change SPR1 to 34.42T14.002
2010/7/5	P.14[PCH (3 of 9)-DMI/FDI]	Change D3 to schottky diode.
	P.37[Thermal / Fan Controllor]	Delelte Q29,Q30 main source 84.T3904.C11, follow CARAVEL-CP design
2010/7/6	P.53[UL CIRCUIT]	Rename R642 Pin1 contact to RTC_BAT_1 (Old use RTC_BAT),follow CARAVEL-CP