CANTERBURY
SPRINGFIELD

CPU	: INTEL DIAMONDVILLE
Chip Set	: INTEL 945GSE
Remarks	:
Model Name	: CANTERBURY SPRINGFIELD
PCB Part No	: BA41-01122A (GCE) BA41-01123A (NY) BA41-01124A (HST) BA41-01125A (TRI)
Dev. Step	: PR1
Revision	: 1.0
T.R. Date	: 2009.07.13

DRAW	CHECK	APPROVAL

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CHECK: KIM, MS	DEV. STEP: PV		
APPROVAL: CHUN, YB	REV: 1.0		PART NO.: BA41-xxxxxx
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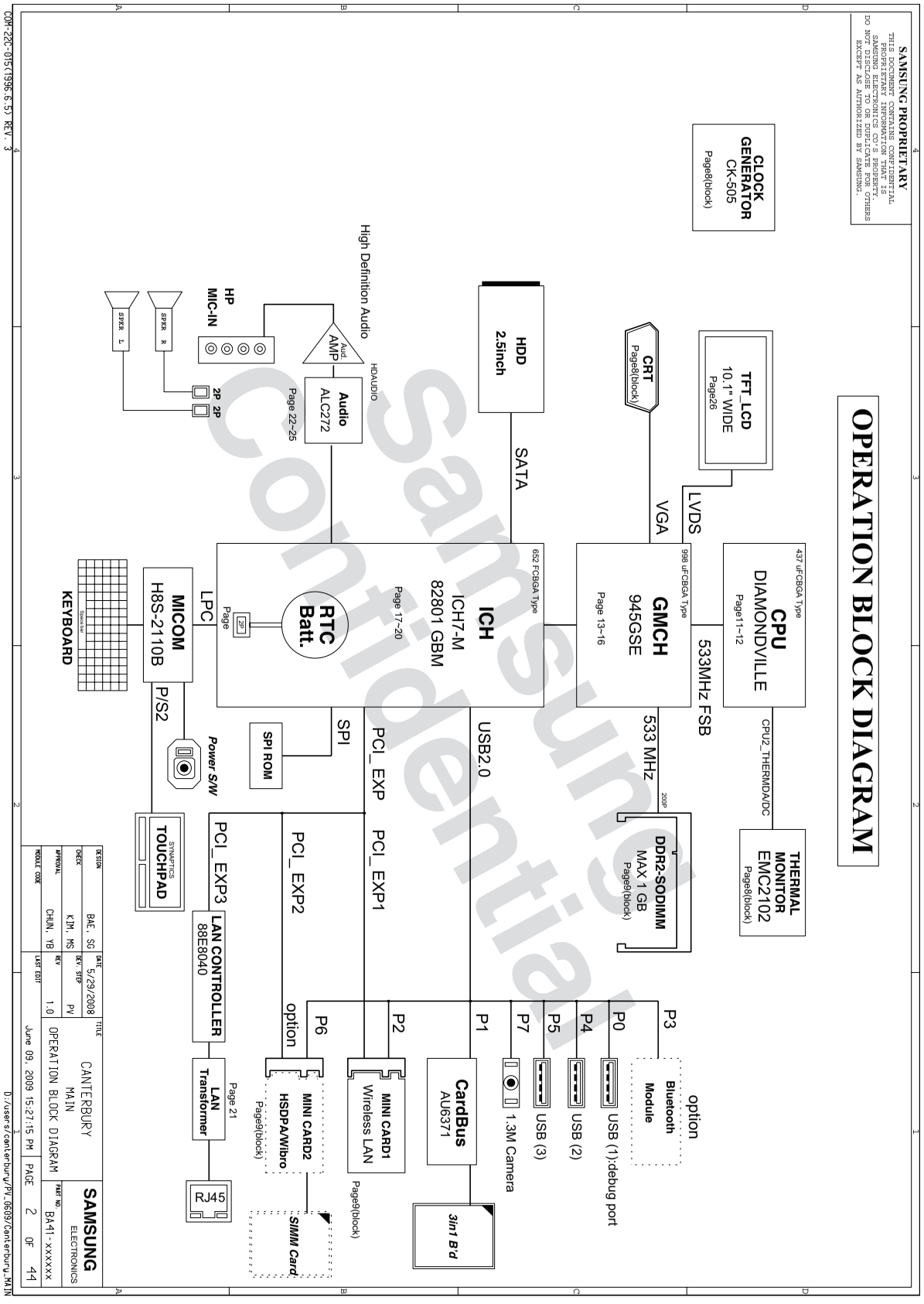
8. Block Diagram and Schematic



BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
USB	AD29(internal)	Programable	
Hub to PCI	AD30(internal)		
LPC Bridge/IDE/AC97/SMBUS	AD31(internal)		
Internal MAC	AD24(internal)		

I²C / SMB Address

Devices	Address	Hex	Bus
ICH7M	**Master**		**SMBUS Master**
CK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	-
CPU Thermal Sensor	0111 101X	7Ah	Thermal Sensor

USB PORT Assign

Port Number		ASSIGNED TO	Port Number		ASSIGNED TO
UHCI_0	0	USB PORT	UHCI_2	4	USB PORT
	1	3-IN-1		5	USB PORT
UHCI_1	2	Wireless LAN	UHCI_3	6	HSDPA
	3	BLUETOOTH		7	CAMERA

PCI Express Assign

Port Number	ASSIGNED TO
1	Mini Card 1(Wireless LAN)
2	Mini Card 2 (HSDPA/Wibro)
3	LOM

Voltage Rails

Power Rail	Descriptions
PRTC_BAT	3.3V (can drop to 2.0V min. in G3 state) supply for the RTC well.
VDC	Primary DC system power supply (9 to 19V)
P1.05V(VCCP)	VTT for CPU, Calistoga & ICH7-M
P3.3V_MICOM	3.3V always power rail(for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S4-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
CPU_CORE	Core voltage for Atom CPU

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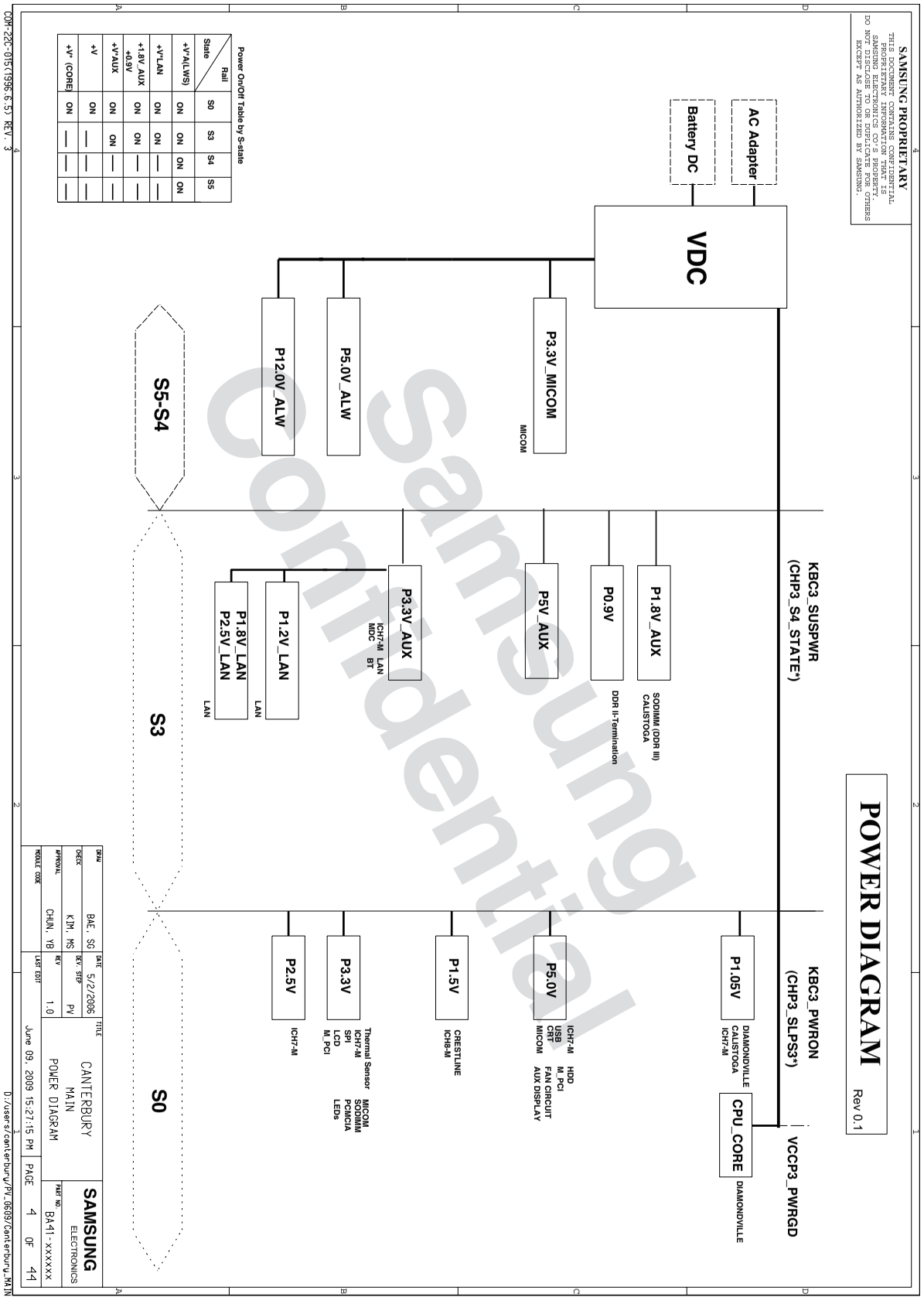
8. Block Diagram and Schematic



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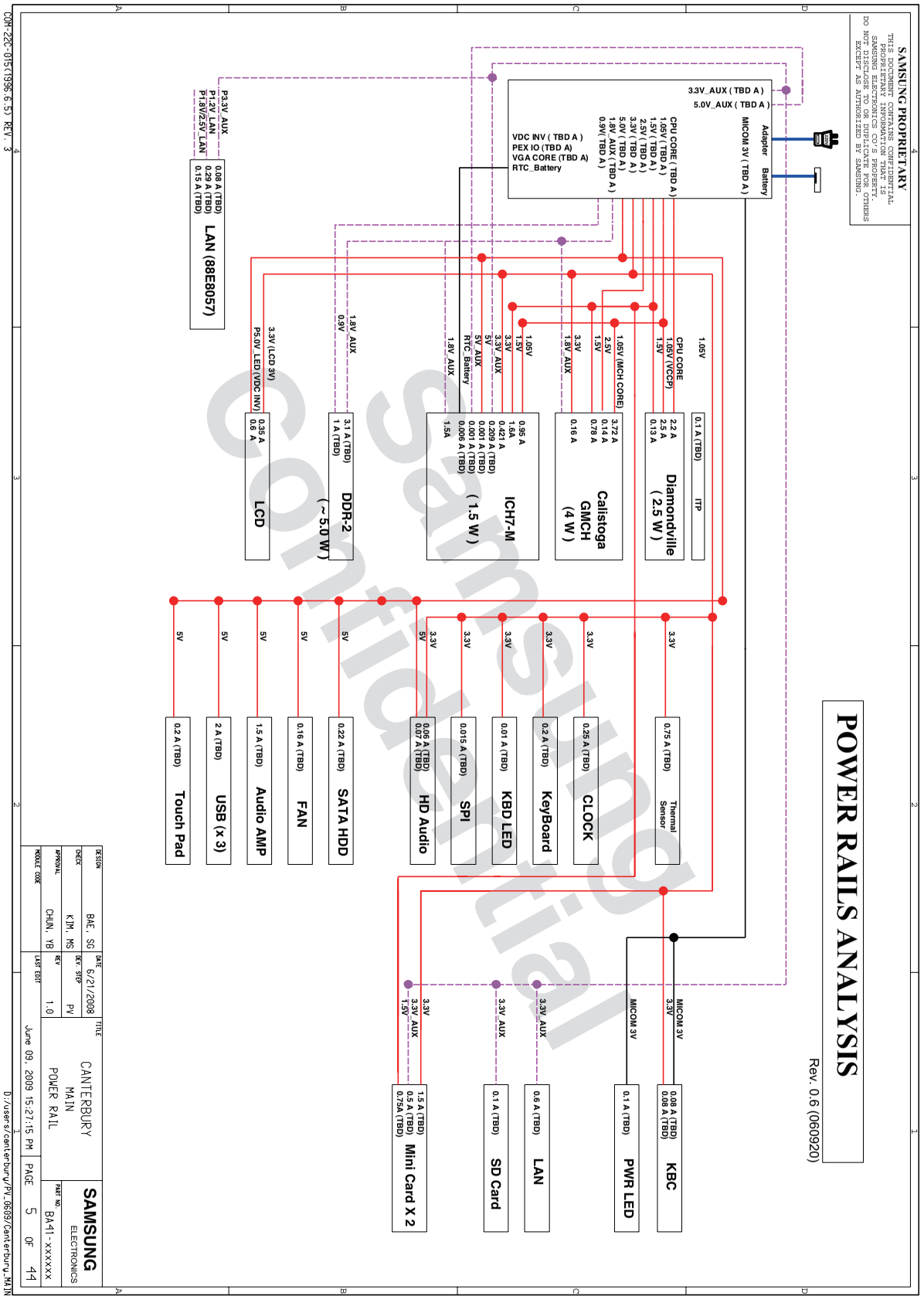

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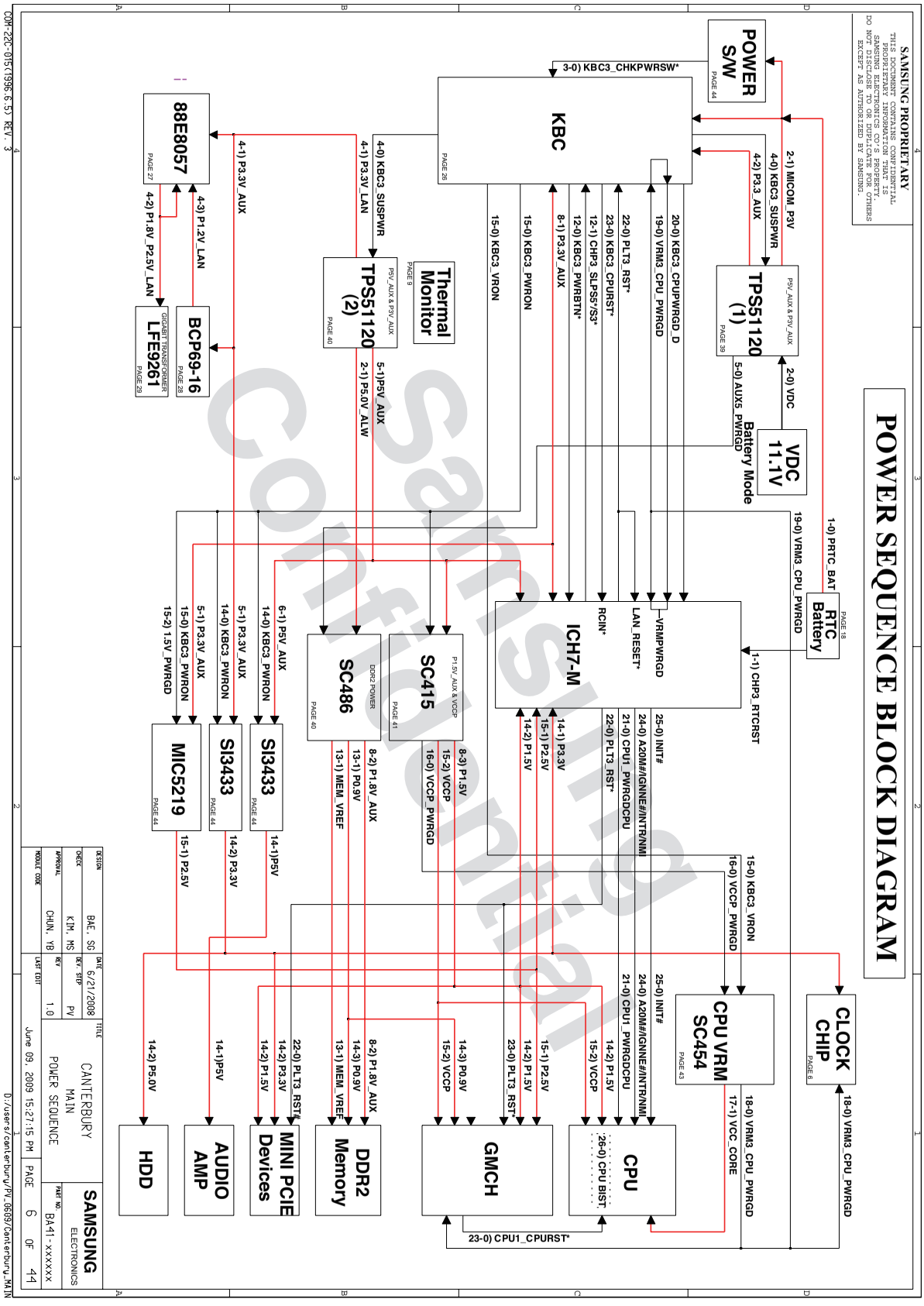

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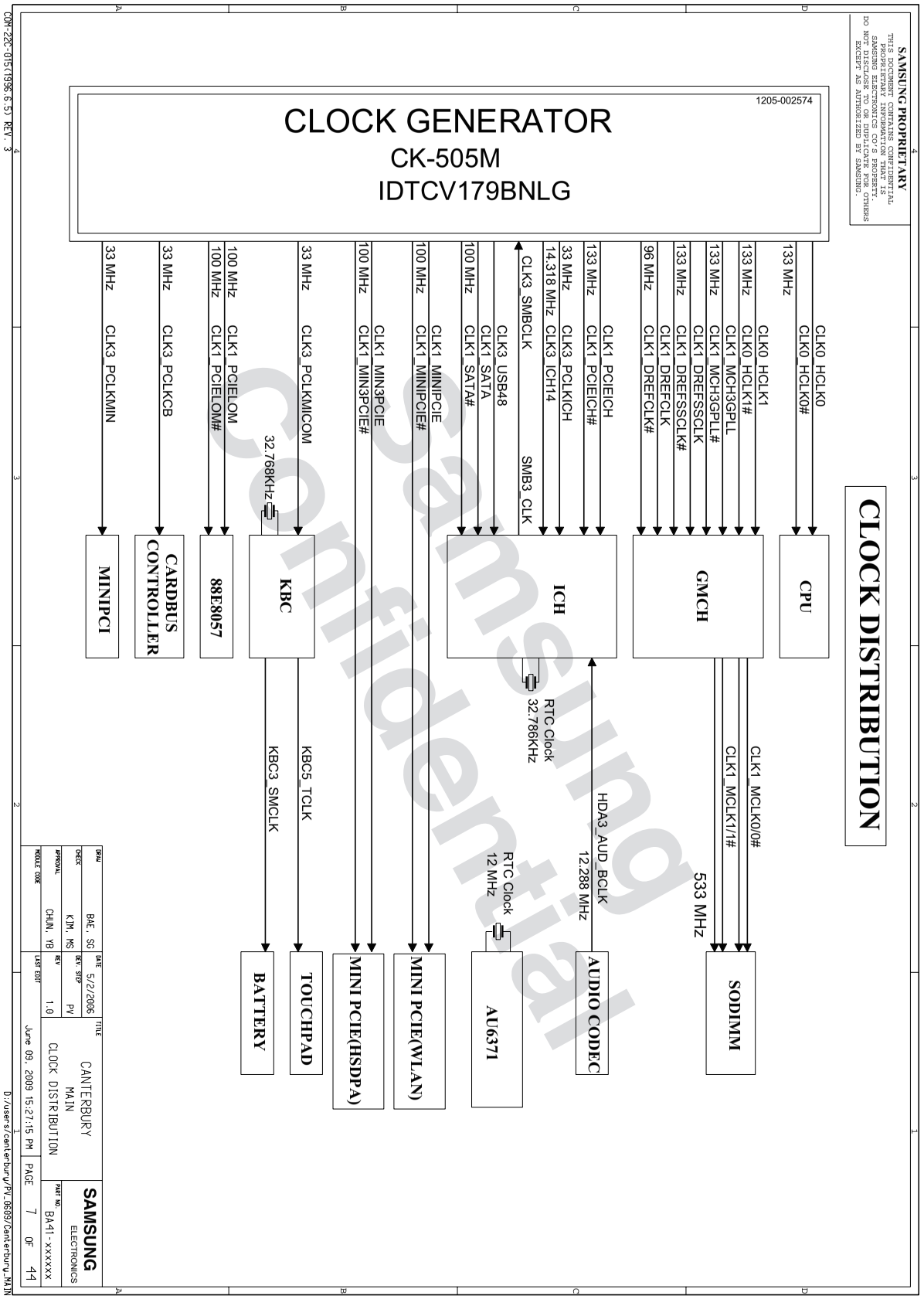
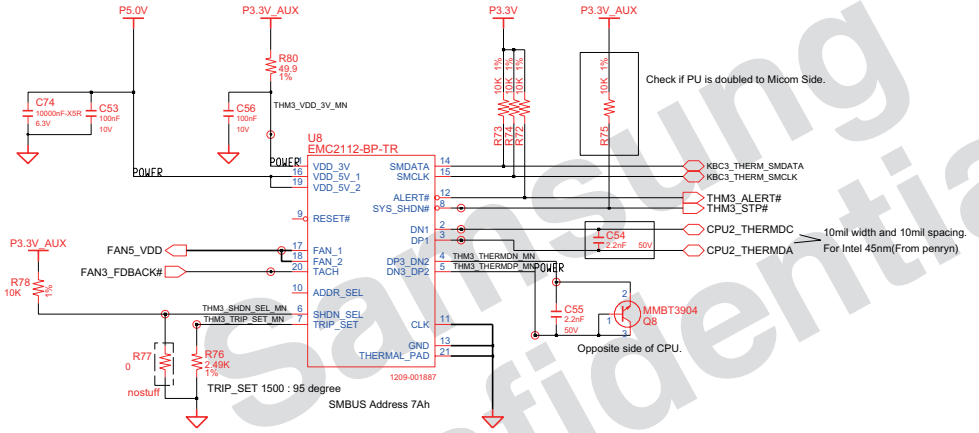
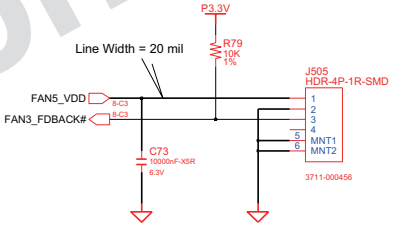


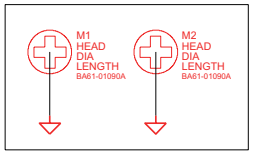
THERMAL SENSOR & FAN CONTROL



SHDN_SEL MODE	
0	INTEL TR MODE
HIGH Z	AMD CPU/DIODE MODE
✓ 1	EXT.DIODE 2 MODE

ADDRESSS_SEL MODE	
0	0101 111xb
✓ HIGH Z	0111 101xb (7A)
1	0101 110xb





To support heatsink

DESIGN	BAE, SG	DATE	6/5/2008	TITLE	CANTERBURY MAIN THERMAL SENSOR
CHECK	KIM, MS	DEV. STEP	PV		
APPROVAL	CHUN, YB	REV	1.0		
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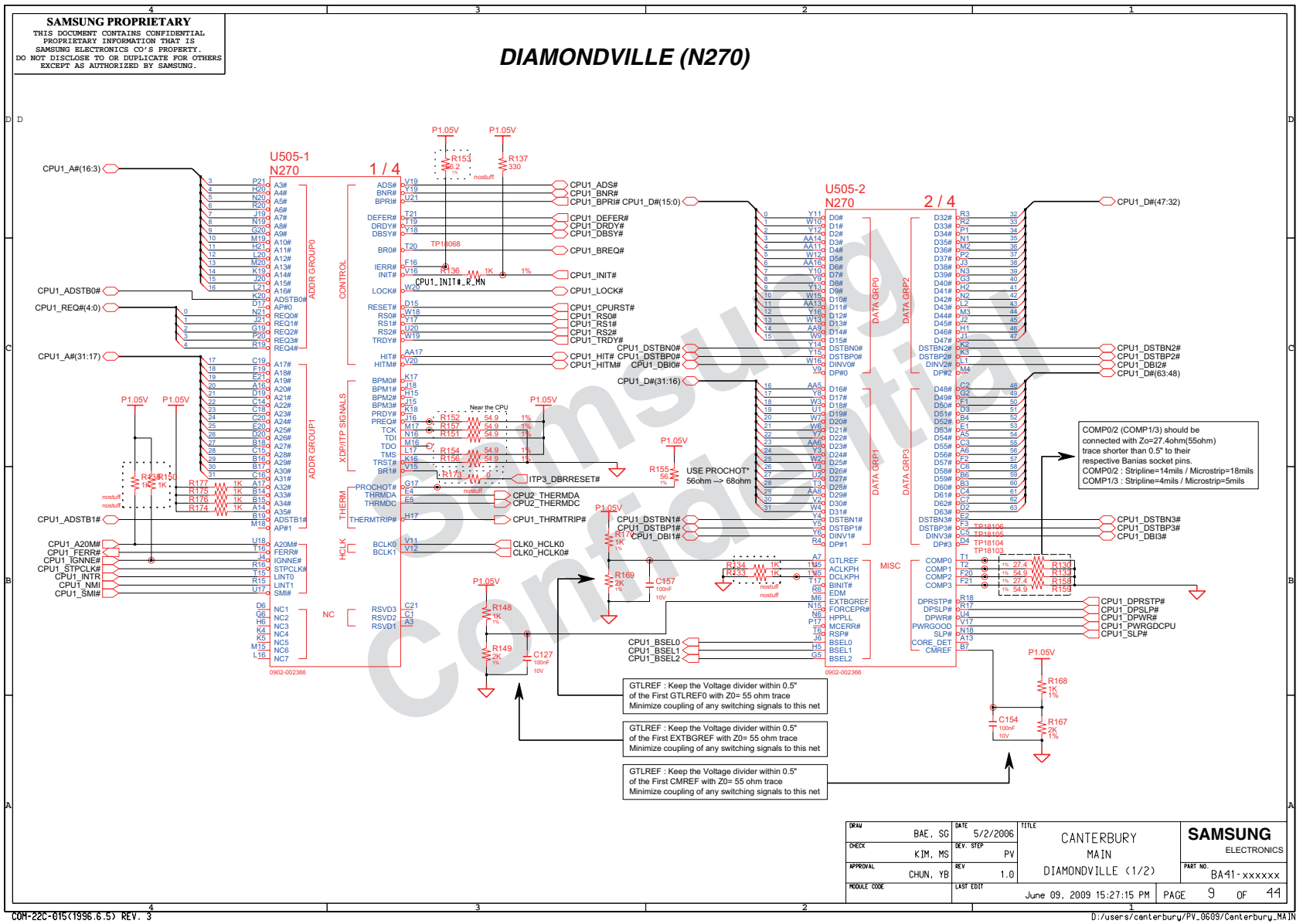
DIAMONDVILLE (N270)



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CHECK	KIM, MS	DEV. STEP	PV		SAMSUNG ELECTRONICS
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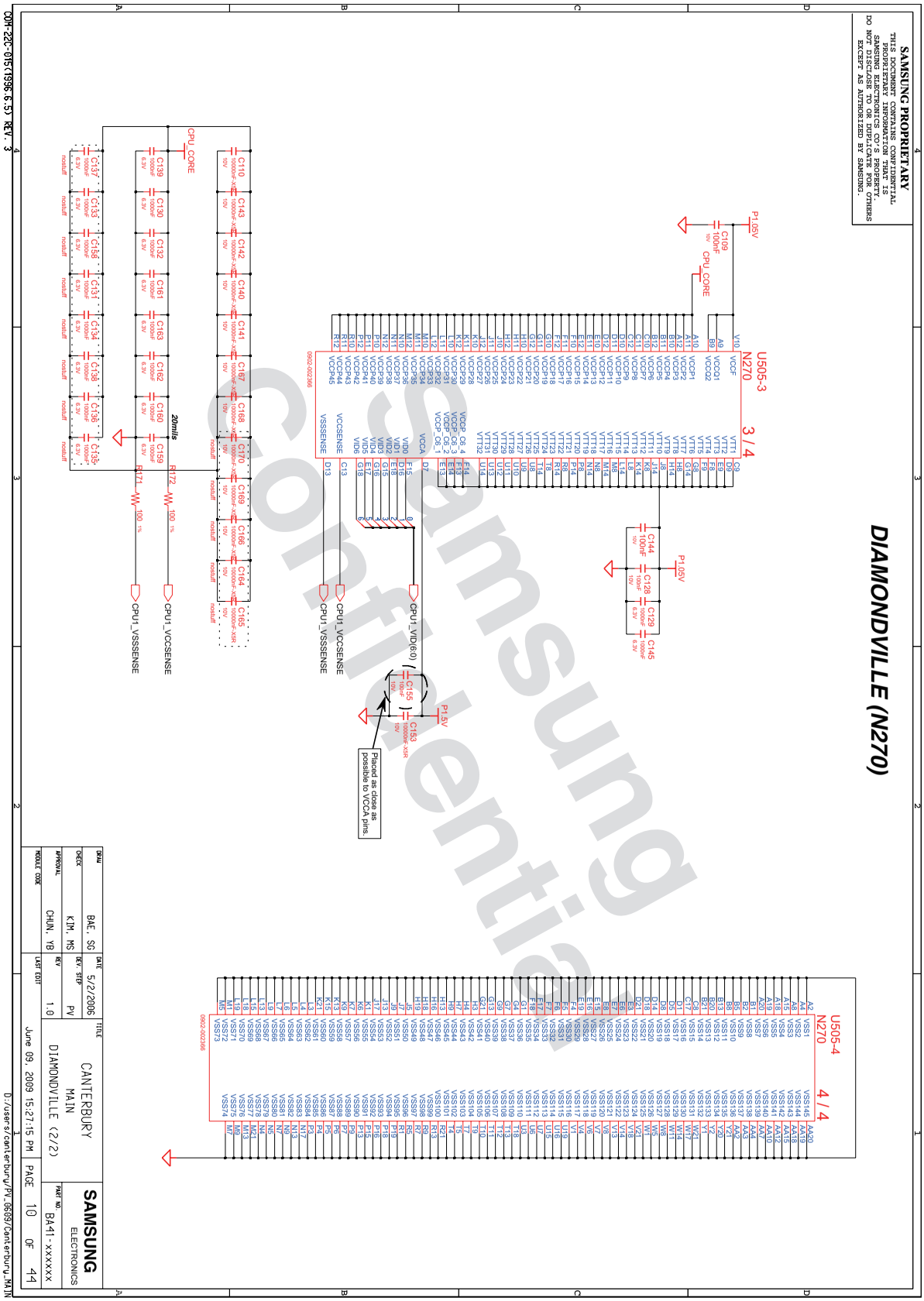

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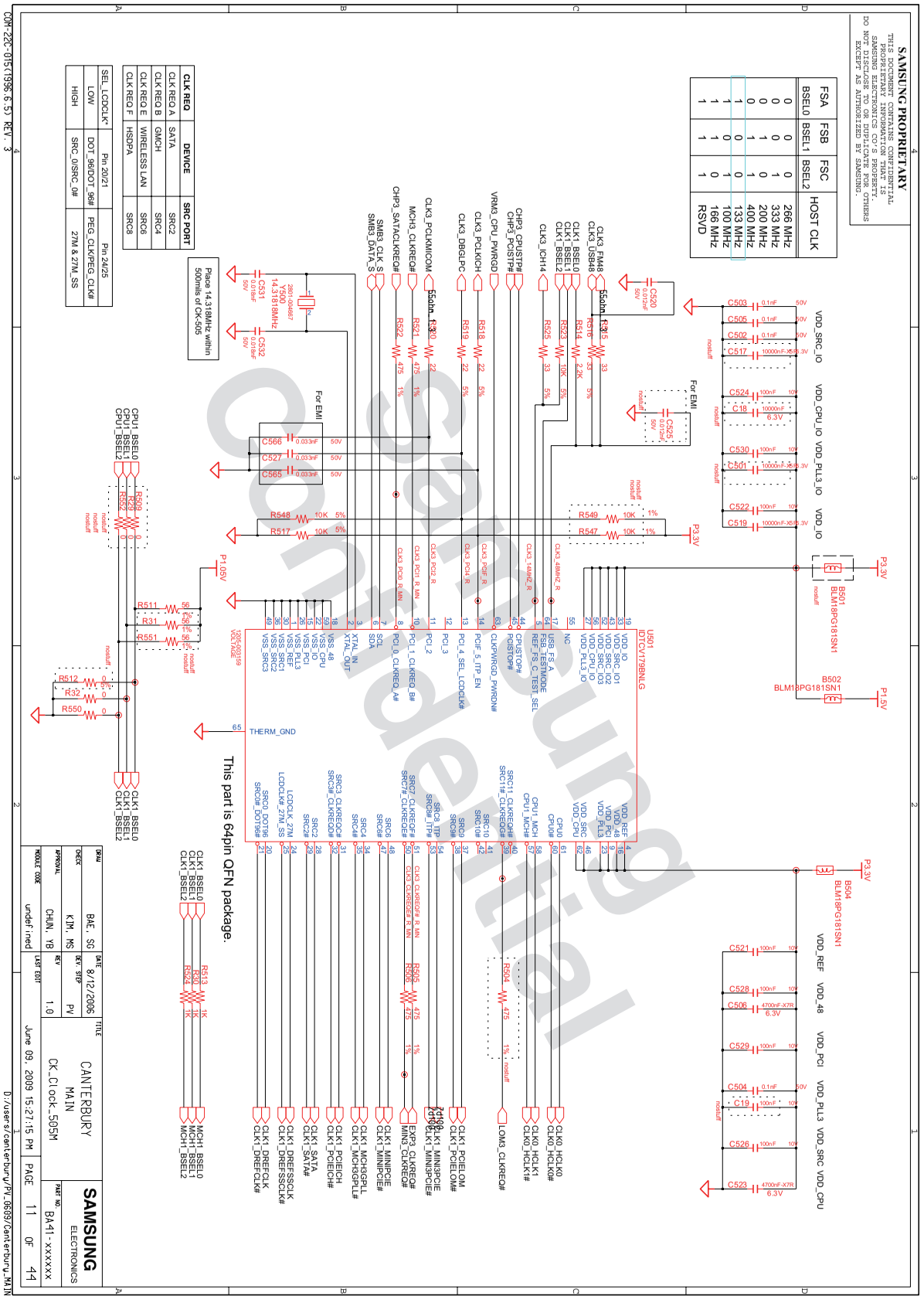

8. Block Diagram and Schematic

CALISTOGA (945GSE)

U504-1
945GSE
1 / 5
0904-002420

CPU1_D#(63:0) — HD0* … HD63*

CPU1_A#(31:3) — HA3* … HA31*

CPU1_REQ#(4:0) — HREQ0* … HREQ4*

CPU1_ADSTB0#, CPU1_ADSTB1#

HVREF0 — MCH1_HVREF

CLK0_HCLK1#, CLK0_HCLK1

CPU1_DBI0#, CPU1_DBI1#, CPU1_DBI2#, CPU1_DBI3#

CPU1_DSTBN0#, CPU1_DSTBN1#, CPU1_DSTBN2#, CPU1_DSTBN3#

CPU1_DSTBP0#, CPU1_DSTBP1#, CPU1_DSTBP2#, CPU1_DSTBP3#

CPU1_ADS#, CPU1_BNR#, CPU1_BPRI#, CPU1_BREQ#

CPU1_DBSY#, CPU1_DEFER#, CPU1_DRDY'#, CPU1_HIT#, CPU1_HITM#, CPU1_LOCK#, CPU1_TRDY#

CPU1_DPWR#, CPU1_CPURST#, CPU1_SLP#

HSLPCPU* - GMCH : Enhanced mode (def.)
HSLPCPU* - ICH : Legacy mode

P1.05V

MCH1_HXSWING — R131 54.9 1% — HXSWING
MCH1_HYSWING — R124 54.9 1% — HYSWING
R125 29.9 1% — HXRCOMP
R127 24.9 1% — HYRCOMP
width: 10mil, within 20mil

CPU1_RS0#, CPU1_RS1#, CPU1_RS2# — HRS0*, HRS1*, HRS2*

MCH1_HYSWING — R128 221 1% — C107 100nF 10V — R126 100 1% — within 20mil — **0.327V**

MCH1_HXSWING — R122 221 1% — C83 100nF 10V — R123 100 1% — within 20mil — **0.327V**

MCH1_HVREF — R129 100 1% — C106 10V — R125 200 1% — nearby Pin J13 — **0.7V**

Layout Note
Place 100nF within 100mils near HVREF pin

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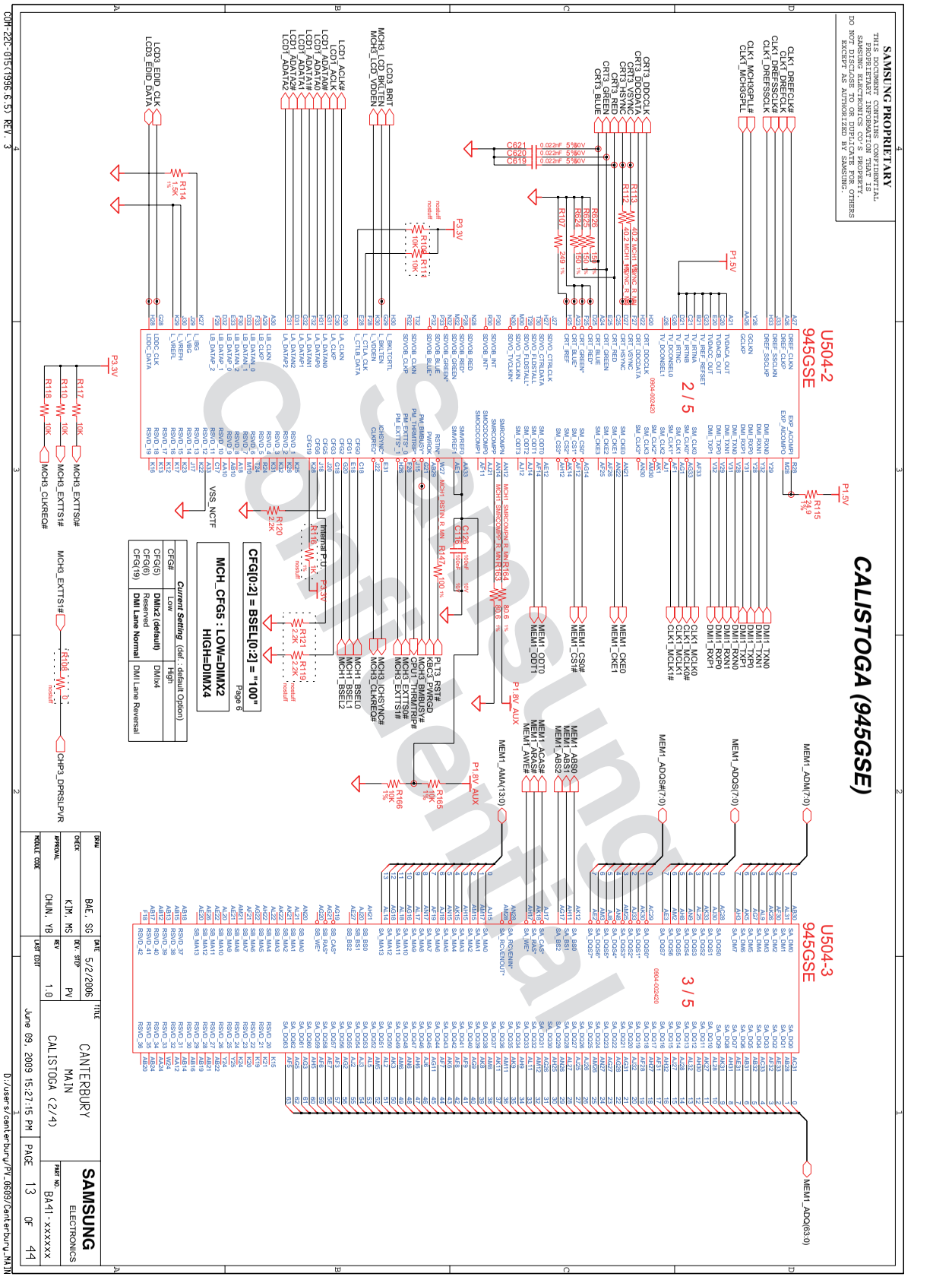

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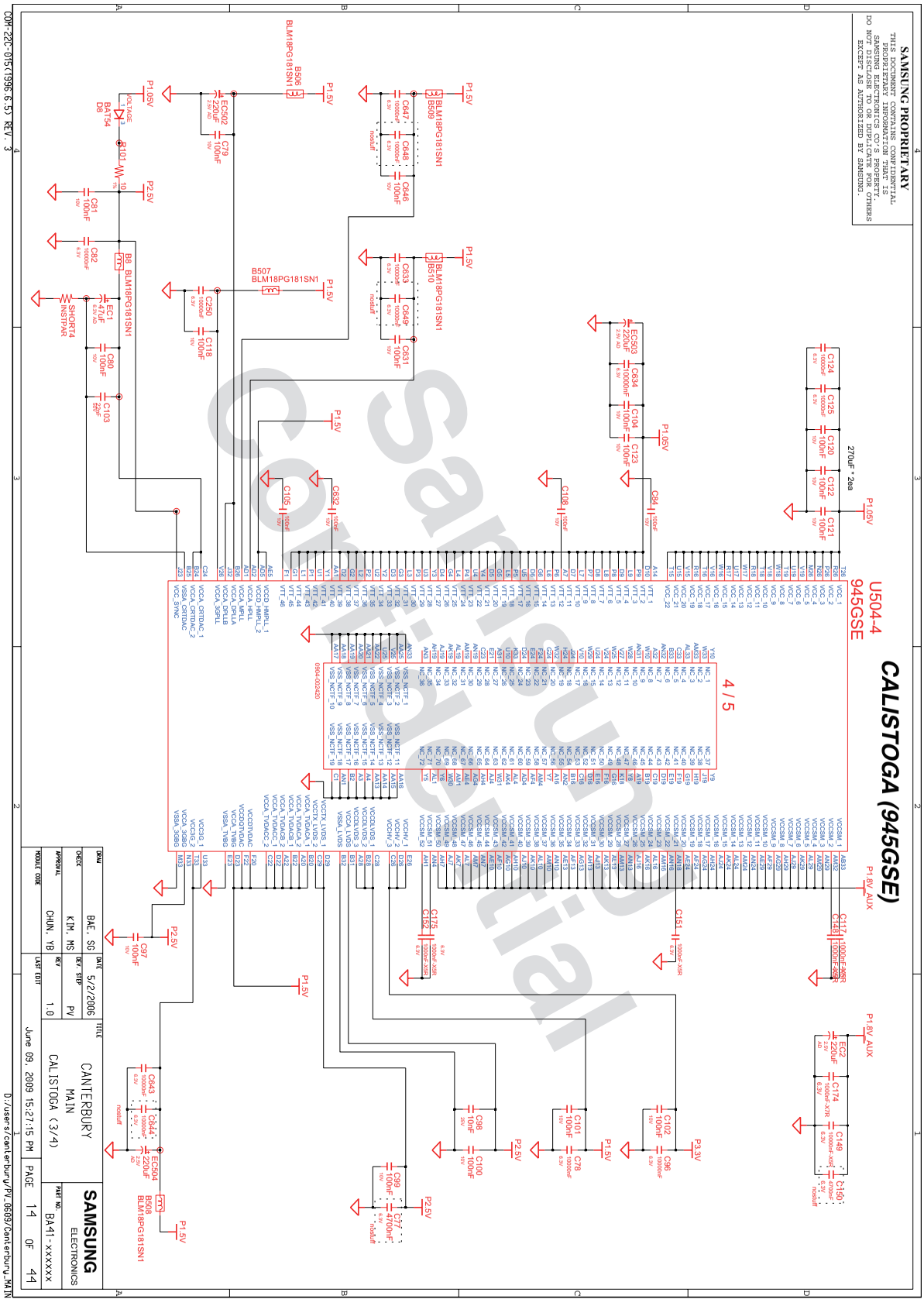

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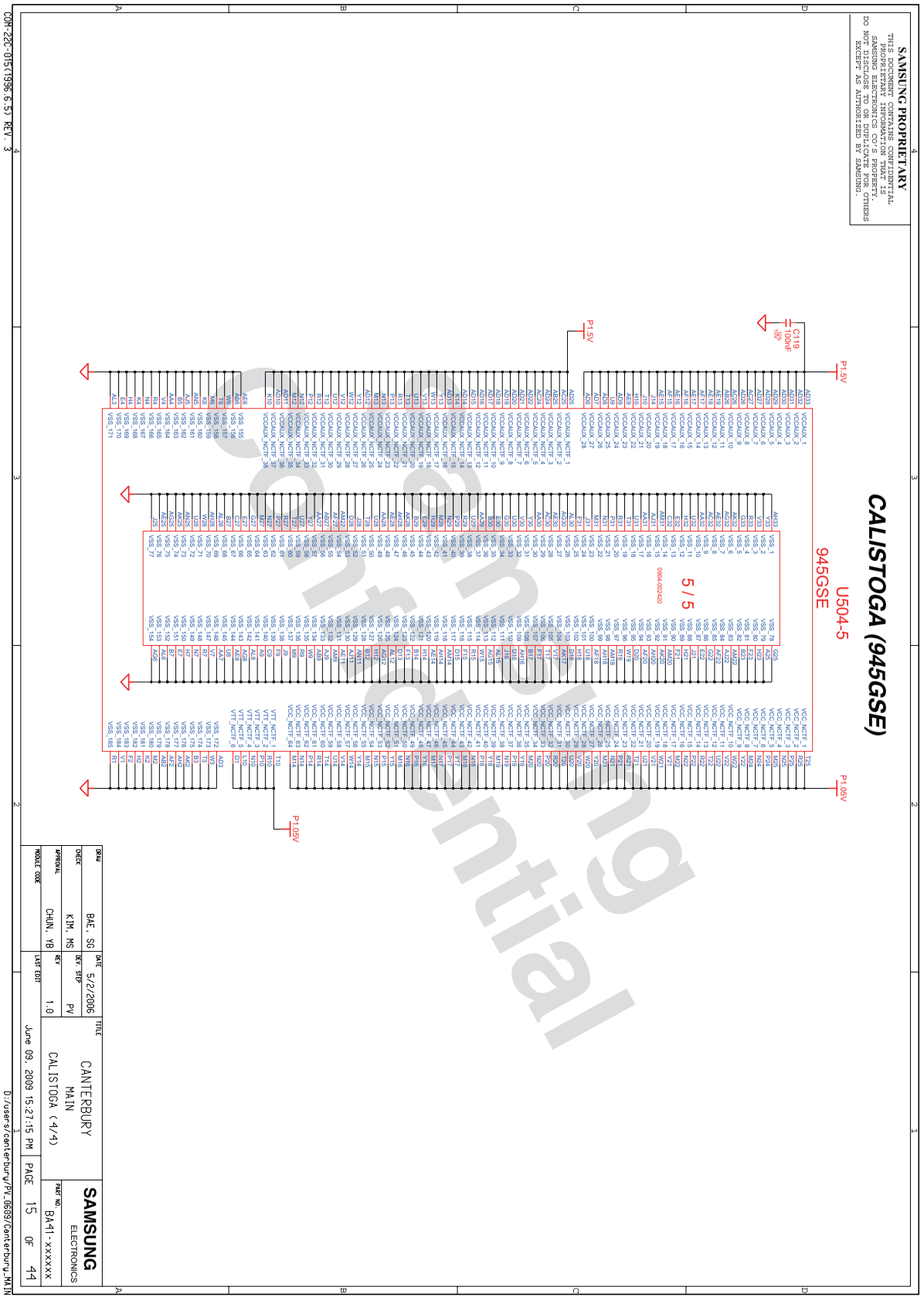

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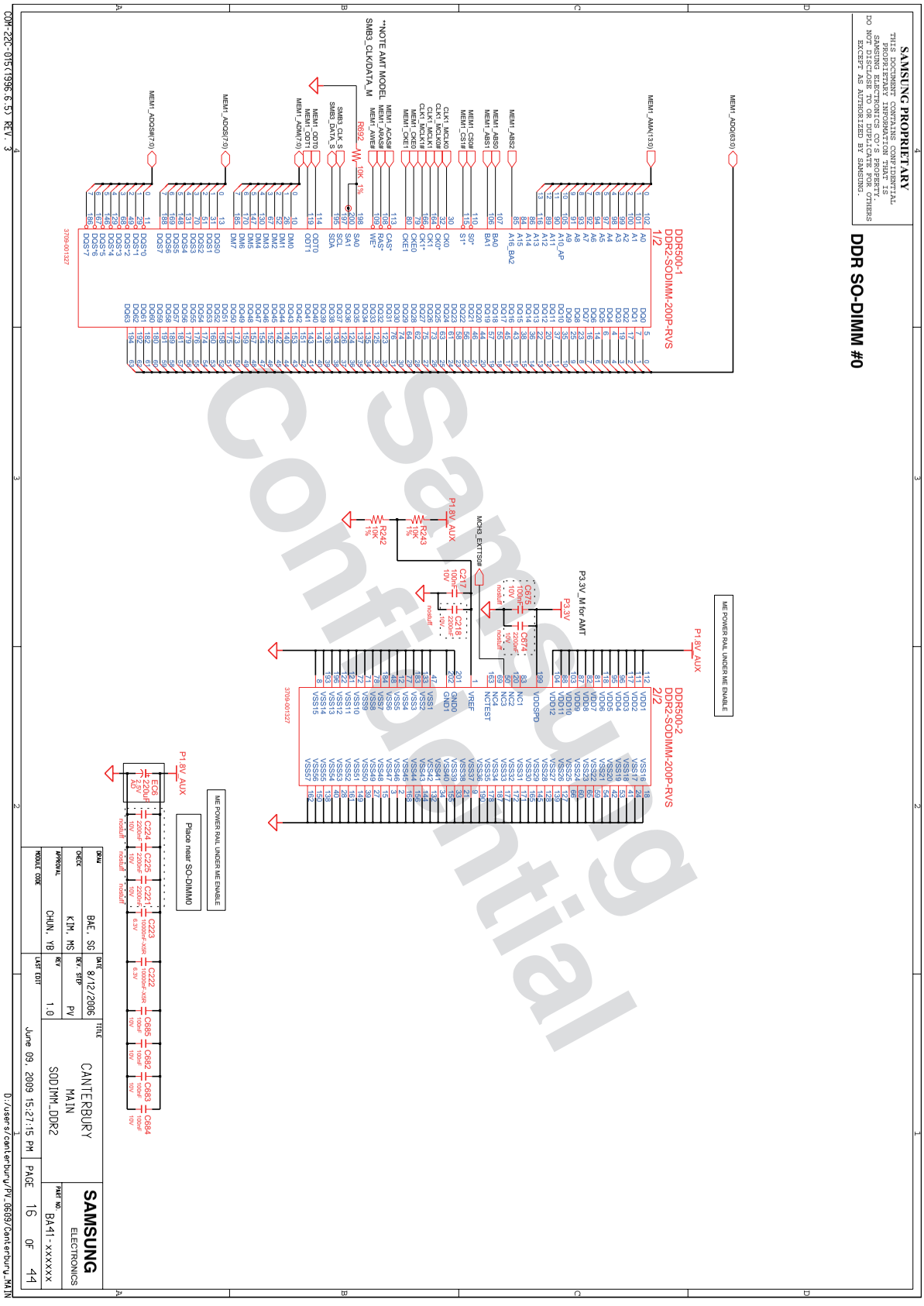

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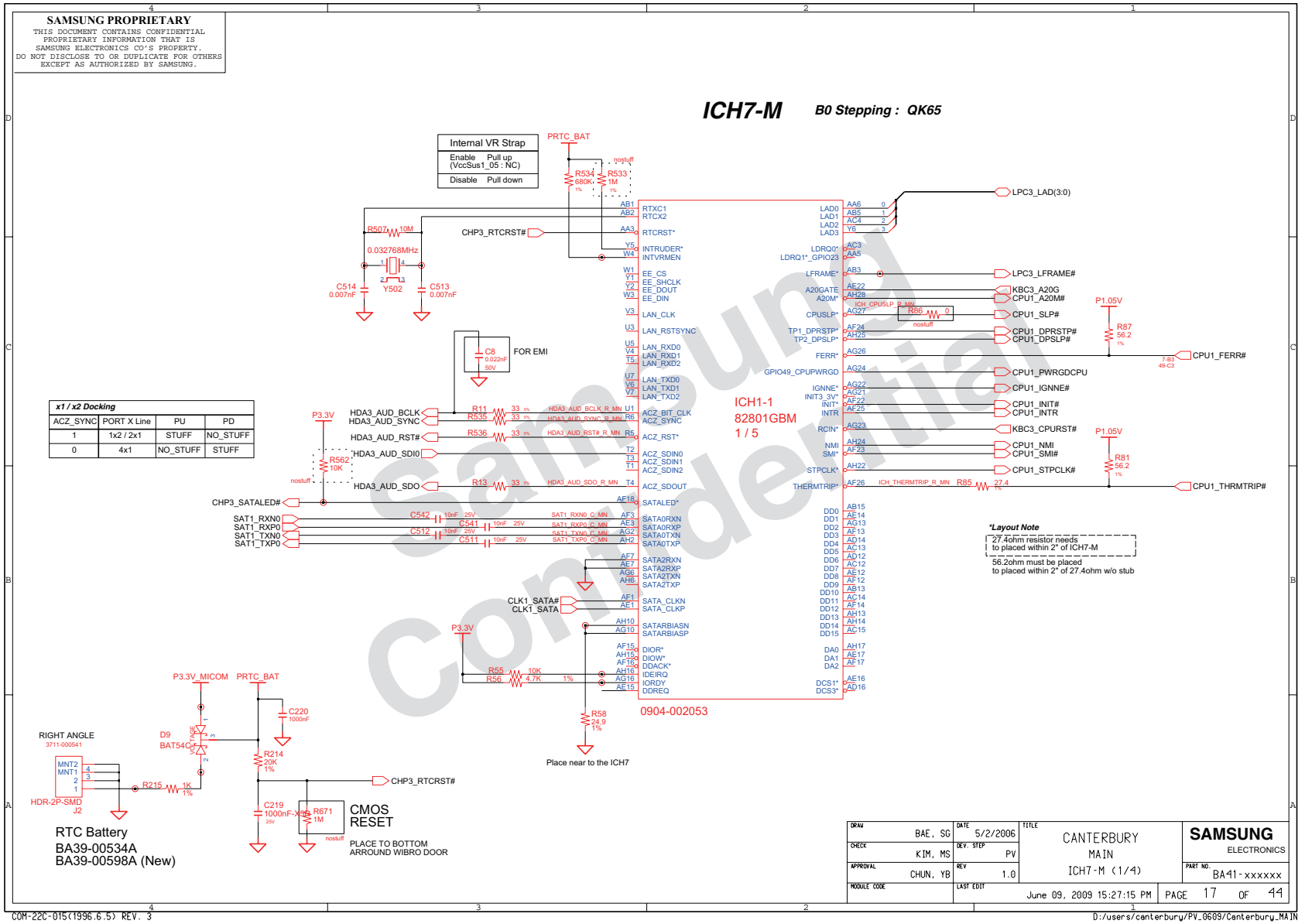

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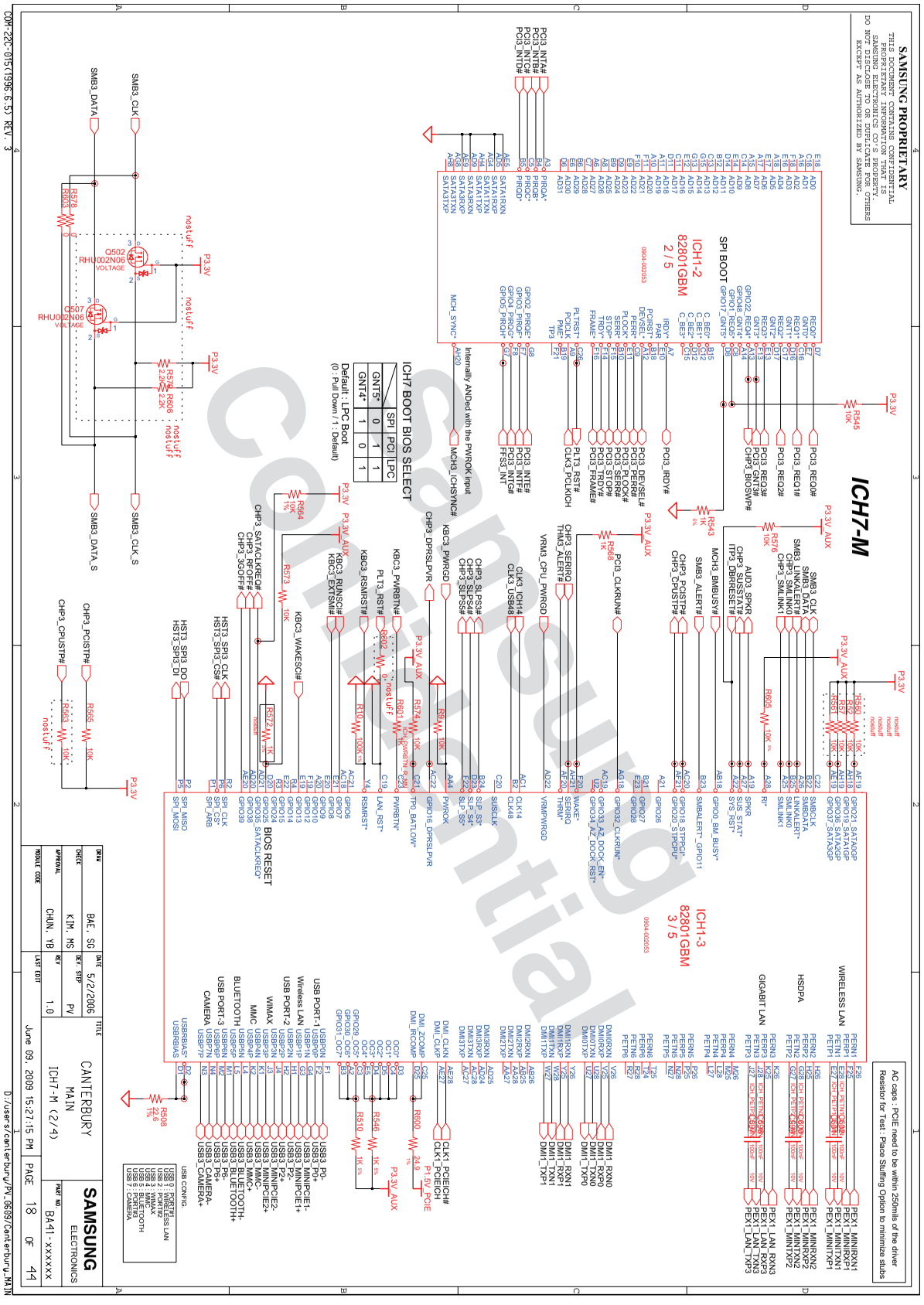

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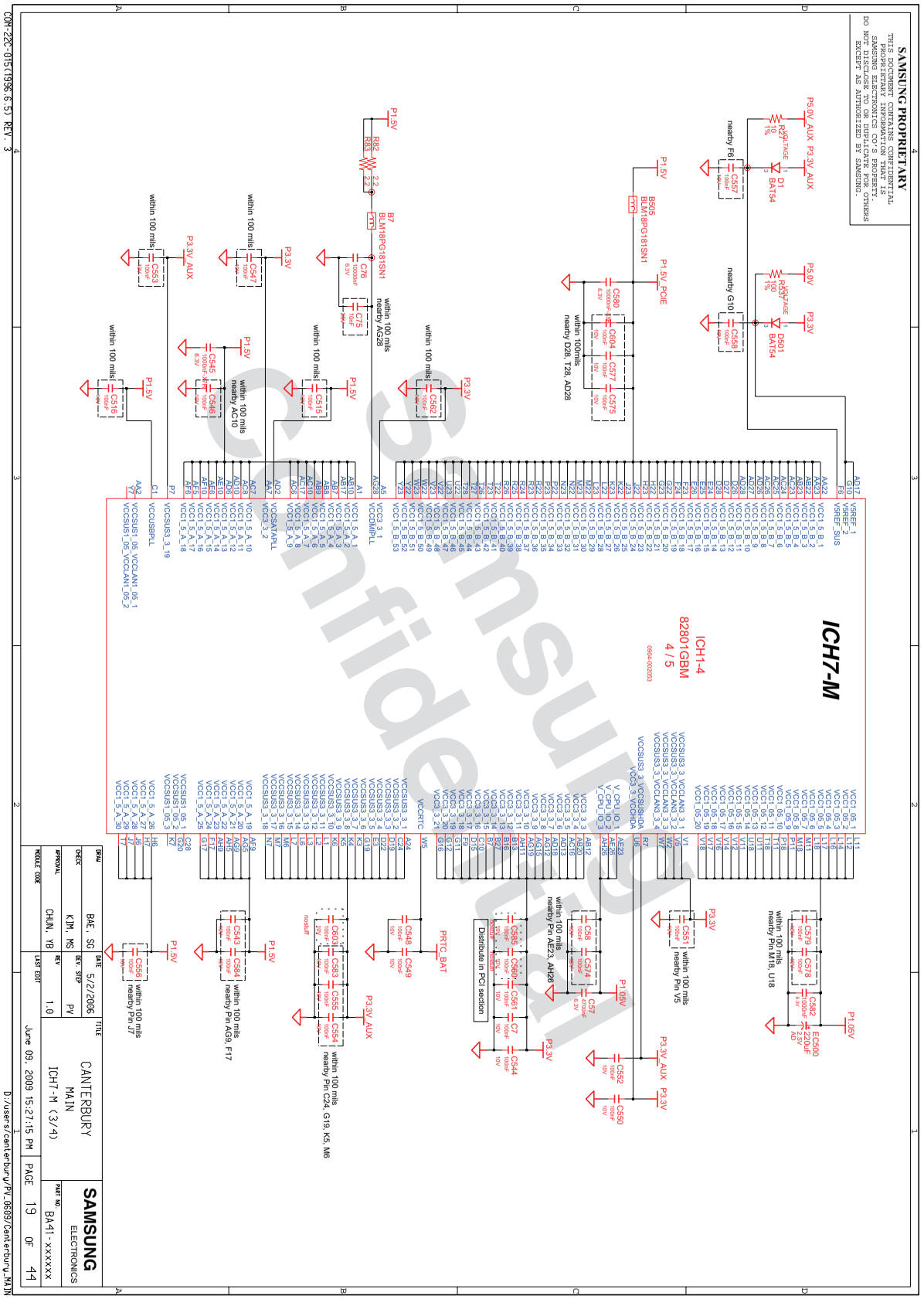

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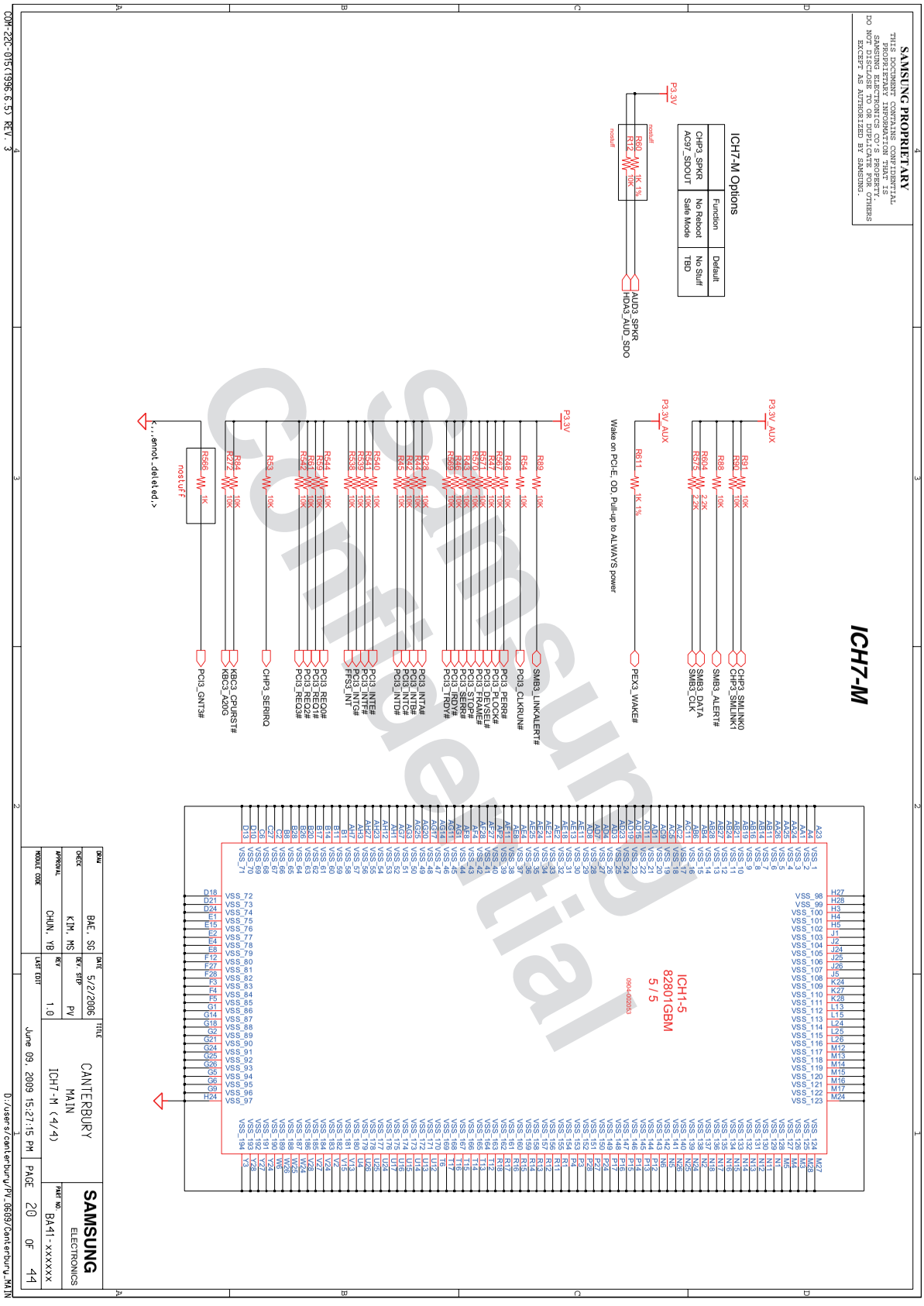

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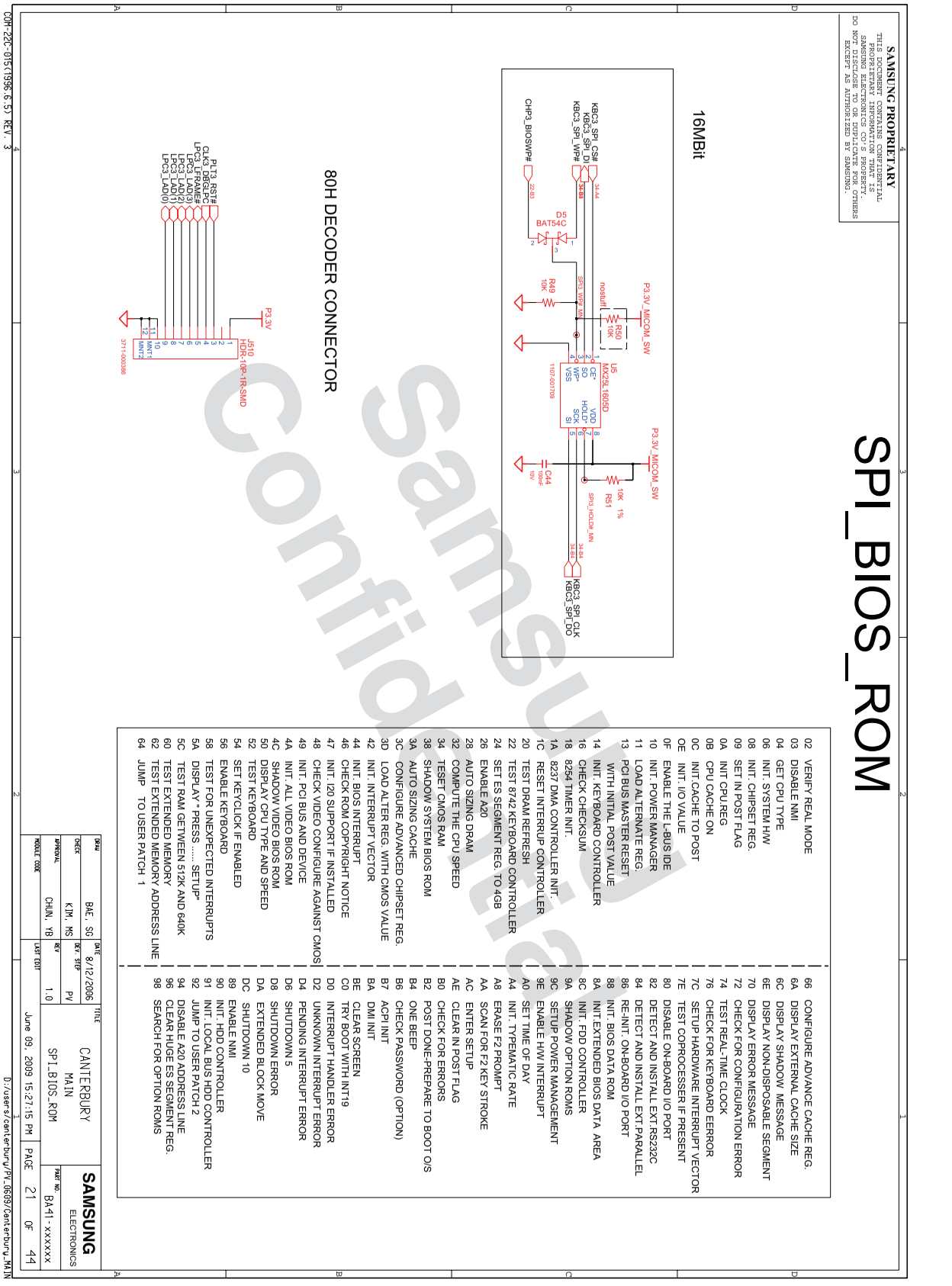

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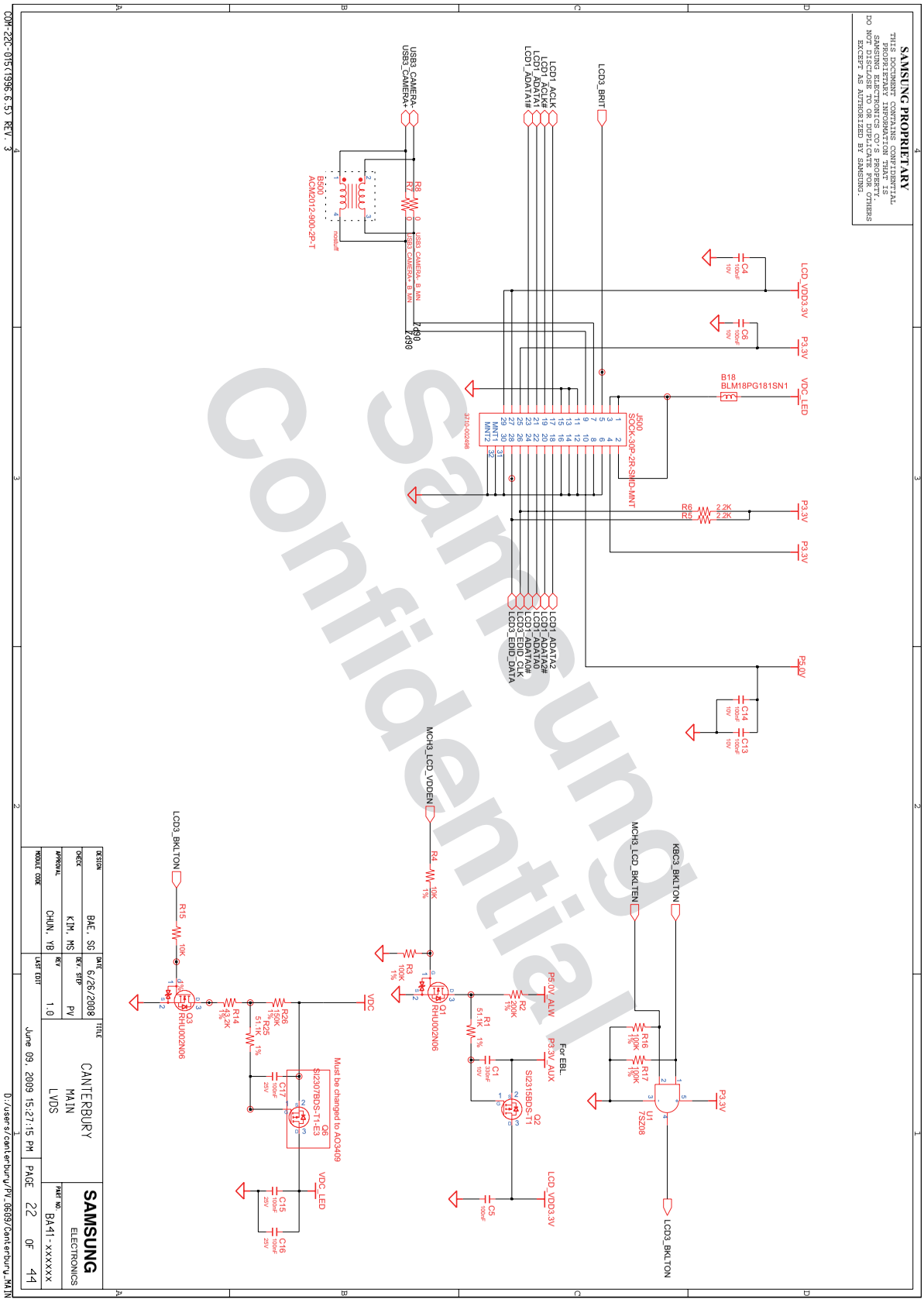

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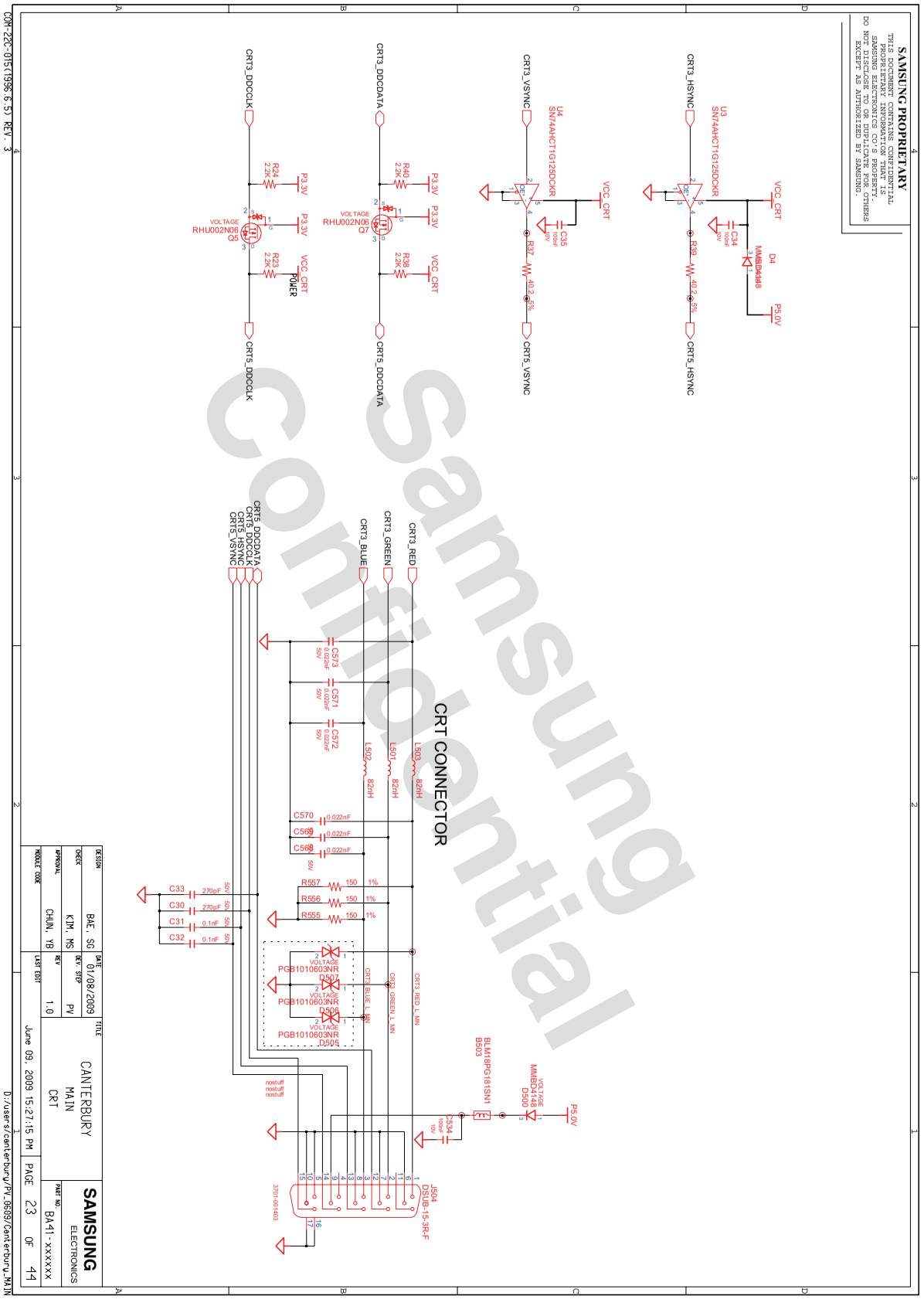

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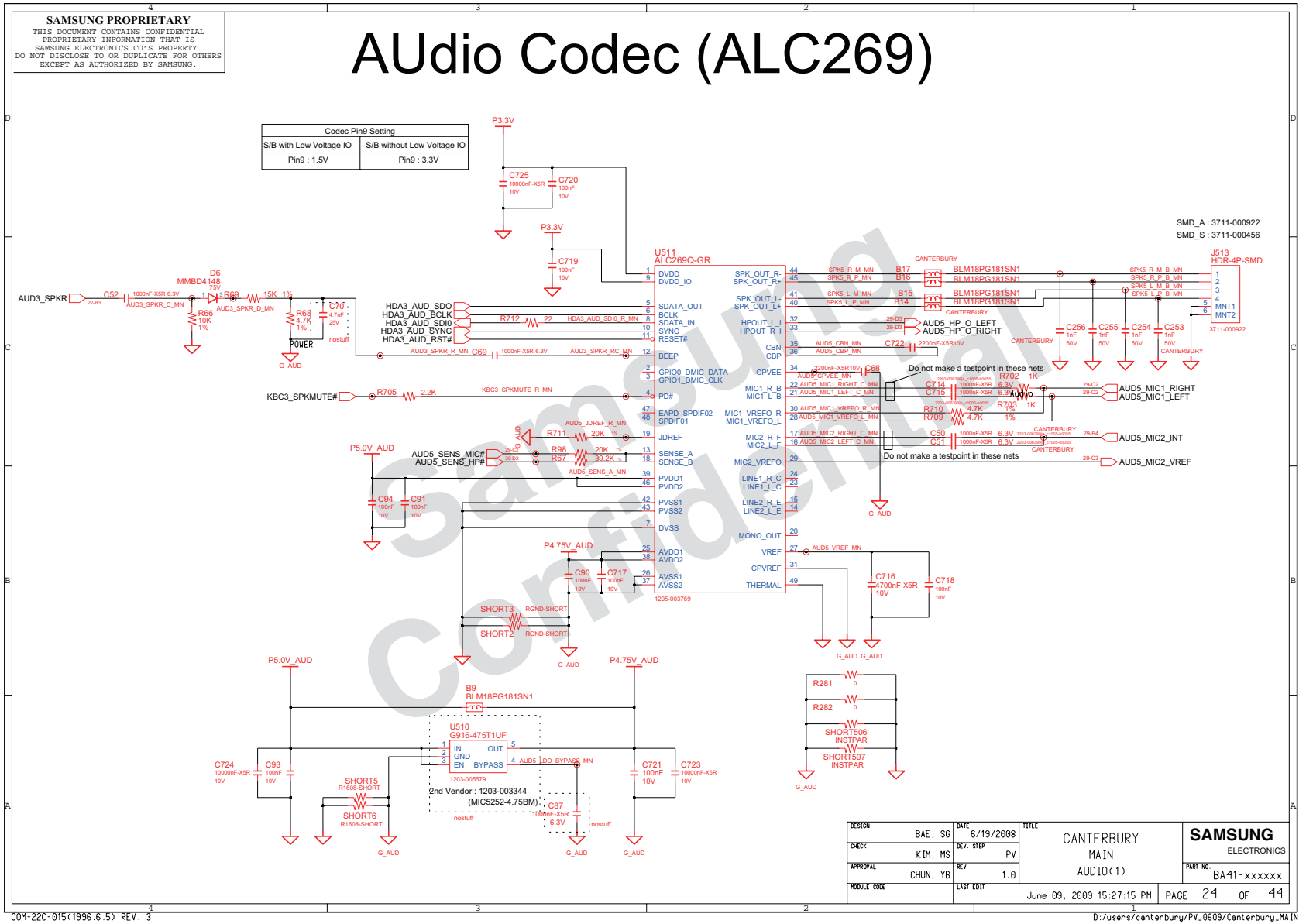

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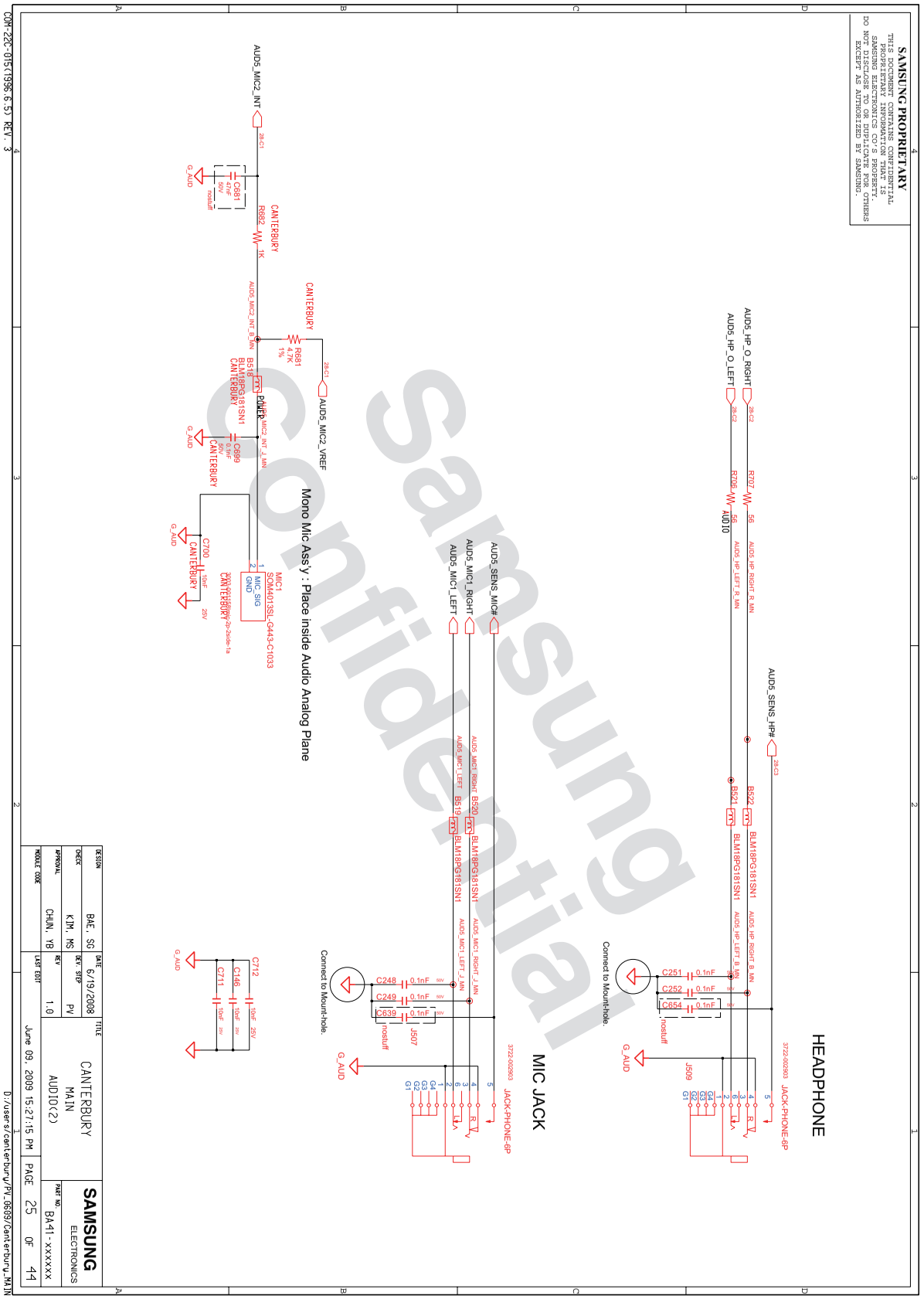
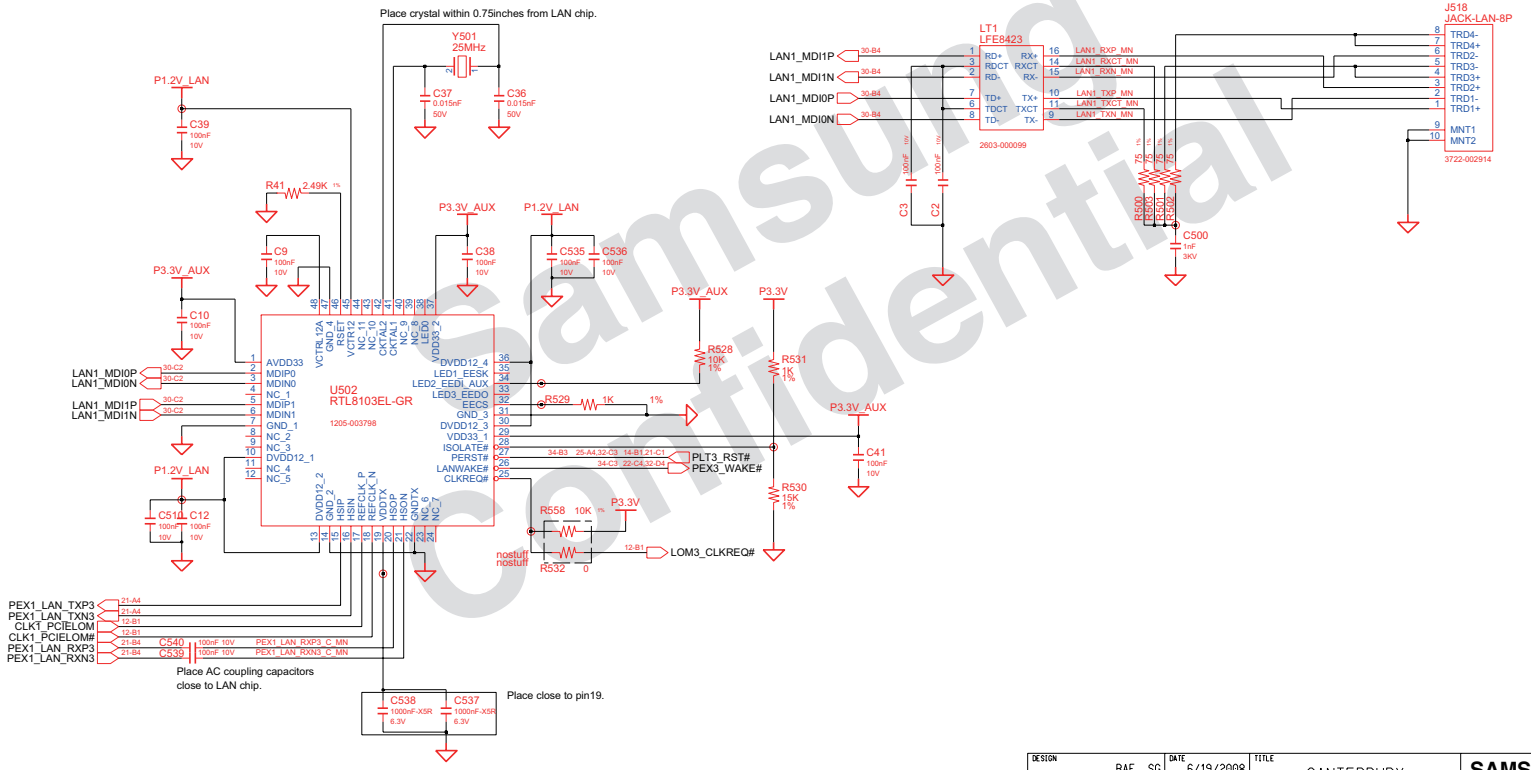


8. Block Diagram and Schematic

LAN Controller (RTL8103EL)



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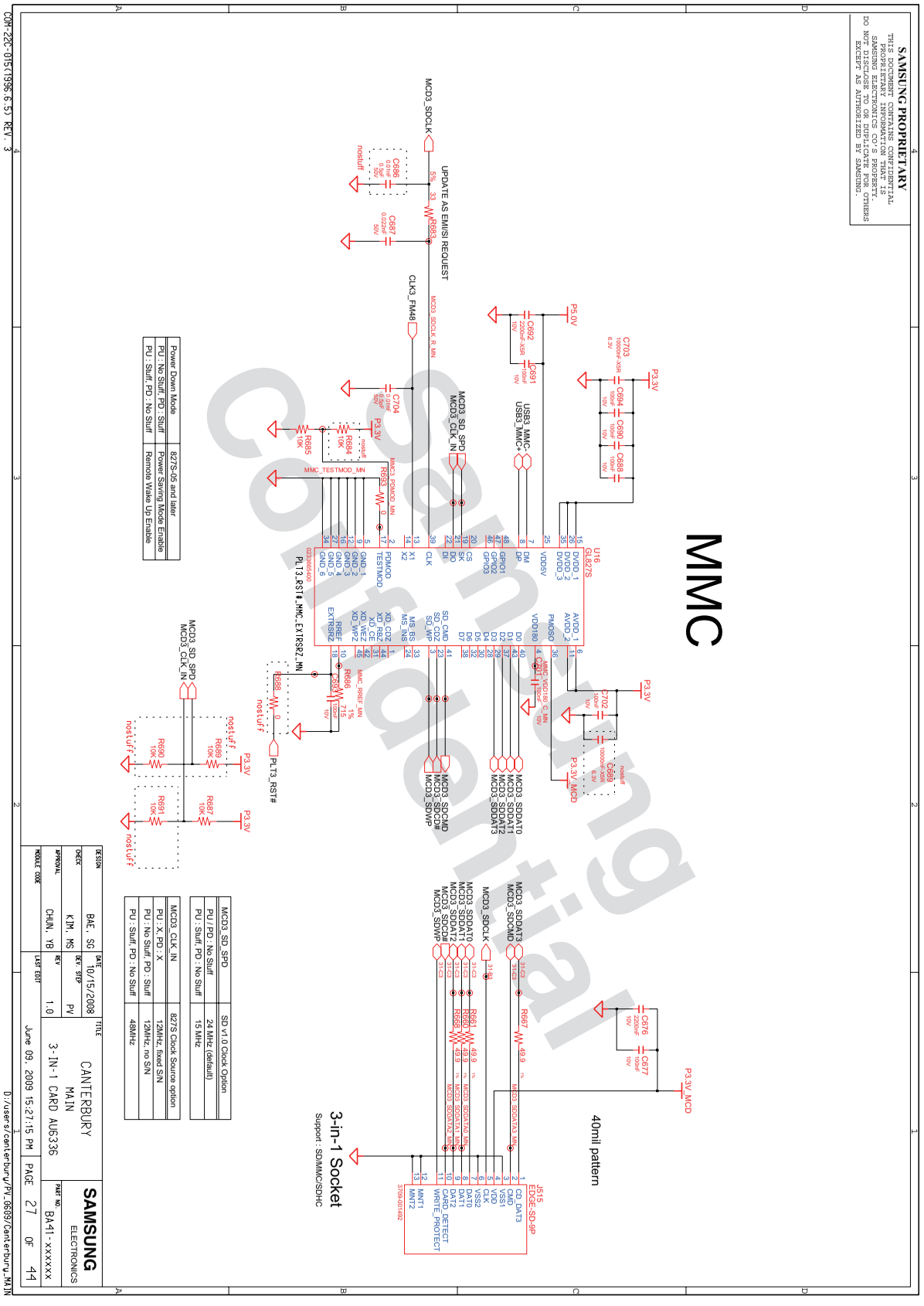

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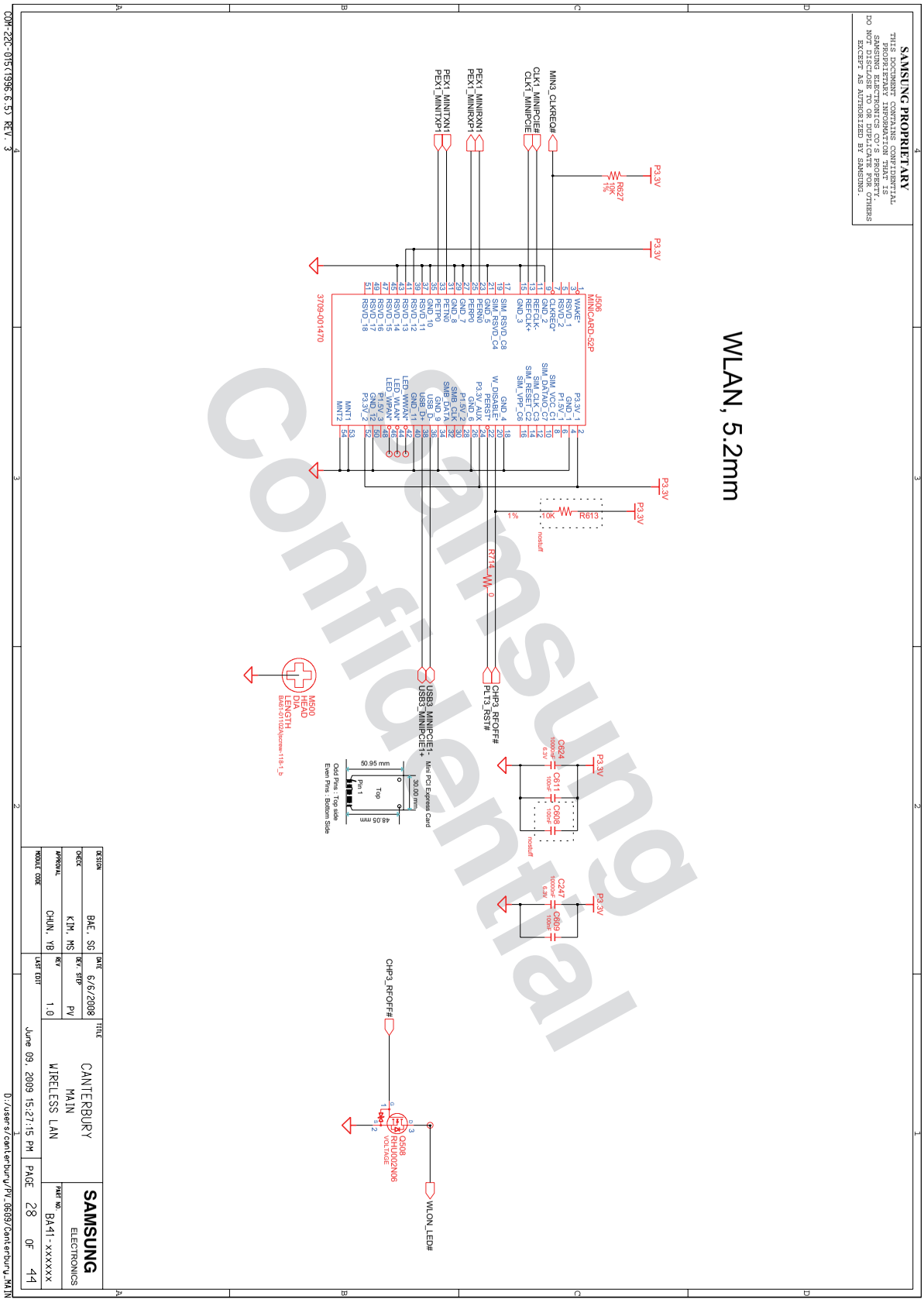

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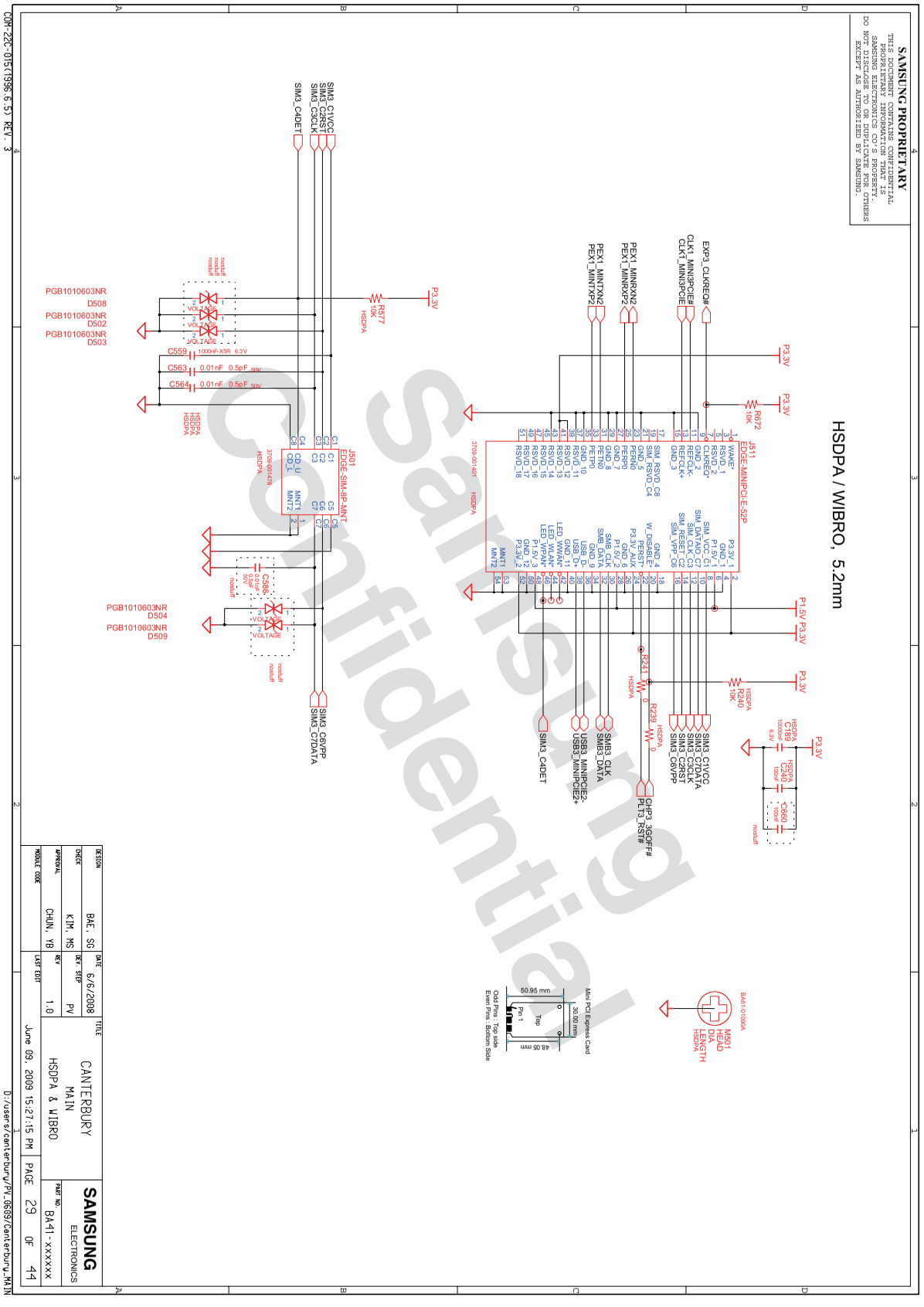

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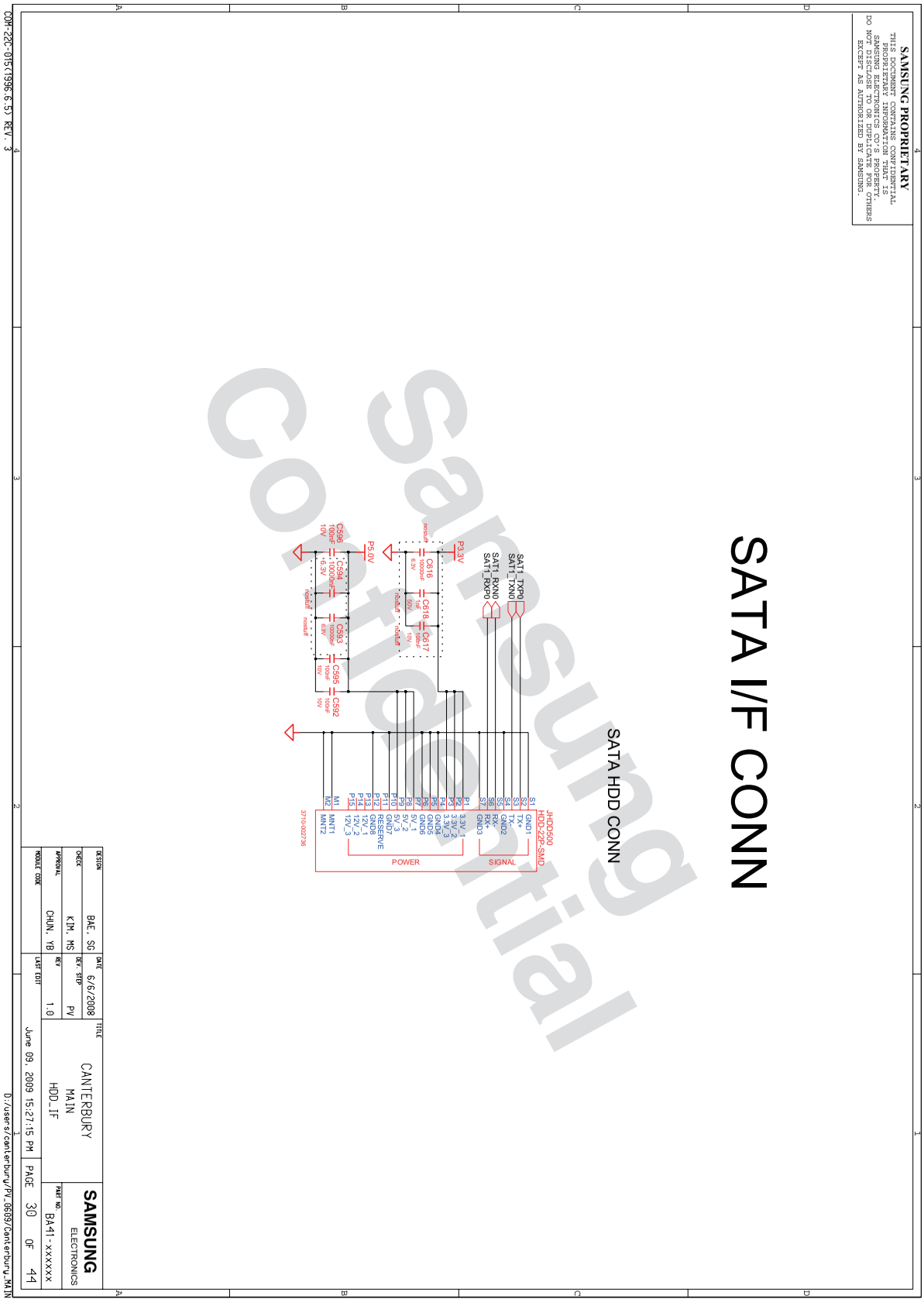

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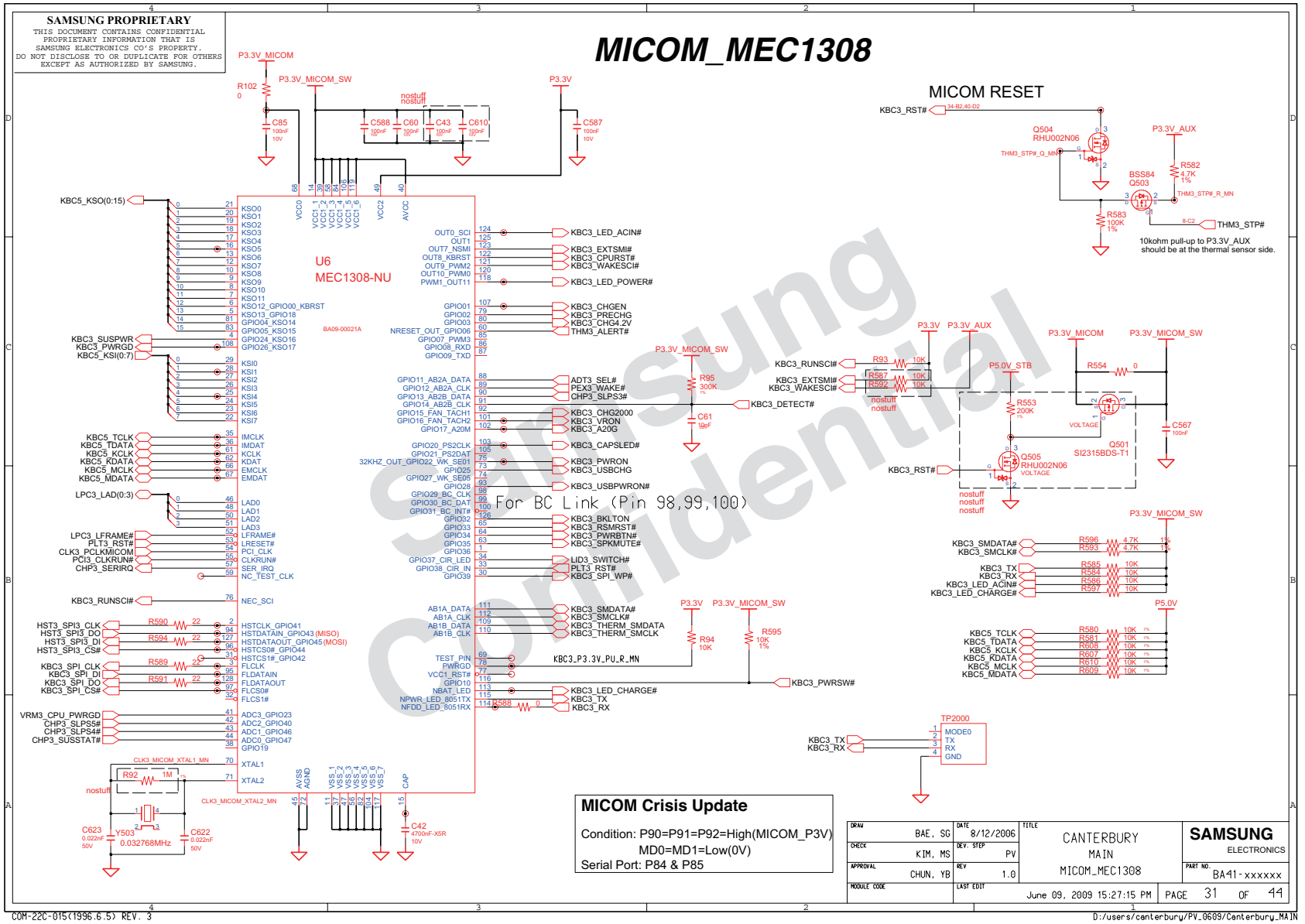
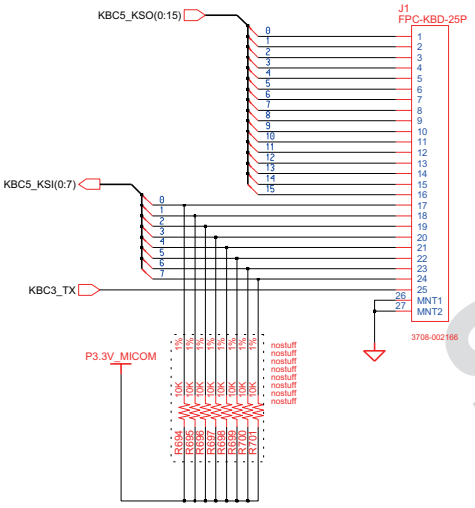
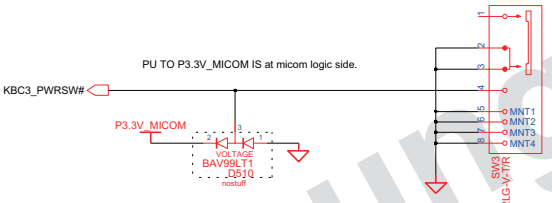


Micom Glue Logic

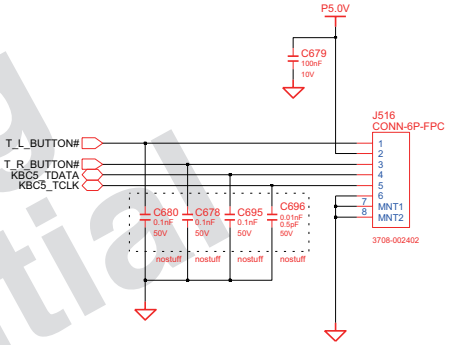
KEYBOARD



Power Switch Button



TOUCHPAD



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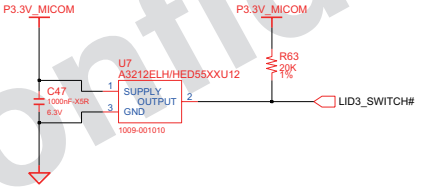

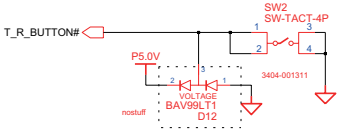

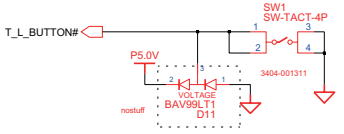

DESIGN: BAE, SG	DATE: 6/27/2008	TITLE: CANTERBURY MAIN MICOM GLUE LOGIC	SAMSUNG ELECTRONICS
CHECK: KIM, MS	DEV. STEP: PV		
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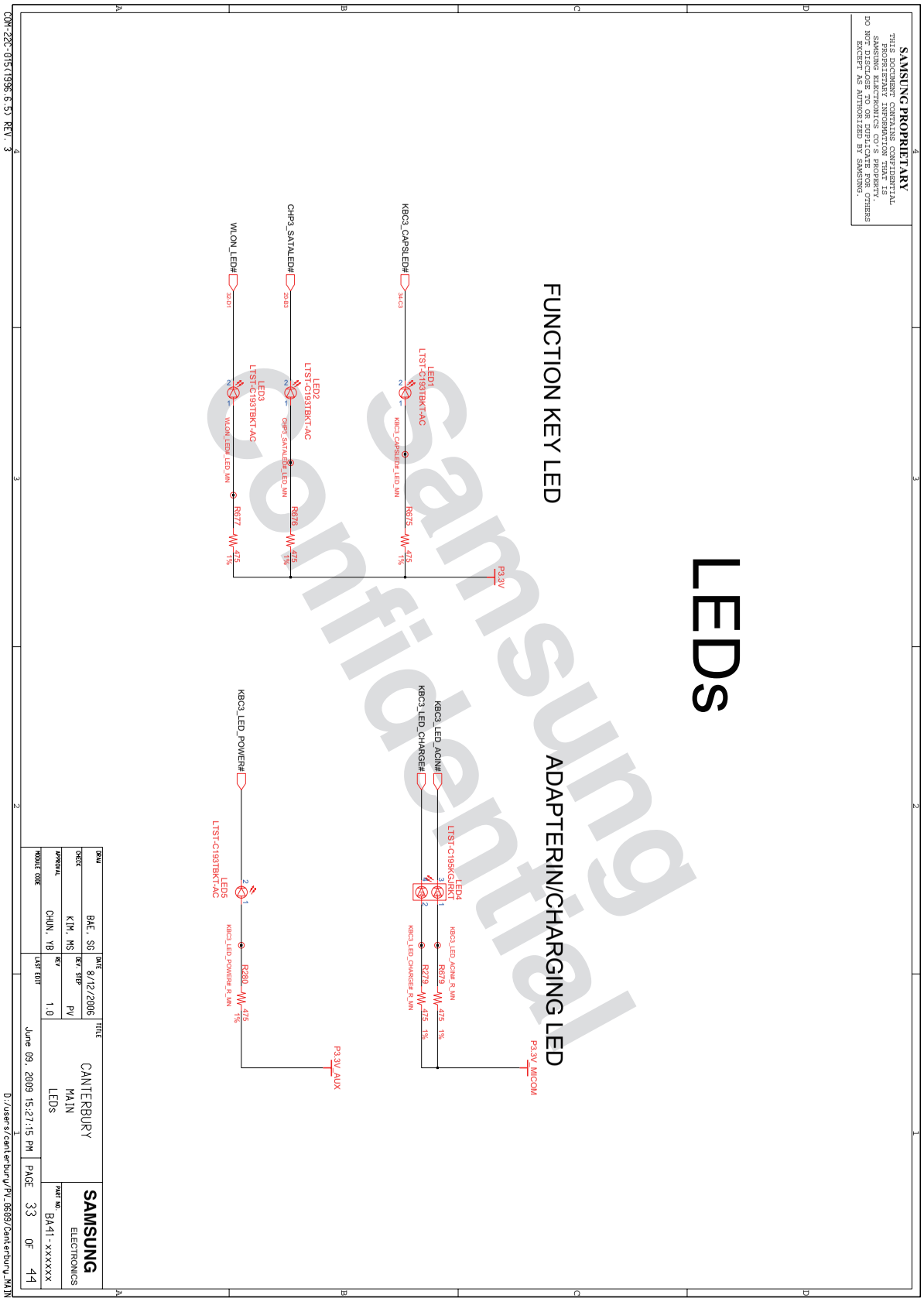

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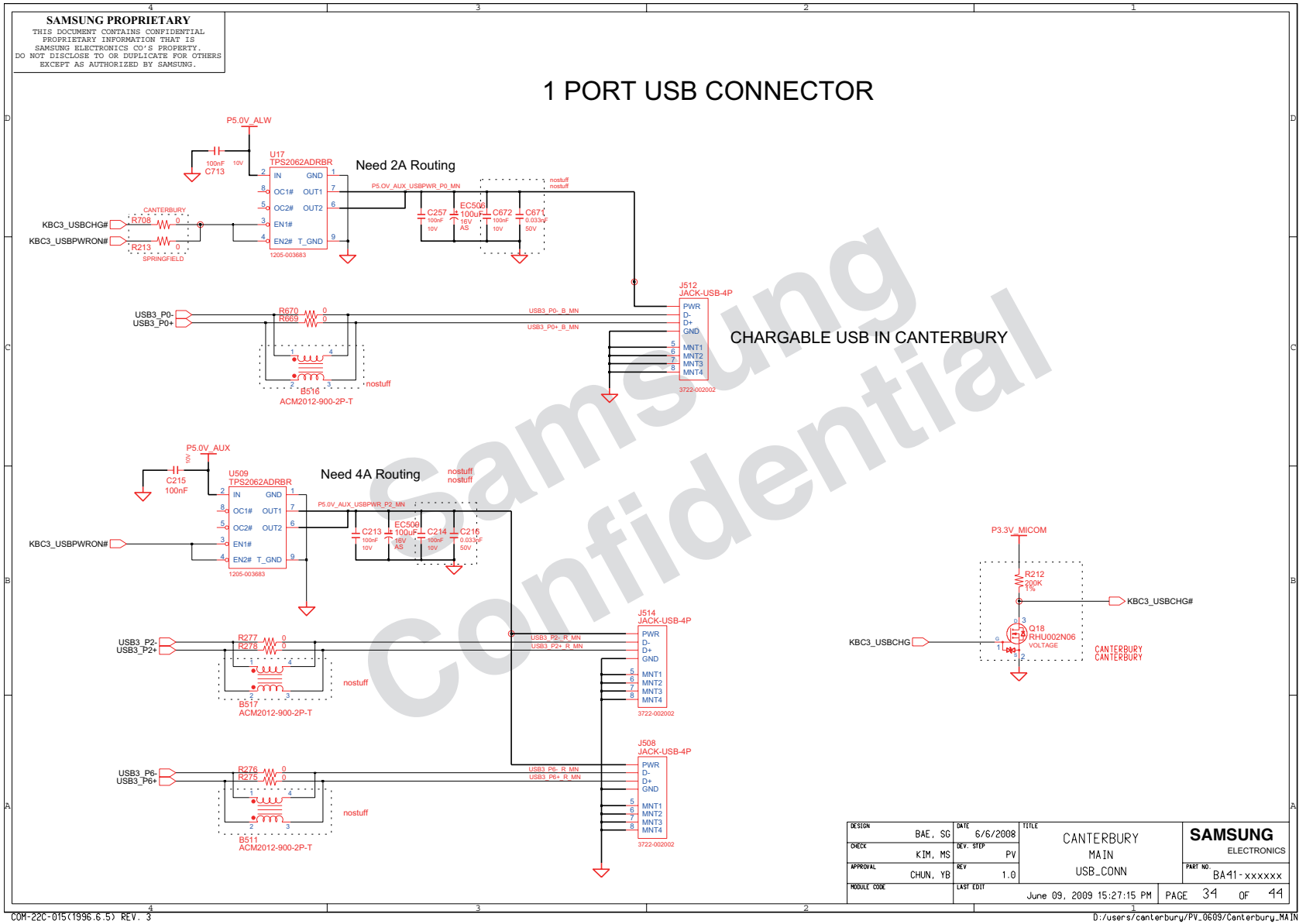

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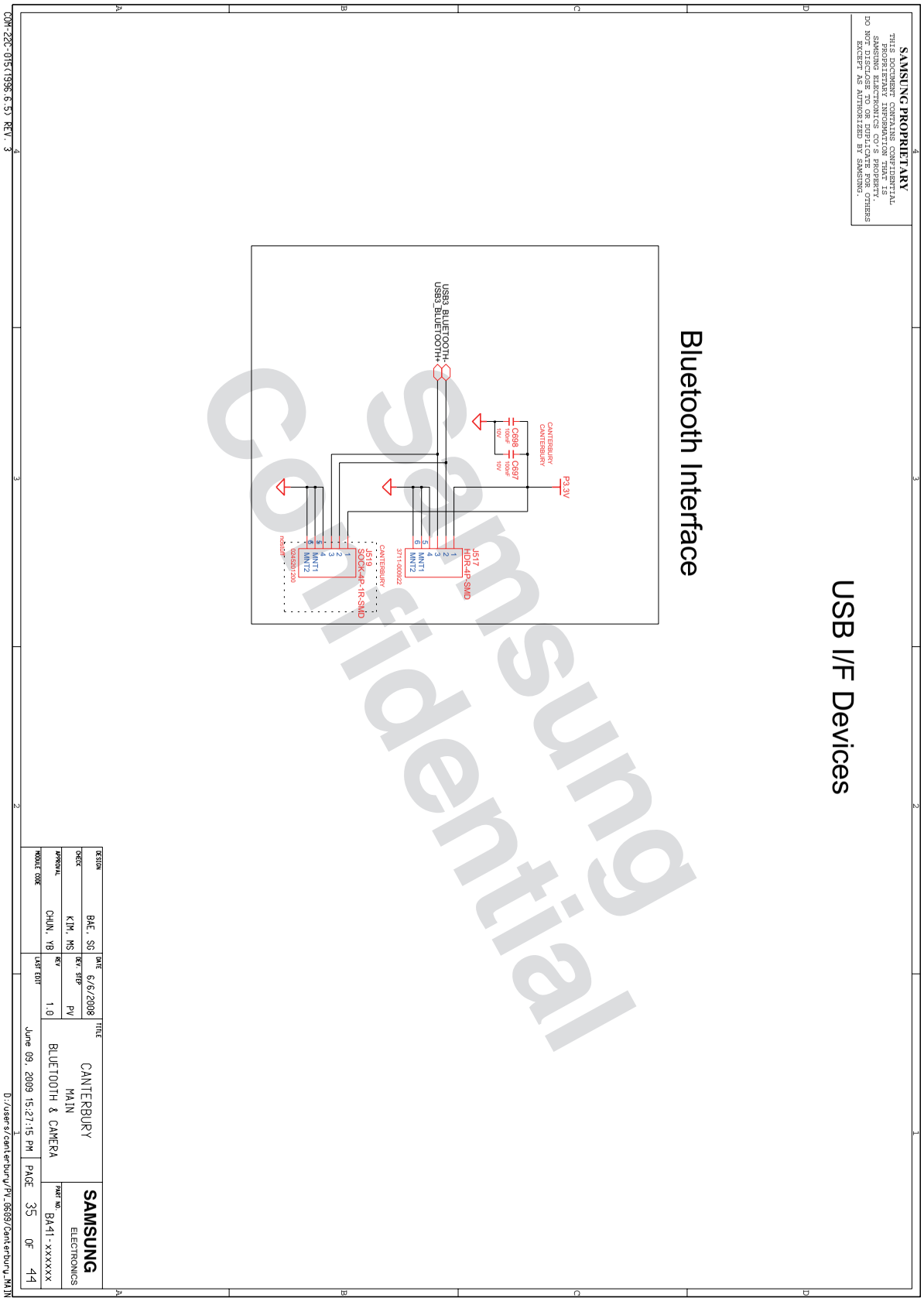

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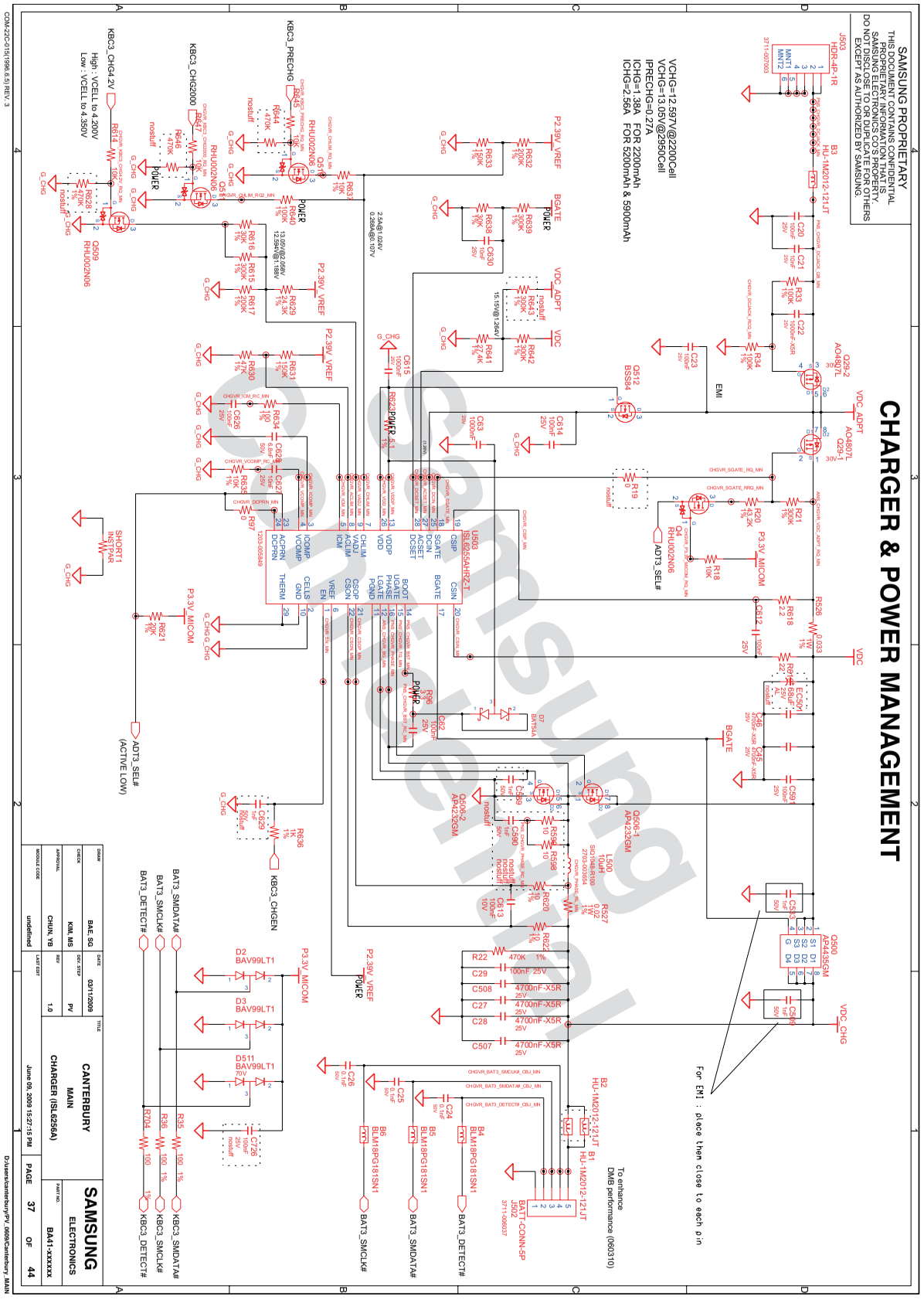
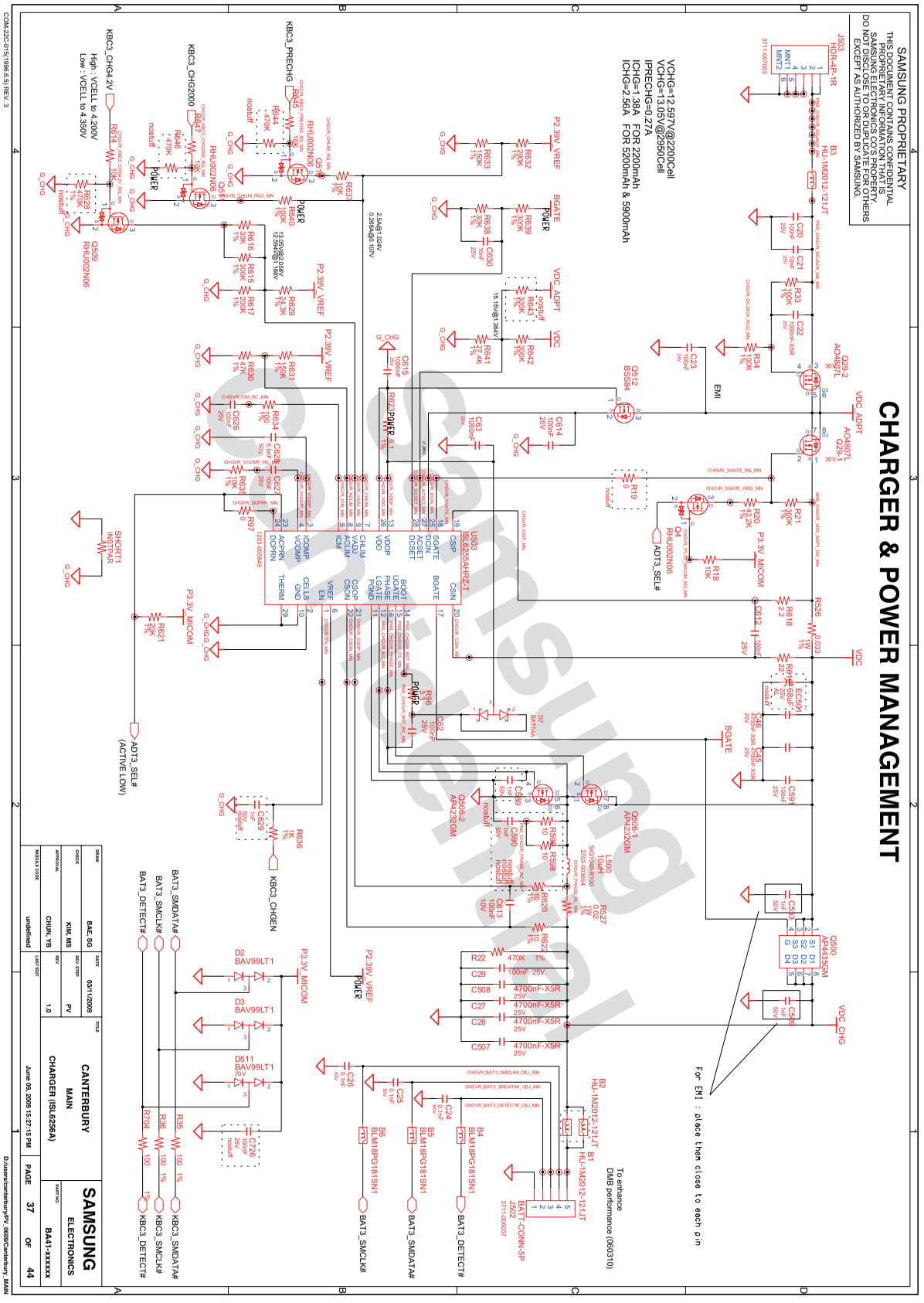
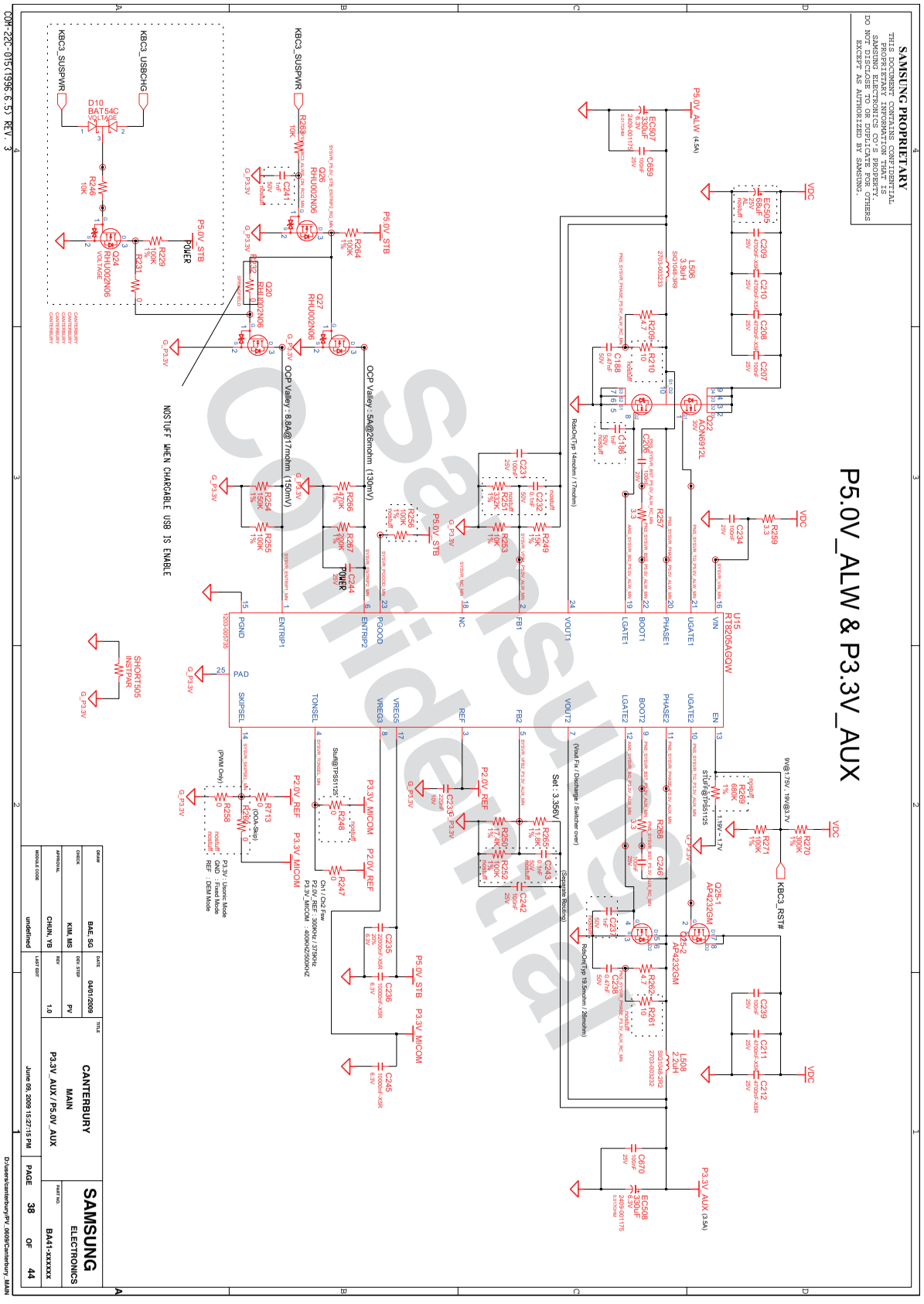


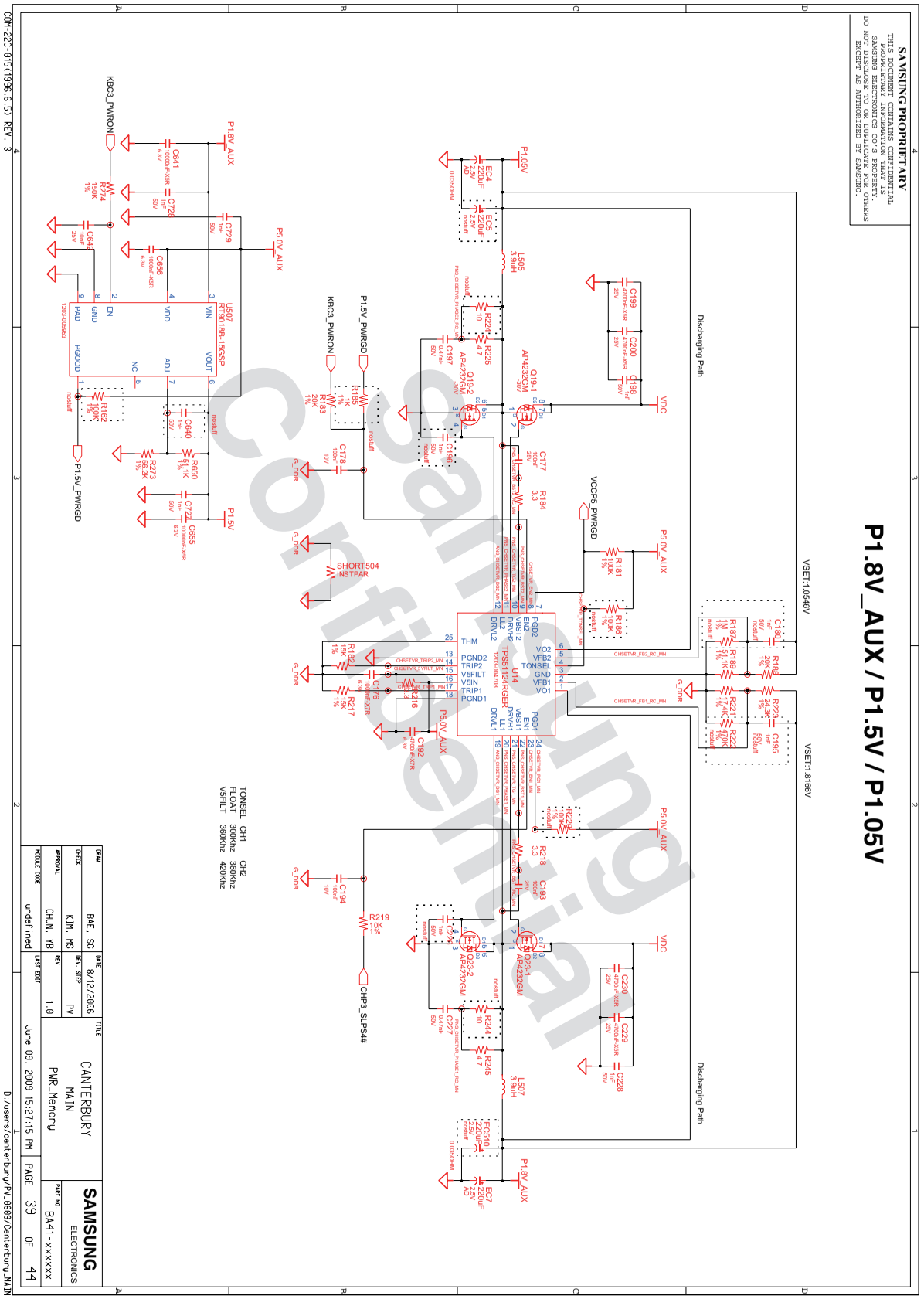
8. Block Diagram and Schematic



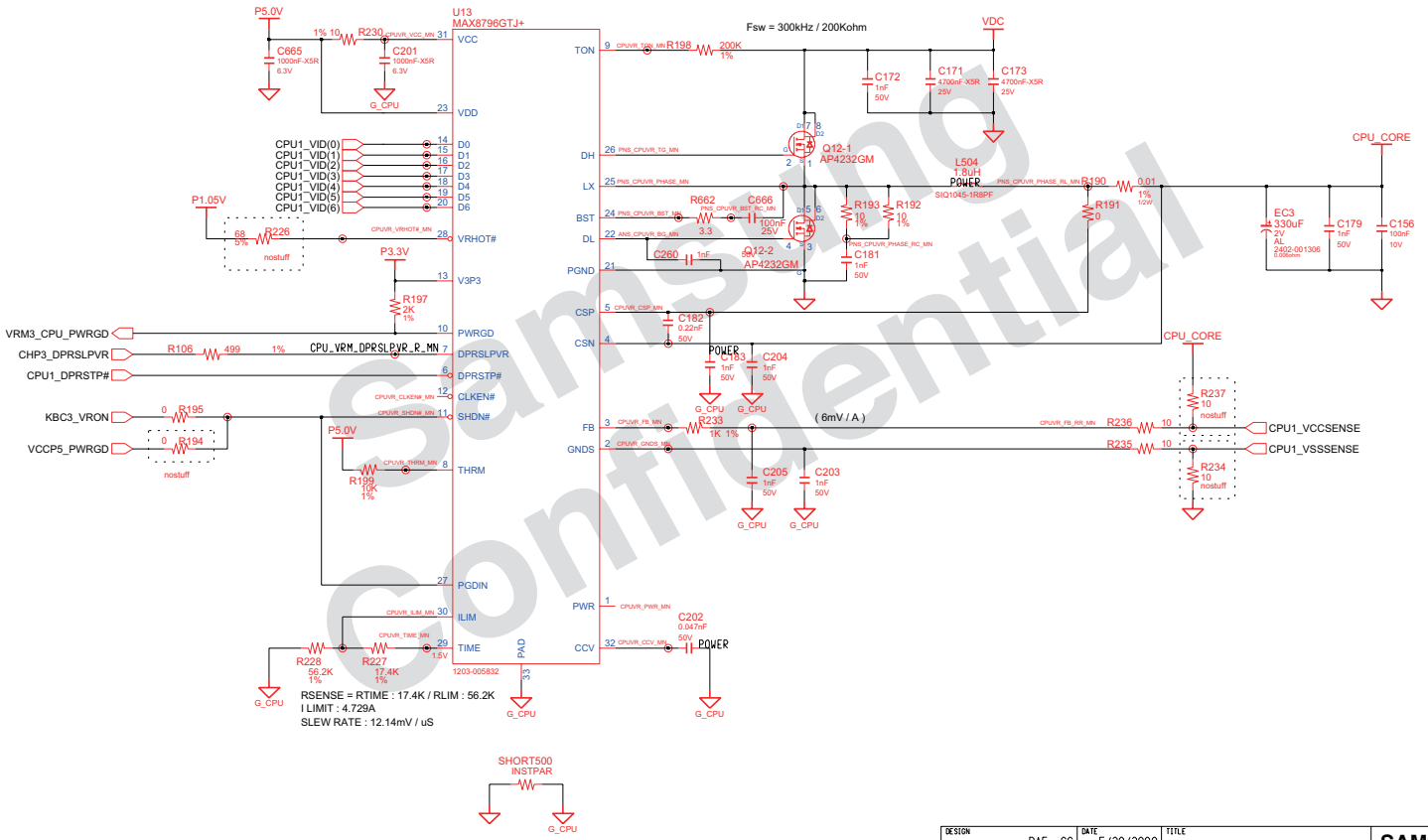
8. Block Diagram and Schematic



8. Block Diagram and Schematic



CPU VRM POWER



DESIGN	BAE, SG	DATE	5/30/2008	TITLE	CANTERBURY MAIN CPU VRM
CHECK	KIM, MS	DEV. STEP	PV		
APPROVAL	CHUN, YB	REV	1.0		
MODULE CODE		LAST EDIT	June 09, 2009 15:27:15 PM	PAGE	40 OF 44

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PART NO. BA41-xxxxxx

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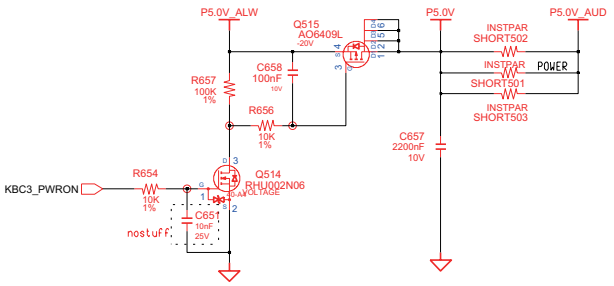
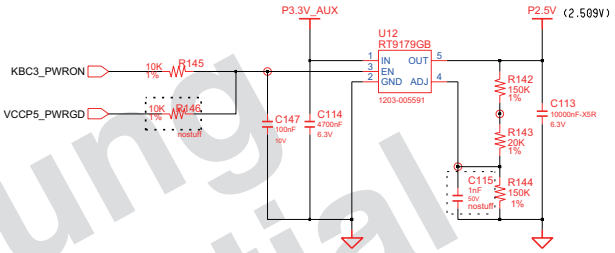
D:/users/canterbury/PV_0609/Canterbury_MAIN

8. Block Diagram and Schematic

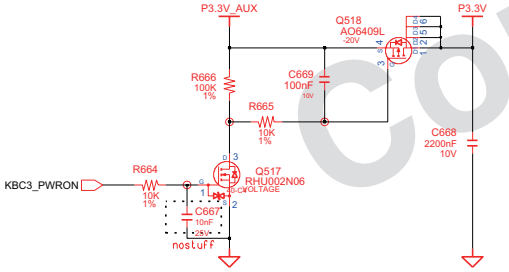
Load Switch Control(P5.0V)



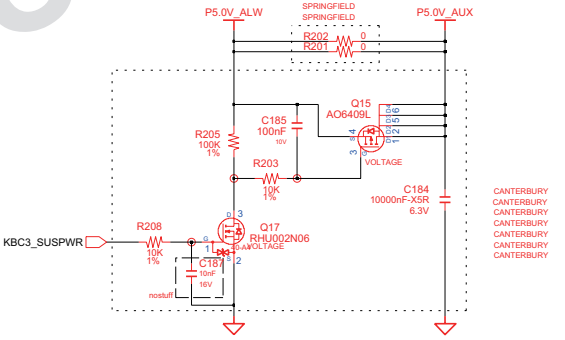
LDO Power (P2.5V)



Load Switch Control(P3.3V)



Load Switch Control(P5.0V_AUX)



DESIGN: BAE, SG	DATE: 5/30/2008	TITLE: CANTERBURY MAIN SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK: KIM, MS	DEV. STEP: PV		
APPROVAL: CHUN, YB	REV: 1.0		PART NO.: BA41-xxxxxx
MODULE CODE	LAST EDIT: June 09, 2009 15:27:15 PM	PAGE 41 OF 44	

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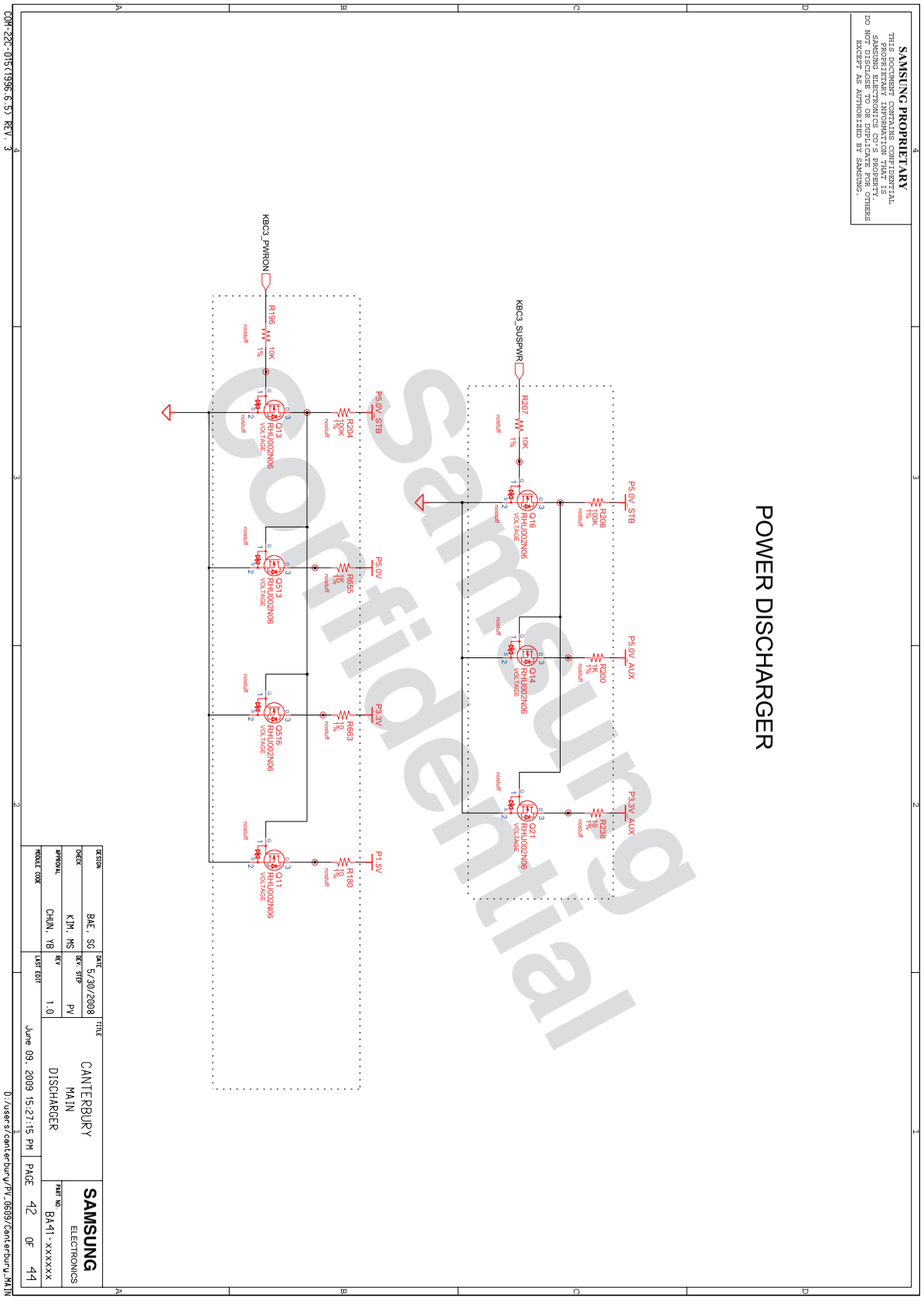
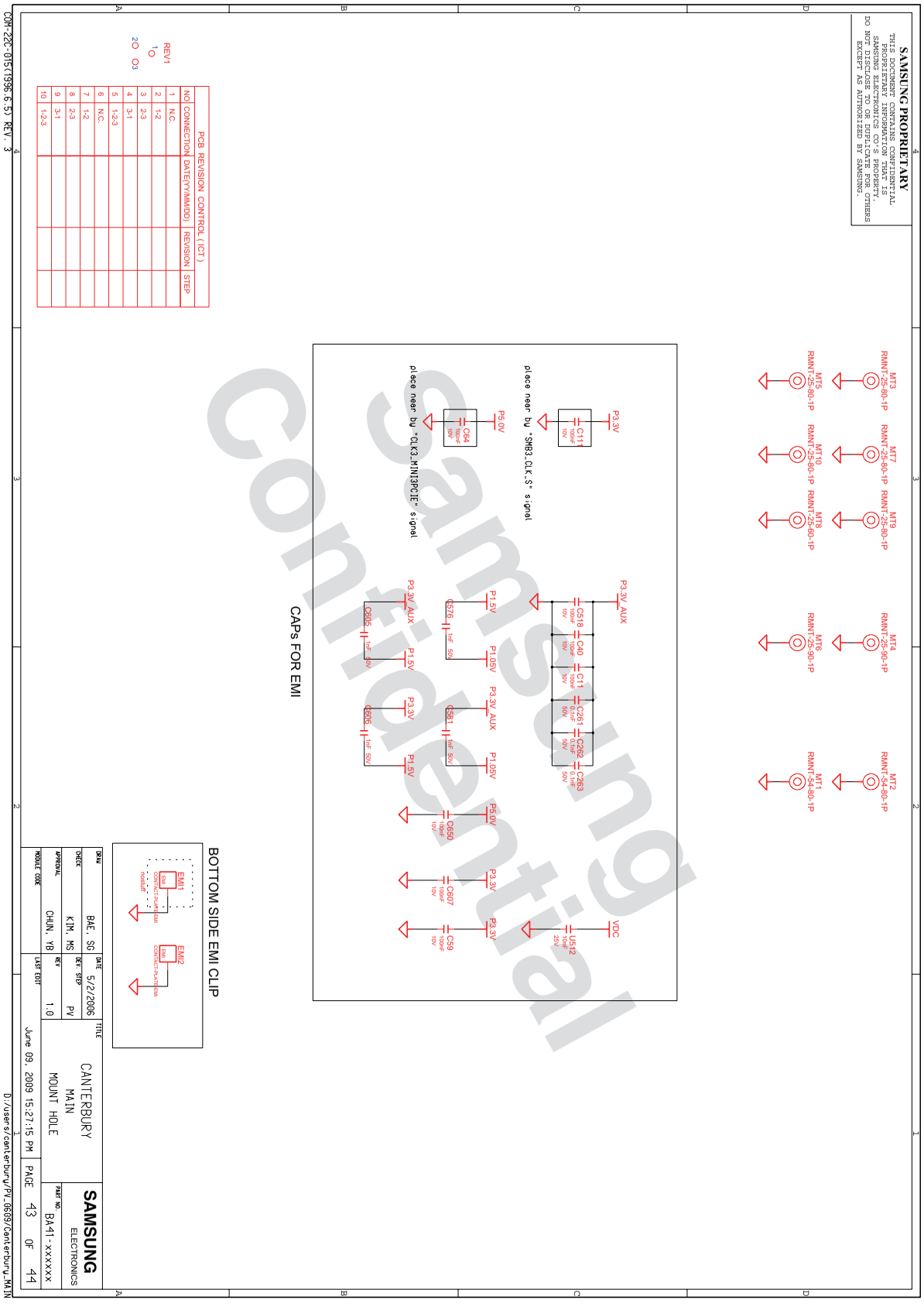
D:/users/canterbury/PV_0609/Canterbury_MAIN

8. Block Diagram and Schematic



8. Block Diagram and Schematic



8. Block Diagram and Schematic