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BRIGHTON

CPU : VIA ISAIAH
Chip Set : VIA VX800
Remarks :

Model Name : BRIGHTON MAIN

PCB Part No :

Dev. Step : PV

Revision : 1.0

T.R. Date : 2008.11.07

DRAW	CHECK	APPROVAL

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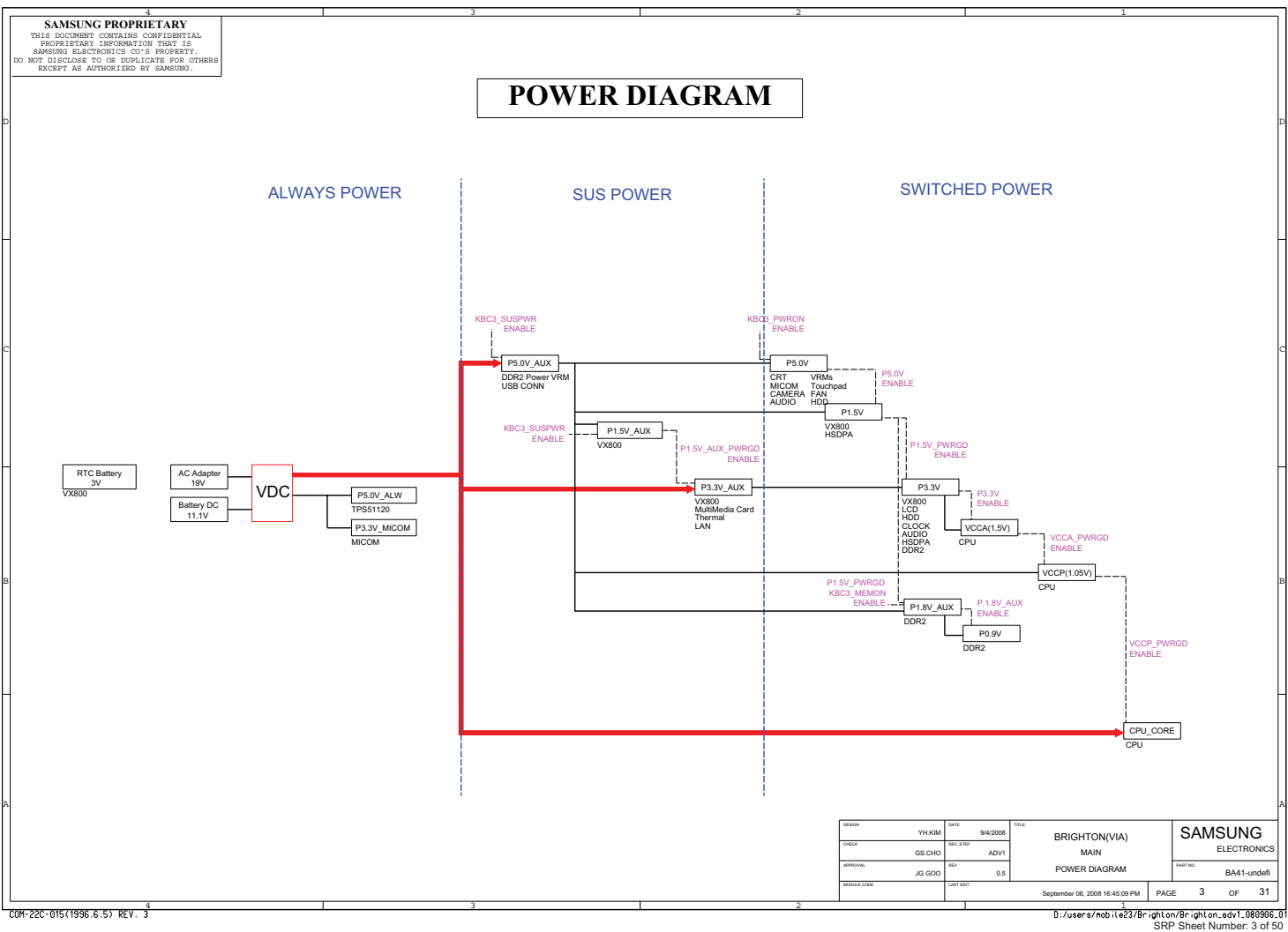
DESIGN	YH.KIM	DATE	9/4/2008	TITLE	BRIGHTON(VIA)	SAMSUNG
CHECK	GS.CHO	DEV. STEP	ADV1	MAIN		ELECTRONICS
APPROVAL	JG.GOO	REV	0.5	COVER		PART NO. BA41-undefi
MODULE CODE		LAST EDIT				

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8. Block Diagram and Schematic

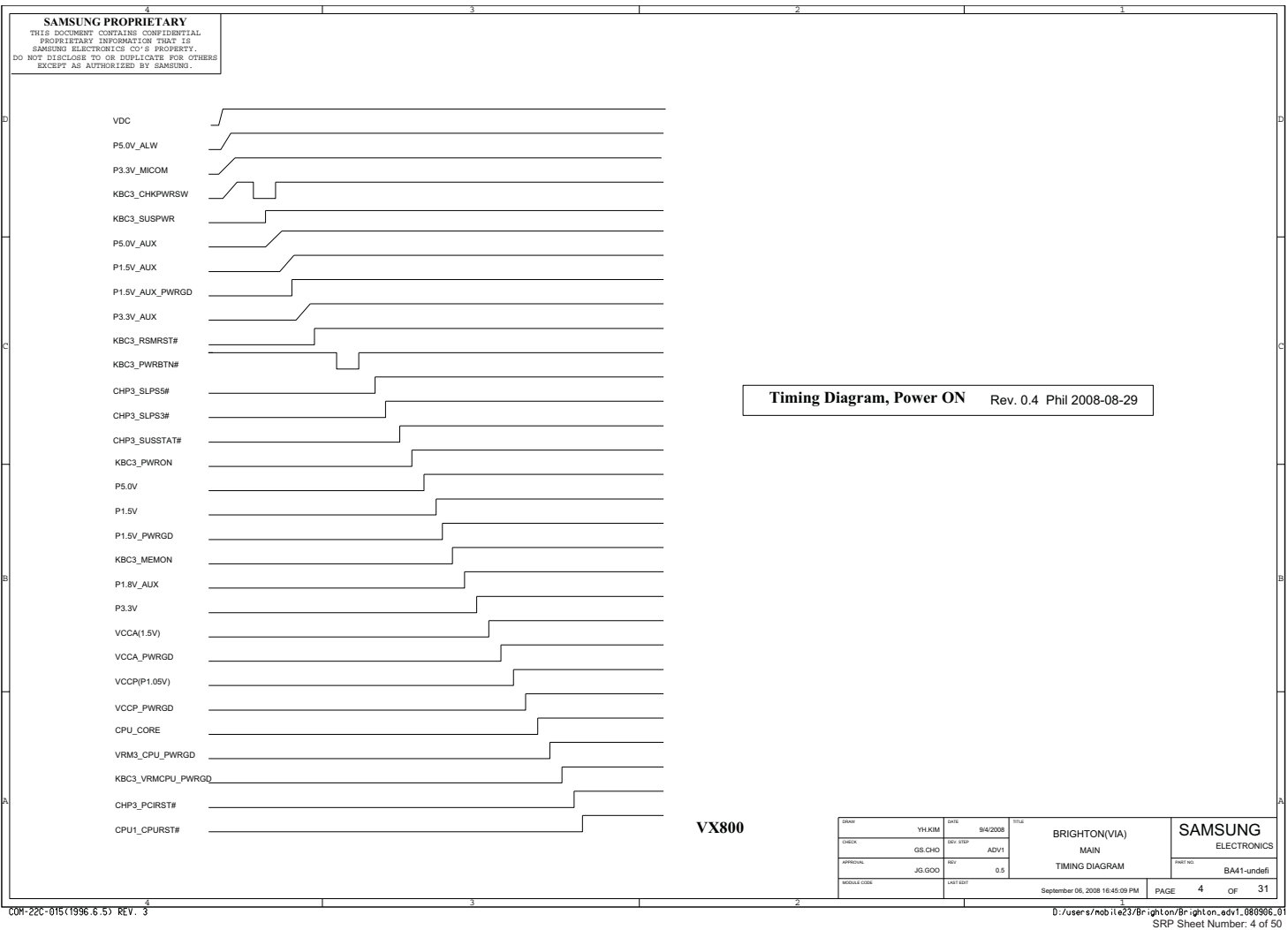
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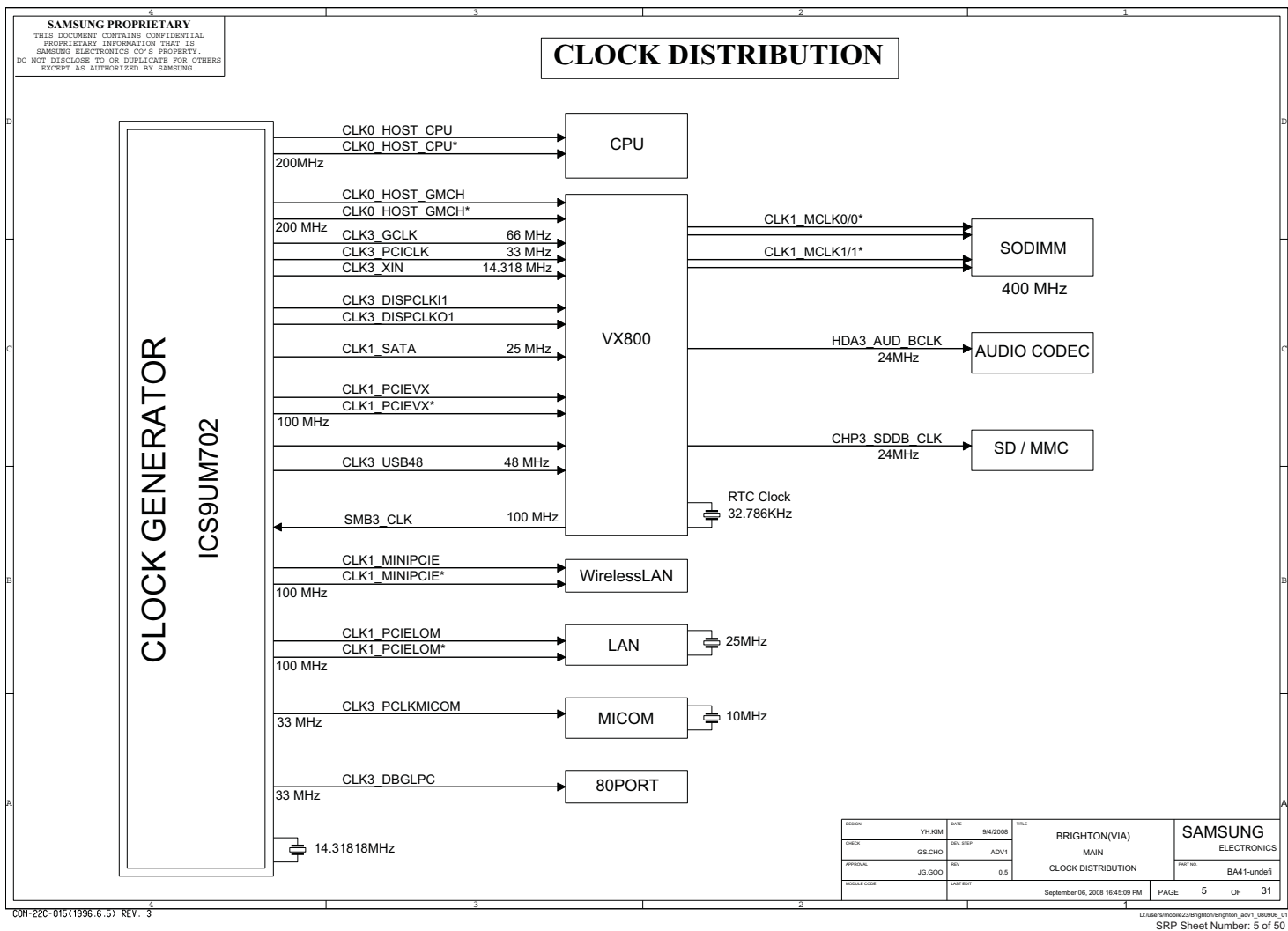
- ## 8. Block Diagram and Schematic



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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

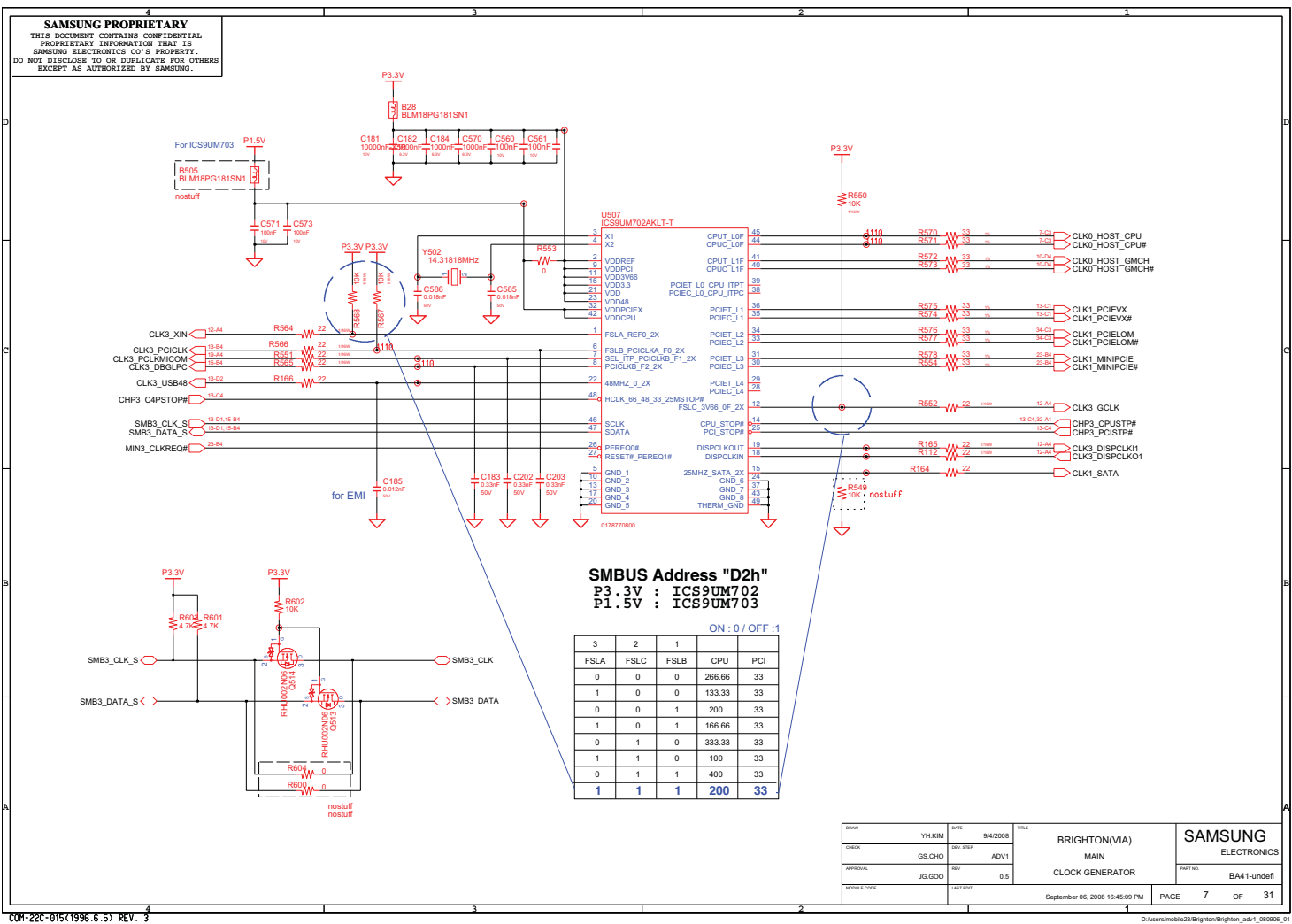
Power Rail	Devices (Page Number)
PSV	FAN(8) MICOM(8) CRT(8) CAMERA(9) AUDIO(20) VRM(25) TOUCHPAD(9) HDD(8)
P3.3V	VX800(13) LCD(24) HDD(8) CLOCK(7) AUDIO(20) HSDPA(9) DDR2(9)
P1.5V	VX800(13) HSDPA(9)
VCCA(P1.5V)	CPU(11)
VCCP(1.05V)	CPU(11)
PSV_AUX	DDR2 PWR VRM(10) USB(9,30)
P3.3V_AUX	VX800(13) MULTIMEDIA CARD(18) THERMAL(8) LAN(19)
P1.8V_AUX	DDR2(9)
P1.5V_AUX	VX800(13)
CPU_CORE	CPU(11)

V0	V1	V2	V3	V4	V5	V6	V7	V8	V9	Voltage	V1D5	V1D4	V1D3	V1D2	V1D1	V1D0	Voltage
0	0	0	0	0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V
0	0	0	0	0	0	0	0	0	1	1.892 V	1	0	0	0	0	1	1.180 V
0	0	0	0	0	0	0	0	0	1	1.876 V	1	0	0	0	0	1	1.164 V
0	0	0	0	0	0	0	0	0	1	1.860 V	1	0	0	0	0	1	1.148 V
0	0	0	0	0	0	0	0	0	1	1.844 V	1	0	0	0	0	1	1.132 V
0	0	0	0	0	0	0	0	0	1	1.828 V	1	0	0	0	0	1	1.116 V
0	0	0	0	0	0	0	0	0	1	1.812 V	1	0	0	0	0	1	1.100 V
0	0	0	0	0	0	0	0	0	1	1.796 V	1	0	0	0	1	1	1.084 V
0	0	0	0	0	0	0	0	0	1	1.580 V	1	0	0	0	0	1	1.068 V
0	0	0	0	0	0	0	0	0	1	1.564 V	1	0	0	0	0	1	1.052 V
0	0	0	0	0	0	0	0	0	1	1.548 V	1	0	0	0	0	1	1.036 V
0	0	0	0	0	0	0	0	0	1	1.532 V	1	0	0	0	0	1	1.020 V
0	0	0	0	0	0	0	0	0	1	1.516 V	1	0	0	0	0	1	1.004 V
0	0	0	0	0	0	0	0	0	1	1.500 V	1	0	0	0	0	1	0.988 V
0	0	0	0	0	0	0	0	0	1	1.484 V	1	0	0	0	0	1	0.972 V
0	0	0	0	0	0	0	0	0	1	1.468 V	1	0	0	0	0	1	0.956 V
0	0	0	0	0	0	0	0	0	1	1.452 V	1	0	0	0	0	1	0.940 V
0	0	0	0	0	0	0	0	0	1	1.436 V	1	0	0	0	0	1	0.924 V
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0	0	0	0	0	0	0	0	0	1	1.404 V	1	0	0	0	0	1	0.892 V
0	0	0	0	0	0	0	0	0	1	1.388 V	1	0	0	0	0	1	0.876 V
0	0	0	0	0	0	0	0	0	1	1.372 V	1	0	0	0	0	1	0.860 V
0	0	0	0	0	0	0	0	0	1	1.356 V	1	0	0	0	0	1	0.844 V
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0	0	0	0	0	0	0	0	0	1	1.308 V	1	0	0	0	0	1	0.796 V
0	0	0	0	0	0	0	0	0	1	1.292 V	1	0	0	0	0	1	0.780 V
0	0	0	0	0	0	0	0	0	1	1.276 V	1	0	0	0	0	1	0.764 V
0	0	0	0	0	0	0	0	0	1	1.260 V	1	0	0	0	0	1	0.748 V
0	0	0	0	0	0	0	0	0	1	1.244 V	1	0	0	0	0	1	0.728 V
0	0	0	0	0	0	0	0	0	1	1.228 V	1	0	0	0	0	1	0.712 V
0	0	0	0	0	0	0	0	0	1	1.212 V	1	0	0	0	0	1	0.700 V
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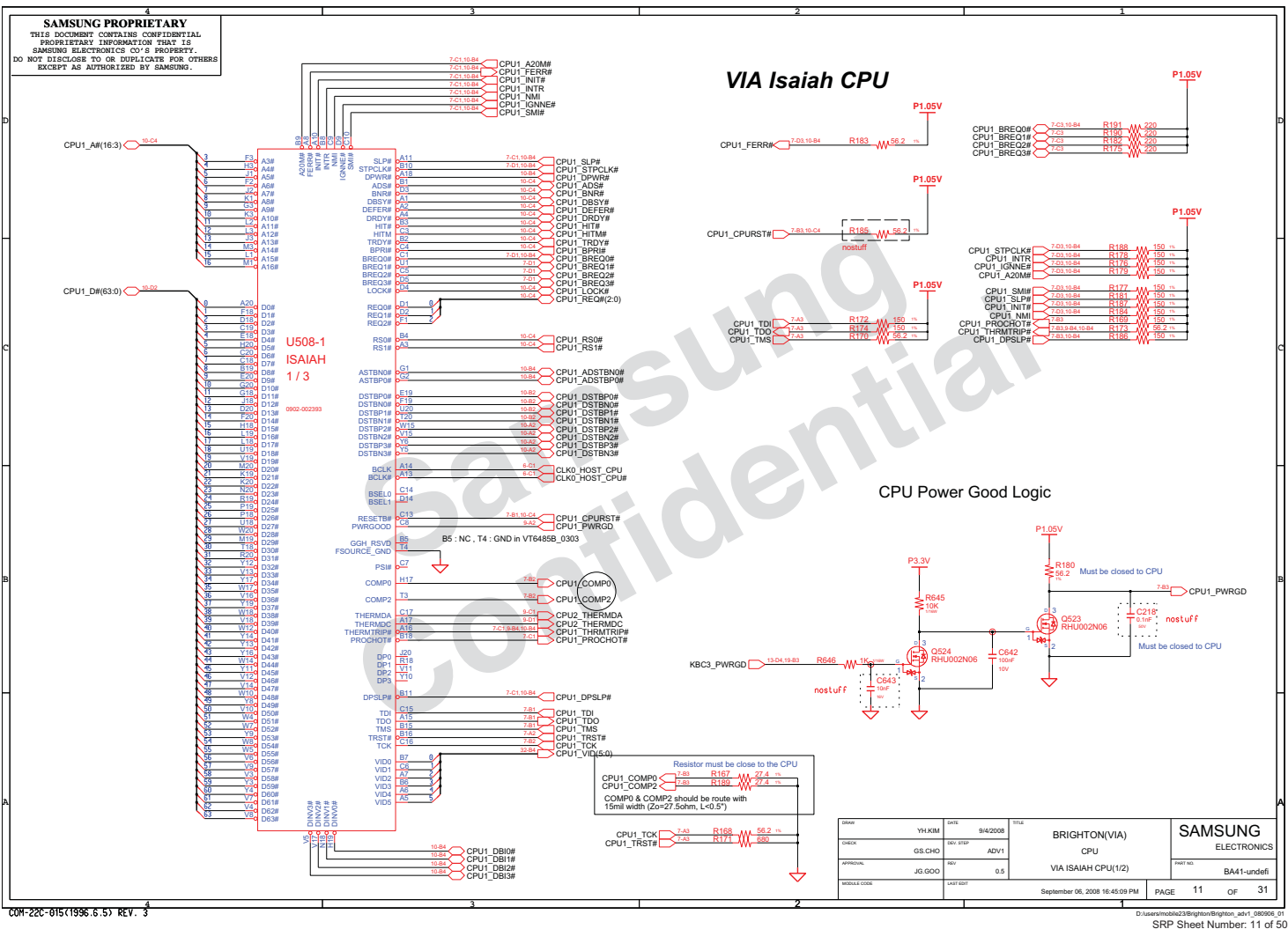
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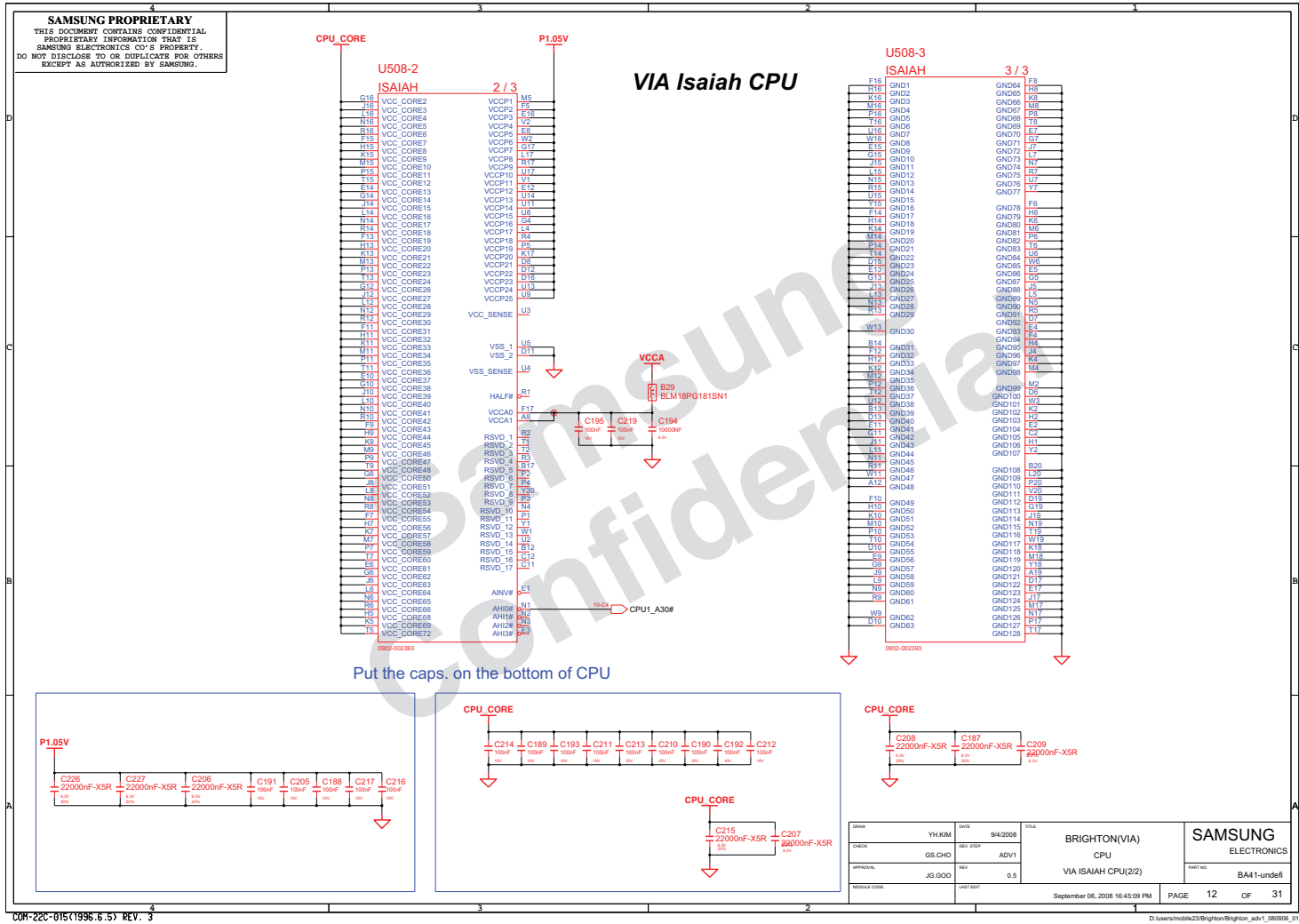
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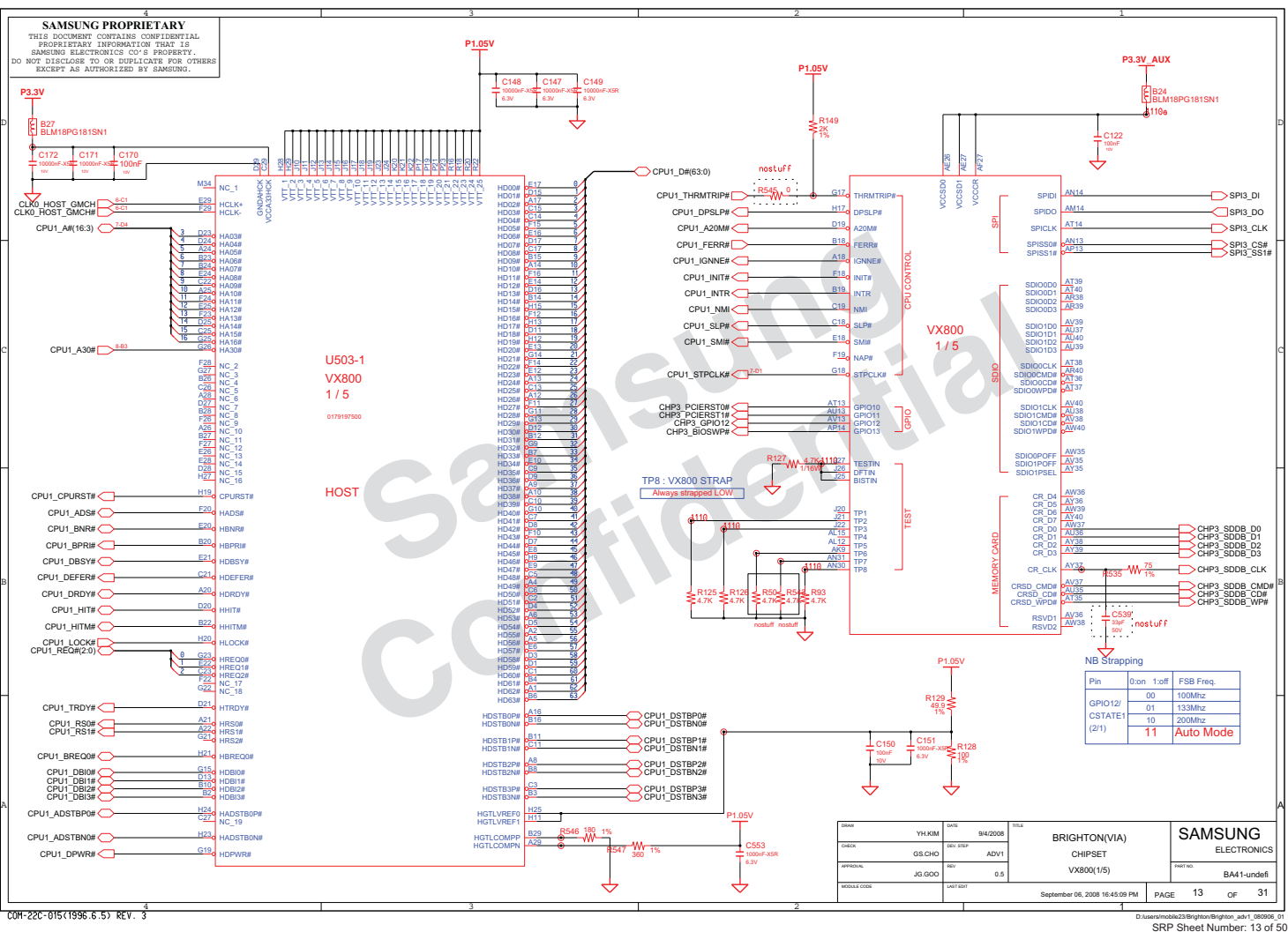
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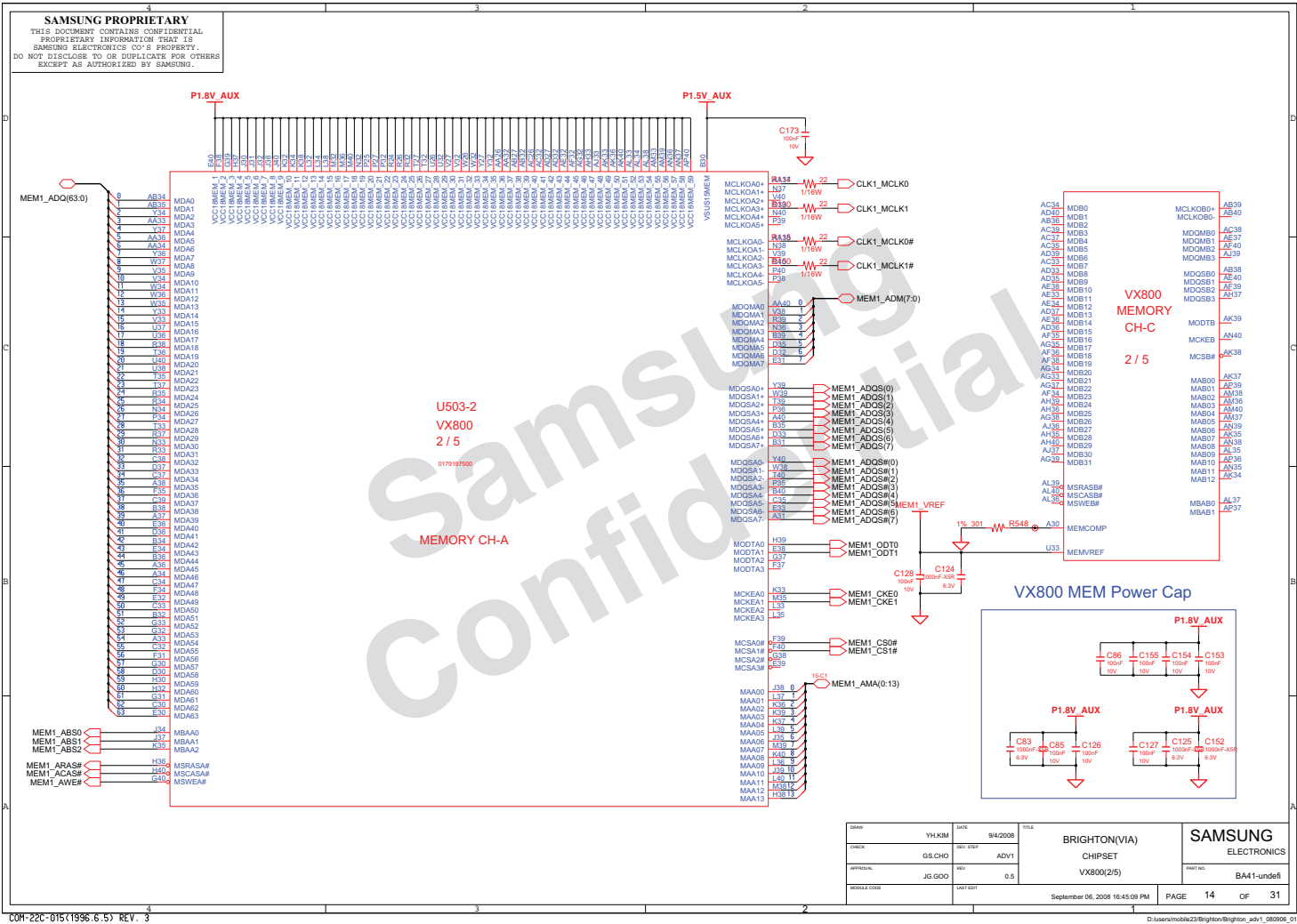
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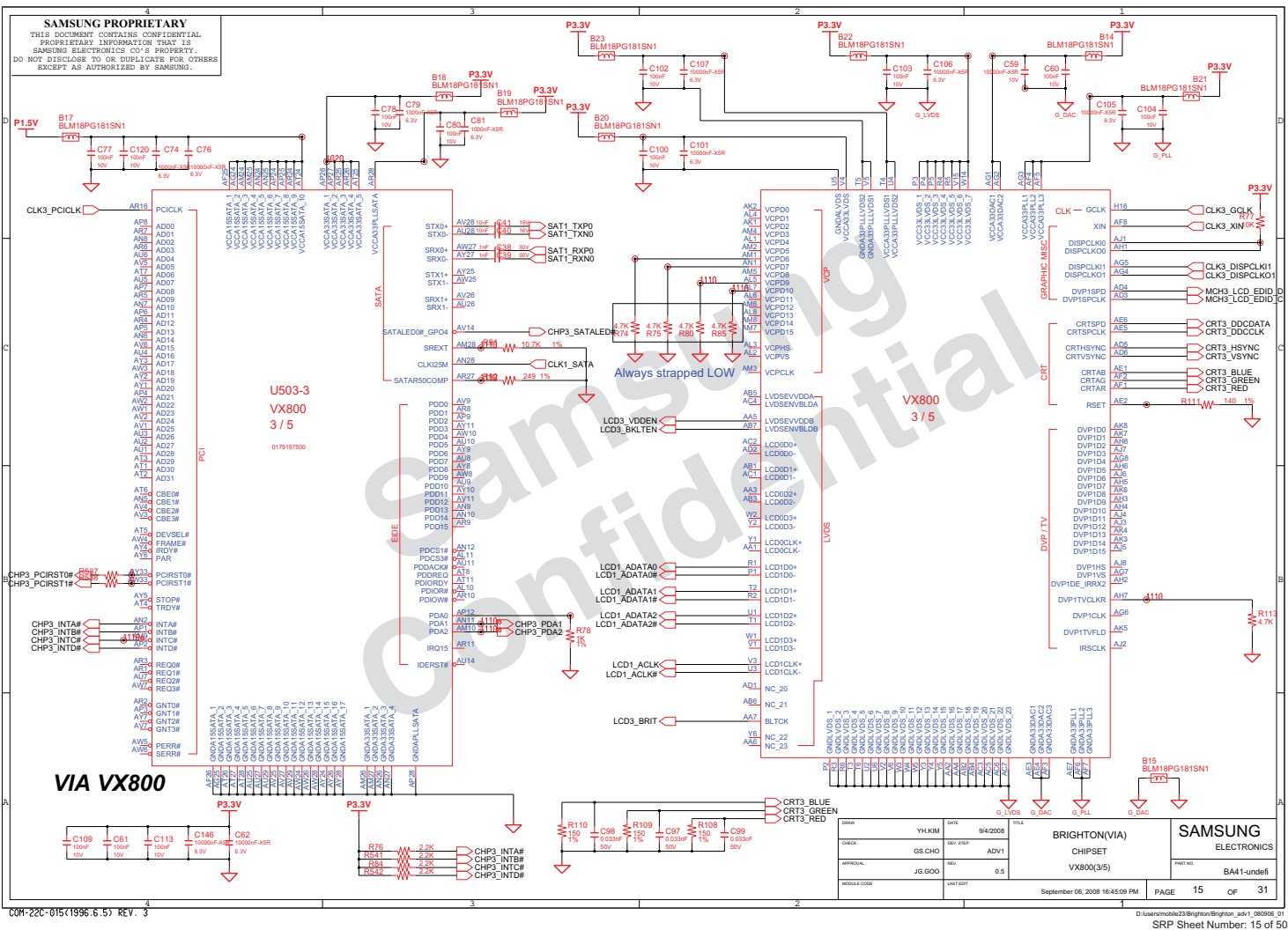
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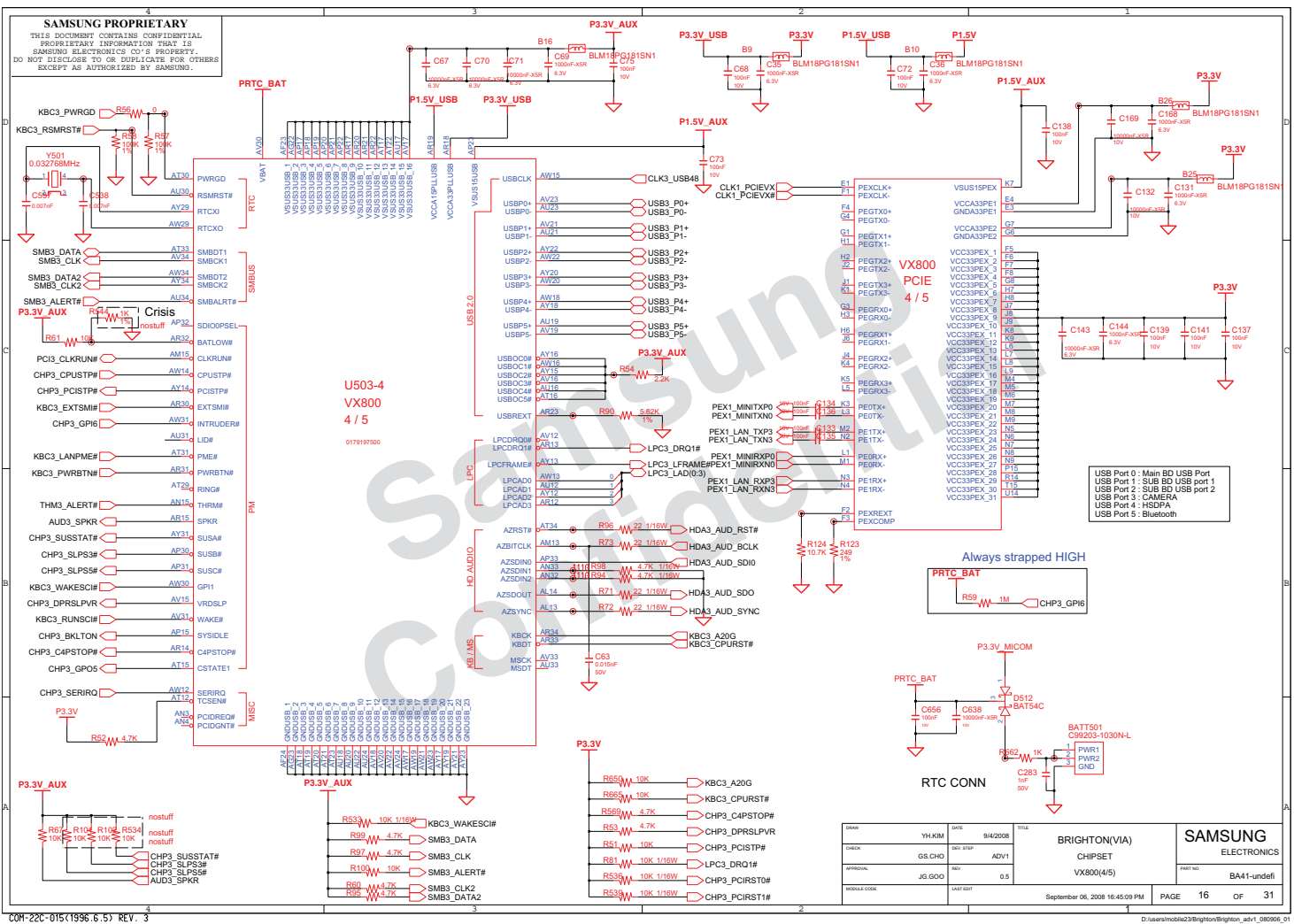


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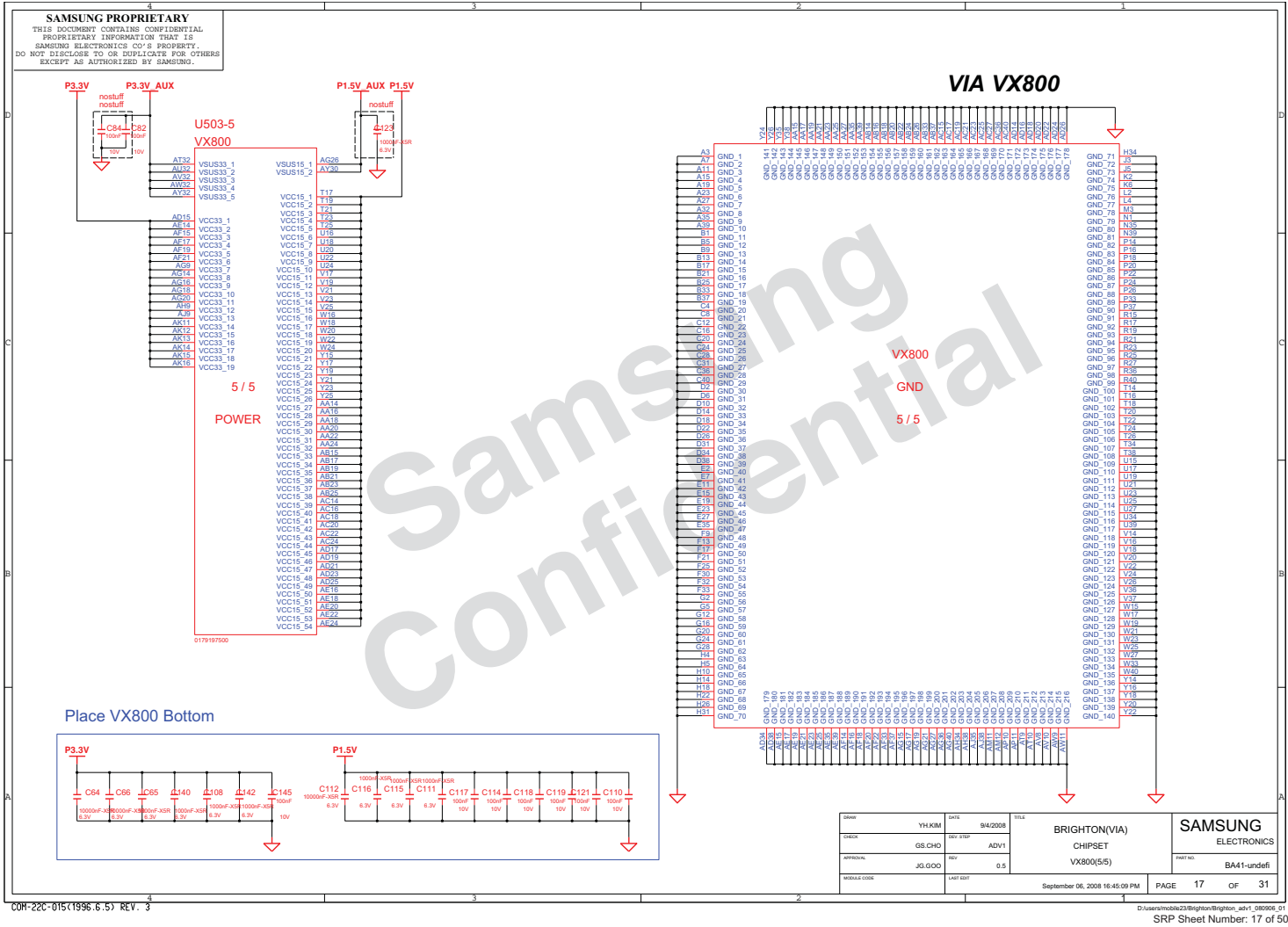


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	Signal	Ball#	Function	Description
	GPIO12 CSTATE1	AV13 AT15	FSB Clock AT15	State(GPIO12 : CSTATE1) Mode(MHz) LL 100MHz LH 133MHz HL 200MHz HH Auto
	SYSIDLE	AP15	IO Queue Depth	L : 12-level deep H : 1-level deep
	GPIO13	AP14	GTL Pull-up	L : Enable internal GTL Pull-up H : Disable internal GTL Pull-up
	PDA1	AN11	Dual Processor Configuration	L : Single Processor H : Dual Processor
	PDA2	AM10	PLL_OK Source Selection	L : PLL_OK from PLL H : PLL_OK_from logic counter
	AZSDOUT	AL14	Auto Reboot	L : Enable H : Disable
	AZSYNC	AL13	LPC FWH Command	L : Enable H : Disable
	AZBITCLK	AM13	SPI/LPC ROM Select	L : LPC ROM H : SPI ROM
	SPISS[1:0]#	AP13 AN13	IDE Controller [sata table support]	State(SPISS[1:0]#) Mode LL IDE Reserved

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9/4/2008

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ADV1

REV.
0.5

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BRIGHTON(VIA)
CHIPSET
VX800 STRAP

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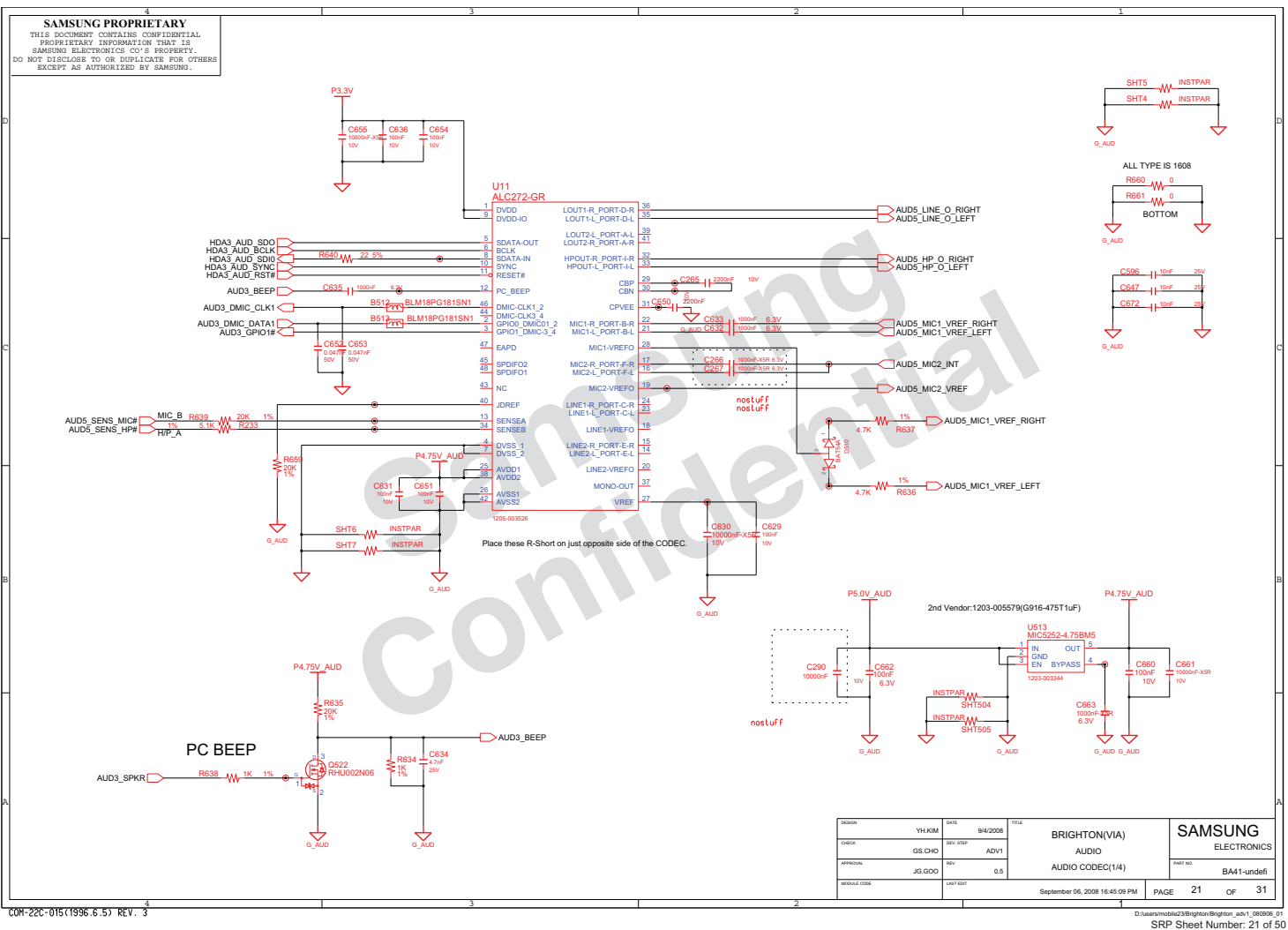
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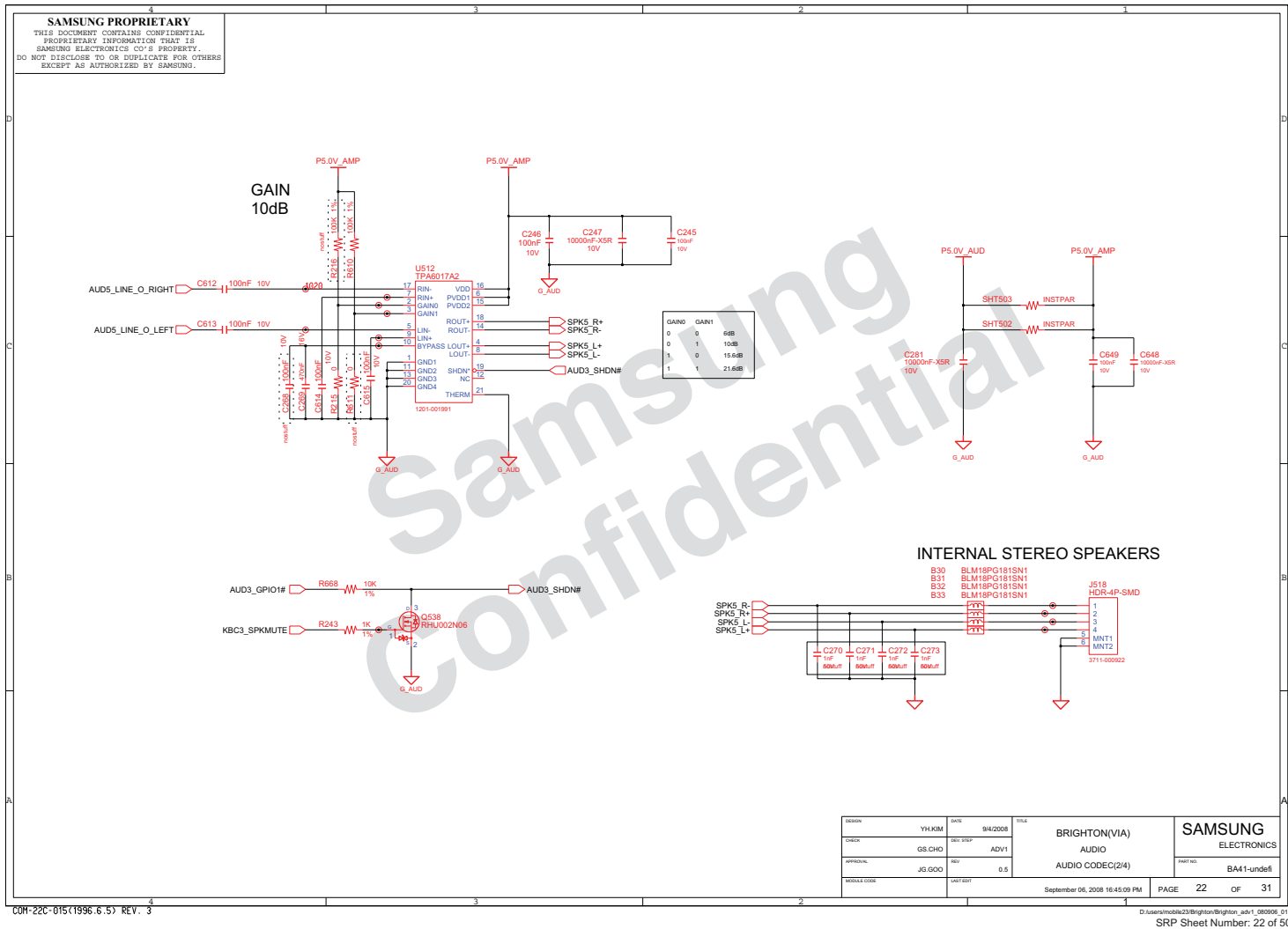
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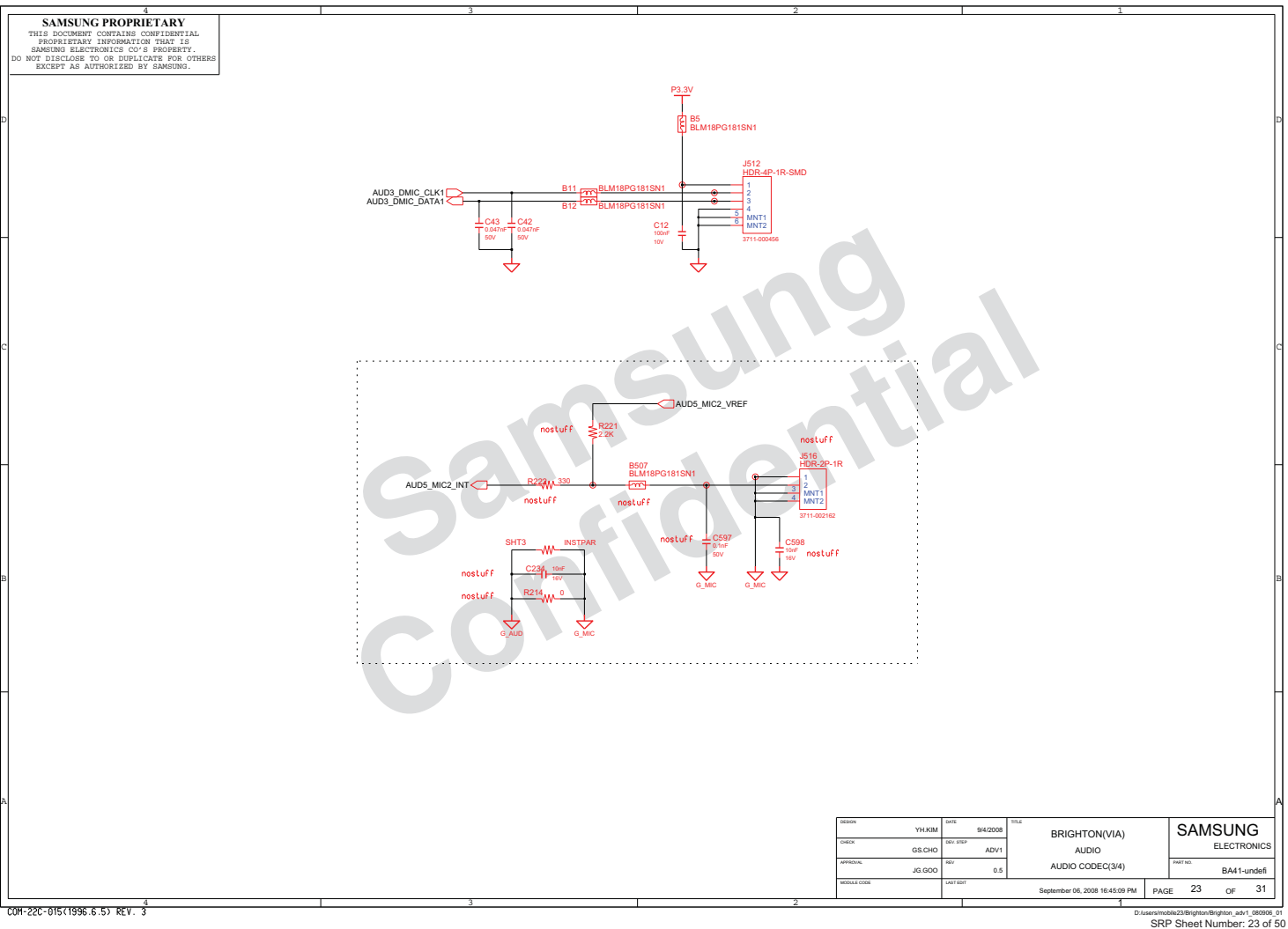


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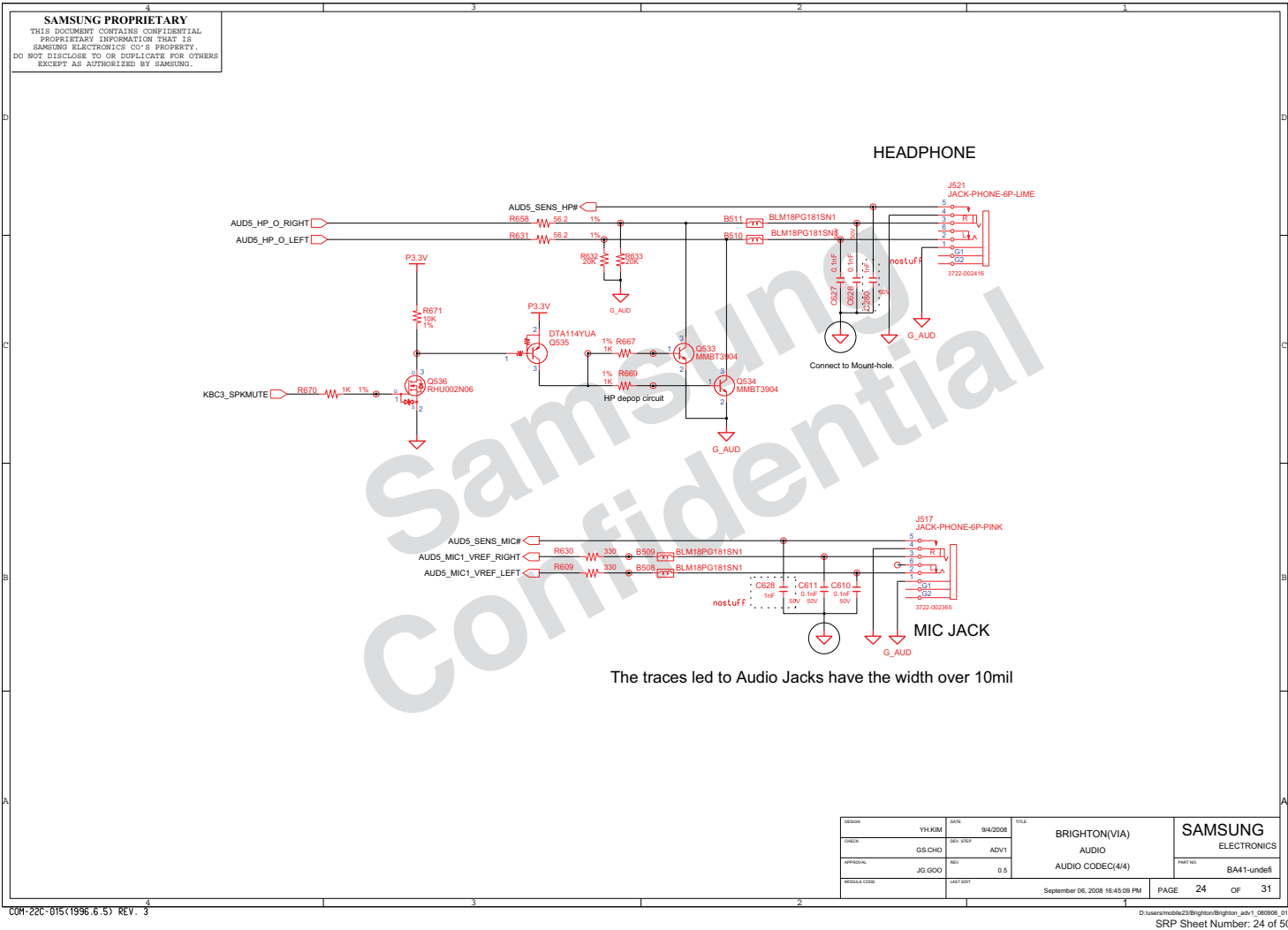
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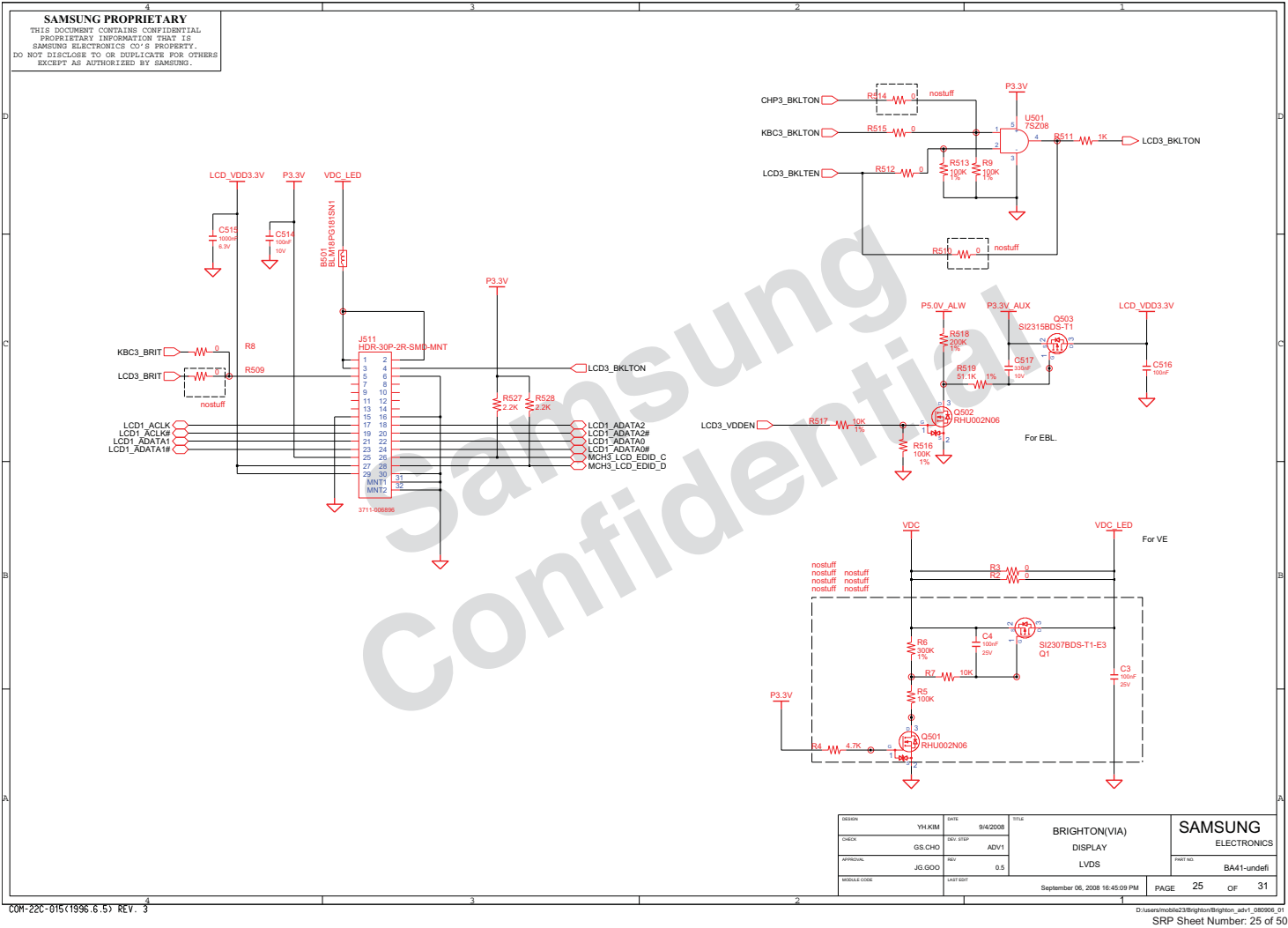


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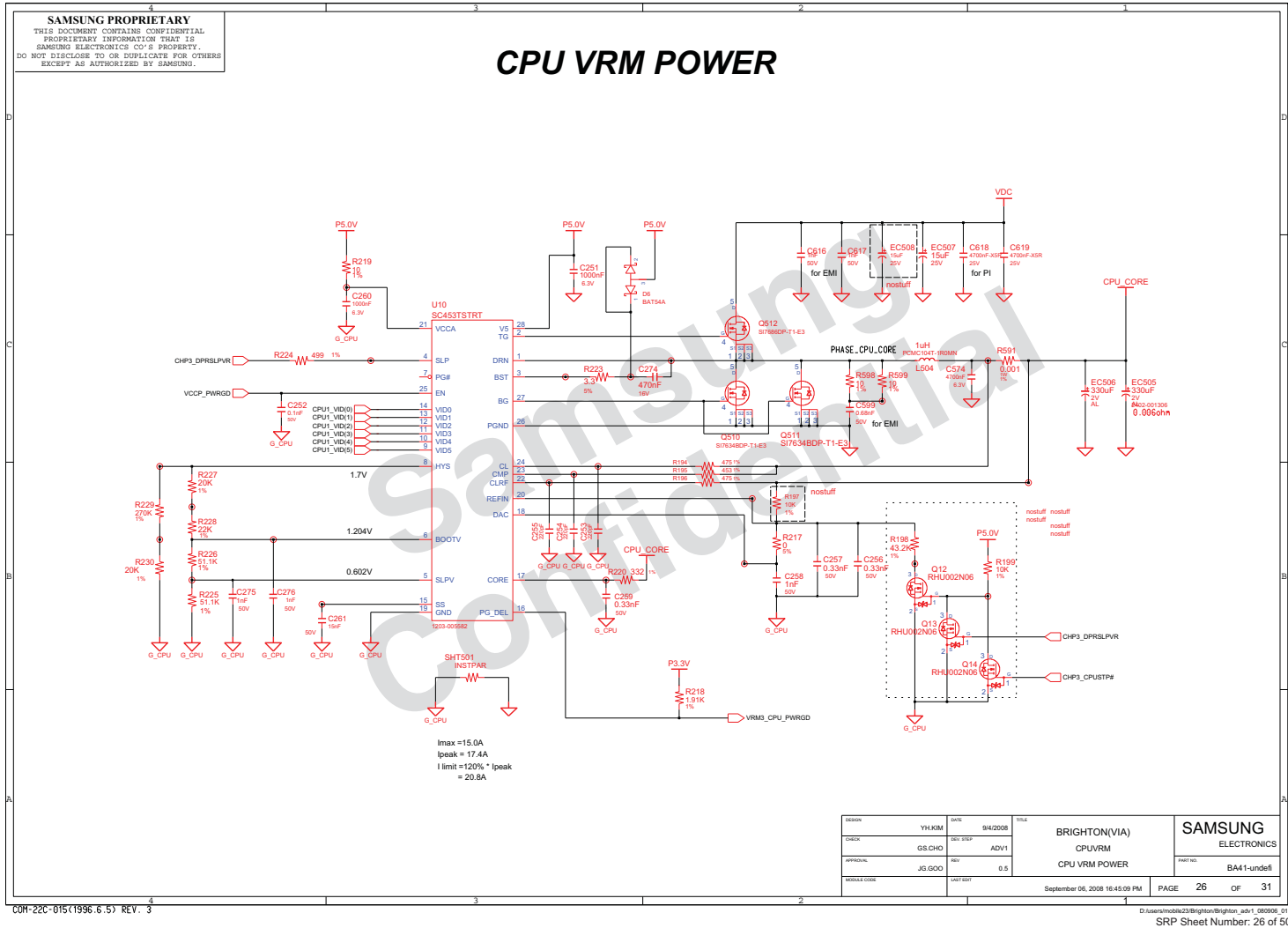


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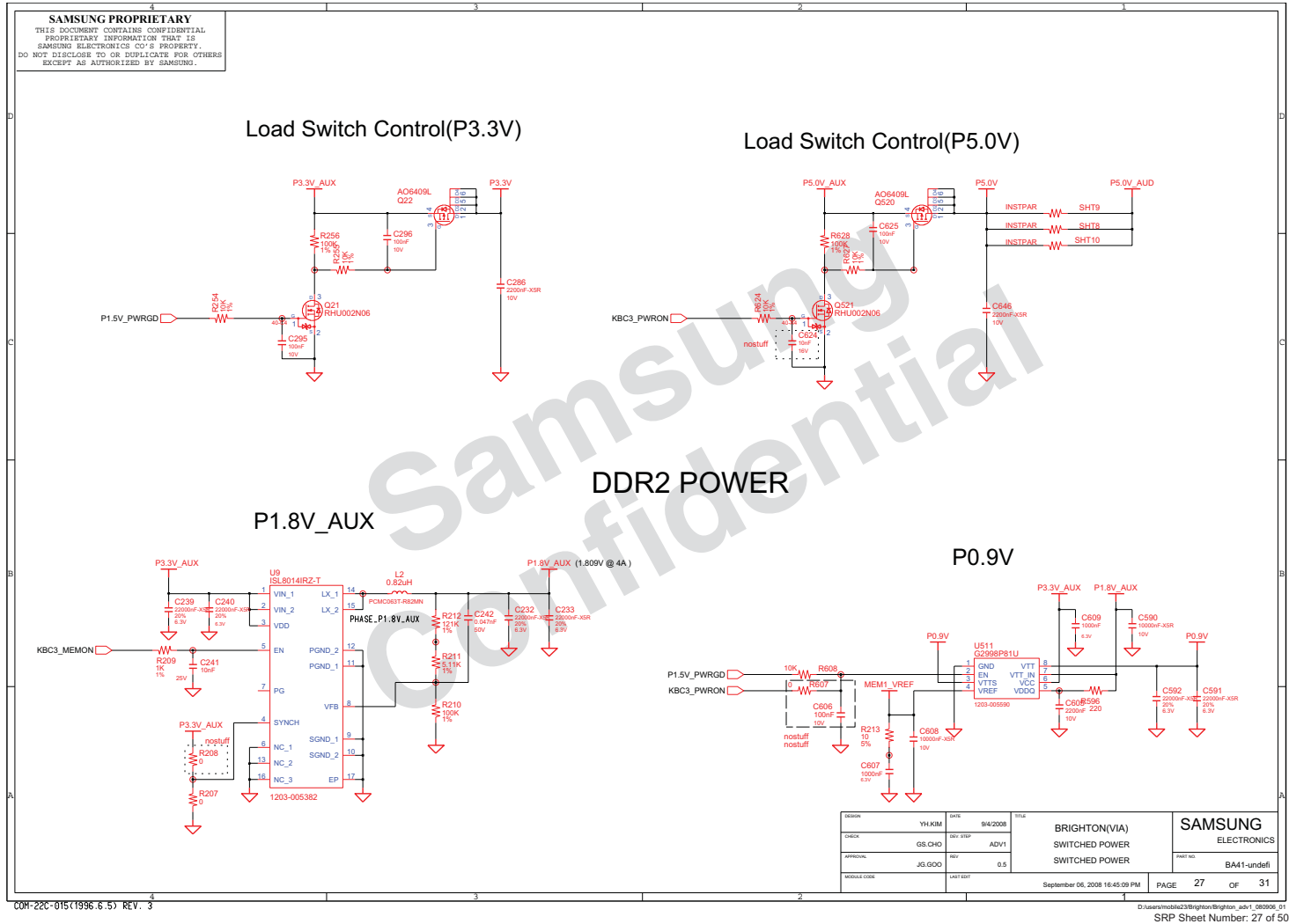


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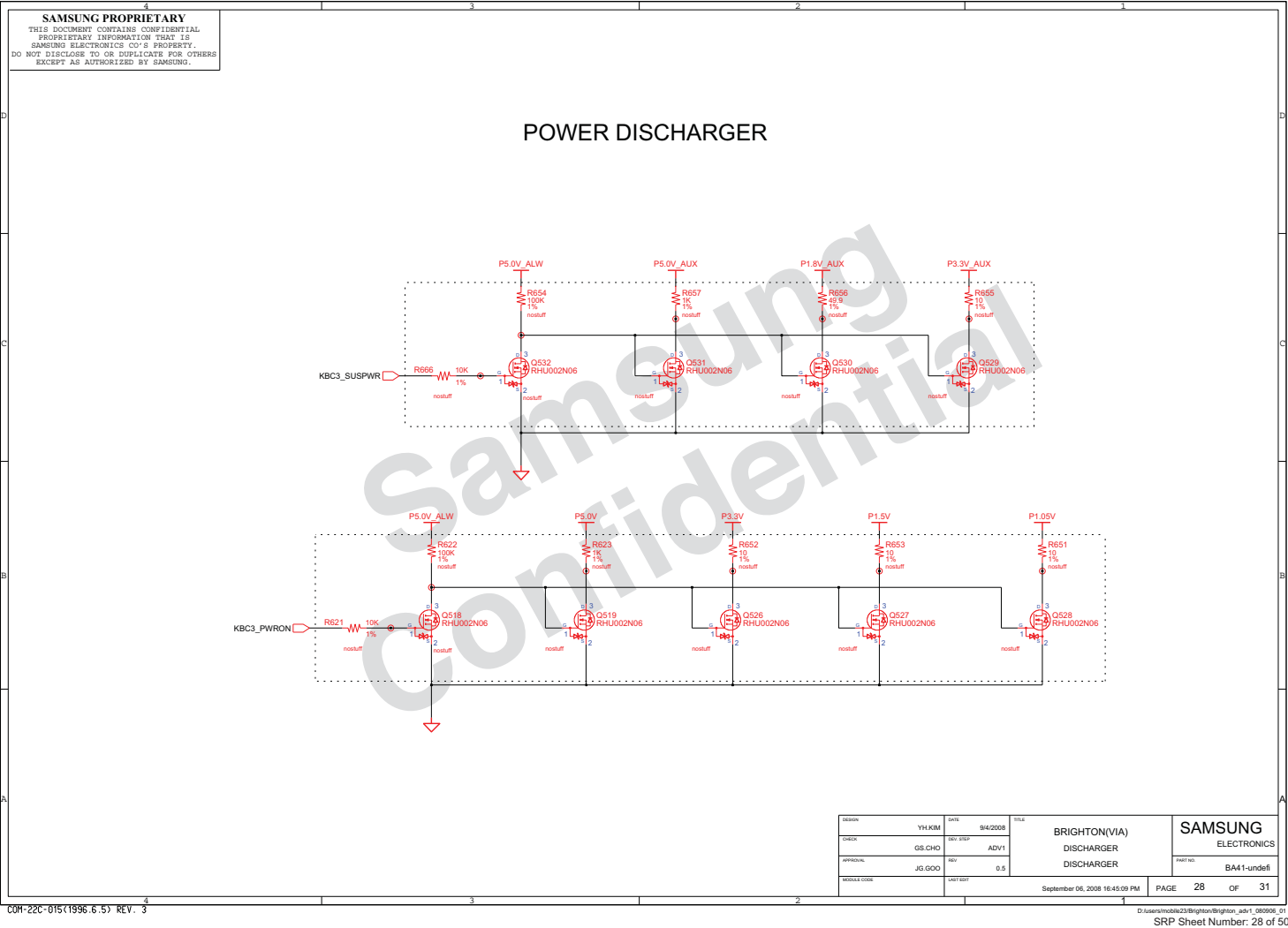
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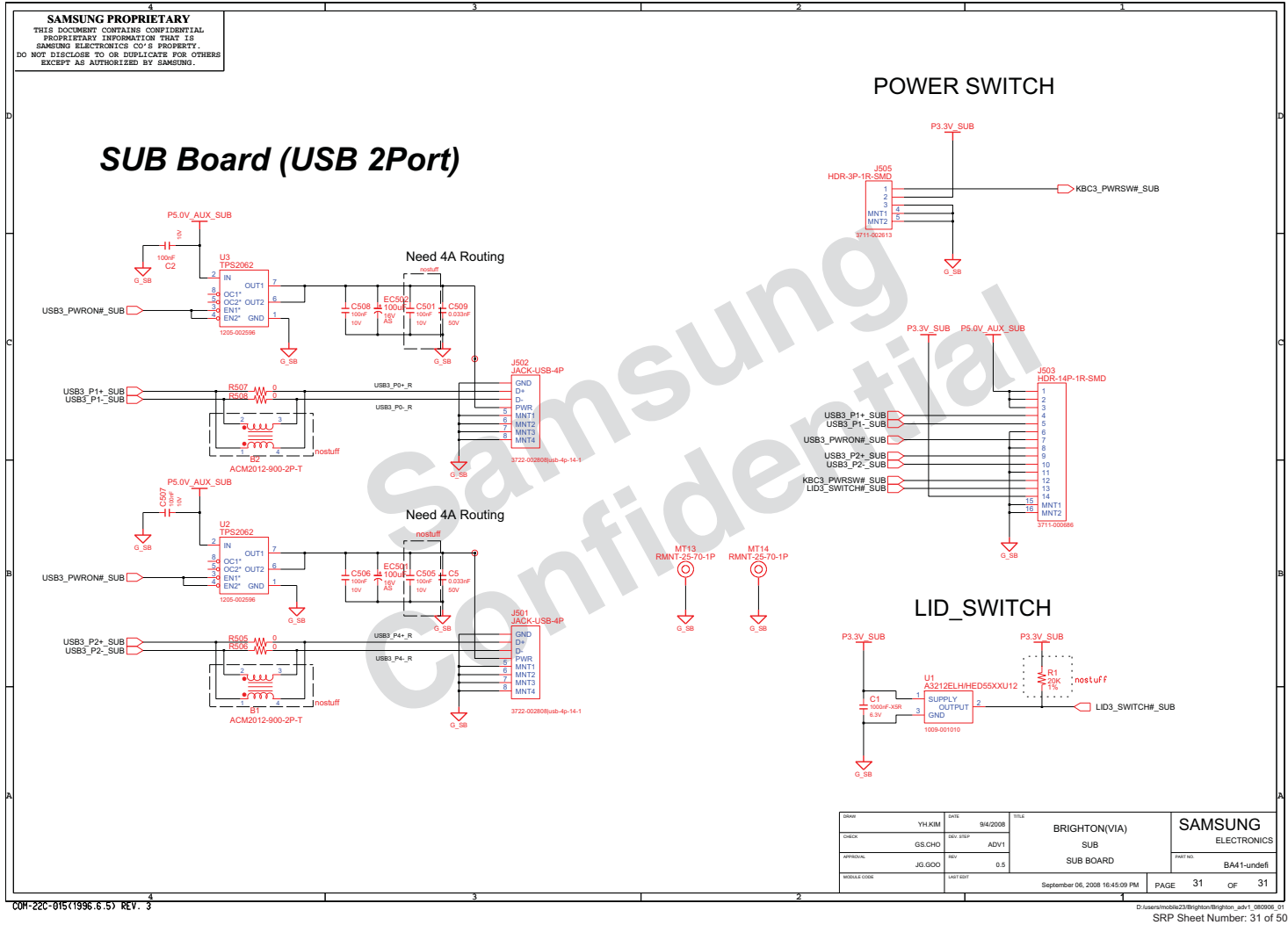


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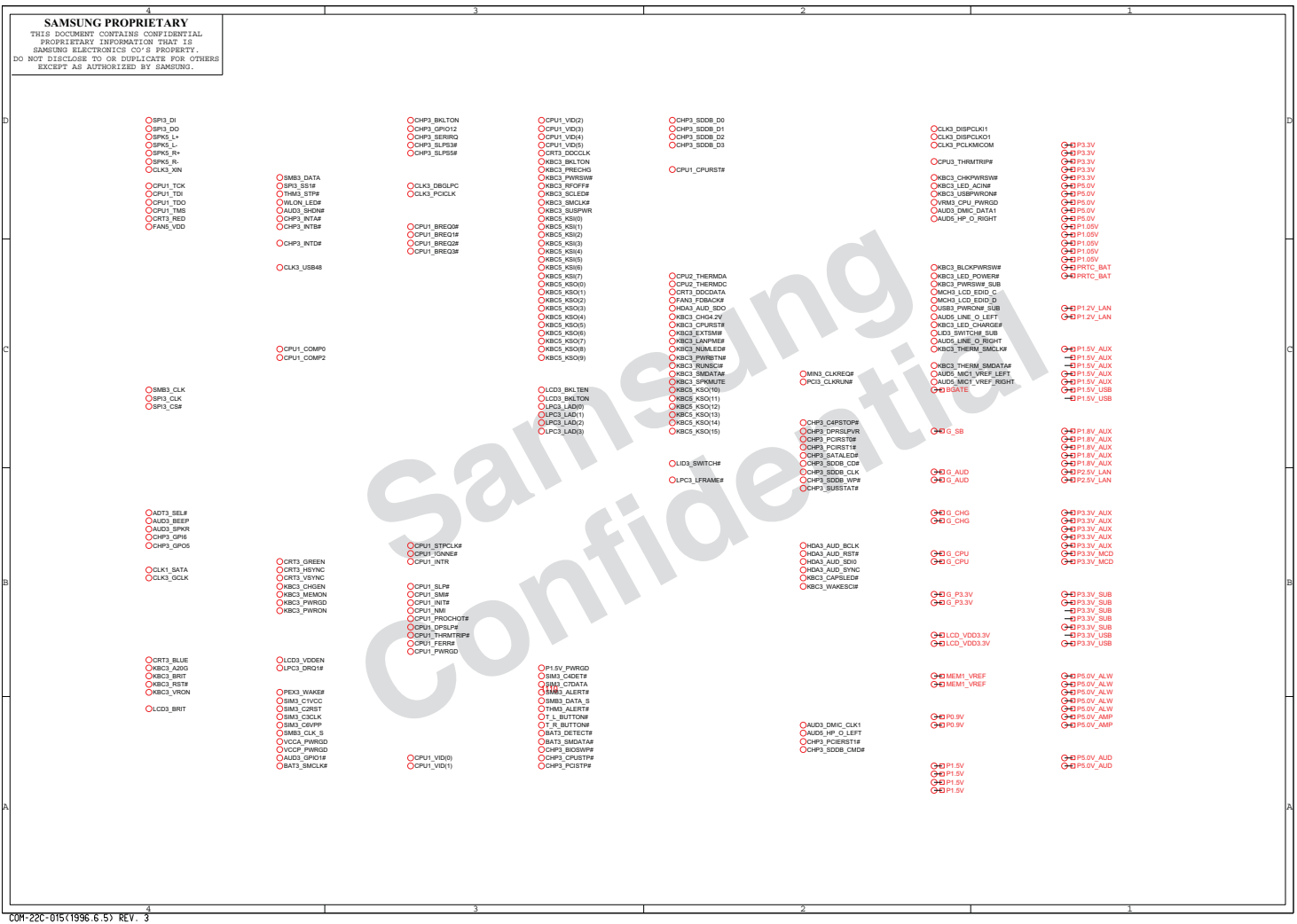
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SIM Card & Main To SUB Board Connector

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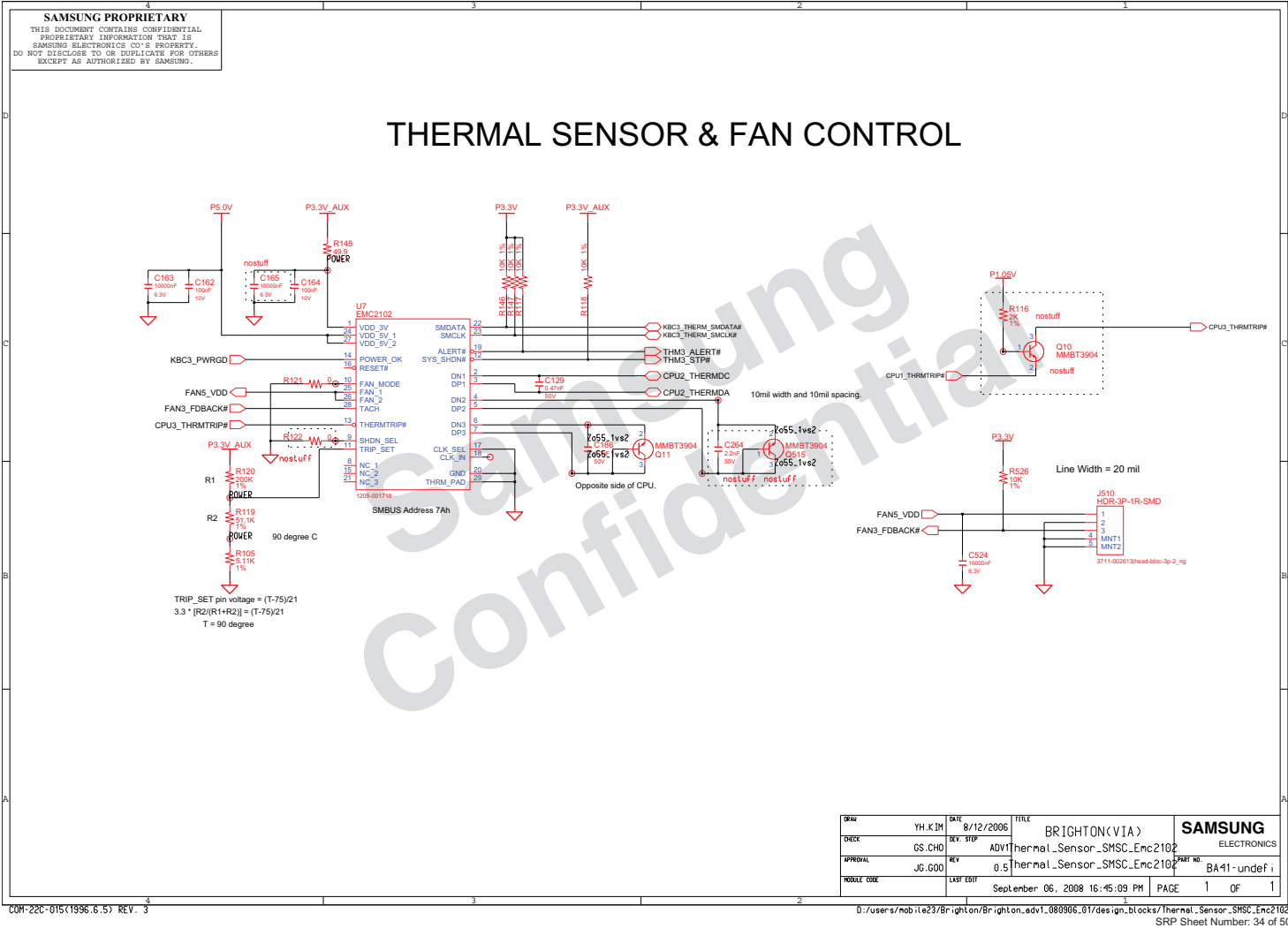


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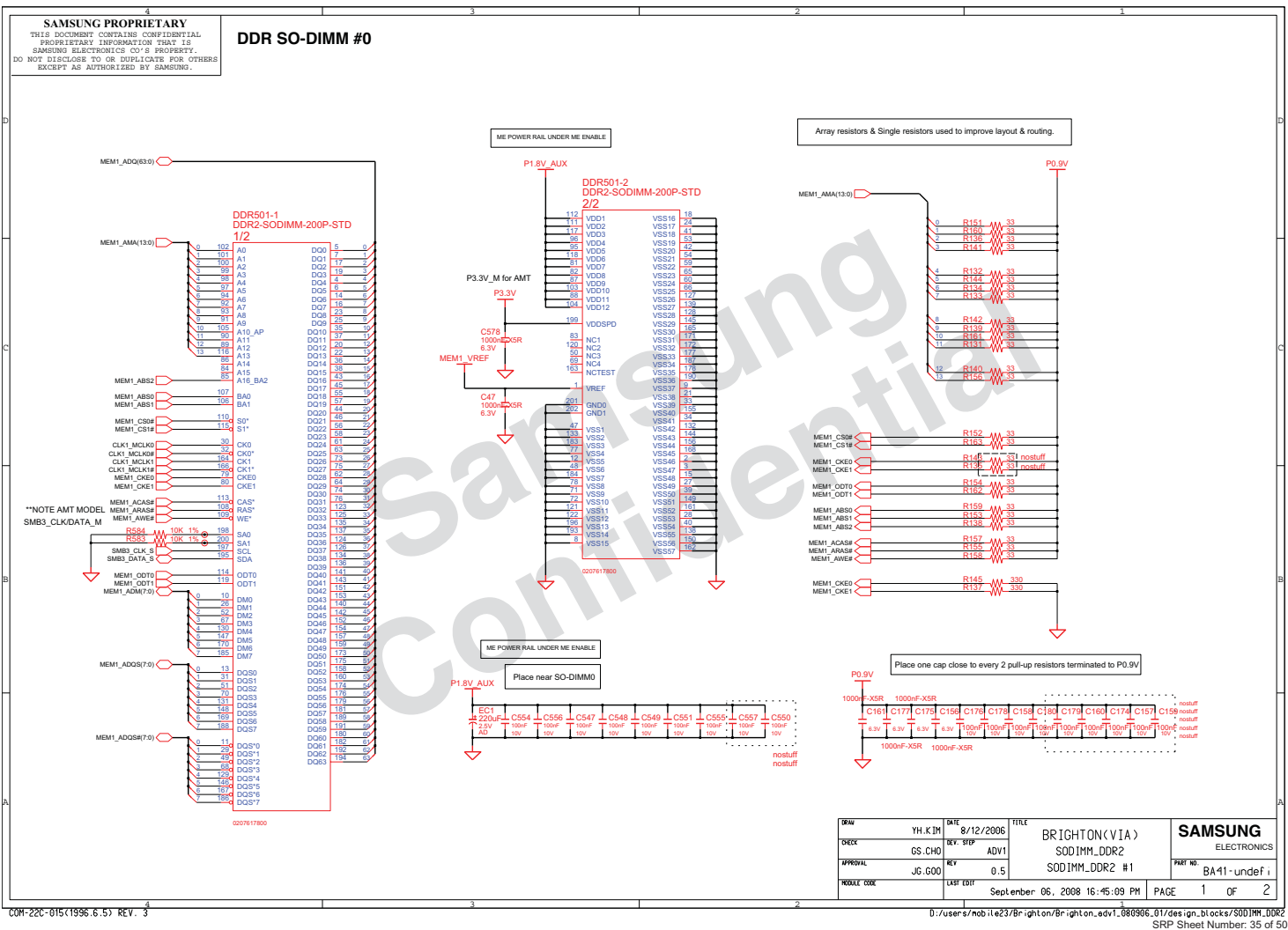


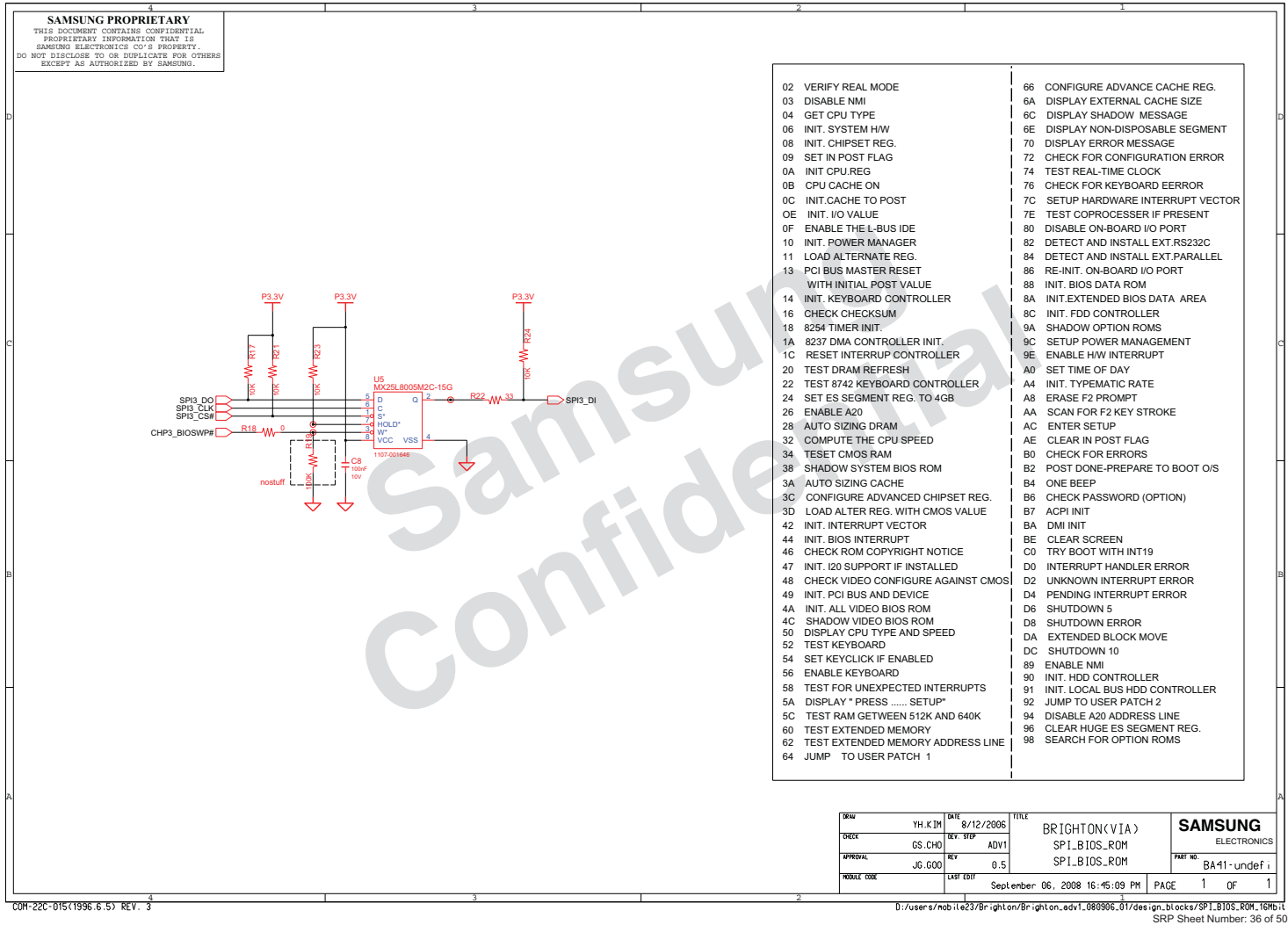
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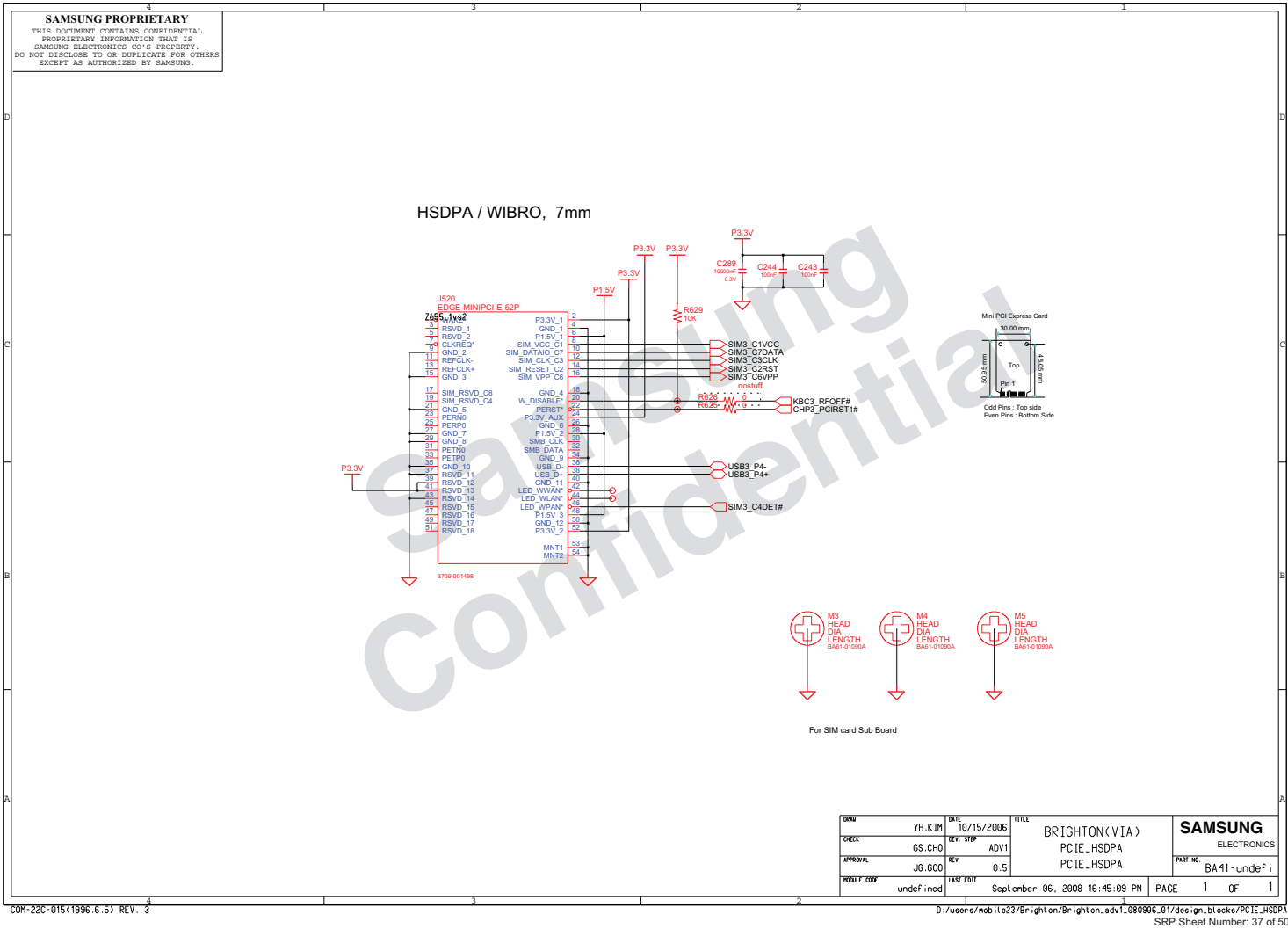




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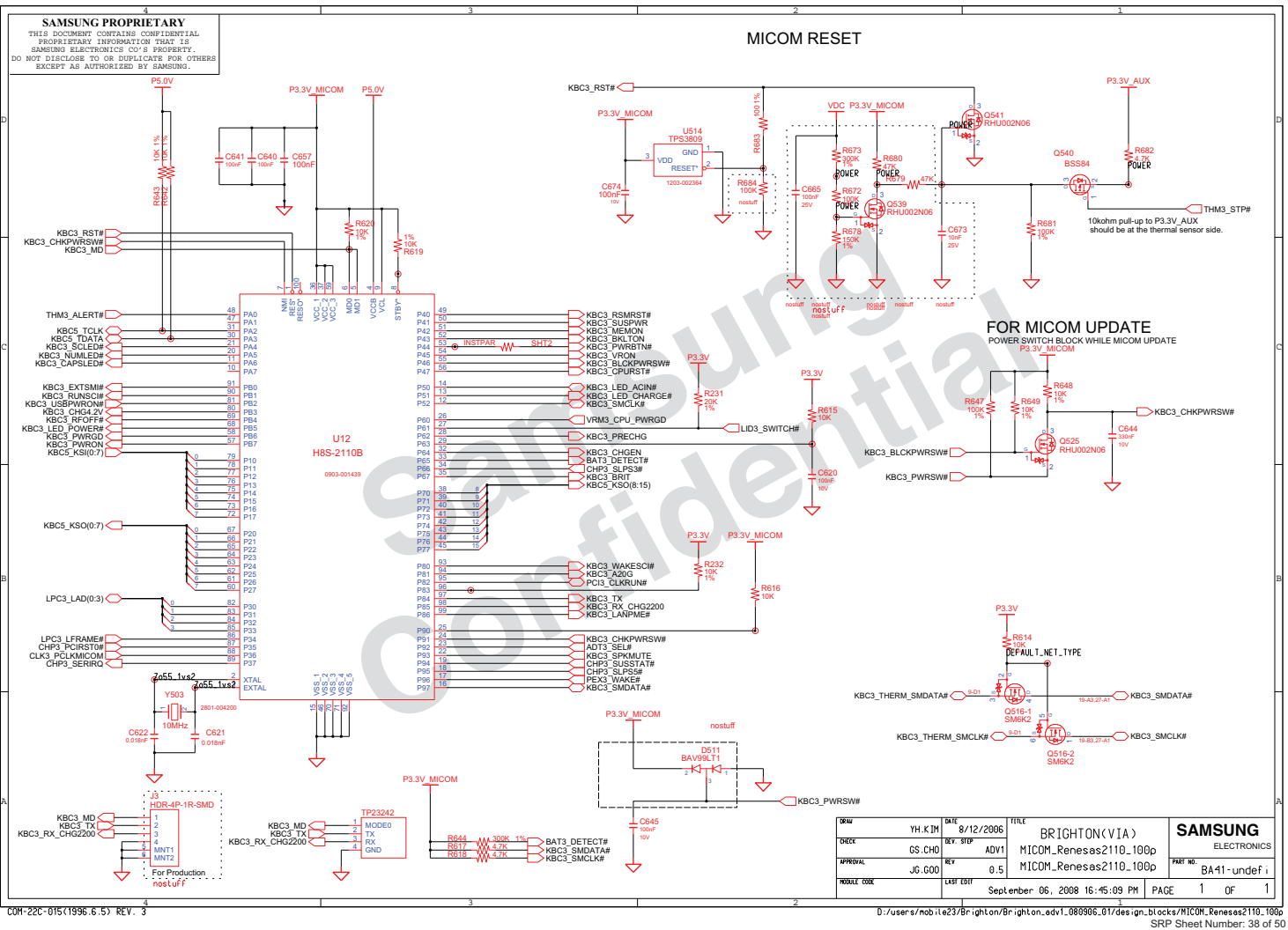
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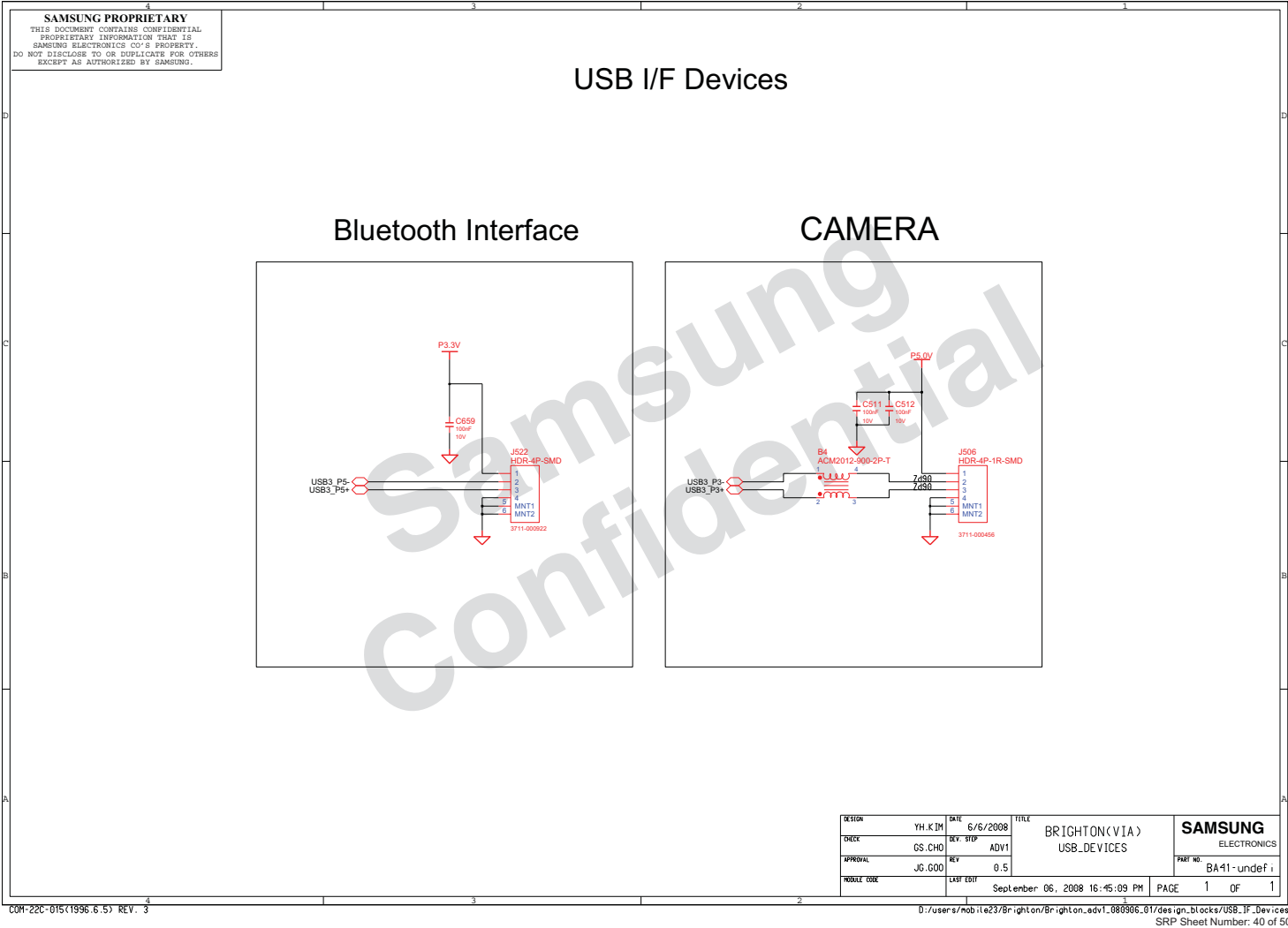
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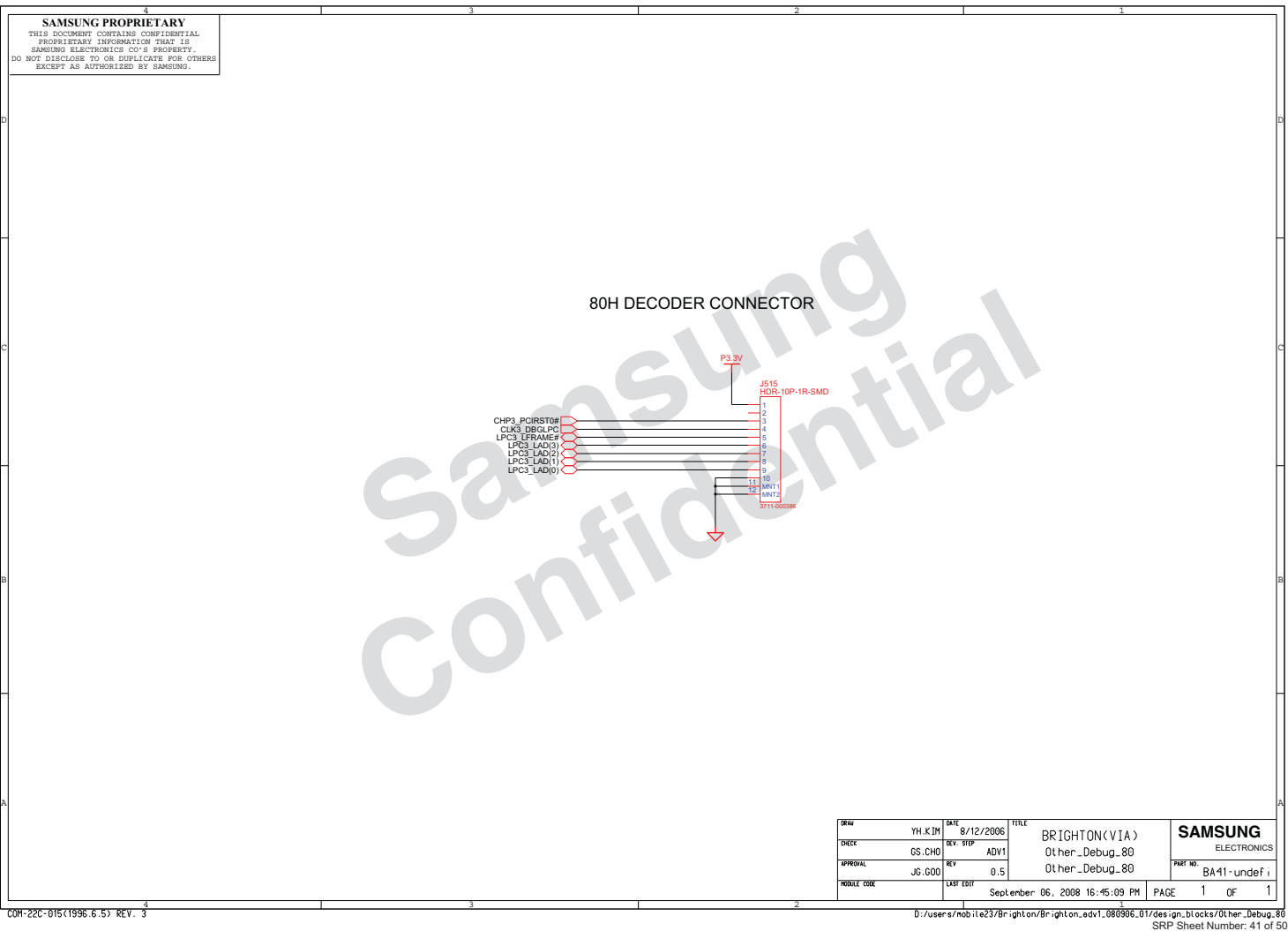
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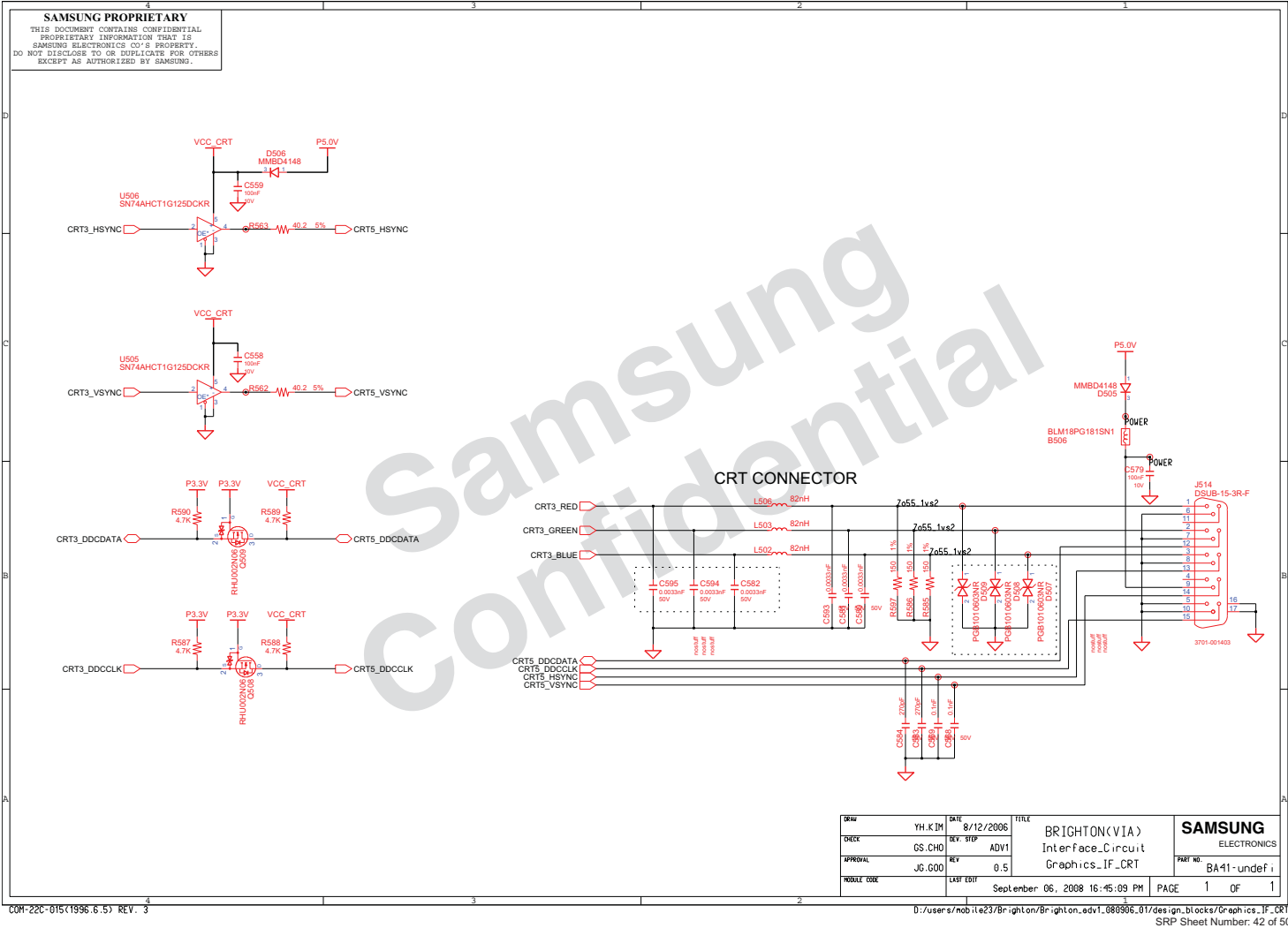


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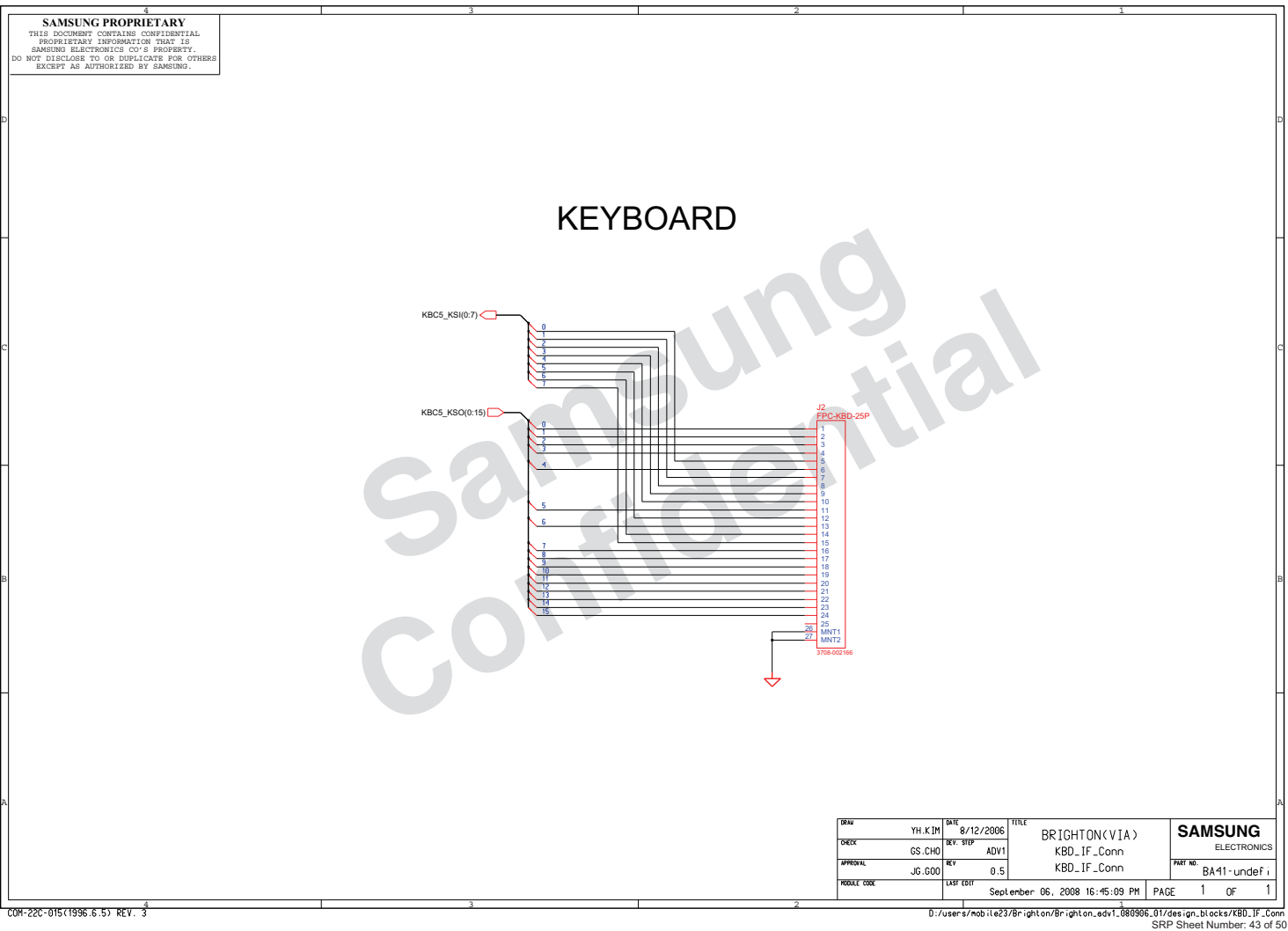


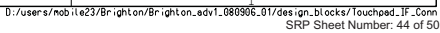
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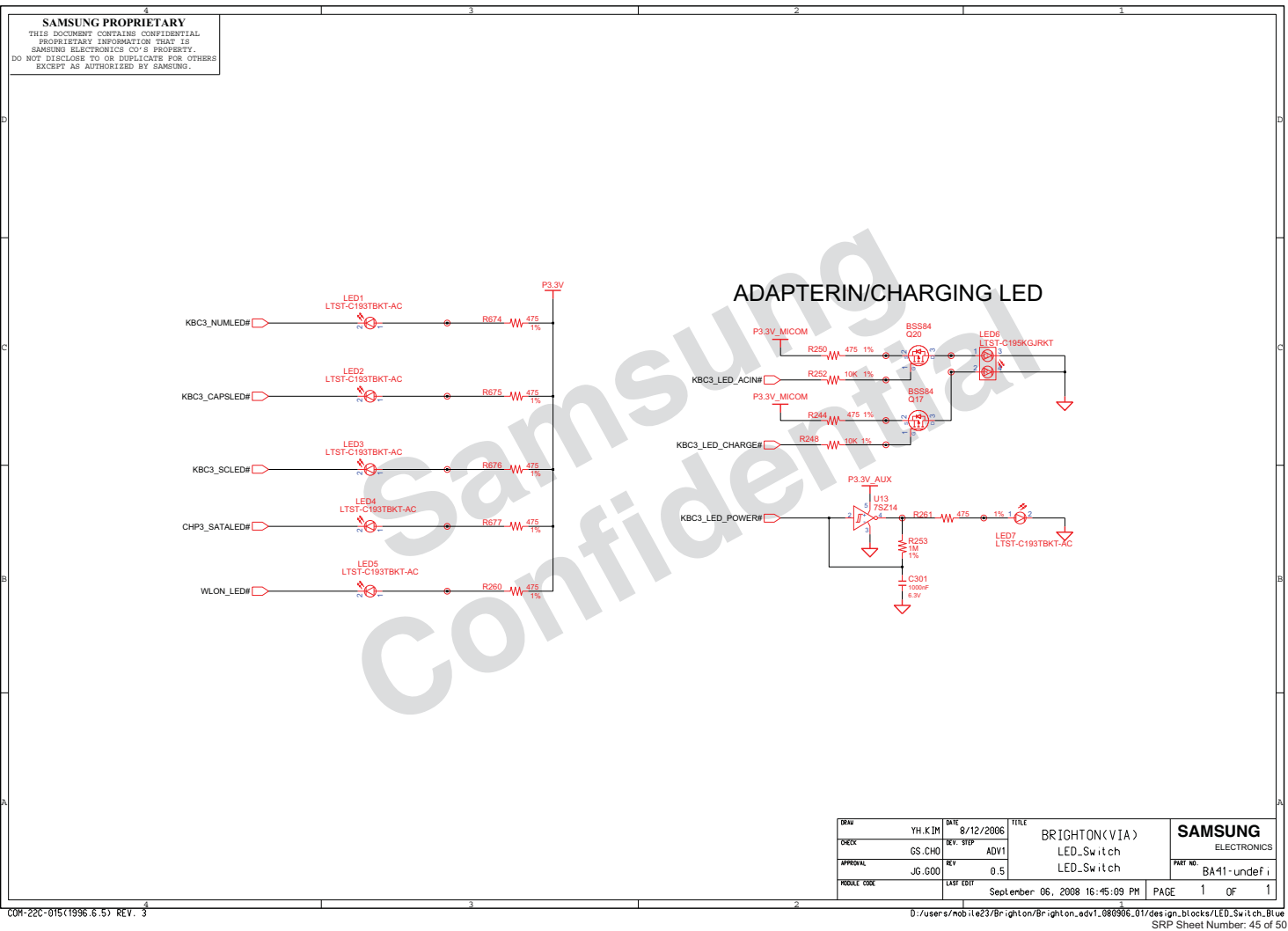
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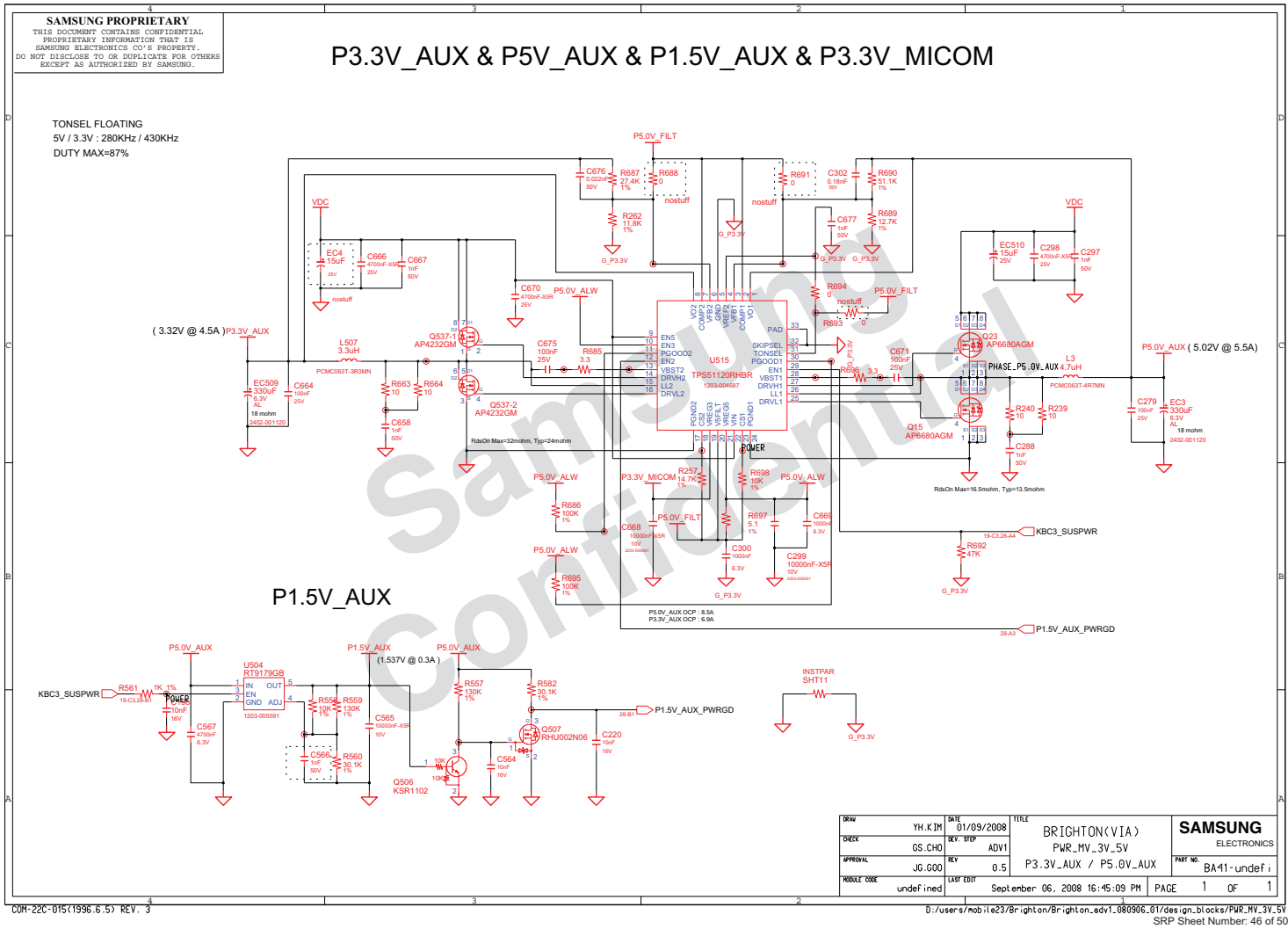




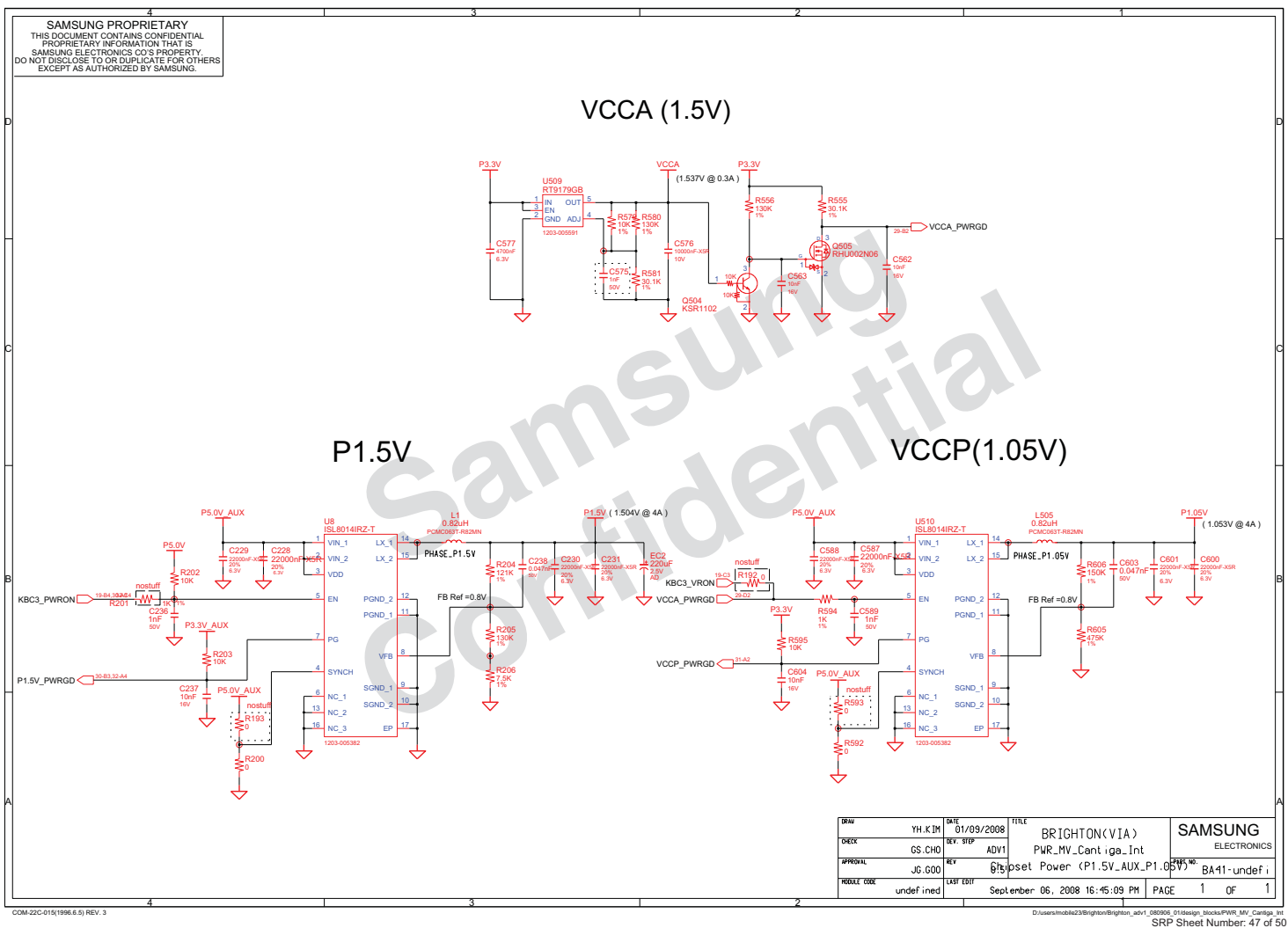
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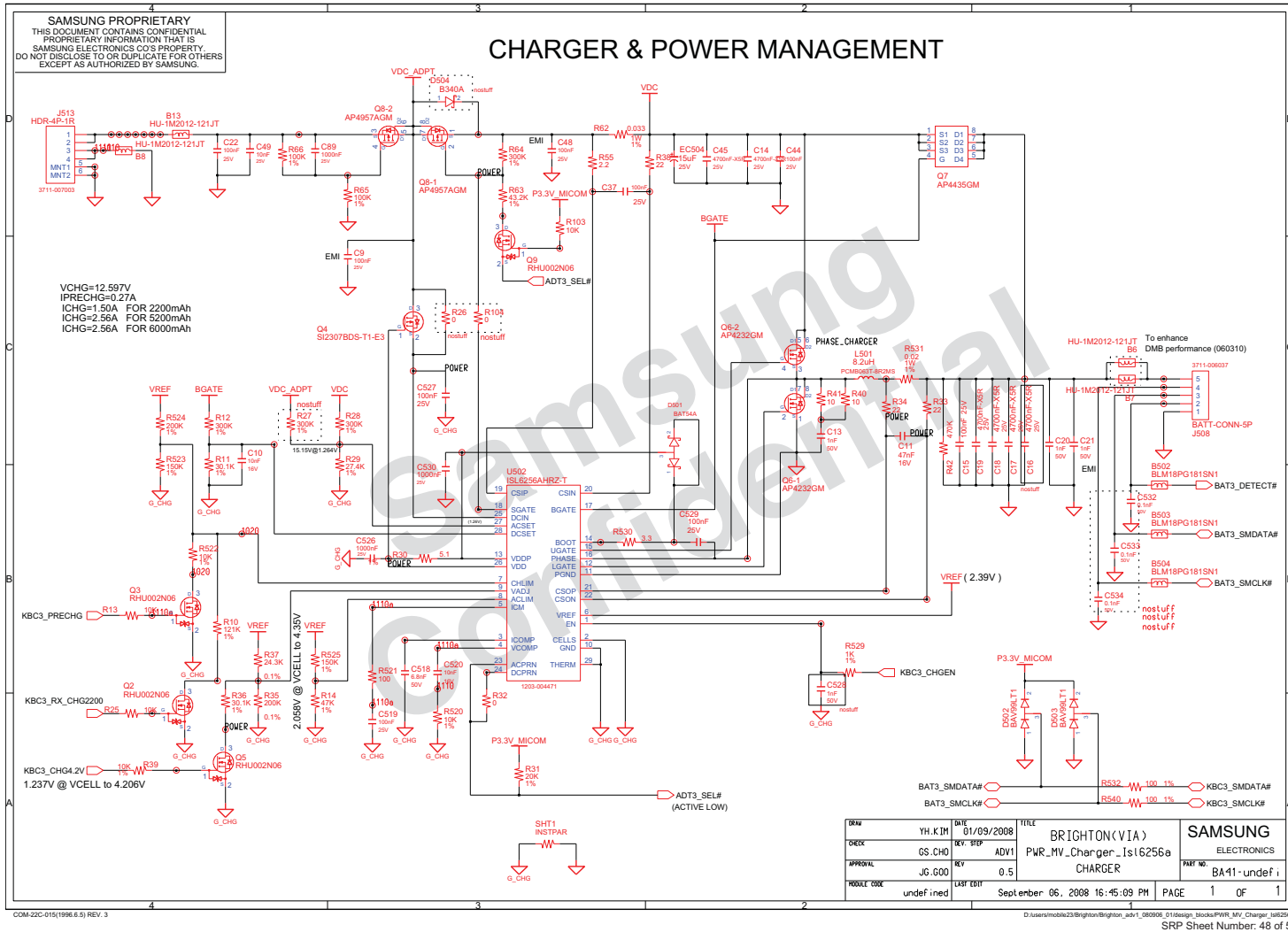
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