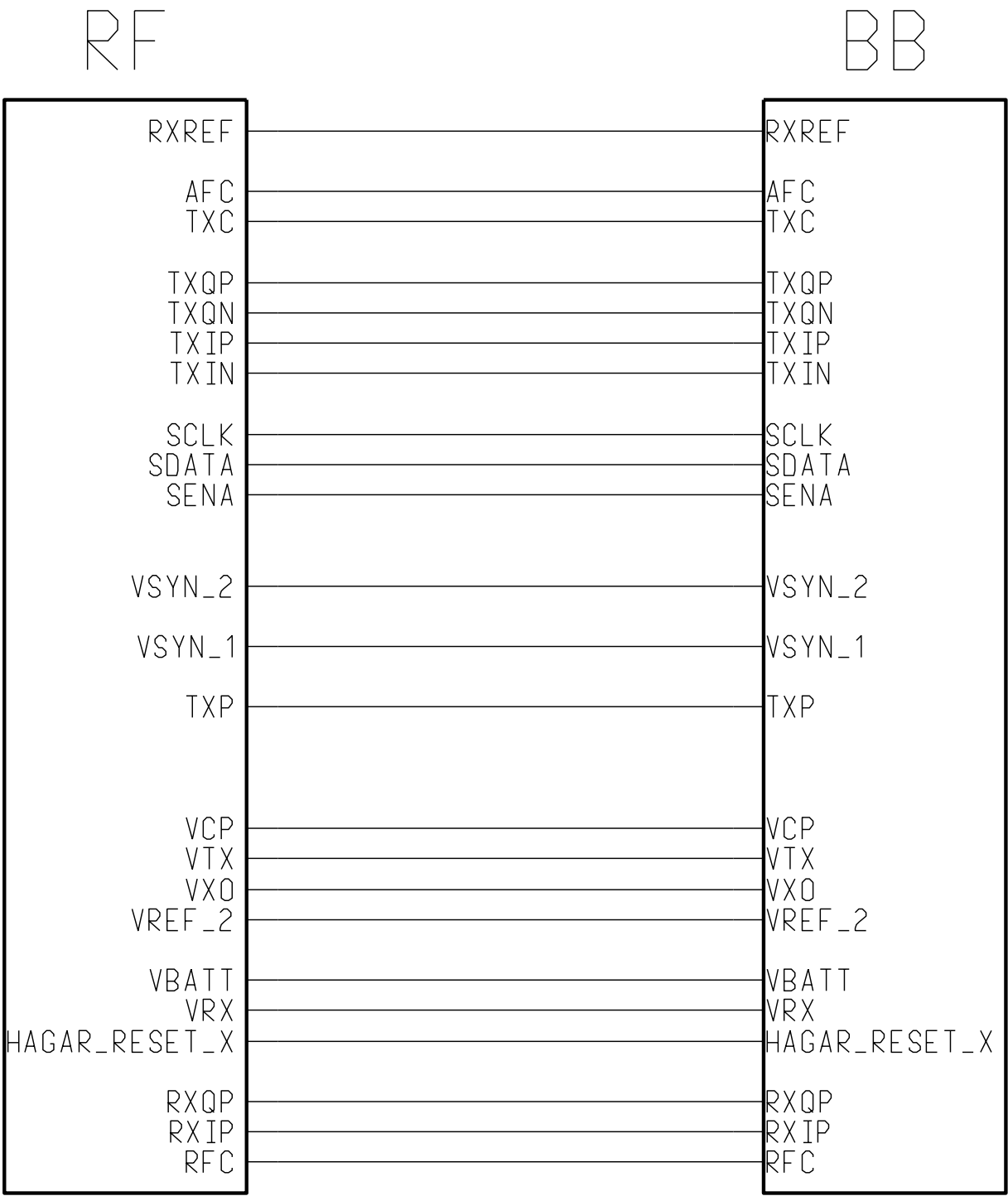
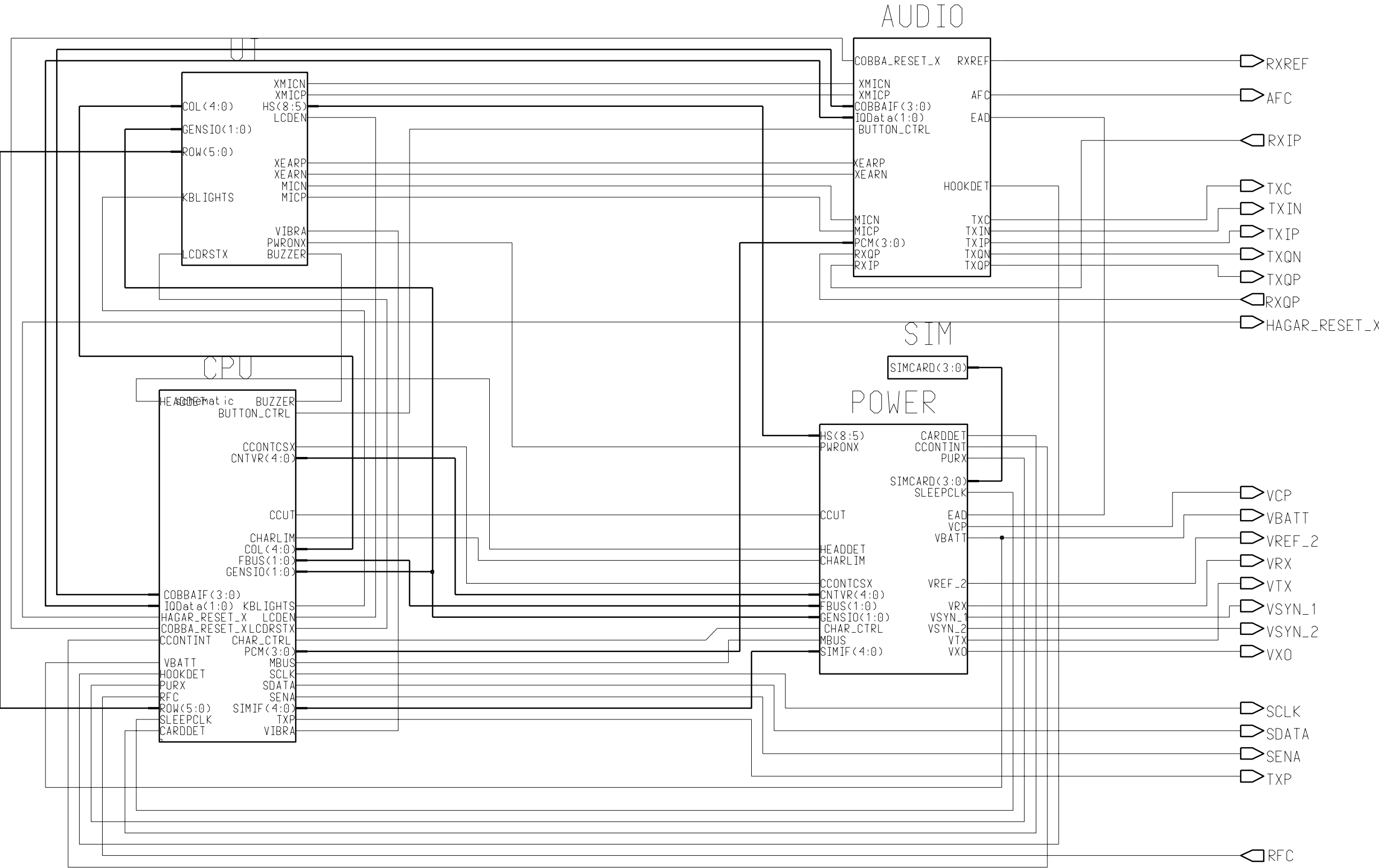


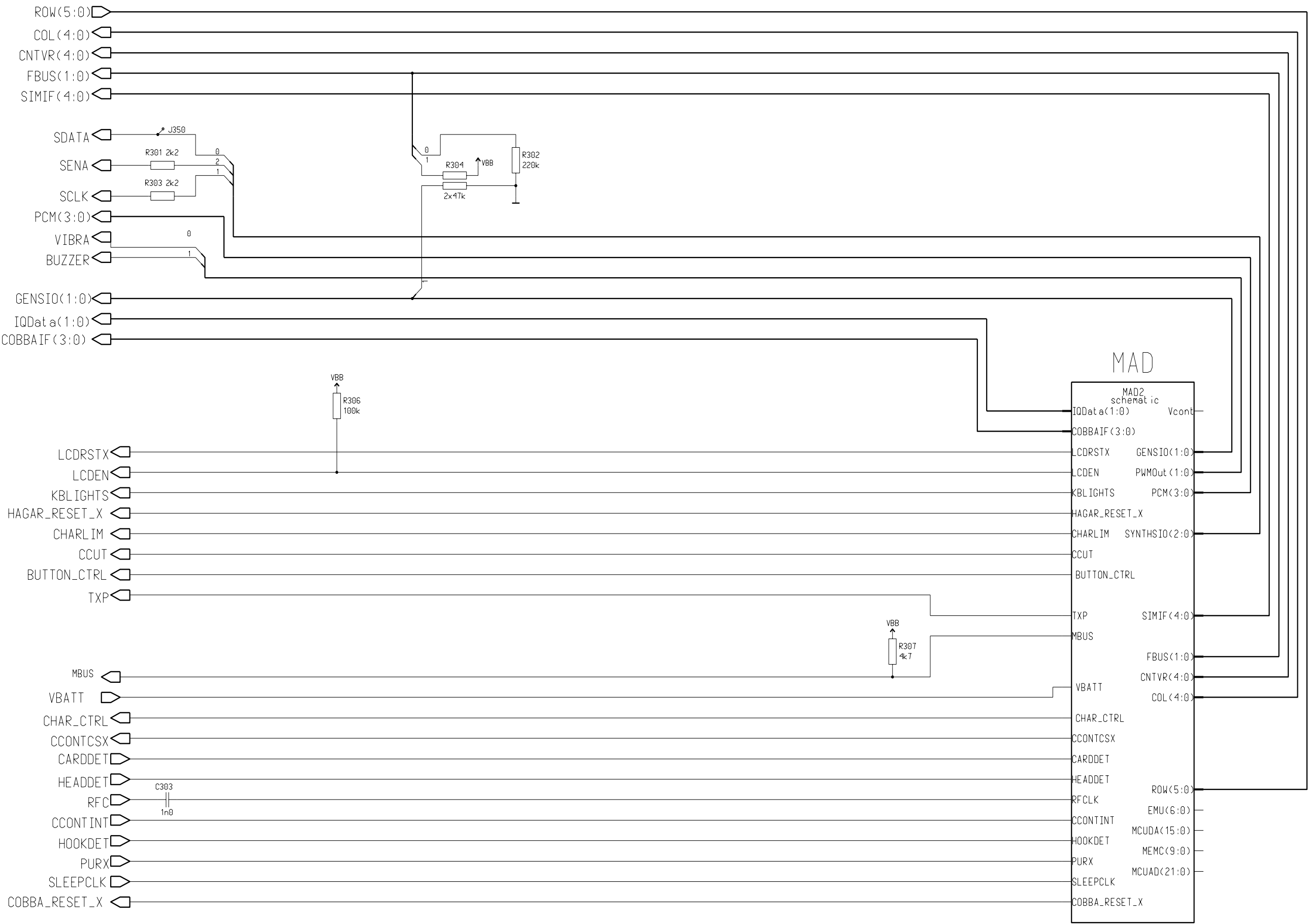
RF / Baseband Connections



Baseband Block



CPU



The diagram illustrates a complex PCB layout for a system featuring multiple MCUs and various peripheral components. The central component is the D300 (MAD2WD1_ROM5_V18_UBGA), which is connected to a series of MCUs (MCUAD(1) to MCUAD(21)). The layout includes several power management sections, including VCC, VDD, and VBAT rails, and various control signals like ROW, HEADDET, SLEEPCLK, and FBUS. The layout is organized into functional blocks with clear labeling for components and signals.

MCU Connections:

- MCUAD(1) to MCUAD(21) are connected to the D300 component.
- MCUAD(1) to MCUAD(21) are also connected to the D301 (GT28F160B3TA110) and D302 (K9F1016U4A-FF10T00) components.

Power Management:

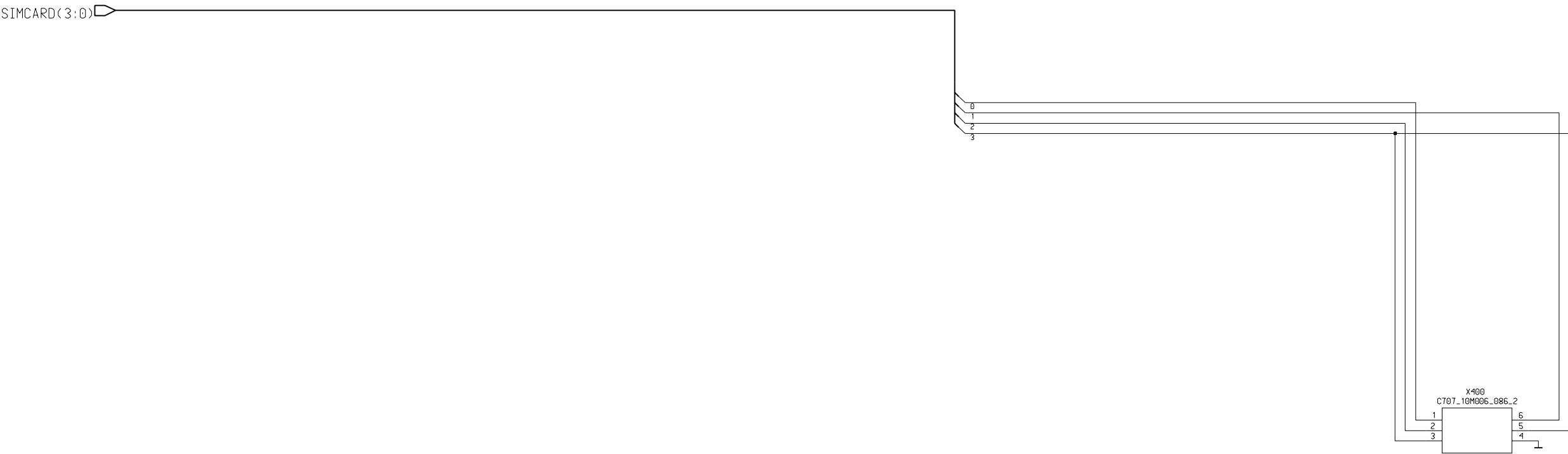
- VCC, VDD, and VBAT rails are shown with various capacitors (C301 to C318) for decoupling.
- Power management components include D303 (V1230BNC), D304 (MC33464N-30ATR), and D305 (MC33464N-30ATR).

Control Signals:

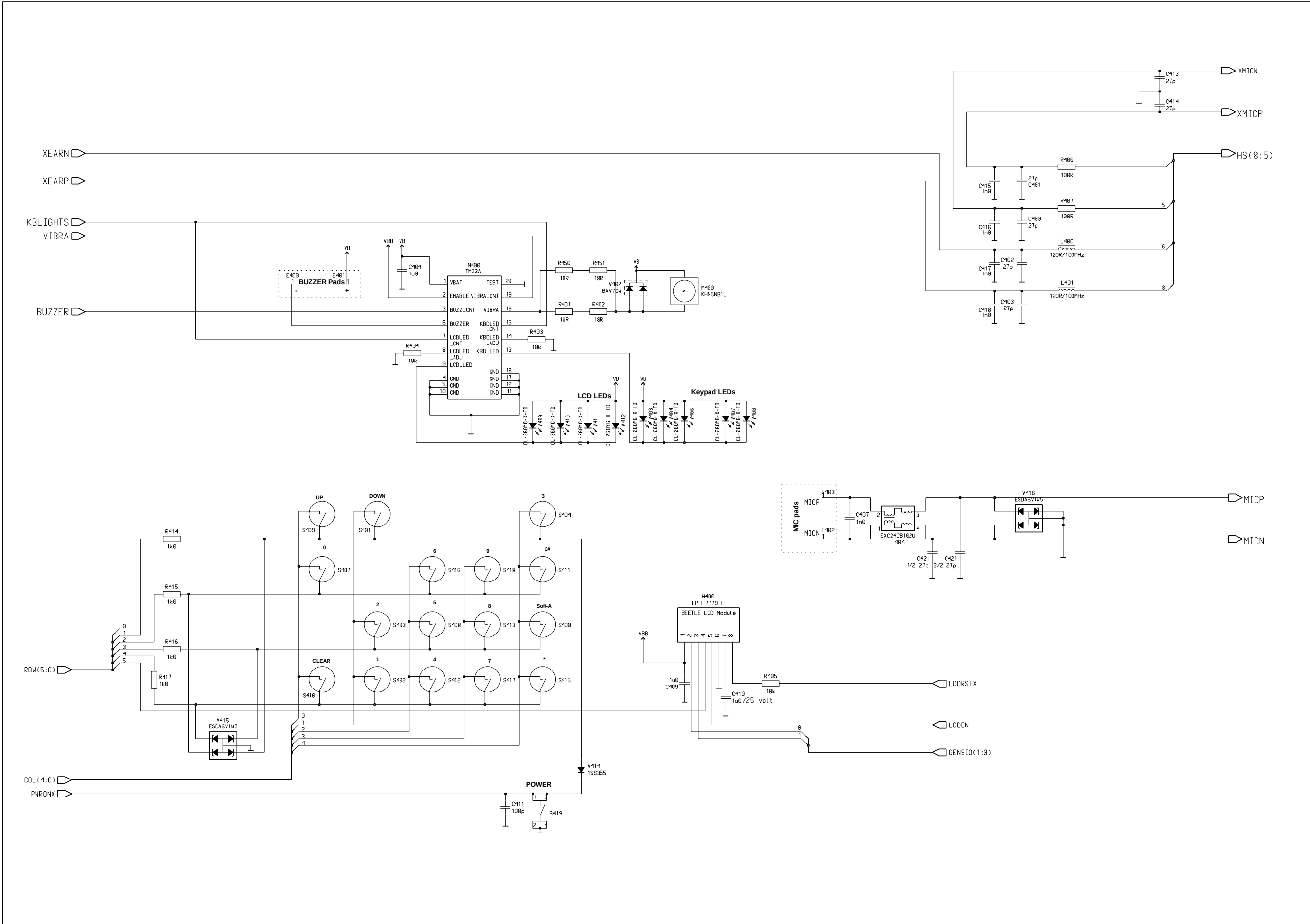
- ROW(5:0), HEADDET, SLEEPCLK, and FBUS(1:0) are control signals connected to the D300 component.
- Other control signals include CCUT, LCDSTX, CHARLIM, CARDDET, EMU(6:0), KBLIGHTS, and Vcont.

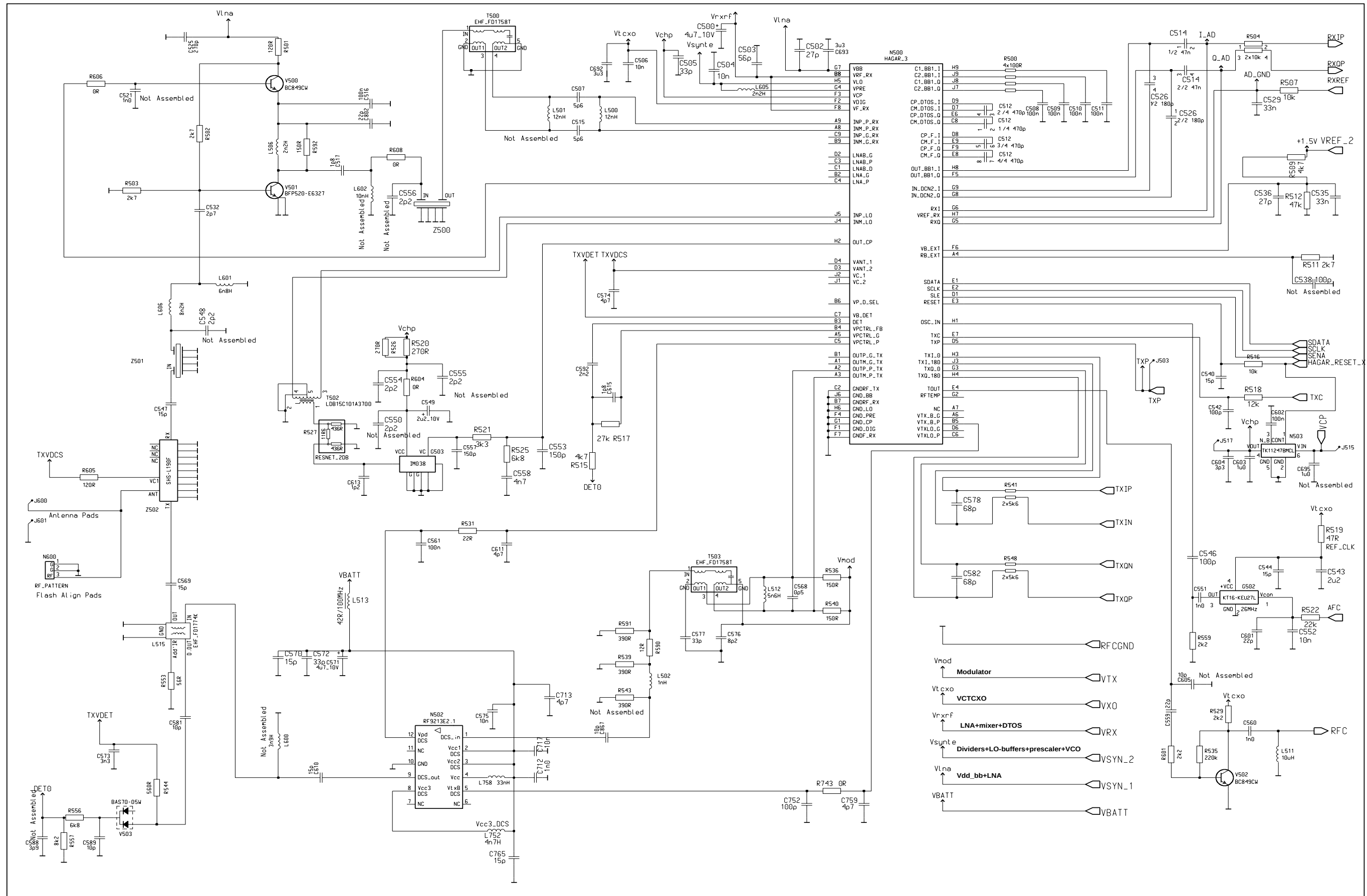
Other Components:

- D301 (GT28F160B3TA110) and D302 (K9F1016U4A-FF10T00) are memory components.
- D303 (V1230BNC), D304 (MC33464N-30ATR), and D305 (MC33464N-30ATR) are power management components.

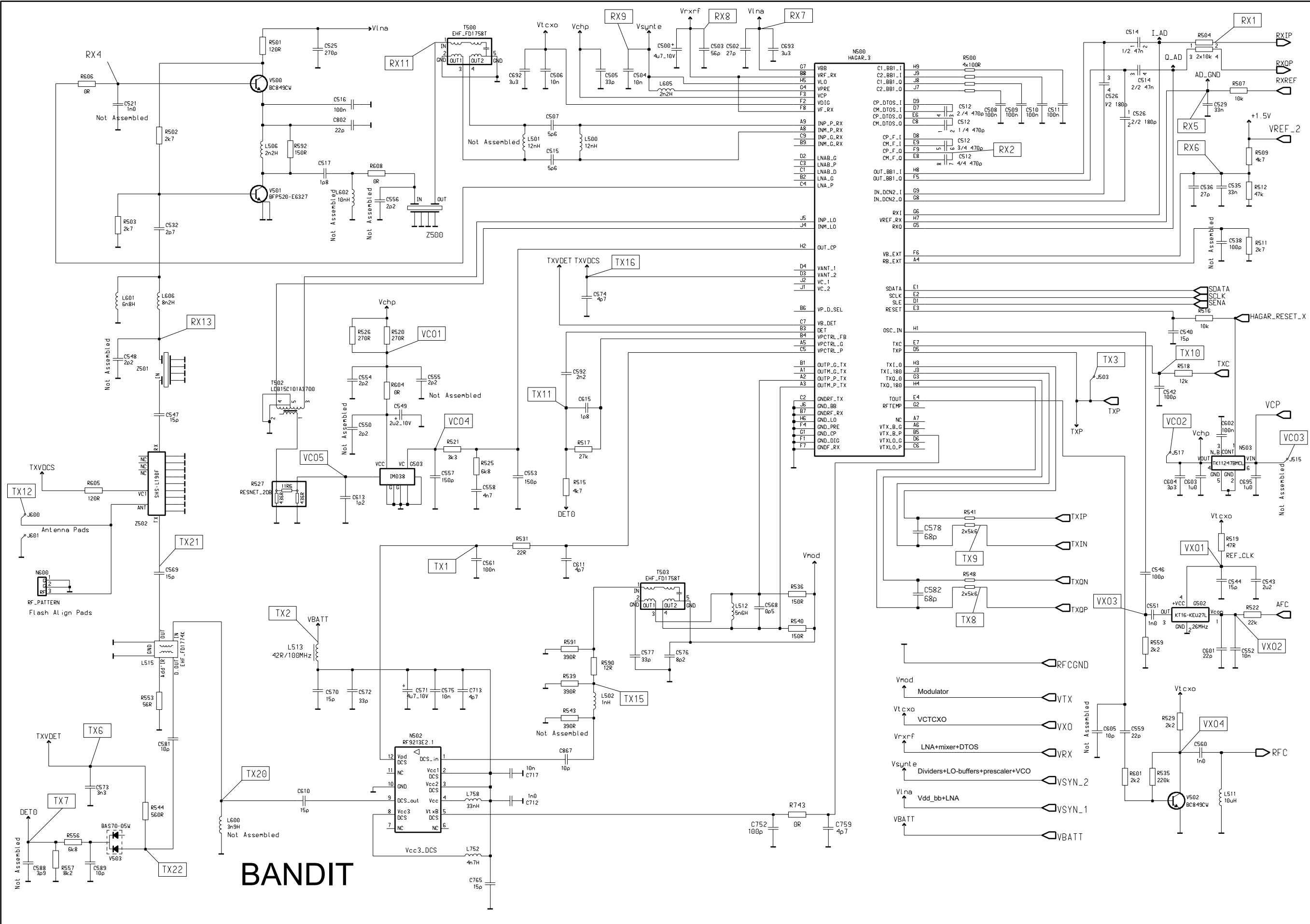


User Interface





RF Test Points



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