NBQAA

Bordeaux 10G

LA-6072P REV 1.0 Schematic

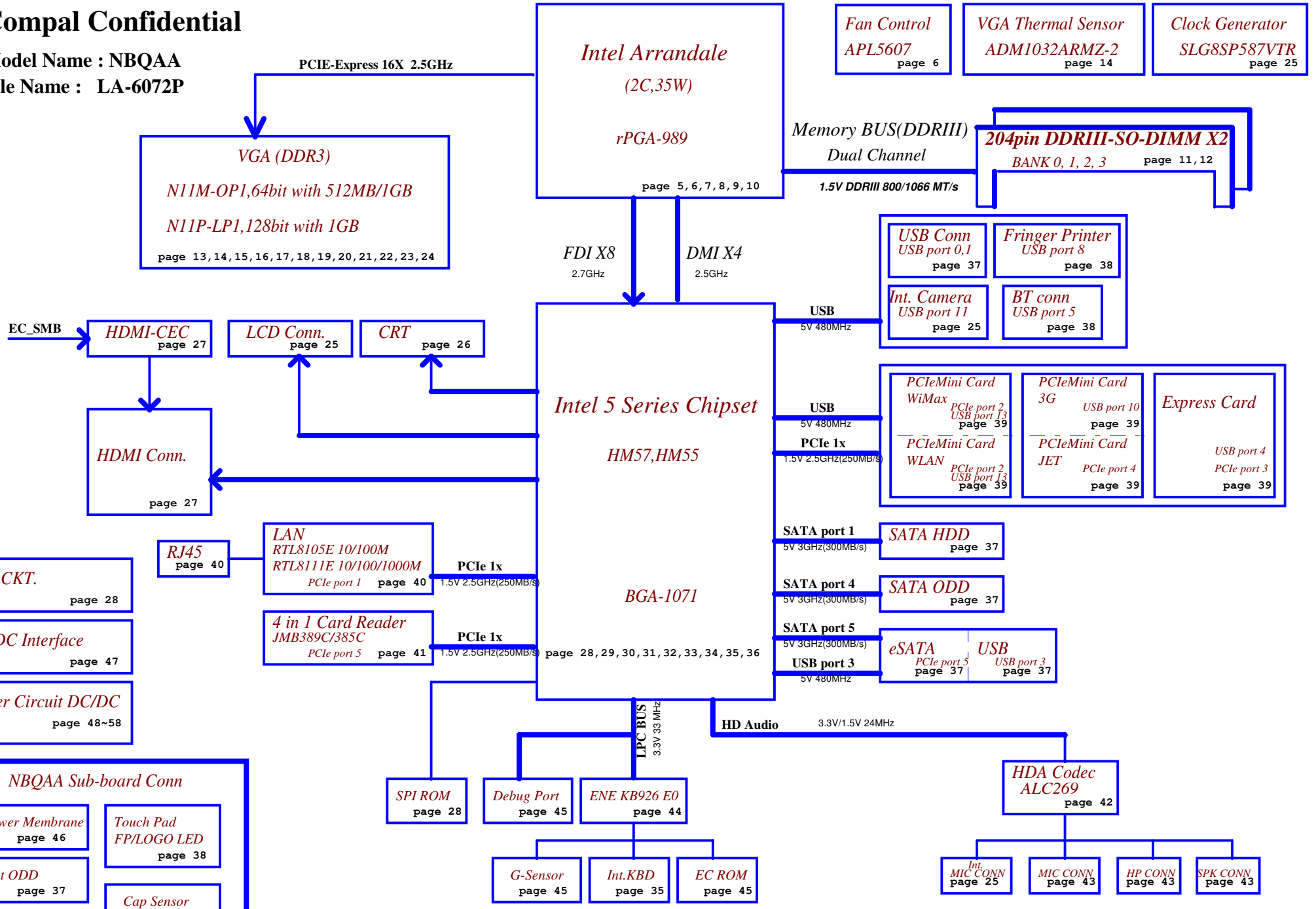
Intel Arrandale CPU / Intel 5 Series Chipset
2010-03-22 Rev 1.0

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.		
Title: Cover Page		
Size: B	Document Number: NBQAA LA6072P M/B	Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 1 of 61	

Compal Confidential

Model Name : NBQAA
File Name : LA-6072P



Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

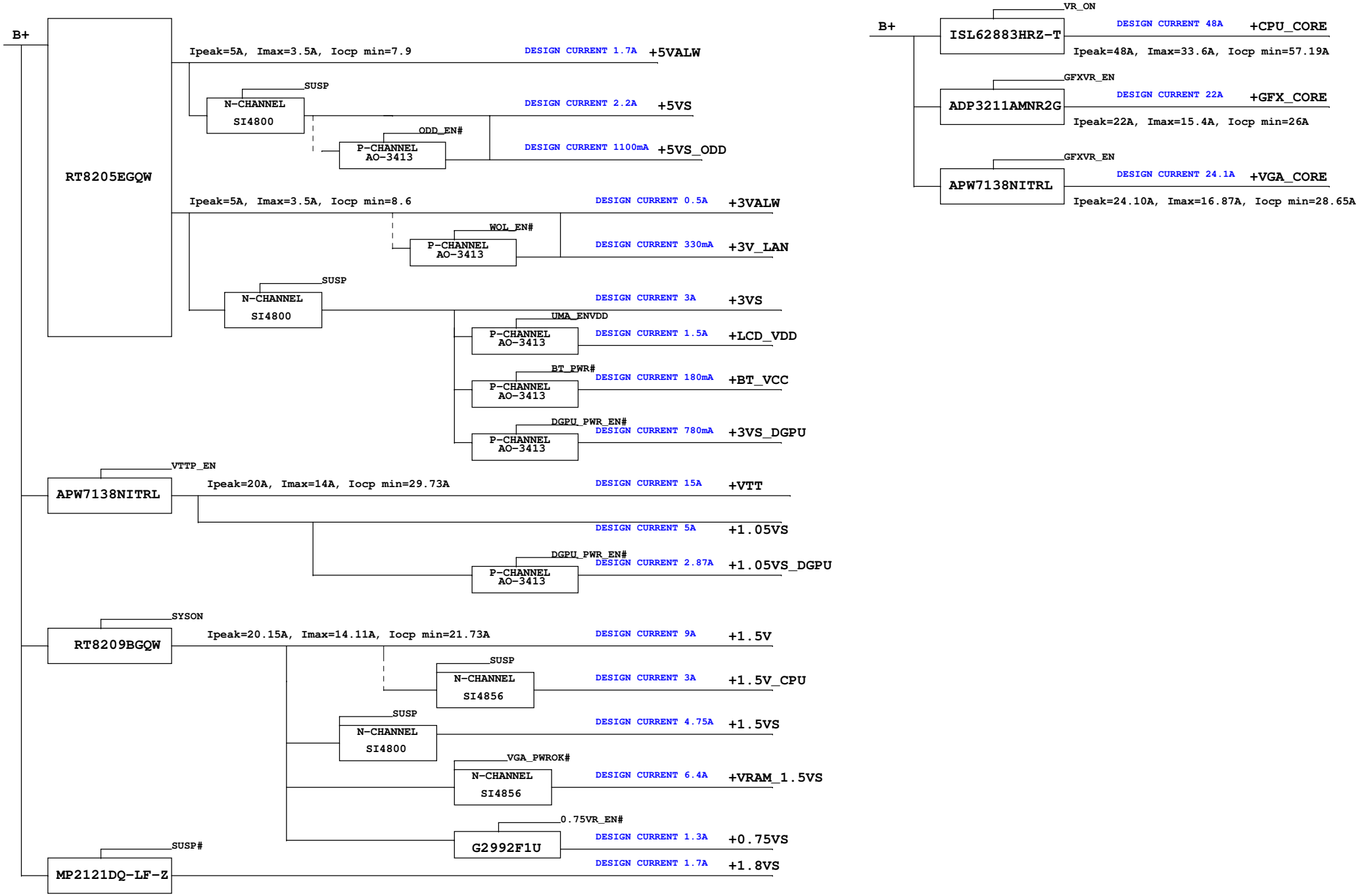
Compal Electronics, Inc.

Title: Block Diagrams

Size | Document Number: NBQAA LA6072P M/B | Rev: 1.0

Date: Tuesday, March 23, 2010 | Sheet 2 of 61

NBQAA Bordeaux Intel Arrandale (Discrete)



Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **Power Tree**

Size	Document Number	Rev
	NBQAA LA6072P M/B	1.0

Date: Monday, March 22, 2010 Sheet 3 of 61

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	+B	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

BTO Option Table

Function	Bluetooth	Card Reader		HDMI-CEC		LAN		CAM+MIC
description	B				Y	U	V	X
explain	Bluetooth	JMB389	JMB385	HDMI	HDMI+CEC	10/100	10/100/1000	CAM
BTO	BT@	JMB389@	JMB385@	IHDMI@	IHDMI@+CEC@	8105E@	8111E@	CAM@

Function	ODD		KB LED	Mini Card				GPU	
description		T	K	G	J		W	P	M
explain	Normal	Slot	KB LED	3G	JET	3G/JFT	WiMAX	N11P-LP1	N11M-OP1
BTO	ODD0@	ODD1@	KBL@	3G@	JET@	3GJFT@	WiMAX@	N11P@	N11P@

Function	PCH		VRAM	
description	H5	H7	512	1G
explain	HM55	HM57	512M	1G
BTO	HM55@	HM57@	4pcs@	4pcs@+8pcs@

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

EC SM Bus1 address

Power	Device	Address
+3VL	EC KB926 D3	
+3VL	HDMI-CEC	
+3VL	Smart Battery	0001 011x b

EC SM Bus2 address

Power	Device	Address
+3VS	EC KB926 D3	
+3VS	AMD GPU Thermal Sensor	
+3VS	Ambient Ligh Sensor	
+3VALW	PCH	
+3VS	G-Sensor	

PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b
+3VS	Express	
+3VS	Slot#1--WLAN/Wimax	
+3VS	Slot#2--JET/3G	

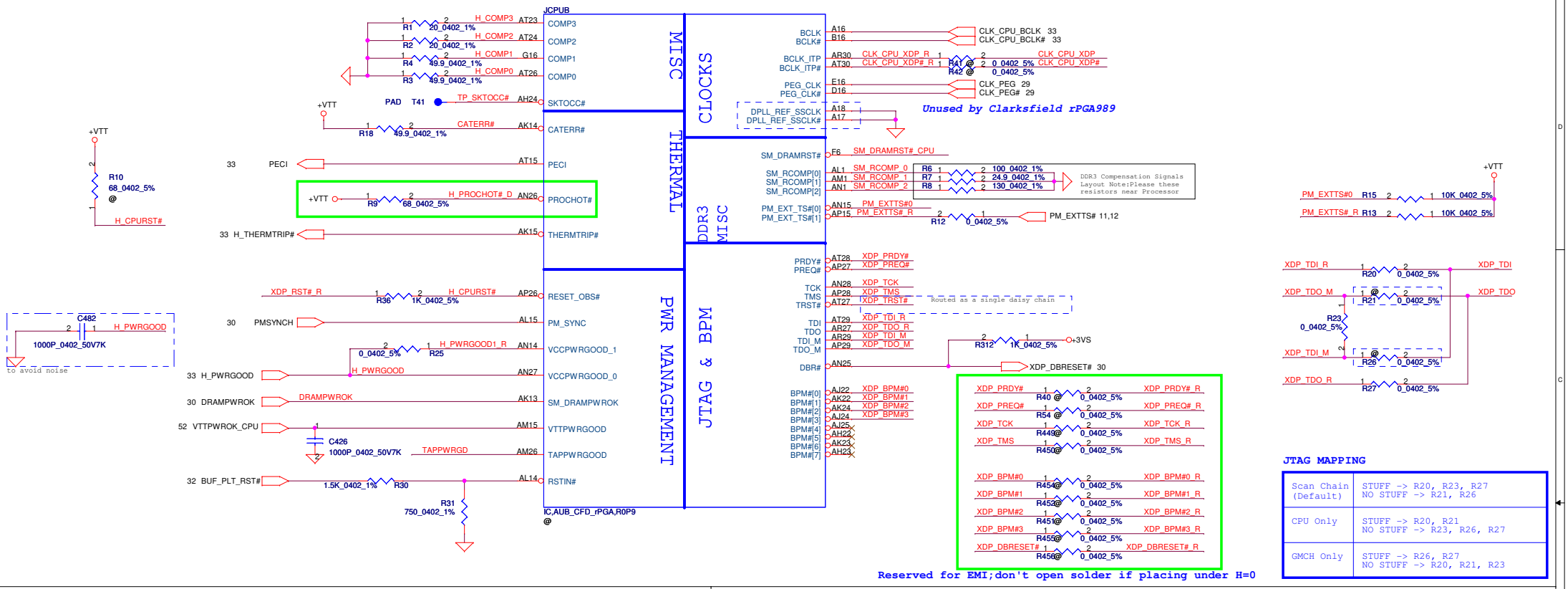
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

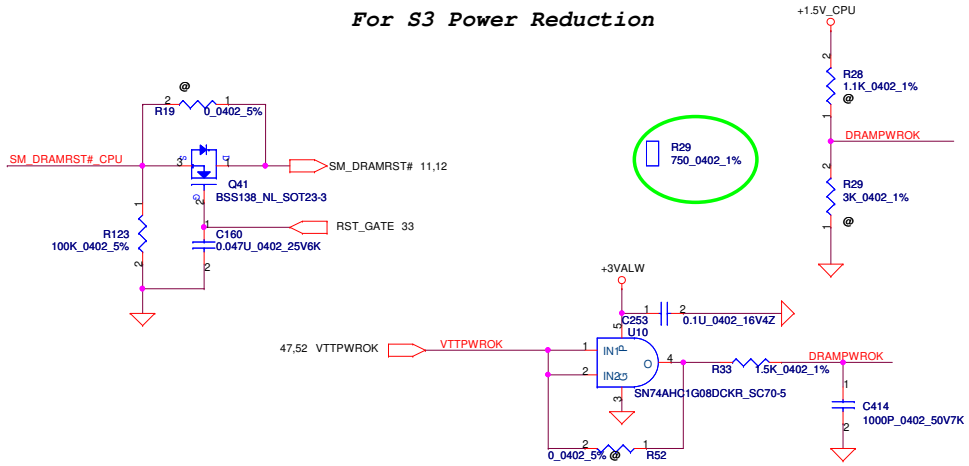
Title: Notes List

Size: Custom | Document Number: NBQAA LA6072P M/B | Rev: 1.0

Date: Tuesday, March 23, 2010 | Sheet 4 of 61

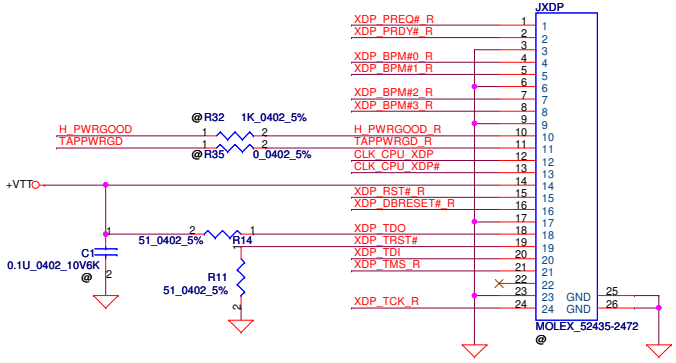


For S3 Power Reduction



XDP Connector

SFF-24Pin



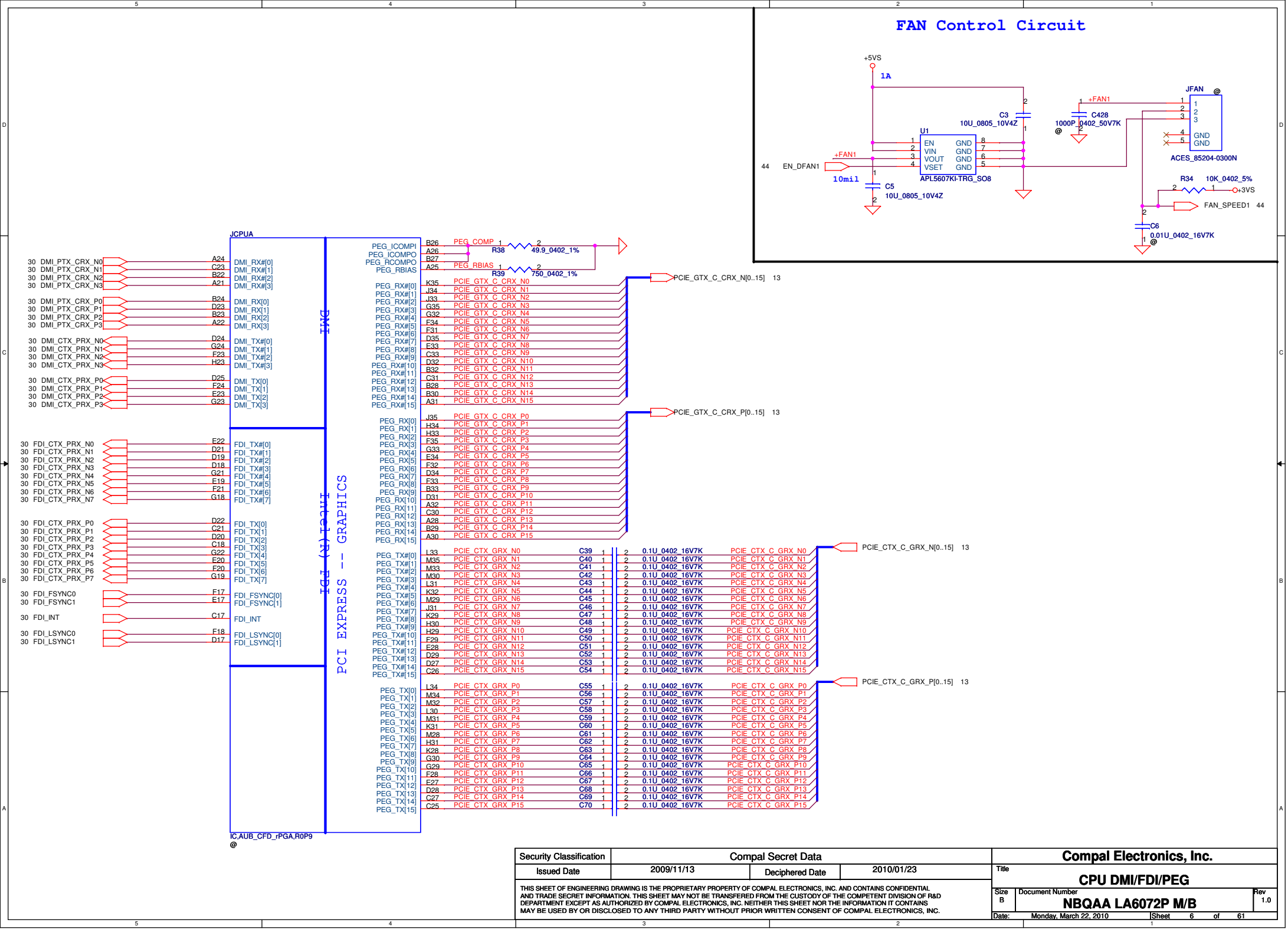
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **CPU CLK/MISC/JTAG**

Size	Document Number	Rev
Custom	NBQAA LA6072P M/B	1.0

Date: Tuesday, March 23, 2010 | Sheet 5 of 61



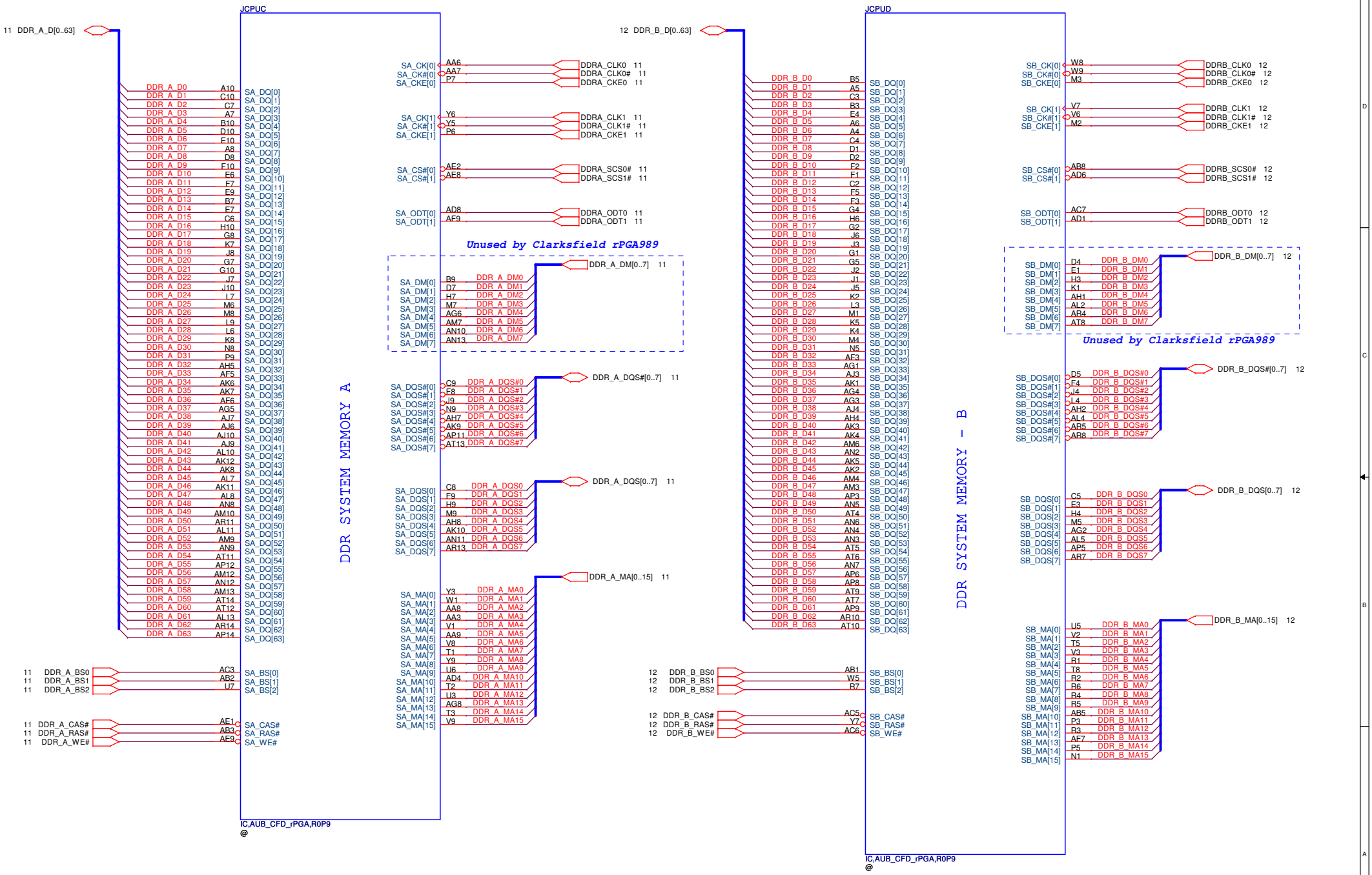
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **CPU DMI/FDI/PEG**

Size	Document Number	Rev
B	NBQAA LA6072P M/B	1.0

Date: Monday, March 22, 2010 Sheet 6 of 61



Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **CPU DDRIII**

Size	Document Number	Rev
B	NBQAA LA6072P M/B	1.0

Date: Monday, March 22, 2010 Sheet 7 of 61

Material Note (+VTT):
330uF/ 6mohm, number are 3,
power x1, HW x2

JCPUF

+CPU_CORE

Clarksfield: 65A
Auburndale:48A

Clarksfield: 21A
Auburndale:18A

(Place these capacitors under CPU socket Edge, top layer)

+VTT

C144 330U_2.5V_M_R17
C159 330U_2.5V_M_R17

SF000002Z00
H=4.5

C87 22U_0805_6.3V6M
C91 22U_0805_6.3V6M

C81 C83 C85 C89 C88 C90 C92 C94 10U_0805_10V4K

1.1V RAIL POWER

CPU CORE SUPPLY

Add on 2/8 to improve ESD

+CPU_CORE

0.1U_0402_16V4Z: C128 C127 C120 C118 C119 C117 C129

(Place these capacitors between inductor and socket on Bottom)

+CPU_CORE

10U_0805_10V4K: C71 C72 C73 C74 C75 C76 C77 C78 C79

(Place these capacitors under CPU socket, top layer)

+CPU_CORE

10U_0805_10V4K: C98 C99 C100 C101 C102 C103 C104

(Place these capacitors on CPU cavity, Bottom Layer)

+CPU_CORE

22U_0805_6.3V6M: C105 C106 C107 C108 C109 C110

+CPU_CORE

22U_0805_6.3V6M: C111 C112 C113 C114 C115 C116

TOP side (under inductor)

+CPU_CORE

SGA00002680

330U_D2_2.5VM_R9M: C121 C122 C123 C124

POWER

CPU VIDS

PSI# AN33 H_PSI# 56

VID[0] AK35 CPU_VID0 56
VID[1] AK33 CPU_VID1 56
VID[2] AK34 CPU_VID2 56
VID[3] AL35 CPU_VID3 56
VID[4] AL33 CPU_VID4 56
VID[5] AM33 CPU_VID5 56
VID[6] AM35 CPU_VID6 56

PROC_DPRSLPVR AM34 H_DPRSLPVR_R R62 0_0402_5% H_DPRSLPVR 56

VTT_SELECT G15 H_VTTSELECT T56 PAD

CRB default setting:
VID[6:0]=[0100111]

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

H_VTTSELECT = low, 1.1V
H_VTTSELECT = high, 1.05V

SENSE LINES

ISENSE AN35 IMVP_IMON 56

VCC_SENSE AJ34 VCCSENSE_R R65 0_0402_5%
VSS_SENSE AJ35 VSSSENSE_R R66 0_0402_5%

R64 100_0402_1% +CPU_CORE
VCCSENSE
VSSSENSE
VCCSENSE 56
VSSSENSE 56
R67 100_0402_1%

near CPU

VTT_SENSE B15 VTT_SENSE 52
VSS_SENSE_VTT A15 VSS_SENSE_VTT 52

Check list:

+CPU_CORE: 6x 470uF, 12x 22uF, 17x 10uF

+VTT: 4x 330uF, 7x 22uF, 8x 10uF

IC,AUB_CFD_rPGA,R0P9
@

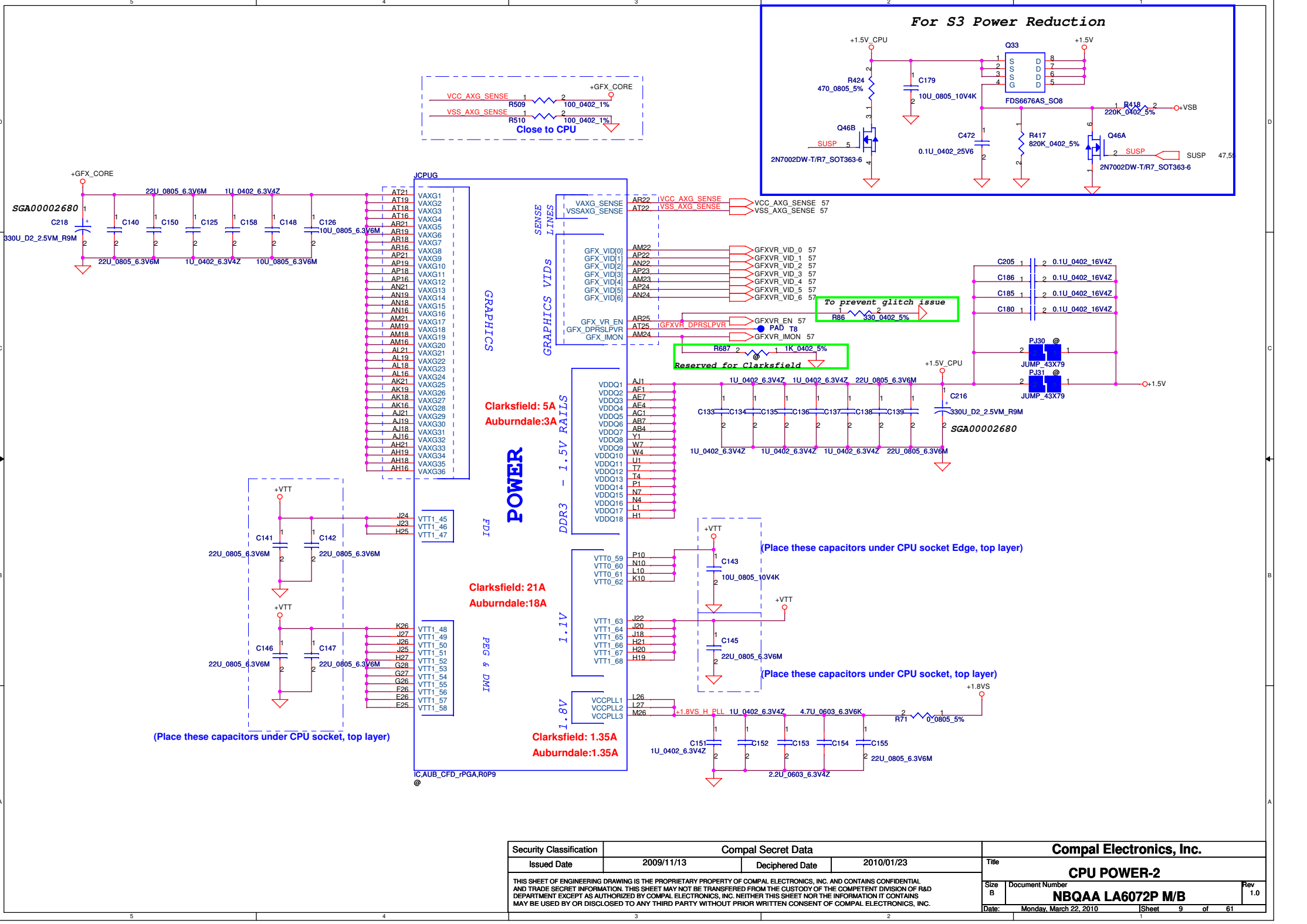
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **CPU POWER-1**

Size: Custom | Document Number: **NBQAA LA6072P M/B** | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 8 of 61



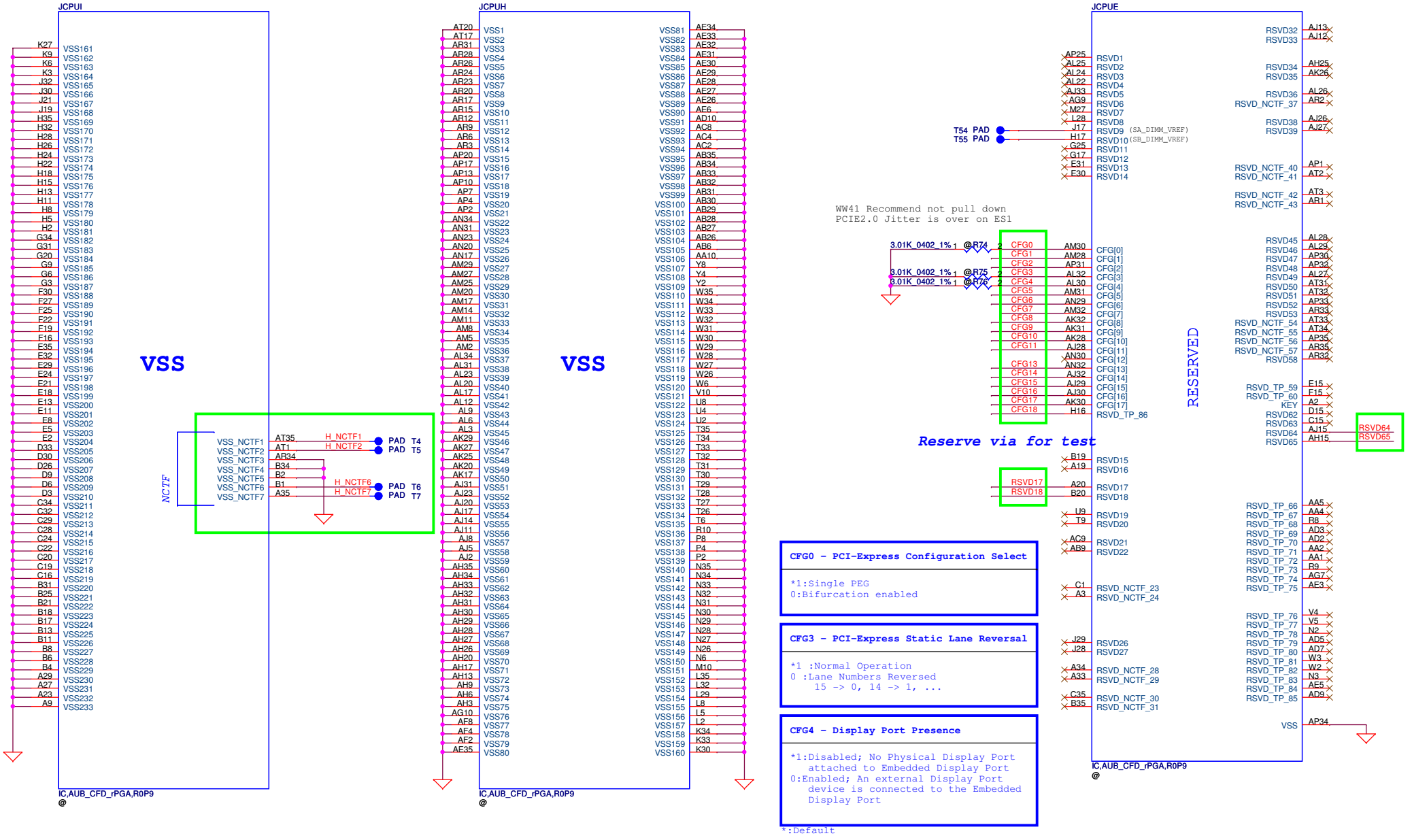
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **CPU POWER-2**

Size	Document Number	Rev
B	NBQAA LA6072P M/B	1.0

Date: Monday, March 22, 2010 Sheet 9 of 61



Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

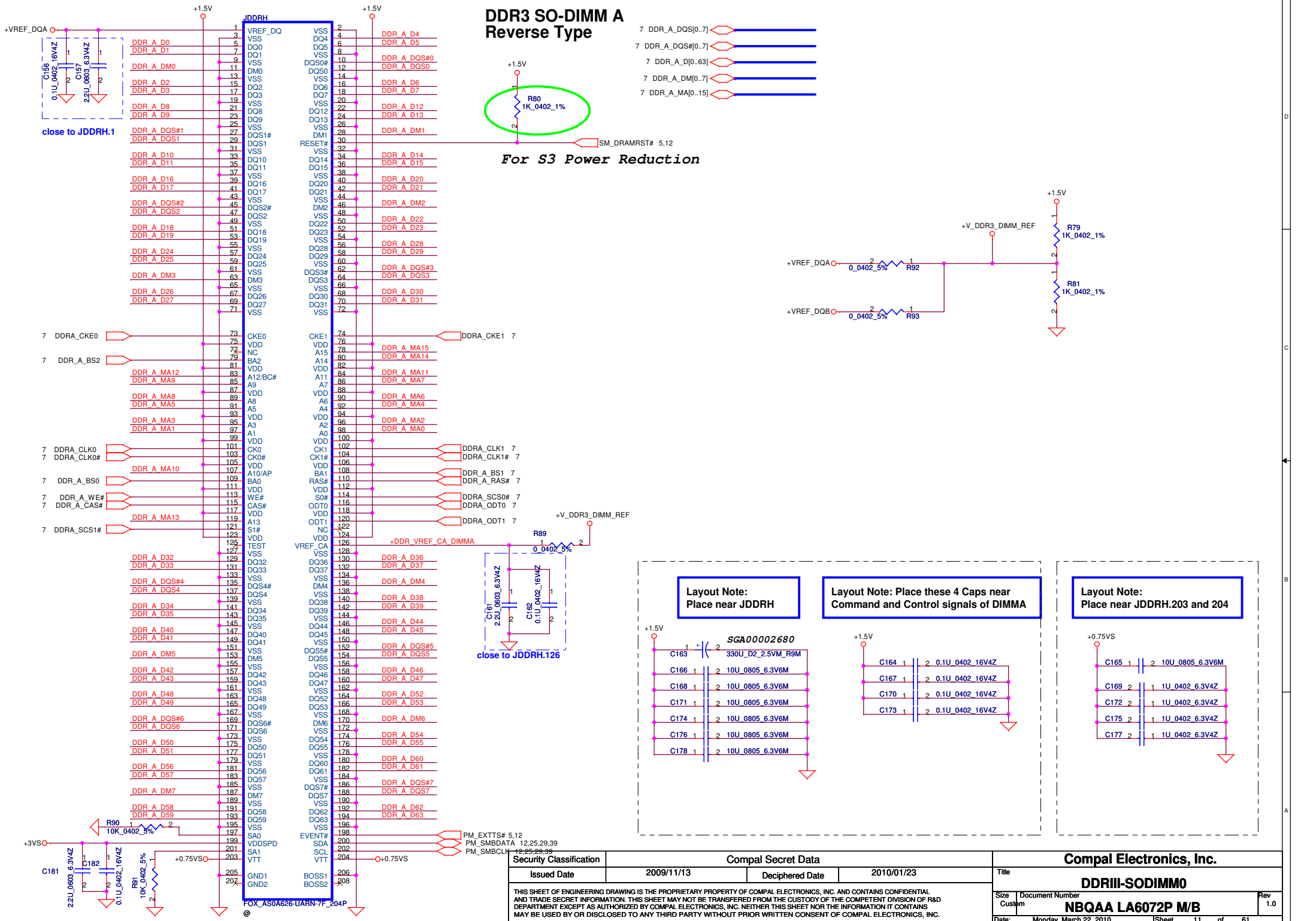
Compal Electronics, Inc.

Title: **CPU GND/RESERVED/XDP**

Size	Document Number	Rev
Custom	NBQAA LA6072P M/B	1.0

Date: Monday, March 22, 2010 Sheet 10 of 61

DDR3 SO-DIMM A
Reverse Type



Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **DDRIII-SODIMM0**

Size: Custom | Document Number: **NBQAA LA6072P M/B** | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 11 of 61

DDR3 SO-DIMM B
Reverse Type

JDDRL

+1.5V

+VREF_DQB

close to JDDRL.1

C183 2.2U_0603_6.3V4Z

C184 0.1U_0402_16V4Z

		1	VREF_DQ	VSS	2		
	DDR_B_D0	3	VSS	DQ4	4	DDR_B_D4	
	DDR_B_D1	5	DQ0	DQ5	6	DDR_B_D5	
		7	DQ1	VSS	8		
	DDR_B_DM0	9	VSS	DQS0#	10	DDR_B_DQS#0	
		11	DM0	DQS0	12	DDR_B_DQS0	
	DDR_B_D2	13	VSS	VSS	14		
	DDR_B_D3	15	DQ2	DQ6	16	DDR_B_D6	
		17	DQ3	DQ7	18	DDR_B_D7	
	DDR_B_D8	19	VSS	VSS	20		
	DDR_B_D9	21	DQ8	DQ12	22	DDR_B_D12	
		23	DQ9	DQ13	24	DDR_B_D13	
	DDR_B_DQS#1	25	VSS	VSS	26		
	DDR_B_DQS1	27	DQS1#	DM1	28	DDR_B_DM1	
		29	DQS1	RESET#	30	SM_DRAMRST# 5,11	
	DDR_B_D10	31	VSS	VSS	32		
	DDR_B_D11	33	DQ10	DQ14	34	DDR_B_D14	
		35	DQ11	DQ15	36	DDR_B_D15	
	DDR_B_D16	37	VSS	VSS	38		
	DDR_B_D17	39	DQ16	DQ20	40	DDR_B_D20	
		41	DQ17	DQ21	42	DDR_B_D21	
	DDR_B_DQS#2	43	VSS	VSS	44		
	DDR_B_DQS2	45	DQS2#	DM2	46	DDR_B_DM2	
		47	DQS2	VSS	48		
	DDR_B_D18	49	VSS	DQ22	50	DDR_B_D22	
	DDR_B_D19	51	DQ18	DQ23	52	DDR_B_D23	
		53	DQ19	VSS	54		
	DDR_B_D24	55	VSS	DQ28	56	DDR_B_D28	
	DDR_B_D25	57	DQ24	DQ29	58	DDR_B_D29	
		59	DQ25	VSS	60		
	DDR_B_DM3	61	VSS	DQS3#	62	DDR_B_DQS#3	
		63	DM3	DQS3	64	DDR_B_DQS3	
	DDR_B_D26	65	VSS	VSS	66		
	DDR_B_D27	67	DQ26	DQ30	68	DDR_B_D30	
		69	DQ27	DQ31	70	DDR_B_D31	
		71	VSS	VSS	72		
7 DDRB_CKE0		73	CKE0	CKE1	74	DDRB_CKE1 7	
		75	VDD	VDD	76		
		77	NC	A15	78	DDR_B_MA15	
7 DDR_B_BS2		79	BA2	A14	80	DDR_B_MA14	
		81	VDD	VDD	82		
	DDR_B_MA12	83	A12/BC#	A11	84	DDR_B_MA11	
	DDR_B_MA9	85	A9	A7	86	DDR_B_MA7	
		87	VDD	VDD	88		
	DDR_B_MA8	89	A8	A6	90	DDR_B_MA6	
	DDR_B_MA5	91	A5	A4	92	DDR_B_MA4	
		93	VDD	VDD	94		
	DDR_B_MA3	95	A3	A2	96	DDR_B_MA2	
	DDR_B_MA1	97	A1	A0	98	DDR_B_MA0	
		99	VDD	VDD	100		
7 DDRB_CLK0		101	CK0	CK1	102	DDRB_CLK1 7	
7 DDRB_CLK0#		103	CK0#	CK1#	104	DDRB_CLK1# 7	
		105	VDD	VDD	106		
	DDR_B_MA10	107	A10/AP	BA1	108	DDR_B_BS1 7	
7 DDR_B_BS0		109	BA0	RAS#	110	DDR_B_RAS# 7	
		111	VDD	VDD	112		
7 DDR_B_WE#		113	WE#	S0#	114	DDRB_SCS0# 7	
7 DDR_B_CAS#		115	CAS#	ODT0	116	DDRB_ODT0 7	
		117	VDD	VDD	118		
	DDR_B_MA13	119	A13	ODT1	120	DDRB_ODT1 7	
7 DDRB_SCS1#		121	S1#	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREF_CA	126	+DDR_VREF_CA_DIMMB	
		127	VSS	VSS	128		
	DDR_B_D32	129	DQ32	DQ36	130	DDR_B_D36	
	DDR_B_D33	131	DQ33	DQ37	132	DDR_B_D37	
		133	VSS	VSS	134		
	DDR_B_DQS#4	135	DQS4#	DM4	136	DDR_B_DM4	
	DDR_B_DQS4	137	DQS4	VSS	138		
		139	VSS	DQ38	140	DDR_B_D38	
	DDR_B_D34	141	DQ34	DQ39	142	DDR_B_D39	
	DDR_B_D35	143	DQ35	VSS	144		
		145	VSS	DQ44	146	DDR_B_D44	
	DDR_B_D40	147	DQ40	DQ45	148	DDR_B_D45	
	DDR_B_D41	149	DQ41	VSS	150		
		151	VSS	DQS5#	152	DDR_B_DQS#5	
	DDR_B_DM5	153	DM5	DQS5	154	DDR_B_DQS5	
		155	VSS	VSS	156		
	DDR_B_D42	157	DQ42	DQ46	158	DDR_B_D46	
	DDR_B_D43	159	DQ43	DQ47	160	DDR_B_D47	
		161	VSS	VSS	162		
	DDR_B_D48	163	DQ48	DQ52	164	DDR_B_D52	
	DDR_B_D49	165	DQ49	DQ53	166	DDR_B_D53	
		167	VSS	VSS	168		
	DDR_B_DQS#6	169	DQS6#	DM6	170	DDR_B_DM6	
	DDR_B_DQS6	171	DQS6	VSS	172		
		173	VSS	DQ54	174	DDR_B_D54	
	DDR_B_D50	175	DQ50	DQ55	176	DDR_B_D55	
	DDR_B_D51	177	DQ51	VSS	178		
		179	VSS	DQ60	180	DDR_B_D60	
	DDR_B_D56	181	DQ56	DQ61	182	DDR_B_D61	
	DDR_B_D57	183	DQ57	VSS	184		
		185	VSS	DQS7#	186	DDR_B_DQS#7	
	DDR_B_DM7	187	DM7	DQS7	188	DDR_B_DQS7	
		189	VSS	VSS	190		
	DDR_B_D58	191	DQ58	DQ62	192	DDR_B_D62	
	DDR_B_D59	193	DQ59	DQ63	194	DDR_B_D63	
		195	VSS	VSS	196		
		197	SA0	EVENT#	198	PM_EXTTS# 5,11	
		199	VDDSPD	SDA	200	PM_SMBDATA 11,25,29,39	
		201	SA1	SCL	202	PM_SMBCLK 11,25,29,39	
		203	VTT	VTT	204	+0.75VS	
		205	GND1	BOSS1	206		
		207	GND2	BOSS2	208		

FOX_AS0A626-U2RN-7F_204P

@

R98 10K_0402_5%

R99 10K_0402_5%

+3VS

+0.75VS

2.2U_0603_6.3V4Z

C207

C208

0.1U_0402_16V4Z

R97 0_0402_5%

+V_DDR3_DIMM_REF

close to JDDRL.126

C187 2.2U_0603_6.3V4Z

C188 0.1U_0402_16V4Z

7 DDR_B_DQS#[0..7]

7 DDR_B_DQS[0..7]

7 DDR_B_D[0..63]

7 DDR_B_DM[0..7]

7 DDR_B_MA[0..15]

Layout Note:
Place near JDDRL

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB

Layout Note:
Place near JDDRL.203 and 204

+1.5V

C189 @ 330U_B2_2.5VM_R15M

C192 10U_0805_6.3V6M

C194 10U_0805_6.3V6M

C197 10U_0805_6.3V6M

C200 10U_0805_6.3V6M

C202 10U_0805_6.3V6M

C204 10U_0805_6.3V6M

+1.5V

C190 0.1U_0402_16V4Z

C193 0.1U_0402_16V4Z

C196 0.1U_0402_16V4Z

C199 0.1U_0402_16V4Z

+0.75VS

C191 10U_0805_6.3V6M

C195 1U_0402_6.3V4Z

C198 1U_0402_6.3V4Z

C201 1U_0402_6.3V4Z

C203 1U_0402_6.3V4Z

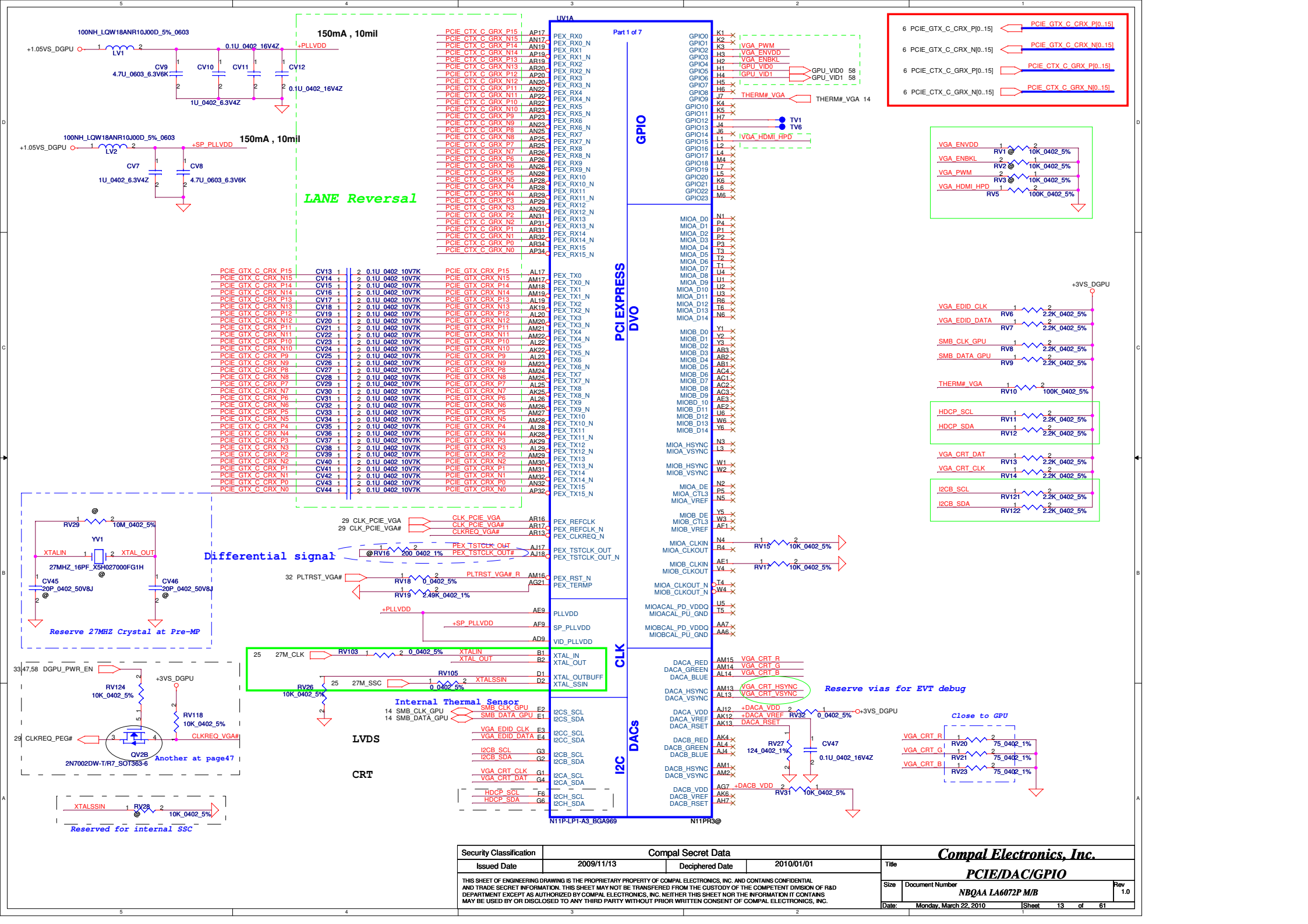
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **DDRIII-SODIMM1**

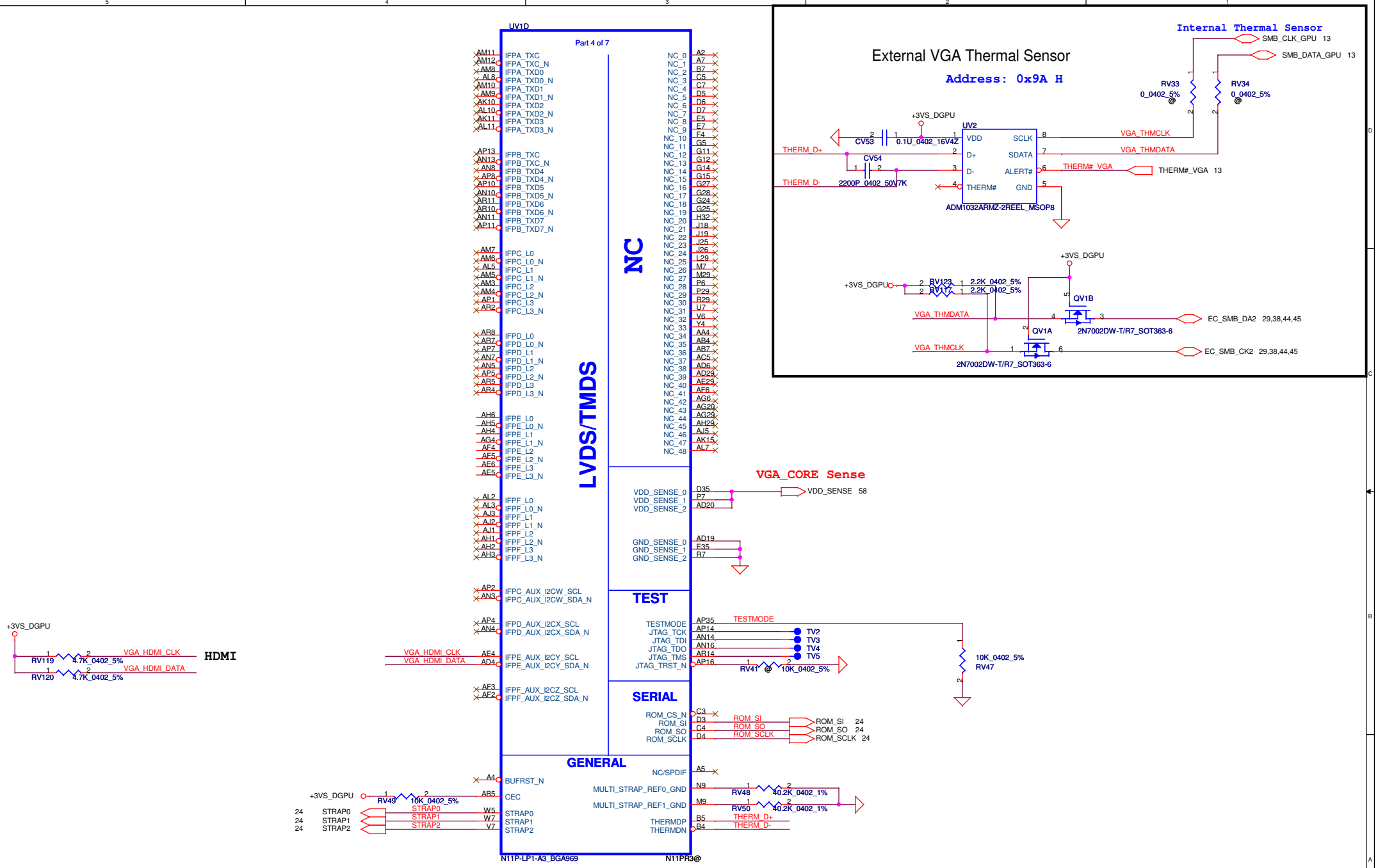
Size: Custom | Document Number: **NBQAA LA6072P M/B** | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 12 of 61



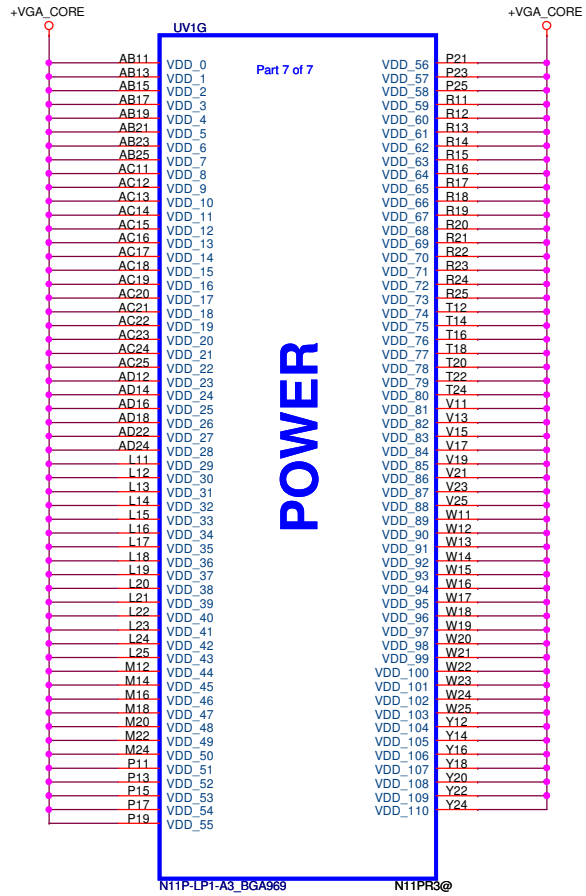
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/01

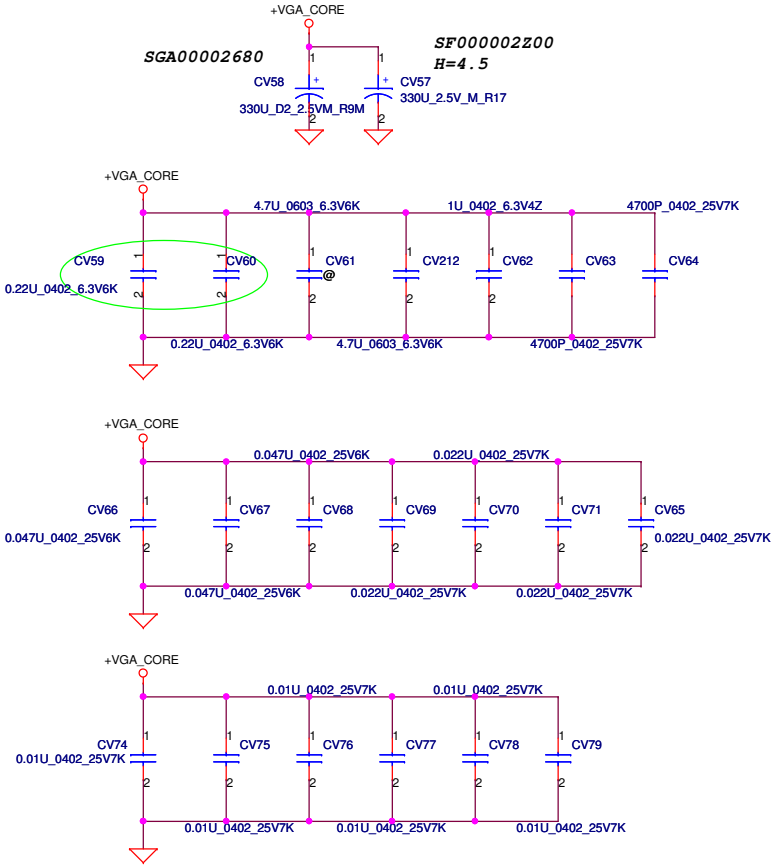
Compal Electronics, Inc.			
Title: PCIE/DAC/GPIO			
Size	Document Number: NBQAA LA6072P M/B		Rev: 1.0
Date: Monday, March 22, 2010	Sheet 13 of 61		



Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/01

Compal Electronics, Inc.			
Title: LVDS/HDMI/DP/THM			
Size	Document Number: NBQAA LA6072P M/B		Rev: 1.0
Date: Monday, March 22, 2010	Sheet 14 of 61		





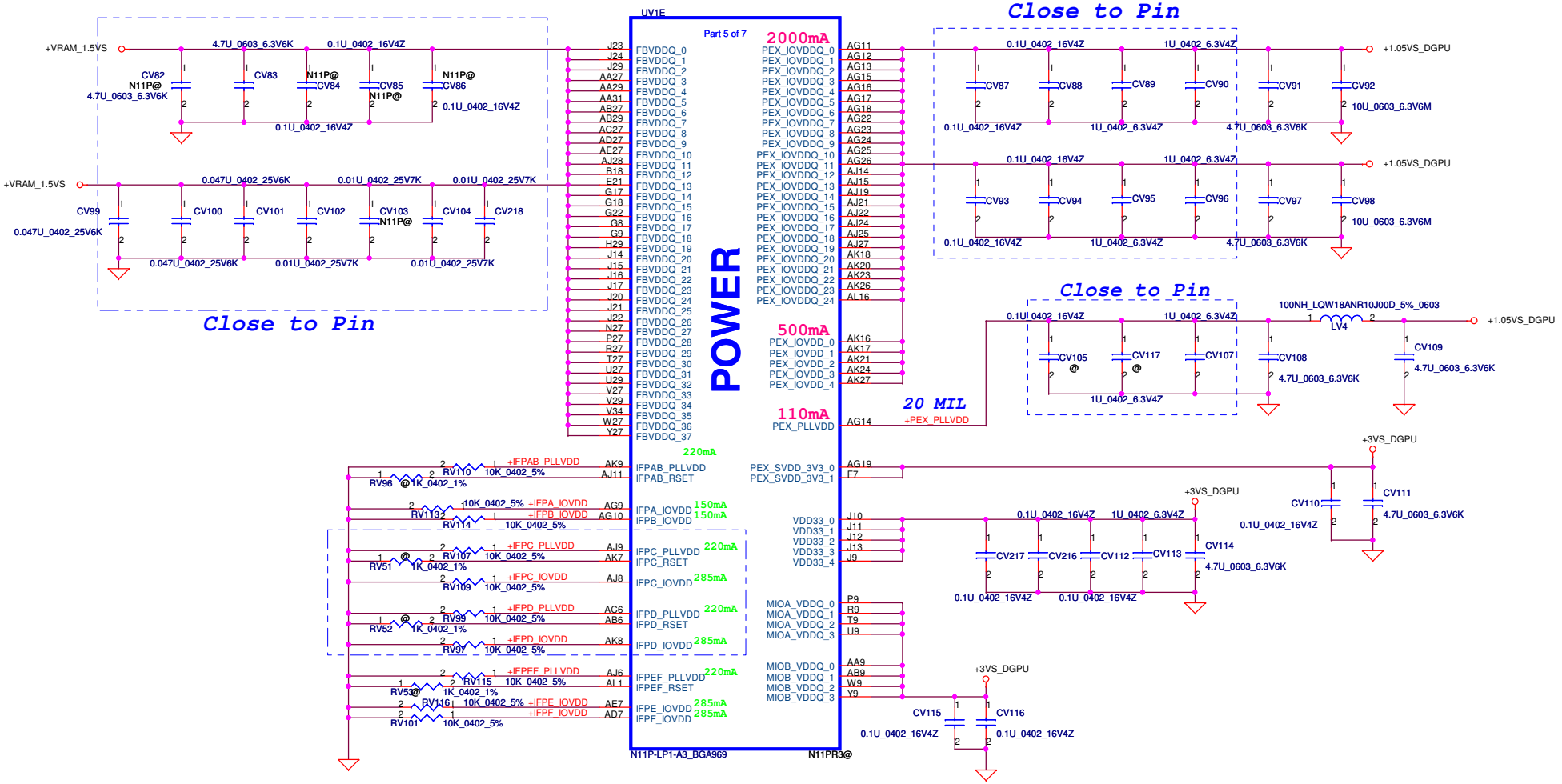
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: **VGA CORE**

Size	Document Number	Rev
	NBQAA LA6072P M/B	1.0

Date: Monday, March 22, 2010 | Sheet 15 of 61



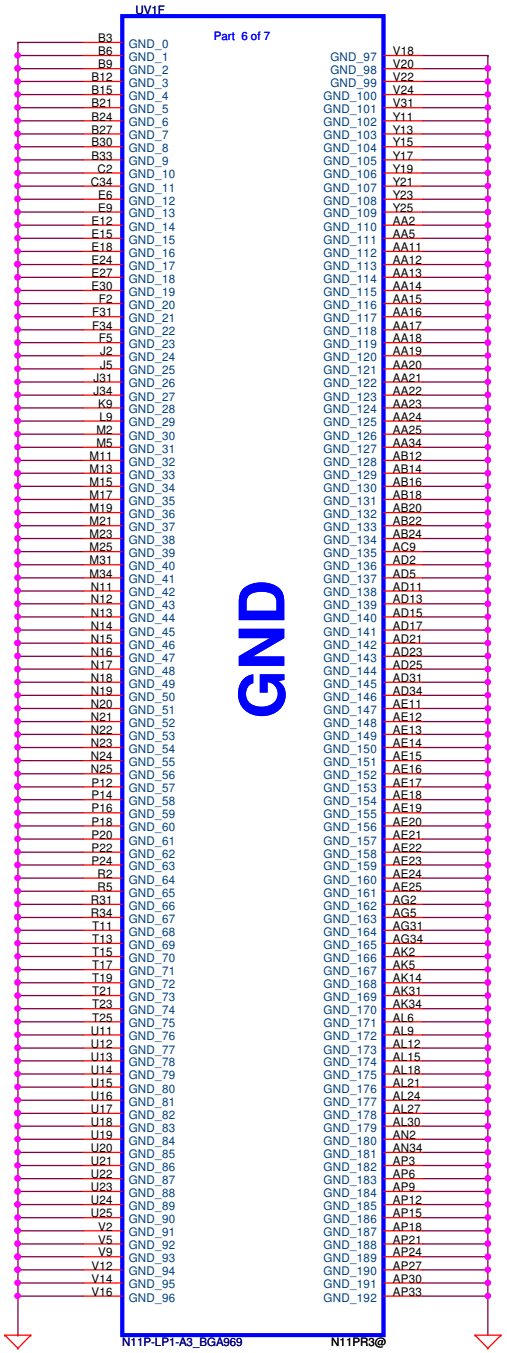
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: **POWER**

Size	Document Number	Rev
	NBQAA LA6072P M/B	1.0

Date: Monday, March 22, 2010 | Sheet 16 of 61



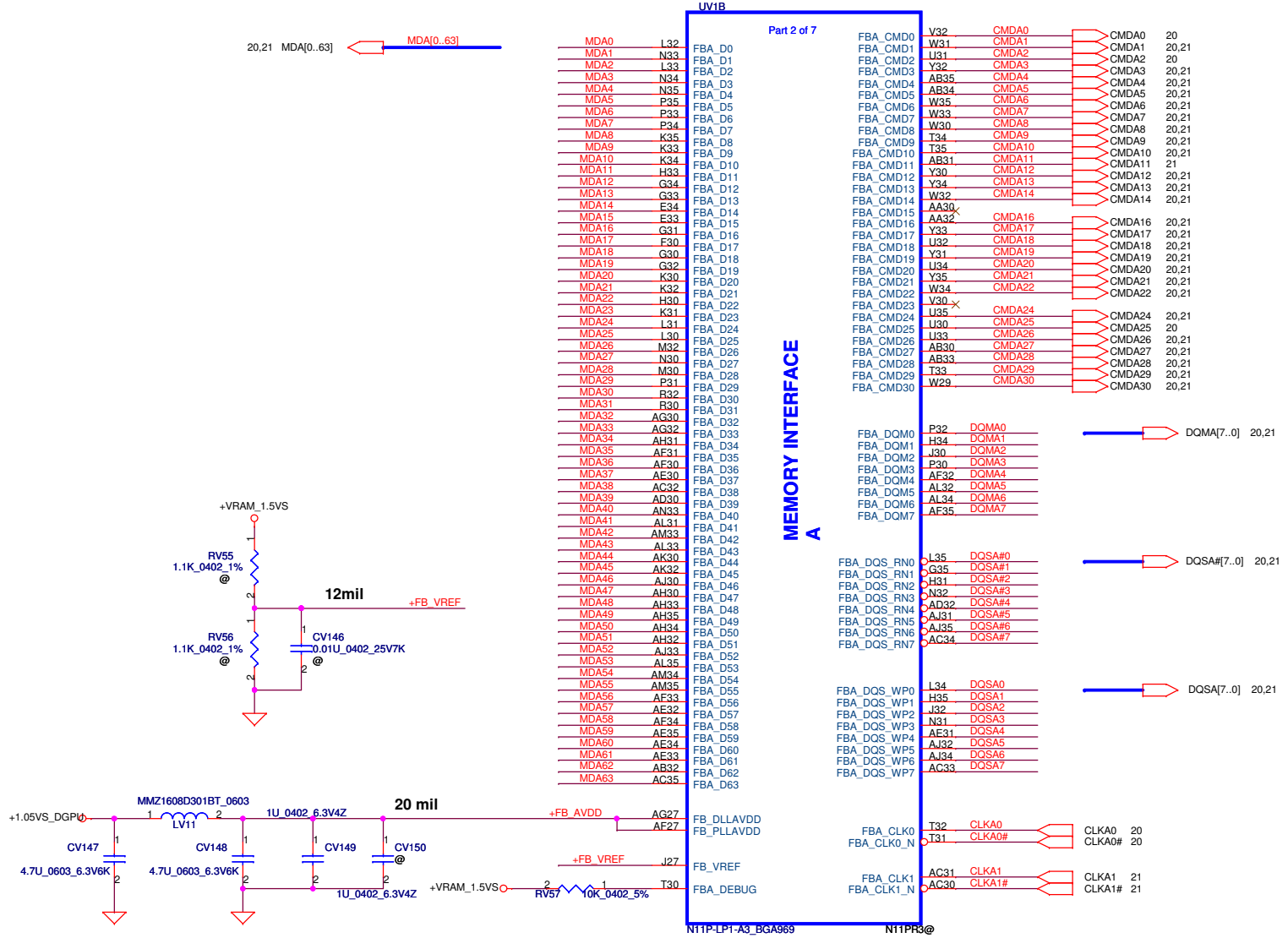
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: **GND**

Size	Document Number	Rev
	NBQAA LA6072P M/B	1.0

Date: Monday, March 22, 2010 | Sheet 17 of 61



Mode C - Mirror Mode Mapping

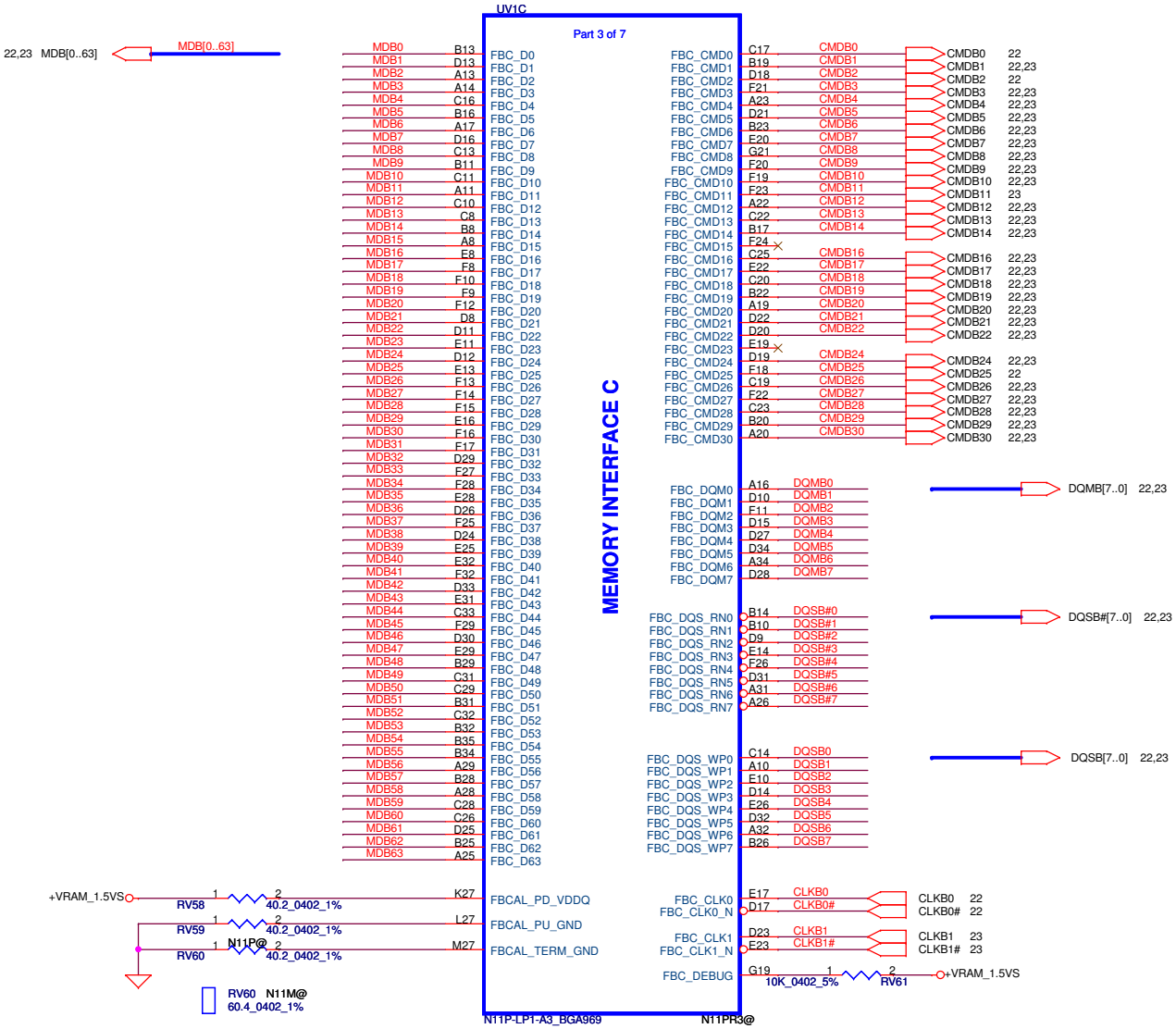
	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Compal Electronics, Inc.

Title: **MEM Interface A**

Size | Document Number: **NBQAA LA6072P M/B** | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 18 of 61



Mode C – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/01

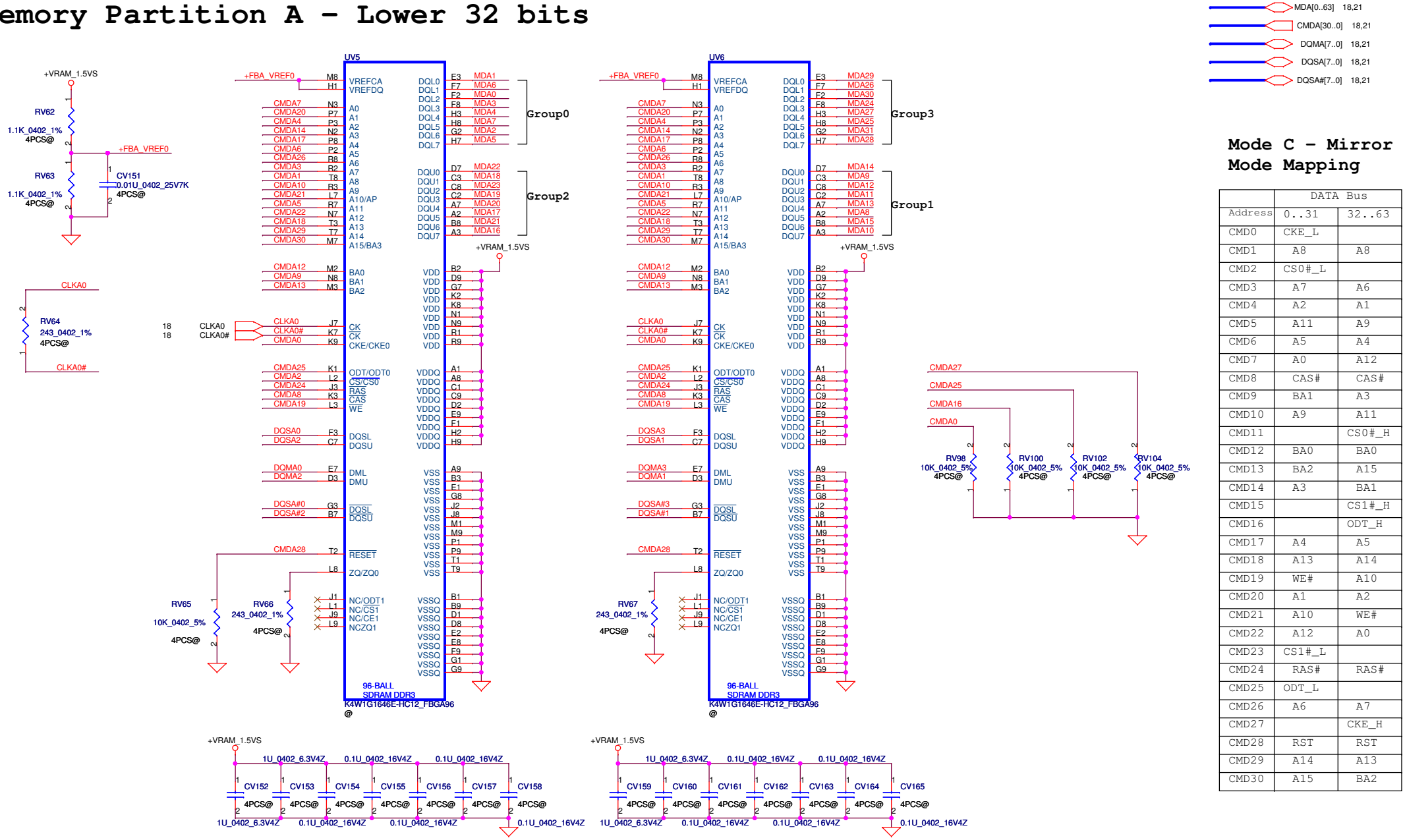
Compal Electronics, Inc.

Title: *MEM Interface C*

Size | Document Number: *NBQAA LA6072P M/B* | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 19 of 61

Memory Partition A - Lower 32 bits



Mode C - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/01

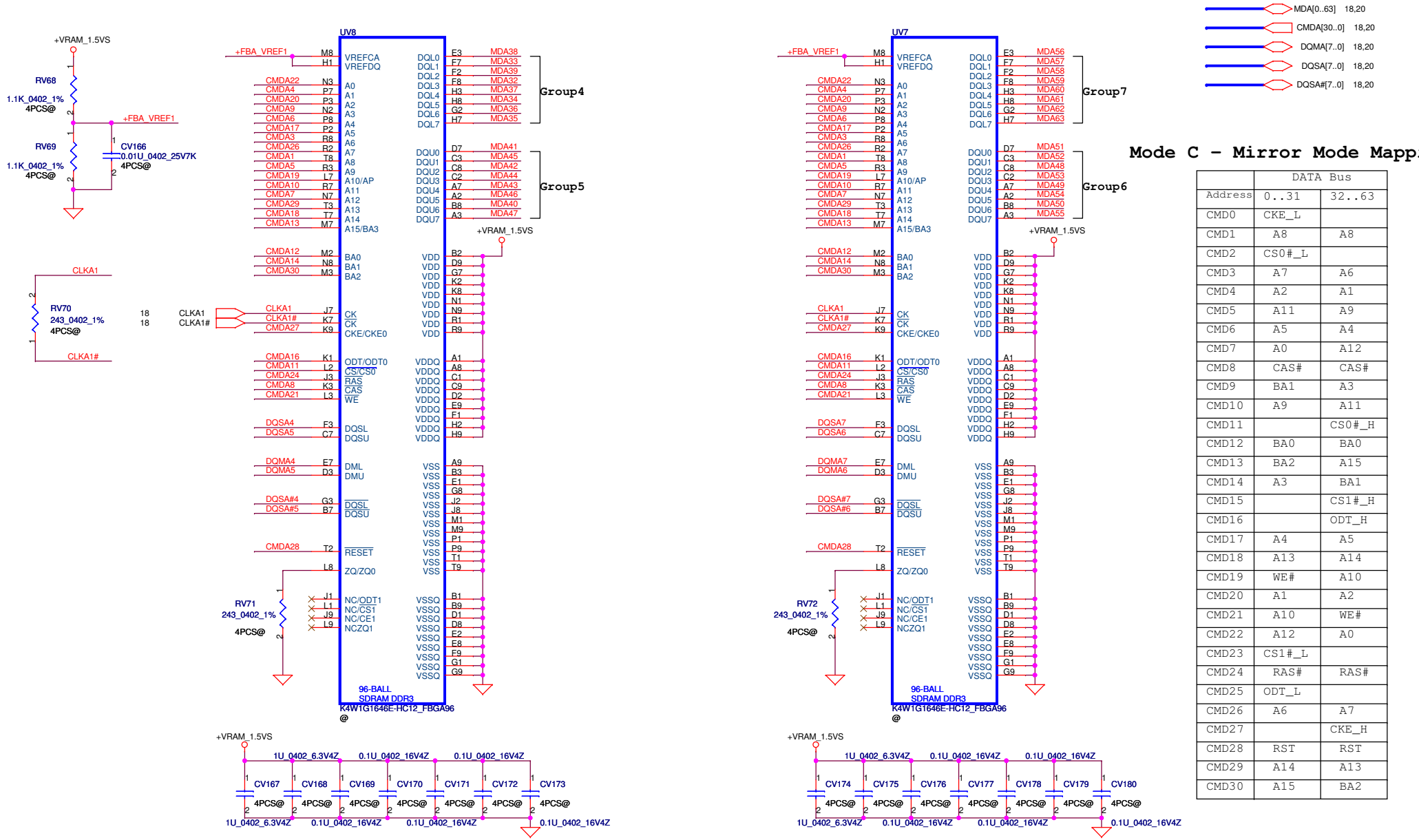
Compal Electronics, Inc.

Title: VRAM A Lower

Size | Document Number: NBQAA LA6072P M/B | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 20 of 61

Memory Partition A - Upper 32 bits



Mode C - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/01

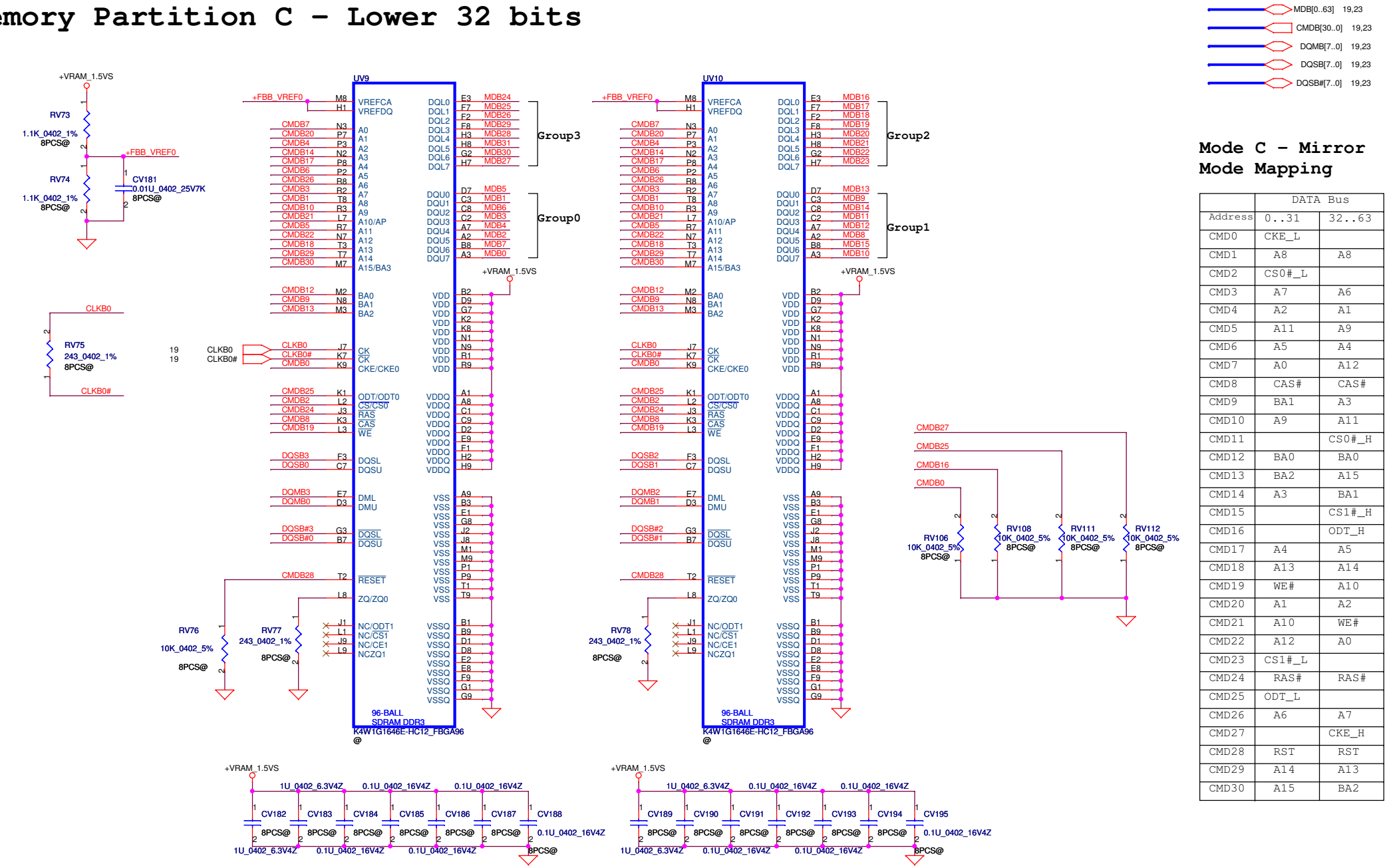
Compal Electronics, Inc.

Title: VRAM A Upper

Size | Document Number: NBQAA LA6072P M/B | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 21 of 61

Memory Partition C - Lower 32 bits



Mode C - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

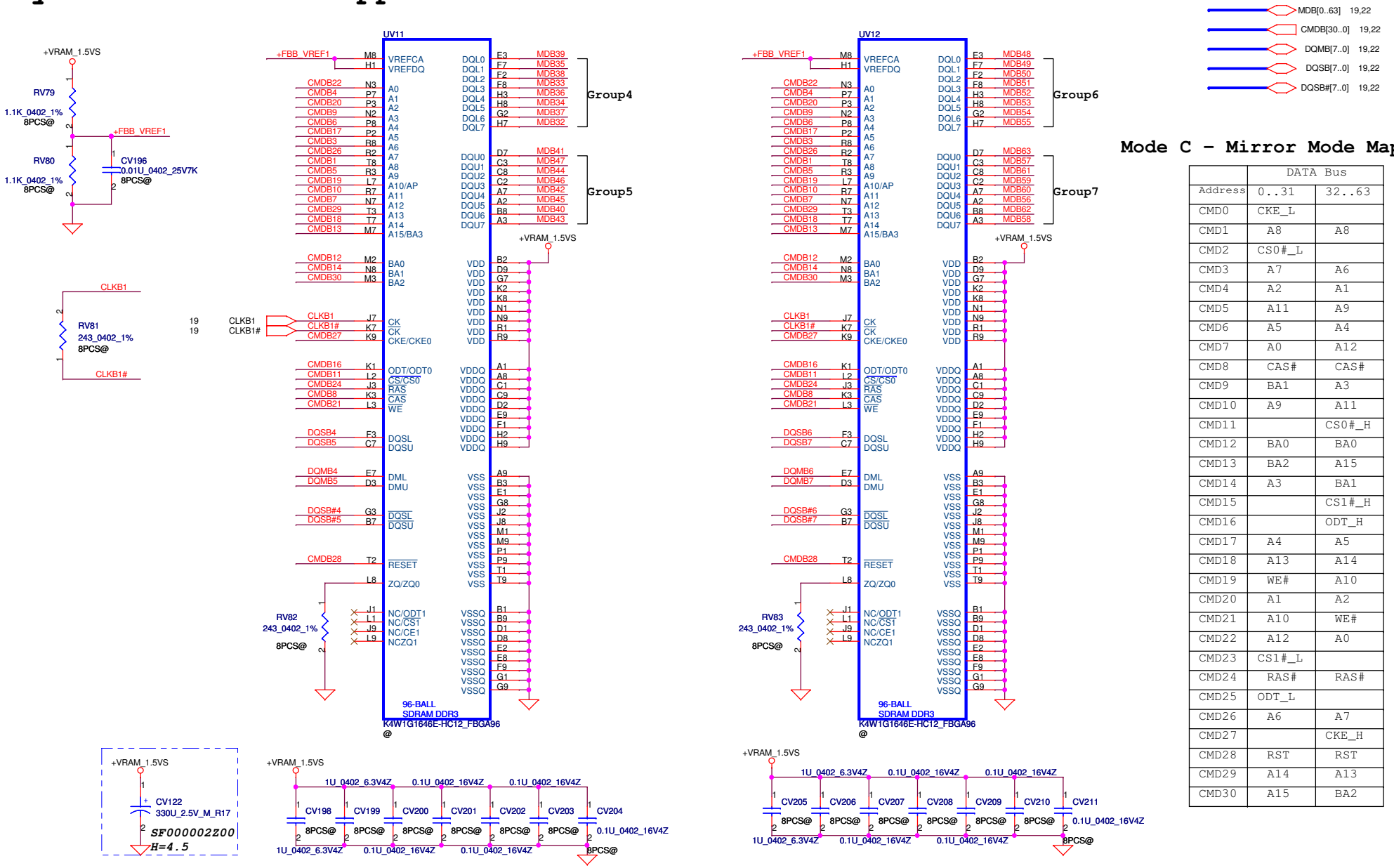
Compal Electronics, Inc.

Title: VRAM C Lower

Size: Custom | Document Number: NBQAA LA6072P M/B | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 22 of 61

Memory Partition C - Upper 32 bits



Mode C - Mirror Mode Mapping

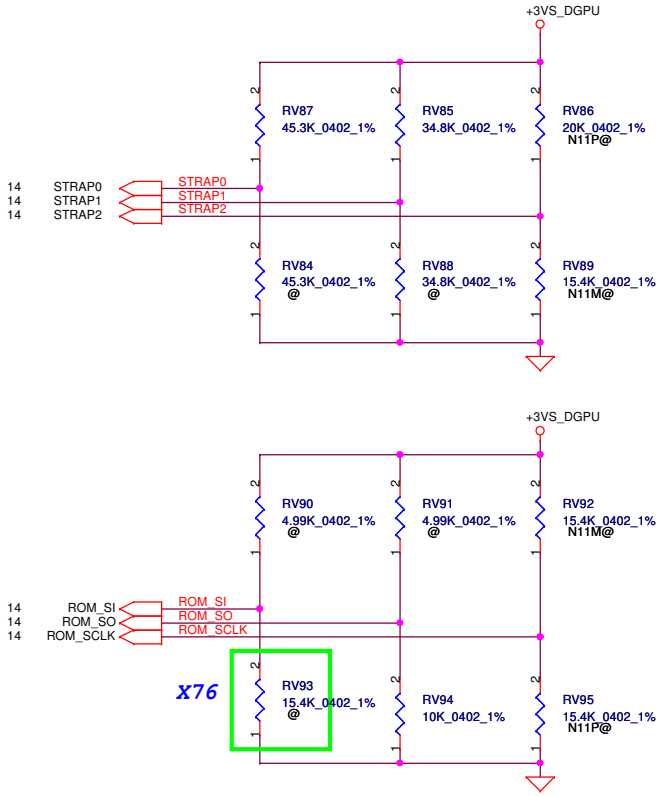
	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Compal Electronics, Inc.

Title: VRAM C Upper

Size: Custom | Document Number: NBQAA LA6072P M/B | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 23 of 61



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD33	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	VDD33	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	VDD33	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	VDD33	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	VDD33	USER[3]	USER[2]	USER[1]	USER[0]

Device ID straps

	DeviceID	PCI_DEVID[4..0]	ROM_SCLK	STRAP2
N11P-LP1	0xA2B	[01011]	Pull down 15K	Pull up 20K
N11M-GE1	0xA75	[10101]	Pull up 15K	Pull down 30K
N11M-OP1	0xA72	[10010]	Pull up 15K	Pull down 15K

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	VRAM		RAMCFG[3..0]	RV93	
DDR3 64M16	Hynix H5TQ1G63BFR-12C SA000032400	512MB	0010	PD 15K	SD034154280
		1GB	0010	PD 15K	SD034154280
	Samsung K4W1G1646E-HC12 SA000035700	512MB	0011	PD 20K	SD034200280
		1GB	0011	PD 20K	SD034200280
DDR3 128M16	Reserved for 128M16				

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	1110=EDID
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
1110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/01

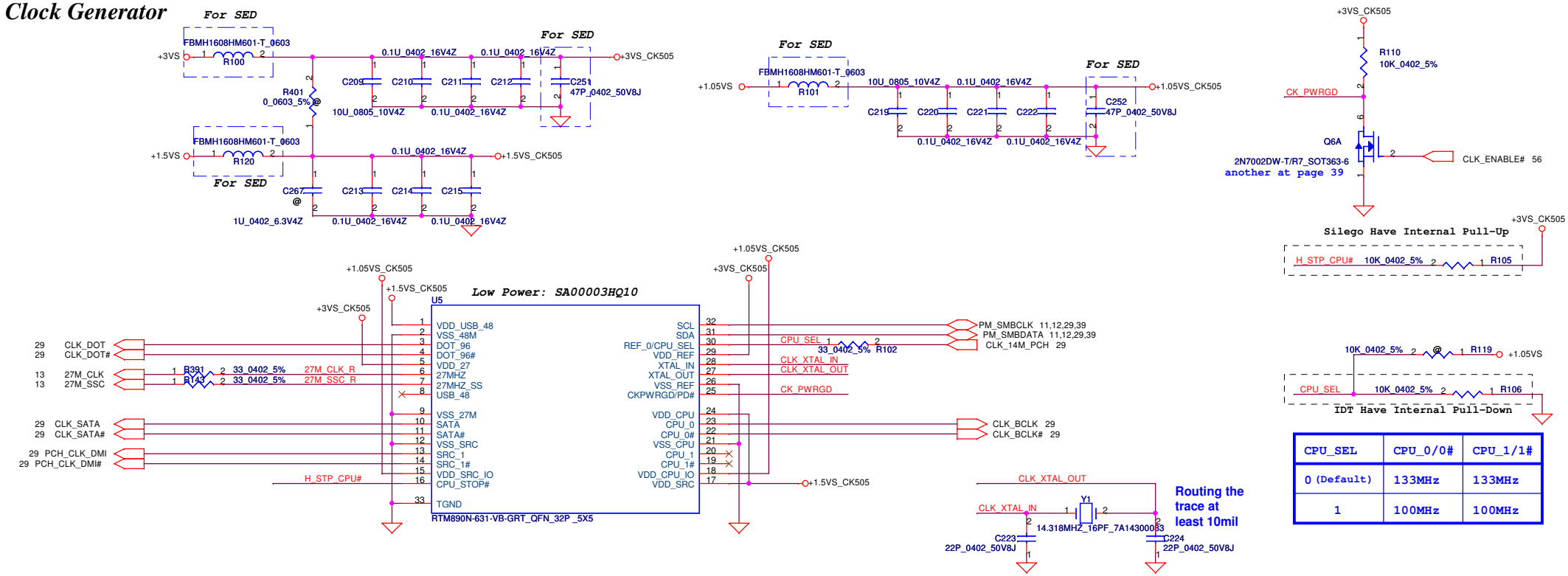
Compal Electronics, Inc.

Title: MSIC

Size: Custom | Document Number: NBQAA LA6072P M/B | Rev: 1.0

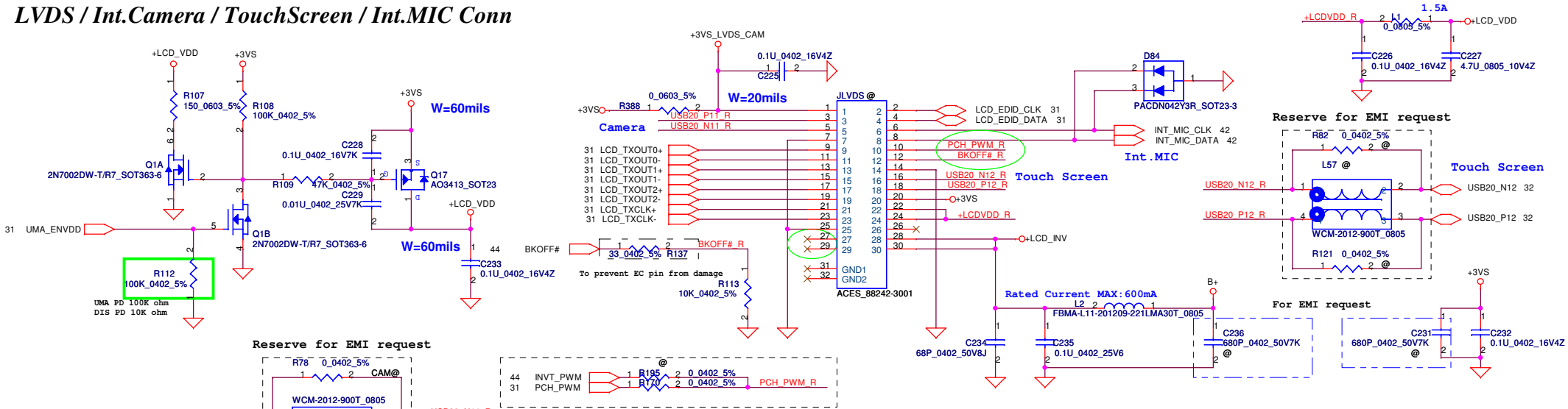
Date: Monday, March 22, 2010 | Sheet 24 of 61

Clock Generator



CPU_SEL	CPU_0/0#	CPU_1/1#
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

LVDS / Int.Camera / TouchScreen / Int.MIC Conn



Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

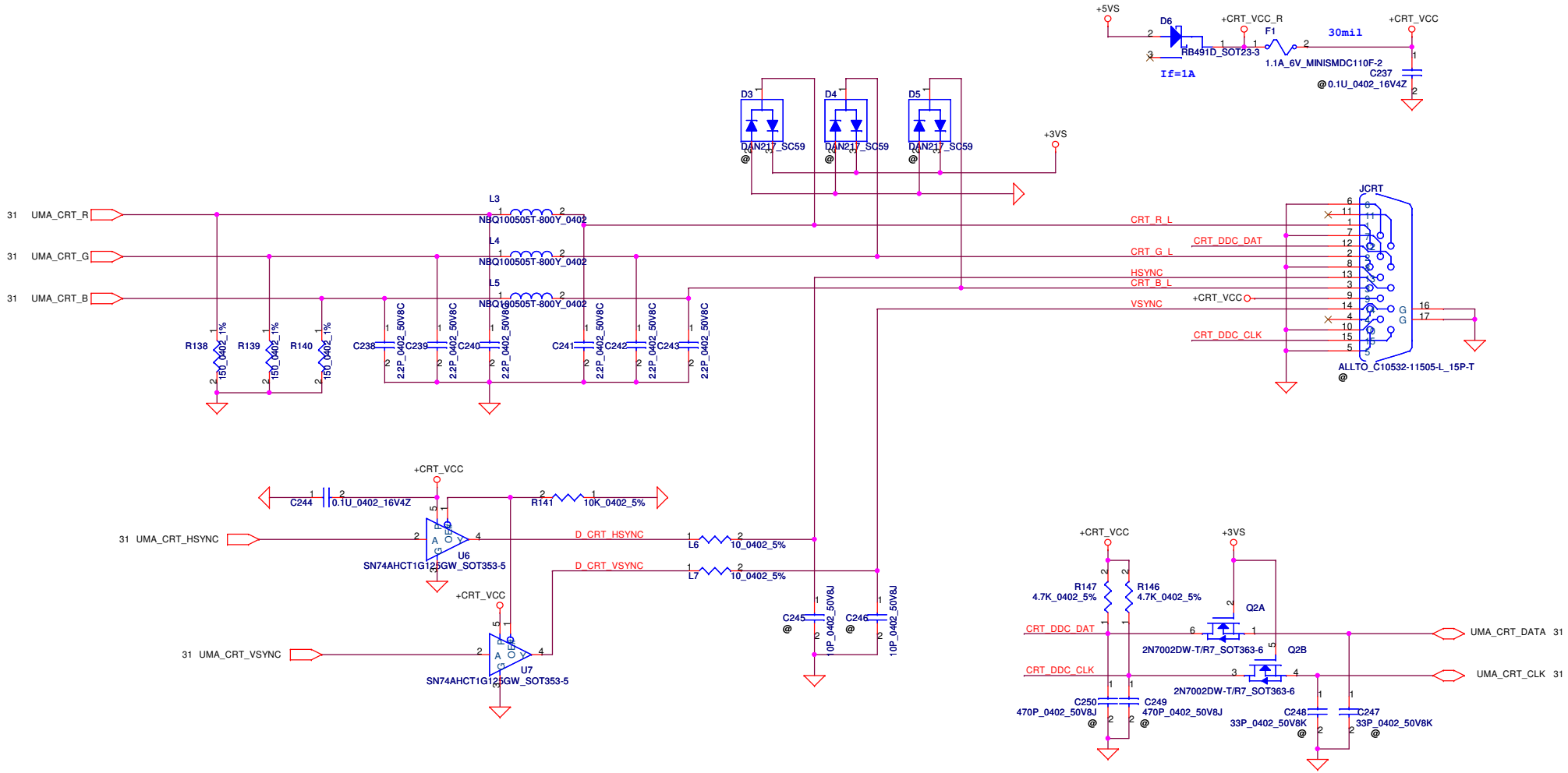
Compal Electronics, Inc.

Title: **Clock Generator (CK505)/ LVDS CONN**

Size	Document Number	Rev
Custom	NBQAA LA6072P M/B	1.0

Date: Monday, March 22, 2010 Sheet 25 of 61

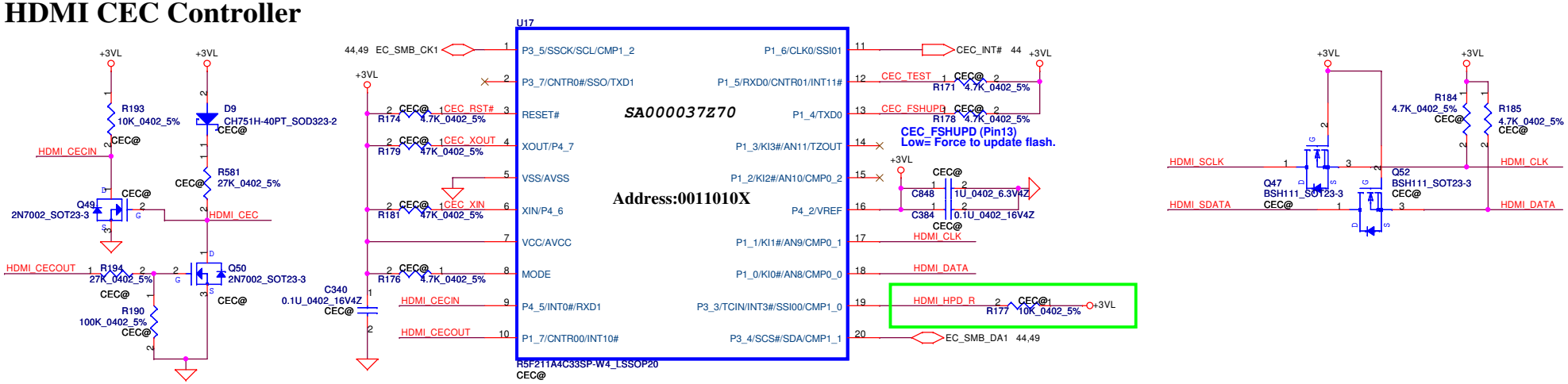
CRT CONNECTOR



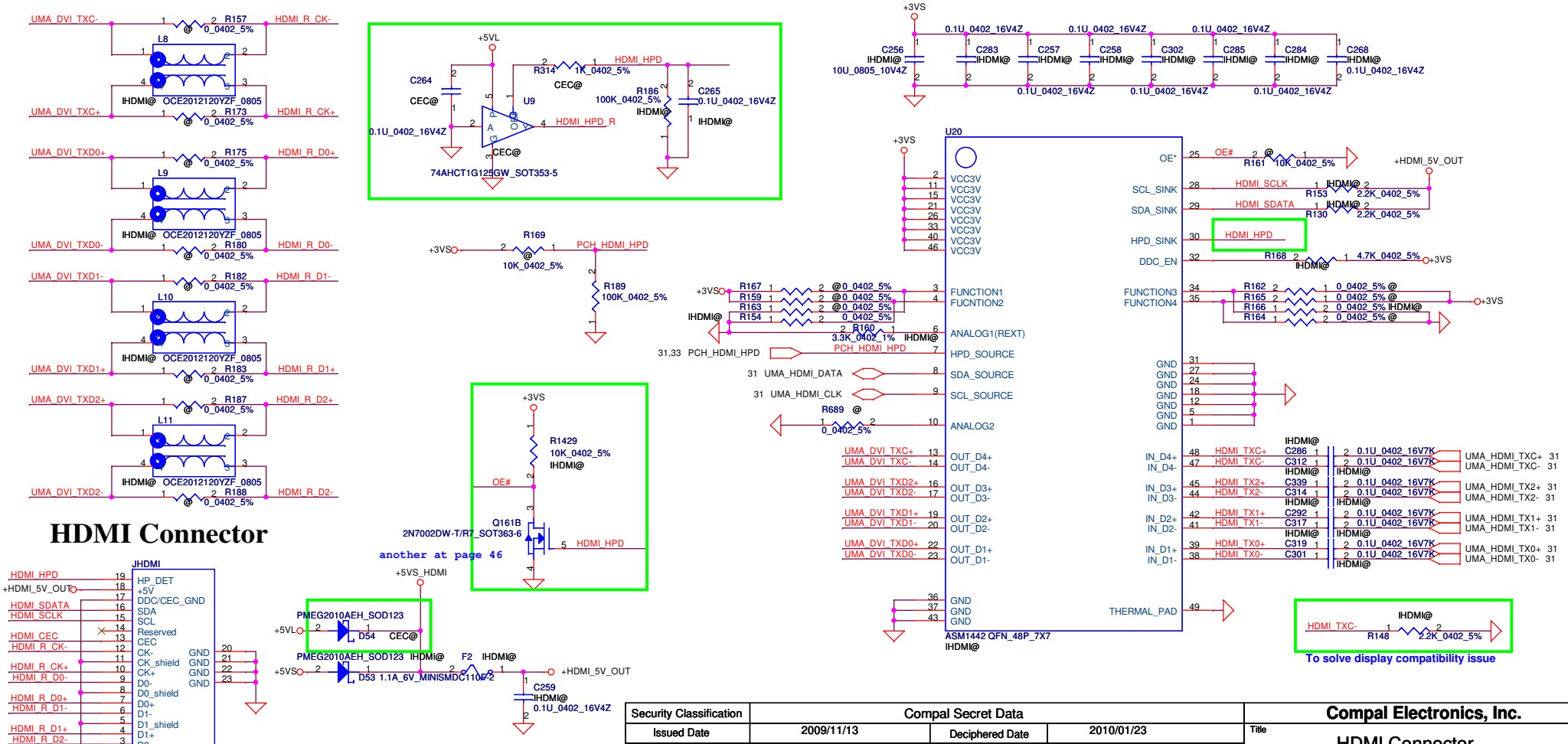
Compal Electronics, Inc.

Title	CRT\TV\LVDS	
Size	Document Number: NBQAA LA6072P M/B	Rev: 1.0
Date: Monday, March 22, 2010	Sheet 26 of 61	

HDMI CEC Controller



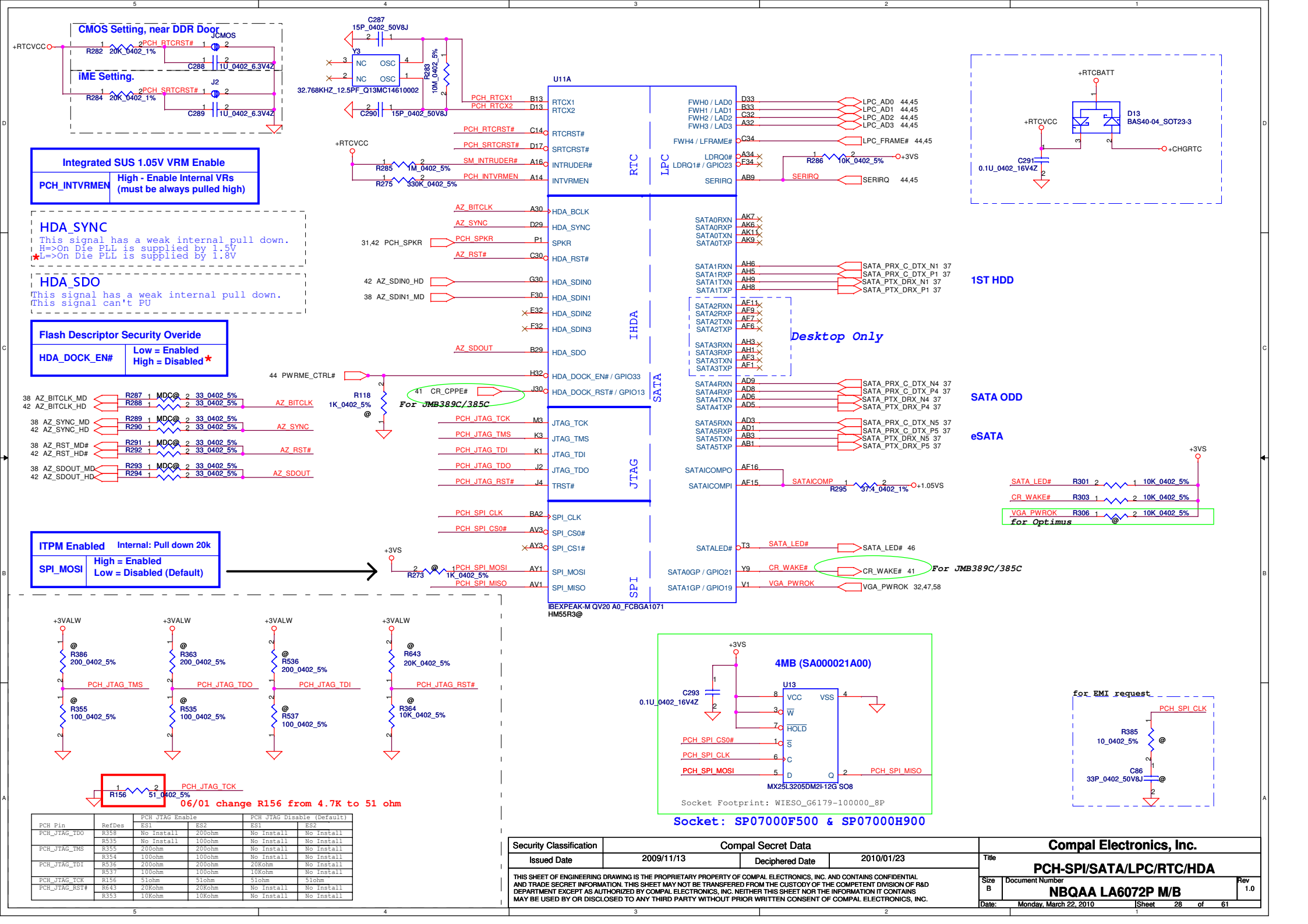
HDMI Connector



Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

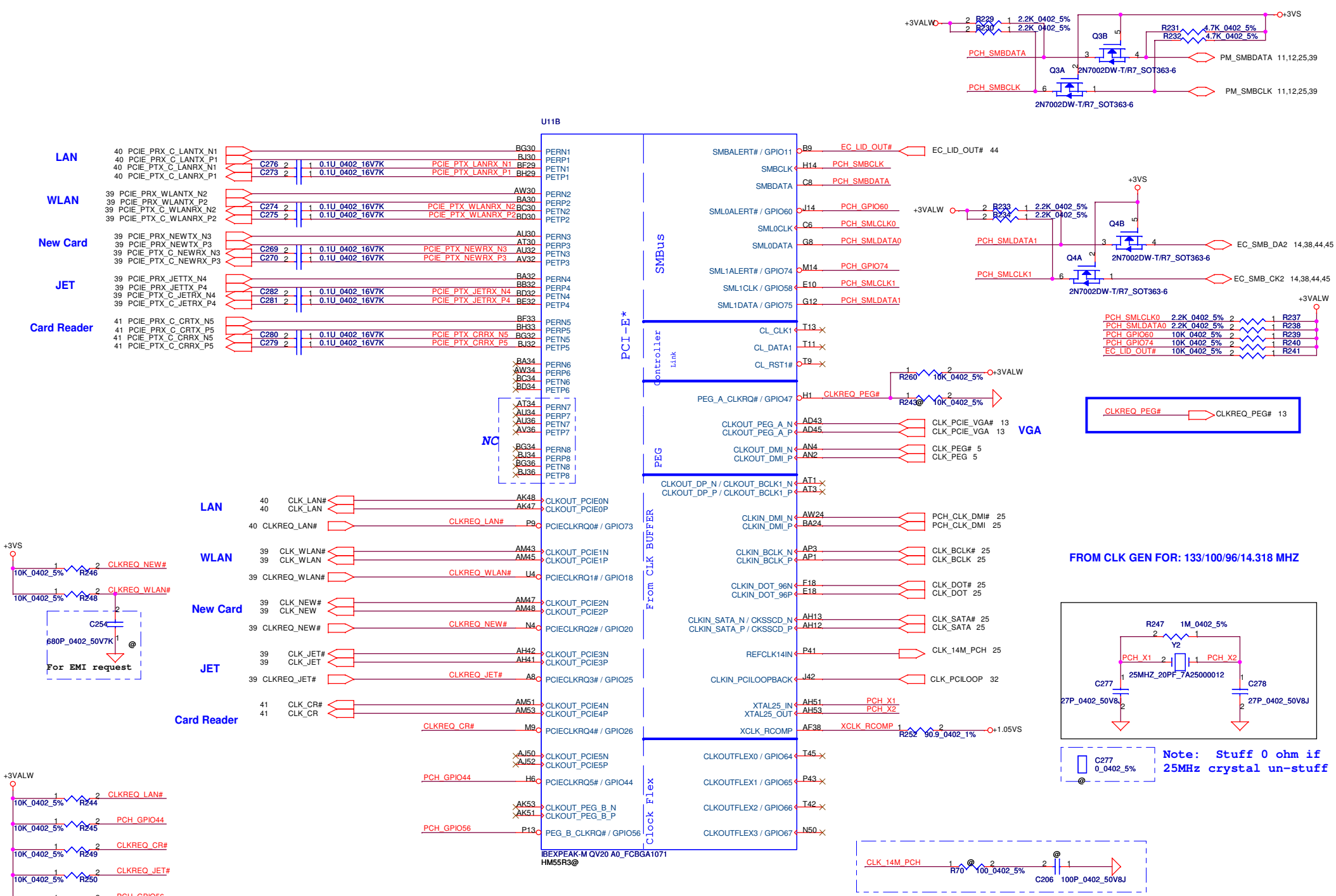
Title	HDMI Connector		
Size	Document Number		Rev
	NBQAA LA6072P M/B		1.0
Date:	Monday, March 22, 2010	Sheet	27 of 61



PCH Pin	RefDes	PCH JTAG Enable ES1	PCH JTAG Enable ES2	PCH JTAG Disable (Default) ES1	PCH JTAG Disable (Default) ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
	R535	No Install	100ohm	No Install	No Install
PCH_JTAG_TMS	R355	200ohm	200ohm	No Install	No Install
	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R536	200ohm	200ohm	20Kohm	No Install
	R537	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
	R353	10Kohm	10Kohm	No Install	No Install

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title	PCH-SPI/SATA/LPC/RTC/HDA		
Size B	Document Number NBQAA LA6072P M/B		Rev 1.0
Date: Monday, March 22, 2010	Sheet 28 of 61		



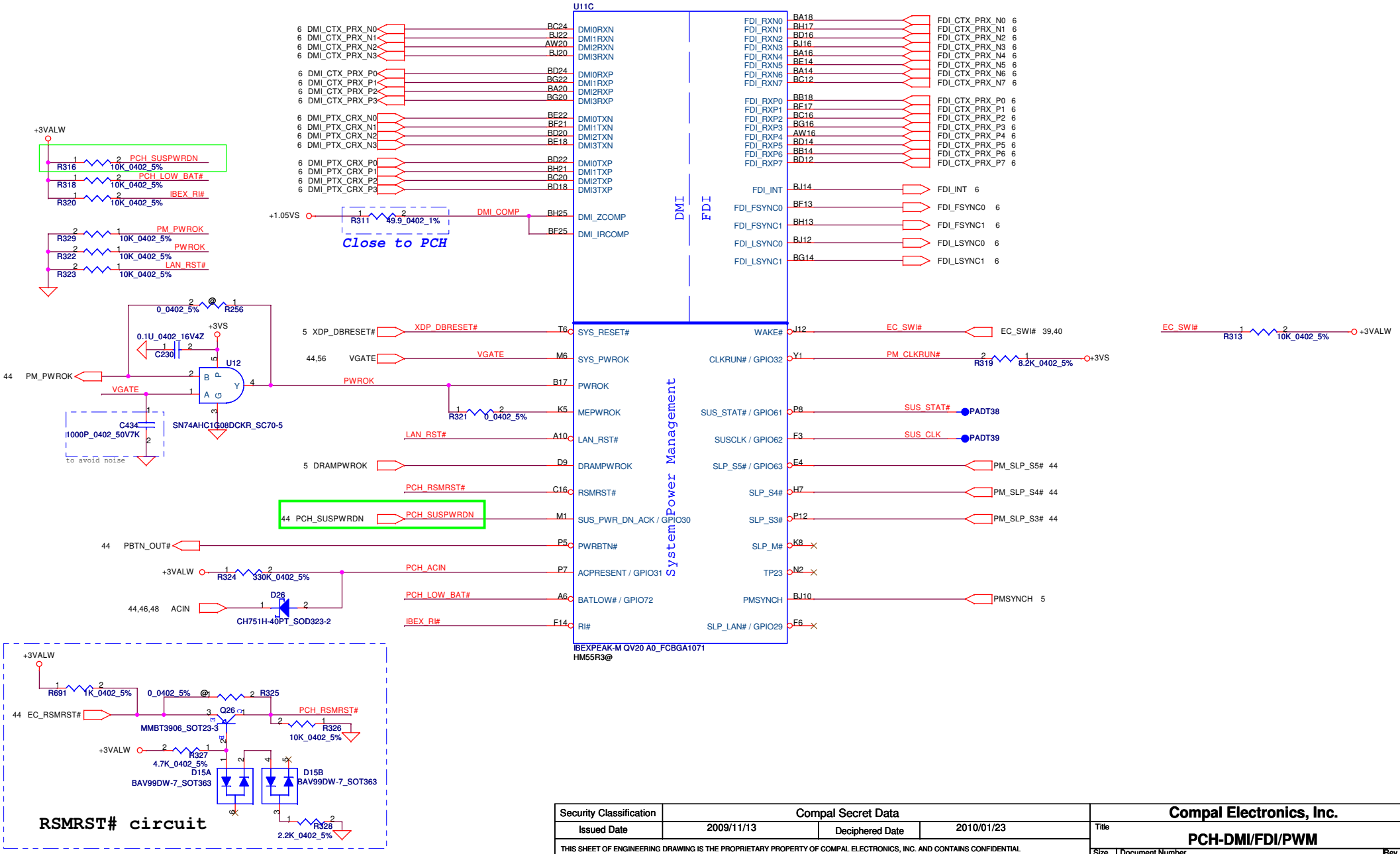
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **CLK/PCIE/SMBUS**

Size	Document Number	Rev
B	**NBQAA LA6072P M/B**	1.0

Date: Monday, March 22, 2010 Sheet 29 of 61



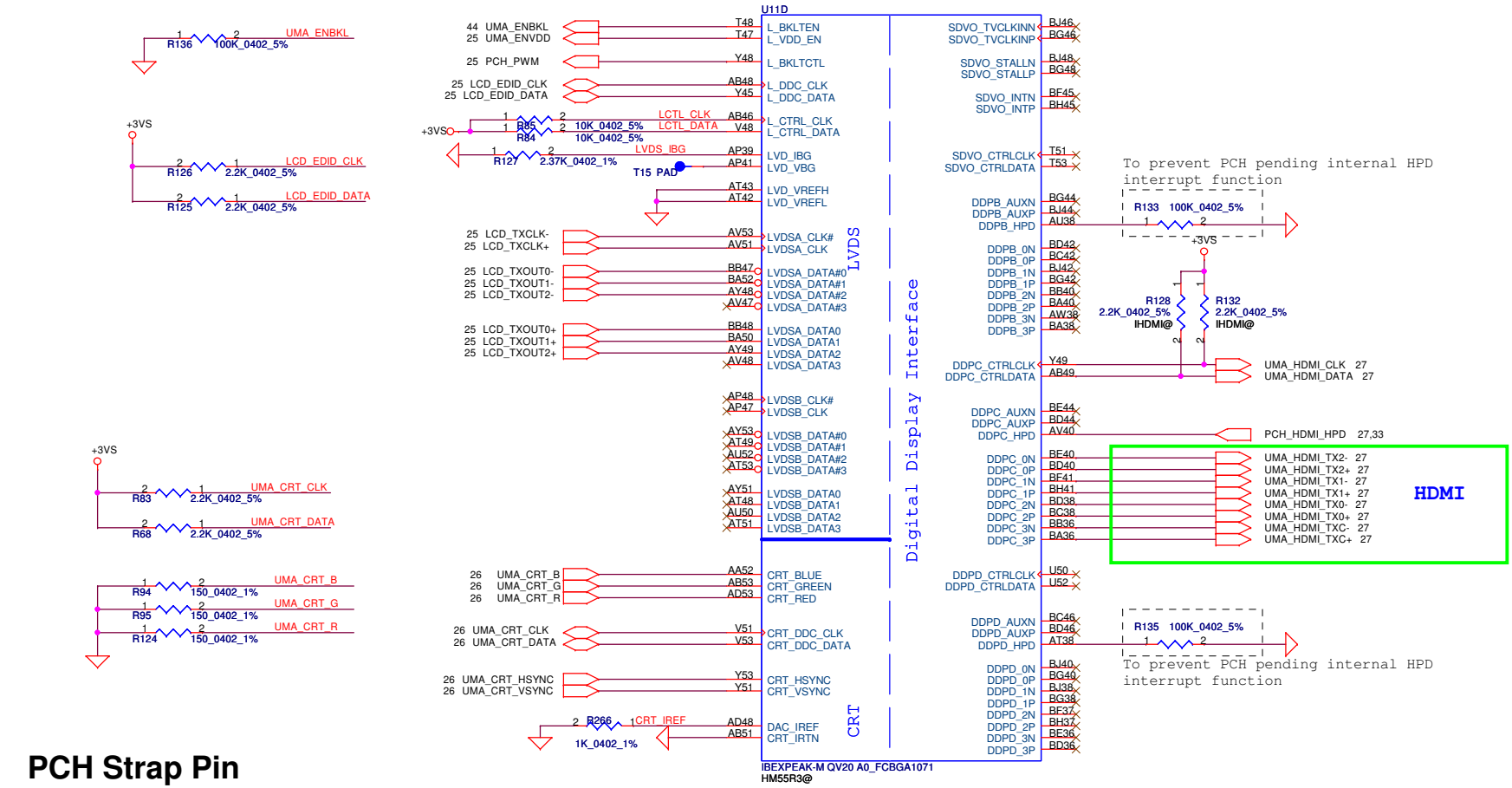
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

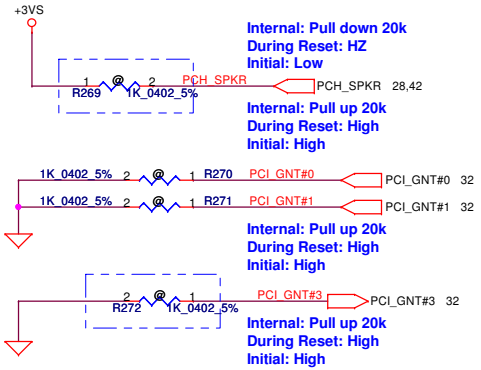
Title: **PCH-DMI/FDI/PWM**

Size	Document Number	Rev
B	NBQAA LA6072P M/B	1.0

Date: Tuesday, March 23, 2010 Sheet 30 of 61



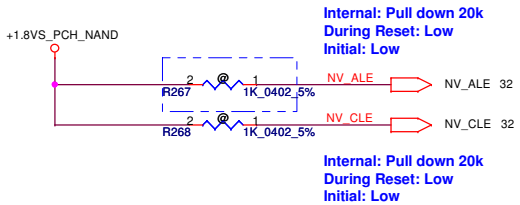
PCH Strap Pin



NO REBOOT Strap	
PCH_SPKR	Low= Disable High= Enable

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Loaction
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable

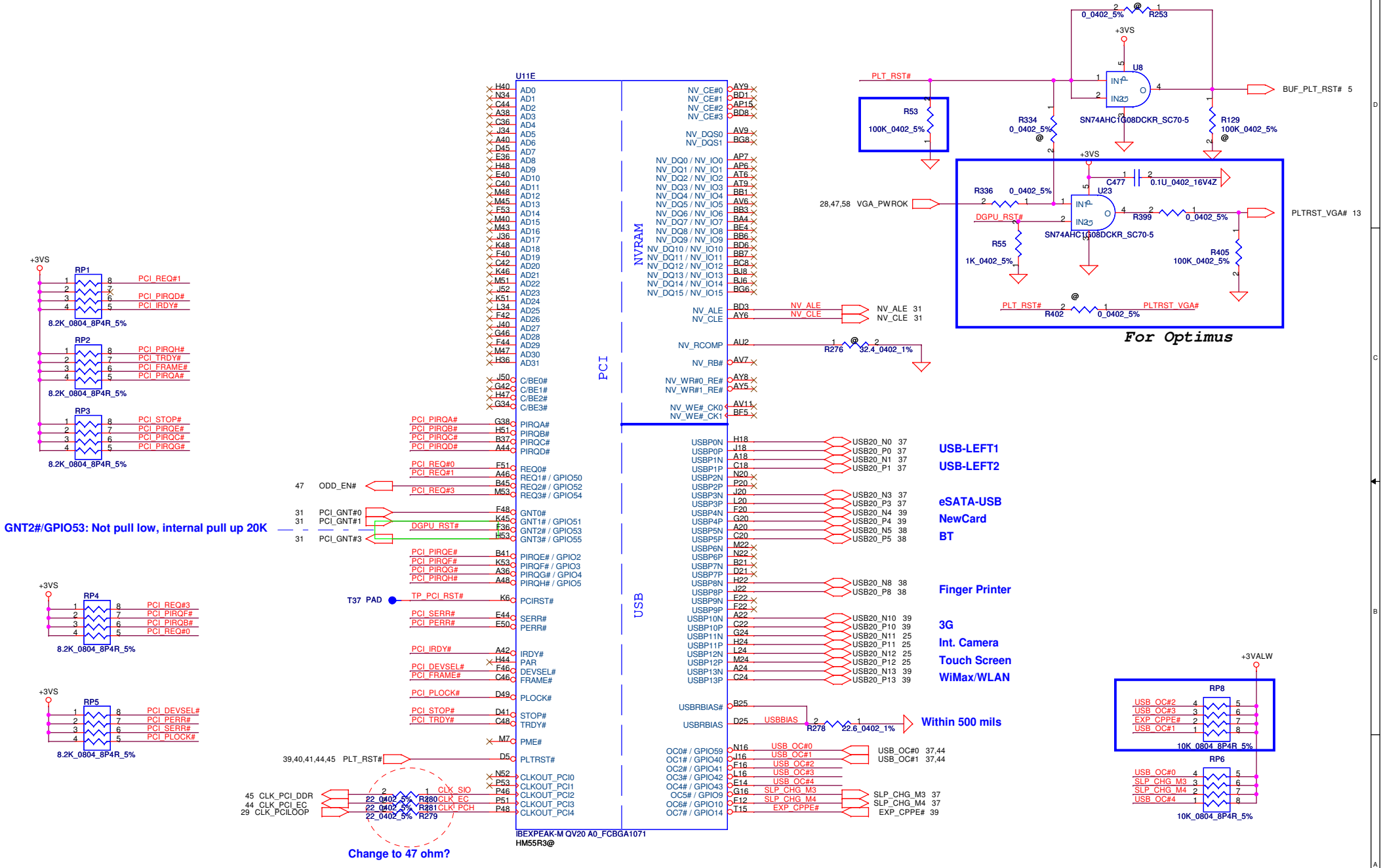


Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.	
Title	PCH-VGA/LVDS/TV
Size: Custom	Document Number: NBQAA LA6072P M/B
Rev	1.0
Date: Monday, March 22, 2010	Sheet 31 of 61



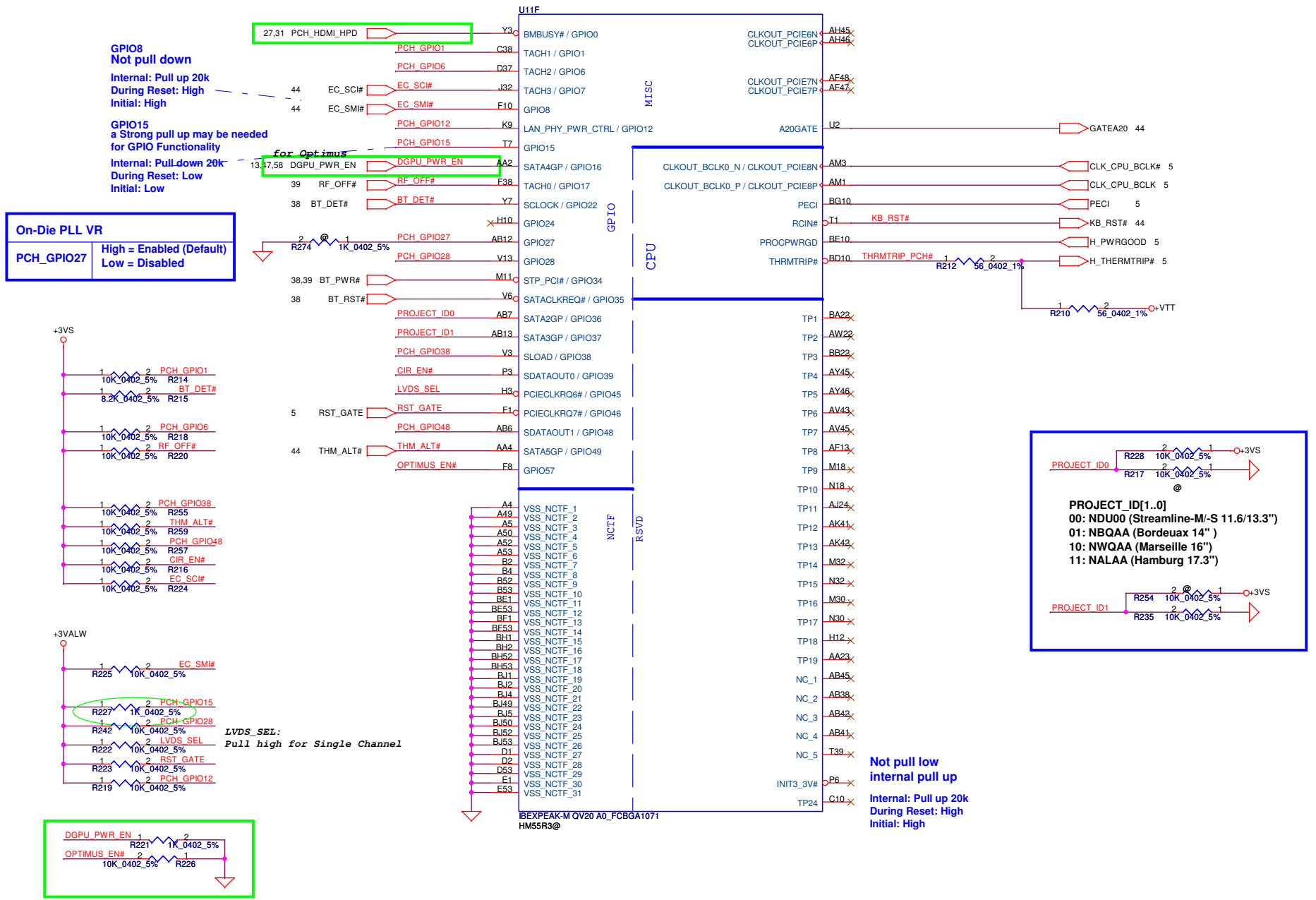
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **PCH USB/PCI/NAND**

Size	Document Number	Rev
B	NBQAA LA6072P M/B	1.0

Date: Monday, March 22, 2010 Sheet 32 of 61



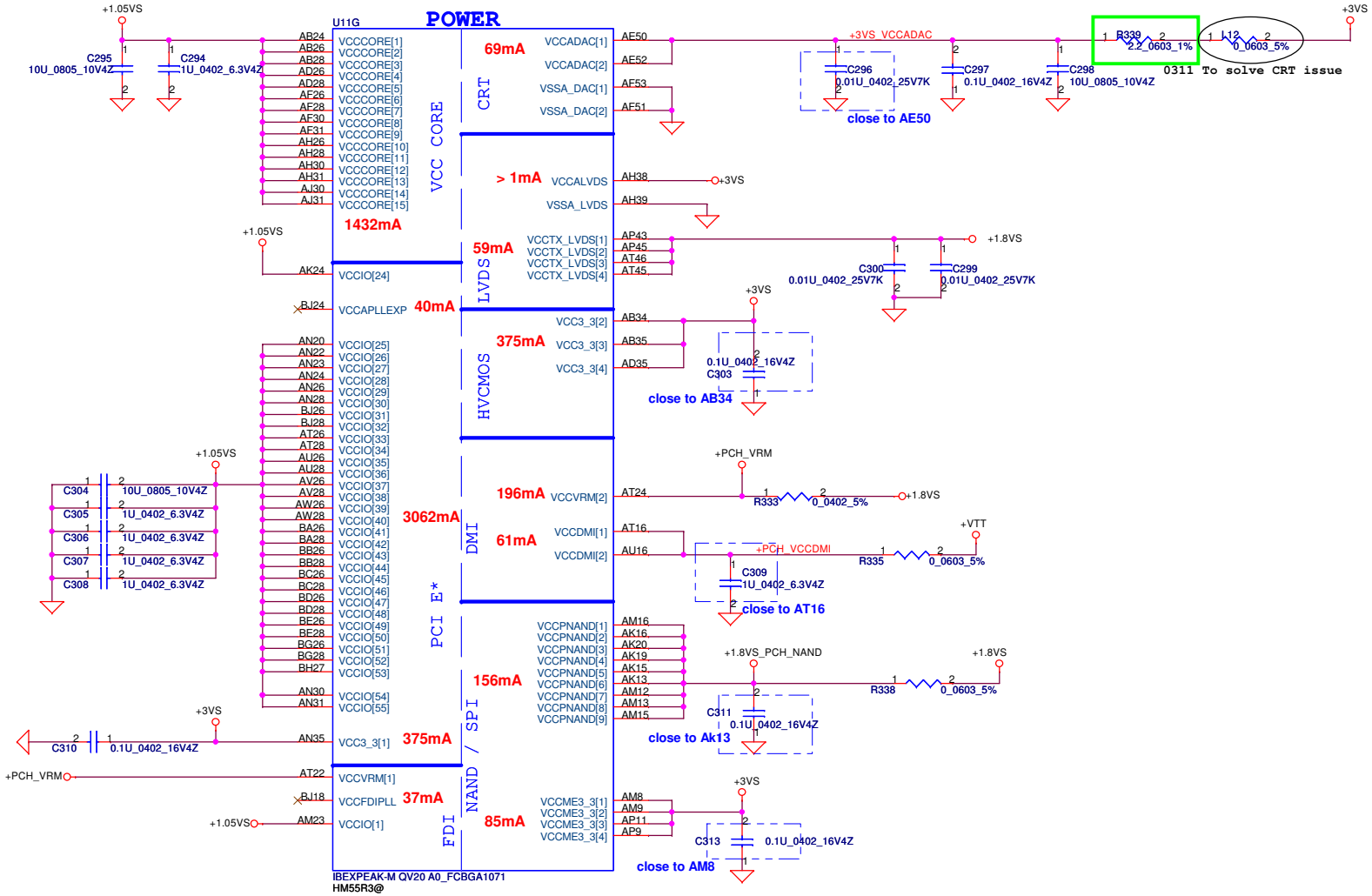
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **PCH CPU/GPIO**

Size	Document Number	Rev
B	NBQAA LA6072P M/B	1.0

Date: Monday, March 22, 2010 Sheet 33 of 61



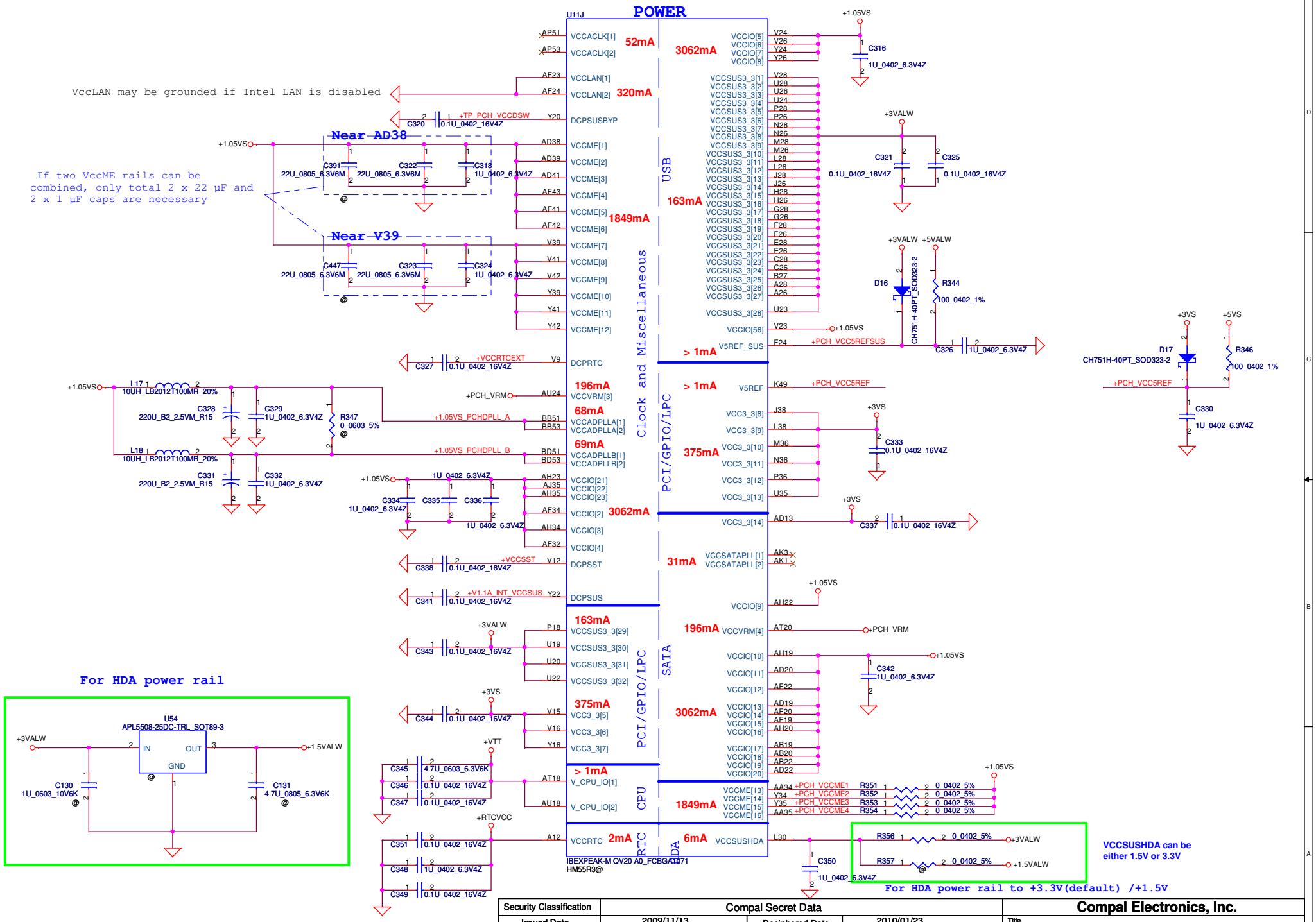
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **PCH POWER-1**

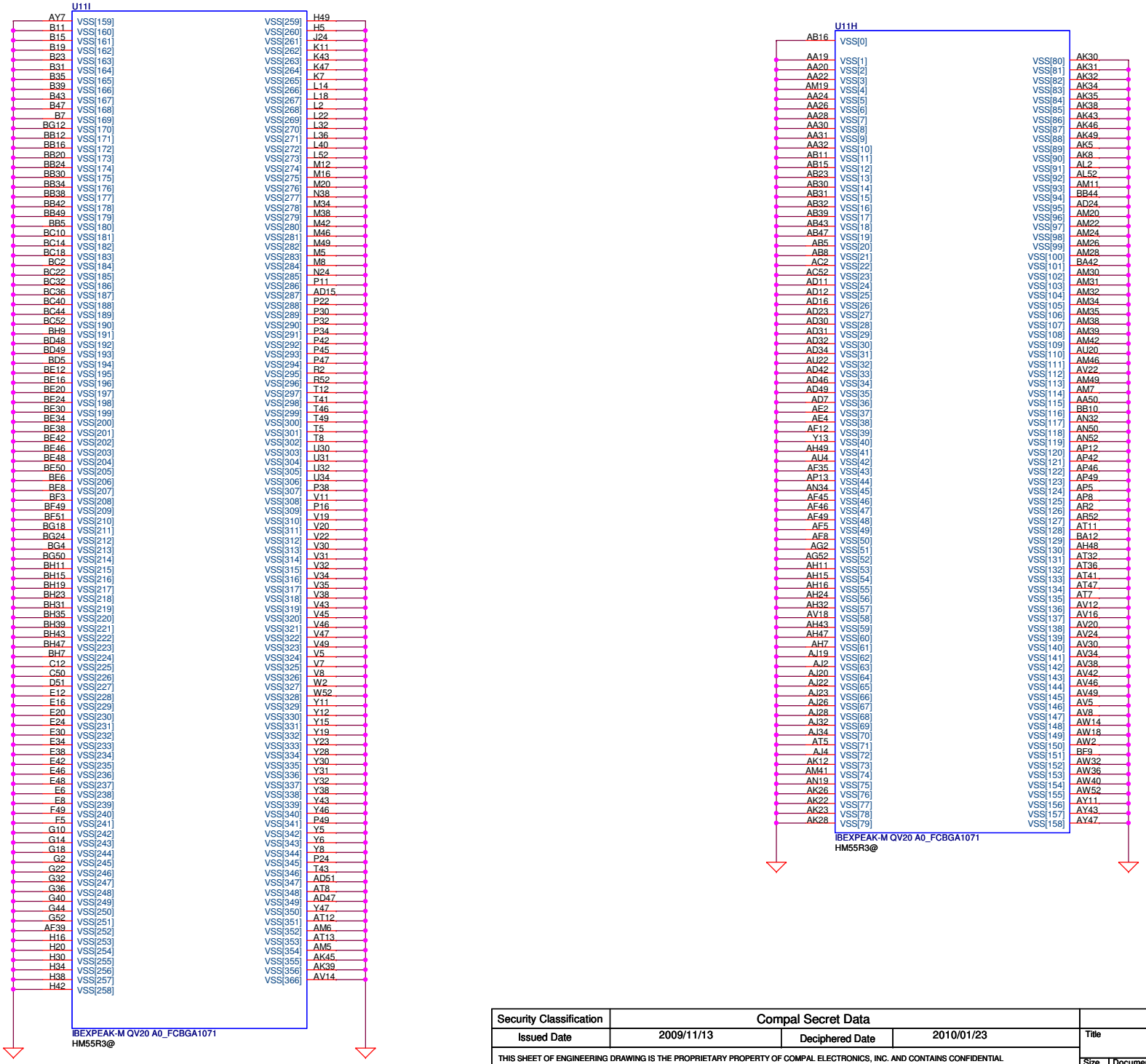
Size	Document Number	Rev
B	NBQAA LA6072P M/B	1.0

Date: Monday, March 22, 2010 Sheet 34 of 61



Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title	PCH POWER-2		
Size: Custom	Document Number: NBQAA LA6072P M/B		Rev: 1.0
Date: Monday, March 22, 2010	Sheet 35 of 61		



Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

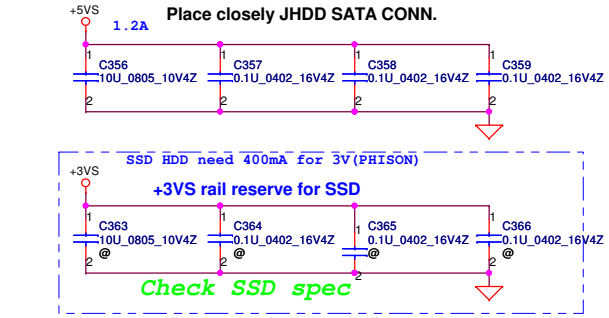
Compal Electronics, Inc.

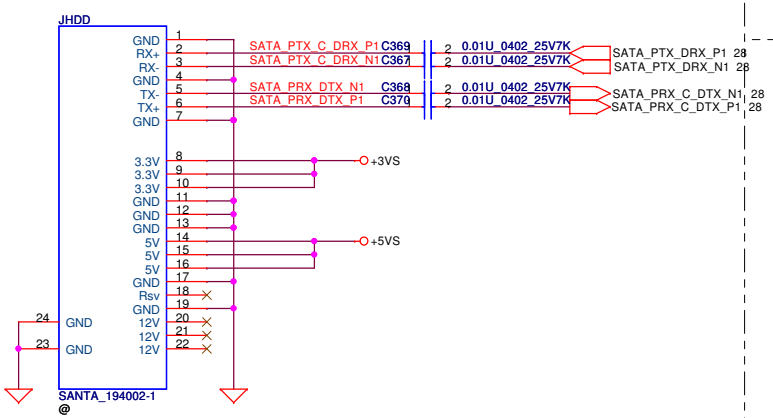
Title: **PCH-GND**

Size	Document Number	Rev
Custom	NBQAA LA6072P M/B	1.0

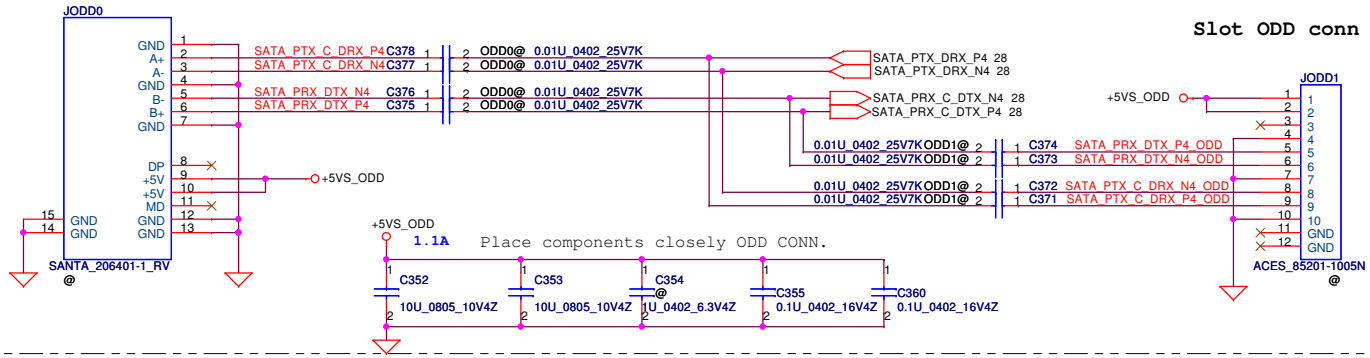
Date: Monday, March 22, 2010 Sheet 36 of 61

SATA HDD Conn.

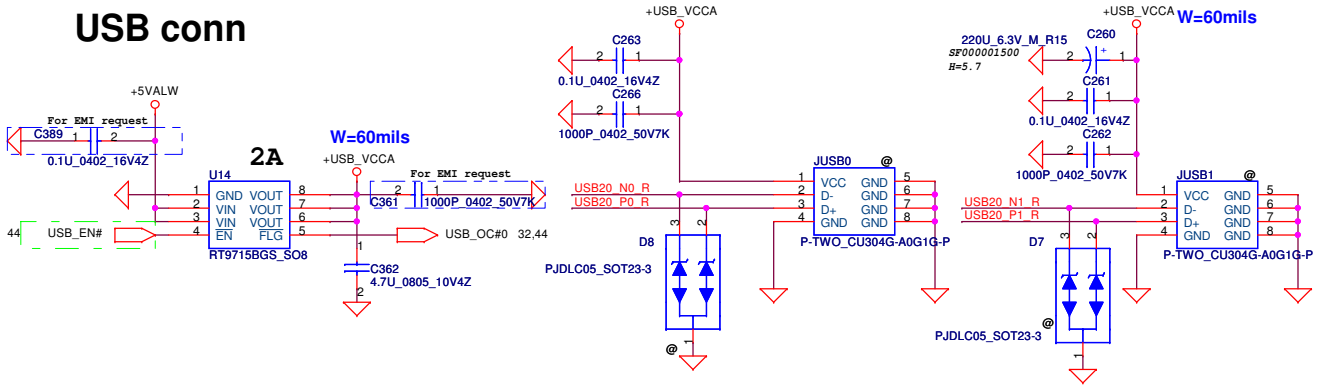




SATA ODD Conn



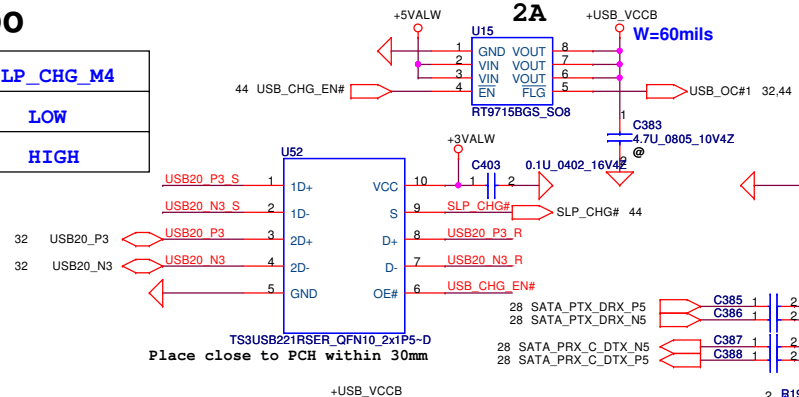
USB conn

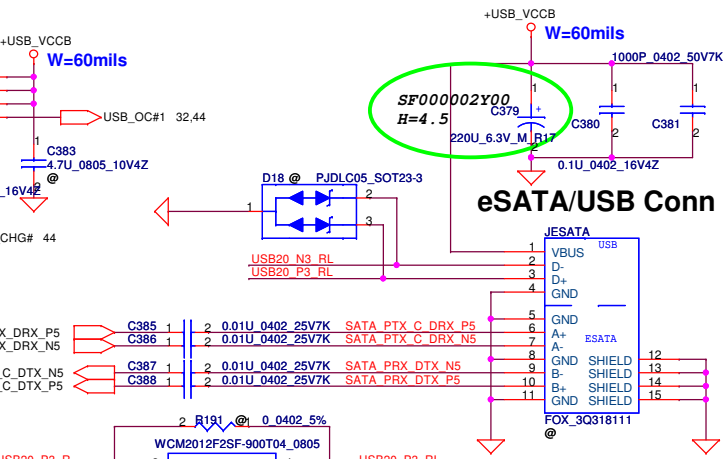


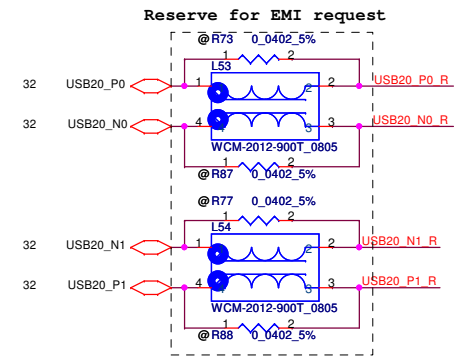
eSATA/USB combo

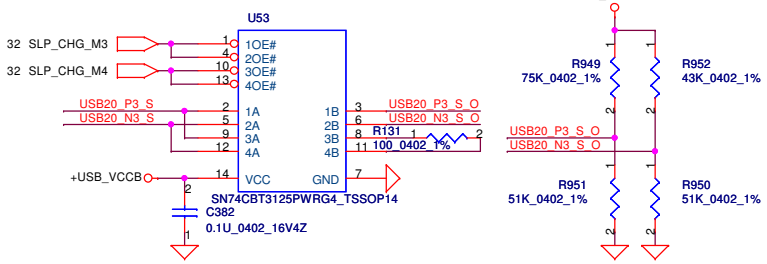
	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D









Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

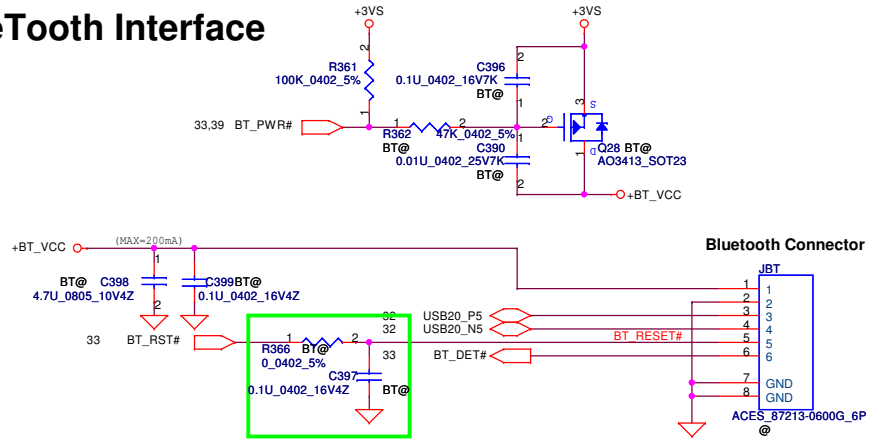
Compal Electronics, Inc.

Title: SATA-HDD/ODD/USB/E-SATA

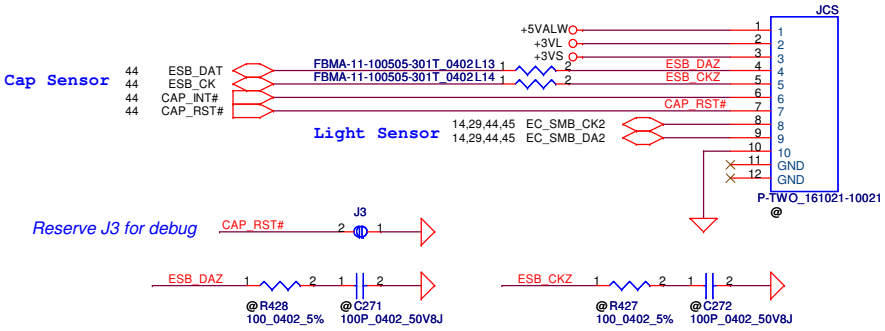
Size	Document Number	Rev
	NBQAA LA6072P M/B	1.0

Date: Tuesday, March 23, 2010 Sheet 37 of 61

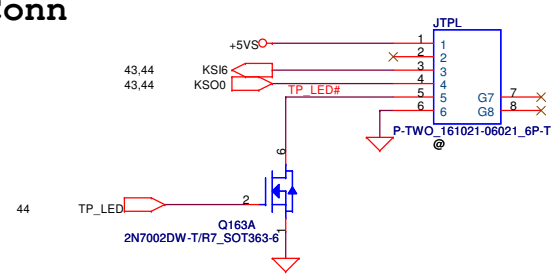
BlueTooth Interface



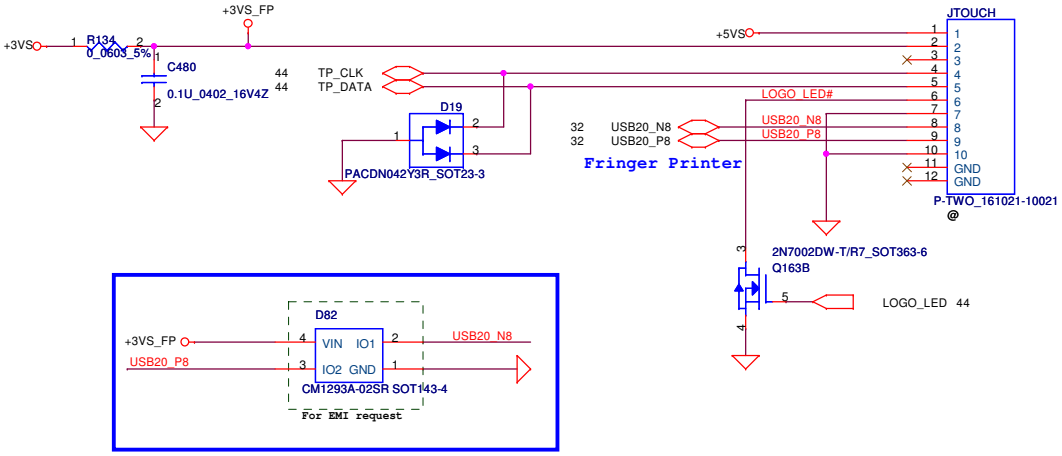
Cap Sensor / Light Sensor Conn



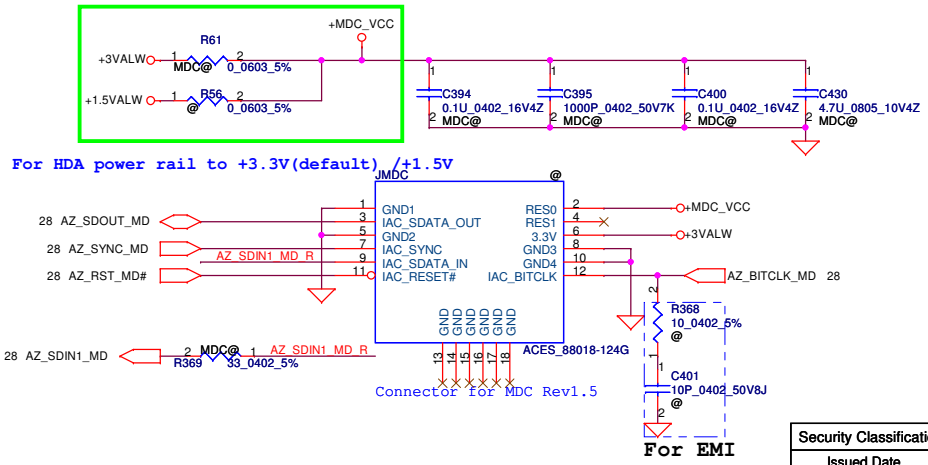
TP LED Conn



TP/B LED/B FP/B Conn



MDC 1.5 Conn



Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title	USB/BT/FP/MDC/TP/CAP		
Size	Document Number	NBQAA LA6072P M/B	Rev 1.0
Date: Monday, March 22, 2010	Sheet 38 of 61		

PCIe Mini Card-WLAN/WiMax

PJ27 +3VALW → +3V_WLAN, DEFAULT, JUMP_43X79
PJ26 +3VS, JUMP_43X79

Short PJ27 for Wimax
Short PJ26 for WLAN

+3V_WLAN: 0.1U_0402_16V4Z CM1, CM2, CM3; 0.01U_0402_25V4Z; 4.7U_0805_10V4Z; CM10 47P_0402_50V8J — For SED

+1.5VS: 0.1U_0402_16V4Z CM7, CM8, CM9; 0.01U_0402_25V4Z; 4.7U_0805_10V4Z; CM11 47P_0402_50V8J — For SED

JWLAN → FOX_AS0B226-S40N-7F @

BT_CTRL
29 CLKREQ_WLAN#
29 CLK_WLAN#
29 CLK_WLAN
PLT_RST#
WL_OFF# 44
PLT_RST# 32,40,41,44,45
29 PCIE_PRX_WLANTX_N2
29 PCIE_PRX_WLANTX_P2
29 PCIE_PTX_C_WLANRX_N2
29 PCIE_PTX_C_WLANRX_P2
PM_SMBCLK 11,12,25,29
PM_SMBDATA 11,12,25,29
USB20_N13 32
USB20_P13 32
LED_WIMAX#
LED_WIMAX# 46
+3V_WLAN
+3VS
RM6 100K_0402_5%
WIMAX@

WLAN/ WiFi

44 E51_TXD
44 E51_RXD
R16 0_0402_5%
R17 0_0402_5%
Debug card using
R345 100K_0402_5%

BT on Combo module		
	Enable	Disable
BT_CRTL	HIGH	LOW
BT_PWR#	LOW	HIGH

WiMax/BT

**If +3V_WLAN is +3VS, please remove D22

DM2 SUSP# → BT_CTRL, CH751H-40PT_SOD323-2
33,38 BT_PWR# → Q14B 2N7002DW-T/R7_SOT363-6

PCIe Mini Card-3G/JET

500mA +1.5VS, 2.75A +3VS

J3G → FOX_AS0B226-S40N-7F @

29 CLKREQ_JET#
29 CLK_JET#
29 CLK_JET
UIM_DATA
UIM_CLK
UIM_RESET
UIM_VPP
+UIM_PWR
PLT_RST#
RF_OFF# 33
29 PCIE_PRX_JETTX_N4
29 PCIE_PRX_JETTX_P4
29 PCIE_PTX_C_JETRX_N4
29 PCIE_PTX_C_JETRX_P4
PM_SMBCLK
PM_SMBDATA
USB20_N10 32
USB20_P10 32
LED_WIMAX#

PCIE--JET

+3VS: 0.1U_0402_16V4Z CM4, CM5, CM6; 0.01U_0402_25V7K; 4.7U_0805_10V4Z; CM12 47P_0402_50V8J — 120 MIL For SED
3GJET@

3G

+UIM_PWR → CM13 0.1U_0402_16V4Z 3G@; DM1 RLZ20A_LL34 3G@
J3GSIM (VCC, RST, CLK, NC, GND, VPP, I/O, NC) → MOLEX_47273-0001~D @
UIM_RESET
UIM_CLK
UIM_VPP
UIM_DATA
CM15 10P_0402_50V8J 3G@
CM16 10P_0402_50V8J 3G@
RM2 4.7K_0402_5% @
CM14 22P_0402_50V8J @

+3VALW_CARD Imax = 0.275A: CN1 10U_0805_10V4Z, CN2 0.1U_0402_16V4Z
+3VS_CARD Imax = 1.35A: CN3 10U_0805_10V4Z, CN4 0.1U_0402_16V4Z
+1.5VS_CARD Imax = 0.75A: CN5 10U_0805_10V4Z, CN6 0.1U_0402_16V4Z

+3VALW
RN4 2 CP_USB# 100K_0402_5%

UN1 TPS2231MRGPR-2 QFN
+1.5VS → 1.5Vin, 1.5Vout → +1.5VS_CARD (60mils)
+3VS → 3.3Vin, 3.3Vout → +3VS_CARD (40mils)
+3VALW → AUX_IN, AUX_OUT → +3VALW_CARD (40mils)
PLT_RST#
44,54 SYSON
44,47,50,53,58 SUSP#
EXP_CPPE#
CP_USB#
RCLKEN
SYSRST#, SHDN#, STBY#, CPPE#, CPUSB#, RCLKEN, OC#, PERST#, NC, GND, Thermal_Pad

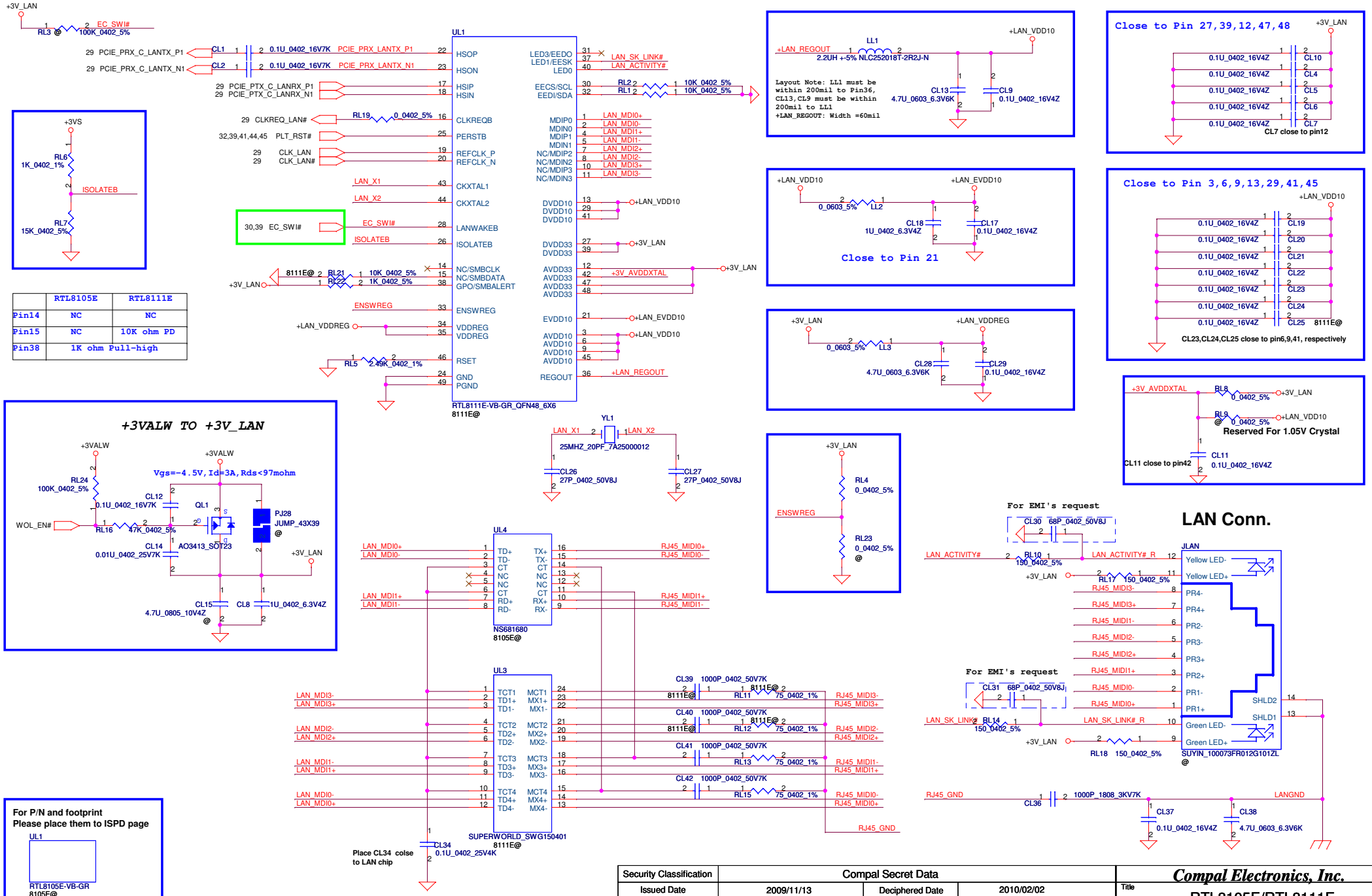
JEXP → SANTA_130861-2_26P_RT-T @
USB20_N4_R
USB20_P4_R
CP_USB#
PM_SMBCLK
PM_SMBDATA
+1.5VS_CARD
30,40 EC_SWI#
+3VALW_CARD
+3VS_CARD
PERST#
CLKREQ#
EXP_CPPE#
29 CLK_NEW#
29 CLK_NEW
29 PCIE_PRX_NEWTX_N3
29 PCIE_PRX_NEWTX_P3
29 PCIE_PTX_C_NEWRX_N3
29 PCIE_PTX_C_NEWRX_P3

+3VS
RN7 10K_0402_5% @
RN6 10K_0402_5% @
CN7 0.1U_0402_16V4Z @
UN2 NC7SZ32P5X_NL_SC70-5
CLKREQ#
CLKREQ_NEW#
CLKREQ_NEW# 29
RCLKEN
Q6B 2N7002DW-T/R7_SOT363-6 another at page46
CLKREQ# RN8 0_0402_5% CLKREQ_NEW#

Reserve for EMI request
RN25 0_0402_5%
WCM-2012-900T_0805 LN1
32 USB20_P4 → USB20_P4_R
32 USB20_N4 → USB20_N4_R
RN24 0_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.
Title: PCIe-WLAN/3G/JET/NEW
Size | Document Number: NBQAA LA6072P M/B | Rev: 1.0
Date: Tuesday, March 23, 2010 | Sheet 39 of 61



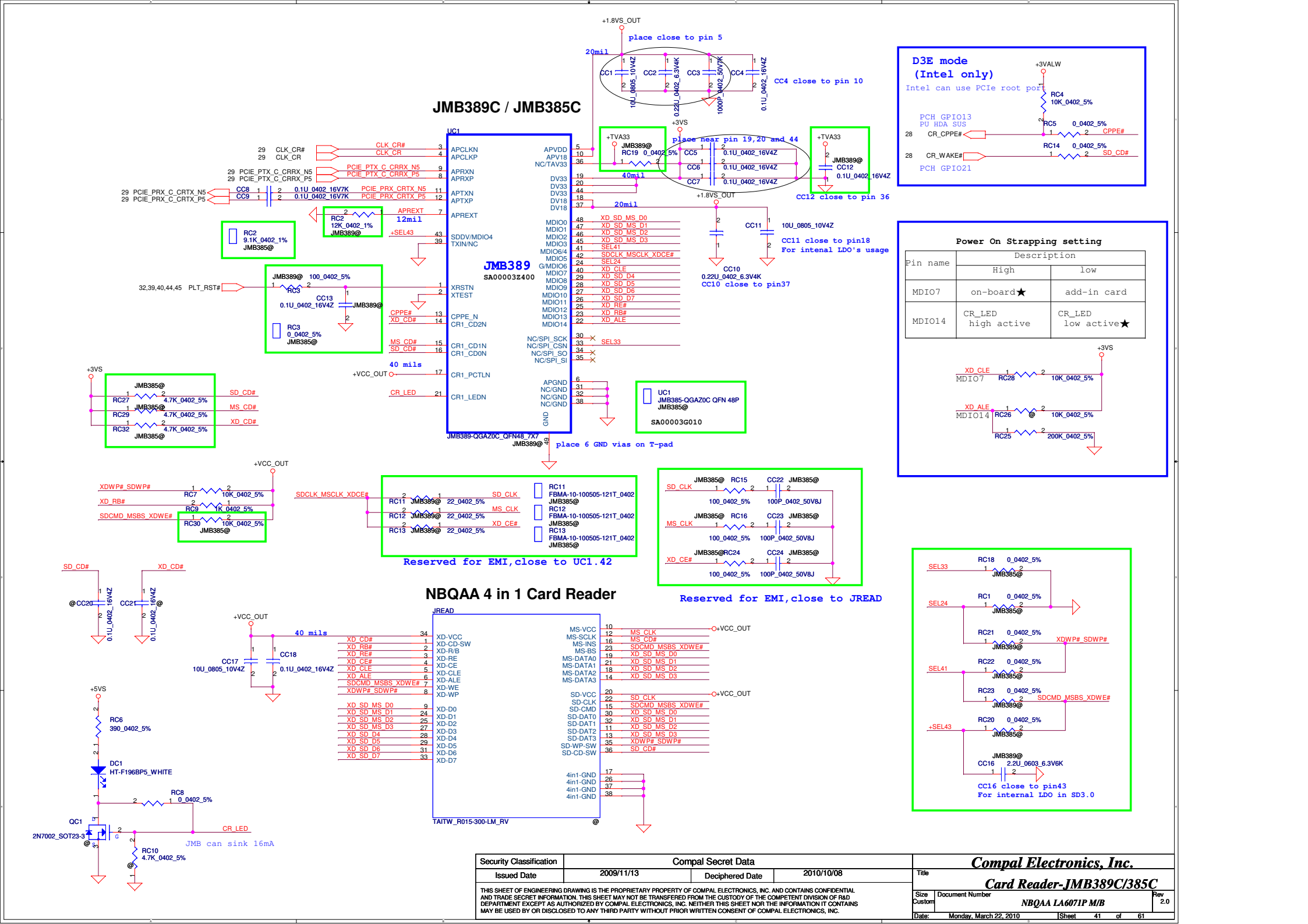
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/02/02

Compal Electronics, Inc.

Title: RTL8105E/RTL8111E

Size | Document Number: NBQAA LA6072P M/B | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 40 of 61



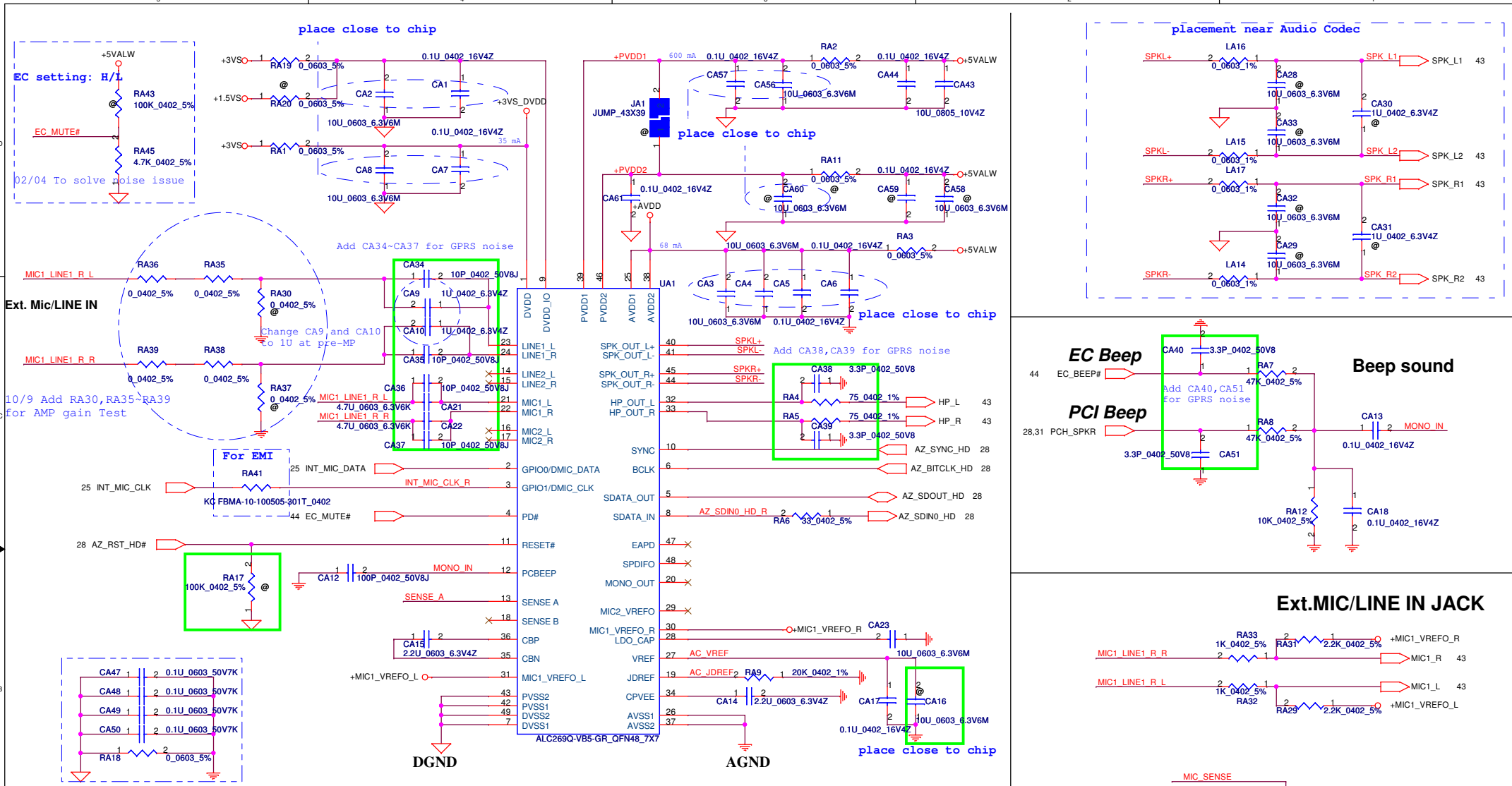
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/10/08

Compal Electronics, Inc.

Title: **Card Reader-JMB389C/385C**

Size	Document Number	Rev
Custom	NBQAA LA6071P M/B	2.0

Date: Monday, March 22, 2010 Sheet 41 of 61



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

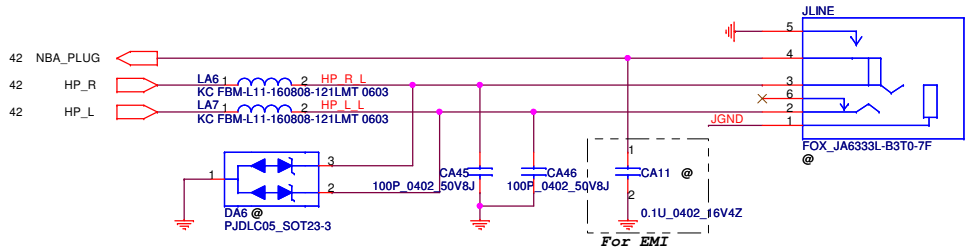
Compal Electronics, Inc.

Title: HDA CODEC ALC269

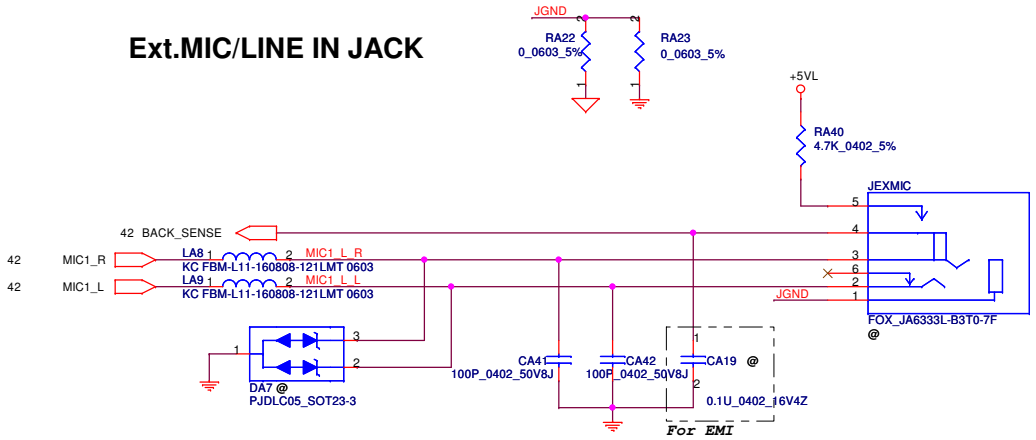
Size | Document Number: NBQAA LA6072P M/B | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 42 of 61

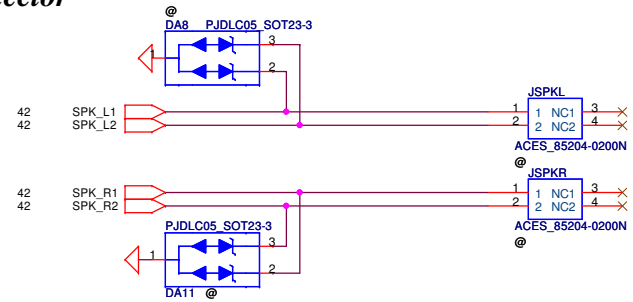
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK

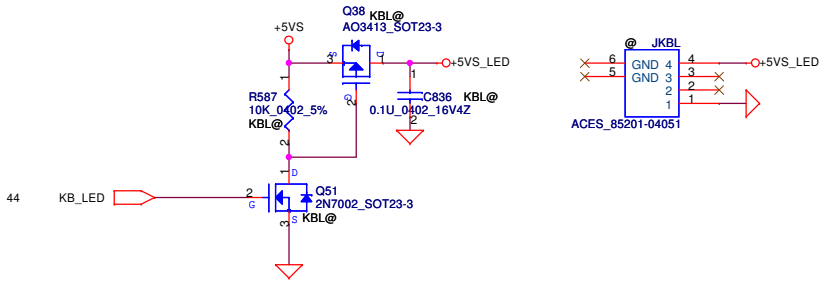


Speaker Connector

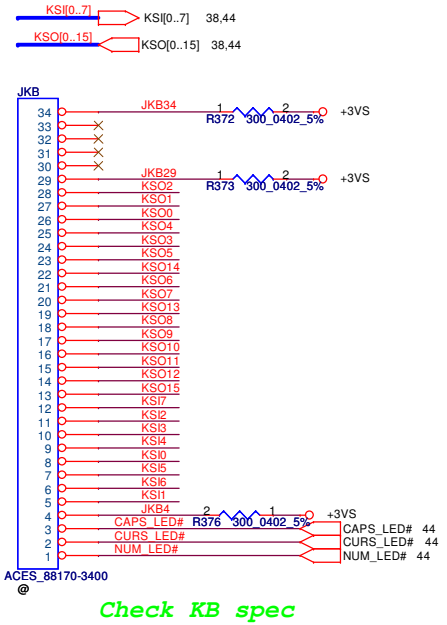


Need to update symbol

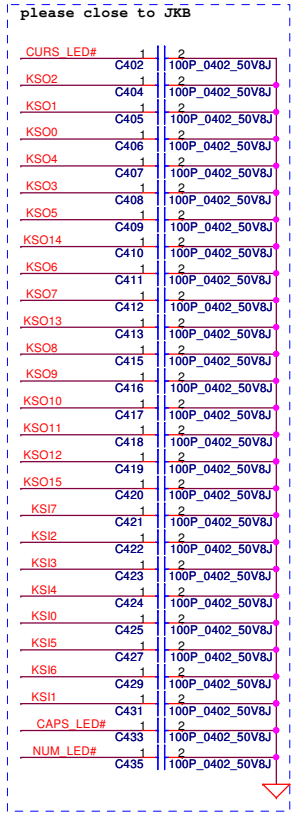
Keyboard LED



KEYBOARD CONN.

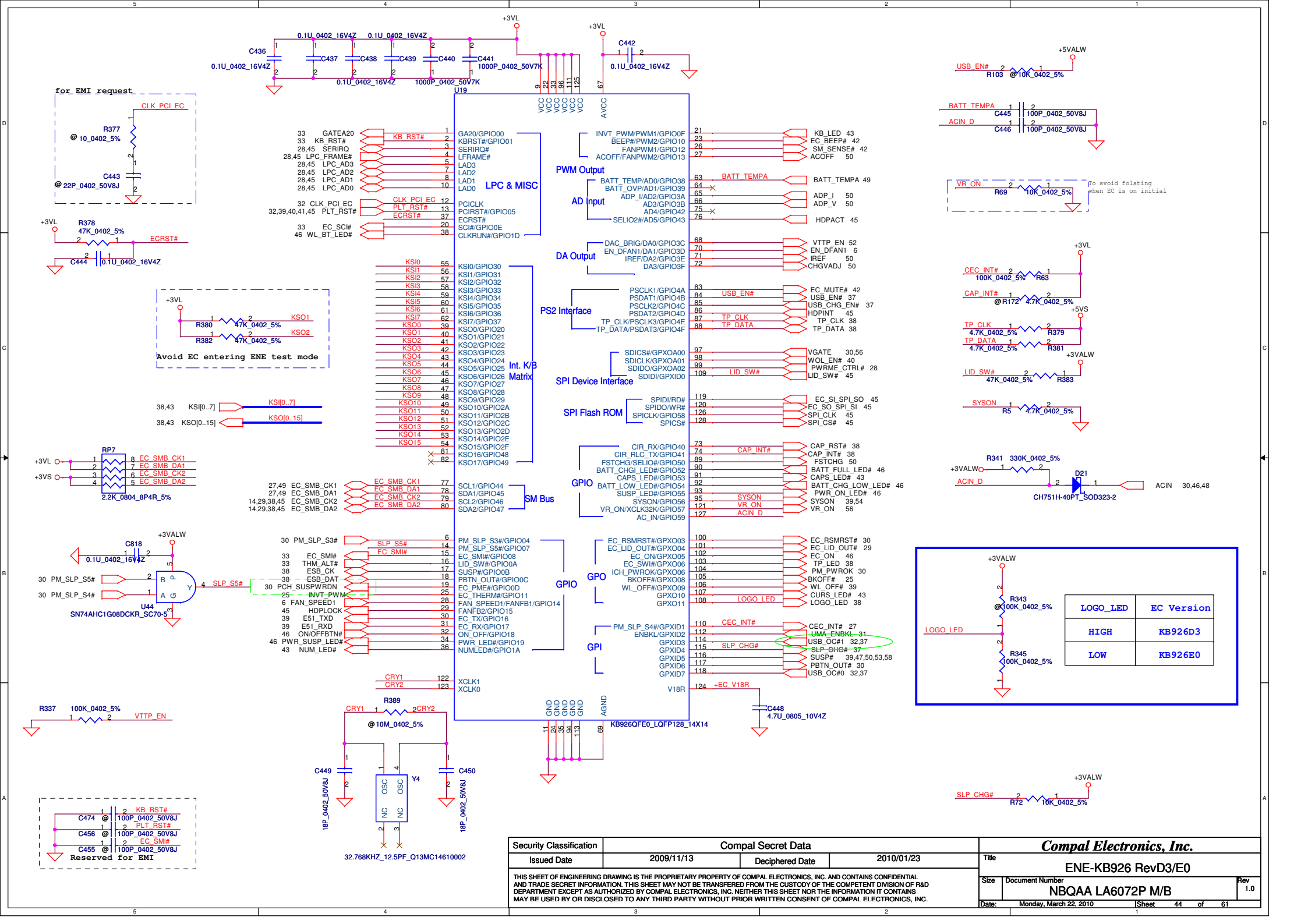


Check KB spec



Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title	AUDIO/KB CONN		
Size	Document Number	NBQAA LA6072P M/B	Rev 1.0
Date: Tuesday, March 23, 2010	Sheet 43 of 61		



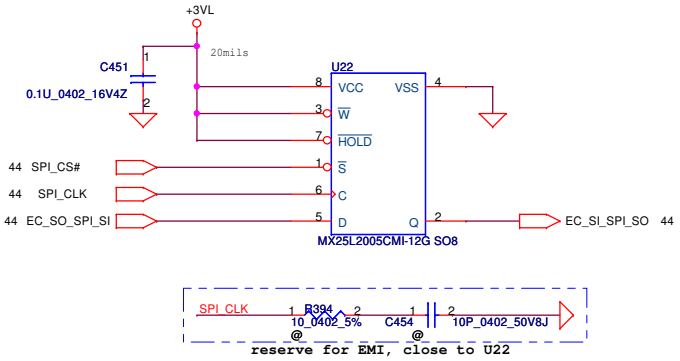
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

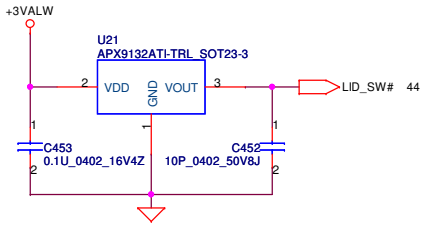
Title	ENE-KB926 RevD3/E0
Size	Document Number: NBQAA LA6072P M/B
Rev	1.0
Date:	Monday, March 22, 2010
Sheet	44 of 61

SPI Flash (256KB)

Socket: SP07000F500 & SP07000H900

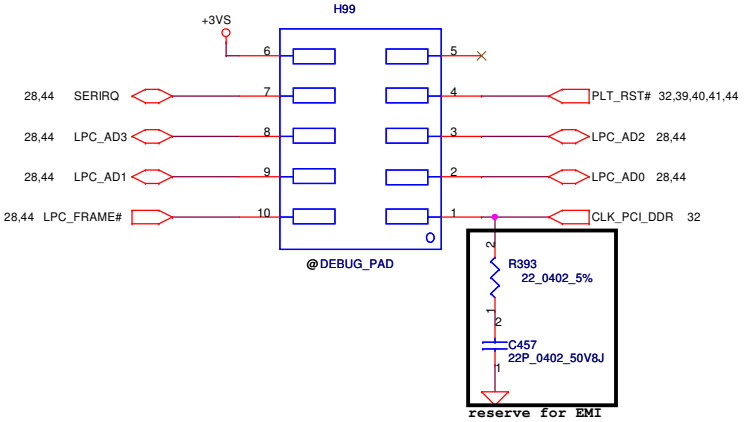


Lid SW

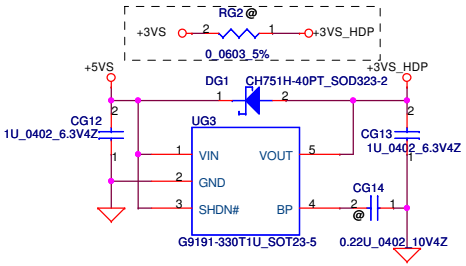


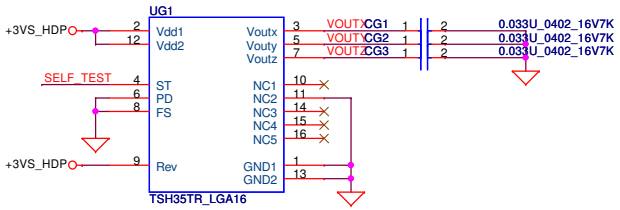
LPC Debug Port

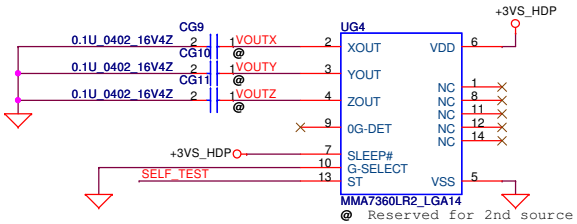
Please place the PAD under DDR DIMM.



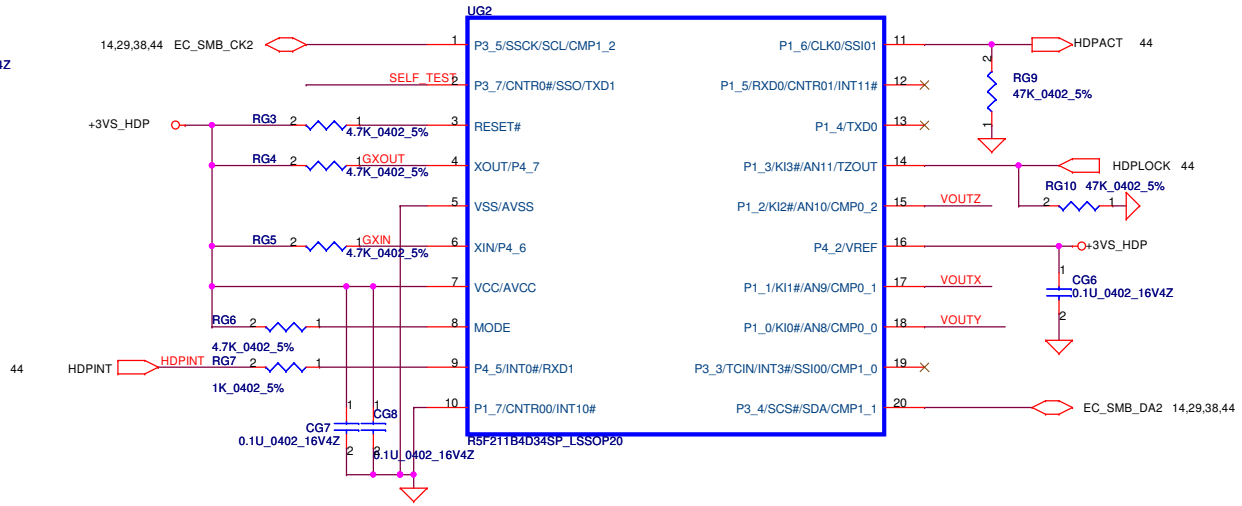
G-Sensor







SA00003A600 Supports ODD unexpected tray eject prevention



Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

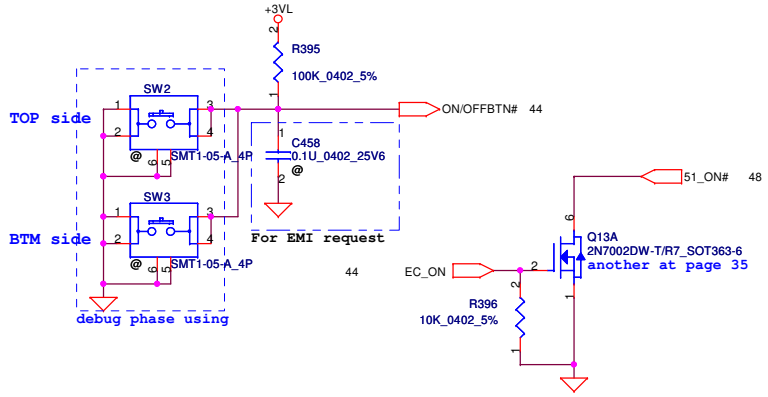
Compal Electronics, Inc.

Title: SPI ROM/G-SENSOR/Debug

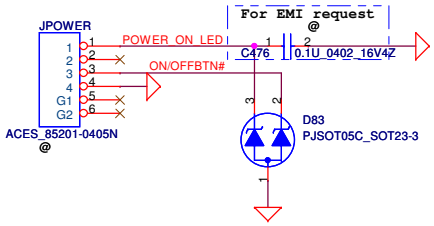
Size | Document Number: NBQAA LA6072P M/B | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 45 of 61

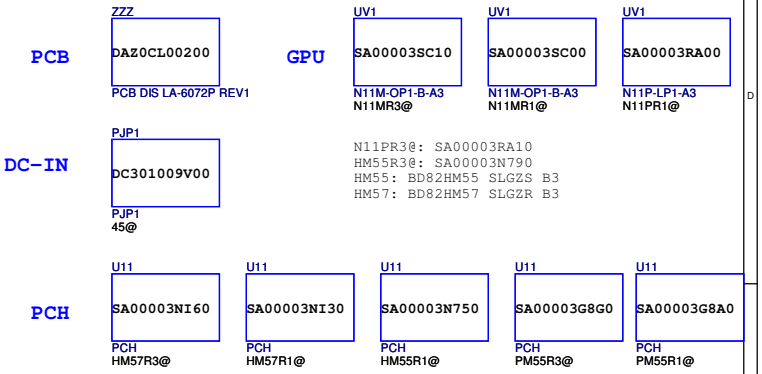
Power Button



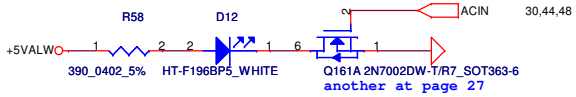
PWR/B Conn



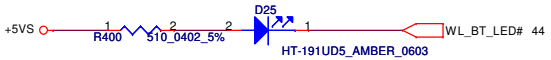
ISPD



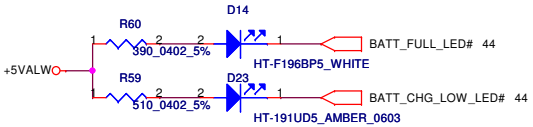
DC-IN LED



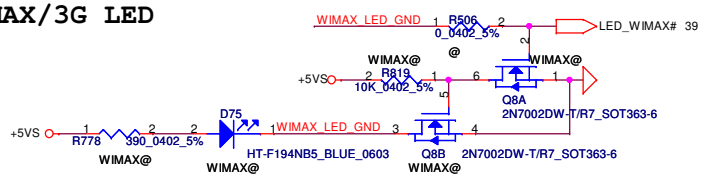
WL/BT LED



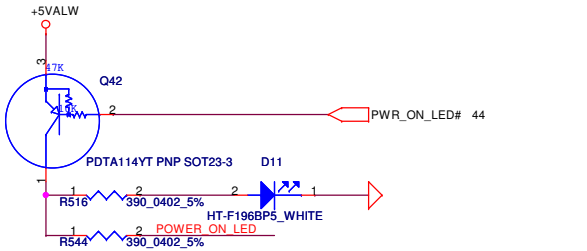
BATT CHARGE/FULL LED

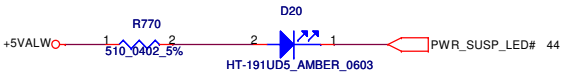


WiMAX/3G LED

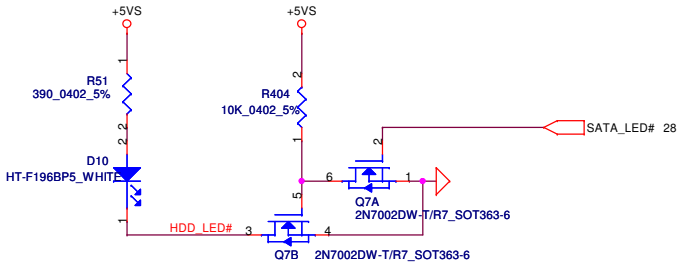


POWER/SUSPEND LED

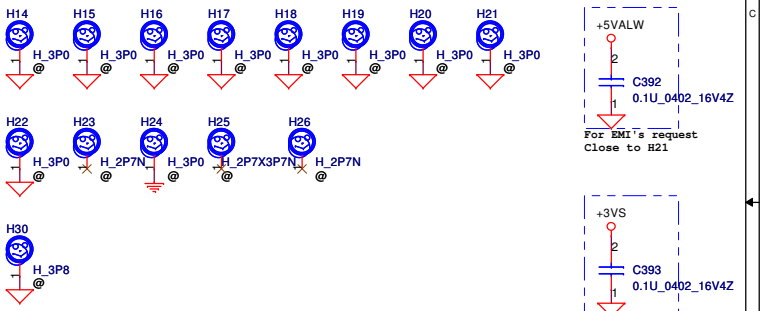




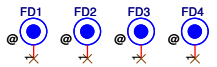
HDD LED



Screw Hole



PCB Fedical Mark PAD



Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

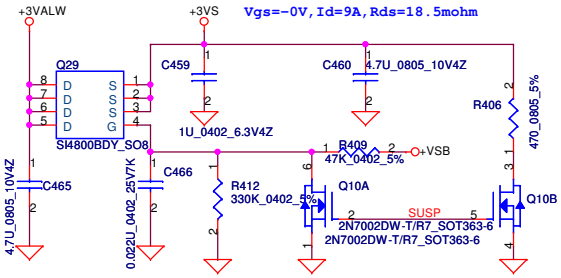
Compal Electronics, Inc.

Title: Comm. SW/ Sub Conn./LEDS

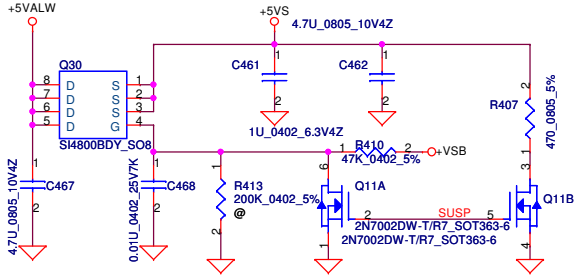
Size	Document Number	Rev
	NBQAA LA6072P M/B	1.0

Date: Tuesday, March 23, 2010 Sheet 46 of 61

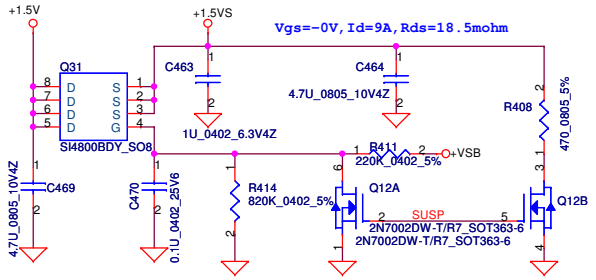
+3VALW TO +3VS



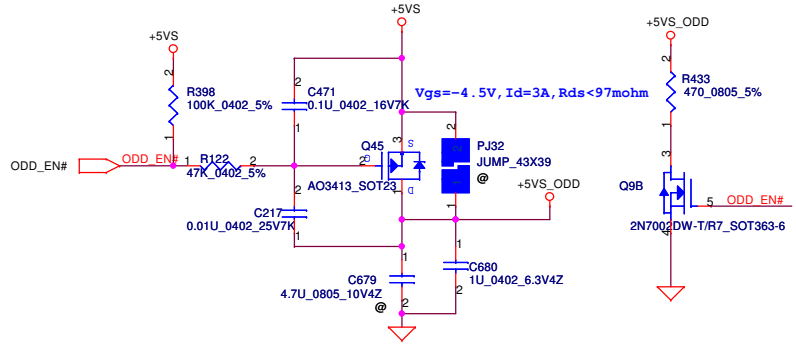
+5VALW TO +5VS



+1.5V to +1.5VS

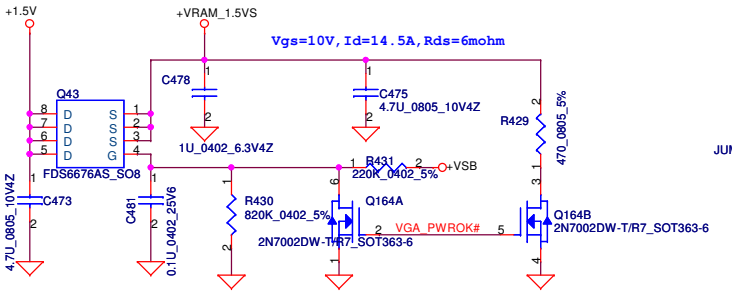


+5VS TO +5VS_ODD



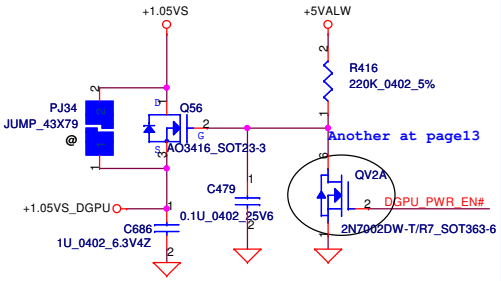
+1.5V to +VRAM_1.5VS

(11A,440mils ,Via NO.= 22)



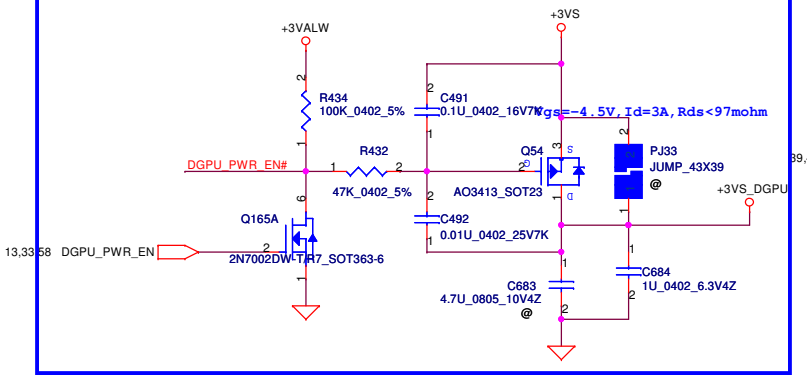
+1.05VS to +1.05VS_DGPU

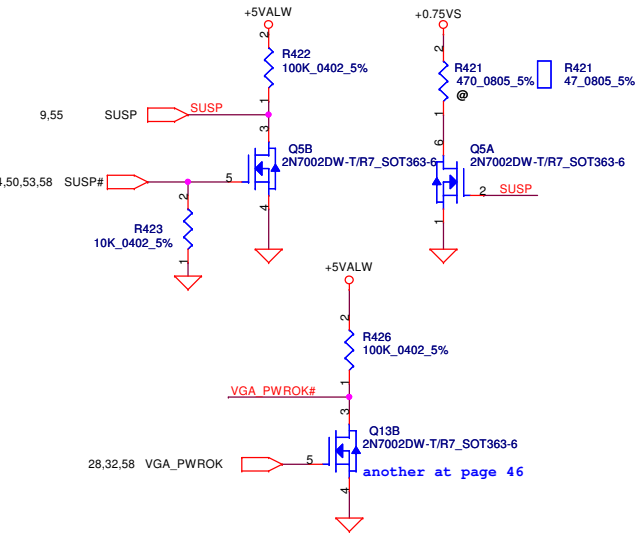
(2.87A,120mils ,Via NO.= 6)



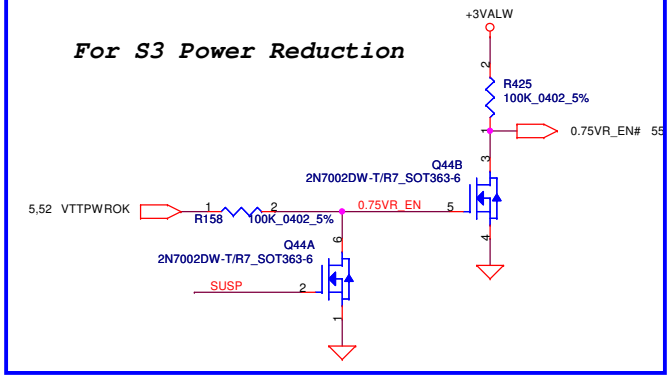
+3VS to +3VS_DGPU

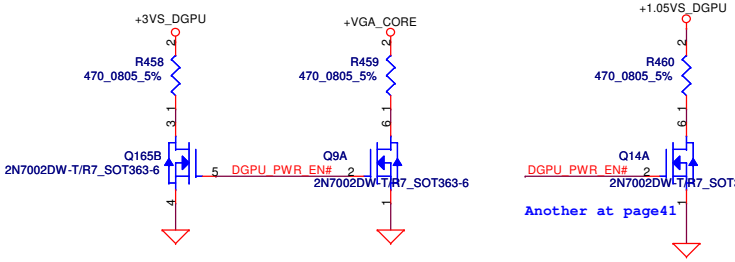
(780mA,40mils ,Via NO.= 2)





For S3 Power Reduction





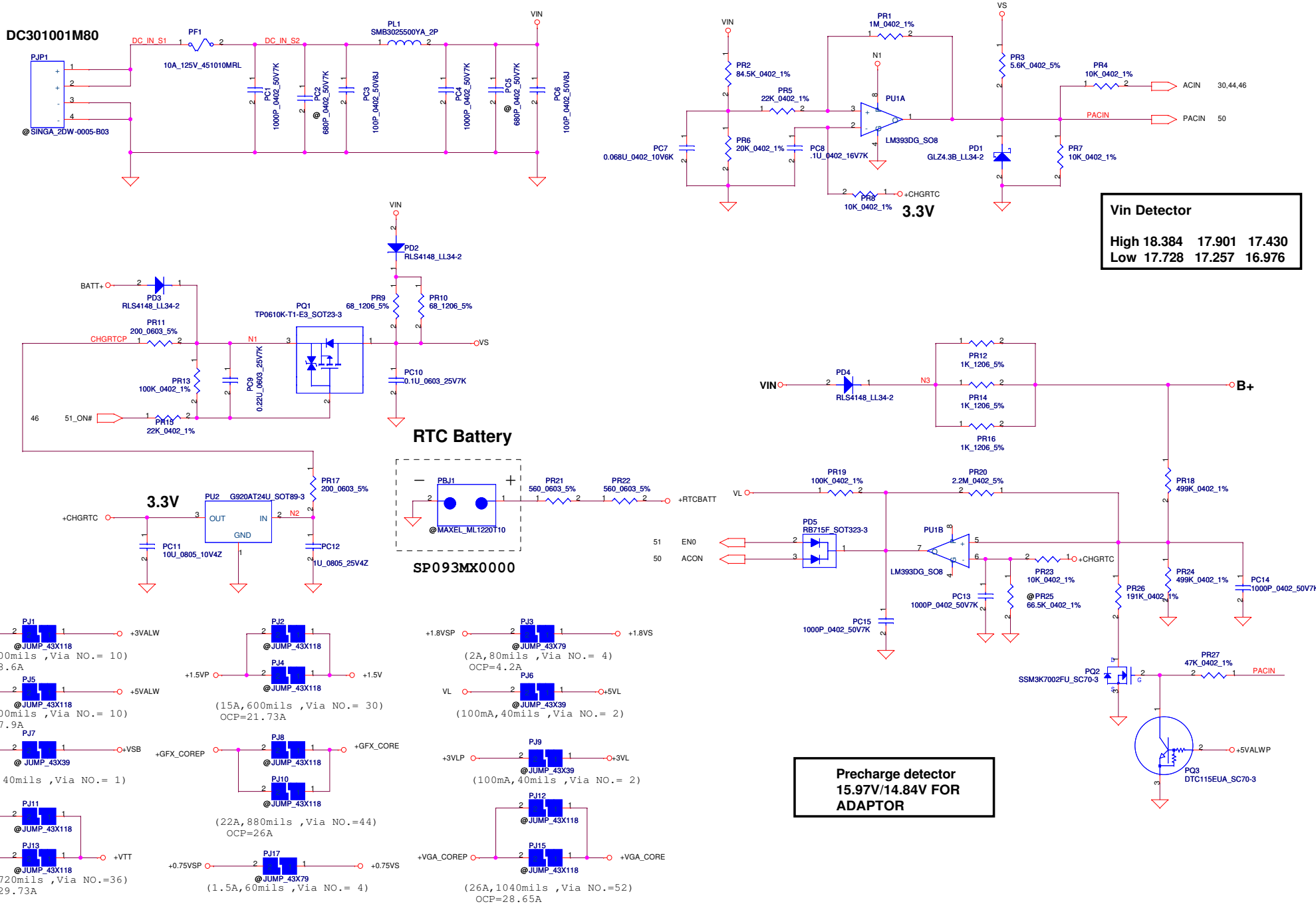
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size	Document Number	Rev
	NBQAA LA6072P M/B	1.0

Date: Monday, March 22, 2010 Sheet 47 of 61

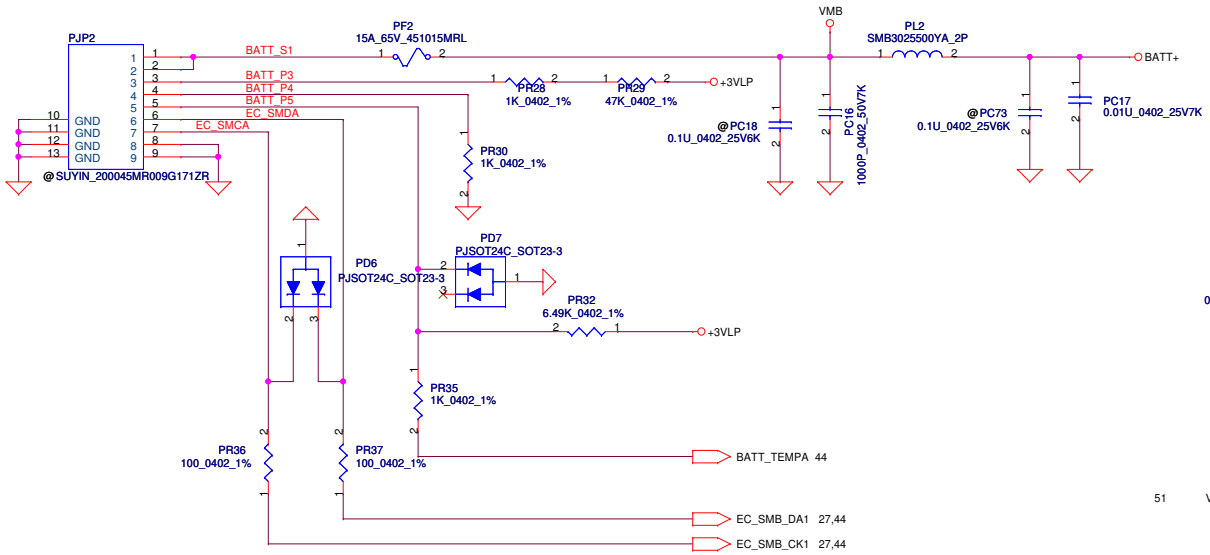


Compal Electronics, Inc.

Title: DCIN / DETECTOR

Size | Document Number: NBQAA DIS | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 48 of 61



PH1 under CPU botten side :

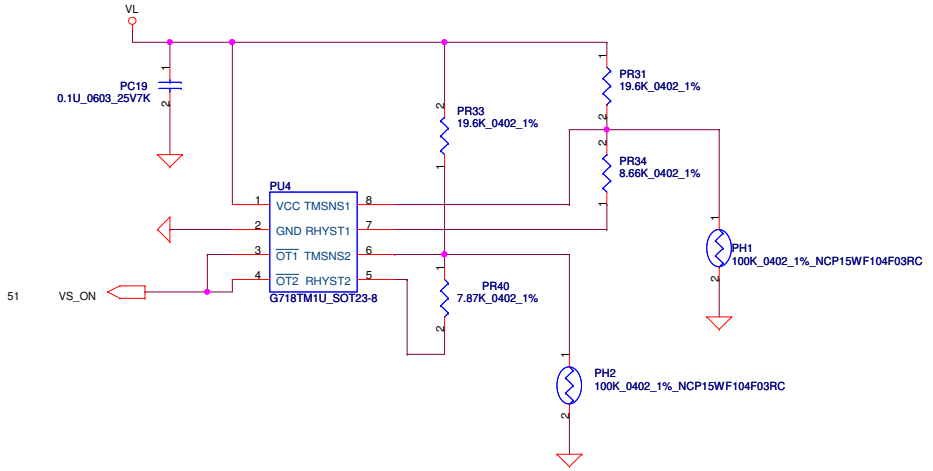
CPU thermal protection at 95 degree C

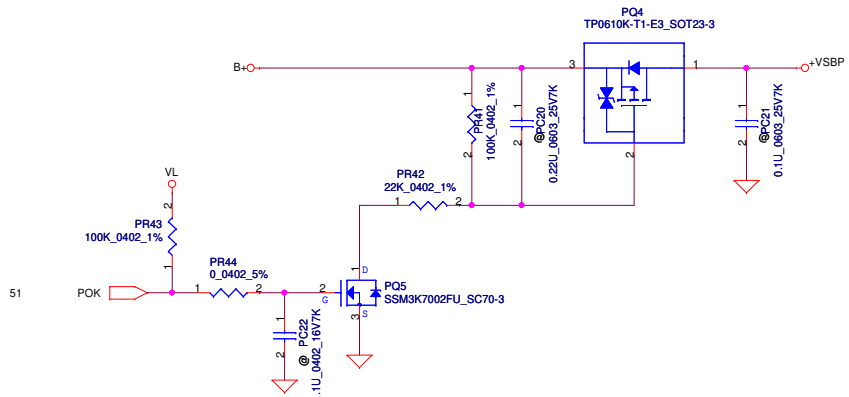
Recovery at 56 degree C

PH2 near main Battery CONN :

BAT. thermal protection at 95 degree C

Recovery at 48 degree C





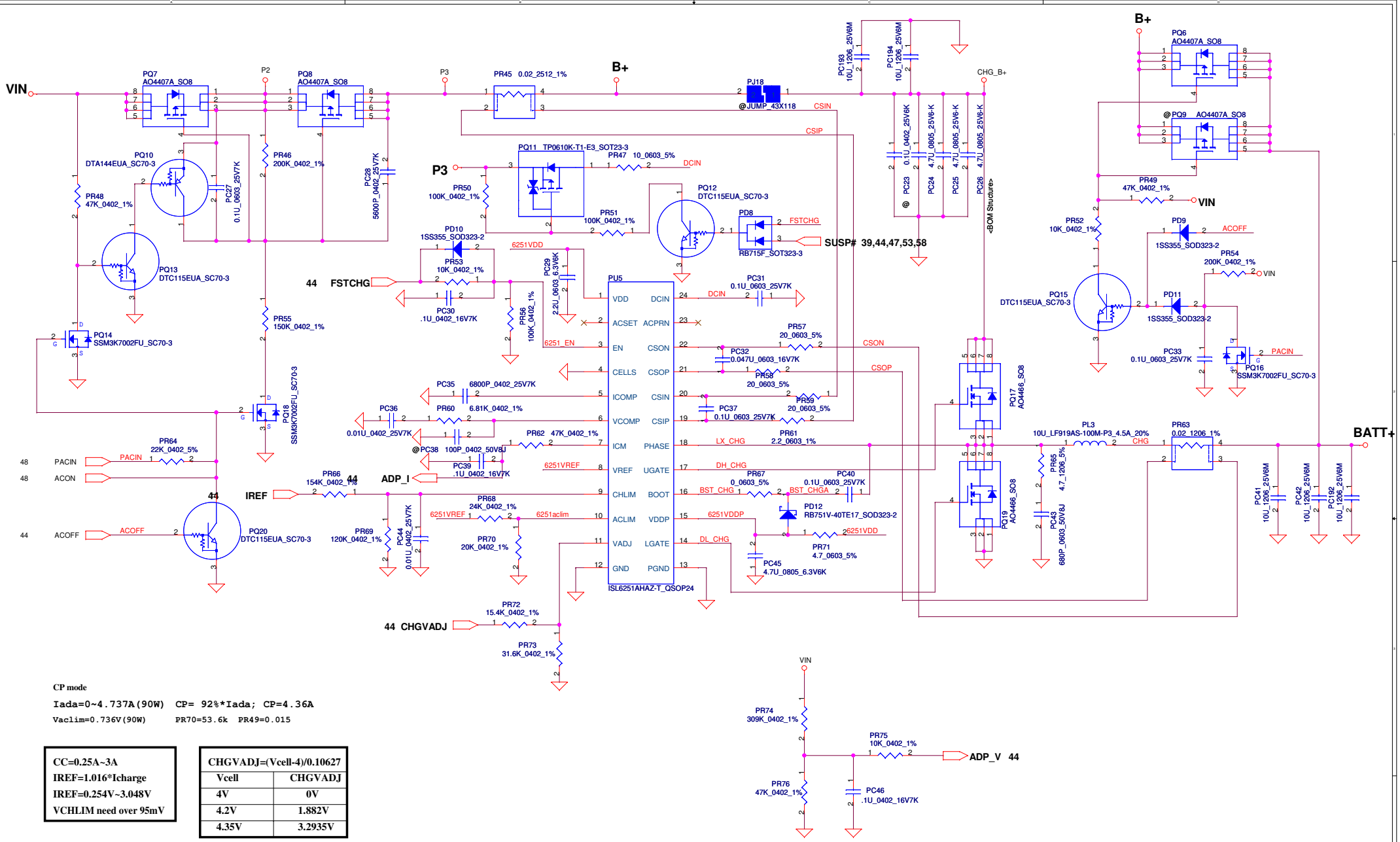
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/10/21

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
	NBQAA	1.0

Date: Monday, March 22, 2010 | Sheet 49 of 61



CP mode

`Iada=0~4.737A(90W)  CP= 92%*Iada; CP=4.36A`

`Vaclim=0.736V(90W)  PR70=53.6k  PR49=0.015`

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

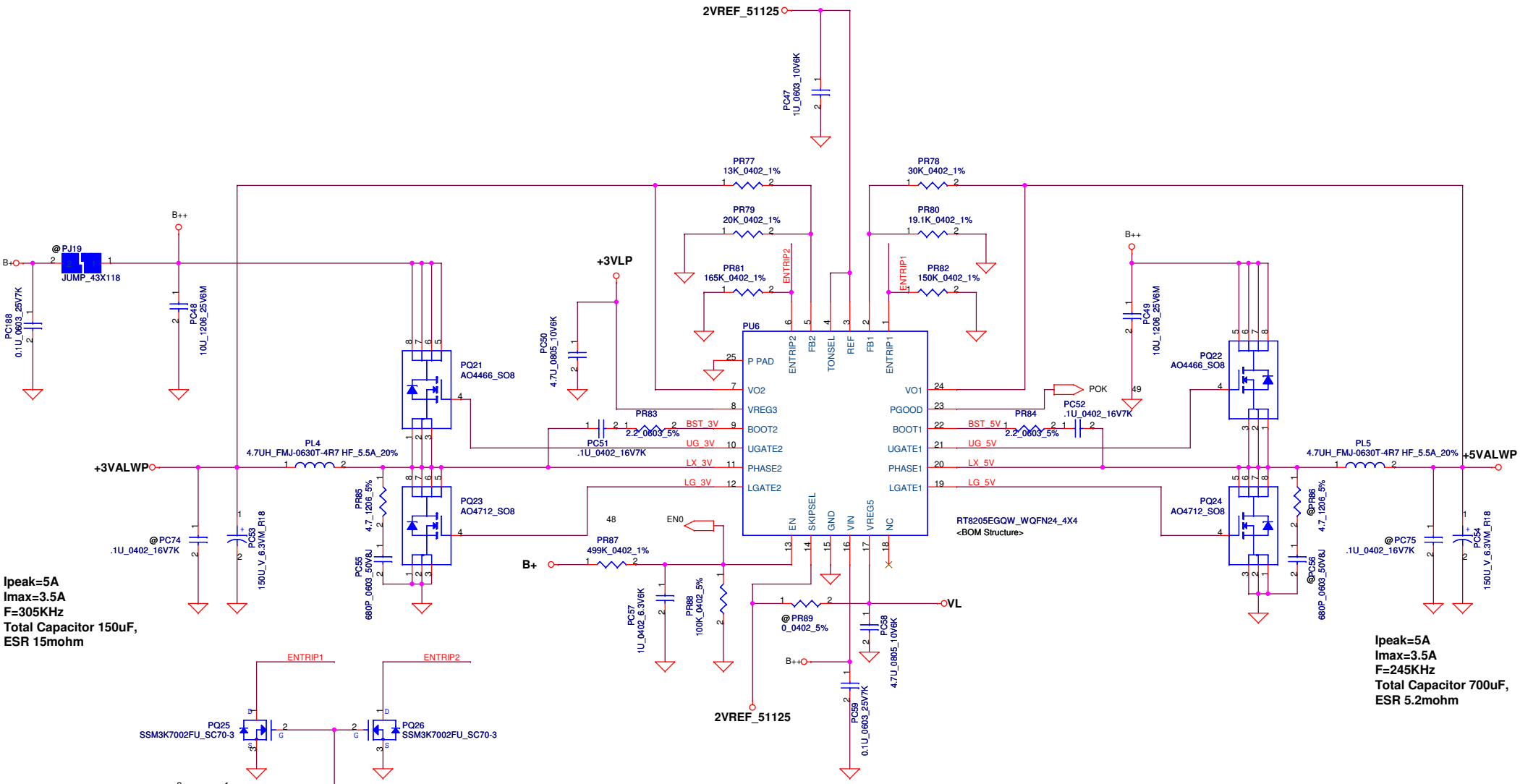
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/10/21

Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
	NBQAA	1.0

Date: Monday, March 22, 2010 | Sheet 50 of 61



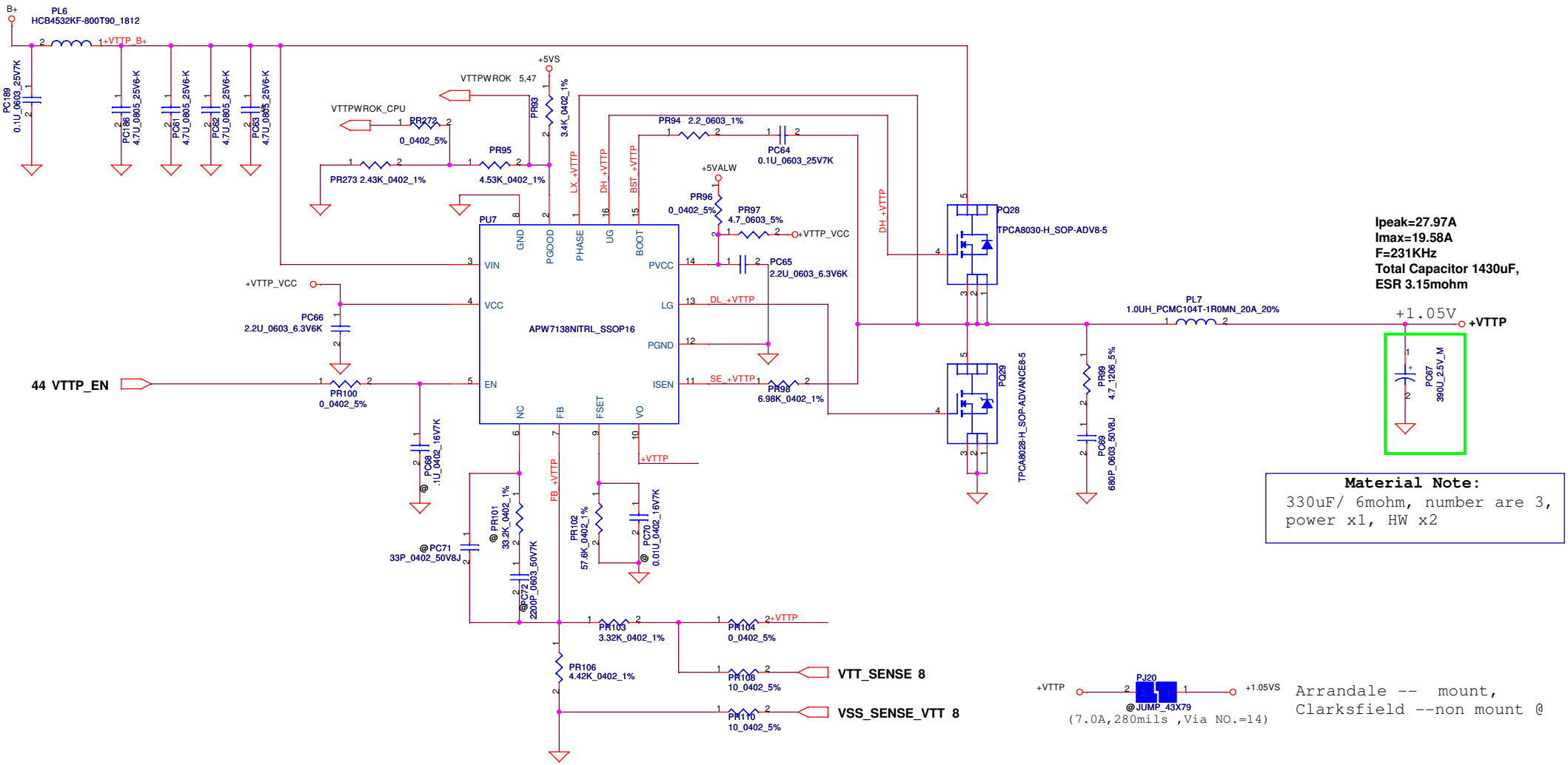
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/10/21

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
	NBQAA	1.0

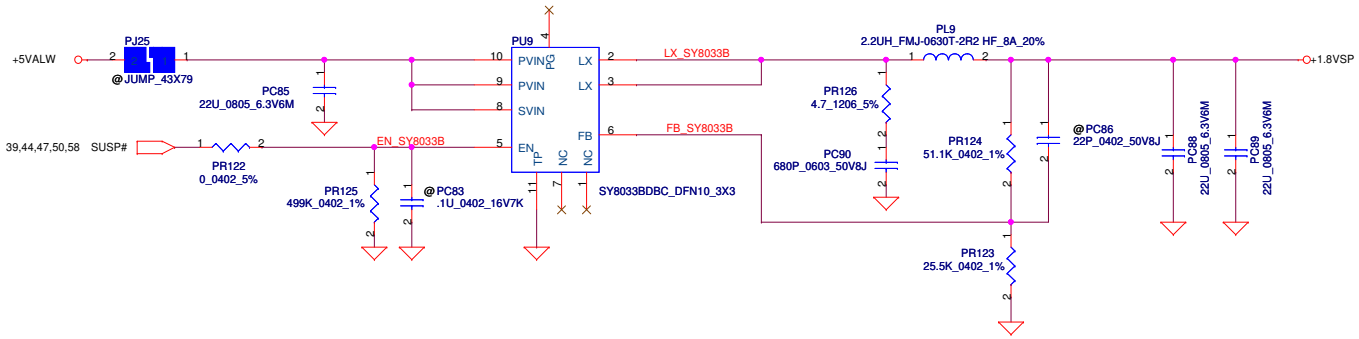
Date: Monday, March 22, 2010 | Sheet 51 of 61



Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/10/21

Compal Electronics, Inc.

Title	+VTTP	
Size	Document Number: NBQAA LA6072P M/B	Rev: 1.0
Date: Monday, March 22, 2010	Sheet 52 of 61	



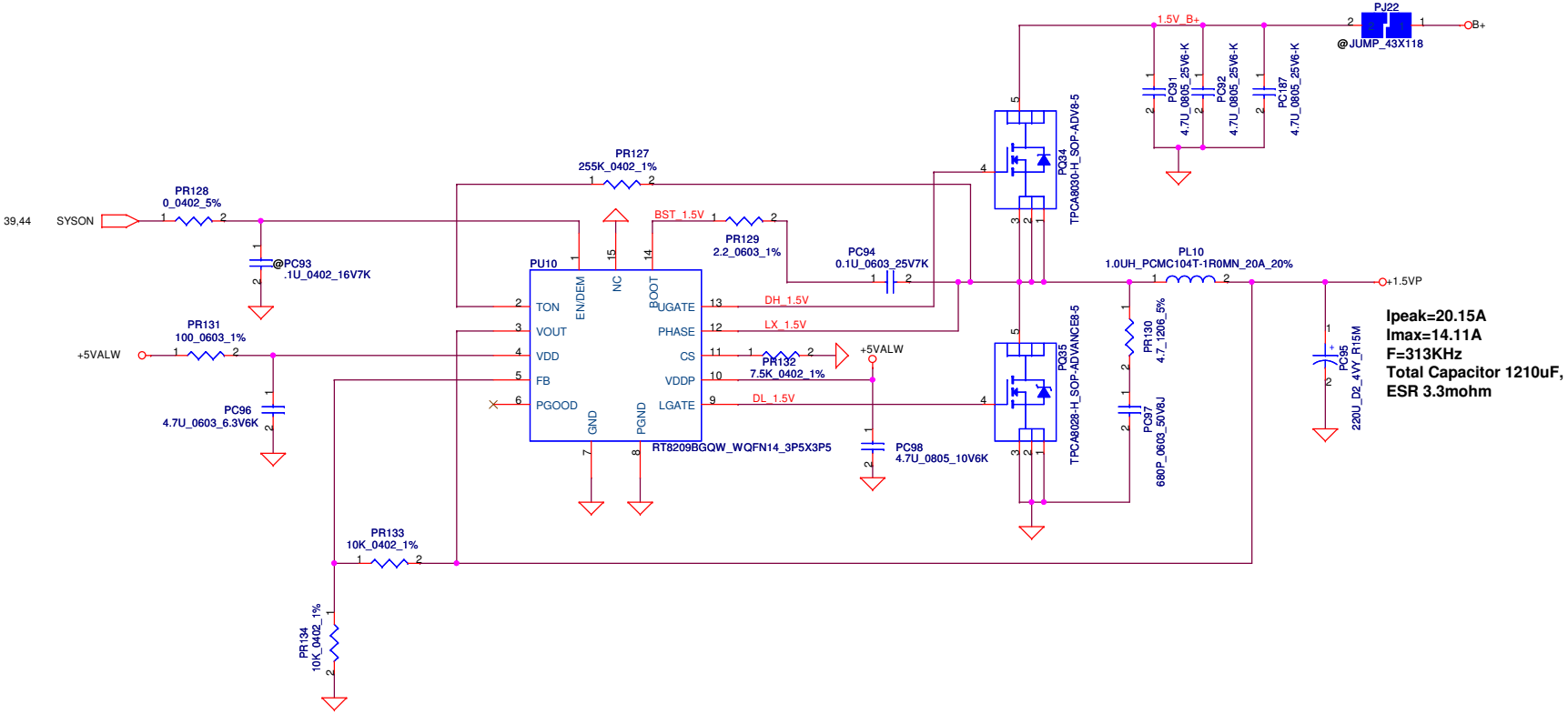
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/10/21

Compal Electronics, Inc.

Title: +1.8VSP

Size	Document Number	Rev
	NBQAA	1.0

Date: Monday, March 22, 2010 | Sheet 53 of 61



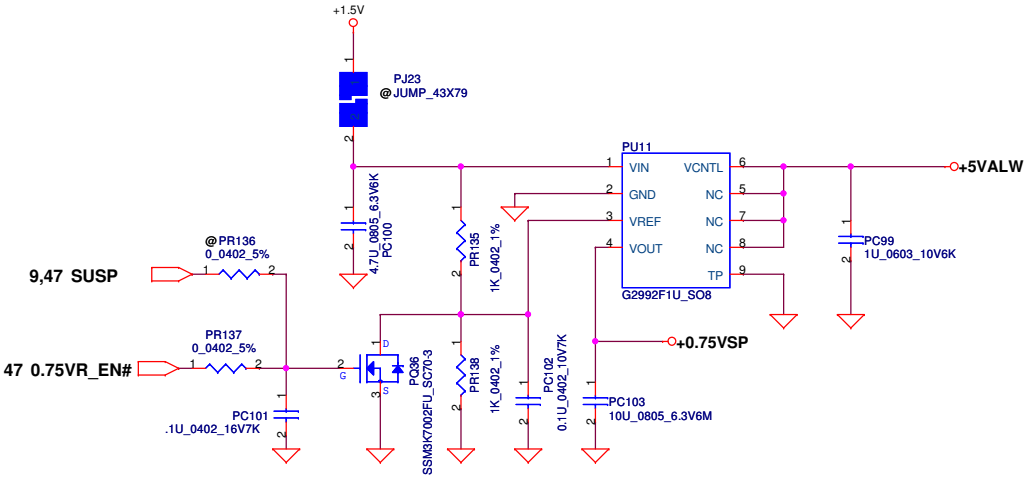
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/10/21

Compal Electronics, Inc.

Title: **+1.5VP**

Size	Document Number	Rev
Custom	NBQAA LA6072P M/B	1.0

Date: Monday, March 22, 2010 | Sheet 54 of 61



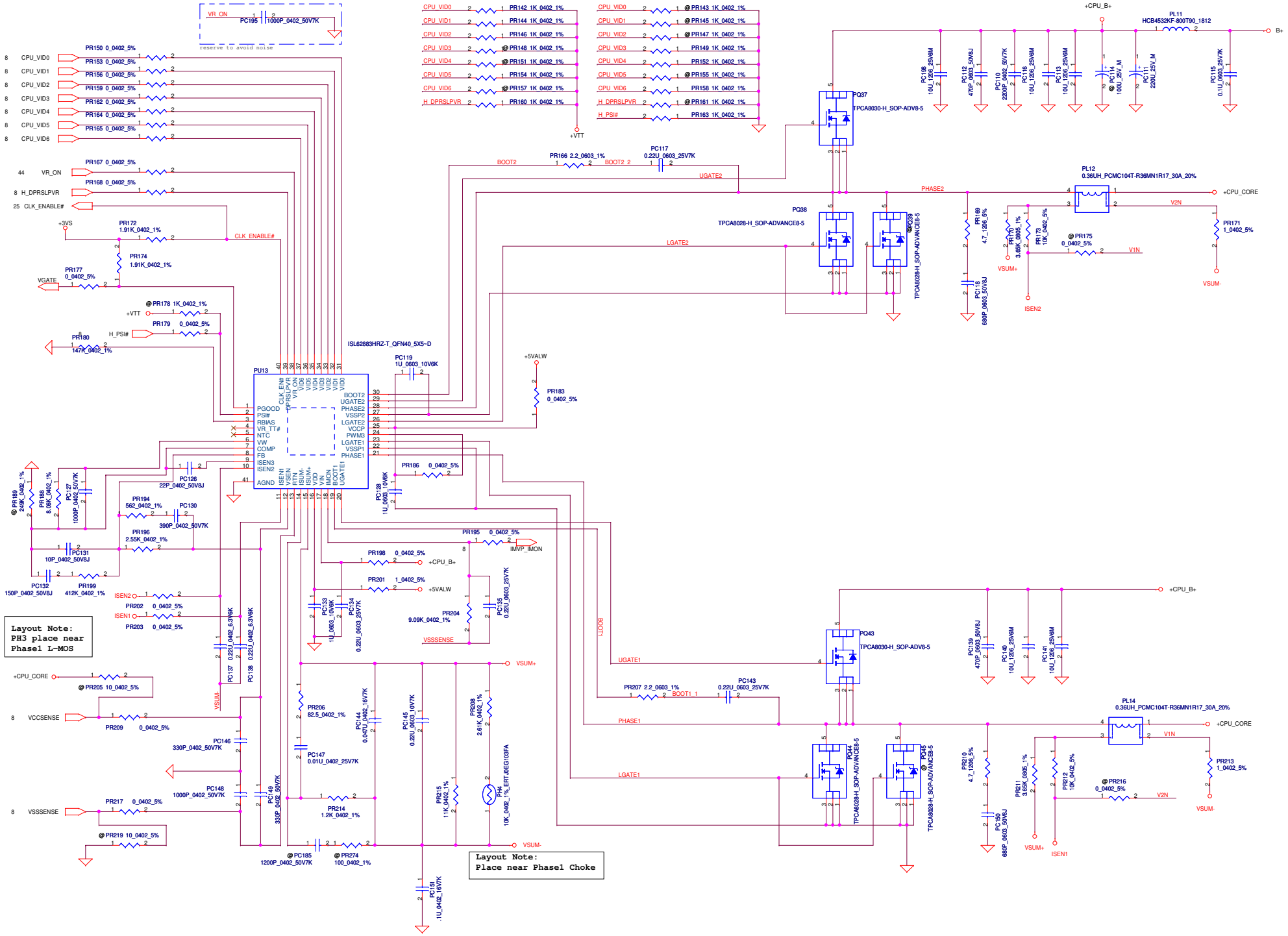
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/10/21

Compal Electronics, Inc.

Title: 0.75VSP/

Size | Document Number: NBQAA LA6072P M/B | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 55 of 61



Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/10/21

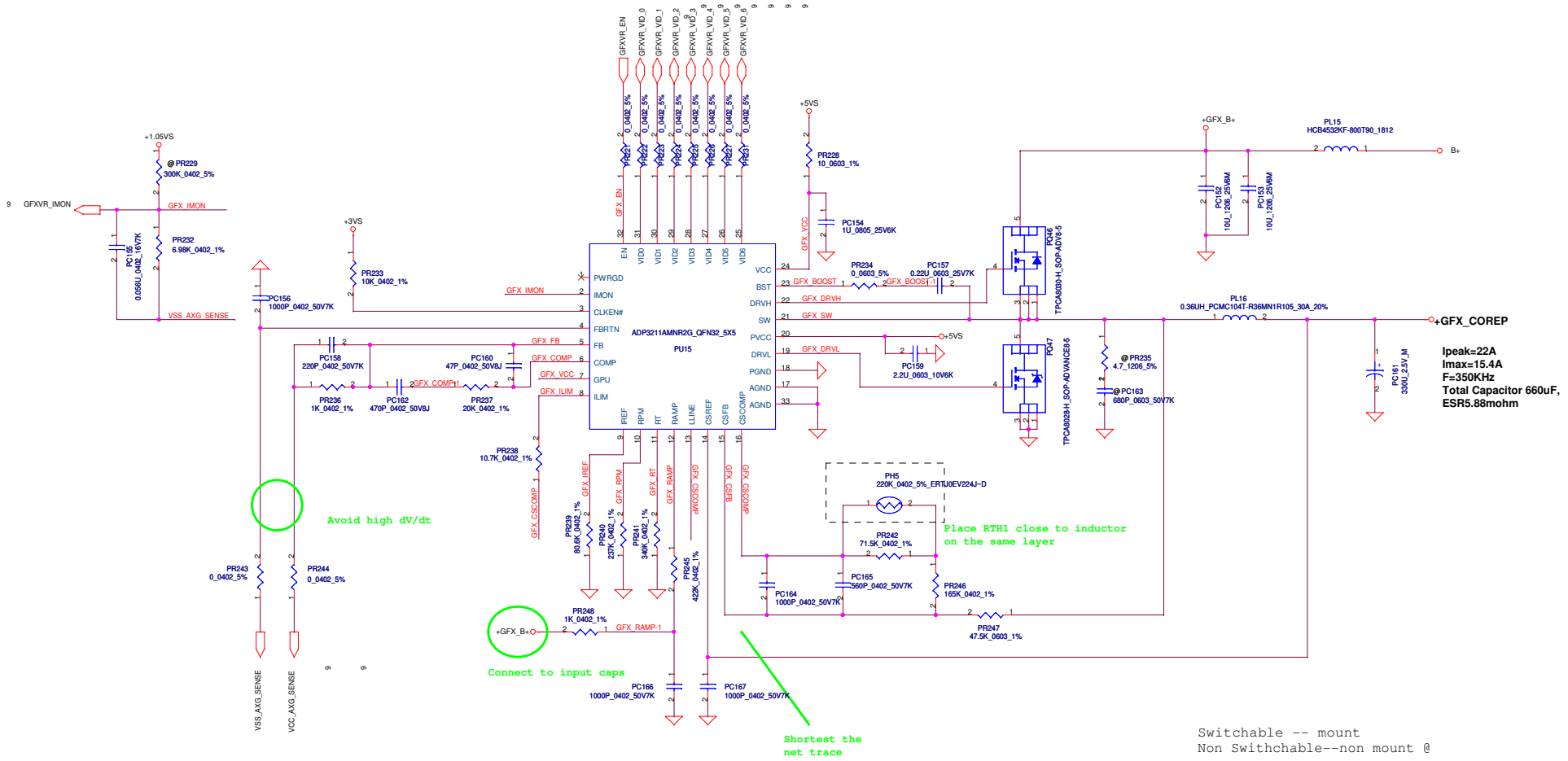
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: +CPU_CORE

Size	Document Number	Rev
C	NBQAA LA6072P M/B	1.0

Date: Monday, March 22, 2010 Sheet 56 of 61



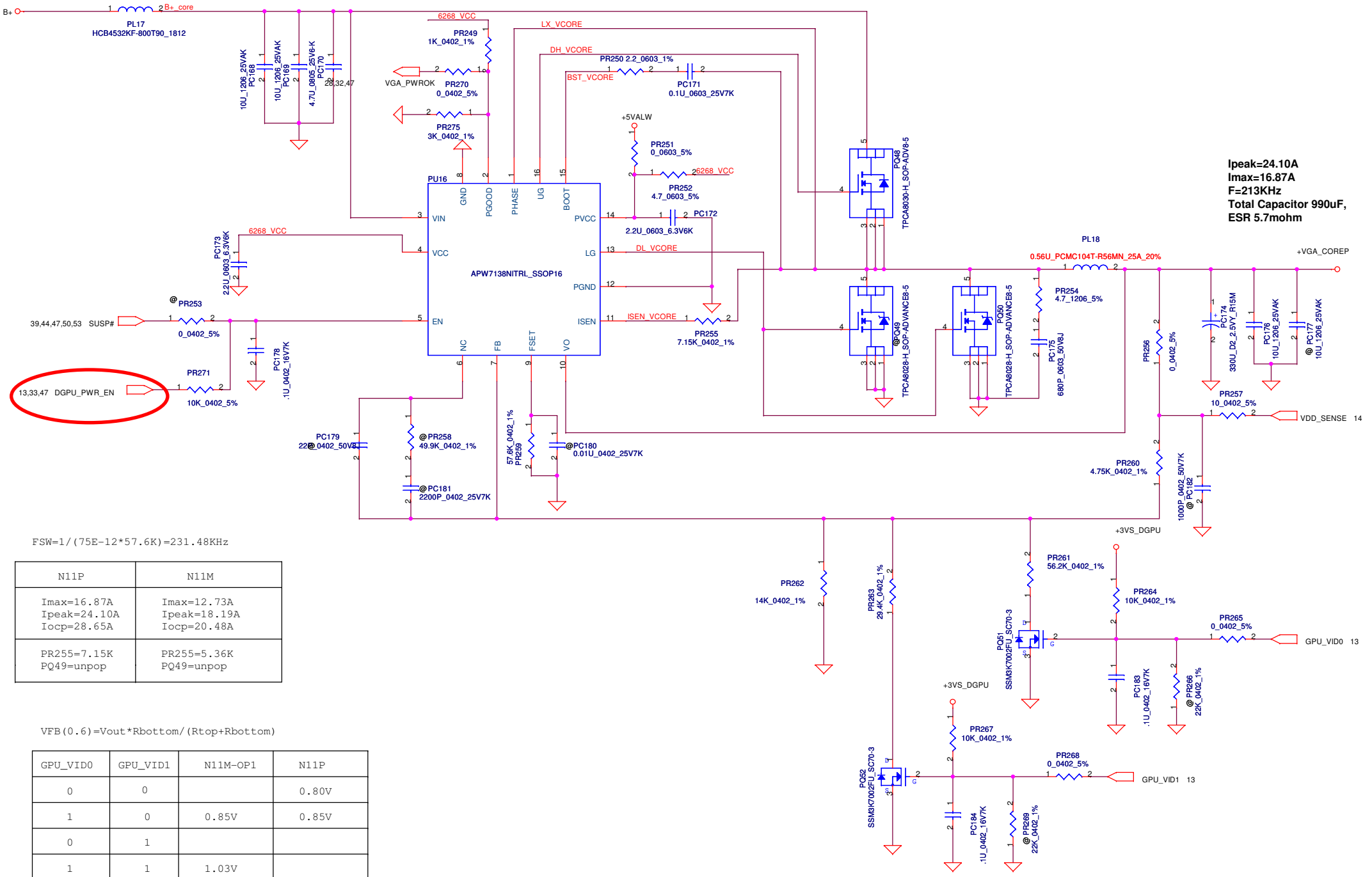
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/10/21

Compal Electronics, Inc.

Title: +GFX_COREP

Size	Document Number	Rev
	NBQAA LA6072P M/B	1.0

Date: Monday, March 22, 2010 | Sheet 57 of 61



Ipeak=24.10A
Imax=16.87A
F=213KHz
Total Capacitor 990uF,
ESR 5.7mohm

FSW=1/(75E-12*57.6K)=231.48KHz

N11P	N11M
Imax=16.87A Ipeak=24.10A Iocp=28.65A	Imax=12.73A Ipeak=18.19A Iocp=20.48A
PR255=7.15K PQ49=unpop	PR255=5.36K PQ49=unpop

VFB(0.6)=Vout*Rbottom/(Rtop+Rbottom)

GPU_VID0	GPU_VID1	N11M-OP1	N11P
0	0		0.80V
1	0	0.85V	0.85V
0	1		
1	1	1.03V	
		PR260= 4.75K PR262 =14K PR261 =56.2K PR263=16.2K	PR260= 4.75K PR262 =14K PR261 =56.2K PR263=29.4K

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/10/21

Compal Electronics, Inc.

Title	+VGA_COREP		
Size: Custom	Document Number: NBQAA LA6072P M/B		Rev: 1.0
Date: Monday, March 22, 2010	Sheet 58 of 61		

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	2009/12/06	P48-59	Release	
	2009/12/18	P49	PR31,PR33,PR34,PR40	PH1,PH2 setting point change
	2009/12/18	P52	PR98	VTT adjust OCP
	2009/12/18	P55	Remove PR136,Add PR137,PC101	0.75VSP Enable signal (EVT added by memo)
	2009/12/18	P58	Add PR254,PC175	VGA add snubber (EVT added by memo)
	2009/12/18	P58	PC174	VGA output cap change to lower
	2009/12/28	P51,P52	Add PC188,PC189,PC115	Add EMC,EMI solution.
	2009/12/28	P51	change PR83,PR84,Add PR85,PC55	For EMI,EMC solution
	2010/01/06	P51	PR81,PR132,PR255	OCP setting.
	2010/01/06	P58	change PR249,PR271,PC178	HW request
	2010/02/05	P53	change PU9 solution	change 1.8V Solution
	2010/02/05	P51	change PL4,PL5	Change to lower height to solve ME request
	2010/01/28	P43	PC197	Reserve 10uF at B+ shape for ripple improvement.
	2010/02/08	P50	Add PD6,PD7	ESD solution.
	2010/02/08	P57	Change PR247	GFX load-line
	2010/02/08	P50	Add PC192,PC193,PC194	ISN issue
	2010/03/16	P50	Change PR45,PR68	CP setting
	2010/03/16	P50	Change PL3	ME issue
	2010/03/16	P51	Change PC53,PC54	ME issue
	2010/03/16	P53	PR122,PC83 unmount	1.8V enable signal adjust
	2010/03/16	P56	Add PC195	VR_ON prevent noise,same as UMA
	2010/03/16	P58	Change PC174	ME issue
	2010/03/16	P58	Change PR264,PR265,PR267,PR268,PR263,PC184,PQ52	GPU voltage adjust
	2010/03/18	P57	Add PC198	High frequency noise
	2010/03/22	P58	Add PR275	Adjust VGA POK voltage level for HW request

PIR (Product Improve Record)

NBQAA LA-6072P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	12/22	25	Change JLVDS routing	To prevent workmanship and burn issue
2.	12/22	09	Change Q33 routing	For common design
3.	12/22	47	Change Q43 routing	For common design
4.	12/22	39	Change JEXP footprint to SANTA_130861-2_26P_RT-T	Modify footprint
5.	12/22	38	Change JTPL footprint to P-TWO_161021-06021_6P-T	For ME's request
6.	12/22	43	Change JKBL footprint to ACES_85201-04051_4P-T	For ME's request
7.	12/22	13	Delete DV2, Add RV124, QV2 for CLKREQ_VGA#	CLKREQ_VGA# circuit for NV's Optimus
8.	12/23	38	Change JCS footprint to P-TWO_161021-10021_10P-T	For ME's request
9.	12/23	38	Change JTOUCH footprint to P-TWO_161021-10021_10P-T	For ME's request
10.	12/23	33	Change PCH's GPIO57 netname to OPTIMUS_EN# and pull down to GND	For BIOS recognizing Optimus
11.	12/23	33	Change PCH's GPIO45 netname to LVDS_SEL	For Common design
12.	12/23	33	Change PCH's GPIO39 netname to CIR_EN#	For Common design
13.	12/24	39	Add DM2, QM1, BT_CTRL on JWLAN.5	For WLAN/BT combo module
14.	12/24	42	Add RA43 on EC_MUTE#	For Audio issue
15.	12/24	43	Detele JEXMIC.5 from GND	For Audio issue
16.	12/24	44	Change PWRME_CTRL to PWRME_CTRL#	Active low signal
17.	12/24	33	Delete GND guide pins of JTOUCH, JCS, JTPL, JODD1	For common design
18.	12/29	29	Add C254 on CLKREQ_WLAN#	For EMI's Request
19.	12/29	43	Exchange JKBL pin1 and pin4	To meet correct footprint
20.	12/29	37	Add C389 on U14	For EMI's Request
21.	12/29	46	Add C392 on H21 for +5VALW	For EMI's Request
22.	12/29	40	Stuff CL7, CL23, CL24	For EMI's Request
23.	12/29	46	Add C393, close to C7 for +3VS	For EMI's Request
24.	12/29	32	Add R55 on DGPU_RST#	For common design
25.	12/29	27	Add R314 on HDMI_HPD and U9	To prevent ESD damage to U9
26.	01/03	47	change +1.05VS_DGPU routing	To turn on/off normally

REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	02/01	31	Change RA40 to pull up +5VL	Support S/M function in battery mode
2.	02/01	30	Change RA34 to pull up +3VL	Support S/M function in battery mode
3.	02/01	44	Add R103 to USB_EN# and pull up +5VALW	For common code with NWQAA
4.	02/01	44	Add R69 to VR_ON and pull low to GND	To avoid folating when EC is on initial
5.	02/01	30	Add C434 to VGATE	Reserve to avoid noise
6.	02/01	05	Add C482 to H_PWRGOOD	Reserve to avoid noise
7.	02/01	40	Add UL4	for 10/100/1000 transformer co-layout
8.	02/01	38	Add MDC circuits	For A51's request, Add MDC in DIS SKU
9.	02/01	35	Reserve U54 for +1.5VALW LDO and change VCCSUSHDA power rail	For MDC design change
10.	02/01	28	Add R287, R289, R291, R293 for Azalia bus to MDC	For MDC design change
11.	02/02	46	Add H31, H32	For MDC design change
12.	02/02	44	Add CAP_RST# on EC pin73 and link to JCS	For Cap sensor design change
13.	02/04	31	Stuff R133, R135 to 100Kohm PD GND	To prevent PCH pending internal HPD
14.	02/04	14	Reserve UV4,RV54,CV56,RV44	Reserved for VBIOS
15.	02/04	42	Add RA45, un-stuff RA43	To solve audio issue
16.	02/06	32	Exchange USB port 4&8	Design change, for A51's request
17.	02/08	08	Change C117,C118,C119,C120,C127,C128,C129	To improve ESD
18.	02/08	40	Change LL1, CL13	For design change
19.	02/09	41	Change RC7, RC8, RC9, RC12, RC13, RC14 from 0 ohm to 22 ohm	For EMI's request

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

Compal Electronics, Inc.		
Title: HW-PIR-1		
Size: Custom	Document Number: NBQAA LA6072P M/B	Rev: 1.0
Date: Monday, March 22, 2010	Sheet 60 of 61	

PIR (Product Improve Record)

NBQAA LA-6072P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.3 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	03/11	27	Add R148	To solve display compatibility issue
3.	03/11	15	Change CV58 from OSCON to POLY type	Due to the keyboard stress test is fail
4.	03/11	09	Change C216 from OSCON to POLY type	Due to the keyboard stress test is fail
5.	03/11	11	Change C163 from OSCON to POLY type	Due to the keyboard stress test is fail
6.	03/11	14	Delete UV4,RV54,CV56,RV44	Design change, no need extra BIOS ROM
7.	03/11	25	Stuff D84,D82,D19,D83	For ESD's request
8.	03/11	34	Change L12 from bead to R389 2.2 ohm+- 1%	For CRT issue
9.	03/14	13	Reserve YV1,RV29,CV45,CV46	Reserved for design change
10.	03/14	33	Change R221 to 1K ohm	For NV's Optimus sequence
11.	03/14	32	Change R55 to 1K ohm	For NV's Optimus sequence
12.	03/14	32	Reserve R334, add R336	For NV's Optimus sequence
13.	03/14	39	Change QM1 to Q14B	For cost down
14.	03/15	42	Un-mount CA16	For audio noise issue
15.	03/15	46	Un-mound SW2,SW3	Power button is no need after pre-MP
16.	03/16	42	Change CA12.1, RA12.2, CA18.2 from GND to AGND	For audio noise issue
17.	03/16	42	Change CA9 and CA10 to from 4700pF tp 1uF	For audio noise issue
18.	03/16	42	Add CA34~CA40 and CA51	For audio noise issue
19.	03/18	41	Change Card reader solution from O2 to JMB389C/385C	For design change
20.	03/19	27	Add D54	For HDMI CEC
21.	03/19	34	Add L12 that reserved 0 ohm for EMI	For CRT issue
22.	03/19	46	H22 from 6.0 to 3.0	For ME's request
23.	03/20	20	Change BIOS ROM footprint to M25P80-VMW6TP_SO8	No need the debug connector in MP phase
24.	03/22	13	Stuff RV28, un-stuff RV105	Reserved for 27M_SSC from clock gen
25.	03/22	43	Add RA22,RA23	Reserved to solve GPRS noise
26.	03/22	05	Stuff C482	To avoid noise
27.	03/22	30	Stuff C434	To avoid noise

Compal Electronics, Inc.		
Title: HW-PIR-1		
Size: Custom	Document Number: NBQAA LA6072P M/B	Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 61 of 61	