

COMPAL CONFIDENTIAL

MODEL NAME : NAL20
PCB NO : LA-5571P (DA80000FP00)
BOM P/N : 43176531LXX

M10 Margaux UMA
rPGA Auburndale +
FCBGA PCH IBEXPEAK-M

2010-01-21
REV : 1.0(A00)

@ : Nopop Component

MB Type	BOM P/N	TCM		TPM		BOM CONFIG
		W(3@)	W/O(4@)	W(5@)	W/O(6@)	
TPM EN, TCM DIS	43176531L01		*	*		4@, 5@
ALL TPM DISABLE	43176531L02		*		*	4@, 6@
TCM EN, TPM DIS	43176531L03	*			*	3@, 6@

MB PCB	
Part Number	Description
DA80000FP00	PCB OAF LA-5571P REV0 M/S UMA

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Title

Cover Sheet

Size

Document Number

LA-5571P

Rev

0.1

Date

Thursday, January 21, 2010

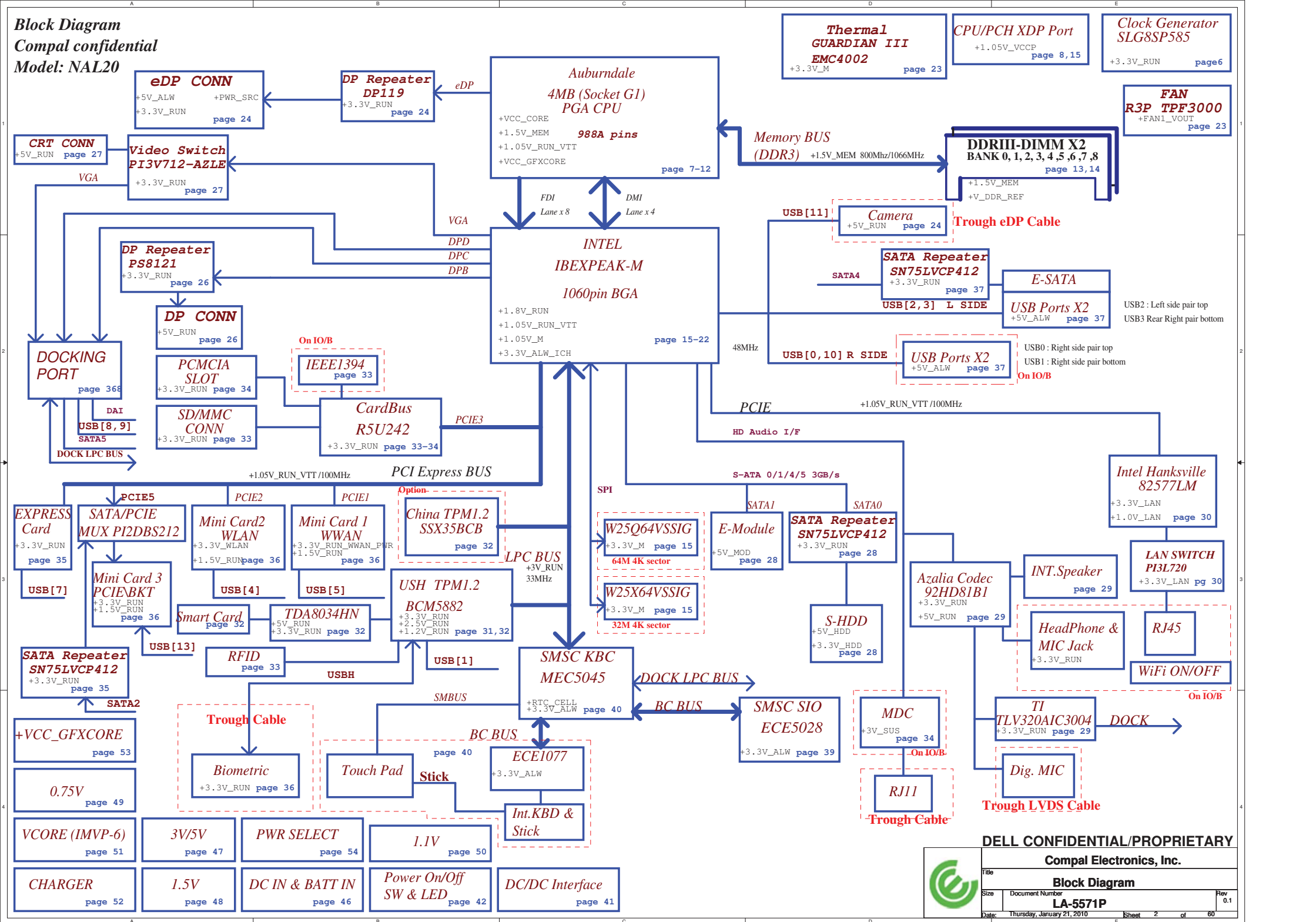
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of

60

Block Diagram
Compal confidential
Model: NAL20



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side Bottom)
	1	JUSB1 (Ext Right Side Top)
	2	JESA1 (Ext Left Side Top)
	3	JESA1 (Ext Left Side Bottom)
	4	WLAN
	5	WWAN
	6	Bluetooth
	7	USH->BIO
	8	DOCKING
	9	DOCKING
	10	Express card
	11	Camera
	12	NA
	13	WPAN/NVMHCI

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Card Bus
Lane 4	EXPRESS CARD
Lane 5	MINI CARD-3 PCIE/BKT
Lane 6	10/100/1G LAN
Lane 7	None
Lane 8	None

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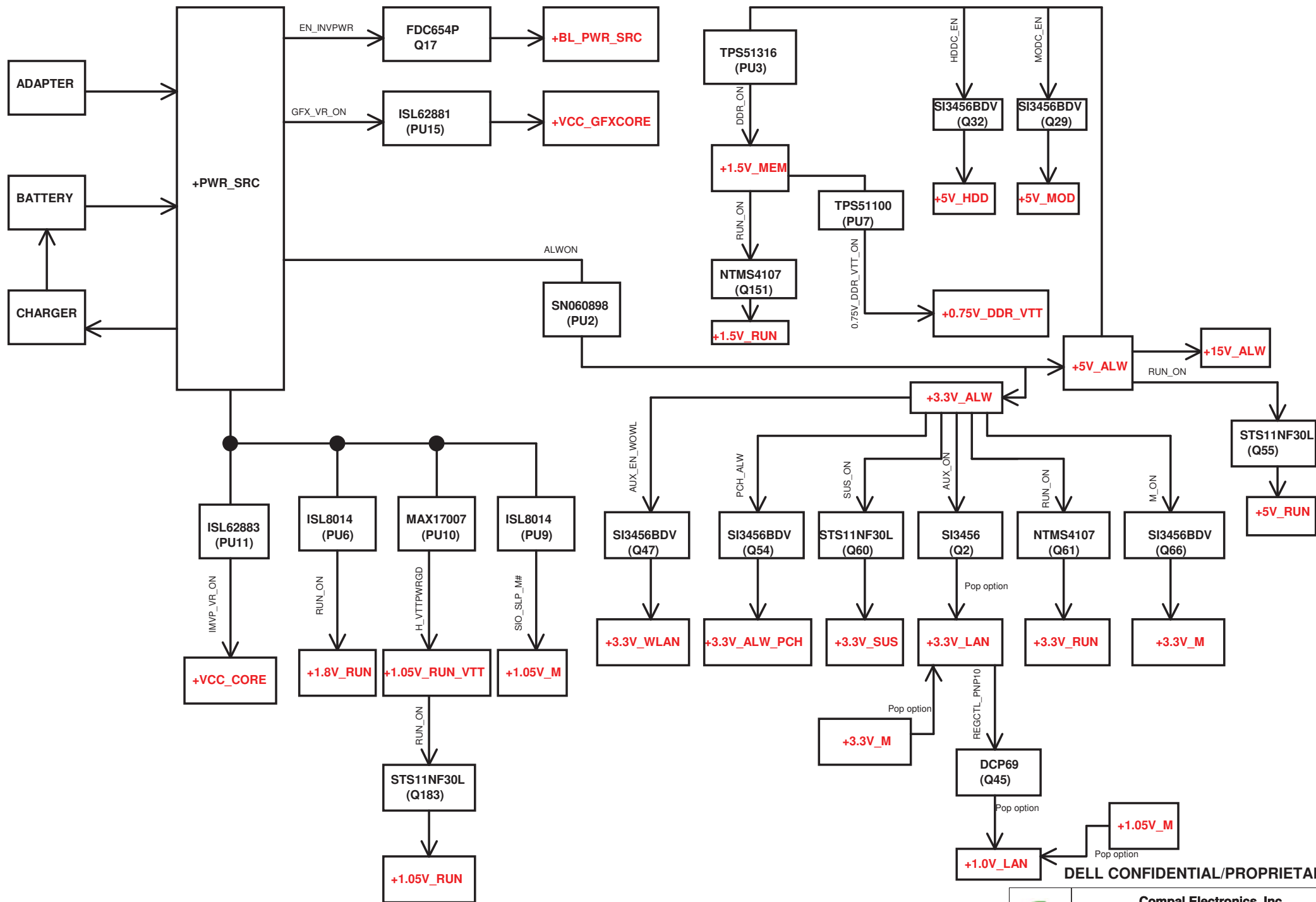
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Index and Config.



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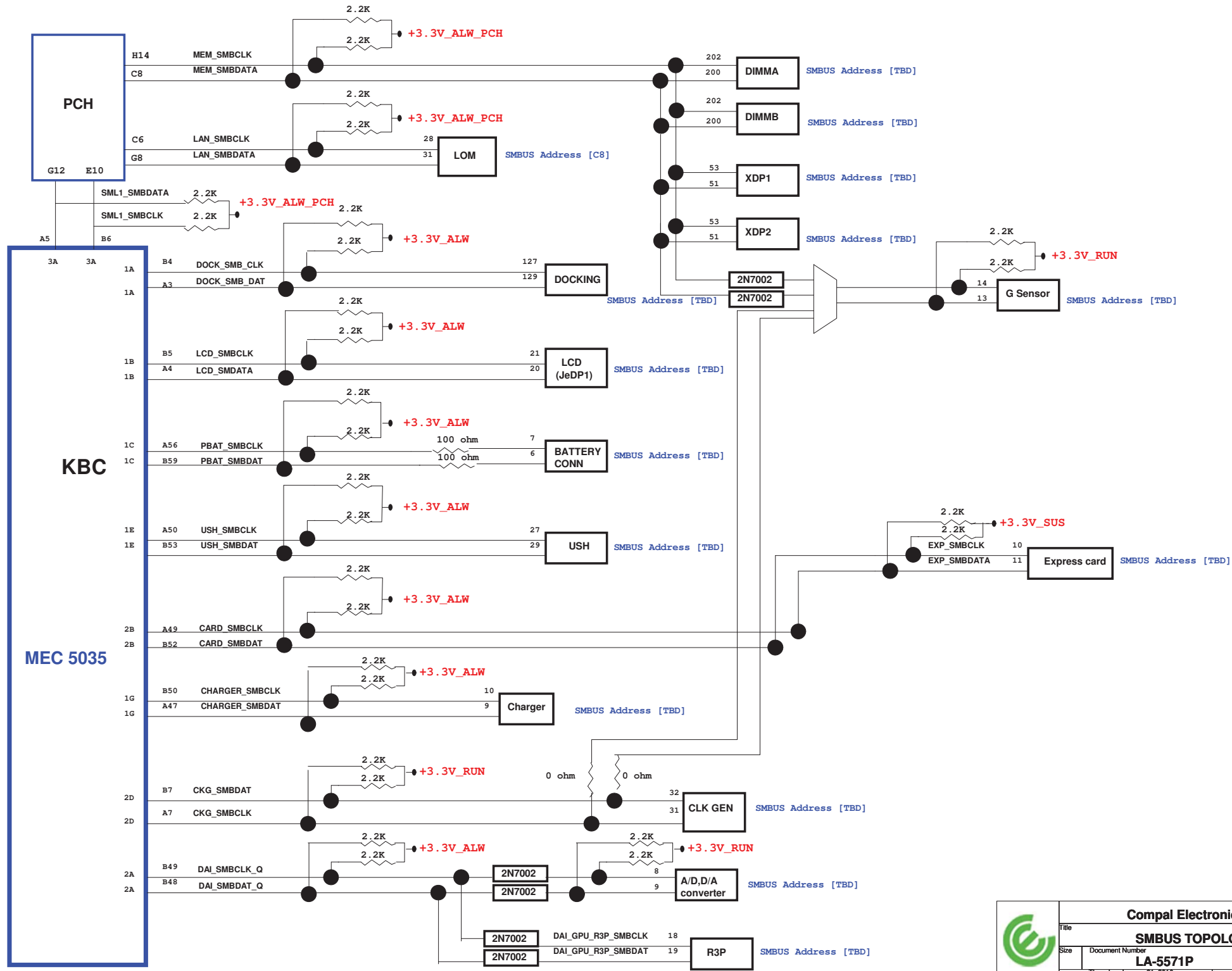


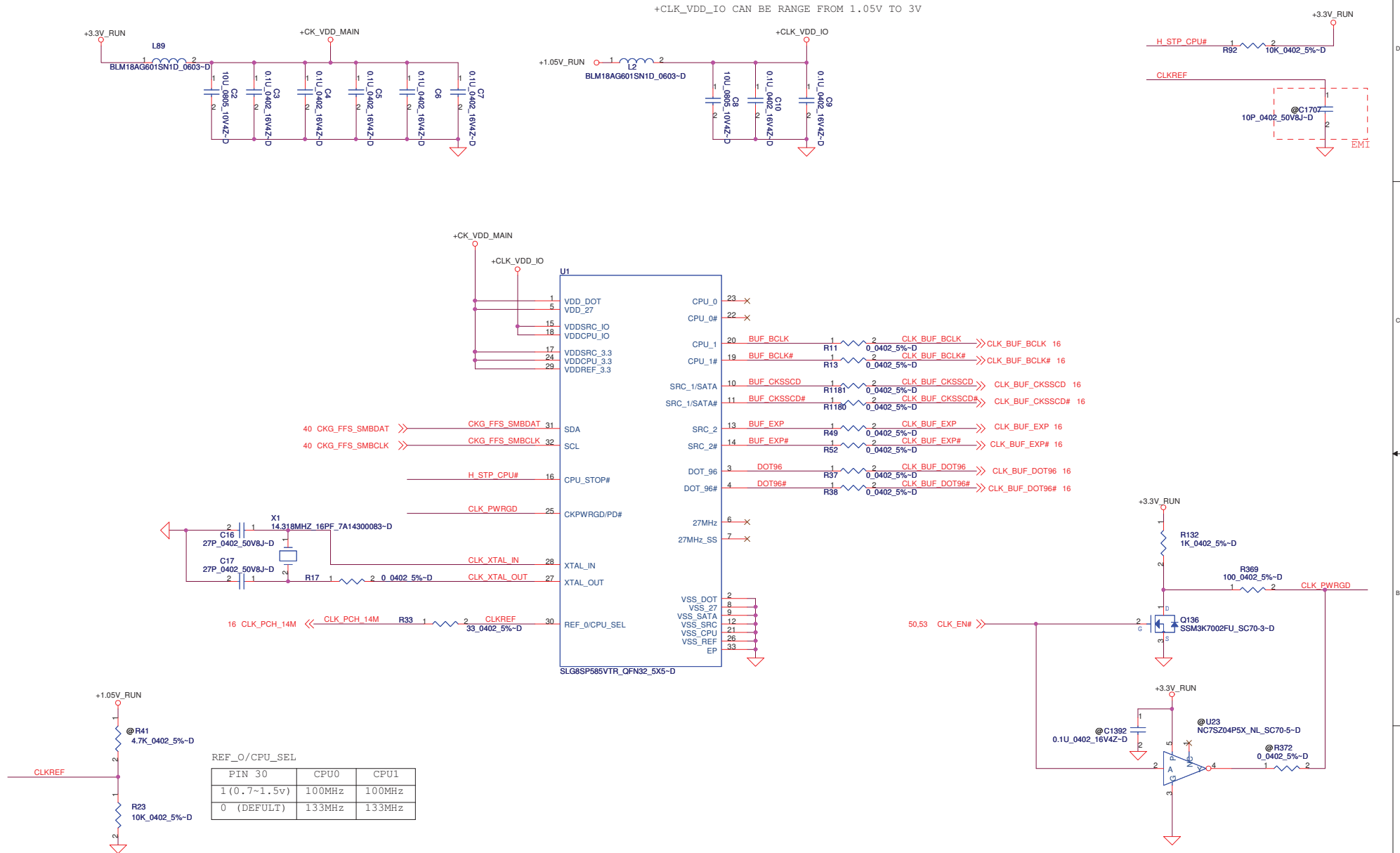
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Clock Generator			Rev 0.1
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17	DMI_CRX_PTX_N0	DMI_CRX_PTX_N0	A24	DMI_RX#0]
17	DMI_CRX_PTX_N1	DMI_CRX_PTX_N1	C23	DMI_RX#1]
17	DMI_CRX_PTX_N2	DMI_CRX_PTX_N2	B22	DMI_RX#2]
17	DMI_CRX_PTX_N3	DMI_CRX_PTX_N3	A21	DMI_RX#3]
17	DMI_CRX_PTX_P0	DMI_CRX_PTX_P0	B24	DMI_RX[0]
17	DMI_CRX_PTX_P1	DMI_CRX_PTX_P1	D23	DMI_RX[1]
17	DMI_CRX_PTX_P2	DMI_CRX_PTX_P2	B23	DMI_RX[2]
17	DMI_CRX_PTX_P3	DMI_CRX_PTX_P3	A22	DMI_RX[3]
17	DMI_CTX_PRX_N0	DMI_CTX_PRX_N0	D24	DMI_TX#0]
17	DMI_CTX_PRX_N1	DMI_CTX_PRX_N1	G24	DMI_TX#1]
17	DMI_CTX_PRX_N2	DMI_CTX_PRX_N2	F23	DMI_TX#2]
17	DMI_CTX_PRX_N3	DMI_CTX_PRX_N3	H23	DMI_TX#3]
17	DMI_CTX_PRX_P0	DMI_CTX_PRX_P0	D25	DMI_TX[0]
17	DMI_CTX_PRX_P1	DMI_CTX_PRX_P1	F24	DMI_TX[1]
17	DMI_CTX_PRX_P2	DMI_CTX_PRX_P2	E23	DMI_TX[2]
17	DMI_CTX_PRX_P3	DMI_CTX_PRX_P3	G23	DMI_TX[3]

17	FDI_CTX_PRX_N0	FDI_CTX_PRX_N0	E22	FDI_TX#0]
17	FDI_CTX_PRX_N1	FDI_CTX_PRX_N1	D21	FDI_TX#1]
17	FDI_CTX_PRX_N2	FDI_CTX_PRX_N2	D19	FDI_TX#2]
17	FDI_CTX_PRX_N3	FDI_CTX_PRX_N3	D18	FDI_TX#3]
17	FDI_CTX_PRX_N4	FDI_CTX_PRX_N4	G21	FDI_TX#4]
17	FDI_CTX_PRX_N5	FDI_CTX_PRX_N5	E19	FDI_TX#5]
17	FDI_CTX_PRX_N6	FDI_CTX_PRX_N6	F21	FDI_TX#6]
17	FDI_CTX_PRX_N7	FDI_CTX_PRX_N7	G18	FDI_TX#7]
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17	FDI_CTX_PRX_P2	FDI_CTX_PRX_P2	D20	FDI_TX[2]
17	FDI_CTX_PRX_P3	FDI_CTX_PRX_P3	C18	FDI_TX[3]
17	FDI_CTX_PRX_P4	FDI_CTX_PRX_P4	G22	FDI_TX[4]
17	FDI_CTX_PRX_P5	FDI_CTX_PRX_P5	E20	FDI_TX[5]
17	FDI_CTX_PRX_P6	FDI_CTX_PRX_P6	F20	FDI_TX[6]
17	FDI_CTX_PRX_P7	FDI_CTX_PRX_P7	G19	FDI_TX[7]
17	FDI_FSYNC0	FDI_FSYNC0	E17	FDI_FSYNC[0]
17	FDI_FSYNC1	FDI_FSYNC1	E17	FDI_FSYNC[1]
17	FDI_INT	FDI_INT	C17	FDI_INT
17	FDI_LSYNC0	FDI_LSYNC0	F18	FDI_LSYNC[0]
17	FDI_LSYNC1	FDI_LSYNC1	D17	FDI_LSYNC[1]

REV1.0
TYCO_CALPELLA_AUBURNDALE

DMI

PCI EXPRESS

PCI EXPRESS

PEG_ICOMPI	B26	PEG_IRCOMP_R	R1084	1	2	49.9_0402 1%-D
PEG_ICOMPO	A26					
PEG_RCOMPO	B27	EXP_RBIAS	R1129	1	2	750_0402 1%-D
PEG_RBIAS	A25					
PEG_RX#0]	K35	X				
PEG_RX#1]	J34	X				
PEG_RX#2]	J34	X				
PEG_RX#3]	G35	X				
PEG_RX#4]	G32	X				
PEG_RX#5]	F34	X				
PEG_RX#6]	F31	X				
PEG_RX#7]	D35	X				
PEG_RX#8]	E33	X				
PEG_RX#9]	C33	X				
PEG_RX#10]	D32	X				
PEG_RX#11]	C33	X				
PEG_RX#12]	C31	X				
PEG_RX#13]	B28	X				
PEG_RX#14]	B30	X				
PEG_RX#15]	A31	X				
PEG_RX[0]	J35	X				
PEG_RX[1]	H34	X				
PEG_RX[2]	H33	X				
PEG_RX[3]	F35	X				
PEG_RX[4]	G33	X				
PEG_RX[5]	E34	X				
PEG_RX[6]	F32	X				
PEG_RX[7]	D34	X				
PEG_RX[8]	F33	X				
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PEG_RX[14]	B29	X				
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PEG_TX#4]	L31	X				
PEG_TX#5]	K32	X				
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PEG_TX#8]	K29	X				
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PEG_TX#10]	H29	X				
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PEG_TX#12]	E28	X				
PEG_TX#13]	D29	X				
PEG_TX#14]	D27	X				
PEG_TX#15]	C26	X				
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PEG_TX[10]	G29	X				
PEG_TX[11]	F28	X				
PEG_TX[12]	E27	X				
PEG_TX[13]	D28	X				
PEG_TX[14]	C27	X				
PEG_TX[15]	C25	X				

EDP_CPU_AUX# 24

EDP_HPDP# 24
EDP_CPU_AUX# 24

EDP_CPU_LANE_N1 24
EDP_CPU_LANE_N0 24

EDP_CPU_LANE_P1 24
EDP_CPU_LANE_P0 24

K27	VSS161
K9	VSS162
K6	VSS163
K3	VSS164
J32	VSS165
J30	VSS166
J21	VSS167
J19	VSS168
H35	VSS169
H32	VSS170
H28	VSS171
H26	VSS172
H24	VSS173
H22	VSS174
H18	VSS175
H15	VSS176
H13	VSS177
H11	VSS178
H8	VSS179
H5	VSS180
H2	VSS181
G34	VSS182
G31	VSS183
G20	VSS184
G9	VSS185
G6	VSS186
G3	VSS187
F30	VSS188
F27	VSS189
F22	VSS190
F19	VSS191
F16	VSS192
E35	VSS193
E32	VSS194
E29	VSS195
E24	VSS196
E21	VSS197
E18	VSS198
E13	VSS199
E11	VSS200
E8	VSS201
E5	VSS202
D33	VSS203
D30	VSS204
D26	VSS205
D9	VSS206
D6	VSS207
D3	VSS208
C34	VSS209
C32	VSS210
C29	VSS211
C28	VSS212
C24	VSS213
C22	VSS214
C20	VSS215
C19	VSS216
C16	VSS217
B31	VSS218
B25	VSS219
B21	VSS220
B18	VSS221
B17	VSS222
B13	VSS223
B11	VSS224
B8	VSS225
B6	VSS226
B4	VSS227
A29	VSS228
A27	VSS229
A23	VSS230
A9	VSS231
	VSS232
	VSS233

VSS

NCTF

VSS_NCTF1	AT35
VSS_NCTF2	AT1
VSS_NCTF3	AR34
VSS_NCTF4	J34
VSS_NCTF5	B2
VSS_NCTF6	B1
VSS_NCTF7	A35

REV1.0
TYCO_CALPELLA_AUBURNDALE

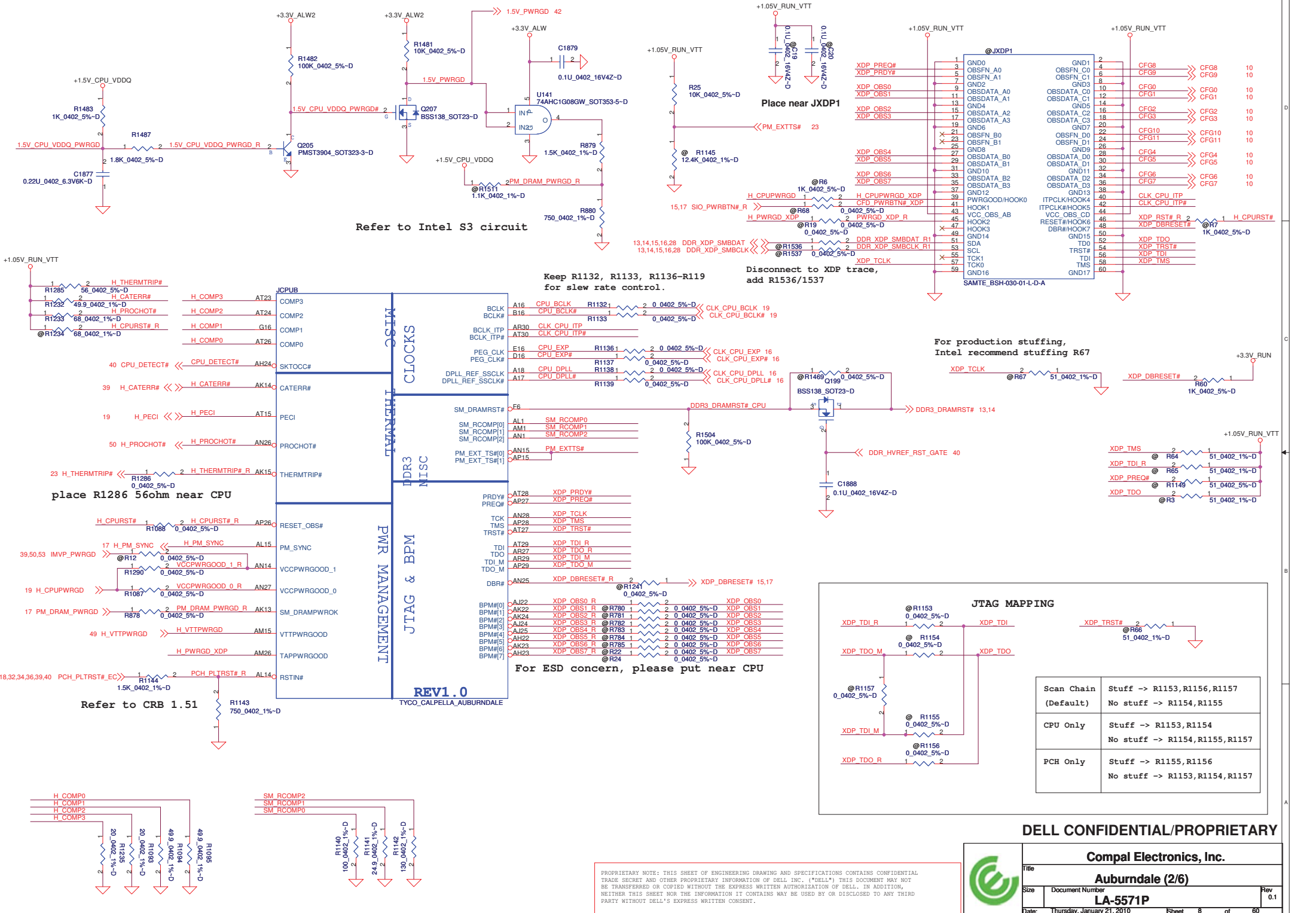
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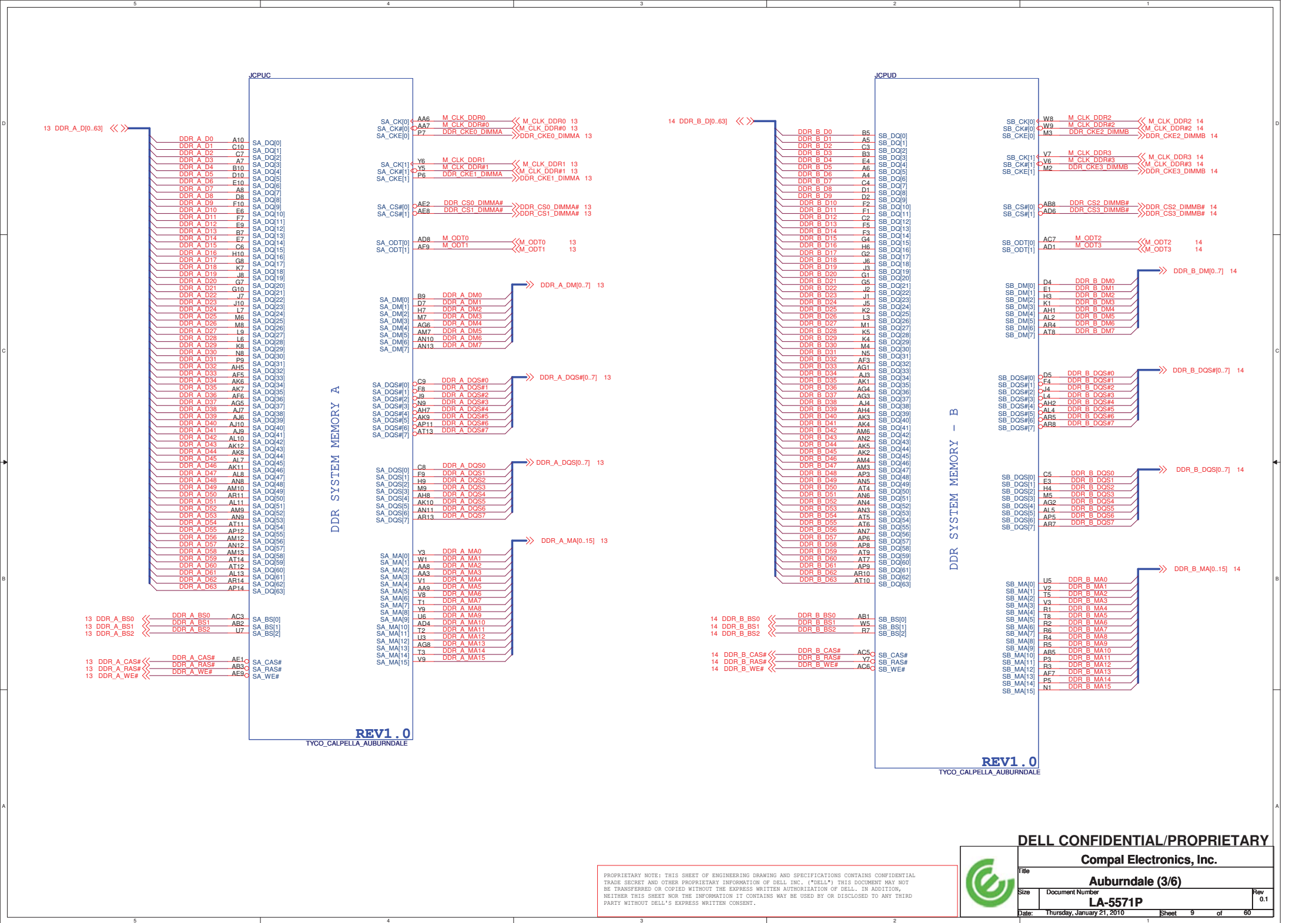
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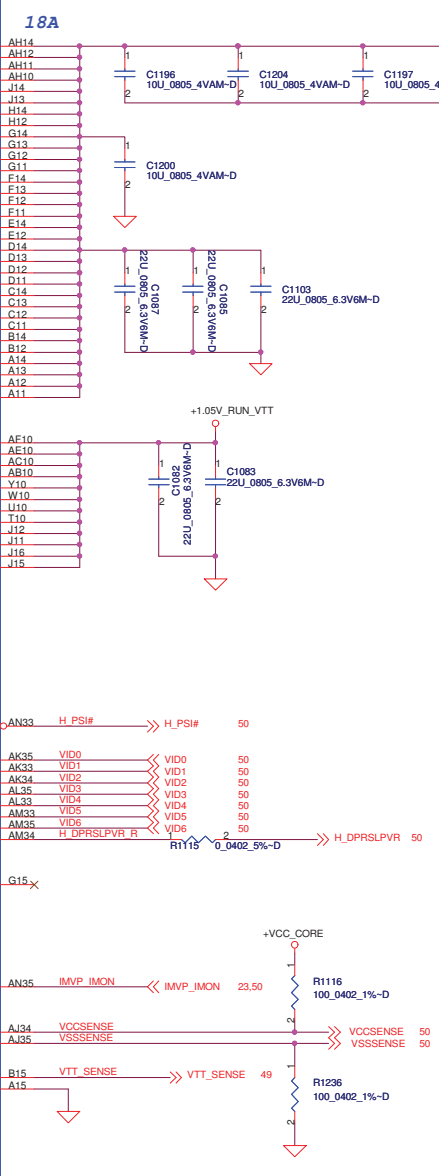
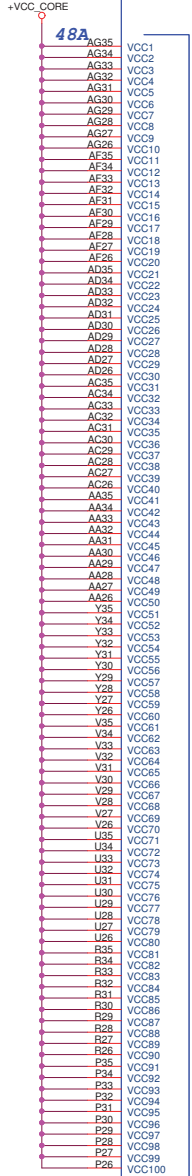
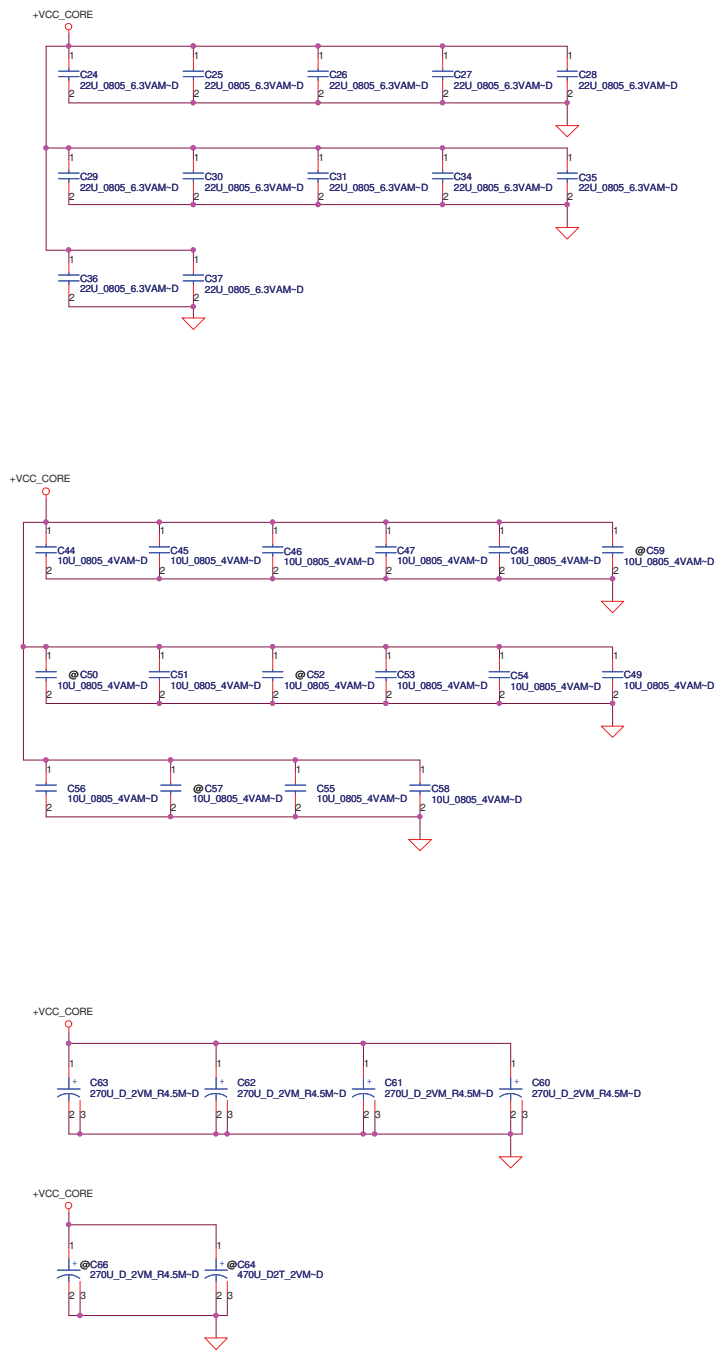
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POWER

CPU VIDS

SENSE LINES

REV1.0

TYCO, CALPELLA, AUBURNDALE

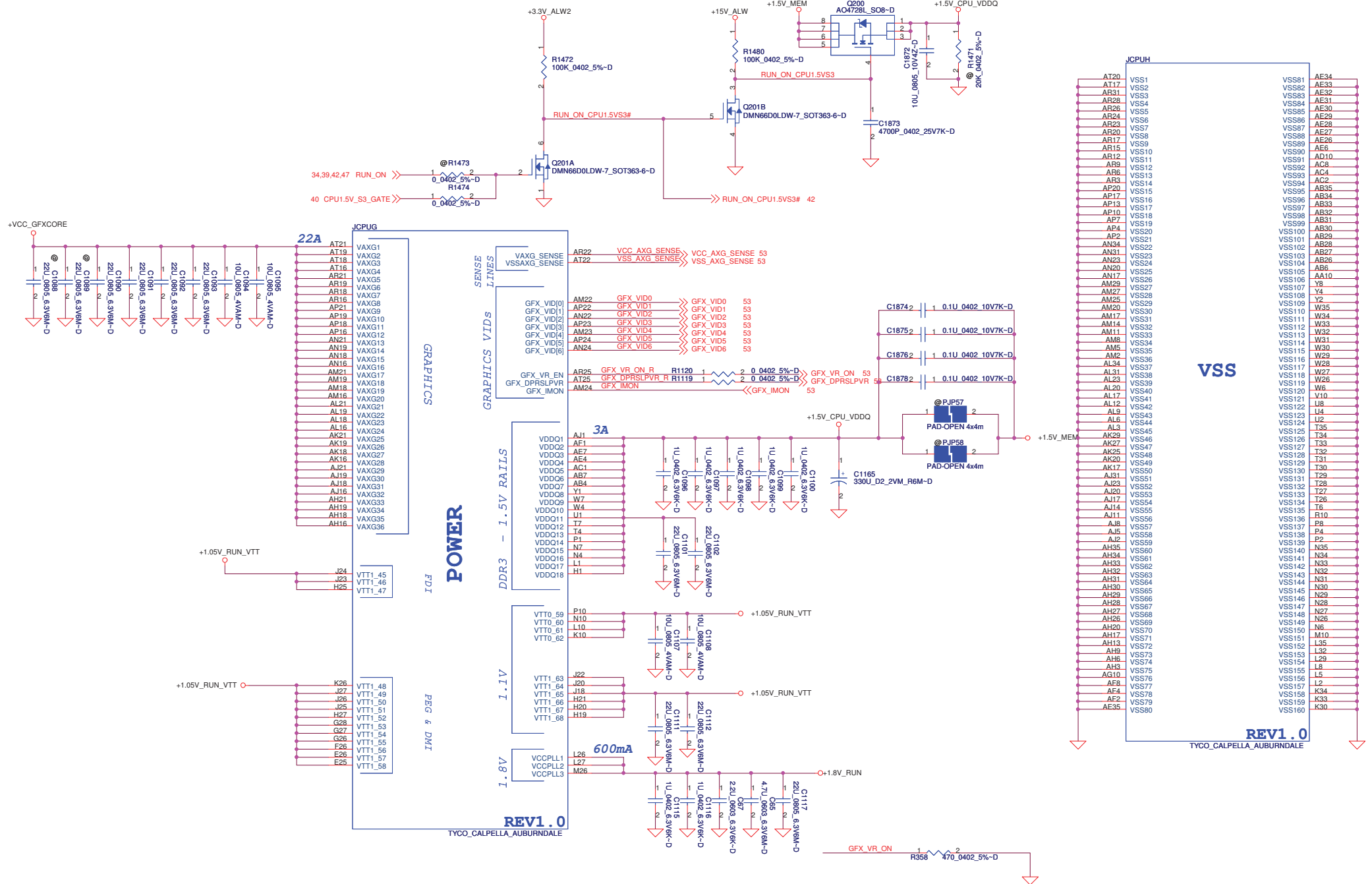
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+1.5V_CPU_VDDQ Source



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Auburndale (6/6)

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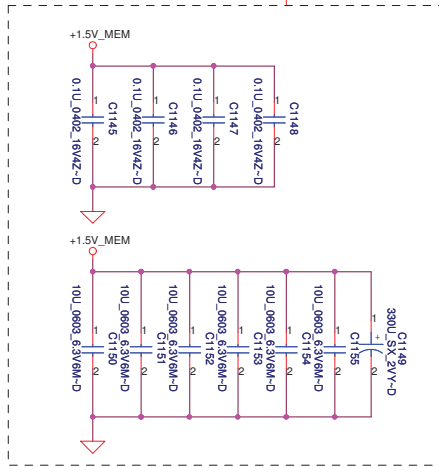
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9 DDR_B_DQS#[0..7] <<>>
 9 DDR_B_DQ[0..63] <<>>
 9 DDR_B_DM[0..7] <<>>
 9 DDR_B_DQS#[0..7] <<>>
 9 DDR_B_MA[0..15] <<>>

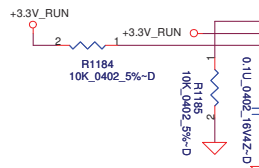
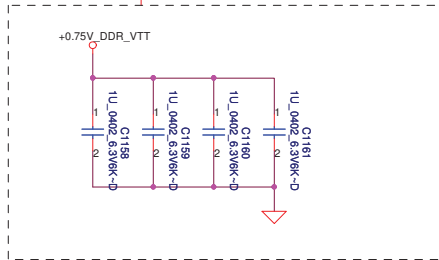
Populate R88 for Intel DDR3
 VREFDQ multiple methods M1

Note:
 Check voltage tolerance of
 VREF_DQ at the DIMM socket

Layout Note:
 Place near JDIMMB



Layout Note:
 Place near JDIMMB.203,204



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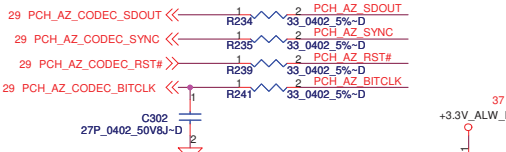
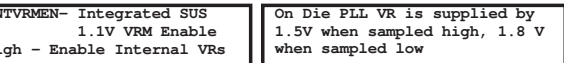
JDIMMB H=9.2

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DDRIII-SODIMM SLOT2			
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ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



**200 MIL SO8
64Mb Flash ROM**

For iAMT

3.3V_M

R298
3.3K_0402_5%-D

C328
0.1u_0402_5%-D

R299
3.3K_0402_5%-D

U12

1 CS#

2 DO

3 /WP

4 GND

5 DIO

6 CLK

7 /HOLD

8 VCC

PCH_SPI_CS#

PCH_SPI_DIN

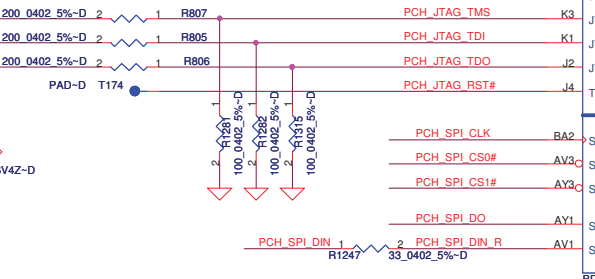
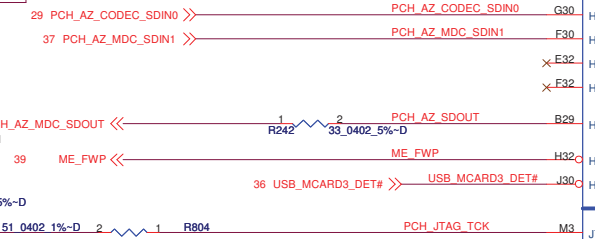
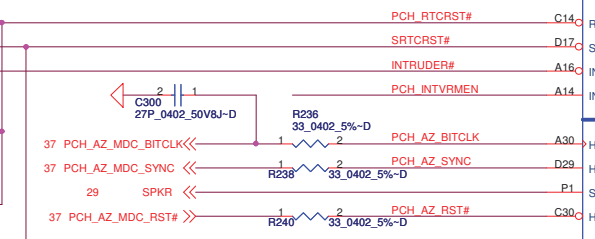
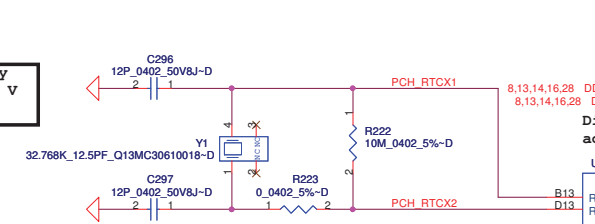
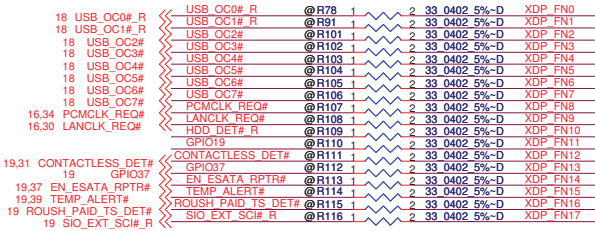
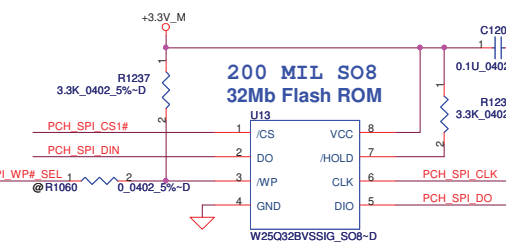
PCH_SPI_CLK

PCH_SPI_DO

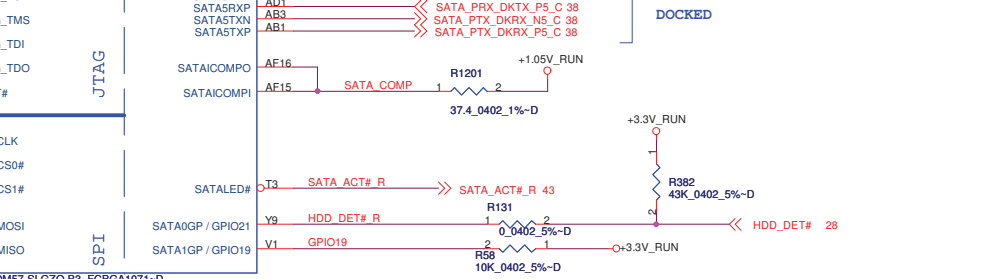
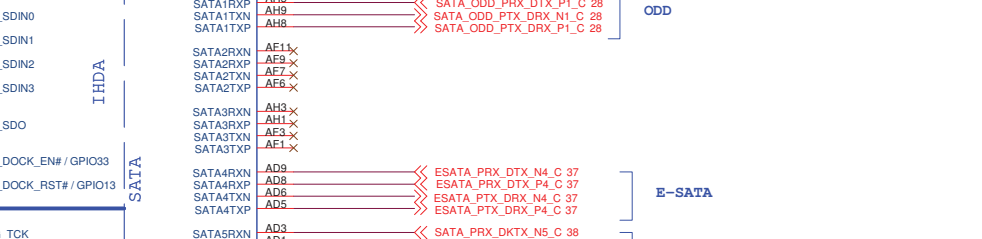
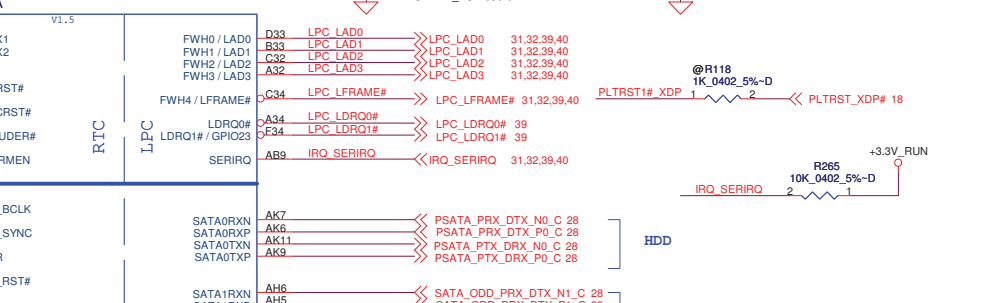
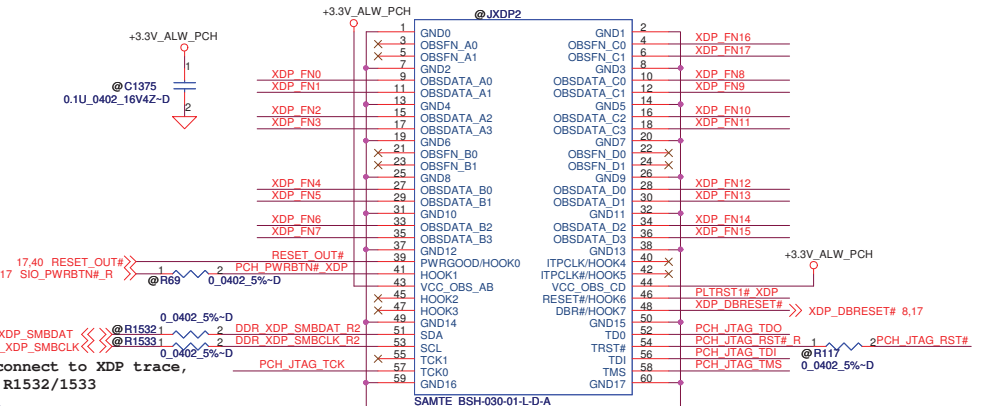
R1246
0.0402_5%-D

W25Q64BVSSIG SO8-D

39 SPI_WP*_SEL



		PCH JTAG Enable		PCH JTAG Disable		Production
PCH Pin	Ref.	ES1	ES2	ES1	ES2	All
TDO	R806	No Stuff	200 ohm	No Stuff	No Stuff	No Stuff
	R1315	No Stuff	100 ohm	No Stuff	No Stuff	No Stuff
TMS	R807	200 ohm	200 ohm	No Stuff	No Stuff	No Stuff
	R1281	100 ohm	100 ohm	No Stuff	No Stuff	No Stuff
TDI	R805	200 ohm	200 ohm	20K ohm	No Stuff	No Stuff
	R1282	100 ohm	100 ohm	10K ohm	No Stuff	No Stuff
TCK	R804	4.7K ohm	4.7K ohm	4.7K ohm	4.7K ohm	No Stuff
TRST#	R808	20K ohm	20K ohm	No Stuff	No Stuff	
	R1316	10K ohm	10K ohm	No Stuff	No Stuff	



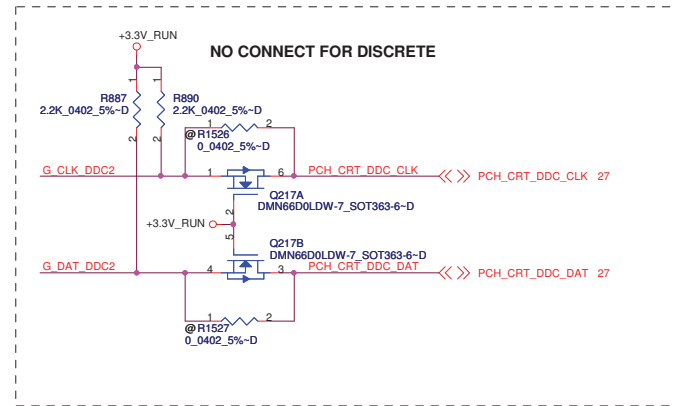
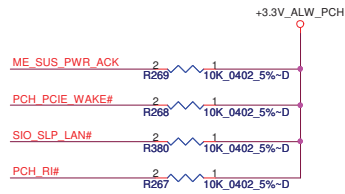
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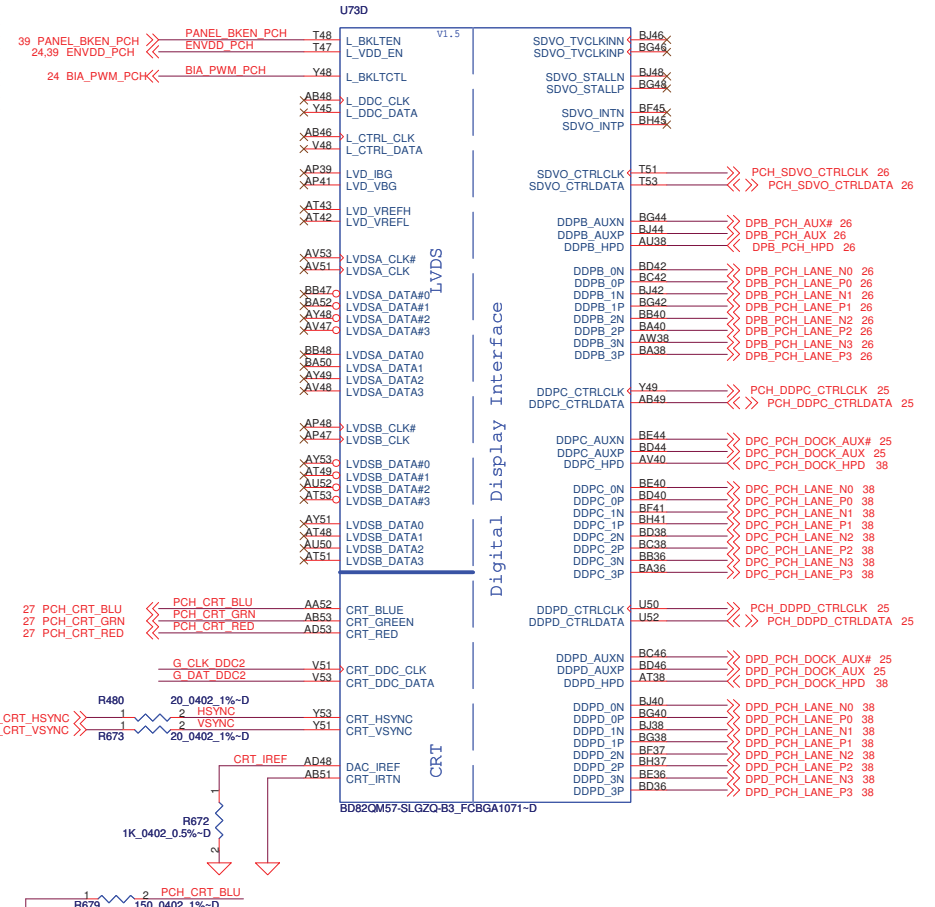
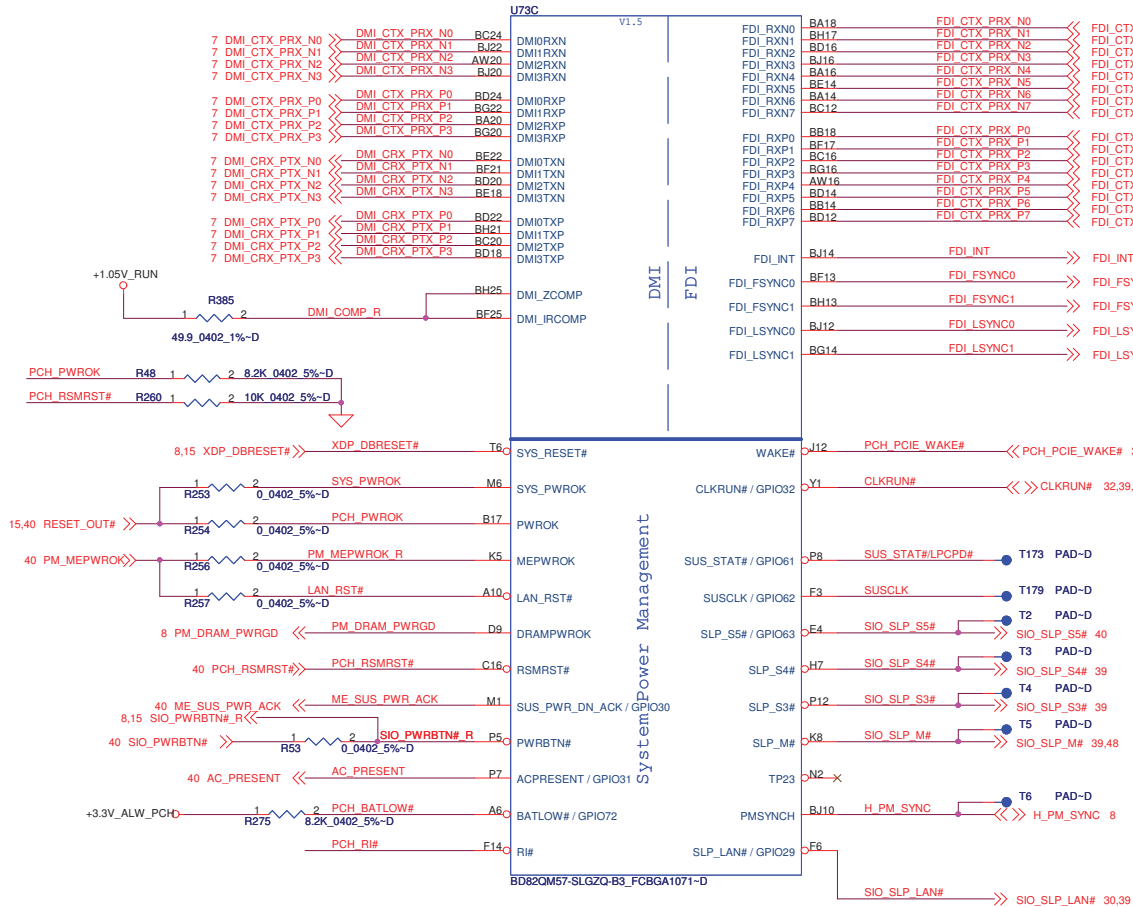
PCH (1/8)

Title			
PCH (1/8)			
Size	Document Number	Rev	
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Intel request DDPB can not support eDP



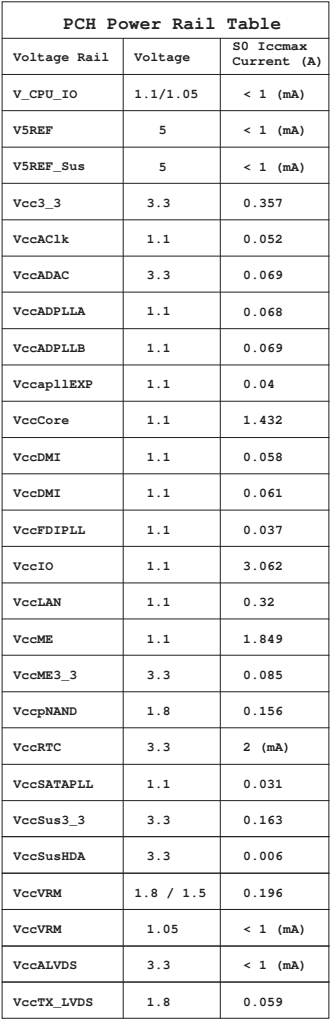
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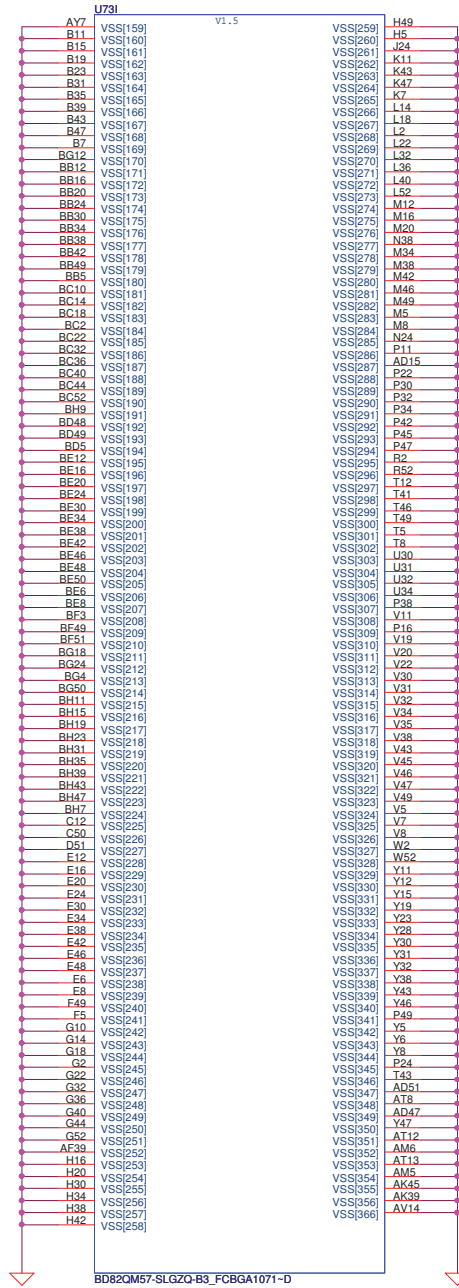
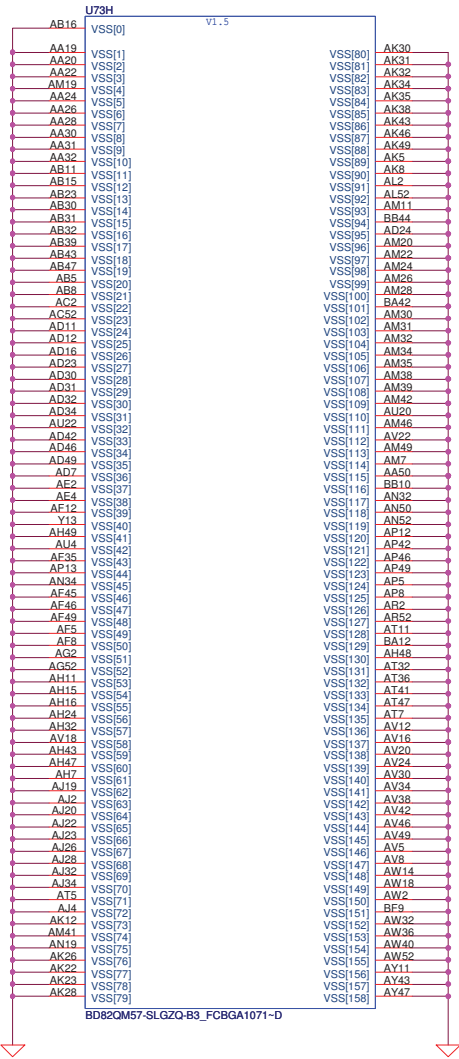
Compal Electronics, Inc.

PCH (3/8)



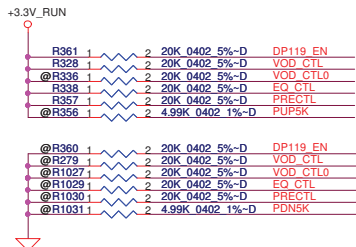
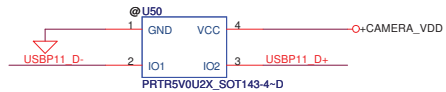
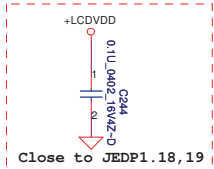
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Size	Document Number	
	LA-5571P	
Date	Thursday, January 21, 2010	Sheet 17 of 60





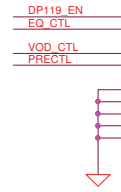
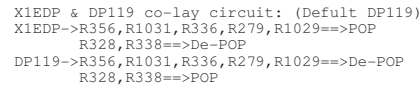
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		Compal Electronics, Inc.	
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Size	Document Number		Rev
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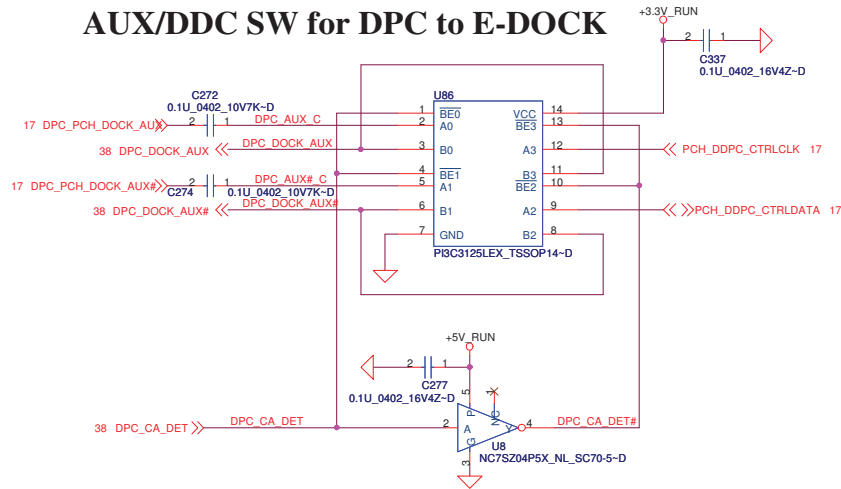
VOD (mV)	PRE (dB)	PRECTL	VOD_CTL
300	2.5	0	0
	6	VCC/2	0
	8.5	1	0
400	0	0	VCC/2
	3.5	VCC/2	VCC/2
	5.5	1	VCC/2
600	0	0	1
	2	VCC/2	1
800	0	1	1

MODE	DP119_EN
PWR Down	0
OUT2 DIS	VCC/2
OUT1 OUT2 EN	1

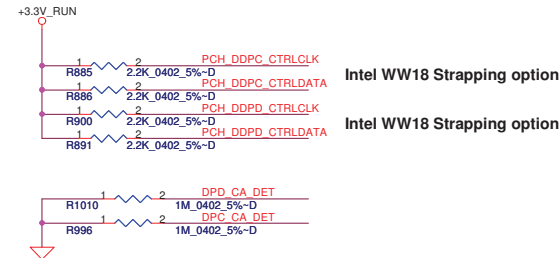
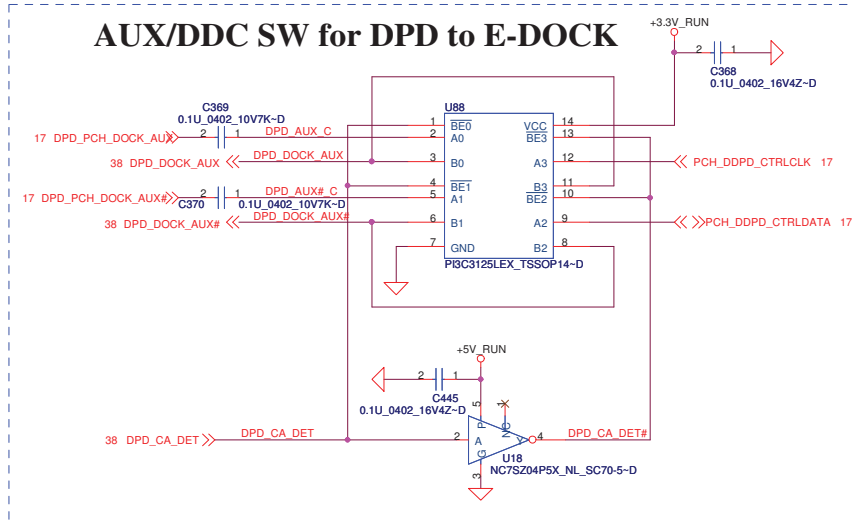


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AUX/DDC SW for DPC to E-DOCK



AUX/DDC SW for DPD to E-DOCK



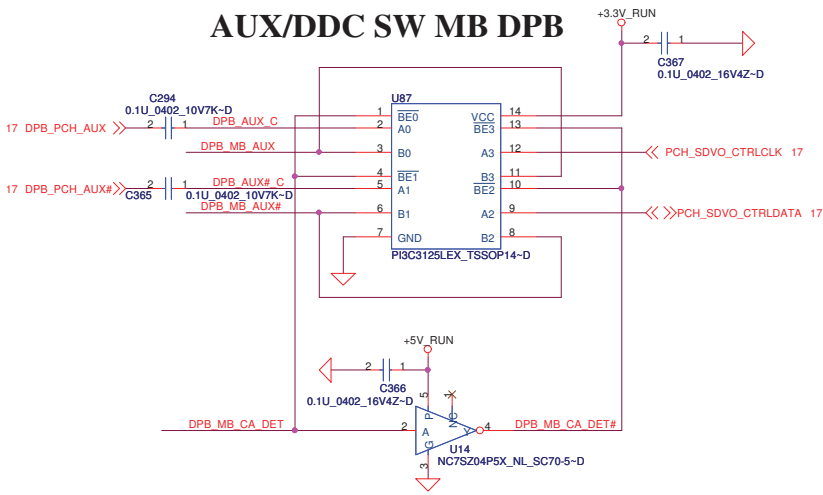
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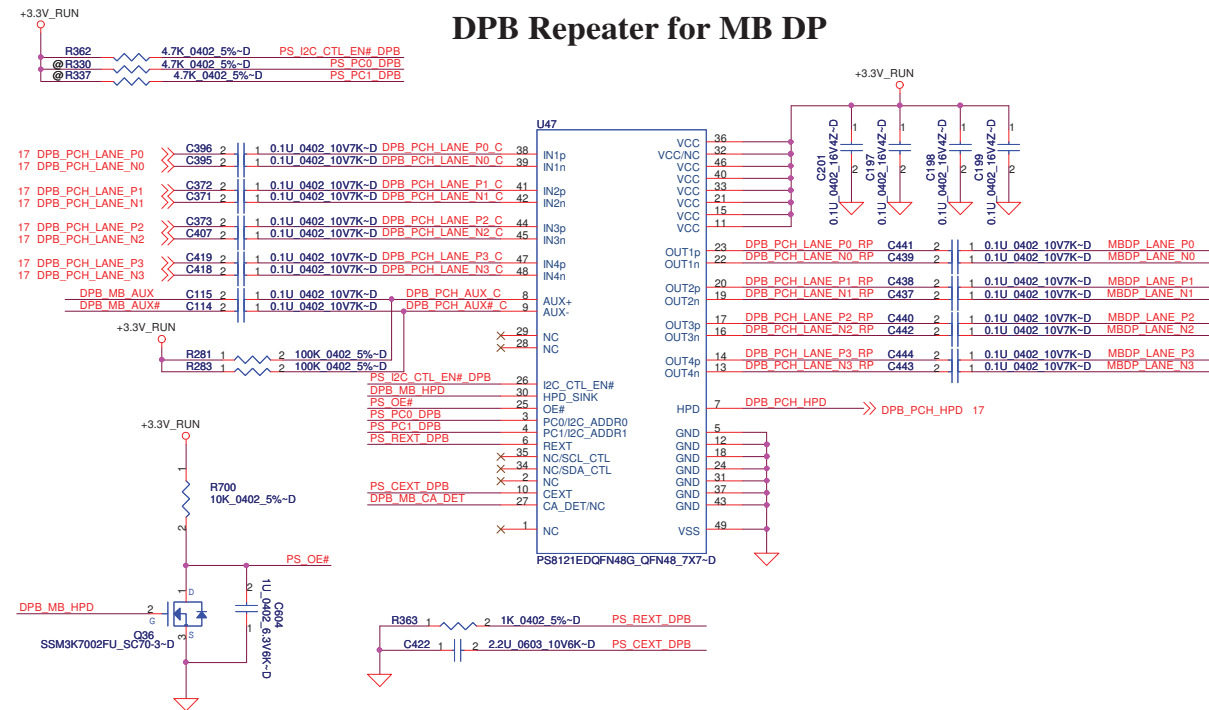
Compal Electronics, Inc.

Title			
DPC DPD SW for DOCK			
Size	Document Number	Rev	
	LA-5571P	0.1	
Date:	Thursday, January 21, 2010	Sheet	25 of 60

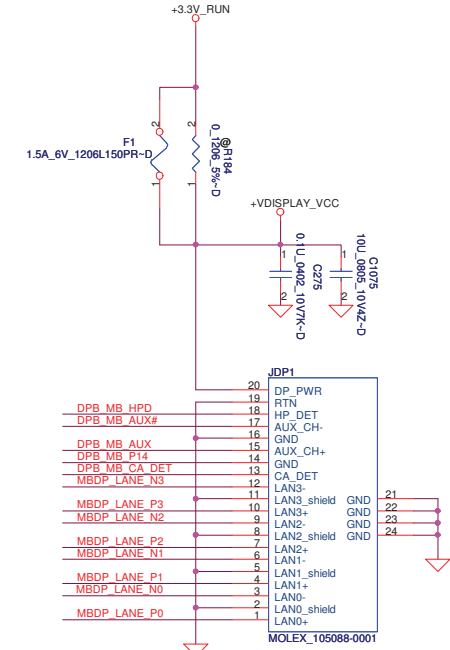
AUX/DDC SW MB DPB



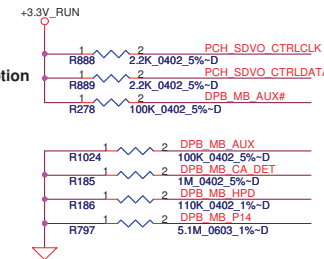
DPB Repeater for MB DP



Display port Dip Connector



Intel WW18 Strapping option

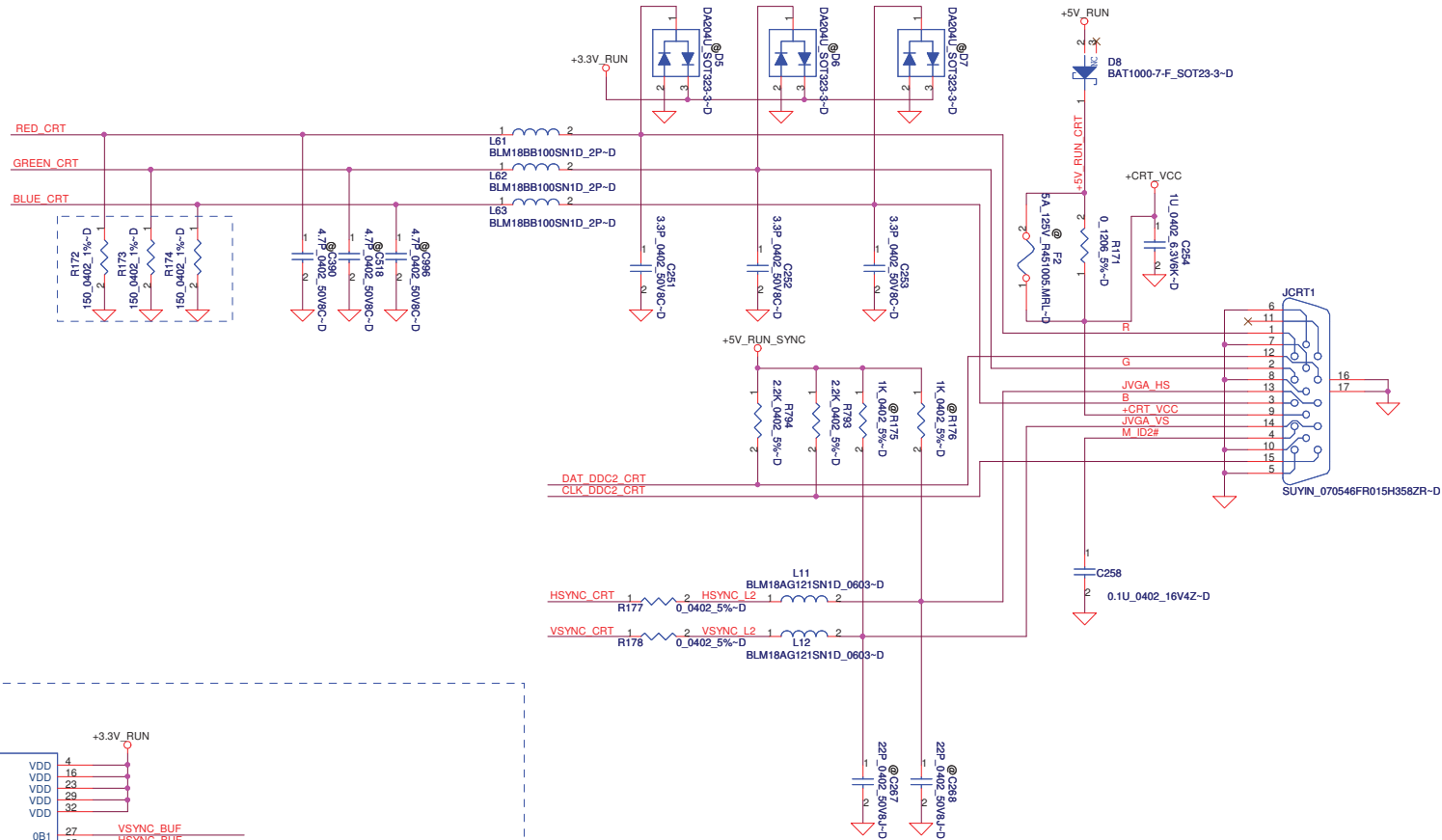


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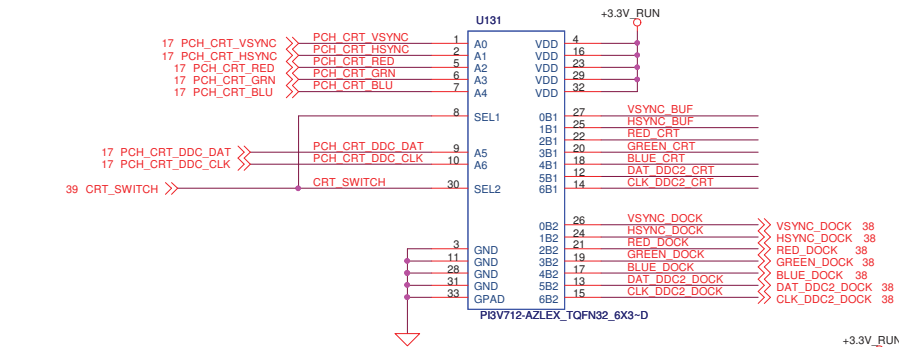
Compal Electronics, Inc.

Title			
Display port			
Size	Document Number	Rev	
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Date:	Thursday, January 21, 2010	Sheet	26 of 60

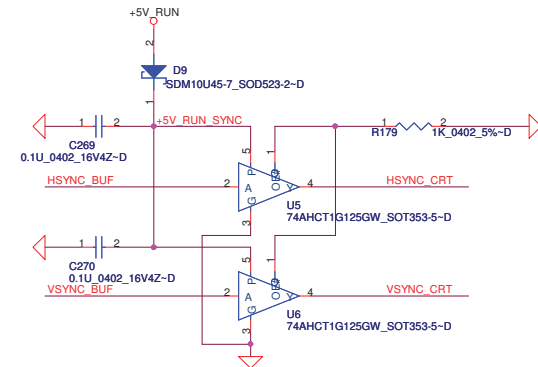
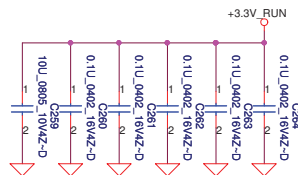
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VGA SW for MB/DOCK



SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR

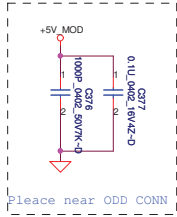


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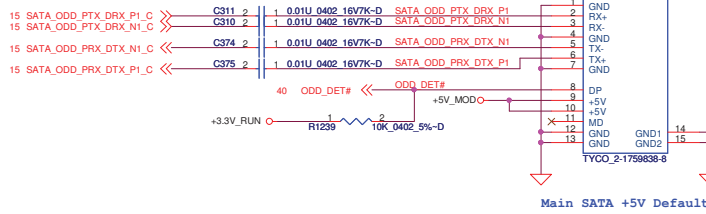


Compal Electronics, Inc.			
Title			
CRT/Video switch			
Size	Document Number	Rev	
	LA-5571P	0.1	
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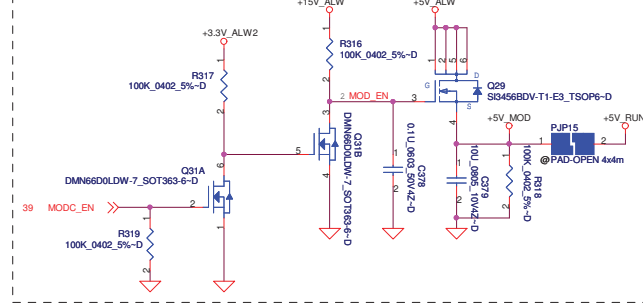
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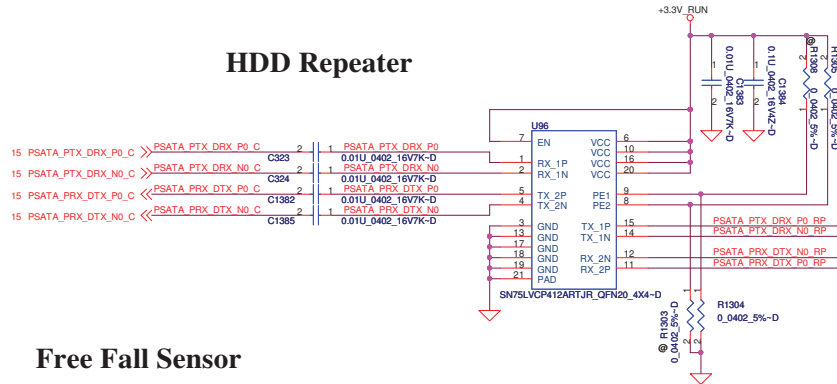
For ODD



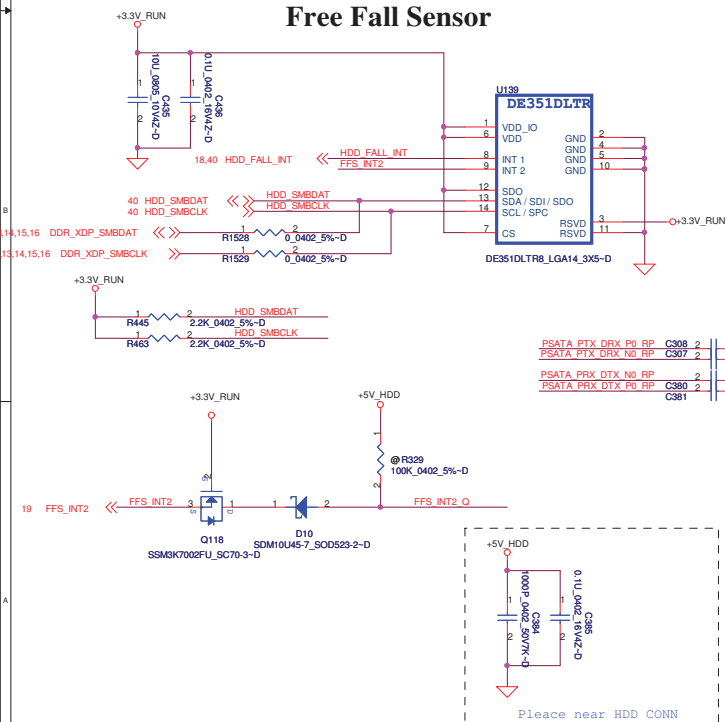
+5VMOD Source



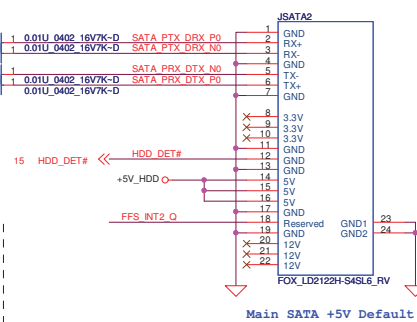
HDD Repeater



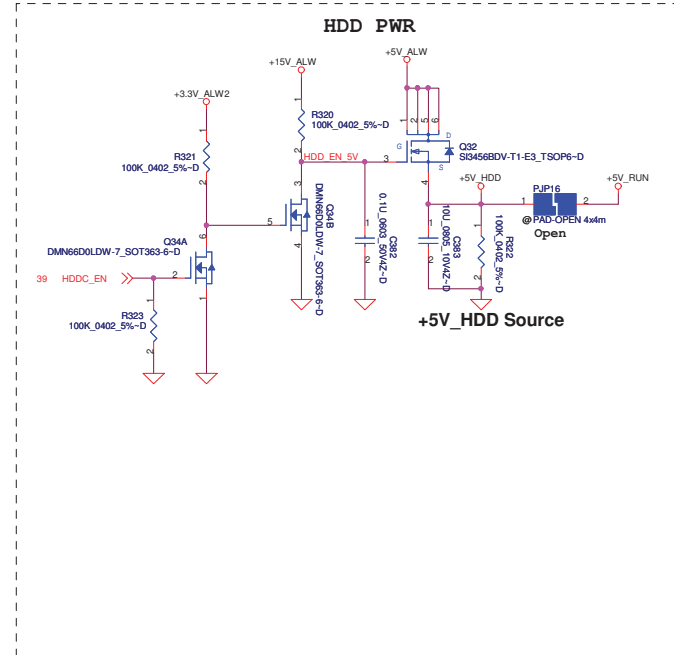
Free Fall Sensor



For HDD Temp.



HDD PWR



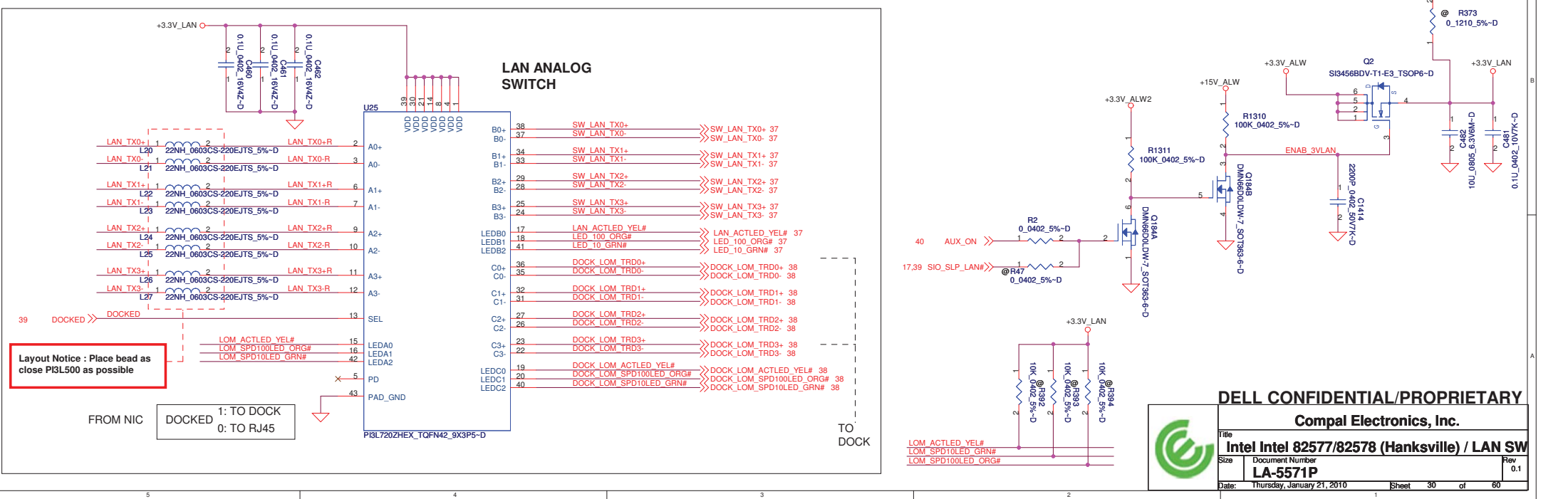
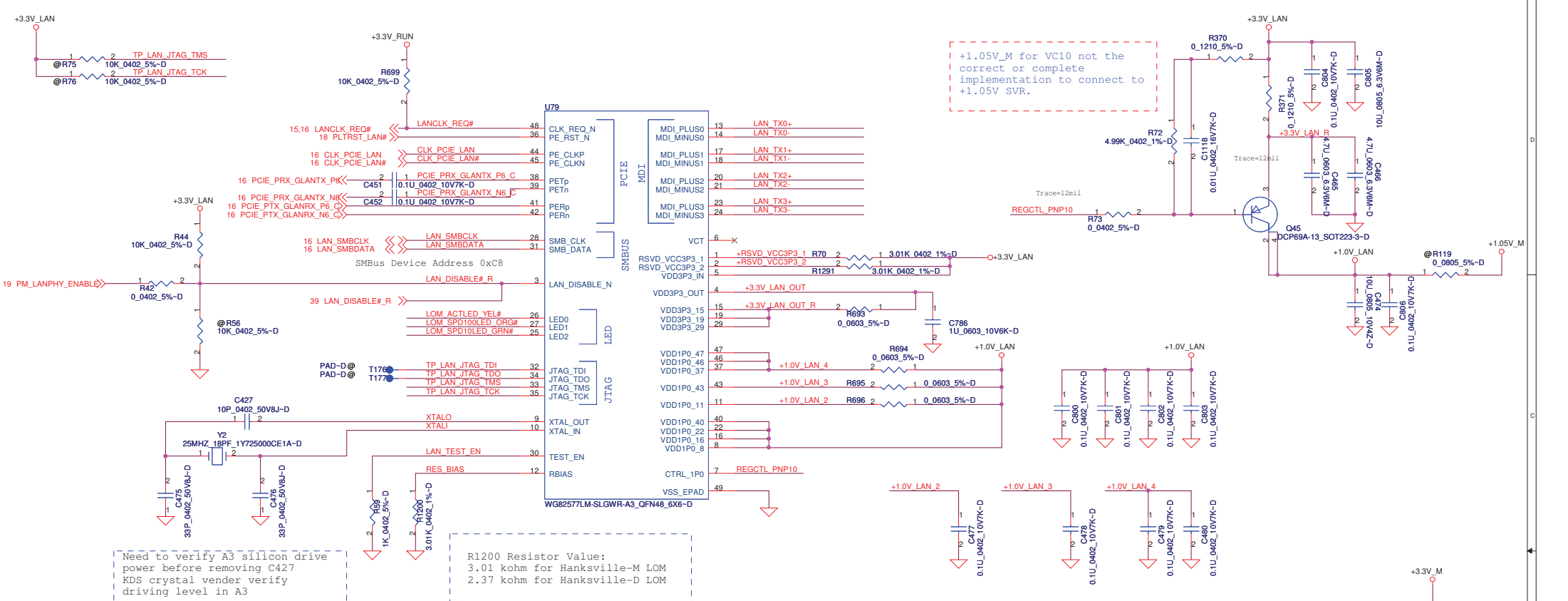
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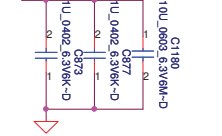
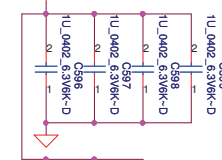
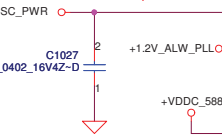
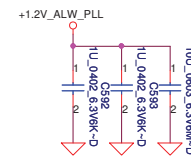
Compal Electronics, Inc.

File	ODD/HDD CONNECTOR		
Size	Document Number	LA-5571P	Rev 0.1
Date	Thursday, January 21, 2010	Sheet 28	of 60

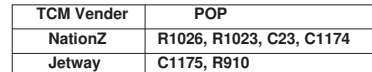
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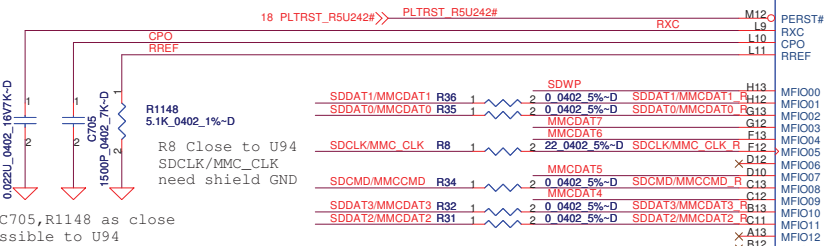
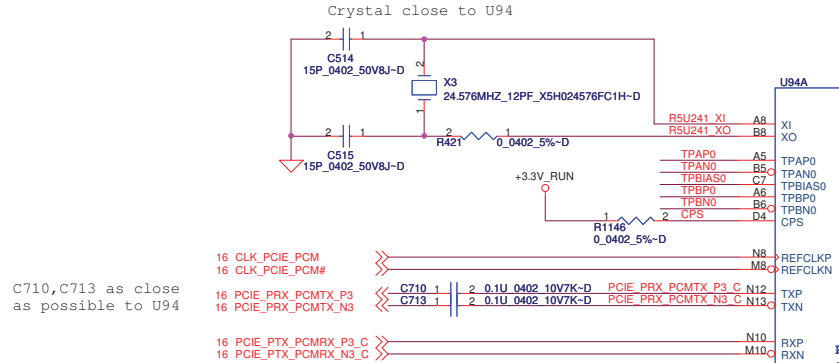




China TCM: NationZ & Jetway co-lay



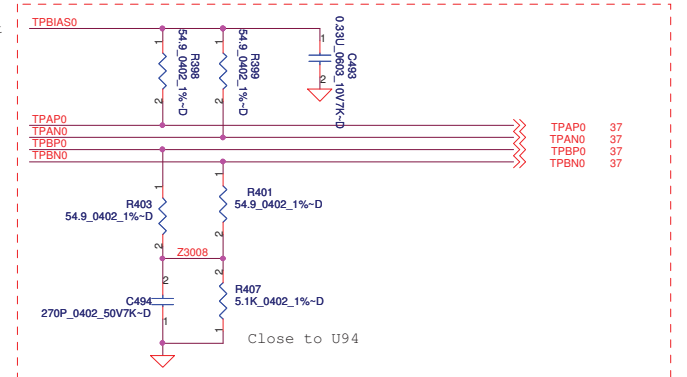
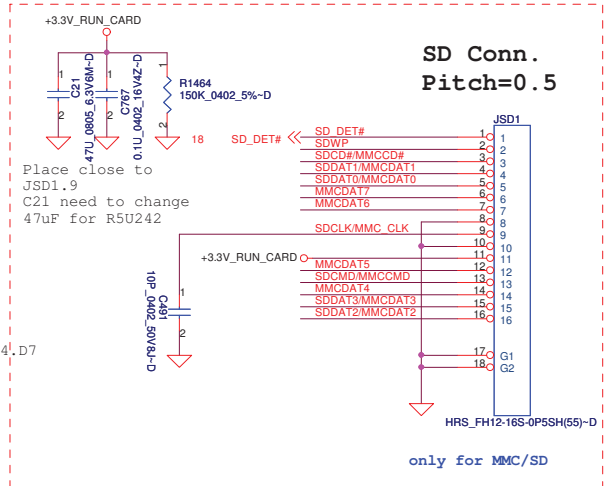
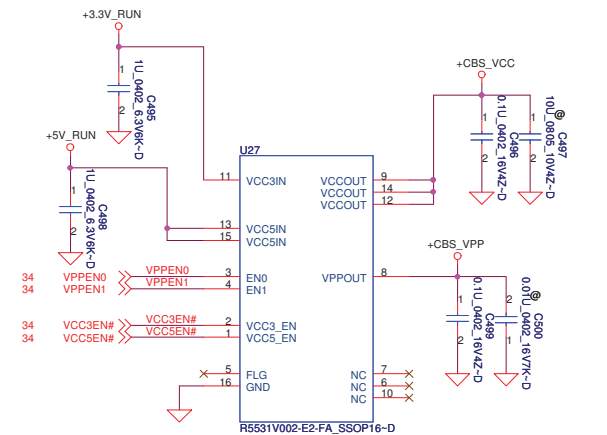
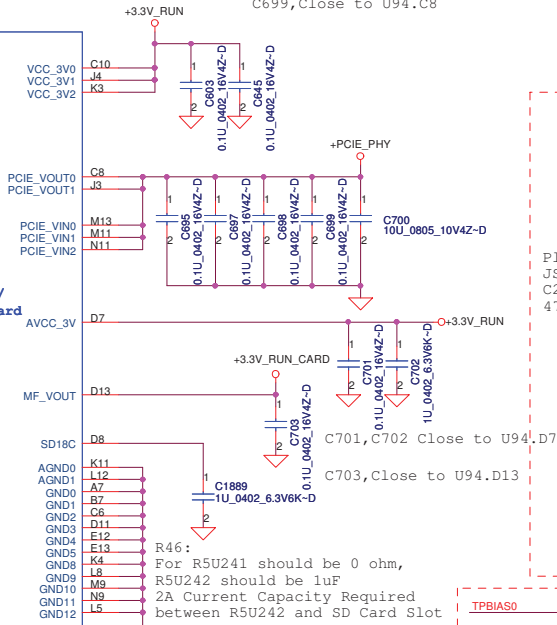
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MFIO Pin Assignment Table

MFIO	SD8	XD	MS8
00	WP	D7	BS
01	D1	D6	-
02	D0	D5	D1
03	D7	D4	-
04	D6	D3	D5
05	CLK	D2	D0
06	-	D1	-
07	D5	D0	D4
08	CMD	WP#	D2
09	D4	WE#	D6
10	D3	ALE	D3
11	D2	CLE	-
12	-	CE#	-
13	-	RE#	D7
14	-	R/B#	CLK

C645, Close to U94.C10
C603, Close to U94.J4/K3
C695, Close to U94.M13
C697, Close to U94.M11/N11
C698, Close to U94.J3
C699, Close to U94.C8



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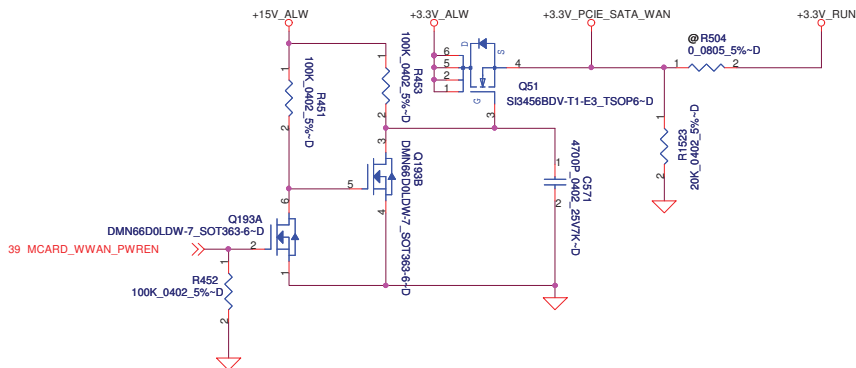
R5U242 (1/2)

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LA-5571P		0.1
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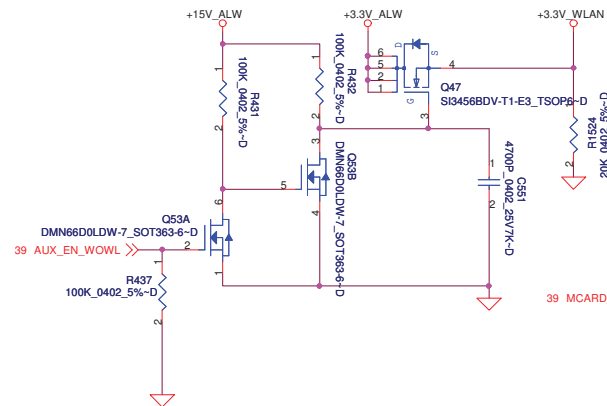


Size	Document Number LA-5571P	Rev 0.1
Date:	Thursday, January 21, 2010	Sheet 34 of 60

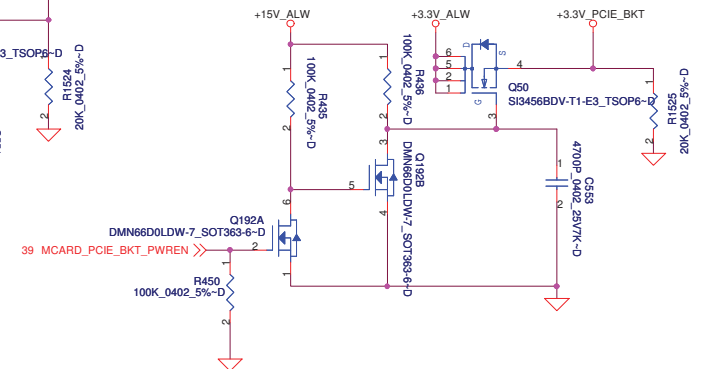
Power Control for Mini card1



Power Control for Mini card2



Power Control for Mini card3



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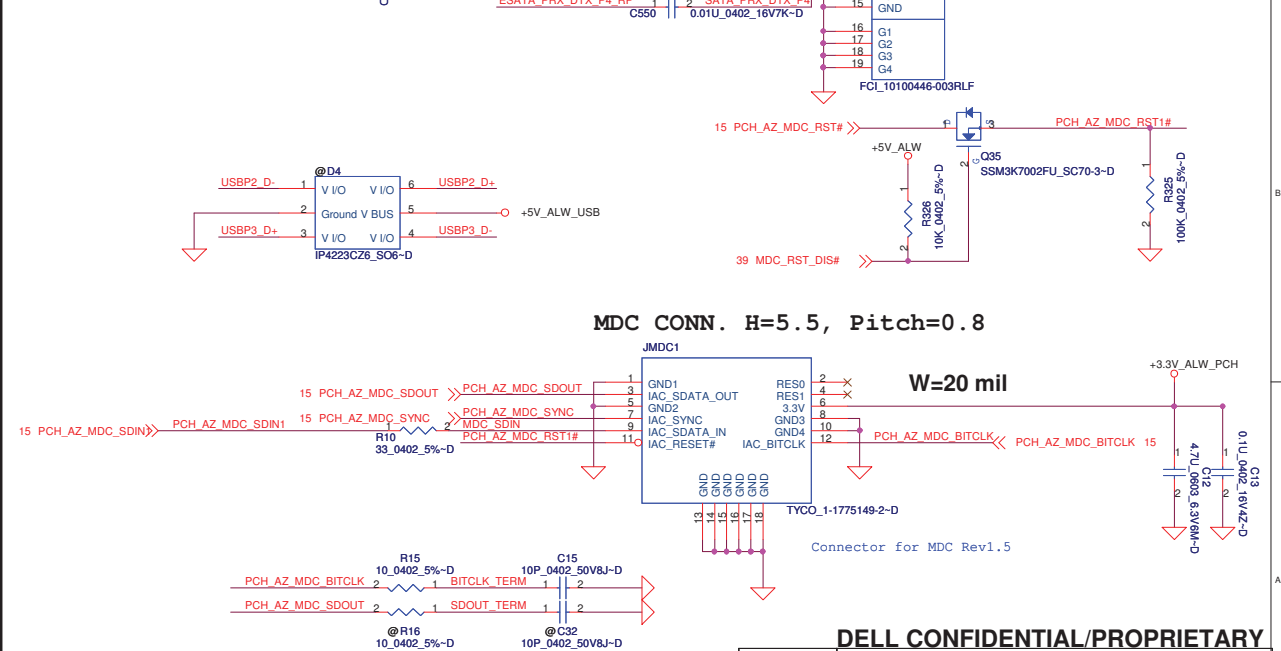
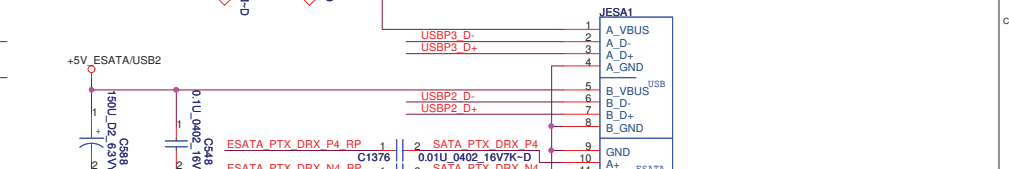
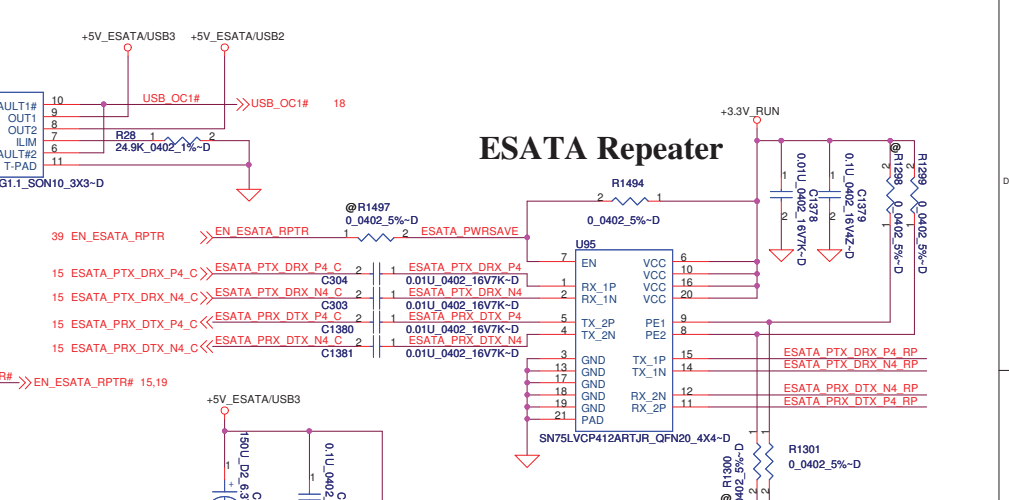
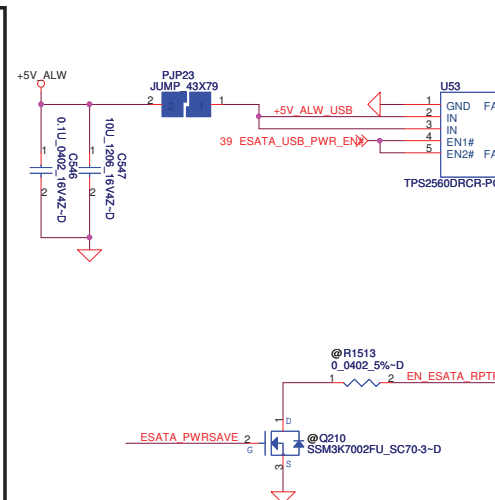
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Title
PCIE PWR

Size Document Number
LA-5571P

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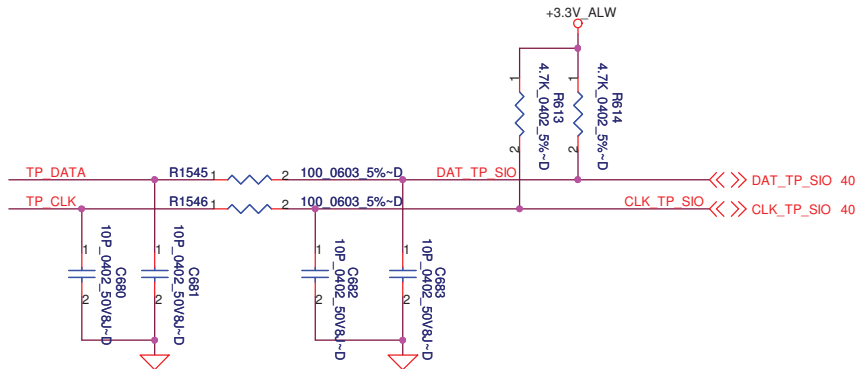
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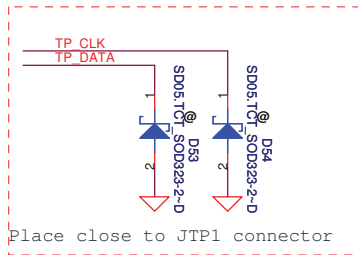
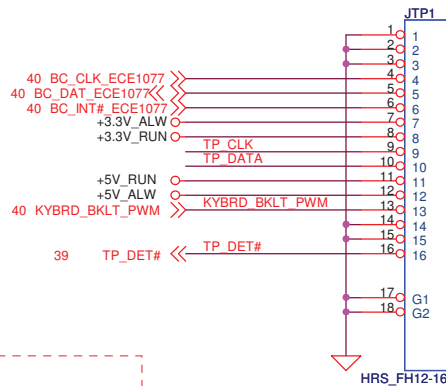
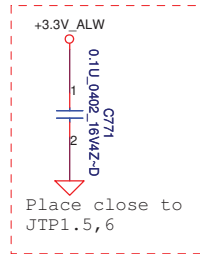
USB 2.0 PORT

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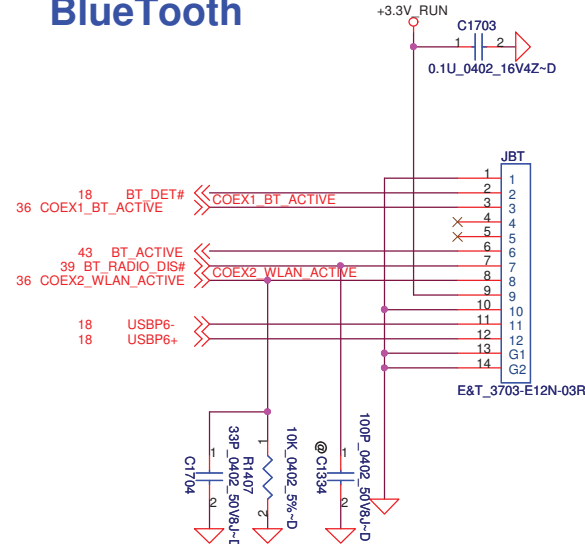
Touch Pad



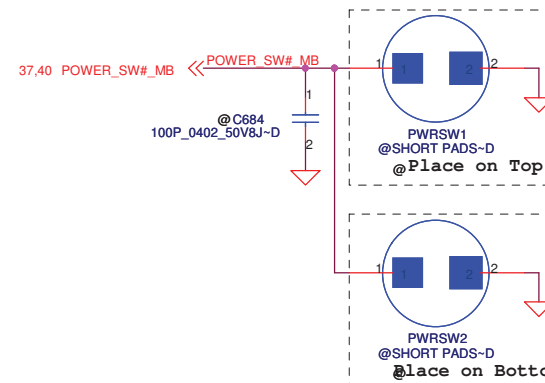
Touch Pad Conn. Pitch=0.5



BlueTooth



Power Switch for debug



@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

@SM CARD BODY

Part Number	Description
SP070007V0L	8 SOCKET TYCO 1770551-1 10P H5.9 SMART

@PCMCIA BODY

Part Number	Description
DC000001Q0L	PCMCIA TYCO 1759096-1

@MDC wire set cable

Part Number	Description
DC02000CS0L	H-CONN SET ZGX MB-MDC

@T/P wire set cable

Part Number	Description
DC02000840L	H-CONN SET ZJX MB-B/T-TP-FP

@LVDS cable

Part Number	Description
DC020003Y0L	H-CONN SET ZJX MB-LCD 14 WXGA+(-1ch)

@LVDS cable

Part Number	Description
DC02000870L	H-CONN SET ZJX MB-LCD 14 WXGA+(-2ch)

@RTC BATT

Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

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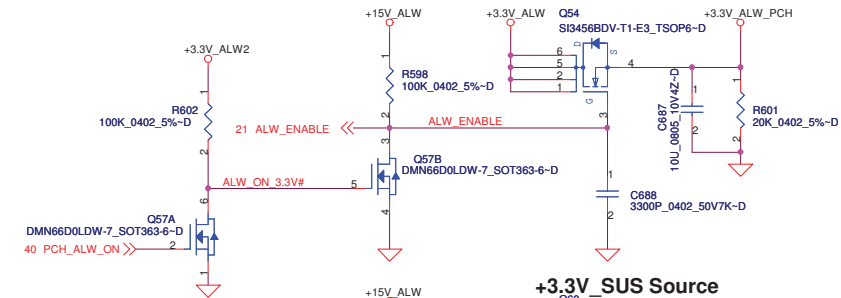
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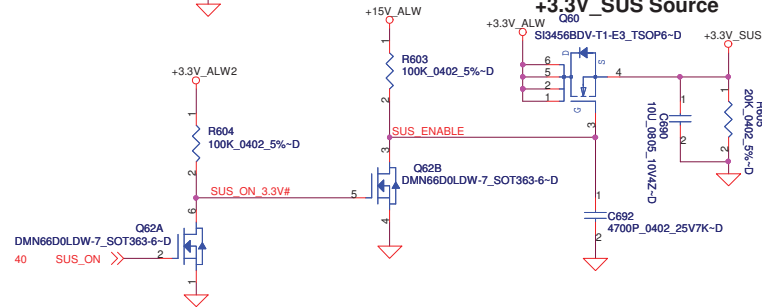
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Touch PAD/Int KB/LID		
Size	Document Number	Rev
	LA-5571P	0.1
Date:	Thursday, January 21, 2010	Sheet 41 of 60

DC/DC Interface

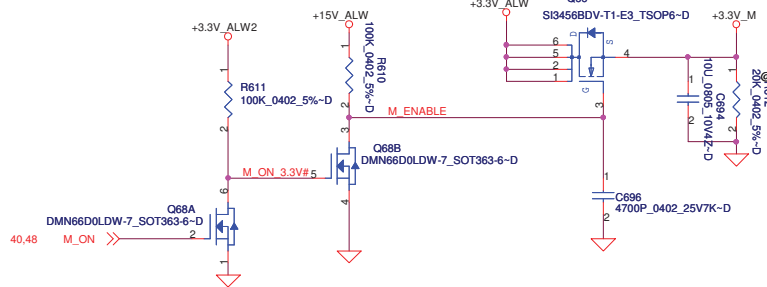
+3.3V_ALW_PCH Source



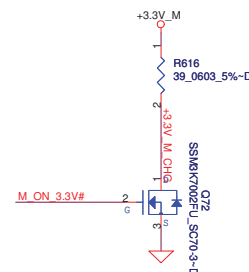
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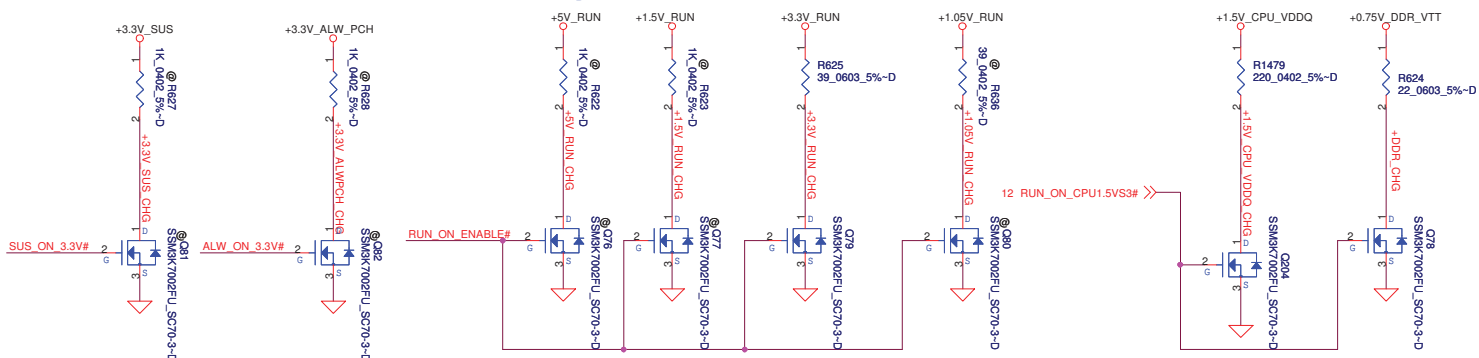
+3.3VM Source



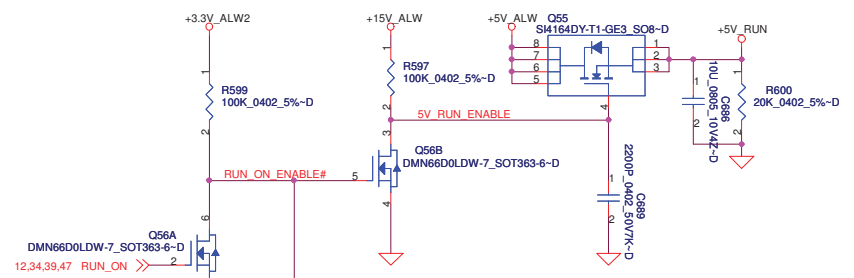
Discharg Circuit



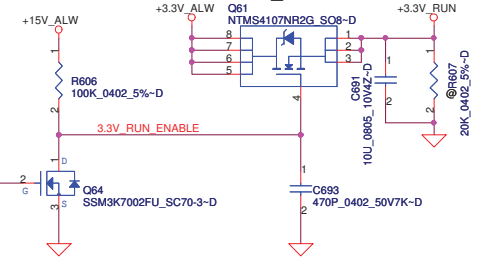
Discharg Circuit



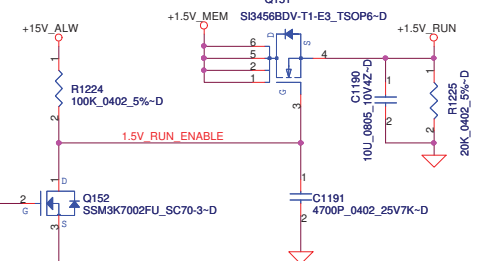
+5VRUN Source



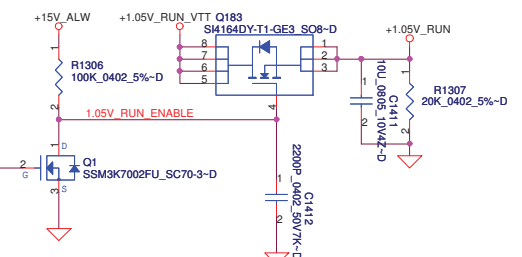
+3.3V_RUN Source



+1.5V_RUN Source



+1.05V_RUN Source



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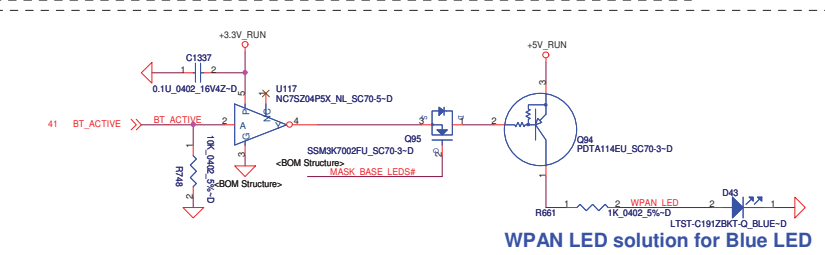
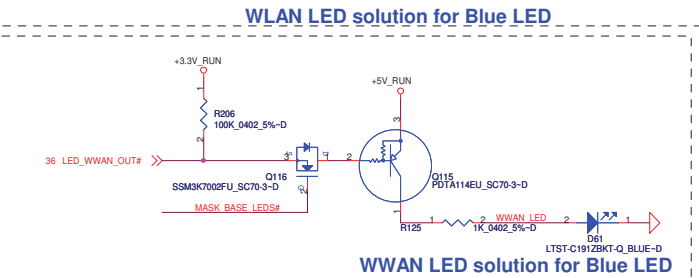
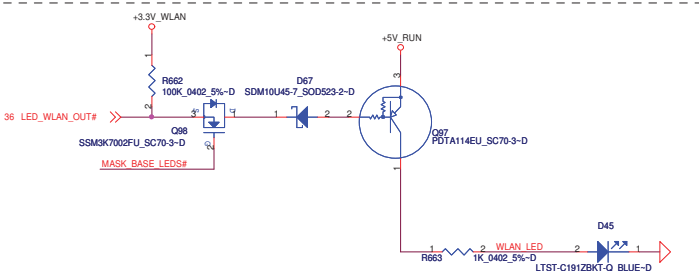
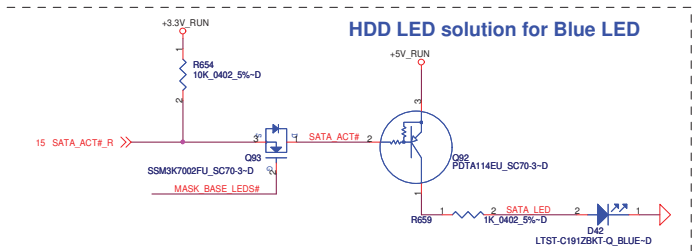
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POWER CONTROL

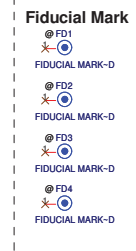
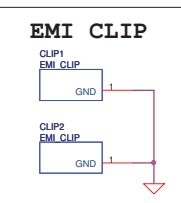
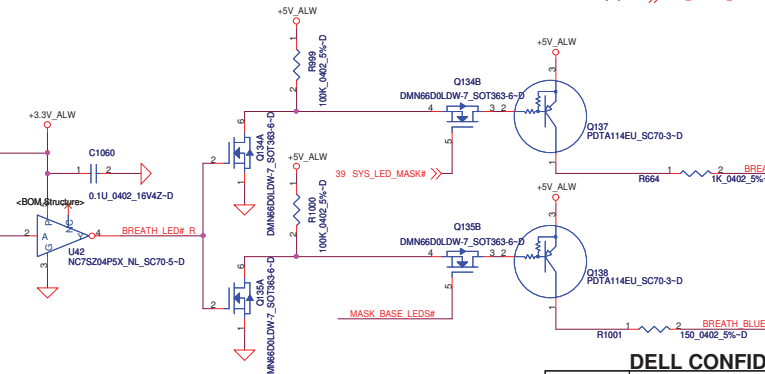
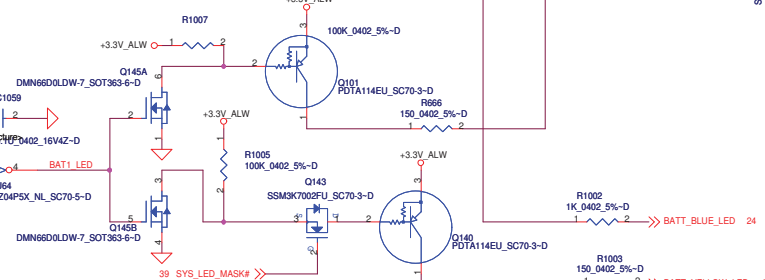
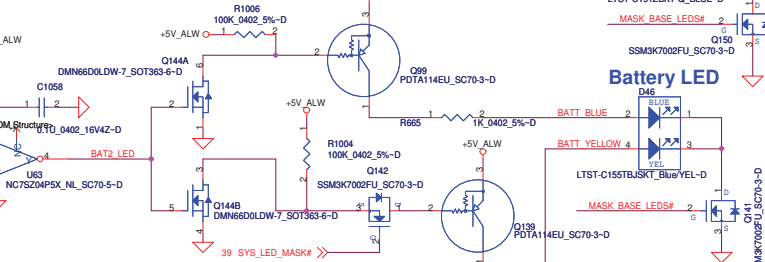
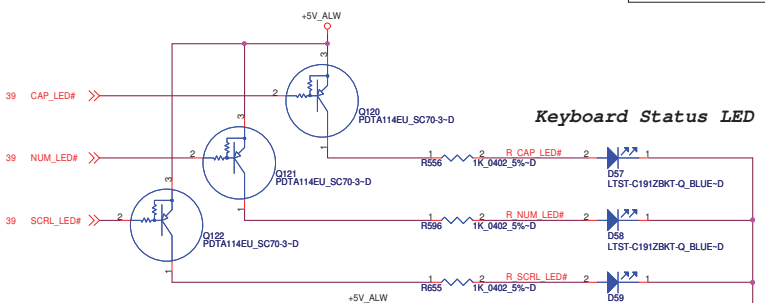
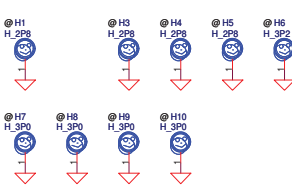
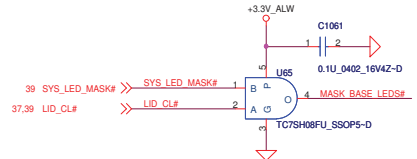
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LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



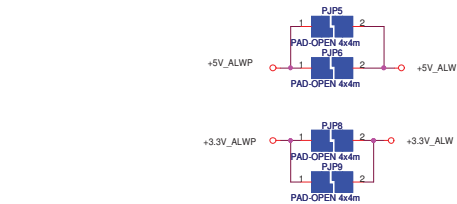
+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2 / +15V_ALWP/ +3.3V_RTC_LDO

5 Volt +/-5%
Thermal Design Current:5.196A
Peak Current:7.423A
OCP_MIN:8.165 A

3.3 Volt +/-5%
Thermal Design Current: 3.971A
Peak current: 5.674A
OCP_MIN:6.808 A

VOUT2=5V
L=3.3uF
Fsw=400KHz
D=0.253
Input Ripple Current=TDC*(D*(1-D))^0.5=2.27A
Output Ripple Current=(19-5)*0.263/3u/400K=2.81A
Output Ripple Voltage=3.1*18m=56.75mV

VOUT2=3.3V
L=3.3uF
Fsw=300KHz
D=0.169
Input Ripple Current=TDC*(D*(1-D))^0.5=1.95A
Output ripple current=(19-3.3)*0.173/3u/300K=1.944A
Output ripple Voltage=1.96*18=48.6mV



+15V_ALW
PAD-OPEN1x1m
(100mA, 20mils, Via NO.=1)

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Title: DC/DC +3V/ +5V

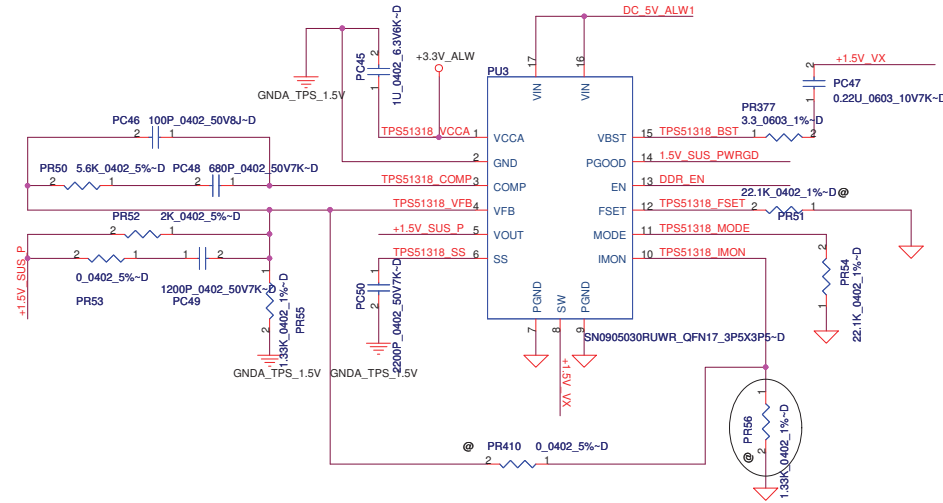
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Date: Thursday, January 21, 2010

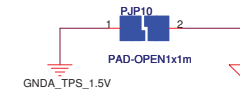
Sheet 45 of 60

Rev 0.1

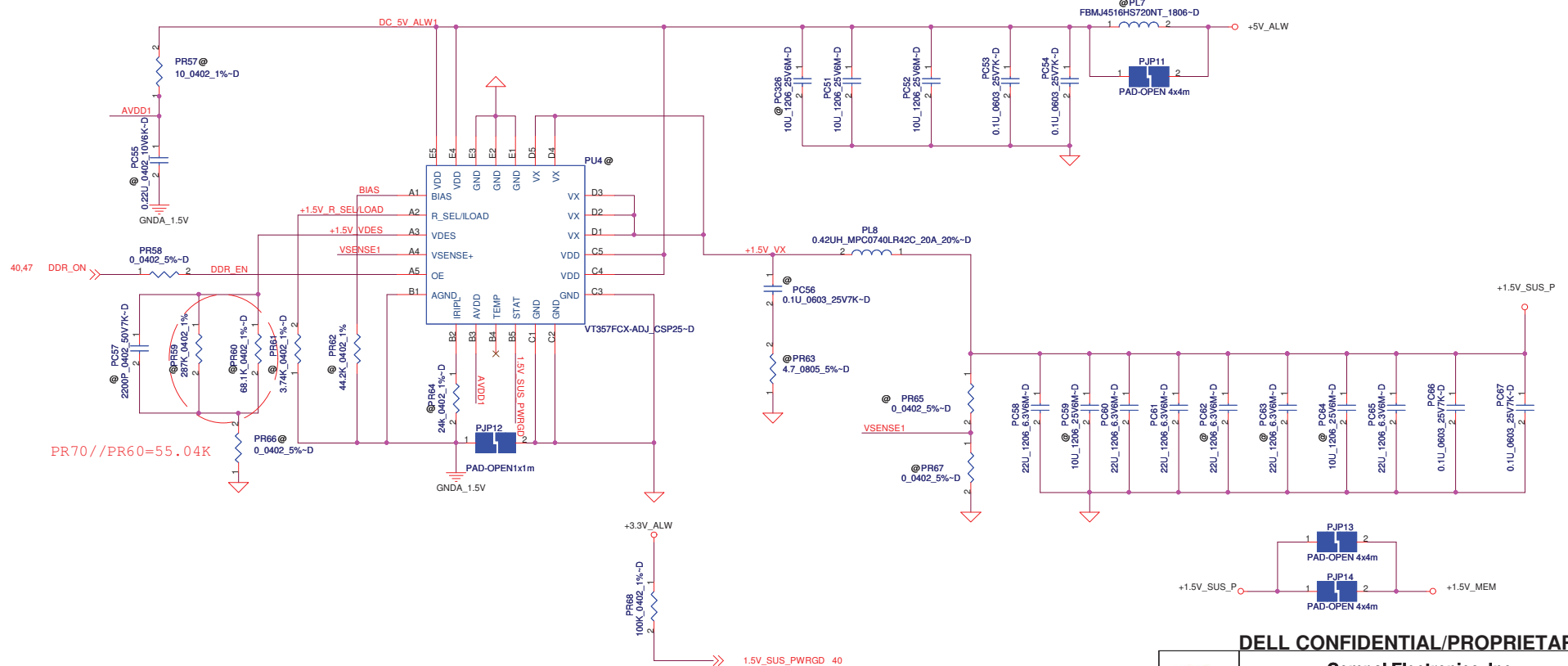
+1.5V_SUS_P (TPS51318)



1.5 Volt +/-5%
Thermal Design Current: 7.876A
Peak current: 11.251A
OCP_MIN:12.376A



+1.5V_SUS_P (VT356)



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+1.5V MEM

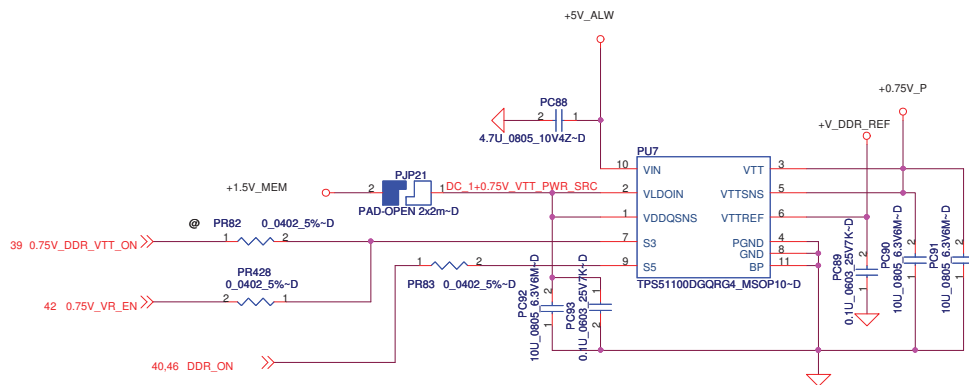
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+0.75V_DDR_VTT
DDR3 Termination



VOUT=1.8V
L=3.3uF
Fsw=290KHz
D=0.092
Input Ripple Current=TDC*(D*(1-D))^0.5=0.884A
Output Ripple Current=1.707A
Output Ripple Voltage=1.707*15m=20.5mV

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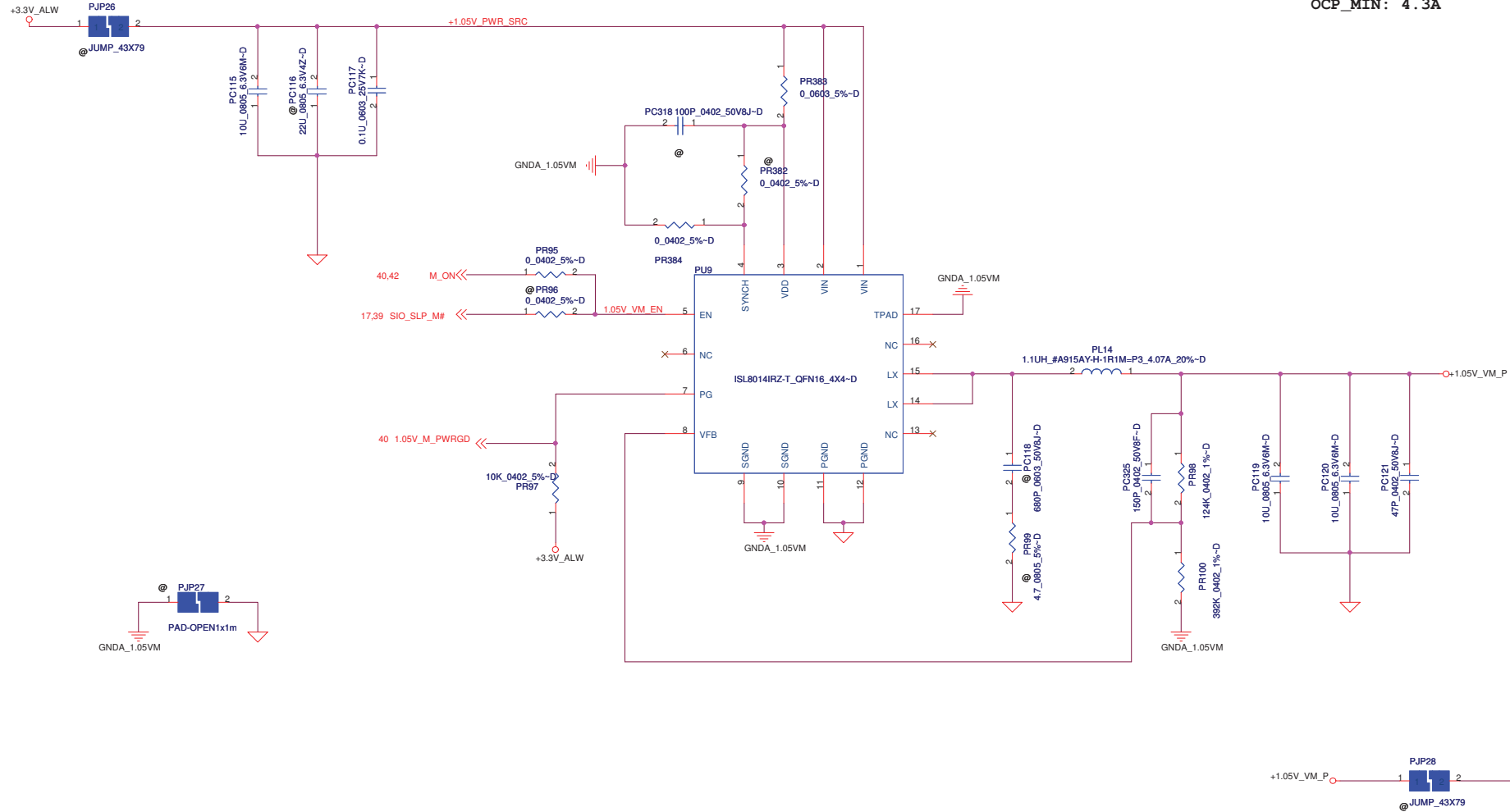
Title	+0.75V DDR VT/+1.8V RUN
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+1.05V_M_P

1.05 Volt +/-5%
Thermal Design Current: 1.518A
Peak current: 2.169A
OCP_MIN: 4.3A

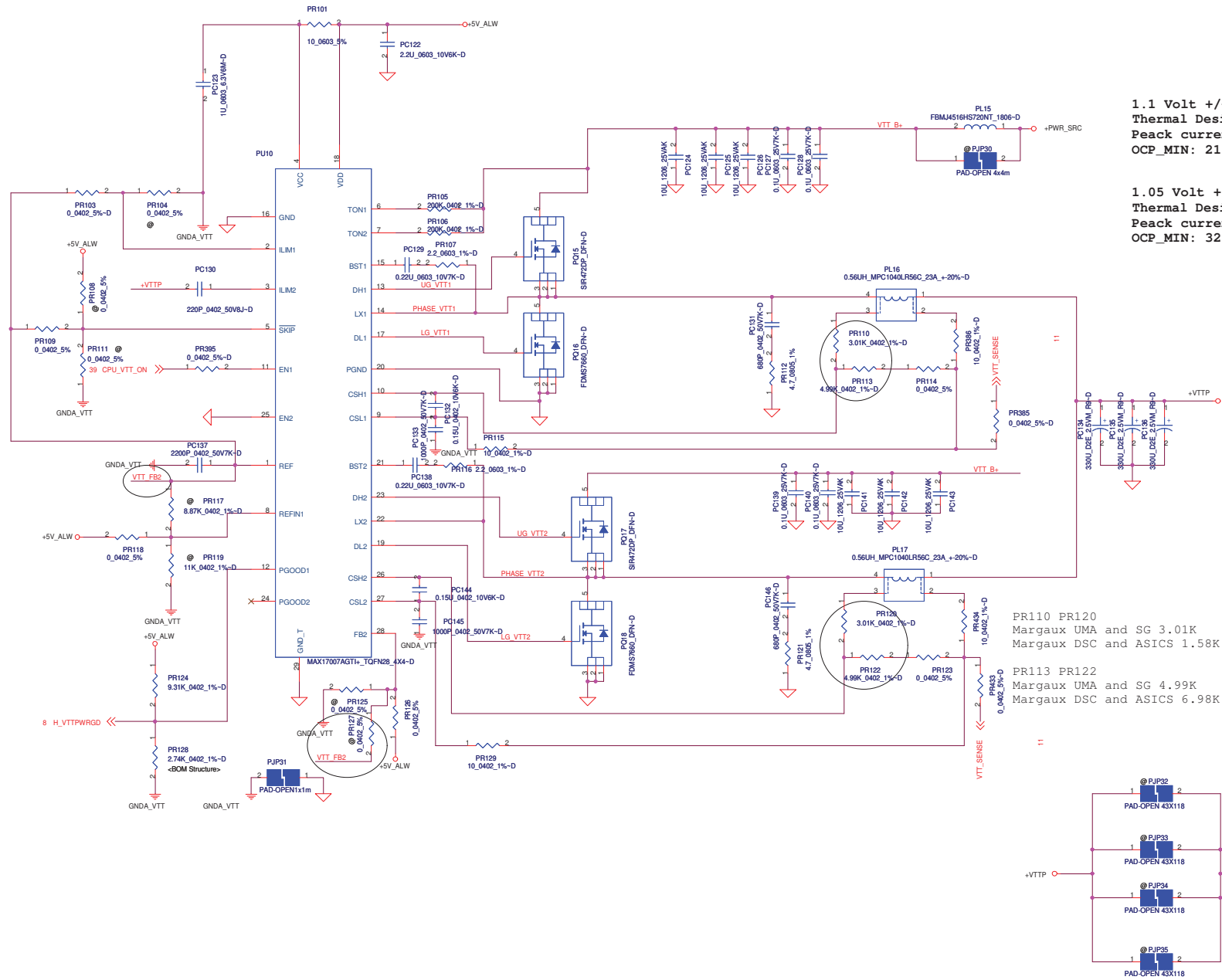


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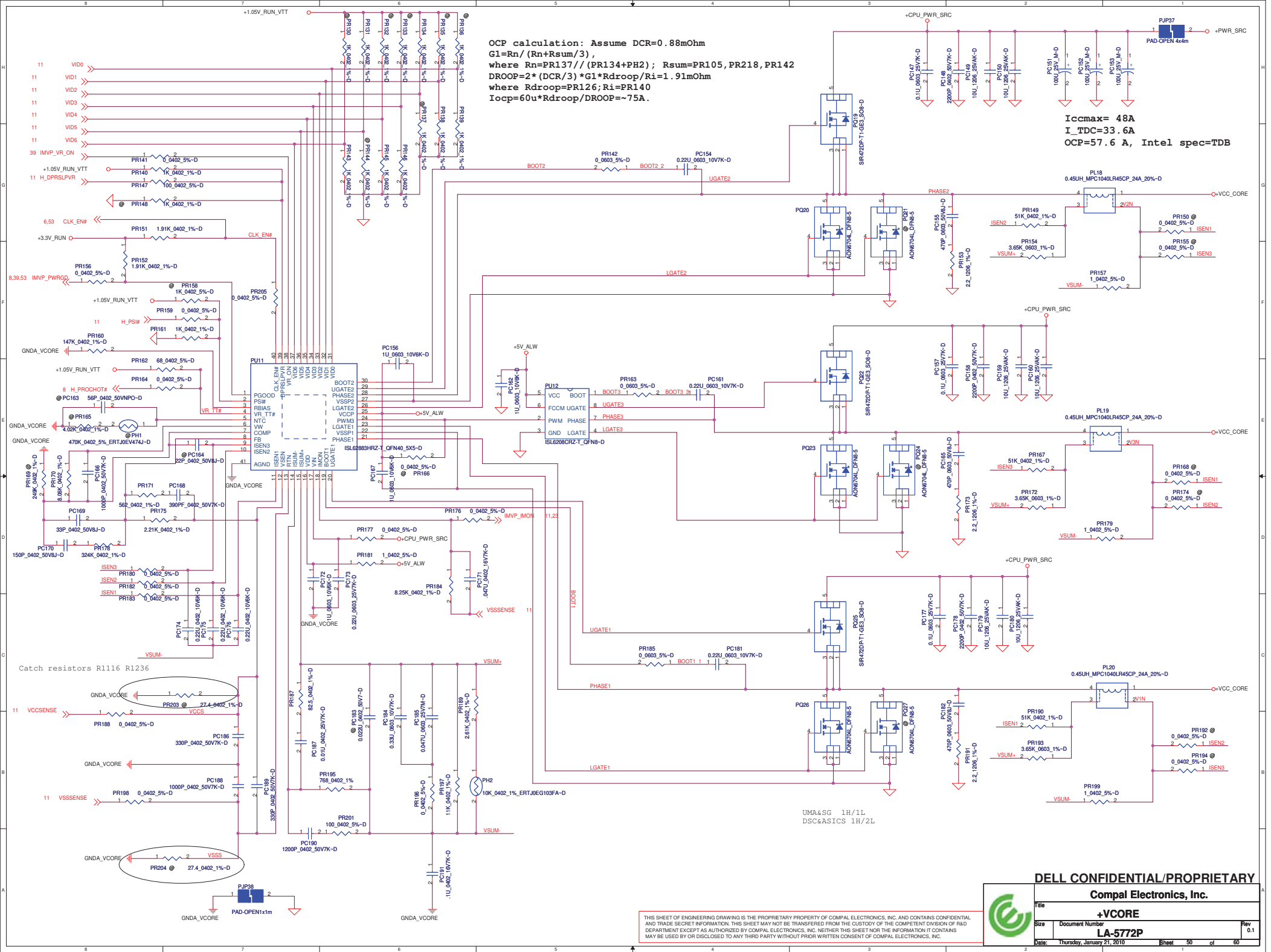
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Title +1.05VM		
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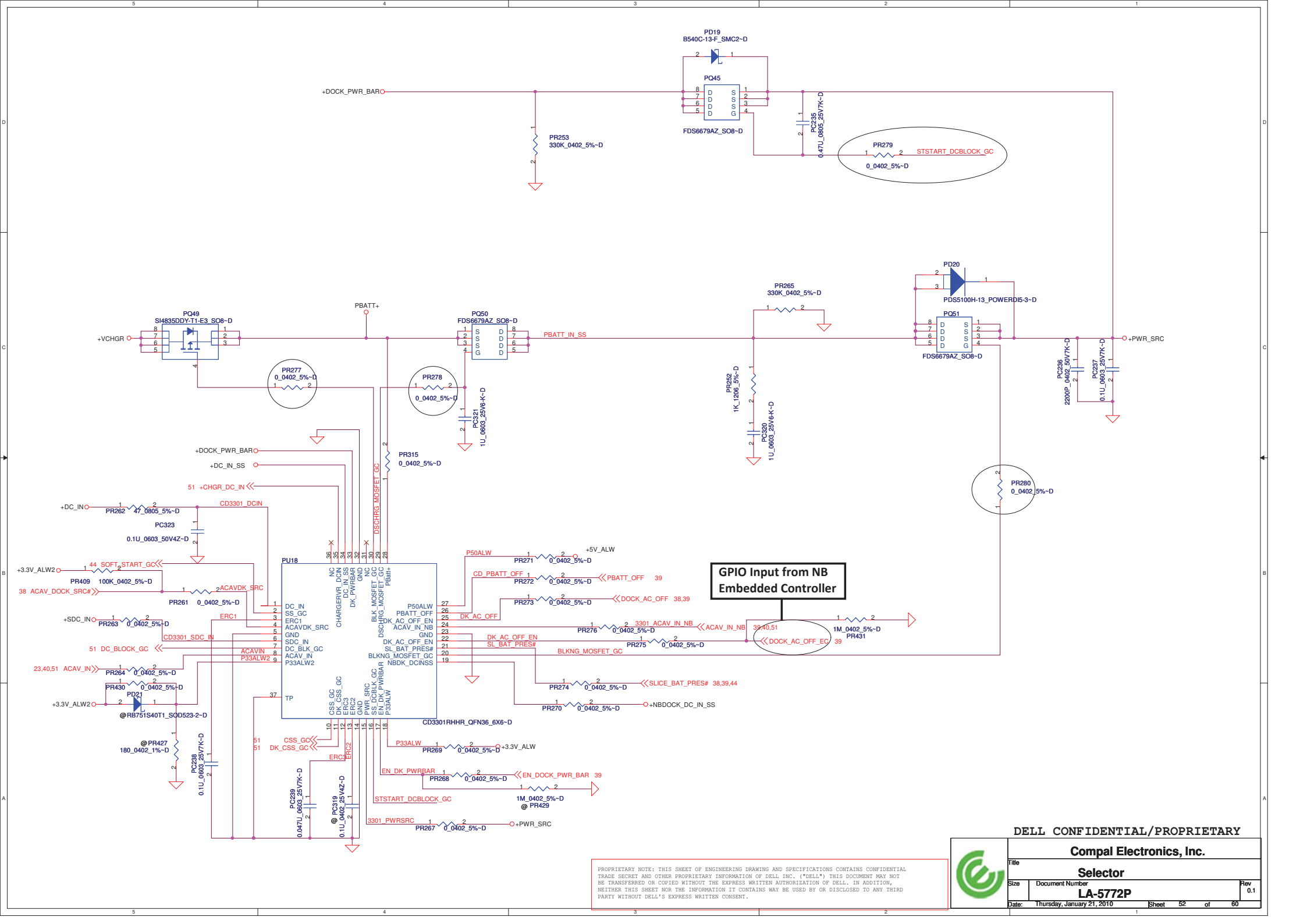
OCP calculation: Assume DCR=0.88mohm
 $G1=Rn/(Rn+Rsum/3)$,
 where $Rn=PR137/(PR134+PH2)$; $Rsum=PR105, PR218, PR142$
 $DROOP=2*(DCR/3)*G1*Rdroop/Ri=1.91mOhm$
 where $Rdroop=PR126$; $Ri=PR140$
 $Iocp=60u*Rdroop/DROOP\approx 75A$

$I_{ccmax}=48A$
 $I_{TDC}=33.6A$
 $OCP=57.6A$, Intel spec=TDB



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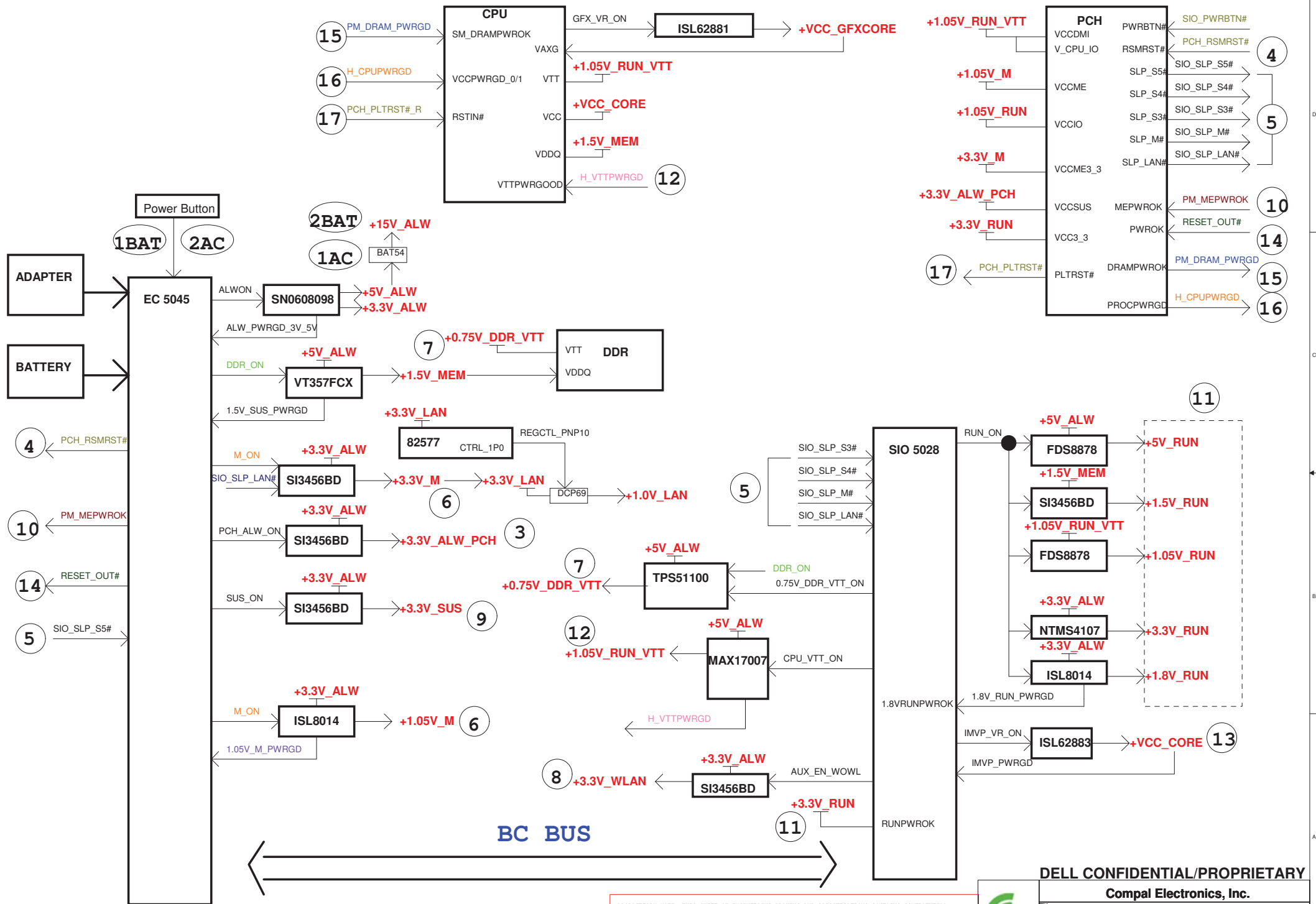


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Power Sequence

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	21	HW	5/19/2009	Intel	Remove R689	R689 is only required is power measurements are planned	X01
2	28	HW	5/19/2009	DELL	Remove AGND	Remove the AGND plane and leave everything as DGND. After discussing with IDT there is no value having AGND plane if there is no AGND plane on the IO board and all along the analog signal path.	X01
3	40	HW	5/19/2009	COMPAL	Board ID	R98 change to 130k ohm	X01
4	31	HW	5/21/2009	DELL	5882 support M25 ROM part	Add U19	X01
5	15	HW	5/27/2009	Intel	ES2 deos not need PU/PD for TRST#	Remove R808 & R1316, add test point	X01
6	31	HW	6/01/2009	Broadcom	Reserve SC_TEST & SCC_CMDVCC_N pad	Add @R775 & R776	X01
7	40	HW	6/02/2009	DELL	to prefent Q18 to glitch	Add R595 100K PD at EN_INVPWR	X01
8	34	HW	6/02/2009	DELL	for U52-STBY to both EXPRCRD_STBY# (Depop 0ohm res) and RUN_ON (Pop 0ohm res) for U52-CPPE to both EXPRCRD_PWREN# (Depop 0ohm res) and Card JEXP1 CPPE# pin 17	Add R684, @R687, depop R683	X01
9	15	HW	6/03/2009	Intel	Follow DPDG & ES2 request	R804 change from 47k to 51 ohm, pop R806 & R1315	X01
10	23	HW	6/03/2009	DELL	Fan solution change to M09 design	POP R507, R516, R519, R529, depop R531, R534, R535, D94-D96	X01
11	23	HW	7/01/2009	SMSC	Fan solution change by SMSC request	Change R1463 from 0.56 to 0.27	X01
12	42	HW	7/01/2009	COMPAL	Cost concern & Rdson concern by ADC	Change Q61 to A04456 & Q55/Q183 to SI4164	X01
13	43	HW	7/01/2009	COMPAL	for derating concern	Change R1001 from 82 to 150 ohm	X01
14	8	HW	7/01/2009	Intel	Follow CRB by Intel request	R1286 needs to change to 0-ohm	X01
15	40	HW	7/01/2009	COMPAL	Board ID	Change R98 to 62K ohm.	X02
16	8,12,13,42	HW	7/13/2009	Intel	Intel S3 reduction circuit.	Add R1469, R1471-R1474, R1476, R1479-R1484, R1487, C1872-C1879, Q199-Q201, Q204-Q207, U141, PJP57, PJP58, PR428, change R624 to 22 ohm, R879 to 1.5K, R880 to 750, pop Q78, add net DDR_HVREF_RST_GATE from U36.A34, CPU1.5V_S3_GATE from U36.A36, change CPU VDDQ net name to +1.5V_CPU_VDDQ connect RUN_ON CPU1.5VS3# to Q78.2 Q204.2,	X02
17	30	HW	7/13/2009	COMPAL	+3.3V_LAN enable control follow M09	De-pop R47	X02
18	8,15	HW	7/14/2009	COMPAL	Depop all related components where are located at 0 Z-hight area	Depop JXDP1, JXDP2, JDEG1, JP2 circuit	X02
19	21	HW	7/14/2009	Intel	Add filter for PCH VCCADPLL/B	Add L97,L98,R1488,C1880-C1883, Remove C105, C106	X02
20	19	HW	7/14/2009	Intel	GPIO1,6,7 PU if not being used	Add R1489-R1491	X02
21	24	HW	7/14/2009	COMPAL	Camera need to be changed from 7 to 8 pin	Change JEDP1 pin definition	X02
22	37	HW	7/16/2009	COMPAL	JTP1, JBI01 power gnd pins redefined	Change JTP1, JBI01 pin definition	X02
23	37,40	HW	7/16/2009	SMSC	LAT_ON_SW# needs to be added a luF cap	Add @C1884, C1885, R1492, change R560 to 100K, JIO.32 change to LAT_ON_SW_BTN#	X02
24	23	HW	7/16/2009	SMSC	R594 has to be a group with R3P circuit	De-pop R594 for M09 fan solution	X02
25	23	HW	7/16/2009	SMSC	Request by SMSC R3P	Remove D94-D96	X02
26	31	HW	7/17/2009	Braodcom	Found both PD R898 and PU R485 pop	depopulate R898 for normal operation	X02
27	31	HW	7/17/2009	Braodcom	RFID disable circuit remove	Remove R1062-R1065	X02
28	16	HW	7/17/2009	Intel	Intel requires the use of the 25Mhz crystal on UMA and SG platforms	Populate Y6, C1168(18pF), R379, R685, R381 change to C1169(18pF).	X02
29	31	HW	7/17/2009	Braodcom	+SC_VCC_Capacitor (C718) Value Change	Broadcom has recommneded changing the value of C718 from .47uF to 220nF	X02
30	42	HW	7/17/2009	COMPAL	Backdrive EA Failure on Margaux/ASICS	Pop R625 and Q79	X02
31	24	HW	7/17/2009	DELL	eDP repeater change to SN75DP119.	update U46 circuit for eDP repeater	X02
32	29	HW	7/17/2009	COMPAL	EMI solution	C676 to 150pF and R1295 to L4 (220 ohm), R1217 change to 47 ohm, pop C673 & R588	X02
33	23	HW	7/17/2009	COMPAL	R3P circuit by SMSC request	R536 depop for 3P FAN, R1457 change to 0 ohm, R138 change to 27K ohm	X02
34	36,39	HW	7/22/2009	DELL	Reconnect the signal UWB_RADIO_DIS#	connect UWB_RADIO_DIS# from EC5028.A56 to MINI3.20	X02
35	23	HW	7/22/2009	DELL	Change FAN solution to M09	De-pop R3P circuit component & pop M09 solution	X02
36	42	HW	7/23/2009	COMPAL	de-rating result fail	Change Q61 from A04456 to NTMS4107	X02

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
37	24	HW	7/23/2009	TI	EDP repeater DP119 vender review request	reserve pop option for X1EDP & DP119, change PU/PD to 20K.	X02
38	28	HW	7/23/2009	DELL	We will never disable the power to HDD redriver, go back connected in SSI	Remove R1493 & delete SATA_PWRSAVE	X02
39	18,28,40	HW	7/23/2009	DELL	There has been some confusion due to the net name showing active low	change net name HDD_FALL_INT1# to HDD_FALL_INT to show correct polarity	X02
40	29	HW	7/24/2009	DELL	use the SiTimes part due to the cost savings	change X4 from TXC to SiTimes.	X02
41	31	HW	7/24/2009	Braodcom	connect pin-L10 of U32 to pin-5 of U33, and disconnect pin-D2 from pin-5 of U33	pop R775, de-pop R776	X02
42	33	HW	7/24/2009	COMPAL	fixed SD/MMC Clock overshoot and undershoot	Changing R8 dumping from 0-ohm to 10-ohm	X02
43	31	HW	7/24/2009	Braodcom	BCM5880 Leakage Issue on Margaux	Add Q208,Q209,R1496 circuit to fix.	X02
44	37,39	HW	7/27/2009	DELL	ESATA repeater power saving	Add a 0 ohm jumper between EN pin and VDD, but no-pop it. Then connect the EN pin to 5028.A47 with a 0 ohm jumper that is popped.	X02
45	39	HW	7/27/2009	DELL	Sometimes VGA_ID_DISC and VGA_ID_UMA both read as low	Change R875 and R881 to +3.3V_ALW rail.	X02
46	26	HW	7/27/2009	Parade	new DP PHY test requirement	change R363 value from 499ohm to 1k ohm	X02
47	23	HW	7/27/2009	SMSC	SMSC review feedback	The pull-up source of the R150 should be changed to +VCC 4002	X02
48	31	HW	7/27/2009	NXP	Better for decoupling noise	Change C1015 ,C633 to 10pf	X02
49	33	HW	7/27/2009	TXC	EA result	C514, C515 have to change to 22pF	X02
50	36	HW	7/27/2009	DELL	For PCH GPIOs rail.	PCIE_MCARD3_DET# & USB_MCARD1_DET# pull-ups (R458 & R438) need to change from +3.3V_ALW_PCH rail to +3.3V_RUN rail	X02
51	23,40	HW	7/29/2009	SMSC	per SMSC 5045 AN 19.6, 4002 AN 16.11	R541, R554, R1492 should be 10K, R147 should be populate, Add R1498	X02
52	35	HW	7/29/2009	DELL	Braidwood has been removed from Ibex Peak platforms	De-pop JBW1 & R1453	X02
53	15,40	HW	7/29/2009	KDS	KDS crystal EA result	change UMA C296 & C297 to 12pF, C674, C675 to 27pF	X02
54	39	HW	7/29/2009	DELL	GPIO MAP update	change net name from RESERVED FOR ESATA to EN_ESATA_RPTR	X02
55	42	HW	7/29/2009	Compal	By Intel S3 timing concern	reserve R1500 & @R1499 0 ohm for Q206.2 from RUN_ON_CPU1.5VS3# & RUN_ON_ENABLE#	X02
56	13,14	HW	7/30/2009	Compal	EMI concern	POP C1121-C1124, C1145-C1148	X02
57	37	HW	7/30/2009	Intel	Intel continues to recommend that all pre-production and production motherboards include common mode choke footprints to enable a stuffing option in case a choke is required to pass EMI testing	Add @L30, @L31, R424-R427	X02
58	31	HW	7/30/2009	Broadcom	Broadcom schematic review request	pop R537; Remove C647, C641,R634, R498, R898; Add @C1886 & @C1887; Remove L73, R631, C1026, R494, Short net RFREADER_TXN1_PI_R to RFREADER_RXP_C; Remove C642, C640, change R487, R496 to 0 ohm; Add @R1501; de-pop R496 & R497; JCS1 pin2 & pin3 and pin4 & pin5 should be short to carry higher current.	X02
59	31	HW	7/30/2009	Compal	Solve smart card cage vender reverse pin definition.	Reverse JSC1 pin definition	X02
60	27	HW	7/31/2009	Compal	CRB EA result	C390, C518, C996, C251-C253 to 4.7pF; L61-L63 to 5-Ohm Bead	X02
61	31	HW	7/31/2009	Broadcom	Broadcom schematic review request	The pin1 of R497 and R496 should be connected to GND	X02
62	8,15	HW	7/31/2009	Intel	For XDP debug concern	Populate all the resistors and leave out the connector	X02
63	27	HW	8/03/2009	Compal	CRB EA result	C251-C253 to 3.3pF; L61-L63 to 10-Ohm Bead ; De-pop C996, C518, C390	X02
64	23	HW	8/03/2009	Compal	If populate R147 PU resistor for THERM_STP#, it will impact ALWON signal at MEC 5045	De-pop R147	X02
65	30,33	HW	8/04/2009	KDS	KDS crystal EA result	change UMA C427 change to 200 ohm, C514, C515 back to 15P and change X3 from CL=16pF to CL=12pF	X02
66	8	HW	8/05/2009	DELL	fix the Intel S3 power up timing	change C1877 from 0.01uF to 0.22uF 0402 cap.	X02
67	21	HW	8/05/2009	Intel	WW30 Calpella MoW	Intel request change L97 & L98 to 10uH, DCR=0.36 ohm	X02

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68	28, 37	HW	8/06/2009	Compal	Per ESATA/SATA EA result	pop R1301, R1304, de-pop R1298, R1308	X02
69	10, 26, 38	HW	8/06/2009	Intel	Per Intel check list rev1.6	change R186, R796, R798 from 100k to 110k ohm, R1109 to 3.3K ohm	X02
70	28	HW	8/06/2009	Compal	ODD_DET# PU from +5V_MOD to +3.3V_RUN	connect R1239.1 to +3.3V_RUN & pop R1239	X02
71	42	HW	8/06/2009	SMSC	Watch dog timer may not be resetED when 4002 VDD_PWRGD is not completely at Logic Low	Pop R616 to 39 & pop Q72	X02
72	30	HW	8/10/2009	Intel	Remove the VCT trace	Remove @R562, @C41	X02
73	35	HW	8/10/2009	DELL	Braidwood Removal on RAM	Remove @JBW1, @C1851, @R1452, @R1453, @C1852, R1411	X02
74	31	HW	8/11/2009	Broadcom	Broadcom review request	Remove @R1061, Change C718 value to 470pF, change C646 value to 220pF. pin2 of R470 should have a 0ohm but de-pop resistor to USB_GPIO27 net. add @R1504 for DDR3_DRAMRST#_CPU PD & add C1888 for PM_DRAMRST# to slow down gate of FET	X02
75	8	HW	8/11/2009	Intel	Intel review request	Change C21 from 10U to 47U, change R46 to C1889 (1uF)	X02
76	33	HW	8/11/2009	Richo	Change pop option for R5U242	Change Q3 to BSS138	X02
77	24	HW	8/12/2009	DELL	EDP_HP signal may too low to turn on FET.	No stuff C111 and C112	X02
78	21	HW	8/12/2009	Intel	Follow CRB rev 1.6 schematic	pop R496 & R497 (0 ohm)	X02
79	31	HW	8/12/2009	Broadcom	Per Broadcom request	change R772 to 47 Ohm for resolving SC_CLK Rise/Fail timing issue	X02
80	31	HW	8/12/2009	Compal	Smart card EA result	pop R1504 & change C1888 to 470pF	X02
81	8	HW	8/12/2009	Intel	Follow Intel S3 white paper rev0.9	rename IO VCT to +LOM_VCT_IO & reserve C712 pad for test.	X02
82	37	HW	8/12/2009	Compal	disconnect IO & DOCK VCT	need to have 4.7K pull-up to 3.3V_ALW for BCM5882 pin-C1 "RSTOUT_N"	X02
83	31	HW	8/13/2009	Broadcom	Per Broadcom request	change C1888 to 0.1u, add @R1511 for PM_DRAM_PWRGD_R	X02
84	8	HW	8/13/2009	DELL	Avoid a glitch for DDR_HVREF_RST_GATE, please add a 1.1K 1% no-stuff pull-up to +1.5V_CPU_VDDQ rail on the PM_DRAM_PWRGD_R signal for a back-up option		
85	8, 45	HW	8/13/2009	DELL	CPU detection since the edge diode has been removed from M'09	Add R1512 for CPU_DETECT# and connect JCPU.AH24 to U36.B18	X02
86	37	HW	8/14/2009	DELL	Invert the EN_ESATA_RPTR signal and connect this to SATAGP4/GPIO16	Add @R1513 & @Q210, pop R1494 and de-pop R1497, change net name from GPIO16 to EN_ESATA_RPTR#	X02
87	33	HW	8/14/2009	Compal	Solve 1394 impedance issue	Change R399, R400, R401, R403 to 54.9 ohm.	X02
88	37	HW	8/14/2009	Compal	EMI solution	pop L30 & L31, de-pop R424-R427	X02
89	11, 12	HW	9/11/2009	Compal	Per PWR EA result	De-pop C66, pop C1090, C1091	X02
90	16	HW	9/11/2009	KDS	crystal EA result	Y6 change to CL=12pF & change C1168 & C1169 to 12pF.	X02
91	33, 34	HW	9/11/2009	COMPAL	EMI solution for SD CLOCK & EXP card USB	R8 change to 22 ohm, pop L64 & depop R791, R792	X02
92	21	HW	9/11/2009	Intel	Intel request	de-pop C39, C610	X02
93	31	HW	9/11/2009	Broadcom	Broadcom review feedback	change C718 from 470p to .47u, C646 from 220p to .22u	X02
94	30	HW	9/11/2009	Intel	Follow Intel document request	change R1502 to C427 10pF, C475, C476 to 33pF	X02
95	12	HW	9/11/2009	DELL	Intel S3 circuitry issue on Margaux UMA	change C1873 from 4700p to 0.01uF	X02
96	21	HW	10/15/2009	Intel	Isolate pins AF32, AF34 and AH34 of PCH	Add C1893.	X02
97	35	HW	10/23/2009	Compal	Add PD 10k for Minicard PWR	Add R1523-R1525	X03
98	31	HW	10/23/2009	Compal	Smart card connector DFM issue	change JSC1 type (the same with Rothschild)	X03
99	40	HW	10/23/2009	COMPAL	Board ID	Change R98 to 4.3K ohm.	X03
100	17, 21	HW	10/23/2009	Intel	Intel schematic check list 2.0 request	R268 change from 1k ohm to 10k ohm, de-pop C1881 & C1883	X03
101	40	HW	10/23/2009	SMSC	SMSC review feed back	R561 and R1046 are too large it is recommend that no PU/PD be larger than 100K	X03
102	12, 42	HW	10/23/2009	COMPAL	avoid double bleed off	+3.3V_M, +3.3V_RUN, +1.5V_CPU_VDDQ power plane discharge circuit have been pop, de-pop R612, R607, R1471.	X03
103	36	HW	10/23/2009	DELL	support WiMax LED status	Need to populate R840	X03
104	40	HW	10/25/2009	KDS	KDS Crystal EA result	change C674, C675 from 27pF to 33pF	X03
105	16, 32	HW	10/25/2009	COMPAL	Change R910 placement	Please put R910 close to PCH not TCM chip	X03
106	41	HW	10/25/2009	COMPAL	Touch Pad PU need to move from 5V to 3V	R613, R614 change power rail from +5V_ALW to +3.3V_ALW	X03
107	31	HW	10/28/2009	Broadcom	For 5882-B0 request	L71, L72 68nH, 2%, 400mA; C1070, C1071 1500pF, 2%, 50V; C1886, C1887 150pF, 2%, 50V	X03

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108	29	HW	10/28/2009	IDT	create a low pass filter with the pole set at 36kHz to filter out of band noise	de-pop C1066 & C1067, R1090, R1089 ; R340 & R342, R1091 & R1092 change to 2k, add C1894-C1897 1000pF.	X03
109	24	HW	10/28/2009	COMPAL	EMI concern	add 220 ohm bead for BIA_PWM_PCH	X03
110	29	HW	10/28/2009	COMPAL	ME request for JSPK1 swap	JSPK1 Pin 2 and pin 4 swap, pin 3 and pin 5 swap	X03
111	17	HW	10/29/2009	COMPAL	PCH CRT DDC pin up to 3.8V	add CRT DDC level shift, Q217, @R1526, @R1527	X03
112	8,12,13, 15,16,28	HW	10/29/2009	DELL	MEM SMBus design needs to change	Move Q190 connection, add R1528,R1529, add net name DDR_XDP_CLK/DAT	X03
113	31	HW	10/29/2009	DELL	smart card clock resistor	Change R772 from 47 ohm to 22 ohm	X03
114	37	HW	10/29/2009	COMPAL	EMI concern	pop R15 with 10 ohm and C15 with 10pF	X03
115	36	HW	10/29/2009	COMPAL	USB MCARD2_DET# change to +3.3V_ALW_PCH	R447 pull up should change to +3.3V_ALW_PCH	X03
116	40	HW	10/29/2009	COMPAL	avoid RESET_OUT# double PD	de-pop R5	X03
117	15	HW	11/02/2009	COMPAL	EMI, RF team concern	pop C300, C302	X03
118	24	HW	11/04/2009	COMPAL	LCD power sequencing issue	change R161 from 470 to 130 ohm	X03
119	37	HW	11/05/2009	COMPAL	EMI concern	Change choke vender from Murata to Delta on L30,L31	X03
120	29	HW	11/05/2009	COMPAL	RF team concern	X4 change from Sitime to TXC	X03
121	15	HW	11/05/2009	COMPAL	RTC issue	Y1 & Y4 change from 30ppm to 10ppm.	X03
122	15	HW	11/05/2009	COMPAL	For flash ROM EOL issue	U13 change from W25X32 to W25Q32	X03
123	19	HW	11/09/2009	DELL	PCH driving the siganl low at GPIO15 initial	add R1530 2.2K PU resistor to +3.3V_ALW_PCH on the SIO_EXT_WAKE# signal	X03
124	39	HW	11/10/2009	DELL	add a 10K 5% PU to +3.3V_RUN on ME_FWP	Add R1531	X03
125	12	HW	11/11/2009	COMPAL	Surge voltage found at UMA GFX core	R358 changed from 4.7k ohm to 470 ohm	X03
126	8,15	HW	11/13/2009	COMPAL	To cut redundant trace for SMBUS	Add @R1532/R1533/R1536/R1537	X03
127	19	HW	11/17/2009	Intel	By Intel check list request	Add R1543 & R1544 for PCH GPIO22/34	X03
128	41	HW	12/24/2009	Compal	To solve touch pad ESD issue	Change L41 and L42 to R1545 & R1546 with 100 ohm.	X03
129	29	HW	12/24/2009	Compal	RF noise issue concern	change Sitime 12MHz oscillator X4 to driver strength 1x	X03
130	15	HW	12/24/2009	Intel	Follow Intel check list rev2.0	Change R224 to tolerance from 5% to 1%	X03
131	36	HW	12/24/2009	DELL	Wimax LED abnormal operation.	de-pop R1409	X03
132	38	HW	12/24/2009	Compal	Simplo battery slice EMI issue	Add C1899 and C1898(Depop,reserve for EMI test)	A00
133	31	HW	12/24/2009	Braodcom	By Broadcom request	Change L71,L72 from 68nH to 150nH, C1070,C1071 from 1500pF to 390pF.C1887, C1888 from 150pF to 390pF.	A00
134	40	HW	12/30/2009	DELL	Board ID	Change R98 from 4.3K to 1K for A00	A00
135	33,34	HW	12/30/2009	COMPAL	Change R5U242 to rev ES3	Change U94 from ES2 to ES3	A00
136	8,15	HW	12/30/2009	Intel	De-pop XDP & JTAG resistor	de-pop C19,C20,R6,R7,R68,R19,R3,R1153,R1156,R1157,R66,R1241,R780-R785, R22,R24,R78,R91,R101-R116,C1375,R69,R118,R123,R804,R807,R805,R806,R1281, R1282,R1315	A00
137	24	HW	01/14/2010	COMPAL	RF team concern	reserve C1900 for PWM	A00
138	28,37	HW	01/15/2010	COMPAL	Change Esata repeater for power save	Change U95 U96 from 412 to 412A	A00
139	11	HW	01/18/2010	COMPAL	No stuff MLCC caps to fix Acoustic noise	de-pop C50, C52, C57, C59	A00
140	15	HW	01/21/2010	COMPAL	For factory to do JTAG test	Pop R123, R804-R807, R1281, R1282, R1315	A00

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1	52	Selector	6/1	Compal	CD3301 burn issue	Change PR262 to 47_ohm, add PC323 0.1uF. Add PR409 pull up to +3.3V_ALW2. Delete PR266, add PD21 RB751.	
2	49	+1.05VTT	6/1	Compal ADC Guangyong	Change high side MOS to power pak	Change PQ15 PQ17 to Power pak SIR472DP.	
3	47	+0.75_DDR_VT/ +1.8V_RUN	6/1	Compal ADC Guangyong	Add type 3 cap	Add PC324 150pF	
4	48	+1.05V_VM_UMA	6/1	Compal ADC Guangyong	Add type 3 cap	Add PC325 150pF	
5	46	1.5V_MEM_UMA	6/1	Compal ADC Guangyong	Add droop resistor and input cap.	Add PR410 PC326	
6	47	+0.75_DDR_VT/ +1.8V_RUN	6/1	Compal ADC Guangyong	optimize ISL8014	change PR78 to 10K_ohm change PC81 PC85 PC86 to 10uH unpop PC82 unpop PR379 pop PR381	
7	48	+1.05V_VM_UMA	6/1	Compal ADC Guangyong	optimize ISL8014	change PR97 to 10K_ohm change PC115 PC119 PC120 to 10uH unpop PC116 unpop PR382 pop PR384	
8	50	+VCORE	6/8	Intersil	Change Isen resistor to 11K	Change PR149 PR167 PR190 to 11K_ohm SD03411028L	
9	46	+1.5V_MEM_UMA	6/11	Compal / TI	+1.5V_MEM_UMA output voltage over 2V	unpop PR56	
10	44	+DCIN	6/3	Dell	remove PBAT_ALARM# (6/3 Youssef_Daou)	delete DP5 PR6	
11	50	+VCORE	7/14	Dell / intersil	change Cisense GND to VSUM-	PC174 PC175 PC176 pin2 connect to VSUM-	
12	45	+5V/+3.3V	7/14	Compal ADC Guangyong	change 7*7 & 5*5 choke for cost down	change PL5 from SH00000H90L to SH00000FN0L change PL6 from SH00000HE0L to SH00000HR0L change PL11 from SH00000HE0L to SH00000H00L change PL14 from SH00000HE0L to SH00000HY0L	
13	52	Selector	7/14	TI	CSS GC logic wrong issue	Add PR427 180_ohm to GND	
14	53	ISL62881_UMA	7/16	intersil	change Rbias to 47K_ohm	change PR292 to 47K_ohm	
15	52	Selector	7/16	Compal	Add 1M_ohm pull down to fix ACAV_IN_NB oscillation when battery mode S5	Add PR429	
16	50	+VCORE	7/16	intersil	change Isense resistor to 51K_ohm	change PR149 PR167 PR190 to 51K_ohm	
17	52	Selector	7/22	TI	new version CD3301 (PG2.1) dont need PD21	un-pop PD21 add PR430	
18	52	Selector	7/22	TI	DOCK_AC_OFF_EC floating issue	add PR431	
19	53	ISL62881_UMA	7/22	Intersil	change frequency to 300K	change PR293 to 10K	
20	53	ISL62881_UMA	7/22	Intersil	change Rsum to 0603 package improve Vout accuracy	change PR307 from SD03436518L to SD01436518L	
21	50 / 53	+VCORE / ISL62881_UMA	8/10	Compal	change thermistor from 0603 to 0402 package for cost down	Change PH2 PH3 from SL200000B0L to SL20000100L	

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