



Compal Confidential

Nvdia(T30L) + DDRIIIL

V0JET (A210)_ LA8981P

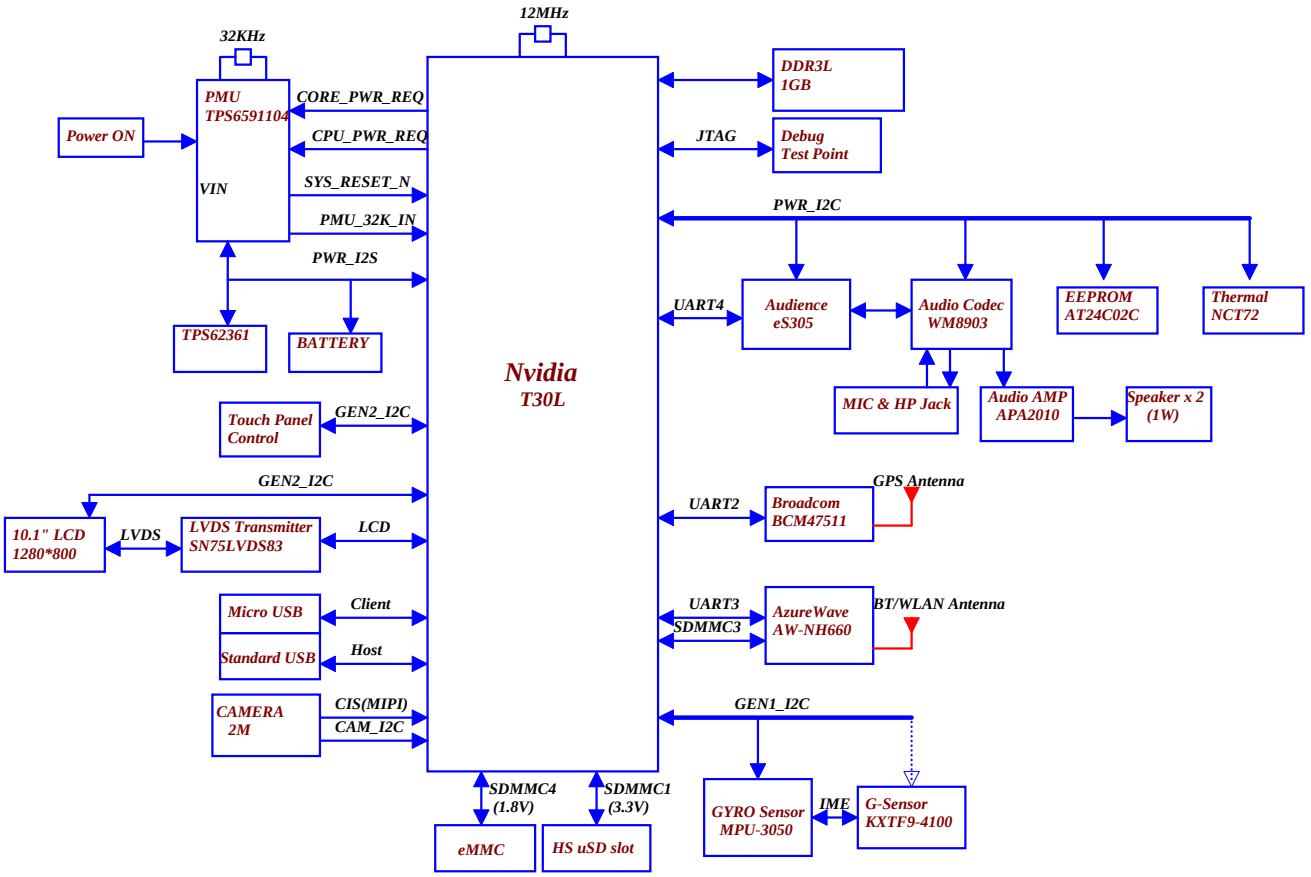
2012-06-11 REV: 1.0

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Model Name : NVIDIA T30L System Block Diagram



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Voltage Rails

Power Plane		ACIN	DCIN	IDLE	Standby
VIN	Adapter power supply (1.2V)	ON	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
VDD_5V0_SBY	Power for always-on	ON	ON	ON	ON
VDD_1V8_PMU_VRTC	Power for RTC and always-on core logic	ON	ON	ON	ON
VDD_1V2_MEM					
VDD_1V35_DDR3_MEM	DDR RX power rail	OFF	OFF	ON	
VDD_1V0_GEN	T30 VDD_CPU Power	OFF	OFF	ON	
VDD_1V2_SOC	T30 VDD_CORE Power	OFF	OFF	ON	
VDD_1V35_DDR3_MEM	DDR power rail	OFF	OFF	ON	
VDD_PMU_LDO1		OFF	OFF	ON	
VDD_PMU_LDO2		OFF	OFF	ON	
VDD_PMU_LDO3		OFF	OFF	ON	
VDD_PMU_LDO4 (VDD_1V2_RTC_TEGRA)	T30 VDD_RTC power rail	OFF	OFF	ON	
VDD_PMU_LDO5 (+VDD_3V3_SDMMC1_TEGRA)	T30 VDDIO_SDMMC1 power rail	OFF	OFF	ON	
VDD_PMU_LDO6 (+AVDD_1V2_DSI_CSI_TEGRA)	T30 AVDD_DSI power rail	OFF	OFF		
VDD_PMU_LDO7 (+AVDD_1V1_PLL_TEGRA)	T30 AVDD_PLL power rail	OFF	OFF		
VDD_PMU_LDO8 (+VDD_1V0_DDR_HS_TEGRA)	T30 VDD_DDR_HS power rail	OFF	OFF		
+5VS	5V System power rail	OFF	OFF		
+3VALW	3.3V System power rail	OFF	OFF		
+3VS	3.3V power rail for standby mode	OFF	OFF		
VDD_1V8_GEN	1.8V System power rail	OFF	OFF		
+VDD_1V8_USB_PLL_TEGRA	T30 USB power rail	OFF	OFF		
+T30S_USB1	USB power rail	OFF	OFF		
+VDD_2V85_EMMC	Core voltage for EMMC	OFF	OFF		
+LEBDVDD	LCD power rail	OFF	OFF		
+LCDVDD	LCD power rail	OFF	OFF		
+VDD_1V8_AUDIO_LDO	Audio power rail	OFF	OFF		
+2.8V_2M_AVDD_R	CAMERA power rail	OFF	OFF		
+VDD_3V3_SDCARD	Micro SD power rail	OFF	OFF		
+VDD_CAM_1V8	CAMERA power rail	OFF	OFF		
+VDD_3V3_FUSE_TEGRA	T30 VPP_Fuse power rail	OFF	OFF		
+VDD_1V8_SENSOR	3.3V Sensor power rail	OFF	OFF		
+VDD_3V3_SENSOR	3.3V Sensor power rail	OFF	OFF		

Bom Structure	01 BOM
A210@	V
A211@	NU
GPS@	V
GS@	NU
LDO@	V
ME@	V
NH660@	V
NONLDO@	NU
SD16GB@	NU
SD8GB@	NU
SS16GB@	NU
SS8GB@	V
WIFI@	V
X76@	V
X76-H@	V
X76-S@	NU

V0JET (A210)

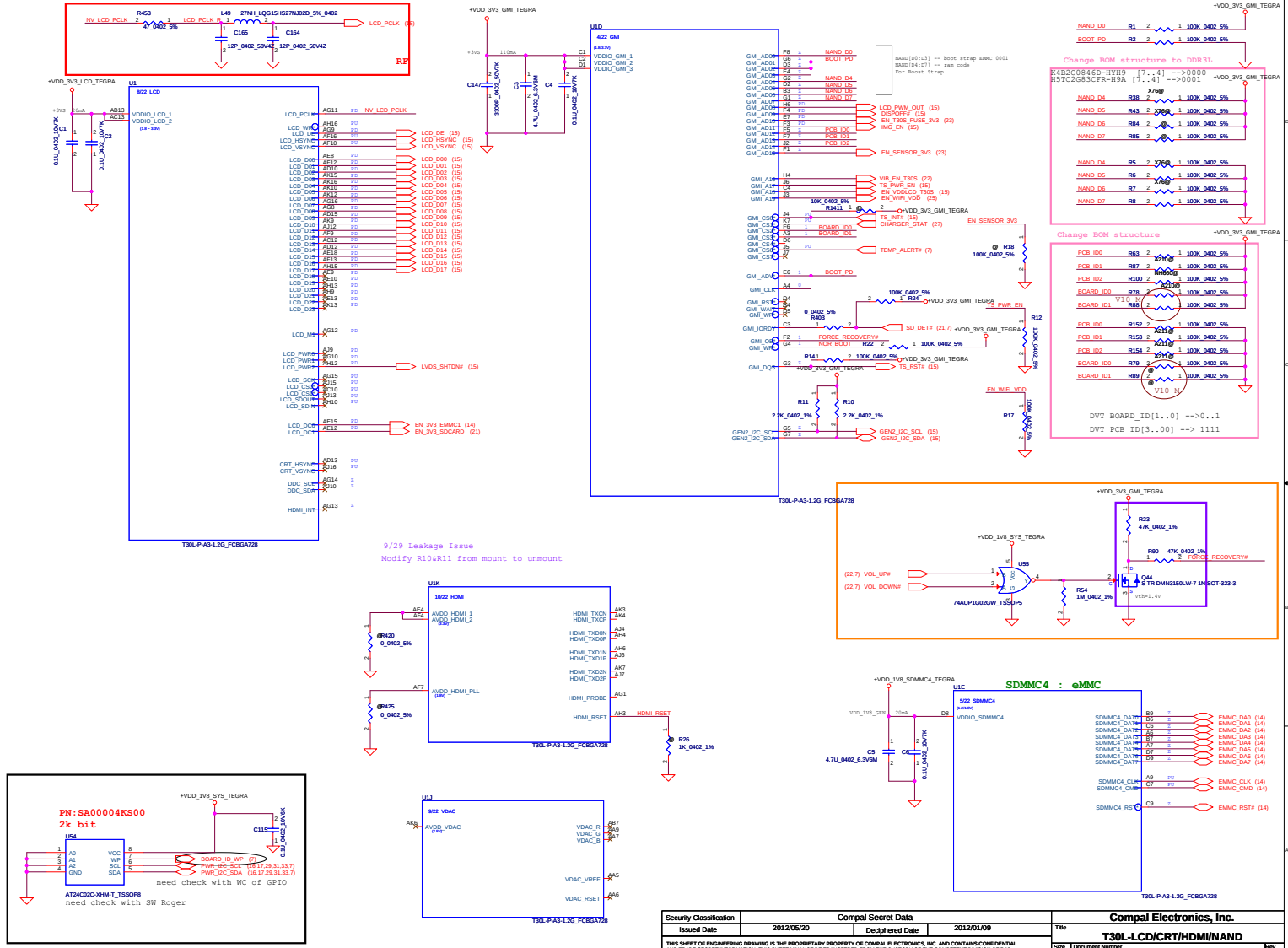
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PCB_ID0	H	H	H		L: A211	H: A210
PCB_ID1	H	H	H		L:	H: NH660
PCB_ID2	H	H	H		L: A210/A211	
PCB_ID3	H	H	H		L: H: A210/A211	

V0JET	Vender PN	Acer PN	NAND_D4	NAND_D5
DDR3L	K4B2G0846D-RYH9 (Samsung)	KN.2GB08.038	0	0
	H5FC2G83CPR-H9A (Hynix)	KN.2GB0G.003	1	0
	FD3J1088D8G-D3-FE1 (Elipida)	KN.2GB09.001	0	1

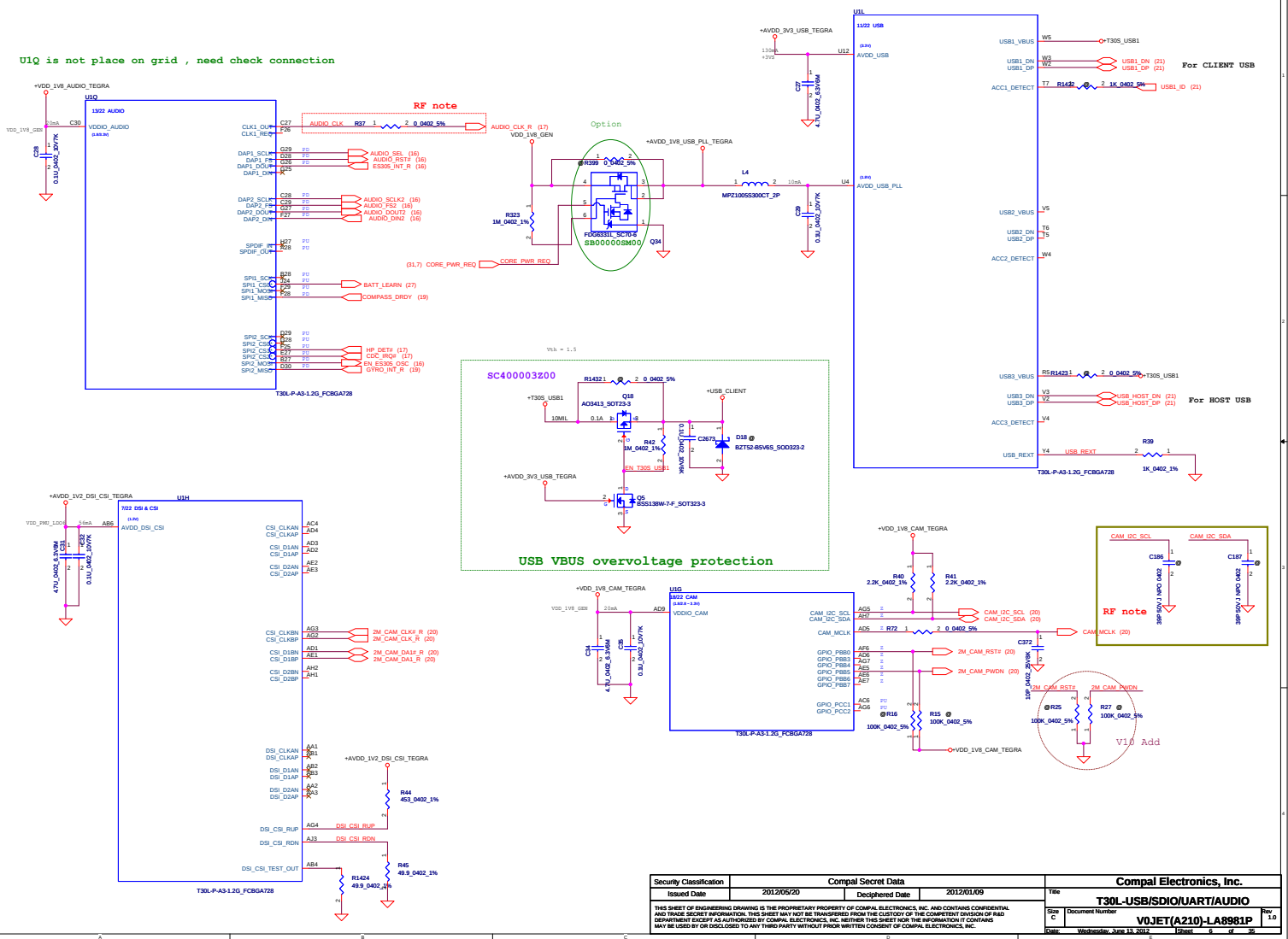
V0JET	EVT	DVT	PVT	MP
Board ID0	0	1	0	1
Board ID1	0	0	1	1

GEN1_I2C (+VDD_1V8_SENSOR)				PWR_I2C (+VDD_1V8_SYS_TEGRA)			
Device	8bit	7bit		Device	8bit	7bit	
E-compass (reserved only)	Write	0x18	0xC	Thermal Sensor	Write	0x98	0x4C
	Read	0x19			Read	0x99	
GYRO	Write	0xD0	0x68	Codec	Write	0x34	0x1A
	Read	0xD1			Read	0x35	
G-Sensor	Write	0x1E	0x0F	Battery	Write	0xAA	0x55
	Read	0x1F			Read	0xAB	
GEN2_I2C (+VDD_3V3_GM1_TEGRA)				EEPROM			
Device	8bit	7bit			low level	0xA0, 0xA1	0x50
Touch_Screen (Atmel)	Write	0x9A	0x4D	Audio Processor		0x7C, 0x7D	0x0E
	Read	0x9B				0x5A, 0x5B	0x2D
Touch_Screen (Focaletech)	Write	0x70	0x38	Processor Core Supply		0xC0, 0xC1	0x60
	Read	0x71					
				CAM_I2C < +VDD_1V8_CAM_TEGRA >			
Device	8bit	7bit		Device	8bit	7bit	
2M Camera	Write	0x78	0x3C		Write	0x78	
	Read	0x79			Read	0x79	

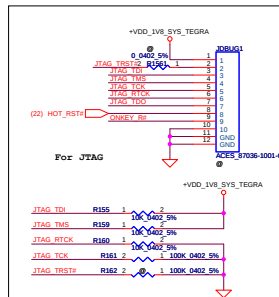
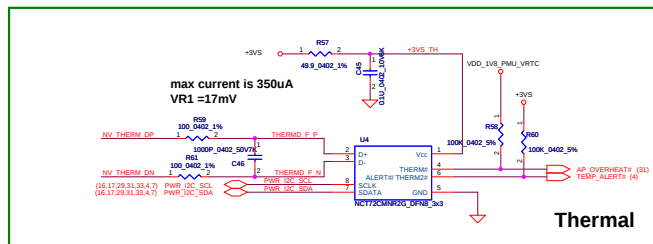
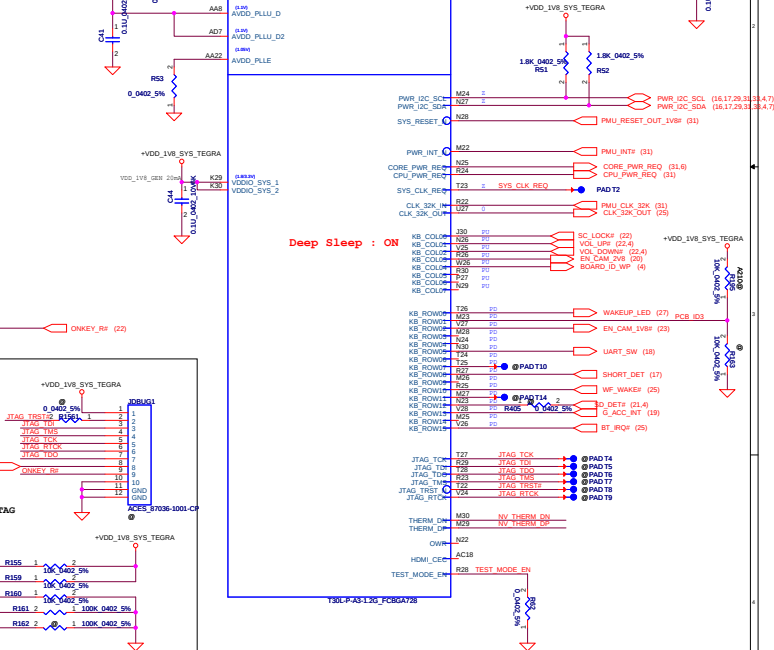
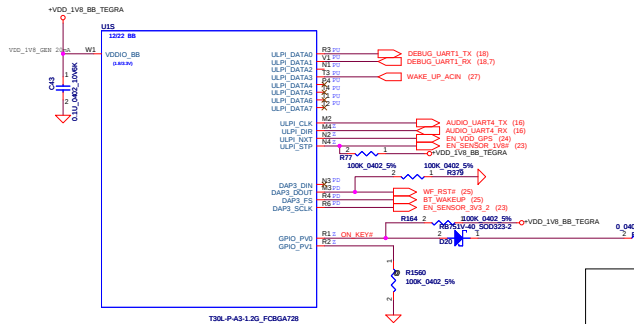
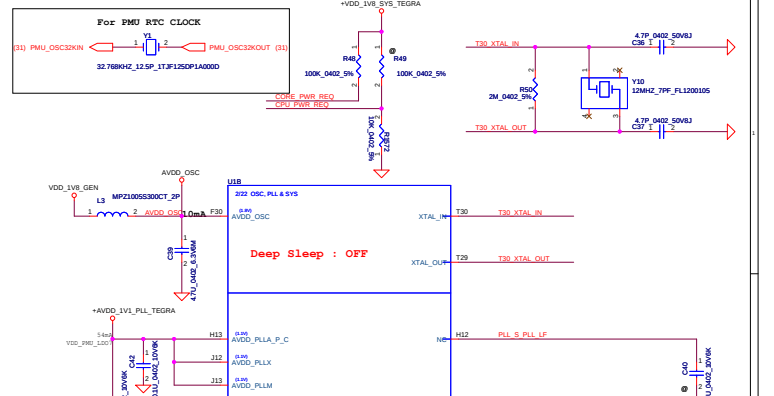
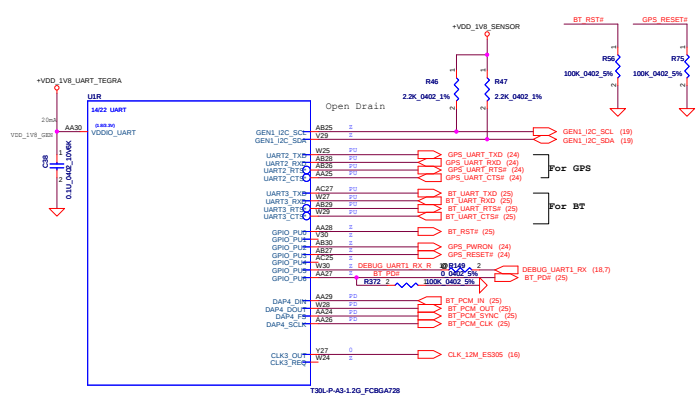
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UIQ is not place on grid , need check connection

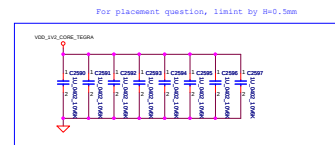
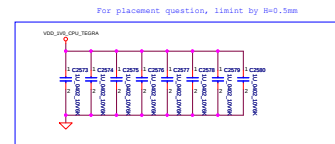
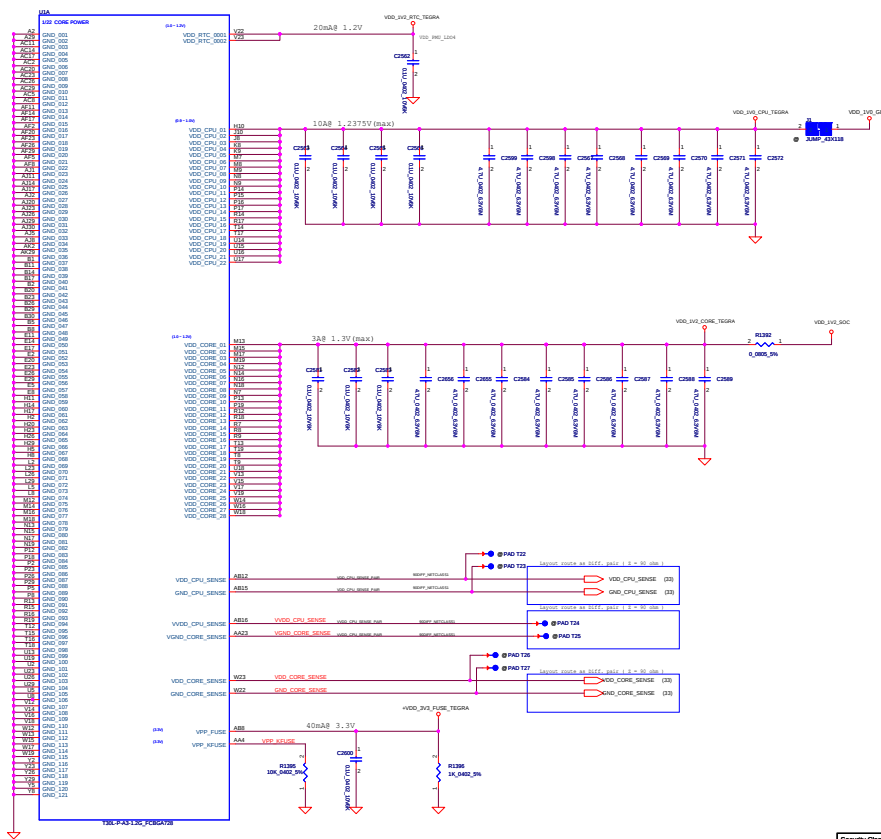


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T30 Core Power

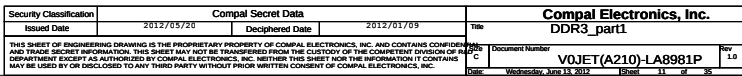
[illegible]

The diagram illustrates the T30L-P-A3-120_FCBGA728 board layout, showing connections for various interfaces and components. The components are organized into four main sections:

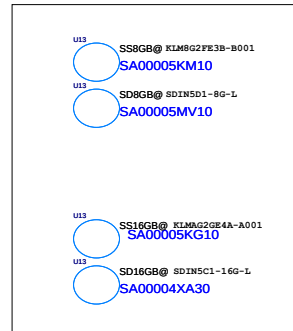
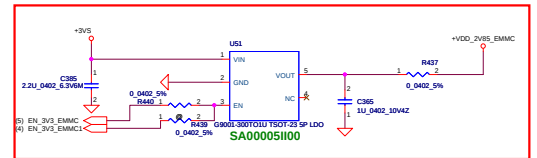
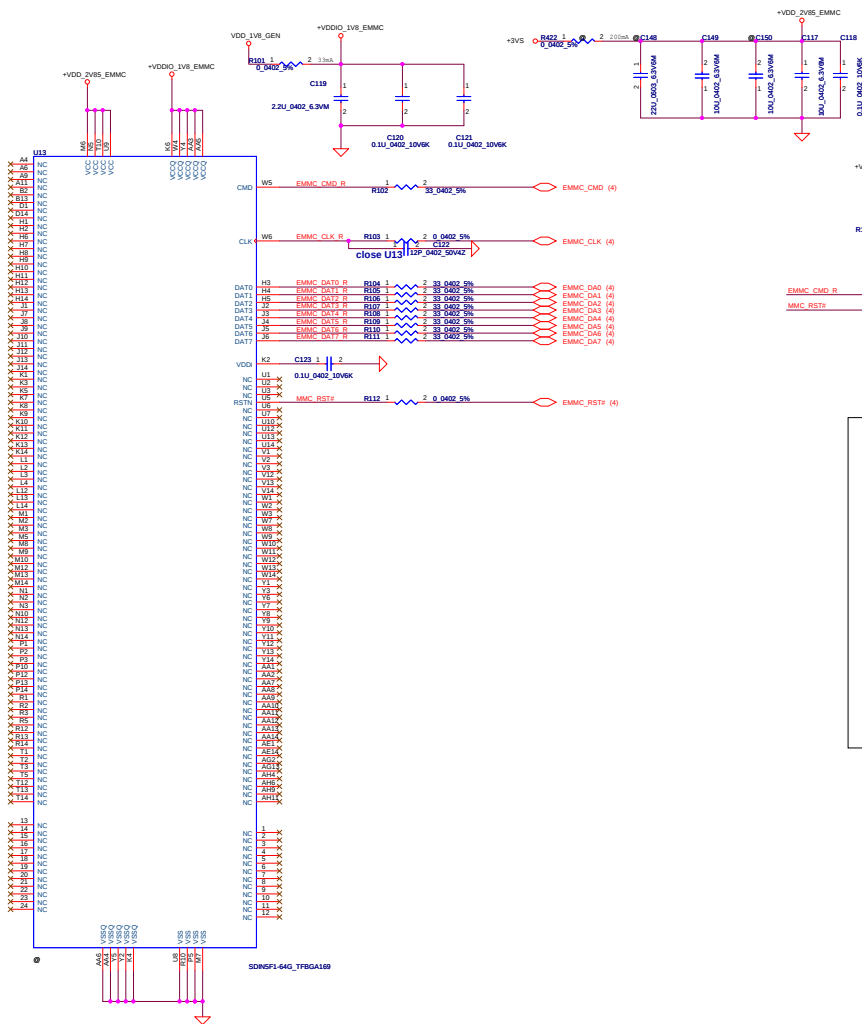
- T30 PEX Interface:** This section shows the connection of the T30 PEX interface to the board. It includes components like **U17** (T30 PEX), **U18** (T30 PEX), and **U19** (T30 PEX). The interface is connected to the board's power and ground planes.
- T30 VI Interface:** This section shows the connection of the T30 VI interface to the board. It includes components like **U20** (T30 VI), **U21** (T30 VI), and **U22** (T30 VI). The interface is connected to the board's power and ground planes.
- T30 SATA Interface:** This section shows the connection of the T30 SATA interface to the board. It includes components like **U23** (T30 SATA), **U24** (T30 SATA), and **U25** (T30 SATA). The interface is connected to the board's power and ground planes.
- T30 SPARE Pins:** This section shows the connection of the T30 SPARE pins to the board. It includes components like **U26** (T30 SPARE), **U27** (T30 SPARE), and **U28** (T30 SPARE). The interface is connected to the board's power and ground planes.

The diagram also shows the connection of various components to the board's power and ground planes, including resistors, capacitors, and connectors. The components are labeled with their part numbers and values, and the connections are shown with lines and arrows.

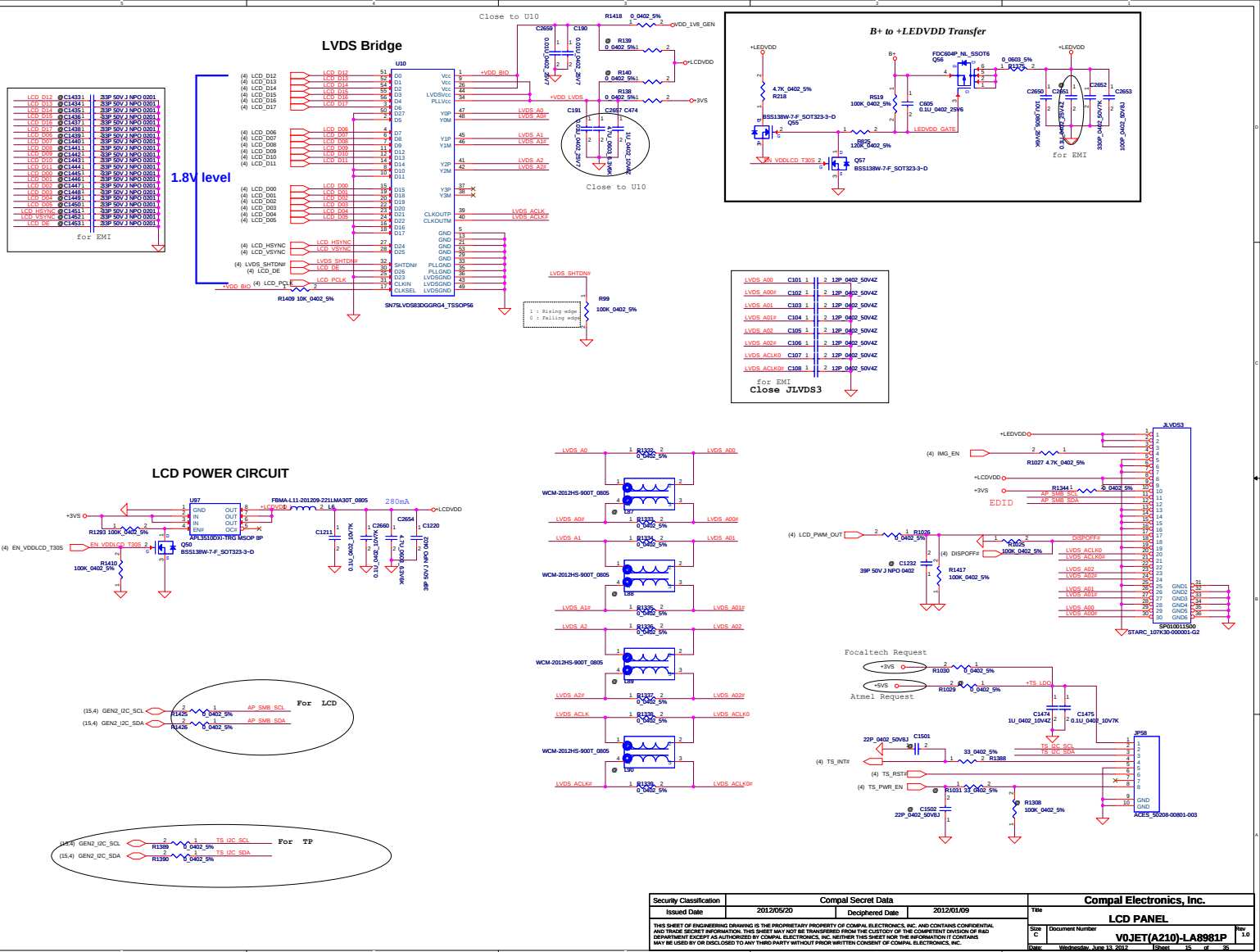
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T30L-PEX/SATAMI			
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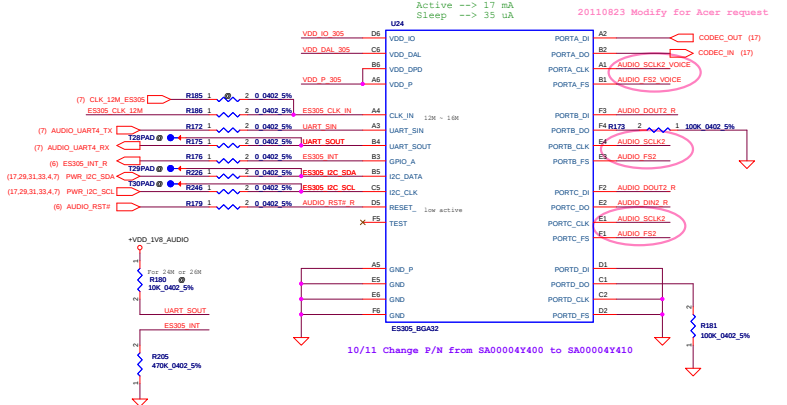
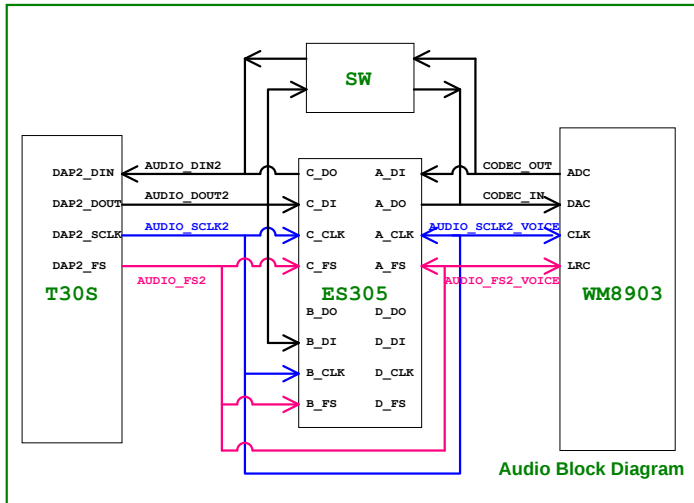
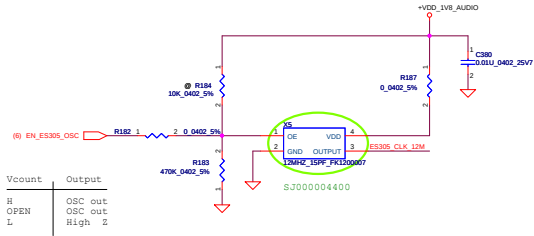
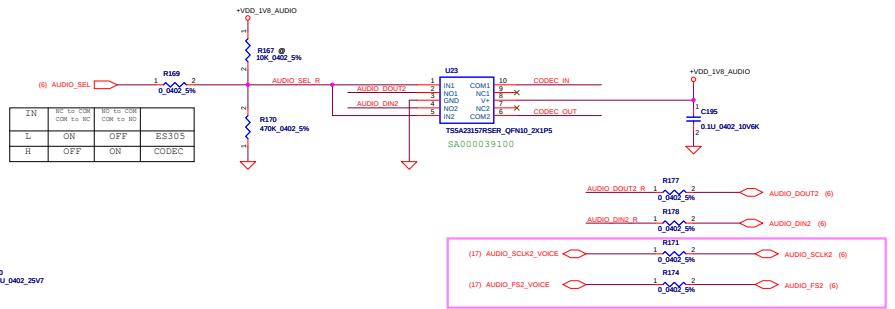
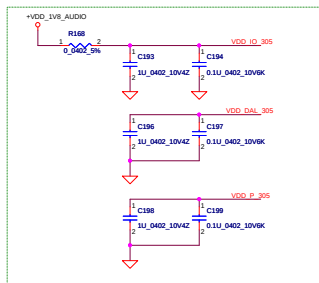
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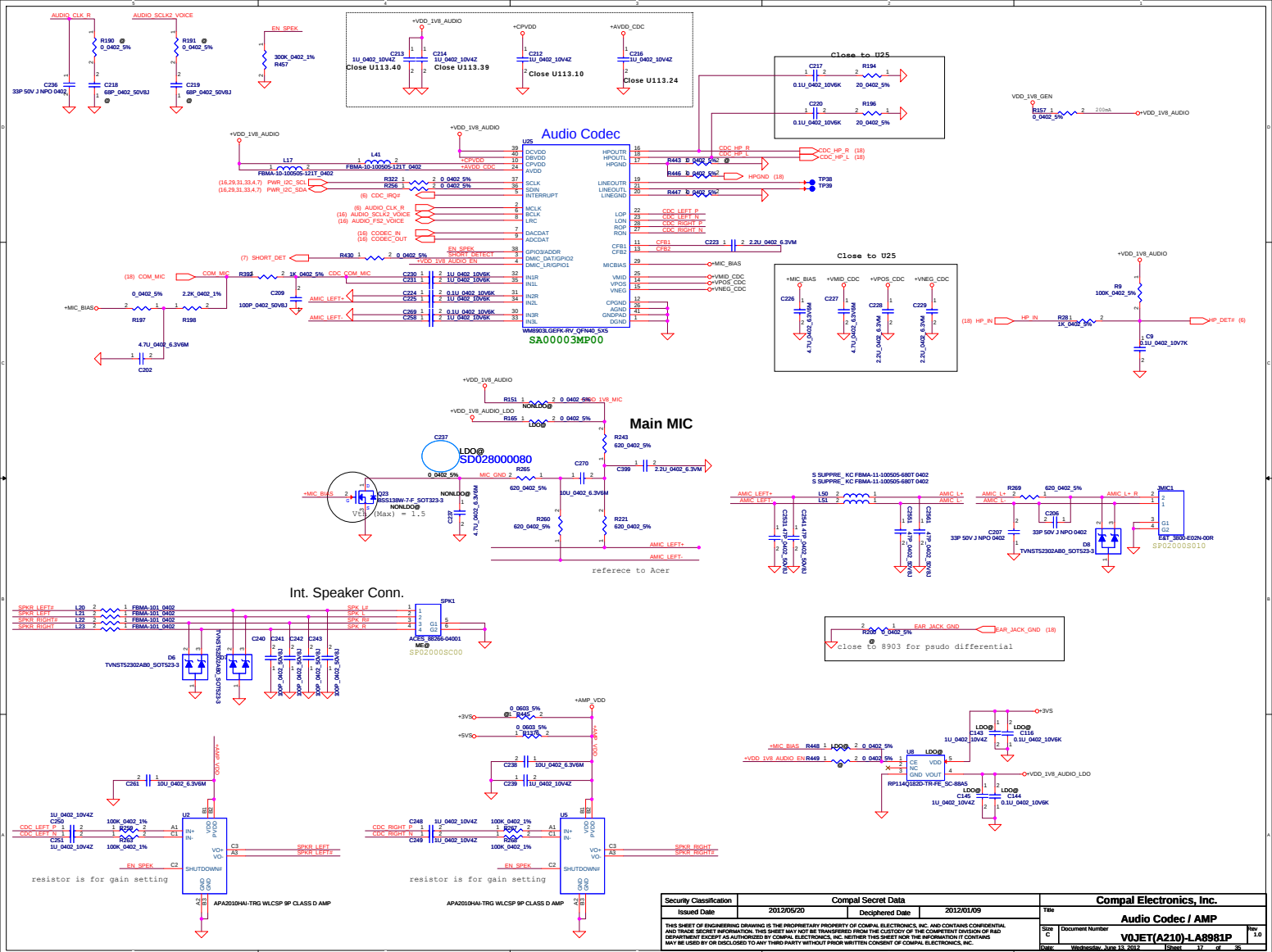


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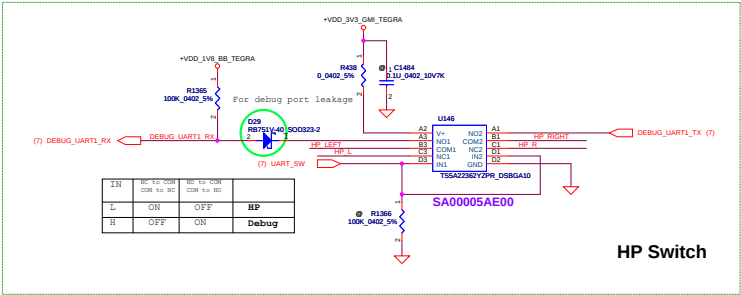
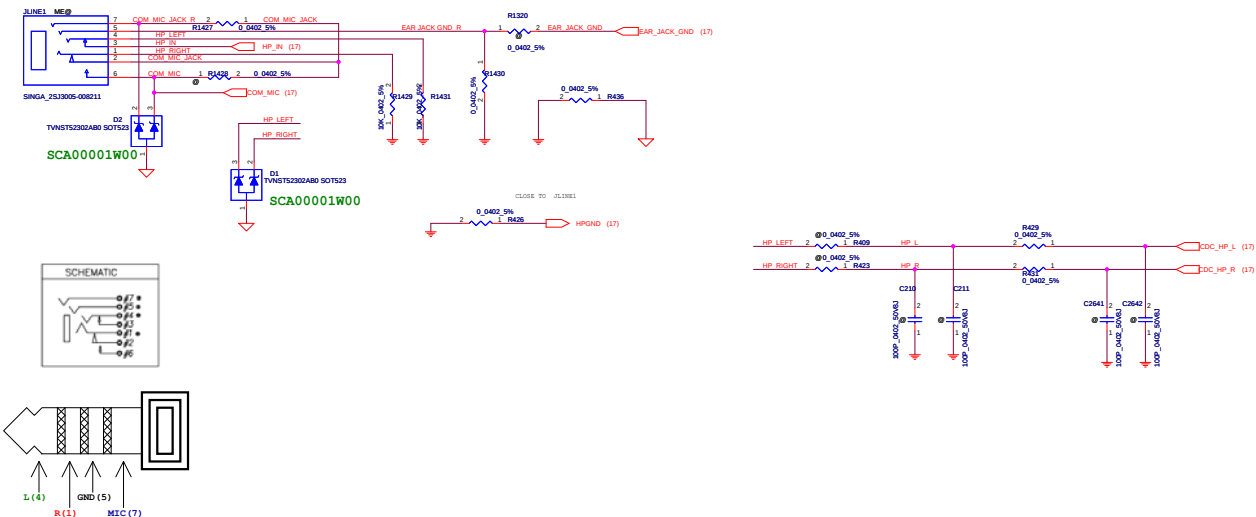
Support for input clock frequencies of 24 MHz and 26 MHz requires a 10k pull-up resistor on the UART_SOUT pin.

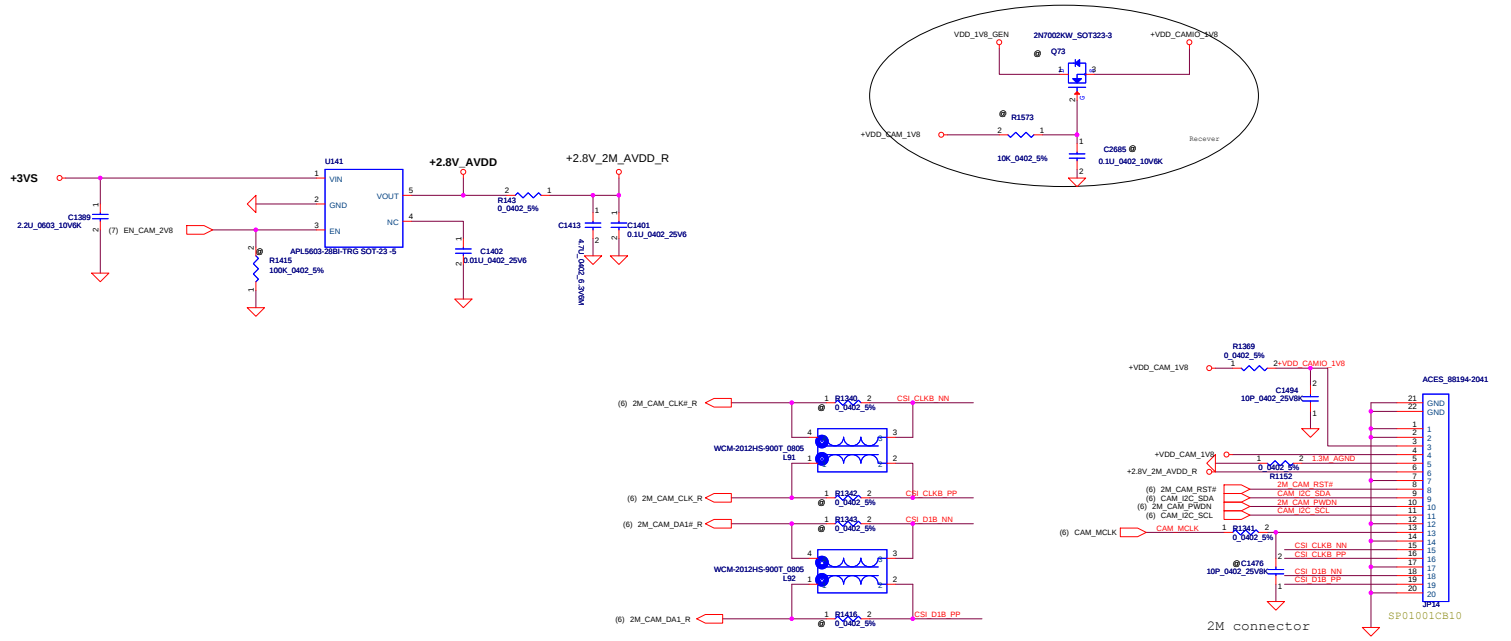
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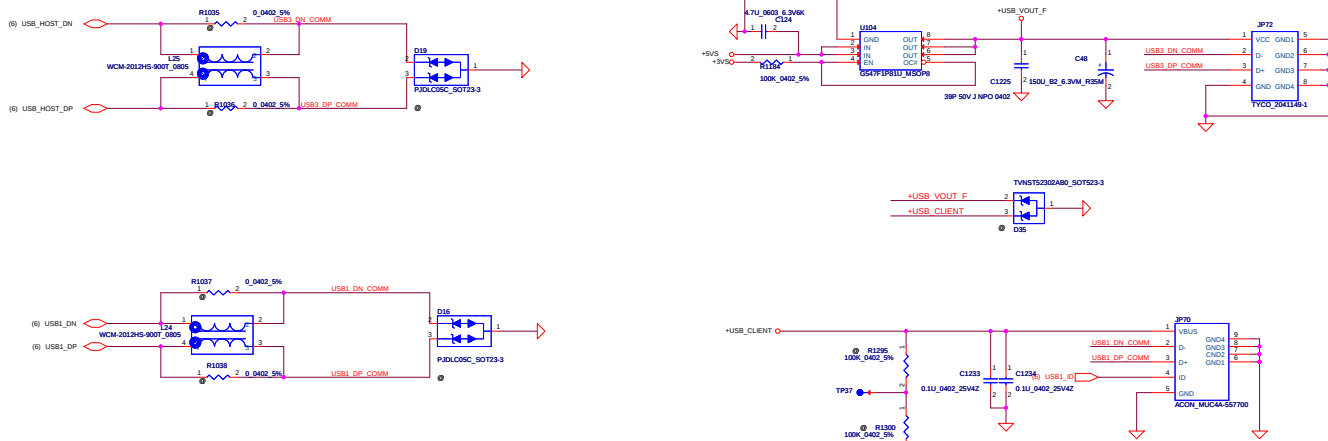
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Audio Jack



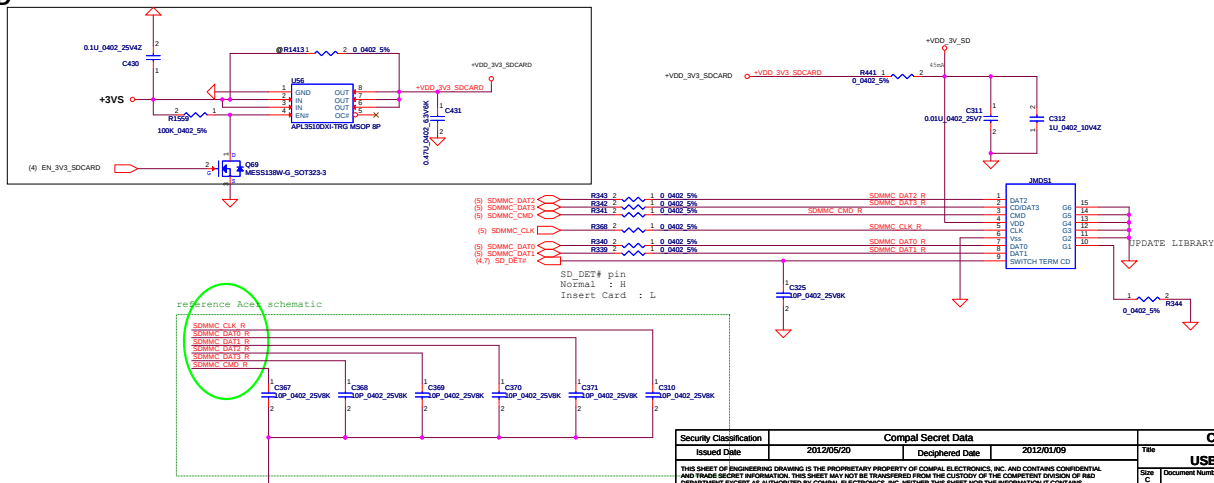


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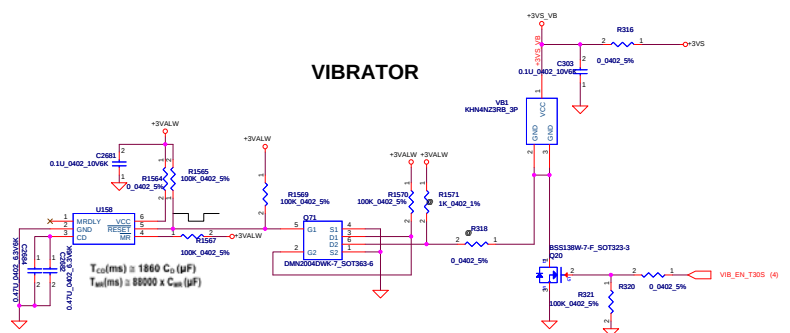
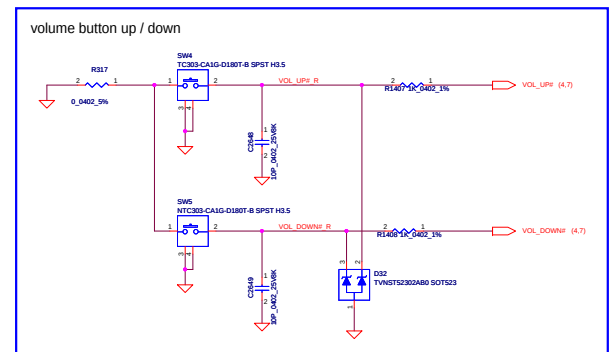
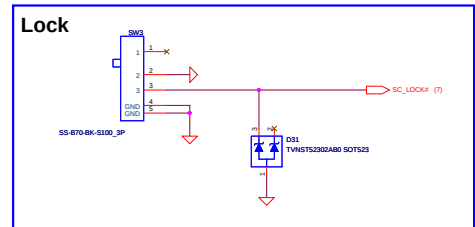
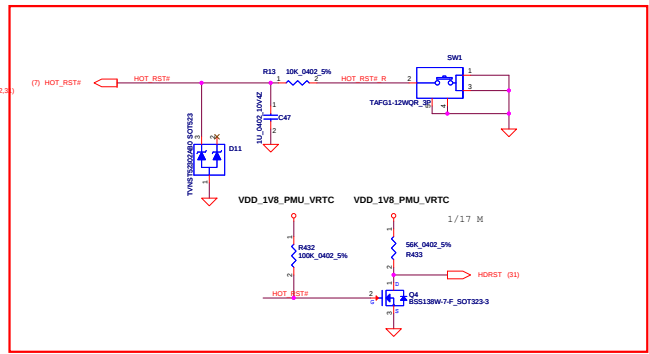


USB Port

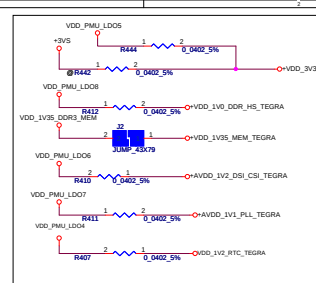
Micro SD



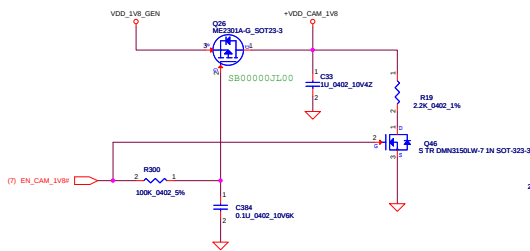
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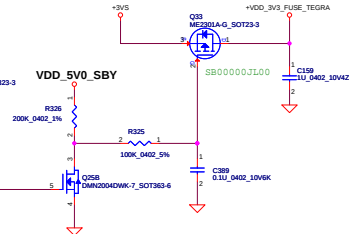
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2012/05/20		2012/01/09		Power LED/Lock LED/Ecompass	
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				Sheet	21 of 35



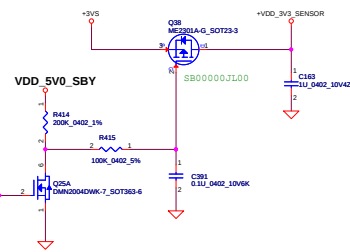
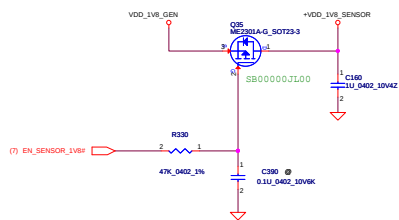
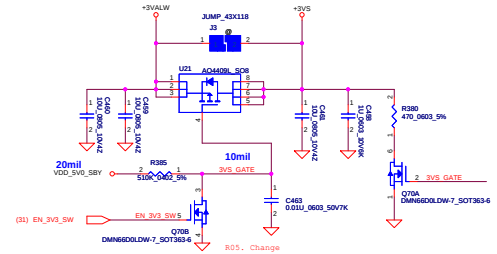
Q26 close to Camera Conn.



Q33 close to T30S

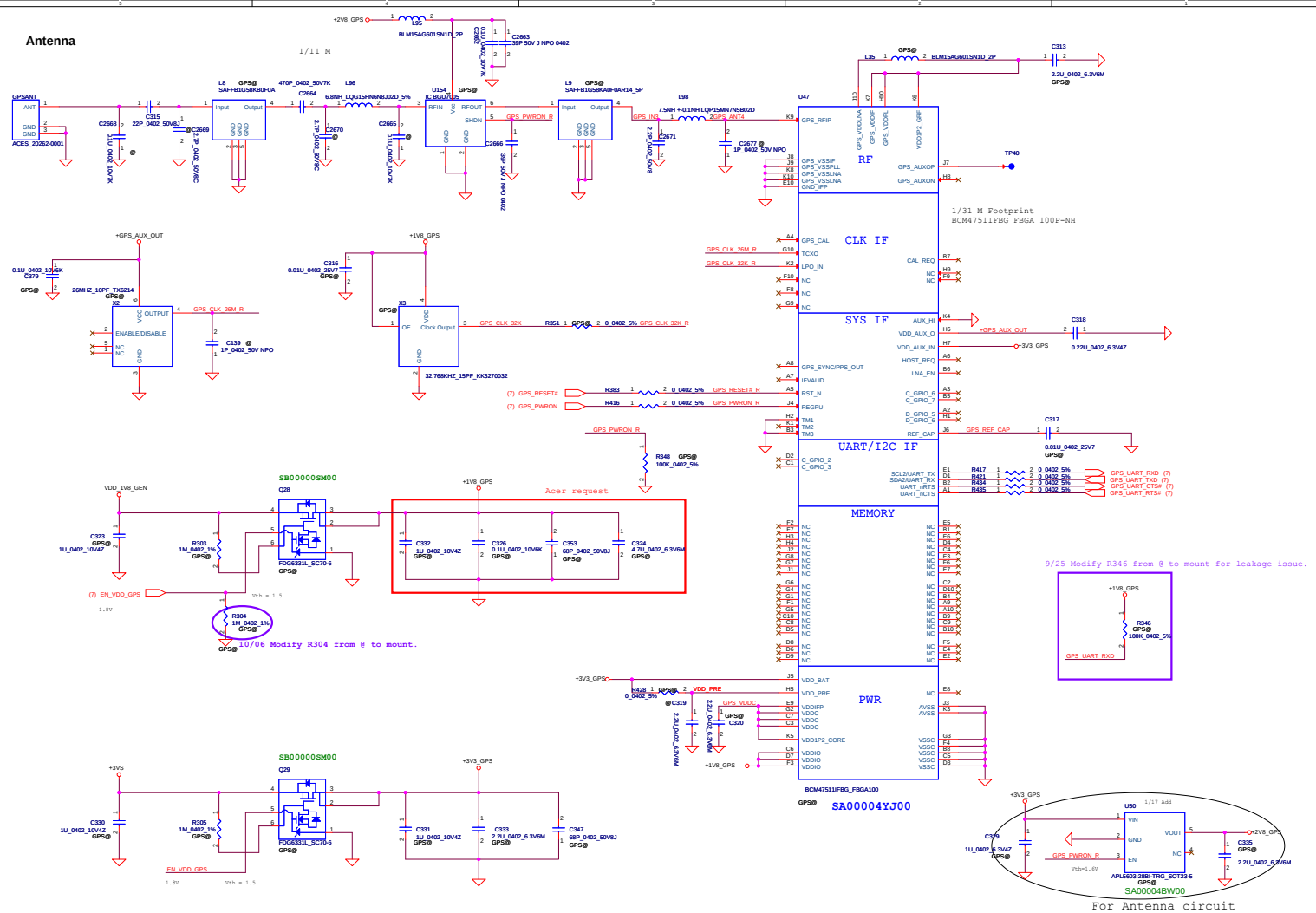


+3VALW TO +3VS



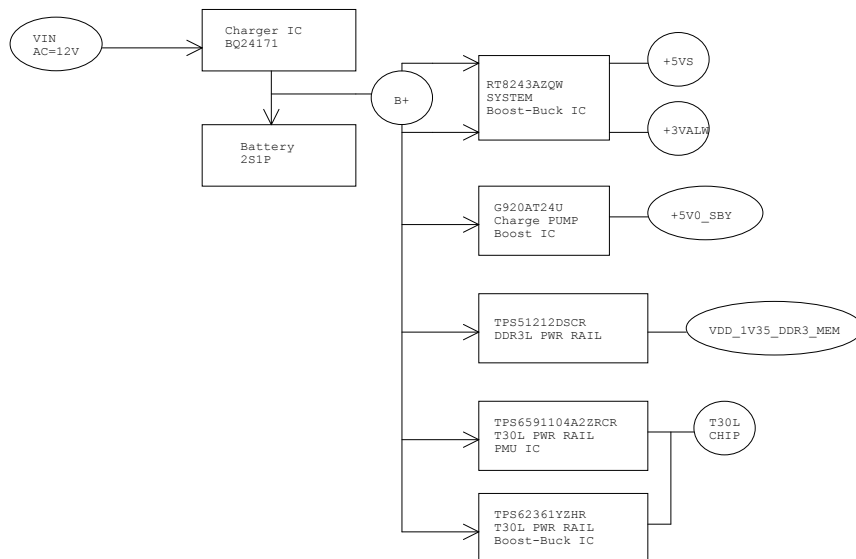
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Antenna



GPS POWER SOURCE

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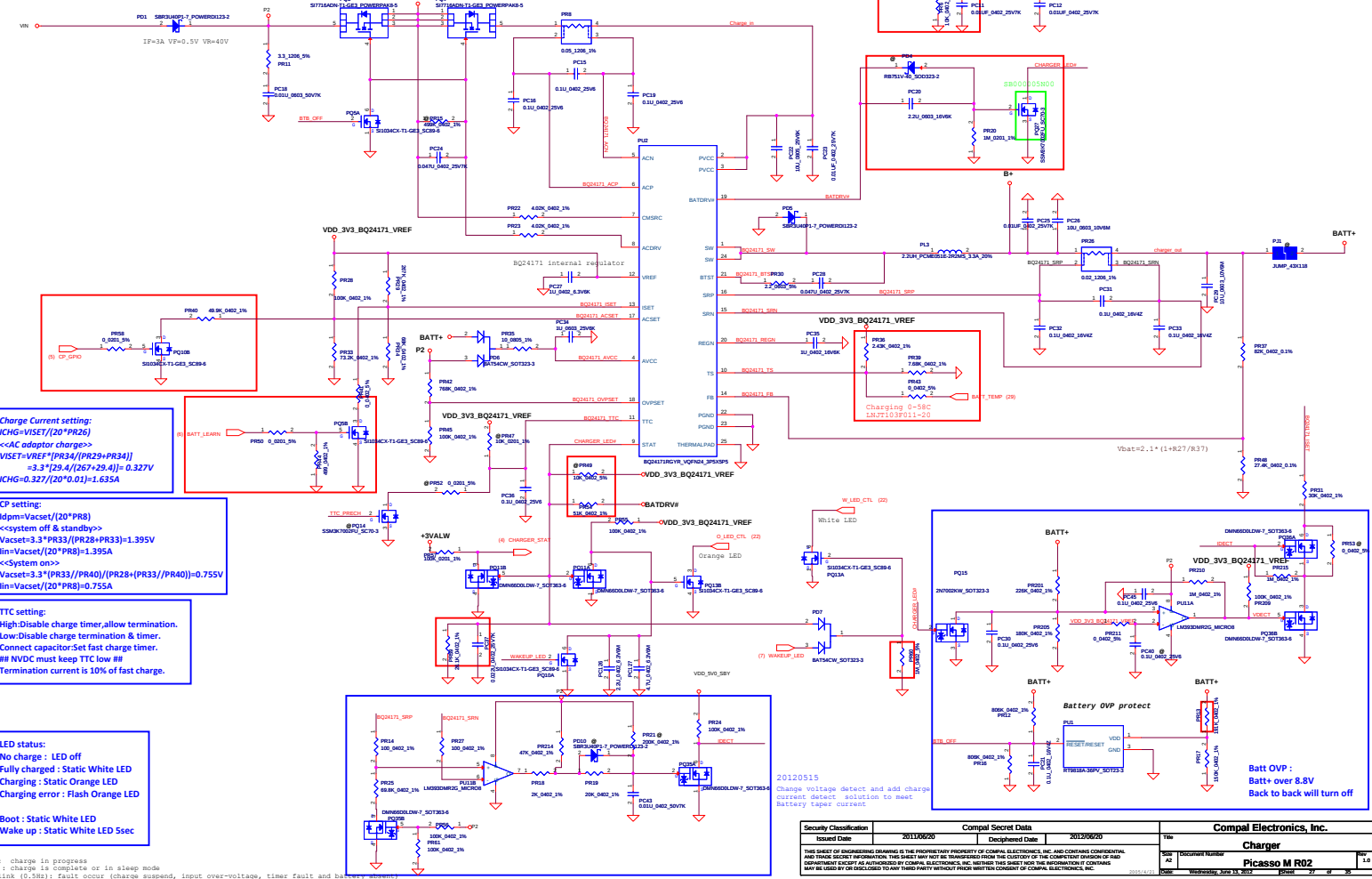
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Size C	Document Number	V0JET(A210)-LA8981P		Rev 1.0
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CHARGER BQ24171

AC Insert or remove --> Wake up T308
USB Insert or remove --> Wake up T308
SW to check if Acer USB --> Charge current to 1A

OVP UVP Range setting:
#OVPSSET voltage is between 0.497-1.6V##
1.6V*(768+100)/100=13.888V
0.497V*(768+100)/100=4.314V
Setting "OVP 13.888V" & "UVP 4.314V"

Max Rds(on) 14.3mOhm



Charge Current setting:
 $ICHG = VISET / (20 * PR26)$
--> AC adaptor charger
 $VISET = VREF * (PR34 / (PR29 + PR34))$
 $= 3.3 * (29.4 / (267 + 29.4)) = 0.327V$
 $ICHG = 0.327 / (20 * 0.01) = 1.635A$

CP setting:
 $Idpm = Vcasel / (20 * PR8)$
--> system off & standby
 $Vcasel = 3.3 * PR33 / (PR28 + PR33) = 1.395V$
 $Iin = Vcasel / (20 * PR8) = 1.395A$
--> system on
 $Vcasel = 3.3 * PR33 / (PR40) / (PR28 + PR33 / PR40) = 0.755V$
 $Iin = Vcasel / (20 * PR8) = 0.755A$

TTC setting:
High: Disable charge timer, allow termination.
Low: Disable charge termination & timer.
Connect capacitor-Set fast charge timer.
NVDC must keep TTC low ##
Termination current is 10% of fast charge.

LED status:
No charge : LED off
Fully charged : Static White LED
Charging : Static Orange LED
Charging error : Flash Orange LED

Boot : Static White LED
Wake up : Static White LED Ssec

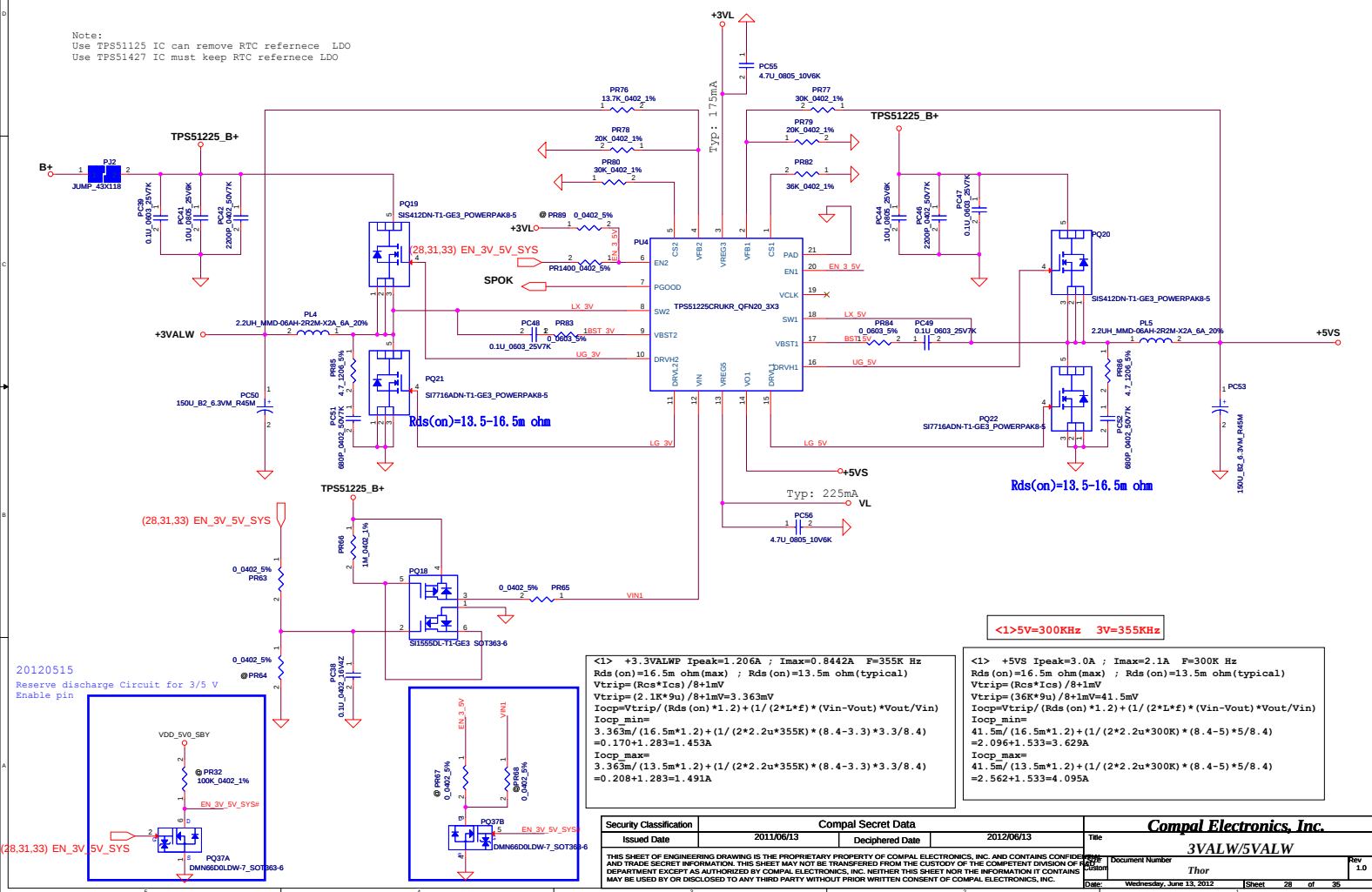
L: charge in progress
B: charge is complete or in sleep mode
Blink (0.5Hz): fault occur (charge suspend, input over-voltage, timer fault and battery warning)

20120515
Change voltage detect and add charge current detect solution to meet Battery taper current

Batt OVP :
Batt+ over 8.8V
Back to back will turn off

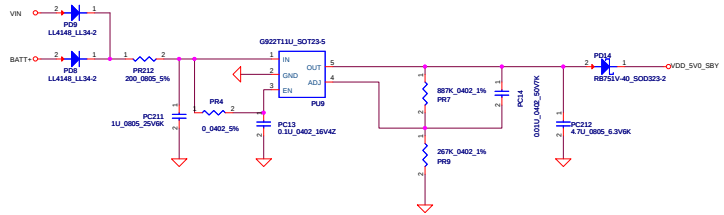
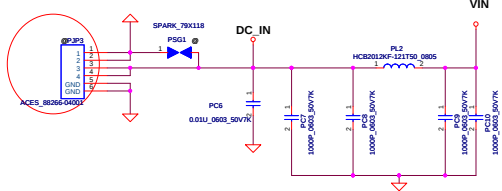
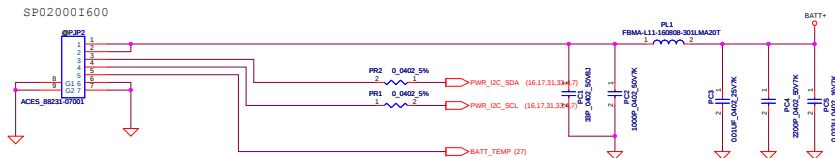
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Compal Electronics, Inc.				Charger	
Pisano M R02				Rev 1.0	
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Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO

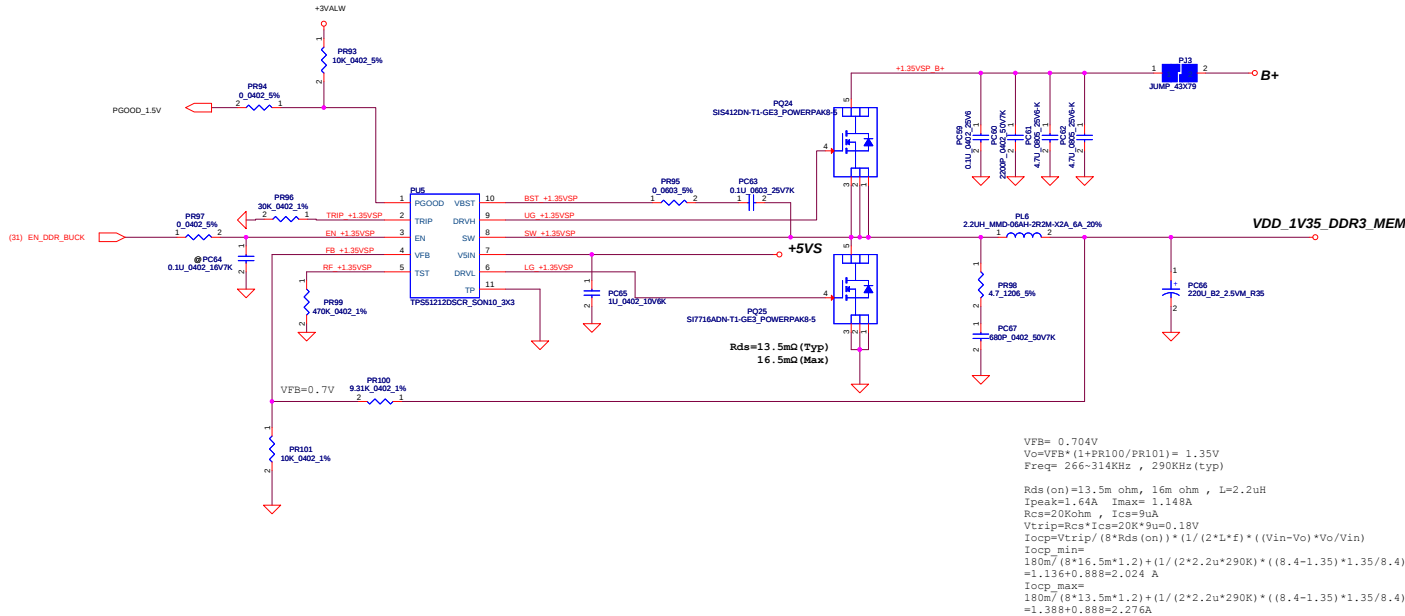


20120515
Reserve discharge Circuit for 3/5 V
Enable pin

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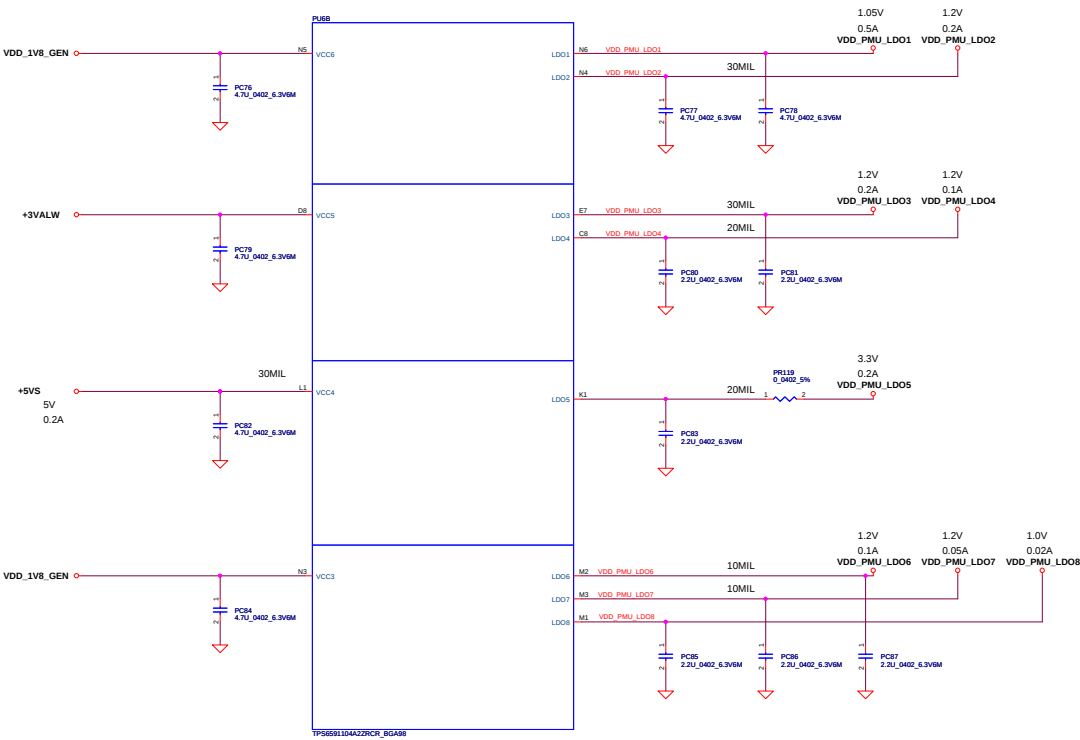


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Note: LDO1 & LDO2 need 4.7uF cap according to TI on July 6th

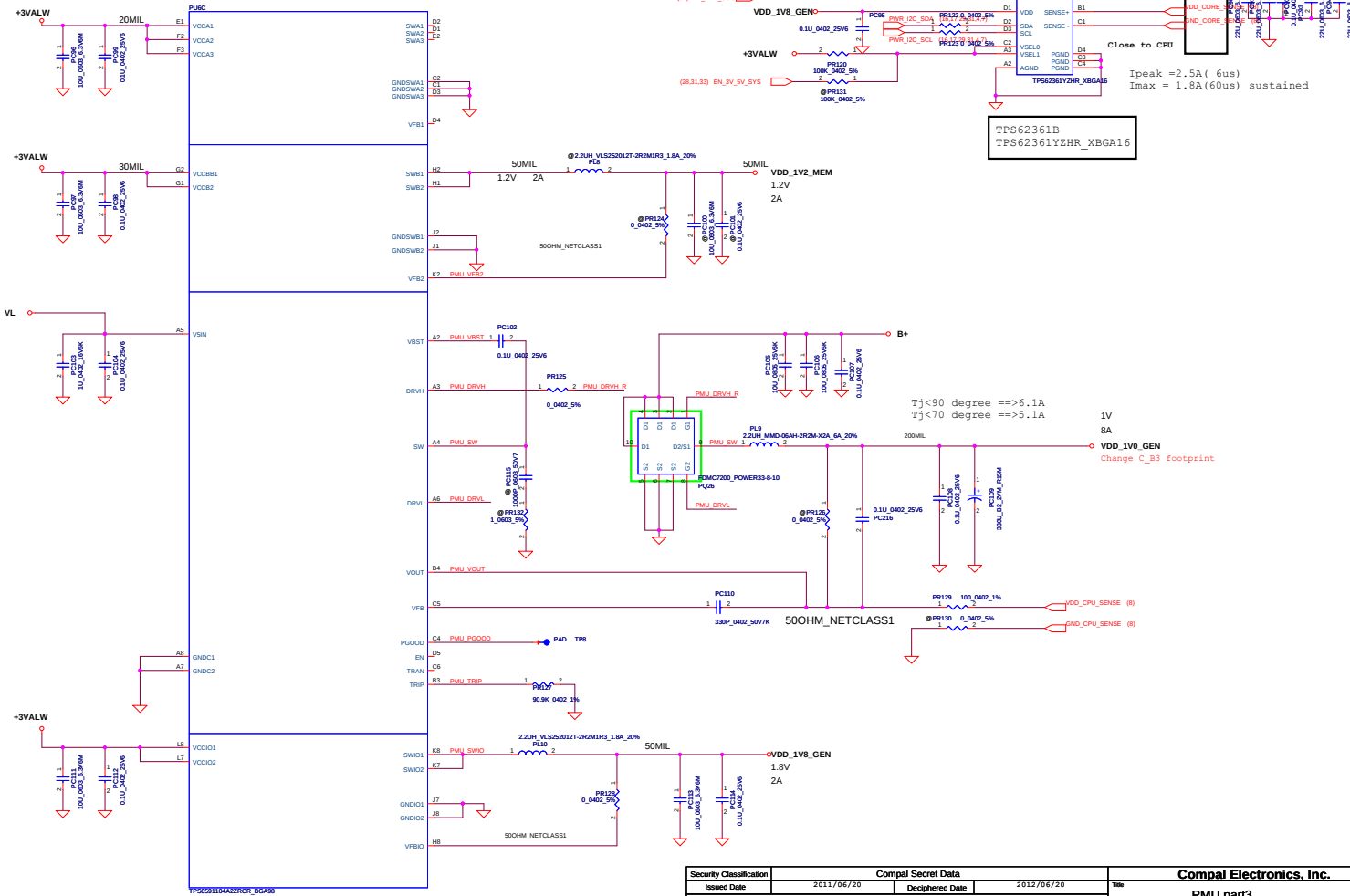
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