

Compal Confidential

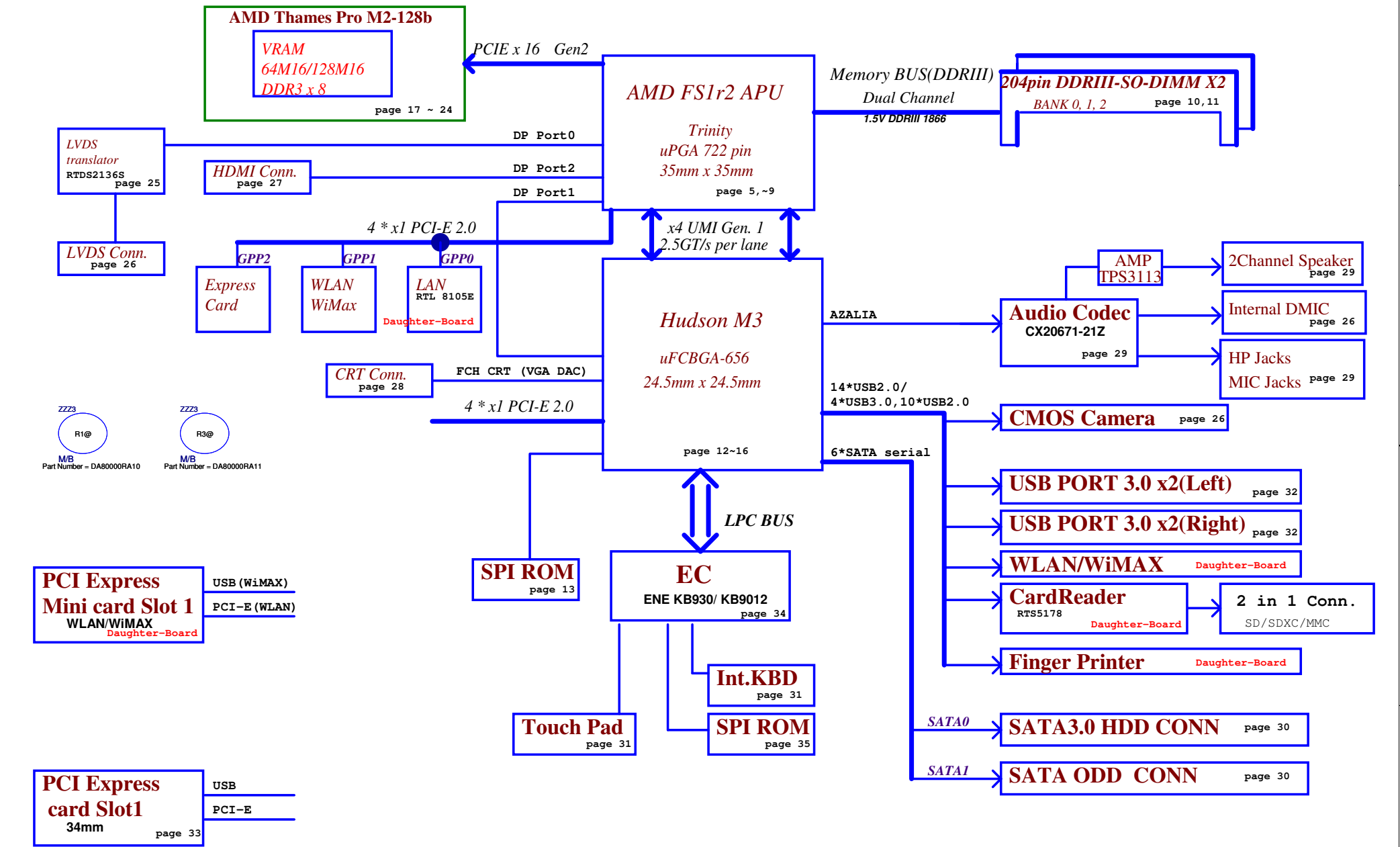
QCL10 Schematics Document

AMD APU Trinity FS1r2 + FCH Hudson-M3 + GPU Seymour/Thames XT

2012-07-13

REV:1.0 (A00)

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Issued Date	2011/08/01	Deciphered Date	2013/01/01	Title	Cover Page
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+1.5V	1.5V power rail for APU VDDIO and DDR	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.2VS	1.2V (VDDR, VDDP) switched power rail for APU	ON	OFF	OFF
+2.5VS	2.5V for APU VDDA	ON	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VGS	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+1.0VGS	1.0V switched power rail for VGA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSb always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	000 1011	11h 0x16	ADM1032ARMZ	100 1101	4Dh 0x9A
Charger IC	000 1001	09h 0x12	SB-TSI	100 1100	4Ch 0x98
			RTD2136	100 1010	4Ah 0x94
			GPU	100 0001	41h 0x82

SM Bus Controller 0 (FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		

SM Bus Controller 1 (FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

FCH Hudson-M3 SATA Port List	
SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

Comal PCIE Port List		
APU	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	ExCARD
	PCIE3	NC
FCH	PCIE0	NC
	PCIE1	NC
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M3 USB Port List	
USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	DEBUG PORT
Port1	WLAN
Port2	NC
Port3	FingerPrint
Port4	NC
Port5	NC
Port6	NC
Port7	CardReader
Port8	ExCARD
Port9	CAM
Port10	LP1
Port11	LP2
Port12	RP1
Port13	RP2

FCH Hudson-M3 USB Port List	
Port0	LP1
Port1	LP2
Port2	RP1
Port3	RP2

BOM Structure

UMA@ : UMA only
DIS@ : DIS muxluss
45@ : 45 Level
9012@: EC9012
930@: EC930
INS@: Inspiron
VOS@: Vostro
M2@: FCH M2
M3@: FCH M3
FFS@: FreeFallSensor
EXP@: Express Card
FP@: FingerPrint
EMC@: EMI&ESD part

SE@: SEYMOUS GPU
CH@: Chelsea GPU
X76@: VRAM
H2G@: Hynix 2G
S2G@: Samsung 2G
R1@: R1 P/N for FCH,PCB
TMSR1@: R1 P/N for GPU,VRAM
R3@: R3 P/N for FCH,PCB
TMSR3@: R3 P/N for GPU,VRAM

Power-Up/Down Sequence

- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

VDDR3(3.3VGS)

PCIE_VDDC(1.0V)

VDDR1(1.5VGS)

VDDC/VDDCI(1.12V)

VDD_CT(1.8V)

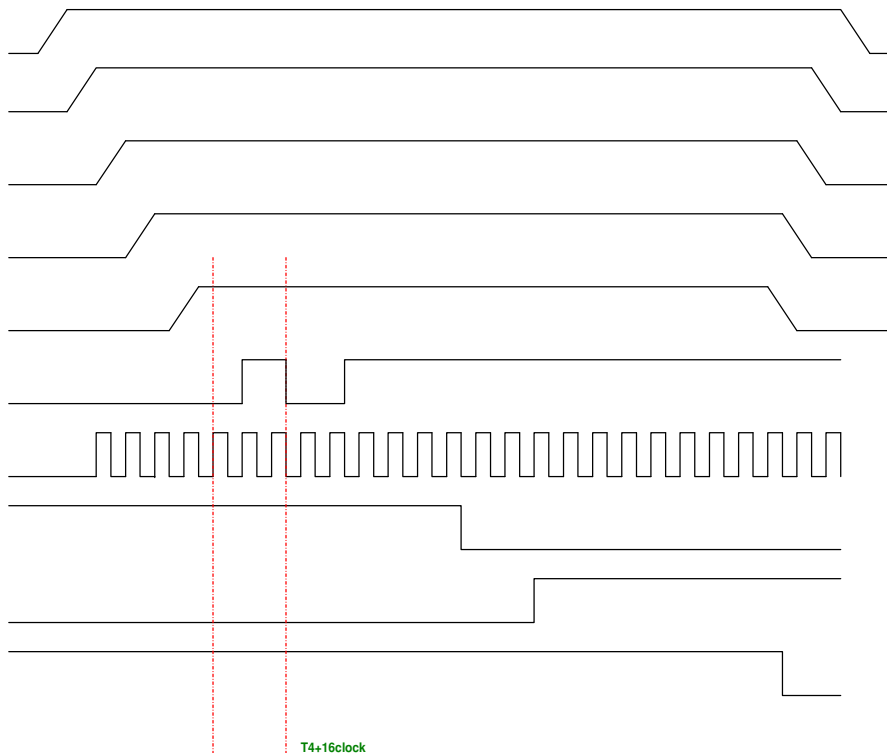
PERSTb

REFCLK

Straps Reset

Straps Valid

Global ASIC Reset



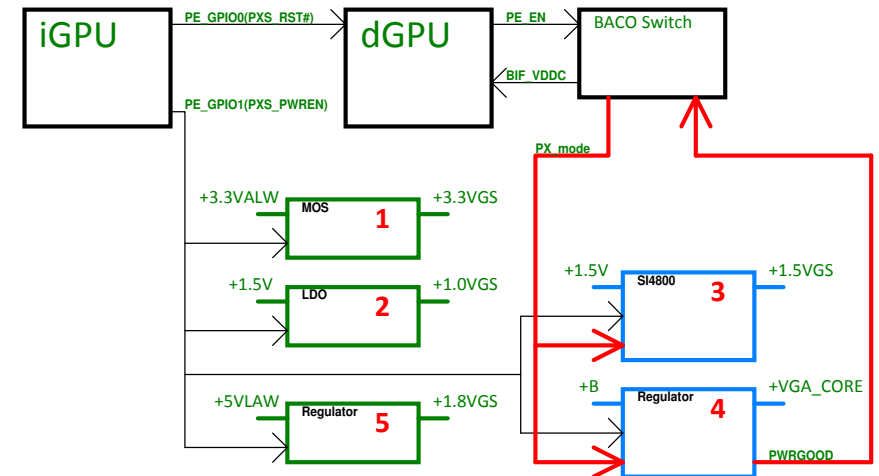
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High -> Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

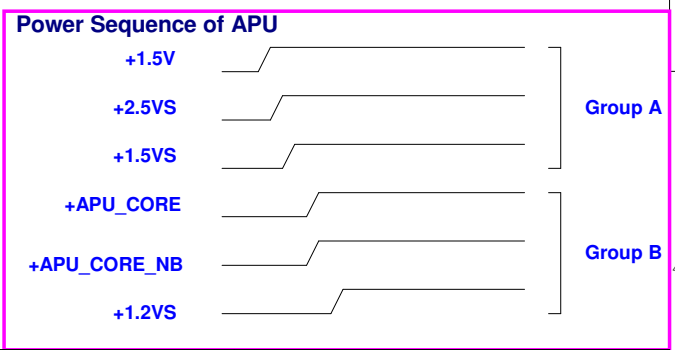
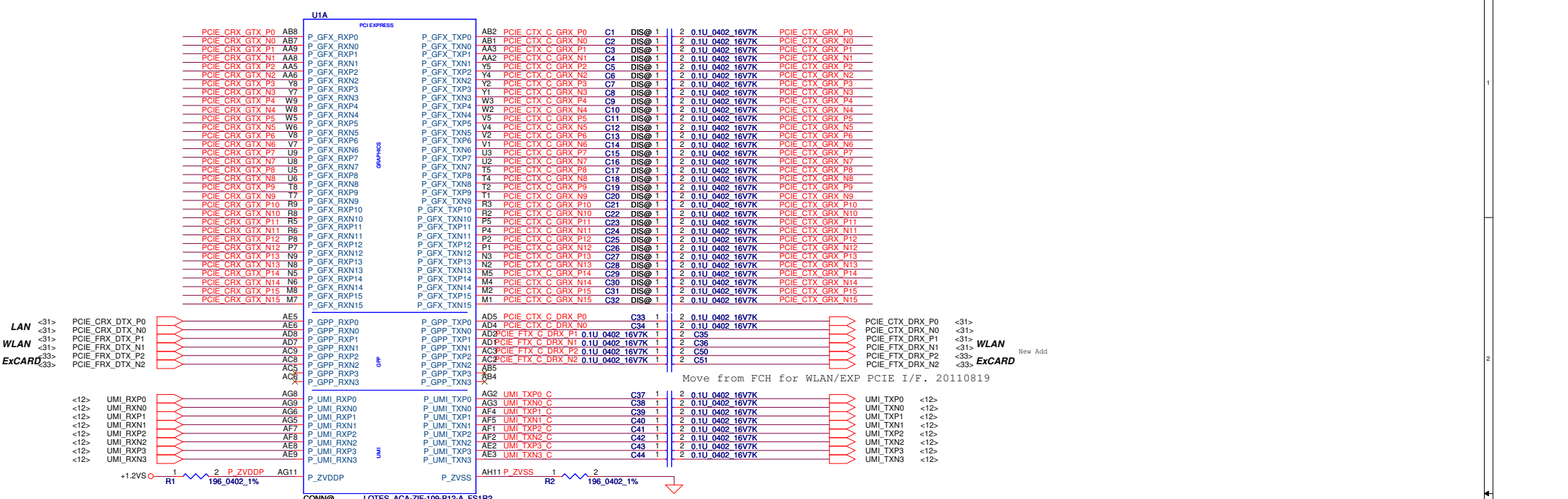
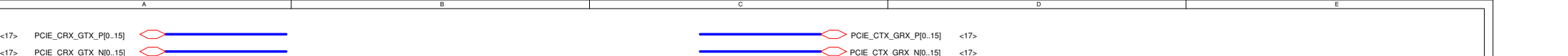
BACO option :

PE_GPIO0 : High -> Normal operation (dGPU is not reset on BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

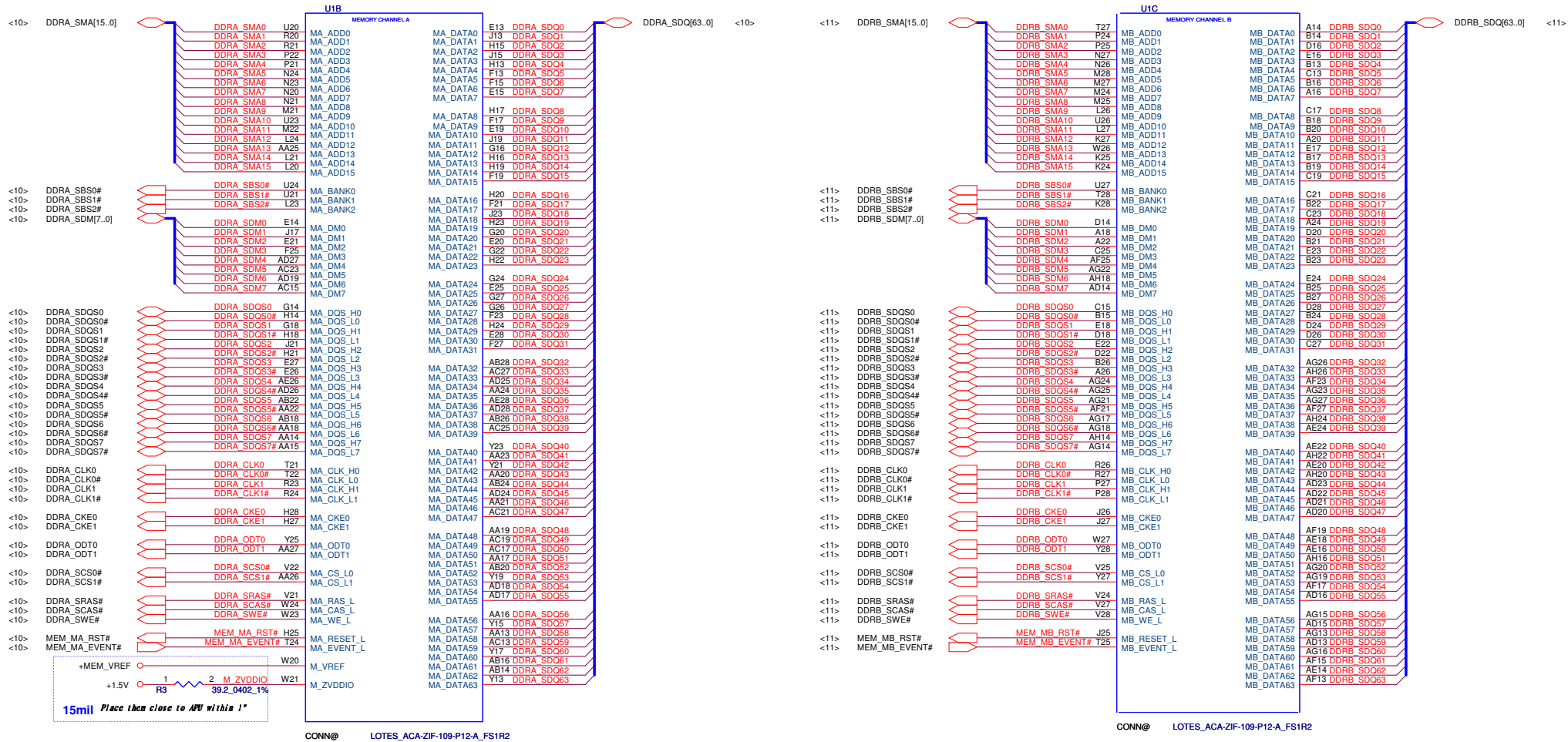
dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	775mA
PCIE_VDDC	1.0V	OFF	ON	1.1A
VDDR3	3.3V	OFF	ON	60mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	1.2A
VDDC/VDDCI	TBD	OFF	OFF	28



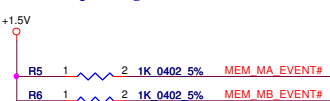
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Issued Date	2011/08/01	Deciphered Date	2013/01/01	Title	dGPU Block Diagram
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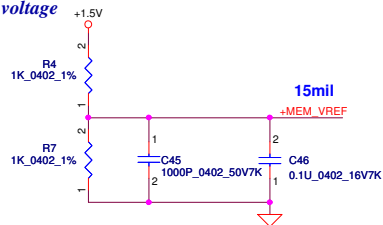
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2013/01/01				Title				FS1r2 PCIE/UMI			
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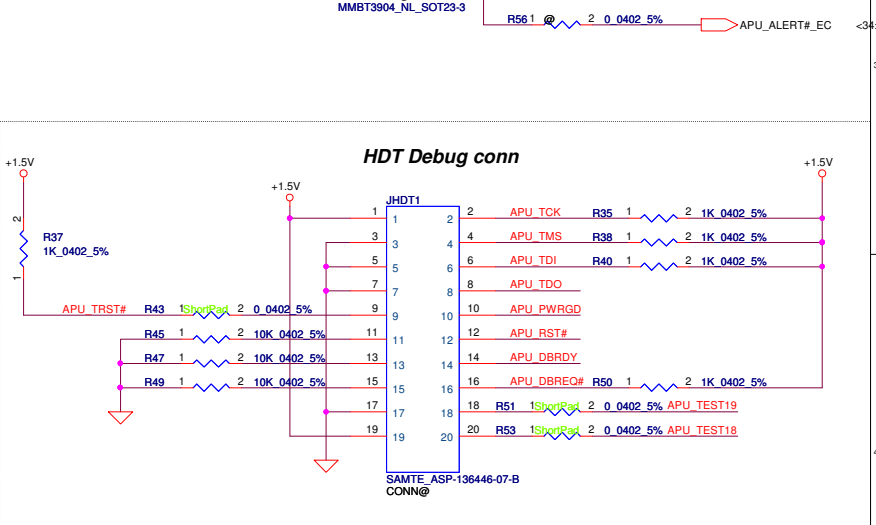
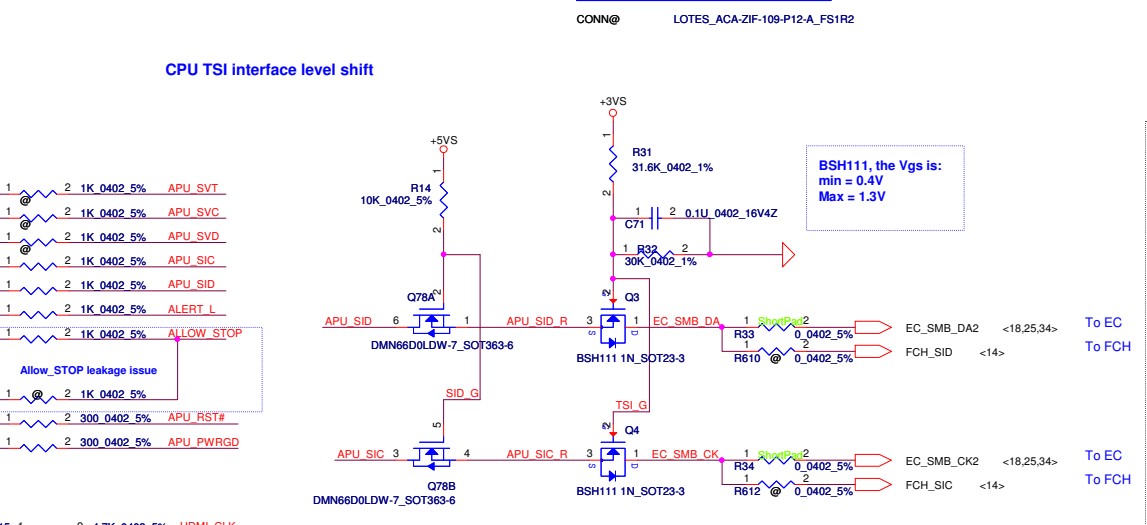
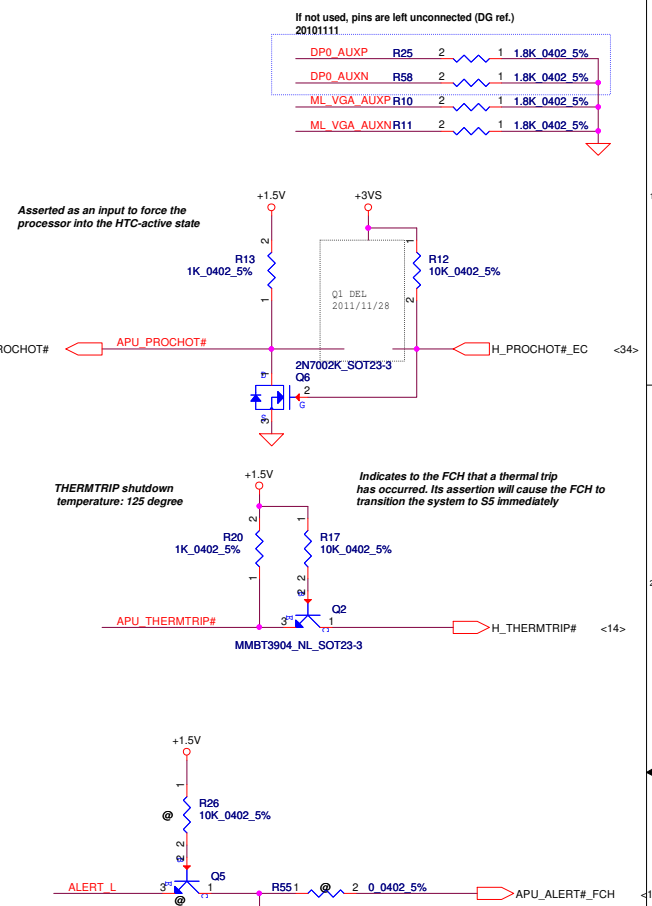
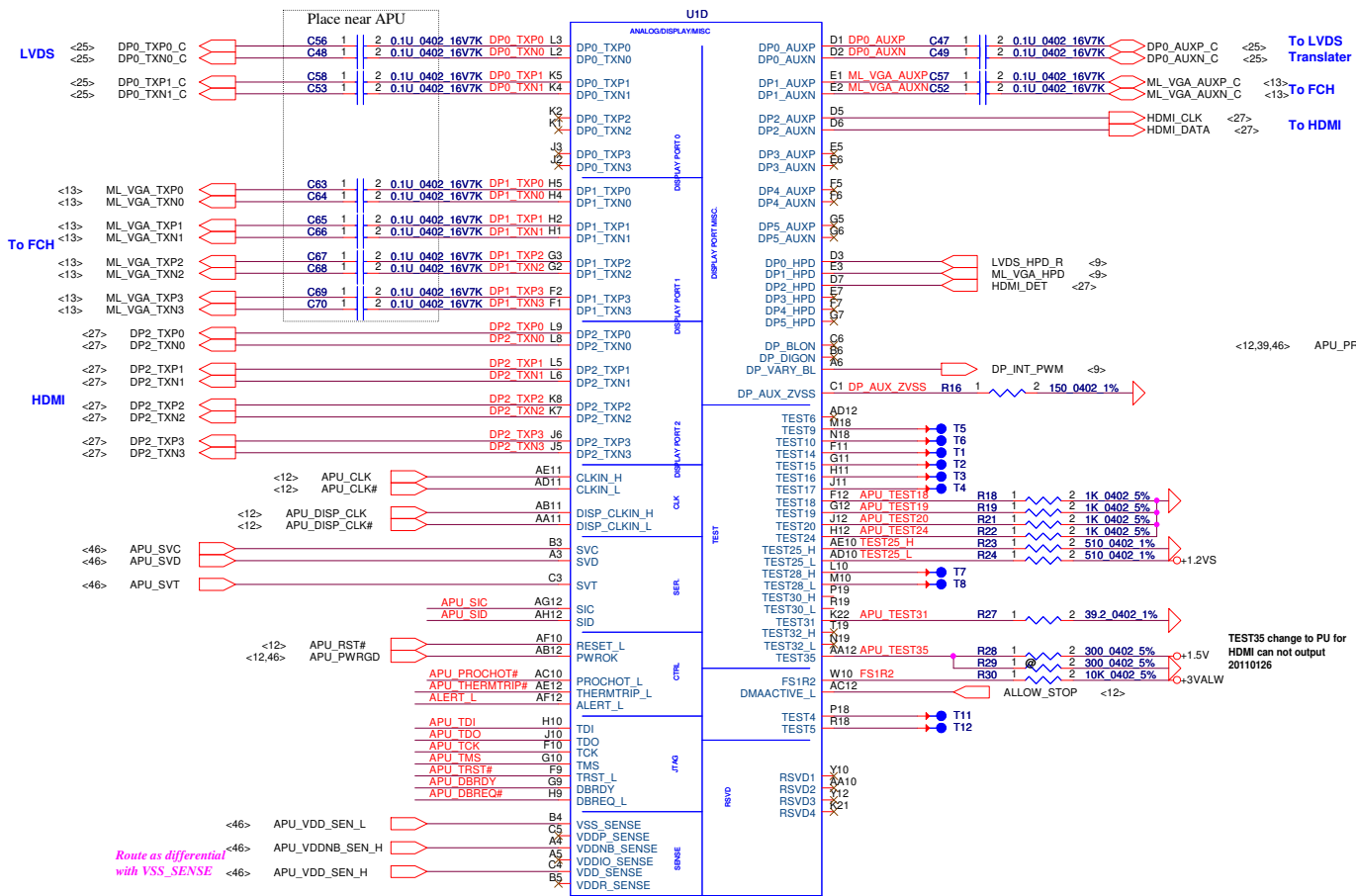
EVENT# pull high



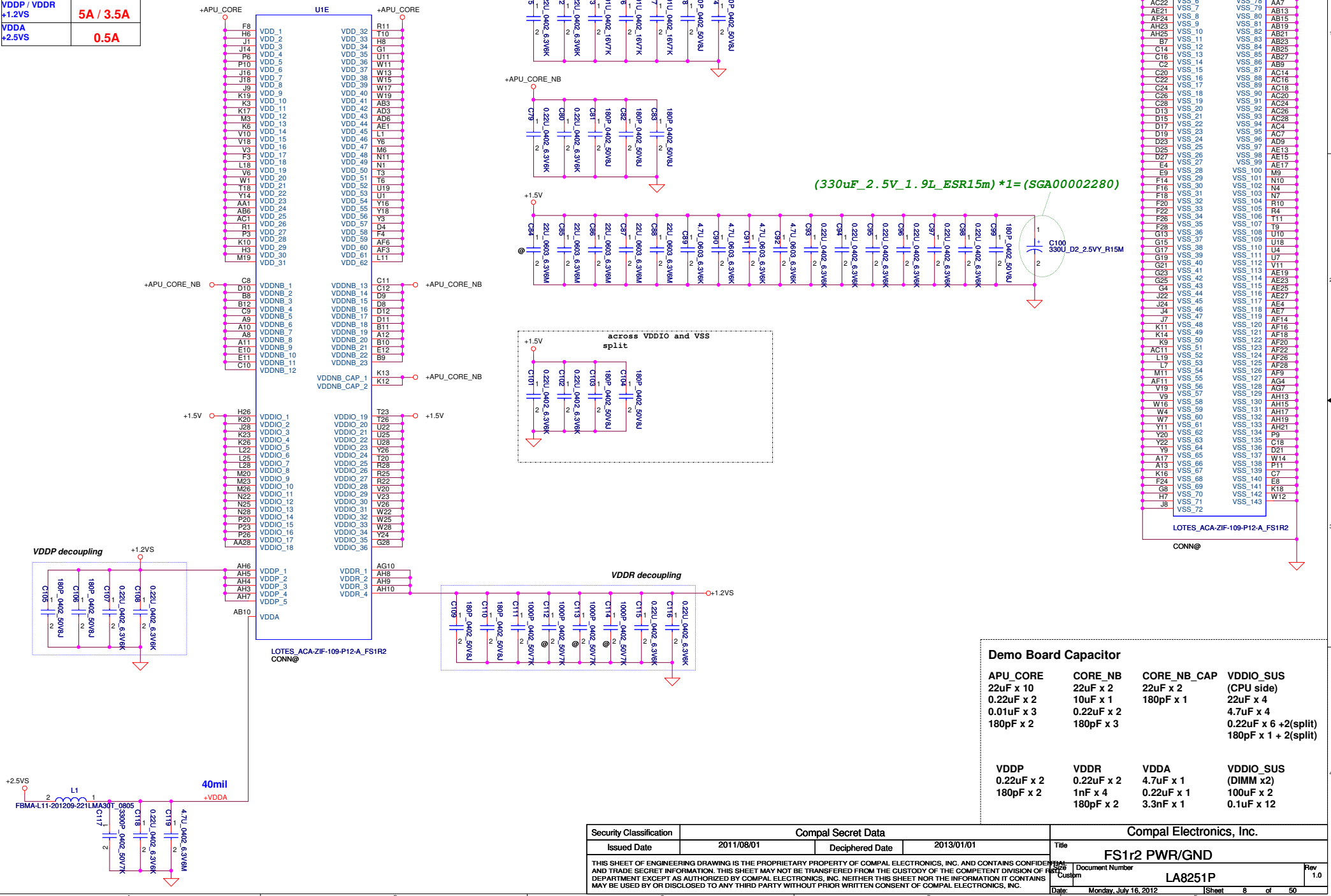
0.75V reference voltage



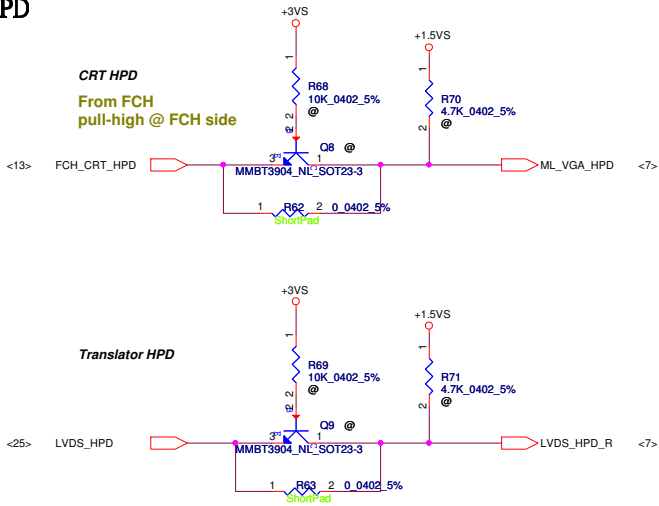
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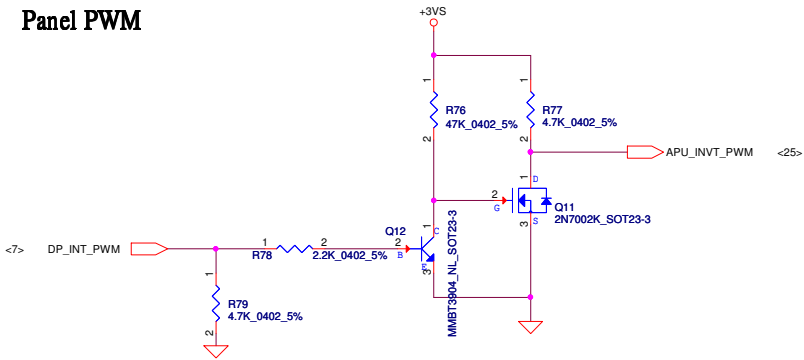
Power Name	Consumption
VDD +APU_CORE	60A
VDDNB +APU_CORE_NB	29A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A



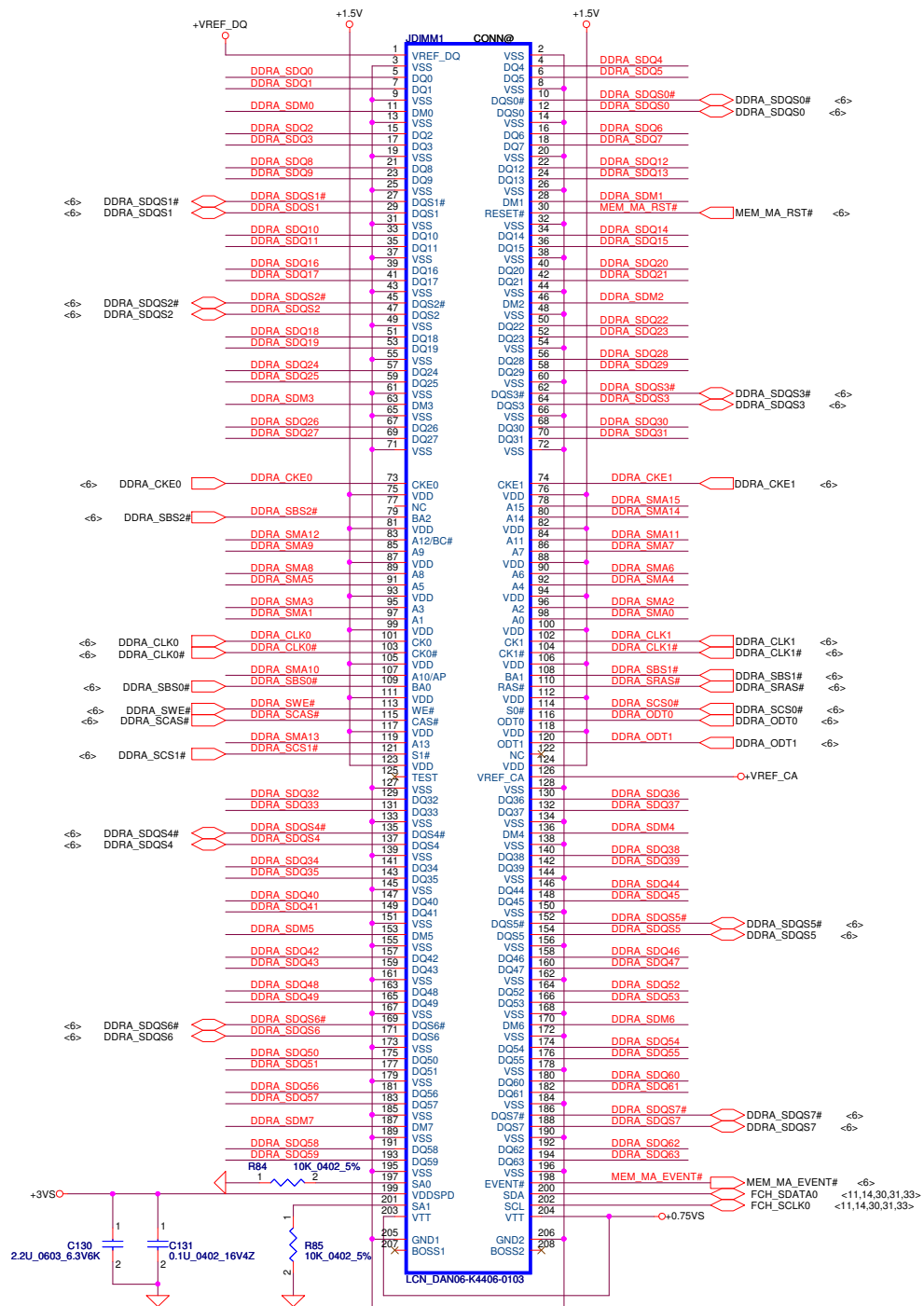
HPD



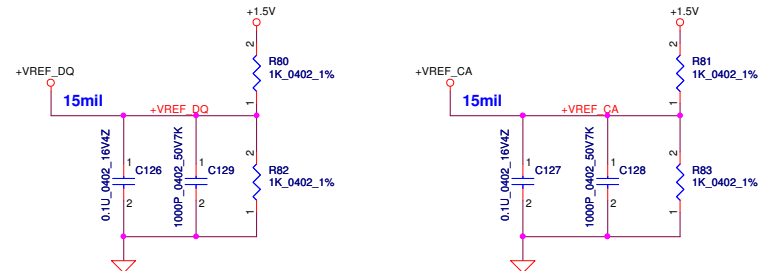
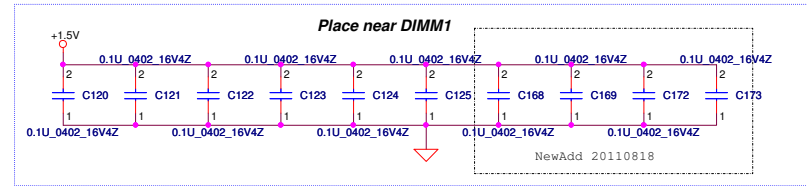
Panel PWM



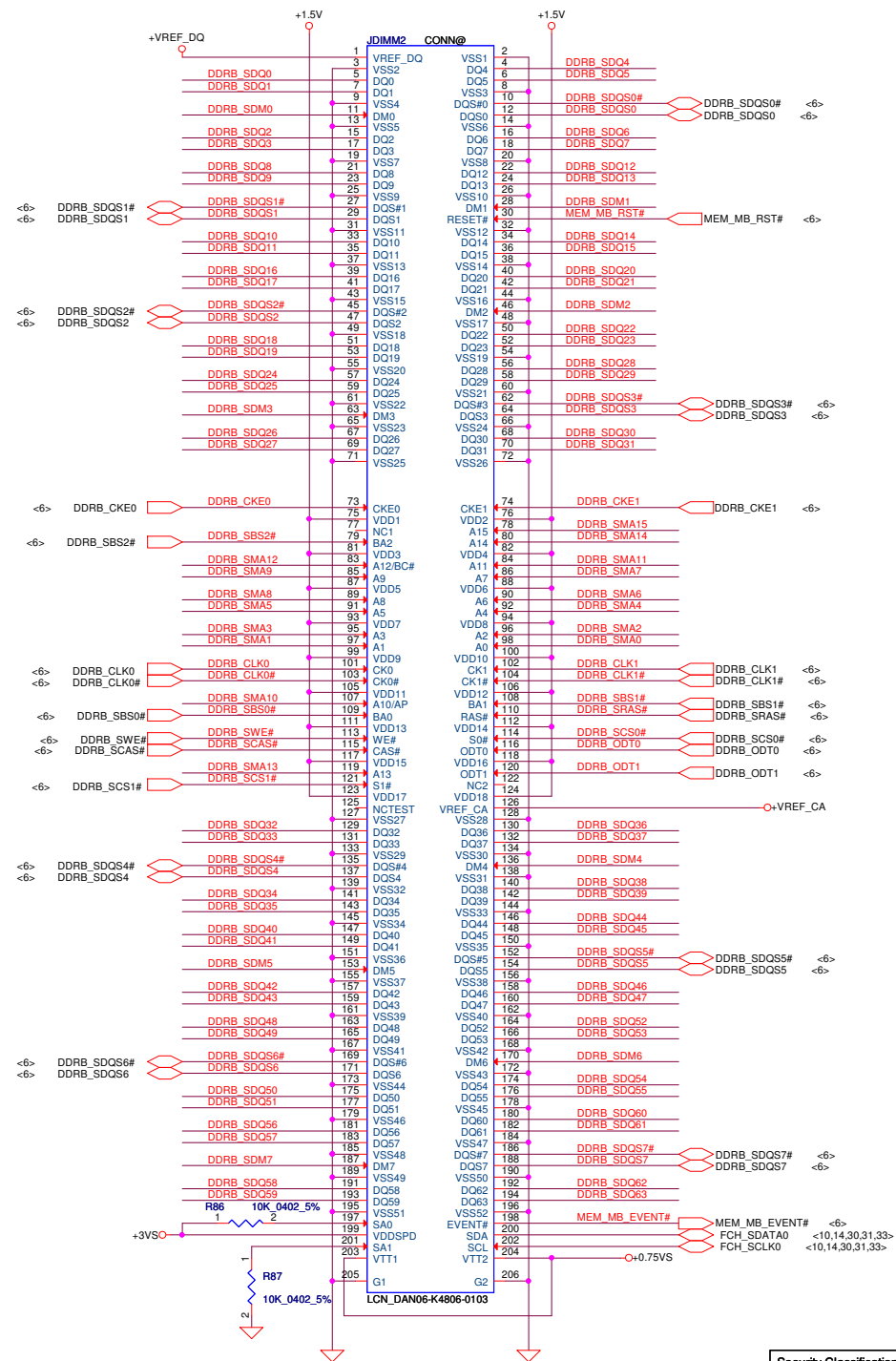
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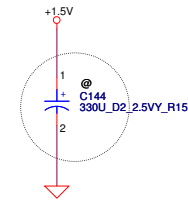
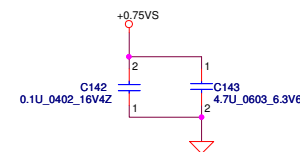
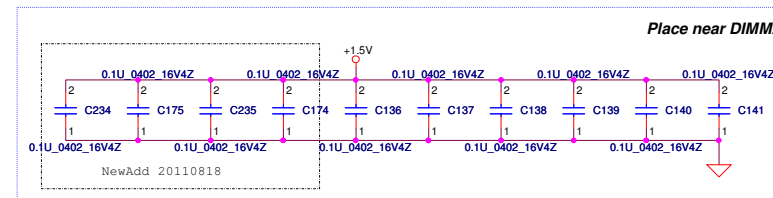
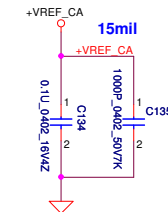
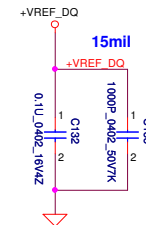
DDR_A_SQ[0..63] <6>
 DDR_A_SDM[0..7] <6>
 DDR_A_SMA[0..15] <6>



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DDR_B_SDM[0.7] DDR_B_SDM[0.7] <6>
DDR_B_SMA[0.15] DDR_B_SMA[0.15] <6>

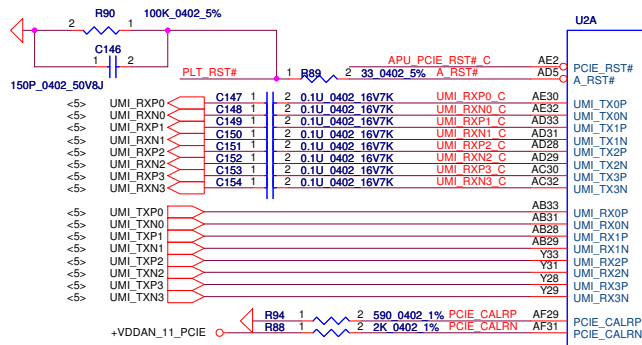


Reserve H:8mm
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U2
FCH-M3
Part Number = SA000043ISL

R90/ C146 close to FCH



Move PCIe device to APU. 20110819

SS

APU DISP

NSS

APU

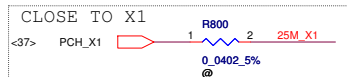
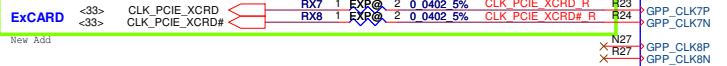
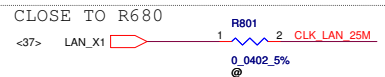
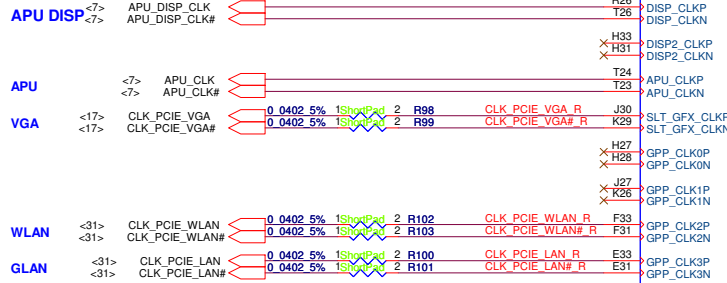
VGA

SS

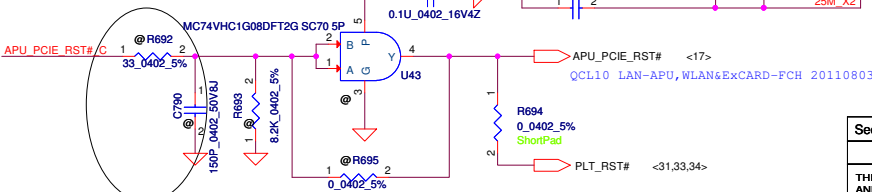
WLAN

GLAN

For "EXT" CLK mode, input to PCIe,



For PCIe device reset on FS1
(GFX, GLAN, WLAN, LVDS Travis)
APU_PCIE_RST# : Reset PCIe device on APU



R692/ C790 close to FCH

U2A

HUDSON-2

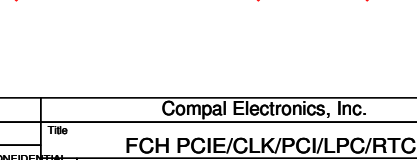
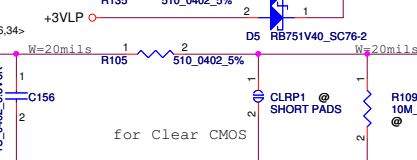
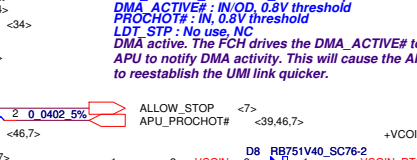
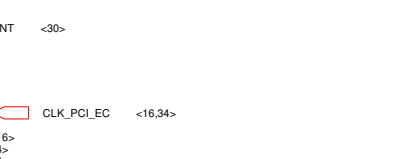
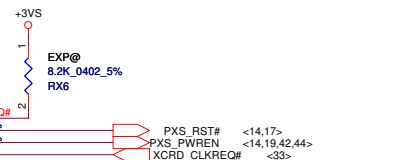
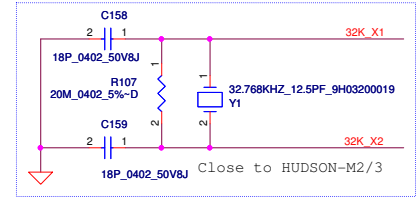
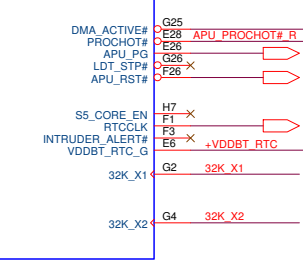
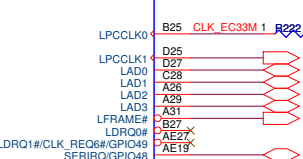
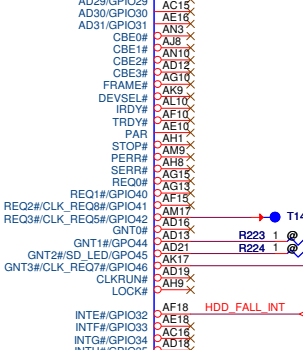
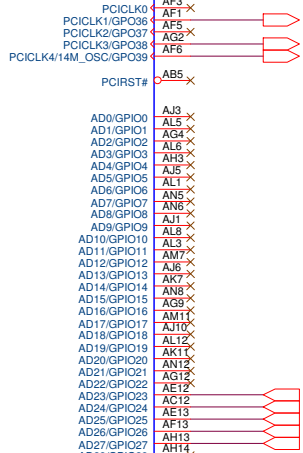
PCI EXPRESS INTERFACES

PCI CLK

CLOCK GENERATOR

APU

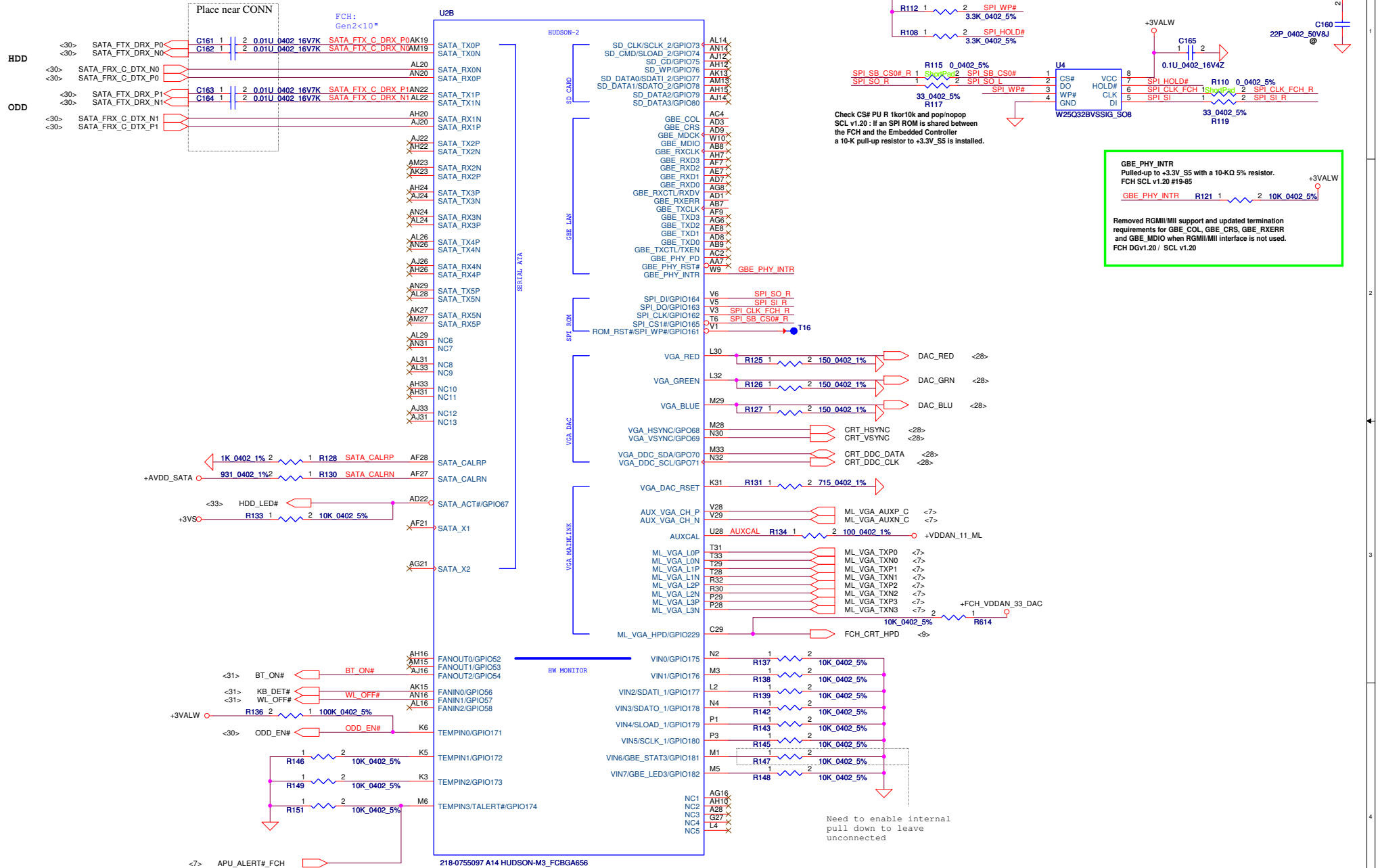
SS PLUS



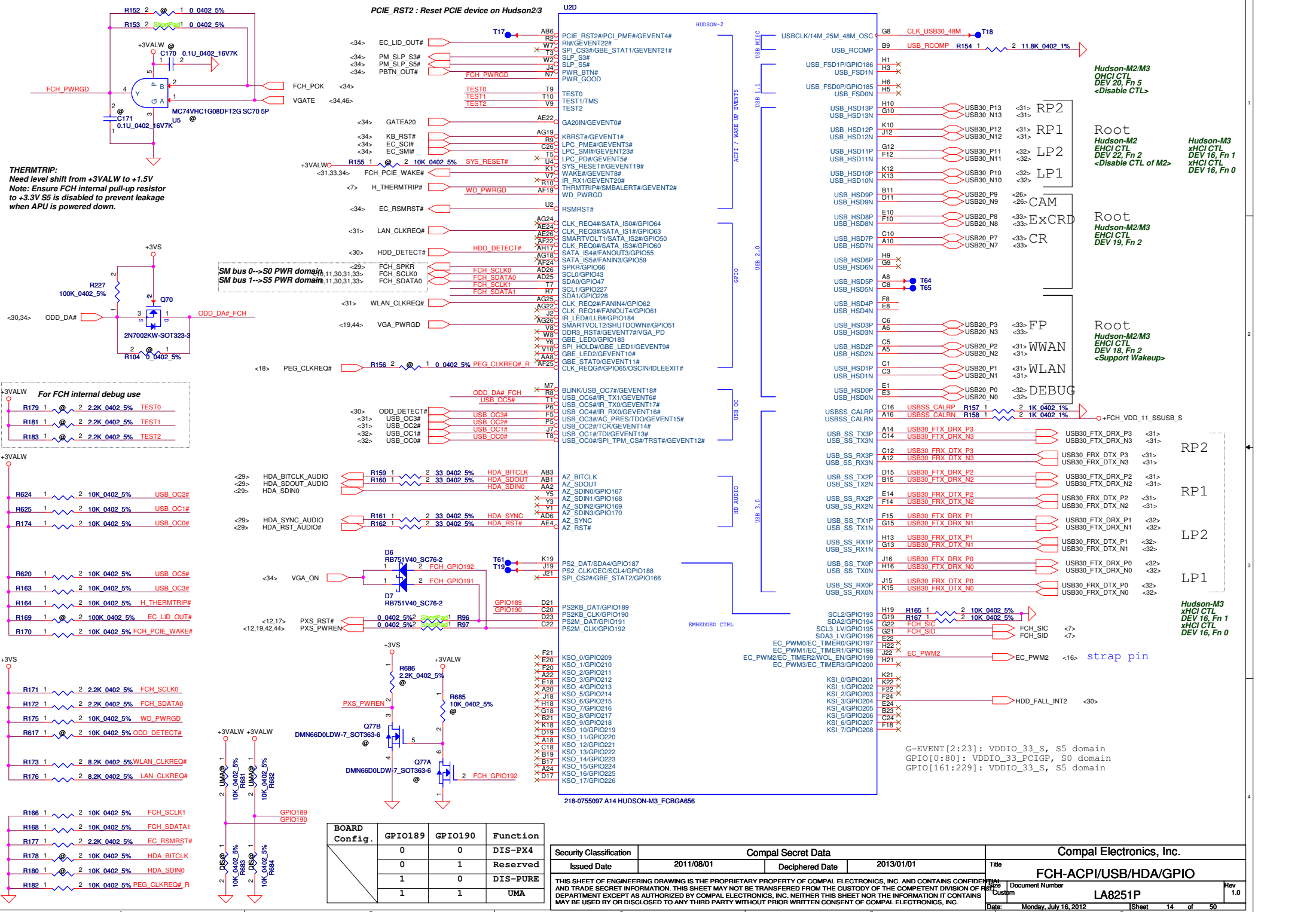
APU_PG/APU_RST#/LDT_STP# : OD pin
DMA_ACTIVE# : IN/OD, 0.8V threshold
PROCHOT# : IN, 0.8V threshold
LDT_STP : No use, NC
DMA active. The FCH drives the DMA_ACTIVE# to
APU to notify DMA activity. This will cause the APU
to reestablish the UMI link quicker.

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4MB SPI ROM & Non-share ROM.



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								Custom			
								Date: Monday, July 16, 2012			



THERMTRIP:
Need level shift from +3VALW to +1.5V
Note: Ensure FCH internal pull-up resistor
to +3.3V S5 is disabled to prevent leakage
when APU is powered down.

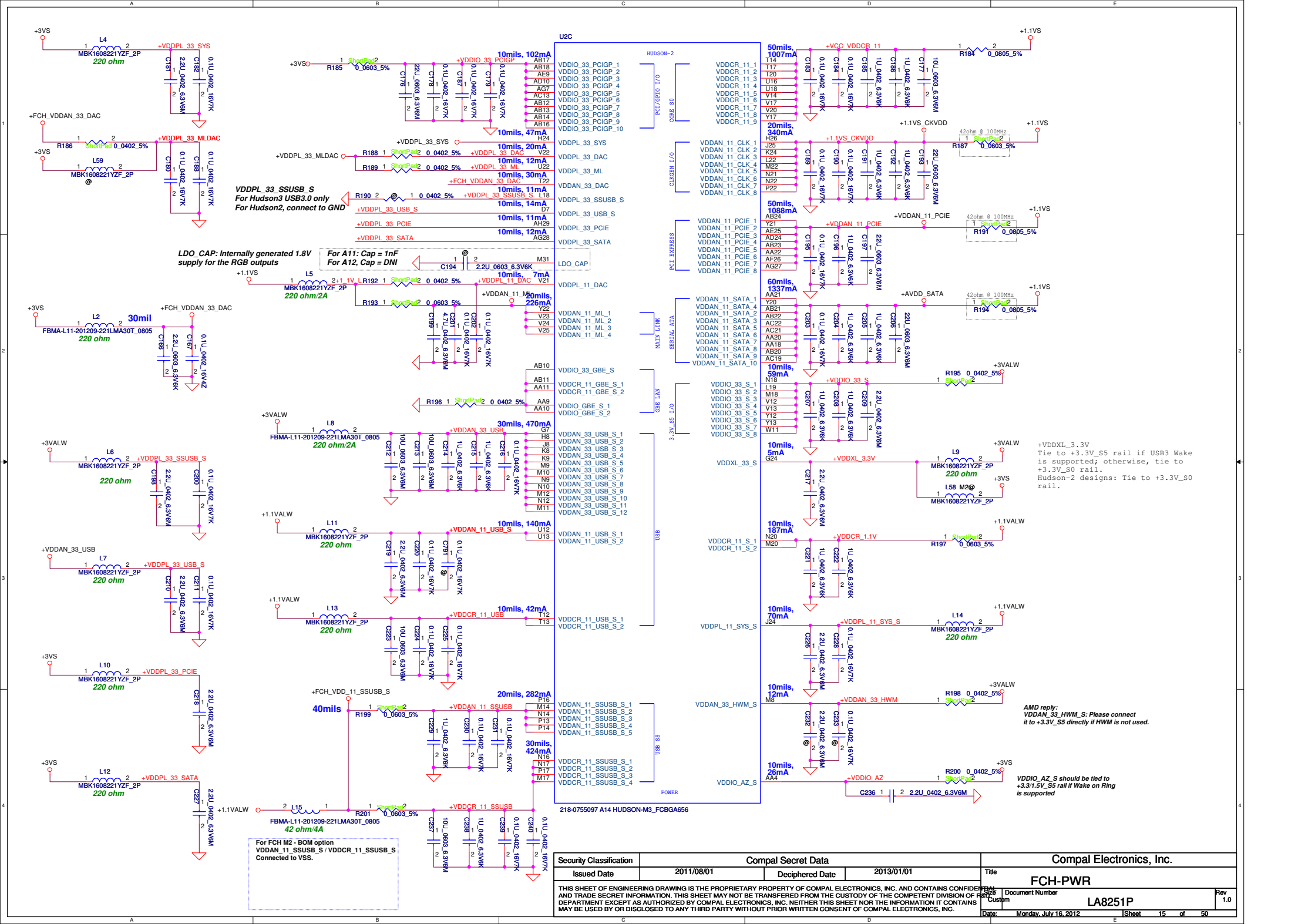
For FCH internal debug use
R179 1 2 2.2K 0402 5% TEST0
R181 1 2 2.2K 0402 5% TEST1
R183 1 2 2.2K 0402 5% TEST2

R171 1 2 2.2K 0402 5% FCH_SCLK0
R172 1 2 2.2K 0402 5% FCH_SDAT0
R175 1 2 10K 0402 5% WD_PWRGD
R617 1 2 10K 0402 5% ODD_DETECT#
R173 1 2 8.2K 0402 5% WLAN_CLKREQ#
R176 1 2 8.2K 0402 5% LAN_CLKREQ#

R166 1 2 10K 0402 5% FCH_SCLK1
R168 1 2 10K 0402 5% FCH_SDAT1
R177 1 2 2.2K 0402 5% EC_RSMRST#
R178 1 2 10K 0402 5% HDA_BITCLK
R180 1 2 10K 0402 5% HDA_SDIN0
R182 1 2 10K 0402 5% PEG_CLKREQ#

BOARD Config.	GPIO189	GPIO190	Function
	0	0	DIS-PX4
	0	1	Reserved
	1	0	DIS-PURE
	1	1	UMA

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								FCH-ACPI/USB/HDA/GPIO	
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						Document Number		Rev	
						LA8251P		1.0	
Date: Monday, July 16, 2012						Sheet		14 of 50	



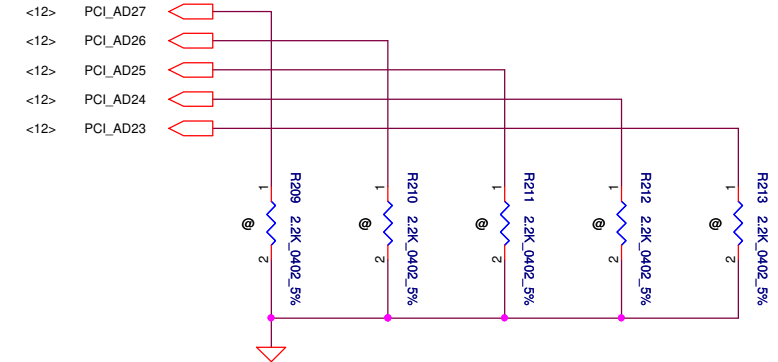
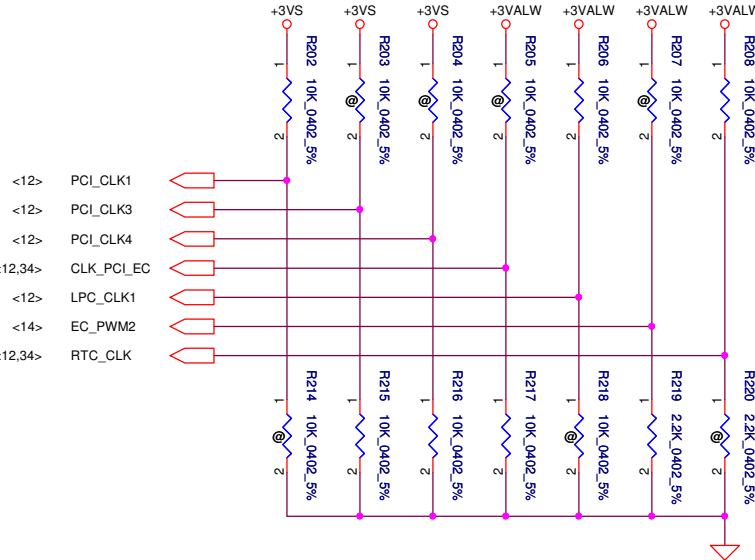
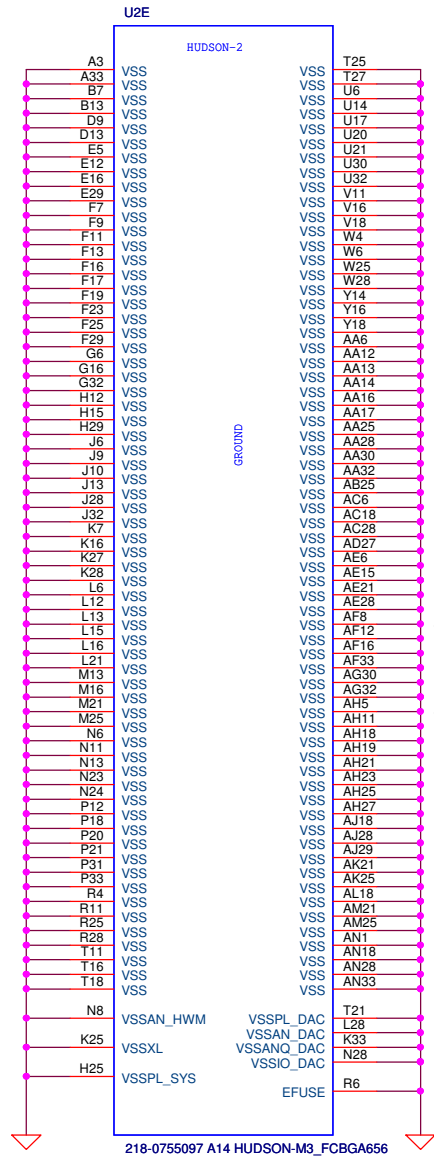
STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

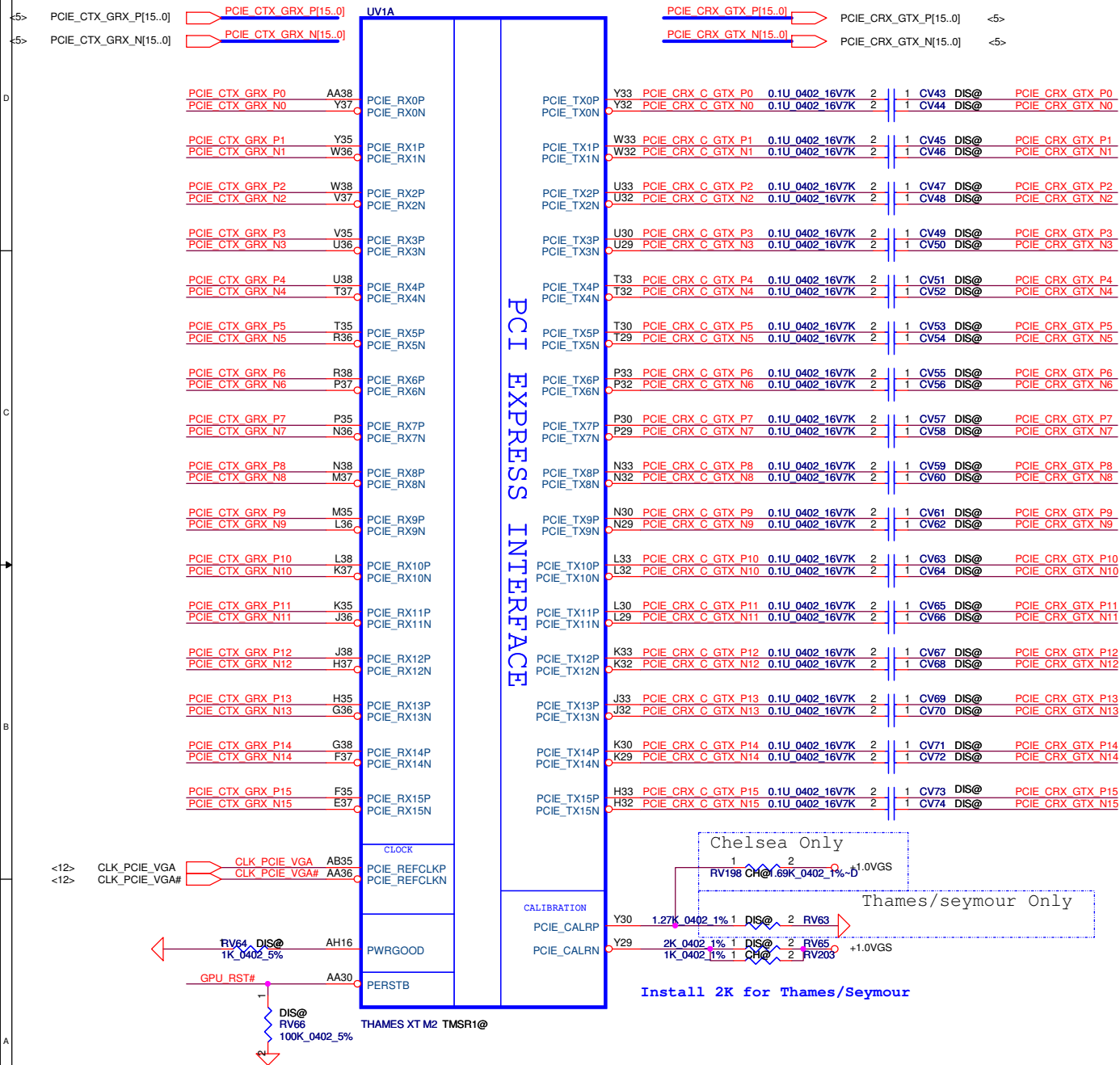
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

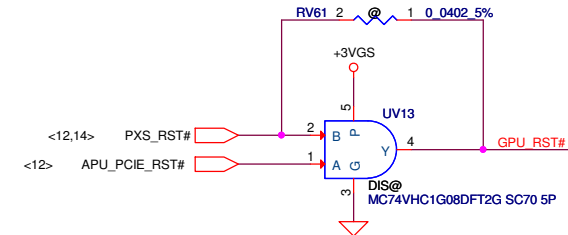
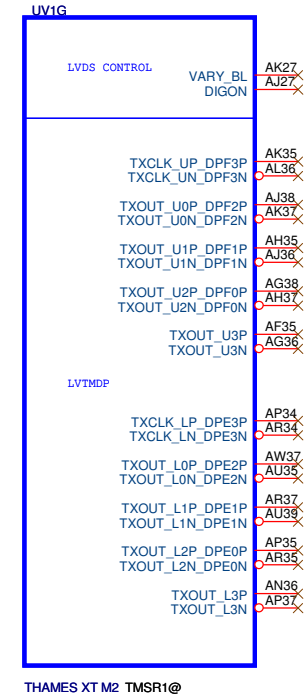


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				Date: Monday, July 16, 2012	Sheet 16 of 50

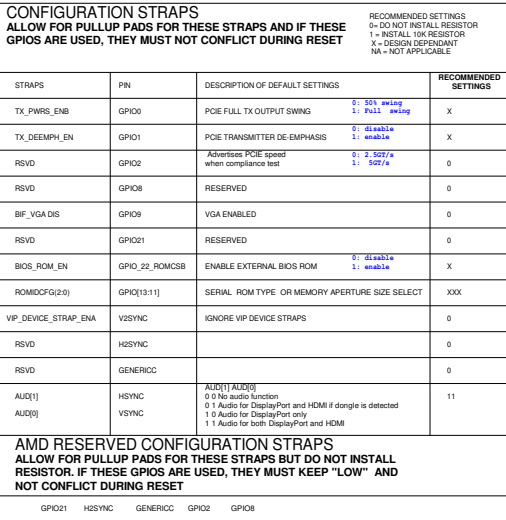
GFX PCIE LANE REVERSAL



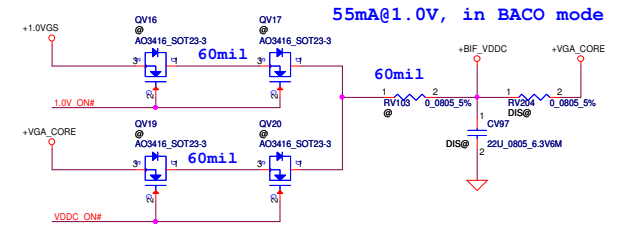
LVDS Interface



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				Date	Monday, July 16, 2012	Sheet 17 of 50

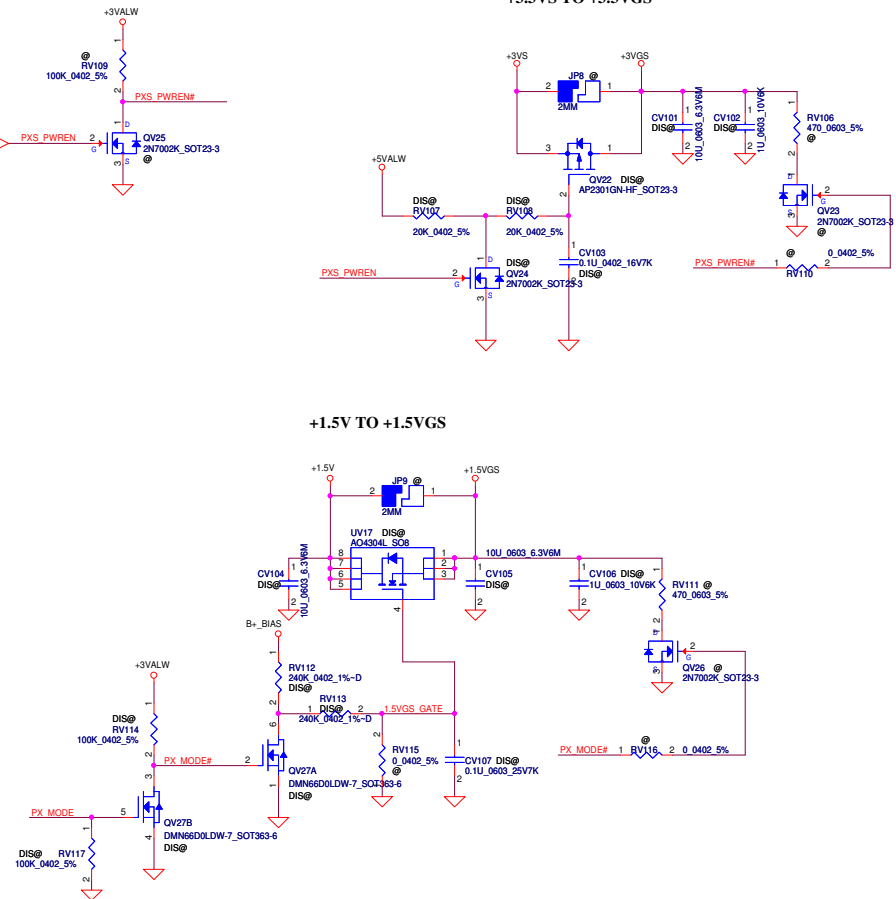


Switch circuits in BACO desings for Thanes/Seymour only

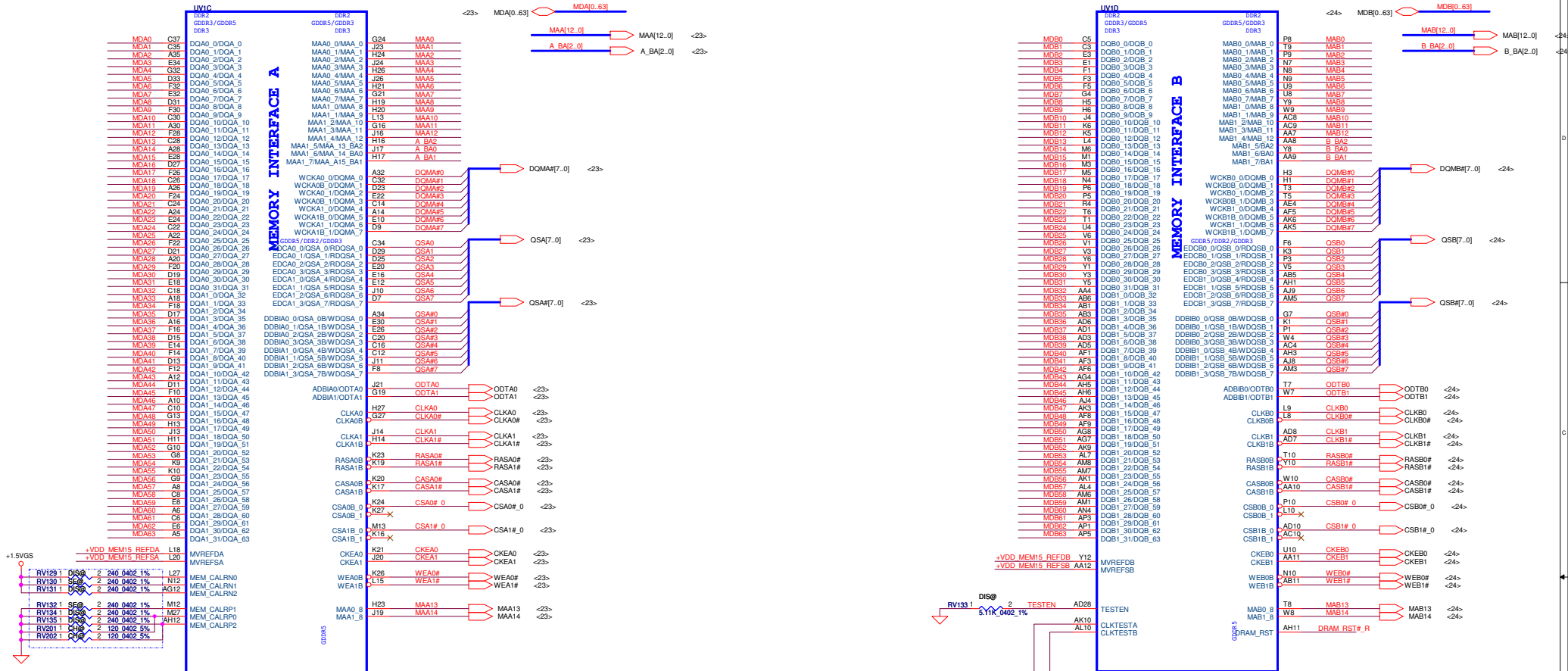


```
PX4.0 +VGA_CORE,VDDCI,+1.5VGS OFF
PX4.0 +3VGS, +1.0VGS,+1.8VGS ON
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF
```

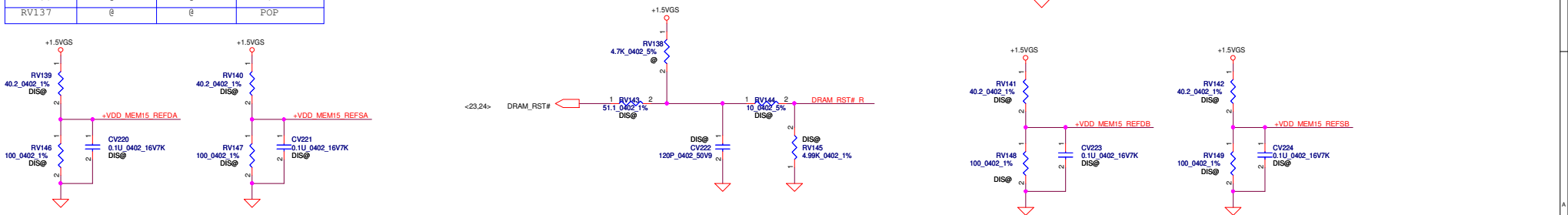
+1.5V TO +1.5VGS



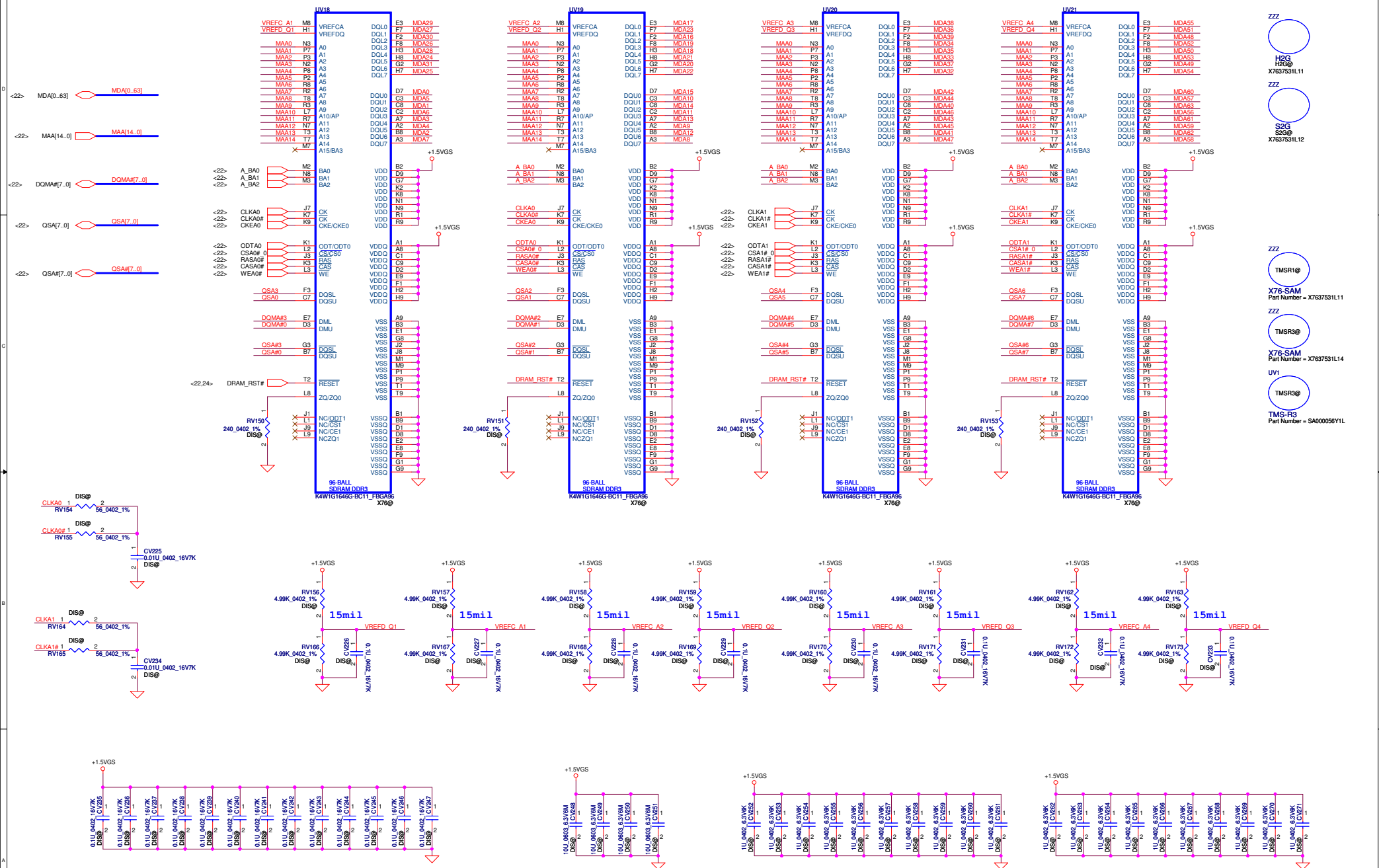
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/08/01	Deciphered Date	2013/01/01	Title	ATI SeymourXT M2 BACO POWER	
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				Date	Monday, July 16, 2012	ISheet



This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitor and Resistor values are an example only. The Series R and I Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec. Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2

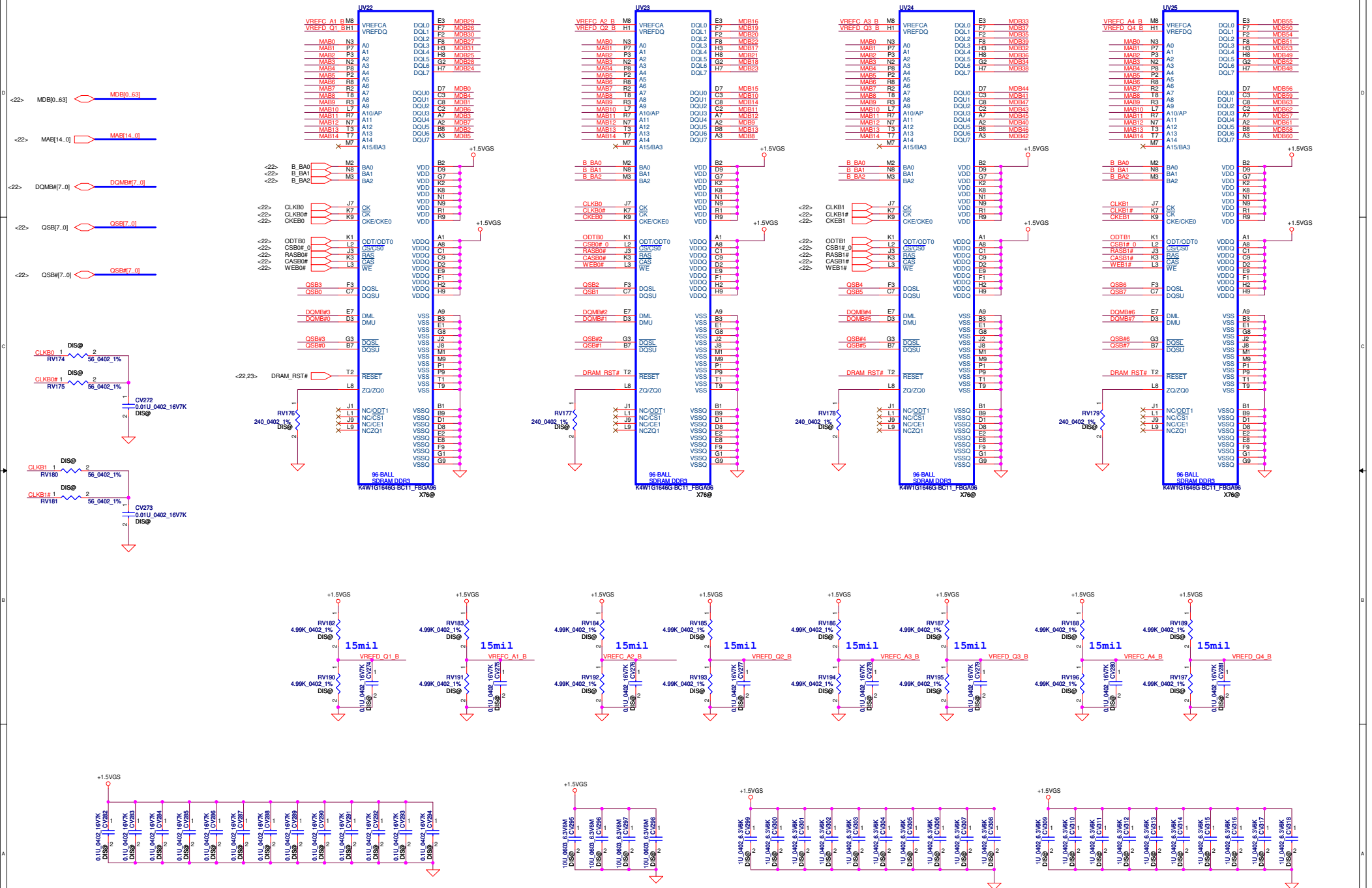


CHANNEL A: 256MB/512MB DDR3



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				ATI SeymourXT M2 VRAM A	
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				Document Number	1.0
				LA8251P	
Date:		Monday, July 16, 2012		Sheet	23 of 50

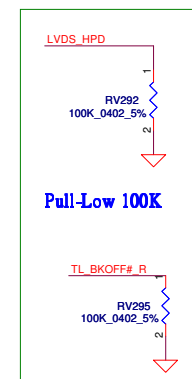
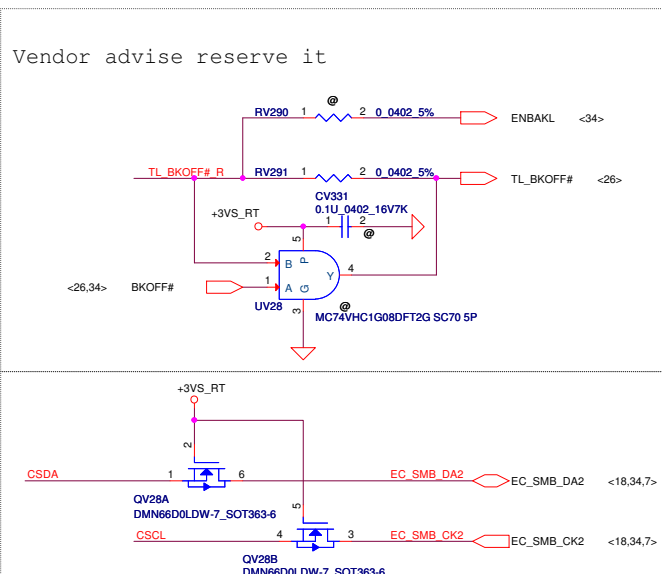
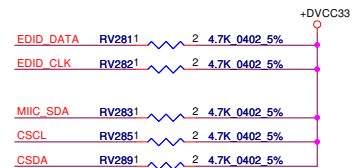
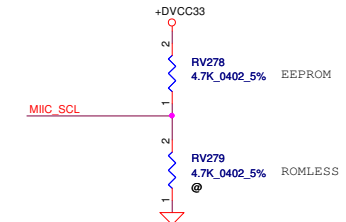
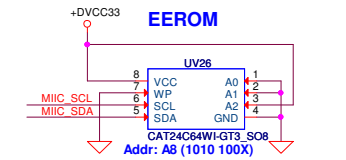
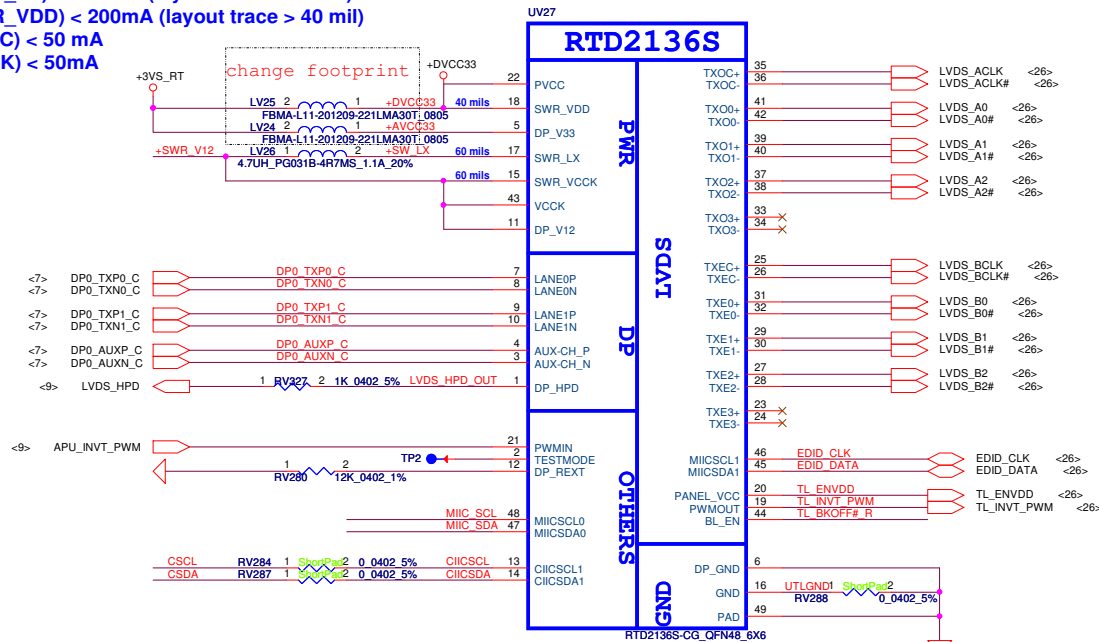
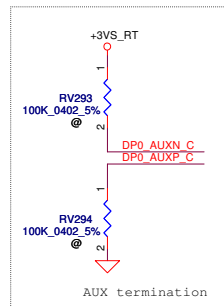
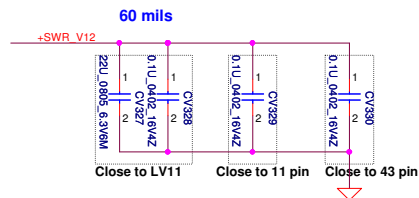
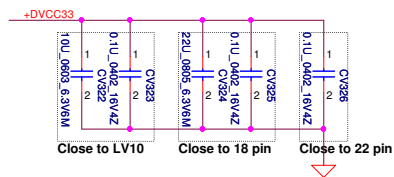
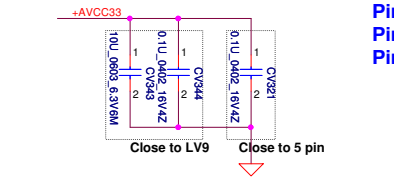
CHANNEL B: 256MB/512MB DDR3



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Size C	Document Number	LA8251P		Rev 1.0
Date: Monday, July 16, 2012	Sheet 24	of 50		

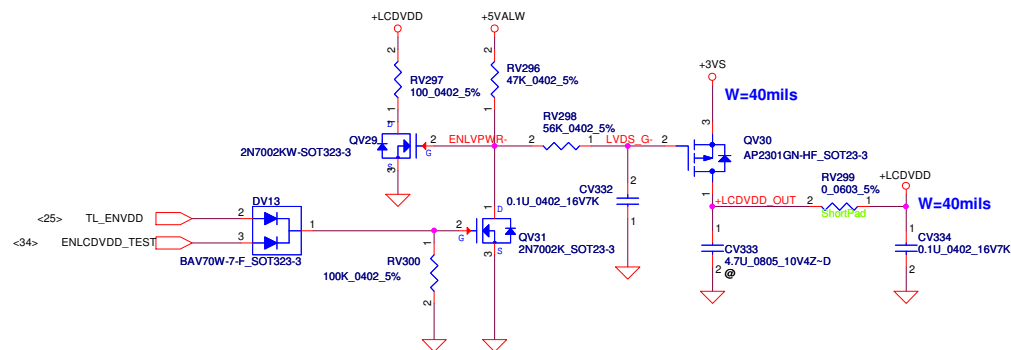
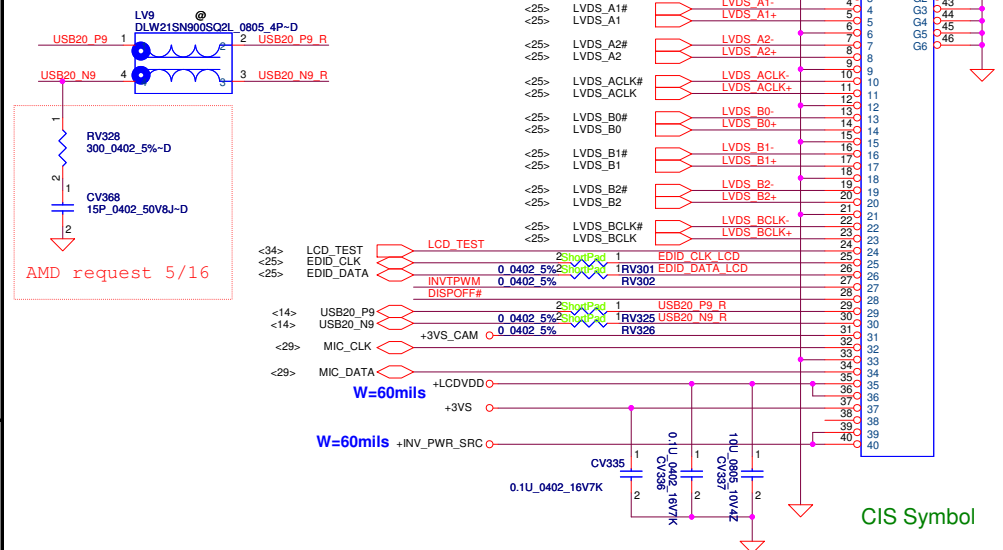
Power Consumption:

Pin5 (DPV33) < 20mA
 Pin 11 (DPV12) < 100mA
 Pin 15 (SWR_VCKK) < 100mA (layout trace > 60 mil)
 Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
 Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
 Pin 22 (PVCC) < 50 mA
 Pin 43 (VCKK) < 50mA

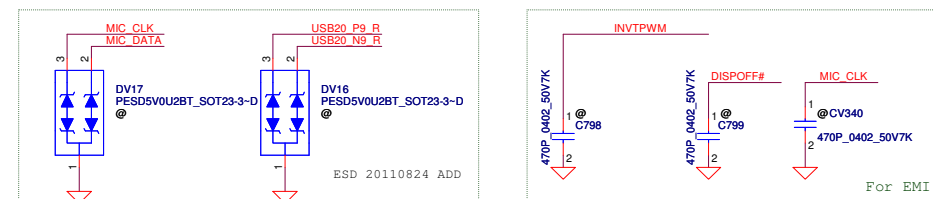
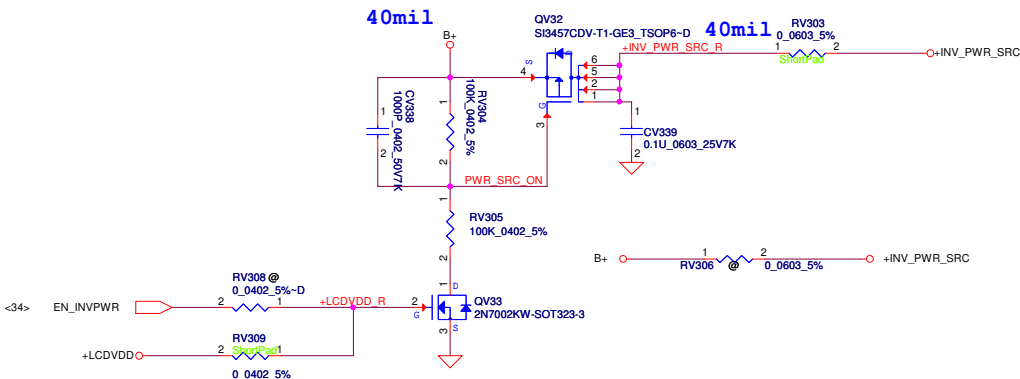
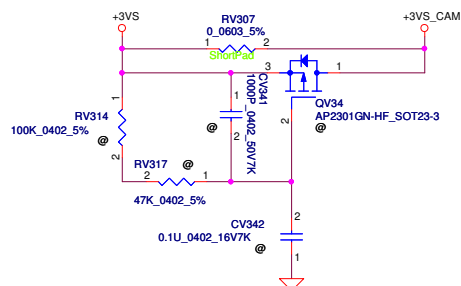


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						Document Number		LA8251P		Rev 1.0	
						Date		Monday, July 16, 2012		Sheet 25 of 50	

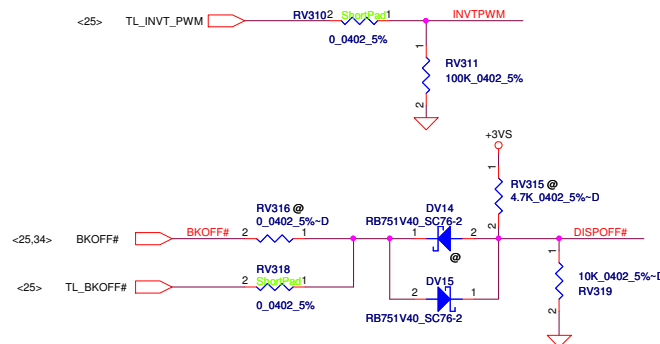
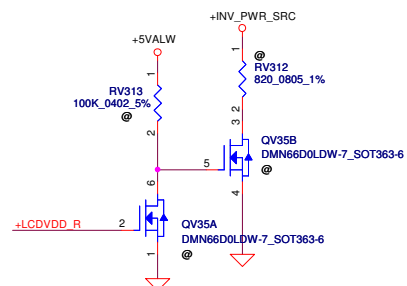
LCD PWR CTRL

**LVDS Conn.**

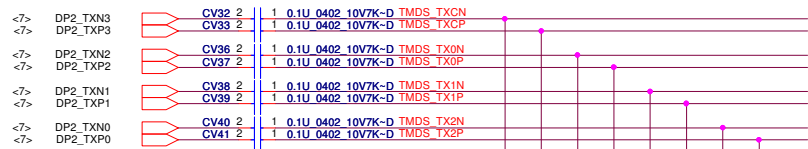
LCD backlight PWR CTRL

**Wedcam PWR CTRL**

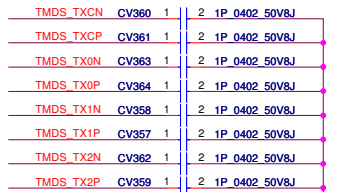
** Reserved for LCD
sequence tuning*



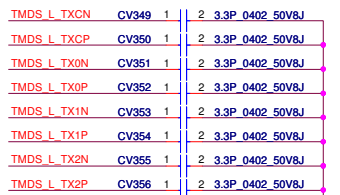
Security Classification		Compal Secret Data		Compal Electronics, Inc. Title: LVDS/CAMERA	
Issued Date	2011/08/01	Deciphered Date	2013/01/01	Document Number	LA8251P
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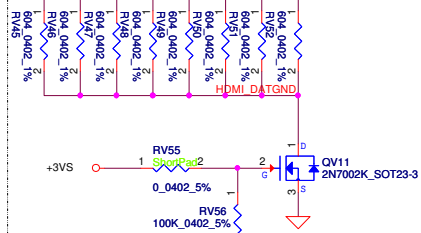
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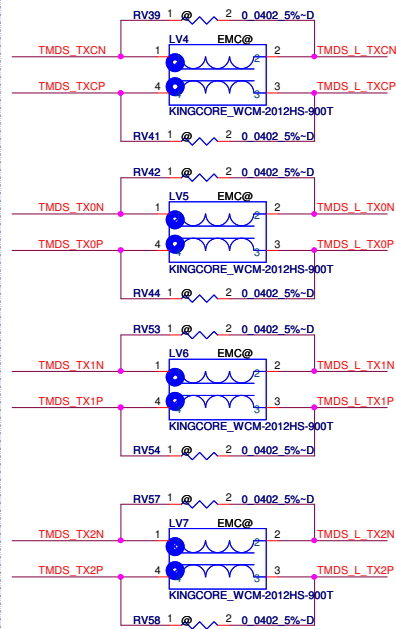
20111026 EMI reserve pi filter.



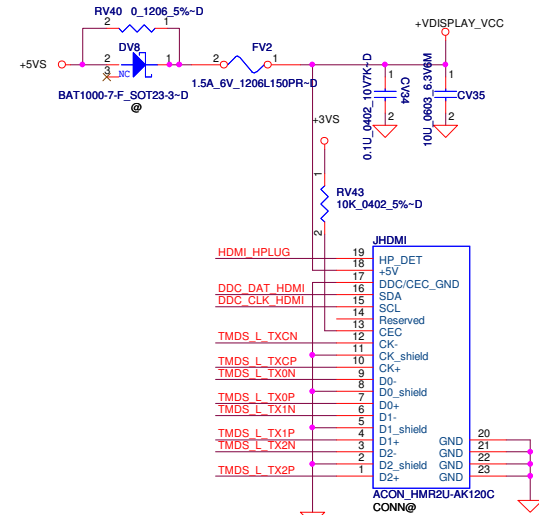
20110805 EMI ADD



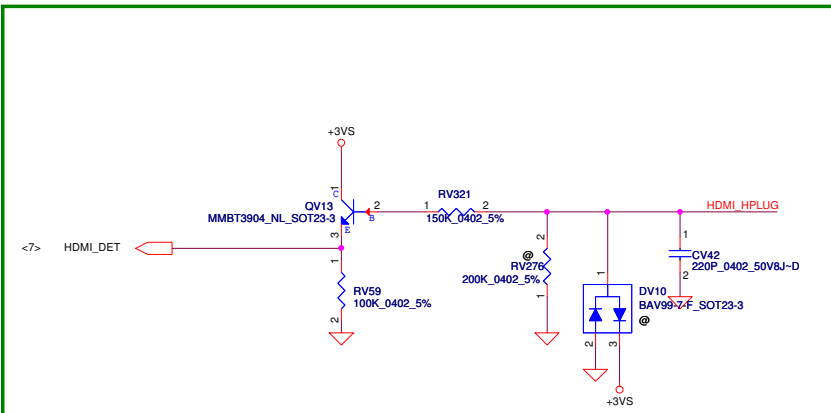
Place close to JHDMI1



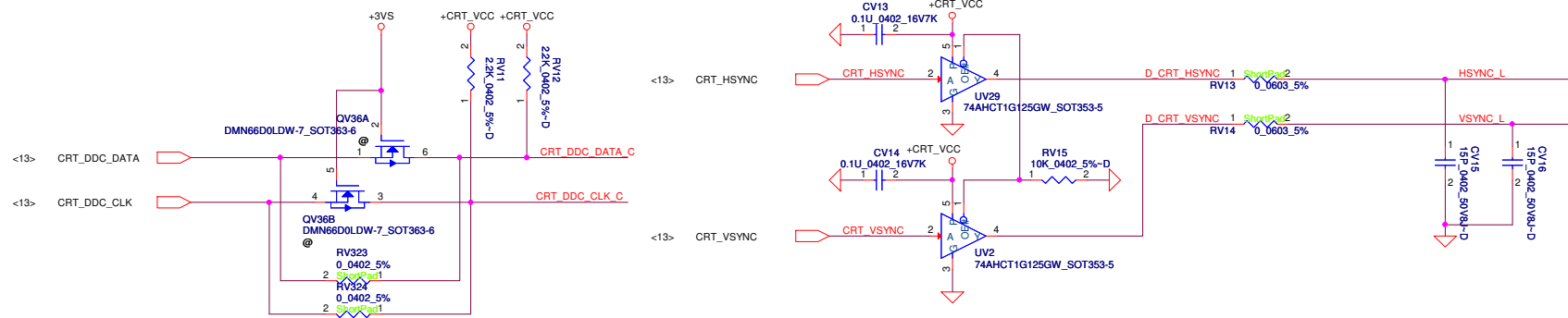
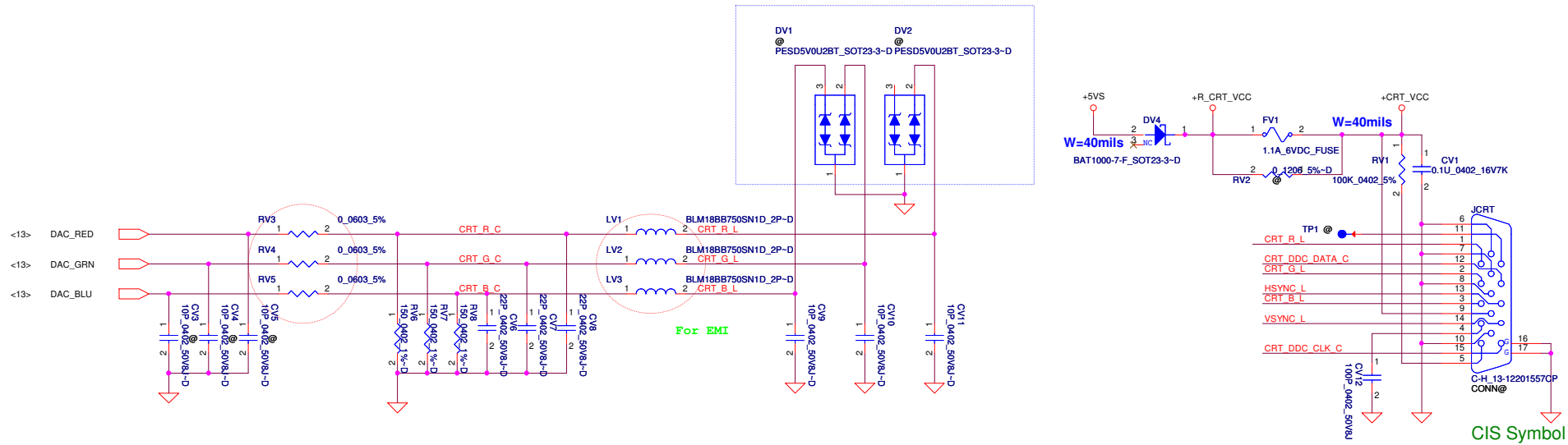
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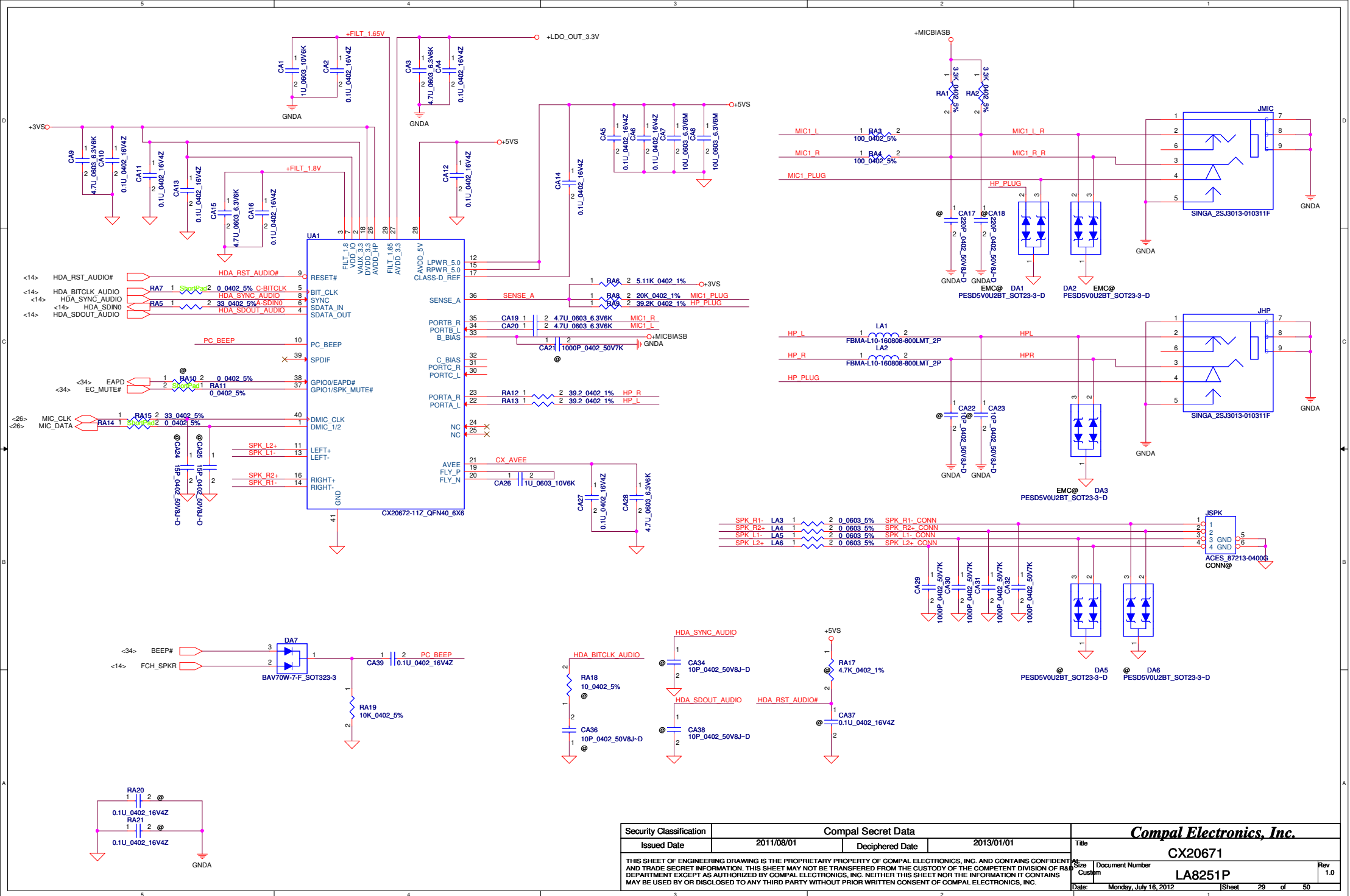
Part Number	Description
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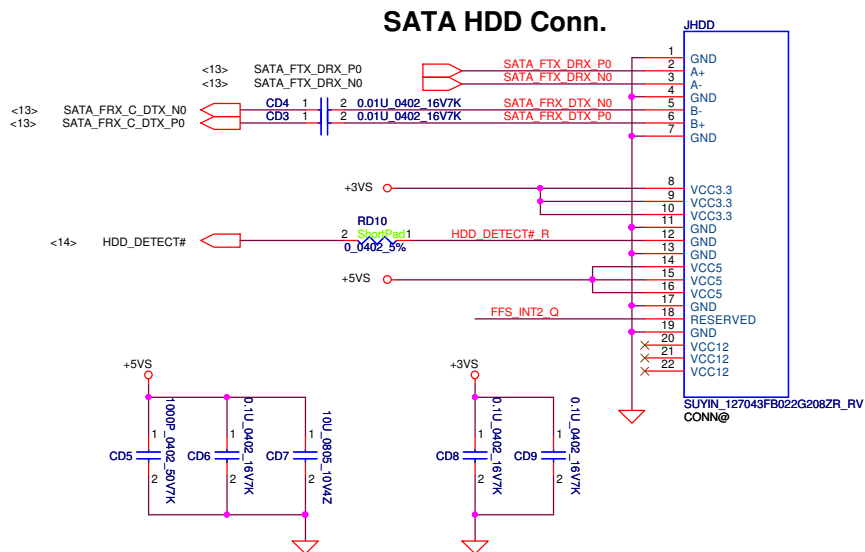
C R T



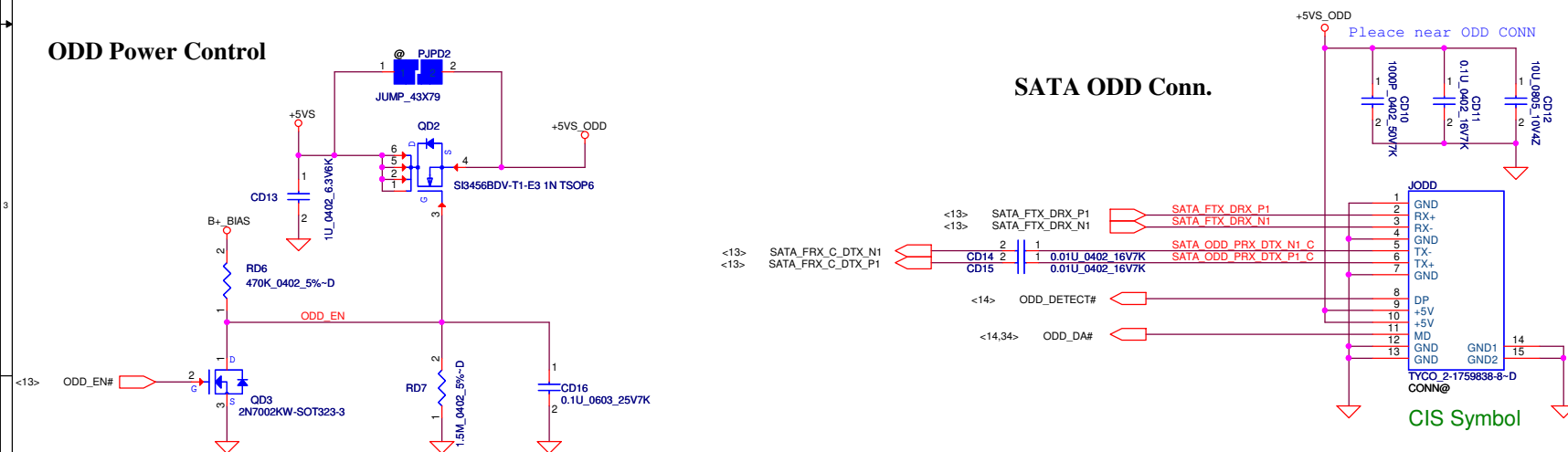
Security Classification		Compal Secret Data		Compal Electronics, Inc. CRT Conn.	
Issued Date	2011/08/01	Deciphered Date	2013/01/01	Title	
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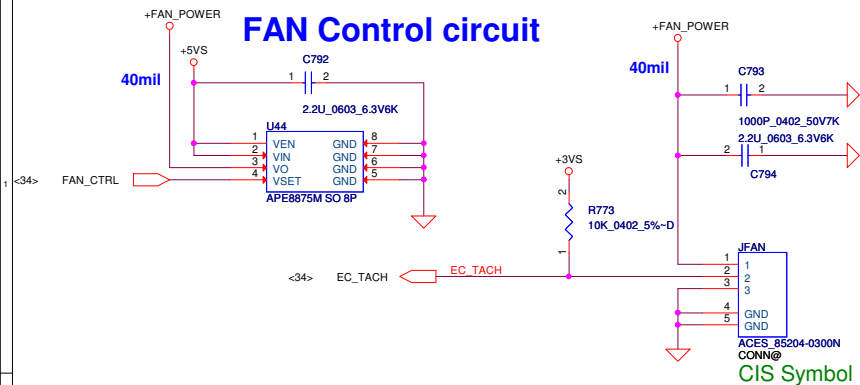


SATA ODD Conn.

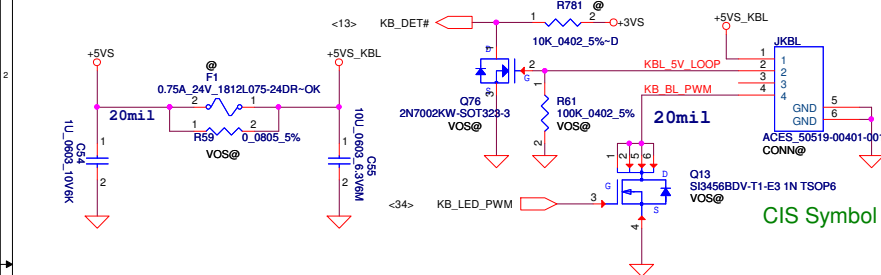


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Issued Date	2011/08/01	Deciphered Date	2013/01/01	Title	HDD/ODD/FAN
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				Custom LA8251P	1.0
Date: Monday, July 16, 2012				Sheet	30 of 50

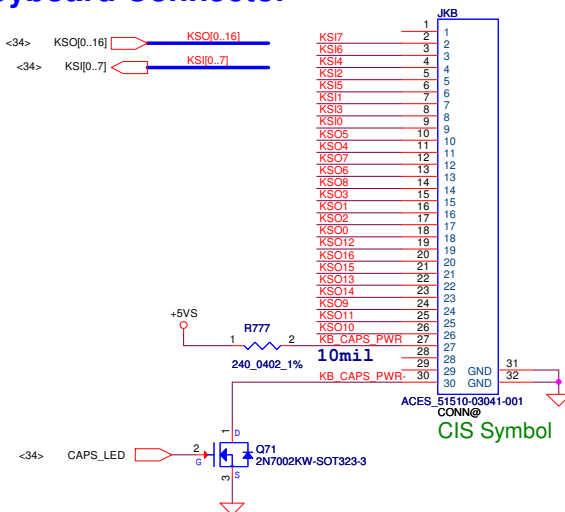
FAN Control circuit



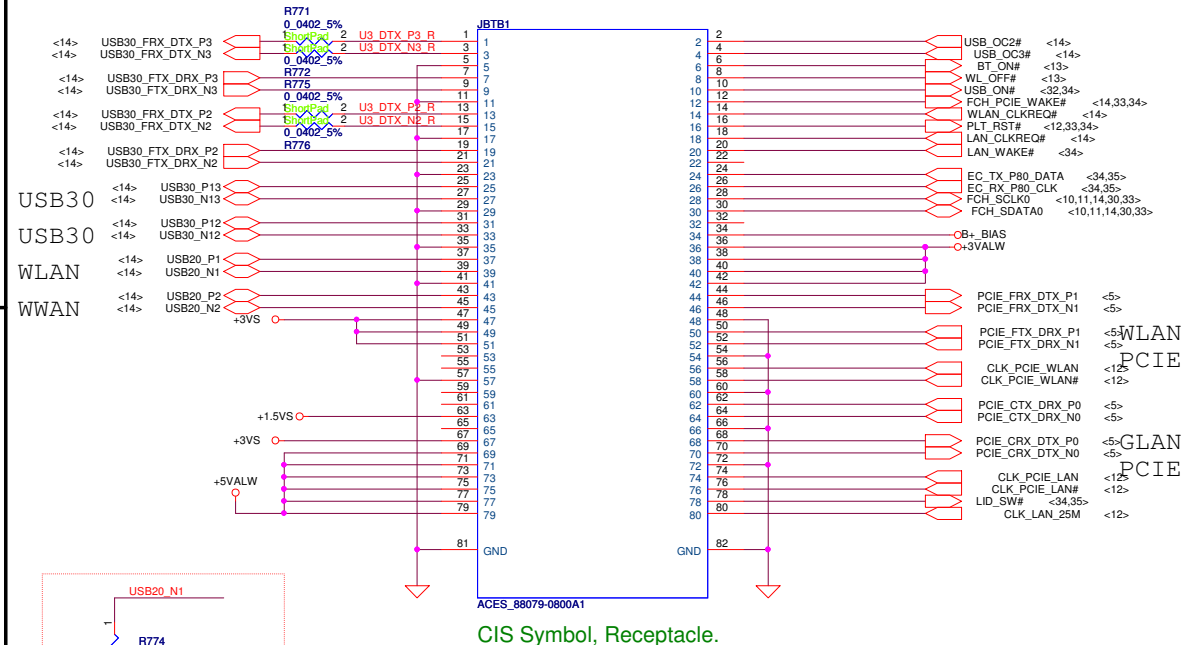
Keyboard back light



Keyboard Connector

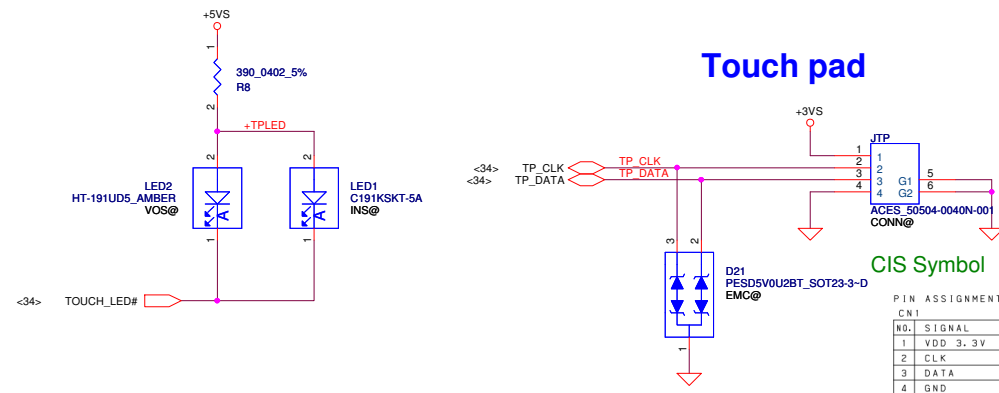


M/B to D/B BTB connector, LAN, FMC, HMC, USB3.0*2



AMD request 5/16

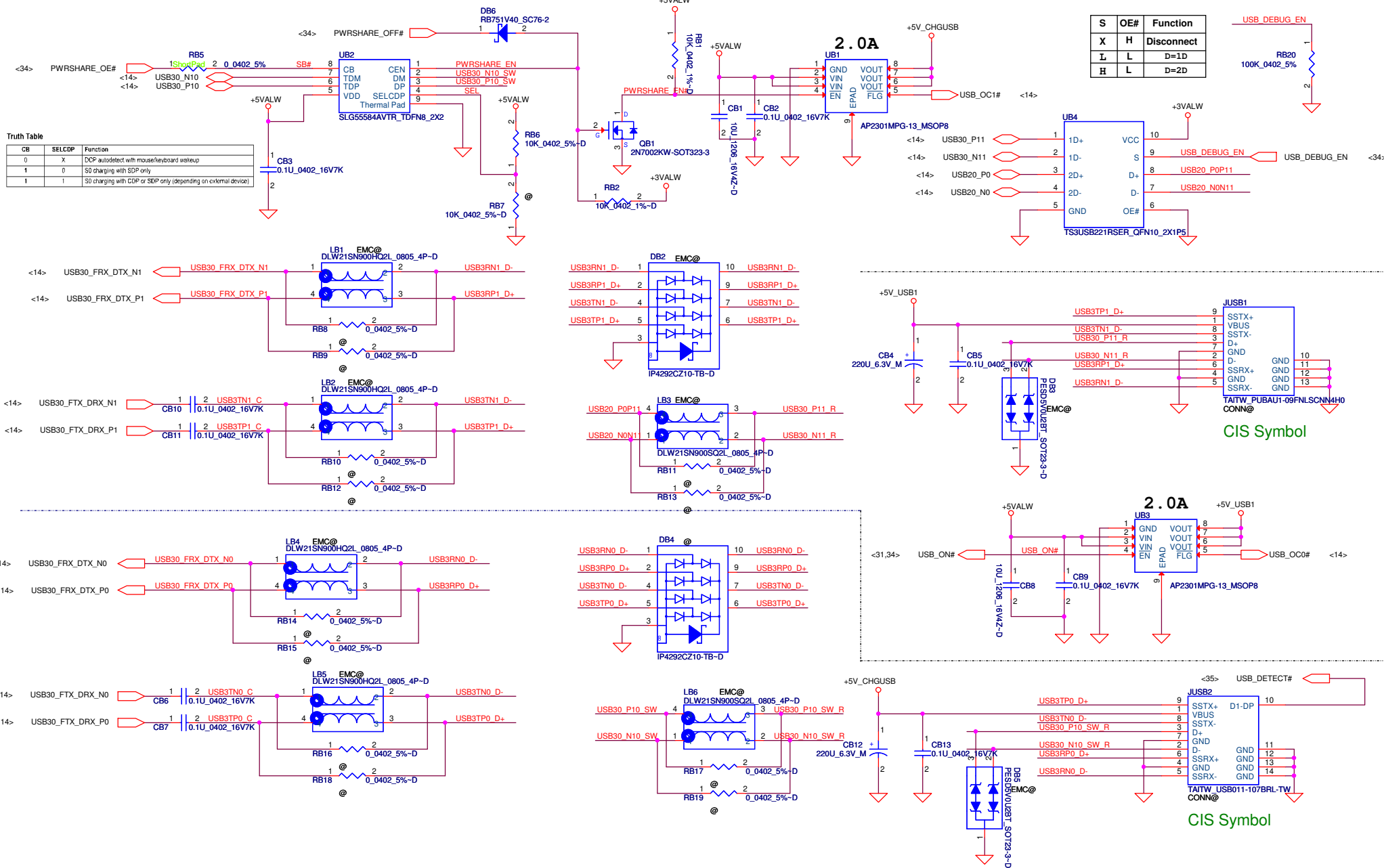
Touch pad



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Issued Date	2011/08/01	Deciphered Date	2013/01/01	Title	
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Date: Monday, July 16, 2012		Sheet 31 of 50			

Power share

CB	Function
L	auto detection charger identification active
H	DP/DM=TDF/TDM

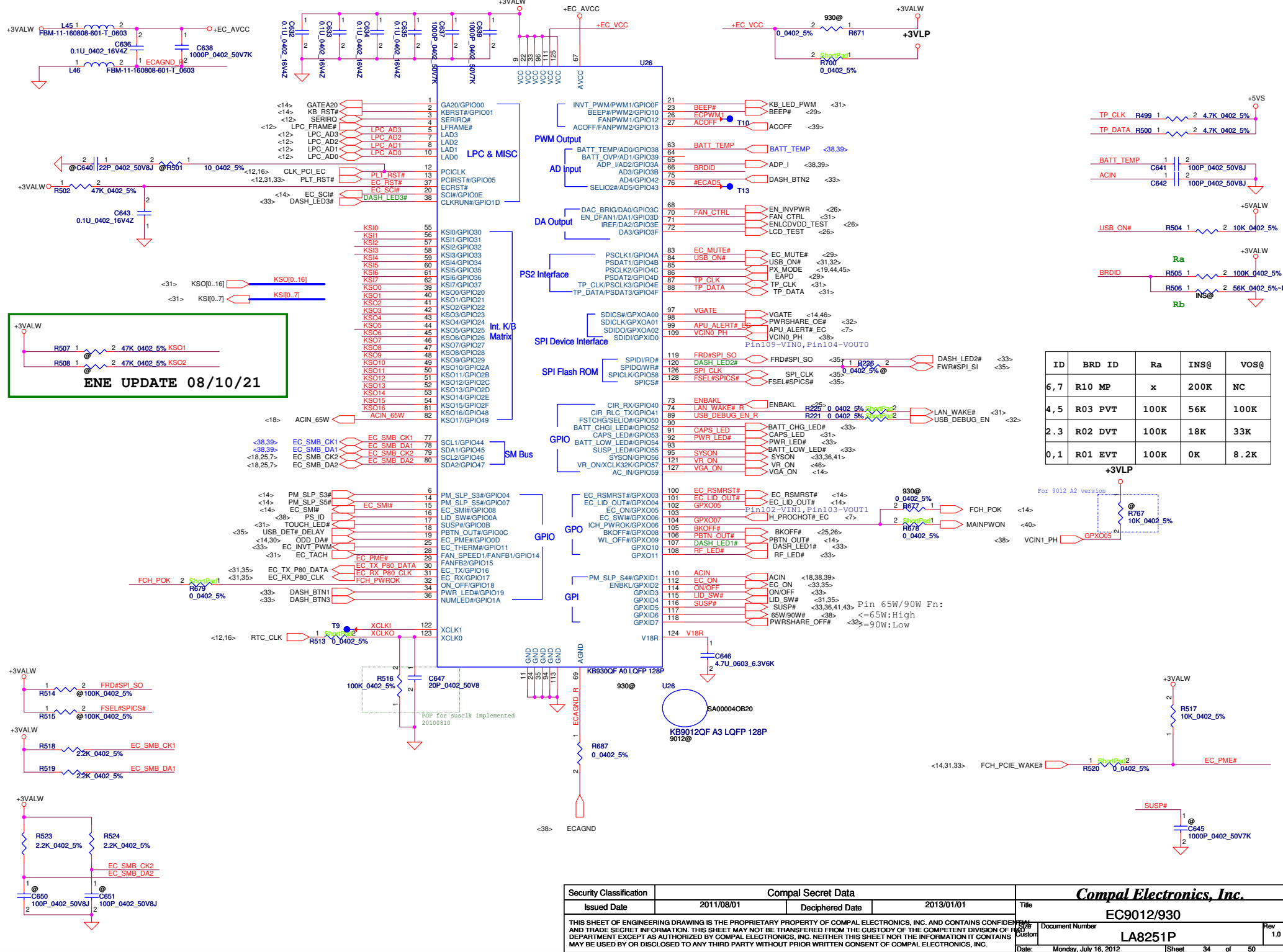


S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D



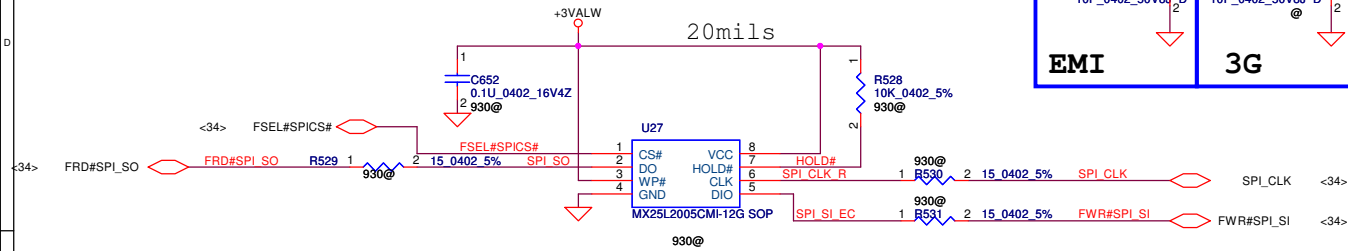
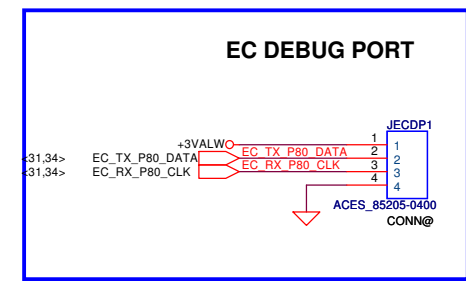
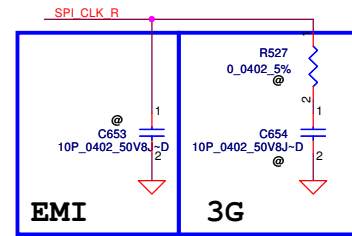
CB	SELCDP	Function
0	X	DCP autidetect with mouse/keyboard wakeup
1	0	SD charging with SDP only
1	1	SD charging with CDP or SDP only (depending on external device)

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Size Custom				Document Number	
Date: Monday, July 16, 2012				LA8251P	
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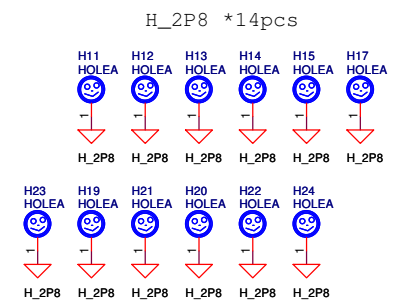
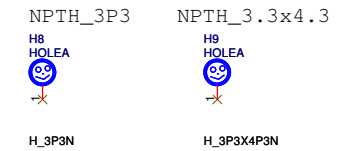
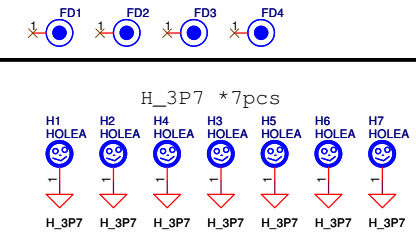
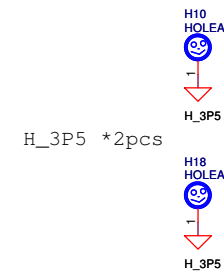
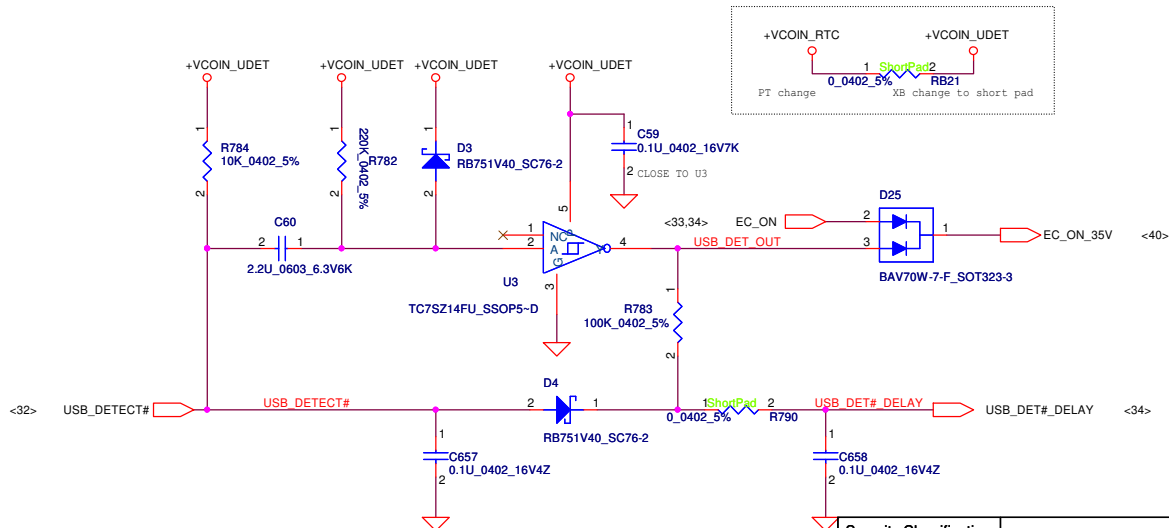
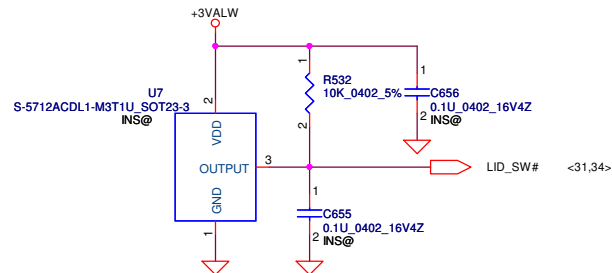


ID	BRD ID	Ra	INS@	VOS@
6, 7	R10 MP	x	200K	NC
4, 5	R03 PVT	100K	56K	100K
2, 3	R02 DVT	100K	18K	33K
0, 1	R01 EVT	100K	0K	8.2K

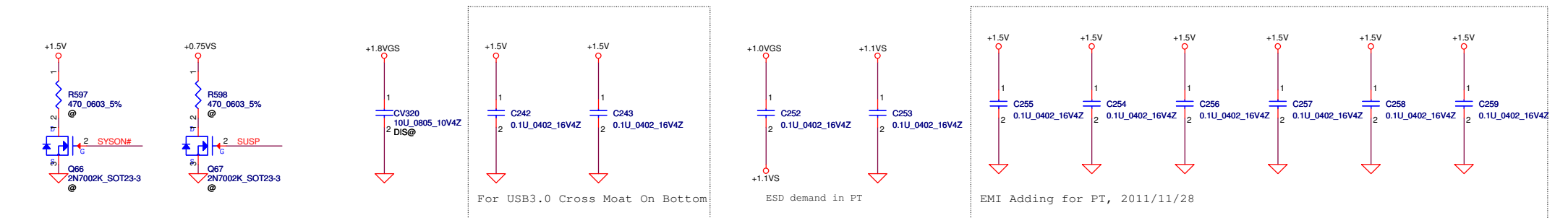
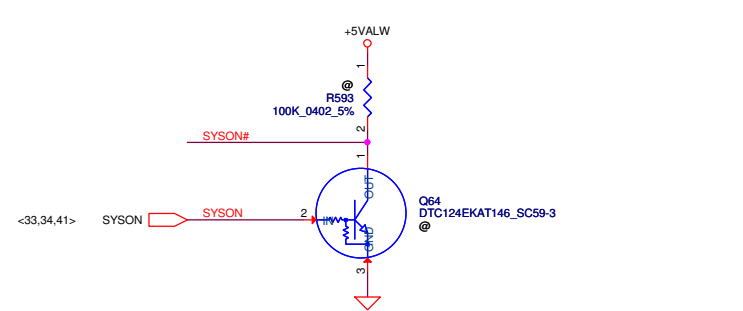
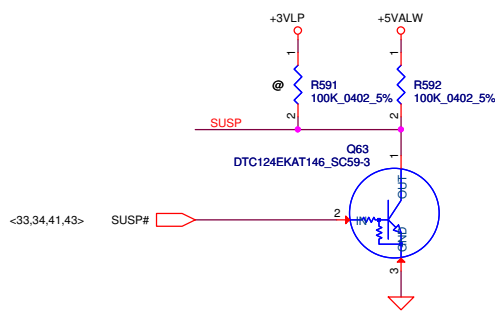
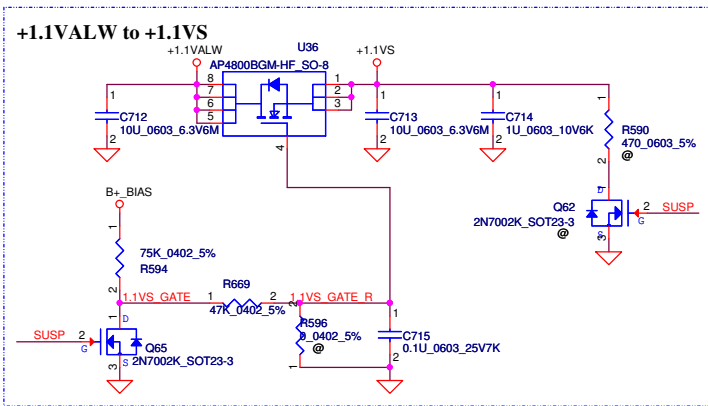
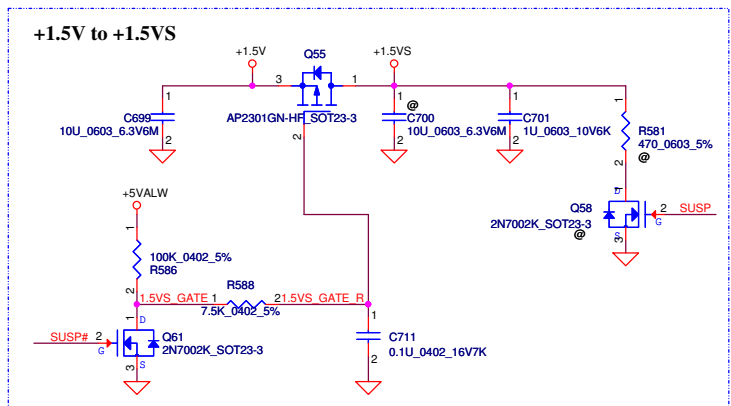
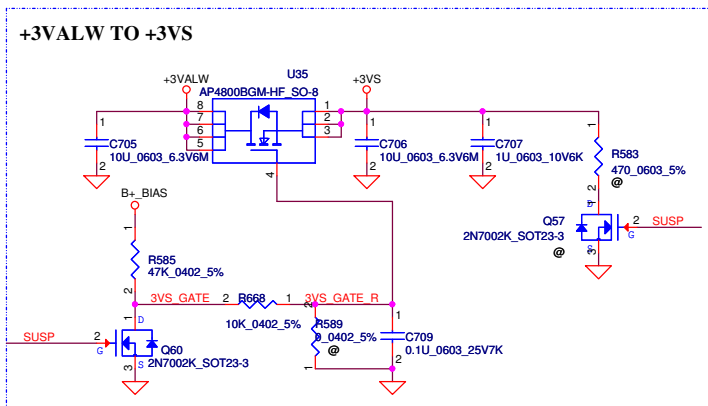
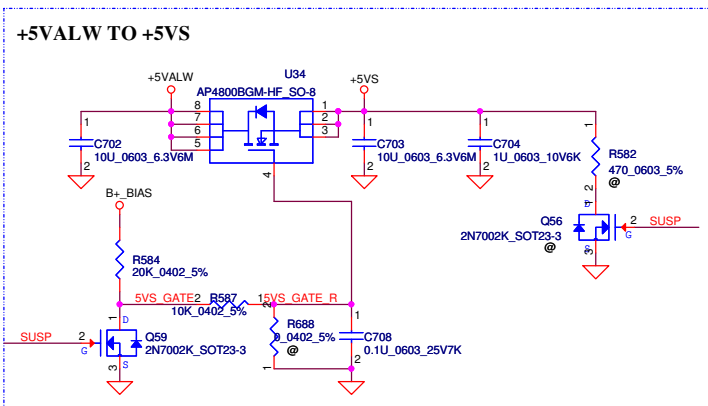
**FOR EC 128KB SPI ROM
(150mil PACKAGE)
SA00003FL10
SA00003JD00**



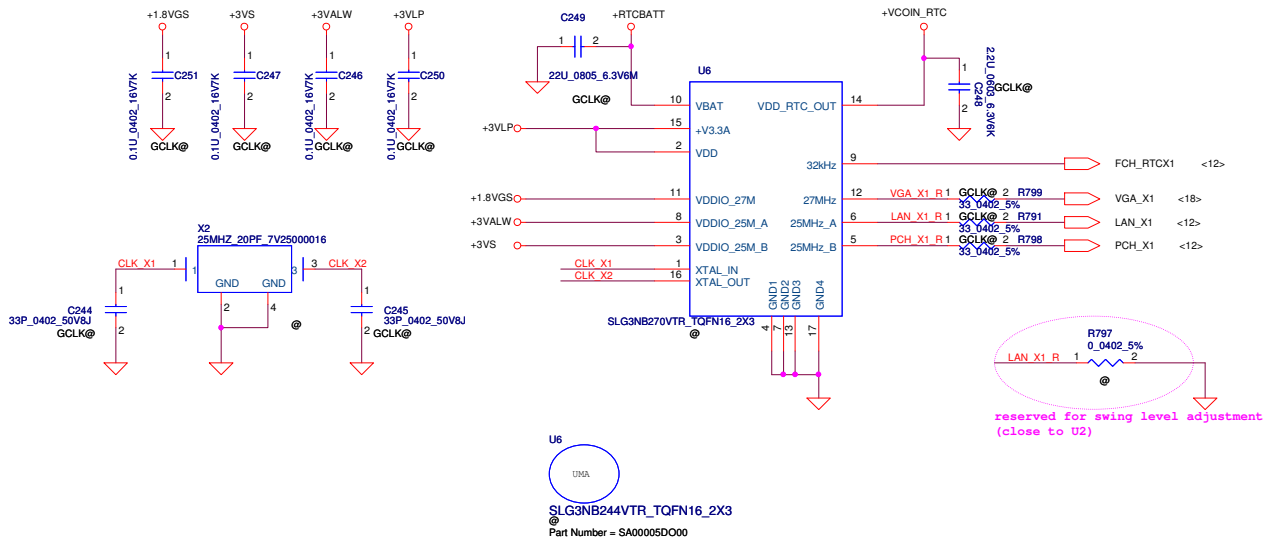
LID SWITCH FOR INS. ONLY



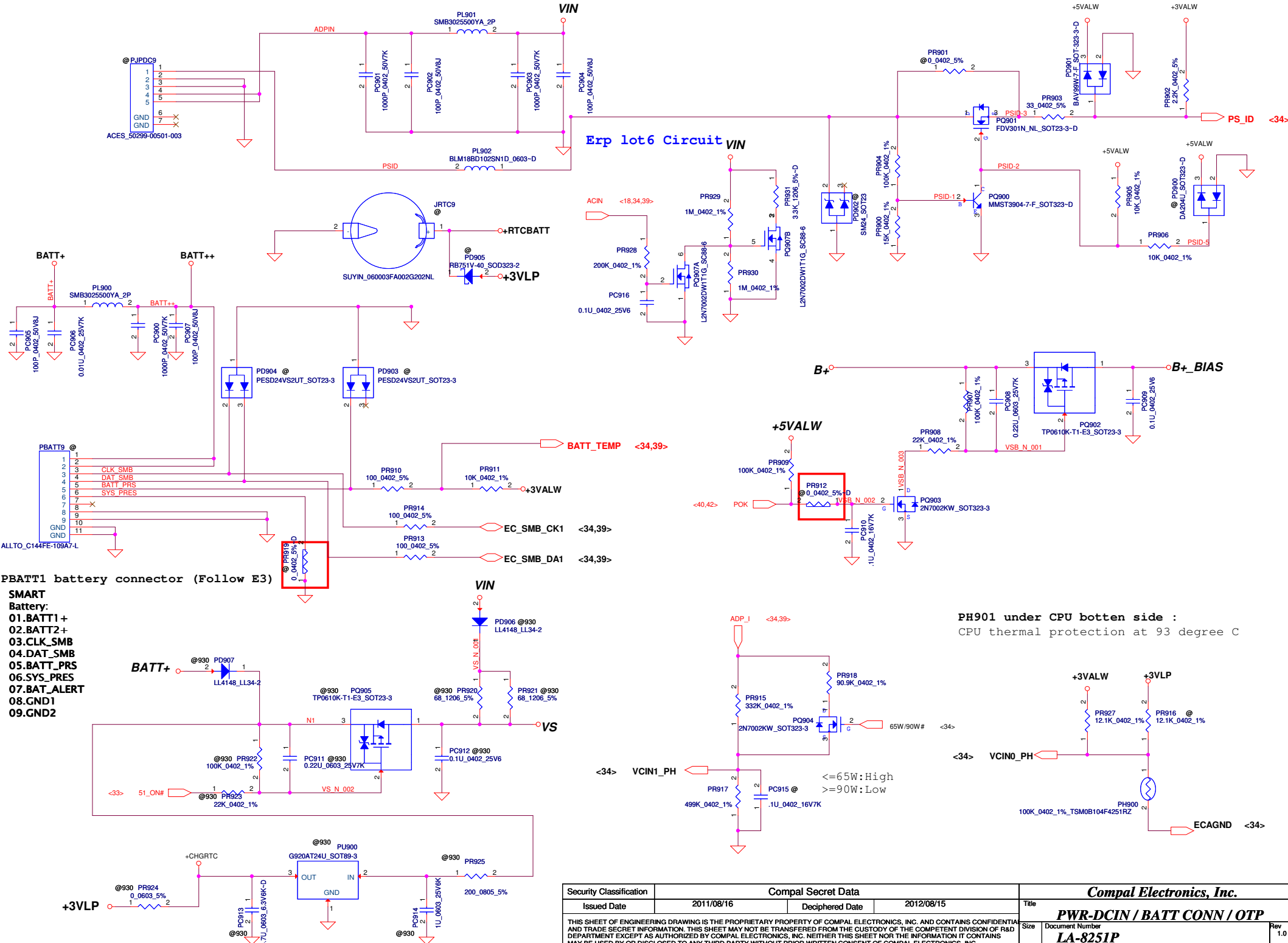
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Issued Date	2011/08/01	Deciphered Date	2013/01/01	Title EC ROM/Debug	
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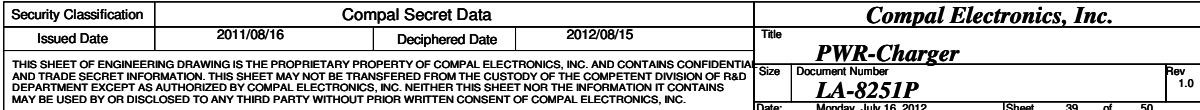
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Issued Date		2011/08/01	Deciphered Date	2013/01/01		Title						
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						C	I	D	E	F	G	H

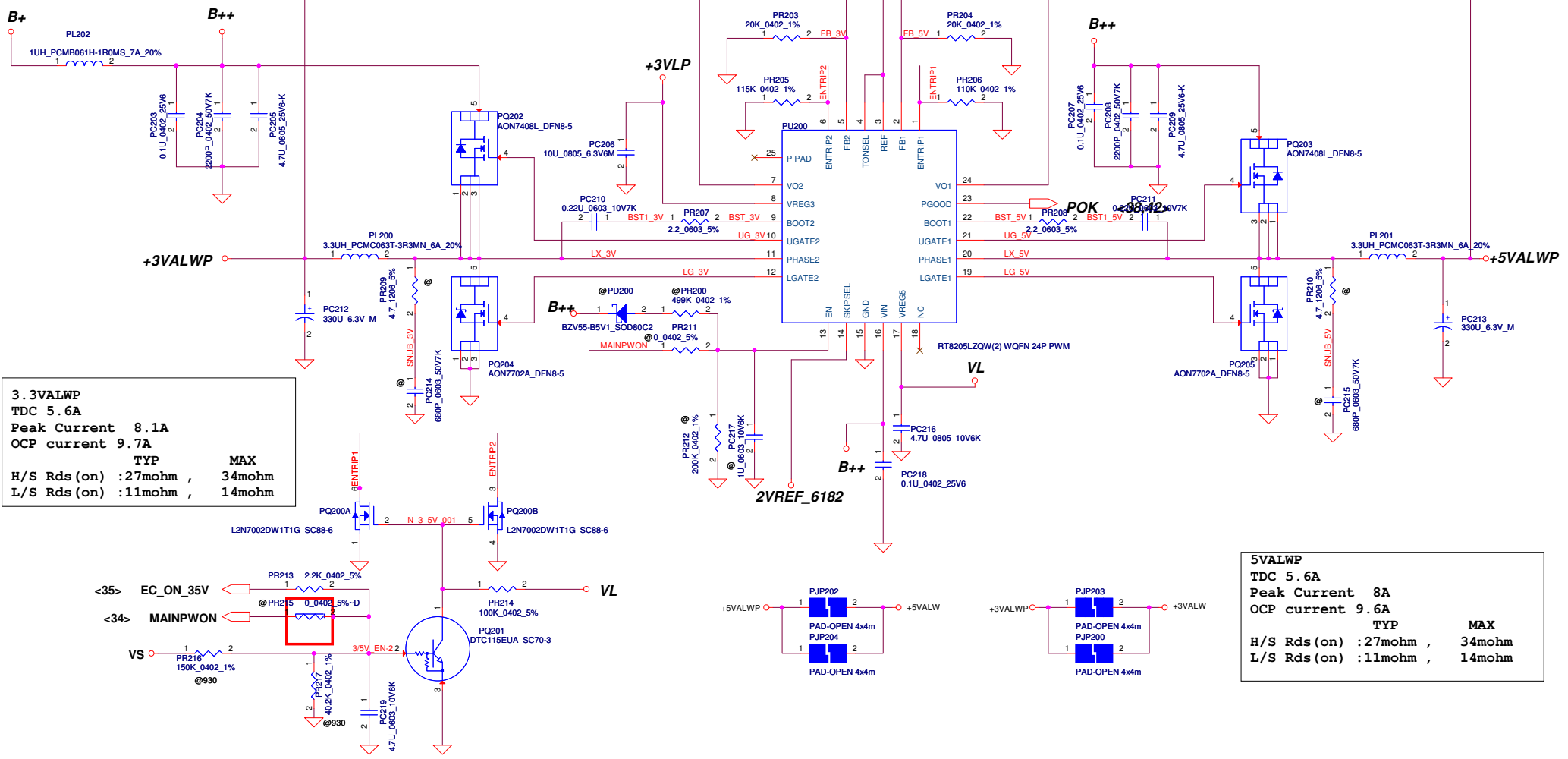


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Issued Date	2011/08/16	Deciphered Date	2012/08/15	Title	PWR-DCIN / BATT CONN / OTP
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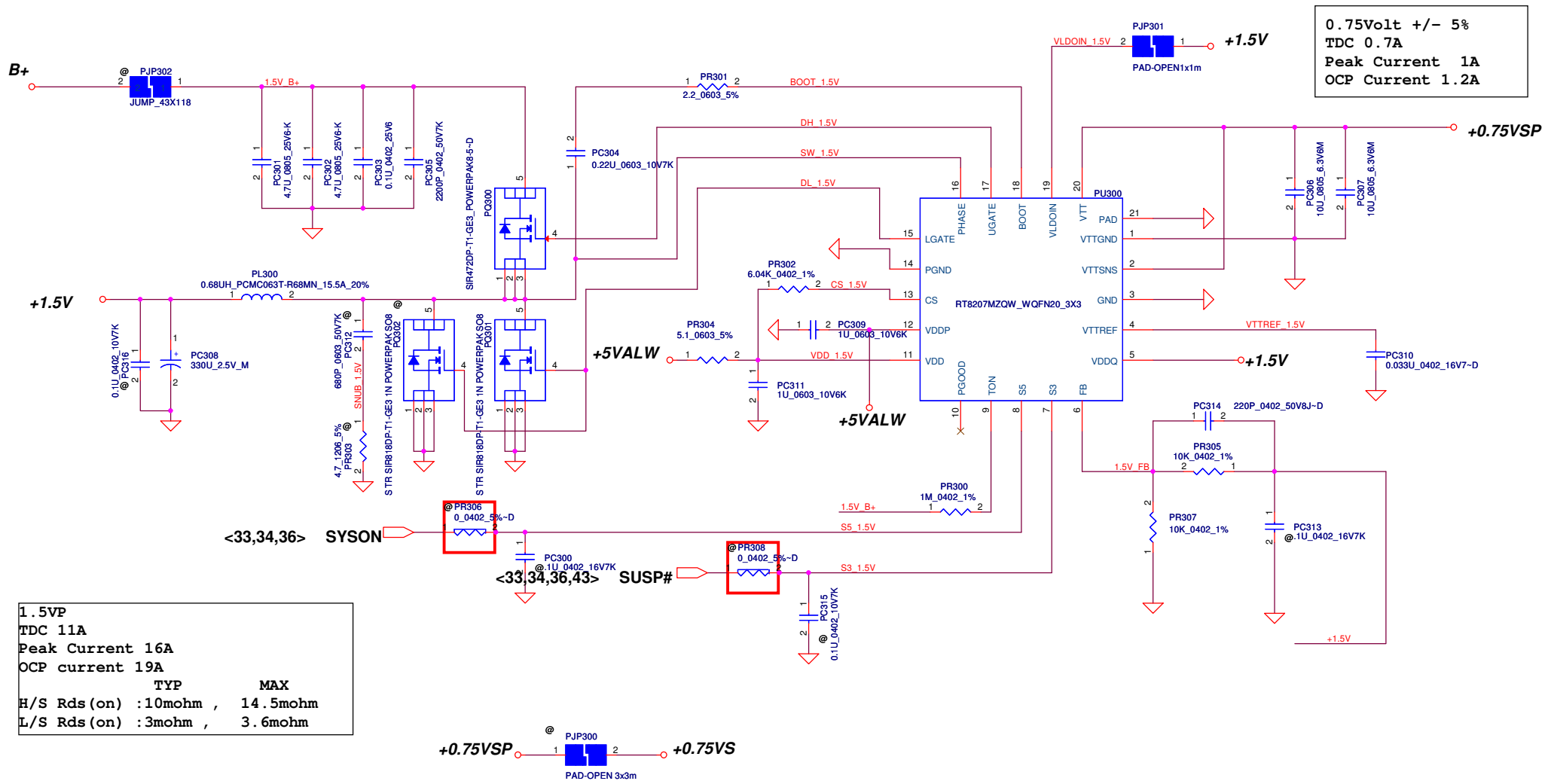


3.3VALWP
 TDC 5.6A
 Peak Current 8.1A
 OCP current 9.7A

	TYP	MAX
H/S Rds (on)	:27mohm	34mohm
L/S Rds (on)	:11mohm	14mohm

5VALWP
 TDC 5.6A
 Peak Current 8A
 OCP current 9.6A

	TYP	MAX
H/S Rds (on)	:27mohm	34mohm
L/S Rds (on)	:11mohm	14mohm

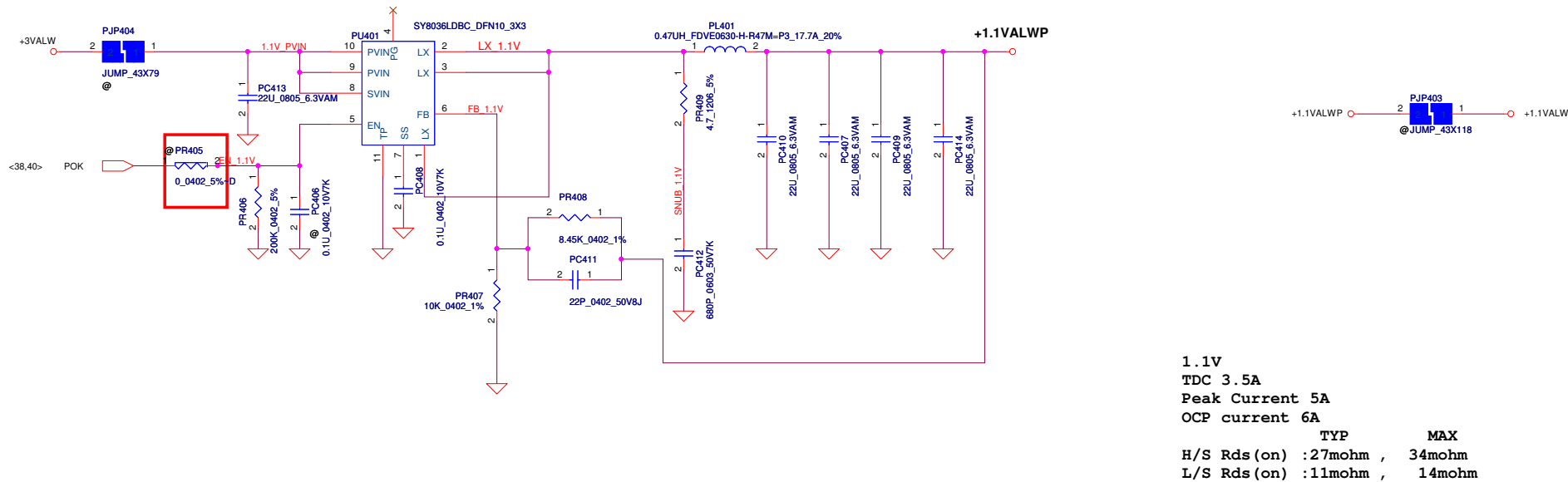
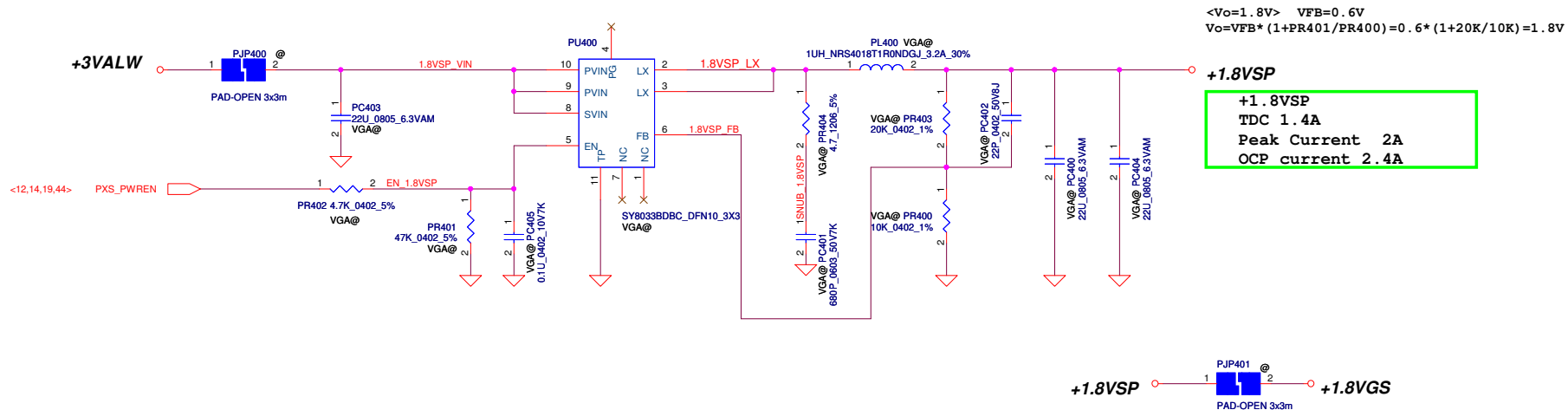


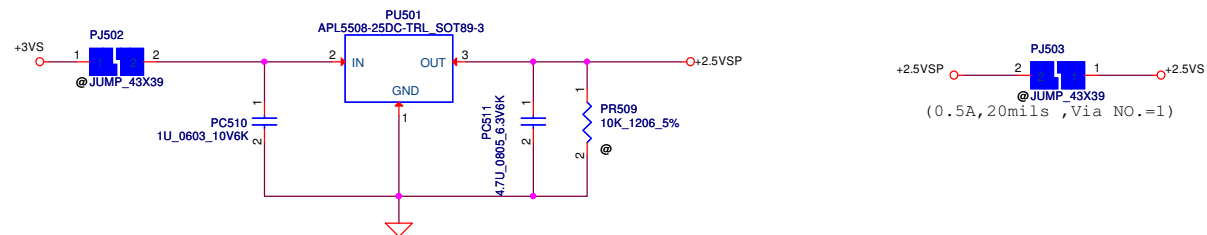
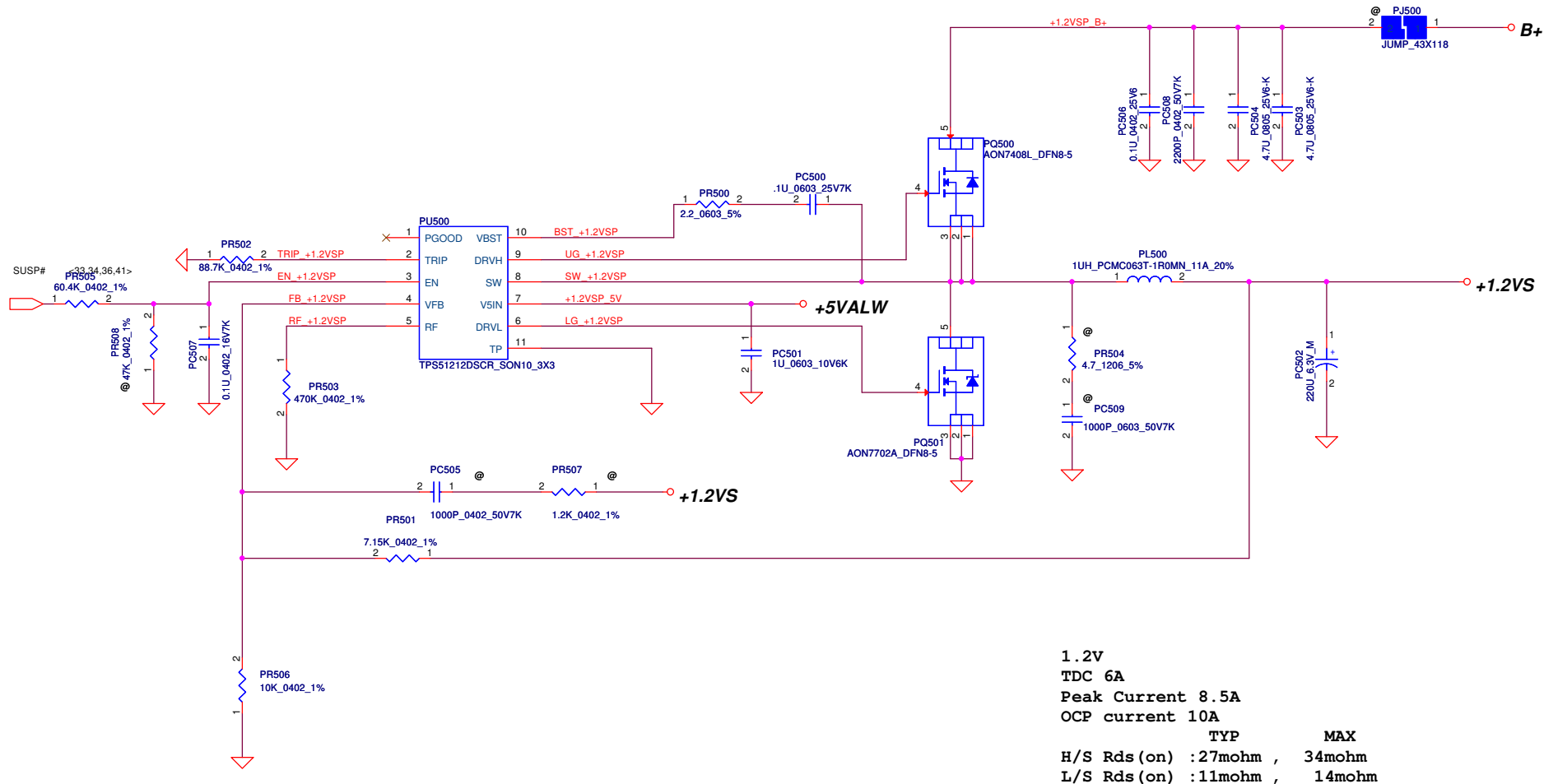
1.5VP
TDC 11A
Peak Current 16A
OCP current 19A

	TYP	MAX
H/S Rds (on)	:10mohm	14.5mohm
L/S Rds (on)	:3mohm	3.6mohm

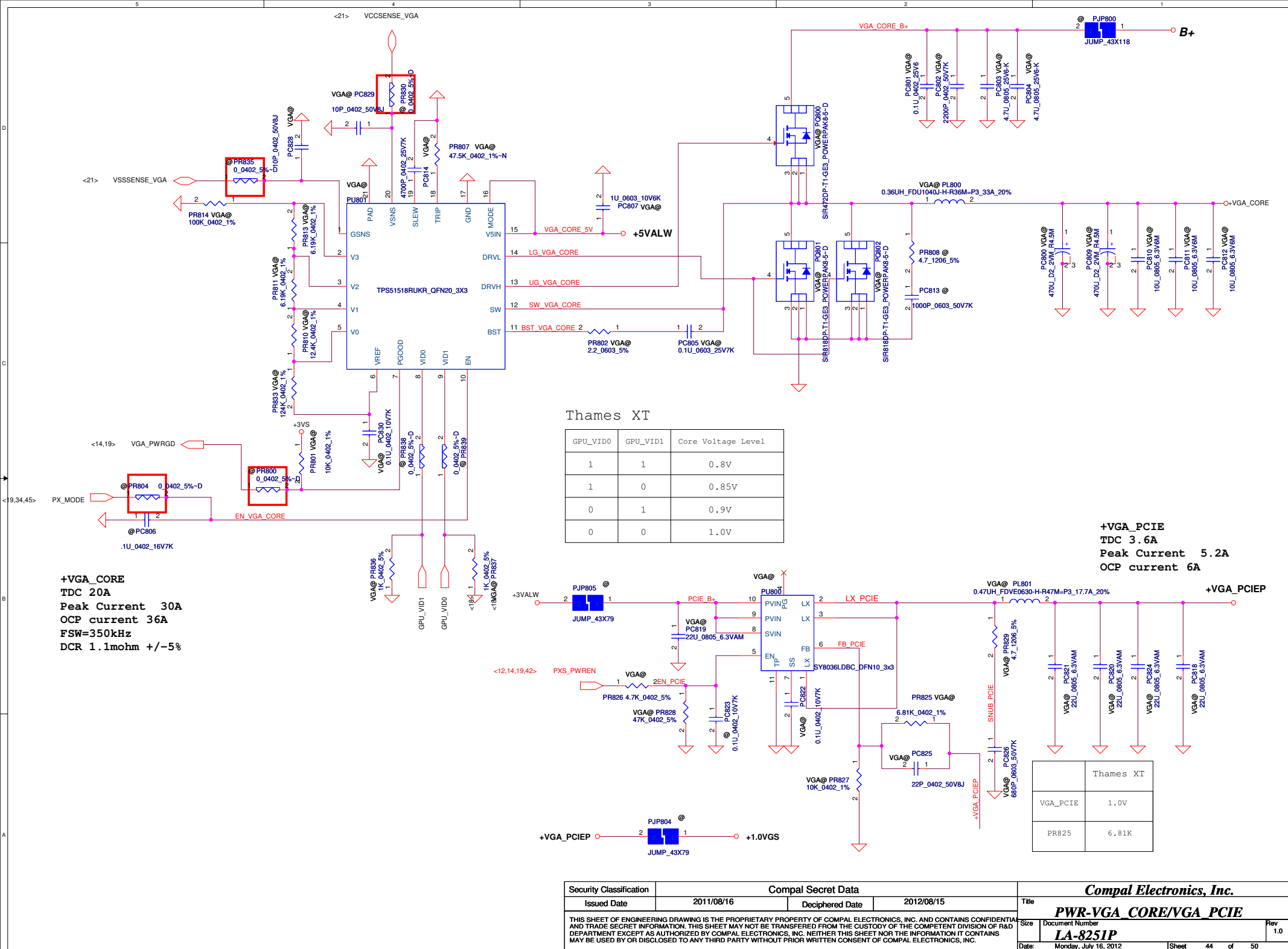
0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

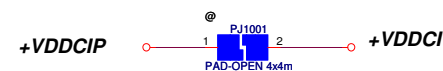
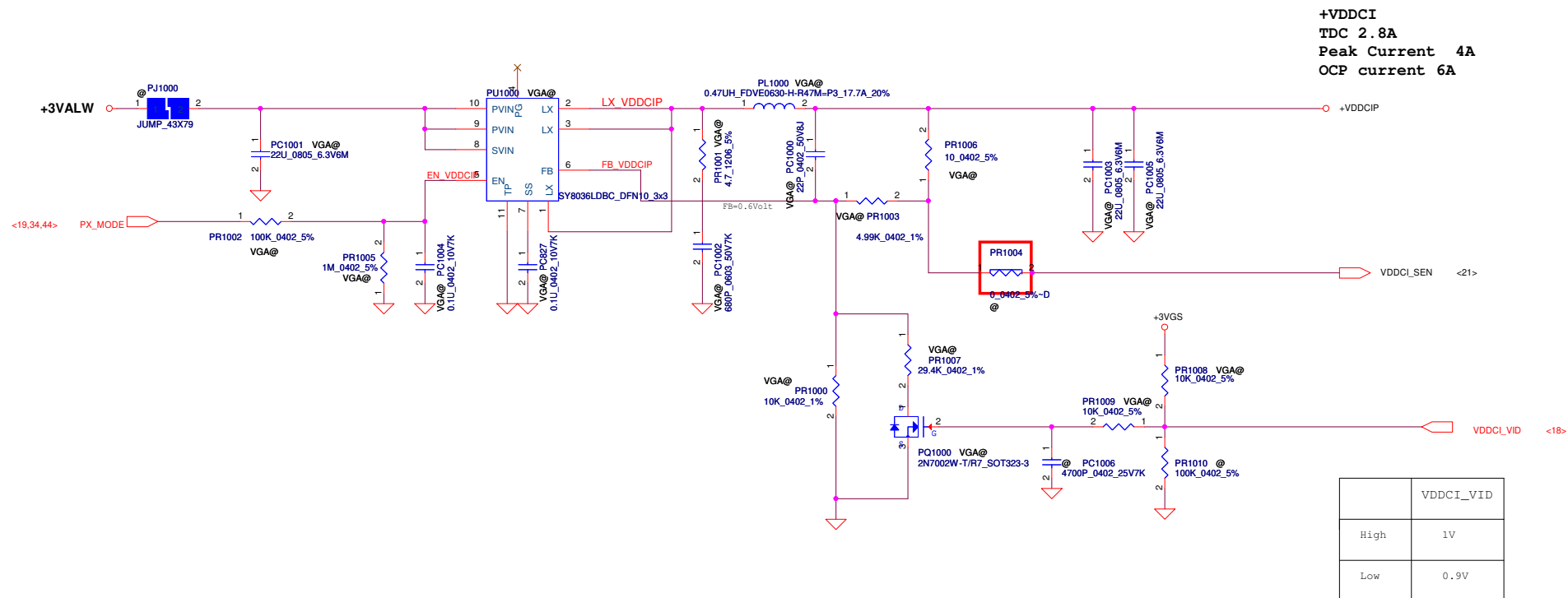
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Issued Date	2011/08/04	Deciphered Date	2012/08/03	Title	PWR-1.5V/0.75VSP
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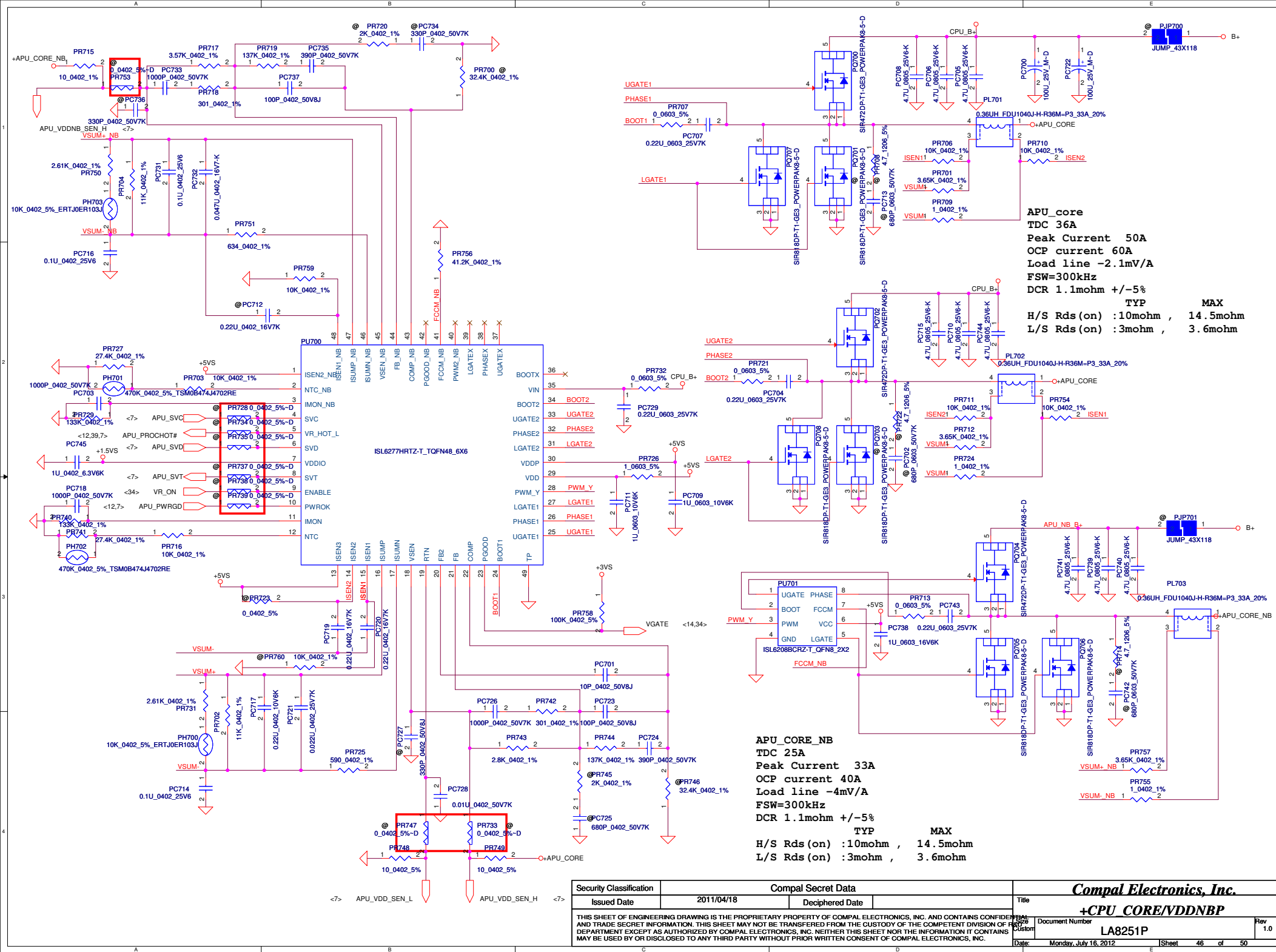




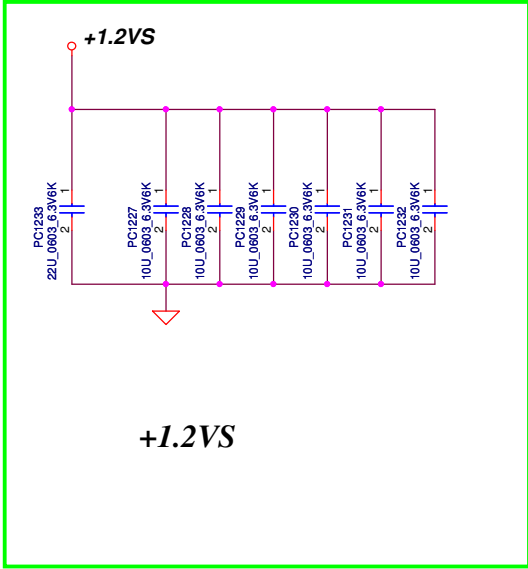
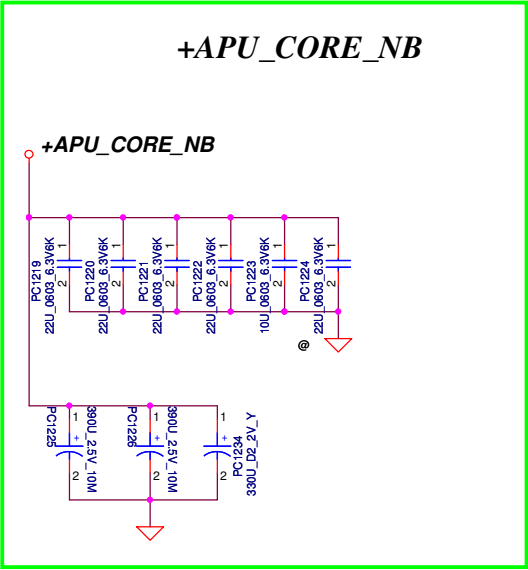
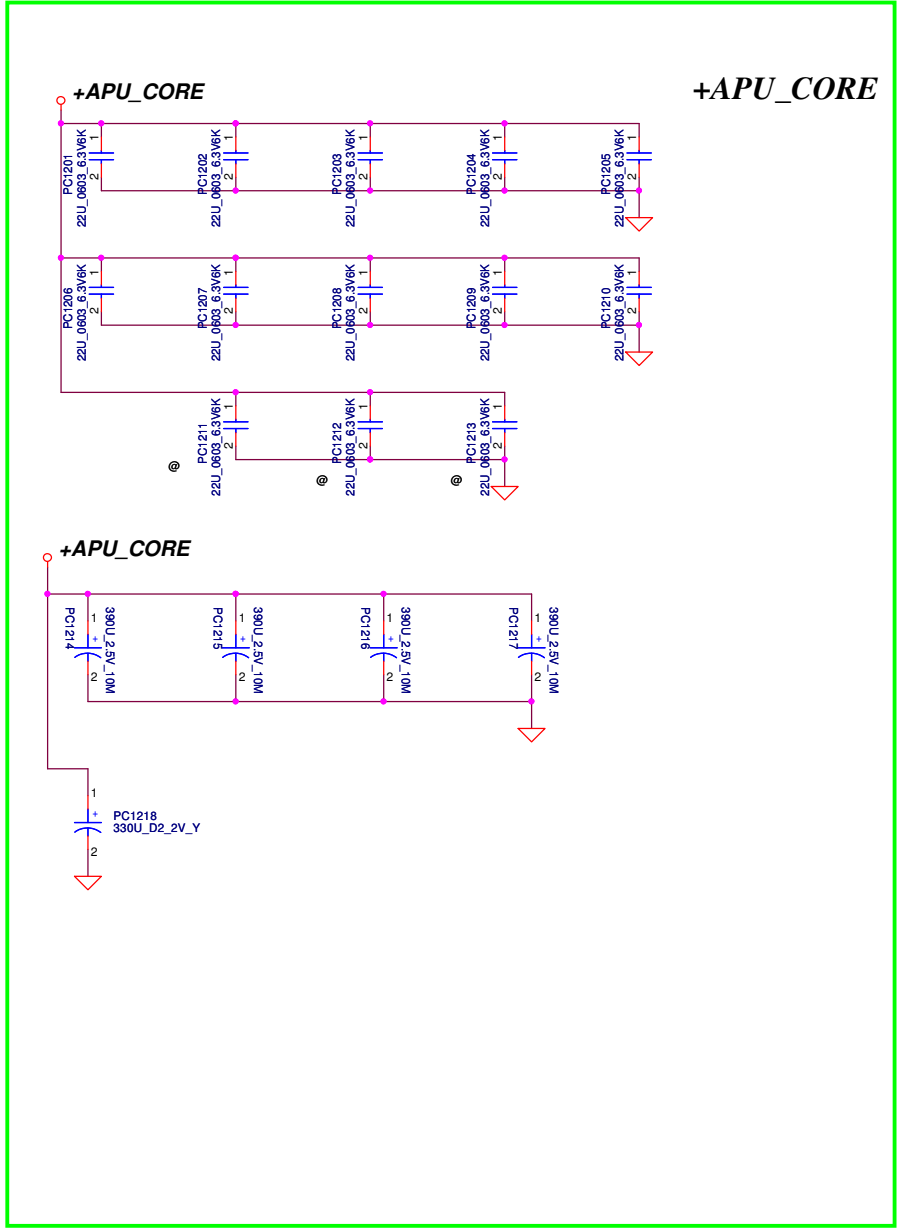
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				Size	Document Number
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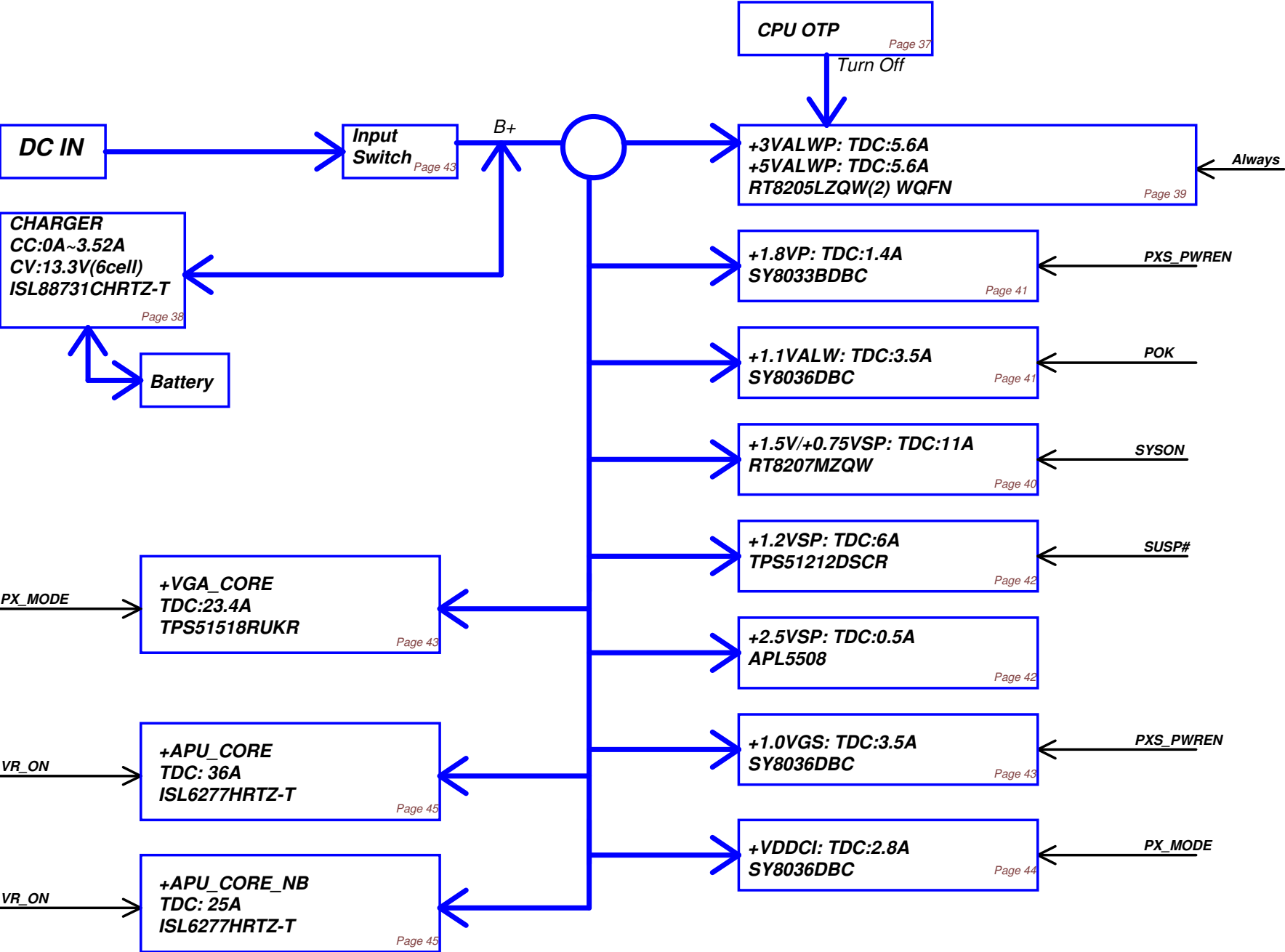


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Power block



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Version Change List (P. I. R. List)

Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	9	XXXX	XX*XX/XX	Compal_XX	XXXXXX	Change XXXX from Xohm to XXXohm.	X01

Design Change				
Date	Page	Part reference	change description	Reason
10/17/2011	33	JLED2	Add JLED2 for Inspiron use only.	ME change drawing.
10/17/2011	30	UD1	Swap nets FCH_SDATA0/FCH_SCLK0	correct connection
10/17/2011	25	LV27.1	ADD RV327 for HPD	Vendor review
10/17/2011	25	RV268	DEL RV268	No need 1.2V from system.
10/17/2011	14	D6.D7	Change D6, D7 to Schottky for VGA PWR control	Original Diode, Vf too high.
10/17/2011	12	C159,C158	Change C159,C158 to 10pF	Vendor review
10/17/2011	12	D5,D8	Change D5, D8 to Schottky	Original Diode, Vf too high. Vendor review.
10/17/2011	27	DV8	Reserve DV8, use RV40 short.	HDMI Voltage issue.
10/17/2011	26	JLVDS	JLVDS Reverse Pin	LVDS connector location change.
10/17/2011	21	RV215	RV215 connect to net:+VDDCI	FB_VDDCI Should connect to +VDDCI
10/17/2011	37	AMP	Add an Audio AMP Circuit in page37	customer requires.
10/19/2011	33	DB7	Reserve DB7 for ESD	ESD request
10/19/2011	35	RB21	Adding RB21, change USB charge circuit power rail to +VCC	USB charge sequence fine tune
10/19/2011	34	U26	Dashboard button change to U26 pin34,36,75	to meet customer spec.
10/19/2011	13	U2	KB_DET# Change to FCH GPIO56, add Q76	EC pin saving.
10/20/2011	34	R503	DEL R503	Leakage form 3VALW to VS
10/20/2011	30	QD4	Add QD4	Leakage form 3VALW to VS
10/21/2011	33	R793,R794,R795,R796,D24	add R793,R794,R795 100K*3,R796 0ohm,D24 BAT54C	For Dashboard support 3 second boot up.
10/21/2011	37	U6	Reserve U6, C244~C251, R797~R799	Reserve GreenCLK
10/21/2011	31	JBTB1	change pin67 to +3VS, pin36,38,40,42 to +3VALW	LAN D/B design changes.
10/21/2011	27,32	JUSB2,JHDMI	update JUSB2 Footprint, JHDMI Footprint	ME change drawing.
10/25/2011	29	CA19,CA20	From 2.2uF to 4.7uF	Vendor review
10/25/2011	28	CV6, CV7, CV8	From 22pF to 10pF	CRT high resolution issue.
10/26/2011	33	R60,R8	Change to 300ohm	LED current need >5mA
10/26/2011	33	R792	Add 100Kohm to GND	Power LED issue.
10/26/2011	33	UX1	SYSON connect to UX1,20	Express Card not support S5 weakup.
10/28/2011	29	RA12,RA13	Change from 5.1ohm to 39.2ohm	Vendor review
11/21/2011	33	UX1	Connect pin1 to +3VS, pin14 to +1.5VS for 2nd GMT	2nd source required.
11/28/2011	7	Q6	Add Q6, Del Q1	ProcHot# change to High active. Common code for EC
11/28/2011	12	R109	10M reserved	Without RTC battery, system should not boot up issue
11/28/2011	36	EMI	Add C254,C255,C256,C257,C258,C259 0.1uF +1.5V	For EMI request
11/28/2011	32	UB4	AMD USB debug Port0 change to JUSB1	JUSB1 USB SI too margin. Due to switch serial resistor approx 10ohm

Design Change for PT				
Date	Page	Part reference	change description	Reason
04/03/12	18	YV1	27MHz package change to small size	Sourcer's recommend for cost down
04/03/12	26	JLVDS	pin assignment change for 31,32,33,34,35,37	Sourcer's recommend for cost down
04/03/12	35	C657	add 0.1u_0402 on USB_DETECT#	ESD required
04/03/12	35	C658	add 0.1u_0402 on USB_DET#_DELAY	ESD required
04/03/12	18	RV205, RV206	add 10K_0402 reserved only.	AMD Chelsea required
04/03/12	18	R804, R805	add 0_0402 reserved only.	AMD Chelsea required
04/03/12	20	RV244, CV366, RV208	add 2K_0402, 10P_0402, 0_0402, reserved	AMD Chelsea required
04/03/12	21	RV247, RV248	add 0_0402 reserved, RV247 stuffed.	AMD Chelsea required
04/03/12	18	RV250	add 0_0402 to GND for Thames, stuffed.	AMD Chelsea required
04/03/12	28	JCRT	footprint changed	DFB required
04/03/12	30	JHDD	footprint changed	DFB required
04/03/12	12	C158,C159,Y1	18p,18p,small size, 10P→18P	Sourcer's recommend for cost down
04/03/12	12	C155,C157,X1	12p,12p,small size, 27P→12P	Sourcer's recommend for cost down
04/12/12	19	RV104,RV101,QV21,CV96,RV103,RV109,QV25,RV99,RV100,QV18,QV19,QV20	Remove from BOM	These parts are PX4.0 supports. We support PX5.0 only.
04/12/12	19	RV112,RV113	RV113 Change 150K→240K, RV112 change 20K→240K.	Power rail +1.5VGS Timing fine tune.
04/12/12	18	R807,R806	Reserve 0ohm, R807 stuffed.	Reserve adaptor choice for dGPU
04/12/12	29	R14, Q78	R14 10K, Q78 NMOS dual.	GPIO5(net:AC_BATT)
04/12/12	32	LB6, RB17, RB19	LB6 add to BOM.	AMD recommend.
04/12/12	13	R136	100K ohm stuffed.	EMI required.
04/12/12	14	R104	Reserve 0ohm.	Add PU for FCH GPIO171. (net:ODD_EN#)
04/12/12	33	C260, C261, C262, C263	0.1uF stuffed.	Reserve for ODD_DA#
04/10/12	8	C100	Change to SGA00002280	ESD required
04/11/12	27	CV365, CV367	add 0.1U_0402_10V7K~D, reserve only.	ME Height limit. 4mm.
04/12/12	33	L3	add DLW21SN900SQ2_0805~D, reserve only.	EMI required, add caps in HDMI DDC
05/02/12	7	C71	pop 0.1U_0402_16V4Z	EMI required, add CC in Cardreader
				EE required, Shutdown issue, Leason learn from CGs

Design Change for ST				
Date	Page	Part reference	change description	Reason
05/31/12	26,33,33	RV328,R808,R774	add 300_0402_5%~D	AMD required, USB20 D- add RC for device lose
05/31/12	26,33,33	CV368,C155,C795	add 15P_0402_50V8J~D	AMD required, USB20 D- add RC for device lose
05/31/12	18,28	RV220,RV223,RV217,RV226,RV222,RV225,RV221,RV224,RV216,RV227,RV218,RV228,RV219,RV229	delete CRT debug	AMD required, for VGA layout concern.
05/31/12	7	Q6	reverse Q6	EE required
05/31/12	27	RV329,RV330	add 0_0603_5%~D	EMI required, DDC EMI issue.
05/31/12	27	D20	add PESD24VS2UT_SOT23-3~D, reserve only.	ESD required, HDMI plug issue, Leason learn from CGs
06/22/12	18	R806	pop R806 0ohm	Fast Power reduce function
06/23/12	27	RV39, RV41, RV42, RV44, RV53, RV54, RV57, RV58	Remove these part	change to common mode chock
06/24/12	27	LV4, LV5, LV6, LV7	add these KINGCORE WCM-2012HS-900T common mode chock	EMI required for HDMI noise
06/25/12	27	CV351, CV352, CV349, CV350, CV353, CV354, CV355, CV356	add these 3.3pF 50V 0402	EMI required for HDMI noise
06/26/12	27	CV364, CV363, CV360, CV361, CV358, CV357, CV362, CV359	add these 1pF 50V 0402	EMI required for HDMI noise
06/22/12	32	DB4	Remove	USB detect issue

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