

COMPAL CONFIDENTIAL

MODEL NAME : ZAM81
PCB NO : LA-A913P
BOM P/N :
GPIO MAP: 3.1

Huston 15" DSC
Broadwell U

2013-08-20
REV : 0.1 (X00)

@ : Nopop Component
EMC@ : EMI, ESD and RF Component
@EMC@ : EMI, ESD and RF Nopop Component
XDP@ : XDP Component
CONN@ : Connector Component

MB PCB	
Part Number	Description
DAA0887Y088	PCB 13N LA-A913P REV0 MB DSC DOCK 3

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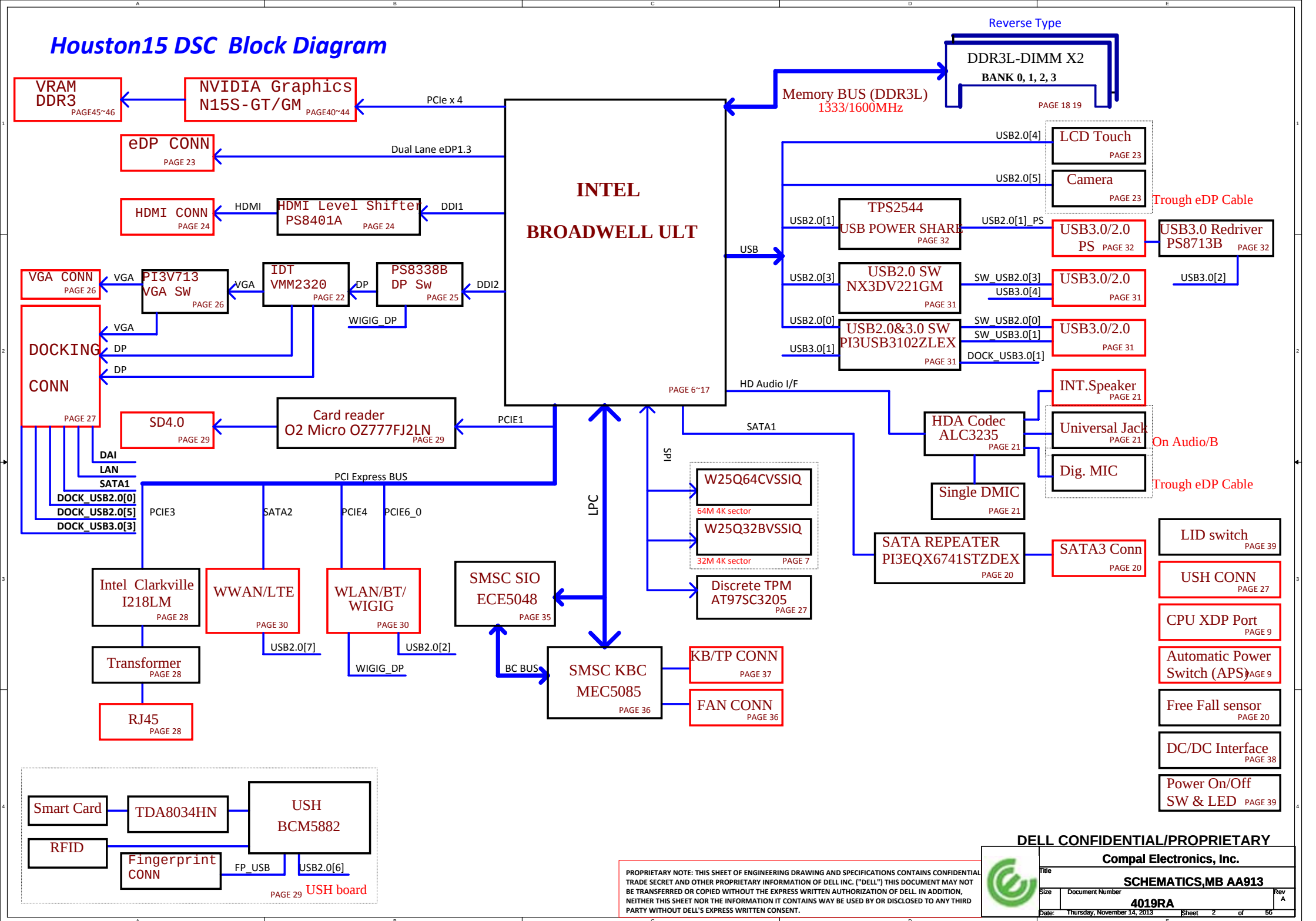
4019RA

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Rev **A**

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Houston15 DSC Block Diagram



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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and
PM Table

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN
PCIE 5			GPU/WIGIG
PCIE 6		SATA 3	WIGI/Express
		SATA 2	mSATA/PCIE
		SATA 1	HDD
		SATA 0	DOCK

BDW ULT	USB PORT#	DESTINATION
	0	JUSB1
	1	JUSB3
	2	WLAN + BT
	3	JUSB2
	4	Touch Screen
	5	CAMERA
	6	USH
	7	WWAN

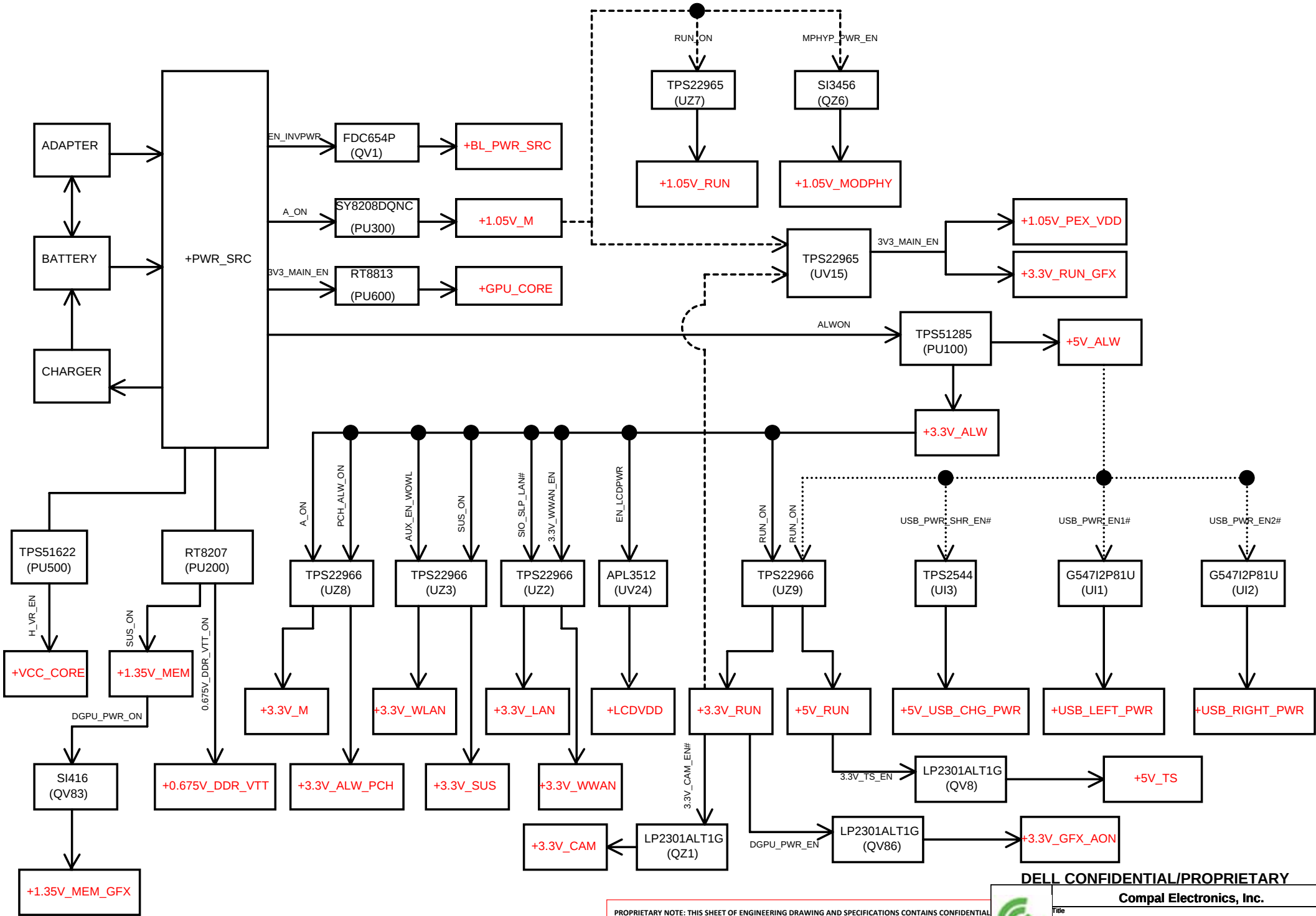
USH	0	BIO
	1	NA

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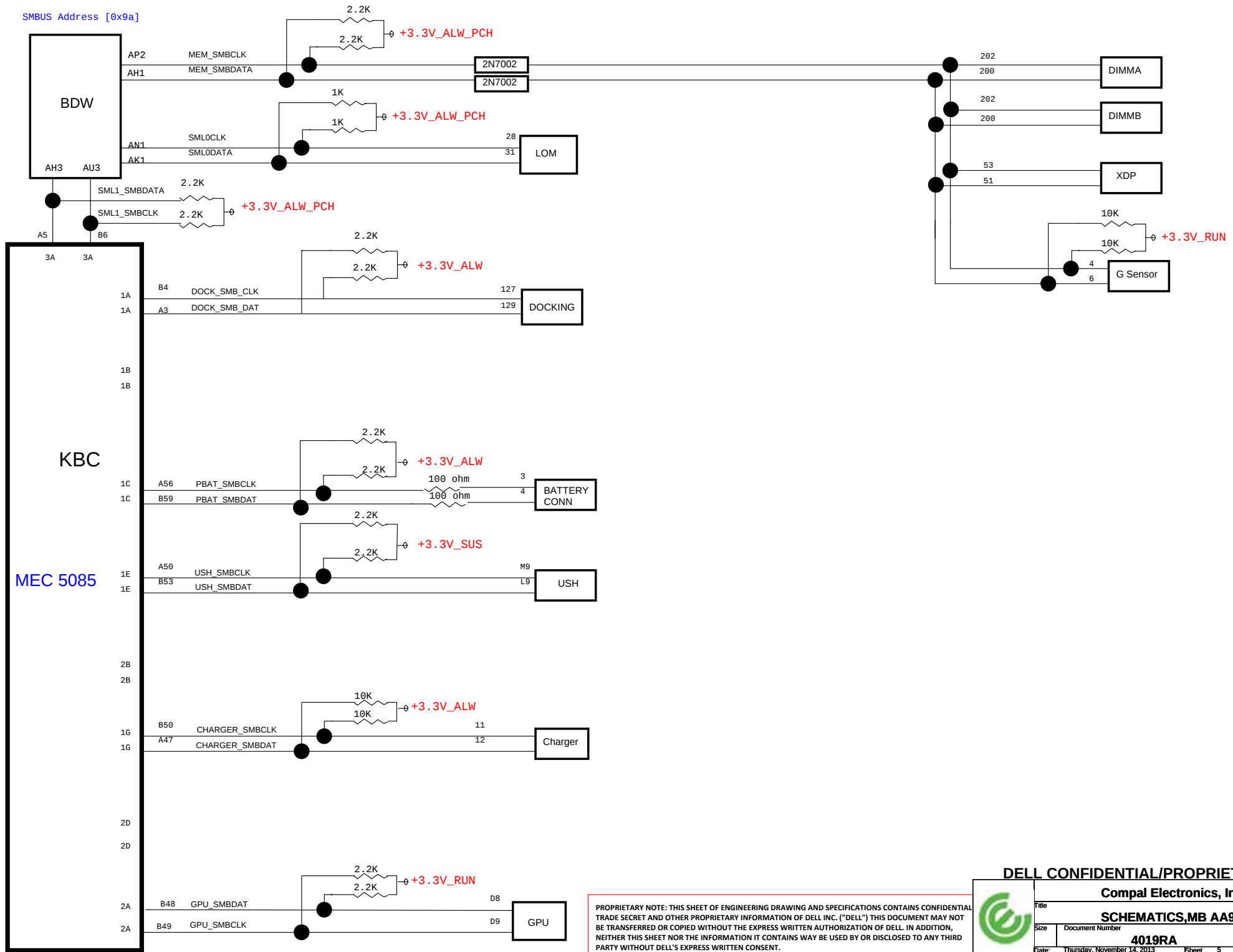


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SMBUS Address [0x9a]



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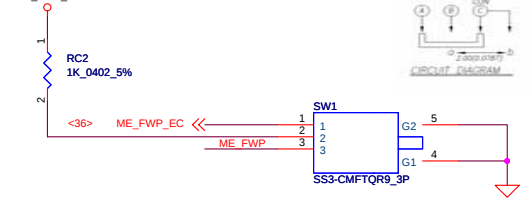
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DSC SATA port

Service Mode Switch:

Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

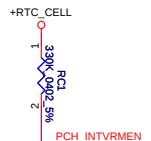
+3.3V_ALW_PCH



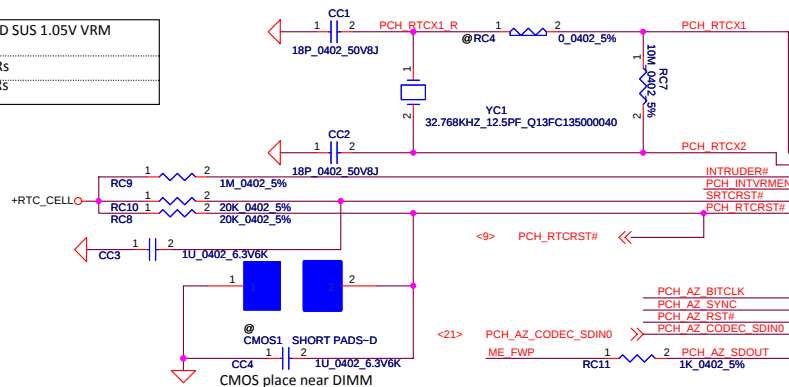
ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE

ME_FWP=LOW → ENABLE ME (DEFAULT) → Pin1 & Pin3 short
=HIGH → DISABLE ME (ME can update) → Pin2 & Pin3 short

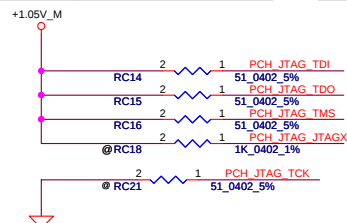


INTVRMEN - INTEGRATED SUS 1.05V VRM
ENABLE
High - Enable Internal VRs
Low - Enable External VRs

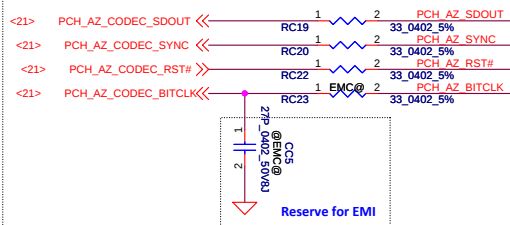


ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS



HDA for Codec



SATA0	SATA1	PCB	SATA2/PCIE6 L1	SATA3/PCIE6 L0
E-Dock	HDD	H12 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	HDD	H12 Entry	NA	NA
E-Dock	HDD	H14 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG
E-Dock	HDD	H14 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	HDD	H14D_En	NA	M2 3030 WIGIG
NA	HDD	H14U_En	NA	NA
E-Dock	HDD	H15 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG
E-Dock	HDD	H15 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	HDD	H15D_En	NA	M2 3030 WIGIG
NA	HDD	H15U_En	NA	Express card

contact to WWAN

SATA2/PCIE6_L1 contact to WWAN
SATA3/PCIE6 L0 contact to WLAN

contact to WWAN

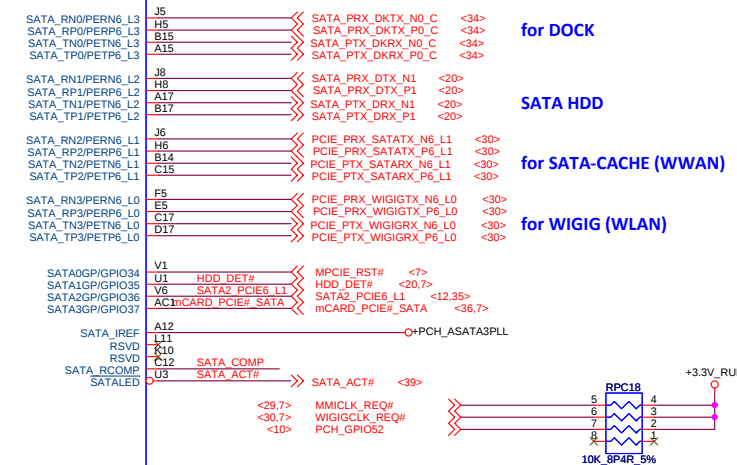
contact to WLAN

SATA2/PCIE6_L1 contact to WWAN
SATA3/PCIE6 L0 contact to WLAN

contact to WWAN

contact to WLAN

contact to Express card



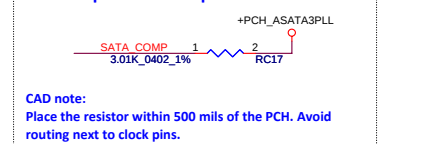
for DOCK

SATA HDD

for SATA-CACHE (WWAN)

for WIGIG (WLAN)

SATA Impedance Compensation

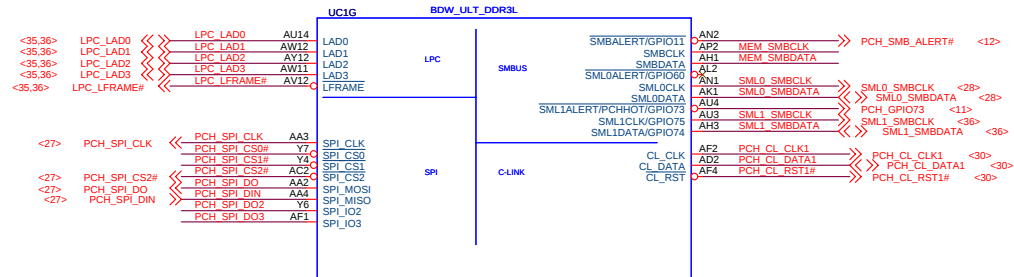


CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

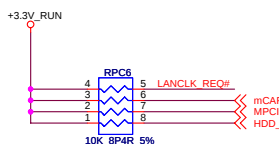
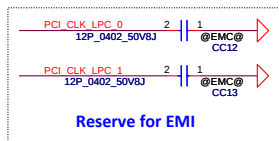
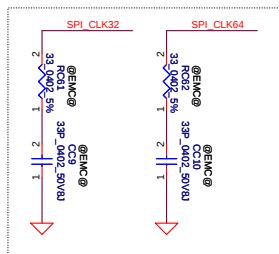
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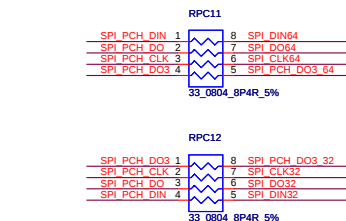
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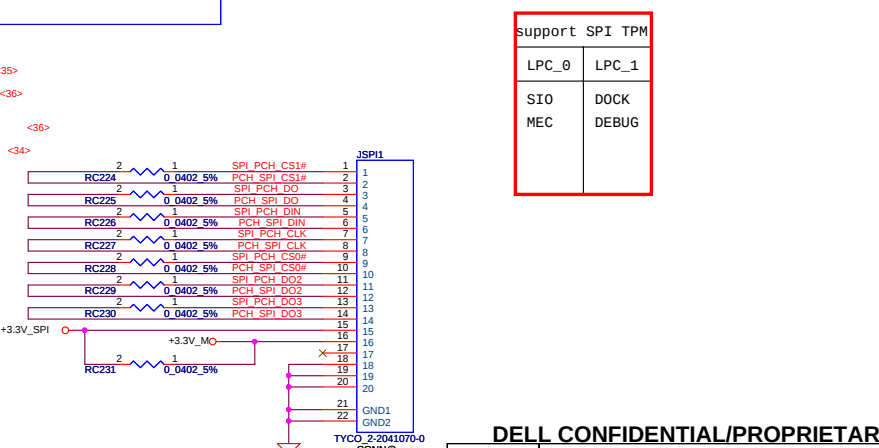
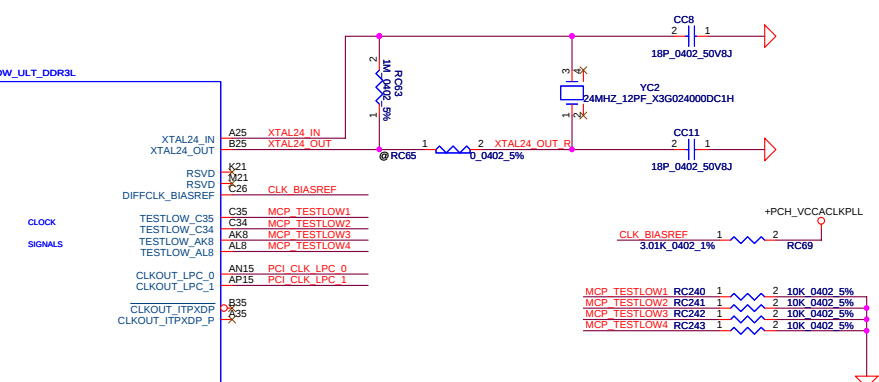
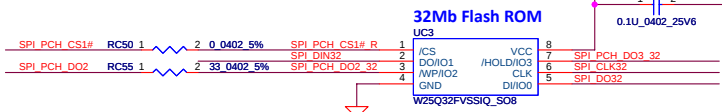
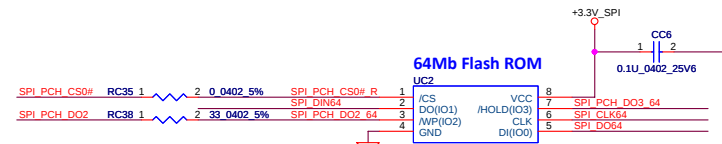
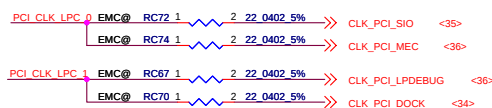
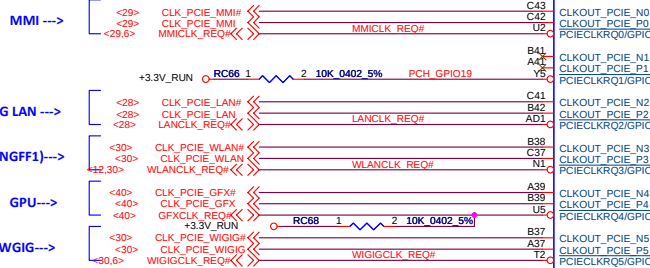
SOFTWARE TAA



PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
H14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H14U_En	SD card	NA	LOM	WLAN	WIGIG	NA
H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	Express card



PCIECLK for DSC

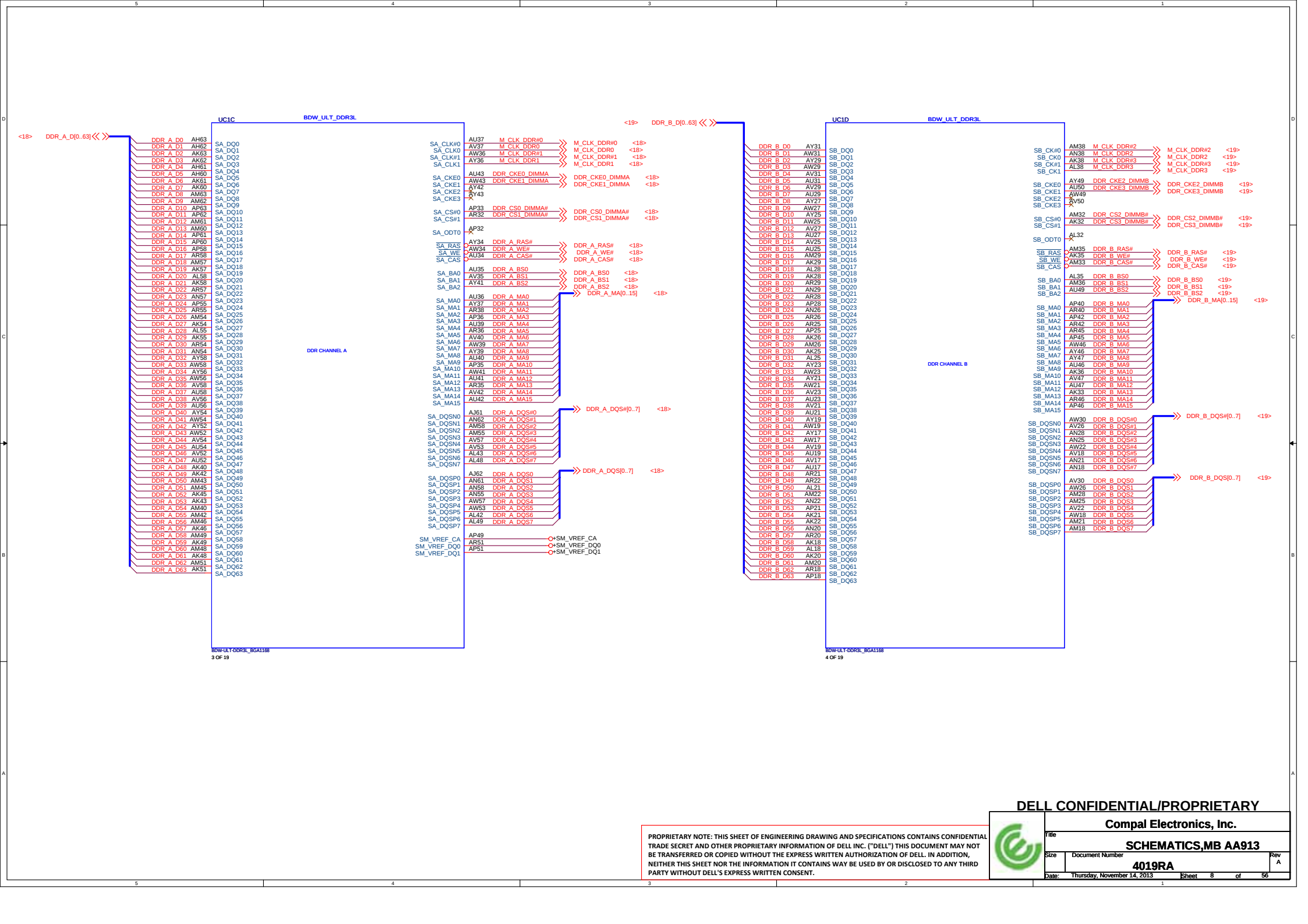


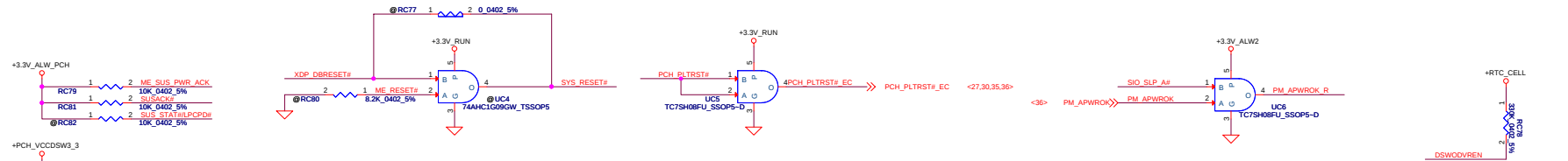
Support SPI TPM	
LPC_0	LPC_1
SI0	DOCK
MEC	DEBUG

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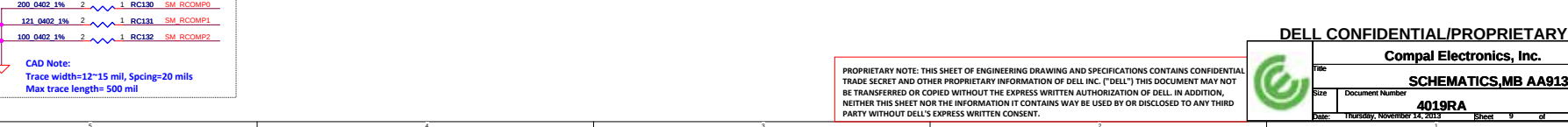
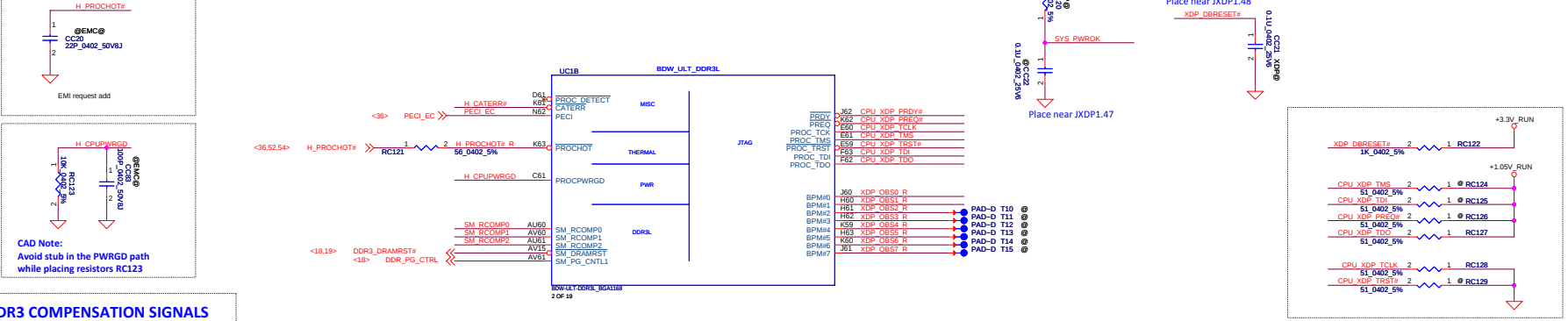
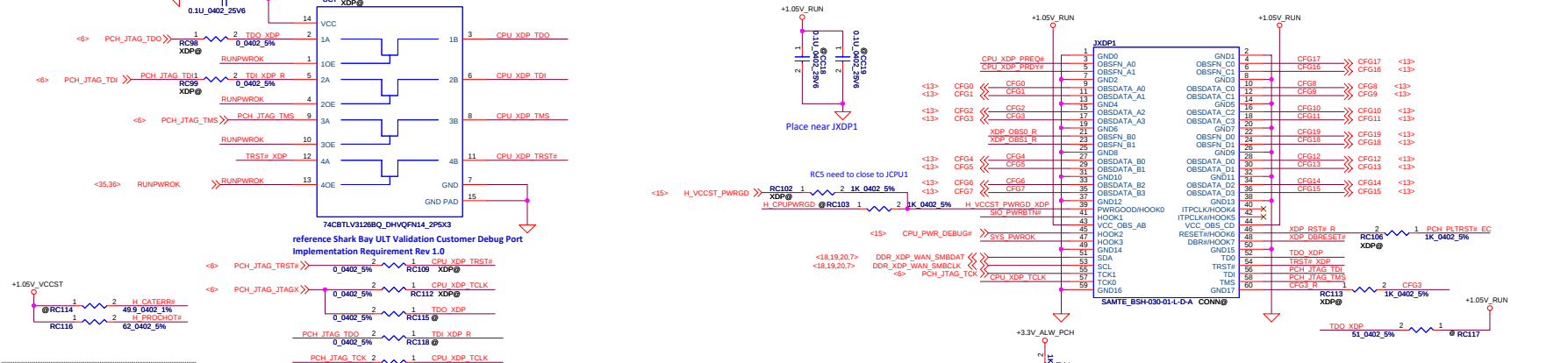
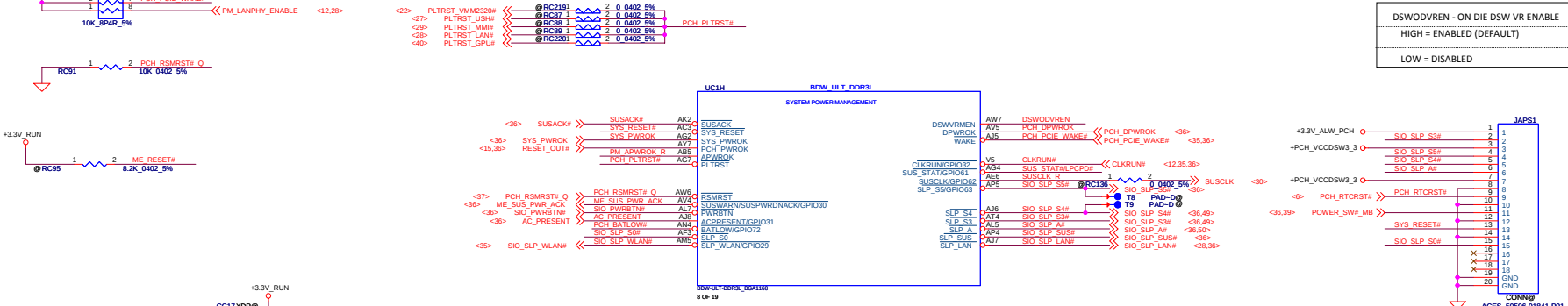
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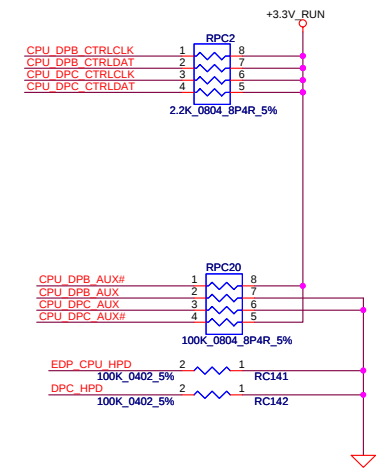
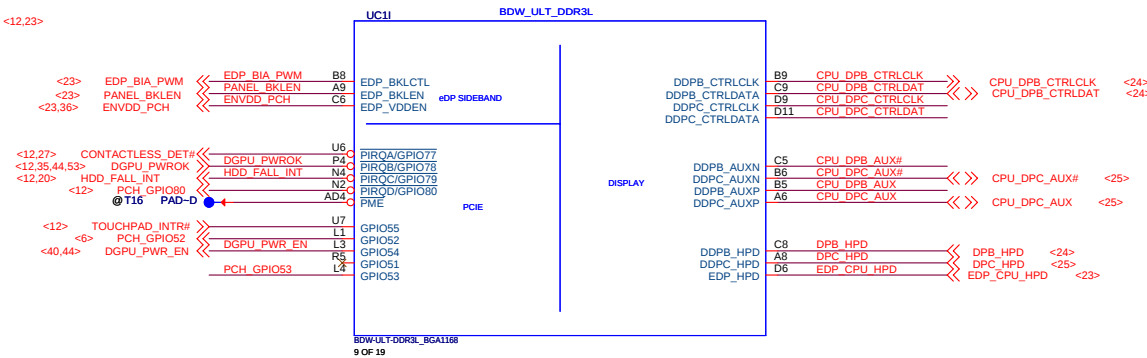
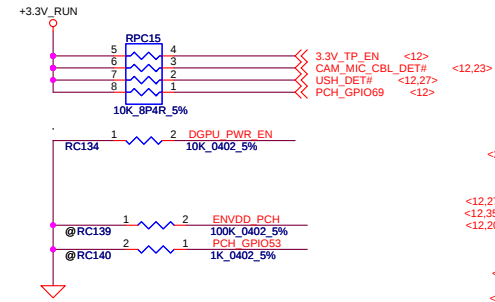
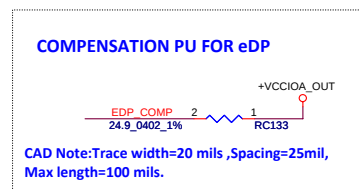
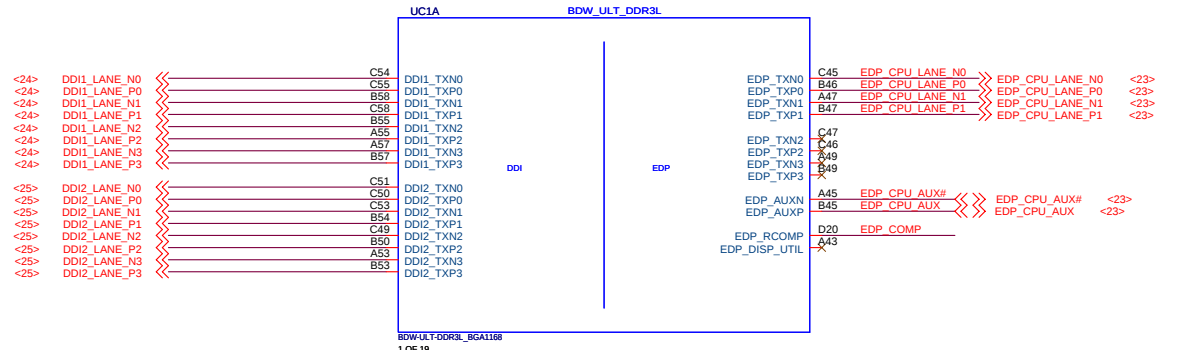
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DSWOODREN - ON THE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED





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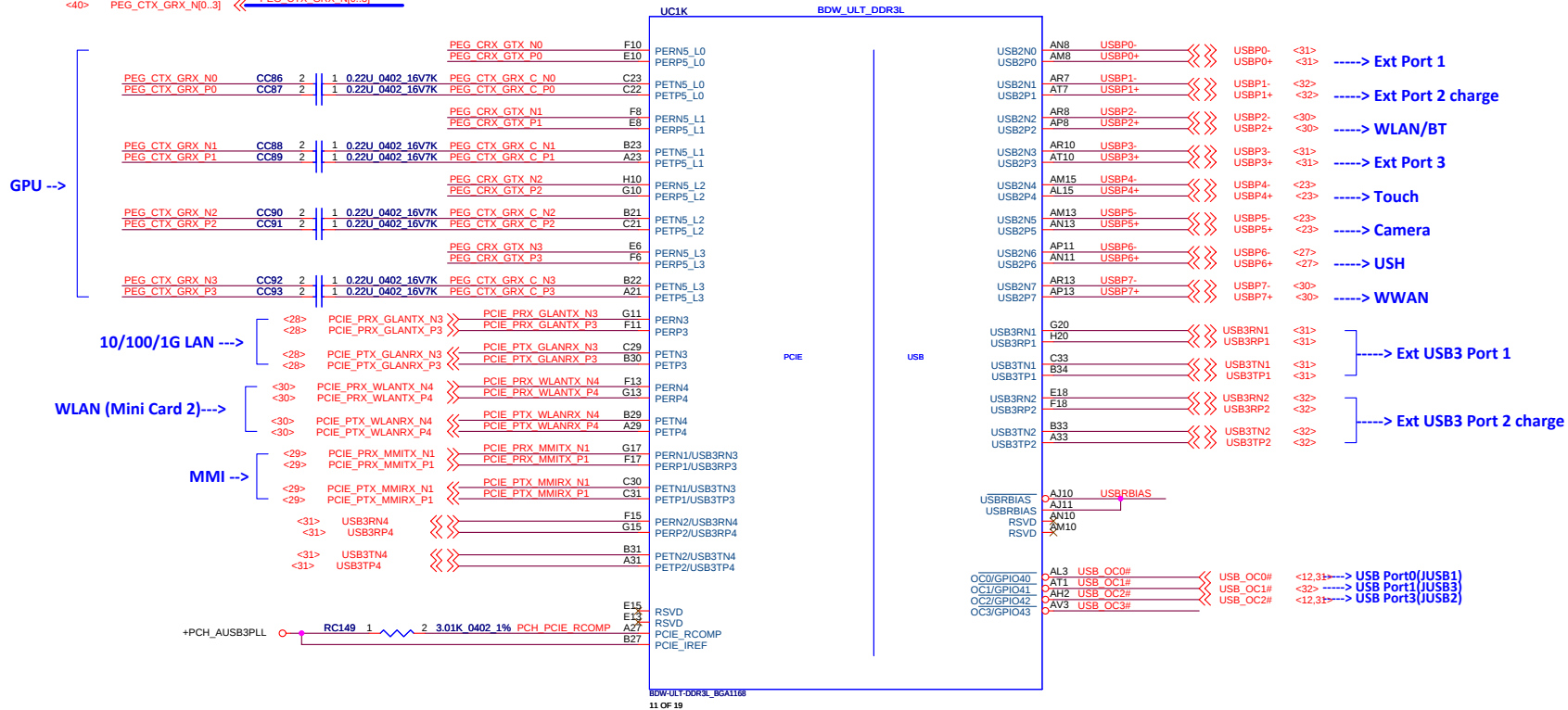
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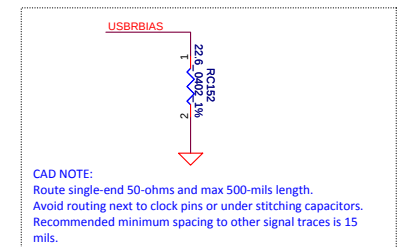
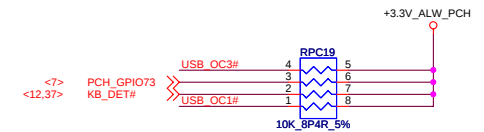
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PCIe for DSC



PCB	USB2	7
H12 UMA	WWAN	
H12 Entry	NA	
H14 DSC	WWAN	
H14 UMA	WWAN	
H14D_En	NA	
H14U_En	NA	
H15 DSC	WWAN	
H15 UMA	WWAN	
H15D_En	NA	
H15U_En	Express	

PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
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H14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H14U_En	SD card	NA	LOM	WLAN	WIGIG	NA
H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	Express card



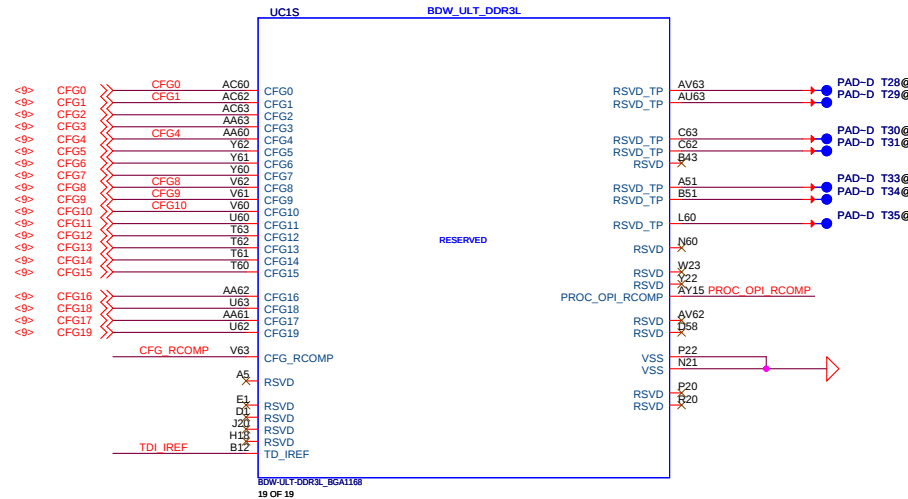
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CFG STRAPS for CPU



EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed

SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0:Disable Noa will be available pegrardless of the locking of the unit

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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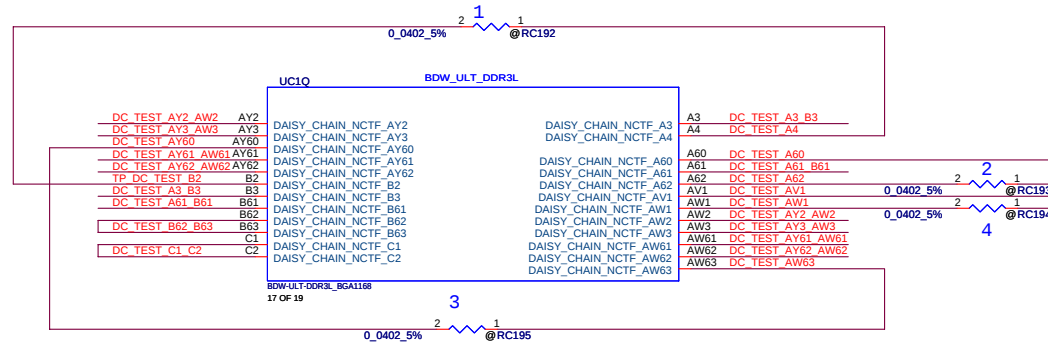
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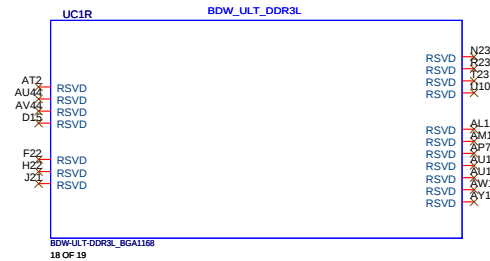
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Package Daisy Chain:

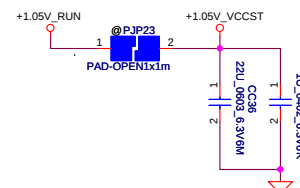
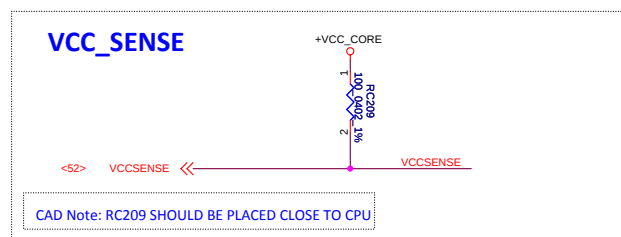
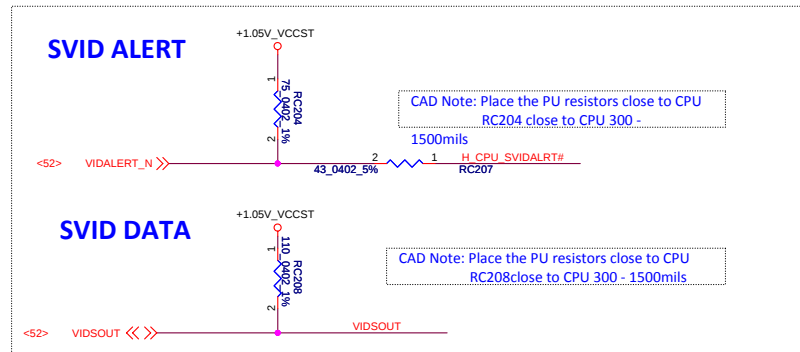
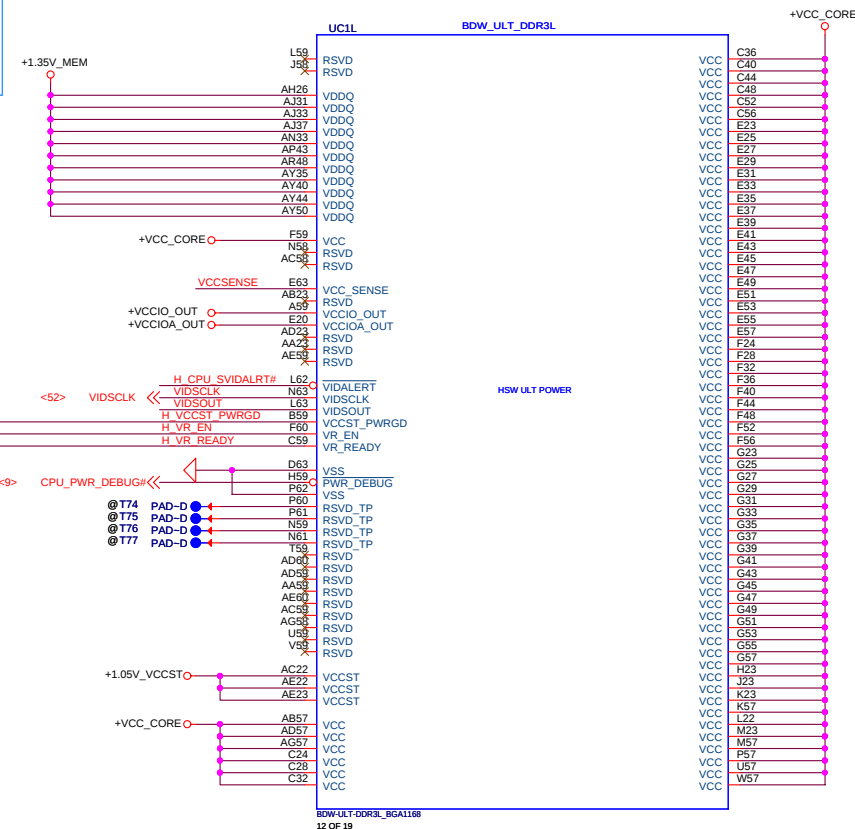
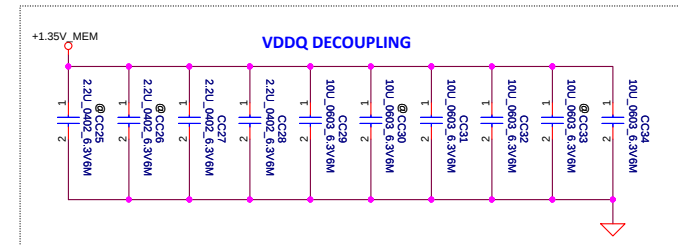
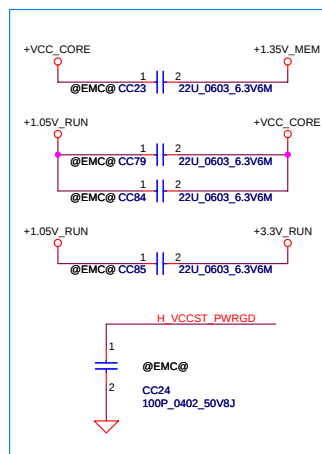
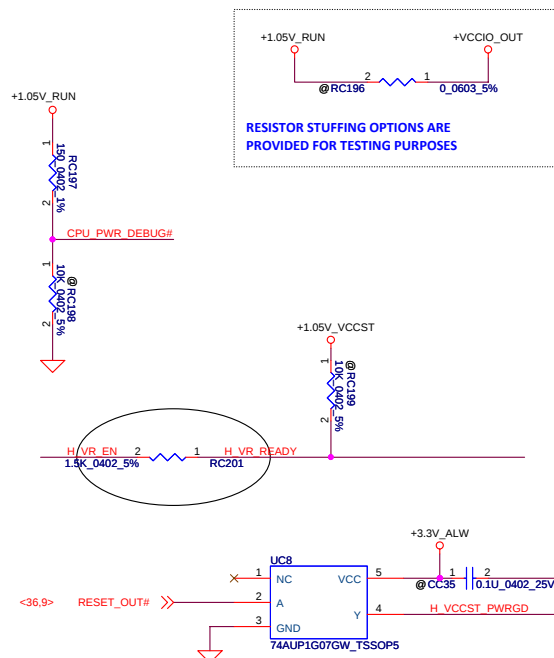
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- 2.A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60
- 3.AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63
- 4.AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1



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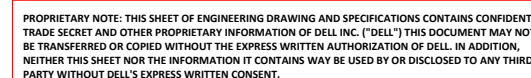


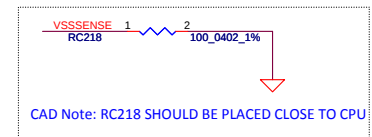
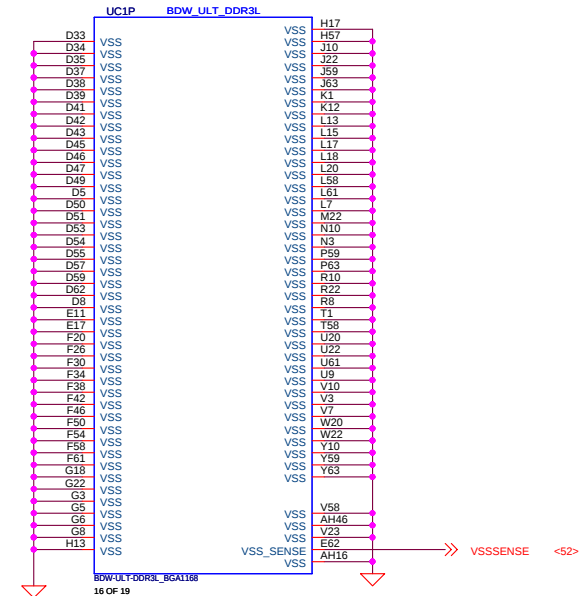
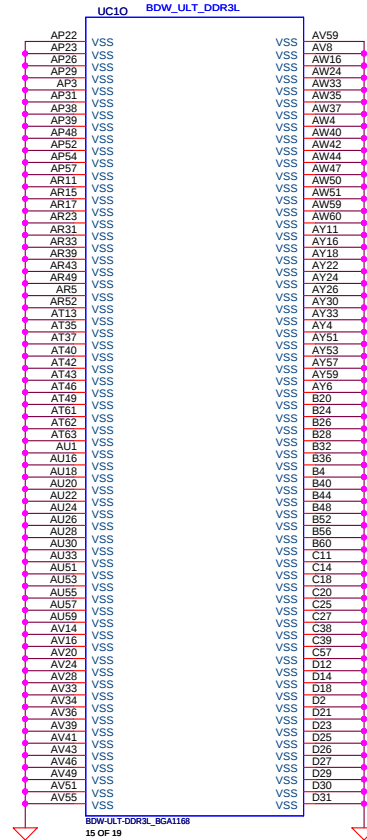
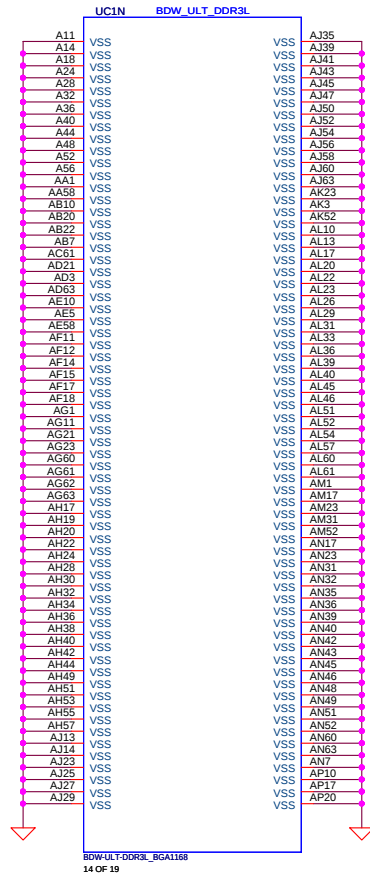
Compal Electronics, Inc.

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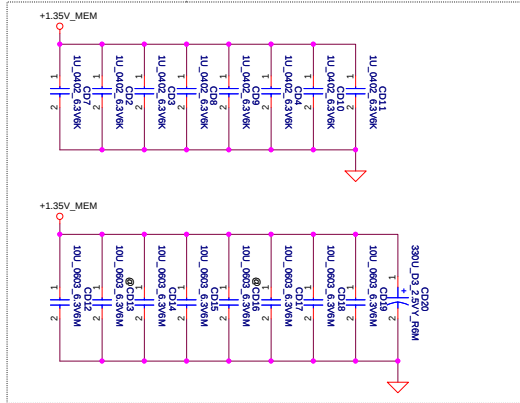
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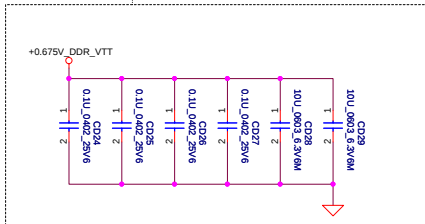
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SCHEMATICS,MB AA913			
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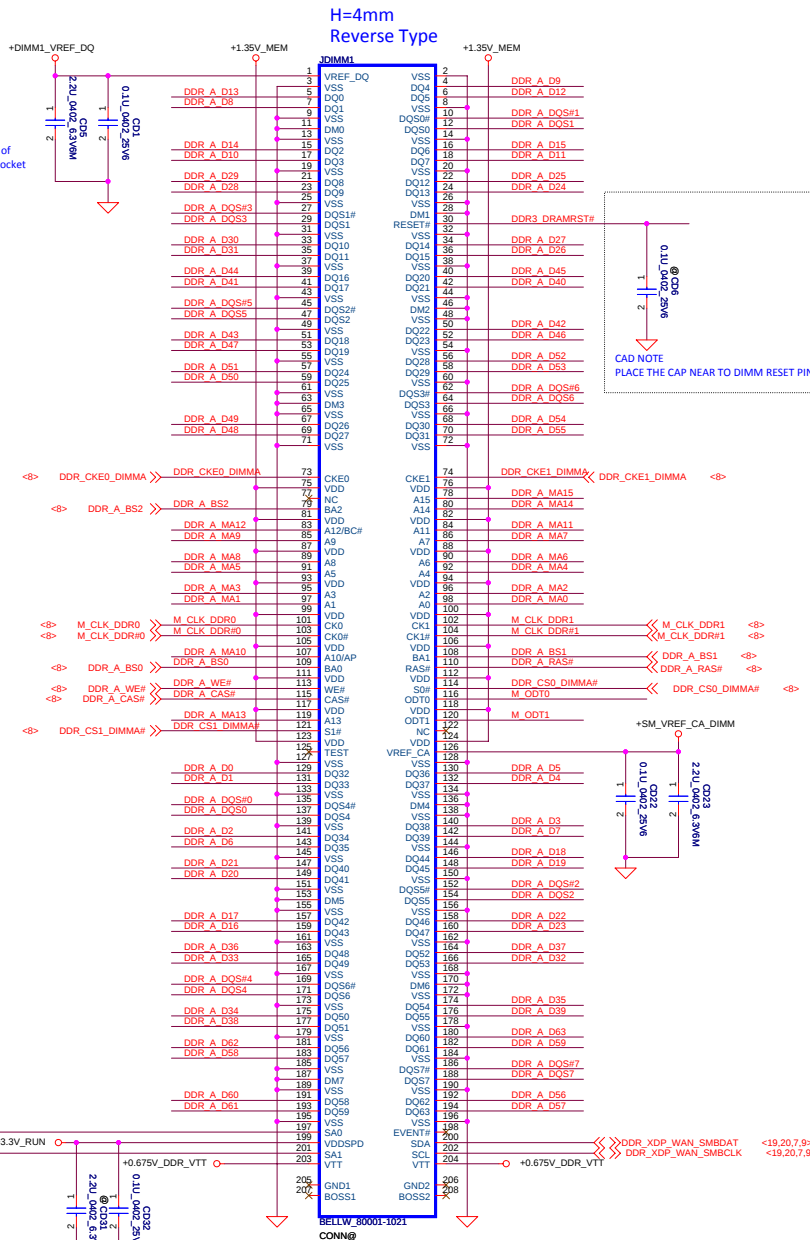
Layout Note:
Place near JDIMM1



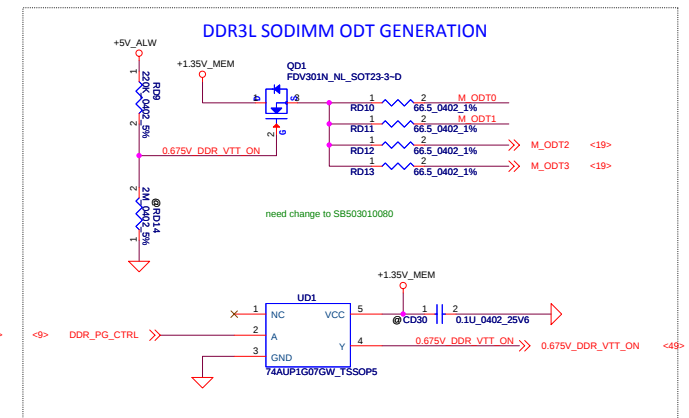
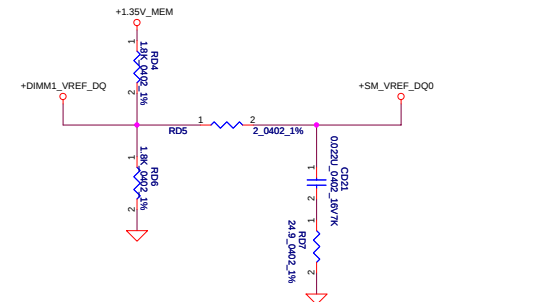
Layout Note:
Place near
JDIMM1.203,204



Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



SP07000P700 LINK DONE



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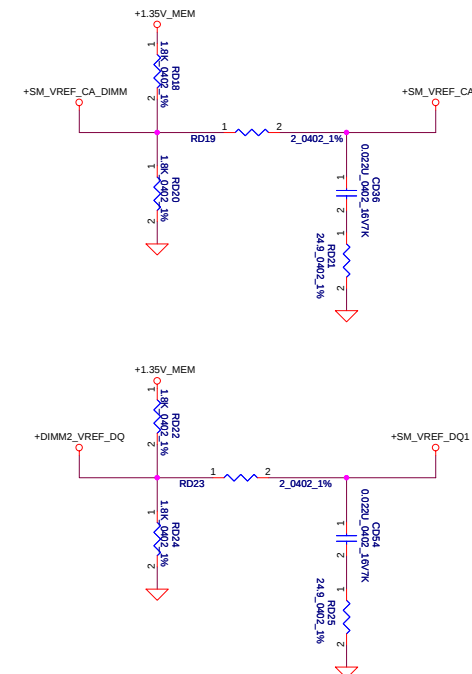
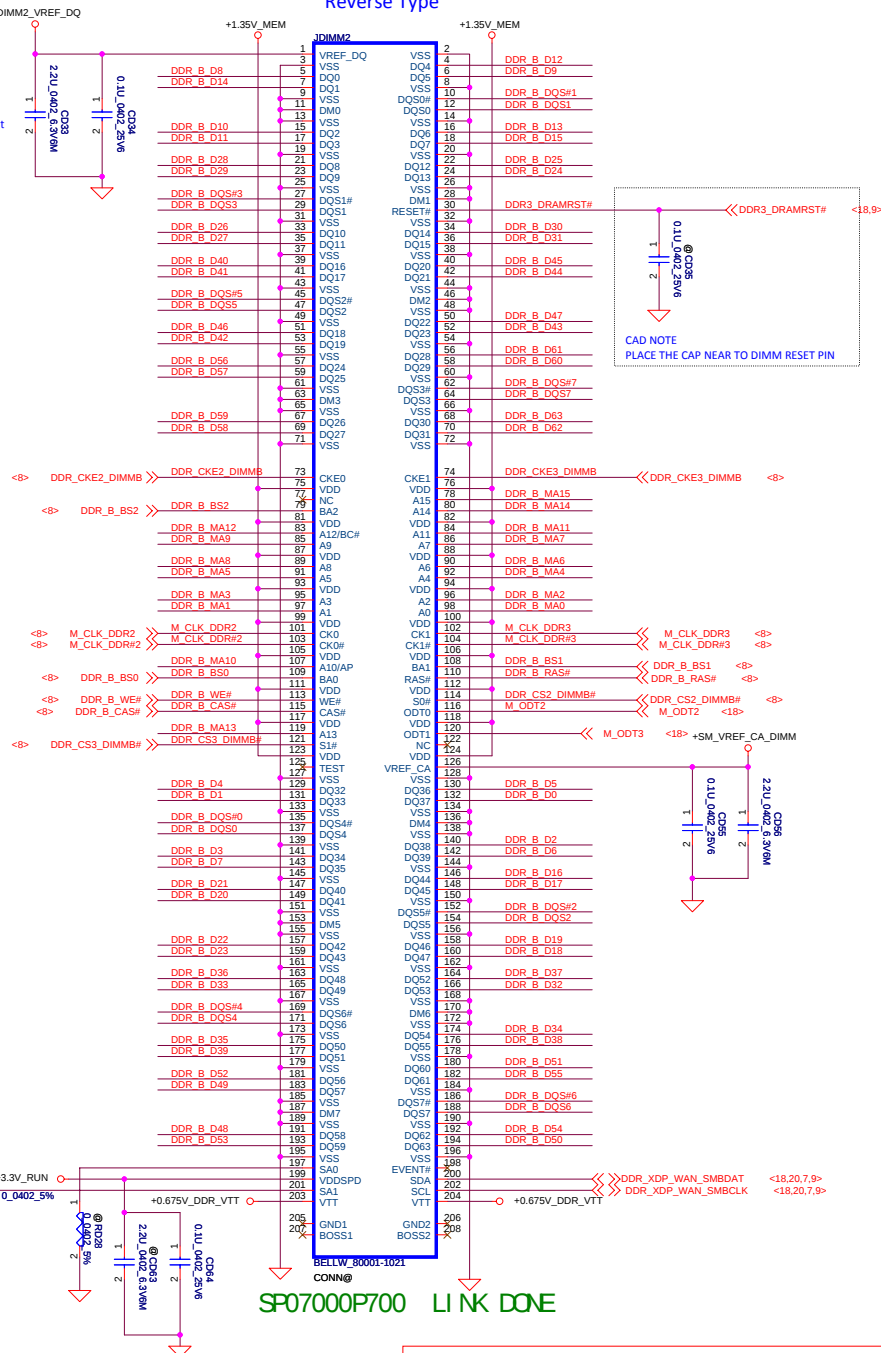
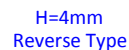
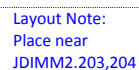
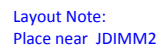


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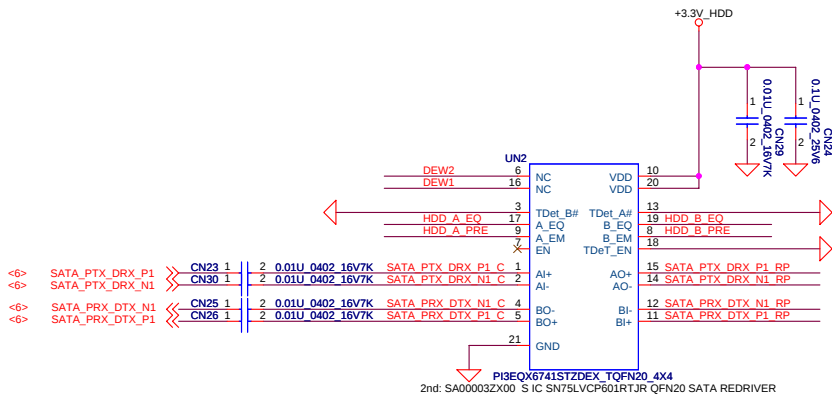
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	4019RA		
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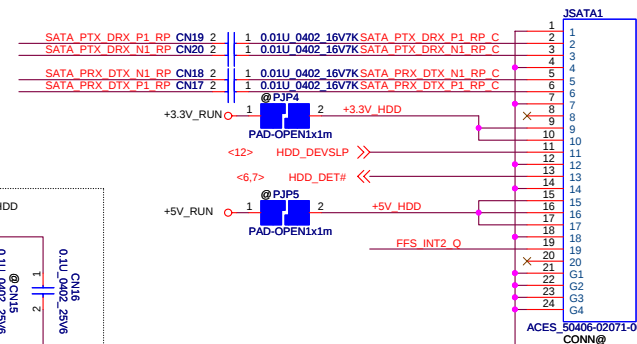
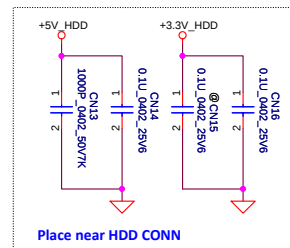
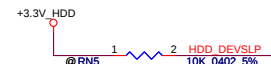
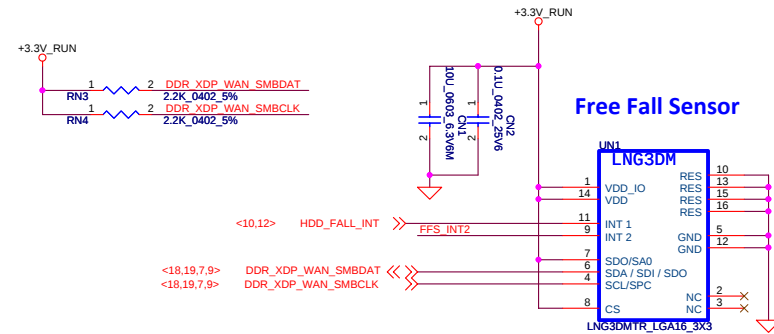
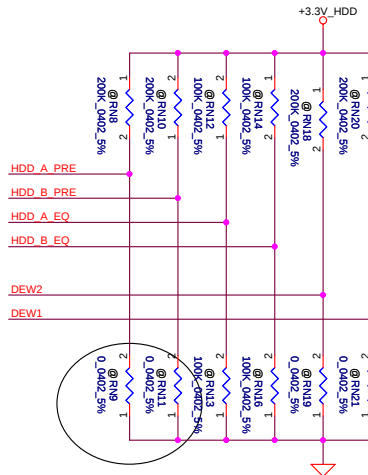
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SATA Repeater



PERICOM PI3EQX6741ST:
Pin6/16, NC
Pin8/9, Pre-emphasis

TI SN75LVCP601RTJR
Pin6/16, de-emphasis width setup
Pin8/9, de-emphasis



SP010016L00 LI NK DONE

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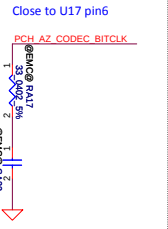
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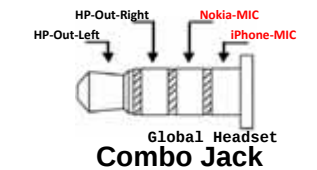
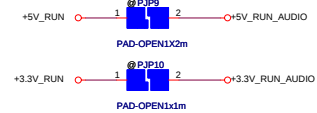
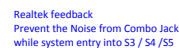
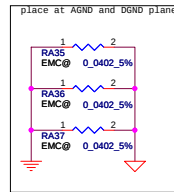
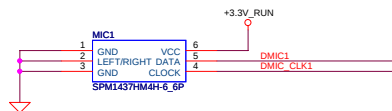
1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

40 mils trace keep 20 mil spacing

40 mils trace keep 20 mil spacing



Place closely to Pin 13. AUD_SENSE_A



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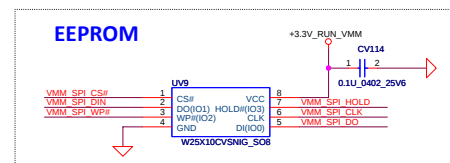
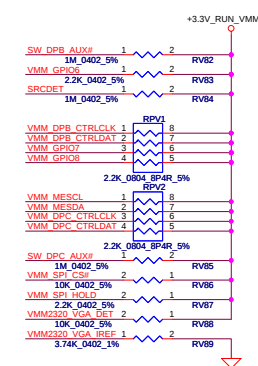
September 14, 2013

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Sheet 21 of

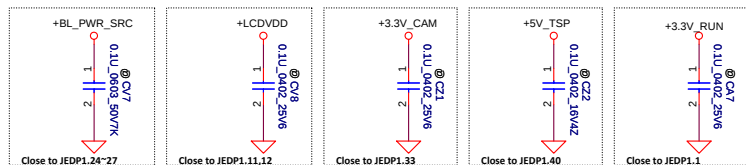
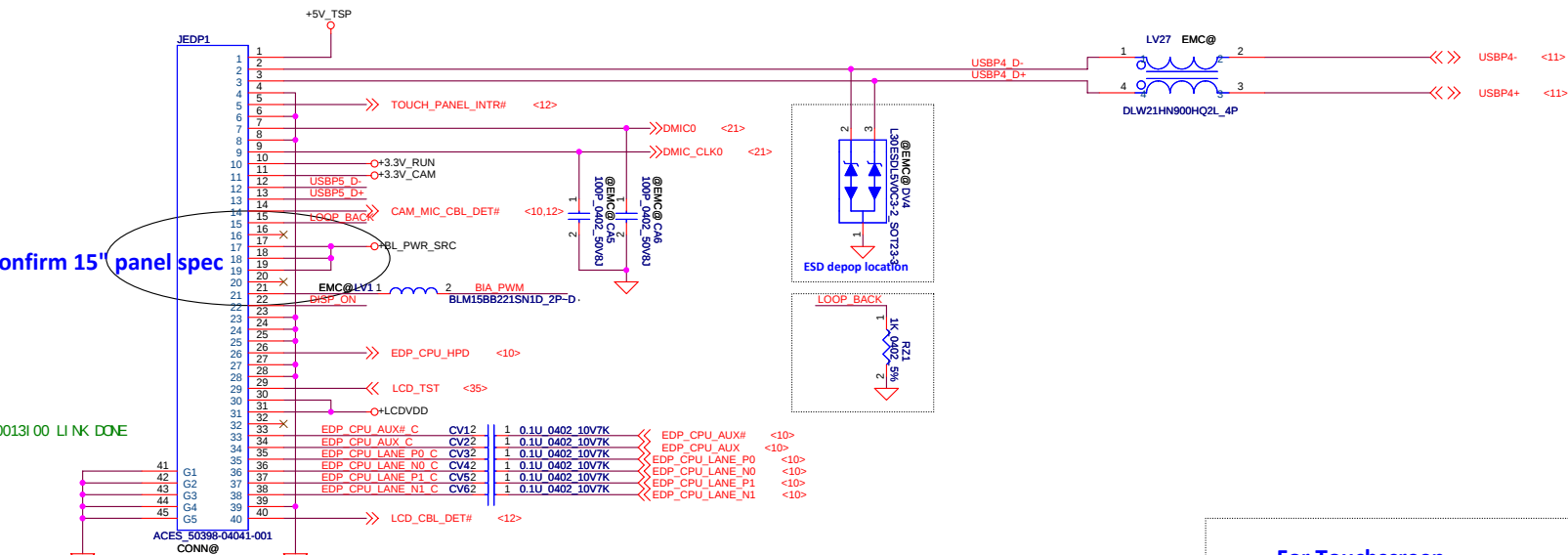
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56

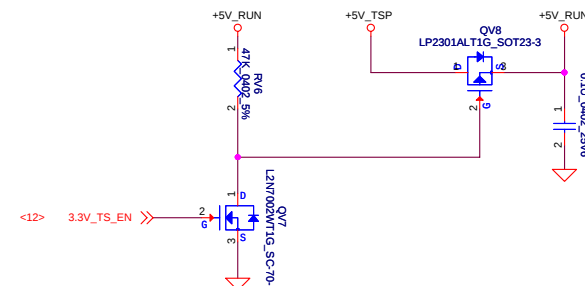


confirm 15" panel spec

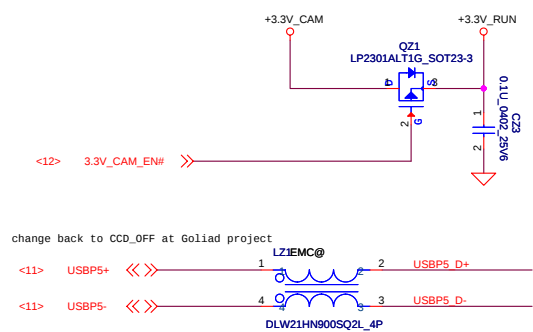
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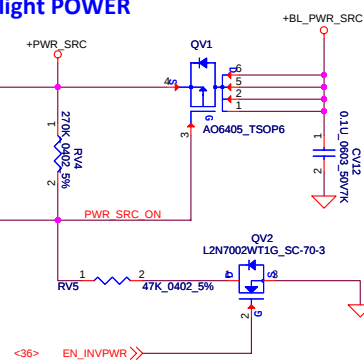
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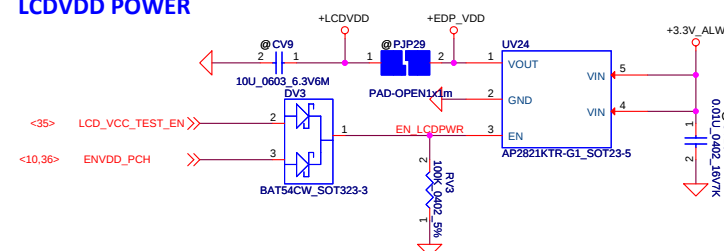
WebCAM



Backlight POWER



LCDVDD POWER



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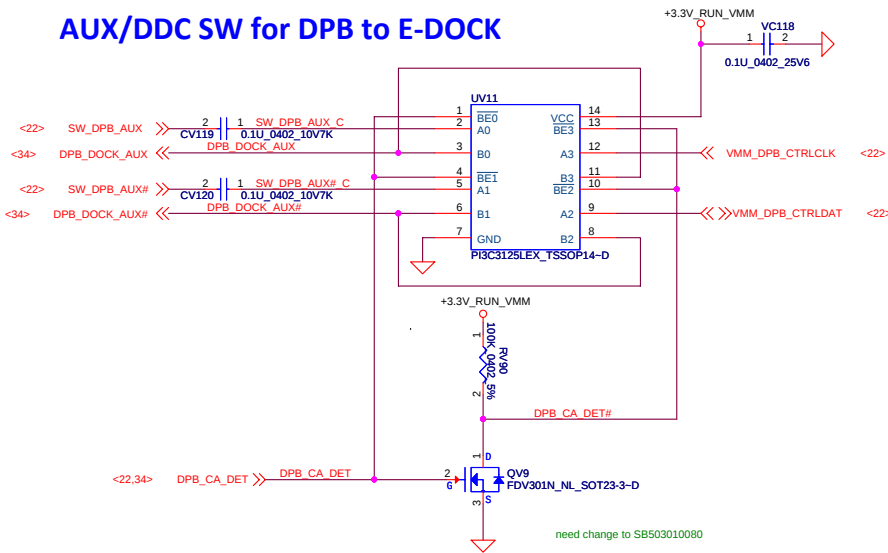
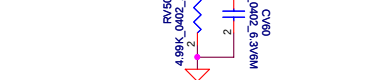
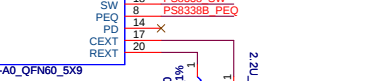
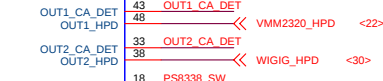
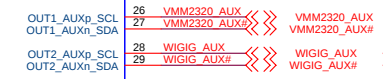
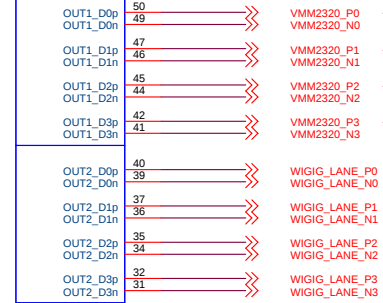
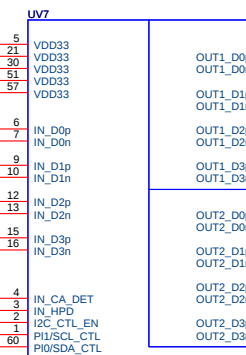
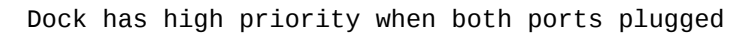
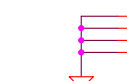
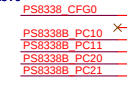
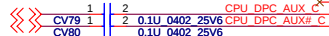
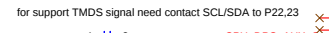
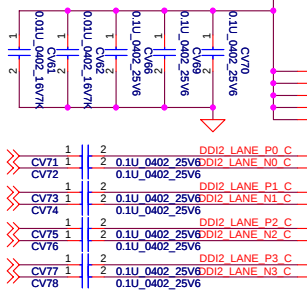
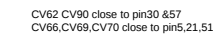
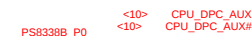
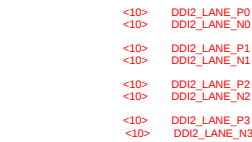
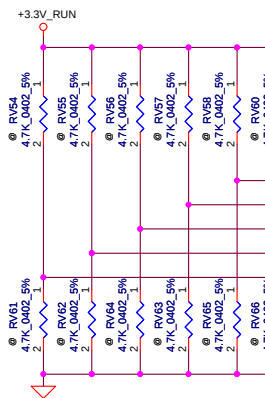
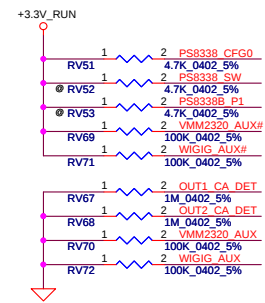
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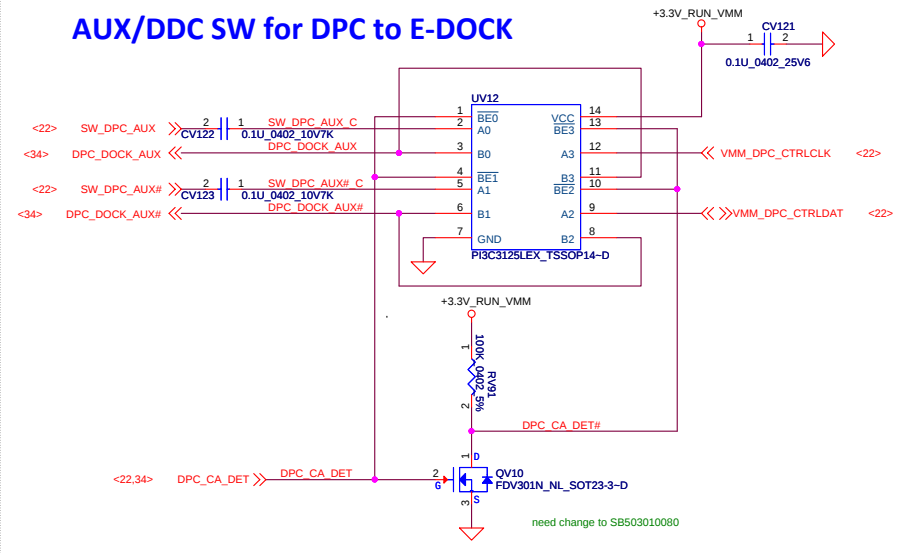
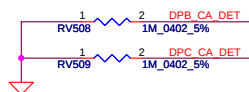
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14"/15" use 8338 at DOCK config
14"/15" use 12412 at Entry config

PCB	DP SWITCH
H12 UMA	PS8339+DP12412
H12 Entry	PS8339
H14 DSC	PS8338
H14 UMA	PS8338
H14D_En	DP12412
H14U_En	DP12412
H15 DSC	PS8338
H15 UMA	PS8338
H15D_En	DP12412
H15U_En	DP12412



need change to SB503010080



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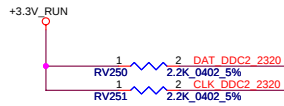
Size	Document Number	Rev
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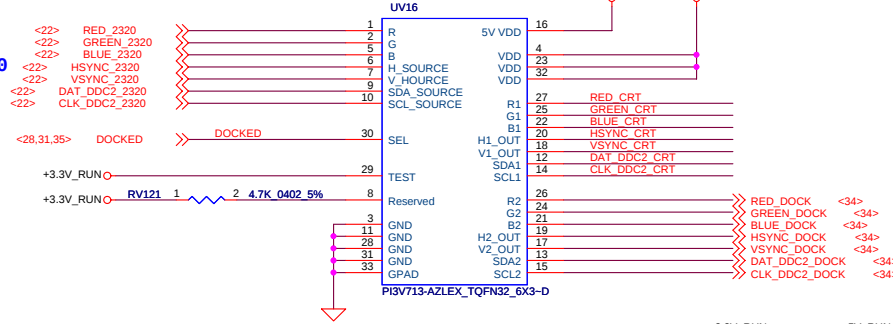
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VGA SW

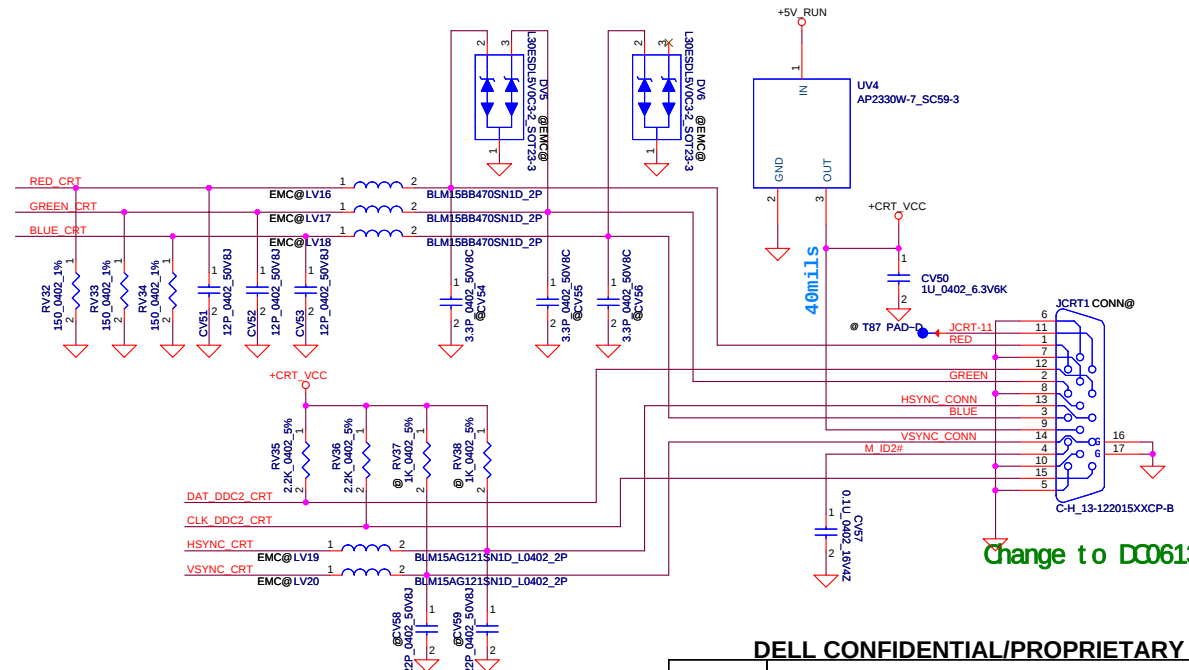
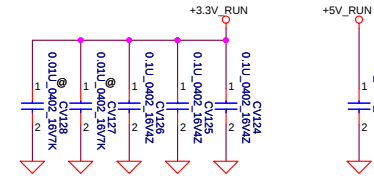
PCB	VGA SWITCH
H12 UMA	NA
H12 Entry	NA
H14 DSC	PI3V713
H14 UMA	PI3V713
H14D_En	NA
H14U_En	NA
H15 DSC	PI3V713
H15 UMA	PI3V713
H15D_En	NA
H15U_En	NA



source from VMM2320



SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR



Change to D0061307290.

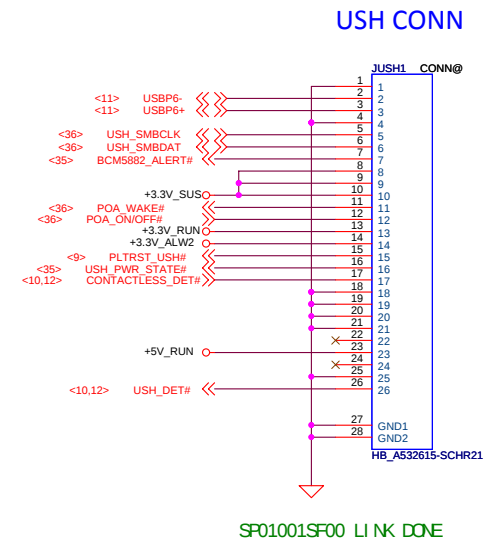
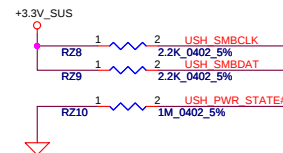
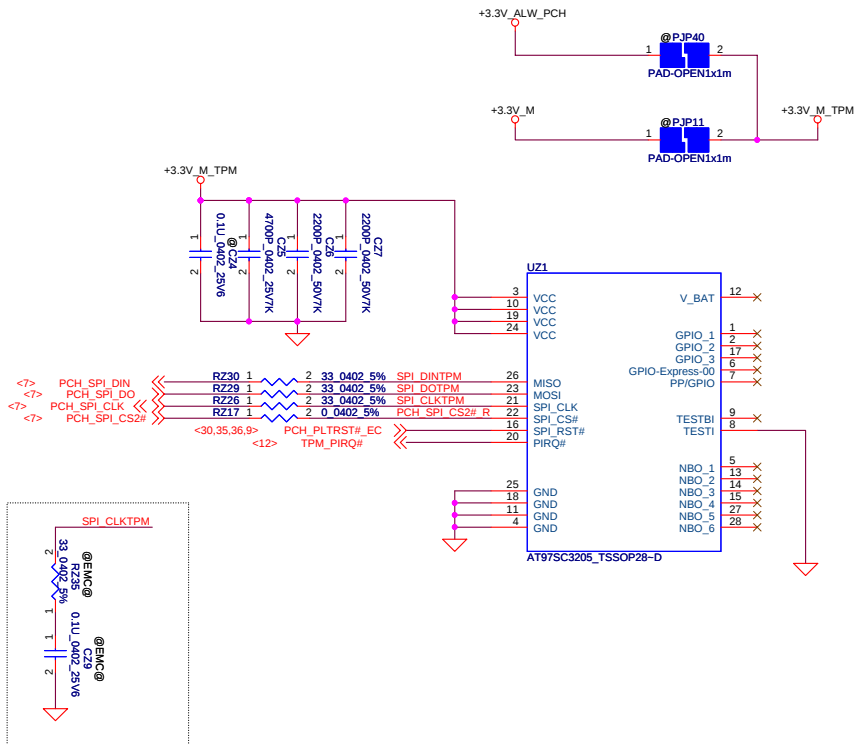
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Size Document Number
4019RA

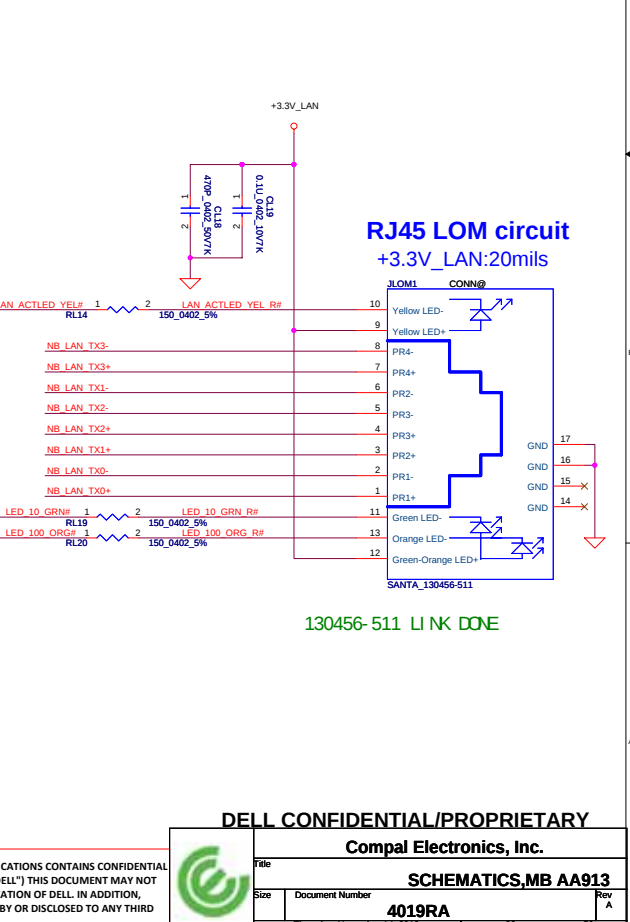
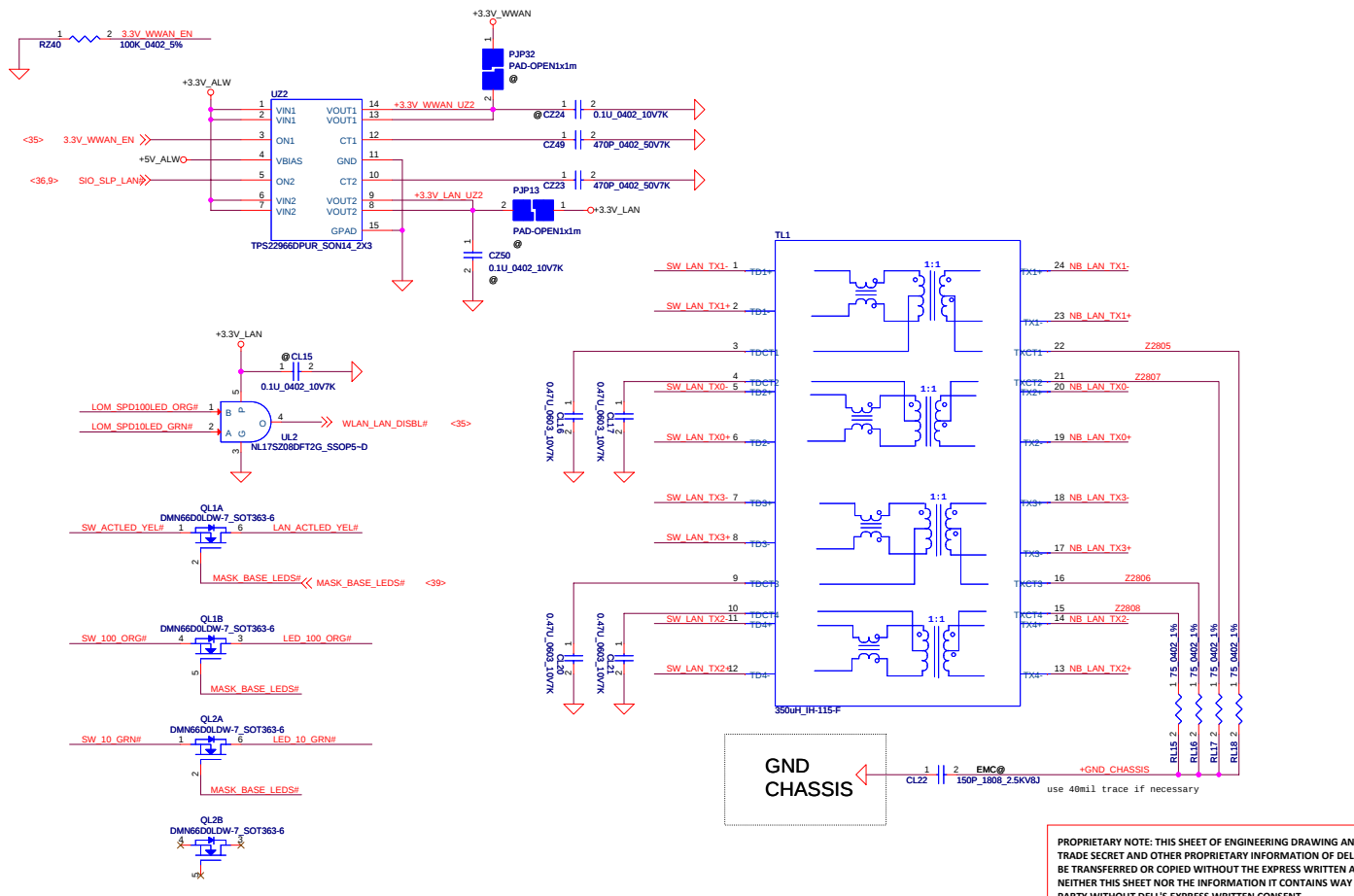
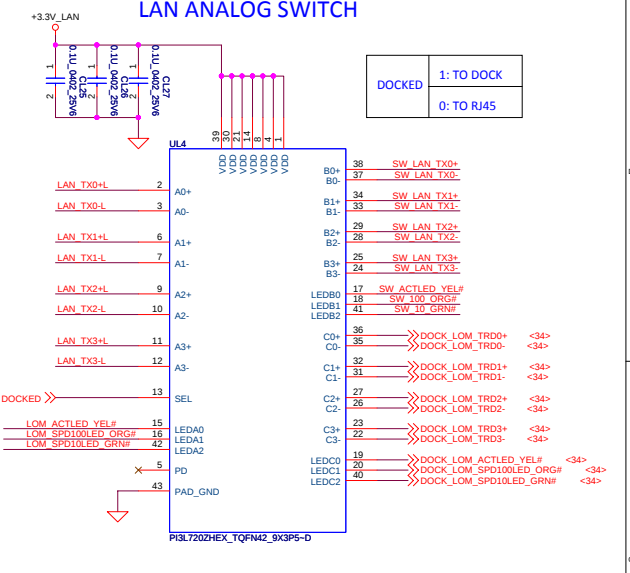
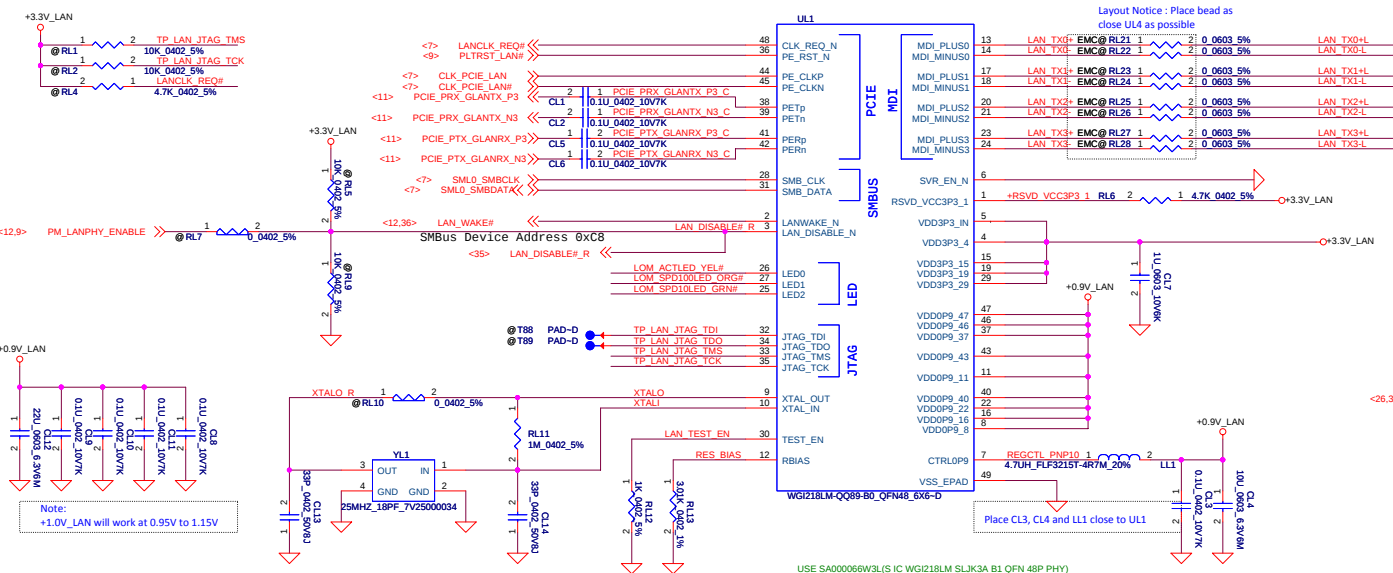
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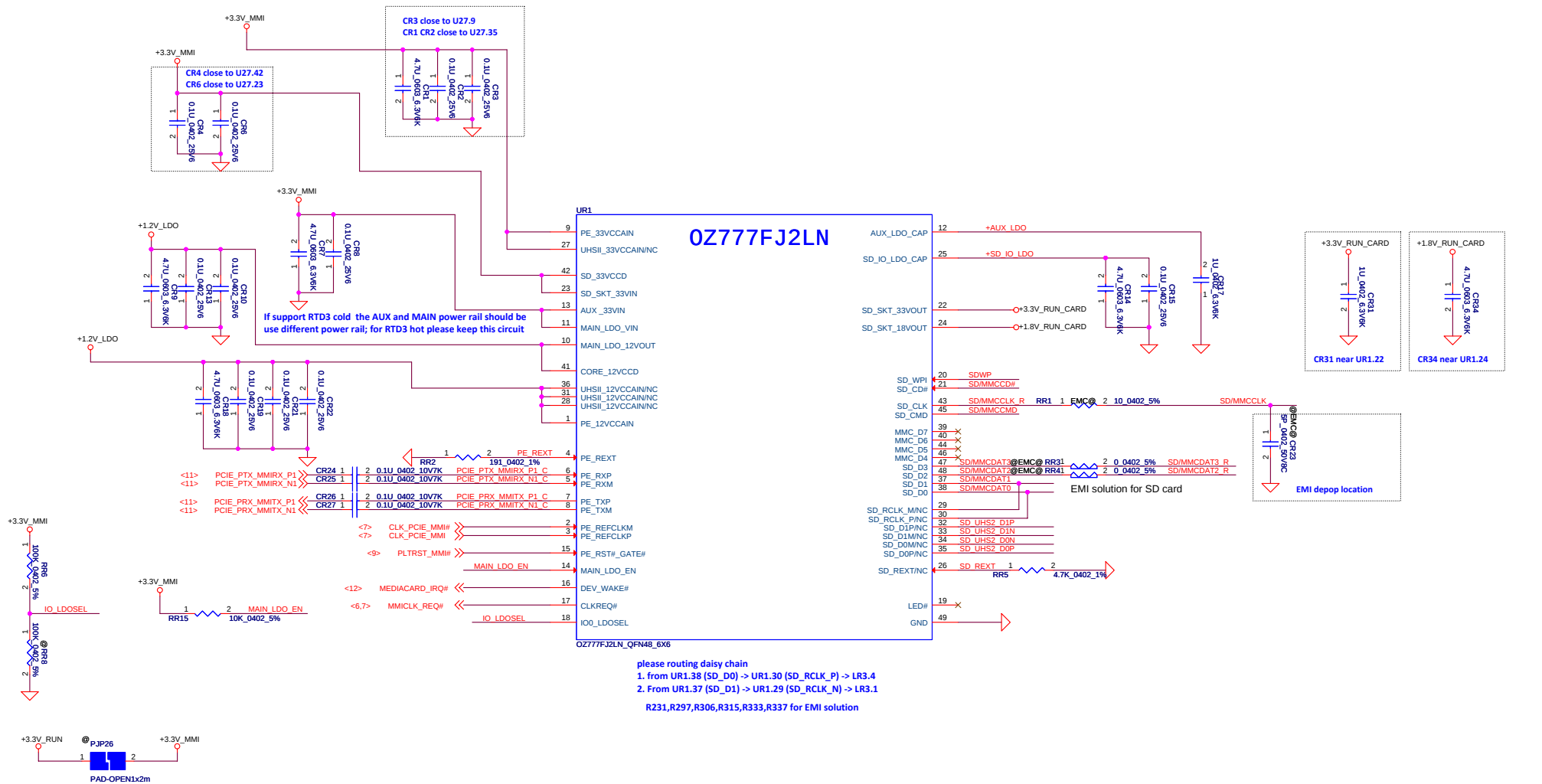


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SF070011L00 LI NK DONE

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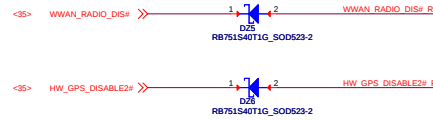
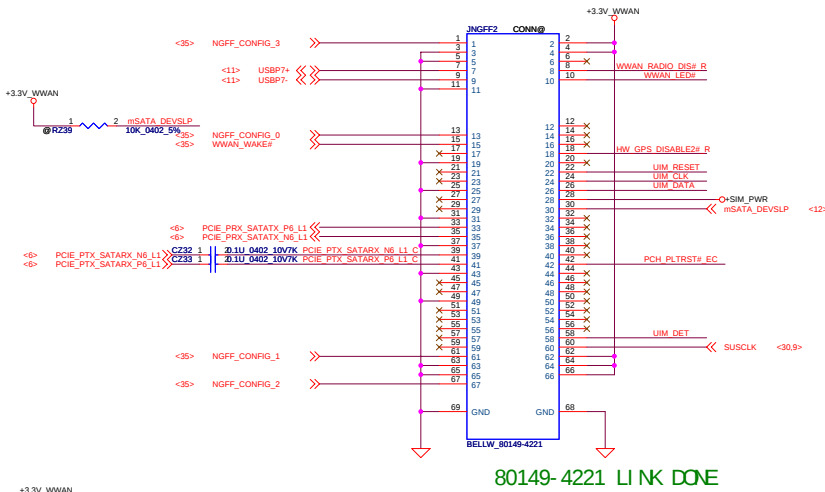
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NGFF slot B Key B

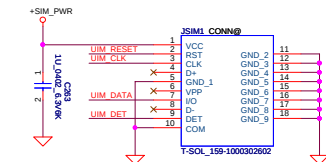
NGFF for DSC

NGFF slot A Key A

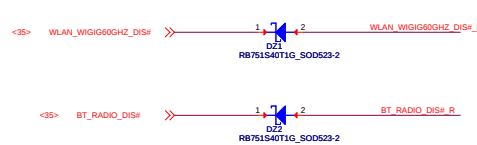
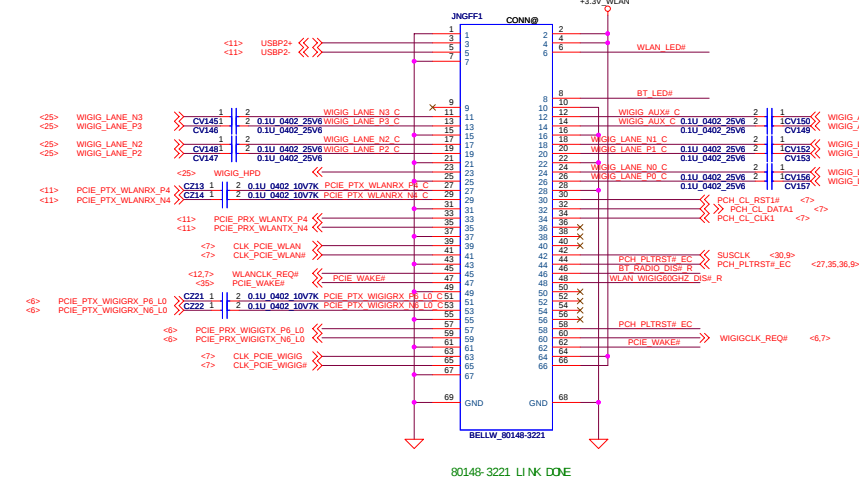
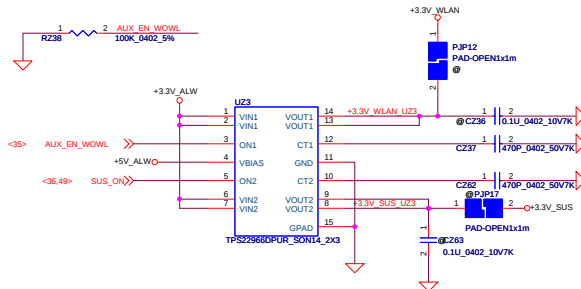


STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIE
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE
15	HIGH	HIGH	HIGH	HIGH	NA

SIM Card Push-Push



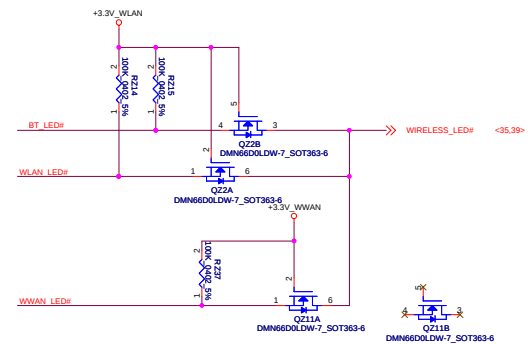
SP070011M00 LI NK DONE



Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

LED control circuit



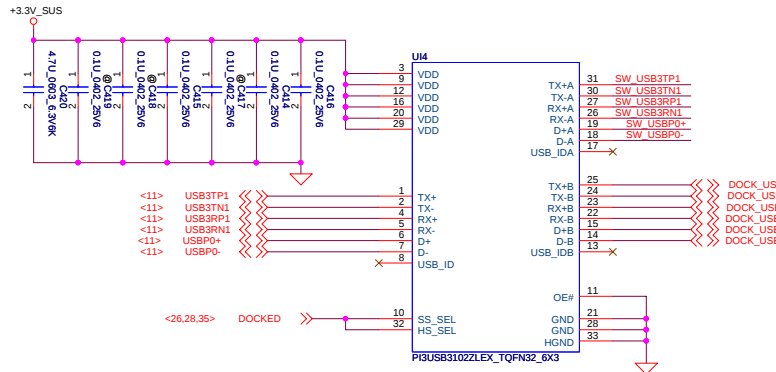
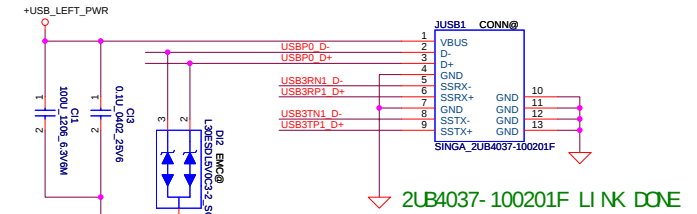
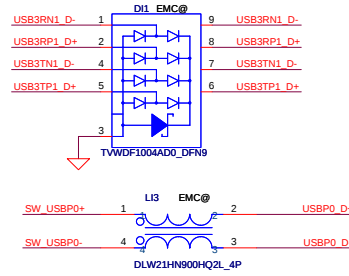
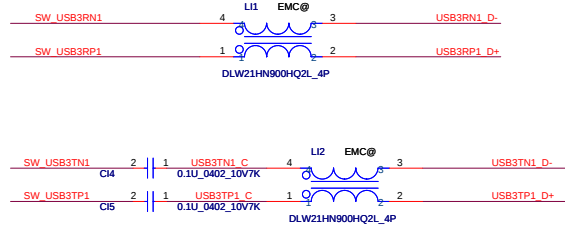
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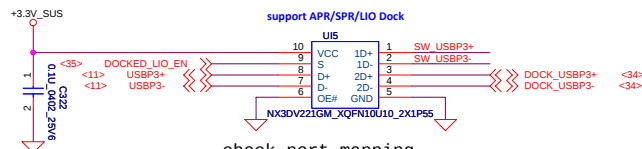
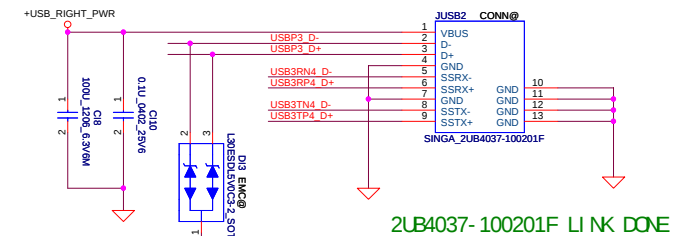
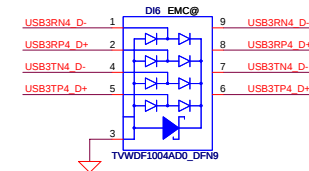
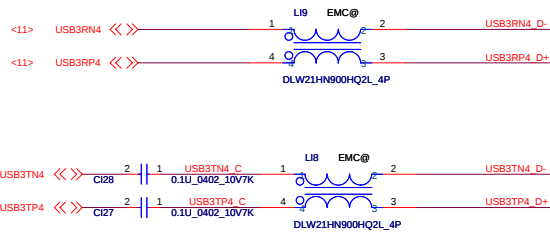
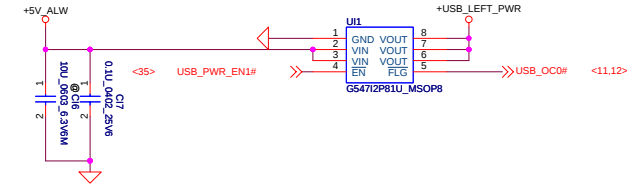
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check port mapping

DOCKED	function
1	Dock
0	M/B

PCB	USB2 0	USB2 3
H12 UMA	USB3102	NX3DV221
H12 Entry	NA	NA
H14 DSC	USB3102	NX3DV221
H14 UMA	USB3102	NX3DV221
H14D_En	NA	NA
H14U_En	NA	NA
H15 DSC	USB3102	NX3DV221
H15 UMA	USB3102	NX3DV221
H15D_En	NA	NA
H15U_En	NA	NA

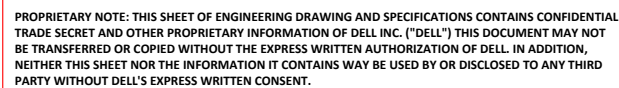


check port mapping

DOCKED_LIO_EN	function
1	Dock
0	M/B

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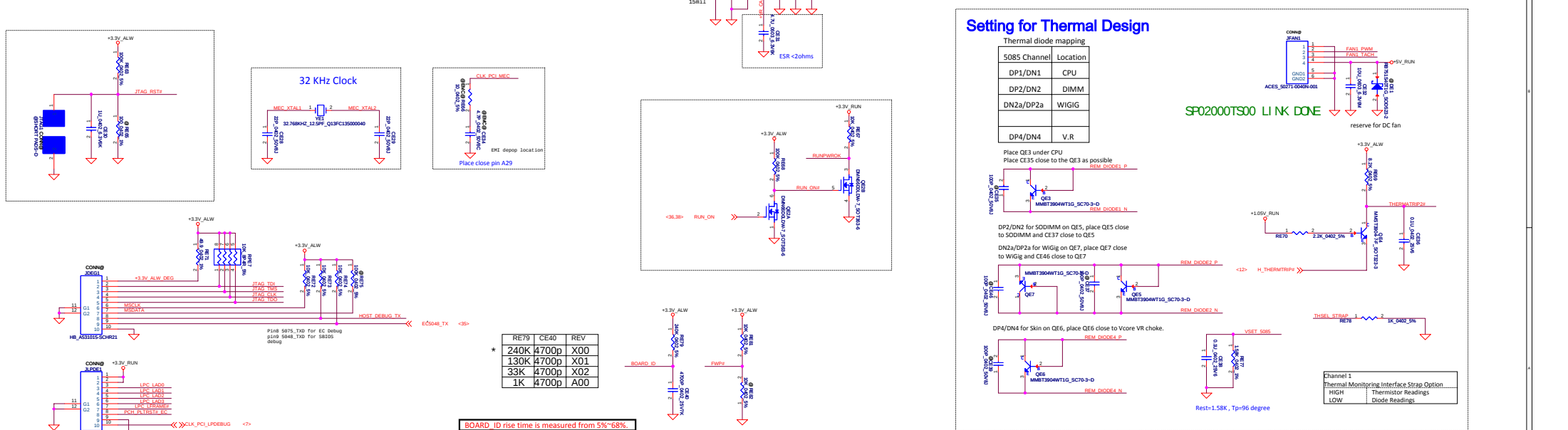
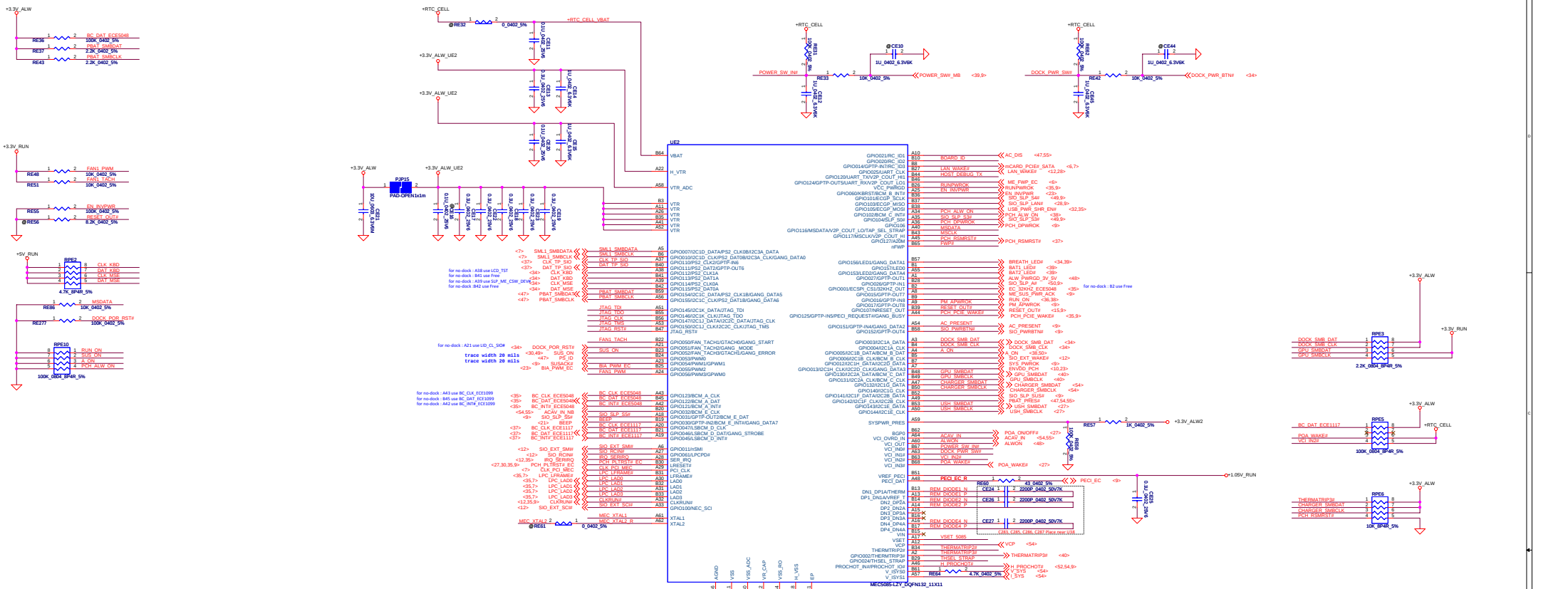
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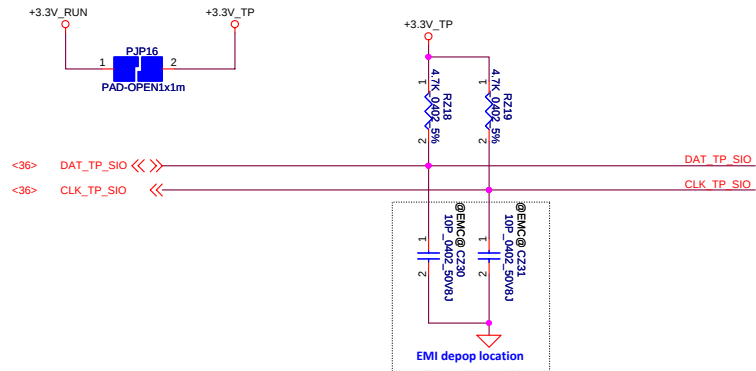
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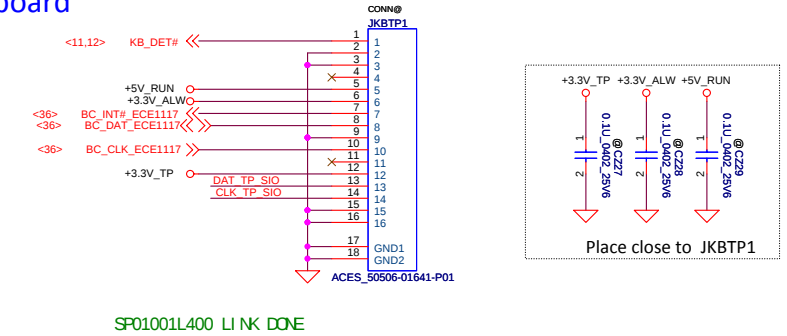
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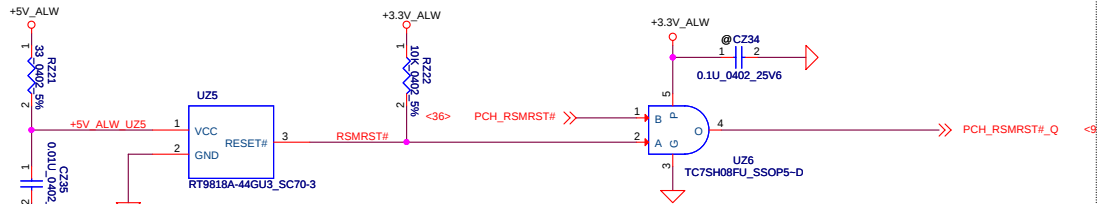
Touch Pad



Keyboard



RSMRST circuit



@eDP Cable

Part Number	Description
DC82C087A08	H-CONN SET 13M MB-EDP

@eDP Cable w camera

Part Number	Description
DC82C087908	H-CONN SET 13M MB-EDP-CAMERA

@eDP TS Cable w camera

Part Number	Description
DC82C087808	H-CONN SET 13M MB-EDP-CAMERA-TS

@SATA Cable-Spindle HDD

Part Number	Description
DC82C087808	H-CONN SET 13M MB-SPINDLE HDD

@SATA Cable-mSATA

Part Number	Description
DC82C087708	H-CONN SET 13M MB-MSATA HDD

@DC-IN Cable

Part Number	Description
DC30180MF08	CONN SET 0VN DCJACK-MB 20W1803-038110F

@RTC BATT

Part Number	Description
DC30180MF08	CONN SET 0VN DCJACK-MB 20W1803-038110F

@FAN

Part Number	Description
DC28A080808	FAN SET DAQ26 DC5V AB7405HB-HB3 ADDA

@KBTP FFC

Part Number	Description
NBX08081JH08	FFC 16P G P8.5 PAD=0.3 66.5MM MB-TP 13M

@Audio Board FFC

Part Number	Description
NBX08081JP08	FFC 12P F P.5 PAD=-.35 26.85MM MB-AUDIO/B

@USH Board FFC

Part Number	Description
NBX08081JF08	FFC 26P G P8.5 PAD=0.3 58MM MB-USH/B 13M

@LED Board FFC

Part Number	Description
NBX08081JM08	FFC 10P G P.5 PAD.3 192.5MM MB-LED/B 13M

@PWR Board FFC

Part Number	Description
NBX08081JL08	FFC 6P G P8.5 PAD=0.3 31MM MB-PWR/B 13M

@FP FFC-Validity

Part Number	Description
NBX08081JN08	FFC 8P F P8.5 PAD=0.3 170MM USH/B-FP VALIDITY

@FP FFC-TCS

Part Number	Description
NBX08081JO8	FFC 8P F P8.5 PAD=0.3 164.8MM USH/B-FP-TCS

@Speak

Part Number	Description
PK2308083Q0L	SPK PACK ZJX 2.0W 4 OHM FG

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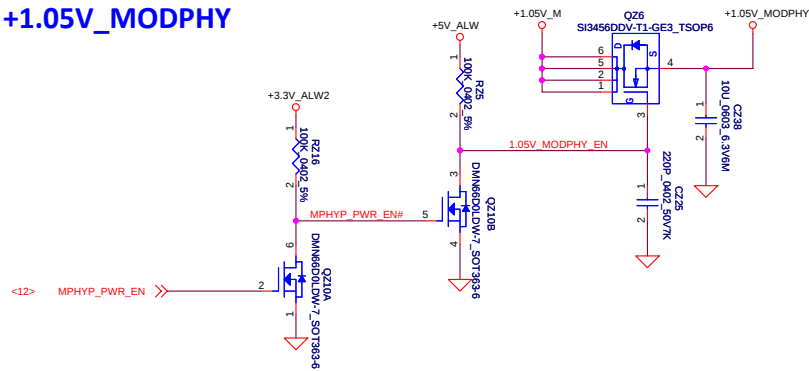
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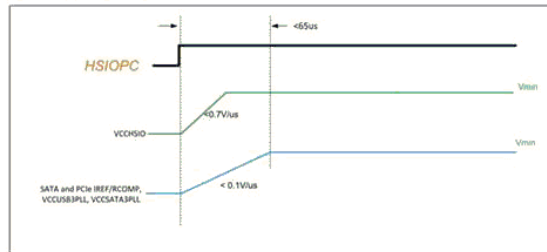
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+1.05V_MODPHY

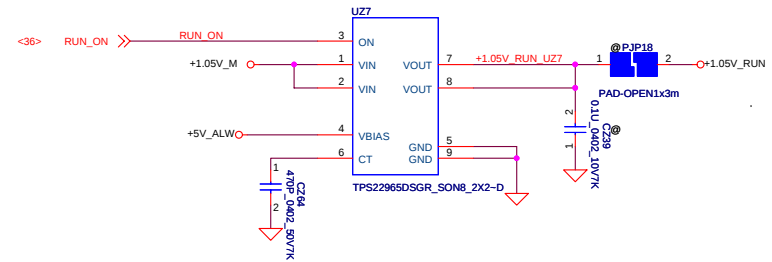


if support MODPHY off keep DSC solution
MODPHY timing spec 0.7V/us and <65us

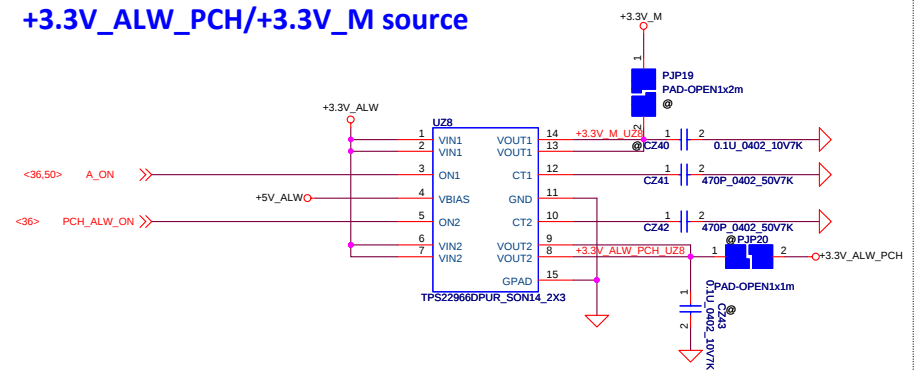
Figure 5-6. Sequencing Requirements between HSIOPC and LPT-LP 1.05V rails and COMP/IREF signals



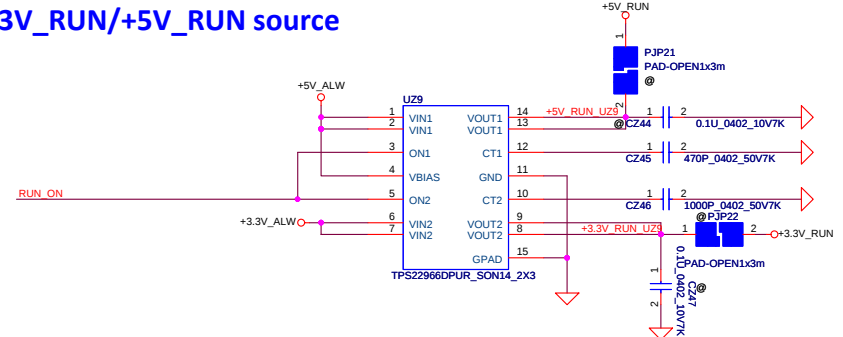
+1.05V_RUN source



+3.3V_ALW_PCH/+3.3V_M source



+3.3V_RUN/+5V_RUN source



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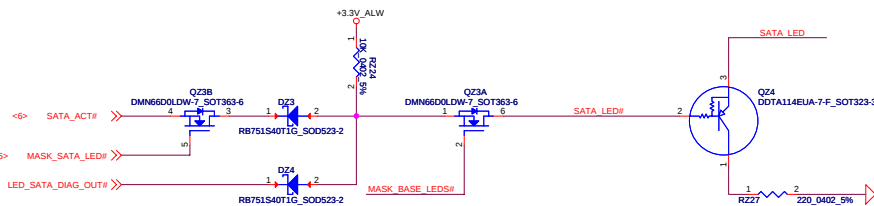
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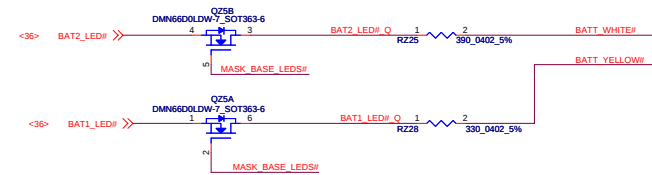
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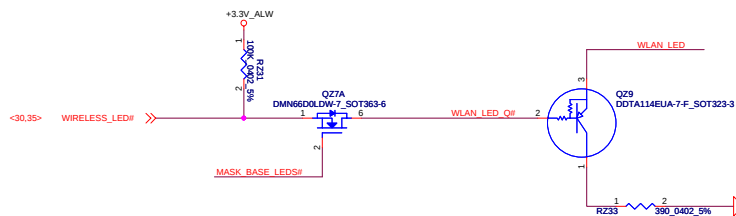
HDD LED solution for White LED



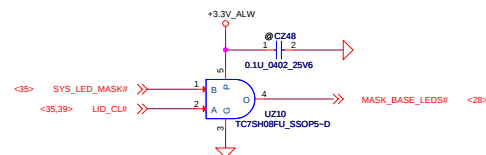
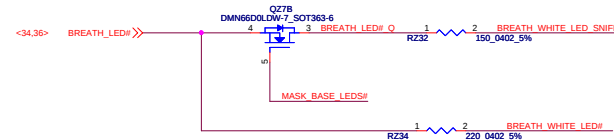
Battery LED



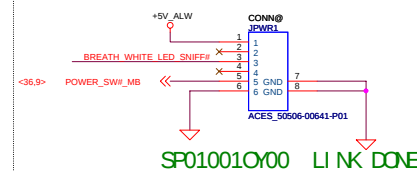
WLAN LED solution for White LED



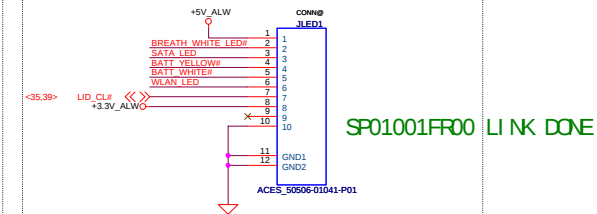
Breath LED



POWER board CONN



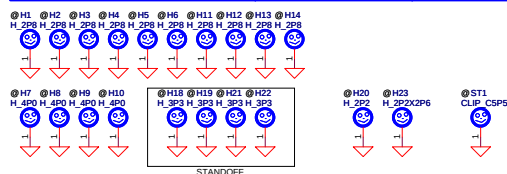
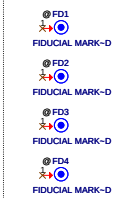
LED board CONN



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark



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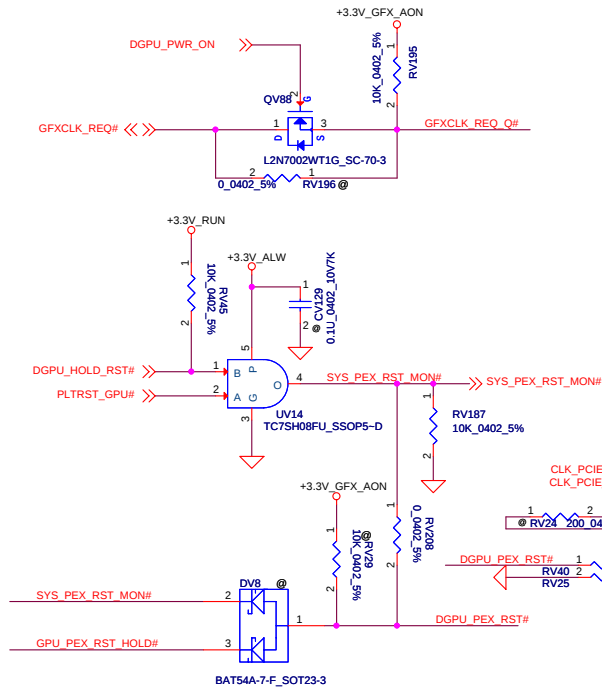
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PEG_CTX_GRX_P[0..3] >> PEG_CTX_GRX_P[0..3]
 PEG_CTX_GRX_N[0..3] >> PEG_CTX_GRX_N[0..3]
 PEG_CRX_GTX_P[0..3] << PEG_CRX_GTX_P[0..3]
 PEG_CRX_GTX_N[0..3] << PEG_CRX_GTX_N[0..3]

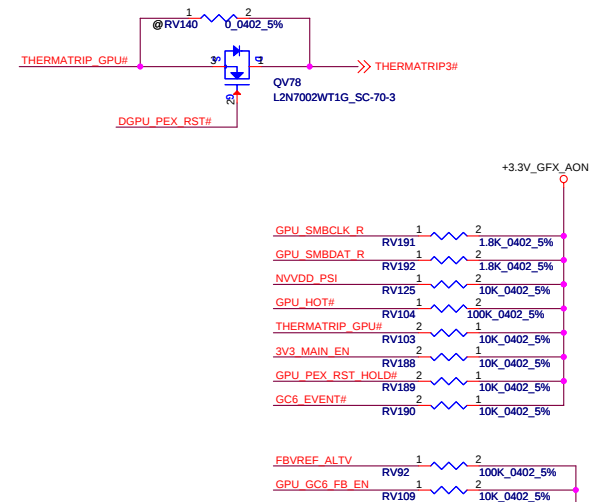
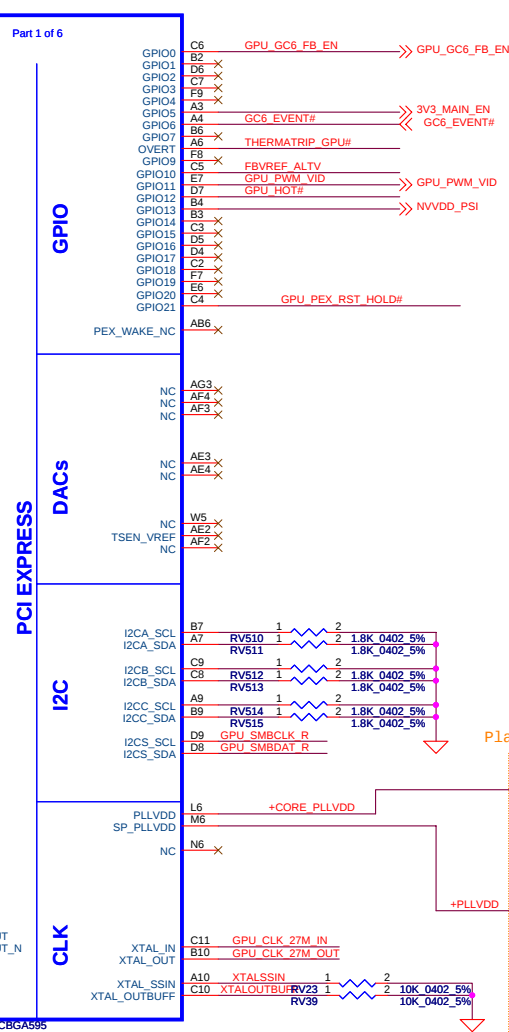
PEG_CRX_GTX_P0	CV188	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P0
PEG_CRX_GTX_N0	CV189	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N0
PEG_CRX_GTX_P1	CV190	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P1
PEG_CRX_GTX_N1	CV191	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N1
PEG_CRX_GTX_P2	CV192	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P2
PEG_CRX_GTX_N2	CV193	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N2
PEG_CRX_GTX_P3	CV194	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P3
PEG_CRX_GTX_N3	CV195	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N3



ES sample : Depop DV8,RV29 , Pop RV208
 QS sample : pop DV8,RV29 , depop RV208

GPU_PWR_LEVEL	
LOW	Low Performance
HIGH	High Performance

PEG CTX GRX P0	AG6	PEX_RX0
PEG CTX GRX N0	AG7	PEX_RX0_N
PEG CTX GRX P1	AF7	PEX_RX1
PEG CTX GRX N1	AE7	PEX_RX1_N
PEG CTX GRX P2	AE9	PEX_RX2
PEG CTX GRX N2	AF9	PEX_RX2_N
PEG CTX GRX P3	AG9	PEX_RX3
PEG CTX GRX N3	AG10	PEX_RX3_N
	AE10	NC
	AE12	NC
	AG10	NC
	AG11	NC
	AF13	NC
	AE13	NC
	AE15	NC
	AG15	NC
	AG16	NC
	AF16	NC
	AE16	NC
	AE18	NC
	AF18	NC
	AG18	NC
	AG19	NC
	AE19	NC
	AE21	NC
	AG20	NC
	AG21	NC
	AG22	NC
	X	NC
PEG CRX GTX C P0	AC9	PEX_TX0
PEG CRX GTX C N0	AB9	PEX_TX0_N
PEG CRX GTX C P1	AB10	PEX_TX1
PEG CRX GTX C N1	AC10	PEX_TX1_N
PEG CRX GTX C P2	AD11	PEX_TX2
PEG CRX GTX C N2	AC11	PEX_TX2_N
PEG CRX GTX C P3	AC12	PEX_TX3
PEG CRX GTX C N3	AB12	PEX_TX3_N
	AB13	NC
	AD13	NC
	AD14	NC
	AC14	NC
	AC15	NC
	AB16	NC
	AB18	NC
	AC16	NC
	AD17	NC
	AC17	NC
	AC18	NC
	AB19	NC
	AB19	NC
	AC19	NC
	AD20	NC
	AC20	NC
	AC21	NC
	AB21	NC
	AD23	NC
	AE23	NC
	AE24	NC
	AE24	NC
	AG24	NC
	AG25	NC
	AE8	PEX_REFCLK
	AB8	PEX_REFCLK
◀◀GFXCLK REQ Q#	AC8	PEX_CLKREQ
PEX_TSTCLK_OUT	AF22	PEX_TSTCLK
PEX_TSTCLK_OUT#	AE22	PEX_TSTCLK
DGPPU_PEX_RST_R#	AC7	PEX_RST_TERM
0_0402_5%	AF25	PEX_TERM
K_0402_1%		
		GM108-ES03



Place close to ball

SP PLLVDD and VDD PLLVDD Power rail Filtering Combined		PLLVD Filtering	
Capacitor	Type	Population	Population
0.1uF	0402	1	1
4.7uF	0603	1	1
22uF	0805	1	1
Bead 180 ohm (ESR=0.2 ohm)	0603	1	1

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I2CSlave Address

SMBUS_ALT_ADDR Description	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

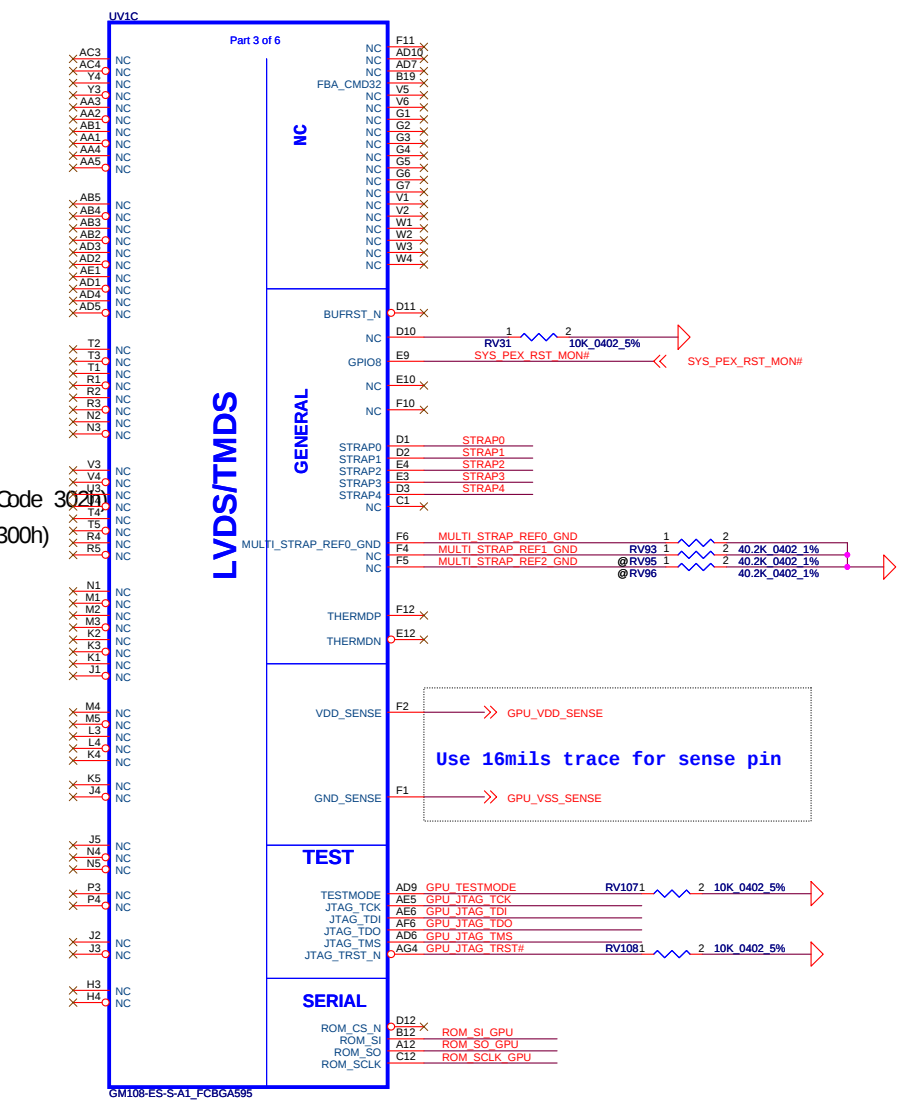
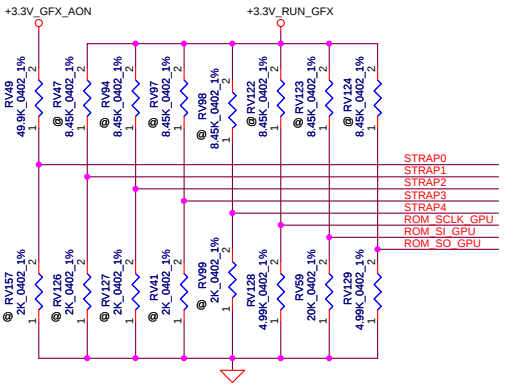
VGA_DEVICE Setting

VGA_DEVICE Description	
0	Non-Primary 3D Acceleration Device (Class Code 3020)
1	Primary Display or VGA Device (Class Code 300h)

Resistance Mapping to Hex Values

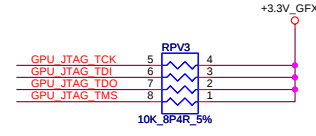
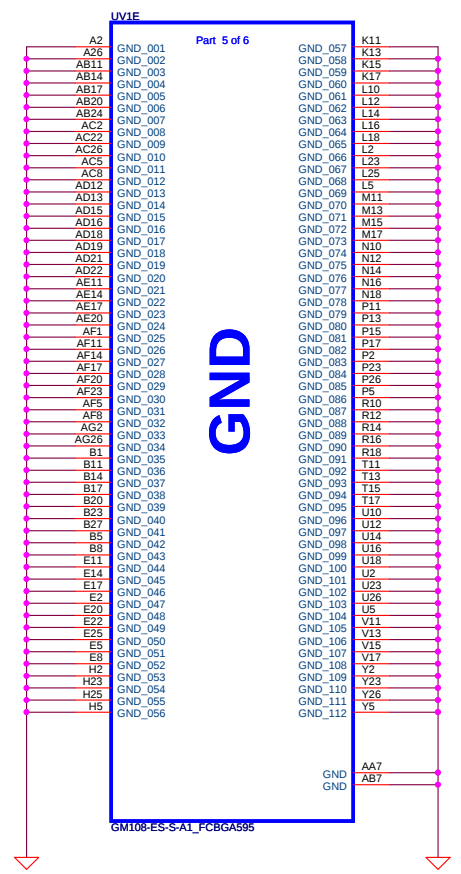
Resistor Value	Pull-up to VDD3	Pull-down to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Decide ID change to 0x1056



Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0	Note
ROM_SCLK	SOR3_EXPOSED->0	SOR2_EXPOSED->0	SOR1_EXPOSED->0	SOR0_EXPOSED->0	ROM_SCLK pull-down 4.99k to GND
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]	ROM_SI pull-down 20k to GND
ROM_SO	DEVID_SEL->0(default)	PCIE_CFG->0(default)	SMB_ALT_ADDR->0(default)	VGA_DEVICE->0	ROM_SO pull-down 4.99k to GND
STRAP0	Keep pull up to 3V3_AON and pull-down to GND footprint and stuff 50k ohm pull up				STRAP0 pull up 50k to +3.3V_GFX_AON
STRAP1 STRAP2 STRAP3 STRAP4	Reserve				

DEVID_SEL/PCIE_CFG default set 0, need refer Platform Update Notification for the latest configuration



VENDER	STRAP	Part Number	Note(ROM_SI)
Hynix	0x3	H5TC4G63AFR-11C	20k PD
Micron	0x4	MT41J256M16HA-093G:E	24.9k PD need change to MT41K256M16HA-107G:E
Samsung	0x5	K4W4G1646D-HC1A	30.1k PD

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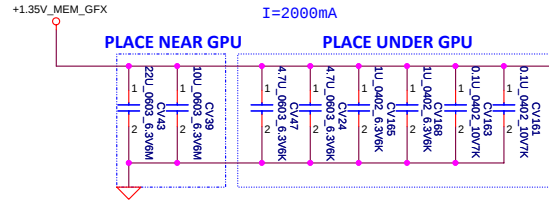
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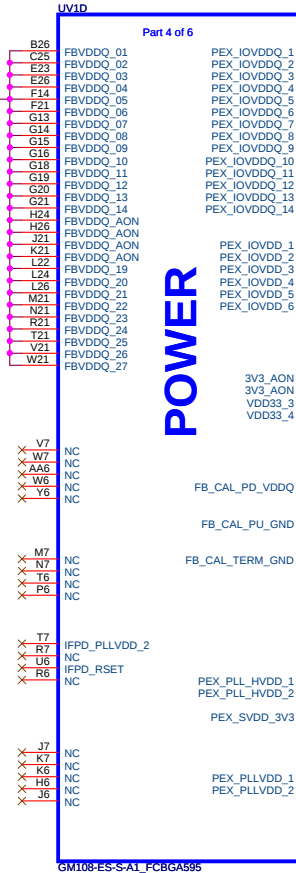
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DDR3 CPU side FBVDD/FBVDDQ Combined Decoupling		
Capacitor	Type	Population
0.1uF	0402	2
1.0uF	0603	2
4.7uF	0603	2
10uF	0805	1
22uF	0805	1

Power Supply Rail	NLS-GM	NLS-GT
(V)	(A)	(A)
GPU_Core	-	26
GPU_FBI_O	1.5/1.35	TBD
PEX_I_OVDD/Q	1.05	0.765
PEX_PLLVDD	1.05	0.130
FBA_PLL_AVDD	1.05	0.062
FBA_DLL_AVDD	1.05	0.032
PLL_VDD	1.05	0.058
SP_PLLVDD	1.05	0.030
1.05V Total	1.05	1.060
VDD83+3V3AON	3.3	0.036
PEX_SVDD_3V3	3.3	0.167
PEX_PLL_HVDD	3.3	0.022
3.3V Total	3.3	0.225



PEX_PLLVDD Decoupling		
Capacitor	Type	Population
0.1uF	0402	1
1uF	0603	1
4.7uF	0805	1

PEX_SVDD/PEX_PLL_HVDD Decoupling		
Capacitor	Type	Population
0.1uF	0402	1
4.7uF	0603	2

3V3_MAIN Decoupling		
Capacitor	Type	Population
0.1uF	0402	2
1uF	0603	1
4.7uF	0603	1

3V3_AON Decoupling		
Capacitor	Type	Population
0.1uF	0402	1
1uF	0603	1
4.7uF	0603	1

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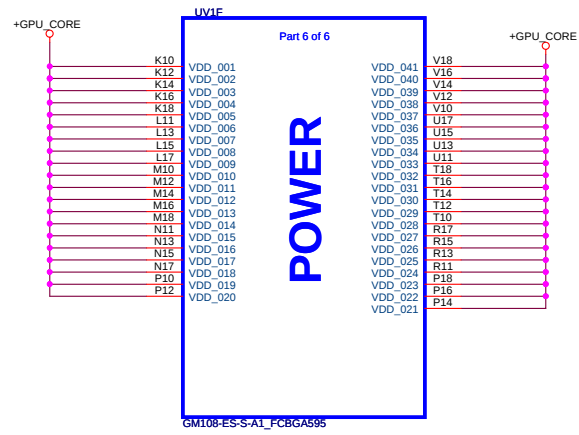
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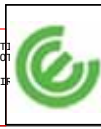
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Caps on Power Side
1UX4 4.7UX10 under GPU
4.7UX5 22UX1 47UX2 330UX2 near GPU



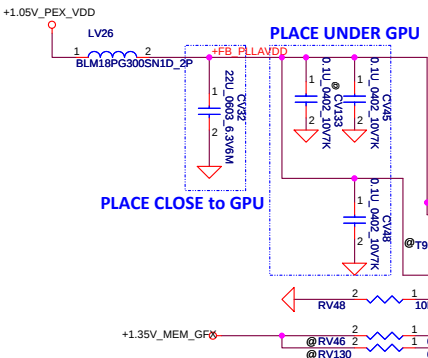
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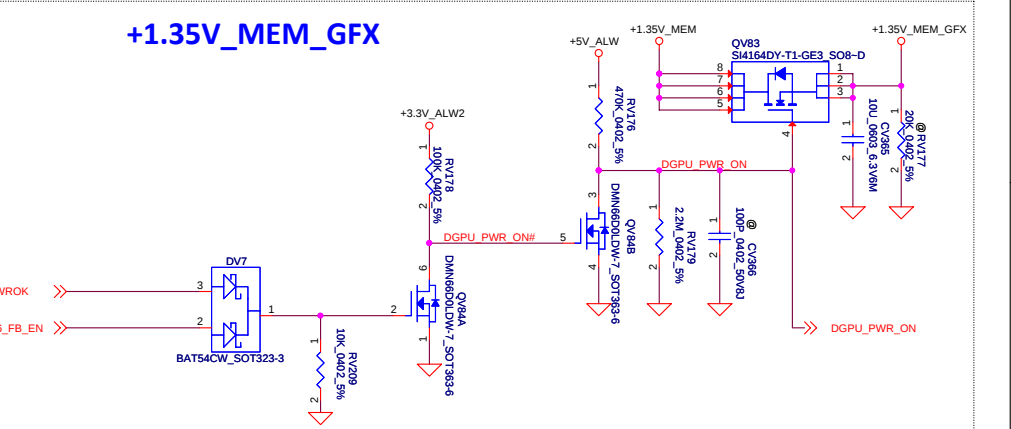
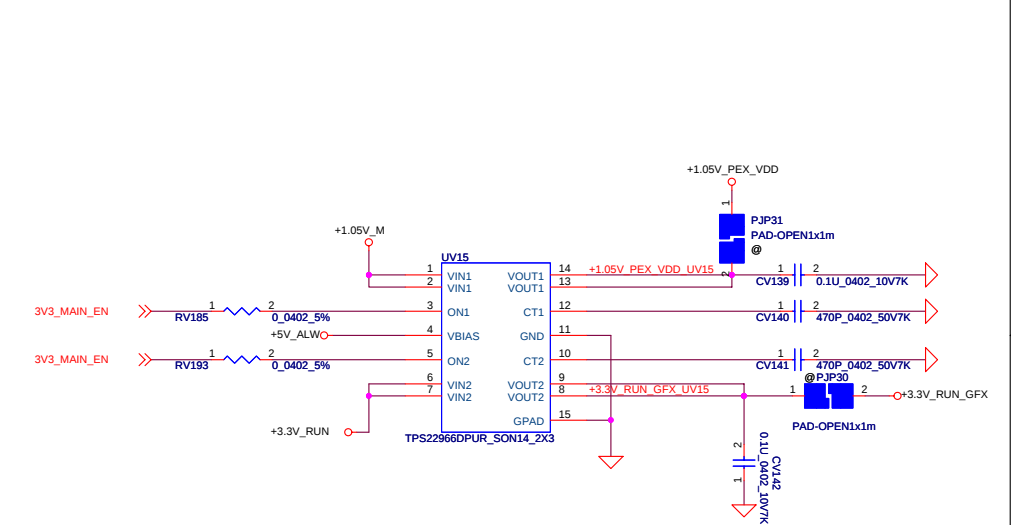
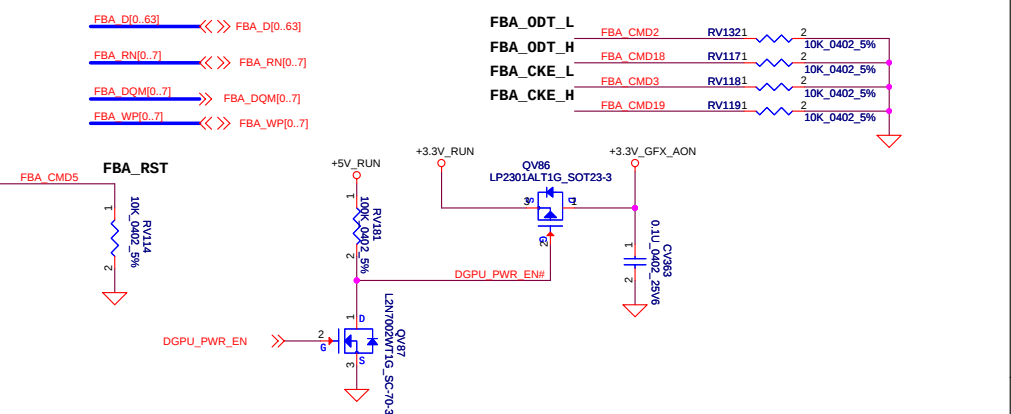
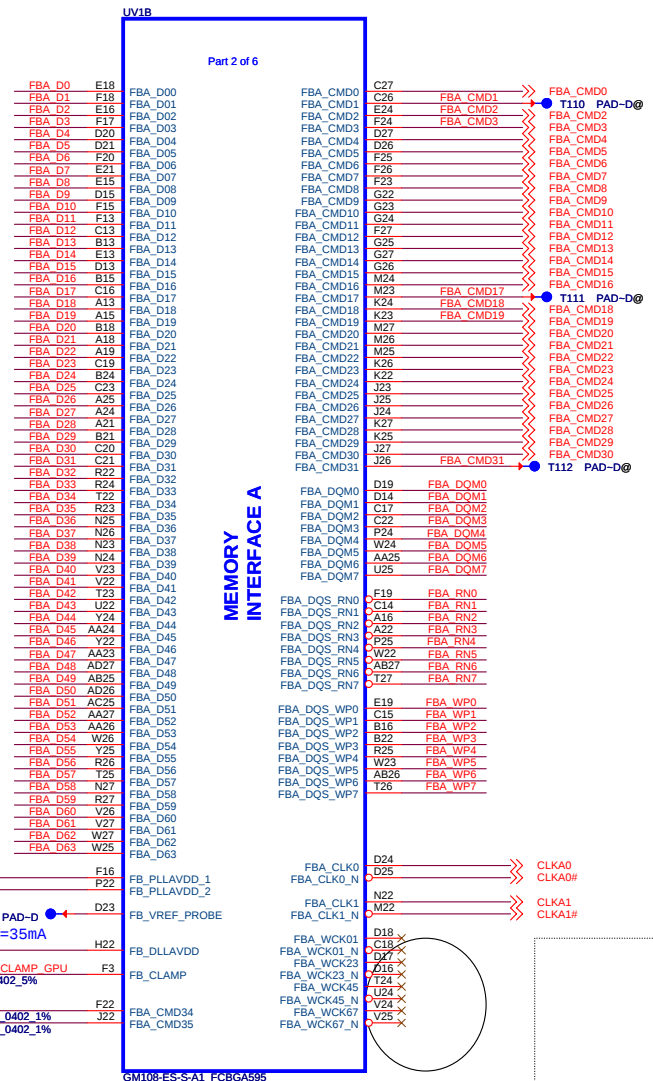
GDDR3L CMD Mapping Table

CMD0	CS0#	CMD32	
CMD1	ODT	CMD33	
CMD2	CKE	CMD34	
CMD3	A14	CMD35	
CMD4	RST	CMD36	A14
CMD5	A9	CMD37	RST
CMD6	A7	CMD38	A9
CMD7	A2	CMD39	A7
CMD8	A0	CMD40	A2
CMD9	A0	CMD41	A0
CMD10	A4	CMD42	A4
CMD11	A1	CMD43	A1
CMD12	BA0	CMD44	BA0
CMD13	WE#	CMD45	WE#
CMD14		CMD46	
CMD15	CAS#	CMD47	CAS#
CMD16		CMD48	CS0#
CMD17		CMD49	
CMD18		CMD50	ODT
CMD19		CMD51	CKE
CMD20	A13	CMD52	A13
CMD21	A8	CMD53	A8
CMD22	A6	CMD54	A6
CMD23	A11	CMD55	A11
CMD24	A5	CMD56	A5
CMD25	A3	CMD57	A3
CMD26	BA2	CMD58	BA2
CMD27	BA1	CMD59	BA1
CMD28	A12	CMD60	A12
CMD29	A10	CMD61	A10
CMD30	RAS#	CMD62	RAS#
CMD31		CMD63	



FBx PLL AVDD and FB DLL AVDD
Combi ned
Capaci t or Type Popul at ion

0.1uF 0402	2
22uF 0805	1
Bead 30 ohm (ESR=0.01 ohm) 0603	1



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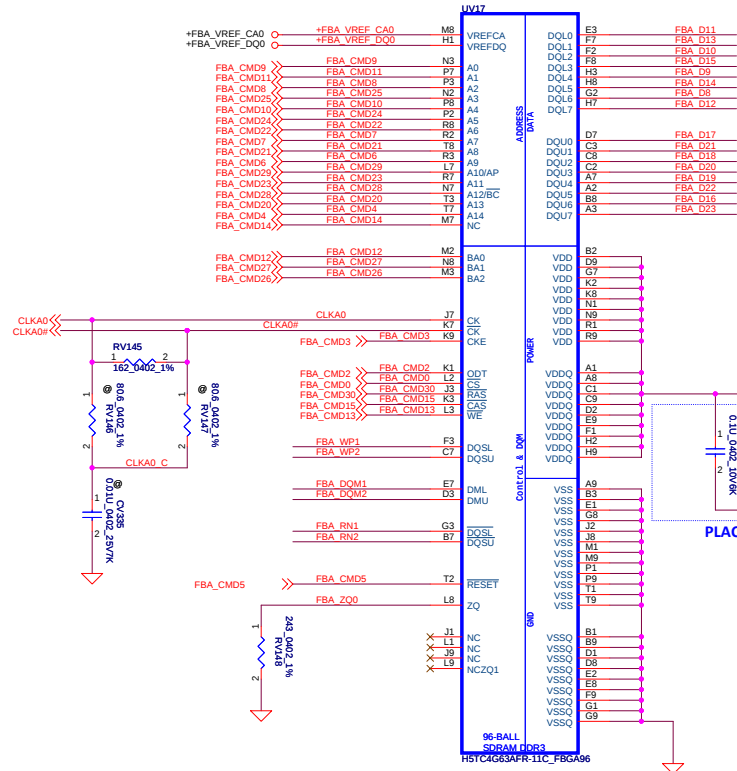
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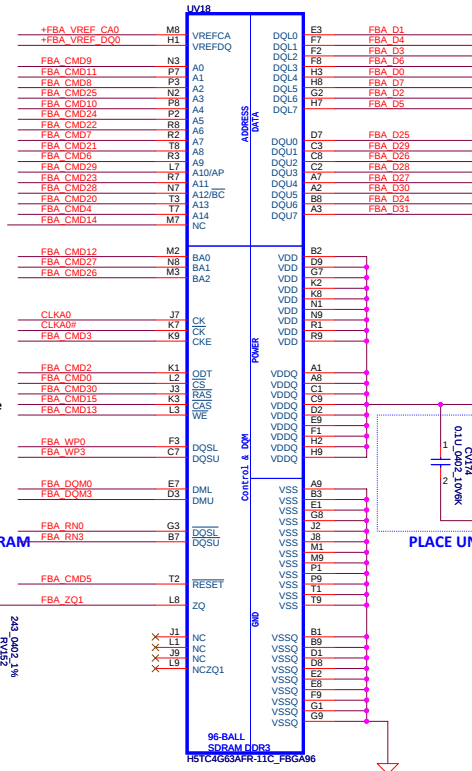
Memory Partition A - Upper 16 bits

256x16 DDR3L

FBA_D[0..31] <<> FBA_D[0..31]
FBA_WP[0..3] <<> FBA_WP[0..3]
FBA_DQM[0..3] <<> FBA_DQM[0..3]
FBA_RN[0..3] <<> FBA_RN[0..3]

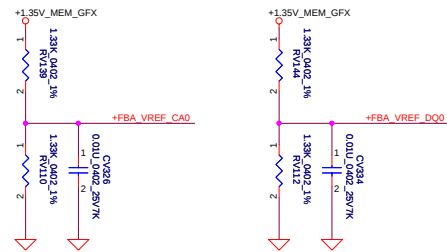


SA00006E800 Link done



SA00006E800 Link done

DDR3 per Memory FBVDD/Q Decoupling		
FBVDD/Q Combined		
Capacitor Type	Population	
0.1uF 0402	2	
1.0uF 0603	4	
10uF 0805	0	



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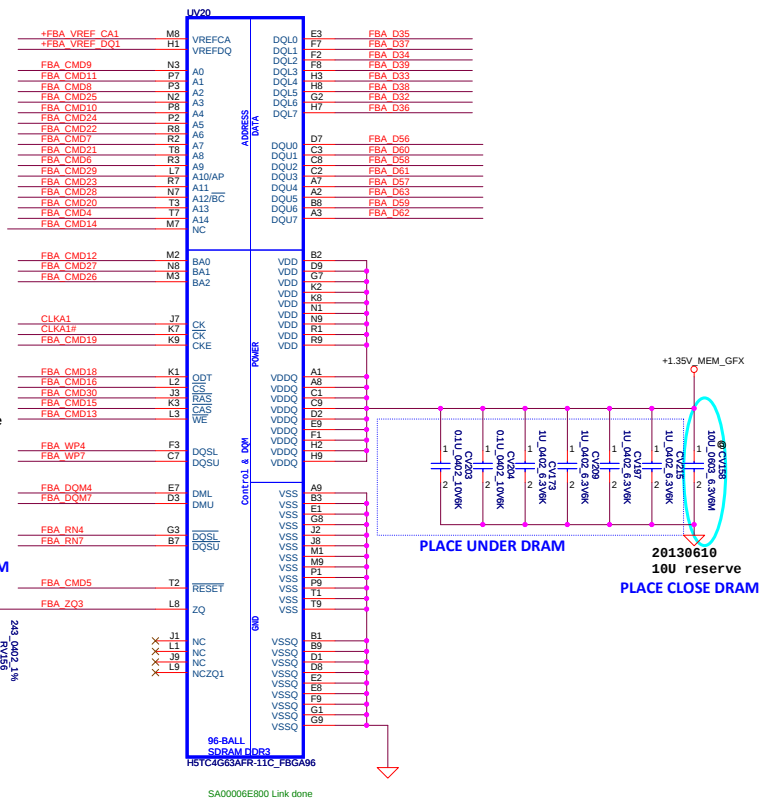
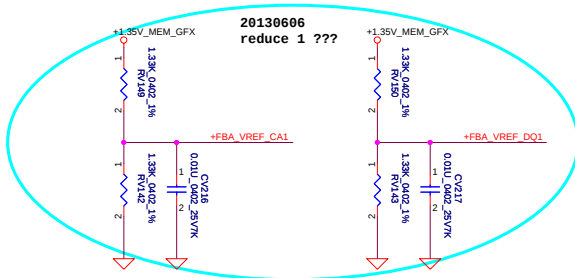
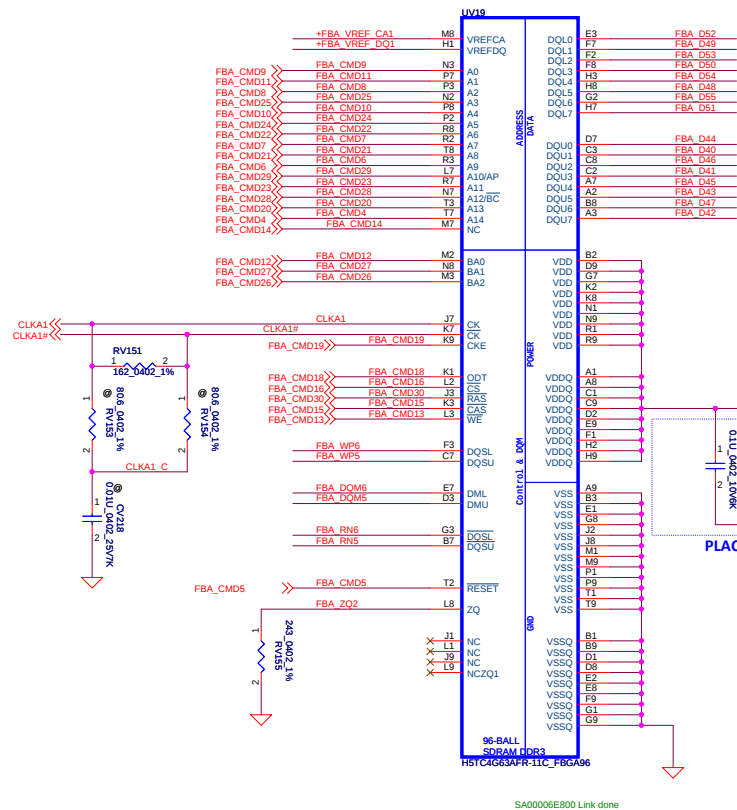
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Memory Partition A - Lower 16 bits

256x16 DDR3L

FBA_D[32..63] <<>> FBA_D[32..63]
FBA_WP[4..7] <<>> FBA_WP[4..7]
FBA_DQM[4..7] <<>> FBA_DQM[4..7]
FBA_RN[4..7] <<>> FBA_RN[4..7]

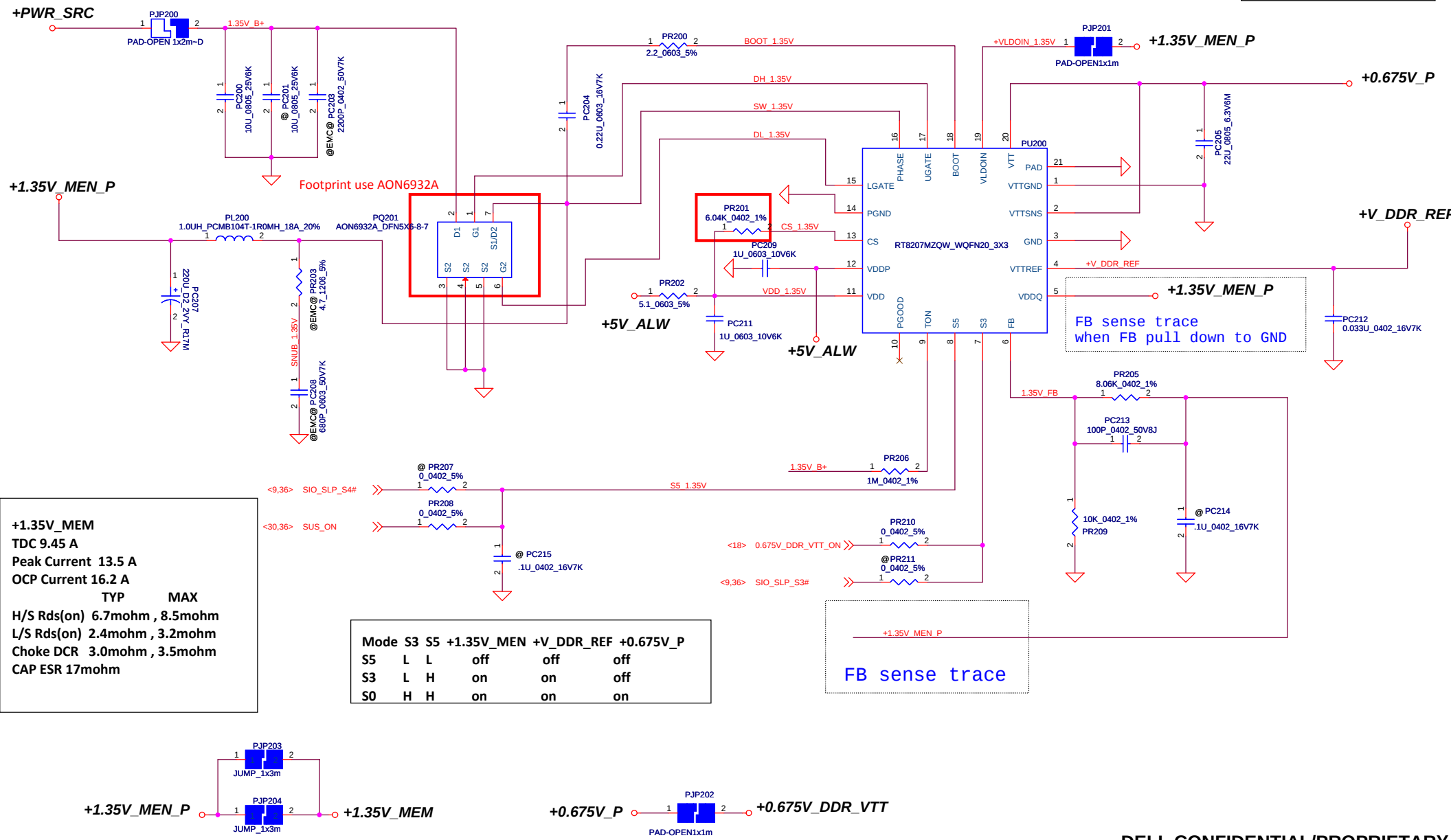


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0.675Volt +/- 5%
TDC 0.7 A
Peak Current 1.0 A
OCP Current 1.2 A



+1.35V_MEM
TDC 9.45 A
Peak Current 13.5 A
OCP Current 16.2 A

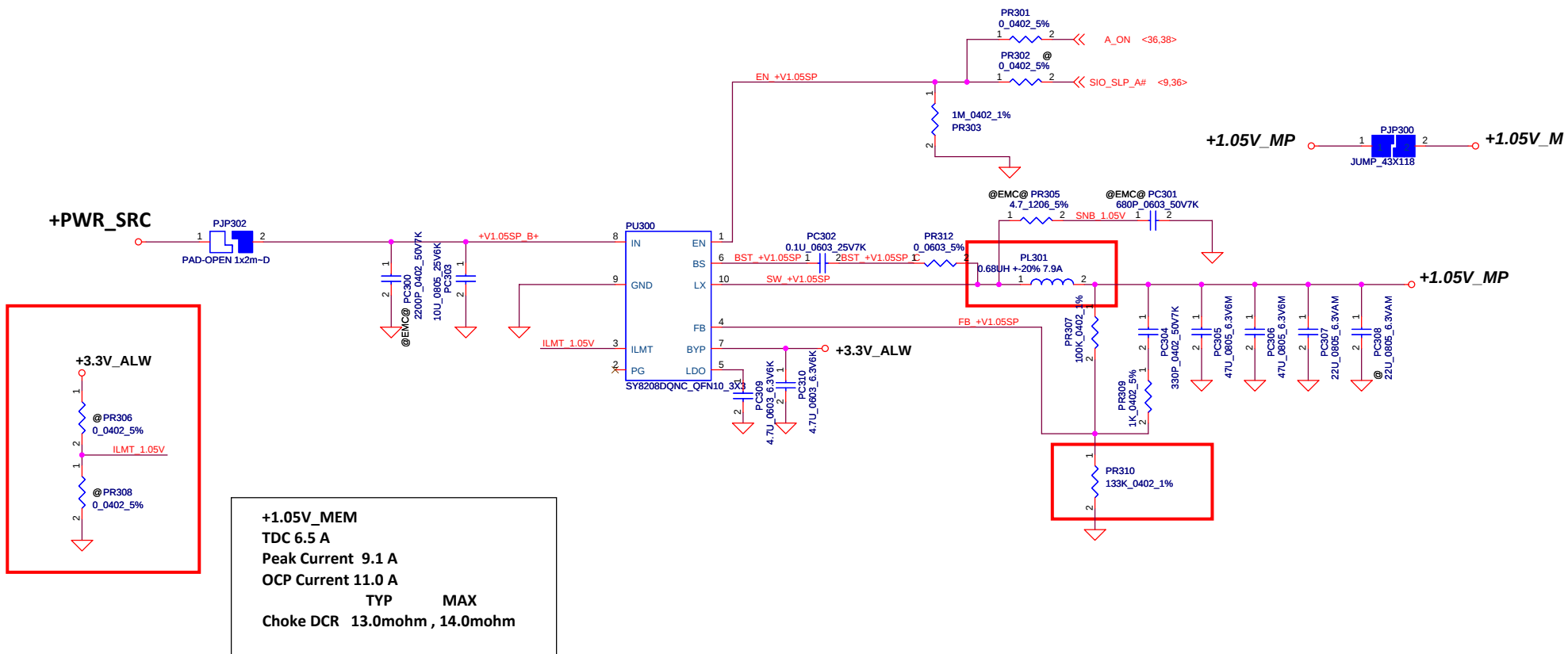
	TYP	MAX
H/S Rds(on)	6.7mohm	8.5mohm
L/S Rds(on)	2.4mohm	3.2mohm
Choke DCR	3.0mohm	3.5mohm
CAP ESR	17mohm	

Mode	S3	S5	+1.35V_MEN	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off
S0	H	H	on	on	on

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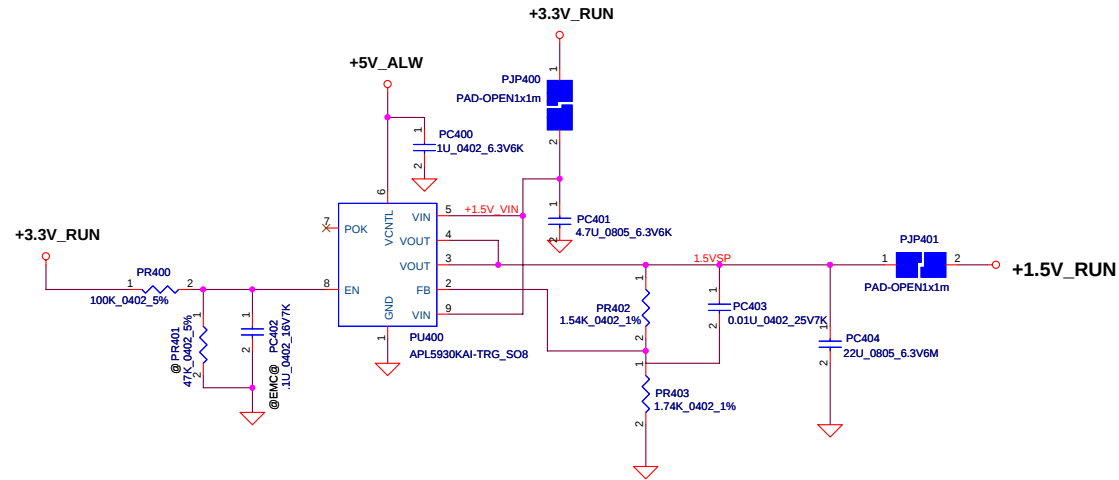
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+1.5V_RUN
TDC 0.47 A
Peak Current 0.67 A

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Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
 Rt=Rrefad // (Rboot+Rref2)
 $V_{min} = V_{vref} * [Rref2 / (Rref2 + Rboot)] * [Rt / (Rref1 + Rt)]$
 $V_{max} = V_{vref} * Rref2 / [(Rref1 / Rrefad) + Rboot + Rref2]$
 $V_{out} = V_{min} + N * V_{step}$
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

PWM-VID Spec and component Values

PWM-VID Spec	Config A	Config B	Config C
Vmin	0.6V	0.6V	0.65V
Vmax	1.2V	1.2V	1.15V
Vboot	0.875V	0.9V	0.9V
Voltage step	6.25mV	6.25mV	25mV
N of Voltage level	96	96	20
Rrefad	PR9 39K	20K	39K
Rref1	PR5 39K	20K	30K
Rboot	PR8 1.5K	2K	3K
	PR10 30K	18K	24K
Rref2=PR10+PR12	PR12 1.5K	0	3K
C	PC8 1.5nf	2.7nf	1.8nf

Module model information:
 RT8813A_V1A for IC module
 RT8813A_V1B for SW module

Current Limit threshold setting
 $R_{ocset} = (I_{valley} * R_{ds(on)} + 40 \text{ mV}) / 10 \mu\text{A}$

ripple=(19-0.9)*0.9/
 (304.89KHz*0.36u*19)=7.811A

OCp=54A/2=27A per phase
 $I_{valley}=27A-7.811A/2=23.1A$

H-side MOS:TPCA8065
 Rds(on):
 11.7mohm@Vgs=10V
 9.4mohm@Vgs=4.5V
 Id:16A@Ta=25 degC

L-side MOS:TPCA8057
 Rds(on):
 2.0mohm@Vgs=10V
 2.6-3.2mohm@Vgs=4.5V
 Id:42A@Ta=25 degC

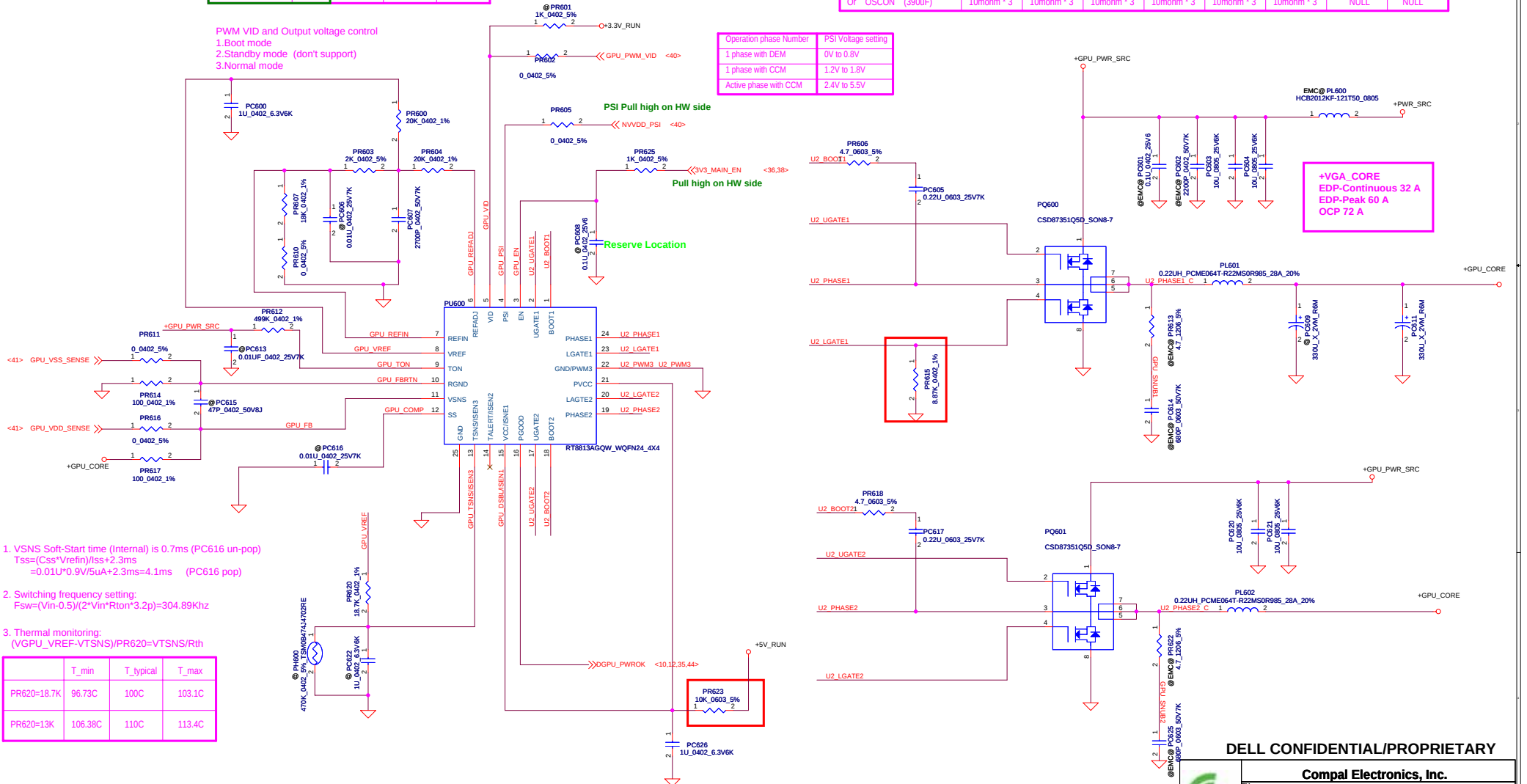
Choke: 0.36uH (Size:10*10*4)
 Rdc=1.1mohm +-5%
 Heat Rating Current=30A
 Saturation Current=50A

C=3*330uF (9mohm)=990uF
 $V_{ripple} = \text{ripple} * \text{ESR}(\text{min}) = 7.811A * 3\text{mohm} = 23.4\text{mV}$

Different VGA Chip (different EDP-Peak Current) need select different solution

VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B
Rated TDP Power at Tj=102C	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W
Boosted GPU Total at Tj=102C	25W	32W	25W	20W	23W	N/A	30W	40W
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A	60A	75A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A
OCp Setting Current	42A	66A	54A	42A	42A	48A	72A	90A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL

PWM VID and Output voltage control
 1.Boot mode
 2.Standby mode (don't support)
 3.Normal mode



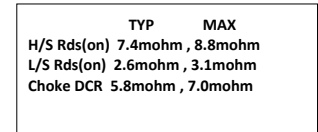
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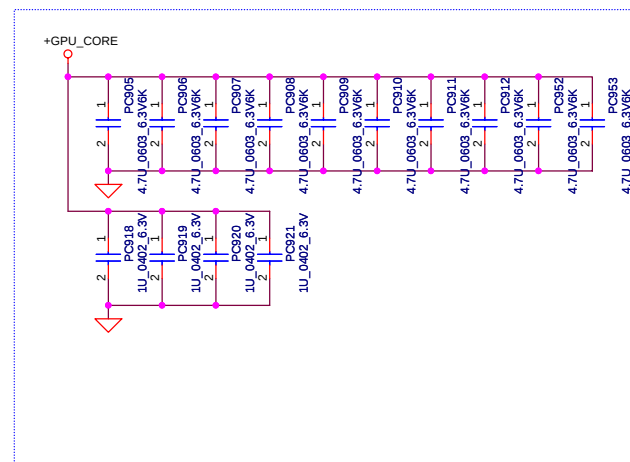
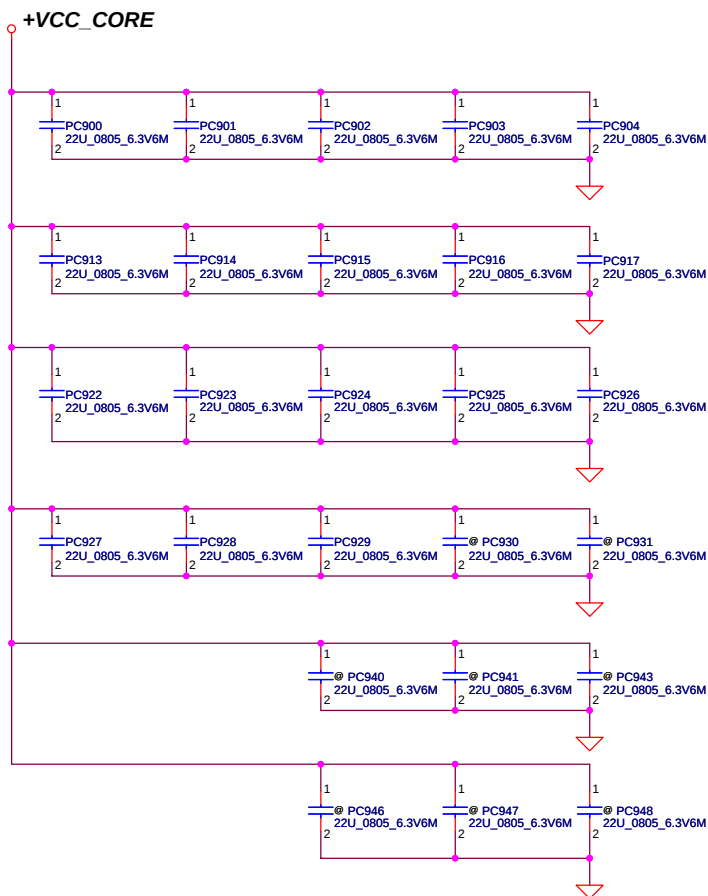
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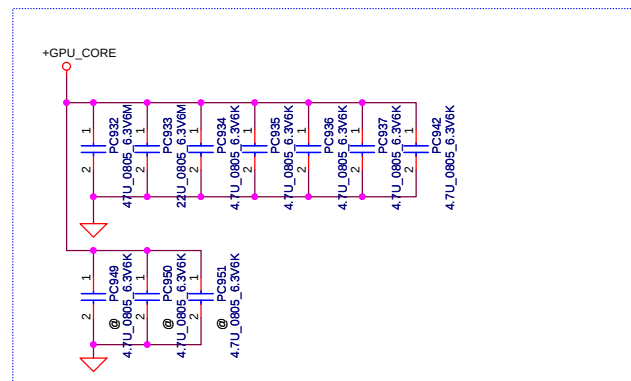
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nVidia GB4-64 package
Under GPU
4.7uF 0603 * 10
1uF 0402 * 4



nVidia GB4-64 package
Near GPU
47uF 0805 *1
22uF 0805 *1
4.7uF 0805 *5

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