

Compal Confidential

HBL50 Schematics Document

Intel Yonah Processor with 945GM/945PM + DDRII + ICH7M
(With nVIDIA NB7M-SE)

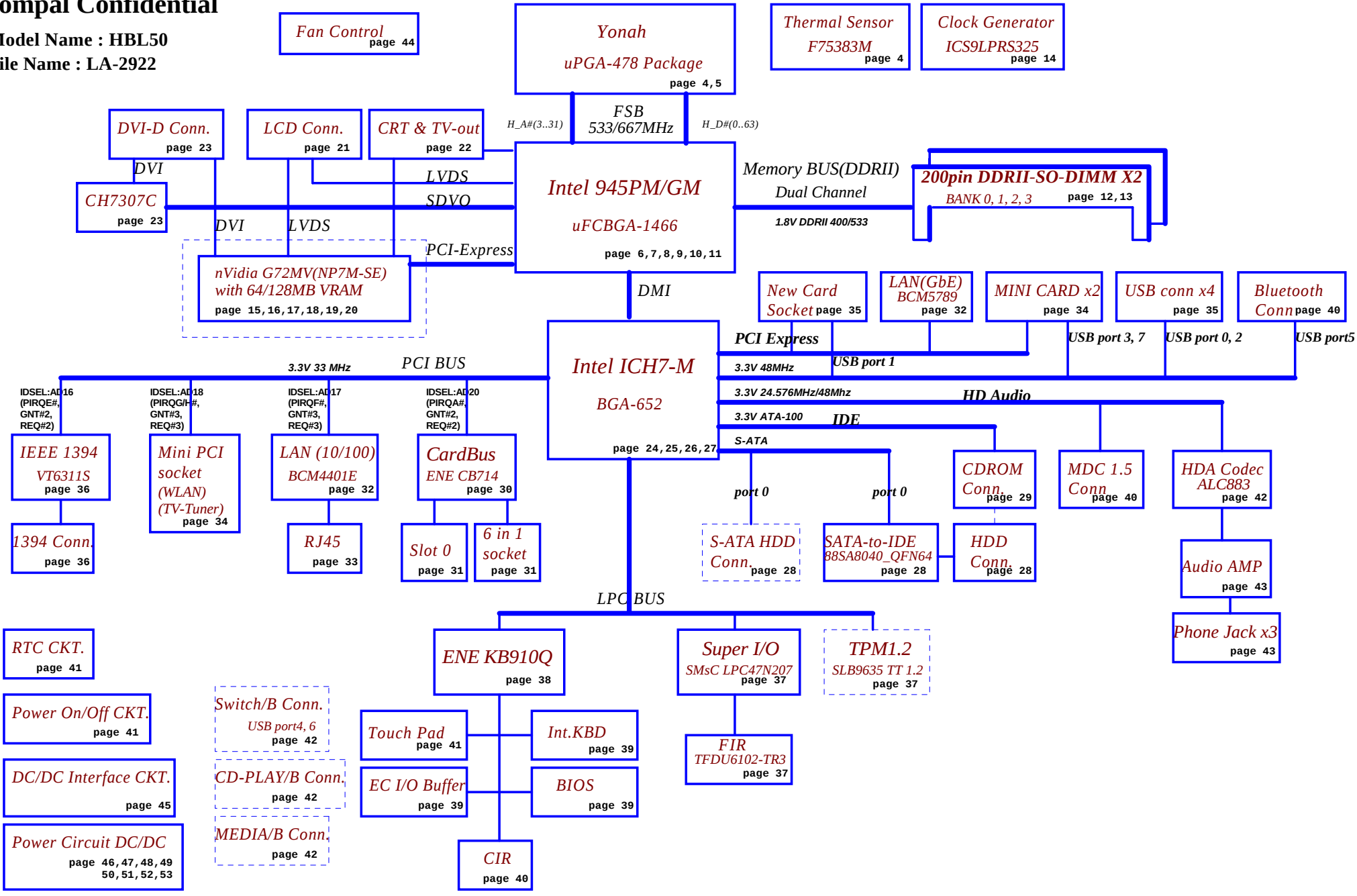
2006-09-05

REV: 1.0

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Model Name : HBL50
File Name : LA-2922



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

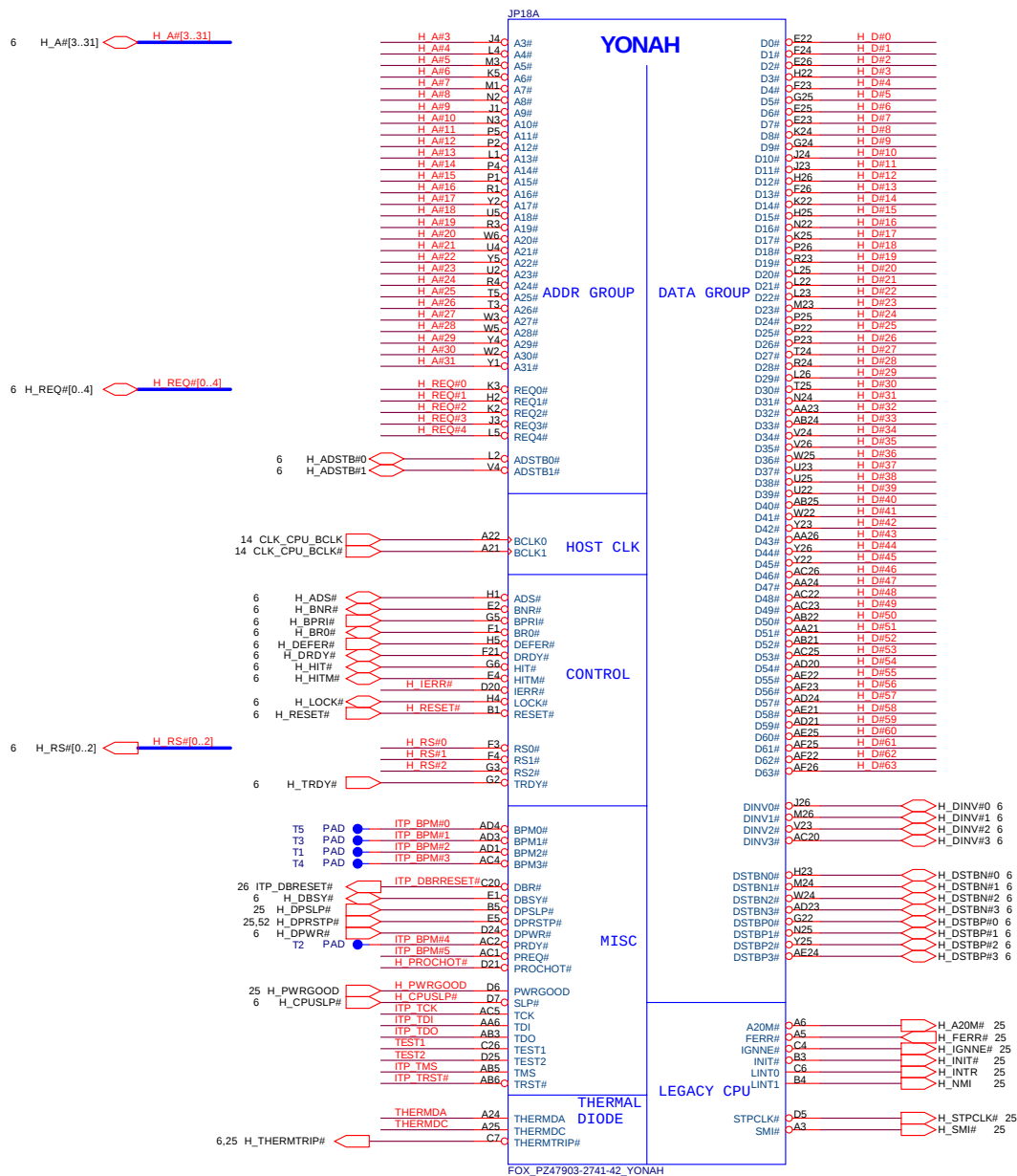
BTO Item	BOM Structure
VGA	PM@ + VGA@
UMA	GM@
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI_CARD1	MINI1@
MINI_CARD2	MINI2@
SATA-to-IDE	8040@
PATA	PATA@
GRAPEVINE	GRA@
G72MV Only	G72@
G73 Only	G73@
VRAM	X76@
VRAM 64M	64@
VRAM 128M	64@+128@
VRAM 256M	64@+128@+256@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
Sub-woofer	SUB@
5789&5787	8789@
4401&5789	0189@
VP1020	VP1020@
INTERNAL MIC	INTMIC@
1394	1394@
SATA HDD	SATA@
DVI	DVI@
CardReader	4IN1@
New Card	EXP@

SKU ID Table

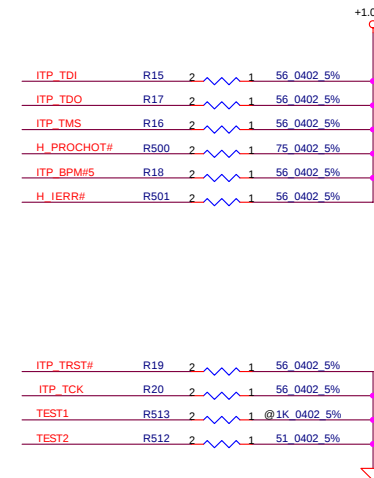
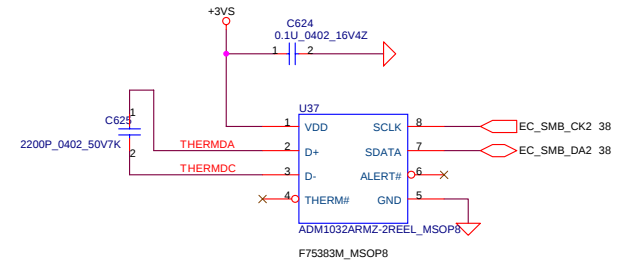
SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

G72MV	G72MV@
	G72MV64@
	G72MV128@
G72MZ	G72MZ@
G73	G73M128@

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H_D# [0..63] H_D# [0..63] 6

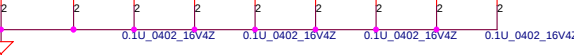
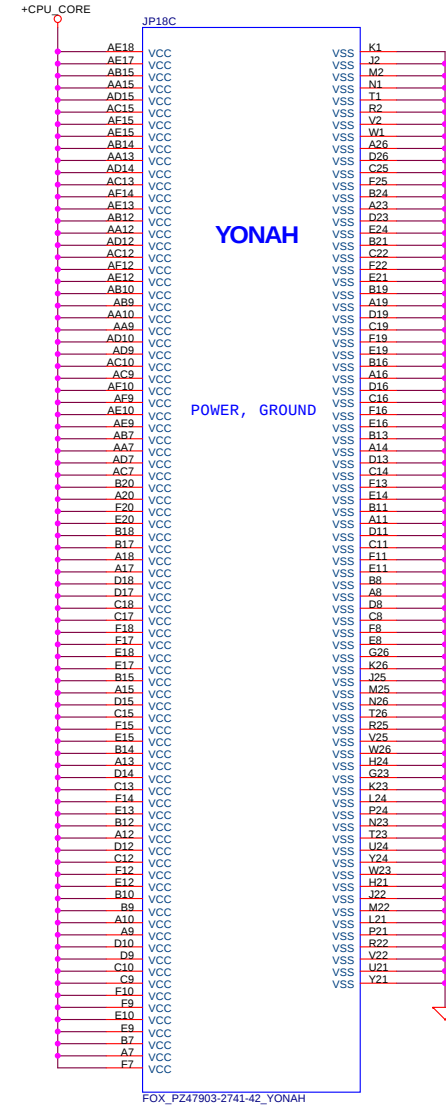
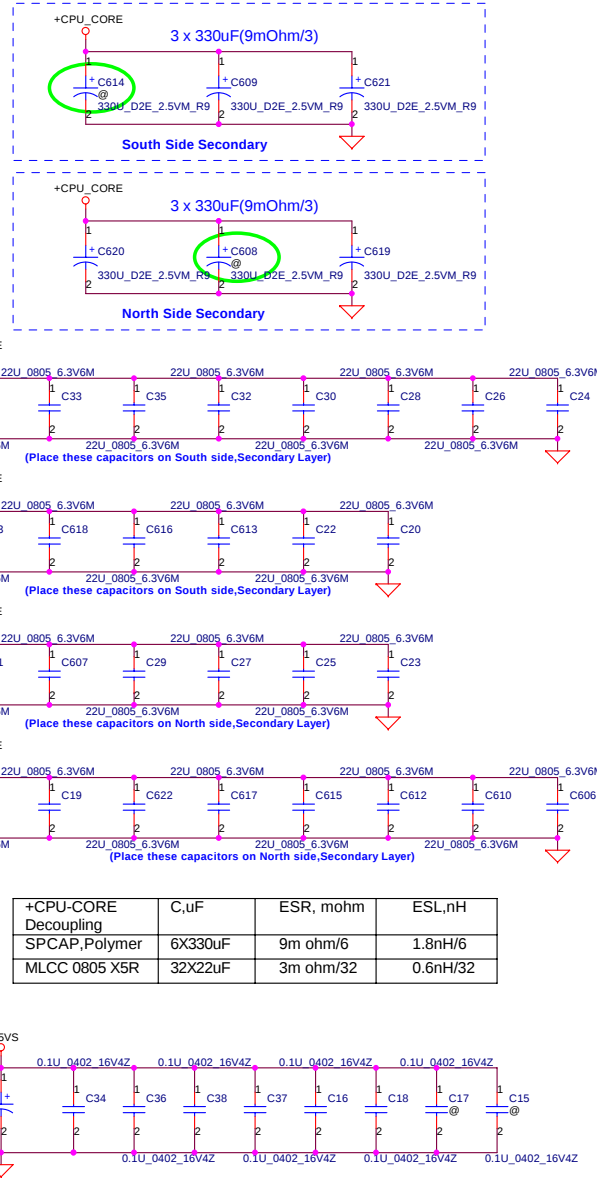
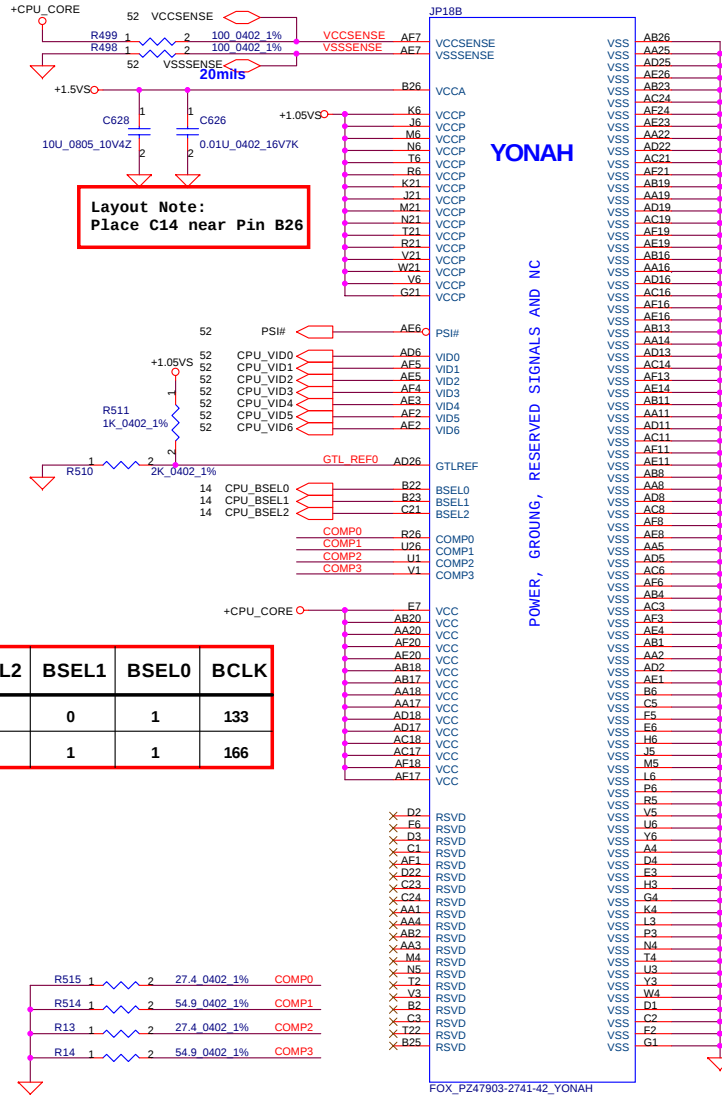


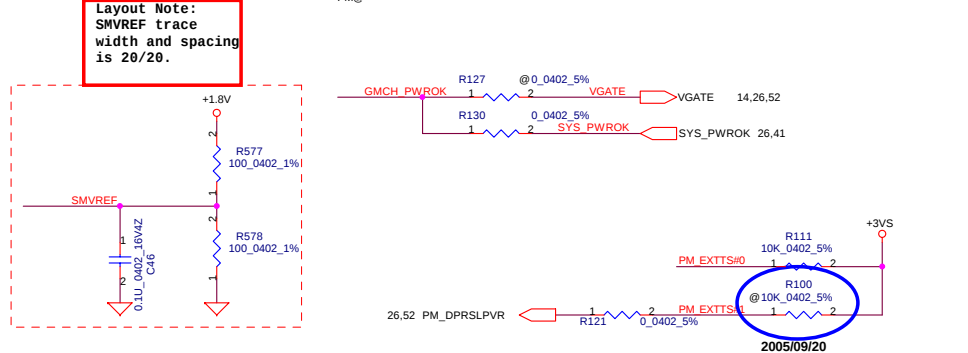
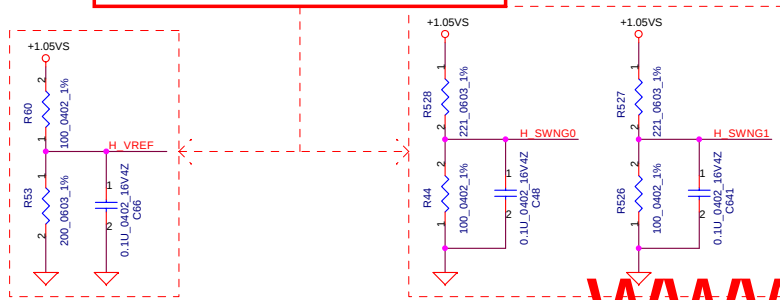
Layout Note:
THERMDA & THERMDC Trace / Space = 10 / 10 mil

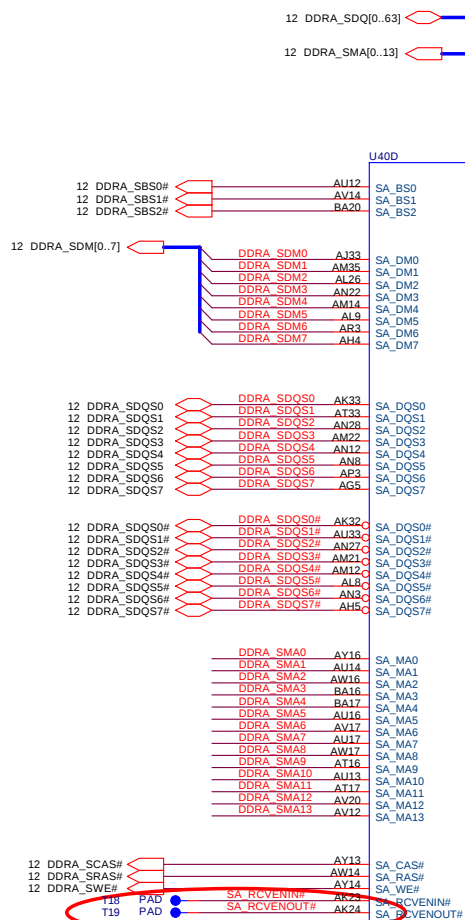
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Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.40hms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.





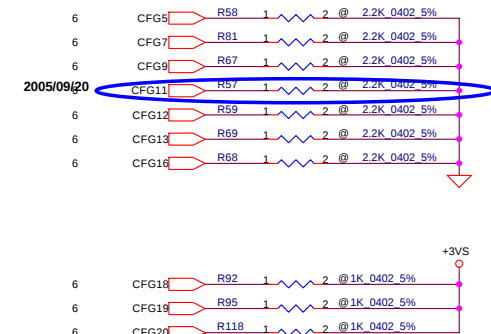
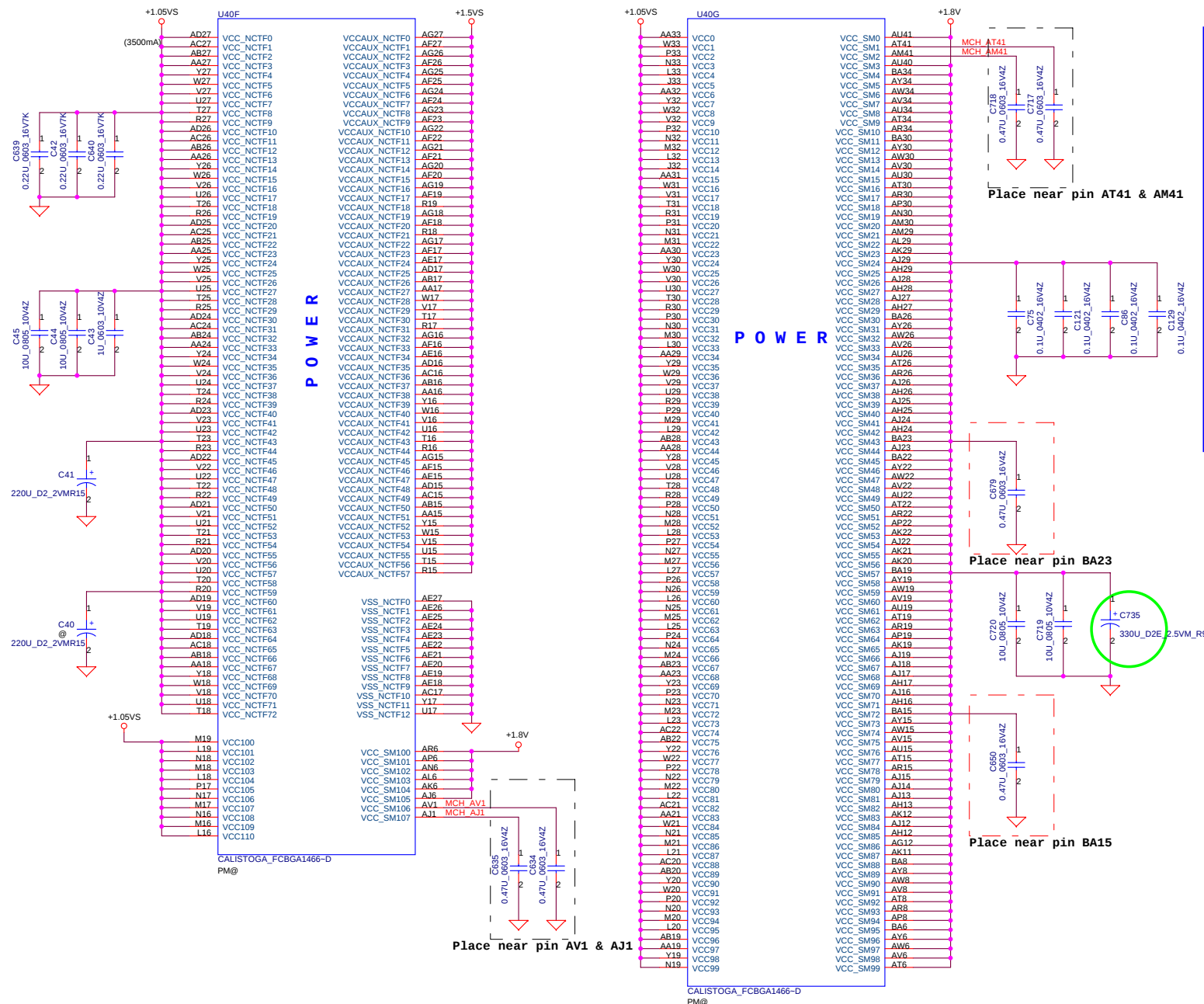


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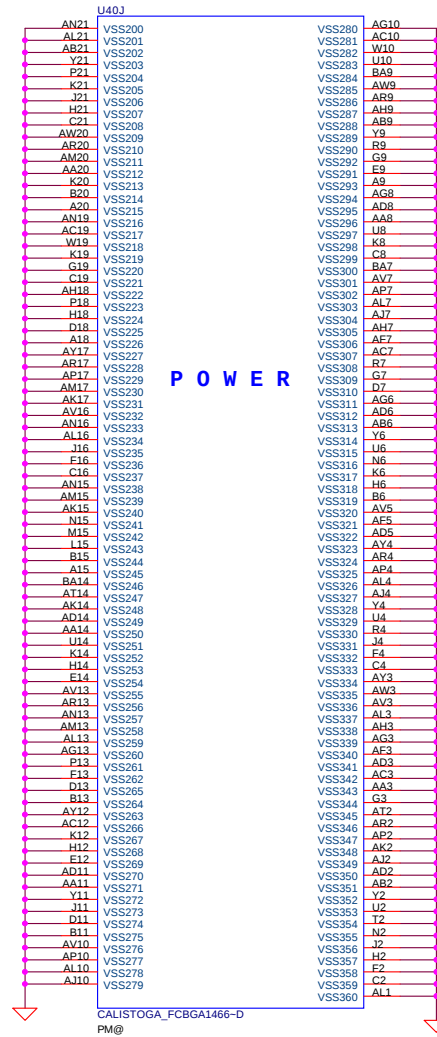
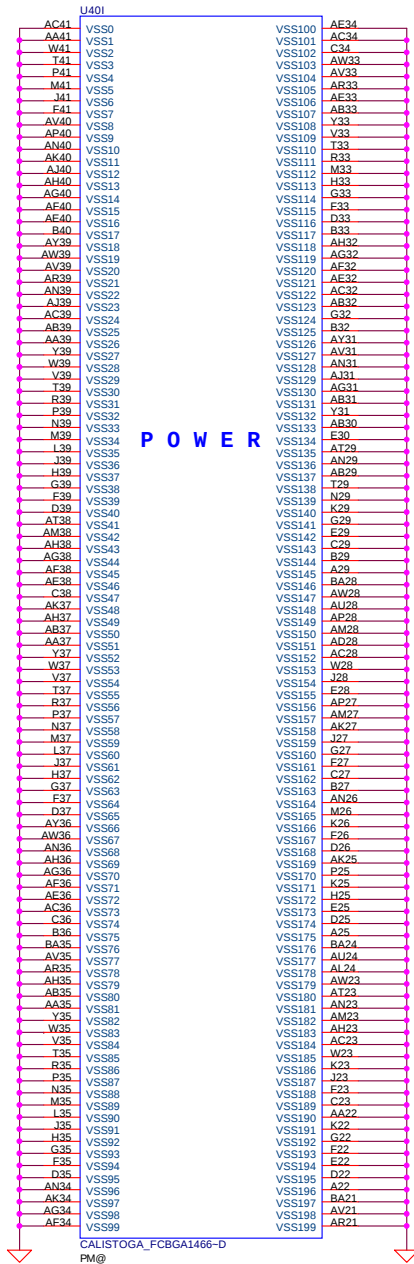
Strap Pin Table

CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

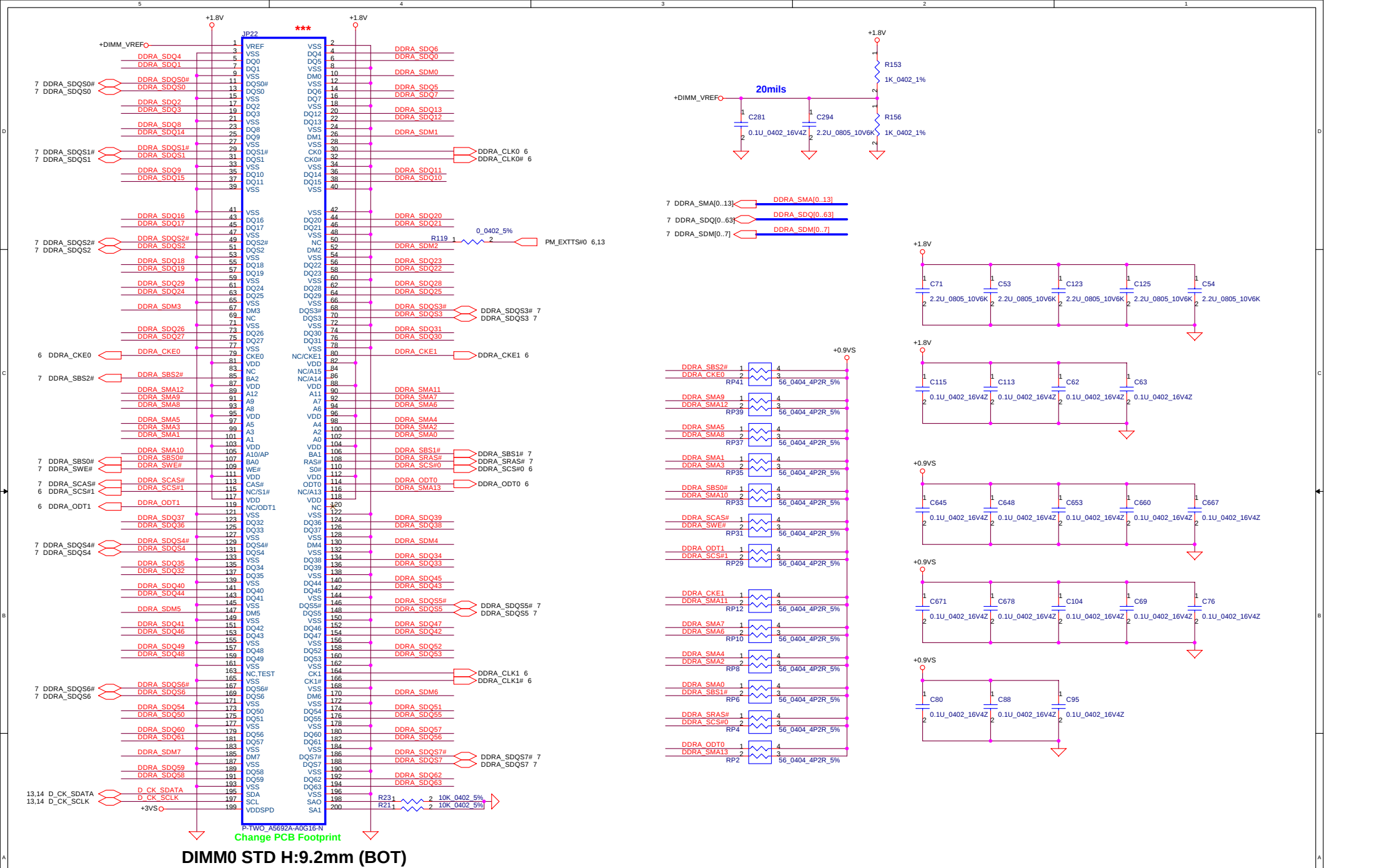
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG11	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.95V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



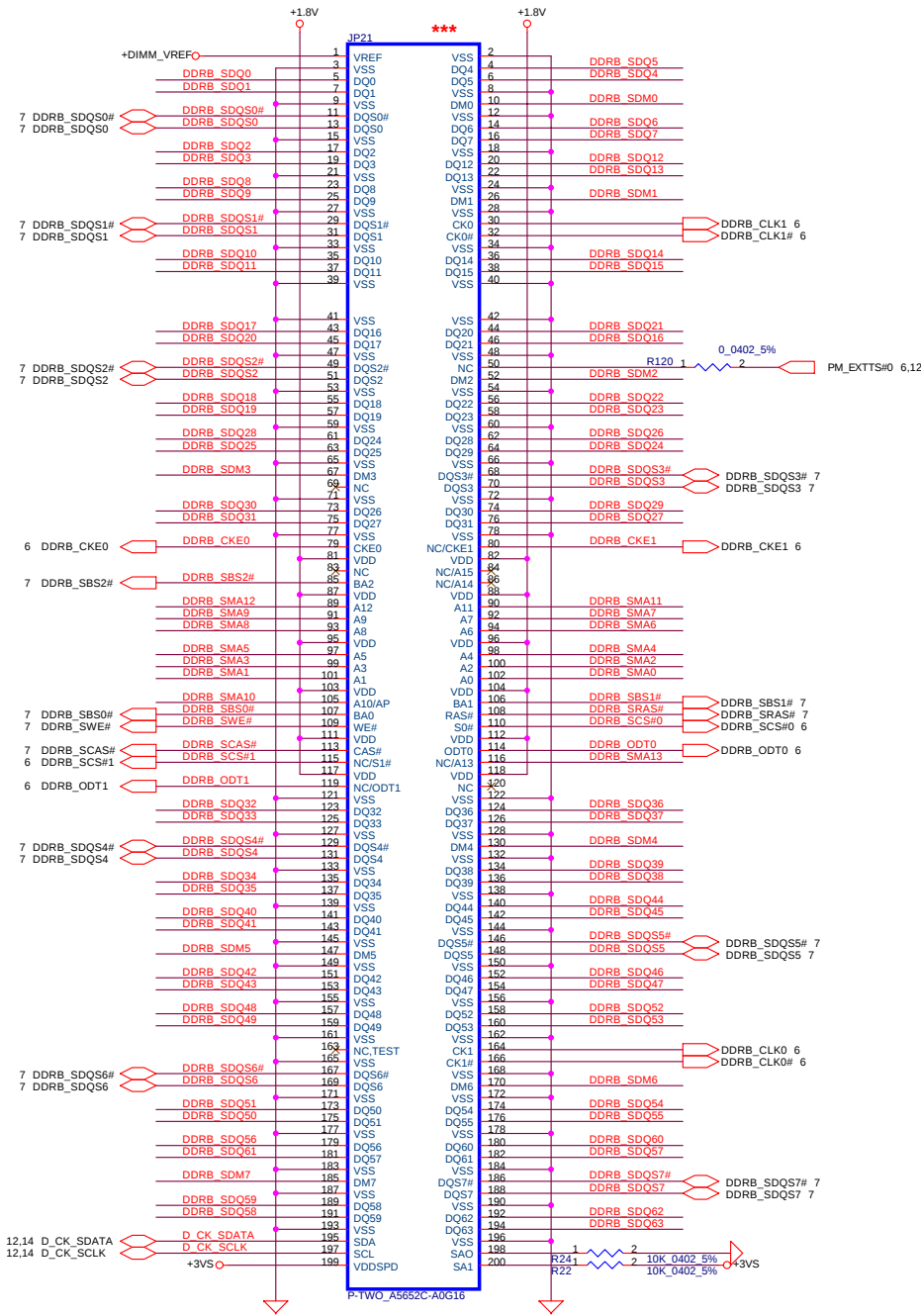
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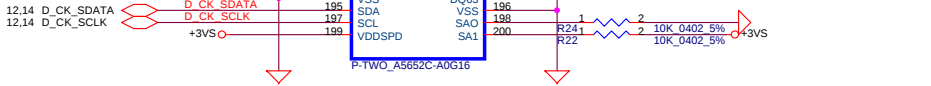
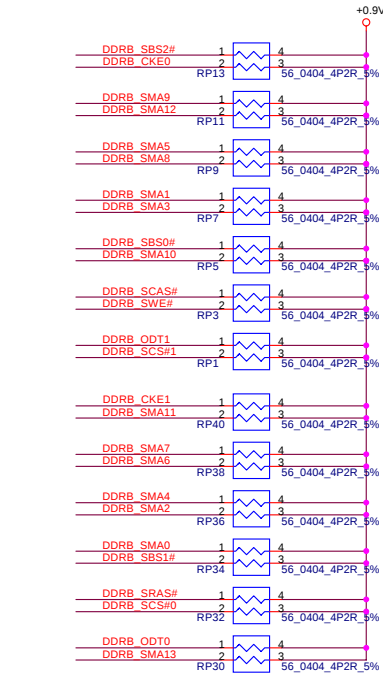
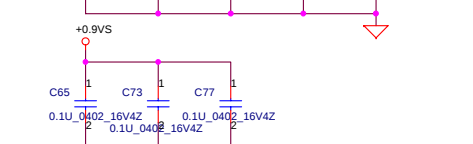
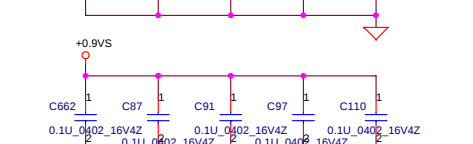
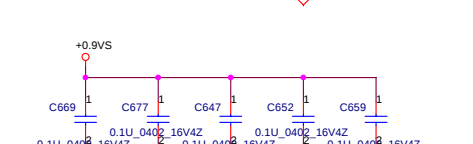
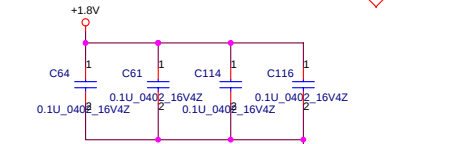
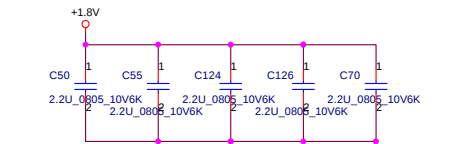
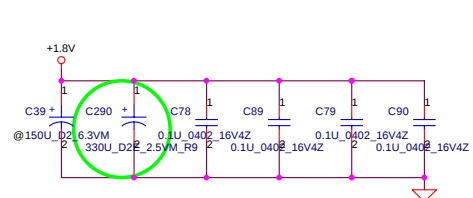
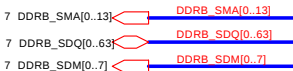
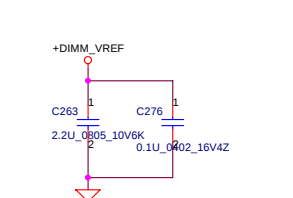
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DIMM1 STD H:5.2mm (BOT)



FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

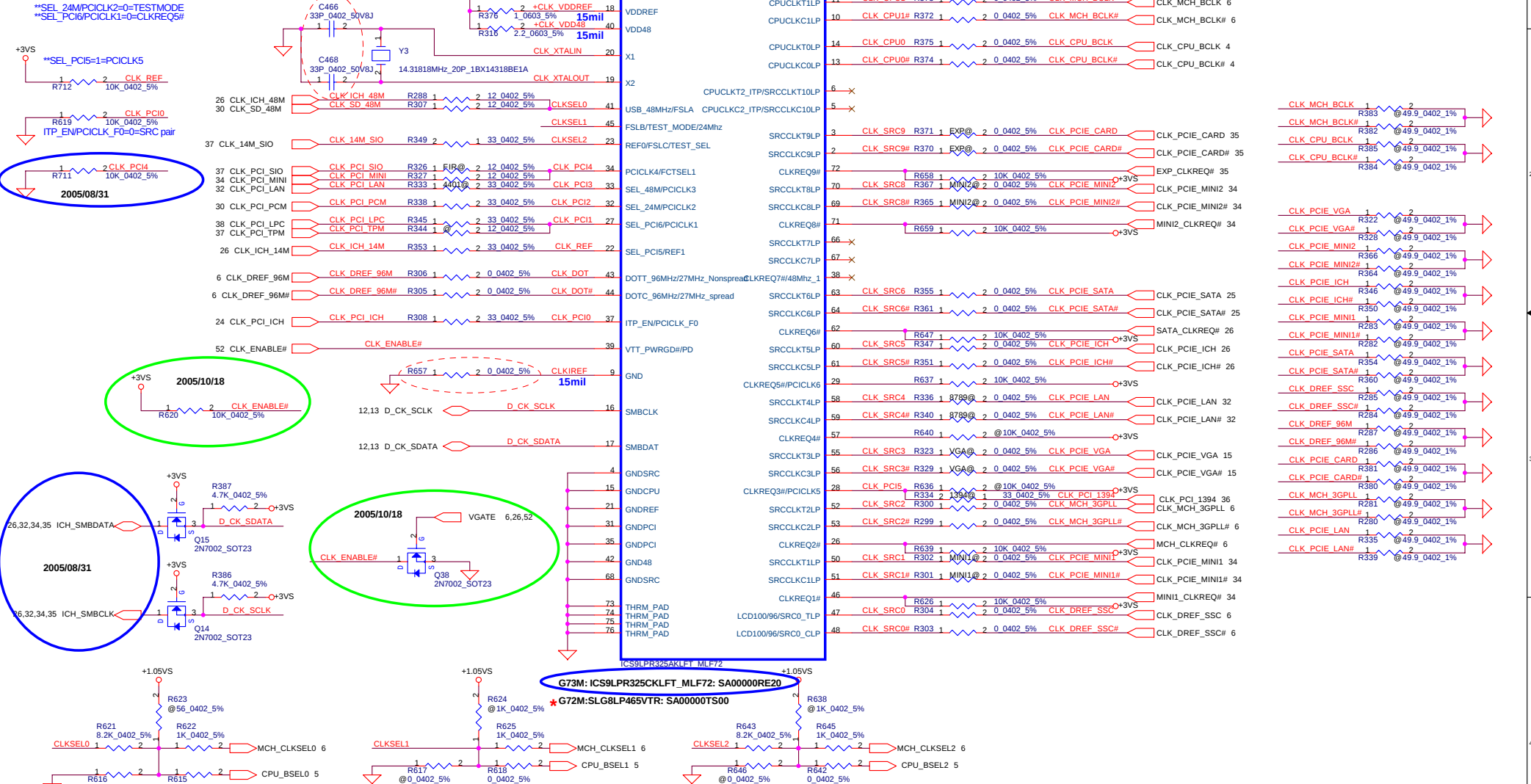
Table : ICS9LPR325

	0	1
**SEL_PCI5/REF1	CLKREQ3#	33.3MHz PCICLK5
**SEL_PCI6/PCICLK1	CLKREQ5#	33.3MHz PCICLK6
**SEL_24M/PCICLK2	TESTMODE	24MHz Output
**SEL_48M/PCICLK3	CLKREQ7#	48MHz 1 Output
ITP_EN/PCICLK_F0	SRC pair	CPU_ITP pair

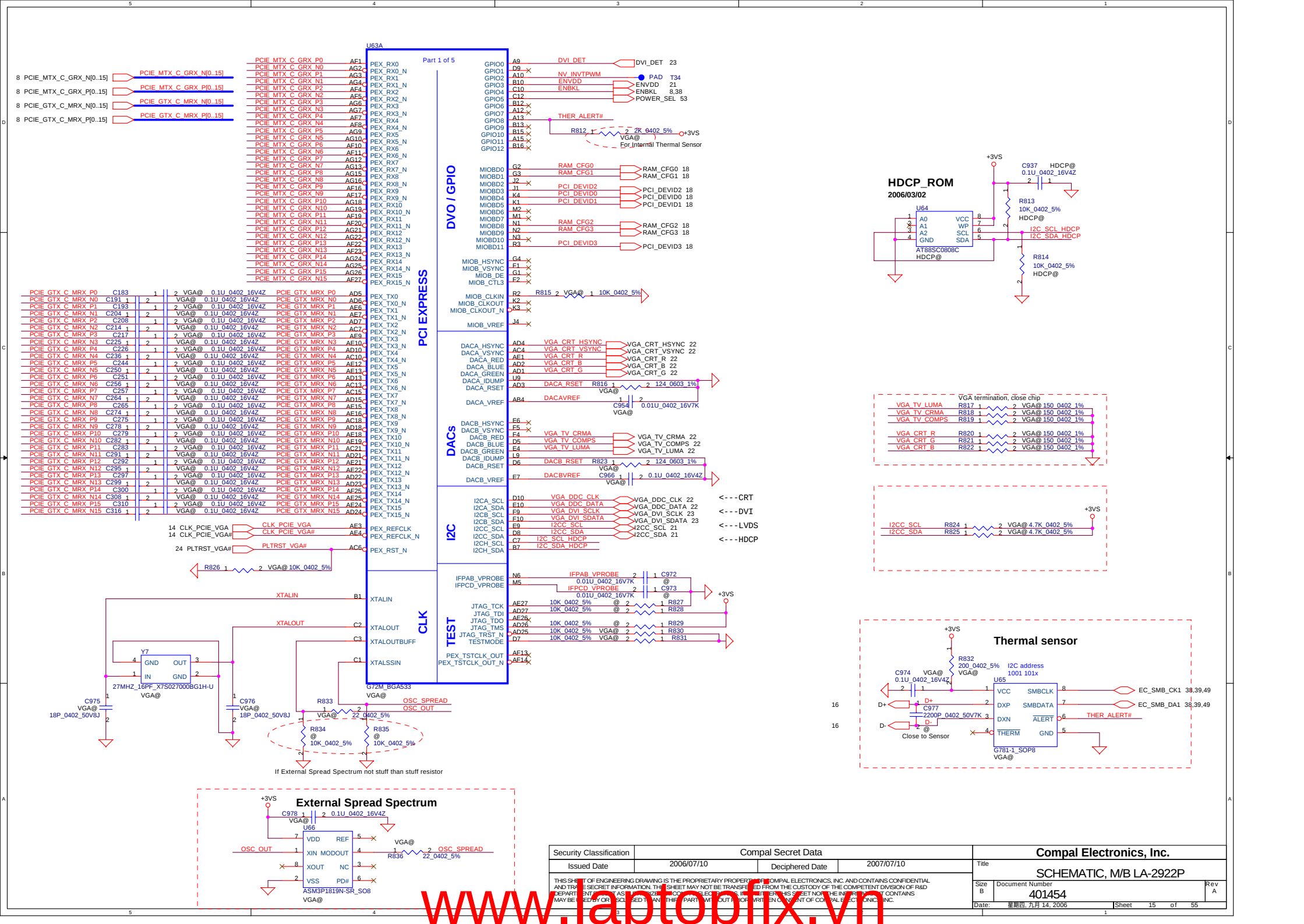
**SEL_24M/PCICLK2=0=TESTMODE
**SEL_PCI6/PCICLK1=0=CLKREQ5#

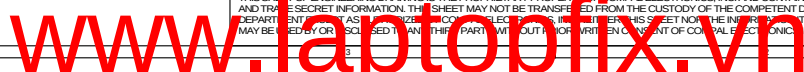
**SEL_PCI5=1=PCICLK5

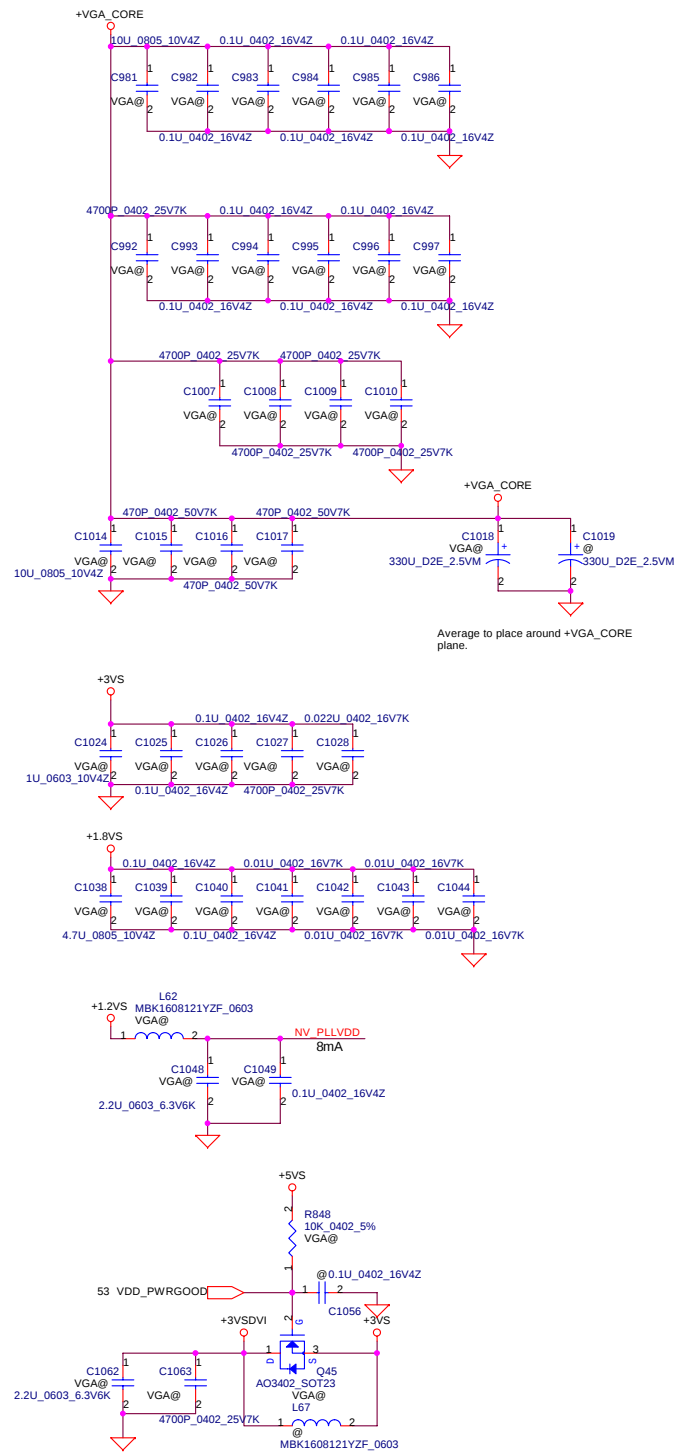
ITP_EN/PCICLK_F0=0=SRC pair



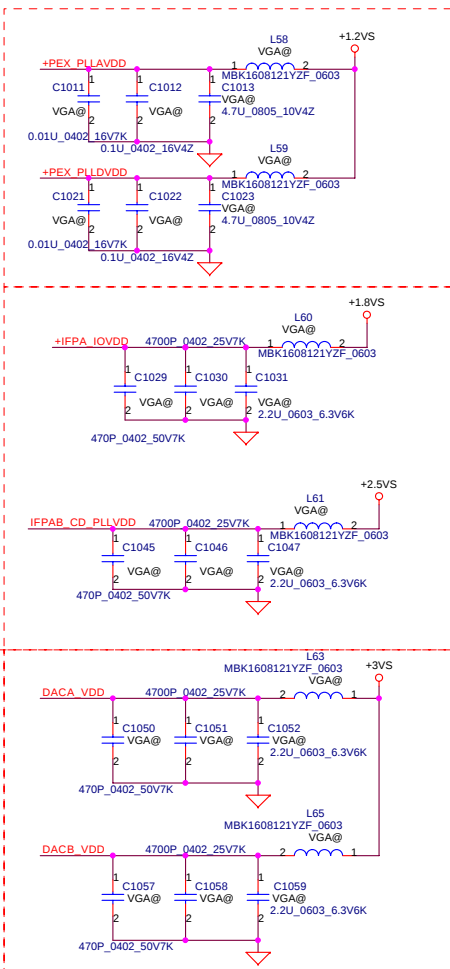
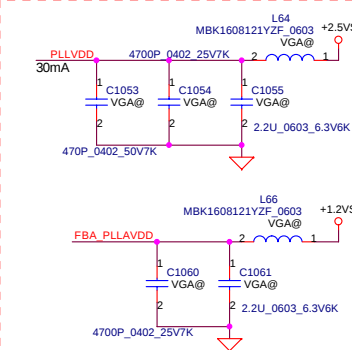
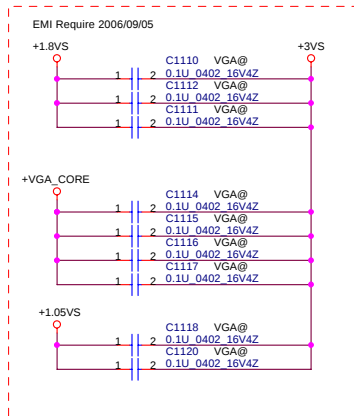
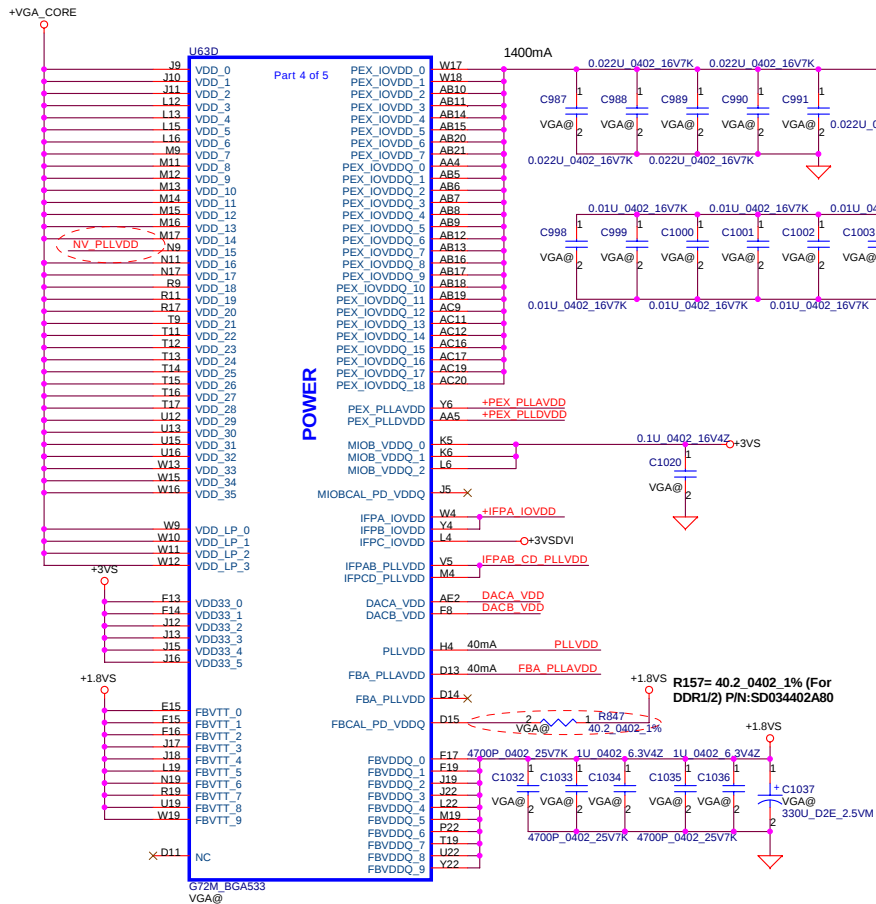
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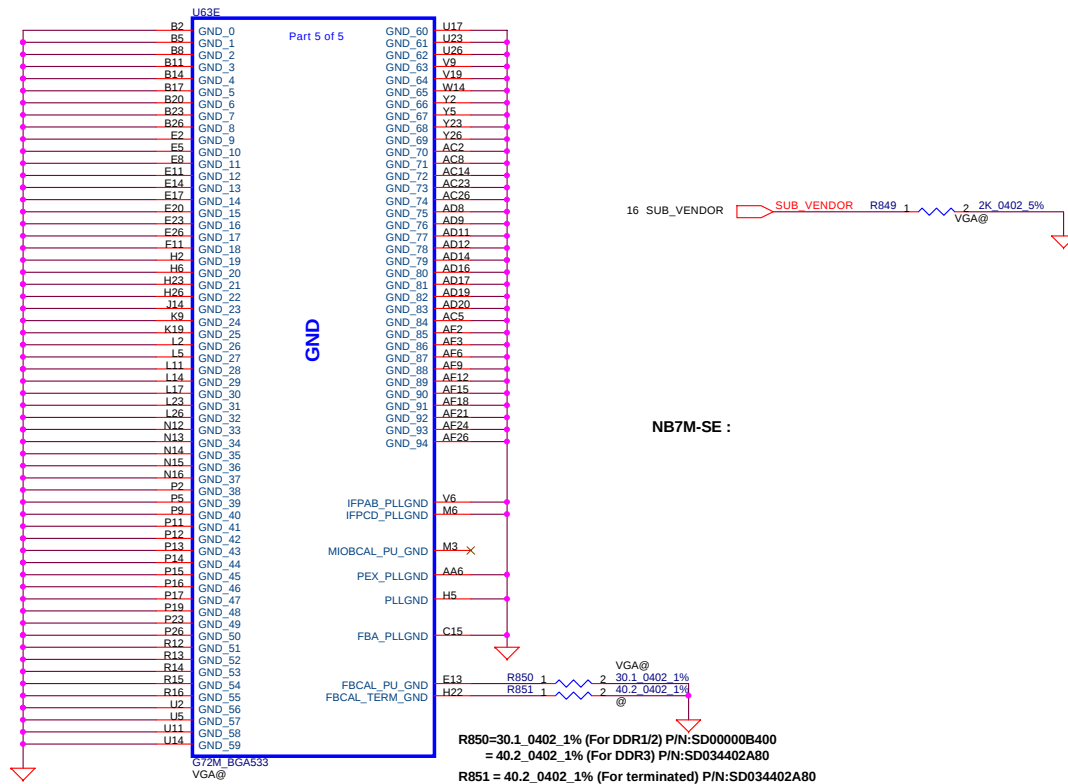




For NV43 DVI leakage issue



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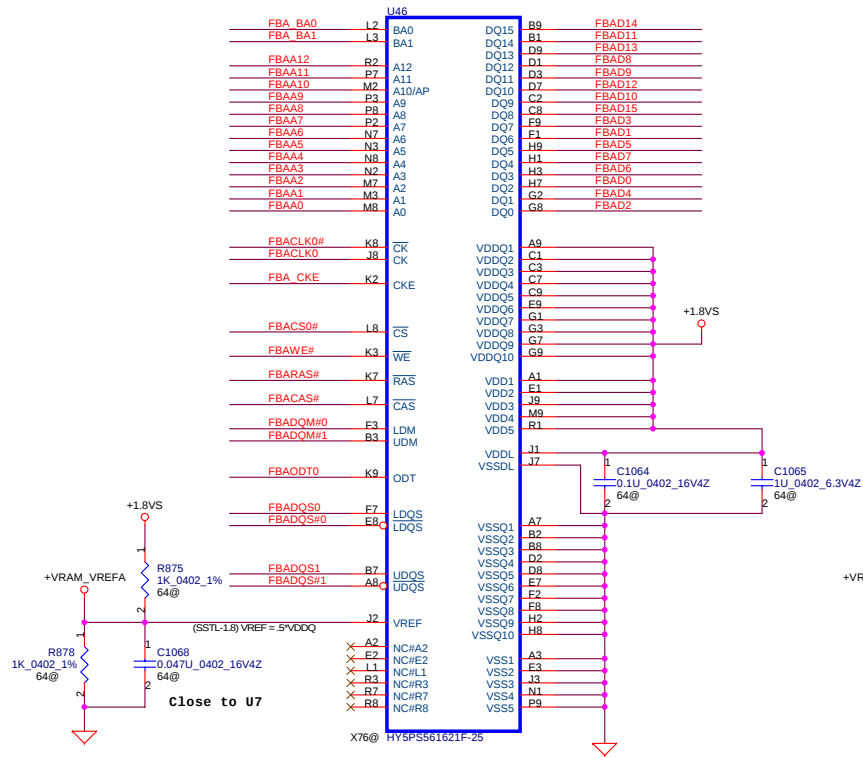
G73M		G72MV		
STRAPS	PIN	DESCRIPTION	Value	Value
SUB_VENDOR	MIOAD1	VB10S on card (pull high) VB10S with system BIOS (pull down)	0	
PEX_PLL_TERM	MIOAD0		0	
PEX_CFG[2:0]	MIOAD [9, 8, 6]	Recommended for G7x	001	
RAM_CFG[3:0]	MIOAD[5:2]	RAM_CFG[3] (Bandwidth 0=Full, 1=Half)		
		RAM_CFG[2] (0=16M or 1=32M)		
		RAM_CFG[1:0] (Manufacture) (01=Sam, 10=Inf, 11=Hyn)		
PCI_DEVID[3:0]	VIPD[5:3] MIOA_HSYNC	G73M-xxxxx8 G72M-0x01D8	1000	
		G72MV-0x01D7 TBD/TBD	0111	

- 15 RAM_CFG0
- 15 RAM_CFG1
- 15 RAM_CFG2
- 15 RAM_CFG3
- 15 RAM_CFG0
- 15 PCI_DEVID0
- 15 PCI_DEVID1
- 15 PCI_DEVID2
- 15 PCI_DEVID3
- 15 PEX_CFG0
- 16 PEX_CFG1
- 16 PEX_CFG2
- 16 PEX_PLL_TERM

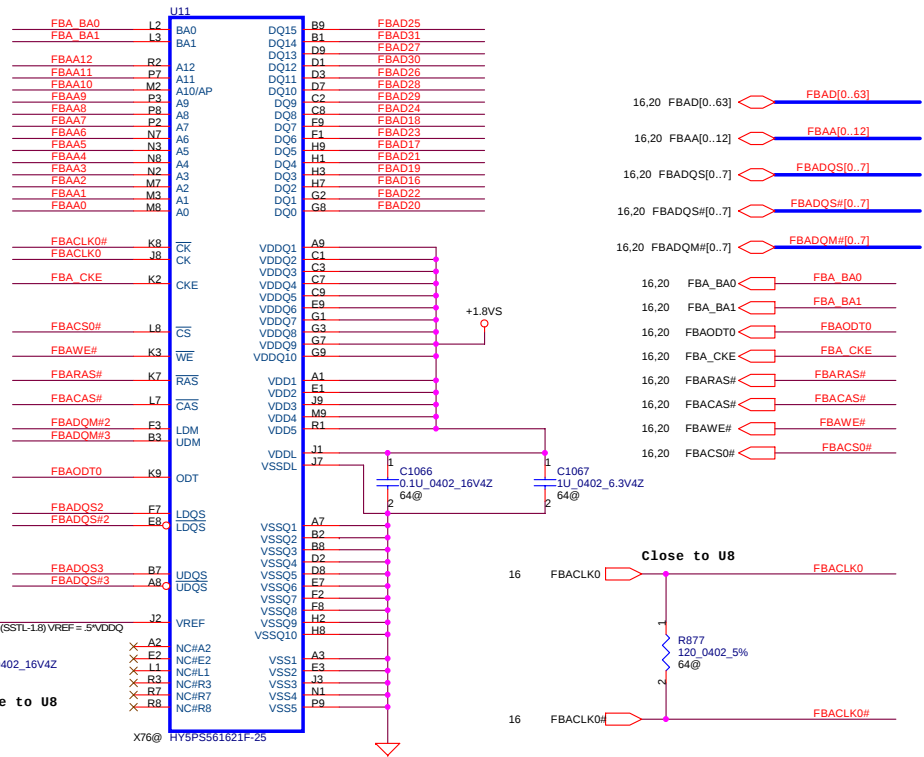
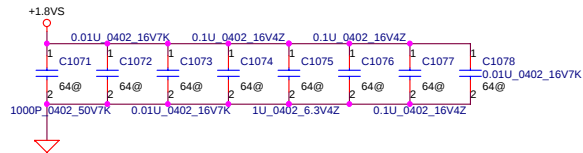
Bandwidth	RAM Type	Vendor
FULL R49	32M R51	Samsung R553, R55
HALF R48	16M R52	Hynix R539, R55
		Infineon R539, R56

Package		
(10*12.5)	Infineon GDDR2(400): SA00000S800 (HYB18T256161AF-25)	Infineon GDDR2(350): SA00000T700 (HYB18T256161AF-28)
(11*13)	Samsung GDDR2 (400): SA00000FG10 (K4N56163QF-ZC25)	Samsung GDDR2 (350): SA00000TB00 (K4N56163QF-ZC2A)
(8*13)	Hynix GDDR2 (400): SA00000FF10 (HY5PS561621AFP-25)	Hynix GDDR2 (350): SA00000TJ00 (HY5PS561621AFP-28)

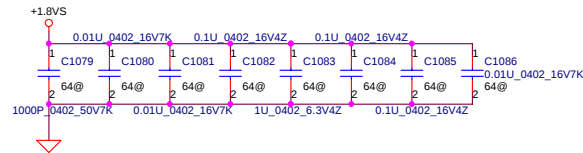
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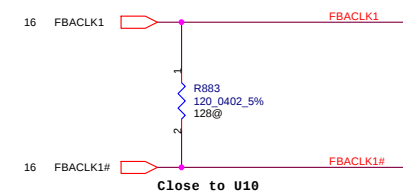
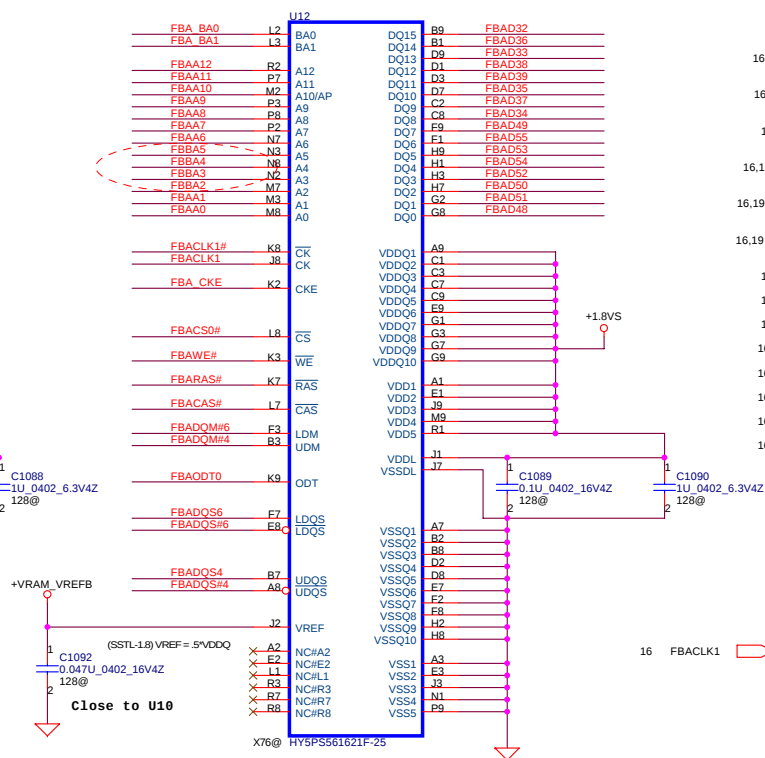


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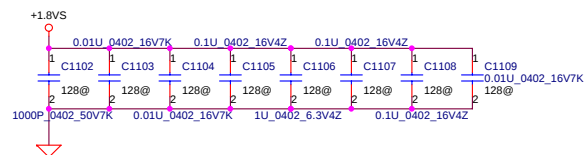


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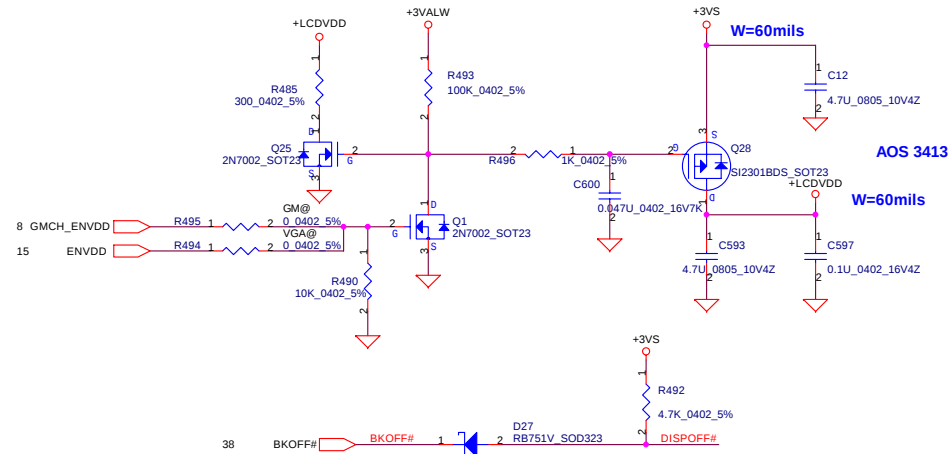


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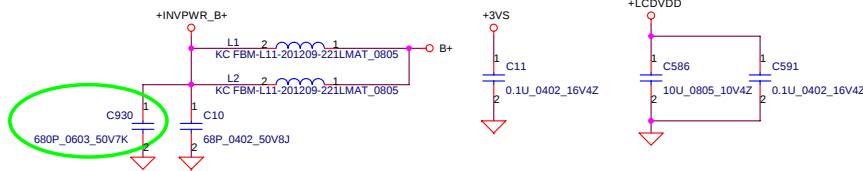
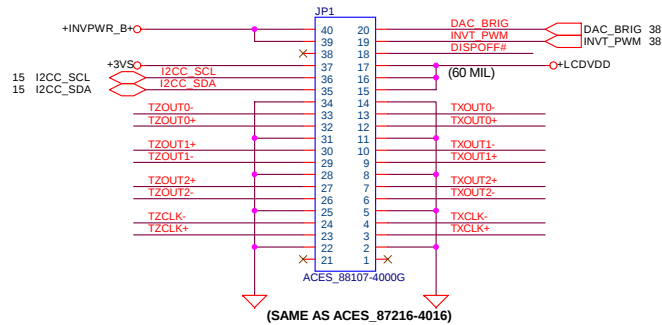
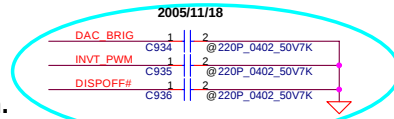


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LCD POWER CIRCUIT

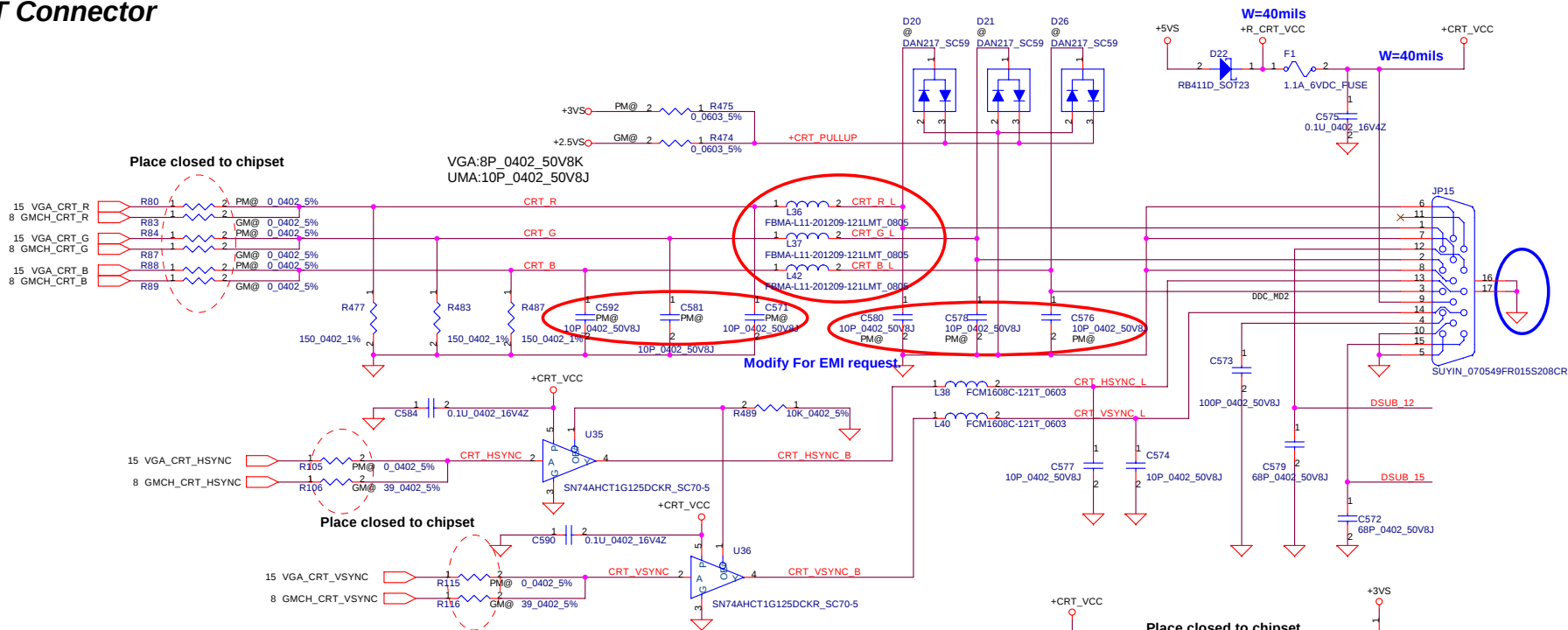


LCD/PANEL BD. Conn.

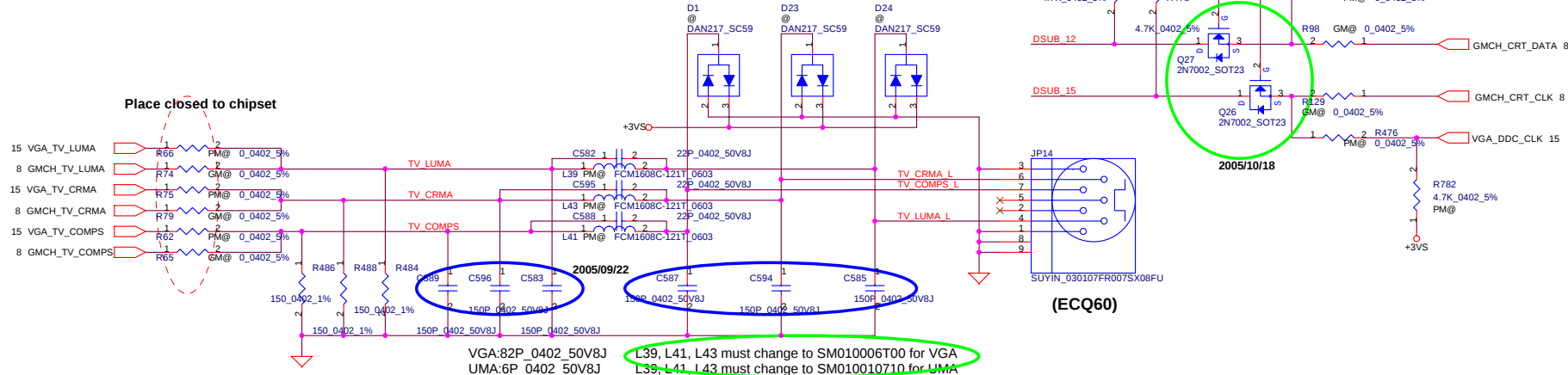


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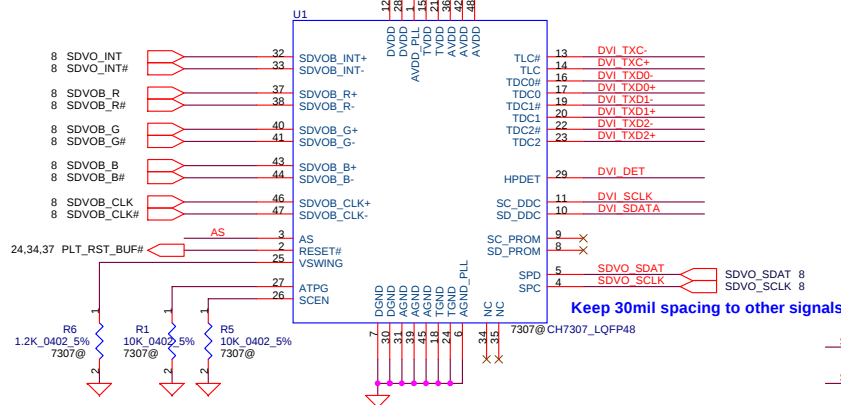
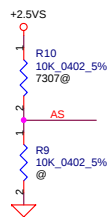
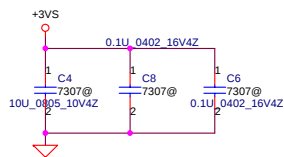
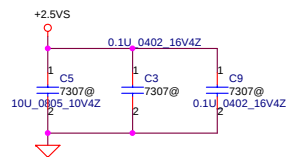
CRT Connector



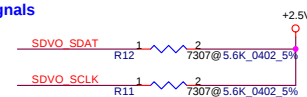
TV-OUT Conn.



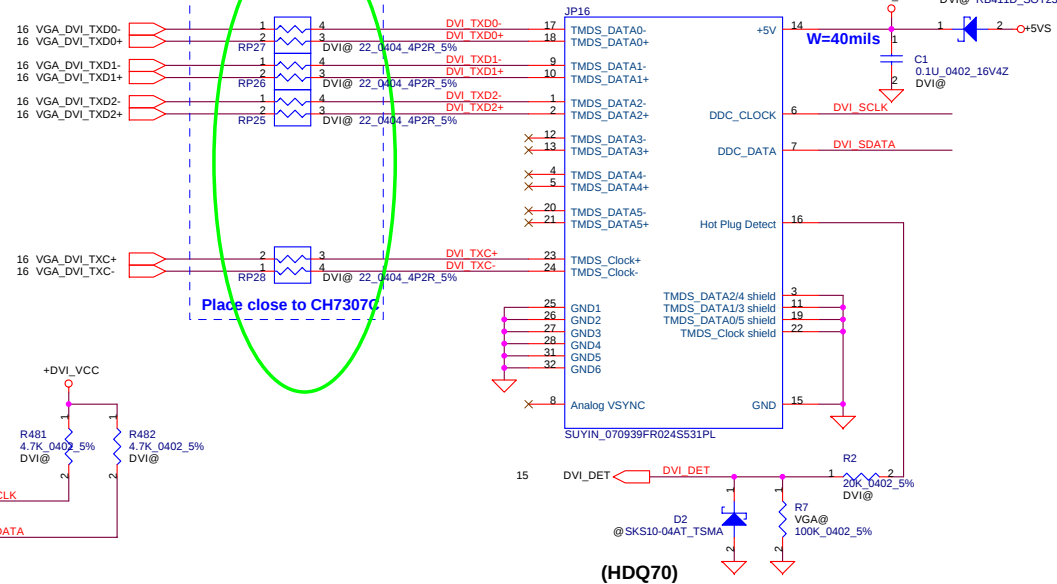
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BOM structure	DVI from SDVO	DVI from Discrete VGA
7307@	Stuff	No_Stuff
VGA@	No_Stuff	Stuff
@	No_Stuff	No_Stuff



DVI-D Connector

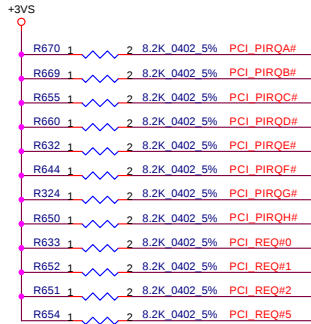
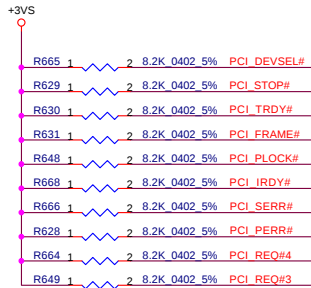


(HDQ70)

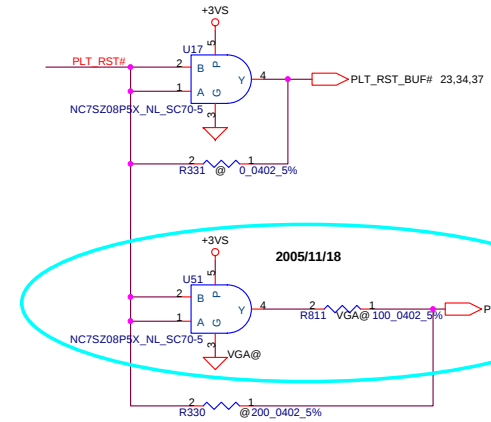
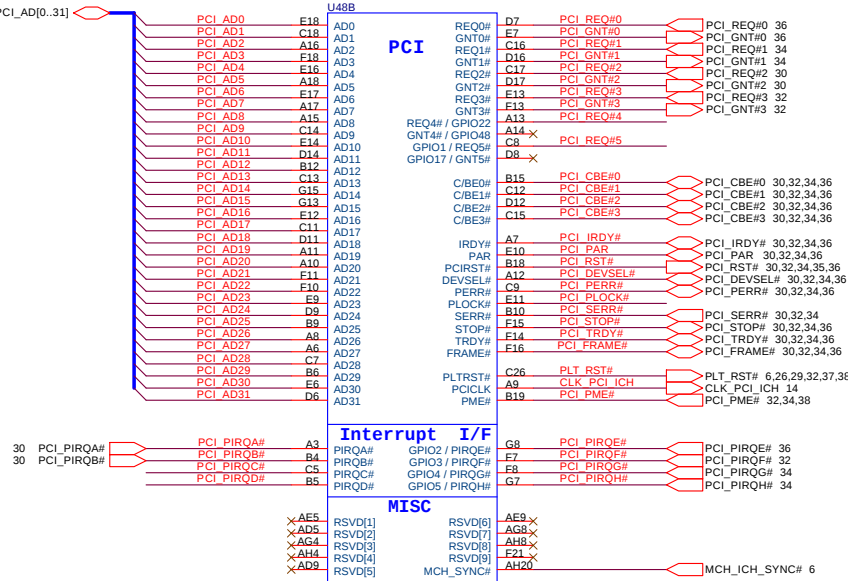
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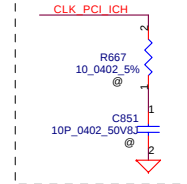
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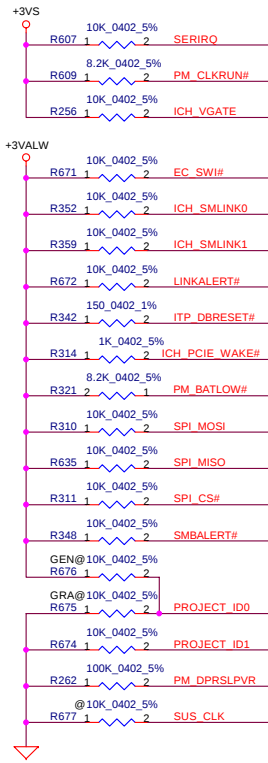
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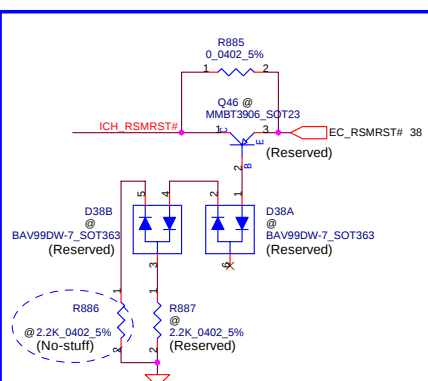
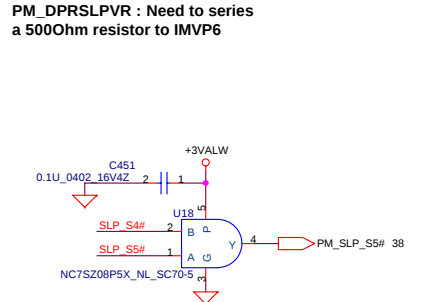
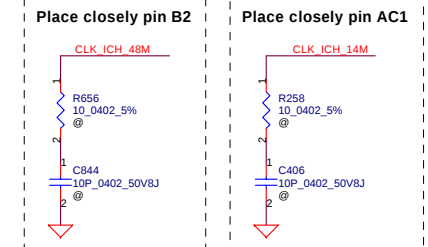
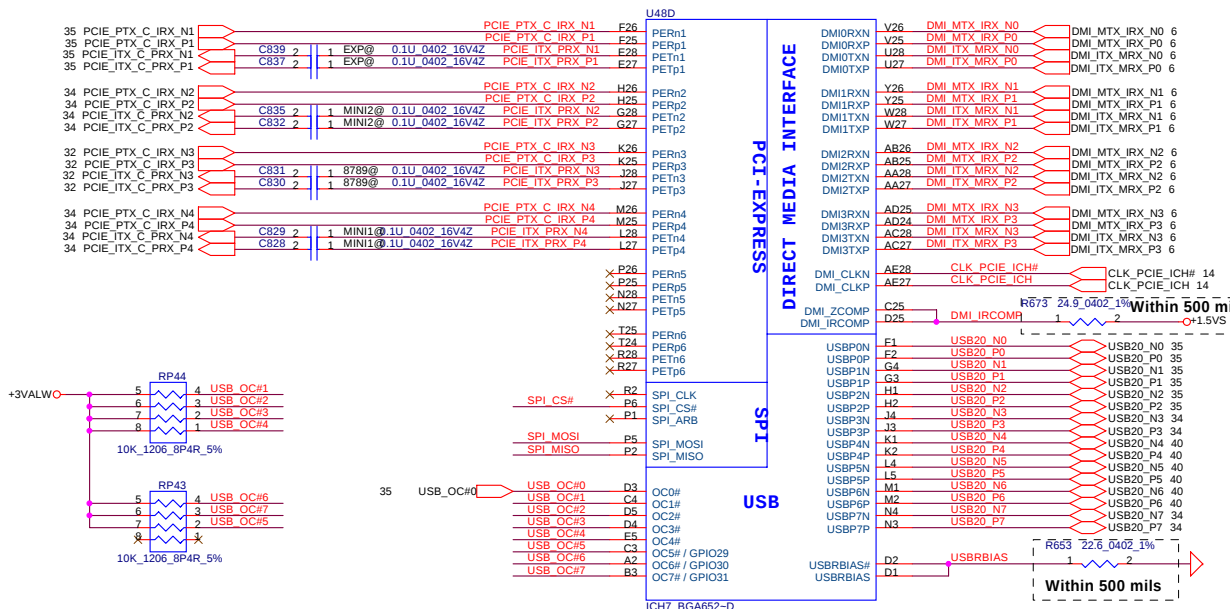
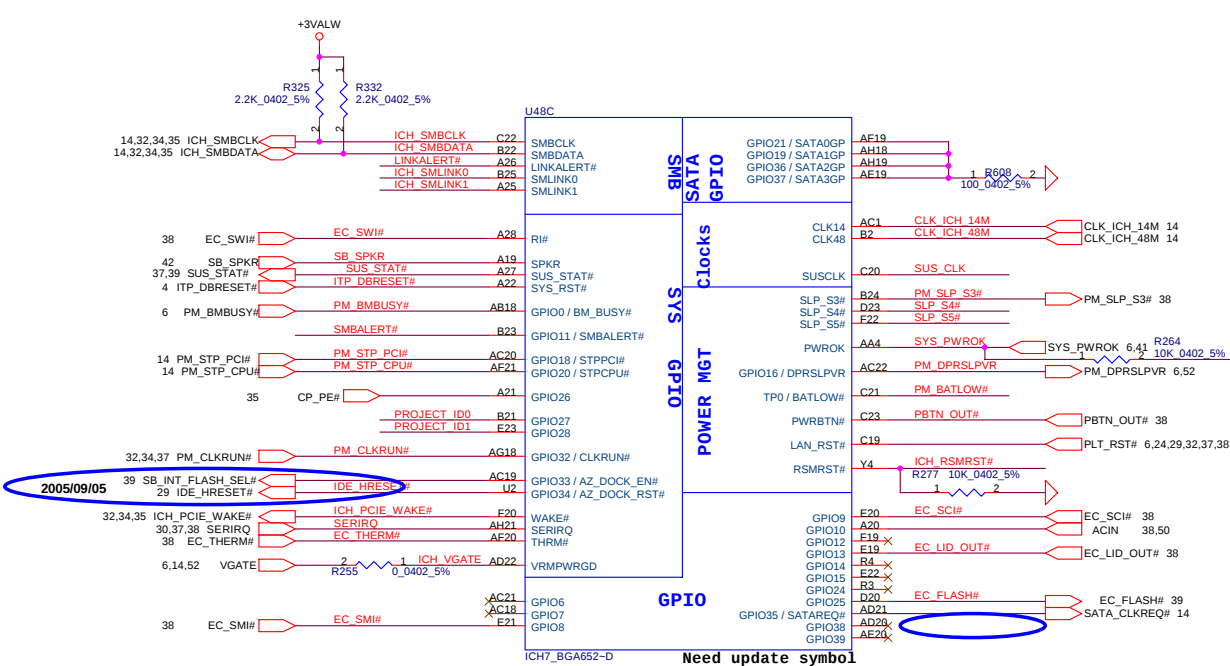
Place closely pin A9



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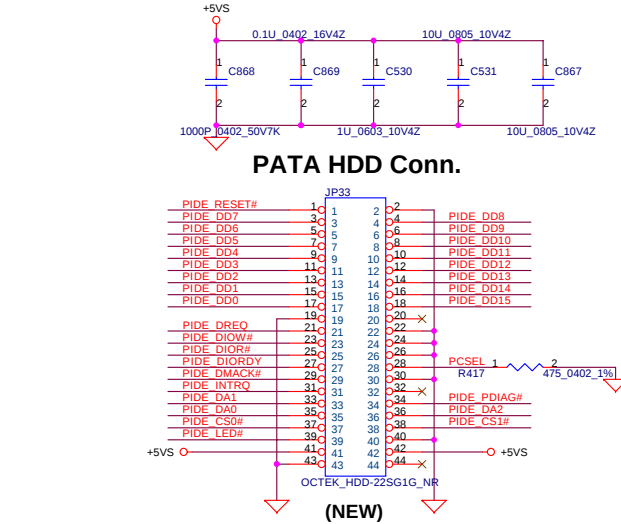
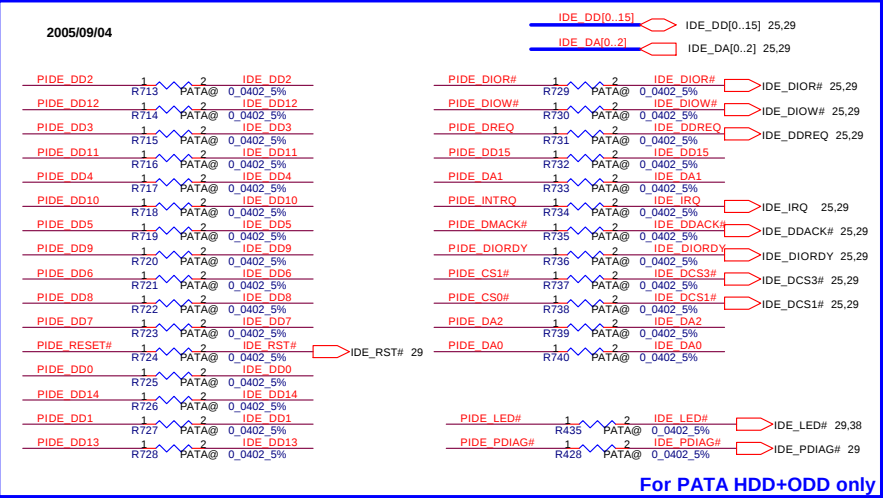
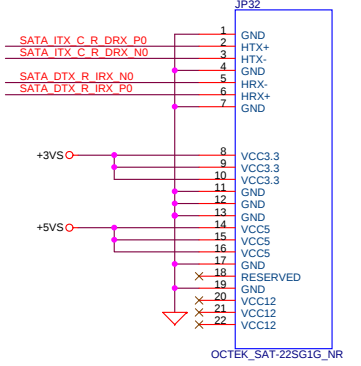
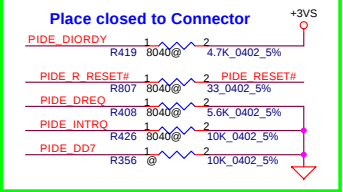
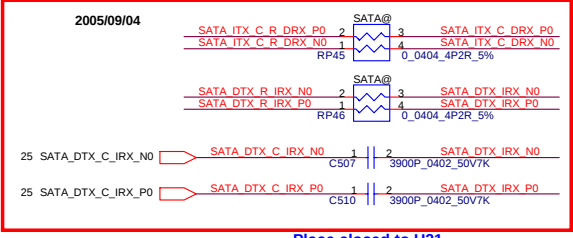
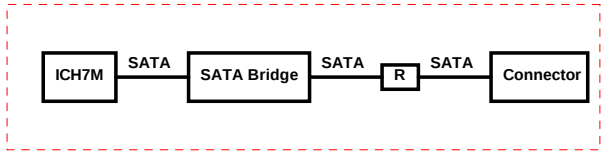
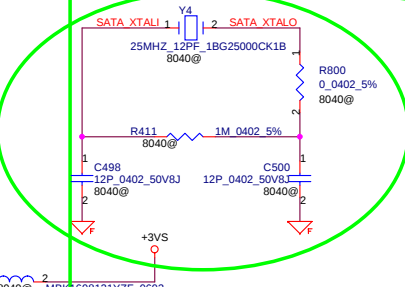
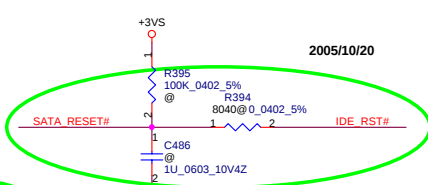
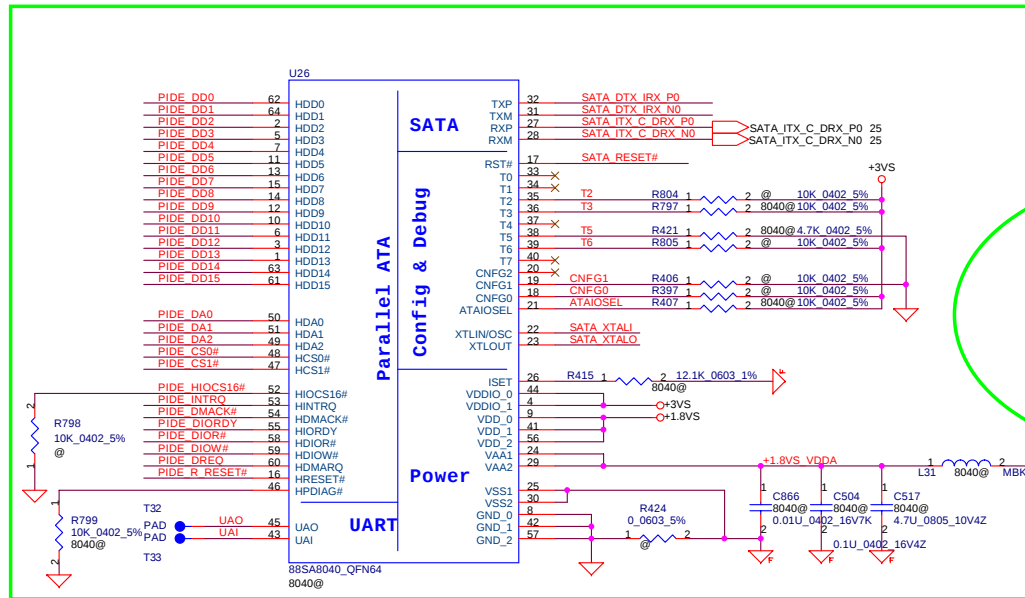


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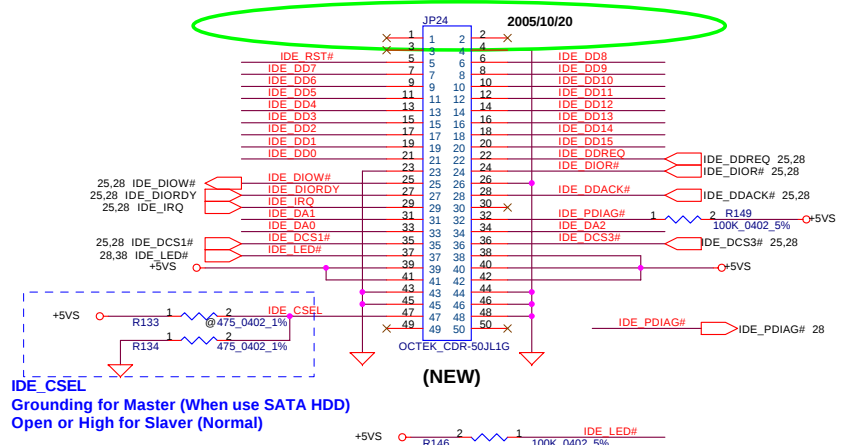
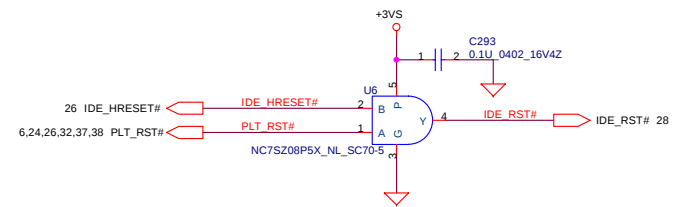
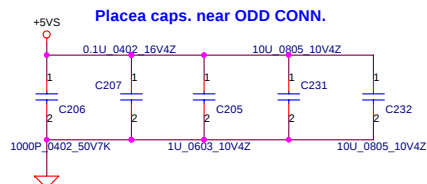


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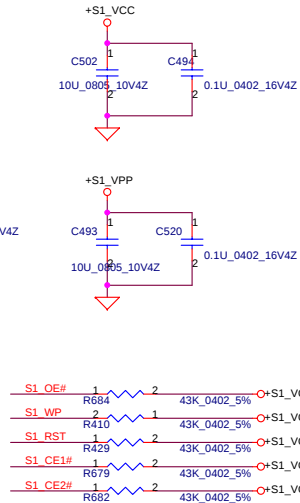
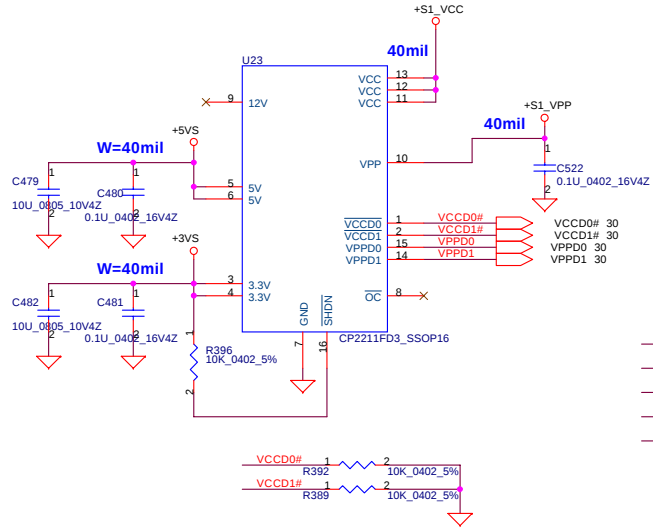
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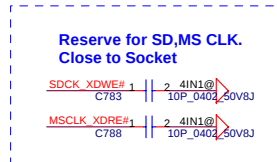
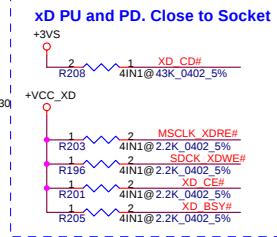
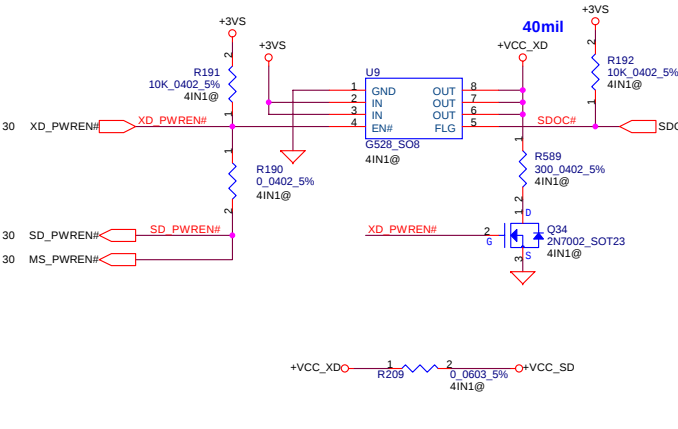


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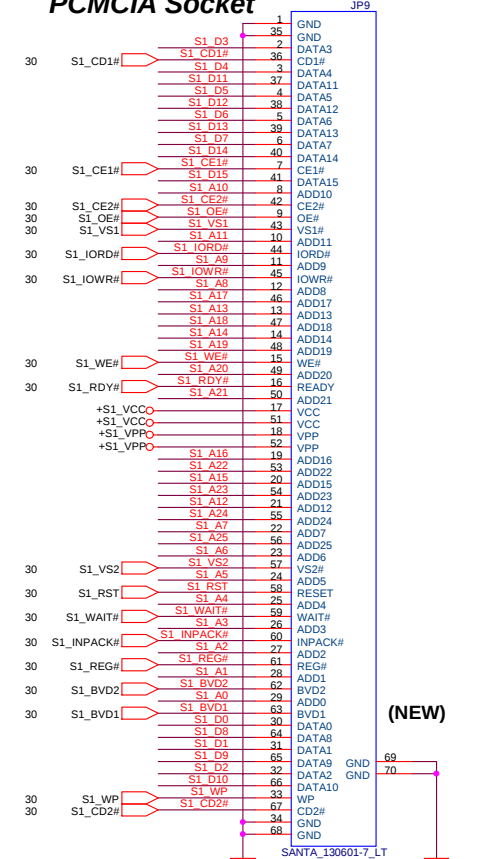
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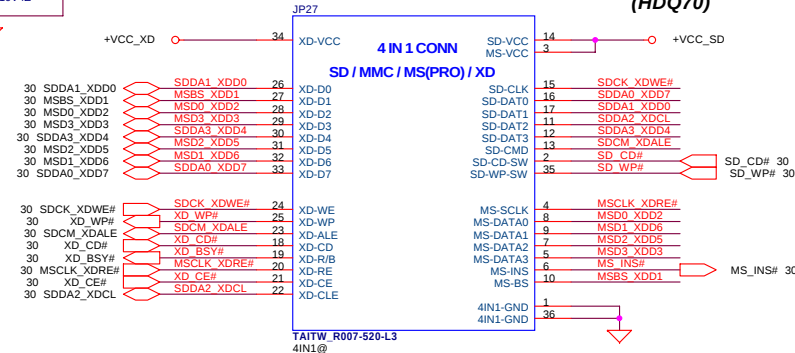
SD/MS Power Control



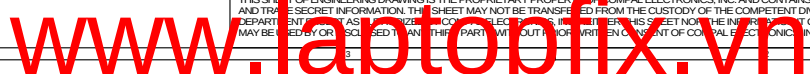
PCMCIA Socket



4 IN 1 Socket (HDQ70)



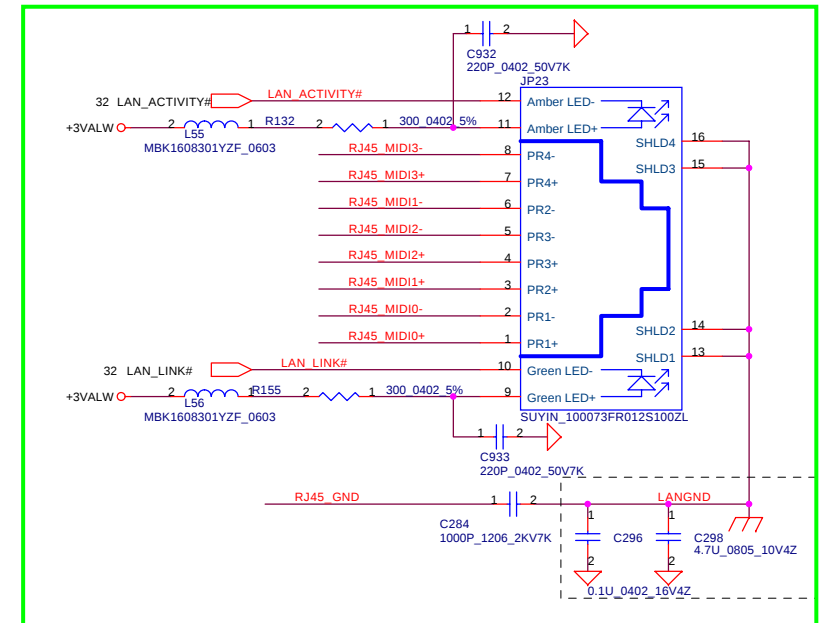
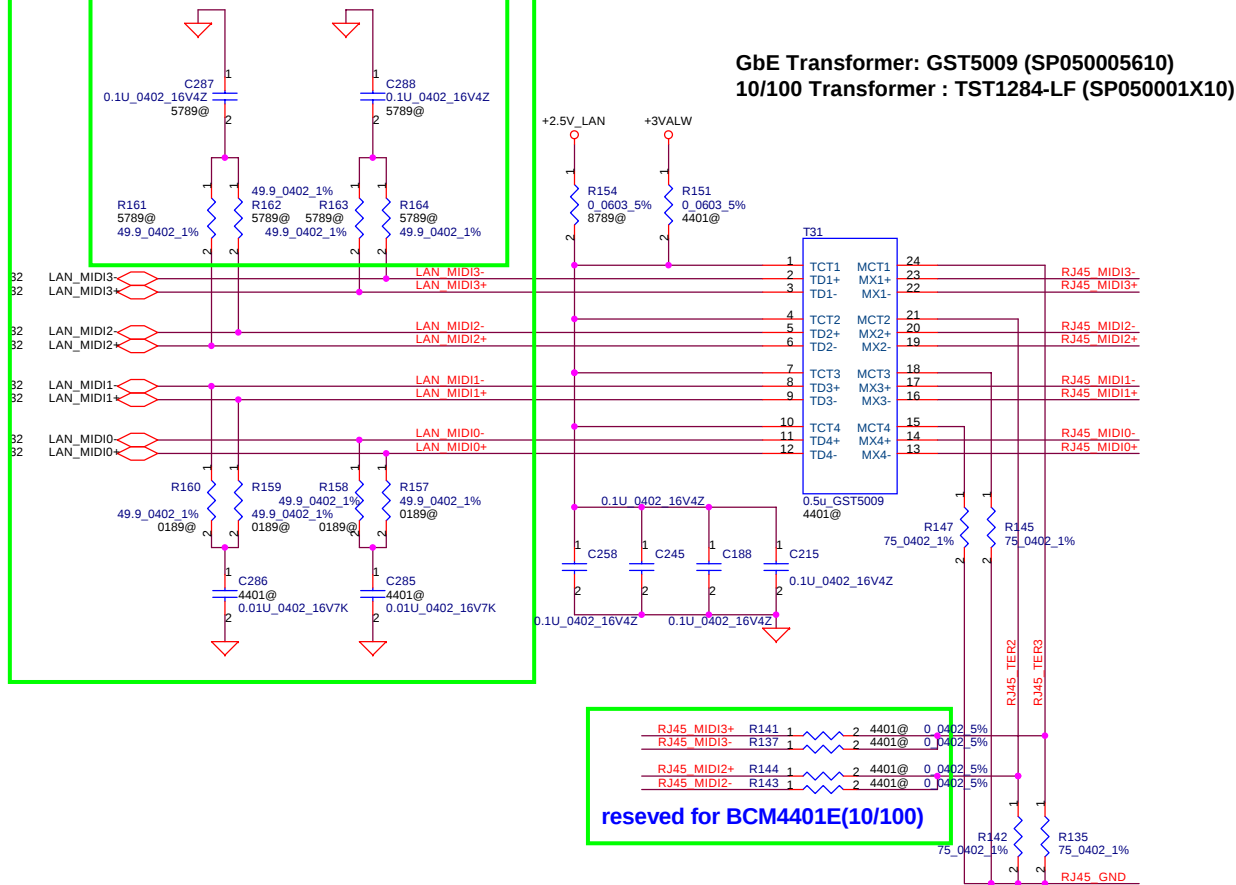
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LAN BCM4401E/ BCM5789

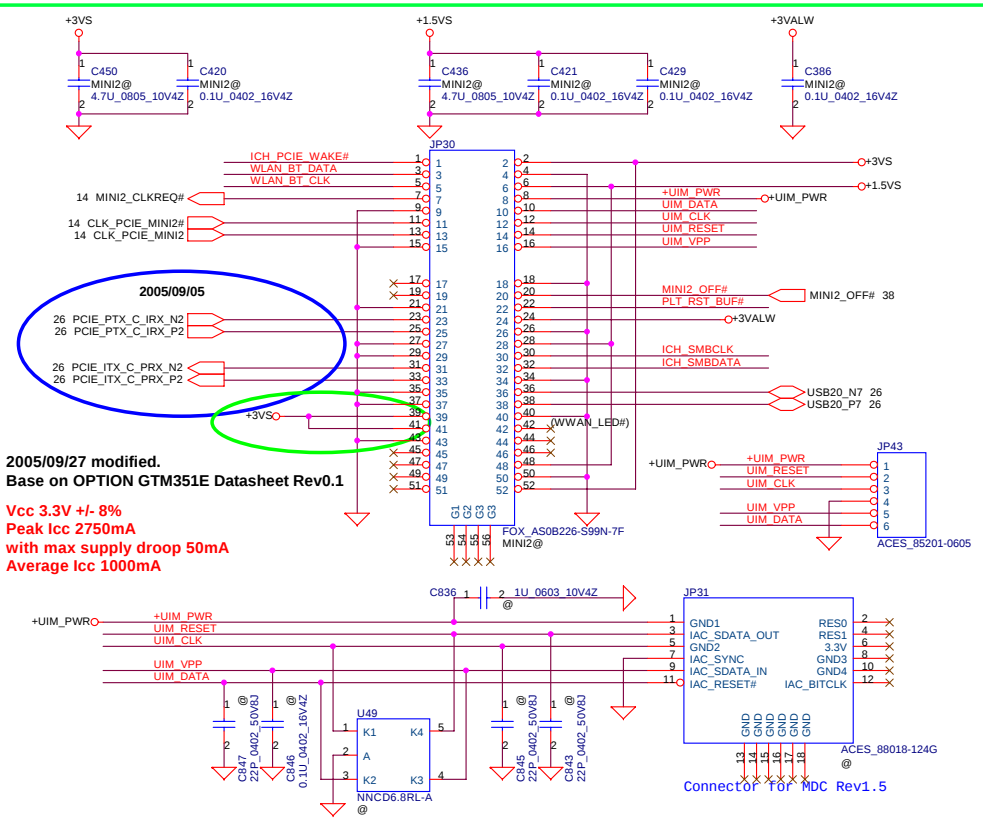
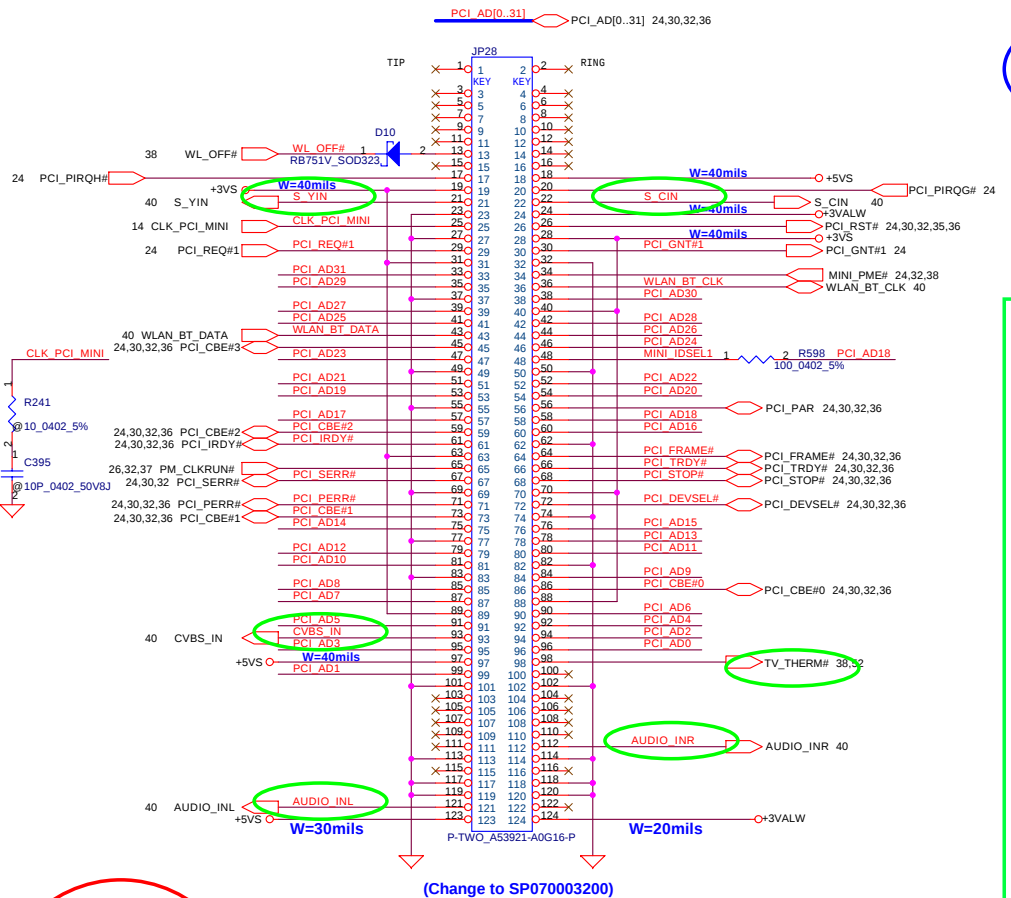
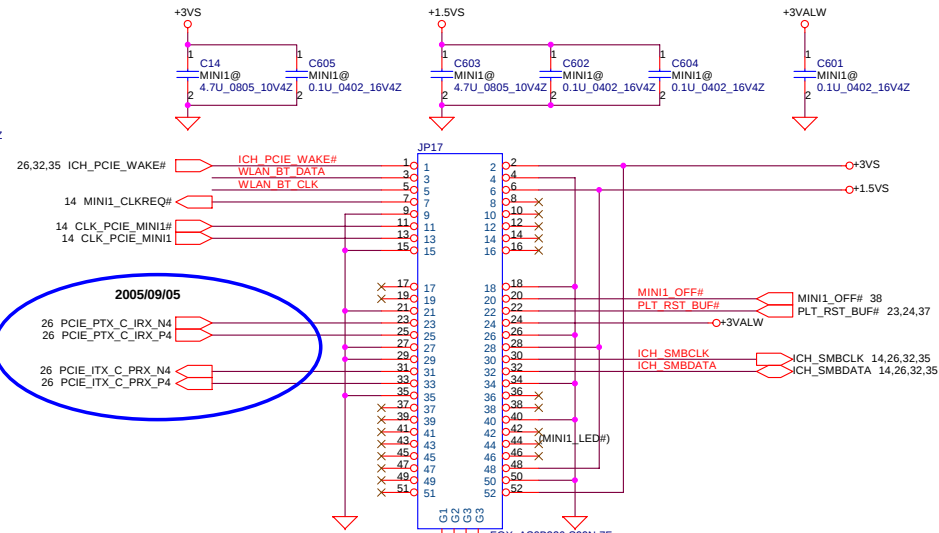
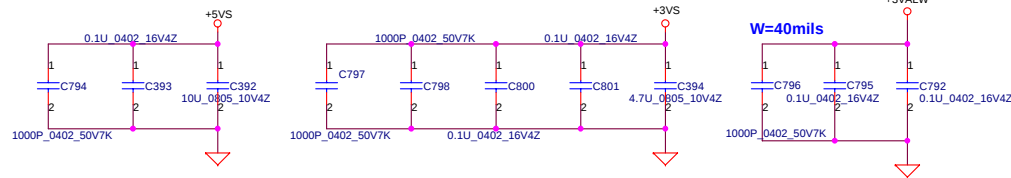
Place these components colsed to LAN chip

unpop when use BCM4401E(10/100)



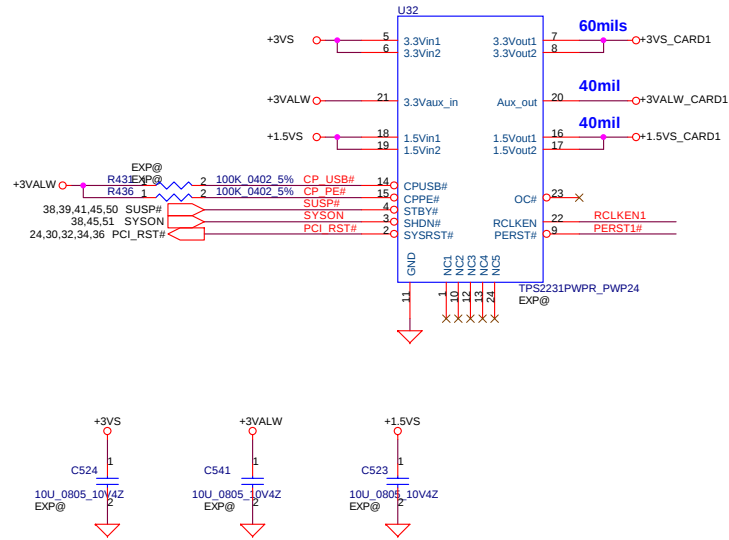
reserved for BCM4401E(10/100)

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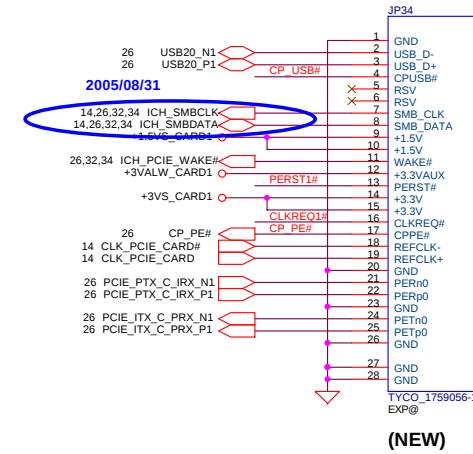


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

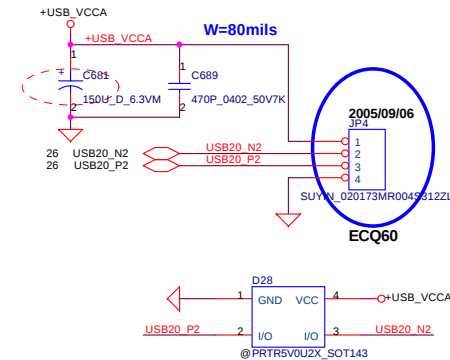
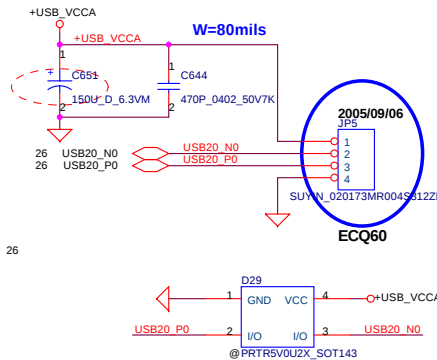
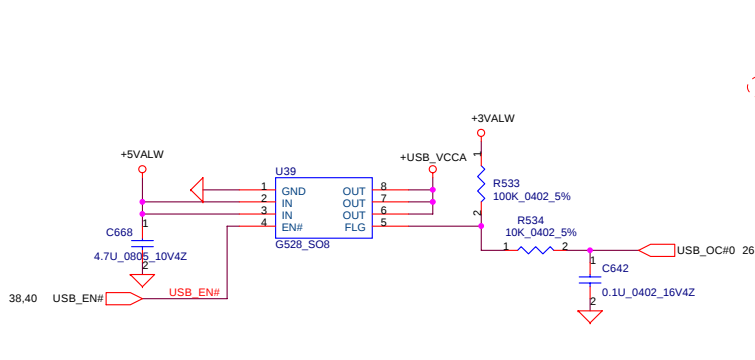
New Card Power Switch



New Card Socket (Left)



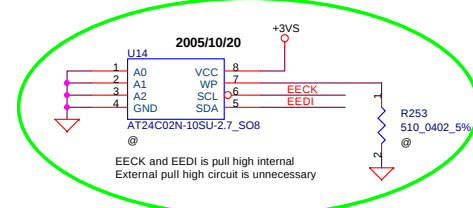
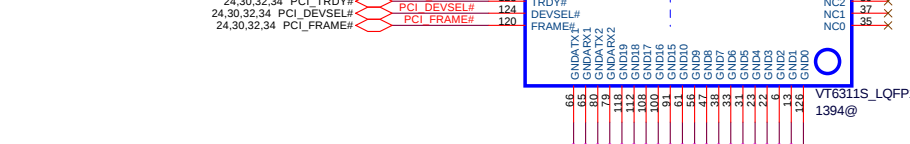
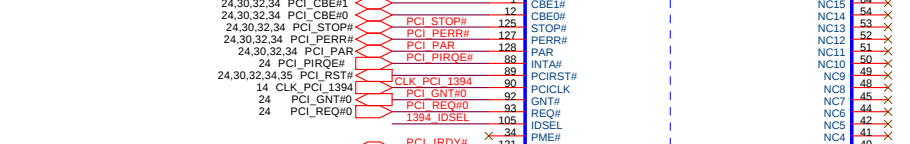
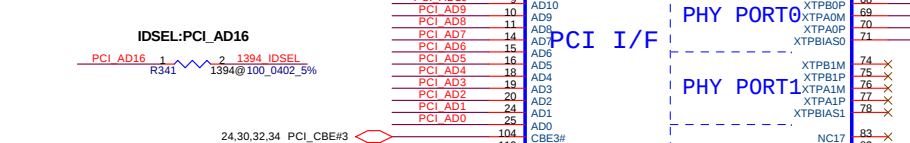
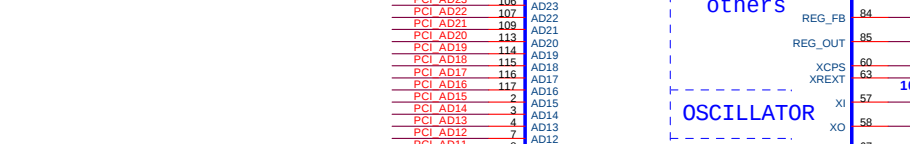
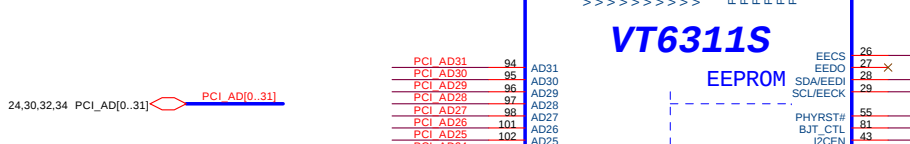
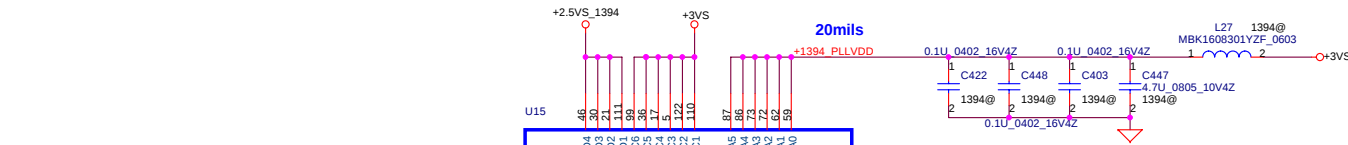
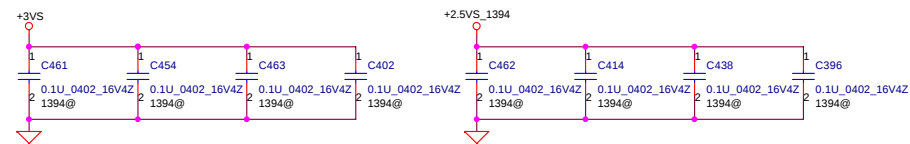
USB CONN. 1 & 2



SUYIN_020173MR004G533ZR_4P

SUYIN_020173MR004G533ZR_4P

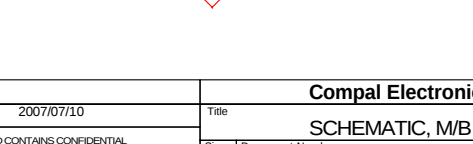
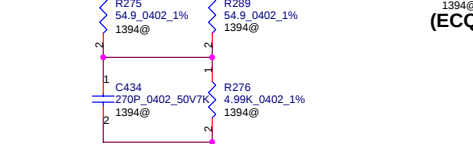
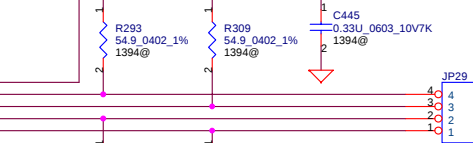
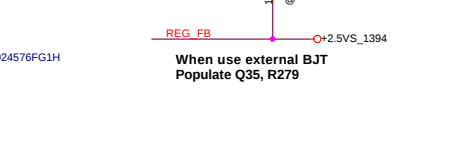
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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When use external EEPROM
Populate U14, R246, R253
Un-populate R261



When use external BJT
Populate Q35, R279



24,30,32,34 PCI_AD[0..31] PCI_AD[0..31]

IDSEL:PCI_AD16

- 24,30,32,34 PCI_CBE#3
- 24,30,32,34 PCI_CBE#2
- 24,30,32,34 PCI_CBE#1
- 24,30,32,34 PCI_CBE#0
- 24,30,32,34 PCI_STOP#
- 24,30,32,34 PCI_PERR#
- 24,30,32,34 PCI_PAR
- 24,30,32,34 PCI_PIRQE#
- 24,30,32,34,35 PCI_RST#
- 14 CLK PCI_1394
- 24 PCI_GNT#0
- 24 PCI_REQ#0
- 24,30,32,34 PCI_IRDY#
- 24,30,32,34 PCI_TRDY#
- 24,30,32,34 PCI_DEVSEL#
- 24,30,32,34 PCI_FRAME#

VT6311S

EEPROM

others

OSCILLATOR

PHY PORT0

PHY PORT1

PCI I/F

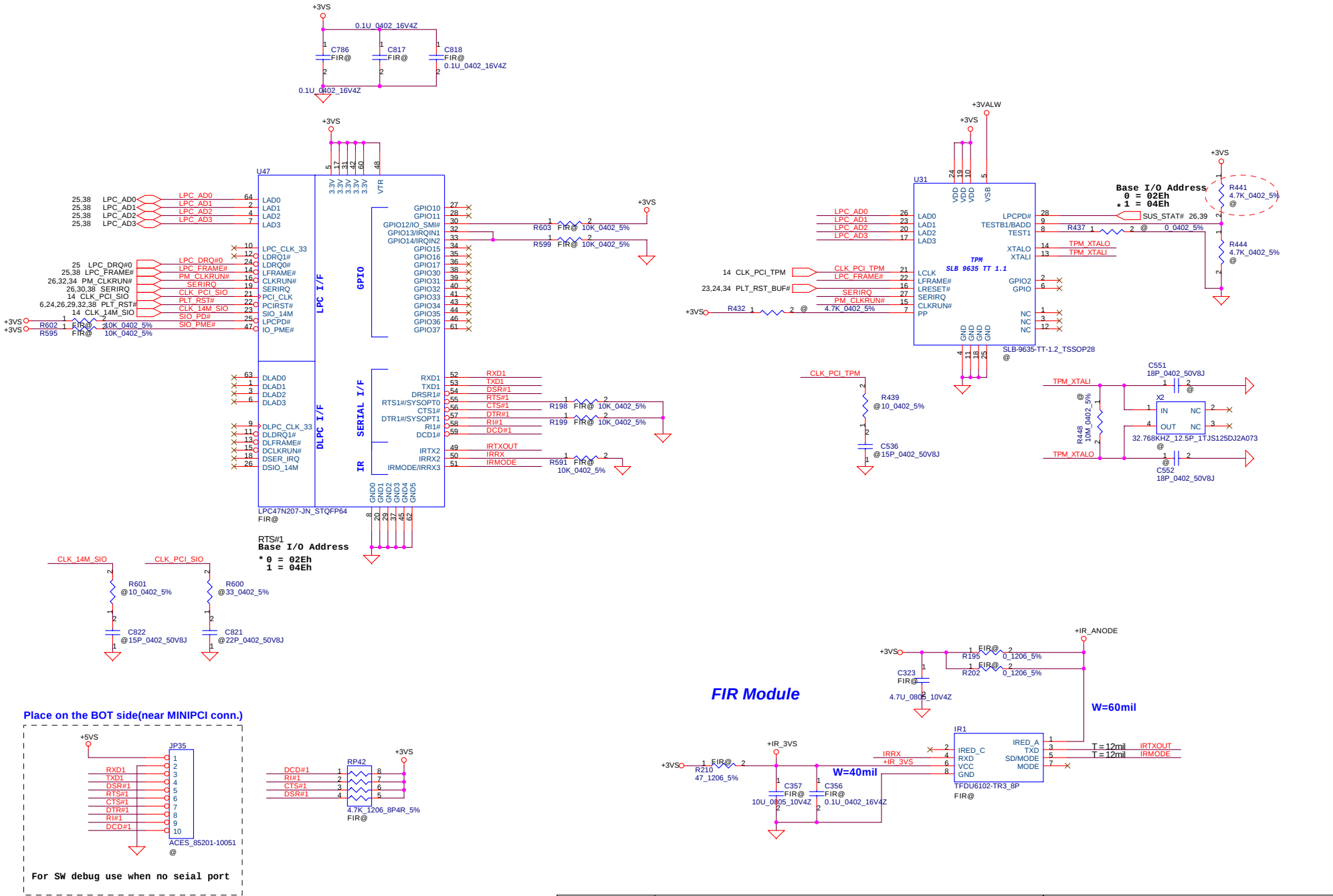
VT6311S_LQFP128
1394@

2005/12/18
Change P/N : SA00000P510

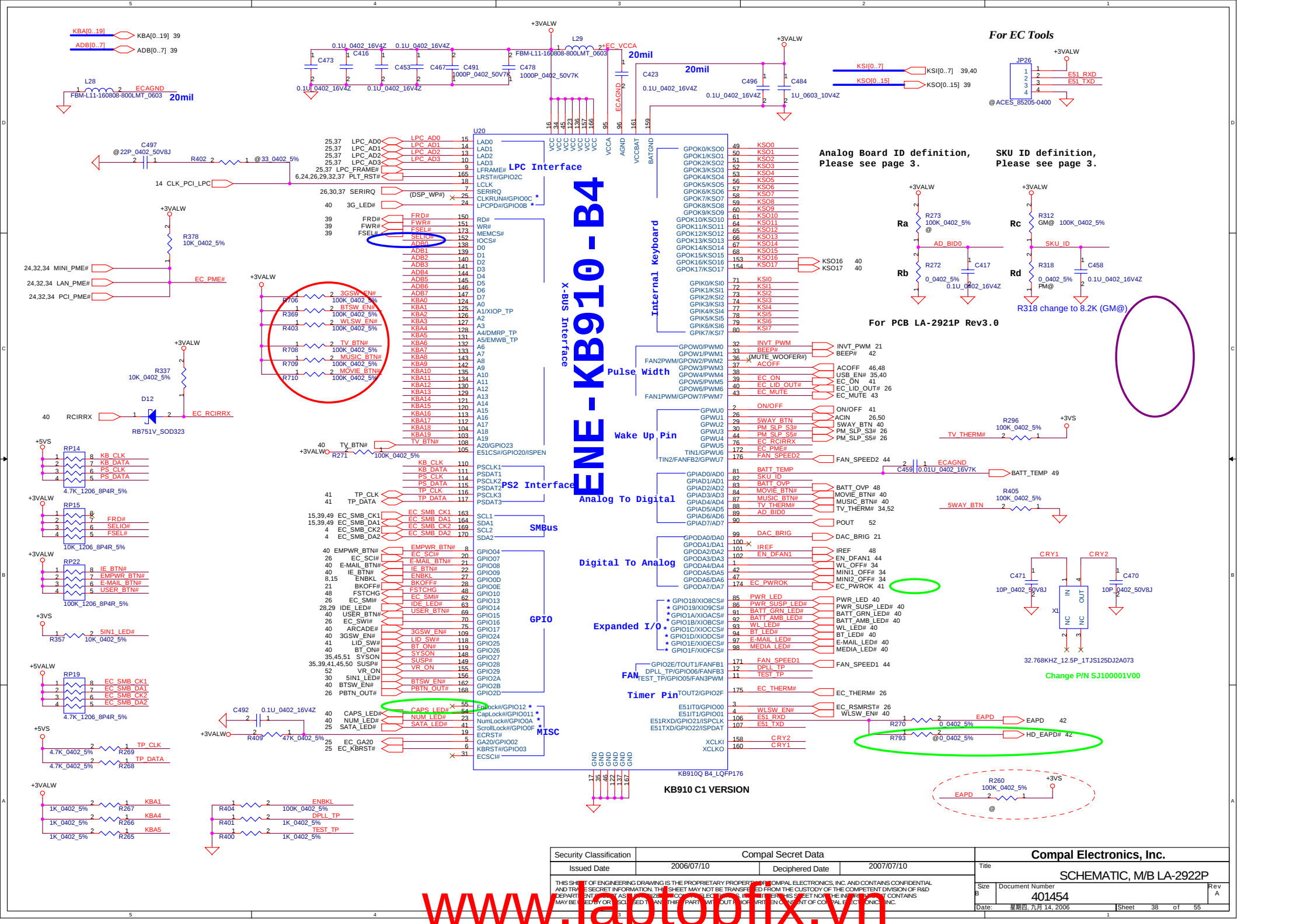
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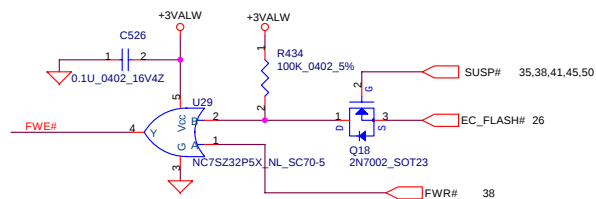
www.laptopfix.vn

SUPER I/O SMSc LPC47N207

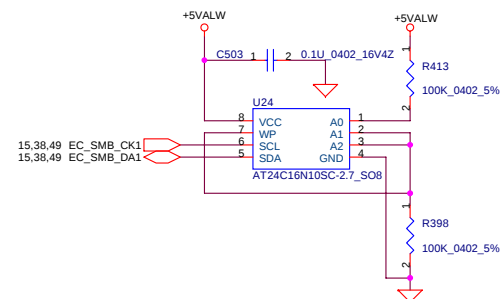


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Size	Document Number	Rev		
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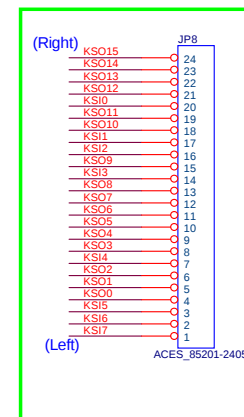




Check PCB Footprint



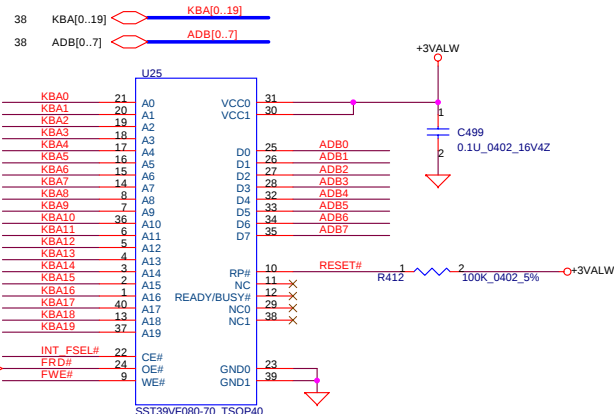
INT_KBD Conn.



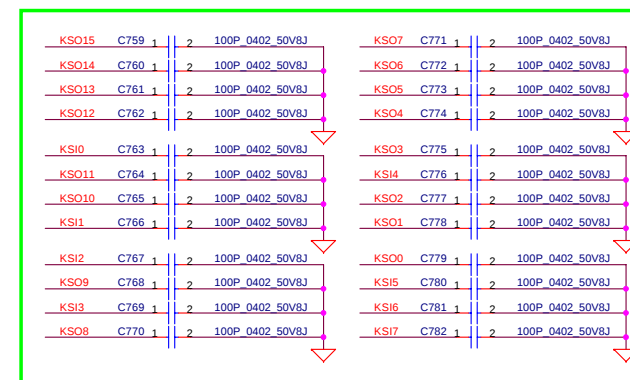
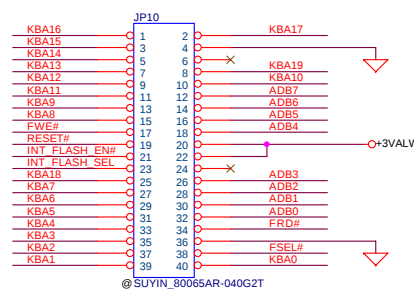
FOR DEBUG ONLY



1MB Flash ROM

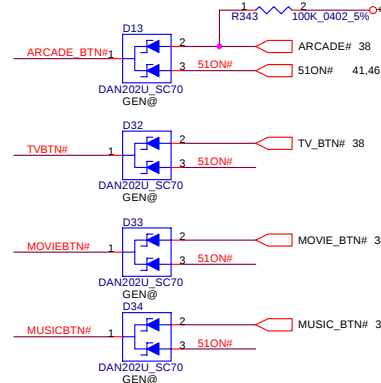
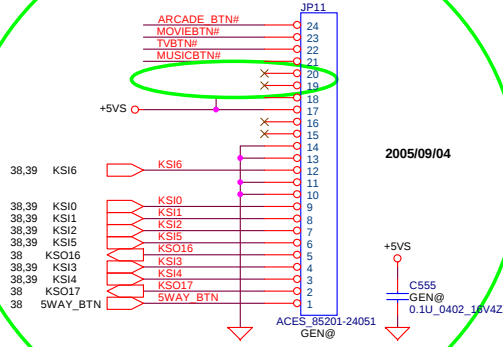


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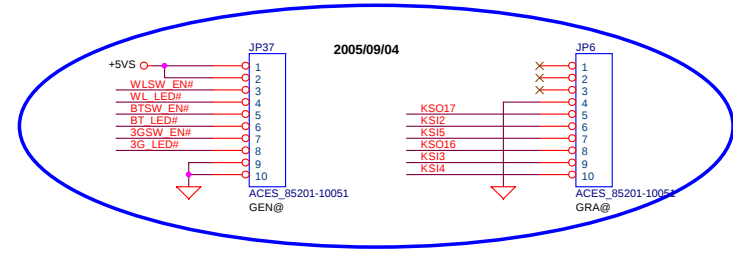
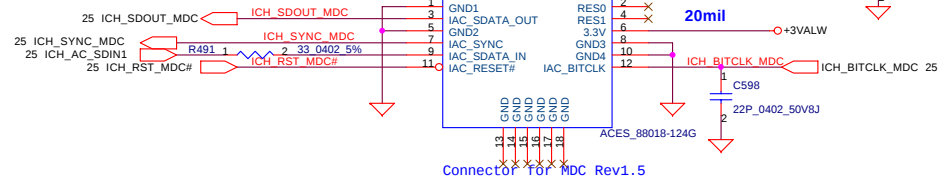


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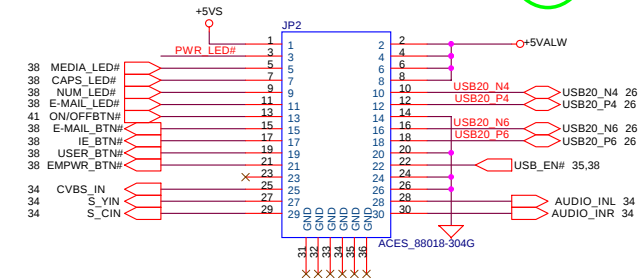
To CD-PLAY/B Conn.



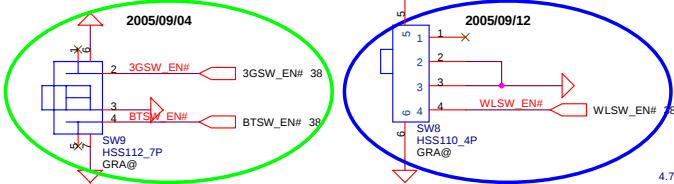
MDC Conn.



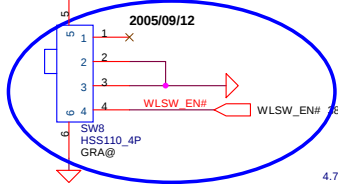
To LED/B Conn.



BT_SW & 3G_SW

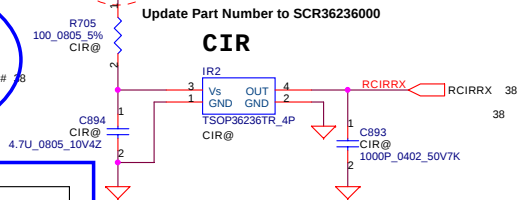


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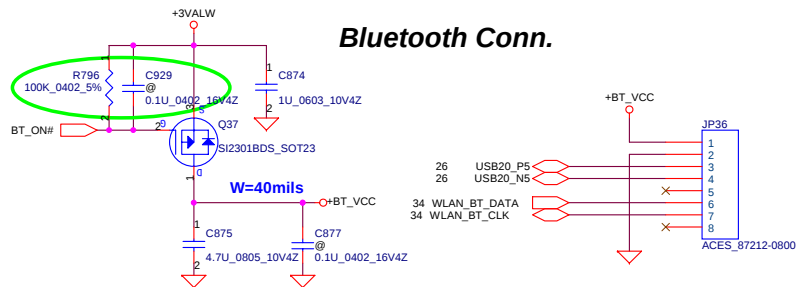


Update Part Number to SCR36236000

CIR



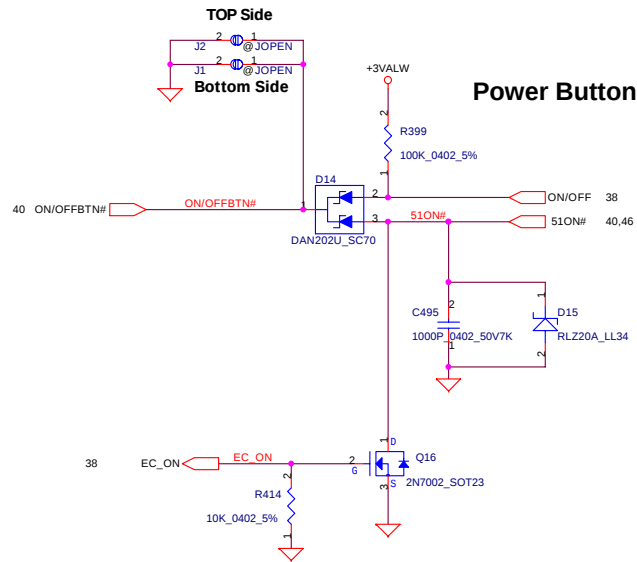
Bluetooth Conn.



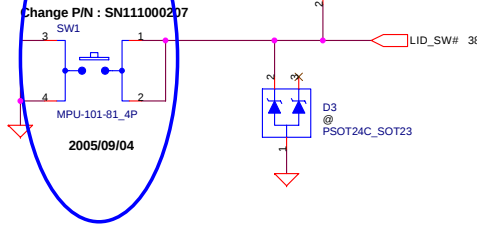
Geneva		Grapevine	
KSI0	KSI1	KSI2	KSI3
VOL_UP	RIGHT	PLAY	STOP
STOP	PLAY	NEXT	REV
NEXT	RECORD	VOL_DOWN	ARCANE_TV
REV			

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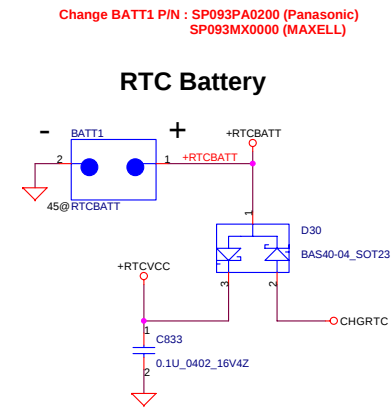
ON/OFF switch



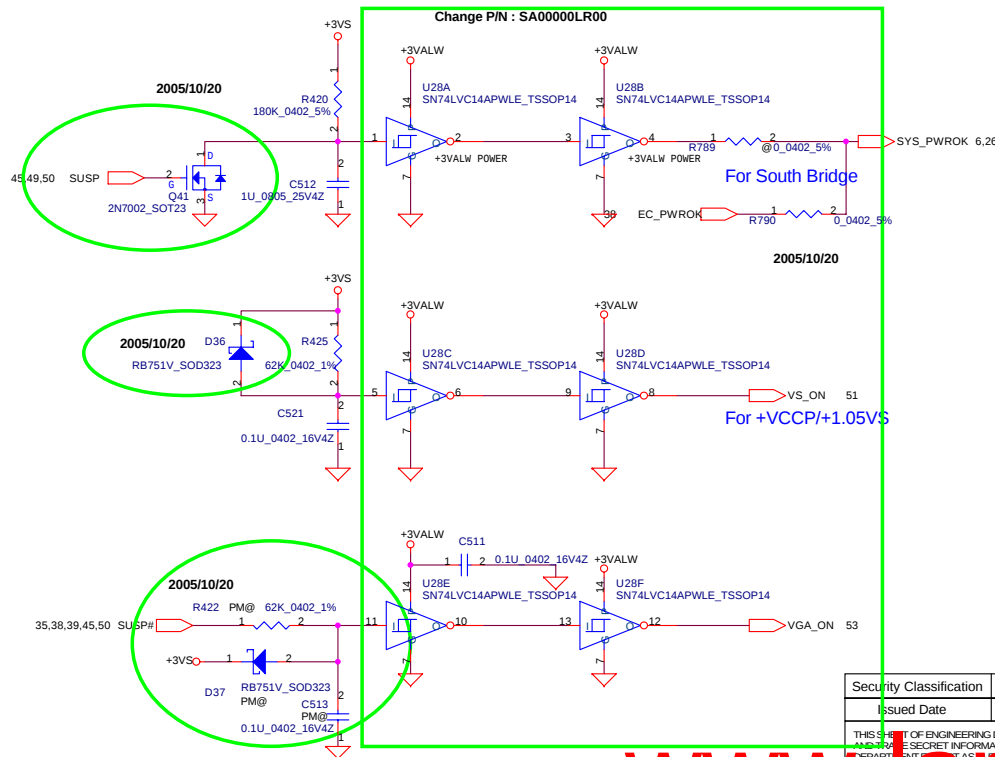
Lid Switch



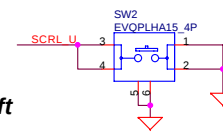
RTC Battery



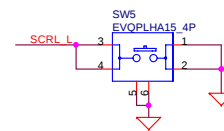
Power ON Circuit



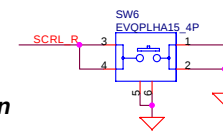
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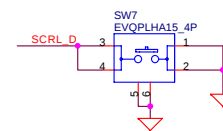
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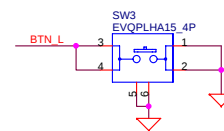
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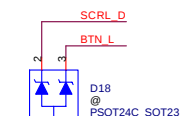
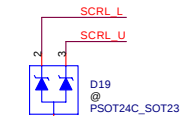
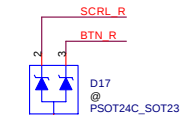
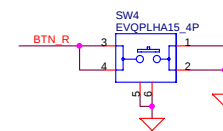
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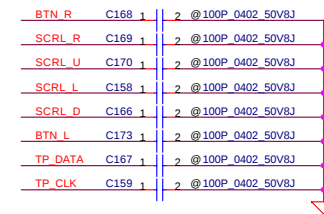
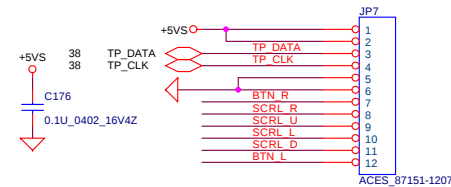
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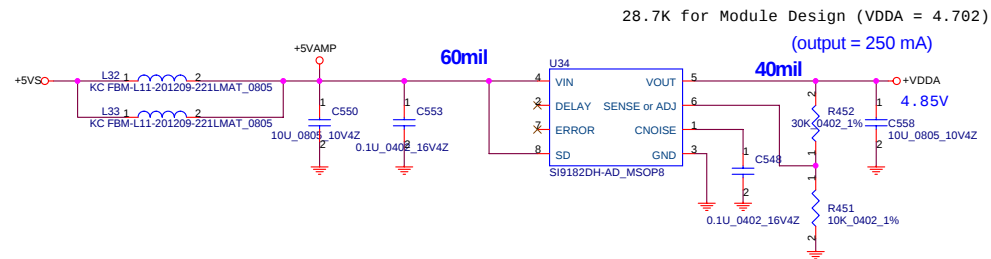
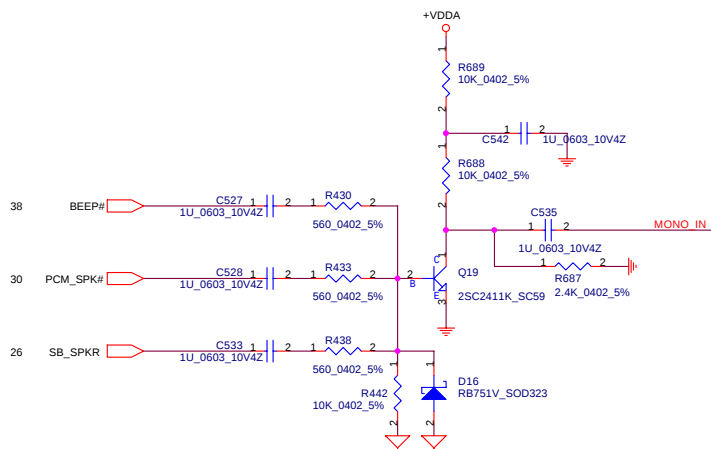
Right



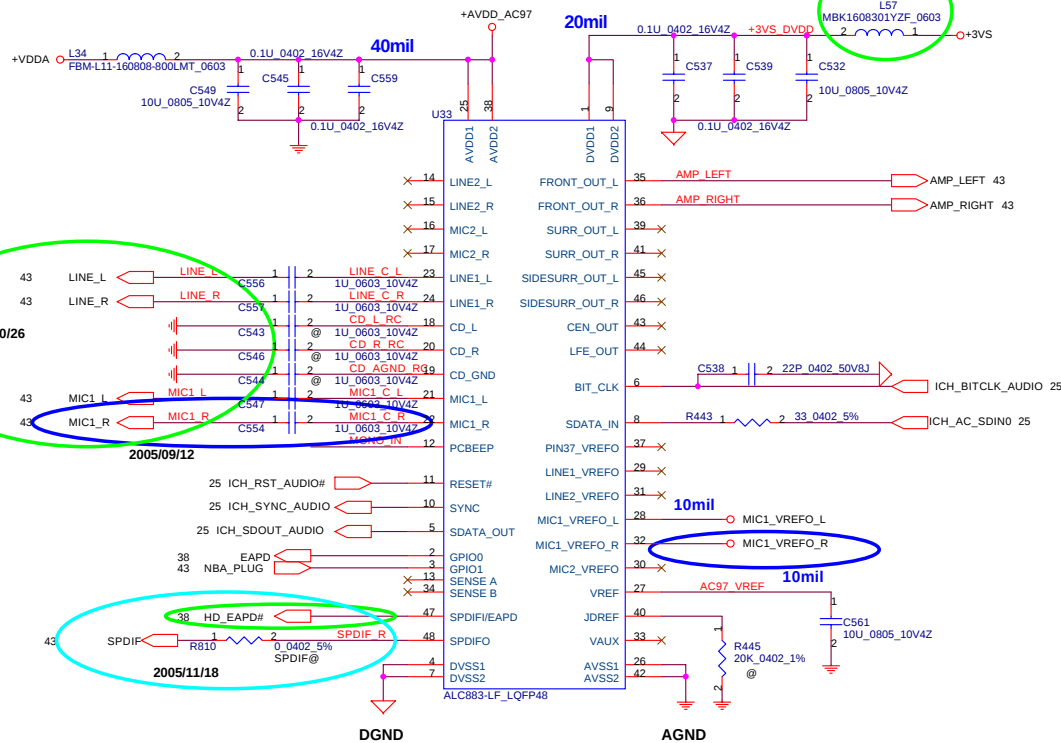
To TP/B Conn.



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HD Audio Codec



2005/10/26

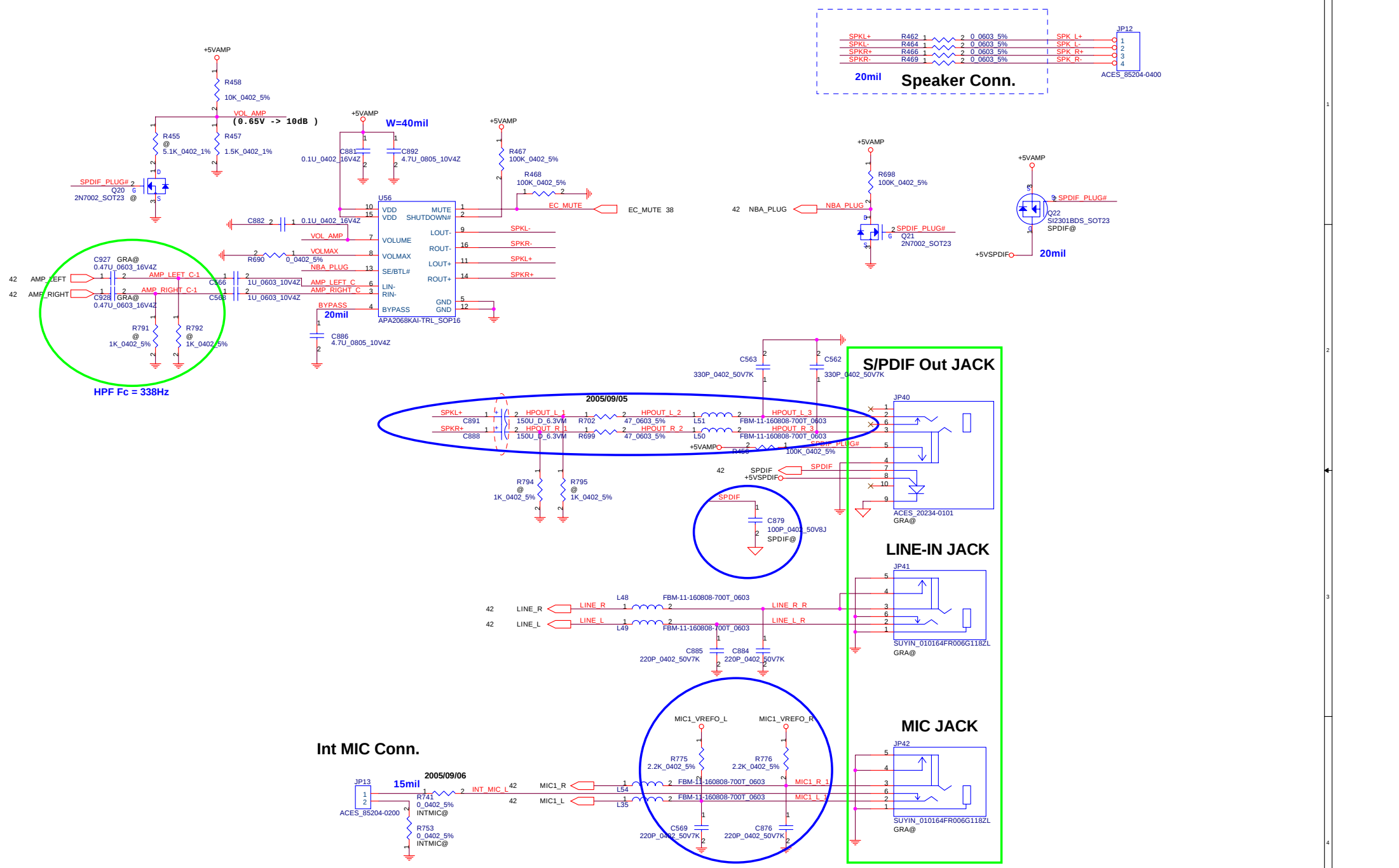
2005/09/12

2005/11/18

2005/09/20

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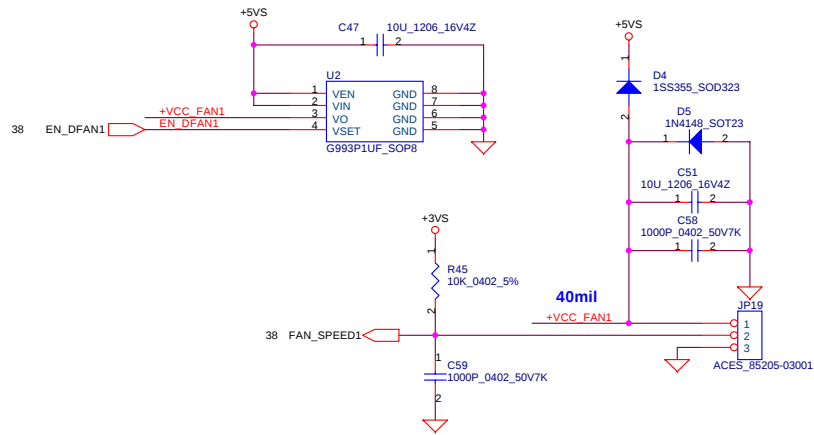
www.laptopfix.vn



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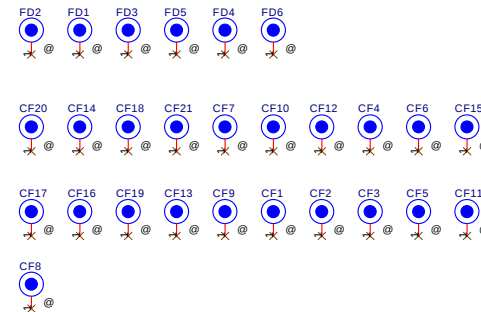
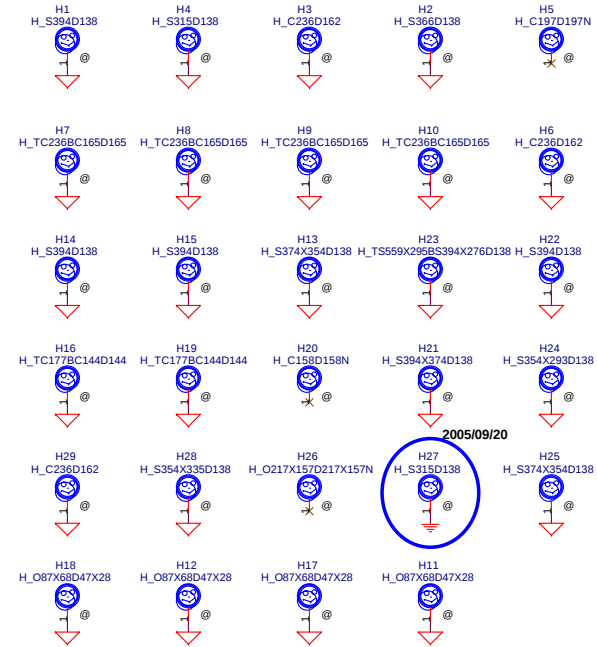
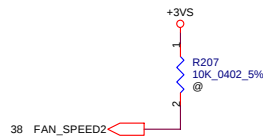
www.laptopfix.vn

FAN1 Conn



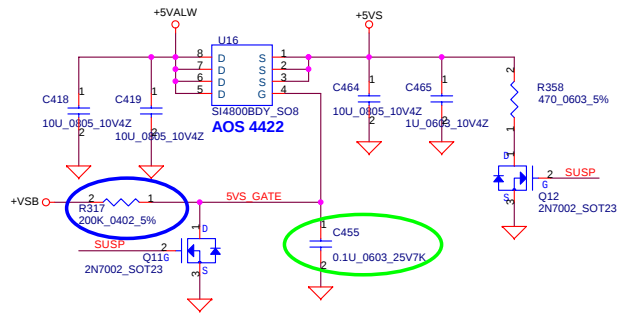
FAN2 Conn

2005/12/29: Remove 2nd FAN support components

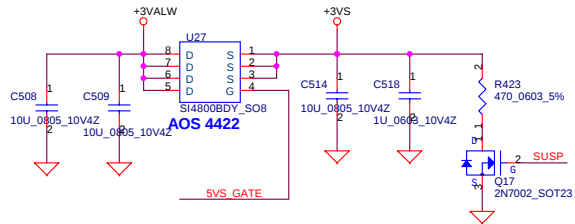


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+5VALW TO +5VS

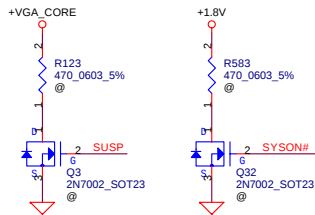
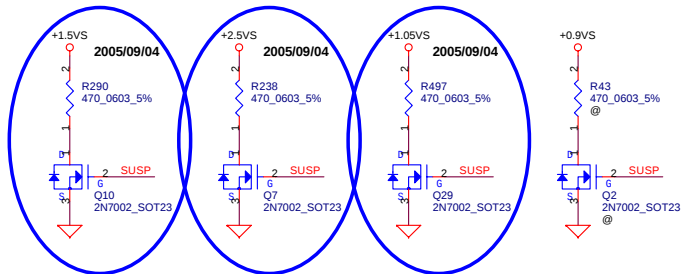
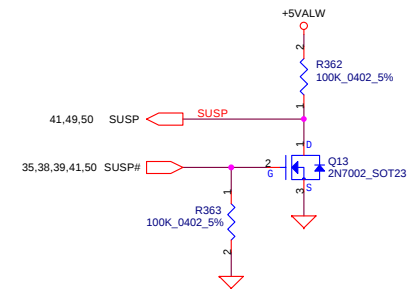
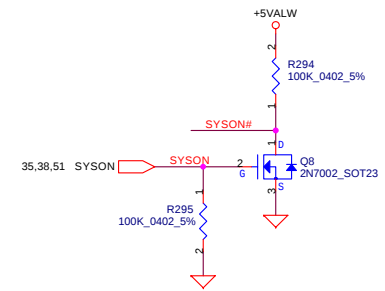
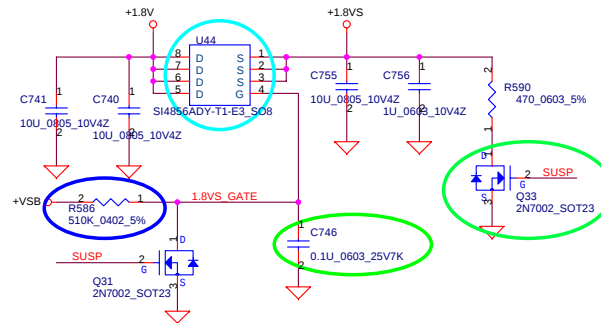


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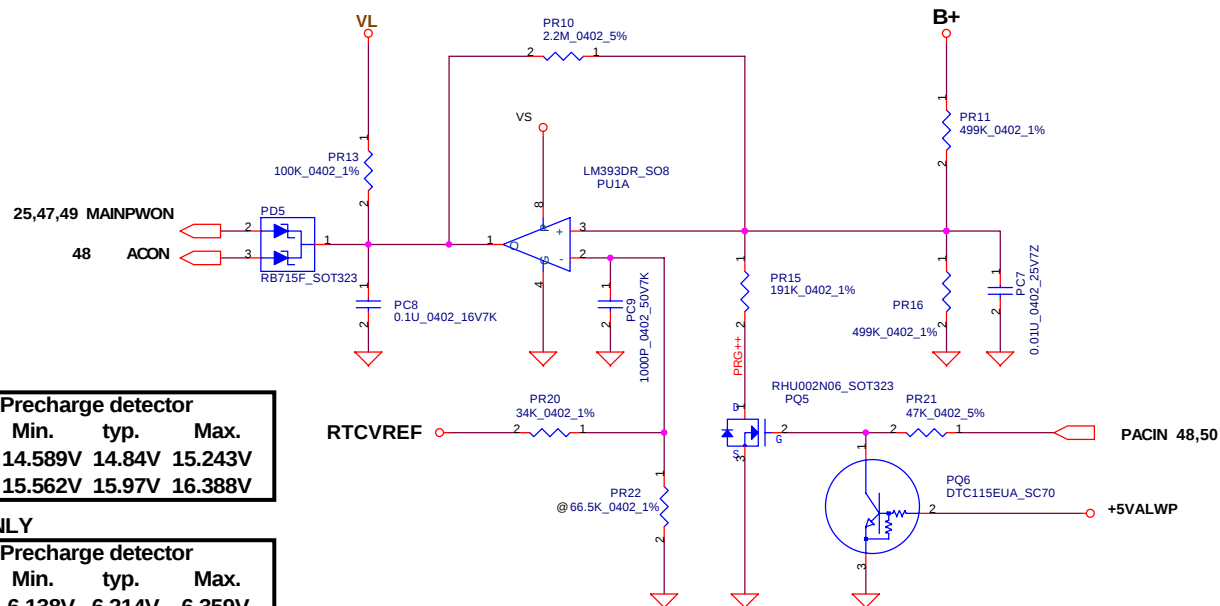
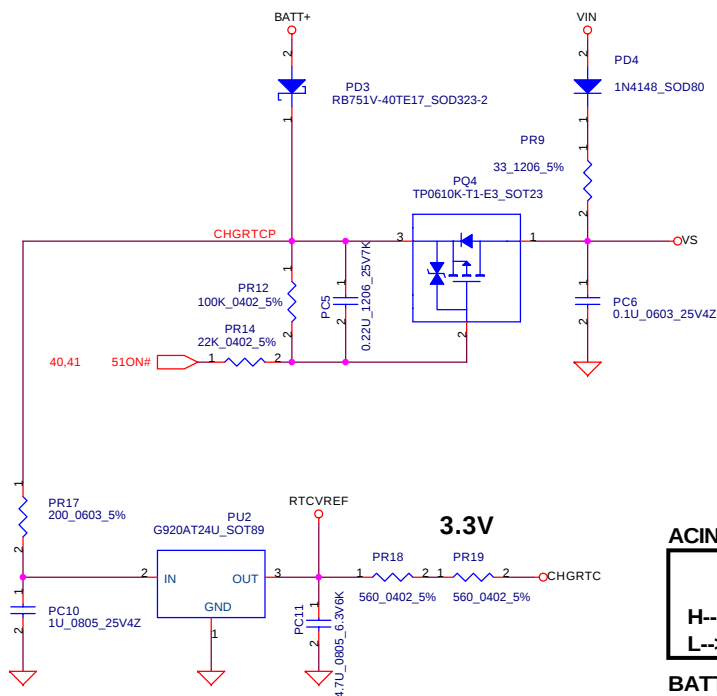
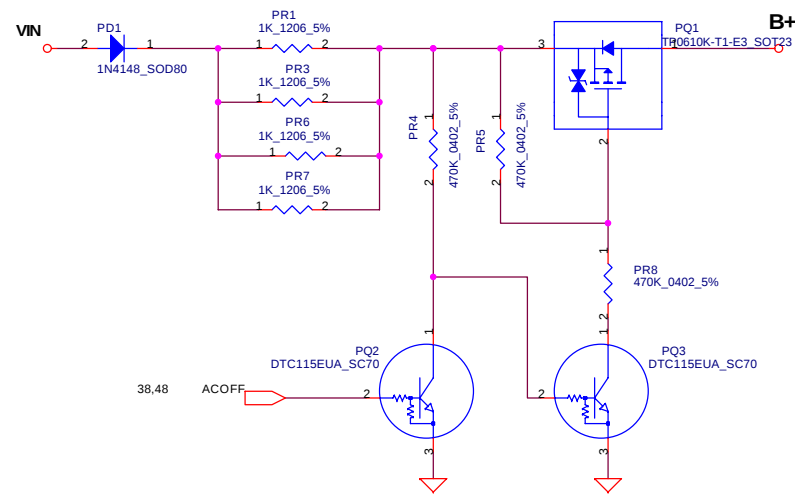
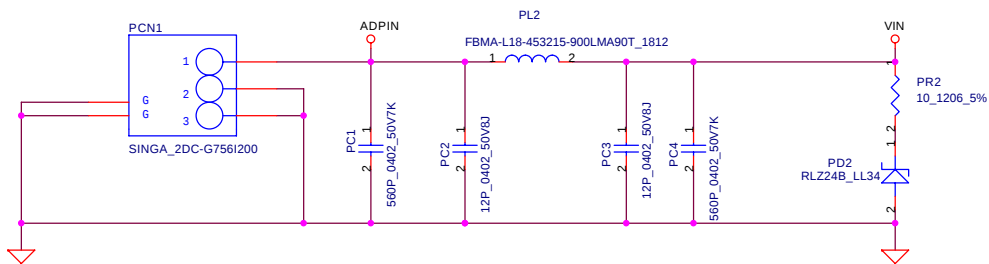


2005/12/18
Change P/N : SB000001Y00(New) SI4856ADY
SB548000310(Old)

+1.8V to +1.8VS



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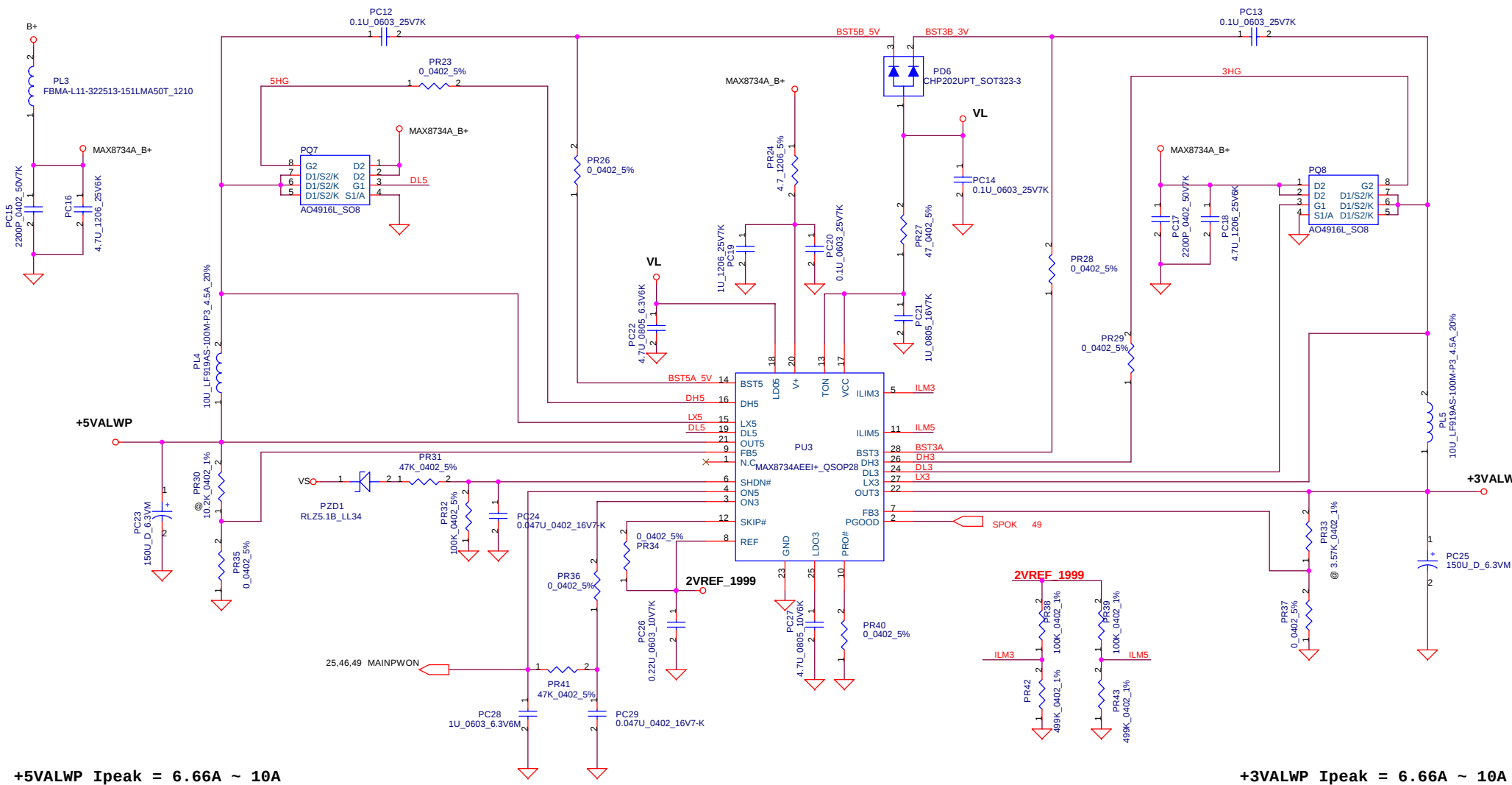


ACIN			
Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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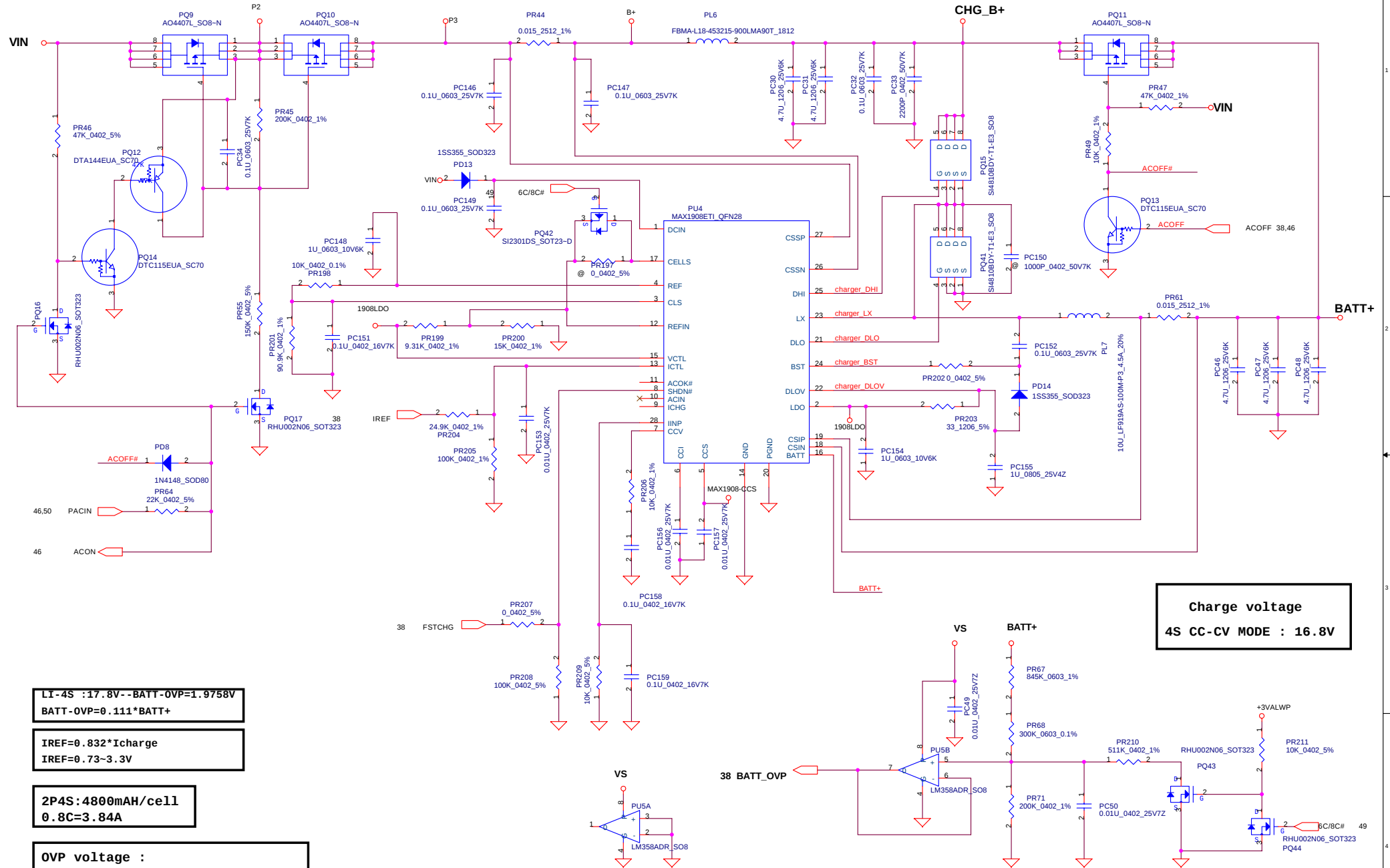
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Iadp=0~4.74A(90W)



Charge voltage
4S CC-CV MODE : 16.8V

LI-4S :17.8V--BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+

IREF=0.832*Icharge
IREF=0.73~3.3V

2P4S:4800MAH/cell
0.8C=3.84A

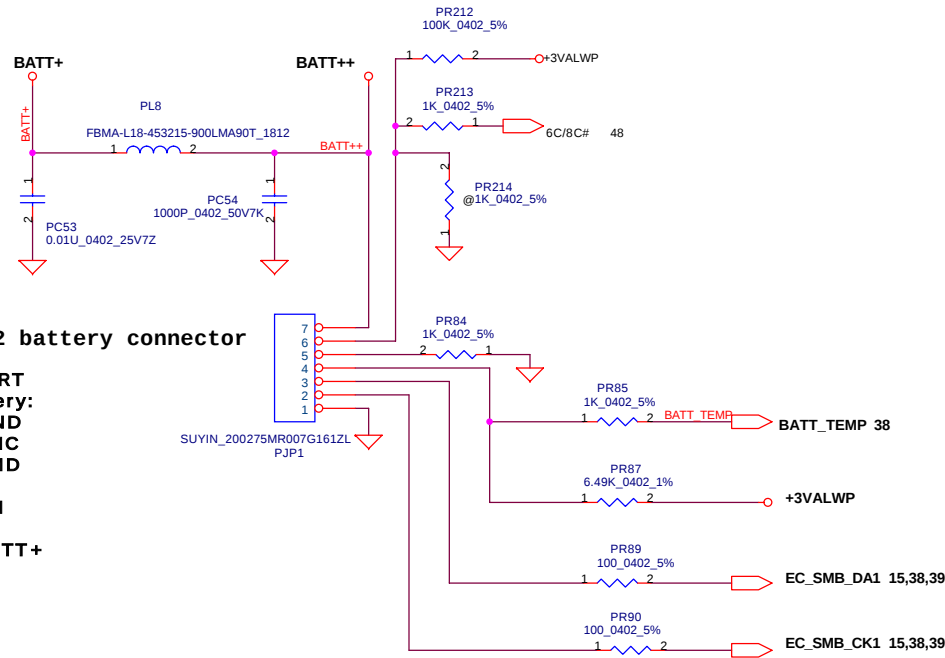
OVP voltage :

LI-3S :17.8V---BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+

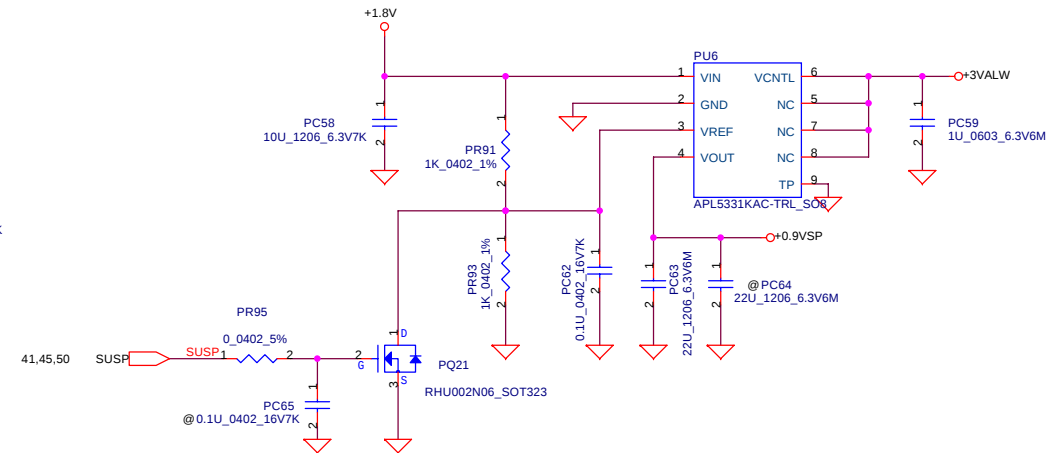
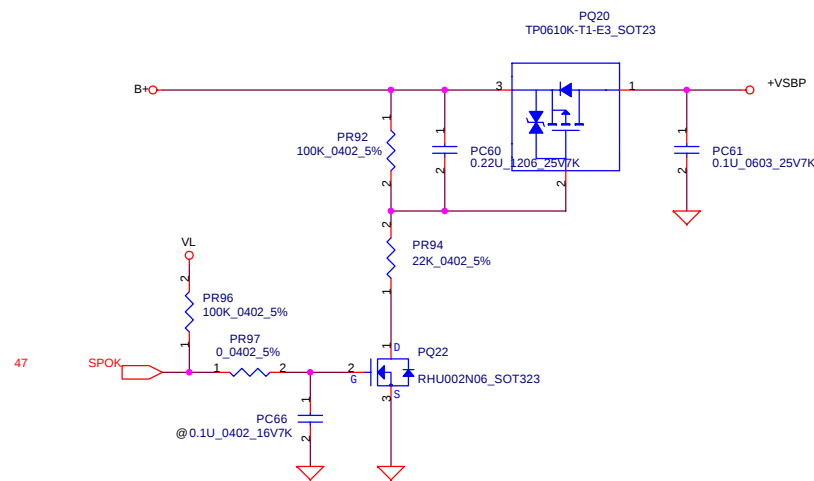
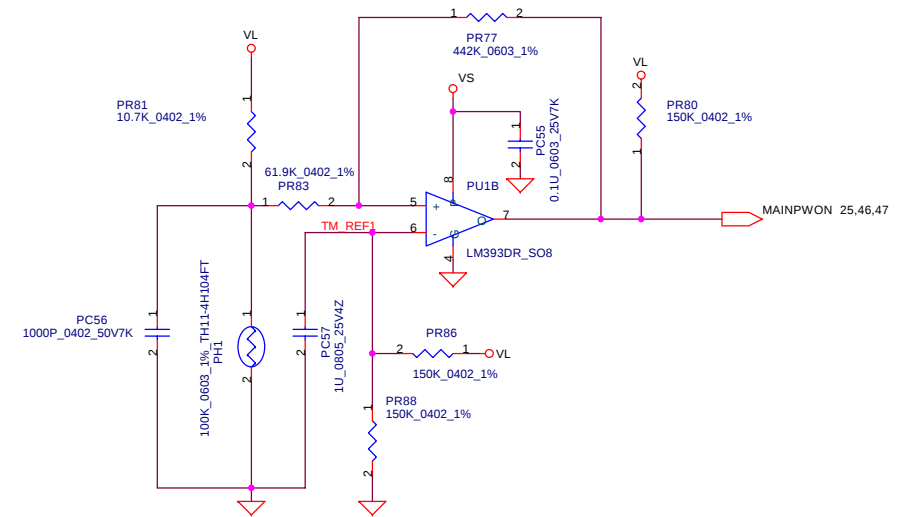
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PJP2 battery connector

SMART Battery:
1.GND
2.SMC
3.SMD
4.TS
5.B/I
6.ID
7.BATT+

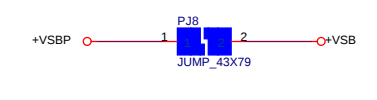
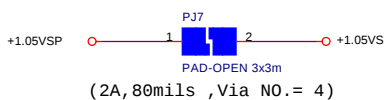
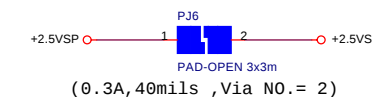
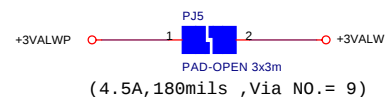
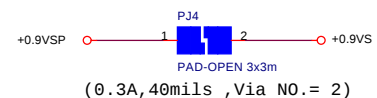
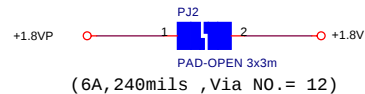
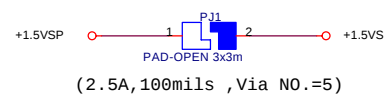


PH1 under CPU botten side :
CPU thermal protection at 80 degree C
Recovery at 44(45) degree C

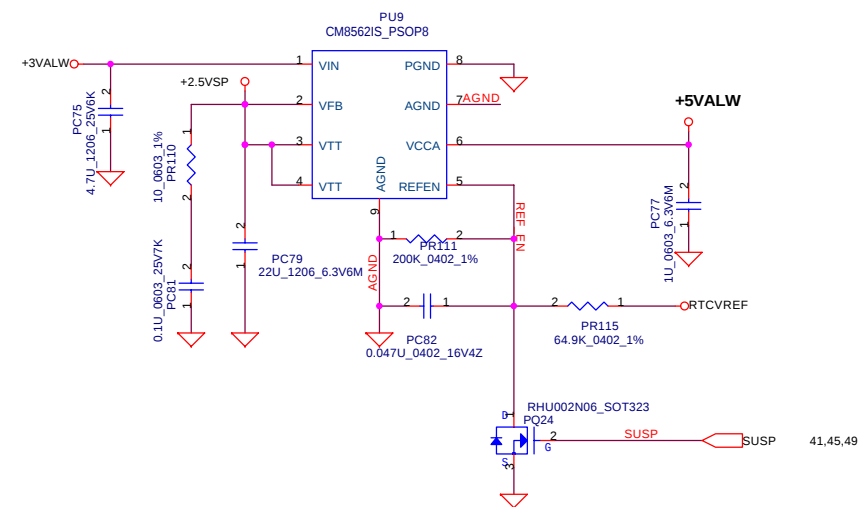
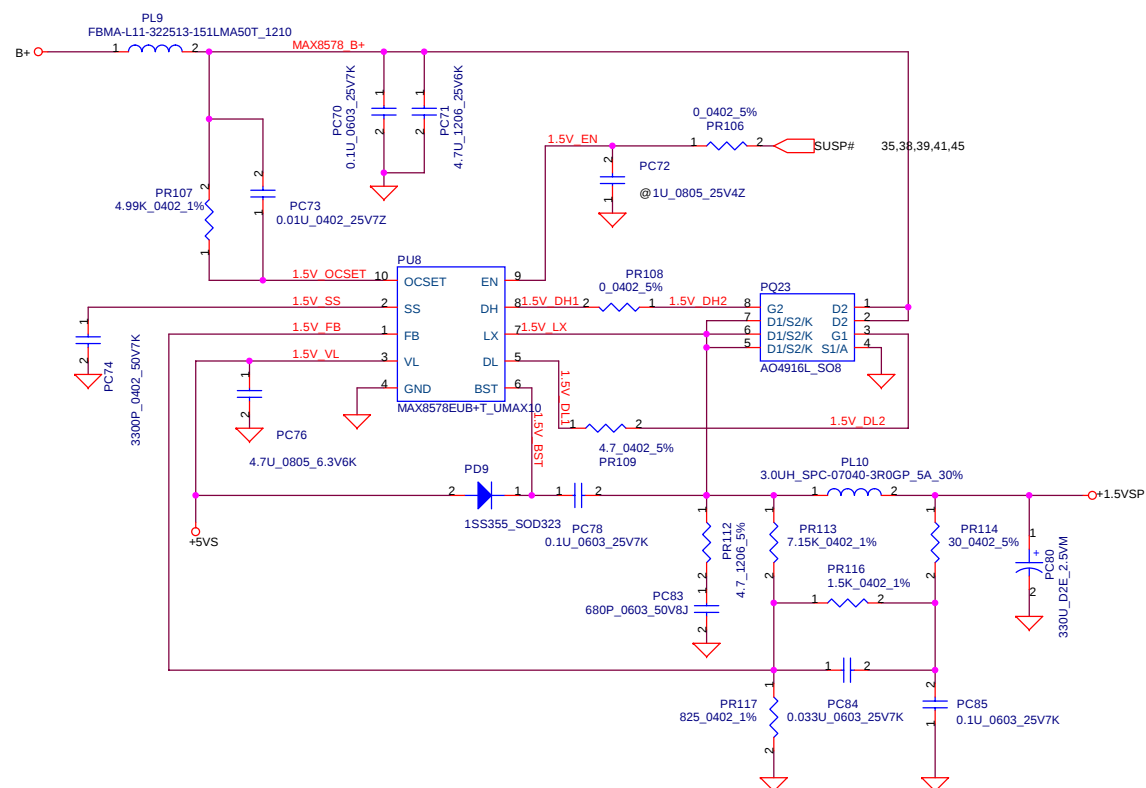
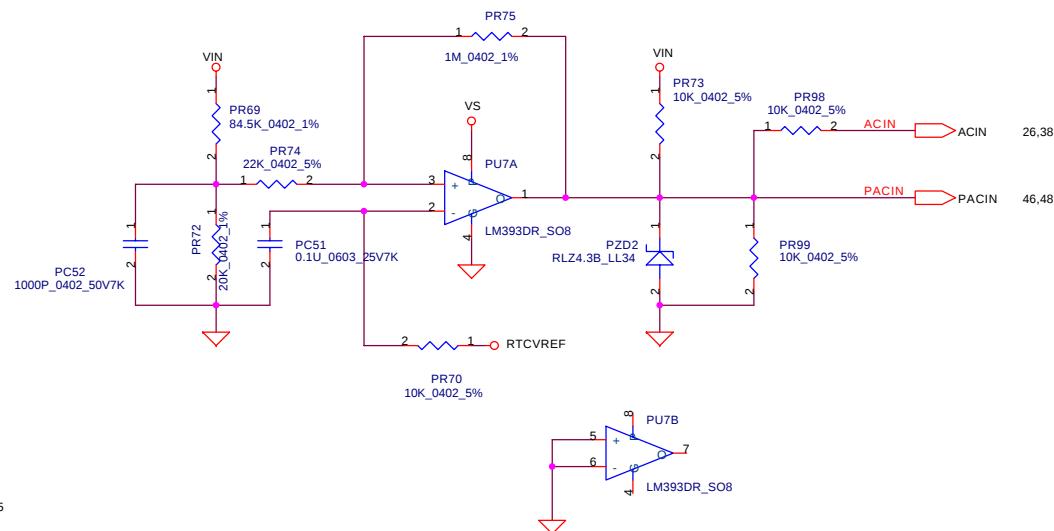


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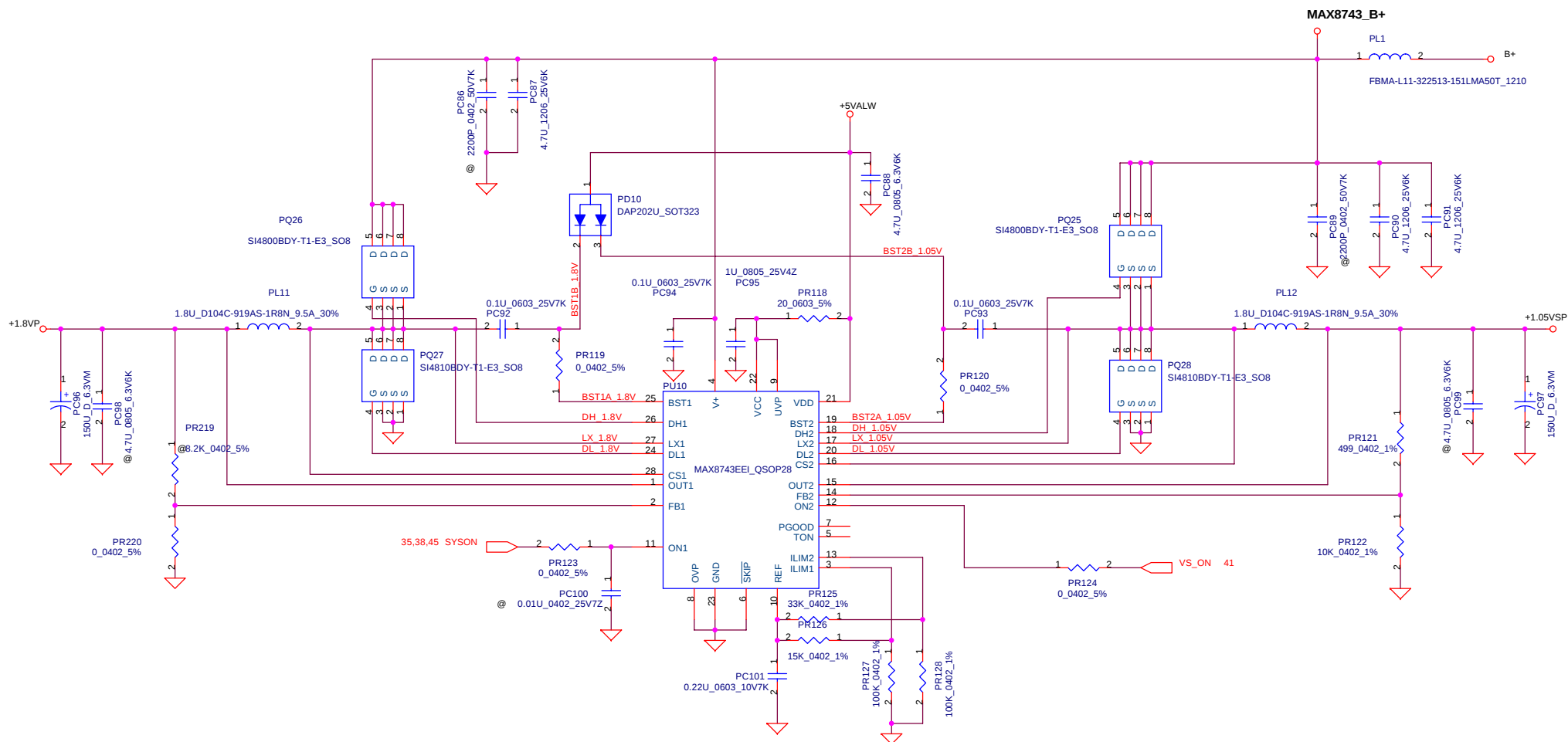
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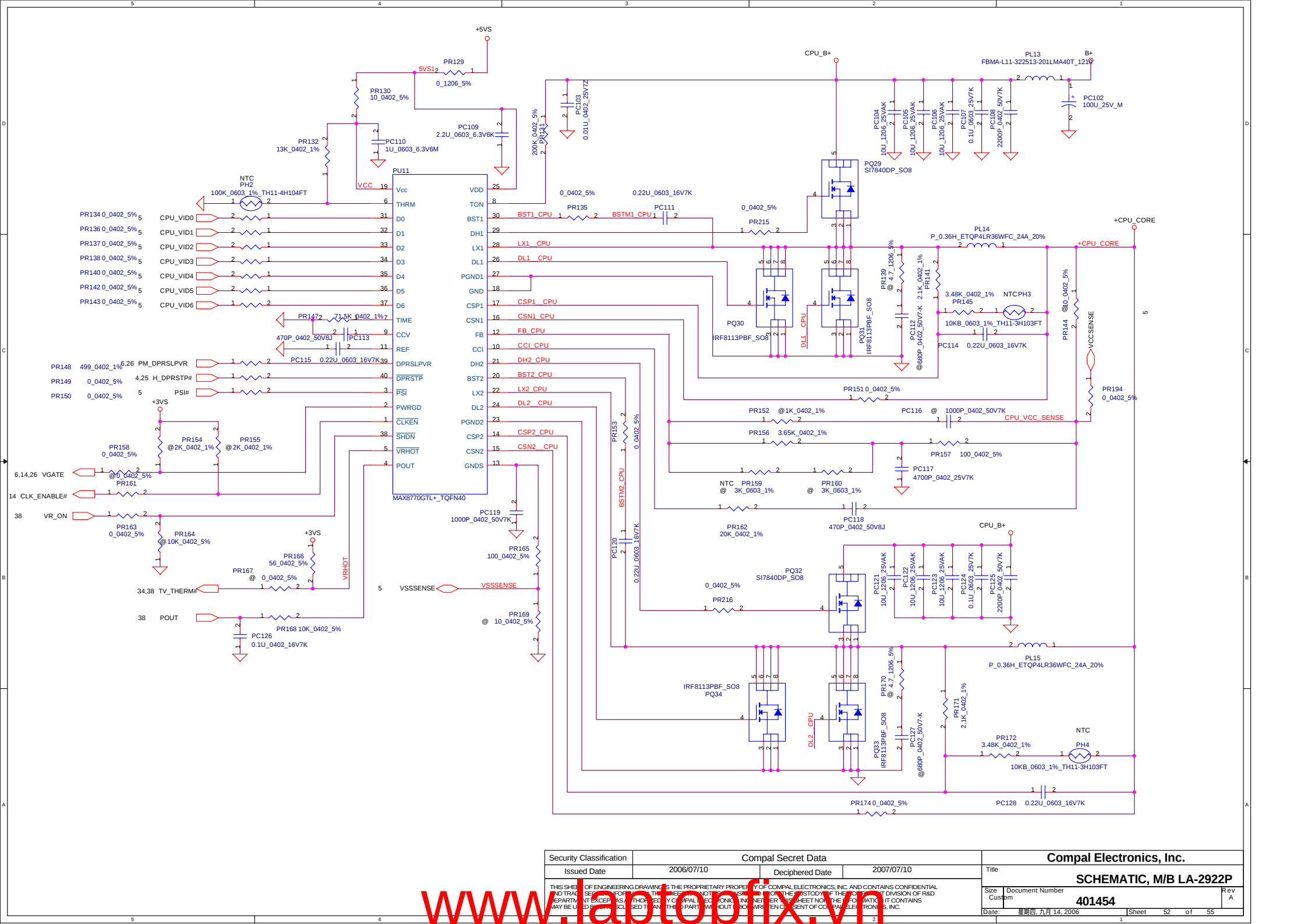
Vin Detector 17.90V/17.24V



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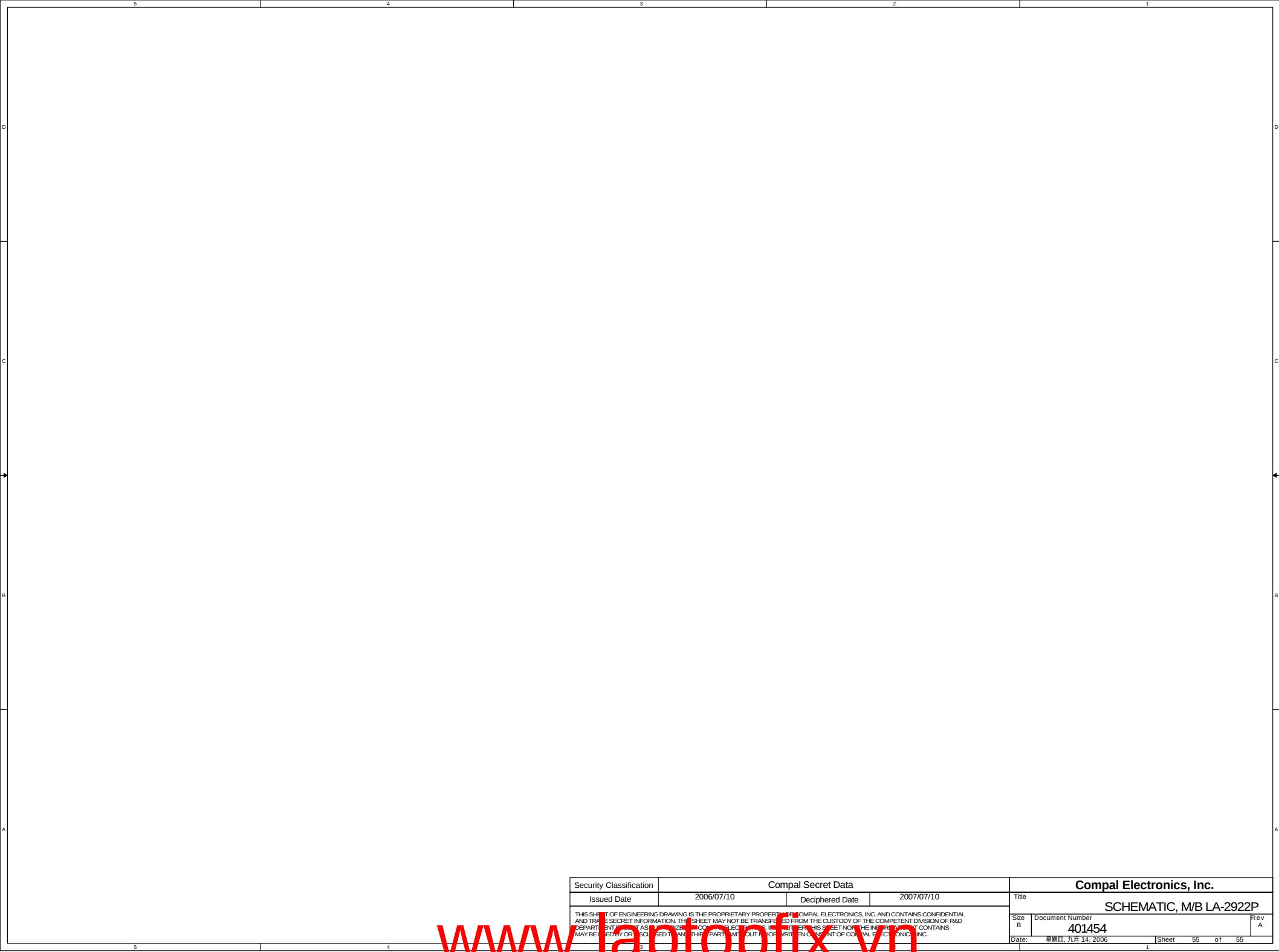


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Rev 0.1 --> Rev 1.0 Change List

- 1. Page15 : Change BOM structure of R831 to VGA@
- 2. Page17 : Add C1110 to C1120 on power plane for EMI Require.
- 3. Page26 : Add BOM structure @ on D38 & R887

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