Compal confidential

LC-Marseille 10AD

PWWAE LA-6843P Schematics Document

Mobile AMD S1G4/ RS880M / SB820M

2010-08-16 Rev. 1.0

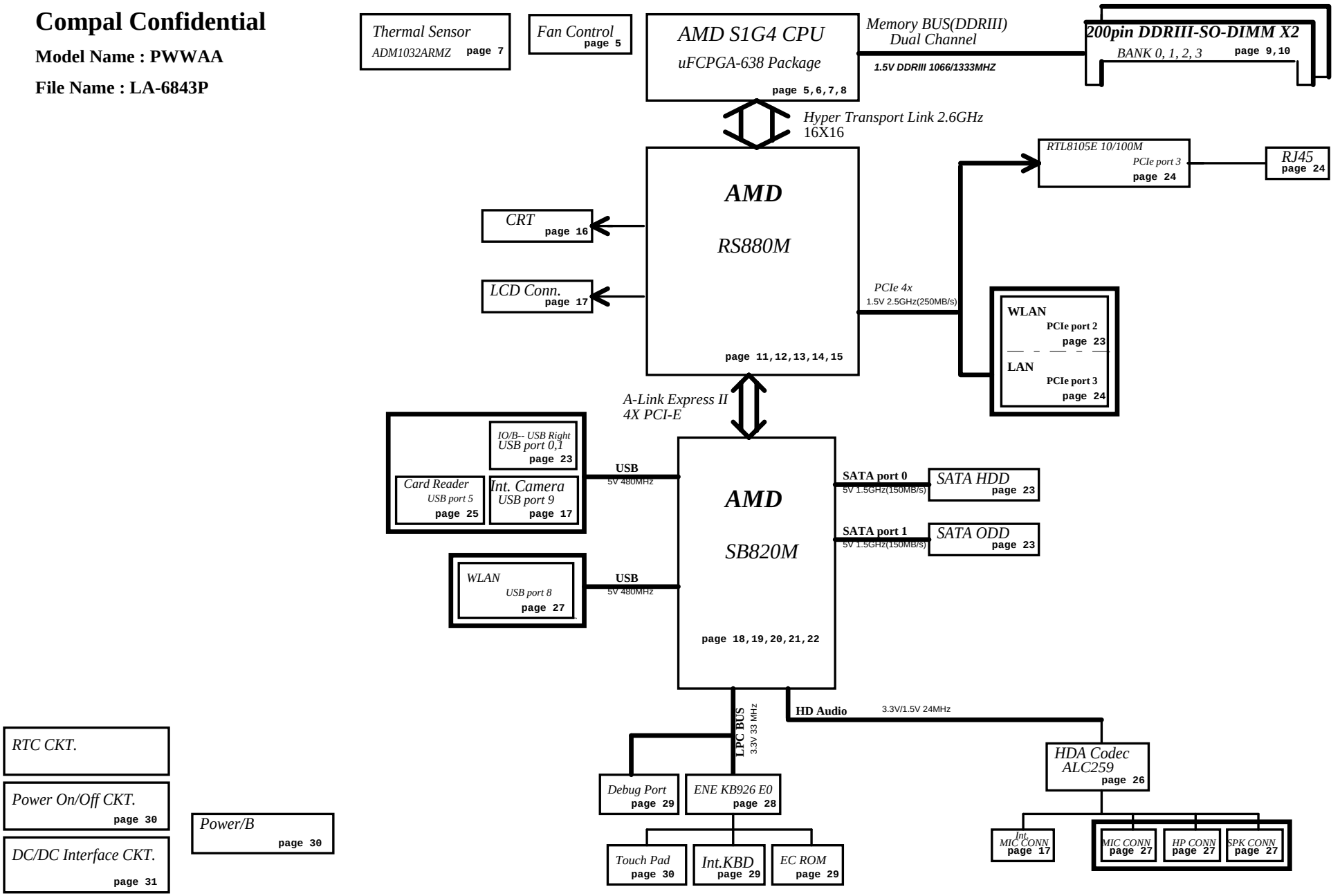
Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.		
Title	*SCHEMATICS,MB A6843*	
Size: Custom	Document Number *401982*	Rev B
Date: Wednesday, September 01, 2010	Sheet 1 of 40	

Compal Confidential

Model Name : PWWAA

File Name : LA-6843P



RTC CKT.

Power On/Off CKT. page 30

DC/DC Interface CKT. page 31

Power Circuit DC/DC page 31,32,33,34,35 36,37,38,39

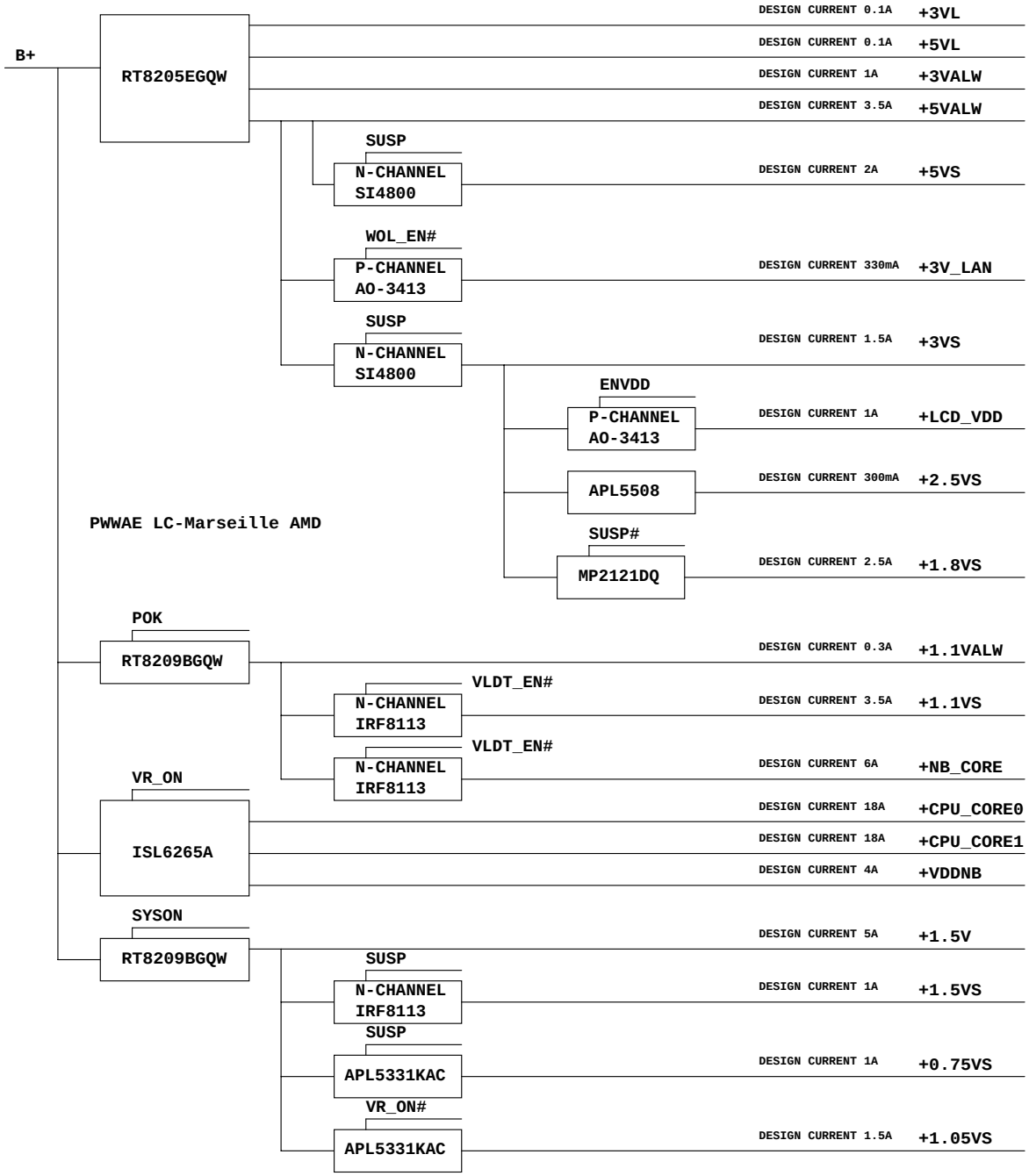
Power/B page 30

Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.

Title: **SCHEMATICS,MB A6843**

Size: Custom	Document Number: 401982	Rev: B
Date: Wednesday, September 01, 2010	Sheet 2 of 40	



Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.			
Title	SCHEMATICS,MB A6843		
Size: Custom	Document Number: 401982		Rev: B
Date: Wednesday, September 01, 2010	Sheet 3 of 40		

Voltage Rails

O : ON
X : OFF

power plane / State	+B +3VL +5VL +RTCVCC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +1.05VS +0.75VS +VGA_CORE +VDDNB +CPU_CORE
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Platform	CPU	NB	VGA	SB	Comment
Danube	S1G4	RS880M	NA	SB820M	

@ : just reserve , no build
SB820MR1@ : just reserve for SB820MR1 only
R3@ : just reserve for R3 only
CONN@ : just reserve for Connector only
CAM@ : just reserve for WebCam only
BT@ : just reserve for Blue Tooth only
880MR1@: just reserve for 880MR1 only
8105E_VC@: just reserve for 10/100 LAN VC version only
8105E_VB@: just reserve for 10/100 LAN VBversion only

BTO (Build-To-Order) Option Table

Function	Camera					
Description	(C)					
Explain						
BTO	CAM@					

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 0

SMBUS Control Table

	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM
EC_SMB_CK1 EC_SMB_DA1	KB926	V					
EC_SMB_CK2 EC_SMB_DA2	KB926		V				
I2C_CLK I2C_DATA	RS880M						V
DDC_CLK0 DDC_DATA0	RS880M						
SCL0 SDA0	SB820			V	V		
SCL1 SDA1	SB820					V	

EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
EC KB926E0		

EC SM Bus2 address

Device	HEX	Address
EMC1032-1 CPU	98H	1001 100X b
EC KB926E0		

Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.
Title: SCHEMATICS,MB A6843
Size: Custom | Document Number: 401982 | Rev: B
Date: Wednesday, September 01, 2010 | Sheet 4 of 40

+1.1VS

250 mil VLDT CAP. Near CPU Socket

C1 10U_0805_10V6K
C2 10U_0805_10V6K
C3 0.22U_0603_16V4Z
C4 0.22U_0603_16V4Z
C5 180P_0402_50V8J
C6 180P_0402_50V8J

<11> H_CADIP[0..15] H_CADIP[0..15]
<11> H_CADIN[0..15] H_CADIN[0..15]
H_CADOP[0..15] H_CADOP[0..15] <11>
H_CADON[0..15] H_CADON[0..15] <11>

+1.1VS

JCPUA

VLDT=500mA

HT LINK

D1	VLDT_A0	VLDT_B0	AE2		
D2	VLDT_A1	VLDT_B1	AE3		
D3	VLDT_A2	VLDT_B2	AE4		
D4	VLDT_A3	VLDT_B3	AE5		
H_CADIP0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	H_CADOP0
H_CADIN0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2
H_CADIP3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	H_CADOP3
H_CADIN3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	H_CADON3
H_CADIP4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	H_CADOP4
H_CADIN4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	H_CADON4
H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	H_CADON5
H_CADIP6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	H_CADOP6
H_CADIN6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	H_CADON6
H_CADIP7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	H_CADOP7
H_CADIN7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP8	F5	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIN8	E5	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9
H_CADIP10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	H_CADOP10
H_CADIN10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	H_CADON10
H_CADIP11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	H_CADOP11
H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	H_CADON12
H_CADIP13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	H_CADOP13
H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	H_CADON14
H_CADIP15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	H_CADON15
<11> H_CLKIP0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	H_CLKOP0 <11>
<11> H_CLKIN0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	H_CLKON0 <11>
<11> H_CLKIP1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	H_CLKOP1 <11>
<11> H_CLKIN1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	H_CLKON1 <11>
<11> H_CTLIP0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	H_CTLOP0 <11>
<11> H_CTLIN0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	H_CTLON0 <11>
<11> H_CTLIP1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	H_CTLOP1 <11>
<11> H_CTLIN1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	H_CTLON1 <11>

< From NB >

< To NB >

FOX_PZ6382A-284S-41F_Champlian
CONN@

+1.1VS

C7 10U_0805_10V6K

< VLDT_A & VLDT_B : HyperTransport I/O ring power >

< FAN Control Circuit : Vout = 1.6 x Vset >

+5VS

1A

+FAN1

C1120 10U_0805_10V4Z

C1119 10U_0805_10V4Z

U31

1	EN	GND	8
2	VIN	GND	7
3	VOUT	GND	6
4	VSET	GND	5

APL5607KI-TRG_SO8

<28> EN_DFAN1

@ C1121 1000P_0402_25V8J

+FAN1

JFAN

ACES_85204-0300N
CONN@

+3VS

R795 10K_0402_5%

FAN_SPEED1 <28>

@ C1122 0.01U_0402_25V7K

Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6843

Size: Custom | Document Number: 401982 | Rev: B

Date: Wednesday, September 01, 2010 | Sheet 5 of 40

< DDR2 VREF is 0.5 ratio >

< Close to CPU >

+1.5V

R1 1K_0402_1%

+MCH_REF

R2 1K_0402_1%

C9 0.1U_0402_16V7K

C8 1000P_0402_25V8

< Processor DDR3 Memory Interface >

JCPUC

MEM:DATA

<10> DDR_B_D[63..0]

< From/To SO_DIMMB >

DDR_B_D0 C11
DDR_B_D1 A11
DDR_B_D2 A14
DDR_B_D3 B14
DDR_B_D4 G11
DDR_B_D5 F11
DDR_B_D6 D12
DDR_B_D7 A13
DDR_B_D8 A15
DDR_B_D9 A16
DDR_B_D10 A19
DDR_B_D11 A20
DDR_B_D12 C14
DDR_B_D13 D14
DDR_B_D14 C18
DDR_B_D15 D18
DDR_B_D16 D20
DDR_B_D17 A21
DDR_B_D18 D24
DDR_B_D19 C25
DDR_B_D20 B20
DDR_B_D21 C20
DDR_B_D22 B24
DDR_B_D23 C24
DDR_B_D24 E23
DDR_B_D25 E24
DDR_B_D26 G25
DDR_B_D27 G26
DDR_B_D28 C26
DDR_B_D29 D26
DDR_B_D30 G23
DDR_B_D31 G24
DDR_B_D32 AA24
DDR_B_D33 AA23
DDR_B_D34 AD24
DDR_B_D35 AE24
DDR_B_D36 AA26
DDR_B_D37 AA25
DDR_B_D38 AD26
DDR_B_D39 AE25
DDR_B_D40 AC22
DDR_B_D41 AD22
DDR_B_D42 AE20
DDR_B_D43 AE20
DDR_B_D44 AE24
DDR_B_D45 AE23
DDR_B_D46 AC20
DDR_B_D47 AD20
DDR_B_D48 AD18
DDR_B_D49 AE18
DDR_B_D50 AC14
DDR_B_D51 AD14
DDR_B_D52 AE19
DDR_B_D53 AC18
DDR_B_D54 AE16
DDR_B_D55 AE15
DDR_B_D56 AE13
DDR_B_D57 AC12
DDR_B_D58 AB11
DDR_B_D59 Y11
DDR_B_D60 AE14
DDR_B_D61 AE14
DDR_B_D62 AE11
DDR_B_D63 AD11

MB_DATA0 MA_DATA0 G12 DDR_A_D0
MB_DATA1 MA_DATA1 F12 DDR_A_D1
MB_DATA2 MA_DATA2 H14 DDR_A_D2
MB_DATA3 MA_DATA3 G14 DDR_A_D3
MB_DATA4 MA_DATA4 H11 DDR_A_D4
MB_DATA5 MA_DATA5 H12 DDR_A_D5
MB_DATA6 MA_DATA6 C13 DDR_A_D6
MB_DATA7 MA_DATA7 F13 DDR_A_D7
MB_DATA8 MA_DATA8 H15 DDR_A_D8
MB_DATA9 MA_DATA9 E15 DDR_A_D9
MB_DATA10 MA_DATA10 E17 DDR_A_D10
MB_DATA11 MA_DATA11 H17 DDR_A_D11
MB_DATA12 MA_DATA12 E14 DDR_A_D12
MB_DATA13 MA_DATA13 F14 DDR_A_D13
MB_DATA14 MA_DATA14 C17 DDR_A_D14
MB_DATA15 MA_DATA15 G17 DDR_A_D15
MB_DATA16 MA_DATA16 G18 DDR_A_D16
MB_DATA17 MA_DATA17 C19 DDR_A_D17
MB_DATA18 MA_DATA18 D22 DDR_A_D18
MB_DATA19 MA_DATA19 E20 DDR_A_D19
MB_DATA20 MA_DATA20 J19 DDR_A_D20
MB_DATA21 MA_DATA21 E18 DDR_A_D21
MB_DATA22 MA_DATA22 B22 DDR_A_D22
MB_DATA23 MA_DATA23 C23 DDR_A_D23
MB_DATA24 MA_DATA24 F20 DDR_A_D24
MB_DATA25 MA_DATA25 F22 DDR_A_D25
MB_DATA26 MA_DATA26 H24 DDR_A_D26
MB_DATA27 MA_DATA27 J19 DDR_A_D27
MB_DATA28 MA_DATA28 F21 DDR_A_D28
MB_DATA29 MA_DATA29 E22 DDR_A_D29
MB_DATA30 MA_DATA30 H20 DDR_A_D30
MB_DATA31 MA_DATA31 H22 DDR_A_D31
MB_DATA32 MA_DATA32 Y24 DDR_A_D32
MB_DATA33 MA_DATA33 AB24 DDR_A_D33
MB_DATA34 MA_DATA34 AB22 DDR_A_D34
MB_DATA35 MA_DATA35 AA21 DDR_A_D35
MB_DATA36 MA_DATA36 W22 DDR_A_D36
MB_DATA37 MA_DATA37 W21 DDR_A_D37
MB_DATA38 MA_DATA38 Y22 DDR_A_D38
MB_DATA39 MA_DATA39 AA22 DDR_A_D39
MB_DATA40 MA_DATA40 Y20 DDR_A_D40
MB_DATA41 MA_DATA41 AA20 DDR_A_D41
MB_DATA42 MA_DATA42 AA18 DDR_A_D42
MB_DATA43 MA_DATA43 AB18 DDR_A_D43
MB_DATA44 MA_DATA44 AB21 DDR_A_D44
MB_DATA45 MA_DATA45 AD21 DDR_A_D45
MB_DATA46 MA_DATA46 AD19 DDR_A_D46
MB_DATA47 MA_DATA47 Y18 DDR_A_D47
MB_DATA48 MA_DATA48 AD17 DDR_A_D48
MB_DATA49 MA_DATA49 W16 DDR_A_D49
MB_DATA50 MA_DATA50 W14 DDR_A_D50
MB_DATA51 MA_DATA51 Y14 DDR_A_D51
MB_DATA52 MA_DATA52 Y17 DDR_A_D52
MB_DATA53 MA_DATA53 AB17 DDR_A_D53
MB_DATA54 MA_DATA54 AB15 DDR_A_D54
MB_DATA55 MA_DATA55 AD15 DDR_A_D55
MB_DATA56 MA_DATA56 AB13 DDR_A_D56
MB_DATA57 MA_DATA57 AD13 DDR_A_D57
MB_DATA58 MA_DATA58 Y12 DDR_A_D58
MB_DATA59 MA_DATA59 W11 DDR_A_D59
MB_DATA60 MA_DATA60 AB14 DDR_A_D60
MB_DATA61 MA_DATA61 AA14 DDR_A_D61
MB_DATA62 MA_DATA62 AB12 DDR_A_D62
MB_DATA63 MA_DATA63 AA12 DDR_A_D63

DDR_A_D[63..0] <9>

< From/To SO_DIMMA >

<10> DDR_B_DM[7..0]

< To SO_DIMMB >

DDR_B_DM0 A12
DDR_B_DM1 B16
DDR_B_DM2 A22
DDR_B_DM3 F25
DDR_B_DM4 AB26
DDR_B_DM5 AE22
DDR_B_DM6 AC16
DDR_B_DM7 AD12

MB_DM0 MA_DM0 F12 DDR_A_DM0
MB_DM1 MA_DM1 C15 DDR_A_DM1
MB_DM2 MA_DM2 E19 DDR_A_DM2
MB_DM3 MA_DM3 F24 DDR_A_DM3
MB_DM4 MA_DM4 AC24 DDR_A_DM4
MB_DM5 MA_DM5 Y19 DDR_A_DM5
MB_DM6 MA_DM6 AB16 DDR_A_DM6
MB_DM7 MA_DM7 Y13 DDR_A_DM7

DDR_A_DM[7..0] <9>

< To SO_DIMMA >

<10> DDR_B_DQS0
<10> DDR_B_DQS#0
<10> DDR_B_DQS1
<10> DDR_B_DQS#1
<10> DDR_B_DQS2
<10> DDR_B_DQS#2
<10> DDR_B_DQS3
<10> DDR_B_DQS#3
<10> DDR_B_DQS4
<10> DDR_B_DQS#4
<10> DDR_B_DQS5
<10> DDR_B_DQS#5
<10> DDR_B_DQS6
<10> DDR_B_DQS#6
<10> DDR_B_DQS7
<10> DDR_B_DQS#7

DDR_B_DQS0 C12
DDR_B_DQS#0 B12
DDR_B_DQS1 D16
DDR_B_DQS#1 C16
DDR_B_DQS2 A24
DDR_B_DQS#2 A23
DDR_B_DQS3 F26
DDR_B_DQS#3 F26
DDR_B_DQS4 AC25
DDR_B_DQS#4 AC26
DDR_B_DQS5 AF21
DDR_B_DQS#5 AE22
DDR_B_DQS6 AE16
DDR_B_DQS#6 AD16
DDR_B_DQS7 AE12
DDR_B_DQS#7 AE12

MB_DQS_H0 MA_DQS_H0 G13 DDR_A_DQS0
MB_DQS_L0 MA_DQS_L0 H13 DDR_A_DQS#0
MB_DQS_H1 MA_DQS_H1 G16 DDR_A_DQS1
MB_DQS_L1 MA_DQS_L1 G15 DDR_A_DQS#1
MB_DQS_H2 MA_DQS_H2 C22 DDR_A_DQS2
MB_DQS_L2 MA_DQS_L2 C21 DDR_A_DQS#2
MB_DQS_H3 MA_DQS_H3 G22 DDR_A_DQS3
MB_DQS_L3 MA_DQS_L3 G21 DDR_A_DQS#3
MB_DQS_H4 MA_DQS_H4 AD23 DDR_A_DQS4
MB_DQS_L4 MA_DQS_L4 AC23 DDR_A_DQS#4
MB_DQS_H5 MA_DQS_H5 AB19 DDR_A_DQS5
MB_DQS_L5 MA_DQS_L5 AB20 DDR_A_DQS#5
MB_DQS_H6 MA_DQS_H6 Y15 DDR_A_DQS6
MB_DQS_L6 MA_DQS_L6 W15 DDR_A_DQS#6
MB_DQS_H7 MA_DQS_H7 W12 DDR_A_DQS7
MB_DQS_L7 MA_DQS_L7 W13 DDR_A_DQS#7

DDR_A_DQS0 <9>
DDR_A_DQS#0 <9>
DDR_A_DQS1 <9>
DDR_A_DQS#1 <9>
DDR_A_DQS2 <9>
DDR_A_DQS#2 <9>
DDR_A_DQS3 <9>
DDR_A_DQS#3 <9>
DDR_A_DQS4 <9>
DDR_A_DQS#4 <9>
DDR_A_DQS5 <9>
DDR_A_DQS#5 <9>
DDR_A_DQS6 <9>
DDR_A_DQS#6 <9>
DDR_A_DQS7 <9>
DDR_A_DQS#7 <9>

< From/To SO_DIMMA >

< From/To SO_DIMMB >

FOX_PZ6382A-284S-41F_Champlian
CONN@

Place them close to CPU within 1"

+1.05VS

JCPUB

MEM:CMD/CTRL/CLK

+1.05VS

< VTT regulator voltage >

R4 39.2_0402_1% MEM_P

R5 39.2_0402_1% MEM_N

+1.5V

<9> MEM_MA_RST#

MEM_MA_RST# H16

PAD T1

< To SO_DIMMA >

DDR_A_ODT0 T19
DDR_A_ODT1 V22

DDR_CS0_DIMMA# T20
DDR_CS1_DIMMA# U19

DDR_CKE0_DIMMA J22
DDR_CKE1_DIMMA J20

DDR_A_CLK0 N19
DDR_A_CLK0 N20

DDR_A_CLK1 P19
DDR_A_CLK#1 P20

DDR_A_MA[15..0]

DDR_A_MA0 N21
DDR_A_MA1 M20
DDR_A_MA2 N22
DDR_A_MA3 M19
DDR_A_MA4 M22
DDR_A_MA5 L20
DDR_A_MA6 M24
DDR_A_MA7 L21
DDR_A_MA8 L19
DDR_A_MA9 K22
DDR_A_MA10 R21
DDR_A_MA11 L22
DDR_A_MA12 K20
DDR_A_MA13 V24
DDR_A_MA14 K24
DDR_A_MA15 K19

DDR_A_BS#0 R20
DDR_A_BS#1 R23
DDR_A_BS#2 J21

DDR_A_RAS# R19
DDR_A_CAS# T22
DDR_A_WE# T24

MEMZP AE10
MEMZN AE10

MA_RESET_L

MA0_ODT0
MA0_ODT1
MA1_ODT0
MA1_ODT1

MA0_CS_L0
MA0_CS_L1
MA1_CS_L0
MA1_CS_L1

MA_CKE0
MA_CKE1

MA_CLK_H5
MA_CLK_L5
MA_CLK_H1
MA_CLK_L1
MA_CLK_H7
MA_CLK_L7
MA_CLK_H4
MA_CLK_L4

MA_ADD0
MA_ADD1
MA_ADD2
MA_ADD3
MA_ADD4
MA_ADD5
MA_ADD6
MA_ADD7
MA_ADD8
MA_ADD9
MA_ADD10
MA_ADD11
MA_ADD12
MA_ADD13
MA_ADD14
MA_ADD15

MA_BANK0
MA_BANK1
MA_BANK2

MA_RAS_L
MA_CAS_L
MA_WE_L

VDDR1 D10
VDDR2 C10
VDDR3 B10
VDDR4 AD10

VDDR5 W10
VDDR6 AC10
VDDR7 AB10
VDDR8 AA10
VDDR9 A10

VDDR_SENSE Y10 VTT_SENSE

MEMVREF W17 +MCH_REF

MB_RESET_L B18 MEM_MB_RST#

MEM_MB_RST# <10>

MB0_ODT0 W26 DDR_B_ODT0
MB0_ODT1 W23 DDR_B_ODT1
MB1_ODT0 Y26

DDR_B_ODT0 <10>
DDR_B_ODT1 <10>

MB0_CS_L0 V26 DDR_CS0_DIMMB#
MB0_CS_L1 W25 DDR_CS1_DIMMB#
MB1_CS_L0 U22

DDR_CS0_DIMMB# <10>
DDR_CS1_DIMMB# <10>

MB_CKE0 J25 DDR_CKE0_DIMMB
MB_CKE1 H26 DDR_CKE1_DIMMB

DDR_CKE0_DIMMB <10>
DDR_CKE1_DIMMB <10>

MB_CLK_H5 P22 DDR_B_CLK0
MB_CLK_L5 R22 DDR_B_CLK#0
MB_CLK_H1 A17
MB_CLK_L1 A18
MB_CLK_H7 AF18
MB_CLK_L7 AF17
MB_CLK_H4 R26 DDR_B_CLK1
MB_CLK_L4 R25 DDR_B_CLK#1

DDR_B_CLK0 <10>
DDR_B_CLK#0 <10>
DDR_B_CLK1 <10>
DDR_B_CLK#1 <10>
DDR_B_MA[15..0] <10>

MB_ADD0 P24 DDR_B_MA0
MB_ADD1 N24 DDR_B_MA1
MB_ADD2 P26 DDR_B_MA2
MB_ADD3 N23 DDR_B_MA3
MB_ADD4 N26 DDR_B_MA4
MB_ADD5 L23 DDR_B_MA5
MB_ADD6 N25 DDR_B_MA6
MB_ADD7 L24 DDR_B_MA7
MB_ADD8 M26 DDR_B_MA8
MB_ADD9 K26 DDR_B_MA9
MB_ADD10 T26 DDR_B_MA10
MB_ADD11 L26 DDR_B_MA11
MB_ADD12 L25 DDR_B_MA12
MB_ADD13 W24 DDR_B_MA13
MB_ADD14 J23 DDR_B_MA14
MB_ADD15 J24 DDR_B_MA15

MB_BANK0 R24 DDR_B_BS#0
MB_BANK1 U26 DDR_B_BS#1
MB_BANK2 J26 DDR_B_BS#2

DDR_B_BS#0 <10>
DDR_B_BS#1 <10>
DDR_B_BS#2 <10>

MB_RAS_L U25 DDR_B_RAS#
MB_CAS_L U24 DDR_B_CAS#
MB_WE_L U23 DDR_B_WE#

DDR_B_RAS# <10>
DDR_B_CAS# <10>
DDR_B_WE# <10>

< To SO_DIMMB >

FOX_PZ6382A-284S-41F_Champlian
CONN@

Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6843

Size: Custom | Document Number: 401982 | Rev: B

Date: Wednesday, September 01, 2010 | Sheet 6 of 40

< Filtered PLL Supply Voltage >

+2.5VS — L1 FBM_L11_201209_300L_0805 — VDDA=300mA — +2.5VDDA

C11 150U_B2_6.3VM_R45M (@)

C12 4.7U_0805_10V4Z

C13 3300P_0402_50V7K

C14 0.22U_0603_16V4Z

< 200-MHz PLL Reference Clock >

<18> CLK_CPU_BCLK — C16 3900P_0402_50V7K — CPU_CLKIN_SC_P

R10 169_0402_1%

<18> CLK_CPU_BCLK# — C15 3900P_0402_50V7K — CPU_CLKIN_SC_N

Address:100_1100 Place close to CPU wihtin 1.5"

JCPUD

+2.5VDDA	F8 VDDA1	VSS	M11
	F9 VDDA2	RSVD11	W18
CPU_CLKIN_SC_P	A9 CLKIN_H	SVC	A6 CPU_SVC
CPU_CLKIN_SC_N	A8 CLKIN_L	SVD	A4 CPU_SVD
LDT_RST#	B7 RESET_L		
H_PWRGD	A7 PWROK		
LDT_STOP#	F10 LDTSTOP_L	THERMTRIP_L	AF6 CPU_THERMTRIP#
T2 PAD	C6 LDTREQ_L	PROCHOT_L	AC7 CPU_PROCHOT#
		MEMHOT_L	AA8 PAD T3
+1.5V R12 1K_0402_5% CPU_SIC	AF4 SIC		
+1.5V R14 1K_0402_5% CPU_SID	AF5 SID		
	AF6 ALERT_L	THERMDC	W7 THERMDC_CPU
		THERMDA	W8 THERMDA_CPU
+1.1VS R15 44.2_0402_1% CPU_HTREF0	R6 HT_REF0		
R16 44.2_0402_1% CPU_HTREF1	P6 HT_REF1		
<38> CPU_VDD0_RUN_FB_H	CPU_VDD0_RUN_FB_H F6 VDD0_FB_H	VDDIO_FB_H	W9 PAD T15
<38> CPU_VDD0_RUN_FB_L	CPU_VDD0_RUN_FB_L E6 VDD0_FB_L	VDDIO_FB_L	Y9 PAD T16
	Y6 VDD1_FB_H	VDDNB_FB_H	H6 CPU_VDDNB_RUN_FB_H
	AB6 VDD1_FB_L	VDDNB_FB_L	G6 CPU_VDDNB_RUN_FB_L
CPU_DBRDY	G10 DBRDY		
CPU_TMS	AA9 TMS	DBREQ_L	F10 CPU_DBREQ#
CPU_TCK	AC9 TCK		
CPU_TRST#	AD9 TRST_L	TDO	AF9 CPU_TDO
CPU_TDI	AF9 TDI		
CPU_TEST23	AD7 TEST23	TEST28_H	J7
		TEST28_L	H8
CPU_TEST18	H10 TEST18		
CPU_TEST19	G9 TEST19	TEST17	D7 CPU_TEST17 PAD T4
		TEST16	F7 CPU_TEST16 PAD T5
CPU_TEST25H	F9	TEST15	F7 CPU_TEST15 PAD T6
CPU_TEST25L	E8 TEST25_L	TEST14	C7 CPU_TEST14 PAD T7
CPU_TEST21	AB8 TEST21	TEST7	C3
CPU_TEST20	AE7 TEST20	TEST10	K8
CPU_TEST24	AE7 TEST24		
CPU_TEST22	AE8 TEST22	TEST8	C4
CPU_TEST12	AC8 TEST12		
CPU_TEST27	AE8 TEST27		
		TEST29_H	C9 CPU_TEST29_H_FBCLKOUT_P
R24 0_0402_5%	C2 TEST9	TEST29_L	C8 CPU_TEST29_L_FBCLKOUT_N
	AA6 TEST6		R25 80.6_0402_1%
	A3 RSVD1	RSVD10	H18
	A5 RSVD2	RSVD9	H19
	B3 RSVD3	RSVD8	AA7
	B5 RSVD4	RSVD7	D5
	C1 RSVD5	RSVD6	C5

FOX_PZ6382A-284S-41F_Champlian
CONN@

< Serial VID Interface clock & data >

route as differential as short as possible testpoint under package

+1.5V — R11 300_0402_5% — CPU_PROCHOT# — @R13 0_0402_5% — H_PROCHOT# <18>

CPU_SVC 1K_0402_5% R19 — +1.5V

CPU_SVD 1K_0402_5% R20 — +1.5V

CPU_SVC <38>

CPU_SVD <38>

CPU_VDDNB_RUN_FB_H <38>

CPU_VDDNB_RUN_FB_L <38>

+1.5V — R6 10K_0402_5% — R7 1K_0402_5% — Q1 MMBT3904_NL_SOT23-3

CPU_THERMTRIP#_R — H_THERMTRIP# <19>

+1.5V

R22 510_0402_5% CPU_TEST25H

R28 1K_0402_5% CPU_TEST27

R27 510_0402_5% CPU_TEST25L

R29 1K_0402_5% CPU_TEST12

R30 1K_0402_5% CPU_TEST18

R31 1K_0402_5% CPU_TEST19

R32 1K_0402_5% CPU_TEST20

R33 1K_0402_5% CPU_TEST21

R34 1K_0402_5% CPU_TEST22

R265 1K_0402_5% CPU_TEST23

R35 1K_0402_5% CPU_TEST24

+1.5VS — R17 300_0402_5% — <18> LDT_RST# — LDT_RST# — @C17 0.01U_0402_25V7K

+1.5VS — R21 300_0402_5% — <18,38> H_PWRGD — H_PWRGD — @C19 0.1U_0402_16V7K

+1.5VS — R18 300_0402_5% — <12,18> LDT_STOP# — LDT_STOP# — @C18 0.01U_0402_25V7K

< HDT Connector >

JP2

+1.5V — R40 300_0402_5% — CPU_DBREQ#

CPU_DBRDY

R39 220_0402_5% — CPU_TCK

R38 220_0402_5% — CPU_TMS

R37 220_0402_5% — CPU_TDI

+1.5V — R36 220_0402_5% — CPU_TRST#

CPU_TDO

+1.5V — LDT_RST#

SAMTEC_ASP-68200-07
CONN@

< Thermal Sensor >

+3VS — C20 0.1U_0402_16V7K

U1 EMC1402-1-ACZL-TR_MSOP8

VDD — THERMDA_CPU — DP — THERMDC_CPU — DN — CPU_THERM# — THERM#

C21 2200P_0402_50V7K (@)

R44 10K_0402_5% — +3VS

SMCLK — EC_SMB_CK2 <28>

SMDATA — EC_SMB_DA2 <28>

ALERT# — R41 10K_0402_5% (@) — +3VS

GND

Address:0100_1100 EMC1402-1
Address:0100_1101 EMC1402-2

3/30 Change U1 ADM1032 to EMC1402 for cost down

Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6843

Size	Document Number	Rev
Custom	401982	B

Date: Wednesday, September 01, 2010 Sheet 7 of 40

VDD decoupling : +CPU_CORE

+CPU_CORE

C26 330U_X_2VM_R6M
C90 330U_6.3V_M_R15 @
C25 330U_X_2VM_R6M
C96 330U_6.3V_M_R15 @
Near CPU Socket

C35 C34 C28 C29 — 22U_0805_6.3V6M
Under CPU Socket

C36 0.22U_0603_16V4Z
C37 0.01U_0402_25V7K
C38 180P_0402_50V8J
Under CPU Socket

C23 330U_X_2VM_R6M @
C89 330U_6.3V_M_R15 @
C24 330U_X_2VM_R6M @
C95 330U_6.3V_M_R15 @
Near CPU Socket

C30 C31 C32 C33 — 22U_0805_6.3V6M
Under CPU Socket

C39 0.22U_0603_16V4Z
C40 0.01U_0402_25V7K
C41 180P_0402_50V8J
Under CPU Socket

VDDIO decoupling : DDR SDRAM I/O ring power

+1.5V

C44 C45 22U_0805_6.3V6M
C46 C47 0.22U_0603_16V4Z
C48 180P_0402_50V8J
C50 180P_0402_50V8J
Under CPU Socket

C54 C51 C52 C53 — 0.22U_0603_16V4Z
Between CPU Socket and DIMM

C64 0.01U_0402_25V7K
C65 0.01U_0402_25V7K
Between CPU Socket and DIMM

180PF Qt'y follow the distance between CPU socket and DIMM0. <2.5inch>
C66 C67 C68 C69 — 180P_0402_50V8J
Between CPU Socket and DIMM

C71 C72 C73 C74 — 4.7U_0805_10V4Z
Between CPU Socket and DIMM

C56 Co-layout with C75
@ C75 330U_D2E_2.5VM_R6M
C56 390U_2.5V_M_R10

VDDR decoupling.

+1.05VS

C57 C58 4.7U_0805_10V4Z
C59 C60 0.22U_0603_16V4Z
C61 1000P_0402_25V8J
C62 1000P_0402_25V8J
C63 180P_0402_50V8J
C70 180P_0402_50V8J
Near CPU Socket Right side

C76 C77 4.7U_0805_10V4Z
C78 C79 0.22U_0603_16V4Z
C80 1000P_0402_25V8J
C81 1000P_0402_25V8J
C82 180P_0402_50V8J
C83 180P_0402_50V8J
Near CPU Socket Left side

C1124 Co-layout with C1125
@ C1125 330U_D2E_2.5VM
C1124 390U_2.5V_M_R10

+VDDNB decoupling : Northbridge power

+VDDNB

C42 C43 C49 — 22U_0805_6.3V6M

JCPUE

+CPU_CORE

G4	VDD0_1	VDD1_1	P8
H2	VDD0_2	VDD1_2	P10
J9	VDD0_3	VDD1_3	R4
J11	VDD0_4	VDD1_4	R7
J13	VDD0_5	VDD1_5	R9
J15	VDD0_6	VDD1_6	R11
K6	VDD0_7	VDD1_7	T2
K10	VDD0_8	VDD1_8	T6
K12	VDD0_9	VDD1_9	T8
K14	VDD0_10	VDD1_10	T10
L4	VDD0_11	VDD1_11	T12
L7	VDD0_12	VDD1_12	T14
L9	VDD0_13	VDD1_13	U7
L11	VDD0_14	VDD1_14	U9
L13	VDD0_15	VDD1_15	U11
L15	VDD0_16	VDD1_16	U13
M2	VDD0_17	VDD1_17	U15
M6	VDD0_18	VDD1_18	V6
M8	VDD0_19	VDD1_19	V8
M10	VDD0_20	VDD1_20	V10
N7	VDD0_21	VDD1_21	V12
N9	VDD0_22	VDD1_22	V14
N11	VDD0_23	VDD1_23	W4
		VDD1_24	Y2
K16	VDDNB_1	VDD1_25	AC4
M16	VDDNB_2	VDD1_26	AD2
P16	VDDNB_3		
T16	VDDNB_4	VDDIO27	Y25
V16	VDDNB_5	VDDIO26	V25
		VDDIO25	V23
H25	VDDIO1	VDDIO24	V21
J17	VDDIO2	VDDIO23	V18
K18	VDDIO3	VDDIO22	U17
K21	VDDIO4	VDDIO21	T25
K23	VDDIO5	VDDIO20	T23
K25	VDDIO6	VDDIO19	T21
L17	VDDIO7	VDDIO18	T18
M18	VDDIO8	VDDIO17	R17
M21	VDDIO9	VDDIO16	P25
M23	VDDIO10	VDDIO15	P23
M25	VDDIO11	VDDIO14	P21
N17	VDDIO12	VDDIO13	P18

+VDDNB
+1.5V
+1.5V
+CPU_CORE

FOX_PZ6382A-284S-41F_Champlian
CONN@

JCPUF

AA4	VSS1	VSS66	J6
AA11	VSS2	VSS67	J8
AA13	VSS3	VSS68	J10
AA15	VSS4	VSS69	J12
AA17	VSS5	VSS70	J14
AA19	VSS6	VSS71	J16
AB2	VSS7	VSS72	J18
AB7	VSS8	VSS73	K2
AB9	VSS9	VSS74	K7
AB23	VSS10	VSS75	K9
AB25	VSS11	VSS76	K11
AC11	VSS12	VSS77	K13
AC13	VSS13	VSS78	K15
AC15	VSS14	VSS79	K17
AC17	VSS15	VSS80	L6
AC19	VSS16	VSS81	L8
AC21	VSS17	VSS82	L10
AD6	VSS18	VSS83	L12
AD8	VSS19	VSS84	L14
AD25	VSS20	VSS85	L16
AE11	VSS21	VSS86	L18
AE13	VSS22	VSS87	M7
AE15	VSS23	VSS88	M9
AE17	VSS24	VSS89	AC6
AE19	VSS25	VSS90	M17
AE21	VSS26	VSS91	N4
AE23	VSS27	VSS92	N8
B4	VSS28	VSS93	N10
B6	VSS29	VSS94	N16
B8	VSS30	VSS95	N18
B9	VSS31	VSS96	P2
B11	VSS32	VSS97	P7
B13	VSS33	VSS98	P9
B15	VSS34	VSS99	P11
B17	VSS35	VSS100	P17
B19	VSS36	VSS101	R8
B21	VSS37	VSS102	R10
B23	VSS38	VSS103	R16
B25	VSS39	VSS104	R18
D6	VSS40	VSS105	T7
D8	VSS41	VSS106	T9
D9	VSS42	VSS107	T11
D11	VSS43	VSS108	T13
D13	VSS44	VSS109	T15
D15	VSS45	VSS110	T17
D17	VSS46	VSS111	U4
D19	VSS47	VSS112	U6
D21	VSS48	VSS113	U8
D23	VSS49	VSS114	U10
D25	VSS50	VSS115	U12
E4	VSS51	VSS116	U14
F2	VSS52	VSS117	U16
F11	VSS53	VSS118	U18
F13	VSS54	VSS119	V2
F15	VSS55	VSS120	V7
F17	VSS56	VSS121	V9
F19	VSS57	VSS122	V11
F21	VSS58	VSS123	V13
F23	VSS59	VSS124	V15
F25	VSS60	VSS125	V17
H7	VSS61	VSS126	W6
H9	VSS62	VSS127	Y21
H21	VSS63	VSS128	Y23
H23	VSS64	VSS129	N6
J4	VSS65		

FOX_PZ6382A-284S-41F_Champlian
CONN@

Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6843

Size: Custom | Document Number: 401982 | Rev: B

Date: Wednesday, September 01, 2010 | Sheet 8 of 40

DIMM_A STD H:5.2 mm

<Address: 00>

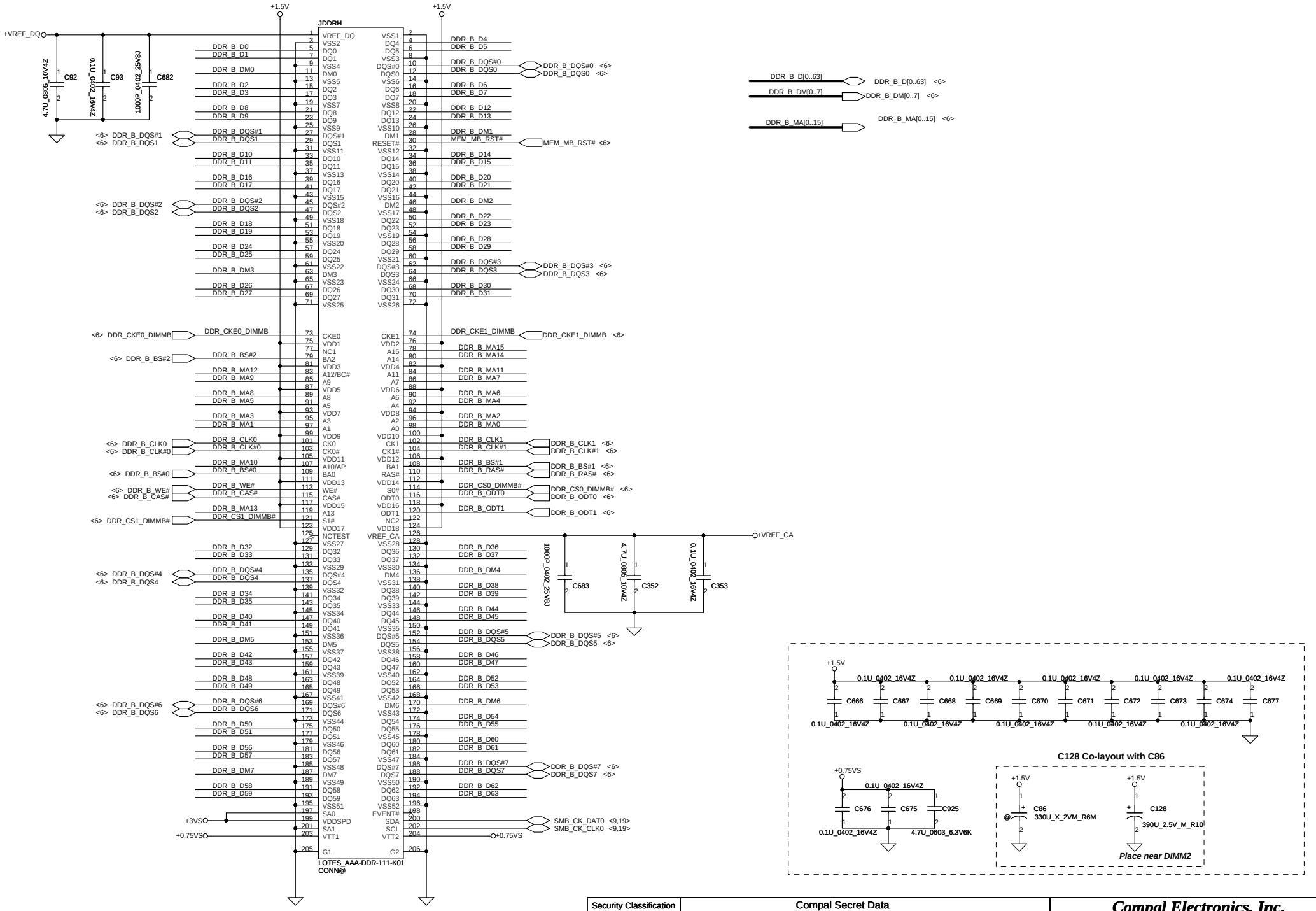
Security Classification	Compal Secret Data			
Issued Date	2010-08-25	Deciphered Date	2010-08-25	

Compal Electronics, Inc.

Title: **SCHEMATICS,MB A6843**

Size: Custom | Document Number: **401982** | Rev: B

Date: Wednesday, September 01, 2010 | Sheet 9 of 40



DIMM_B STD H:9.2 mm

<Address: 01>

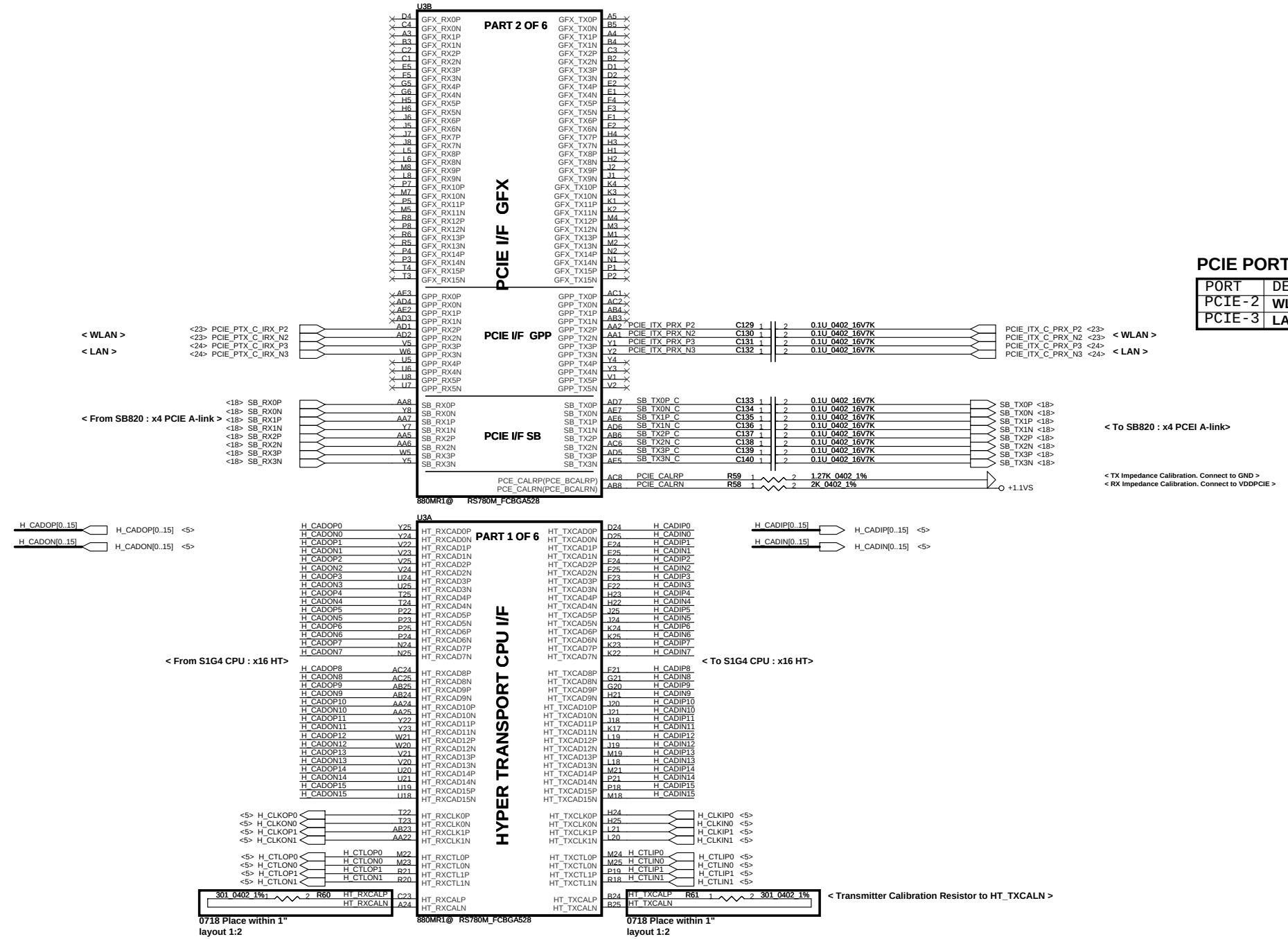
Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.

Title: **SCHEMATICS,MB A6843**

Size: Custom | Document Number: **401982** | Rev: B

Date: Wednesday, September 01, 2010 | Sheet 10 of 40

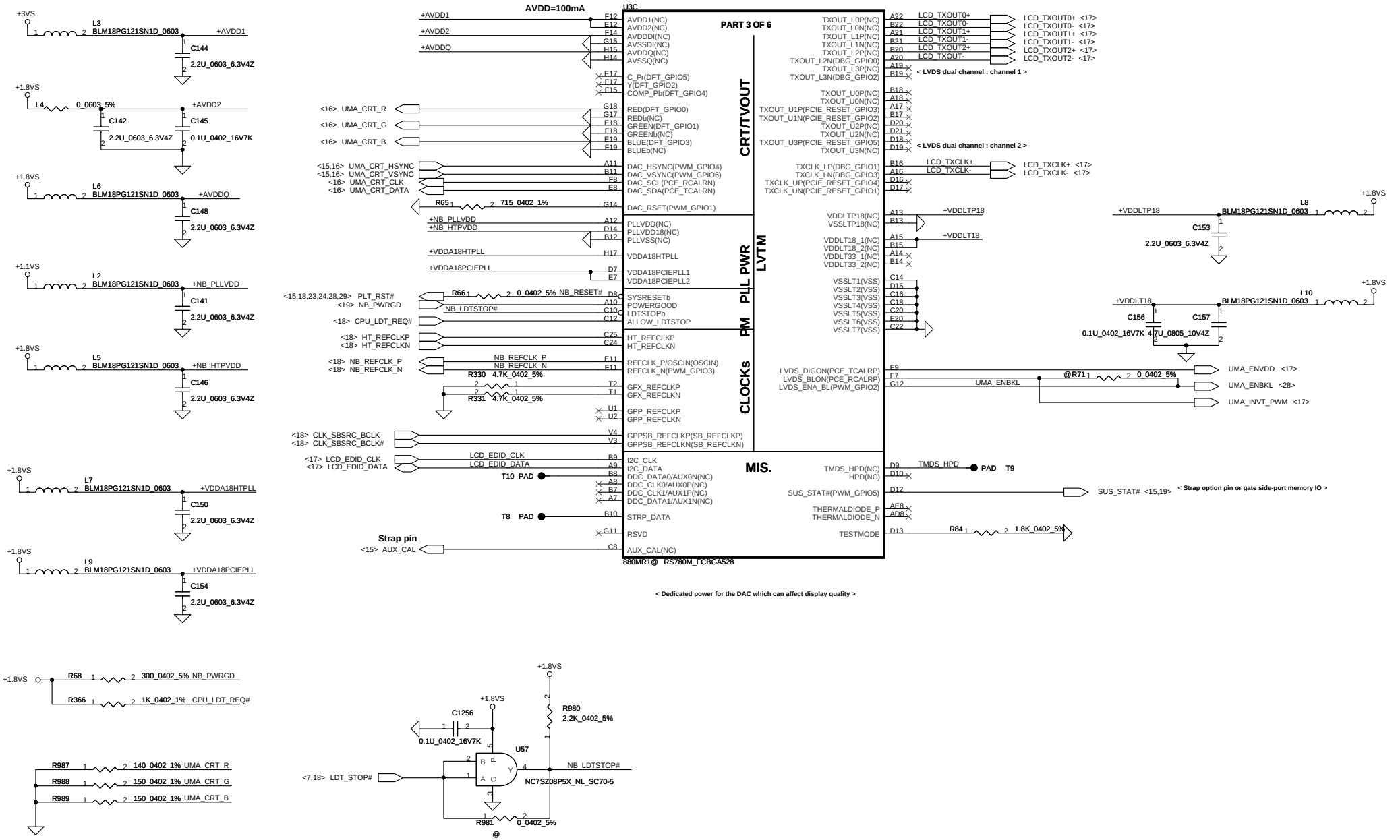


PCIE PORT LIST

PORT	DEVICE
PCIE-2	WLAN
PCIE-3	LAN

Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.			
Title: SCHEMATICS,MB A6843			
Size: Custom	Document Number: 401982		Rev: B
Date: Wednesday, September 01, 2010	Sheet 11 of 40		



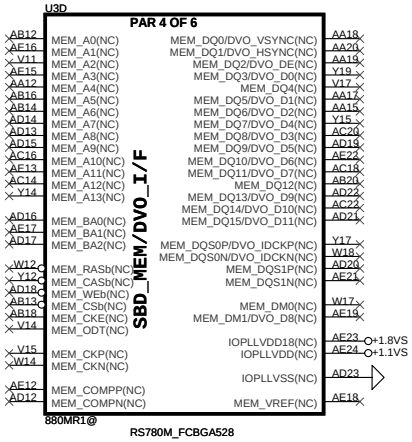
Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.

Title: **SCHEMATICS,MB A6843**

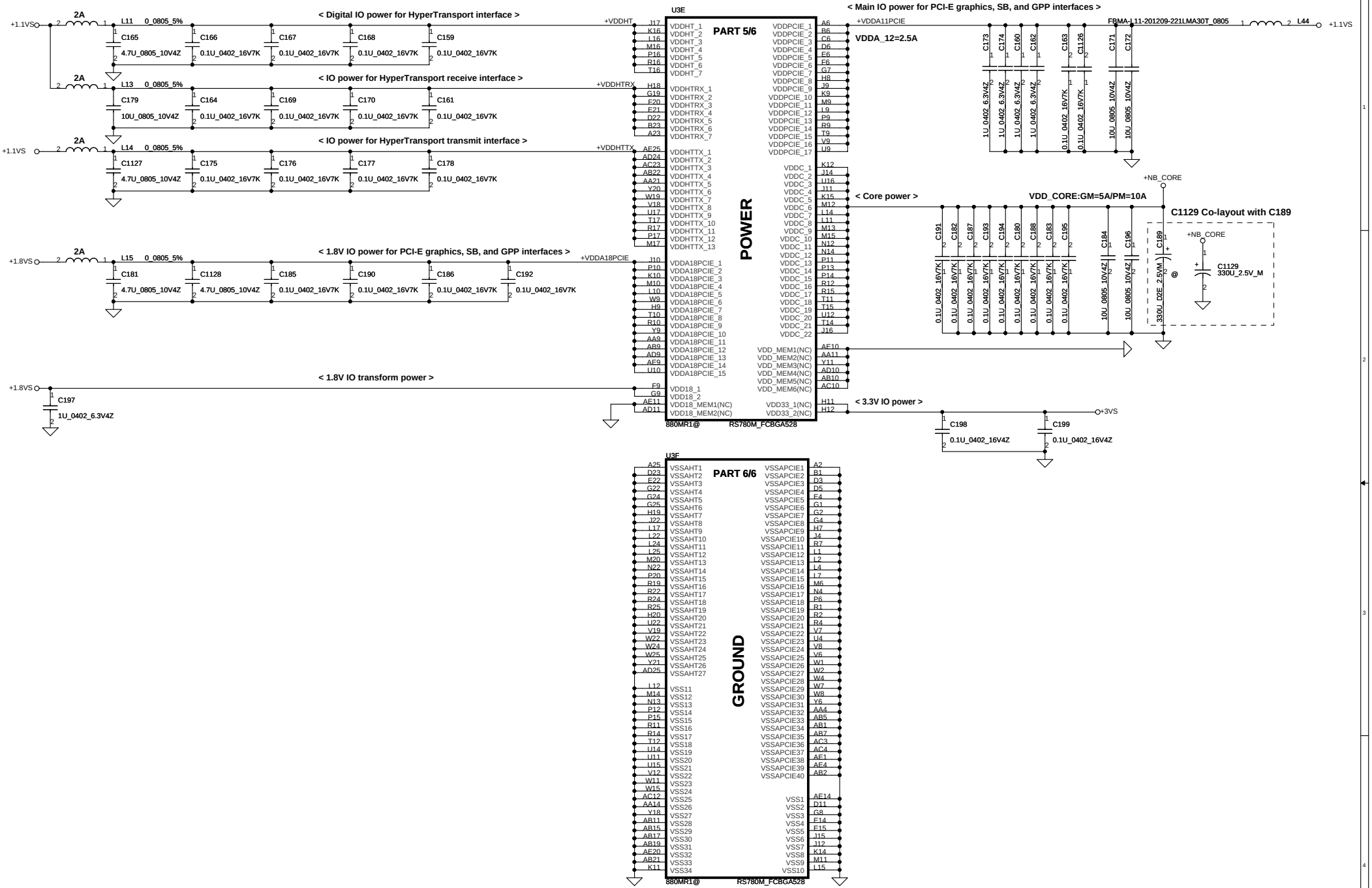
Size	Document Number	Rev
Custom	401982	B

Date: Wednesday, September 01, 2010 | Sheet 12 of 40



Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

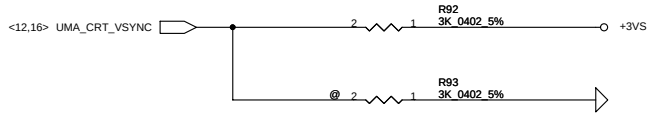
Compal Electronics, Inc.		
Title: SCHEMATICS,MB A6843		
Size: Custom	Document Number: 401982	Rev: B
Date: Wednesday, September 01, 2010	Sheet 13 of 40	



Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.			
Title: SCHEMATICS,MB A6843			
Size: Custom	Document Number: 401982		Rev: B
Date: Wednesday, September 01, 2010	Sheet 14 of 40		

< RS880 VSYNC mux at CRT_VSYNC pull High to 3K >



< VSYNC : STRAP_DEBUG_BUS_GPIO_ENABLEb >

Enables the Test Debug Bus using GPIO.

1 : Disable (RX881, RS880)
0 : Enable (RX881, RS880)

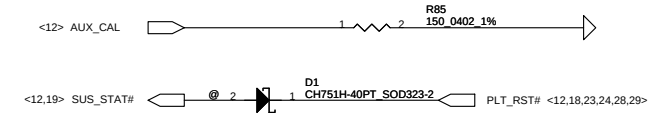
PIN: RS880--> VSYNC#

< RS880 use register to control PCI-E configure >

< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] >

These pin straps are used to configure PCI-E GPP mode.
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011

< RS880 SUS_STAT# >



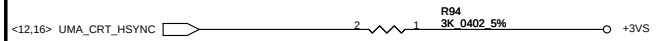
< SUS_SATA# : LOAD_EEPROM_STRAPS >

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880:SUS_STAT#

< RS880 use HSYNC to enable SIDE PORT (internal pull high) >



< HSYNC : STRAP_DEBUG_BUS_PCIE_ENABLEb >

RX881: Enables the Test Debug Bus using PCIE bus

1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

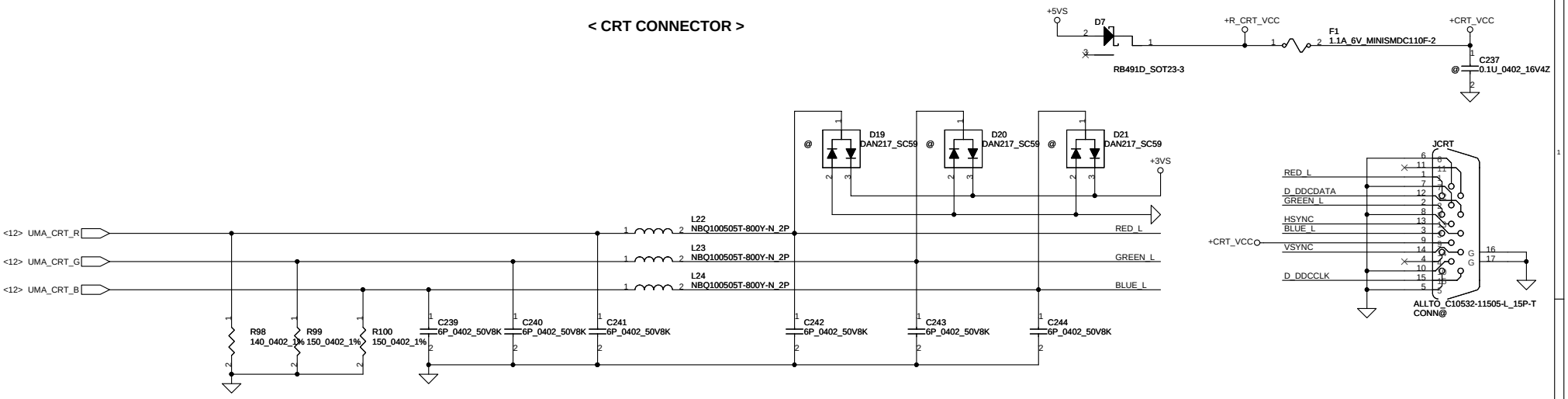
RS880: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS880)
0 : Enable (RS880)

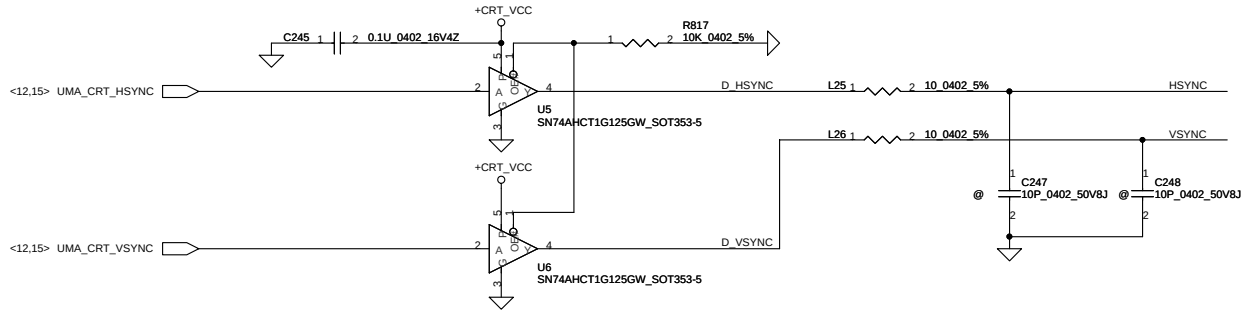
Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.		
Title: SCHEMATICS,MB A6843		
Size: Custom	Document Number: 401982	Rev: B
Date: Wednesday, September 01, 2010	Sheet 15 of 40	

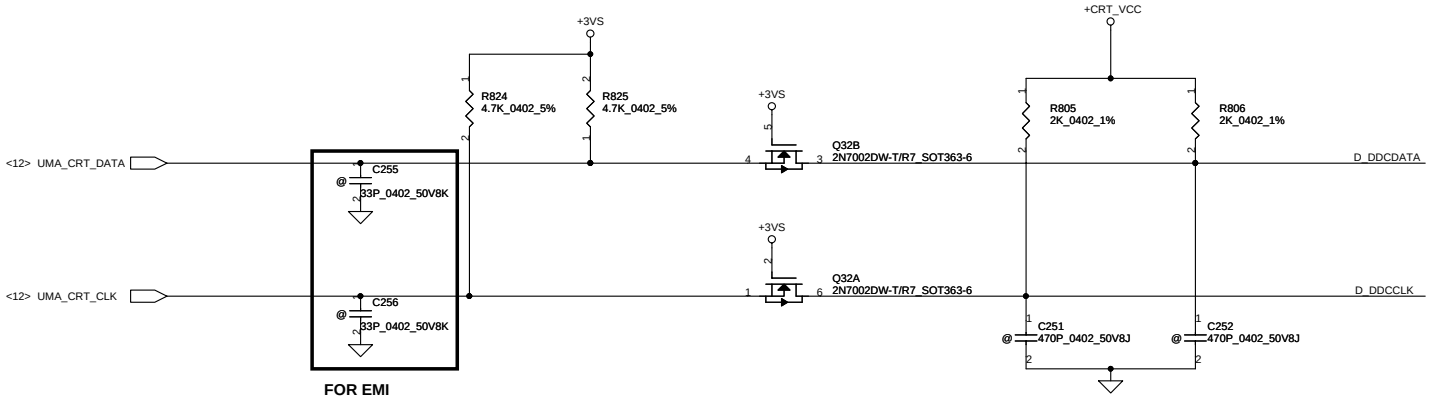
< CRT CONNECTOR >



< SYNC SIGNAL >



< Display Data Channel >



FOR EMI

Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

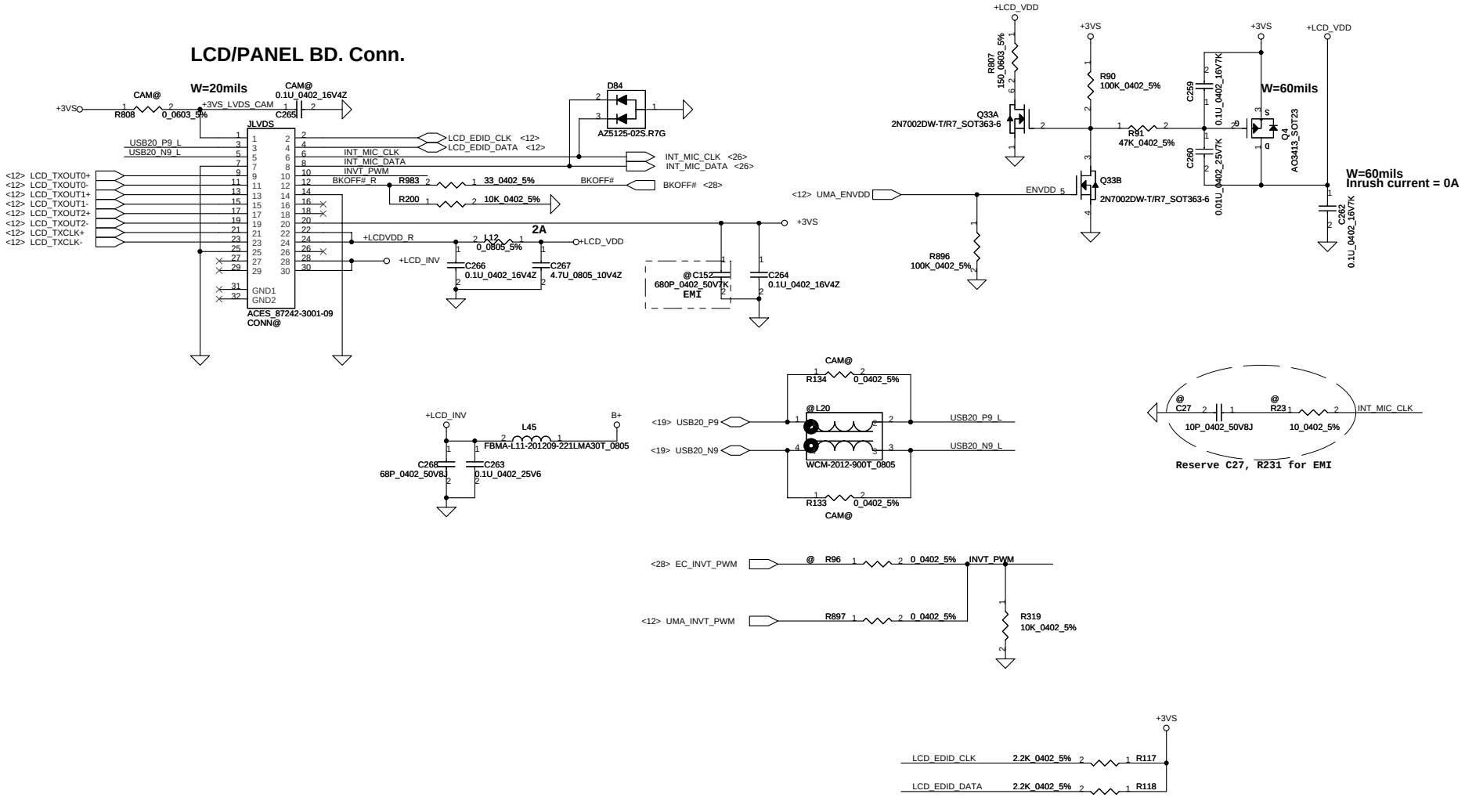
Compal Electronics, Inc.

Title: SCHEMATICS,MB A6843

Size	Document Number	Rev
Custom	401982	B

Date: Wednesday, September 01, 2010 | Sheet 16 of 40

LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.			
Title: SCHEMATICS,MB A6843			
Size: Custom	Document Number: 401982		Rev: B
Date: Wednesday, September 01, 2010	Sheet 17 of 40		

U8A

SB800 Part 1 of 5

SB820M_FCBGA605

SB820MR1@

PCI EXPRESS INTERFACES

PCI CLKS

PCI INTERFACE

CLOCK GENERATOR

LPC

CPU

RTC

level shift to ISL6265

ISL6265 PWROK input, TTL level: 0.8V~2.0V

When this pin is high, the SVI interface is active and I2C protocol is running. While this pin is low, the SVC, SVD, and VFIXEN input states determine the pre-PWROK metal VID or VFIX mode voltage. This pin must be low prior to the ISL6265 PGOOD output going high

4/26 Add test point T38 to T64 for debug

2/23 Reserve R796 pull-down to CLKRUN#

7/15 Add R260 pull up to +3VS

7/21 Change U8 P/N to SA00003IWA0 (A13)

7/2 Add Net RTCCLK for EC Crystal cost down

for Clear CMOS

7/22 Change D8 from DAN202U to CHN202UPT

Close to SB

Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6843

Size	Document Number	Rev
Custom	401982	B

Date: Wednesday, September 01, 2010 Sheet 18 of 40

7/2 Add D27 for abnormal shutdown RSMRST#

D27 CH751H-40PT_SOD323-2: SB_PWRGD → POK <33,35,36>

U8D — SB800 Part 4 of 5 — SB820M_FCBGA605 / SB820MR1@

USB PORT LIST

PORT	DEVICE
USB0	USB0(Right)
USB1	USB1(Right)
USB5	Card Reader
USB8	WLAN
USB9	Int Camera

USB-9 Int Camera
USB-8 WLAN
USB-5 Card Reader 2 IN 1
USB-1 Right side
USB-0 Right side

STRAP PIN

	GPIO201	GPIO202	GPIO203
Nile-M	High	High	High
Nile-S	High	High	Low
Danube Marseille	Low	Low	Low
Danube Hamburg	Low	Low	High
Danube LC Marseille	Low	Low	High *

	GPIO204	GPIO205
Madison LP	Low	Low
None	Low	High
Park XT	High	Low
M92 XTX	High	High

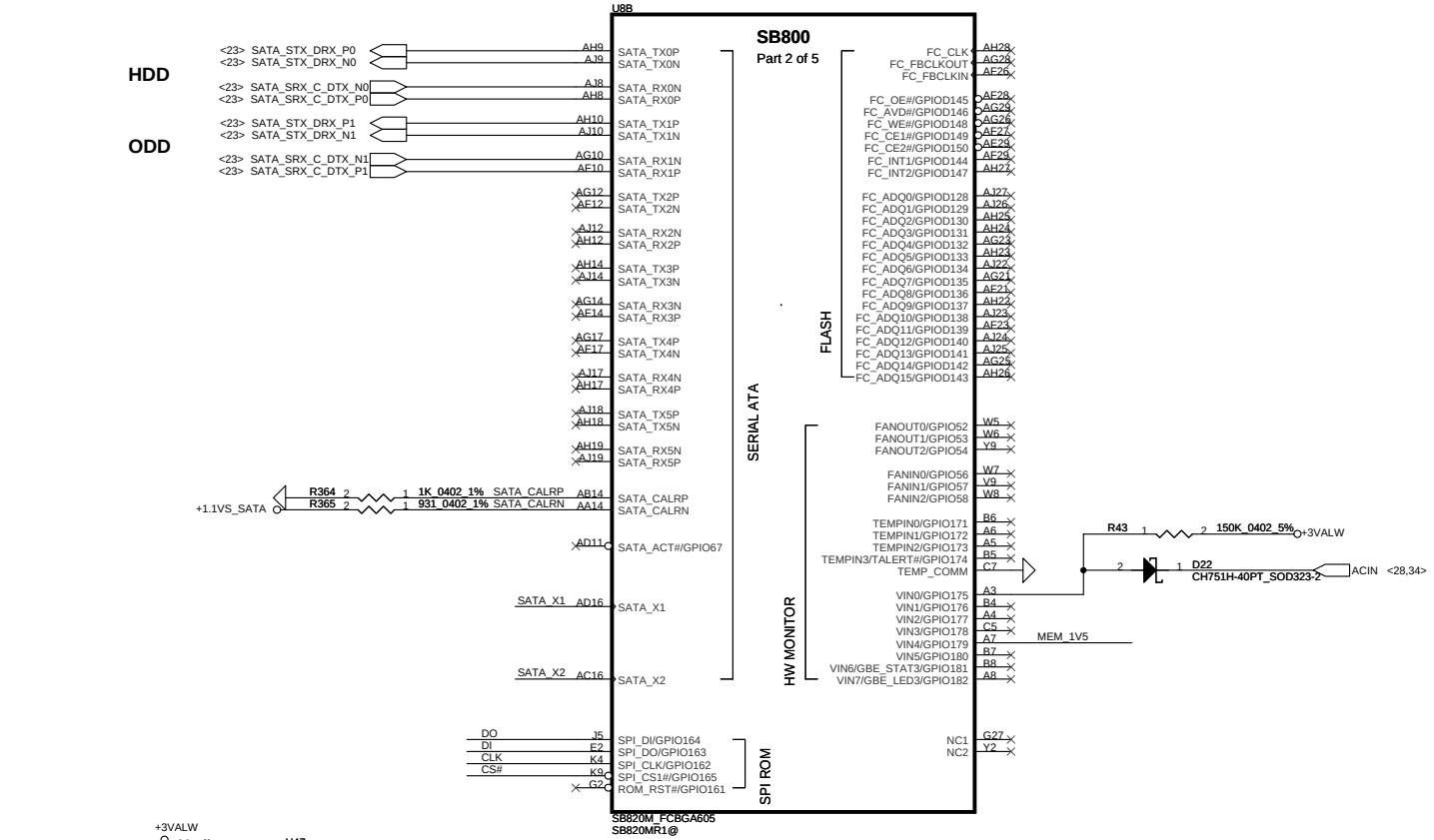
Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

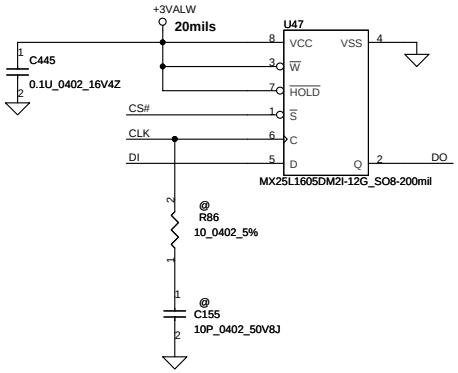
Compal Electronics, Inc.

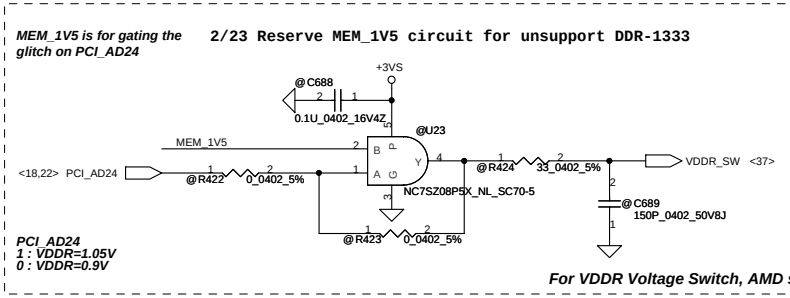
Title: SCHEMATICS,MB A6843

Size: Custom | Document Number: 401982 | Rev: B

Date: Wednesday, September 01, 2010 | Sheet 19 of 40



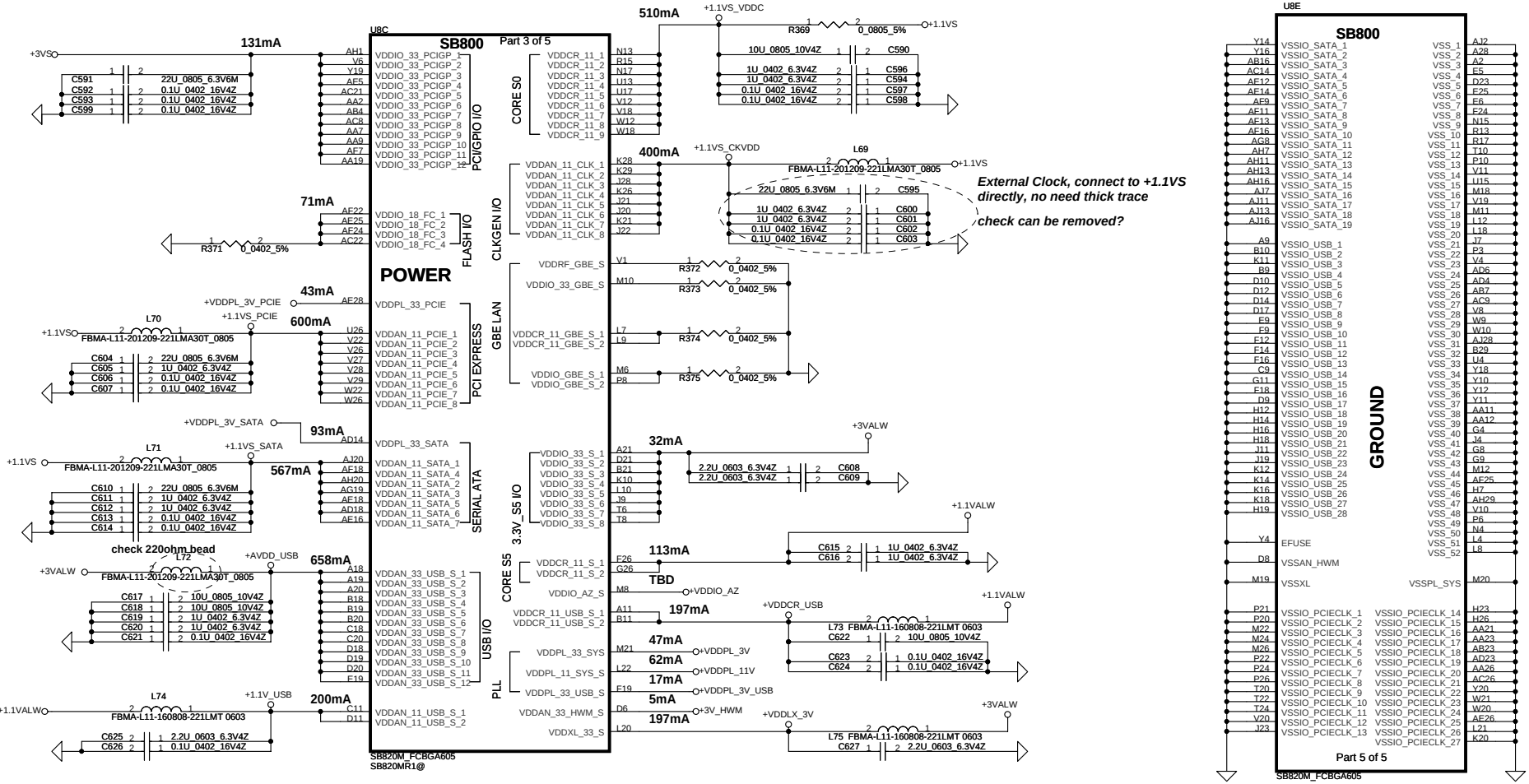


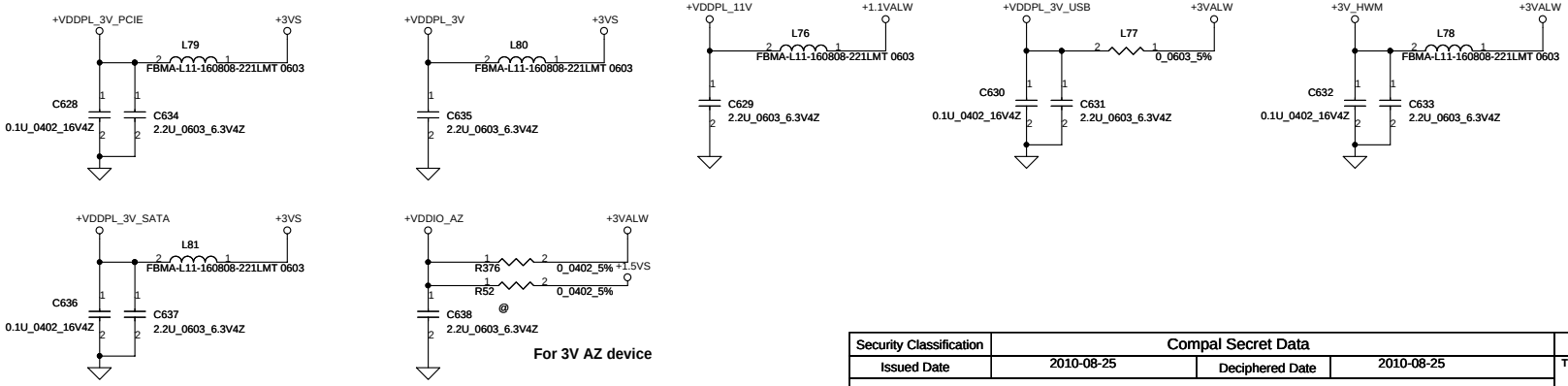


Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.			
Title: SCHEMATICS,MB A6843			
Size: Custom	Document Number: 401982		Rev: B
Date: Wednesday, September 01, 2010	Sheet 20 of 40		

4/16 Change U47 from SA00002TO00 to SA00003FO00





Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6843

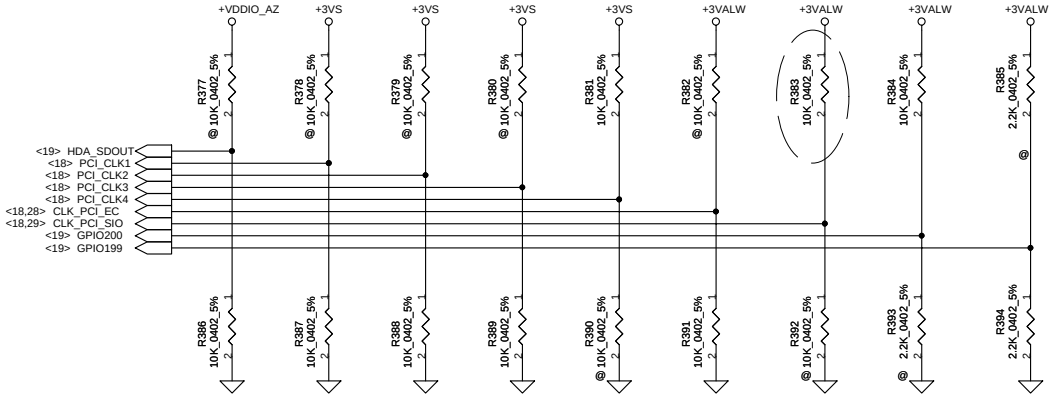
Size	Document Number	Rev
Custom	401982	B

Date: Wednesday, September 01, 2010 Sheet 21 of 40

REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable DEFAULT	EC ENABLE	CLOCKGEN ENABLE DEFAULT	H,H = Reserved H,L = SPI ROM (Default) L,H = LPC ROM L,L = FWH ROM
PULL LOW	Performance MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER DISABLE DEFAULT	IGNORE DEBUG STRAP DEFAULT	Inter CLK Gen Mode Disable	EC DISABLE DEFAULT	CLOCKGEN DISABLE	



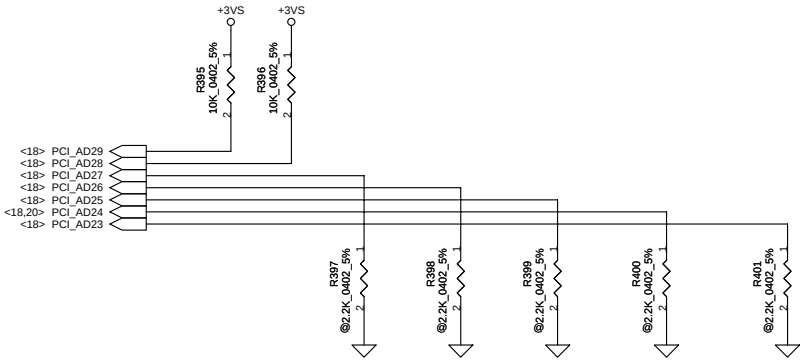
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH		USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW		BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

check default



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010-08-25	Deciphered Date 2010-08-25	Title SCHEMATICS,MB A6843
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size Custom / Document Number 401982 / Rev B
			Date: Wednesday, September 01, 2010 / Sheet 22 of 40

SATA HDD Conn.

Place closely JHDD SATA CONN.

+5VS 1.2A

C1247 10U_0805_10V4Z, C1248 0.1U_0402_16V4Z, C1249 0.1U_0402_16V4Z, C1250 0.1U_0402_16V4Z

SSD HDD need 400mA for 3V(PHISON)

+3VS rail reserve for SSD

C1251 10U_0805_10V4Z @, C1159 0.1U_0402_16V4Z @, C1152 0.1U_0402_16V4Z @, C1253 0.1U_0402_16V4Z @

Close to JHDD

JHDD

SATA_STX_C_DRX_P0 — C1153 0.01U_0402_25V7K — SATA_STX_DRX_P0 <20>
SATA_STX_C_DRX_N0 — C1154 0.01U_0402_25V7K — SATA_STX_DRX_N0 <20>
SATA_SRX_DTX_N0 — C1155 0.01U_0402_25V7K — SATA_SRX_C_DTX_N0 <20>
SATA_SRX_DTX_P0 — C1156 0.01U_0402_25V7K — SATA_SRX_C_DTX_P0 <20>

+3VS, +5VS

D91 RCLAMP0524P.TCT~D @

2/23 Reserve D91 for ESD

SANTA_191201-1 CONN@

SATA ODD Conn

Close to JODD

JODD

SATA_STX_C_DRX_P1 — C1143 0.01U_0402_25V7K — SATA_STX_DRX_P1 <20>
SATA_STX_C_DRX_N1 — C1138 0.01U_0402_25V7K — SATA_STX_DRX_N1 <20>
SATA_SRX_DTX_N1 — C1137 0.01U_0402_25V7K — SATA_SRX_C_DTX_N1 <20>
SATA_SRX_DTX_P1 — C1136 0.01U_0402_25V7K — SATA_SRX_C_DTX_P1 <20>

+5VS

SANTA_206401-1_RV CONN@

Place components closely ODD CONN.

+5VS 1.1A

C1144 10U_0805_10V4Z, C1145 10U_0805_10V4Z, C1146 @ 1U_0402_6.3V4Z, C1147 0.1U_0402_16V4Z, C1148 0.1U_0402_16V4Z

USB Port 0 & Port1

+5VALW 1.4A

U48 RT9715BGS_SO8

W=60mils +USB_VCCA

C1157 @ For EMI request 1000P_0402_50V7K

C1158 4.7U_0805_10V4Z @

<28> USB_EN# — USB_EN#

USB_OC#0 <19,28>

Reserve for EMI request

@R828 0_0402_5%, @R829 0_0402_5%, @R830 0_0402_5%, @R831 0_0402_5%

L82 WCM-2012-900T_0805, L83 WCM-2012-900T_0805

<19> USB20_P0 — USB20_P0_R
<19> USB20_N0 — USB20_N0_R
<19> USB20_N1 — USB20_N1_R
<19> USB20_P1 — USB20_P1_R

7/9 Mount L82,L83 ,Reserve R828,R830 for EMI request

Slot#1 Half PCIe Mini Card-WLAN

+3VS — @PJ27 JUMP_43X79 — +3V_WLAN

Short PJ27 for WLAN

CLKREQ_MCARD2# — @R259 8.2K_0402_5% — +3V_WLAN

+1.5VS: CM21 0.01U_0402_25V7K, CM18 0.1U_0402_16V4Z, CM17 47P_0402_50V8J, CM24 4.7U_0805_10V4Z @ — For SED

+3V_WLAN: CM20 0.01U_0402_25V7K, CM22 0.1U_0402_16V4Z, CM23 47P_0402_50V8J, CM19 4.7U_0805_10V4Z @ — For SED

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	H	L
BT_PWR#	L	H

**If +3V_WLAN is +3VS, please remove DM2

<28,31,37> SUSP# — @DM2 CH751H-40PT_SOD323-2 — BT_CTRL

<18> BT_PWR# — QM1 BT@ 2N7002_SOT23-3

7/25 Reserver DM2 for +3V_WLAN is +3VS

JWLAN

BT_CTRL
<19> CLKREQ_MCARD2#
<18> CLK_PCIE_MCARD2#
<18> CLK_PCIE_MCARD2
<11> PCIE_PTX_C_IRX_N2
<11> PCIE_PTX_C_IRX_P2
<11> PCIE_ITX_C_PRX_N2
<11> PCIE_ITX_C_PRX_P2
+3V_WLAN

WLAN/ WiFi

PLT_RST# — WL_OFF# <28>; PLT_RST# <12,15,18,24,28,29>

SMB_CK_CLK1 <19>
SMB_CK_DAT1 <19>
USB20_N8 <19>
USB20_P8 <19>

+1.5VS 1 A, +3V_WLAN 1 A

BT_CTRL R50 1K_0402_5% ES1_RXD_R

7/25 Add R50 for Intel Rainbow Peak module

<28> ES1_TXD — RM16 0_0402_5%
<28> ES1_RXD — RM15 0_0402_5% — ES1_RXD_R

Debug card using

FOX_AS0B226-S40N-7F CONN@

+USB_VCCA W=40mils

C339 220U_6.3V_M, C340 0.1U_0402_16V4Z, C341 1000P_0402_50V7K

JUSB1 @ ALLTOP C107L8-10405-L

USB20_N0_R, USB20_P0_R

D9 @ PJDLC05_SOT23-3

+USB_VCCA W=40mils

C342 0.1U_0402_16V4Z, C343 1000P_0402_50V7K

JUSB2 @ ALLTOP C107L8-10405-L

USB20_N1_R, USB20_P1_R

D10 @ PJDLC05_SOT23-3

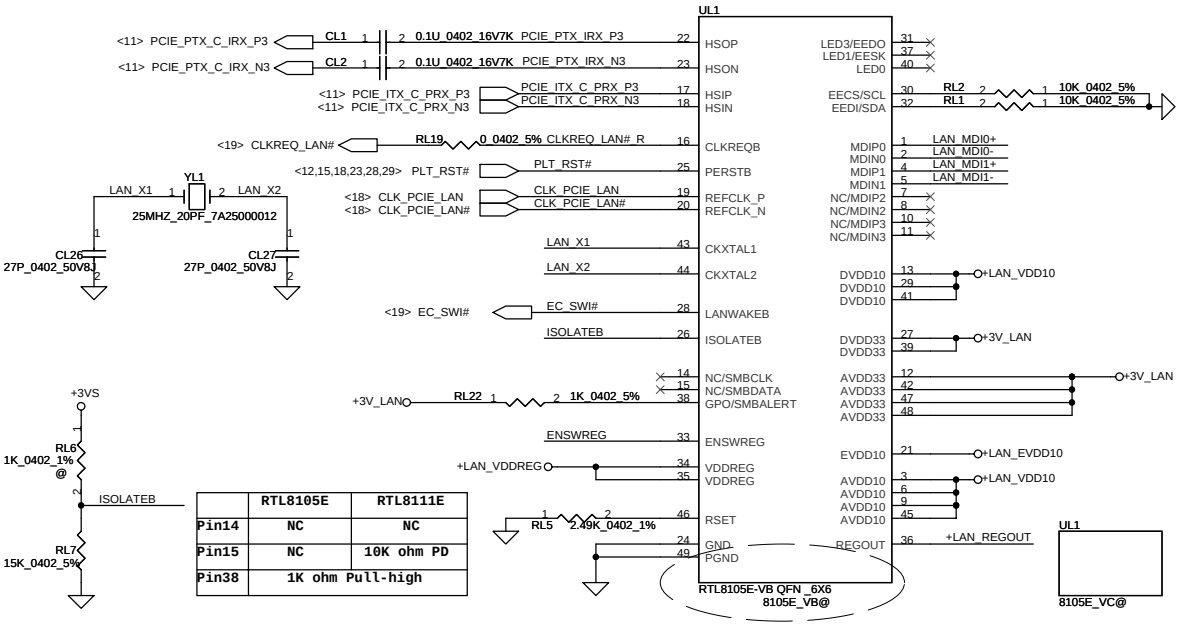
Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.

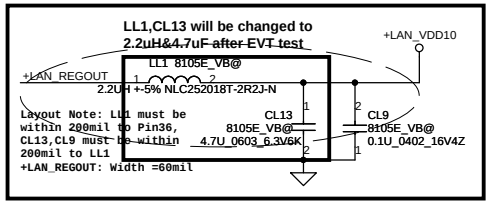
Title: SCHEMATICS,MB A6843

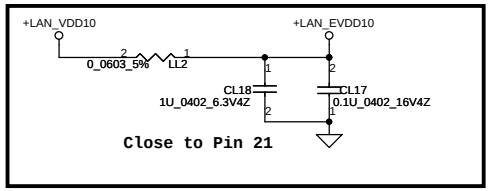
Size | Document Number: 401982 | Rev: B

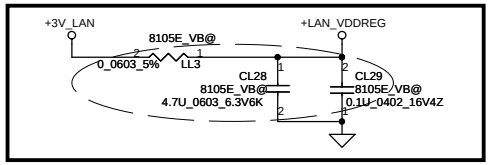
Date: Wednesday, September 01, 2010 | Sheet 23 of 40

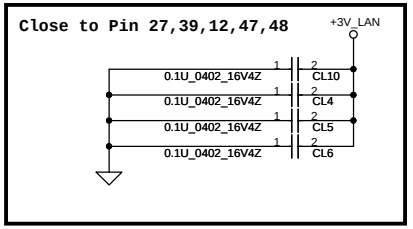


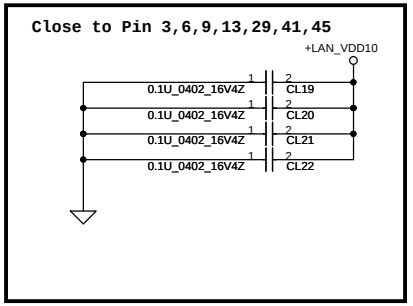
	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	

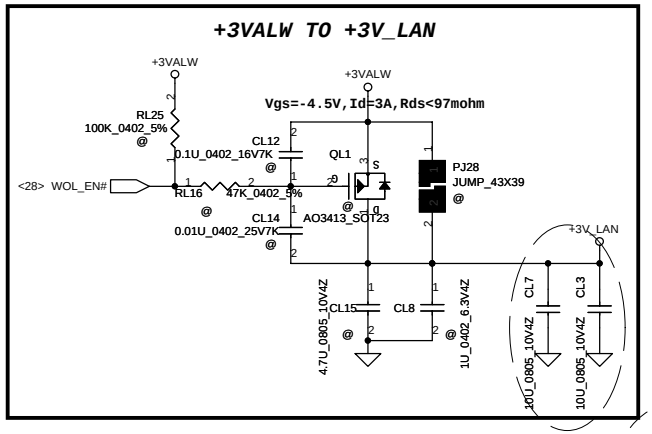






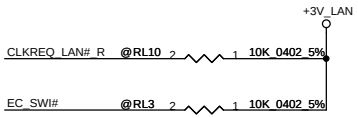




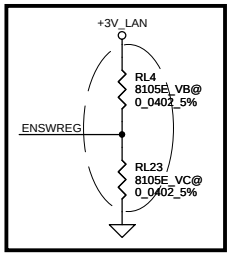


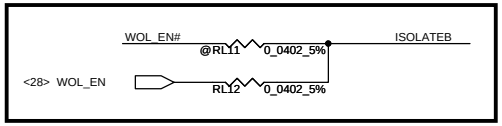
7/16 Change UL1 from RTL8105E-VB (SA00003PO10) to RTL8105E-VC (SA00003PO20)

7/16 For LDO mode :
1. Remove RL4, mount RL23.
2. Remove LL1, CL13, CL9, LL3, CL28, CL29.



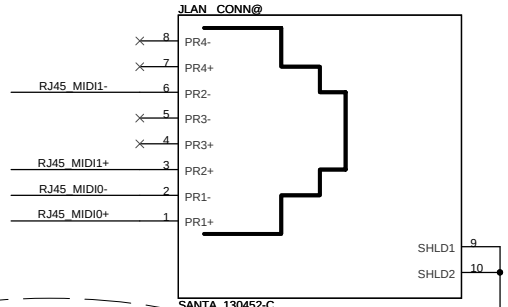
8/7 Chagne UL4 from NS681680 to NS681695

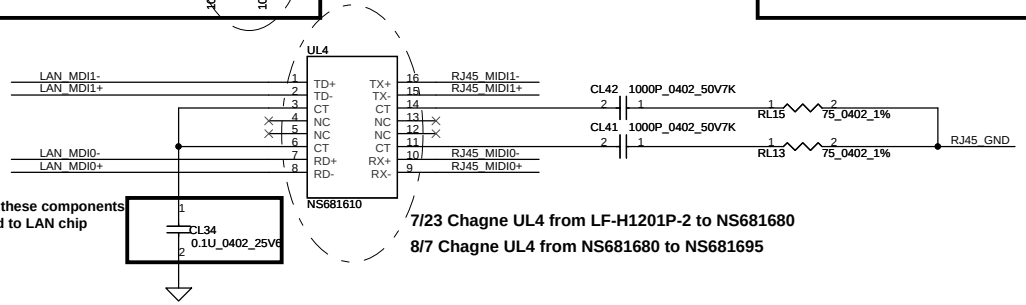




LAN Conn.

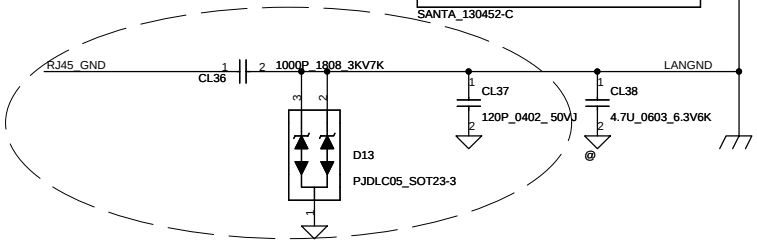
change connector to w/o LED
(use NPVAA LAN conn. before LAN symol ready)





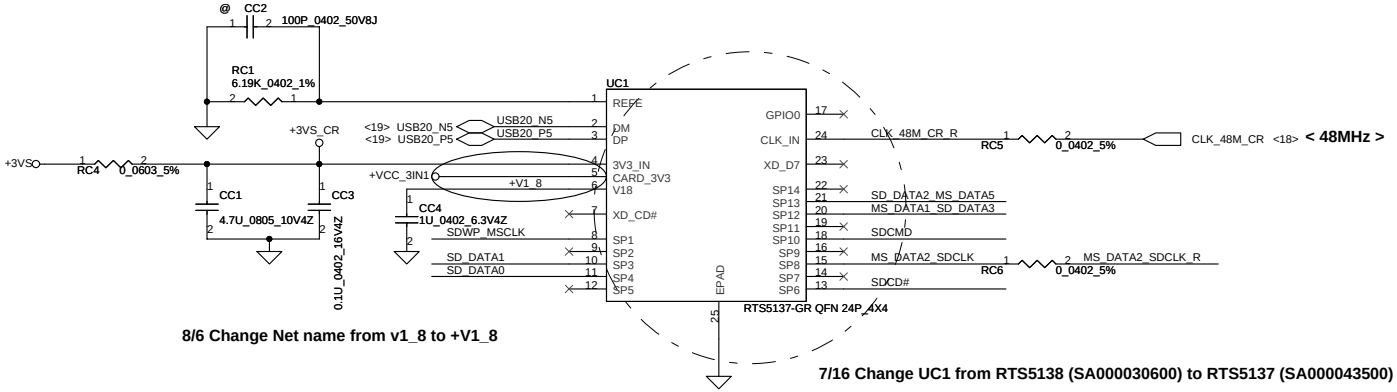
Place these components colsed to LAN chip

7/23 Chagne UL4 from LF-H1201P-2 to NS681680
8/7 Chagne UL4 from NS681680 to NS681695



Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

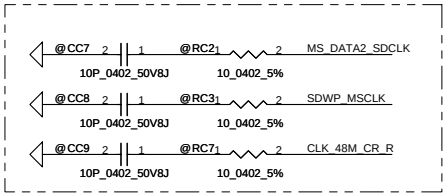
Compal Electronics, Inc.			
Title: SCHEMATICS,MB A6843			
Size: Custom	Document Number: 401982		Rev: B
Date: Wednesday, September 01, 2010	Sheet 24 of 40		



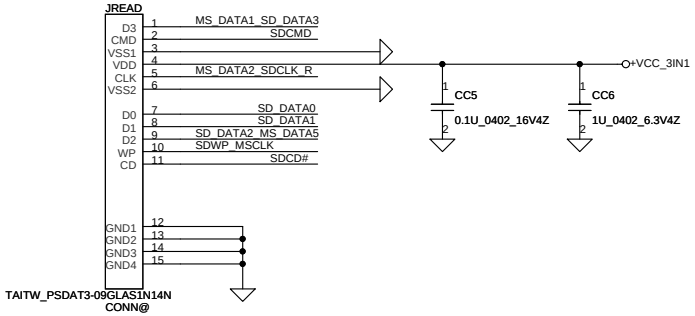
8/6 Change Net name from v1_8 to +V1_8

7/16 Change UC1 from RTS5138 (SA000030600) to RTS5137 (SA000043500)

for EMI request

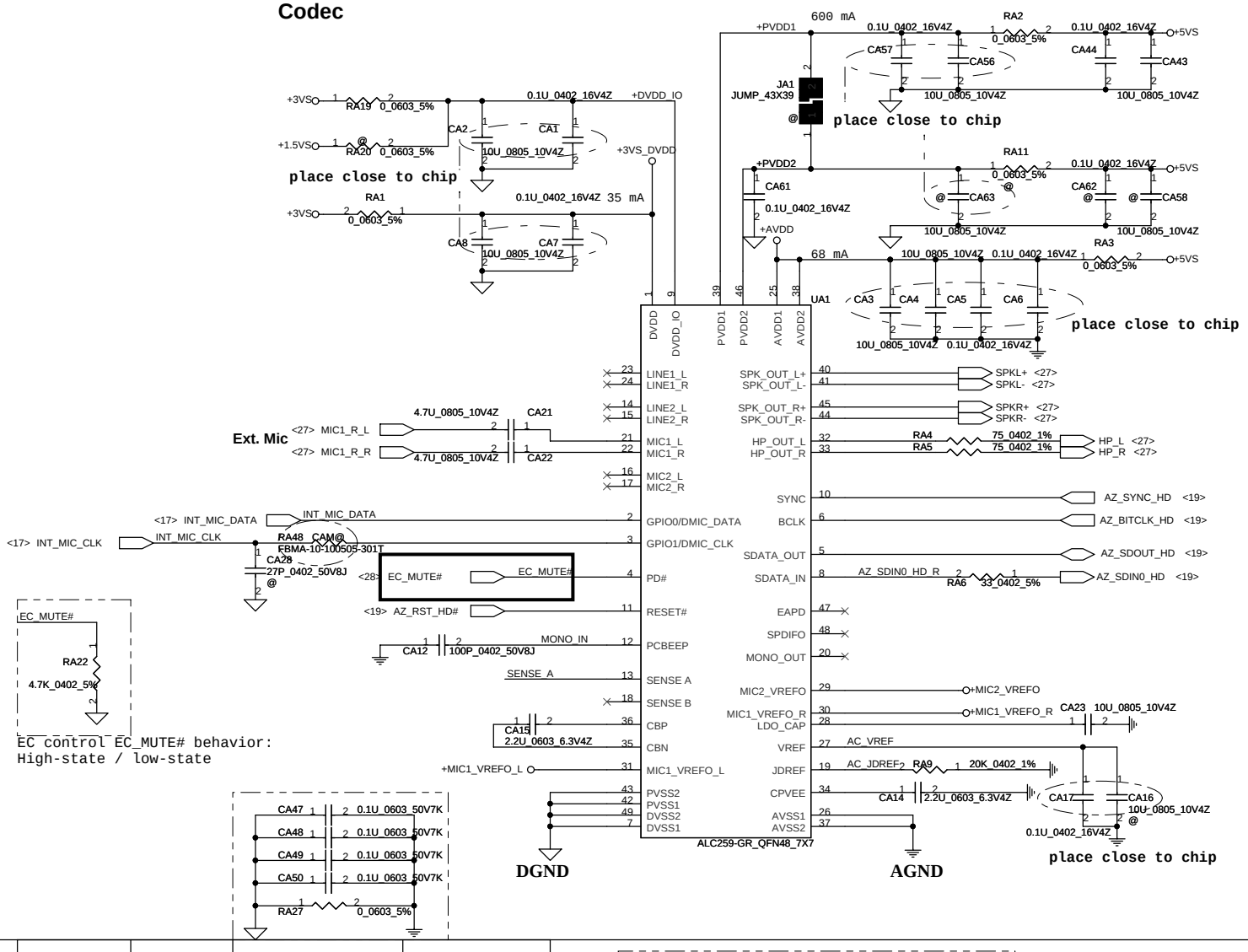


< 2 in 1 Card Reader >



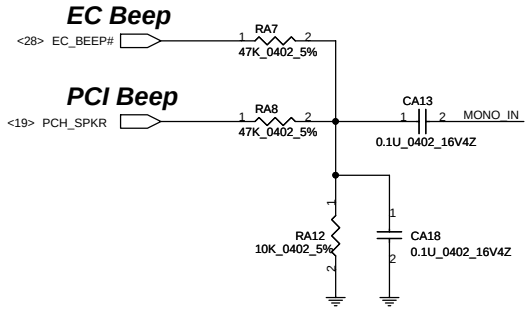
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010-08-25	Deciphered Date 2010-08-25	Title: SCHEMATICS,MB A6843
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: D — Document Number: 401982 — Rev: B
			Date: Wednesday, September 01, 2010 — Sheet 25 of 40

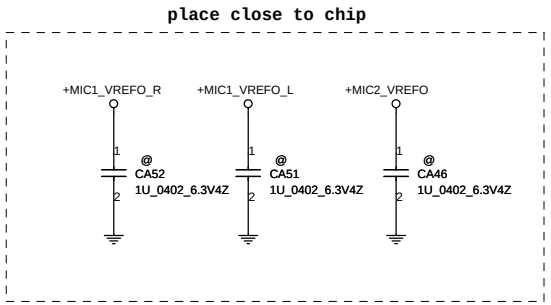
Codec

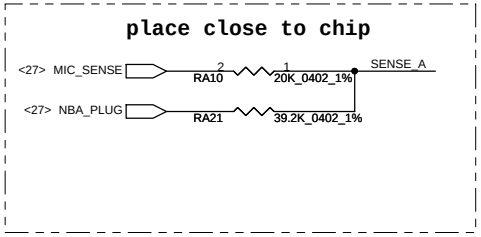


EC control EC_MUTE# behavior:
High-state / low-state

Beep sound







Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

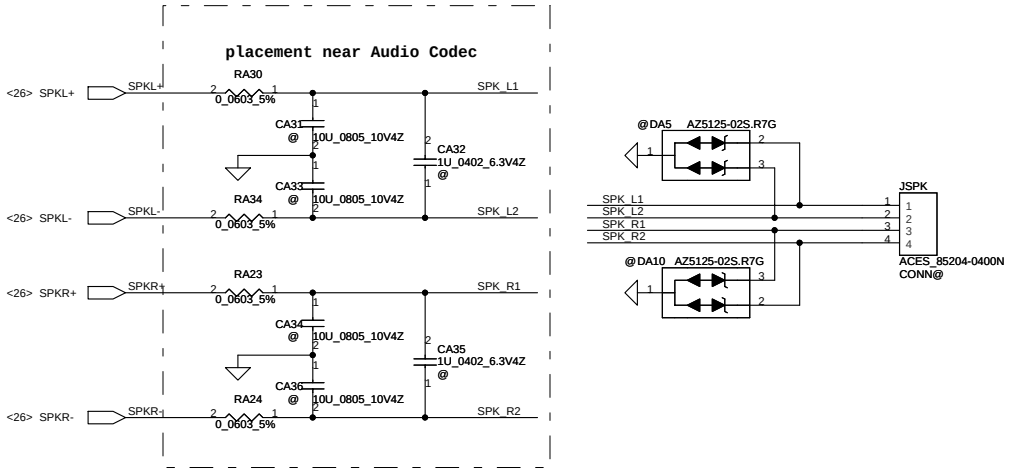
Compal Electronics, Inc.

Title: SCHEMATICS,MB A6843

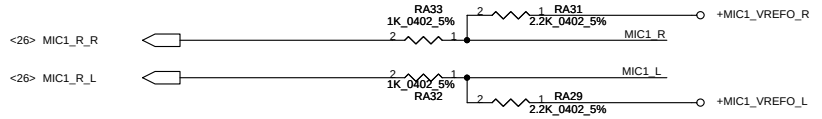
Size | Document Number: 401982 | Rev: B

Date: Wednesday, September 01, 2010 | Sheet 26 of 40

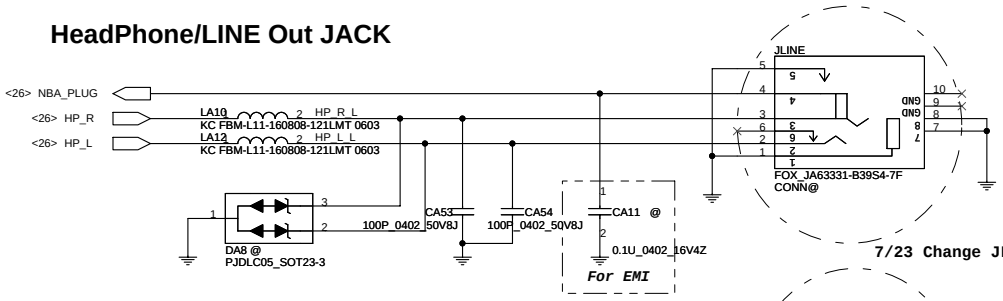
Speaker Connector



Ext.MIC/LINE IN JACK

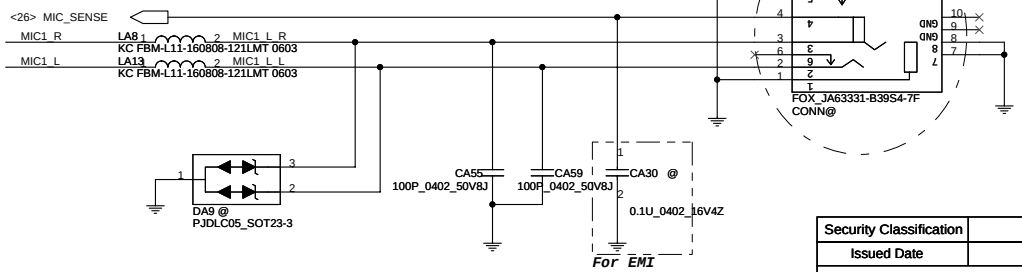


HeadPhone/LINE Out JACK



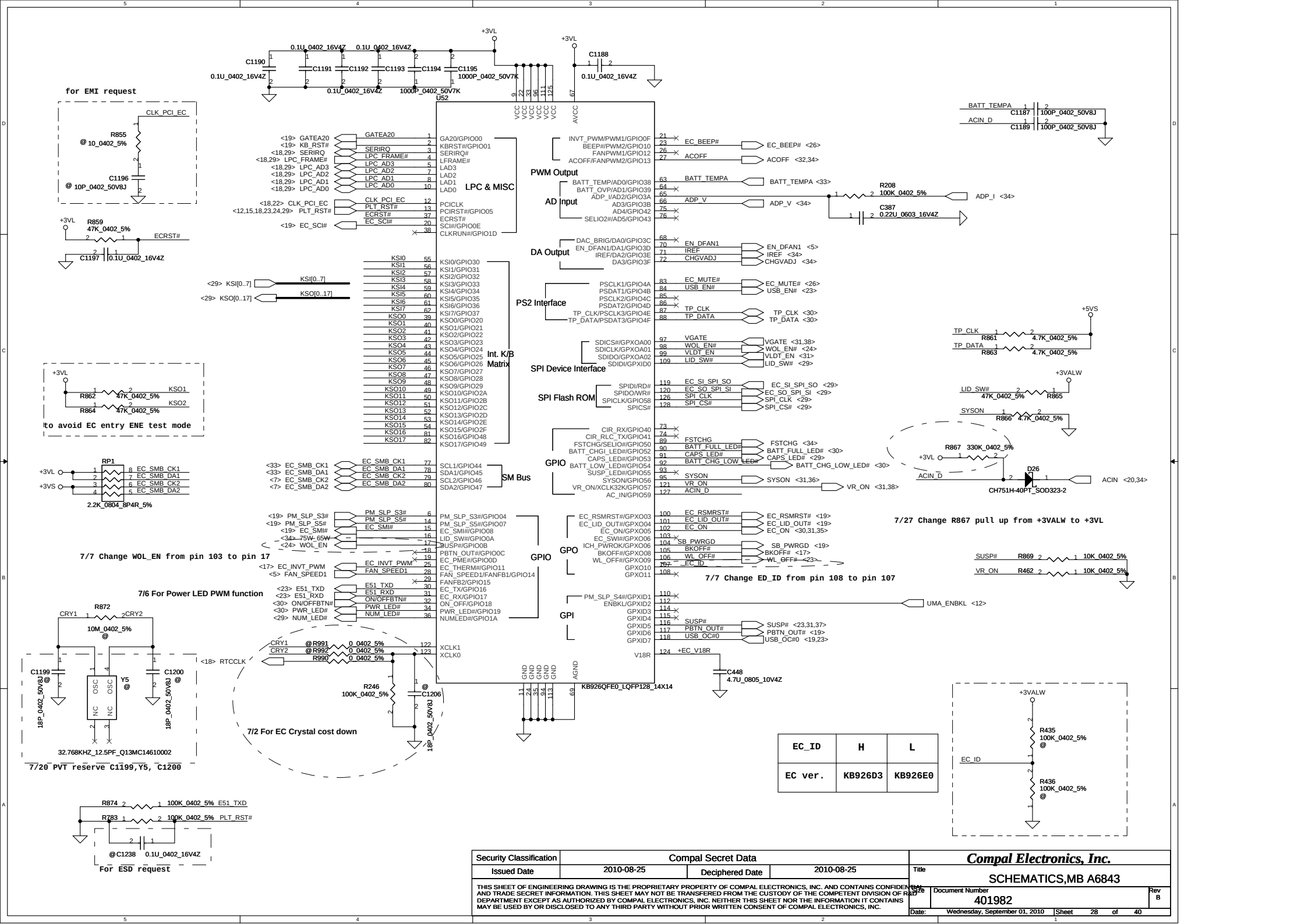
7/23 Change JLINE/JEXMIC to FOX_JA6331-B39S4-7F for DFX

Ext.MIC/LINE IN JACK



Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.			
Title	SCHEMATICS,MB A6843		
Size: Custom	Document Number: 401982		Rev: B
Date: Wednesday, September 01, 2010	Sheet 27 of 40		



Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

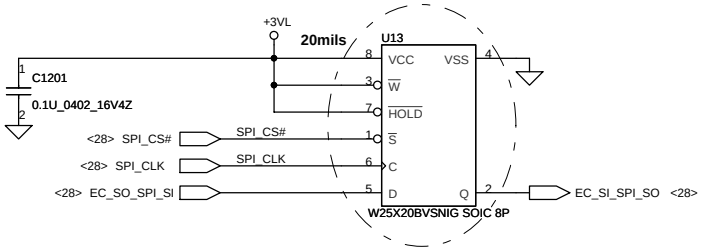
Title: SCHEMATICS,MB A6843

Size: | Document Number: 401982 | Rev: B

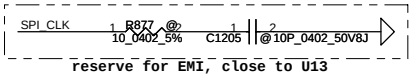
Date: Wednesday, September 01, 2010 | Sheet 28 of 40

SPI Flash (256KB)

7/7 Change U13 from MXIC to WINBOND for EOL

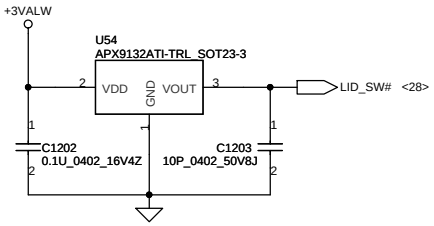


8/6 Change U13 footprint to M25P10-AVMN6T_SO8



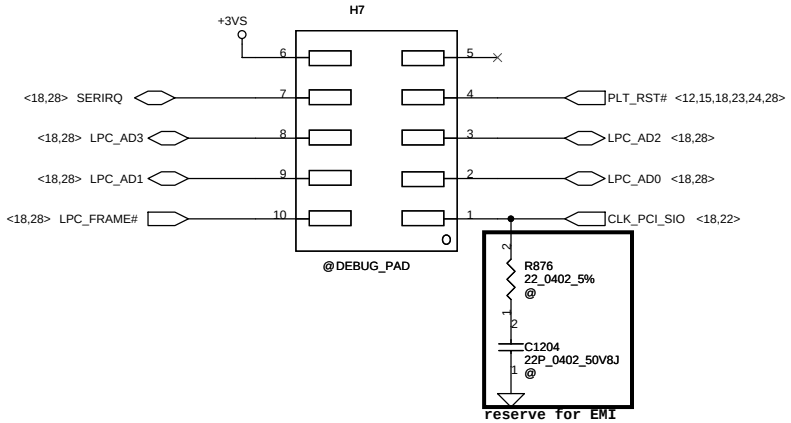
reserve for EMI, close to U13

Lid SW



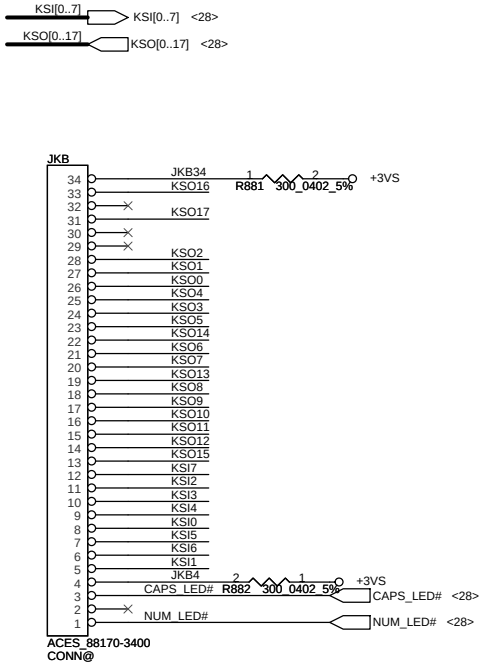
LPC Debug Port

Please place the PAD under DDR DIMM.

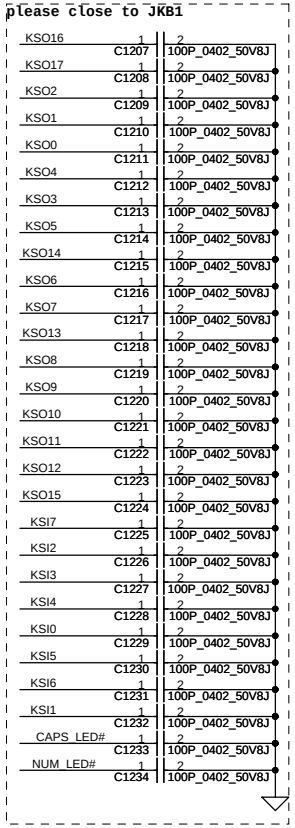


reserve for EMI

KEYBOARD CONN.



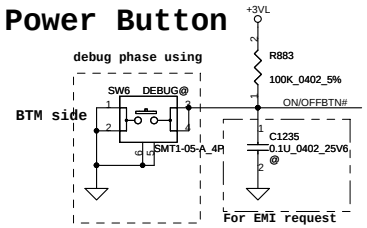
please close to JKB1

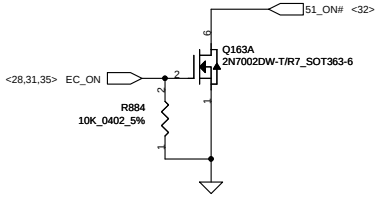


Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

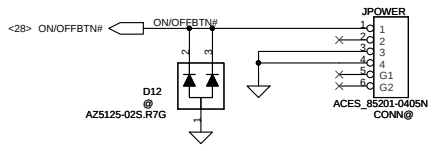
Compal Electronics, Inc.			
Title	SCHEMATICS,MB A6843		
Size	Document Number 401982		Rev B
Date: Wednesday, September 01, 2010	Sheet 29 of 40		

Power Button



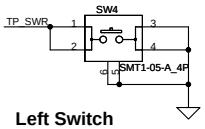


< Power / B Connector >

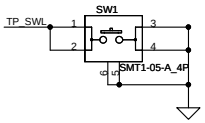


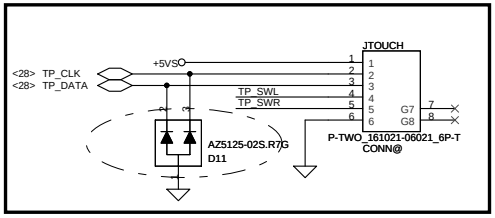
< Touch / B Connector >

Right Switch



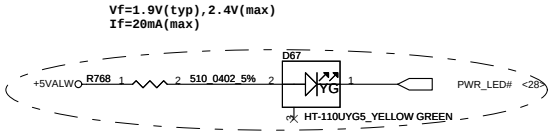
Left Switch





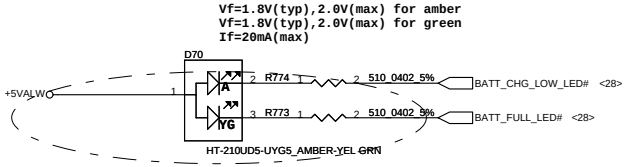
7/13 For ESD request

POWER/SUSPEND LED



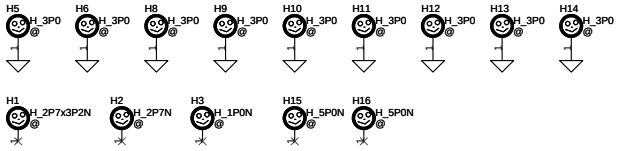
7/6 For Power LED PWM function
7/15 Change D67/D70 to 5mA type
7/23 Change R773 from 120 to 510 ohm
7/23 Change Net name from+3VALW to +5VALW

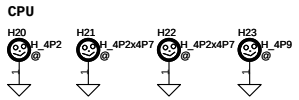
DC IN/ BATT CHARGE

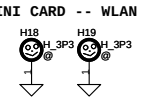


7/23 Change R773 from 120 to 510 ohm
7/23 Change Net name from+3VALW to +5VALW
8/6 Add R774 link to BATT_CHG_LOW_LED#
8/6 Change R773 link to BATT_FULL_LED#

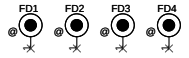
Screw Hole



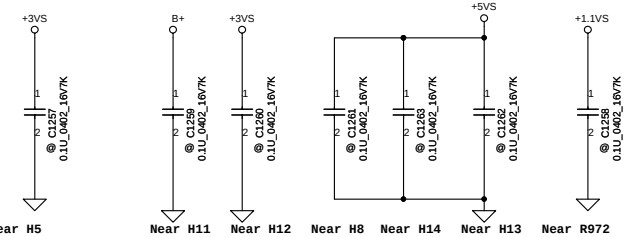




PCB Fedical Mark PAD

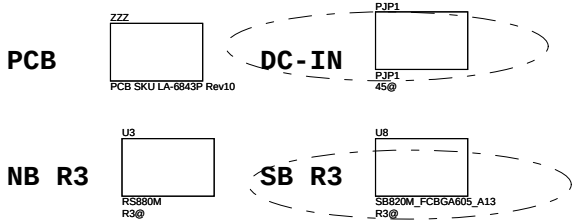


ESD reserved



ISPD

7/13 Change P/N to DC30100A400



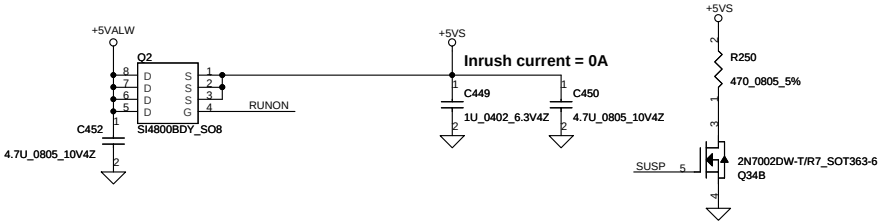
7/21 Change P/N to SA00003IWB0

Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

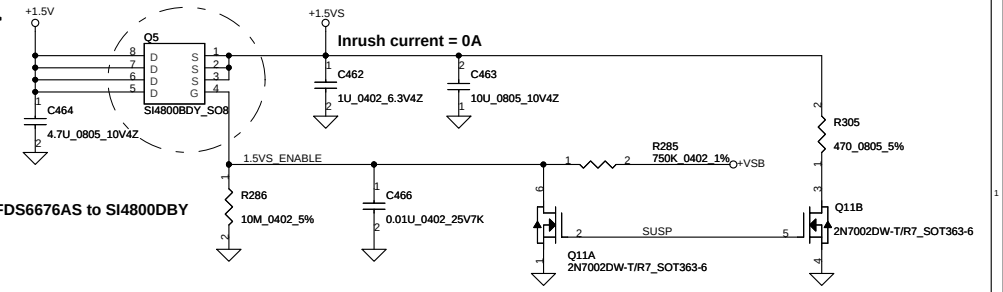
Compal Electronics, Inc.

Title	SCHEMATICS,MB A6843		
Size	Document Number		Rev
	401982		B
Date:	Wednesday, September 01, 2010	Sheet	30 of 40

< +5VALW TO +5VS >

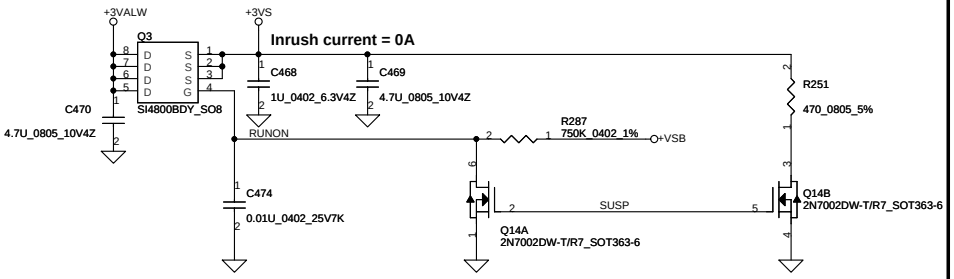


< +1.5V TO +1.5VS >

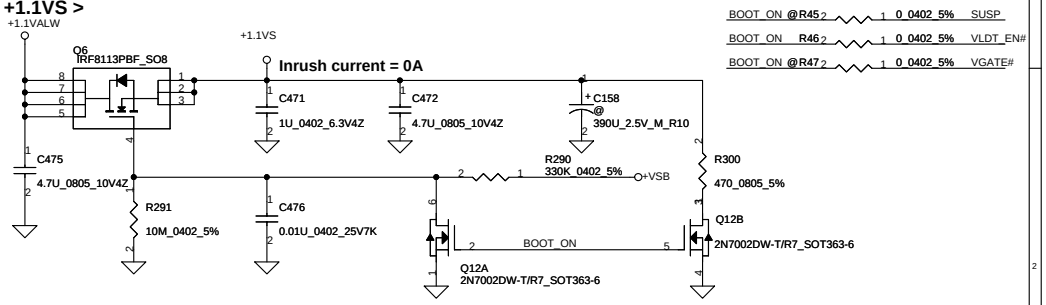


7/8 Change Q5 from FDS6676AS to SI4800DBY

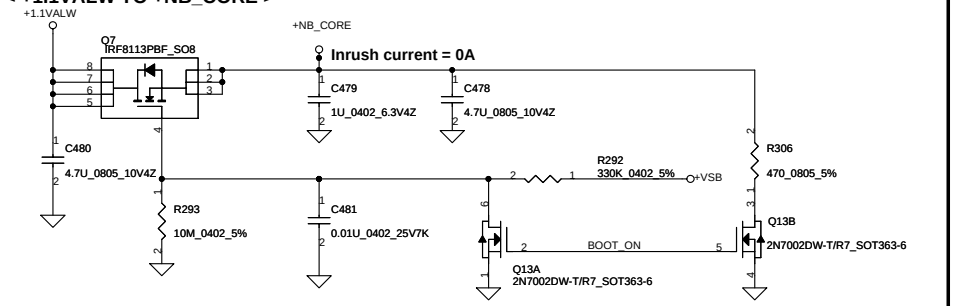
< +3VALW TO +3VS >



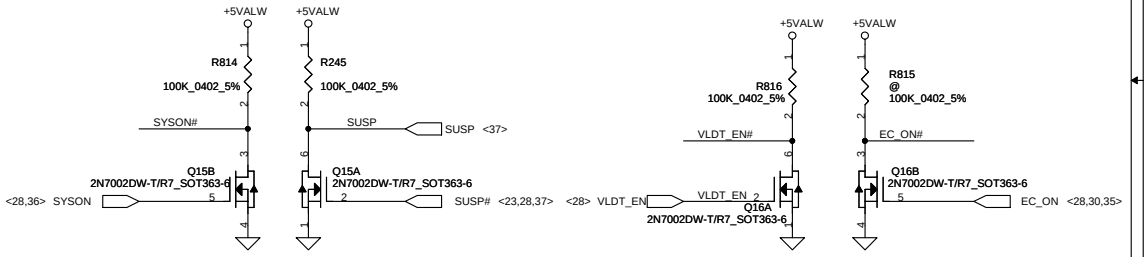
< +1.1VALW TO +1.1VS >

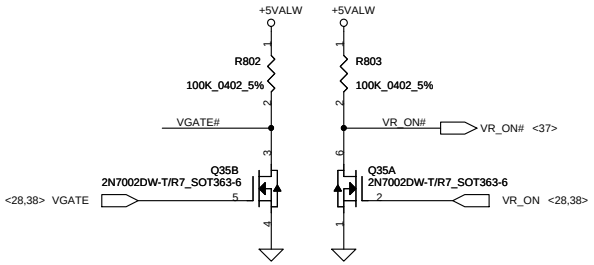


< +1.1VALW TO +NB_CORE >

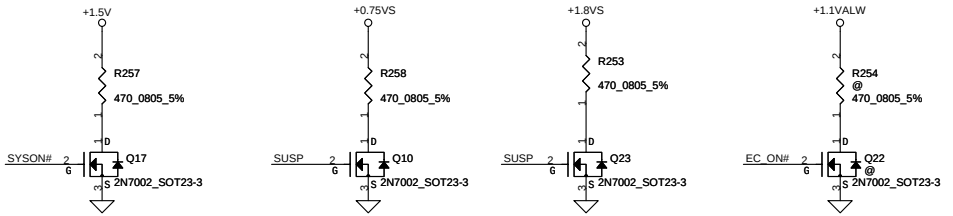


< Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >





< Discharge circuit >



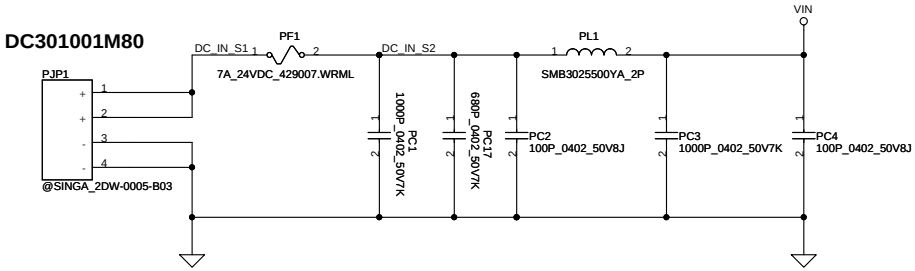
Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

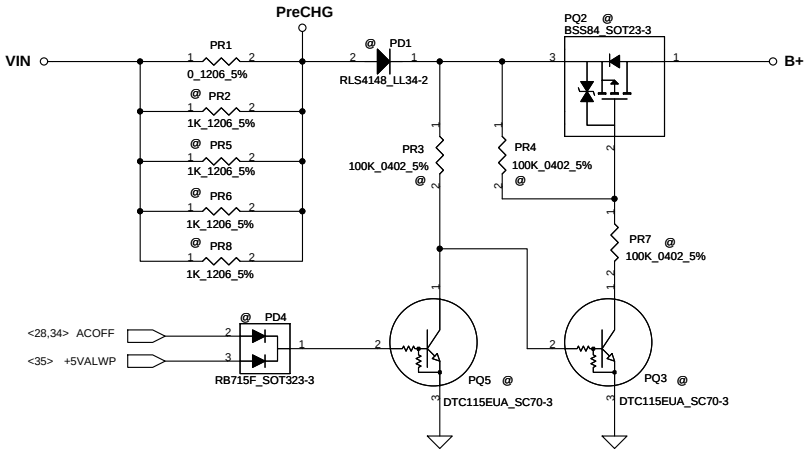
Compal Electronics, Inc.

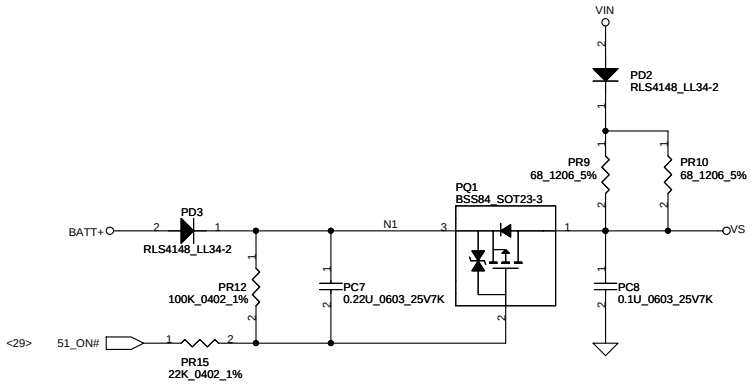
Title: **SCHEMATICS,MB A6843**

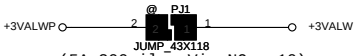
Size: Custom | Document Number: **401982** | Rev: B

Date: Wednesday, September 01, 2010 | Sheet 31 of 40

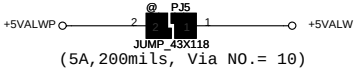




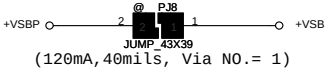




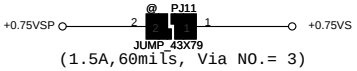
(5A,200mils, Via NO.= 10)
OCP(min) = 8.33A



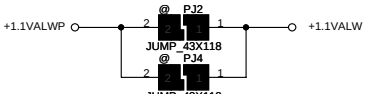
(5A,200mils, Via NO.= 10)
OCP(min) = 8.33A



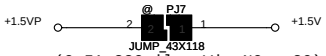
(120mA,40mils, Via NO.= 1)



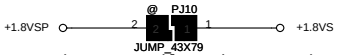
(1.5A,60mils, Via NO.= 3)



(16A,640mils, Via NO.= 32)
OCP(min) = 18.7A

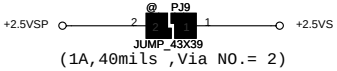


(9.5A,380mils ,Via NO.= 20)
OCP(min) = 8.7A

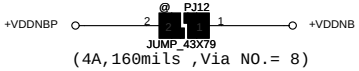


(2.5A,100mils, Via NO.= 5)

(100mA,40mils ,Via NO.= 2)



(1A,40mils ,Via NO.= 2)



(4A,160mils ,Via NO.= 8)

(1.75A,80mils, Via NO.= 4)

Precharge detector 15.97V/14.84V FOR ADAPTOR

Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6843

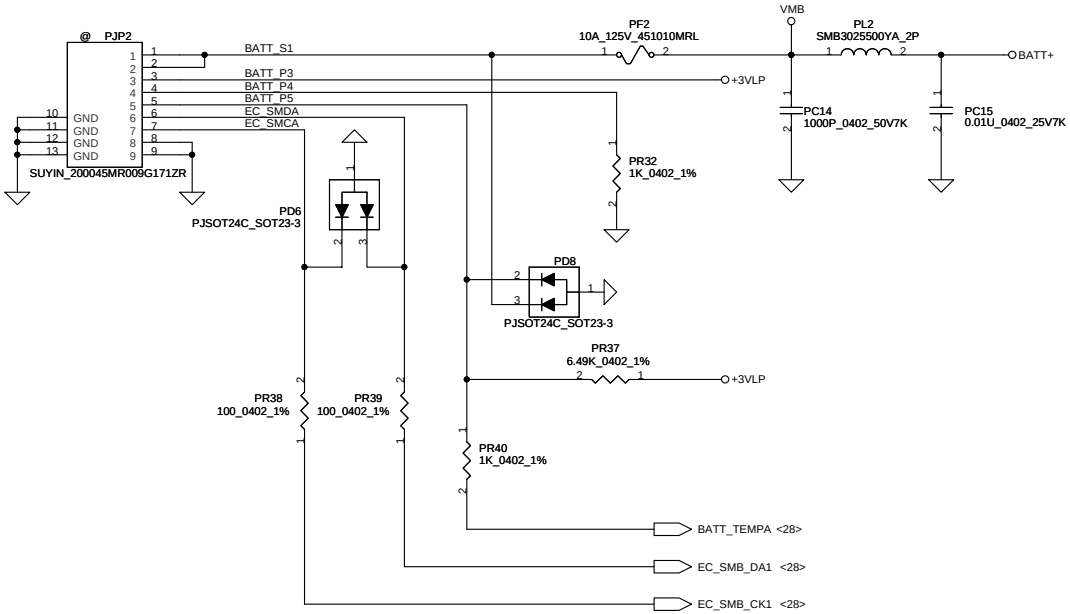
Size: C | Document Number: 401982 | Rev: B

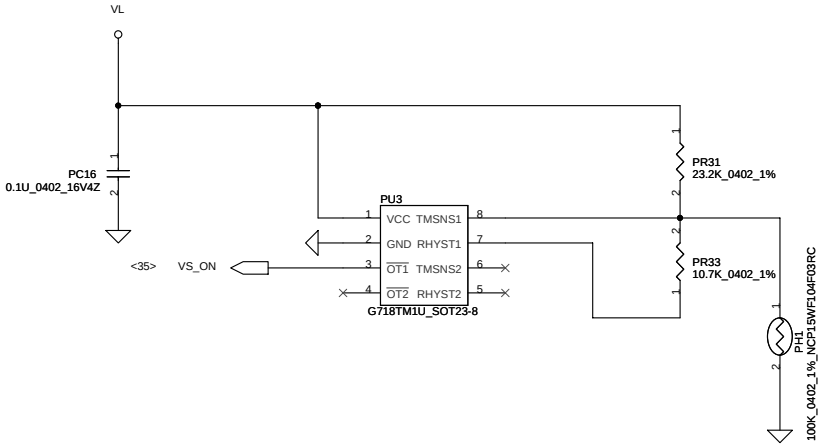
Date: Wednesday, September 01, 2010 | Sheet 32 of 40

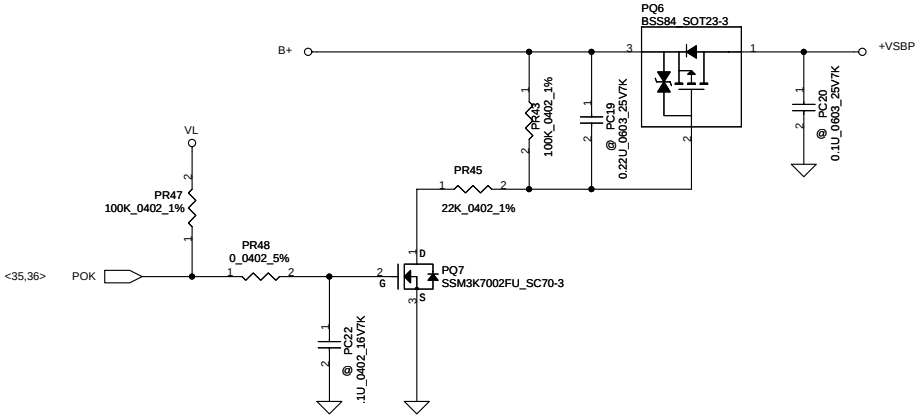
PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C

Rset = 3 * Rtmh
Rhyst = (Rset* Rtml) / (3*Rtml - Rset)

Rtmh at 95C = 6.64K, Rtml at 57C = 25.1K
Rset = 3 * 6.64K = 19.92K ==> 20K
Rhyst = (20K * 25.1K) / (3 * 25.1K - 20K) = 9.078K ==> 9.09K







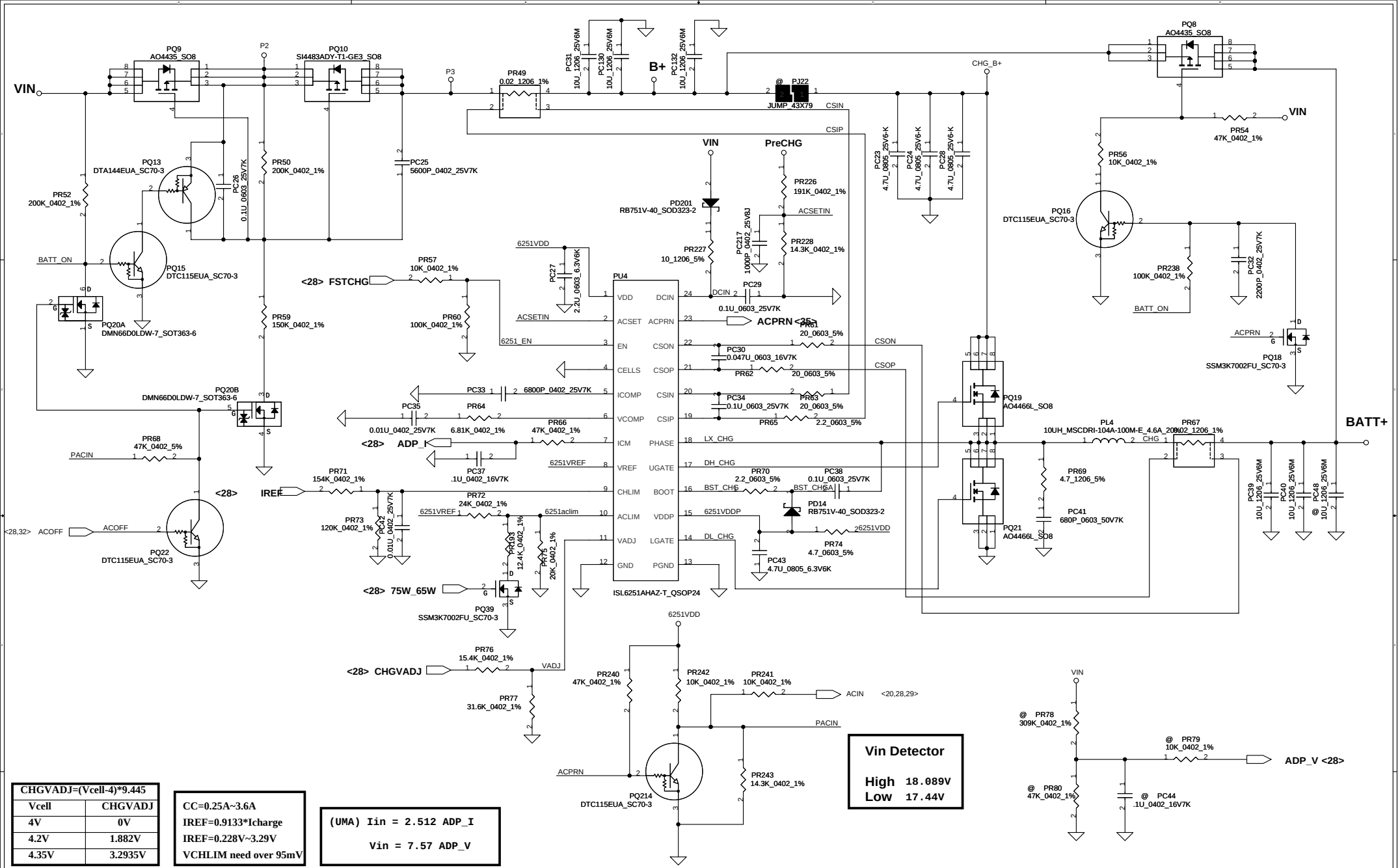
Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6843

Size	Document Number	Rev
	401982	B

Date: Wednesday, September 01, 2010 | Sheet 33 of 40



CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3.6A
IREF=0.9133*Icharge
IREF=0.228V~3.29V
VCHLIM need over 95mV

(UMA) Iin = 2.512 ADP_I
Vin = 7.57 ADP_V

Vin Detector	
High	18.089V
Low	17.44V

UMA Iada=0~3.421A(65W) CP=3.15A PR49=0.02, PR72=24k, PR75=20k, PR35=11.5K, 75W_65W=high
Iada=0~3.947A(75W) CP=3.63A PR49=0.02, PR72=24k, PR75=20k, PR35=11.5K, 75W_65W=low
CP= 92%*Iada

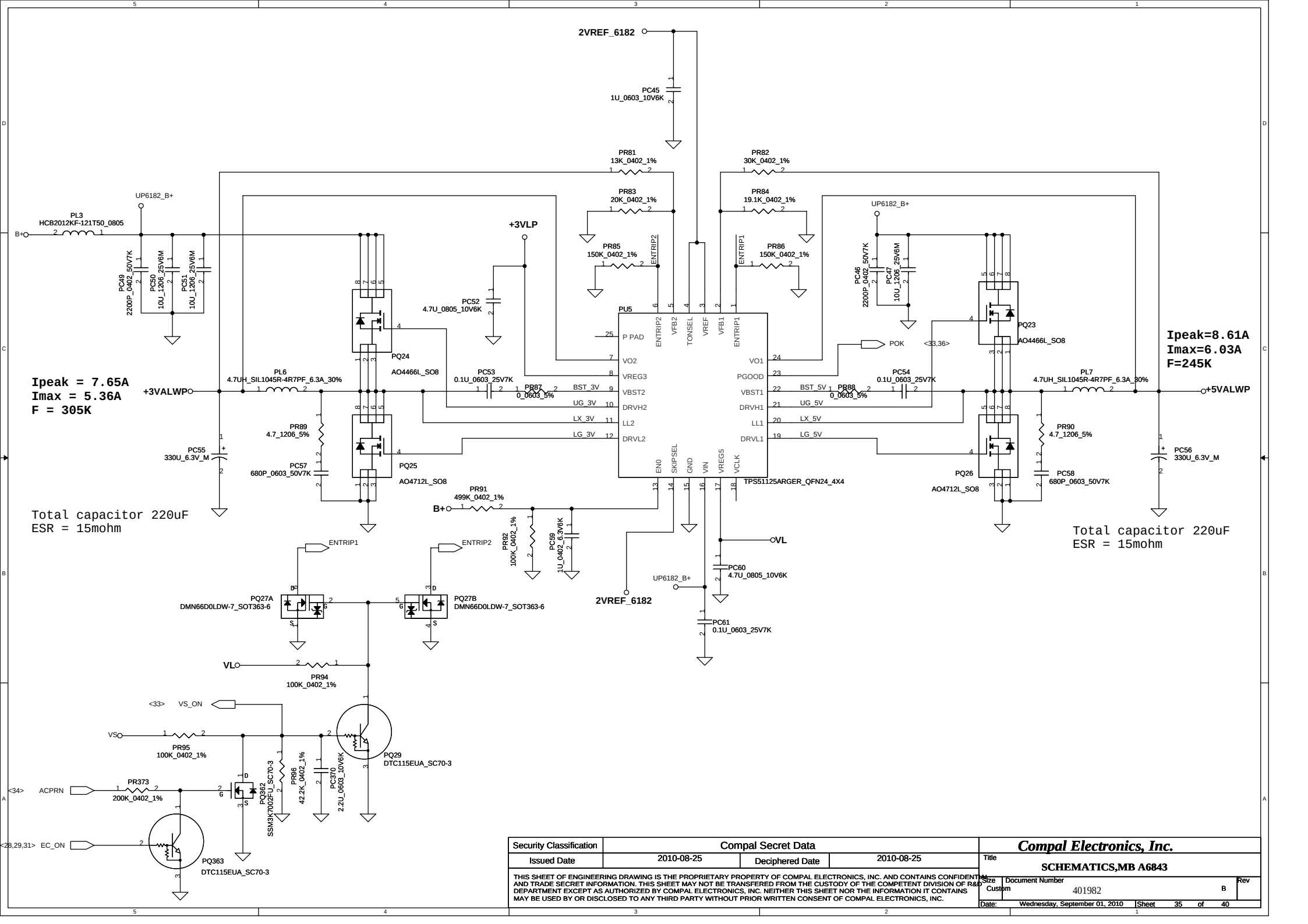
Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6843

Size	Document Number	Rev
Custom	401982	B

Date: Wednesday, September 01, 2010 Sheet 34 of 40



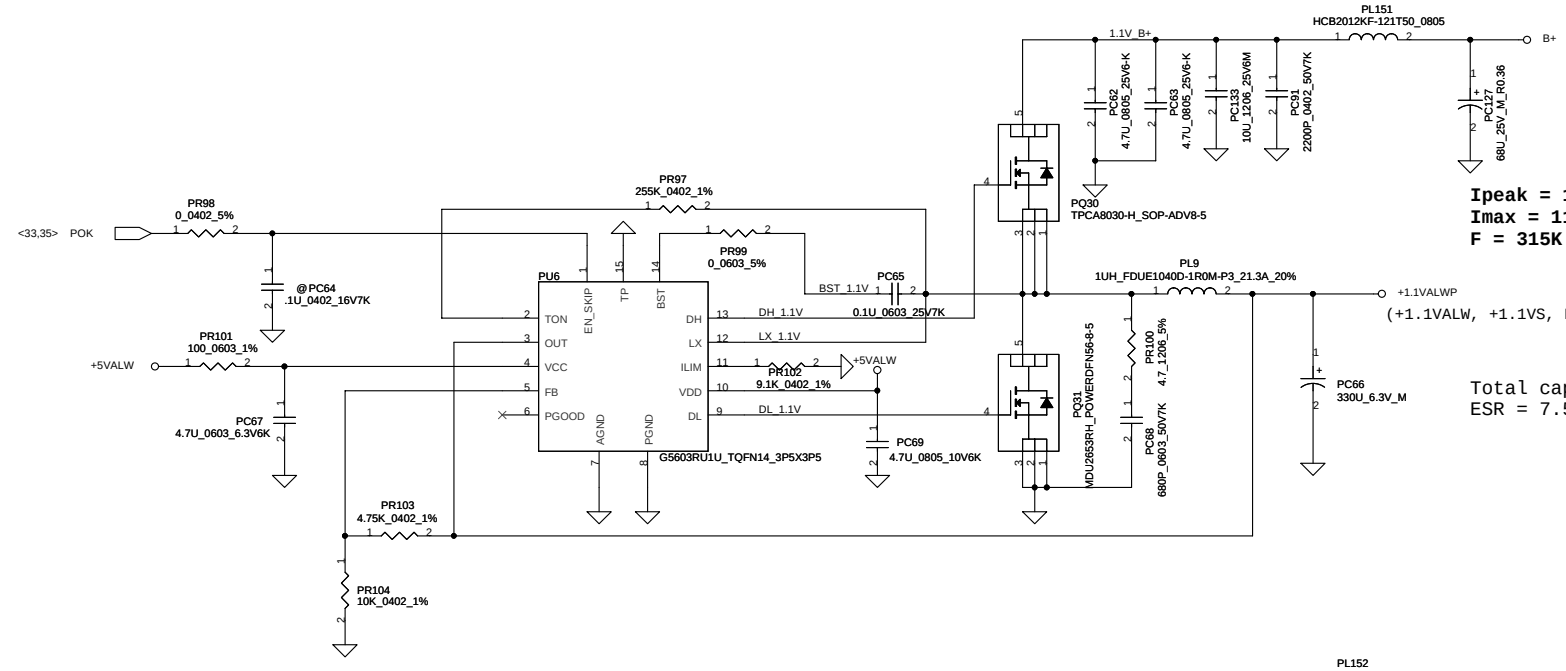
Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

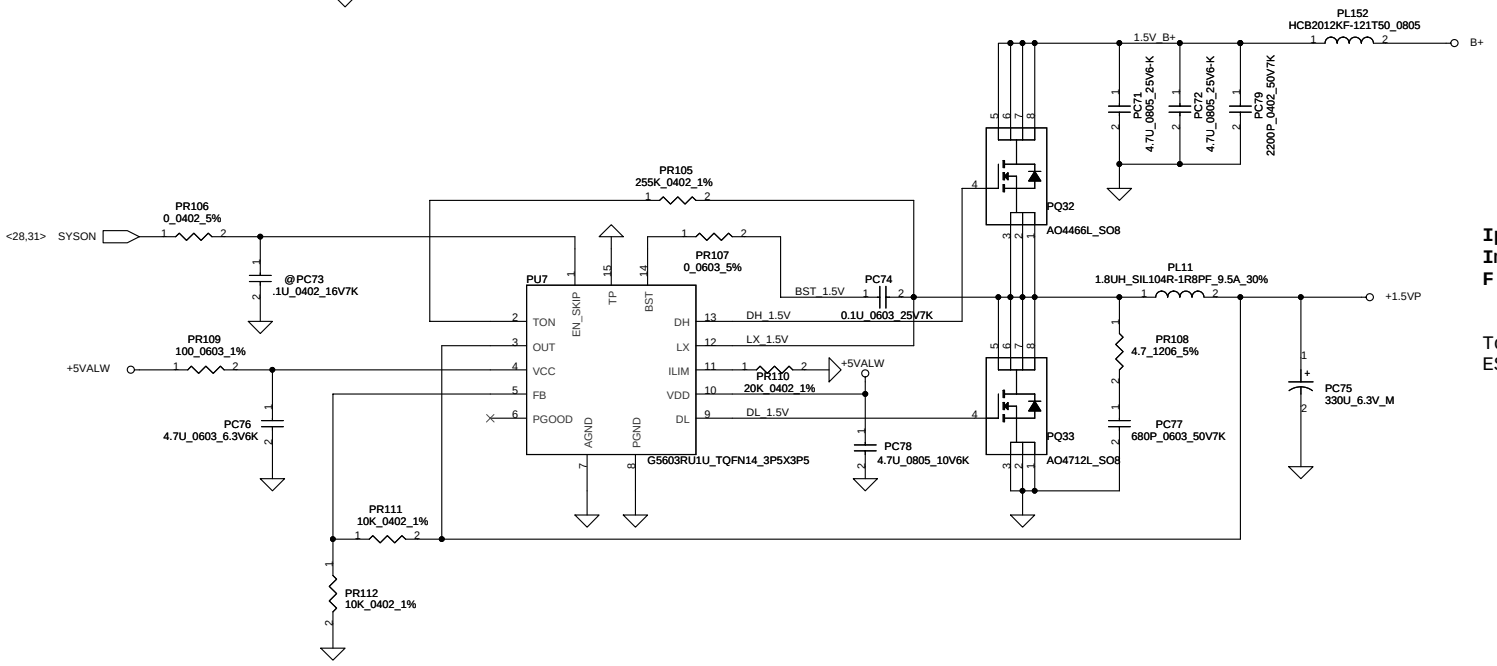
Compal Electronics, Inc.

Title: SCHEMATICS,MB A6843

Size	Document Number	Rev
Custom	401982	B

Date: Wednesday, September 01, 2010 Sheet 35 of 40

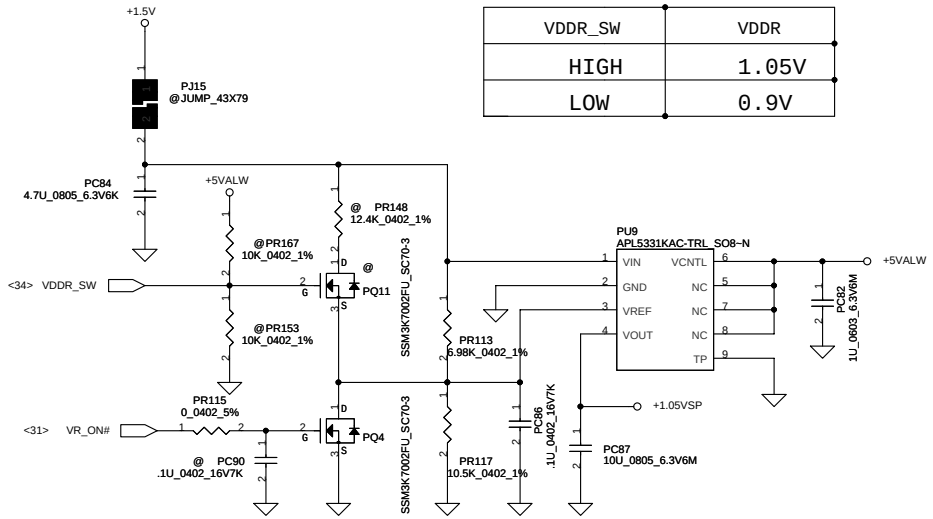


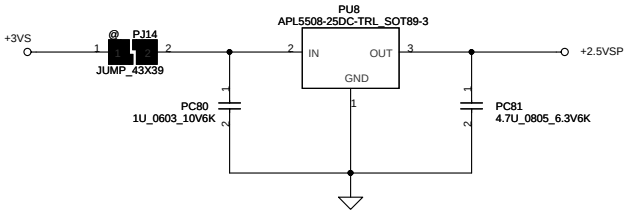


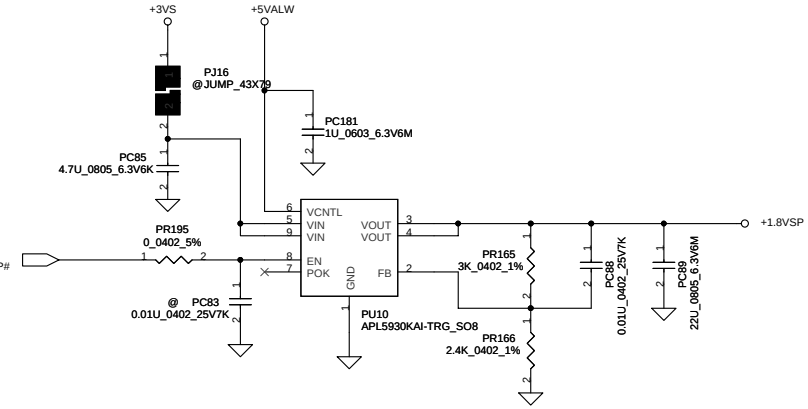
Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

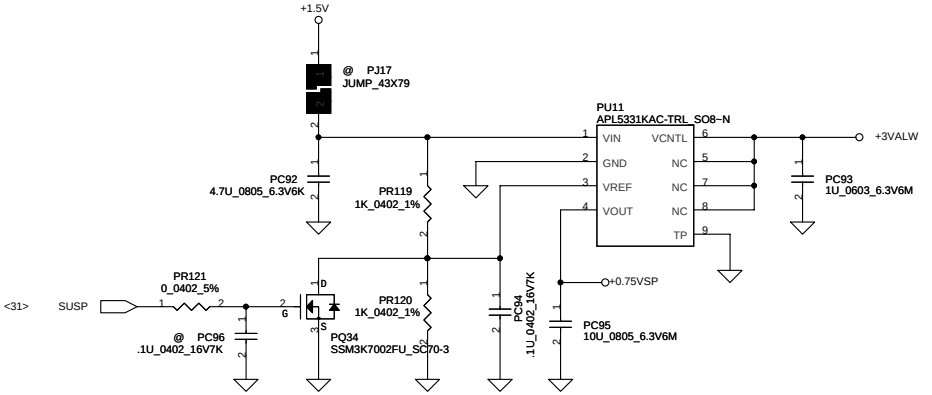
Compal Electronics, Inc.	
Title	SCHEMATICS,MB A6843
Size	Document Number 401982 Rev B
Date: Wednesday, September 01, 2010	Sheet 36 of 40

VDDR_SW	VDDR
HIGH	1.05V
LOW	0.9V







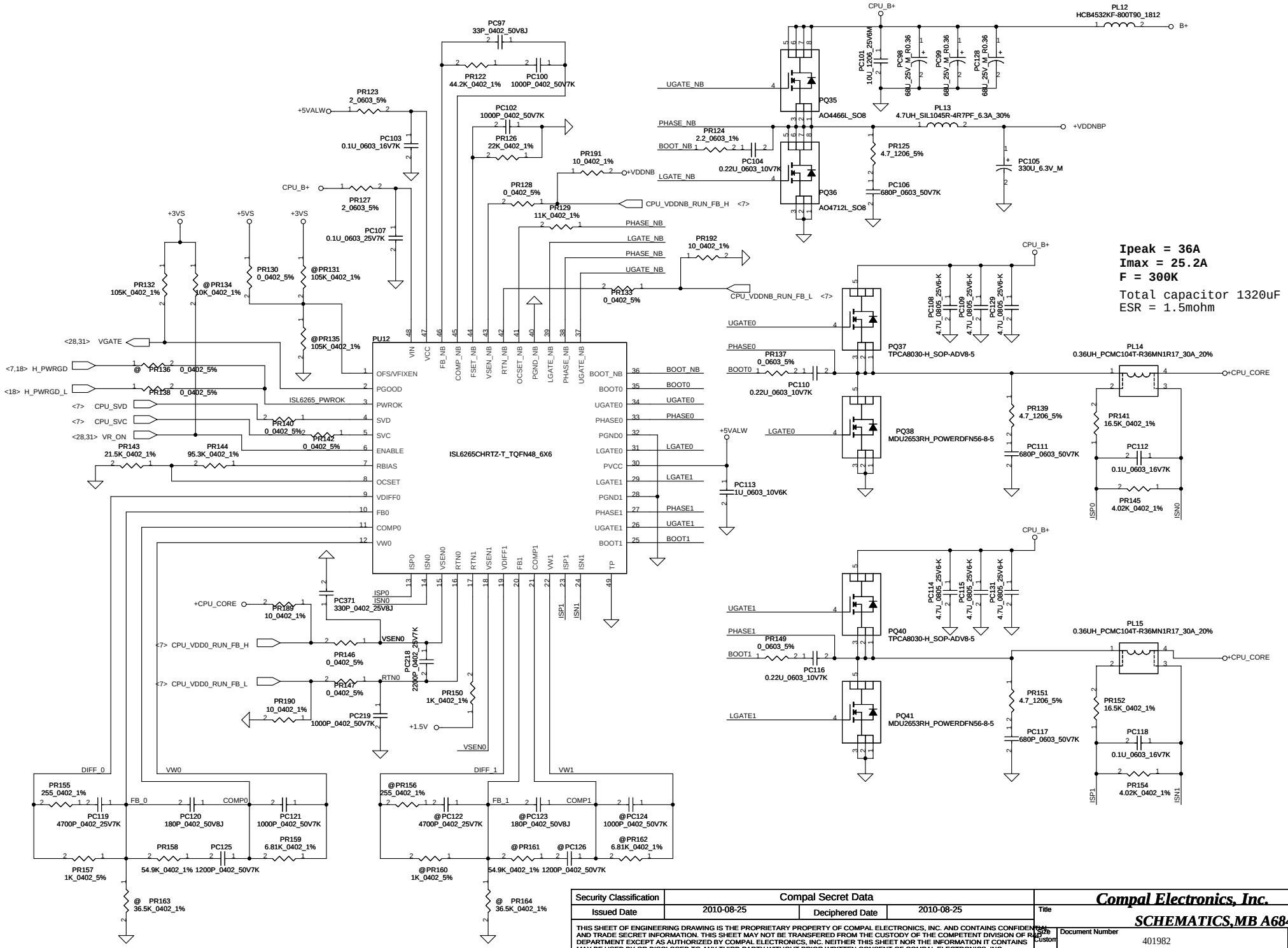


Compal Electronics, Inc.

Title: **SCHEMATICS,MB A6843**

Size: | Document Number: 401982 | Rev: B

Date: Wednesday, September 01, 2010 | Sheet 37 of 40



Security Classification	Compal Secret Data		
Issued Date	2010-08-25	Deciphered Date	2010-08-25

Compal Electronics, Inc.

Title: **SCHEMATICS,MB A6843**

Size	Document Number	Rev
Custom	401982	B

Date: Wednesday, September 01, 2010 | Sheet 38 of 40

PIR (Product Improve Record)

PWWAE LA-6843P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2010/07/20	28	Reserve C1199,Y5,C1200	For design change
2	2010/07/20	28	Reserve R436 for only KB926E0	For design change
	2010/07/20	29	Del R875	For SERIRQ direct connect to H7.7
	2010/07/20	29	Del C588/C589/Y4/R368	For design change
3	2010/07/21	11~15	Change U8 R1 P/N from A12(SA000032WI40) to A13(SA000032WA0)	For SB820 A13 version
	2010/07/21	30	Change U8 R3 P/N from A12(SA000032WI50) to A13(SA000032WB0)	For SB820 A13 version
4	2010/07/23	18	Change D8 from DAN202U to CHN202UPT	For design change
5	2010/07/23	24	Chagne UL4 from LF-H1201P-2 to LFE8456E-R for use 5mA type	For design change
6	2010/07/23	30	Change R768/R773 from 120 to 510 ohm for use 5mA type	For design change
			Change R768.1 pull up from +3VALW to +5VALW for use 5mA type	For design change
			Change R773.1 pull up from +3VALW to +5VALW for use 5mA type	For design change
7	2010/07/23	27	Change JLINE/JEXMIC to FOX_JA6331-B39S4-7F	For DFX request
8	2010/07/26	23	Reserve DM2	For +3V_WLAN is +3VS
9	2010/07/26		Add R50	For Intel Rainbow Peak module
	2010/07/26	24	Reserve CL39	For EMI request
10	2010/07/27	28	Change R867 pull up from +3VALW to +3VL	For design change

REVISION CHANGE: 0.2 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2010/08/06	29	Change U13 footprint to M25P10-AVMN6T-SOP	For design change
2	2010/08/06	25	Change Net name form V1_8 to +V1_8	For customer request
	2010/08/06	29	Add R774 link to BATT_CHG_LOW_LED#	For customer request
	2010/08/06	29	Change R773 link to BATT_FULL_LED#	For customer request
3	2010/08/06	30	Reserve SW6 Del SW5	For debug phase
	2010/08/09	30	Chagne UL4 from NS681680 to NS681610	For design change
4	2010/08/09	08	Mount C26/C89,Reserve C24,C90	For design change
5	2010/08/16	18	Del R42/C94	For EMI request
	2010/08/16	18	Reserve CC9/RC7	For EMI request
6	2010/08/16	24	Add CL3/CL7 link to +3V_LAN	For EMI request
			Reserve CL38	For EMI request
			Change CL37 from 0.1uF to 120 pF	For EMI request
			Add D13 link to LANGND	For EMI request

Size	Document Number	Rev
	401982	B
Date: Wednesday, September 01, 2010	Sheet 39 of 40	

Version Change List (P. I. R. List) for Power Circuit

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE	Rev.
	2010 . 06 . 21 Release				
	2010 . 07.25 modification list				
		P 33	PC16 change to SE070104Z80	Defore material EOL	PVT
		P 38	PU12 change to SA000022M80	Before material MP schedule will impact PWWAE MP schedule	PVT
		P 33	Remove PD6 , PD8 @	ESD test fail	PVT
		P 34	Add PC132 , remove PC130 , PC131 , PR69 , PC41 @	For EMI fail	PVT
		P 35	Add PC51 , remove PC49 , PC46 , PC57 , PC58 , PR89 , PR90 @	For EMI fail	PVT
		P 36	Add PC79 , PC91 , PC133 , remove PR100 , PR108 , PC68 , PC77 @	For EMI fail	PVT
		P 38	Remove PR125 , PR139 , PR151 , PC106 , PC111 , PC117 @	For EMI fail	PVT
	2010 . 08.10 modification list				
		P 37	Change PU9 , PU11 to SA053310110	UP7711 stop using from now on	Pre-MP
		P 38	Add PC218 , PC219 , PC371	For VCORE Ripple	Pre-MP
		P 32	Add PR8	For Precharge rising current	Pre-MP
		P 32 , P 33	PQ1 , PQ2 , PQ6 change to SB900840003	SB906100210 material delivery had problem	Pre-MP
	2010 . 08.16 modification list				
		P 35	Change PU5 to SA000020C80	UPI product stop using	Pre-MP
	2010 . 08.17 modification list				
		P 34	Change PU4 to SA00001EP80	SA00003TK00 stop using	Pre-MP
		P 38	Remove PR127 @	To solve +1.1VALW noise	Pre-MP
	2010 . 08.23 modification list				
		P 34	Remove PR193 , PQ39 @	For PWWAE MP use 25W CPU	Pre-MP

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6843

Size: Custom | Document Number: 401982 | Rev: B

Date: Wednesday, September 01, 2010 | Sheet 40 of 40