

Compal confidential

Schematics Document

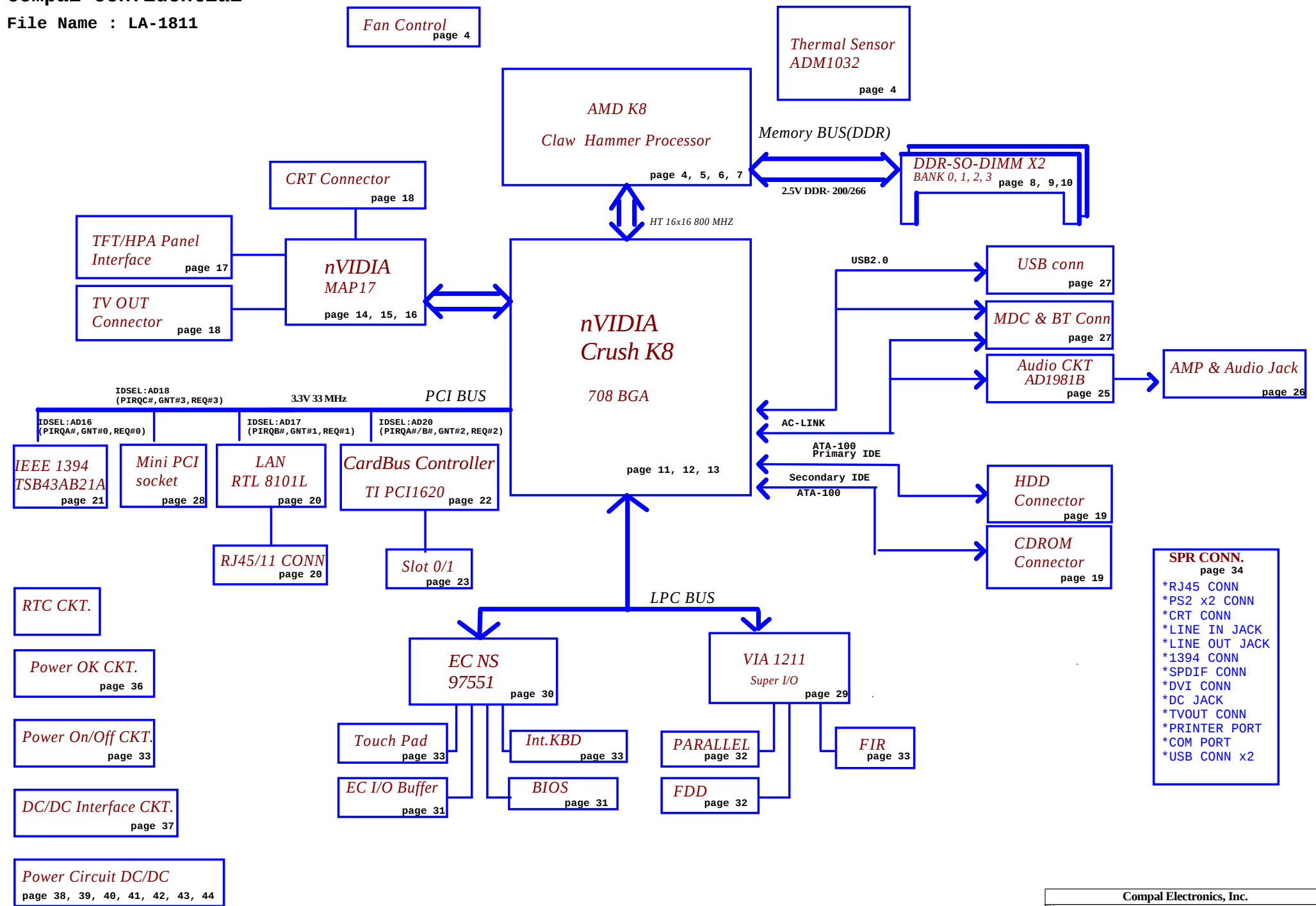
ClawHammer AMD K8 with nVIDIA Chrush K8

2004-04-16

REV: 0.1

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Compal Electronics, Inc.			
Title			
Cover Sheet			
Size	Document Number		Rev
	LA-2392		0.1
Date:	Friday, April 16, 2004		Sheet 1 of 53



Voltage Rails

power plane State	+1.2VALW +3VALW +5VALW 12VALW	+1.25V +2.5V +3V +5V	+1.2V_HT +1.2VS +1.5VS +2.5VS +3VS +5VS
S0	0	0	0
S1	0	0	0
S3	0	0	X
S5 S4/AC	0	X	X
S5 S4/AC don't exist	X	X	X

0 MEANS ON
X MEANS OFF

PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
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INTERNAL

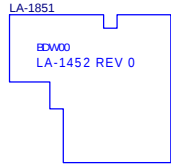
USB 2.0	2	AD13	N/A	G
AC97 MODEM	6	AD17	N/A	M
AC97	6	AD17	N/A	L
ATA 100	8	AD20	N/A	
ETHERNET	5	AD16	N/A	K
LPC I/F	1	AD12	N/A	
SMBUS	1	AD12	N/A	F

EXTERNAL

VGA	0	AD16	N/A	E
1394	0	AD16	0	A
LAN	1	AD17	1	B
CARD BUS	4	AD20	2	A, B
Wireless LAN	2	AD18	3	C
Mini-PCI (no use)	3	AD19	4	D

<11> H_CADIP[0..15] H_CADIP[0..15]
<11> H_CADIN[0..15] H_CADIN[0..15]

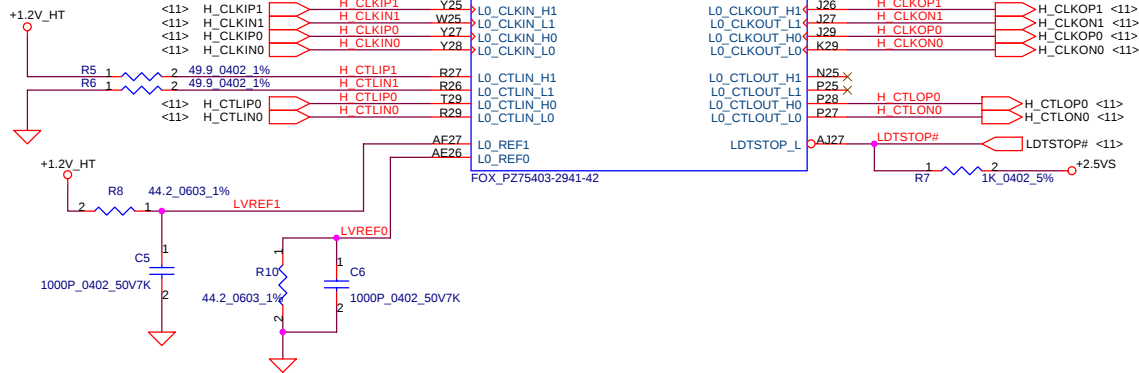
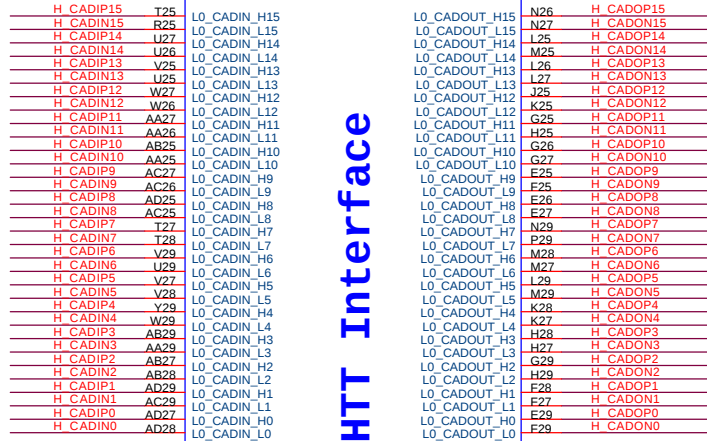
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H_CADON[0..15] H_CADON[0..15] <11>



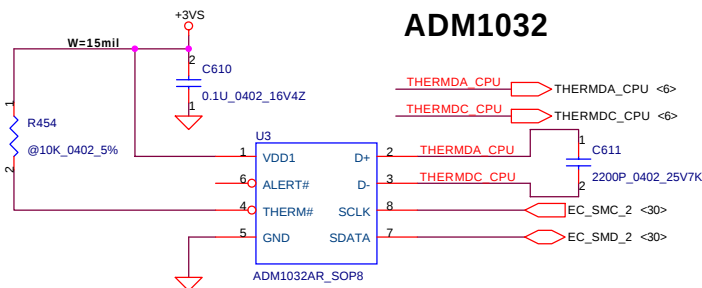
U1A

Claw Hammer-DTR

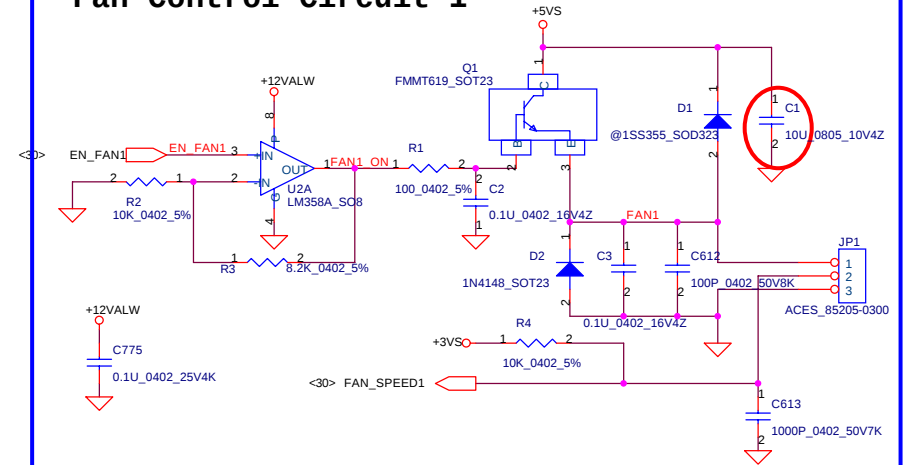
HTT Interface



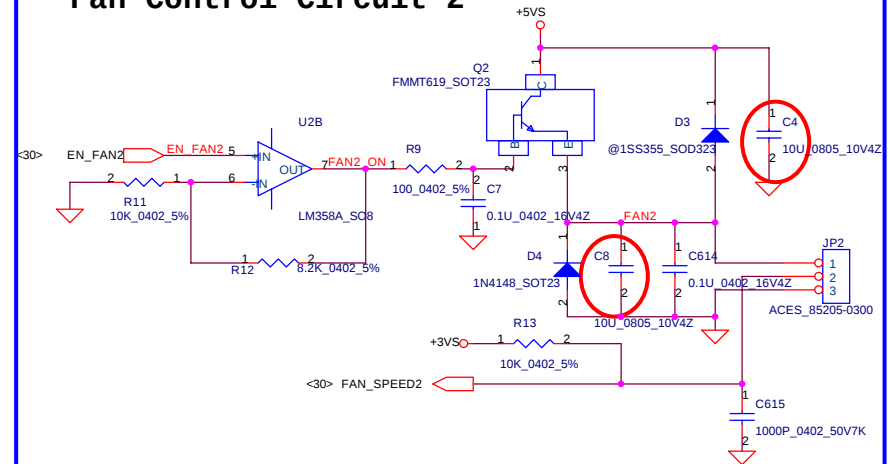
Thermal Sensor ADM1032



Fan Control Circuit 1



Fan Control Circuit 2

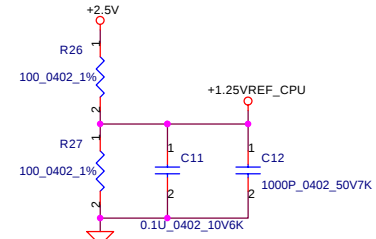


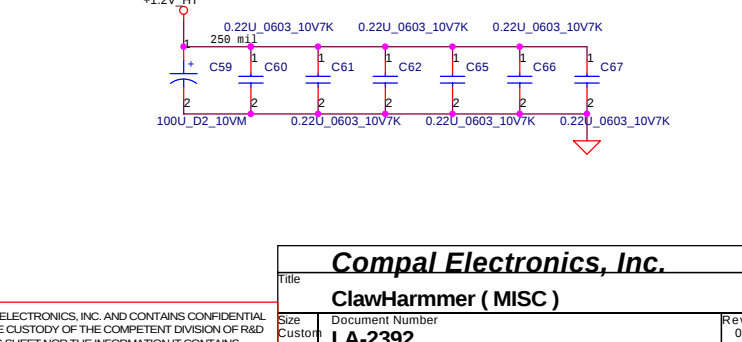
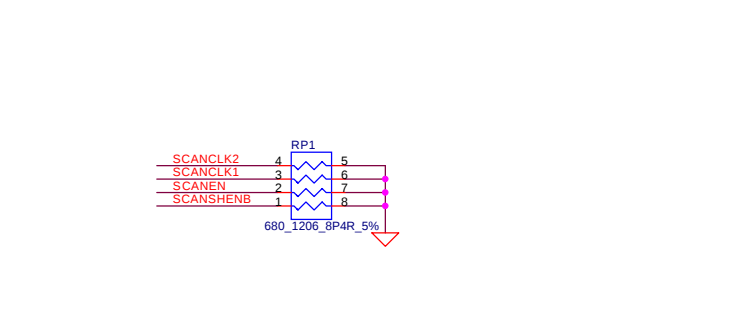
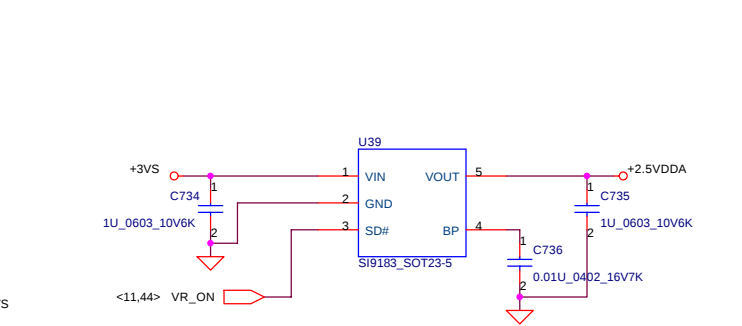
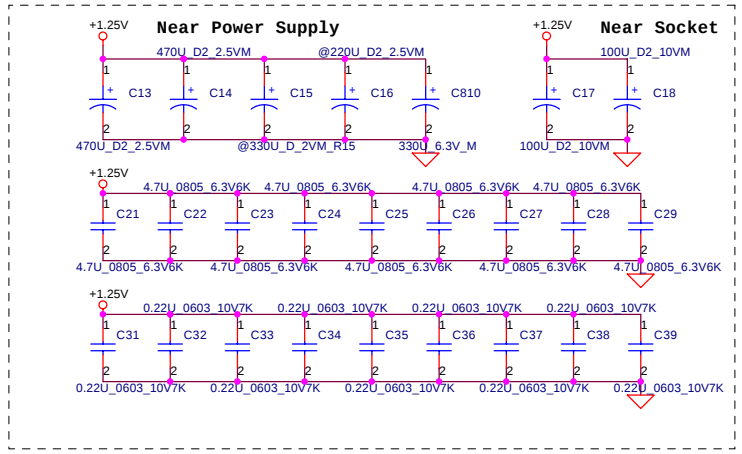
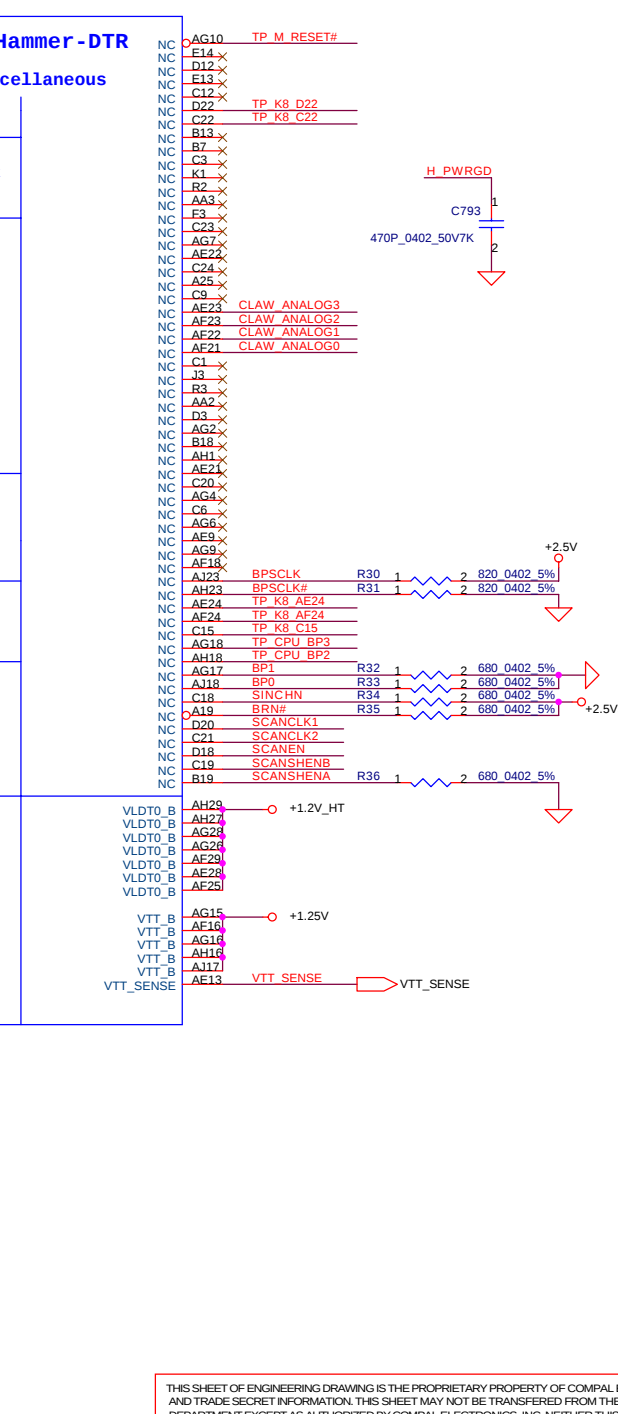
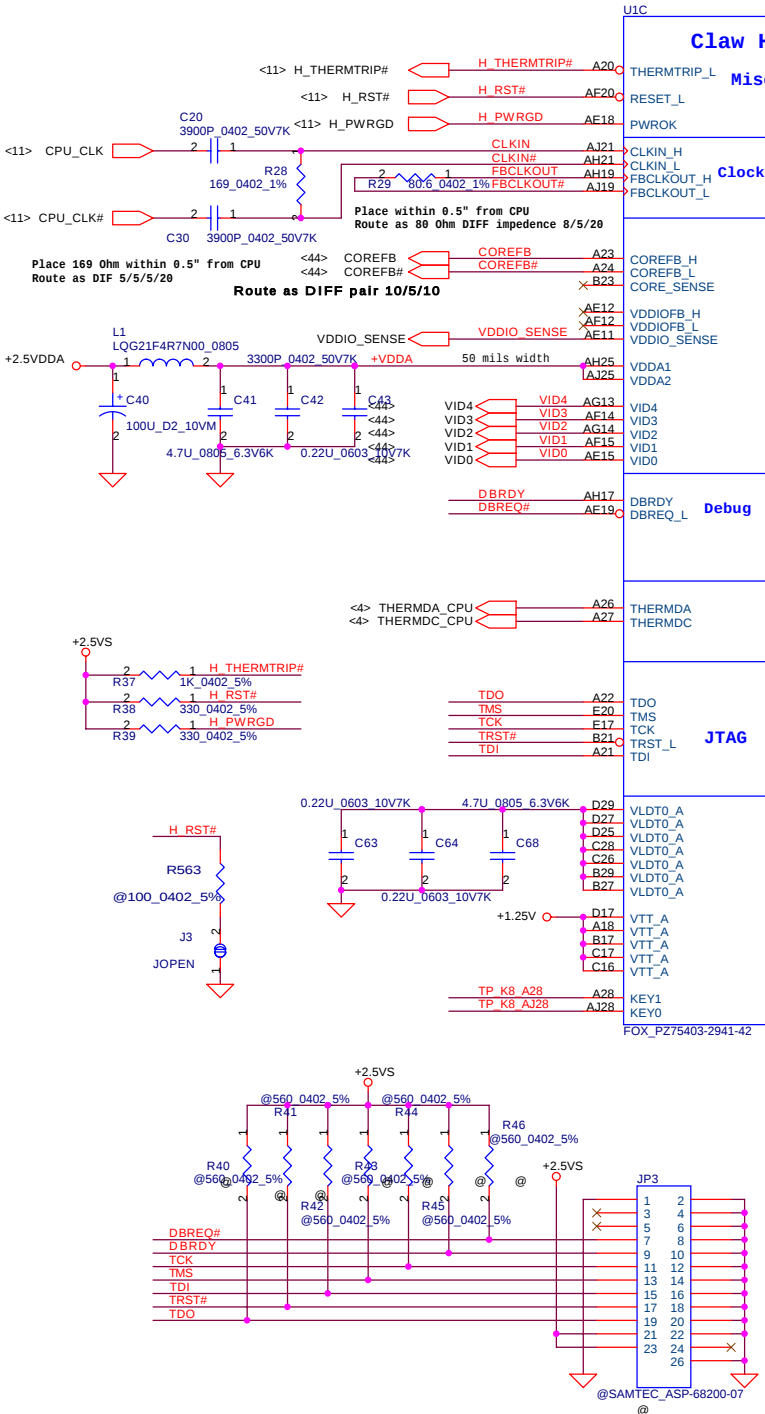
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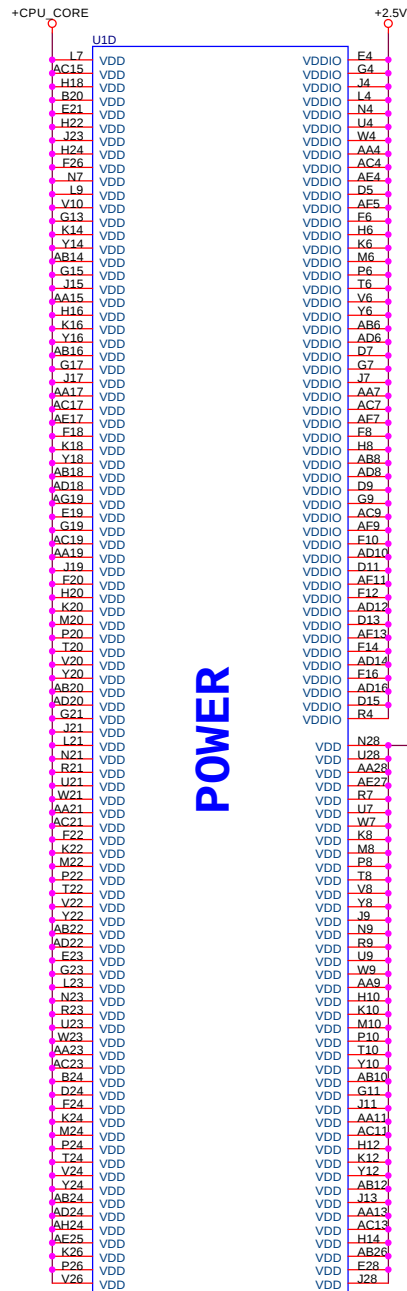
Claw Hammer CPU (Host Bus)

Title	LA-2392	Rev	0.1
Size	Custom	Document Number	
Date:	Friday, April 16, 2004	Sheet	4 of 53

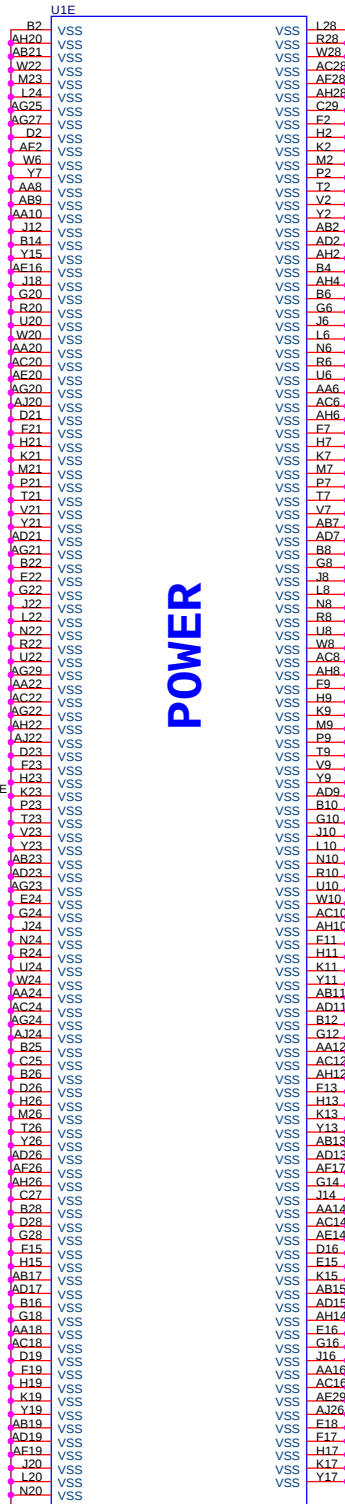
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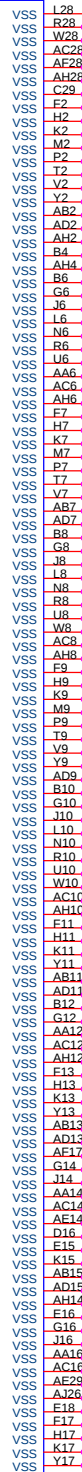


FOX_PZ75403-2941-42

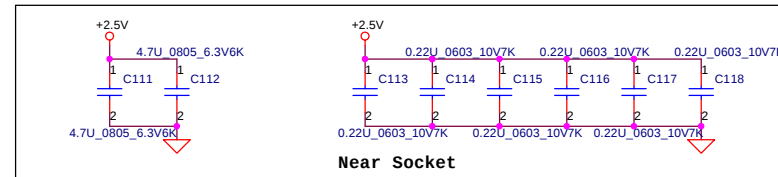
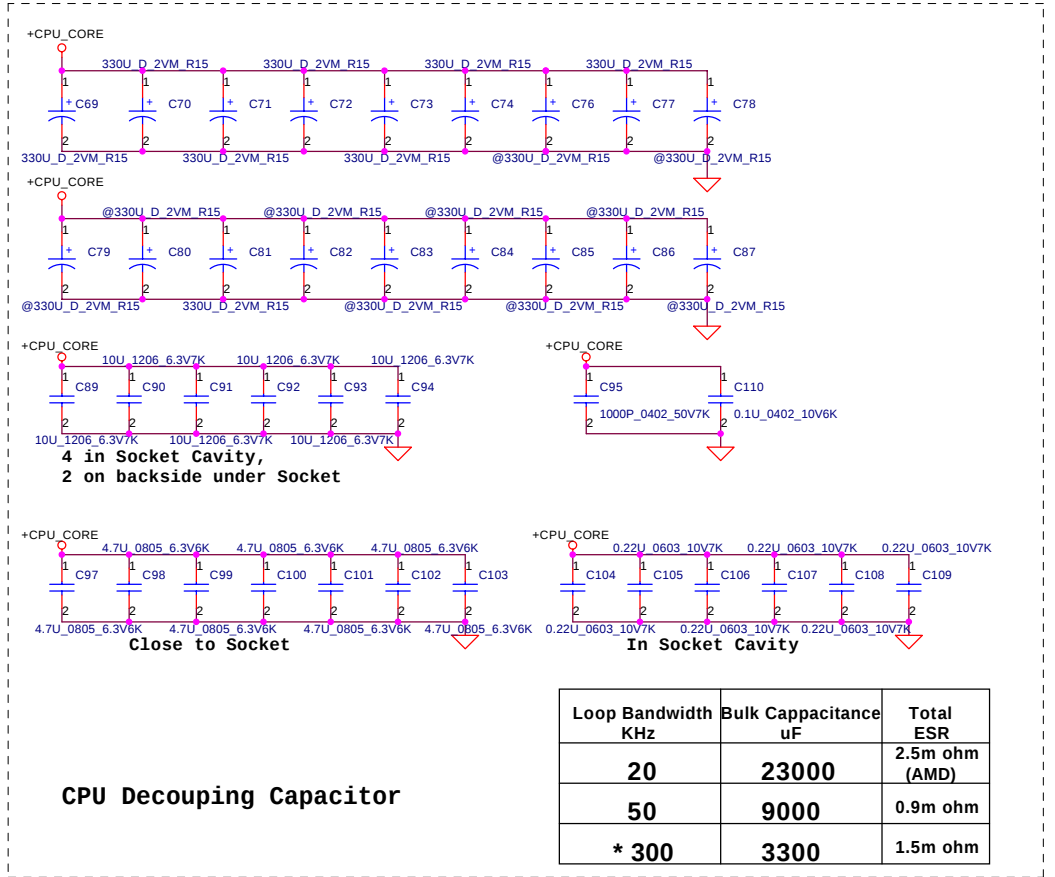


FOX_PZ75403-2941-42

POWER

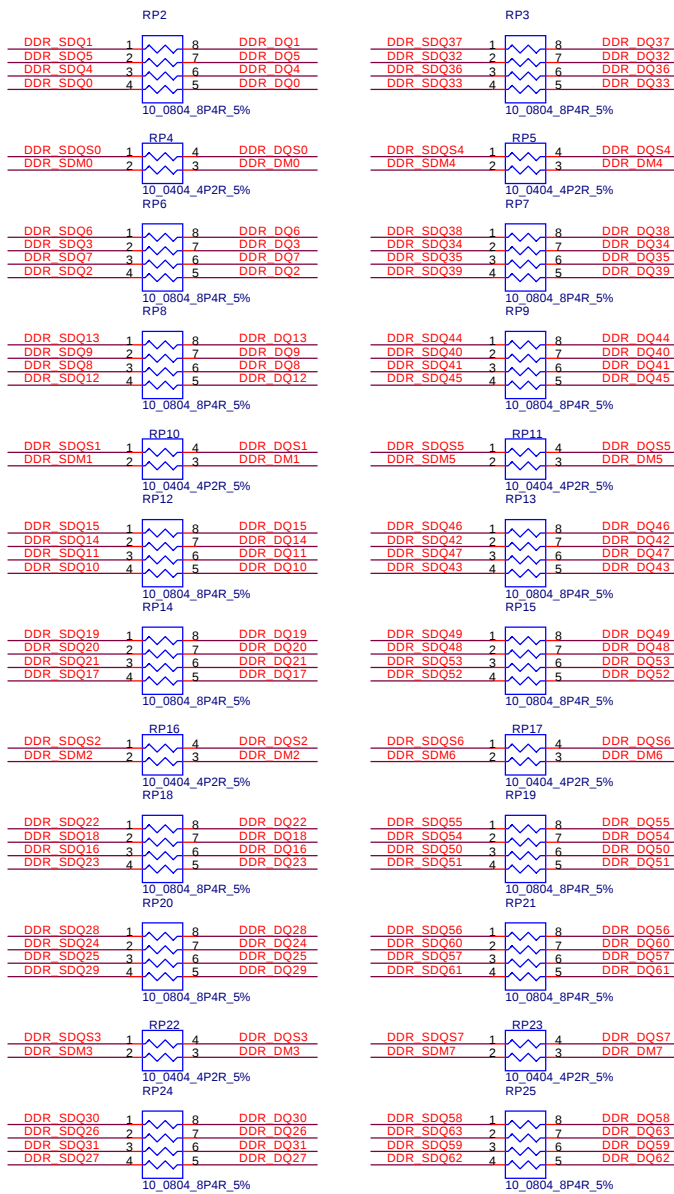


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Near Socket

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Claw Hammer (Power & Ground)		
Title	Document Number	Rev
	LA-2392	0.1
Date:	Friday, April 16, 2004	Sheet 7 of 53



Note:
DDR_SMAA13 Recommend for AMD

Layout note
Place these resistors
close to DIMM0,
all trace length<500 mil

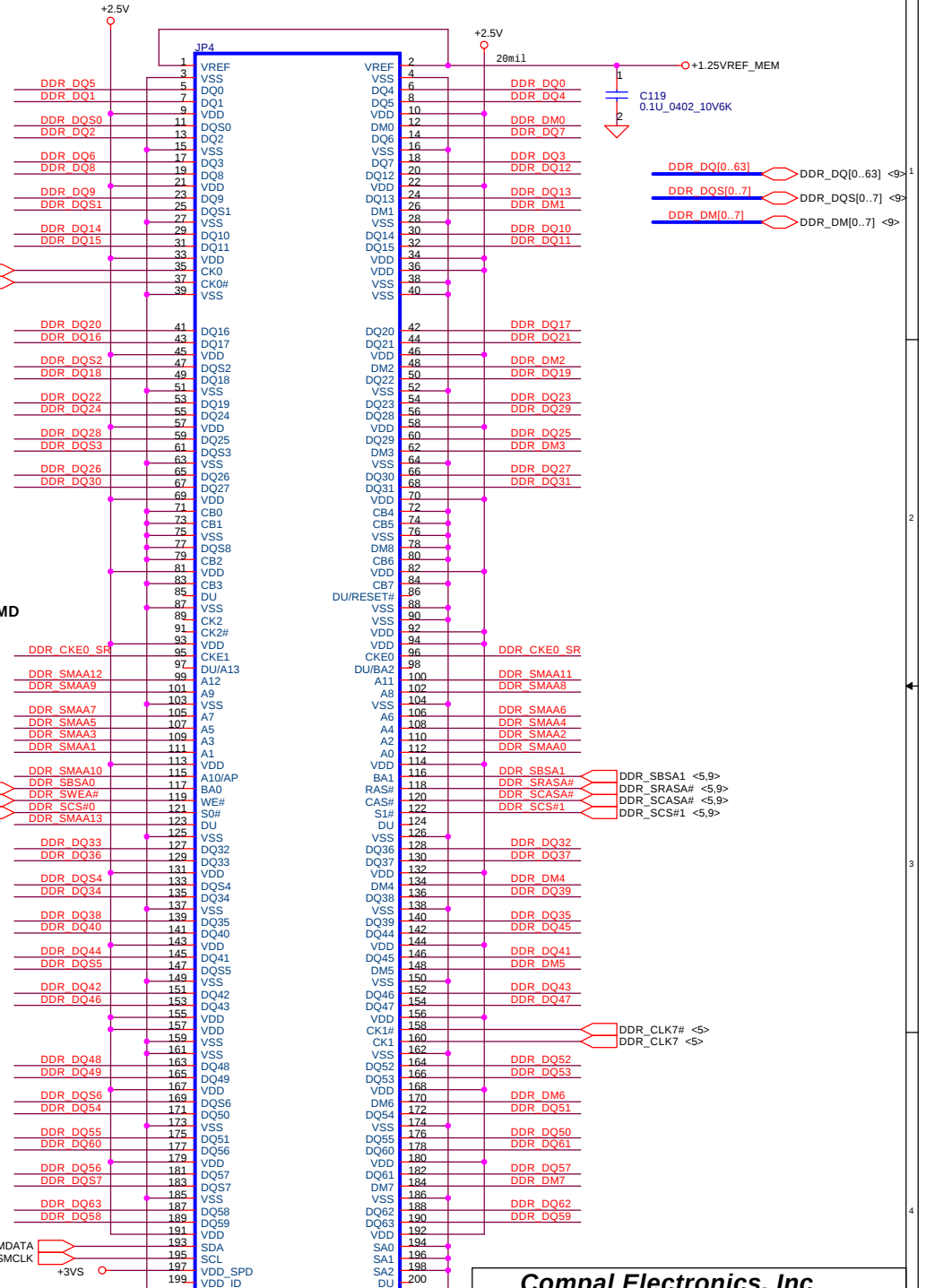
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<5> DDR_SDQ[0..63] DDR_SDQ[0..63]
<5> DDR_SDM[0..7] DDR_SDM[0..7]
<5,9> DDR_SMAA[0..13] DDR_SMAA[0..13]

<5> DDR_CKE0 R47 DDR_CKE0_SR DDR_CKE0_SR <9>
<5> DDR_CKE1 R48 DDR_CKE1_SR DDR_CKE1_SR <9>

<5> DDR_CLK5
<5> DDR_CLK5#

<5,9> DDR_SBSA0
<5,9> DDR_SWEA#
<5,9> DDR_SCS#0

<9,12> DIMM_SMDATA
<9,12> DIMM_SMCLK
+3VS



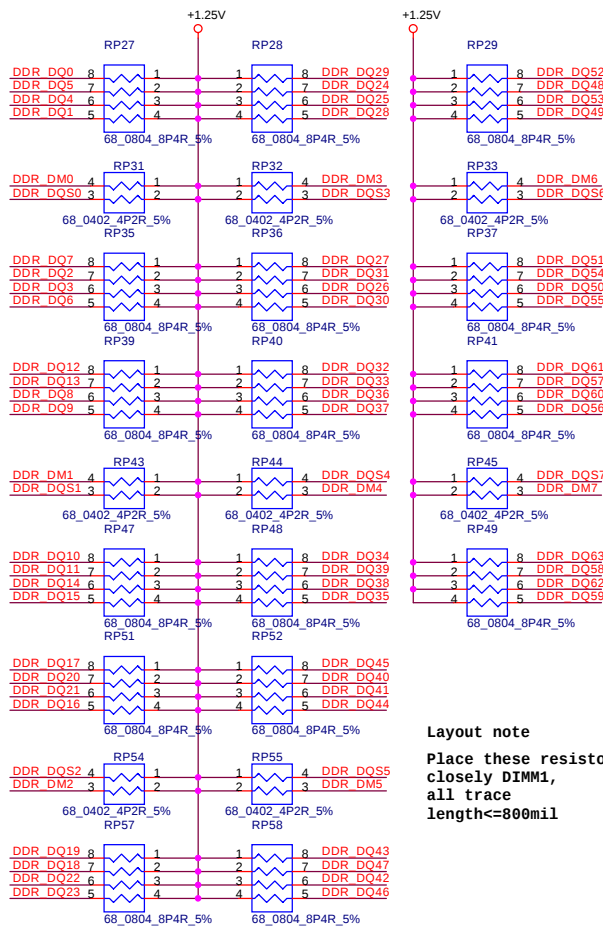
SO-DIMM0
REVERSE

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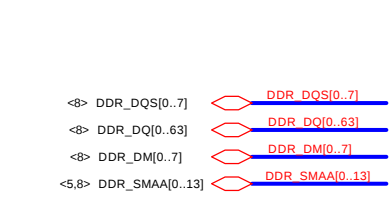
DDR-SODIMM SLOT0

Size	Document Number	Rev
Custom	LA-2392	0.1
Date:	Friday, April 16, 2004	Sheet 8 of 53

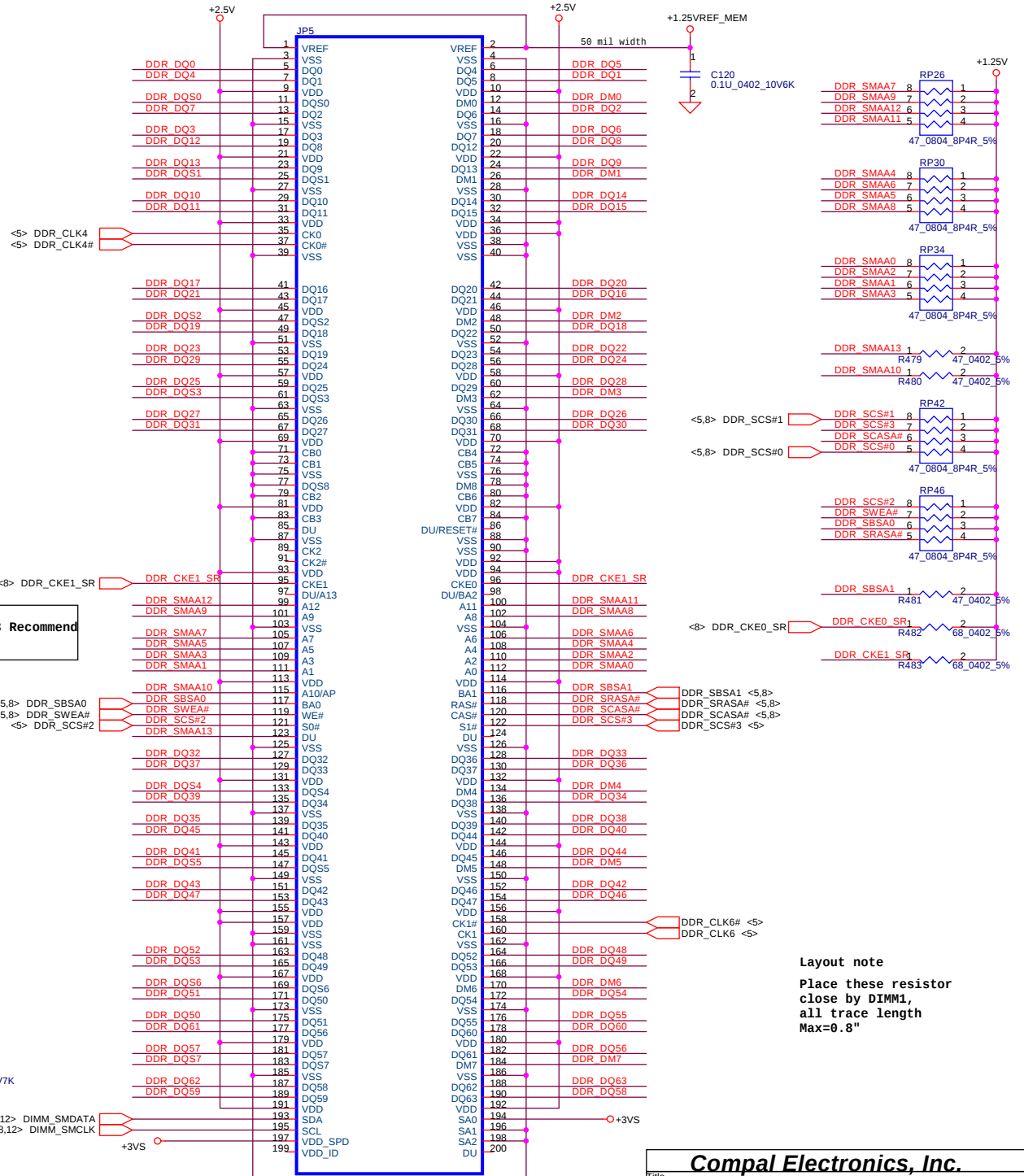
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Note:
DDR_SMAA13 Recommend
for AMD.



<8,12> DIMM_SMDATA
<8,12> DIMM_SMCLK

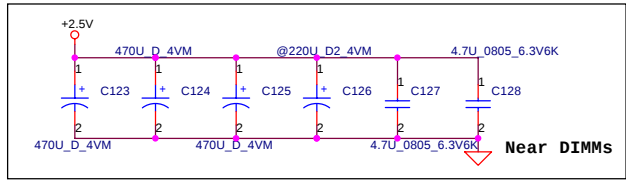


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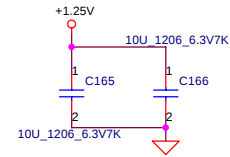
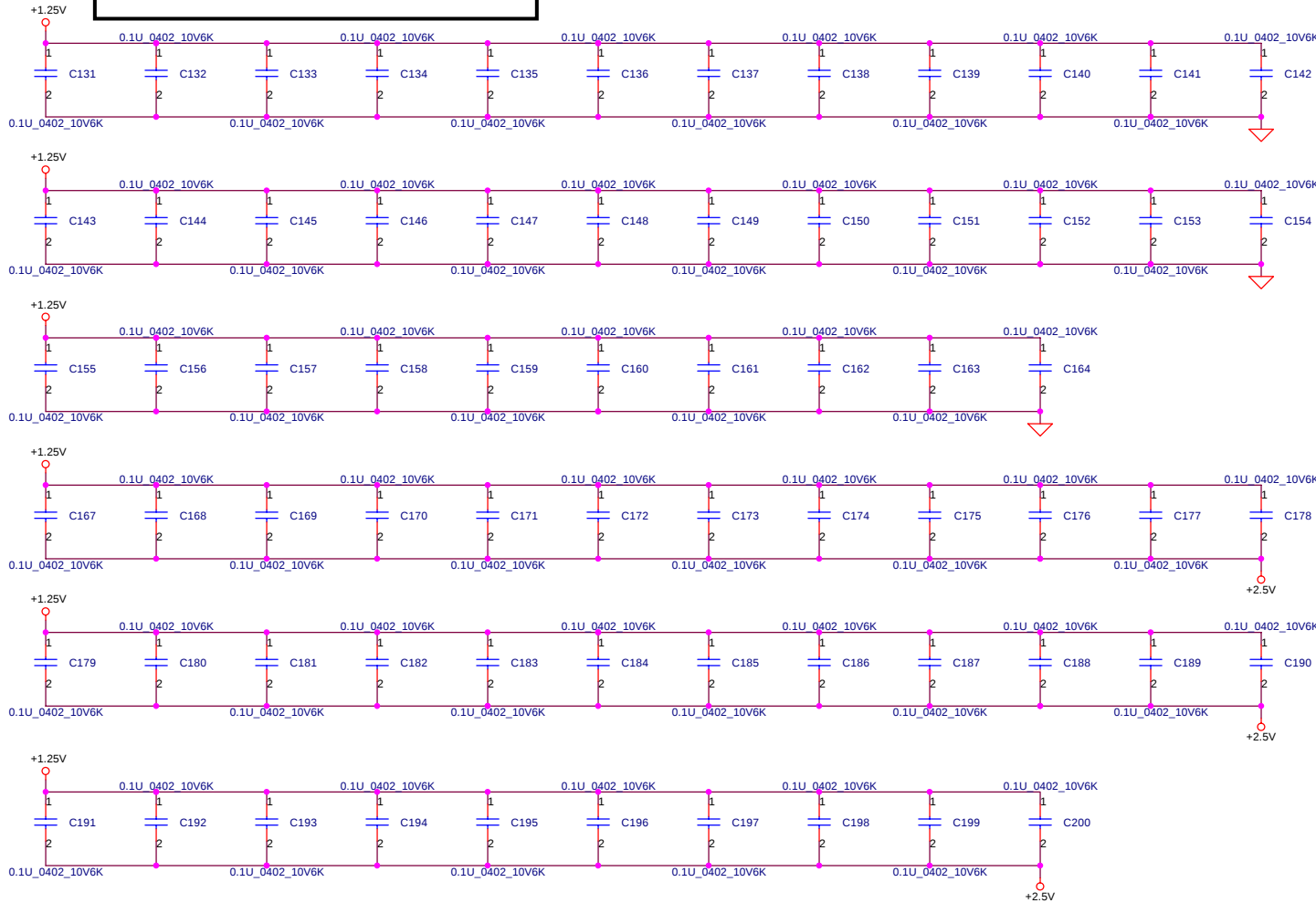
DDR-SODIMM SLOT1

Size	Document Number	Rev
Custom	LA-2392	0.1
Date:	Friday, April 16, 2004	Sheet 9 of 53

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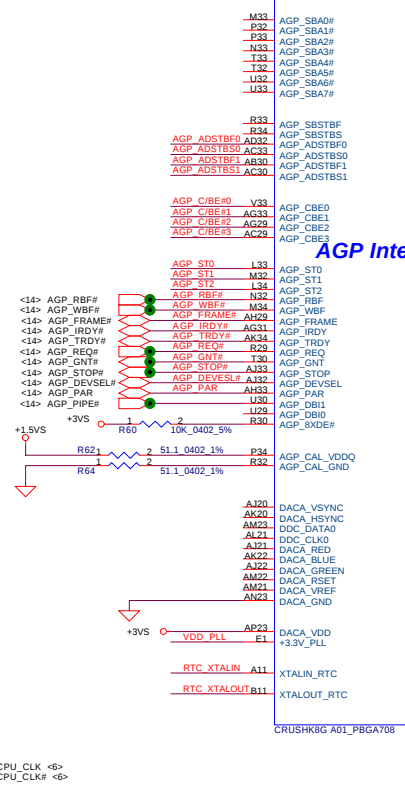
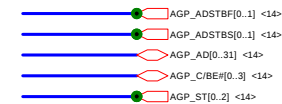


Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25VS

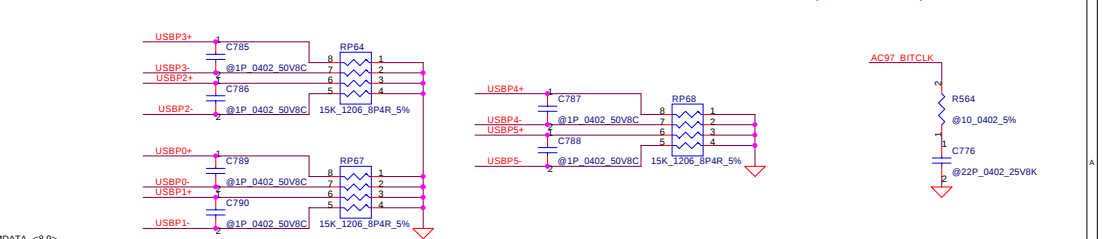
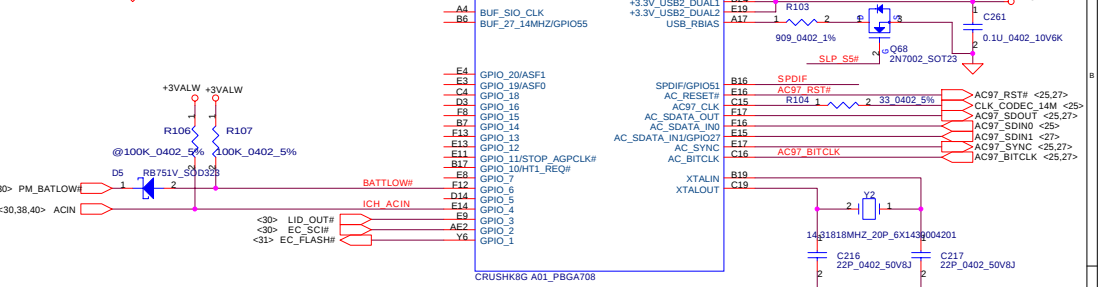
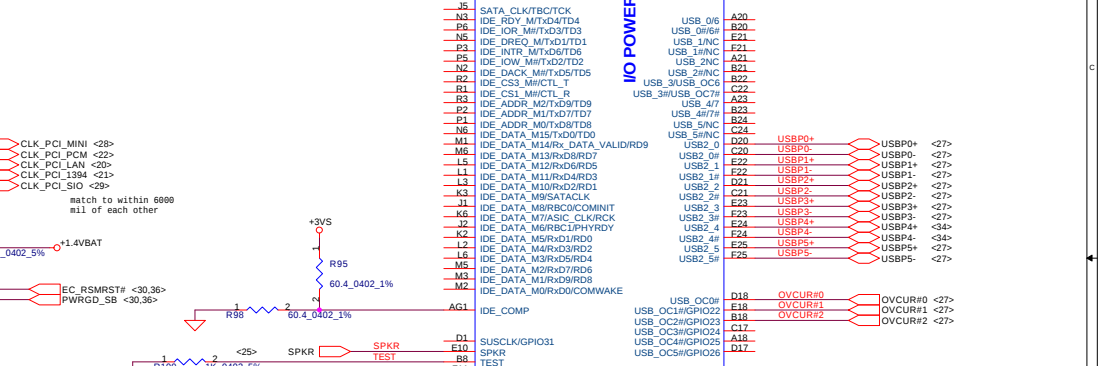
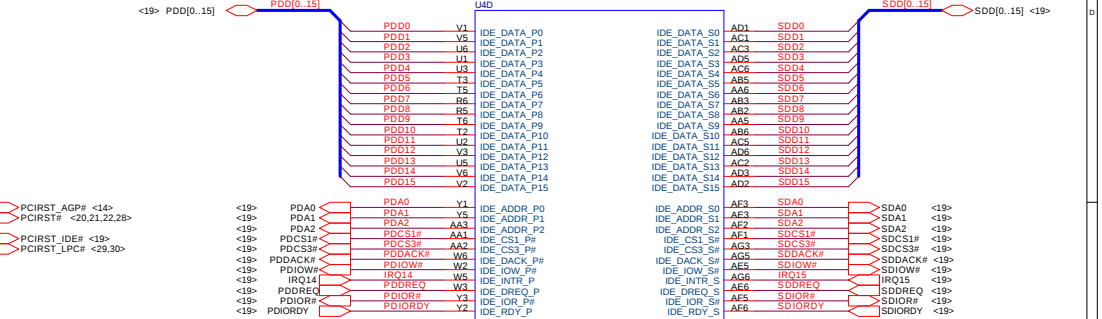
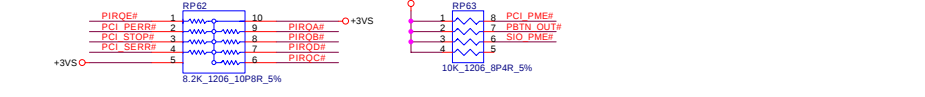
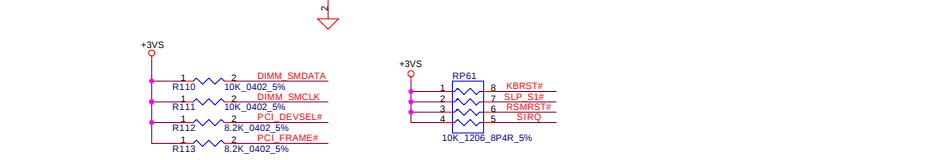
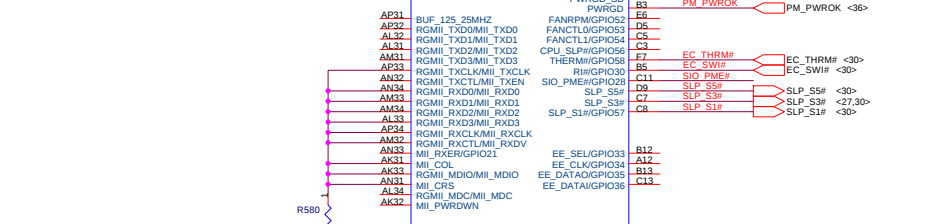
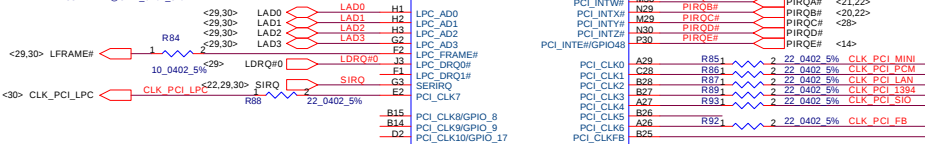
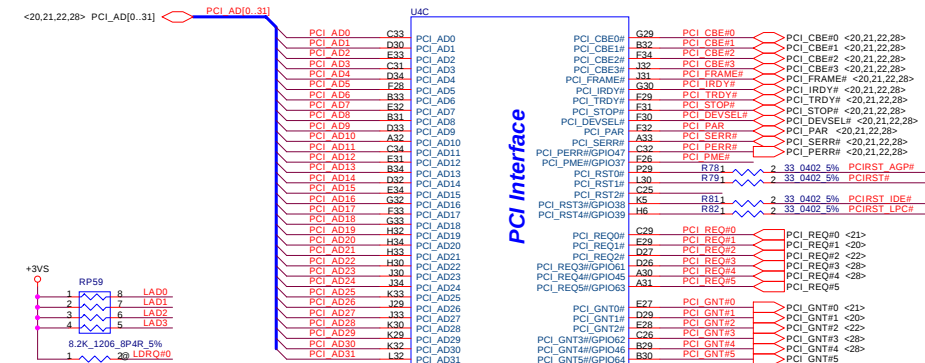
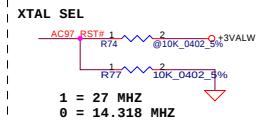


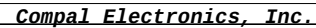
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Title		Compal Electronics, Inc.	
Document Number		DDR SODIMM Decoupling	
Size	Custom	LA-2392	Rev 0.1
Date:	Friday, April 16, 2004	Sheet 10	of 53



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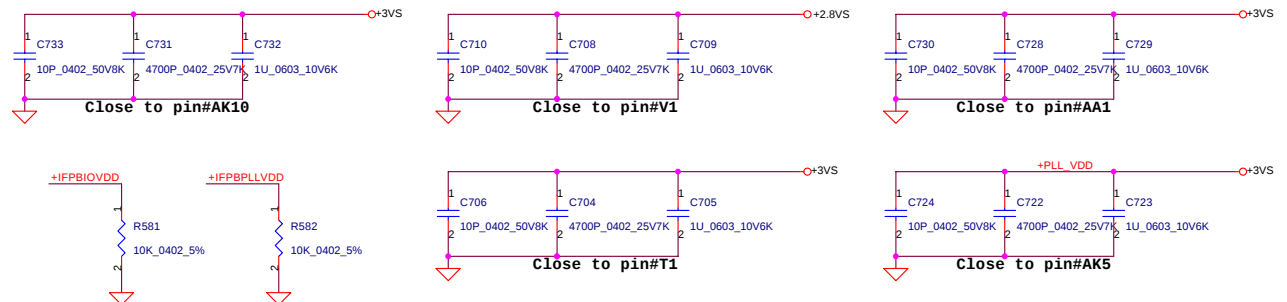
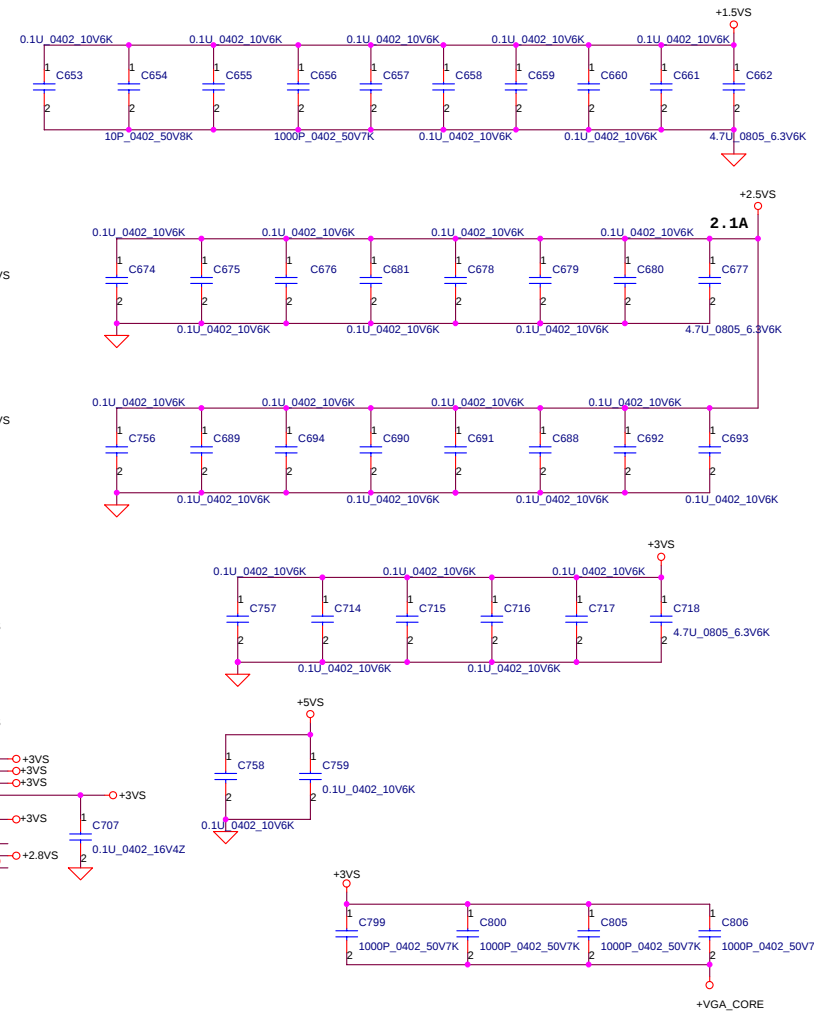
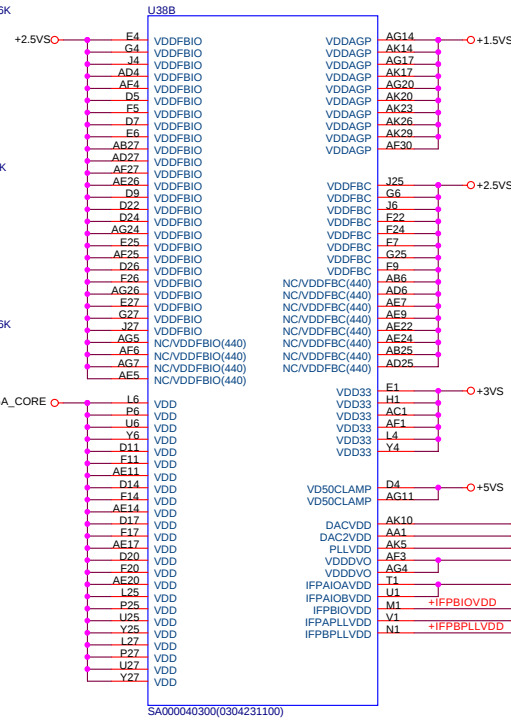
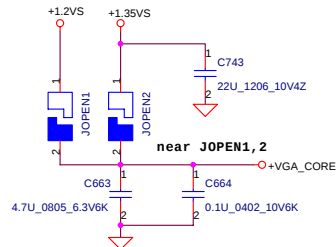
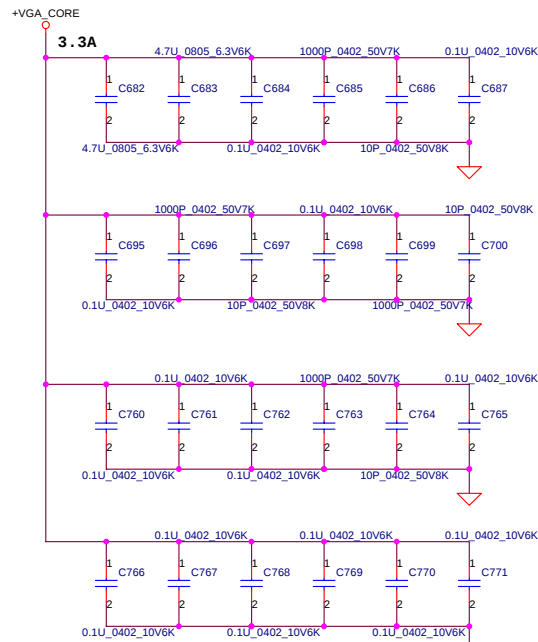
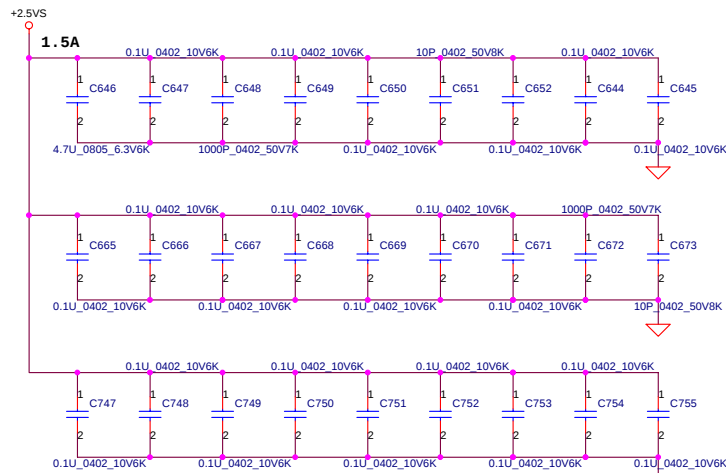
nVIDIA CrushK8 (Power & Ground)

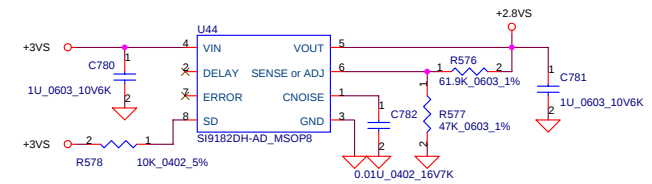
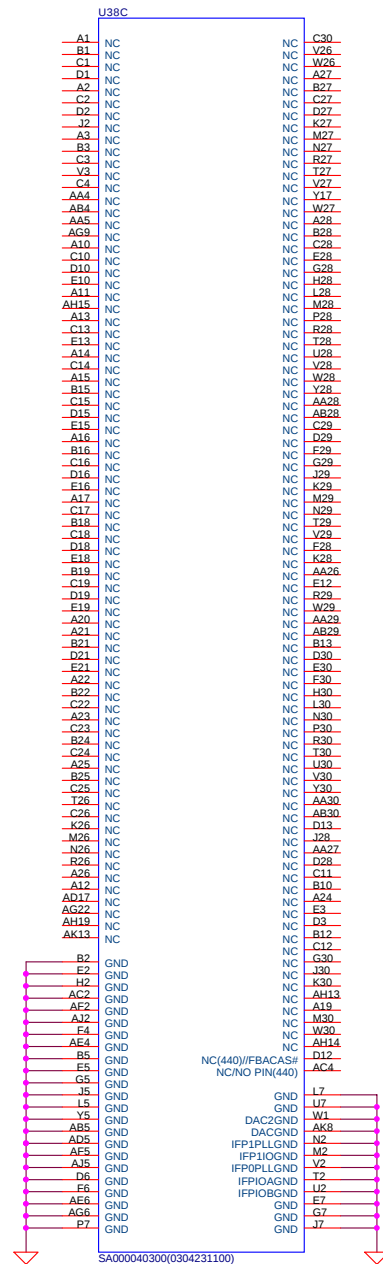
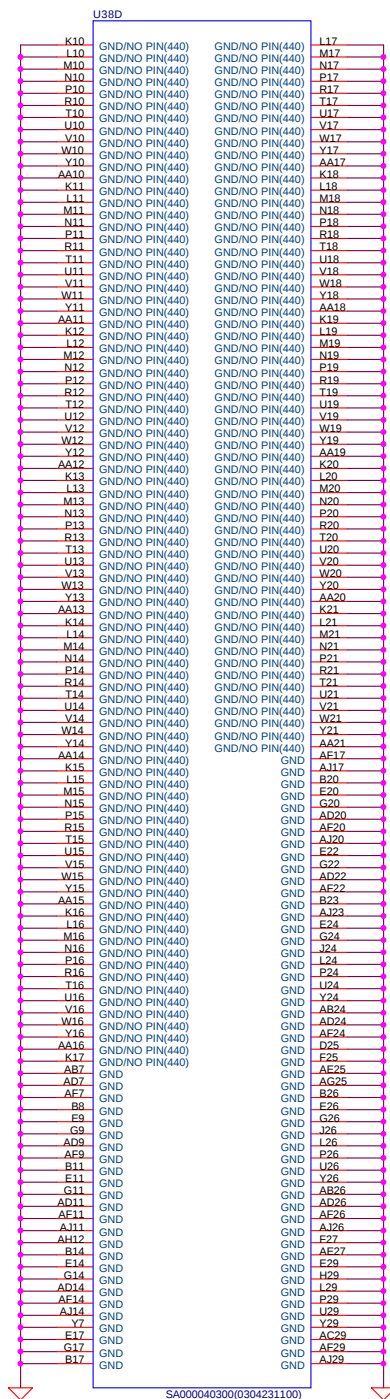
Size C	Document Number LA-2392	Rev 0.1
Date:	Friday, April 16, 2004	Sheet 13 of 53

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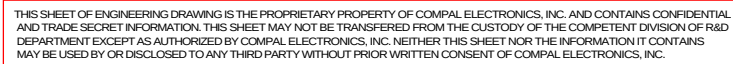
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	MAP17-116/232	MAP17-464
+VGA_CORE	* +1.2VS	+1.35VS

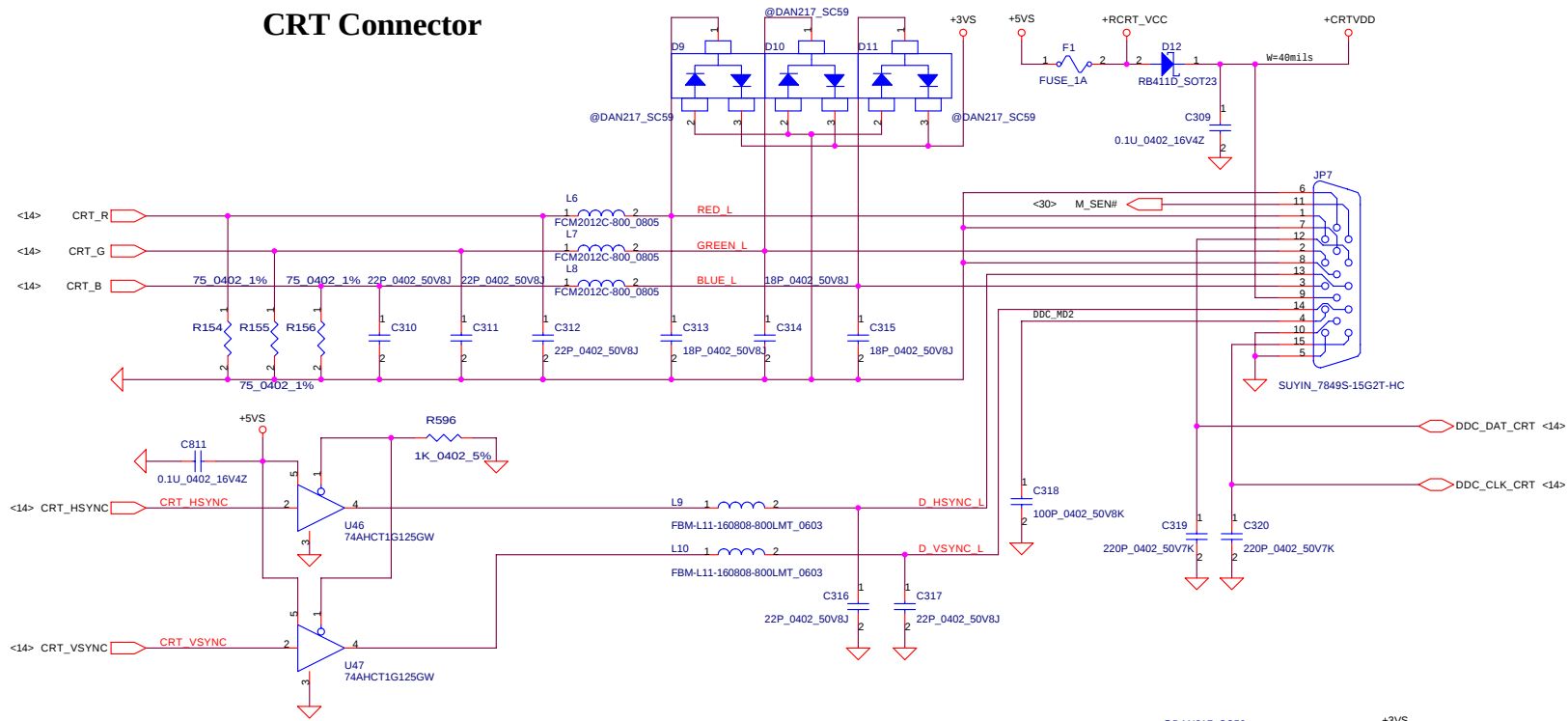




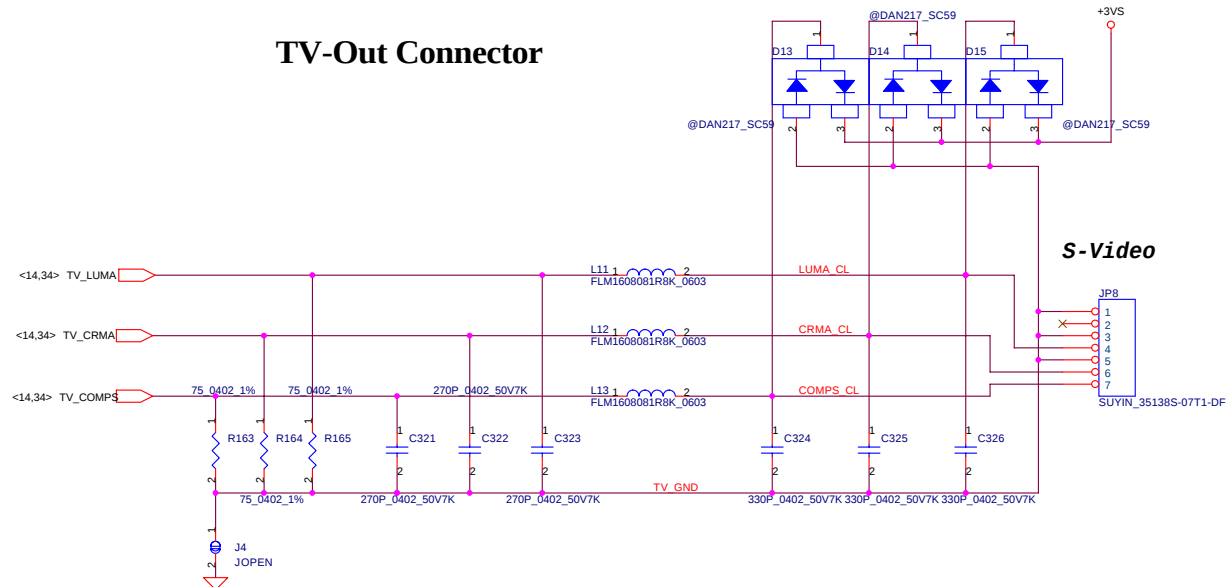
The cap.'s colselly to LCD CONN.



CRT Connector



TV-Out Connector

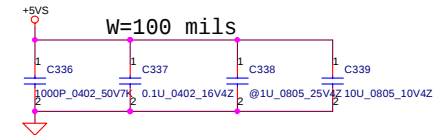


S-Video

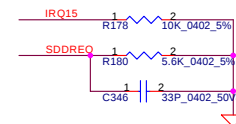
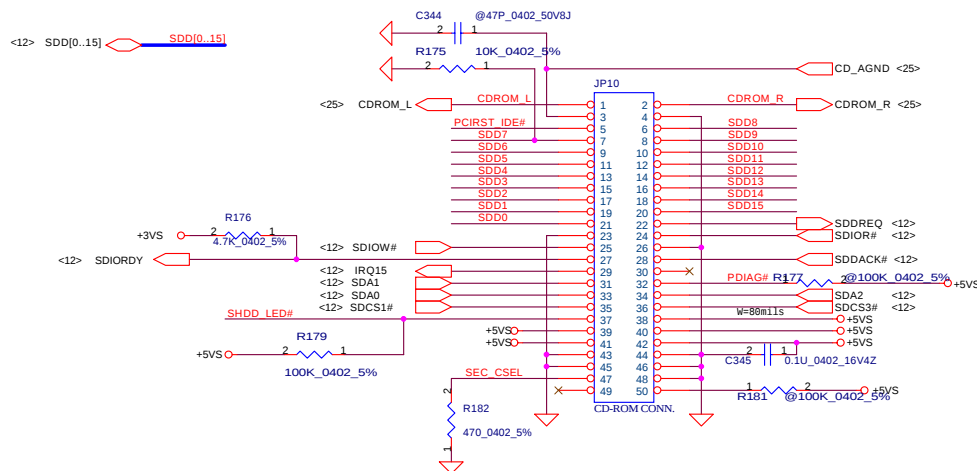
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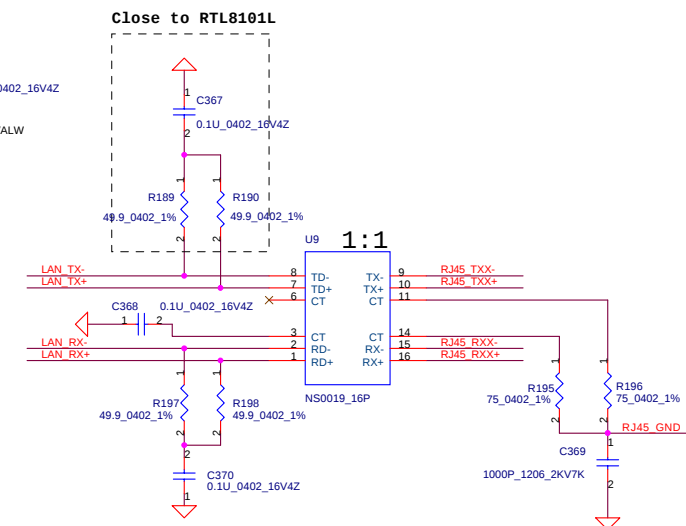
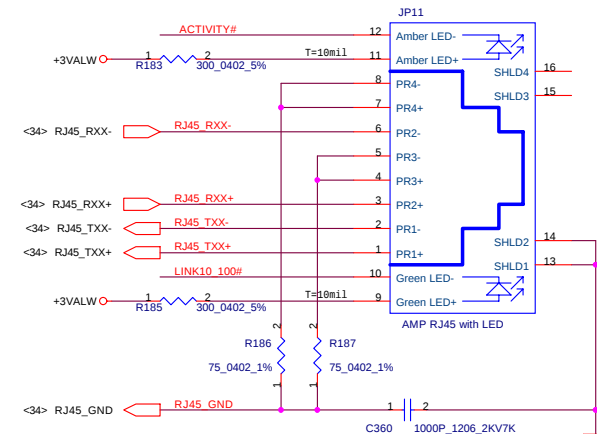
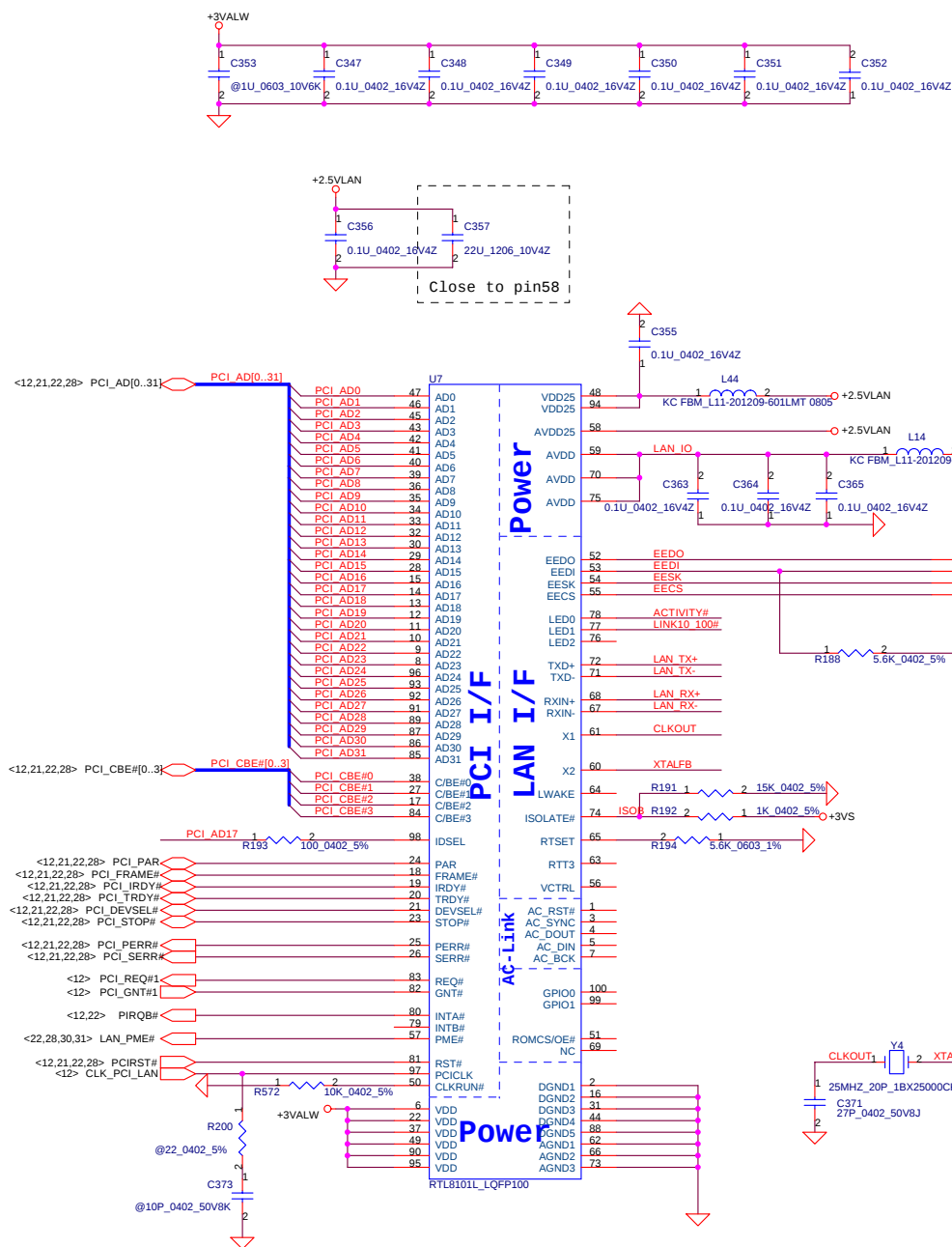
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Title			
CRT & TVout Connector			
Size	Document Number		Rev
	LA-2392		0.1
Date:	Friday, April 16, 2004		Sheet 18 of 53

Pin connection diagram for the SUYIN_Z00006FA044AS5032U component. The diagram shows connections for various pins, including PDD0[0..15], PCIRST_IDE#, PDDREQ, PDIOV#, PDIOIR#, PDDACK#, IRQ14, PDA1, PDA0, PDCS1#, and +5VS. It also shows connections to PDD8, PDD9, PDD10, PDD11, PDD12, PDD13, PDD14, PDD15, PDA2, and PDCS3#. The component is labeled SUYIN_Z00006FA044AS5032U.



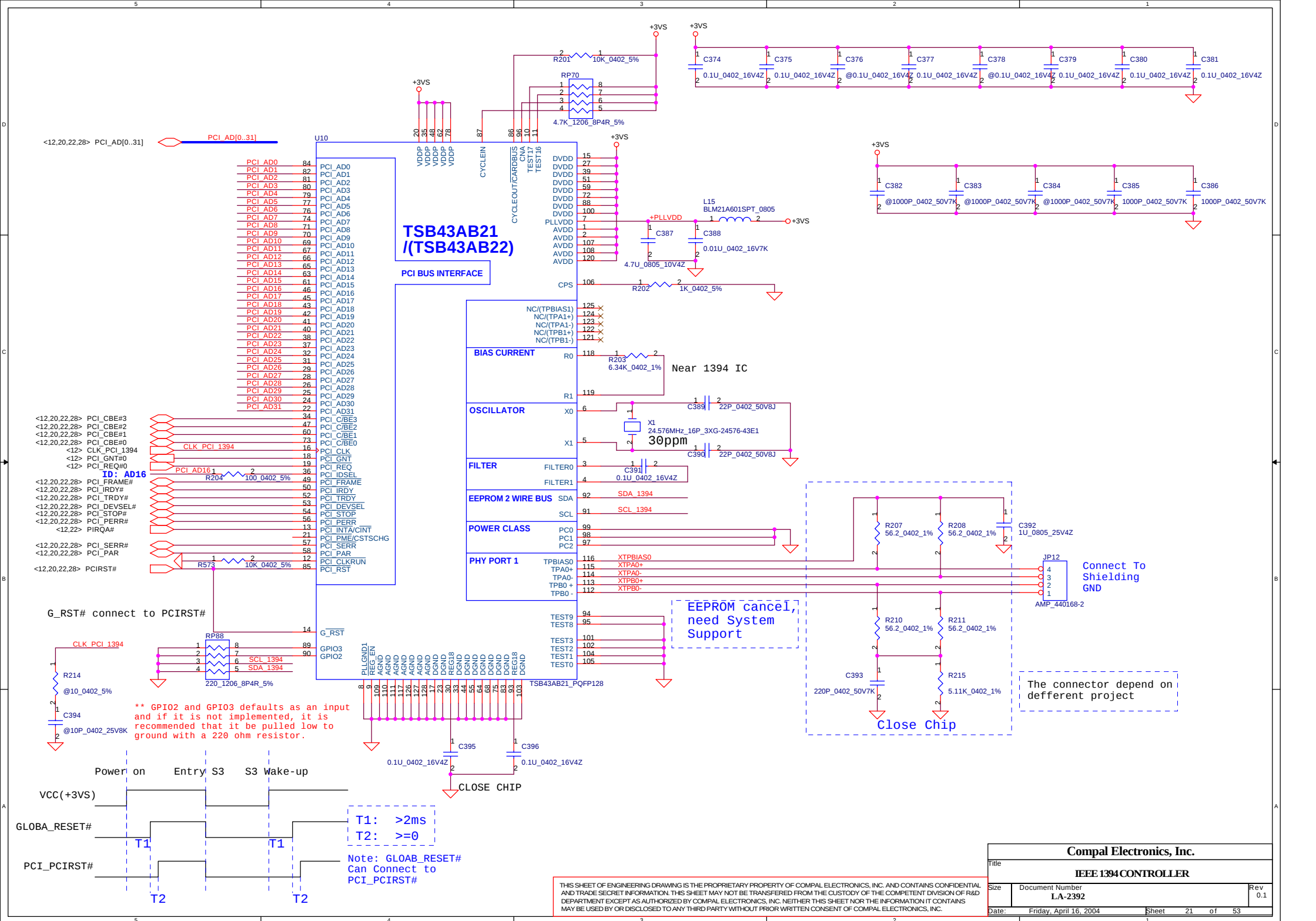
The schematic shows the ACT_LED# signal path. It is a pull-up circuit where the signal line is connected to +5V through a 100K resistor (R474). The signal is also connected to the output of a 1N4148 diode (D53) and the output of a 1N4148 diode (D54). The diodes are connected to PHDD_LED# and SHDD_LED# respectively. The output of the diodes is connected to the ACT_LED# signal, which is then connected to the ACT_LED# pin of the 3339 module.





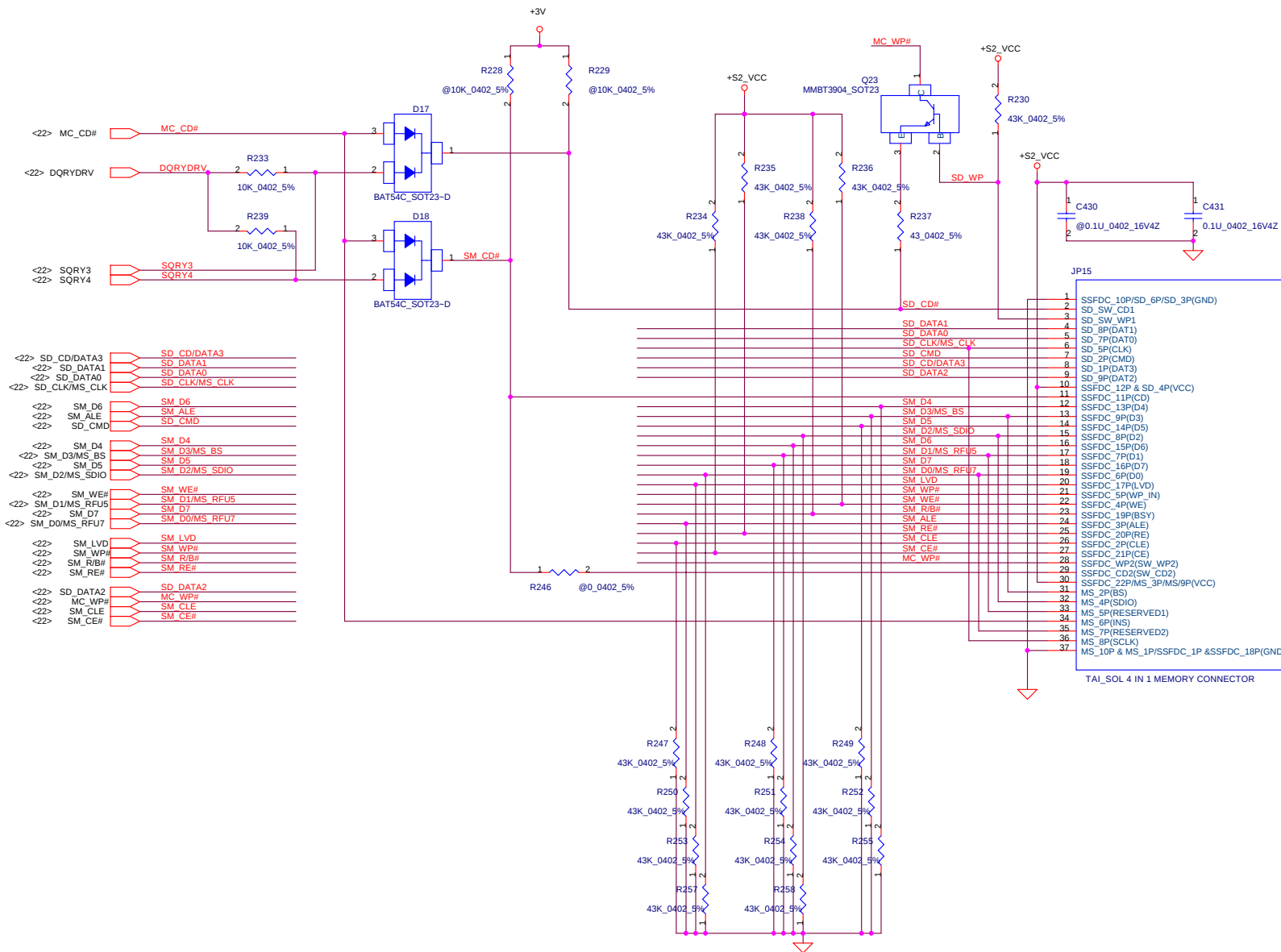
Layout Recommend :

1. LAN_RD+, LAN_RD- should be equal length as possible
2. LAN_TD+, LAN_TD- should be equal length as possible
3. The Maximum trace length between LAN chip(U22) and Magnetic(U24) is 12cm(4.7")
4. The distance between RJ45(Conn.) and Magnetic(U24) should be as short as possible

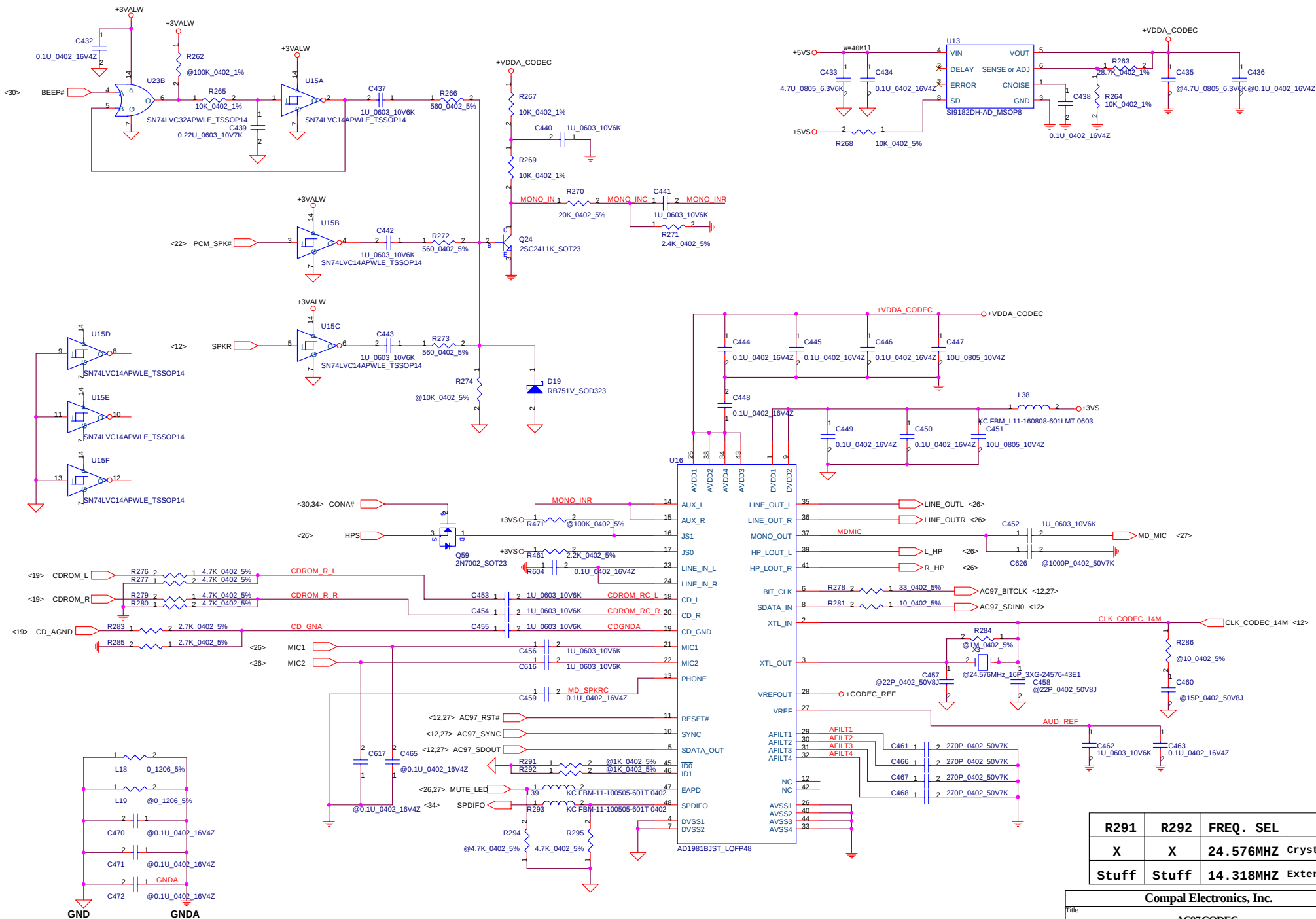


SOCKET

[illegible]



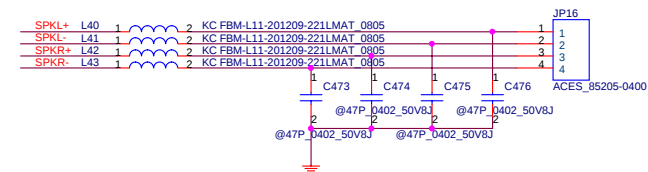
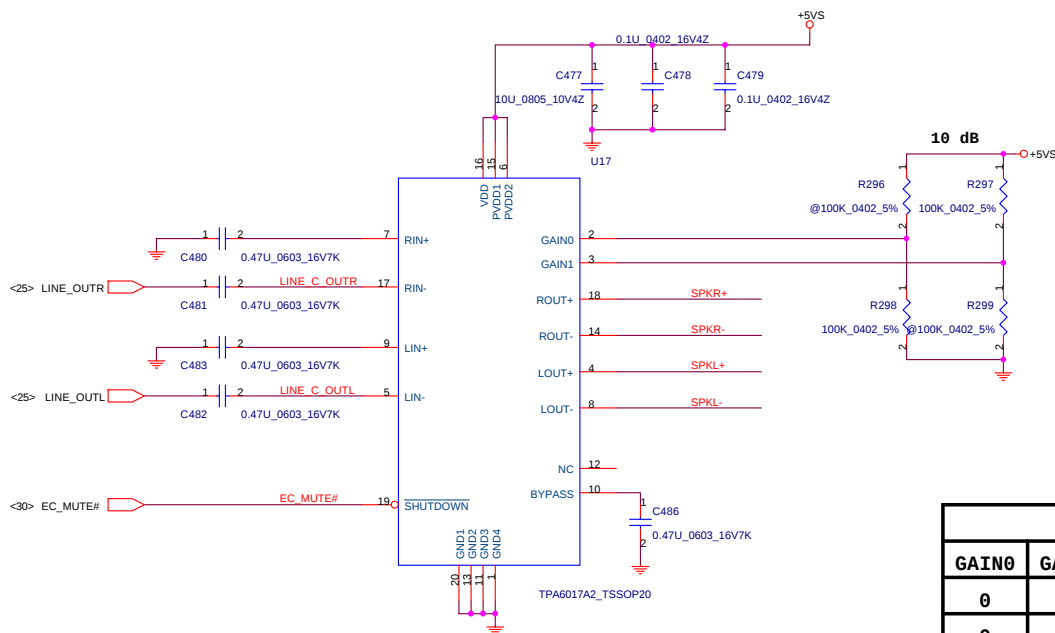
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R291	R292	FREQ. SEL
X	X	24.576MHZ Crystal
Stuff	Stuff	14.318MHZ External

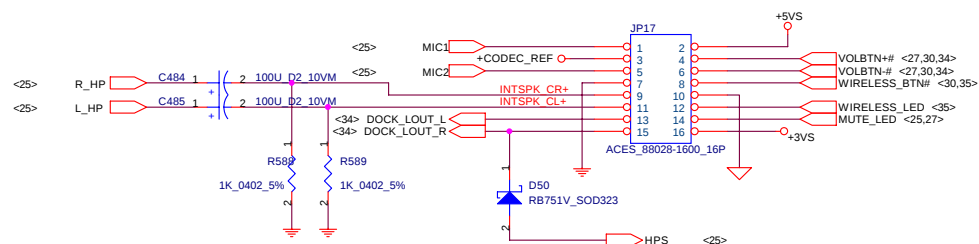
Compal Electronics, Inc.			
AC97 CODEC			
Title	Document Number	Rev	
	L/A-2392	0.1	
Date	Friday, April 16, 2004	Sheet	25 of 53

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Gain Settings		
GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

AUDIO CONNECTOR



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Compal Electronics, Inc.			
Title			
AMP & Audio Jack			
Size	Document Number	Rev	
Custom	L/A-2392	0.1	
Date	Friday, April 16, 2004	Sheet	26 of 53

[illegible]

JP21

Signal	Pin
<26,30,34> VOLBTN+ [#]	1
<30,33> BATLED_0#	2
<26,30,34> VOLBTN- [#]	3
	4
	5
<33> ACT_LED	6
+5VALW	7
+3VS	8
<25,26> MUTE_LED	9
	10
	11
<35> PAV_LEDVCC	12
<30,33> PMLED_1#	13
+5VS	14

ACES_85201-1405

Diagram illustrating the pin connections for the ACES_85201-0805 module. The connections are as follows:

- Pin 1: PMLED_1
- Pin 2: BATLED_0
- Pin 3: ACT_LED
- Pin 4: PRES_LEDVCC+5V
- Pin 5: (Not connected)
- Pin 6: (Not connected)

The module is identified as ACES_85201-0805.

Diagram illustrating the pin connections for the ACES 87152-0807 module:

- Pin 8: +5V
- Pin 7: TP_DATA
- Pin 6: TP_CLK
- Pin 5: X (unconnected)
- Pin 4: Ground
- Pin 3: Ground
- Pin 2: Ground
- Pin 1: Ground

Module Label: ACES 87152-0807

The diagram illustrates the connection of a Bluetooth module (Q60, Si2301DS_SOT23) to the ACES board (ACES_85201-0805) via a JP23 connector. The module's pins are connected as follows:

- Pin 1 (GND):** Connected to the ACES board's GND.
- Pin 2 (VCC):** Connected to the ACES board's +3V.
- Pin 3 (SDA):** Connected to the ACES board's SDA.
- Pin 4 (SCL):** Connected to the ACES board's SCL.
- Pin 5 (RST):** Connected to the ACES board's RST.
- Pin 6 (TX):** Connected to the ACES board's TX.
- Pin 7 (RX):** Connected to the ACES board's RX.
- Pin 8 (LED):** Connected to the ACES board's LED.
- Pin 9 (AD22):** Connected to the ACES board's AD22.
- Pin 10 (PME#):** Connected to the ACES board's PME#.
- Pin 11 (ON#):** Connected to the ACES board's ON#.

The module is also connected to a +3V BT supply and a 1U_0603_10V6K capacitor (C624) for power regulation. The ACES board is labeled ACES_85201-0805.

C

[illegible]

USB CONNECTOR 2

W=40mils

+USB_VCCB

C502 150U_D2_6.3VM

C504

C505 @1000P_0402_50V7K

@0.1U_0402_16V4Z

JP22

1

2

3

4

SUYIN_2569A-04G3T

USBP1- <12>

USBP1+ <12>

USB CONNECTOR 3

W=40mils

+USB_VCCB

C507 150U_D2_6.3VM

C508 0.1U_0402_16V4Z

C509 0.1U_0402_16V4Z

@1000P_0402_50V7K

JP27

1

2

3

4

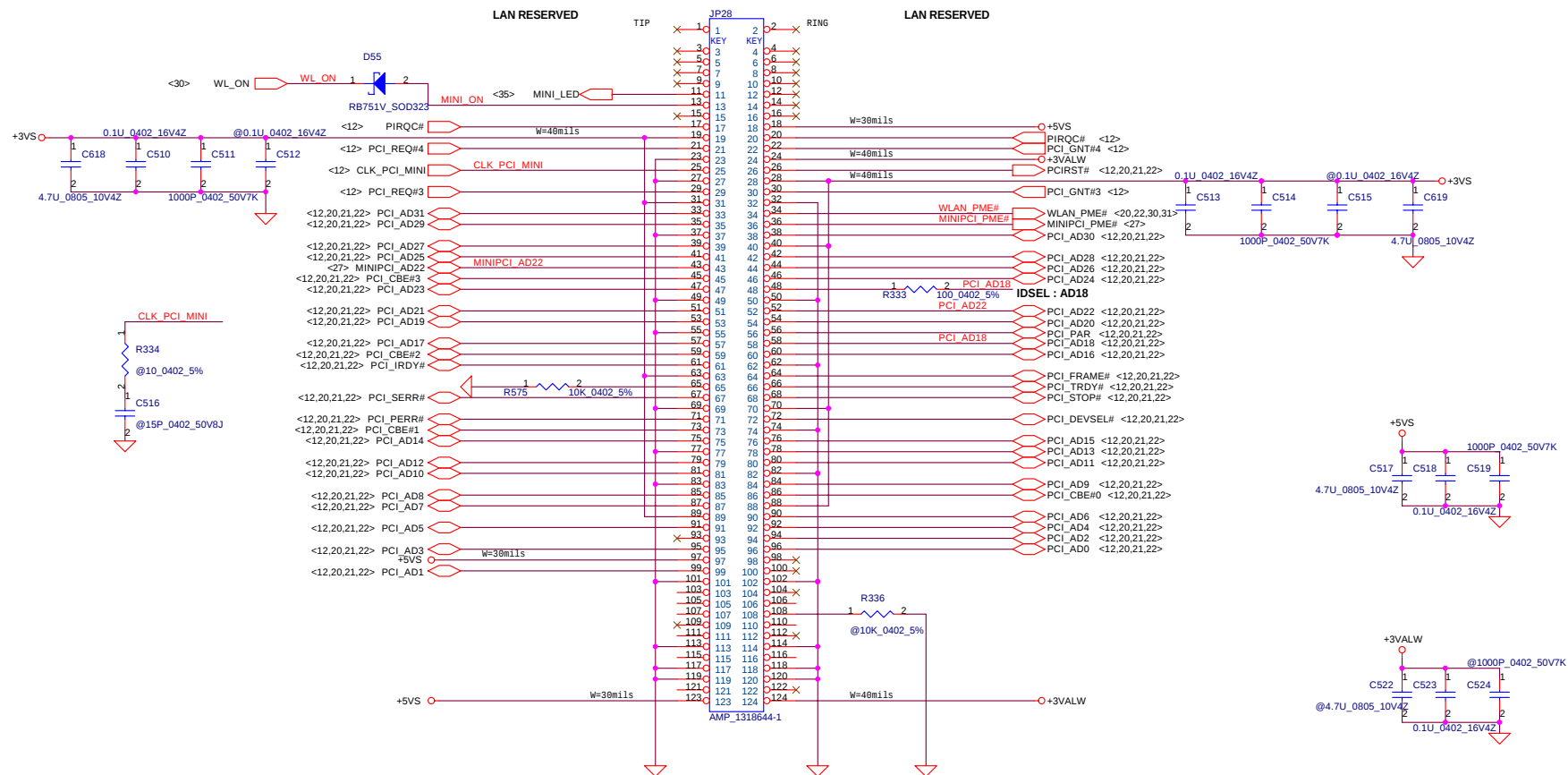
SUYIN_2569A-04G3T

<12> USBP0- USBP0-

<12> USBP0+ USBP0+

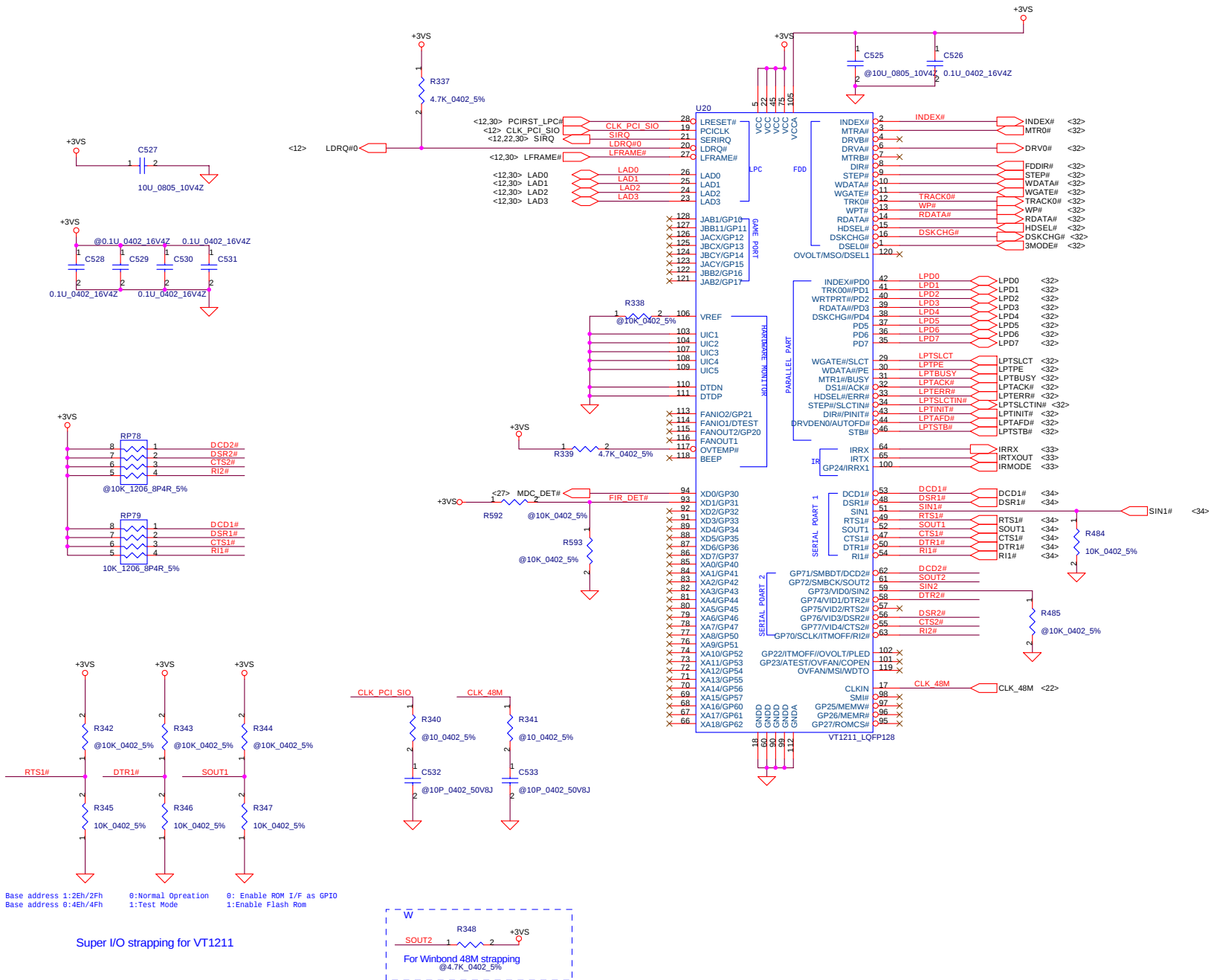
Compal Electronics, Inc.			
Title			
MDC , Bluetooth & USB CONN.			
Size	Document Number		Rev
	LA-2392		0.1
Date:	Friday, April 16, 2004	Sheet	27 of 53

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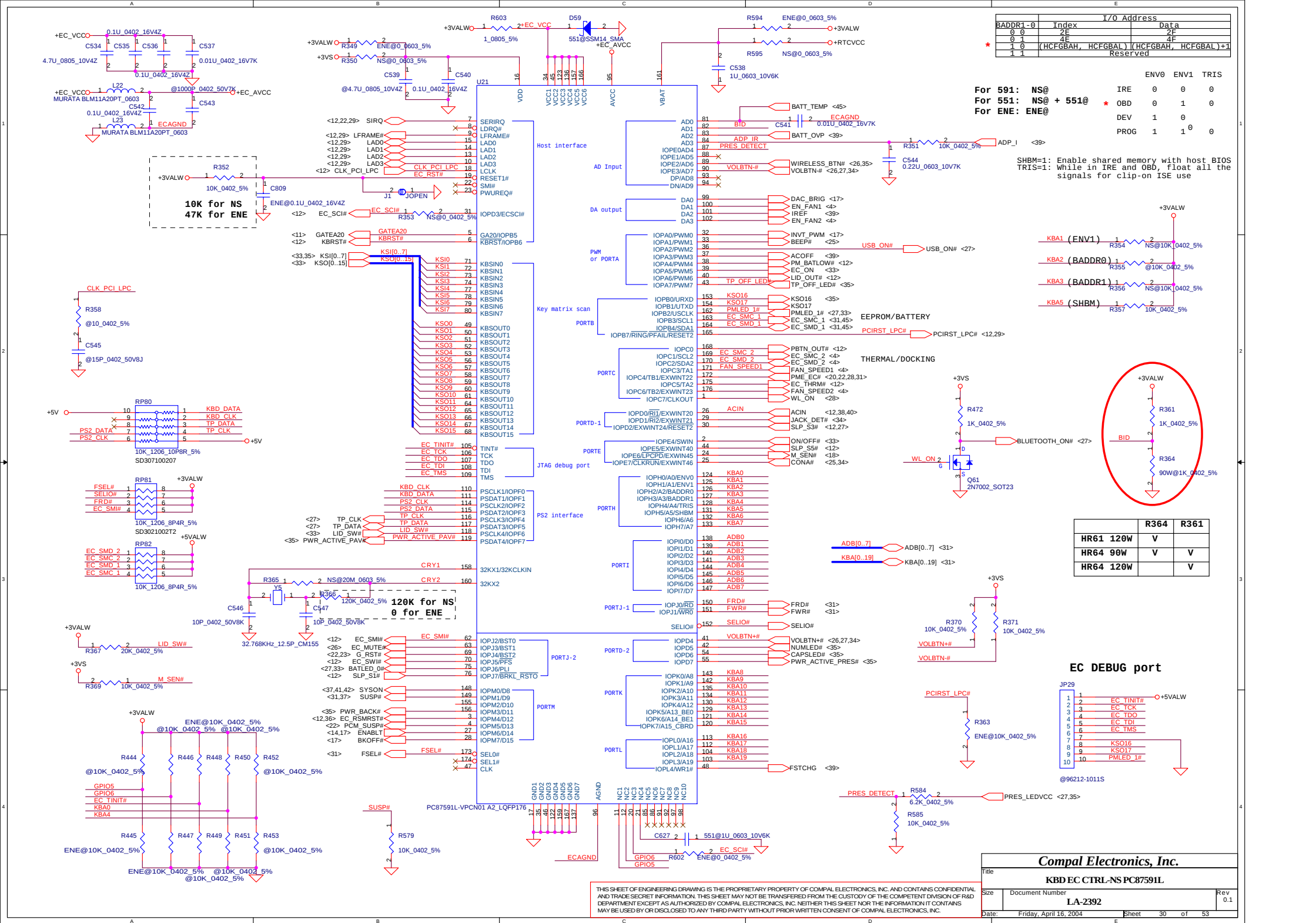
Compal Electronics, Inc.			
Title			
Mini PCI Slot			
Size	Document Number	Rev	
	L.A-2392	0.1	
Date:	Friday, April 16, 2004	Sheet	28 of 53



Super I/O strapping for VT1211

For Winbond 48M strapping
@4.7K_0402_5%

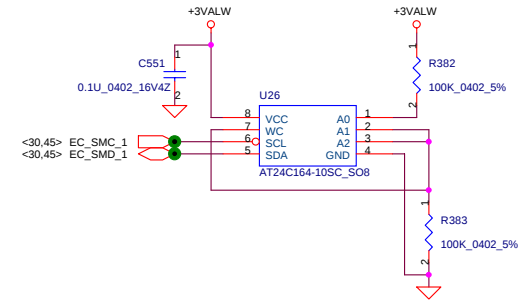
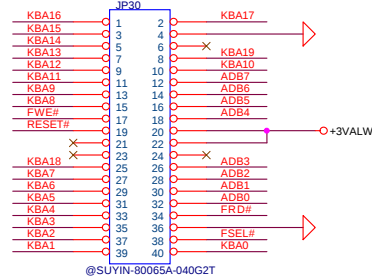
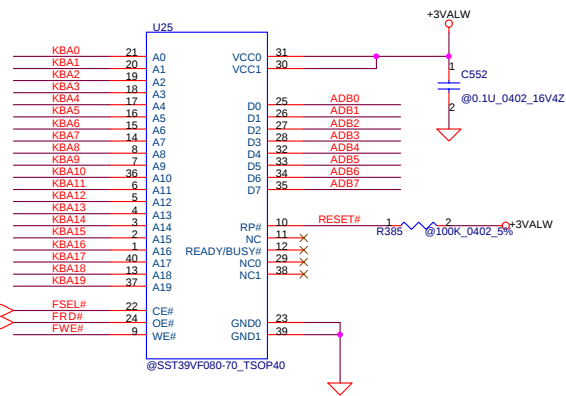
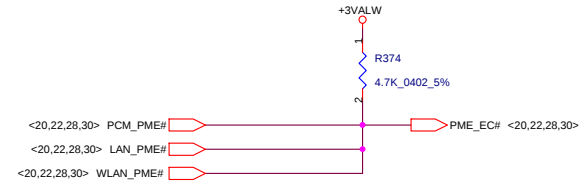
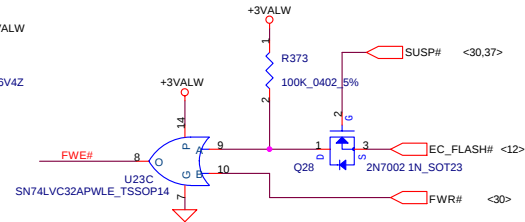
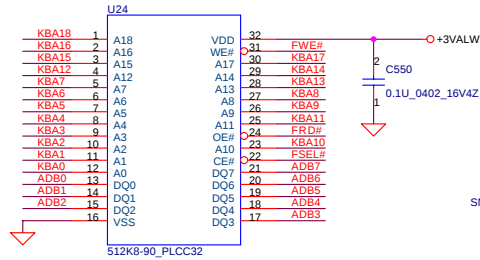
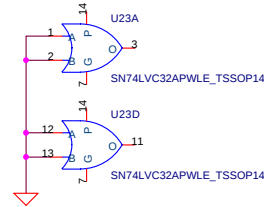
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INPUT

OUTPUT

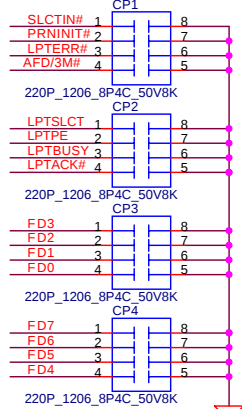
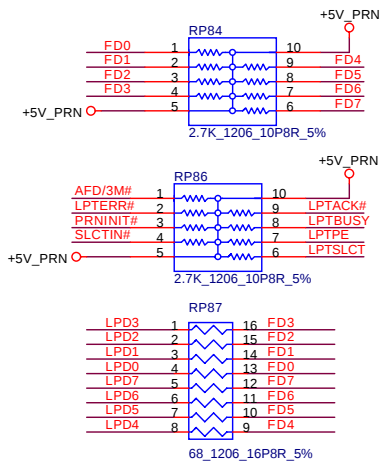
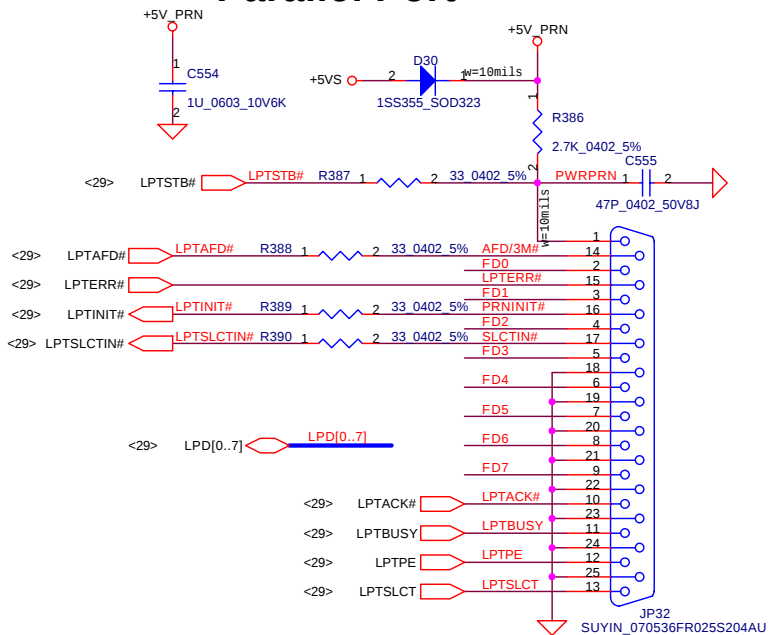
<30> ADB[0..7] ADB[0..7]
<30> KBA[0..19] KBA[0..19]



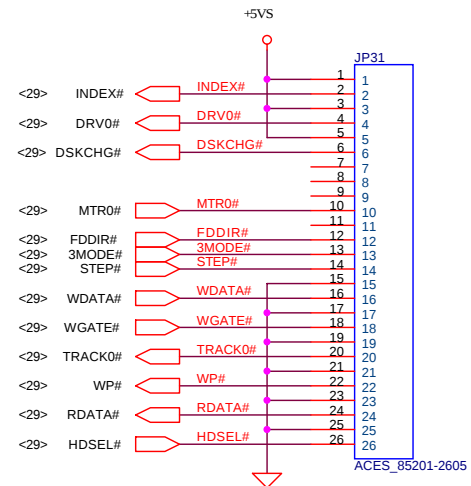
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Title		BIOS & EC I/O Port	
Size	Document Number	LA-2392	
Date:	Friday, April 16, 2004	Sheet	31 of 53
		Rev 0.1	

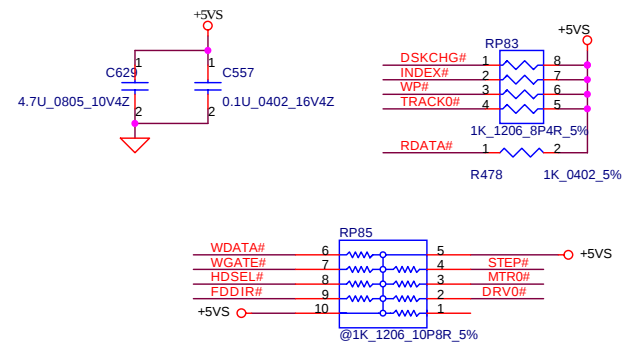
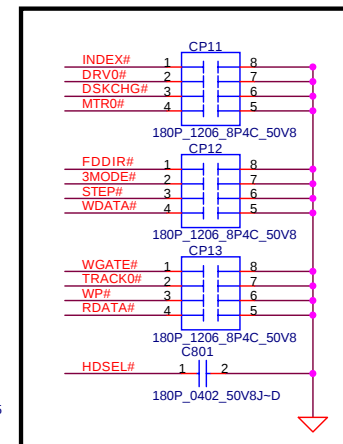
Parallel Port



FDD CONN.



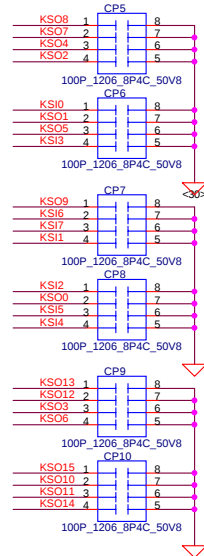
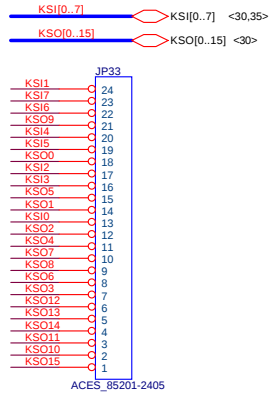
EMI Requirement



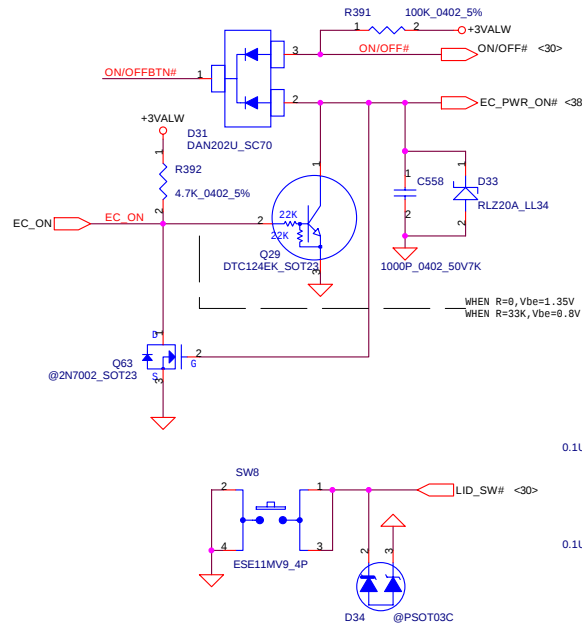
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Title			
Parallel port & FDD Connector			
Size B	Document Number LA-2392		Rev 0.1
Date:	Friday, April 16, 2004	Sheet	32 of 53

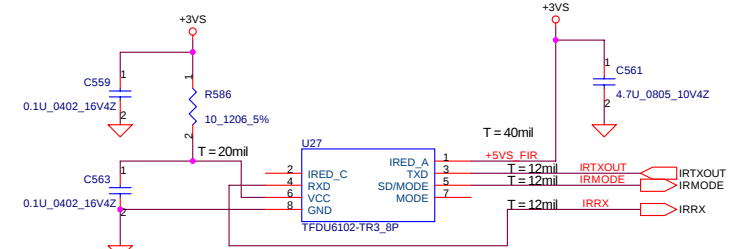
INT_KBD CONN.



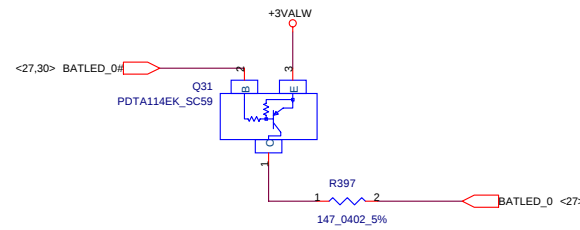
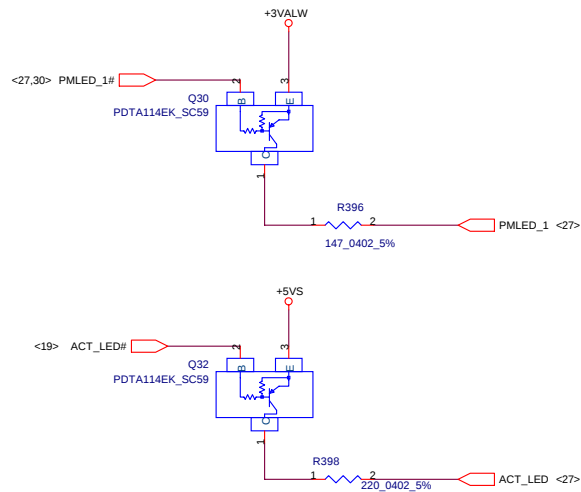
Power BTN



FIR Module

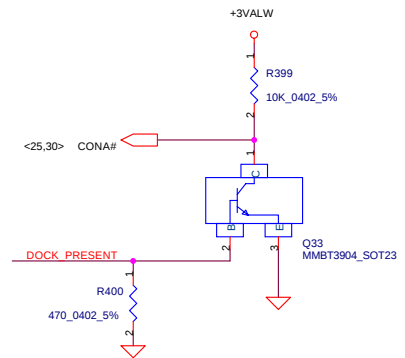
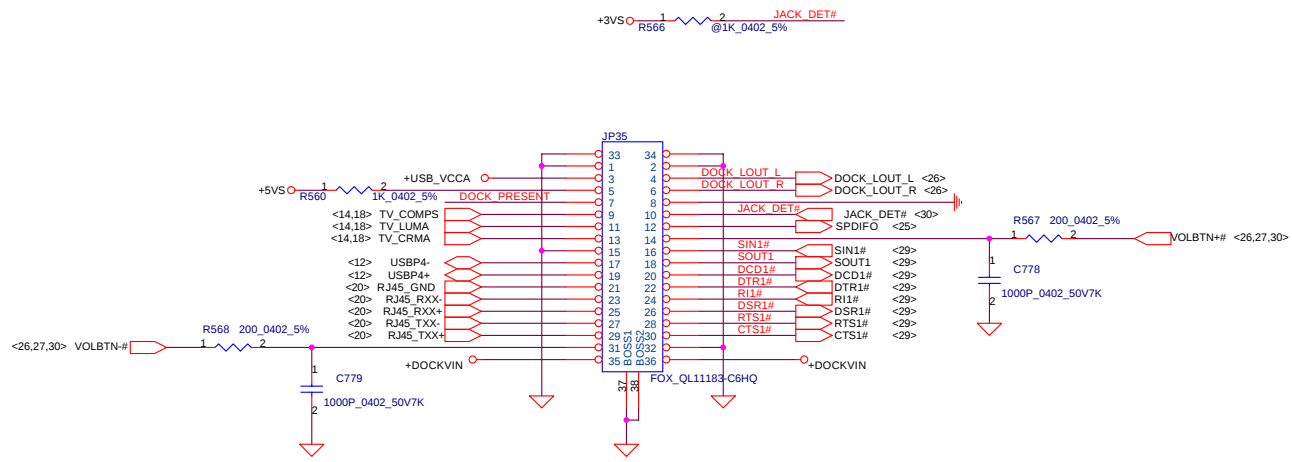


Touch Pad & Status LED Conn.

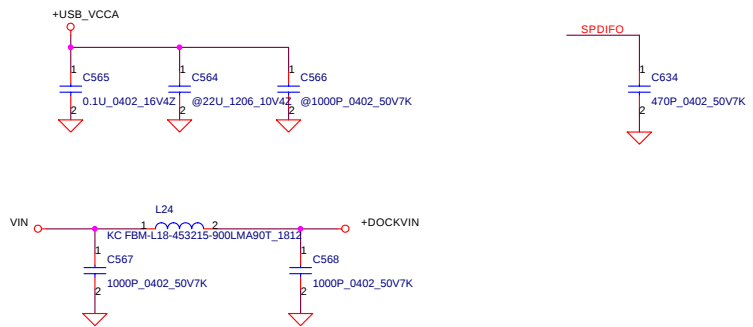
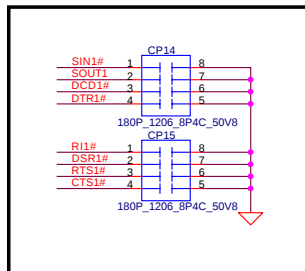


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Title			
KBD,ON/OFF,T/P,LED & FIR			
Size	Document Number	Rev	
	LA-2392	0.1	
Date:	Friday, April 16, 2004	Sheet	33 of 53

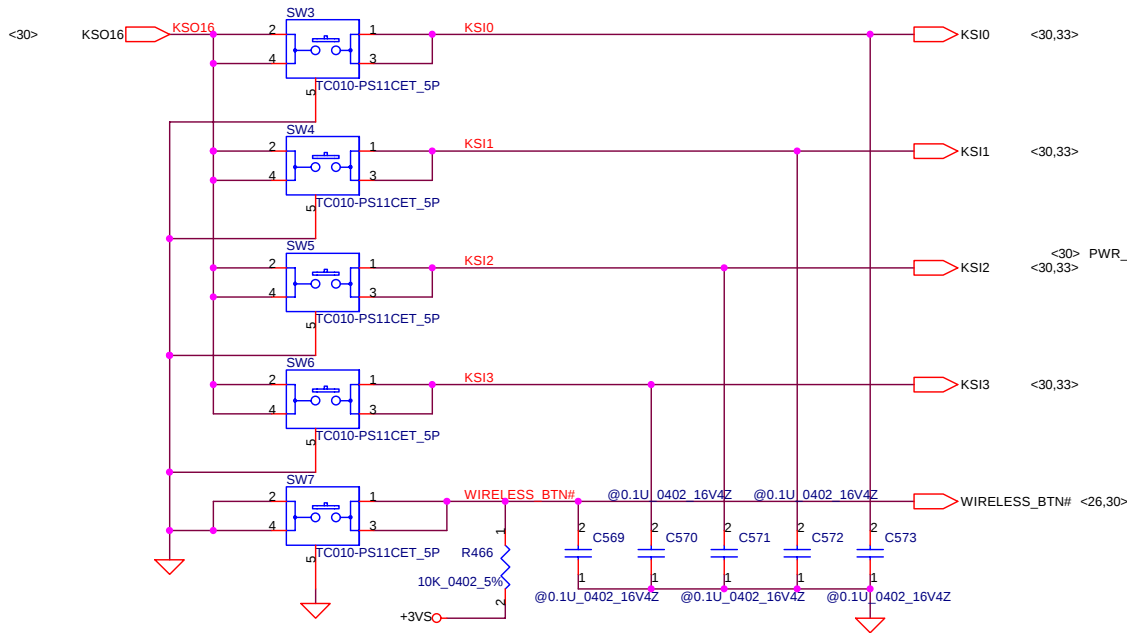


EMI Requirement

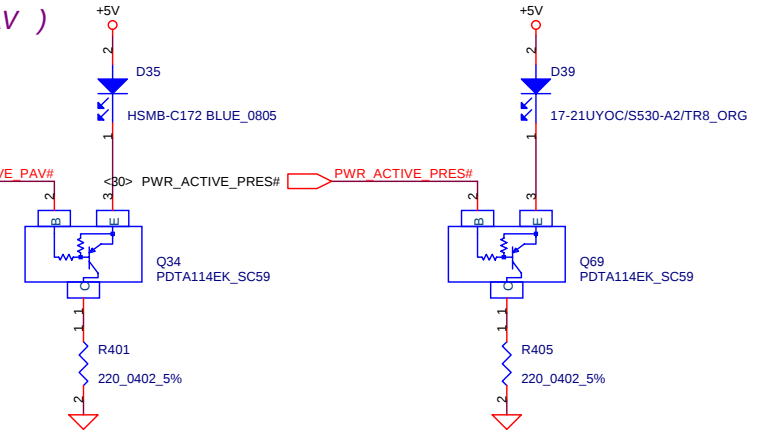


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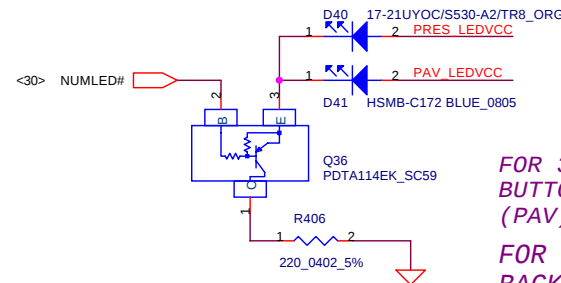
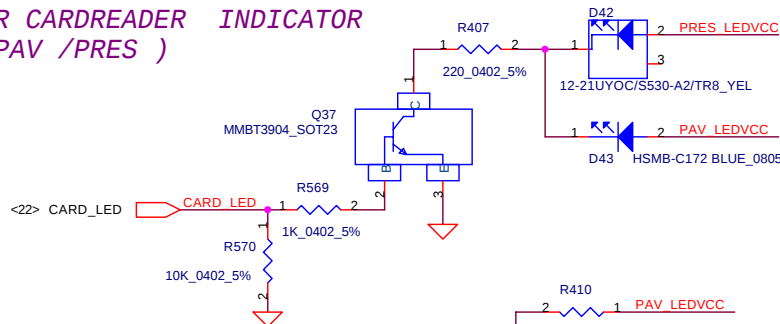
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Title			
SPR Connector			
Size	Document Number	Rev	
	LA-2392	0.1	
Date:	Friday, April 16, 2004	Sheet	34 of 53



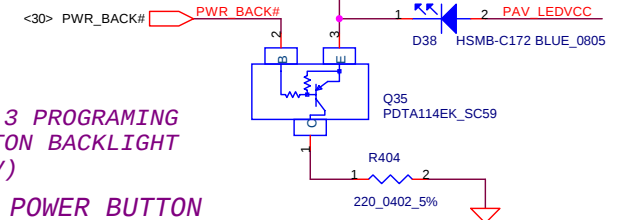
FOR POWER BUTTON
BACKLIGHT (PAV)



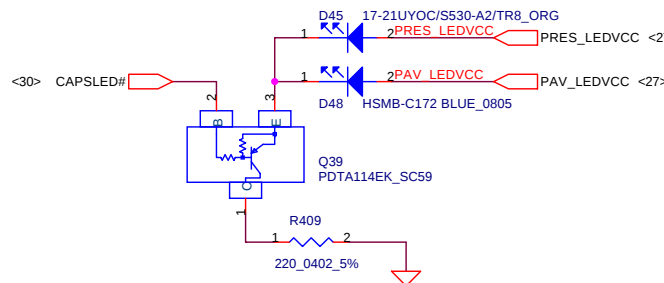
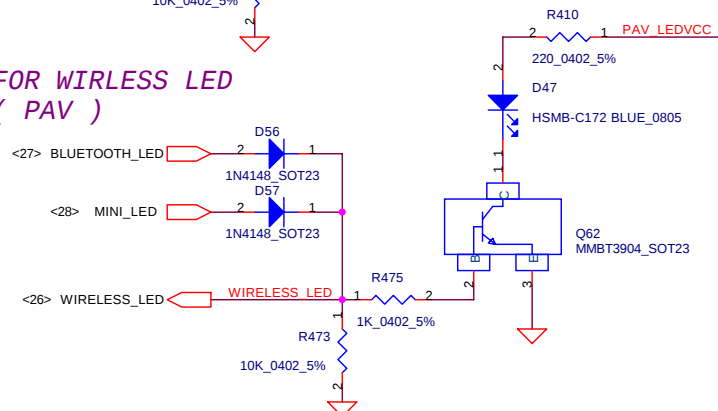
FOR CARDREADER INDICATOR
(PAV /PRES)



FOR 3 PROGRAMING
BUTTON BACKLIGHT
(PAV)
FOR POWER BUTTON
BACKLIGHT (PRES)

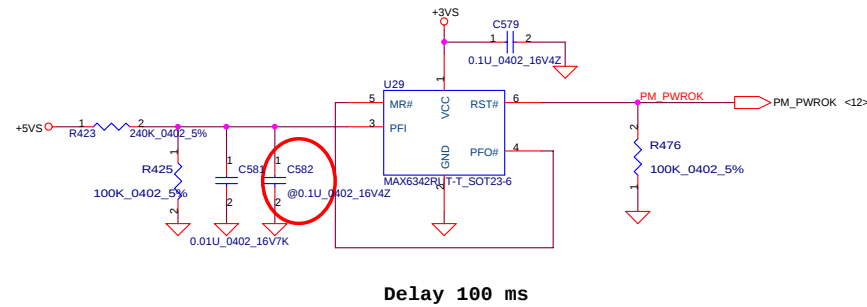
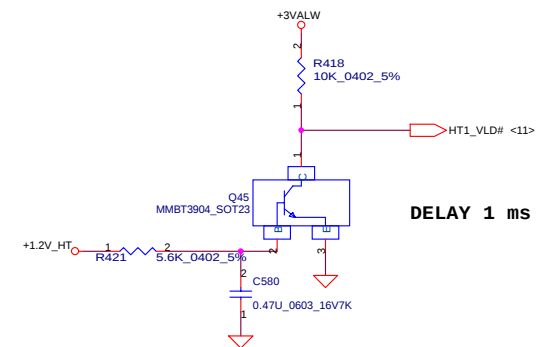
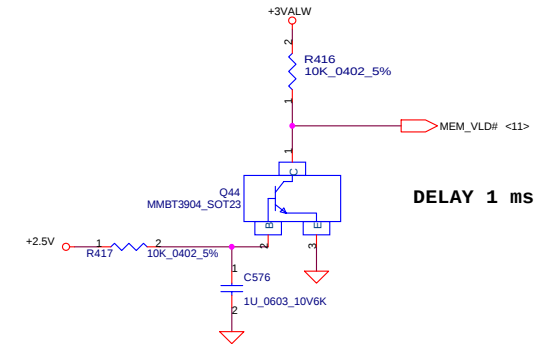
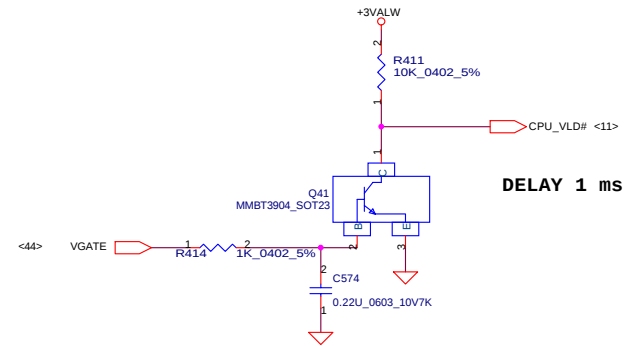
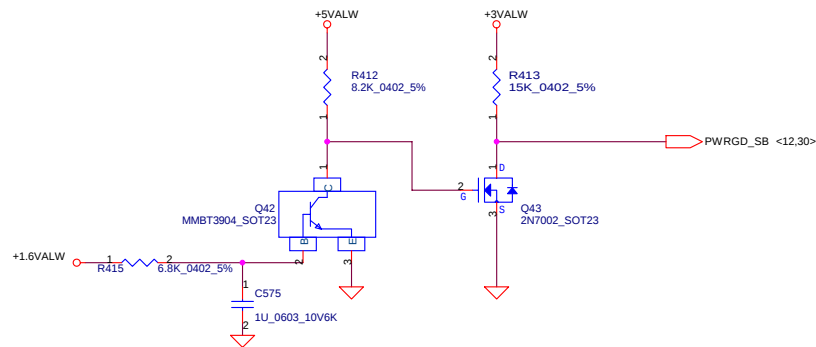


FOR WIRLESS LED
(PAV)



Title LED & Fan Circuit		
Size B	Document Number LA-2392	Rev 0.1
Date Friday, April 16, 2004	Sheet 35	of 53

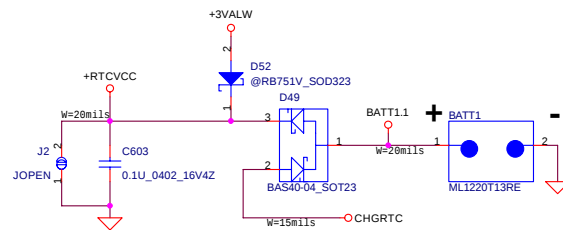
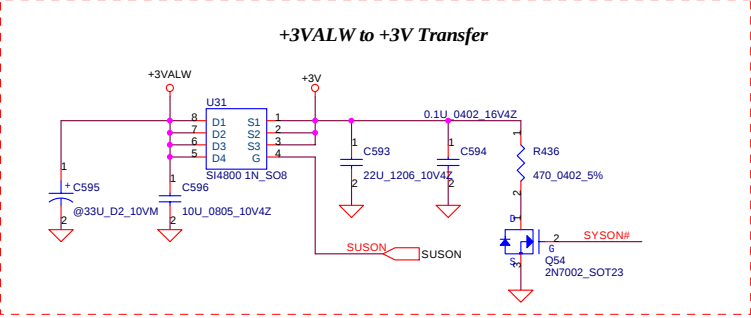
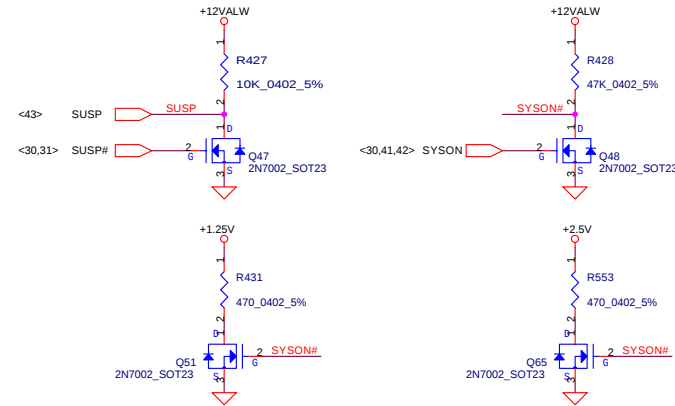
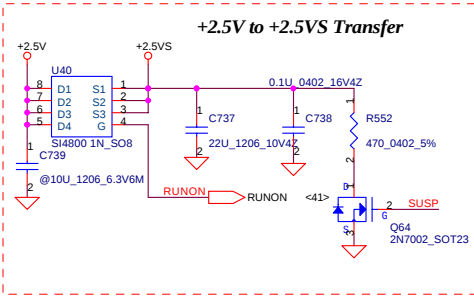
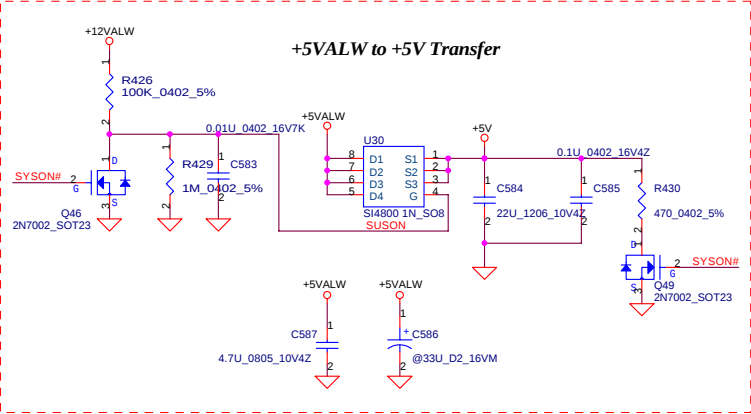
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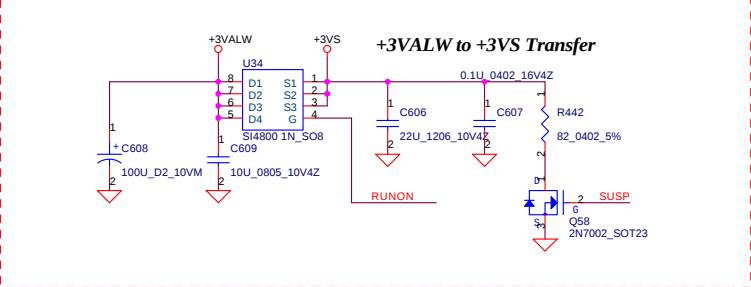
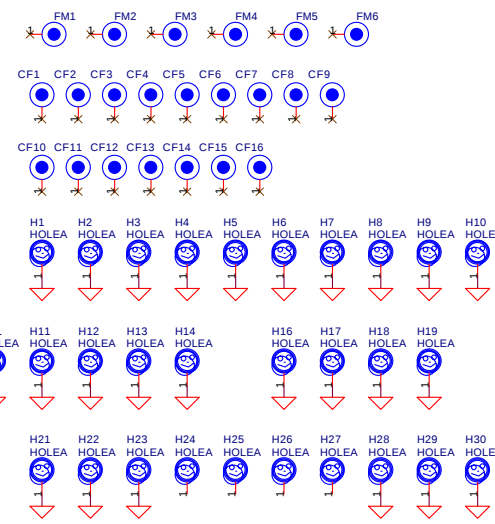
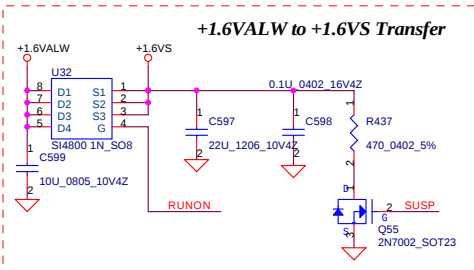
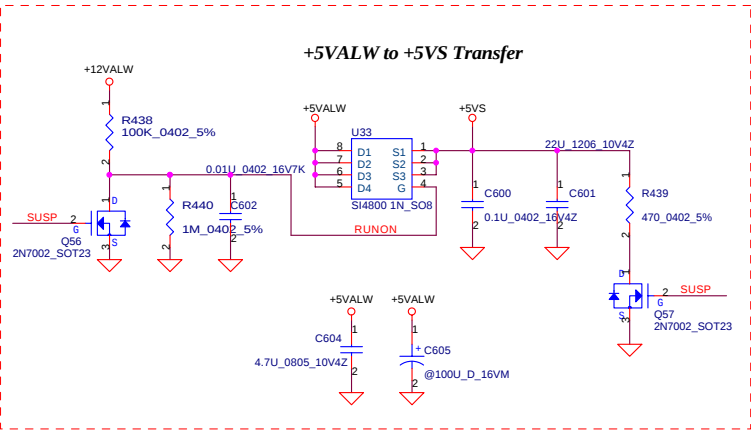
Delay 100 ms

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Compal Electronics, Inc.			
Title	Power OK/Reset Conn.& MUTE Switch		
Size	Document Number	Rev	
Customer	LA-2392	0.1	
Date:	Friday, April 16, 2004	Sheet	36 of 53

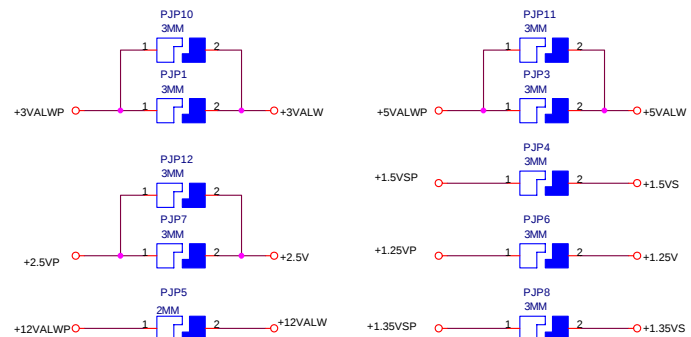
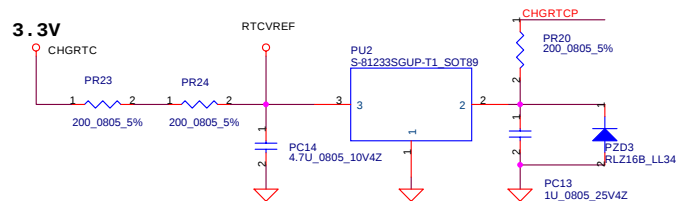
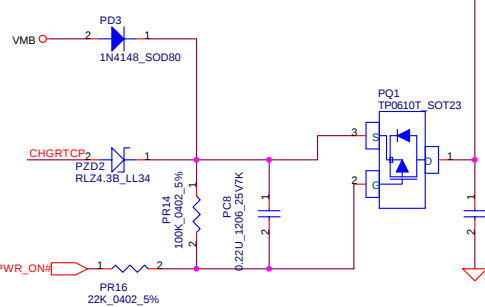
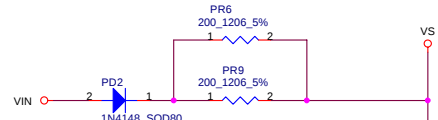
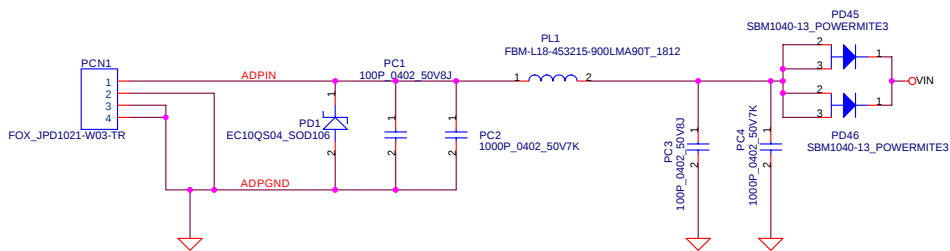


For customer request
they don't wanna
charge RTC

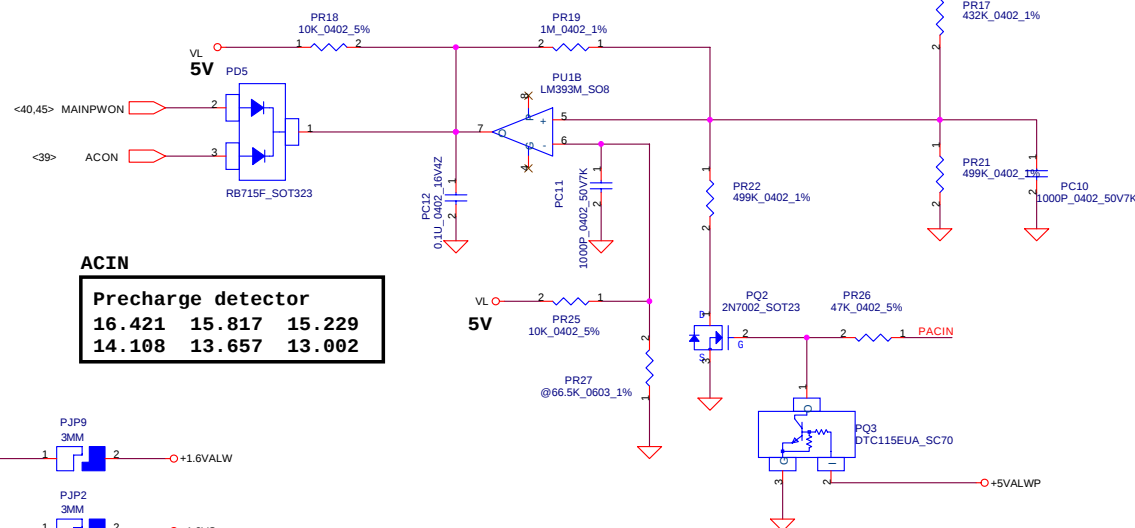
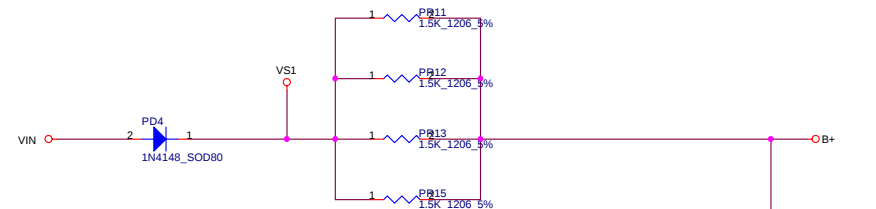
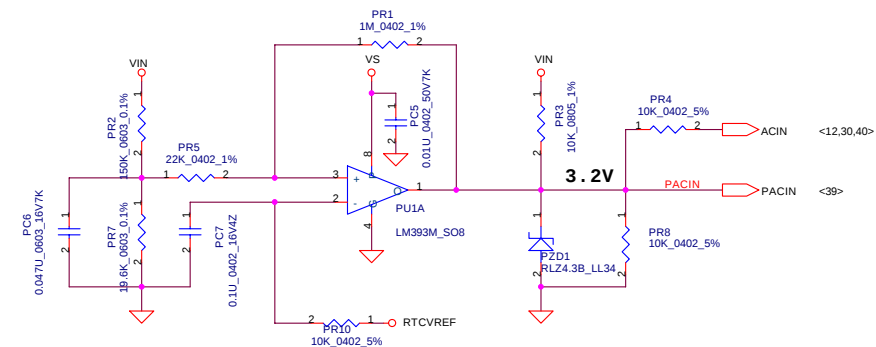


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Compal Electronics, Inc.		
File	DC/DC Circuit	
Size	Document Number	Rev
Custom	LA-2392	0.1
Date:	Friday, April 16, 2004	Sheet 37 of 53



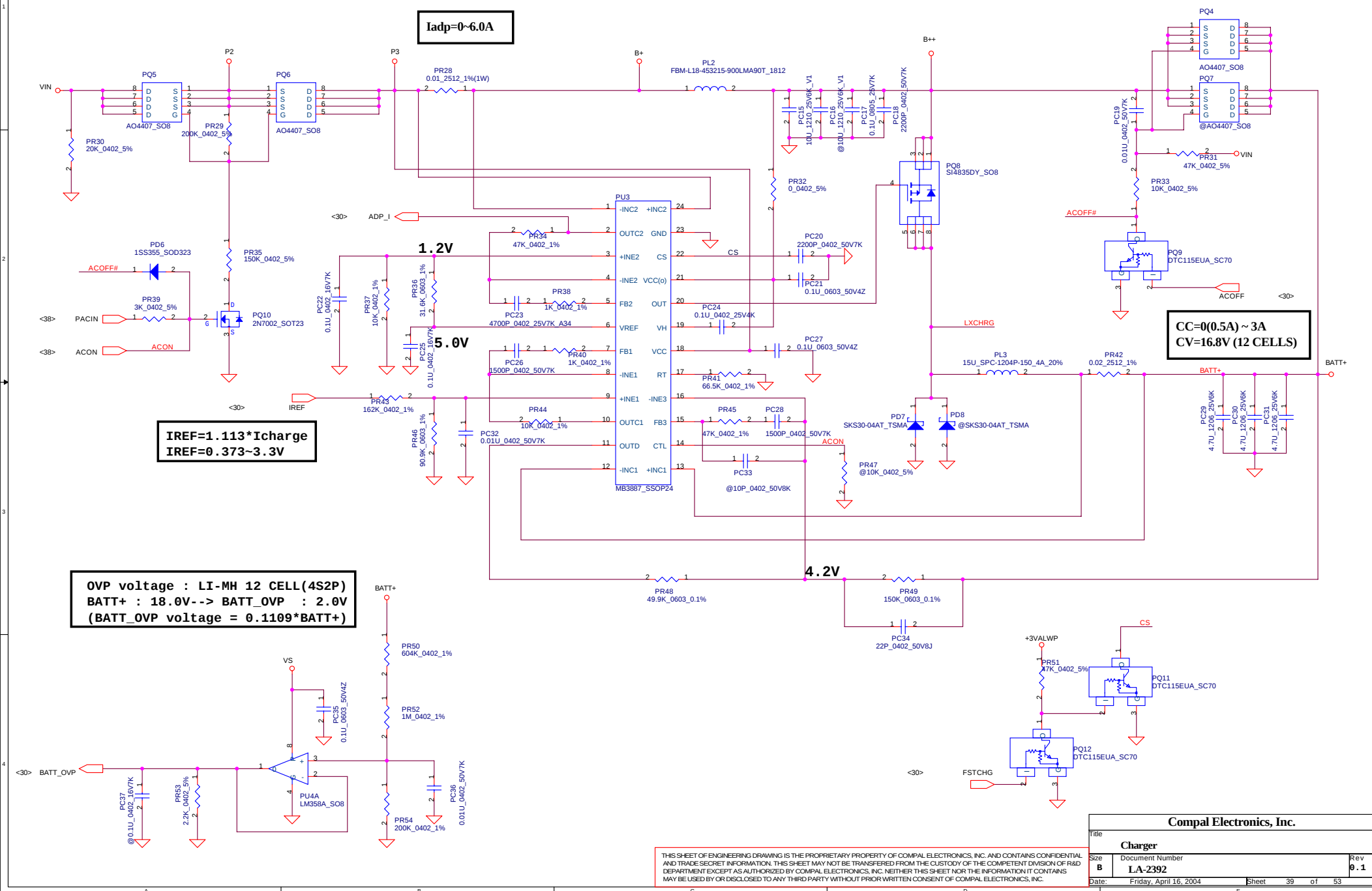
Vin Detector
 18.202 17.841 17.481
 17.568 17.210 16.858

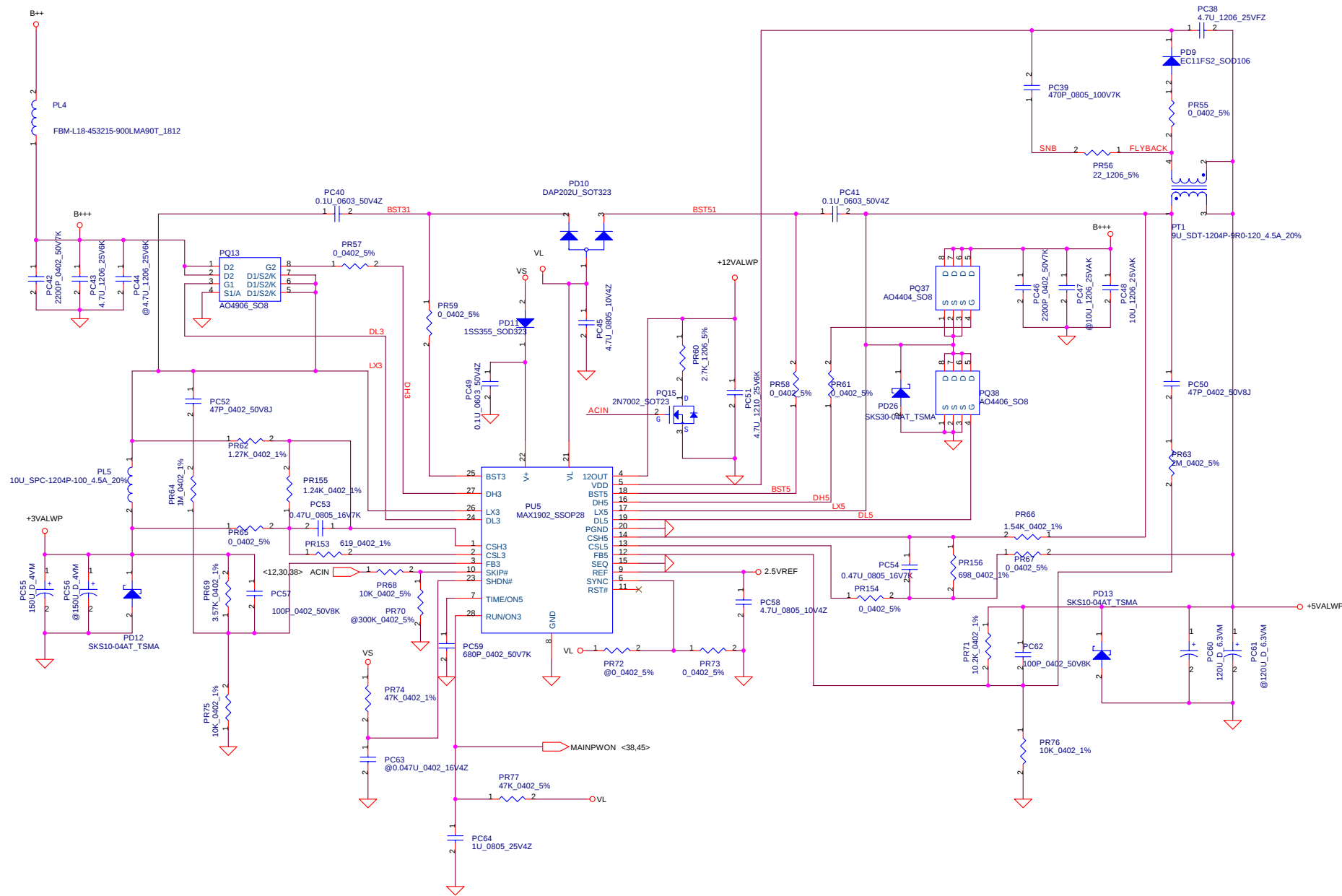


ACIN
 Precharge detector
 16.421 15.817 15.229
 14.108 13.657 13.002

Compal Electronics, Inc.			
File	Detector		
Size	Document Number	Rev	
B	LA-2392	0.1	
Date:	Friday, April 16, 2004	Sheet	38 of 53

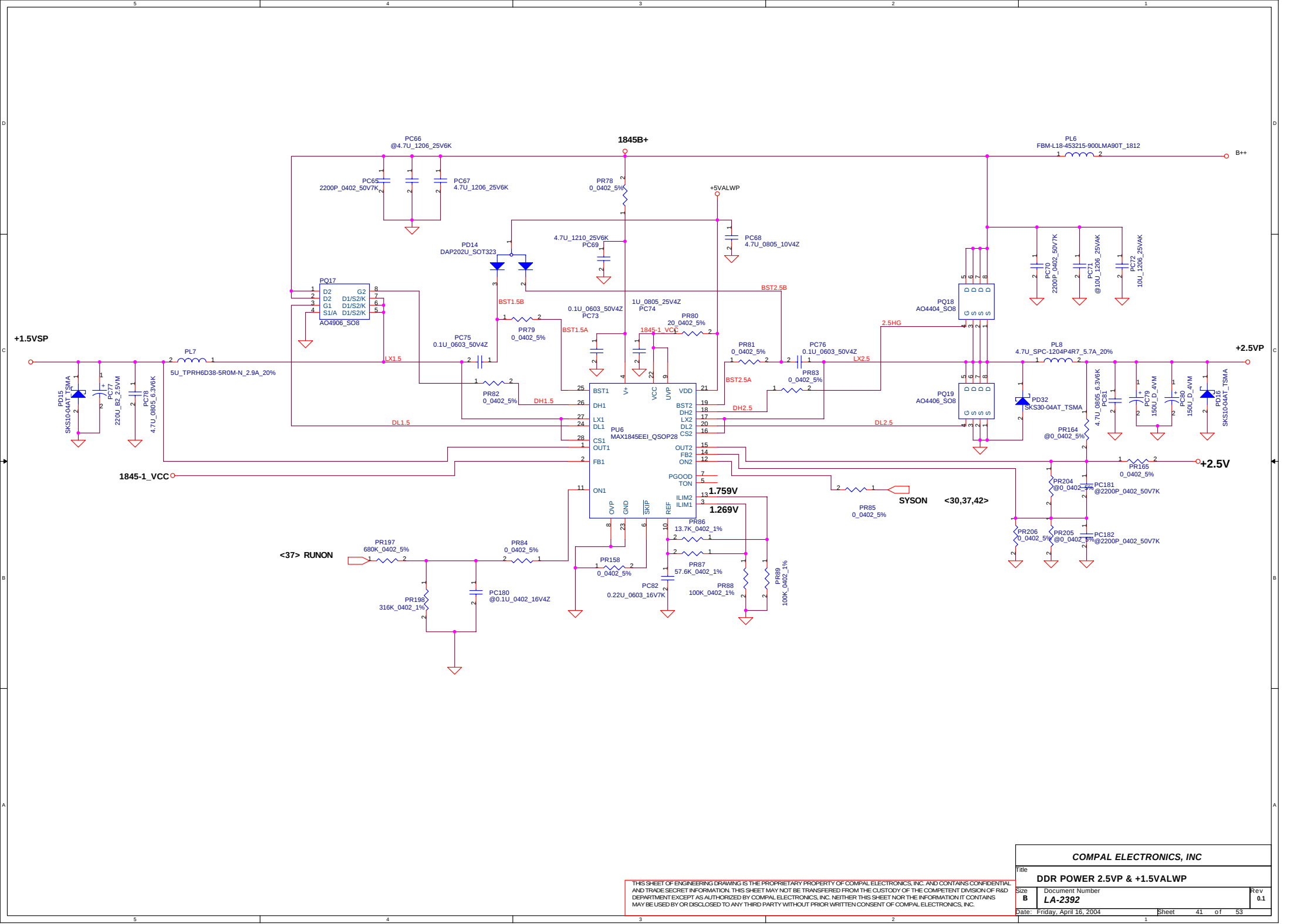
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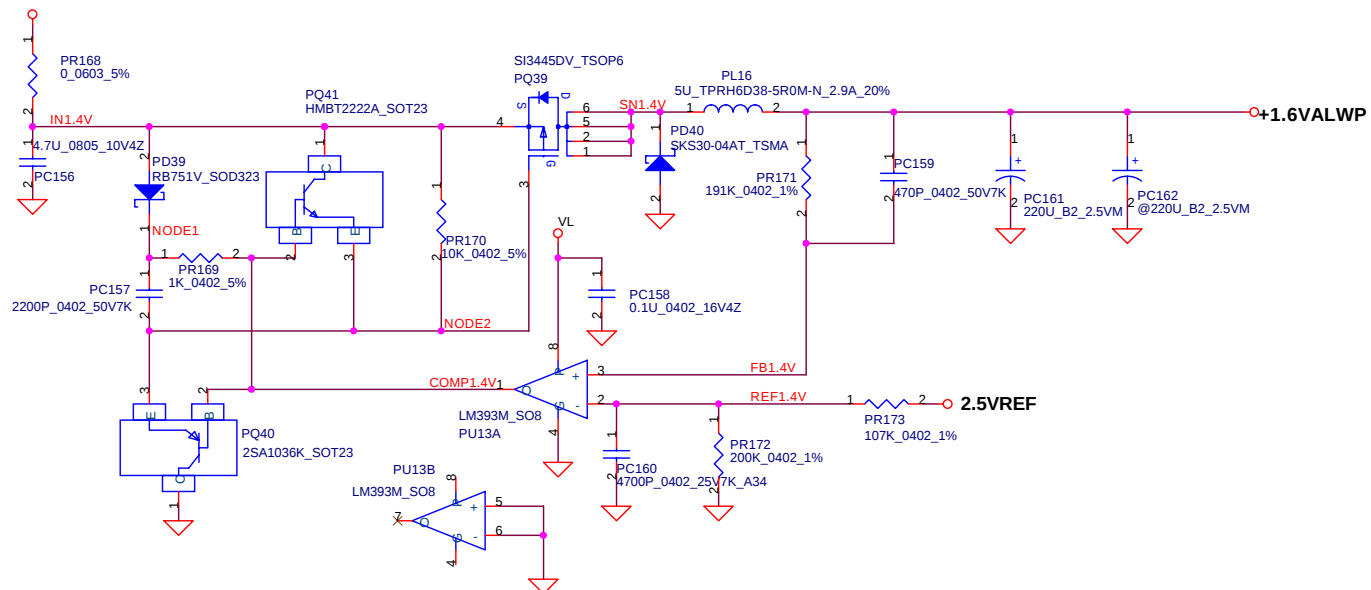
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Compal Electronics, Inc.			
Title	3.3V / 5V / 12V		
Size	Document Number	Rev	
B	LA-2392	1.0	
Date:	Friday, April 16, 2004	Sheet	40 of 53



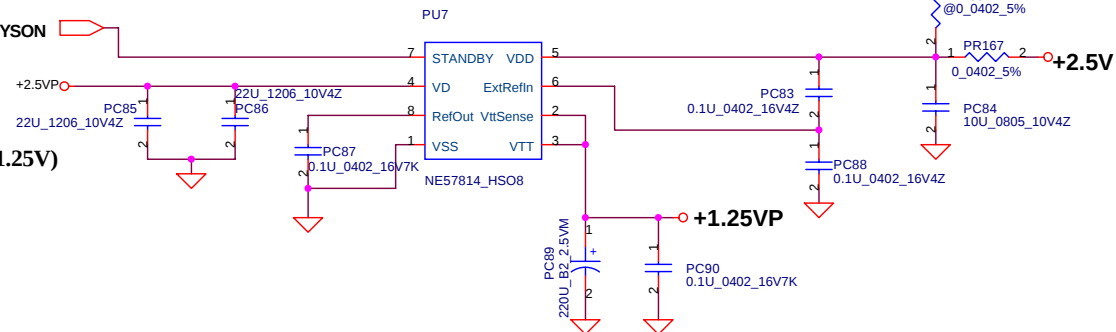
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+5VALWP



<30,37,41> SYSON

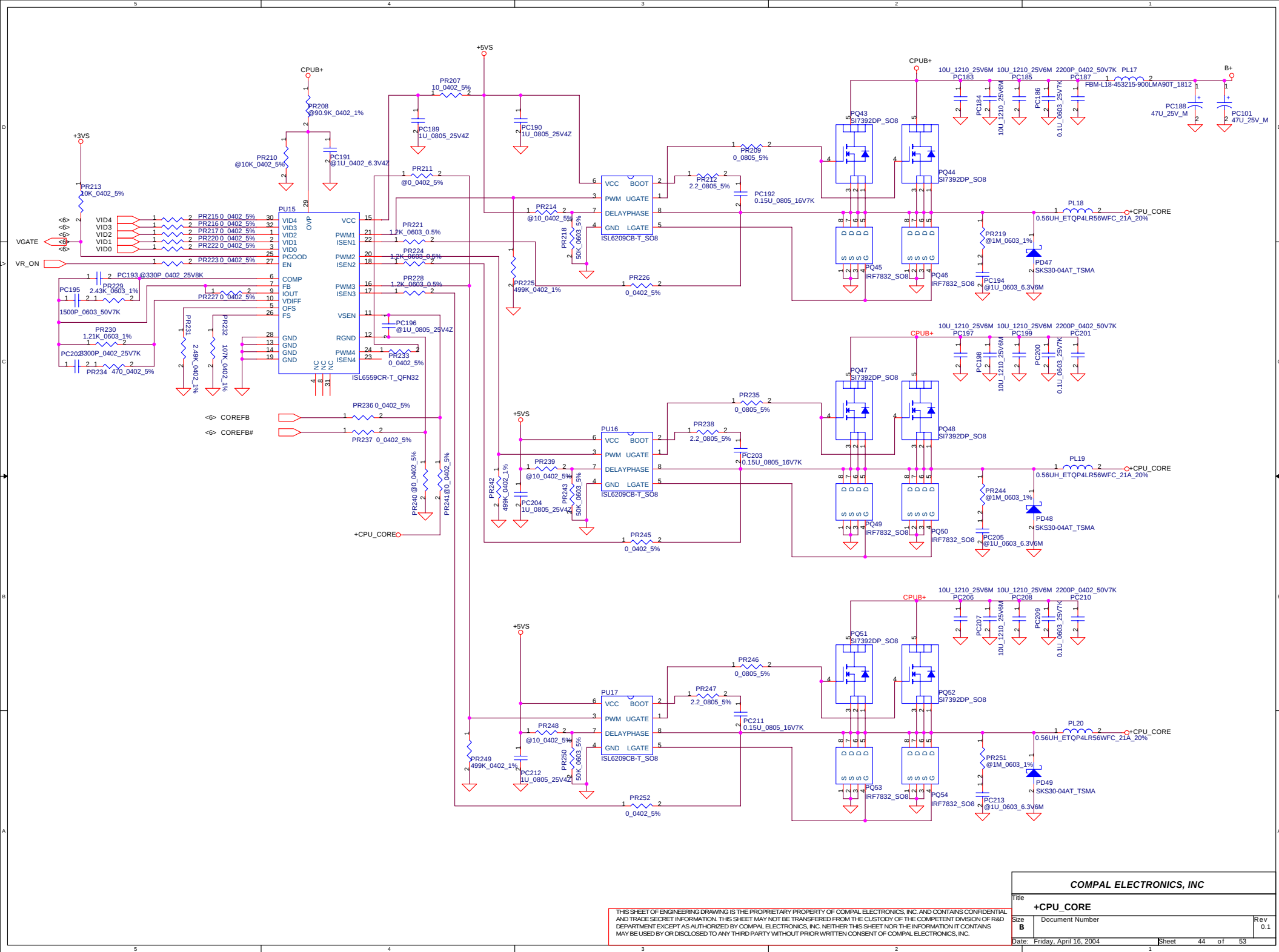
(1.25V)



COMPAL ELECTRONICS, INC

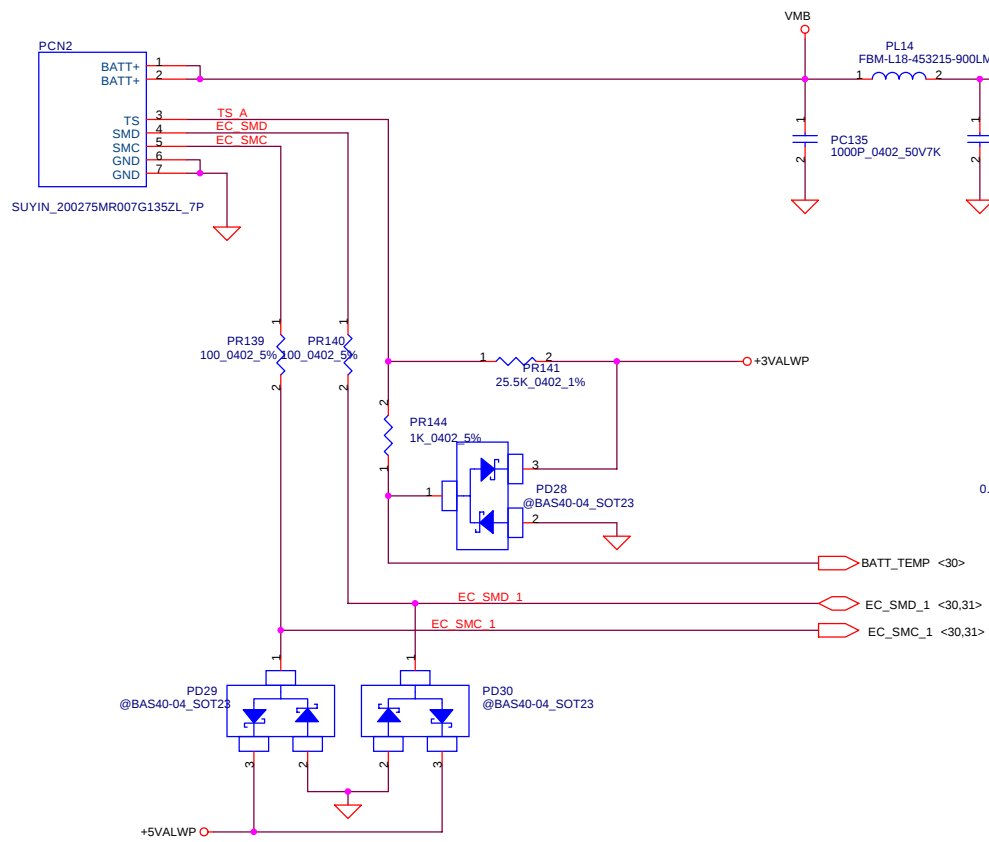
Title		
+1.6VALWP & +1.25VP		
Size	Document Number	Rev
B	LA-2392	0.1
Date:	Friday, April 16, 2004	Sheet 42 of 53

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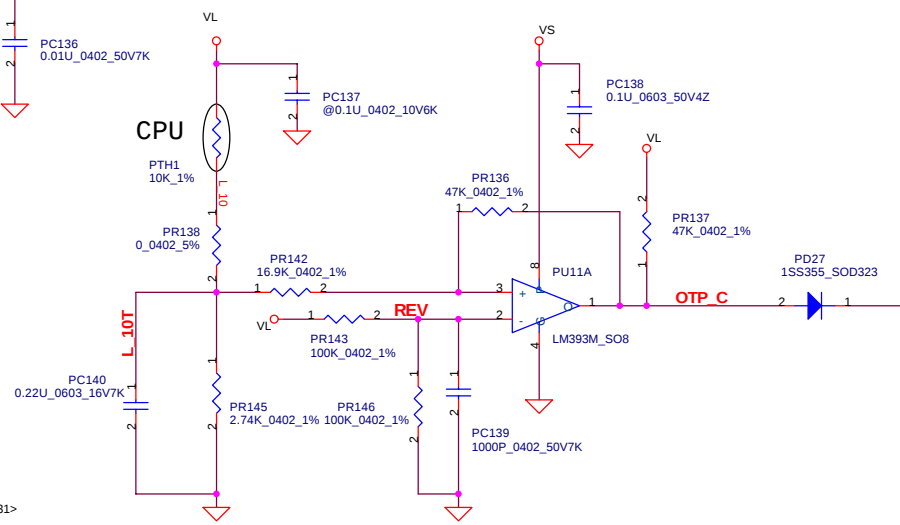


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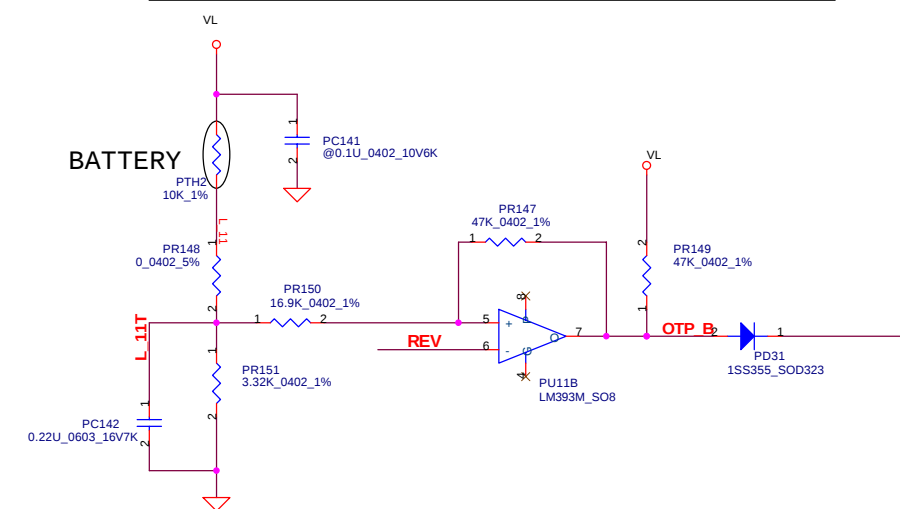
COMPAL ELECTRONICS, INC			
Title +CPU_CORE			
Size B	Document Number	Rev 0.1	
Date: Friday, April 16, 2004		Sheet 44	of 53



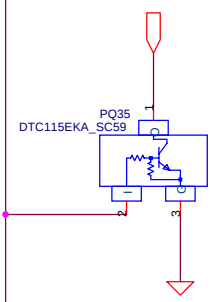
PH1 under CPU bottom side :
 CPU thermal protection at 90 +-3 degree C
 Recovery at 50 +-3 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 84 +-3 degree C
 Recovery at 45 +-3 degree C



<38,40> MAINPWON



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COMPAL ELECTRONICS, INC			
Title			
BATTERY CONN / OTP			
Size	Document Number	Rev	
B	LA-2392	1.0	
Date: Friday, April 16, 2004		Sheet	45 of 53

POWER PIR LIST

PHASE			
DB2	page	Reason for change	Modify list
	40	Modify 3V / 5V Vout and OCP	Change PR66 from 6.49K_0603_1% to 1.54K_0603_1% Change PR156 from 11.8K_0402_1% to 698_0402_1% Change PR154 from 4.12K_0603_1% to 0_0603_5% Change PC54, PC53 from 0.1U_0805_25V7K to 0.47U_0805_25V4Z Change PR62 from 5.76K_0603_1% to 1.27K_0603_1% Change PR155 from 27K_0603_1% to 1.24K_0603_1% Change PR153 from 4.7K_0402_1% to 619_0402_1%
	44,45	For CPU_CORE thermal issue	Change PQ21, PQ26, PQ31, PQ46 From IRLR7821 to SI7392DP Delete PD23, PD43, SC11N4148T8
	42	For 1.6V voltage accuracy	Change PR173 from 113K_0402_1% to 107K_0402_1%
	42	For layout pad issue	Change PC85, PC86 from 22U_1210_10V4Z to 22U_1206_10V4Z
	41	For power sequence setting	Add PR197, 680K_0603_1% Add PR198, 316K_0603_1%
	38	For solving cable dock shutdown issue	Add PD45, SKS80-04CT
SI	38	For thermal issue	Change PD45 from SKS80-04CT to SBM1040
	38	Change VIN detector sensing point because of DOCK issue	Change PR2 from 174k_0603_1% to 150k_0603_0.1% Change PR7 from 75k_0402_1% to 66.5k_0402_1%
	39	Improvment noise issue	
	41	Modify 2.5V / 1.5V OCP	Change PR87 from 24.9k_0402_1% to 57.6k_0402_1% Change PR88 from 0_0603_1% to 13.7k_0402_1% Add PR89, 100k_0402_1%
	43	VGA with 32M VRAM	Remove 1.35V regulator that is for VGA with 64M VRAM
	44,45	Modify CPU_CORE current balance issue	Change the connection of PC122 and PC168 from 14 pin of PU9 to ground. Remove PD22 and PD44.
PV	38	Improve the VIN detector accuracy.	Change PR1, PR2, PR5, PR7, PC6, and re-connect the reference voltage that is VL connected to PR10 to RTC charger output.
	39	Improve the accuracy of Constant Voltage mode of charger.	Change PR48, PR49
	41	reserve devices for the adjustment of 2.5V	Add PR204, PR205, PR206, PC181, PC182
	44	Improve the transient response	Add PR203, PC111, and remove PR202
PV-2	46	Improve the compensation	Change PC168 and PR183
	46	Modify the control signal of MAX1980 (strat the MAX1980 at the same time with MAX1937)	Delete PR180 and add PR208 from pin 13 of MAX1937 to pin 13 of MAX1980

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COMPAL ELECTRONICS, INC		
Title		
PIR		
Size	Document Number	Rev
	LA-2392	0.1
Date: Friday, April 16, 2004		Sheet 46 of 53

POWER PIR LIST

PHASE			
DB2	page	Reason for change	Modify list
	40	Modify 3V / 5V Vout and OCP	Change PR66 from 6.49K_0603_1% to 1.54K_0603_1% Change PR156 from 11.8K_0402_1% to 698_0402_1% Change PR154 from 4.12K_0603_1% to 0_0603_5% Change PC54, PC53 from 0.1U_0805_25V7K to 0.47U_0805_25V4Z Change PR62 from 5.76K_0603_1% to 1.27K_0603_1% Change PR155 from 27K_0603_1% to 1.24K_0603_1% Change PR153 from 4.7K_0402_1% to 619_0402_1%
	44,45	For CPU_CORE thermal issue	Change PQ21, PQ26, PQ31, PQ46 From IRLR7821 to SI7392DP Delete PD23, PD43, SC11N4148T8
	42	For 1.6V voltage accuracy	Change PR173 from 113K_0402_1% to 107K_0402_1%
	42	For layout pad issue	Change PC85, PC86 from 22U_1210_10V4Z to 22U_1206_10V4Z
	41	For power sequence setting	Add PR197, 680K_0603_1% Add PR198, 316K_0603_1%
	38	For solving cable dock shutdown issue	Add PD45, SKS80-04CT
SI	38	For thermal issue	Change PD45 from SKS80-04CT to SBM1040
	38	Change VIN detector sensing point because of D0CK issue	Change PR2 from 174k_0603_1% to 150k_0603_0.1% Change PR7 from 75k_0402_1% to 66.5k_0402_1%
	39	Improvment noise issue	
	41	Modify 2.5V / 1.5V OCP	Change PR87 from 24.9k_0402_1% to 57.6k_0402_1% Change PR88 from 0_0603_1% to 13.7k_0402_1% Add PR89, 100k_0402_1%
	43	VGA with 32M VRAM	Remove 1.35V regulator that is for VGA with 64M VRAM
	44,45	Modify CPU_CORE current balance issue	Change the connection of PC122 and PC168 from 14 pin of PU9 to ground. Remove PD22 and PD44.
PV	38	Improve the VIN detector accuracy.	Change PR1, PR2, PR5, PR7, PC6, and re-connect the reference voltage that is VL connected to PR10 to RTC charger output.
	39	Improve the accuracy of Constant Voltage mode of charger.	Change PR48, PR49
	41	reserve devices for the adjustment of 2.5V	Add PR204, PR205, PR206, PC181, PC182
	44	Improve the transient response	Add PR203, PC111, and remove PR202
PV - 2	46	Improve the compensation	Change PC168 and PR183
	46	Modify the control signal of MAX1980 (strat the MAX1980 at the same time with MAX1937)	Delete PR180 and add PR208 from pin 13 of MAX1937 to pin 13 of MAX1980

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COMPAL ELECTRONICS, INC			
Title PIR			
Size	Document Number LA-2392		Rev 0.1
Date: Friday, April 16, 2004		Sheet	47 of 53

POWER PIR LIST (2)

PHASE			
	page	Reason for change	Modify list
	39	Modify charger for using 90W adapter	Change PR34 from 47K_0402_1% To 10K_0402_1% Change PR38 from 1K_0402_1% To 10K_0402_1% Change PR28 from 0.01_2512_1% To 0.012_2512_1% Change PR36 from 31.6K_0603_1% To 37.4K_0603_1% Change DC Jack
	39,40,41	Change capacitor size for cost down	Change PC48, PC72 from 10u_1210_25V to 10u_1206_25V Change PC29, PC30, PC31, PC43, PC67 from 4.7u_1210_25V to 4.7u_1206_25V

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COMPAL ELECTRONICS, INC		
Title		
PWR PIR(2)		
Size	Document Number	Rev
	LA-2392	0.1
Date: Friday, April 16, 2004		Sheet 48 of 53

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Compal Electronics, Inc.			
Title P.I.R HISTORY			
Size	Document Number		Rev
Custom	LA-2392		0.1
Date:	Friday, April 16, 2004	Sheet	49 of 53

Version change list (P.I.R. List)

Page 2 of 4

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		AMD change Tdiode spec up to 127 degree	P4	Change U3 from MAX6649 to ADM1032	0.4
2		Support wake from Lan	P20	Populate R188	0.4
3		To avoid PCI1620 unknow action	P22	Reserve R591	0.4
4		To restrain audio noise	P25	Change R267 pull up to +5VAMP_CODEC, and delete C626	0.4
5		USB_OC# high should be between 2.5V to 5.5V	P27	Change R310 and R315 to 10K / R314 and R319 to 20K	0.4
6		To detect FIR	P29	Add R592 and R593	0.4
7		TP should be pull up to +5V	P30	RP80 pull up to +5V	0.4
8		In order to compatible with NS97551 -- changing pin87 ~ 90 to GPIO	P30	BID routed from pin88 to pin82	0.4
9		In order to compatible with NS97551 -- removing +RTCVCC	P30	Add R594 and R595	0.4
10		To prevent noise generated from FAN to +5VS cause audio noise while shut down	P4	Delete D1 and D3 / add C3, C8, C612, and C614	0.4
11		Solve for PCI1620 working abnormal -- fine tune G_RST# timing	P22	Populate R587, delete R225, C410	0.4
12		Double mount issue, already exist at audio board.	P30	Delete D28 and D29	0.4
13		Fast power on for battery only	P33	Change R392 from 100K to 4.7K	0.4
14		Presario LED color should be amber	P35	Change D39, D40, D42, D44, and D45 from XX_GRN to XX_ORG	0.4
15		To develop SI9182 max effect	P25	Change C438 from 0.01UF to 0.1UF	0.4
16		For EMI	P26	Add L40, L41, L42, and L43 / delete C473, C474, C475, and C476	0.4
17		For VGA HSYNC/VSYNCR average peak to peak issue	P18	Add R159 and R160	0.4
18		For 512MB non-JEDEC module (16 chips)	P9	Change RP42, RP46, and R481 from 68 Ohm to 47 Ohm	0.4

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Compal Electronics, Inc.			
Title P.I.R HISTORY			
Size	Document Number		Rev
Custom	LA-2392		0.1
Date:	Friday, April 16, 2004		Sheet 50 of 53

Version change list (P.I.R. List)

Page 3 of 4

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		To use the same source as HR60	P4	Change U3 footprint to SOP8	0.5
2		To reset CK8 while boot up control by EC	P12	Add R97 to link EC_RSMRST# and PWRGD_SB	0.5
3		For EMI	P15	Change C648, C672, C685, C696, C699, C763, and C656 to 1000P Change C651, C673, C686, C697, C700, C764, C654, C733, C710, C730, C706, and C724 to 10P	0.5
4		To solve voltage level of HSYNC and VSYNC is over spec	P18	Add U46 and U47, and R596, R597, and R598 on CRT_HSYNC and CRT_VSYNC	0.5
5		Solve for data lost while transfer data from LAN	P20	Change U9 from NS0013 to NS0019	0.5
6		TI recommendation --- avoid unknow state while initiate	P22	Populate R591	0.5
7		Mechanical restricted area	P25	R263 and R264 change footprint to R_0402	0.5
8		For EMI	P25	L39 and R293 change to CHB1608U301_0402	0.5
9		For EMI	P26	L40, L41, L42, and L43 change to KC FBM-L11-201209-221LMAT_0805	0.5
10		nVIDIA recommendation for WOR	P27	Add U48, C807, R599, and R600	0.5
11		Due to MD_SPK is no longer use, so prevent input pin floating.	P25	Delete R287 and change R288 to 0_0402_5%. Also add C808.	0.5
12		Due to USB data has leakage problem, so need to delay USB_VCC power up timing controlled by EC to solve for unknow device while power on with battery only.	P27 P30	Wired R368.2 to U18.4 and U19.4	1.0

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Compal Electronics, Inc.			
Title P.I.R HISTORY			
Size	Document Number		Rev
Custom	LA-2392		0.1
Date:	Friday, April 16, 2004		Sheet 51 of 53

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Cost Down	P4	Change C1, C4, C8, C330, C339, C447, C596, C599, C609 from 10U_1206_10V4Z to 10U_0805_10V4Z	0.5C
2		Cost Down	P6	Delete C15 (330U_D_2VM_R15), Add C810 (330U_6.3V_M)	0.5C
3		Cost Down	P12 P25 P14 P26 P15 P27 P18 P29 P20 P30 P22 P31	Delete 0_0402_5% -- R97, R105, R108, R282, R288, R289, R300, R312, R313, R317, R318, R320, R321, R326, R327, R359, R368, R375, R377, R381, R393, R469, R587, R597, R598, R219 Delete 0_0603_5% -- R462, L26, L27, L30, L32, L33, L34 Delete 0_0805_5% -- R459, R465, L16, L20, Delete 0_1206_5% -- R394,	0.5C
4		Cost Down (VBIOS can cover it)	P14	Delete R502 and R503	0.5C
6		Improve reliability	P18	Add C811	0.5C
7		Cost Down	P18	Change D12 from RB491D_SOT23 to RB411D_SOT23	0.5C
8		Cost Down (RTL8101L integrate those parts)	P20	Delete Q22, C353, C354, C358, C359 and add L44	0.5C
9		Cost Down	P21	Delete C376, C378, C382, C383, C384	0.5C
10		Cost Down (EC can control it)	P22	Delete D16 and R218	0.5C
11		Internal pull up	P23	Delete R227	0.5C
12		Cost Down	P23	Delete C423 and C631	0.5C
13		Cost Down (No reserve PC1520)	P24	Delete R231, R232, R240, R241, R242, R243, R244, R245, R256, R259, R260, RP71, RP71, RP73, RP74, RP75, RP76, RP77, C430	0.5C
14		Cost Down	P25	Delete C435, C436, C808, and add R604	0.5C
15		Cost Down	P28	Delete C512, C515, C522, C524	0.5C
16		Cost Down	P29	Delete C525, C529	0.5C
17		Cost Down	P30	Change U21 from 87591L to 97551, delete C539 and C543, add R603, D59, C627	0.5C
19		Cost Down	P43	Delete C564, C566	0.5C

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Size	Document Number
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Sheet	52 of 53
Rev	0.1

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