



PCB
Part Number = DA60000M700

Compal Confidential

PBL50 Schematics Document

AMD APU Zacate-FT1 + FCH Hudson-M1 + DGPU Seymour XT-M2

2011-02-15

REV: 0.22

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

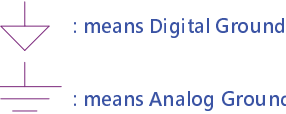
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

SMBUS Control Table

	SOURCE PU Rail	MIINI1	BATT	APU	FCH	SODIMM	VRAM
EC_SMB_CK1 EC_SMB_DA1	KB930 +3VALW	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V +3VS	V	X	V
FCH_SMCLK0 FCH_SMDAT0	FCH +3VS	V	X	X	V	V	X
FCH_SIC FCH_SID	FCH +3VALW	X	X	V Reserve	X	X	X

SCL0, SDA0 (Primary SMBUS in the S0 domain)
SCL1, SDA1 (Secondary SMBUS supporting ASF)
SCL2, SDA2 (Primary SMBUS in the S5 domain)
SCL3, SDA3 (Primary low-voltage SBMBUS for Processor TSI)
SCL4, SDA4 (Primary SMBUS in the S5 domain)

Symbol Note :



FCH Hudson-M1 USB Port List	
USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	JUSB1
Port1	JUSB2
Port2	Camera
Port3	JMINI (WLAN)
Port4	Card Reader
Port5	JUSB3
Port6	NC
Port7	NC
Port8	NC
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List		
APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M1 SATA Port List	
SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

BOM Structure

10G@ : 1.0G CPU (C50)
15G@ : 1.5G CPU (E240)
16G@ : 1.6G CPU (E350)
UMA@ : APU output.
VGA@ : GPU used.
LS@ : Level shift used.
X76@ : VRAM.

X76@L01: Samsung 1G
X76@L02: Hynix 1G
X76@L03: Samsung 512M
X76@L04: Hynix 512M

DIS M/B BOM Config
L01: 16G@/VGA@/LS@ --X76@L04
L02: 16G@/UMA@/LS@
L03: 15G@/VGA@/LS@ --X76@L03
L04: 15G@/UMA@/LS@
L05: 16G@/VGA@/LS@ --X76@L01
L06: 15G@/VGA@/LS@ --X76@L02
L07: 10G@/UMA@/LS@

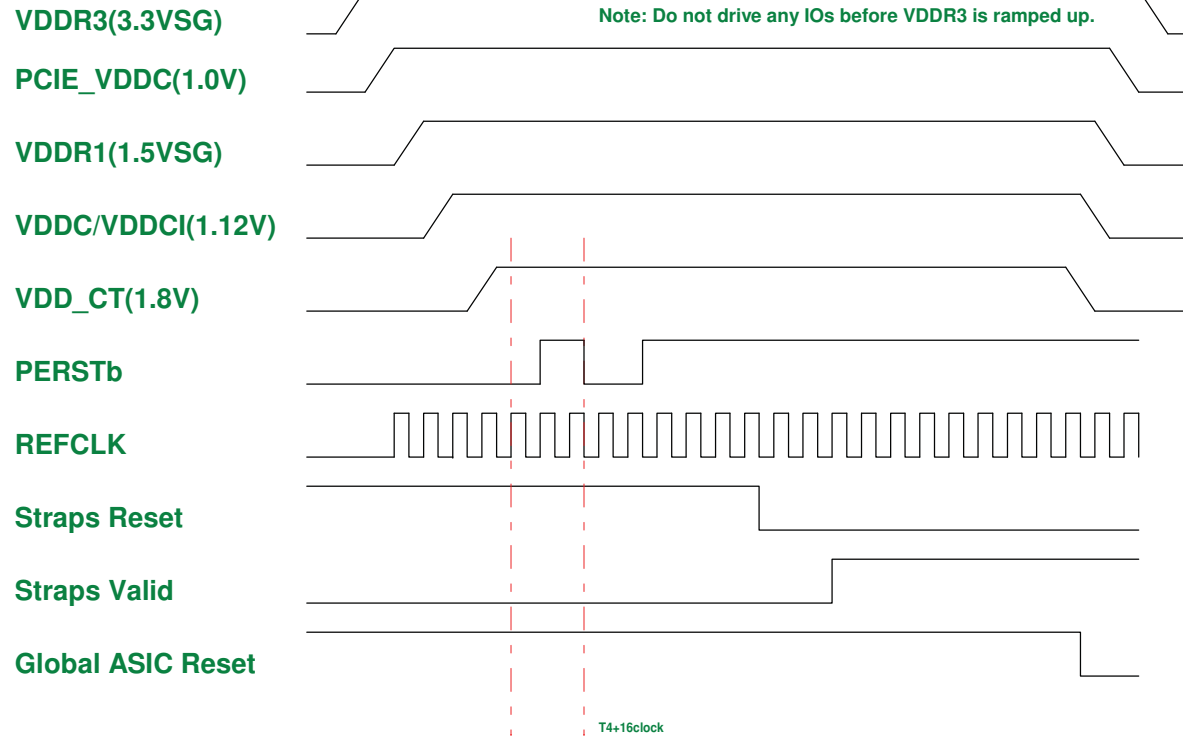
1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5.VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



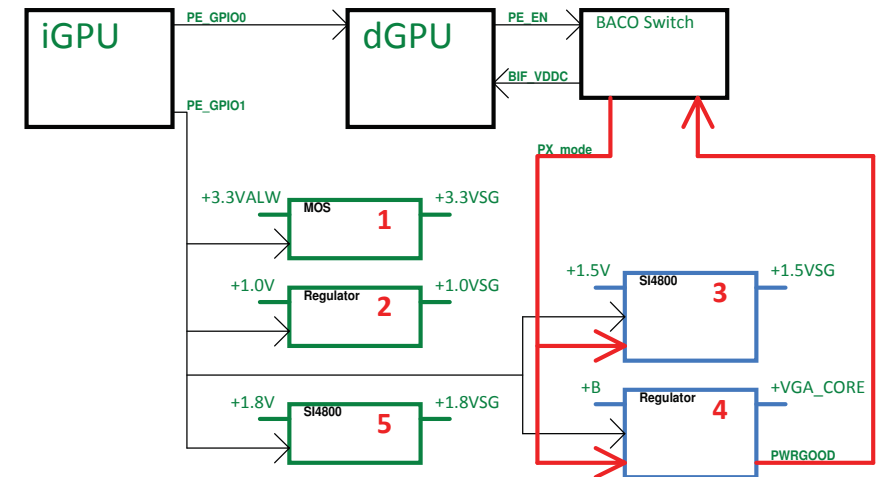
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High -> Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

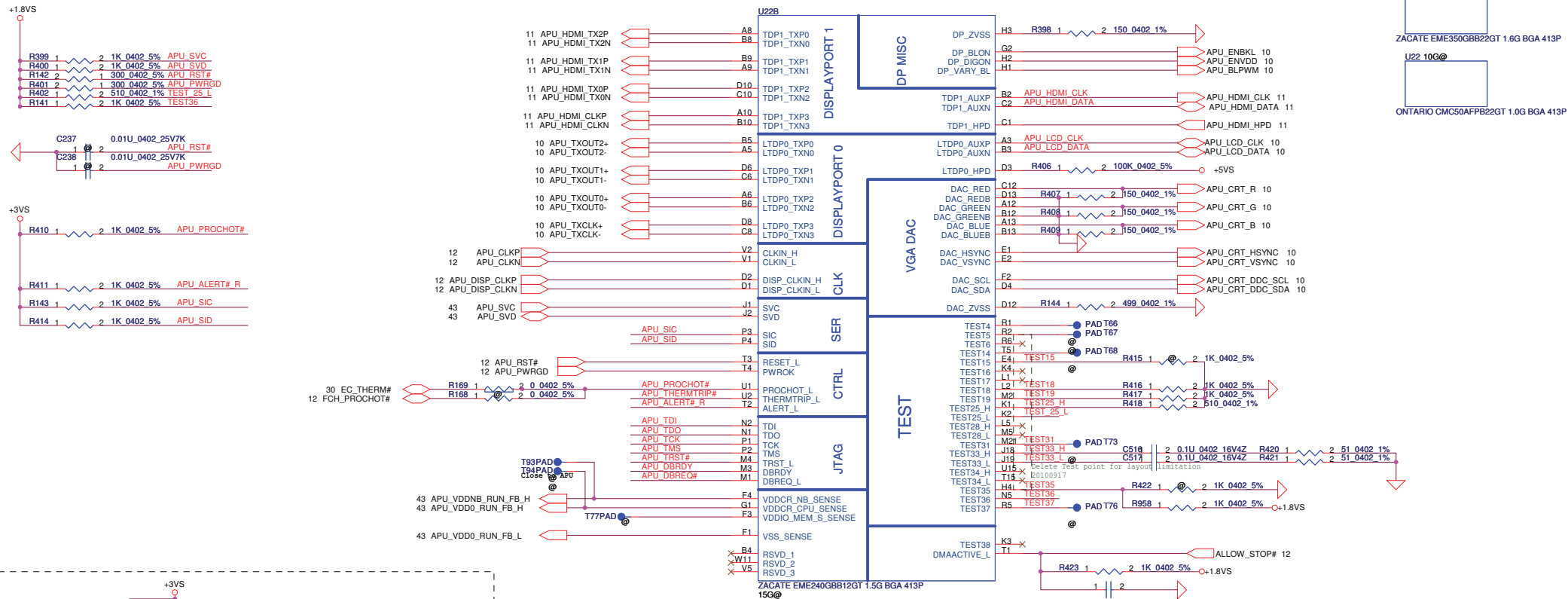
PE_GPIO0 : High -> Normal operation (dGPU is not reset on BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

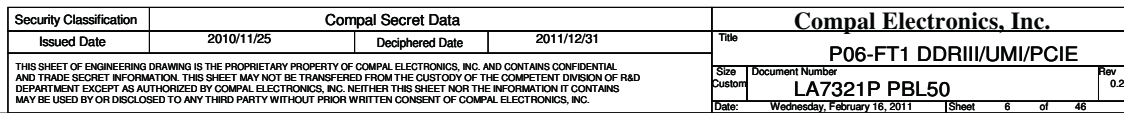
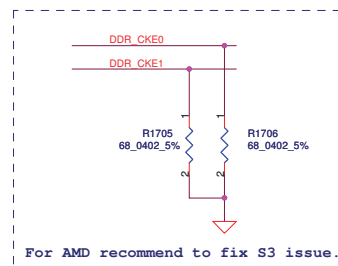
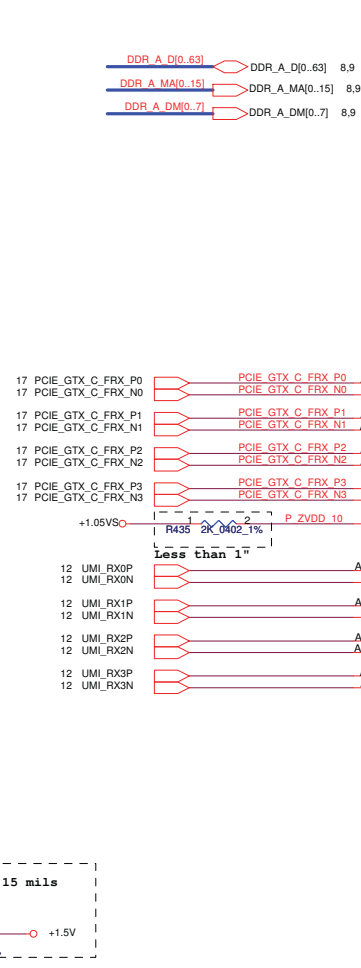
dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1D1, A2VDDQ, VDD2D1, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A

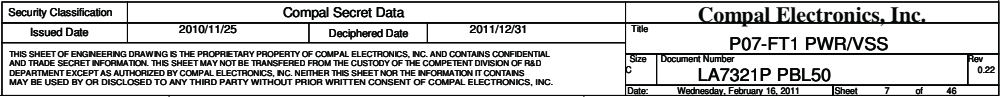


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APU 10G@: SA00004KD70 (S IC ONTARIO CMC50AFB22GT 1.0G BGA 413P) - C50
APU 15G@: SA00004KF50 (S IC ZACATE EME240GBB12GT 1.5G BGA 413P) - E240
APU 16G@: SA00004KG70 (S IC ZACATE EME350GBB22GT 1.6G BGA 413P) - E350



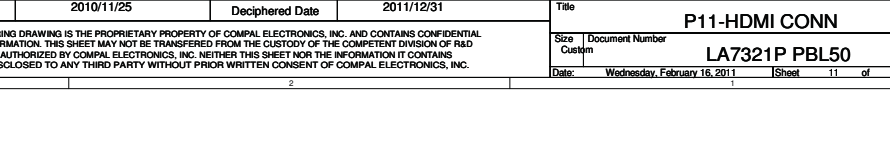
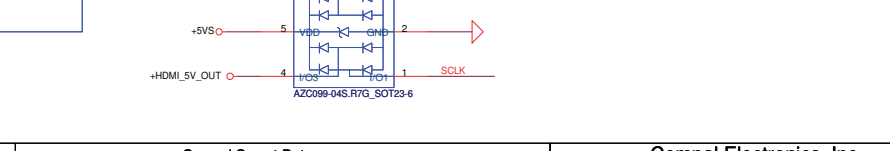
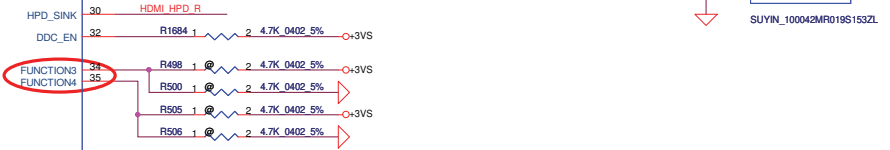
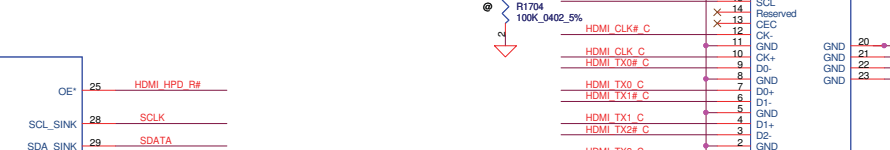
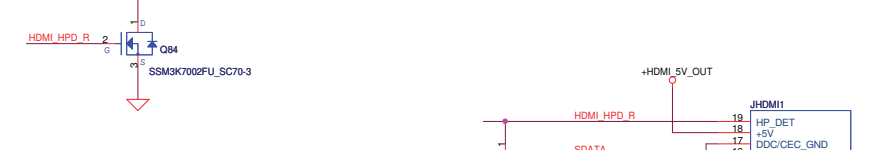
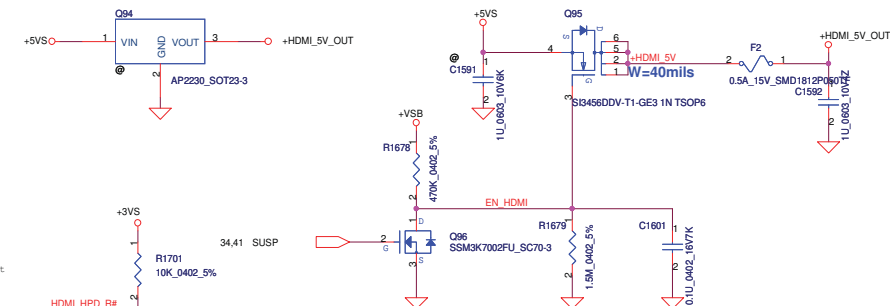
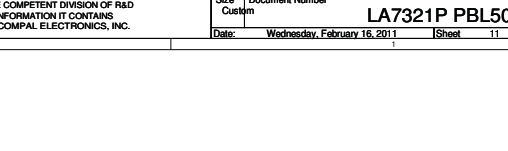
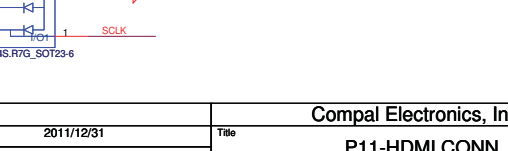
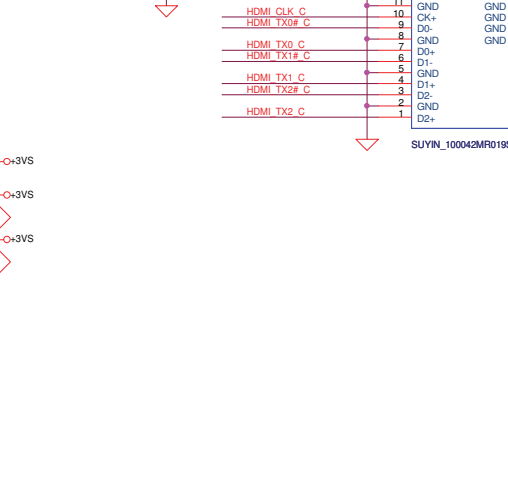
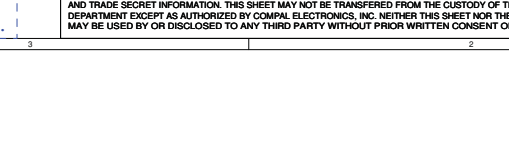
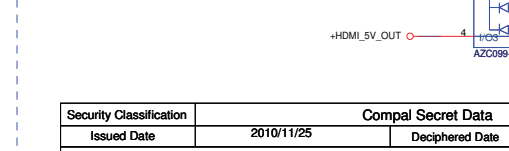
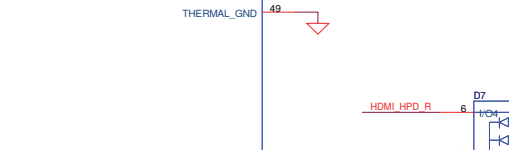
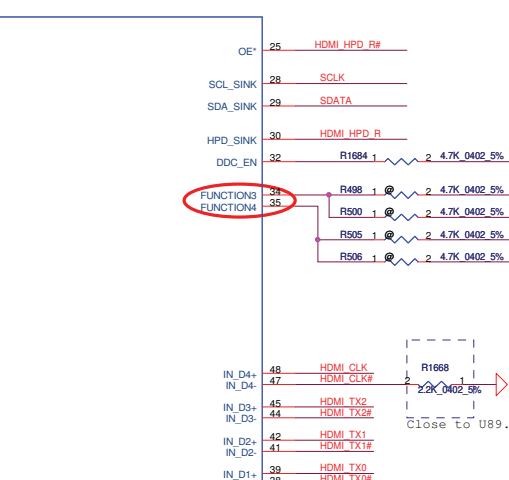
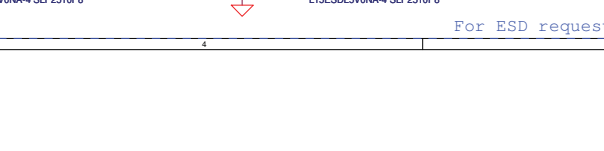
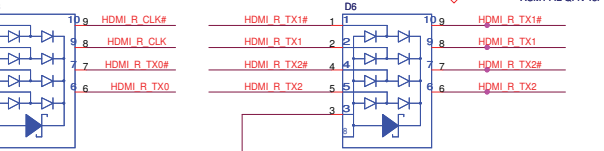
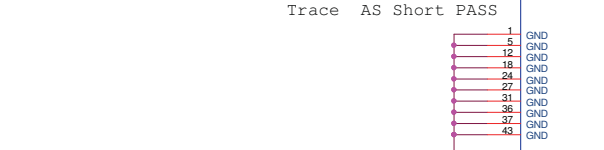
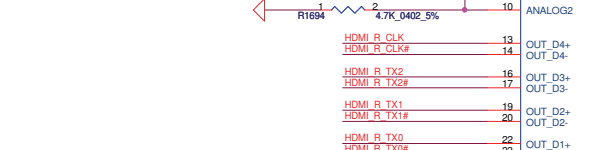
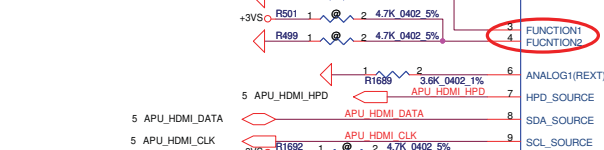
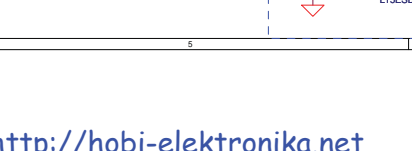
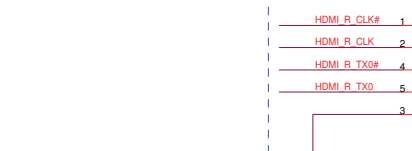
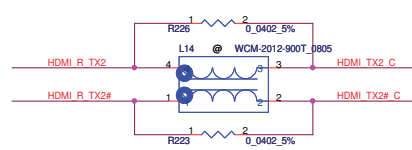
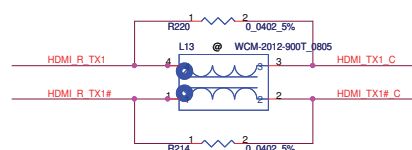
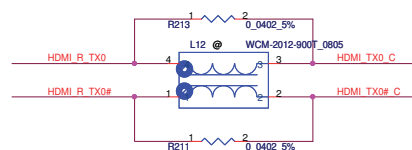
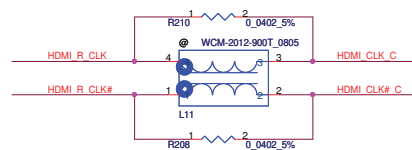
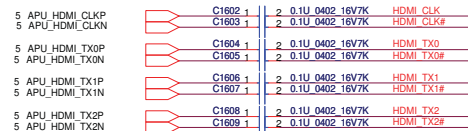
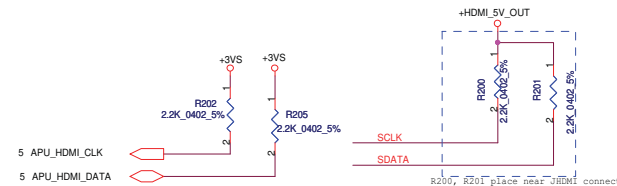
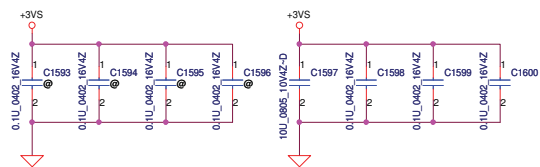




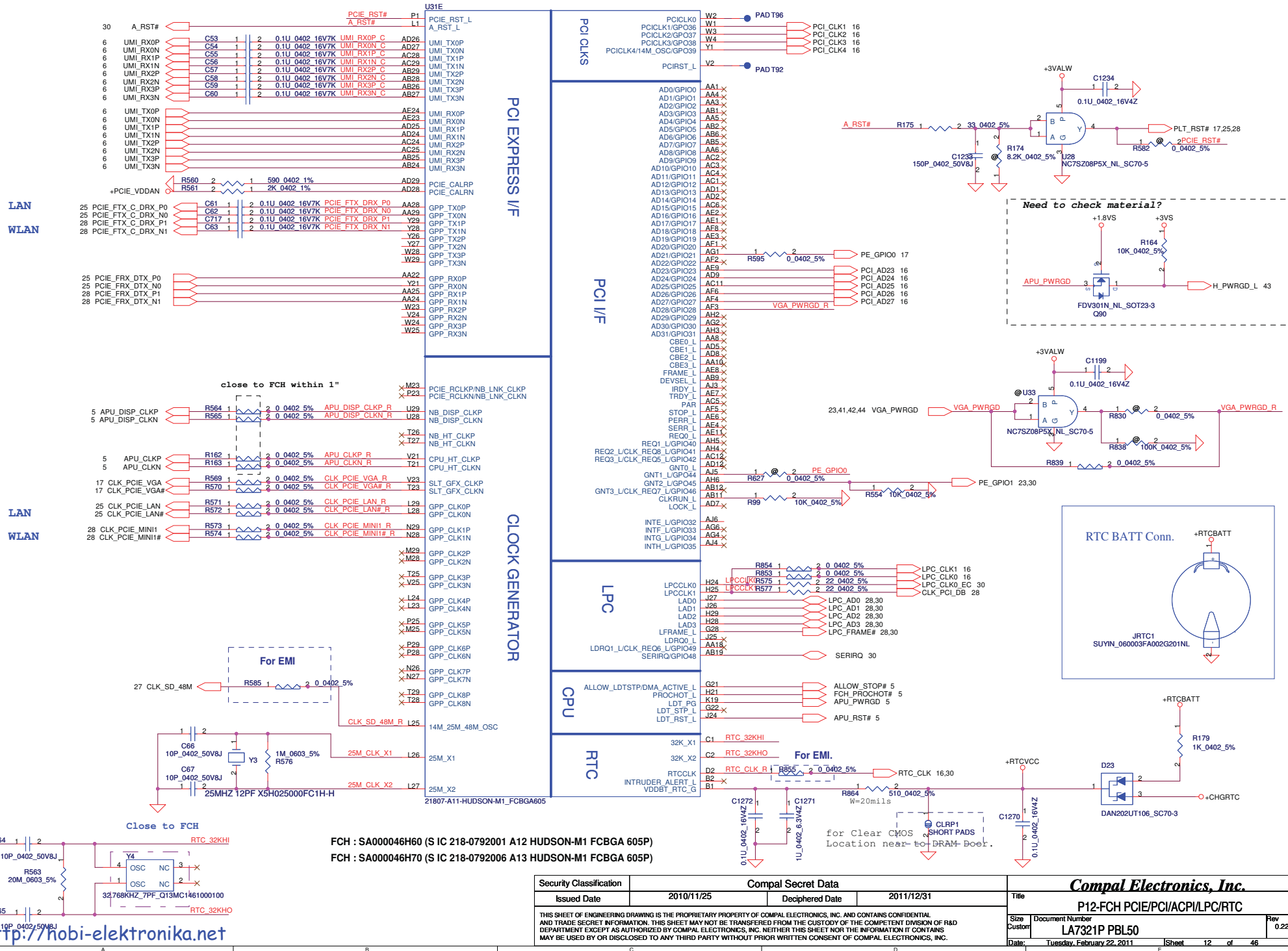


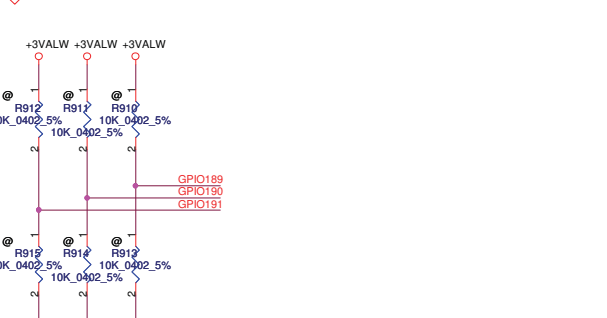
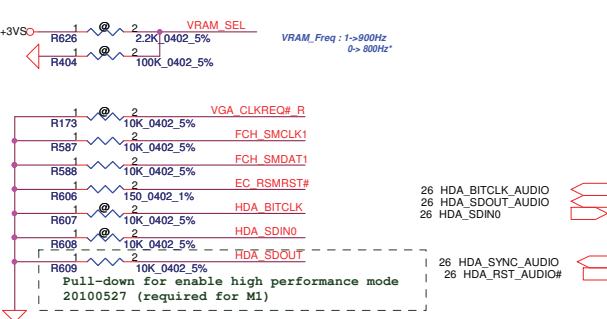
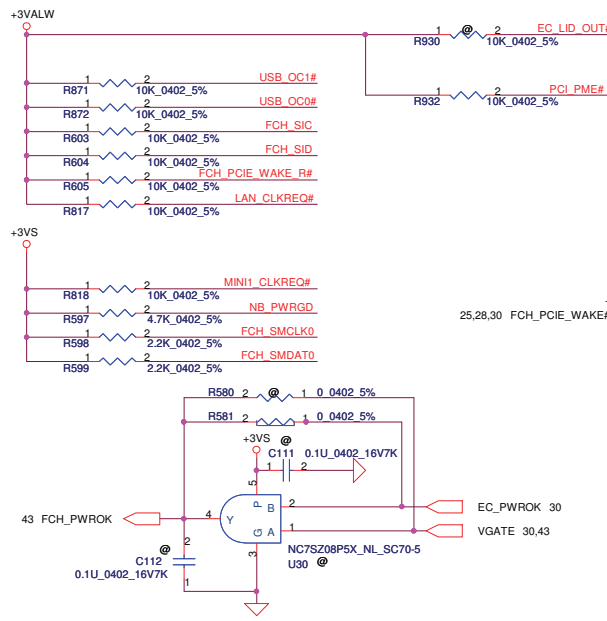


close to U10VCC (+3VS) pins (one Pin one Capacitor)



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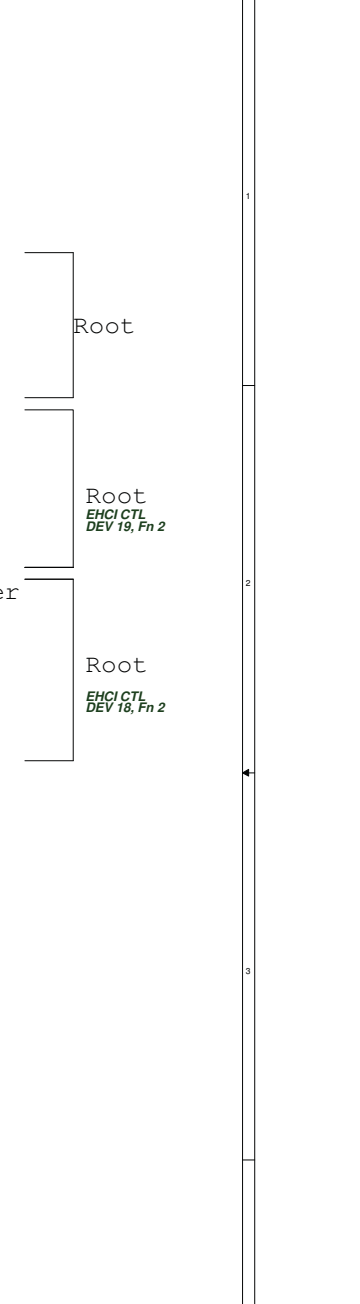
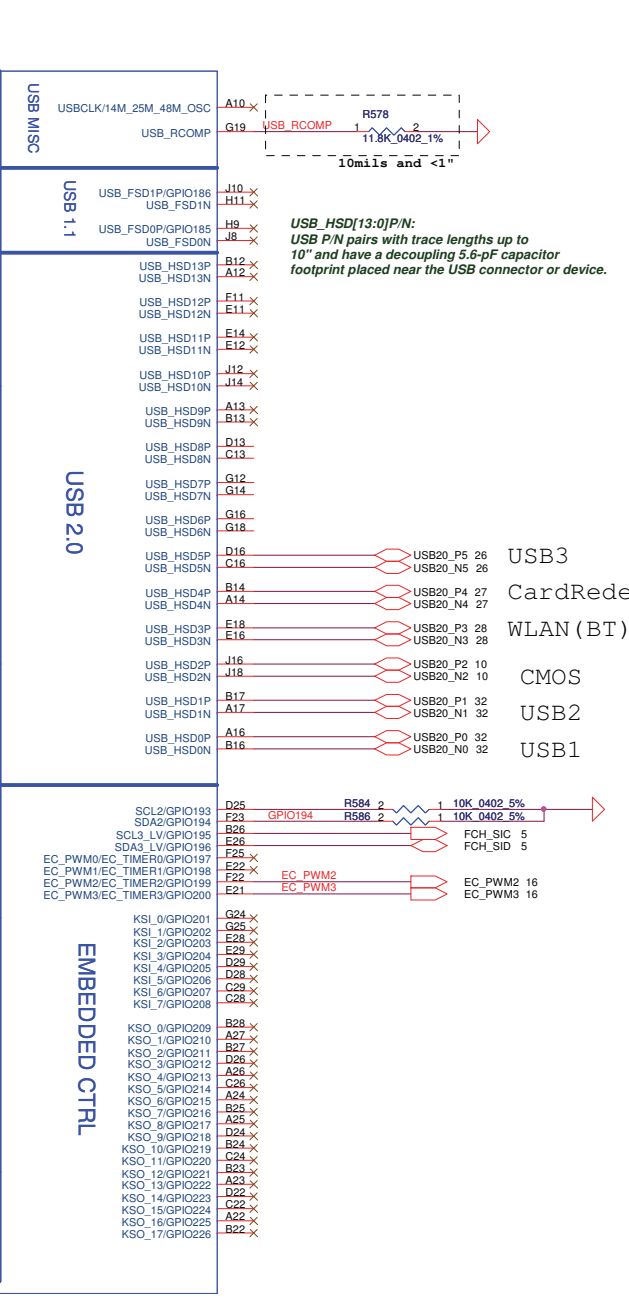
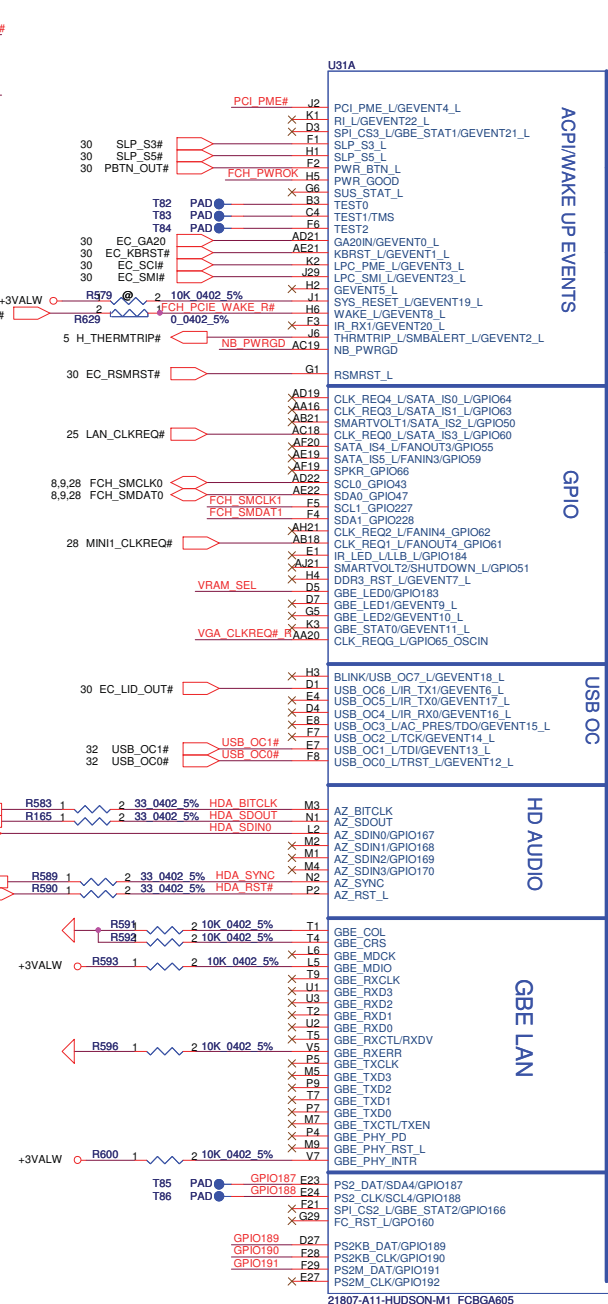


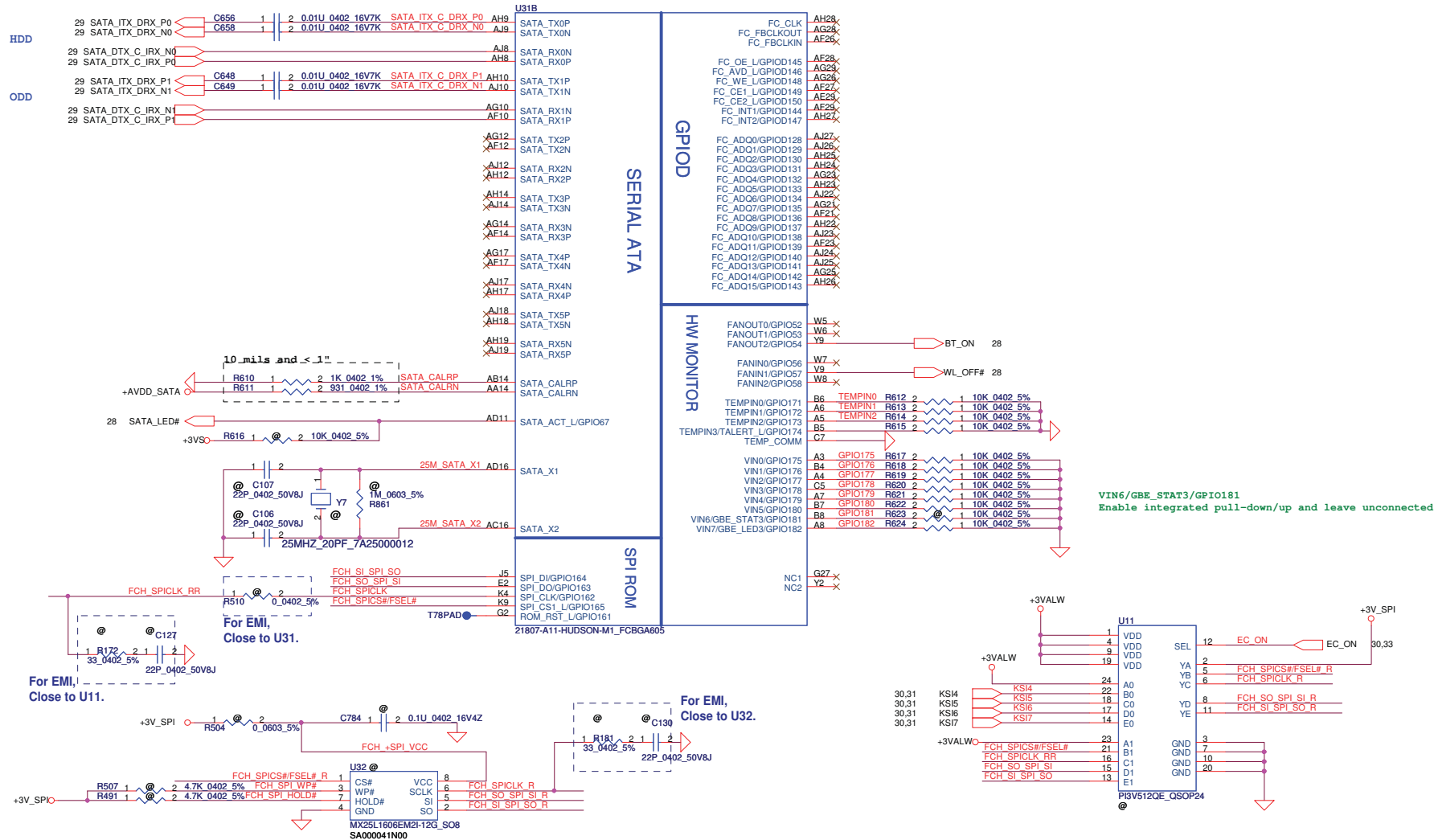


SKU_ID (GPIO189)	SKU_ID : 1→VGA* 0→UMA
PX_FN (GPIO190)	PX_Function : 1→PX Enable* 0→PX Disable
PX_SEL (GPIO191)	PX_SEL : 1→PX 3.0* 0→PX 4.0

Do not Use In PBL50/60/70

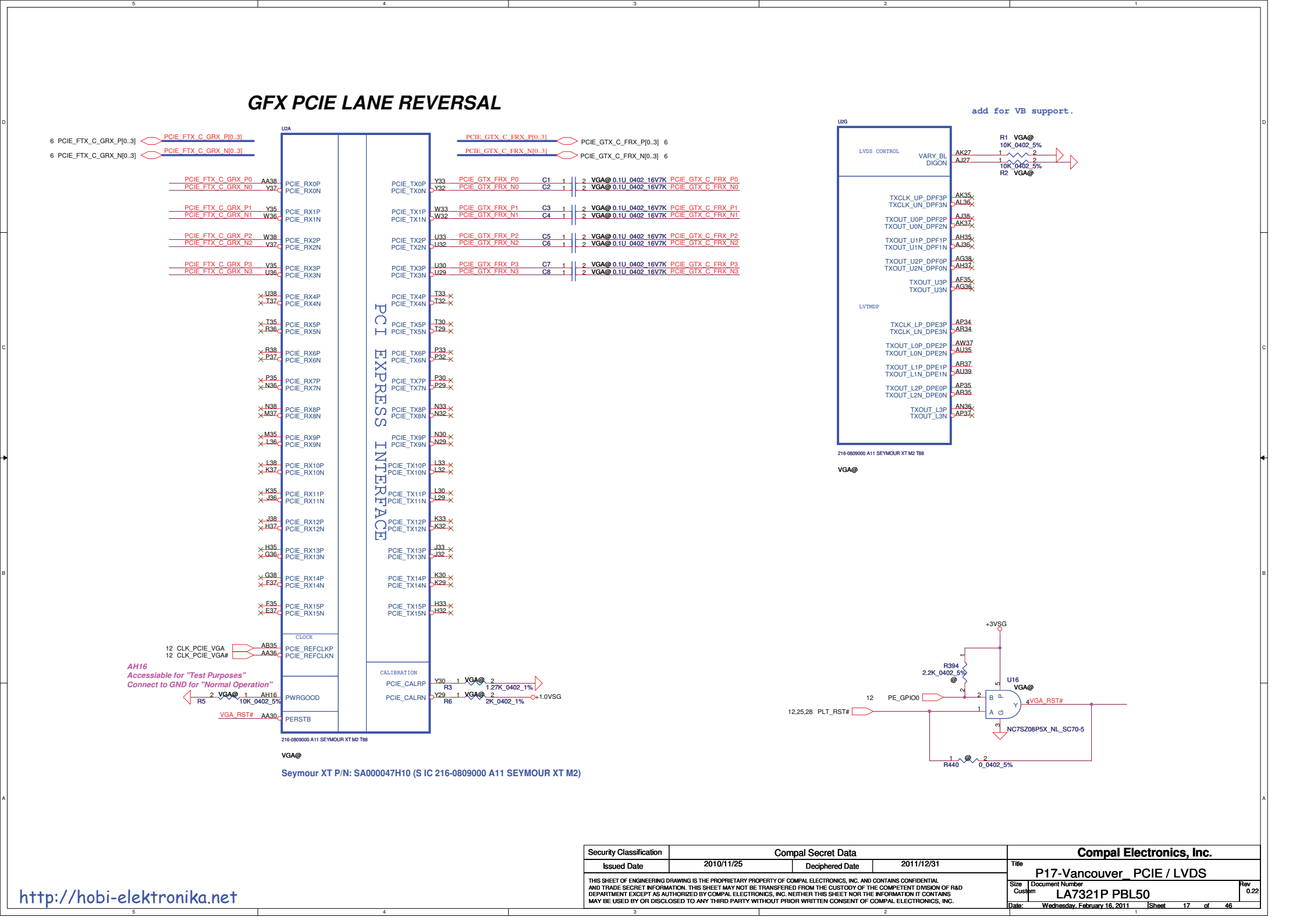
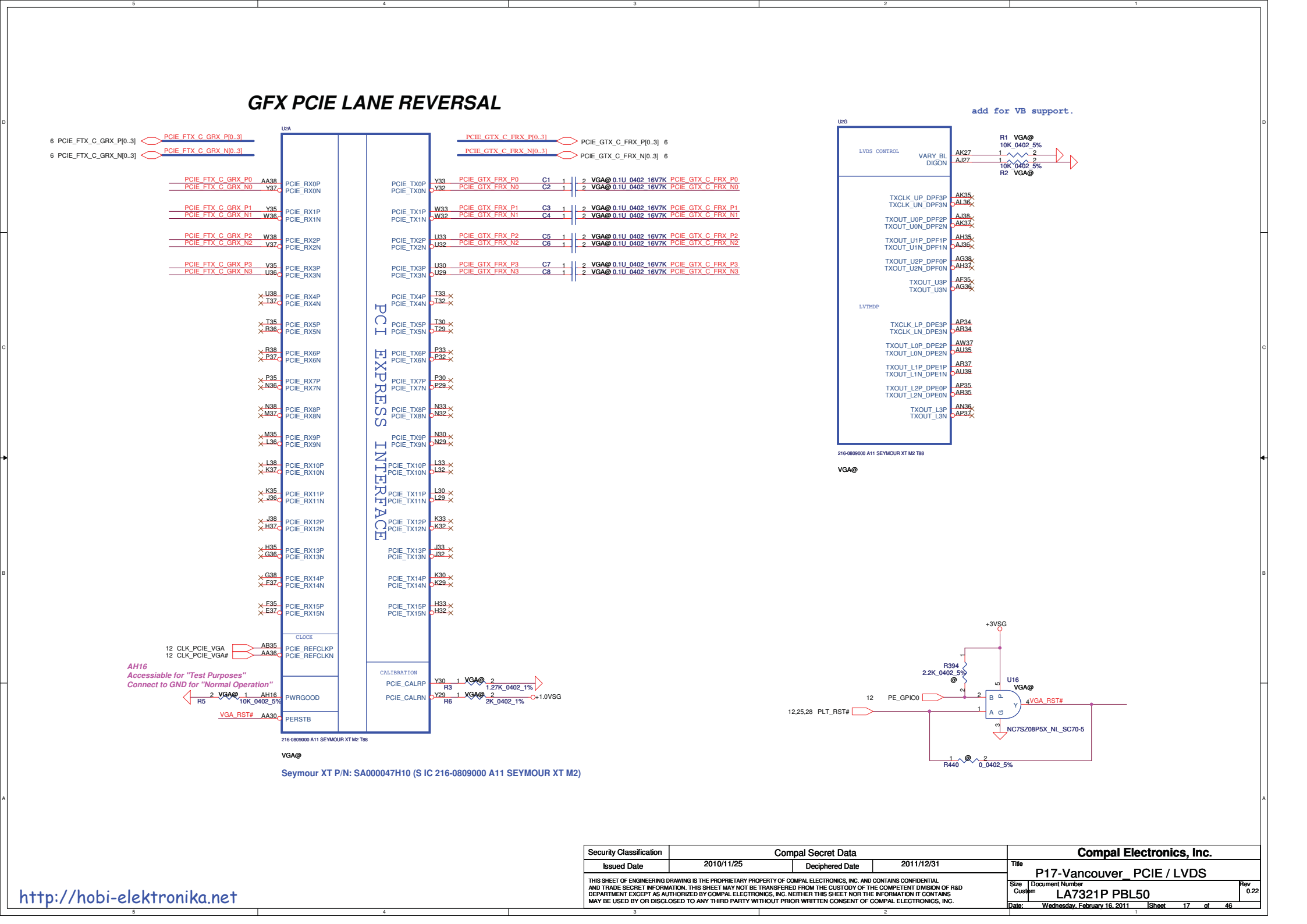
GPIO	189	190	191
UMA	0	0	1
DISO	1	0	1
PX3.0	1	1	1
PX4.0	1	1	0



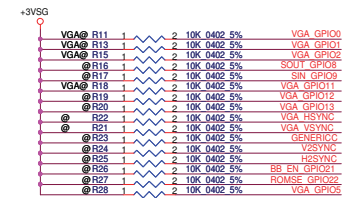


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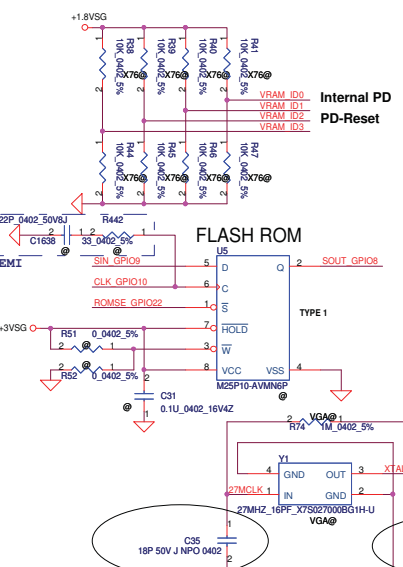


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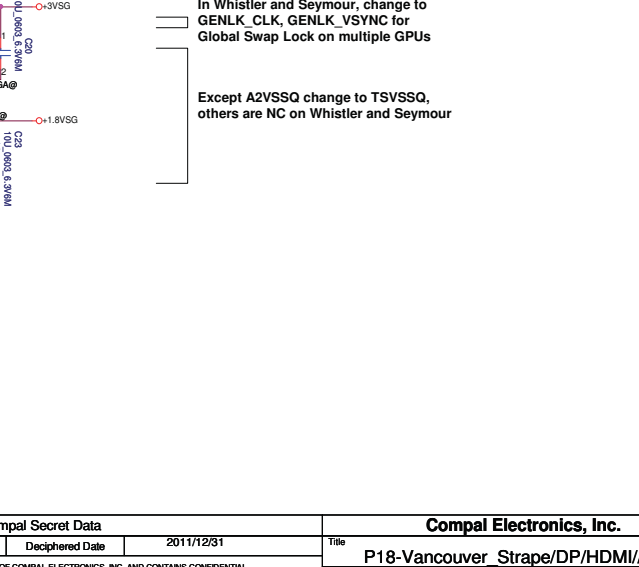
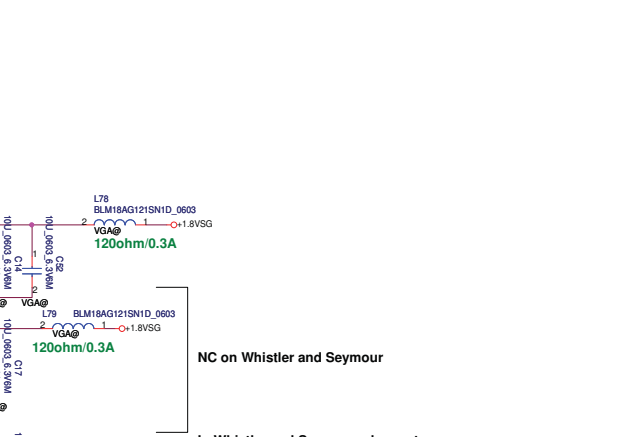
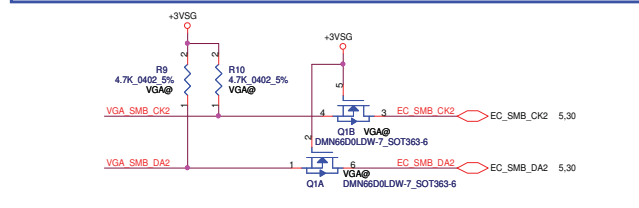
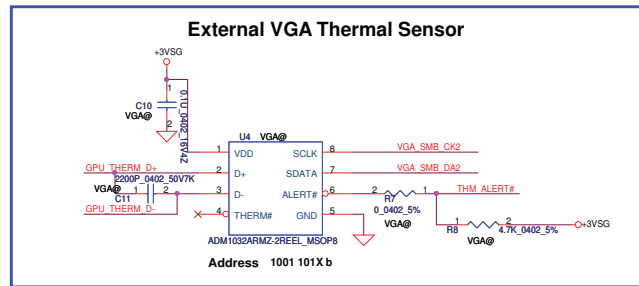
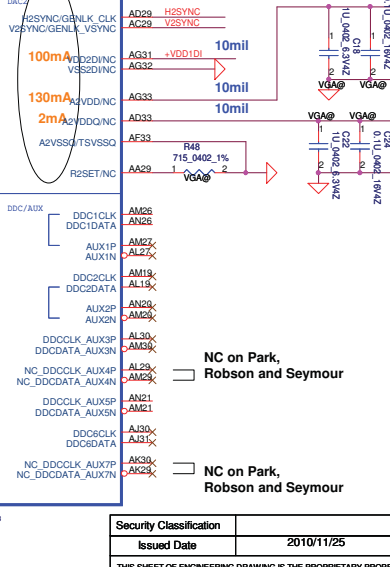
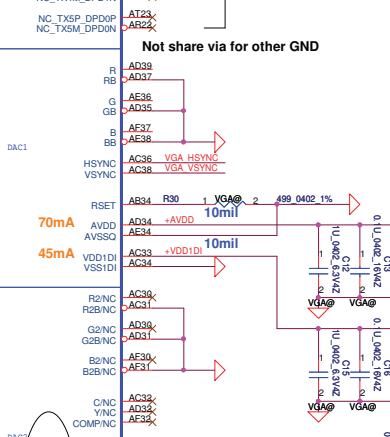
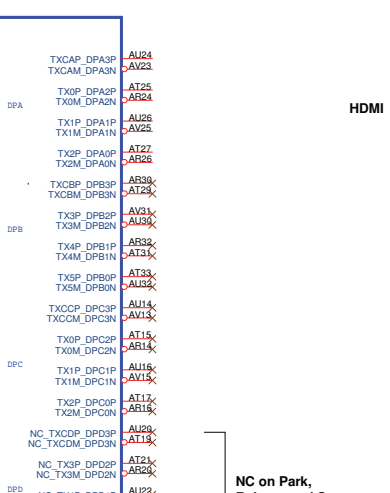
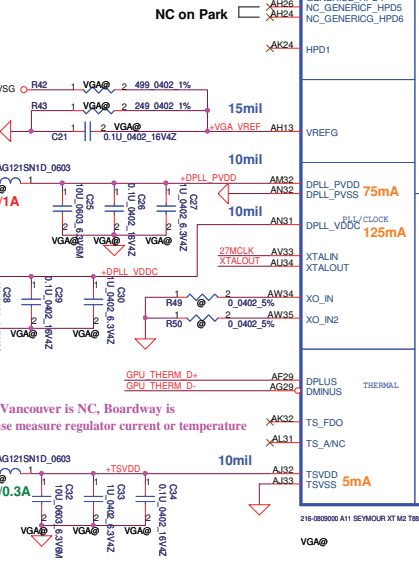
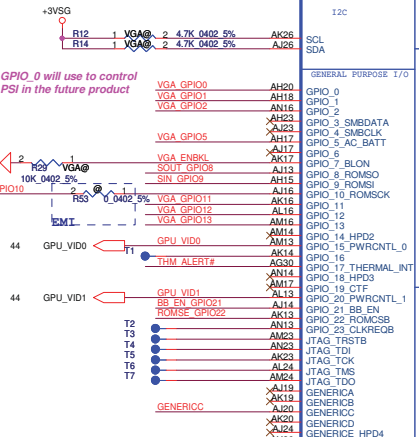
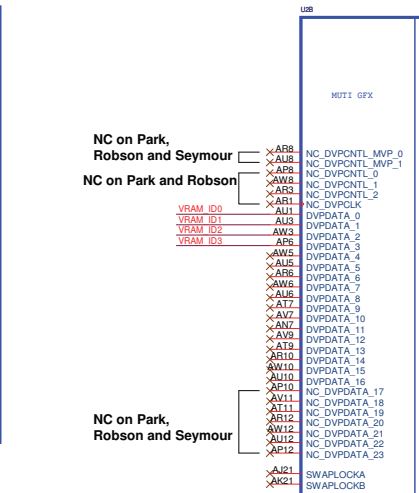
Strap Name	Pin Straps description <all internal PD>	Setting
VGA_DIS	GPIO9 VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0 Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1 PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13,12,11 (config 2,1,0) a) If BIOS_ROM_EN = 1, then Config[3:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22 Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC 00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2 Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	1
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21 GENERICC GPIO5	DNI



VRAM	Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung 1G	X76L01	0	0	0	1
Hynix 1G	X76L02	0	1	0	1
Samsung 512M	X76L03	0	0	0	0
Hynix 512M	X76L04	0	1	0	0

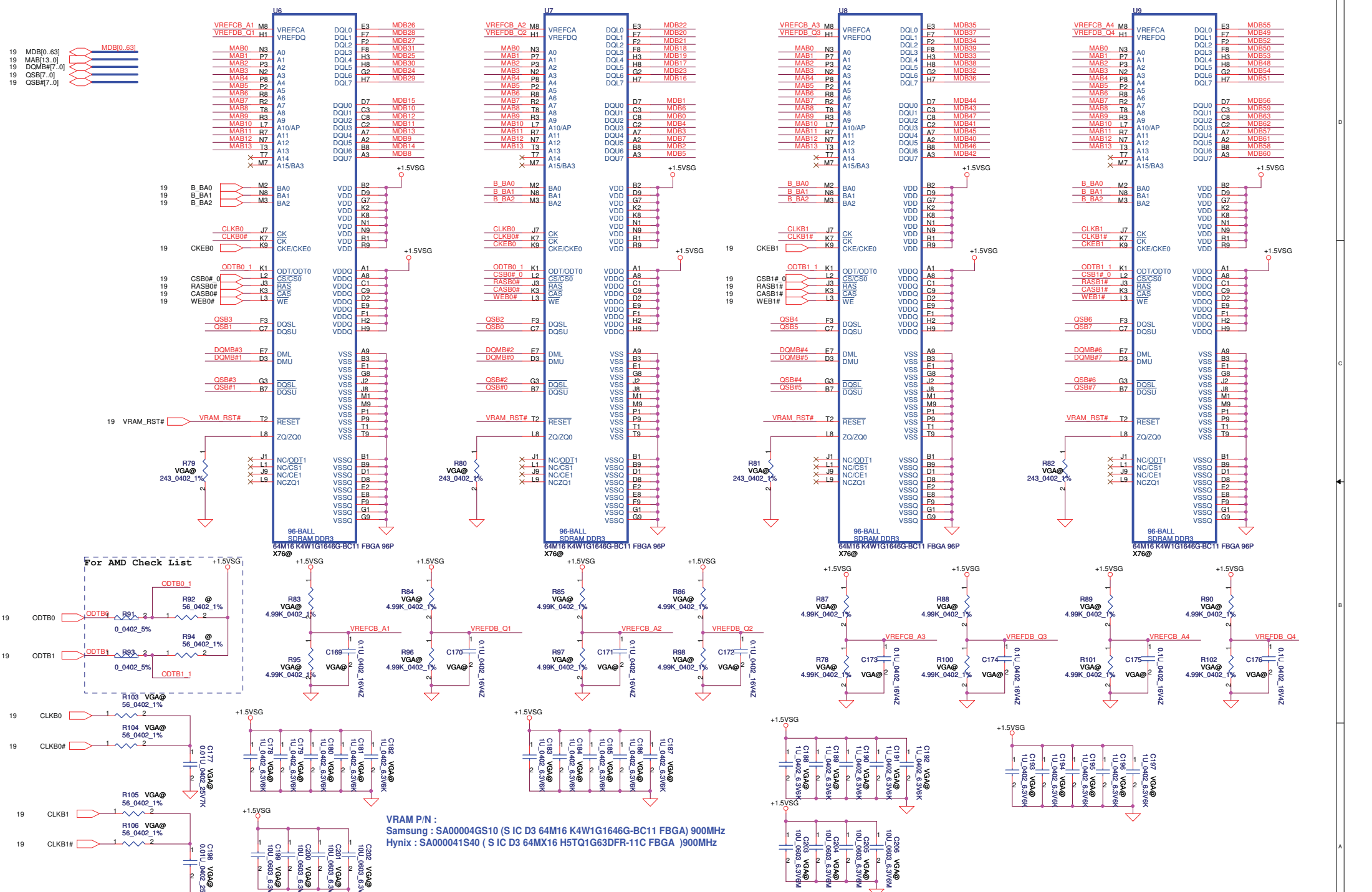


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Size	Custom	Document Number	LA7321P PBL50	Rev	0.22
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Timing diagram showing the relationship between **PE_GPIO1** and **VGA_PWR_ON**. The signal **PE_GPIO1** transitions from high to low, and **VGA_PWR_ON** transitions from low to high. The time interval between the falling edge of **PE_GPIO1** and the rising edge of **VGA_PWR_ON** is labeled as **>1ms**.

SUSP#

+3VSG
(JUMP form +3VS)

VGA_ON

VGA_PWR_ON

1.5_VDDC_PWREN

+VGA_CORE

+1.5VSG

+1.0VSG

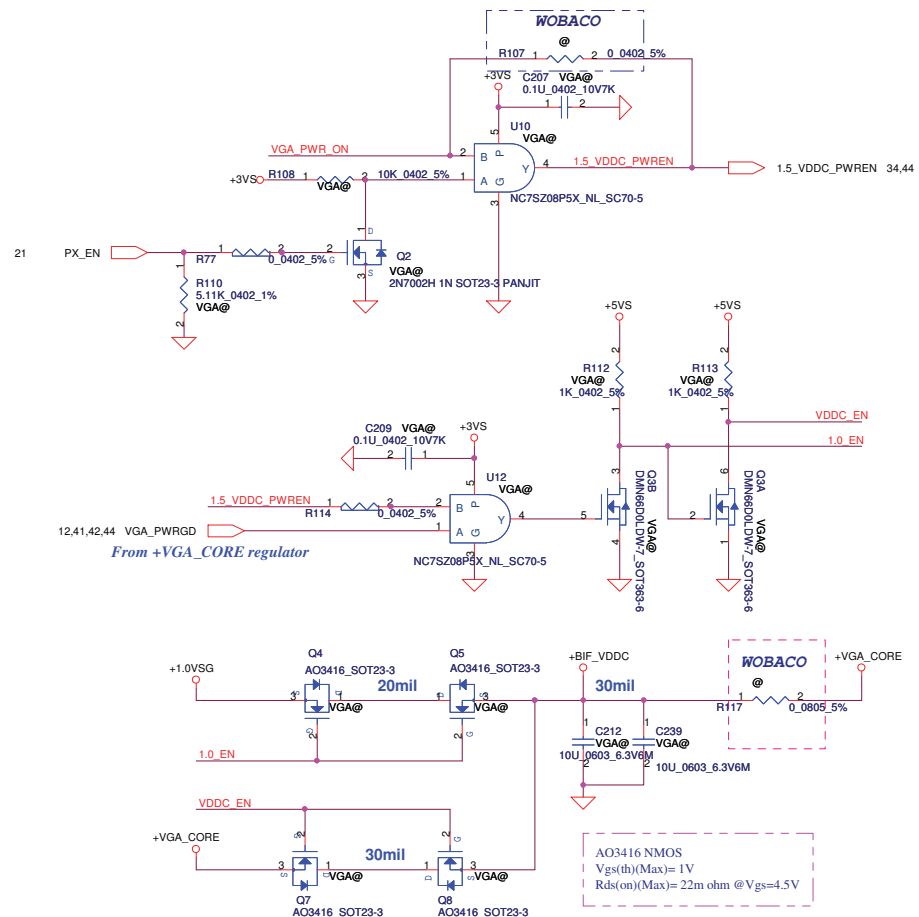
+1.8VSG

10ms

20ms

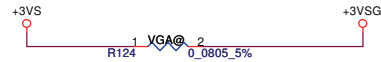
	Normal mode	SBCO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

	Graville	Whistler and Seymour
VGA_PWR_ON source signal	INT_VGAPWR_ON	VGA_ON
+3.3VSG	VGA_PWR_ON	SUSP#
+1.8VSG	VGA_PWR_ON	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON	VGA_PWR_ON
+VDDCI	VGA_PWR_ON	Combine with +VGA_CORE
+VGA_CORE	VGA_PWR_ON	1.5_VDDC_PWREN
+1.5VSG	VGA_PWR_ON	1.5_VDDC_PWREN

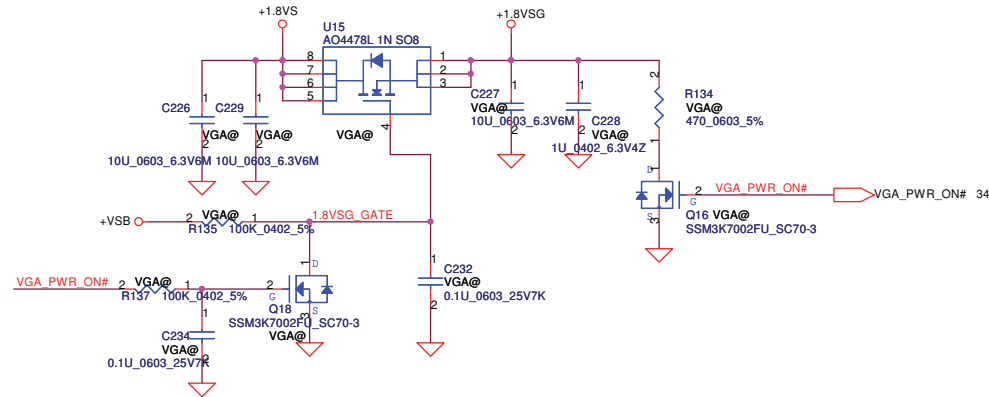


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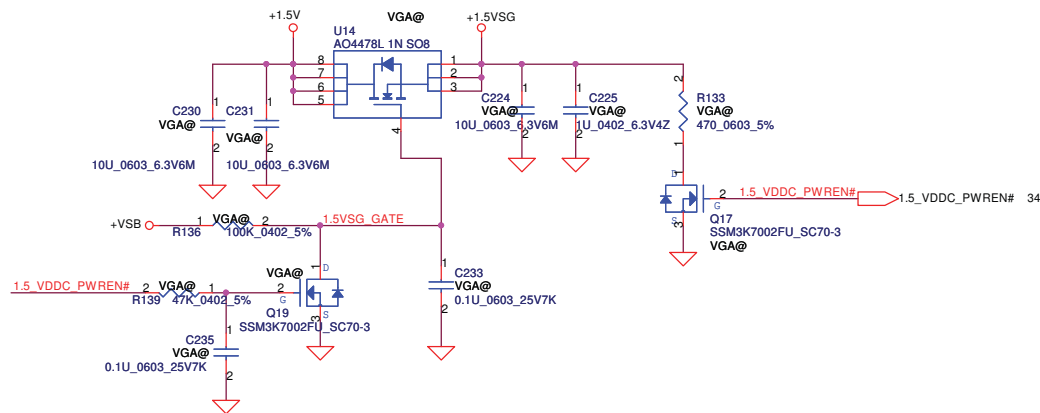
+3.3VS TO +3.3VSG



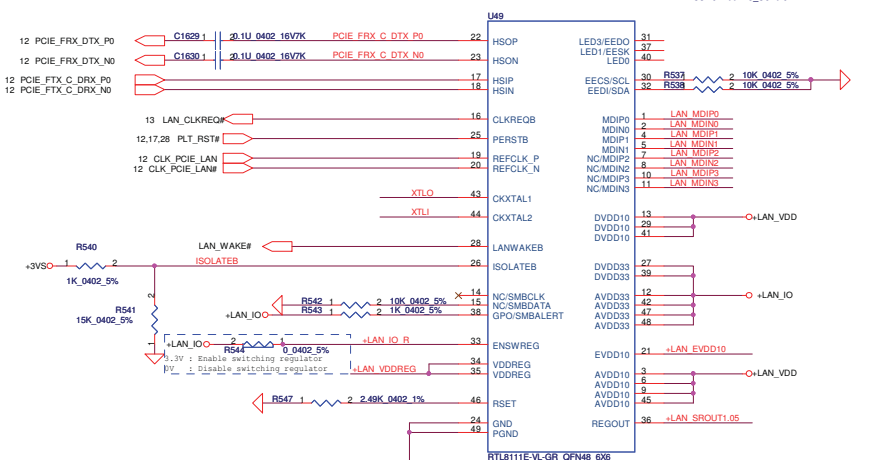
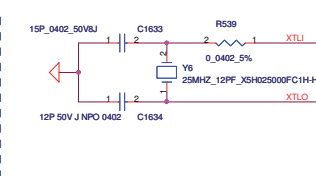
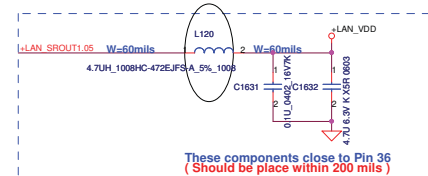
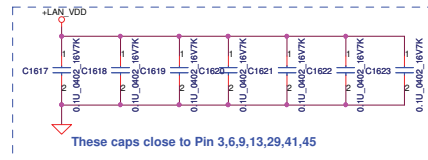
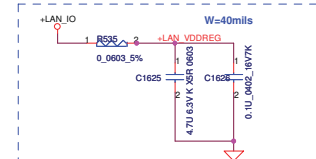
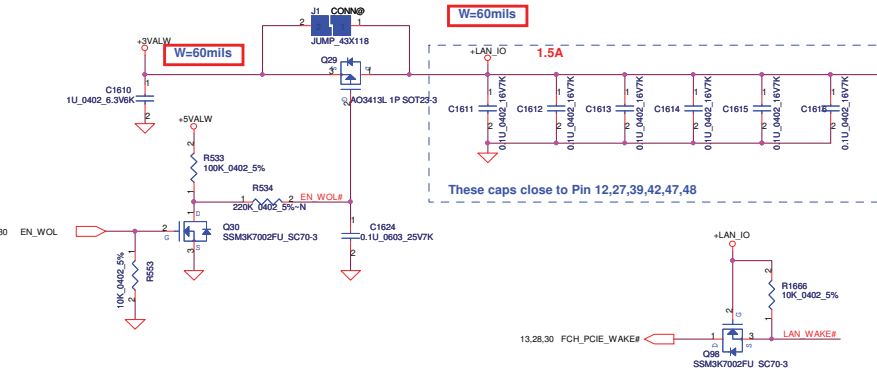
+1.8VS TO +1.8VSG



+1.5V TO +1.5VSG

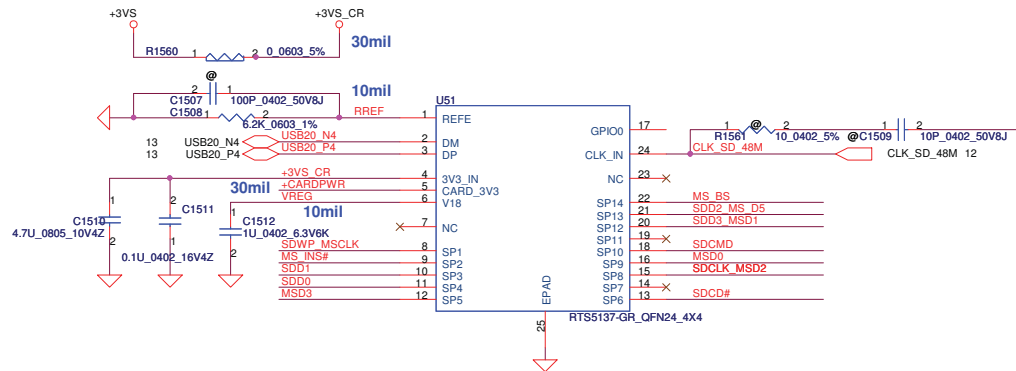


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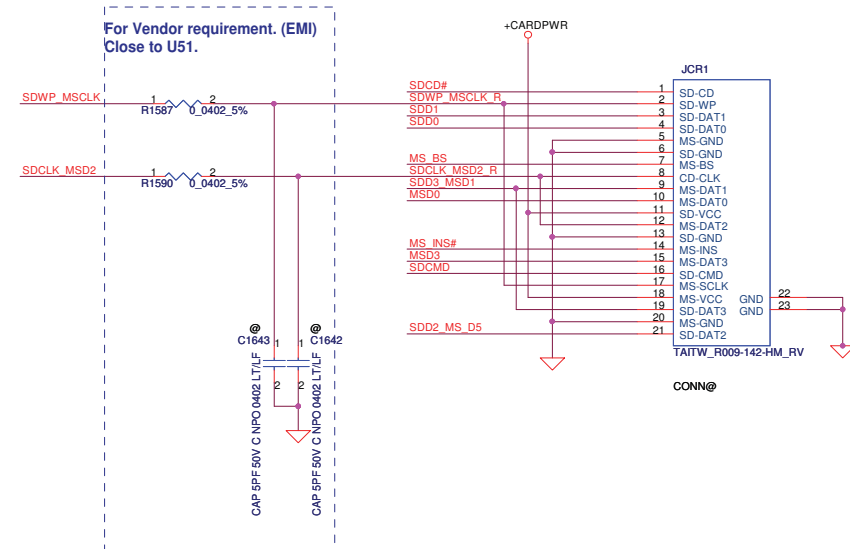
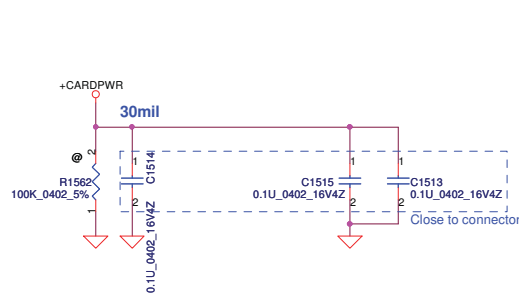




Card Reader RTS5137 (only SD/MMC/MS function)



Card Reader Connector

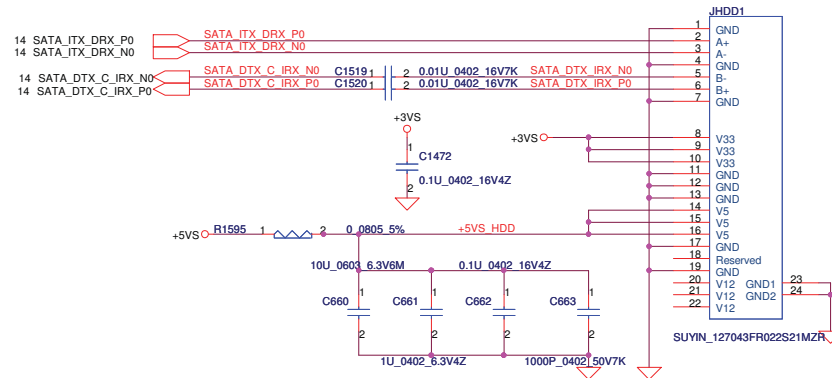


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					Size	Document Number	Rev
					Customer	LA7321P PBL50	0.22
					Date:	Thursday, February 17, 2011	Sheet

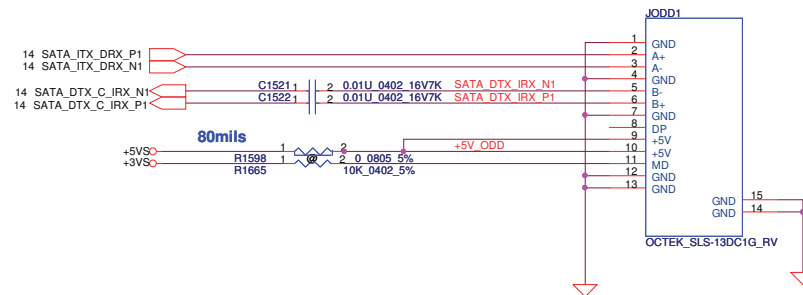
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				Revised	End User: End User: 10/2011
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SATA HDD Conn.

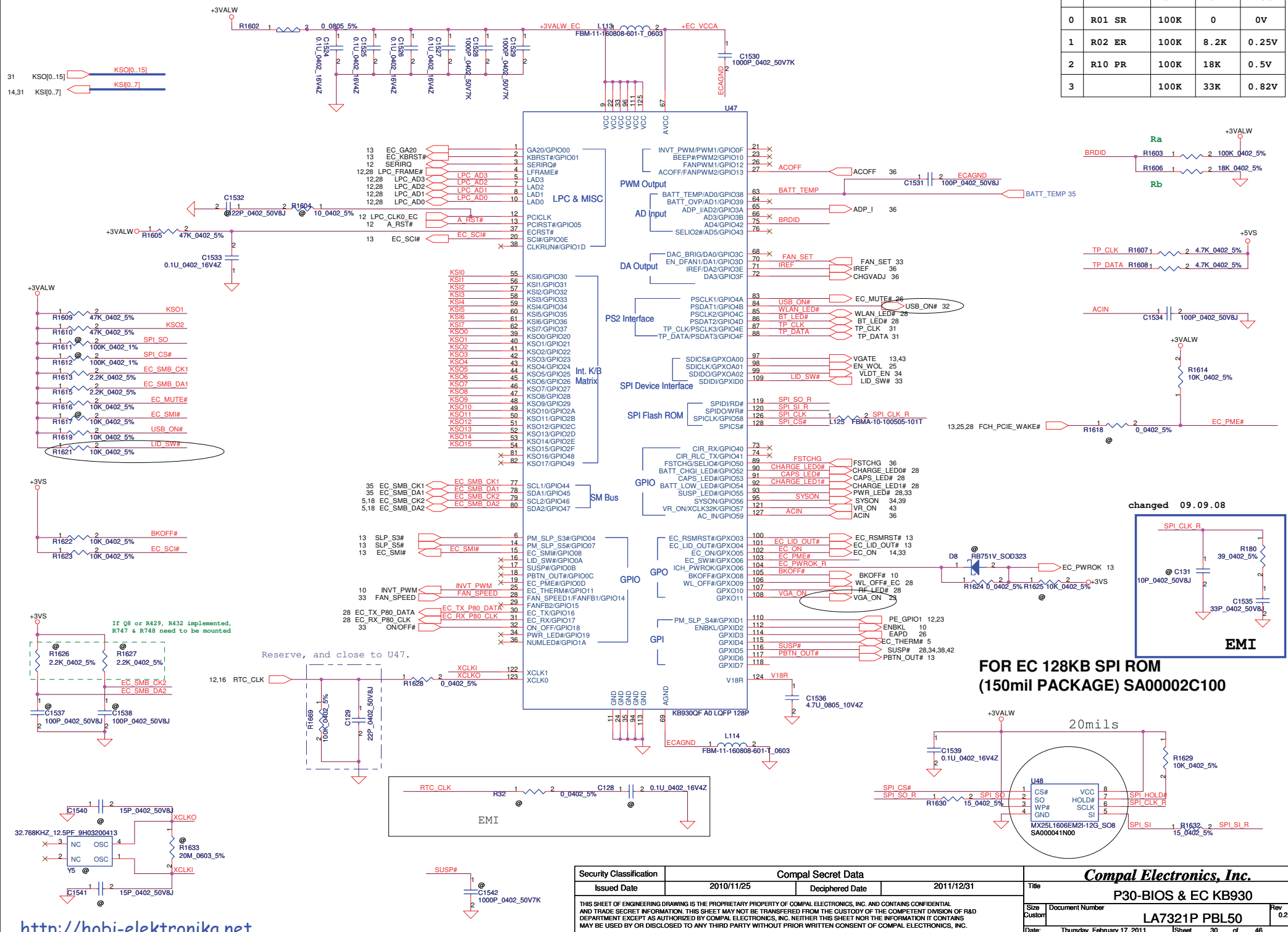


SATA ODD FFC Conn.

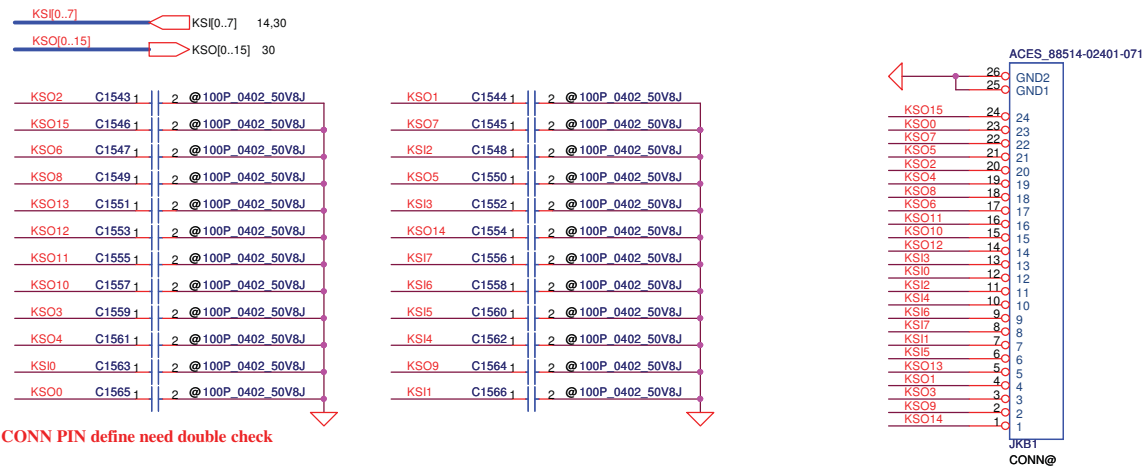


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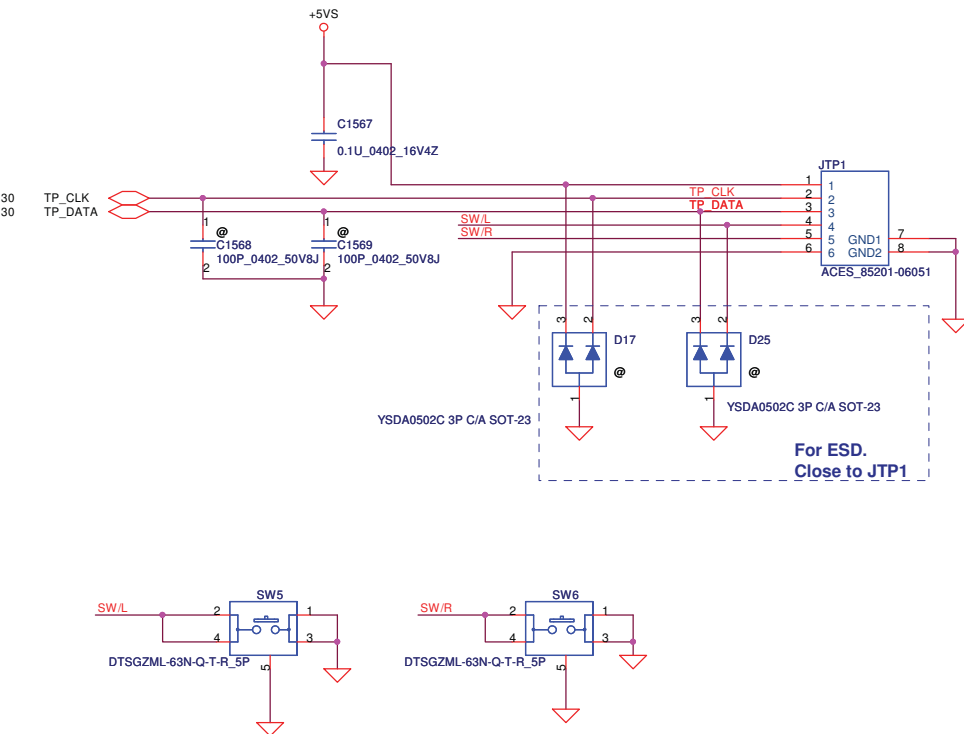
ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R10 PR	100K	18K	0.5V
3		100K	33K	0.82V



INT_KBD Conn.



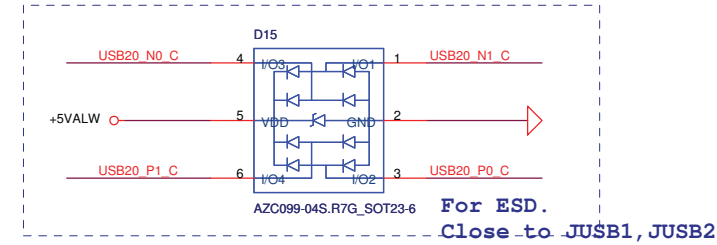
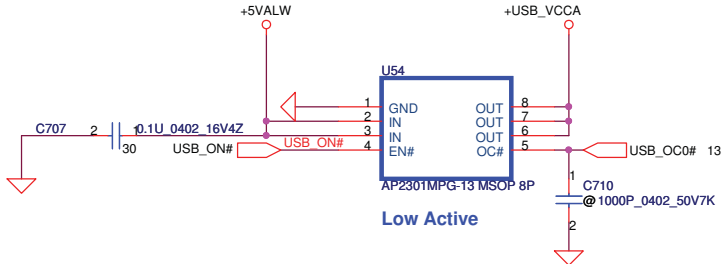
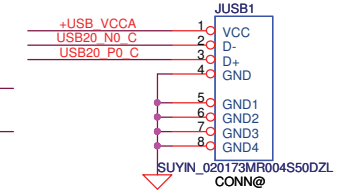
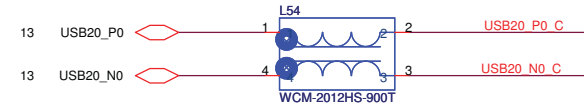
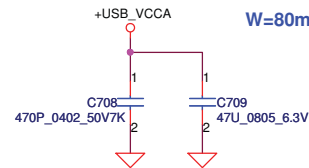
To TP/B Conn.



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Left USB1 Conn.

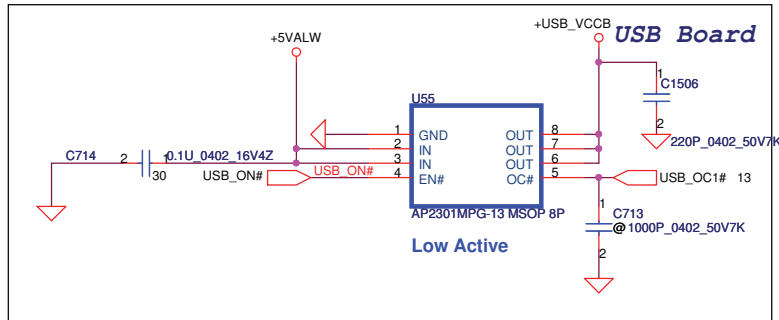
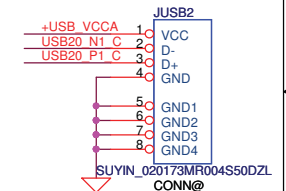
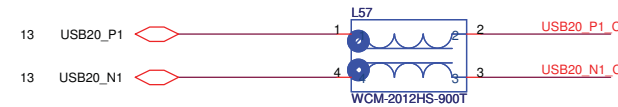
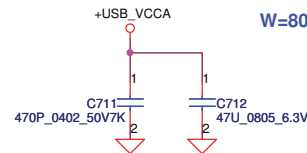
W=80mils



EMI request

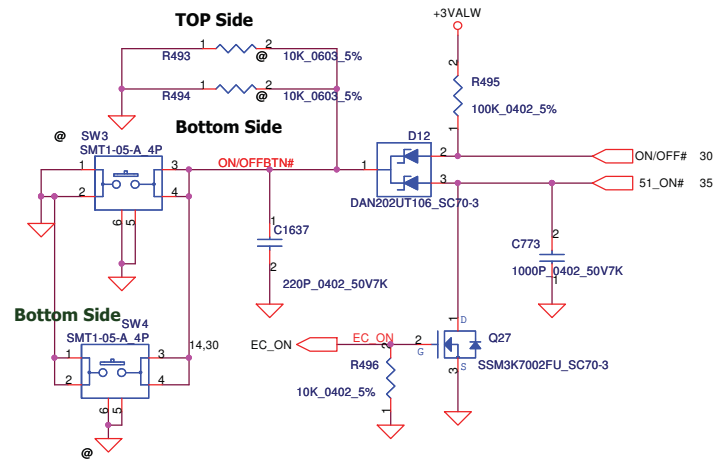
Left USB2 Conn.

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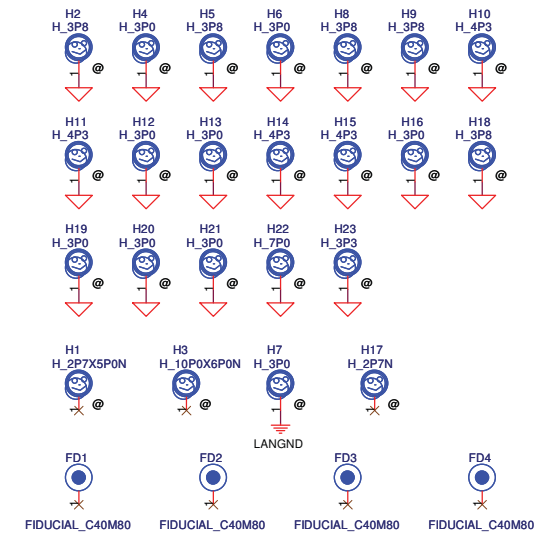
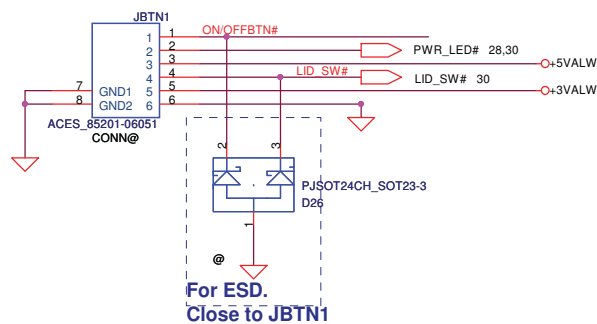
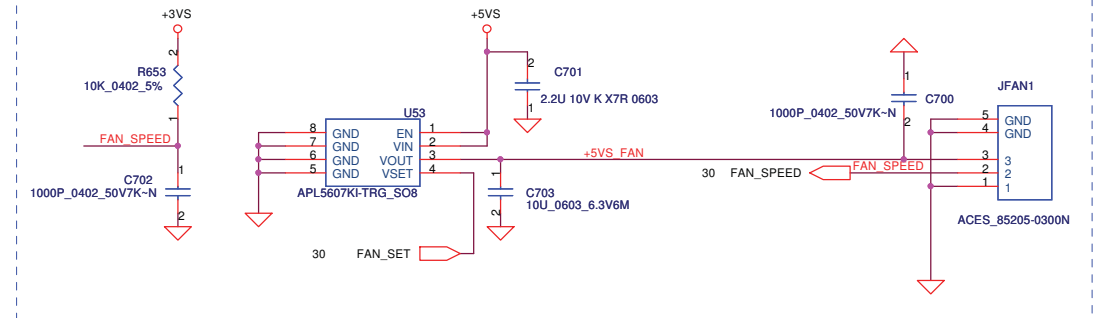


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ON/OFF switch **Power Button**

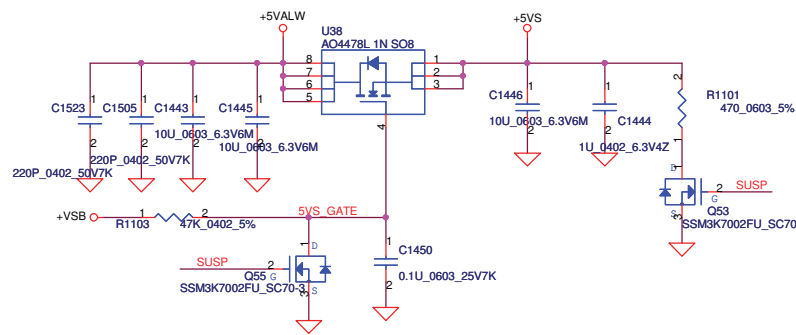


Fan Control Circuit

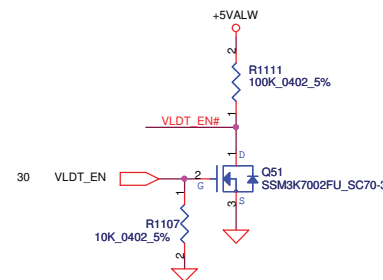
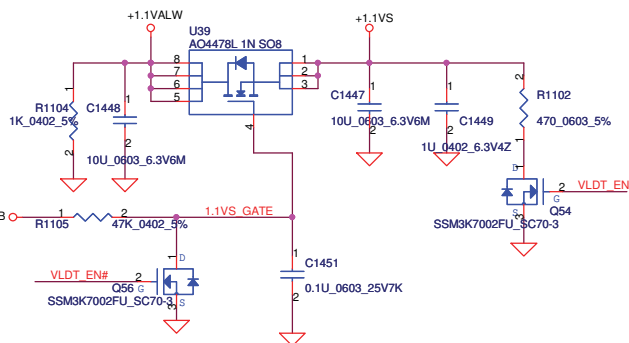


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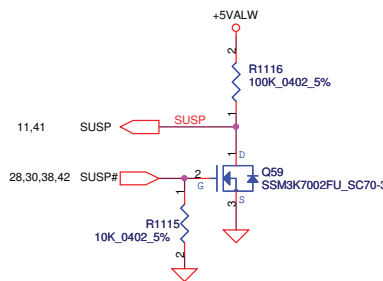
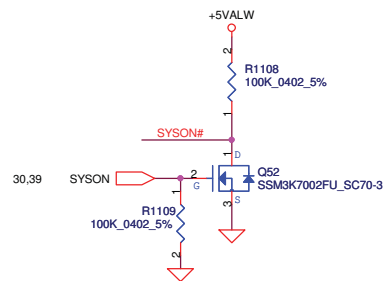
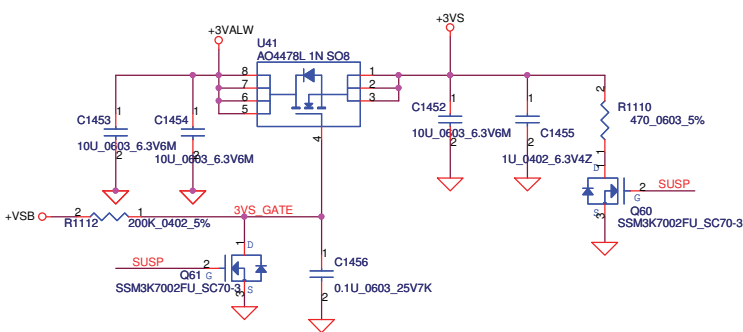
+5VALW TO +5VS



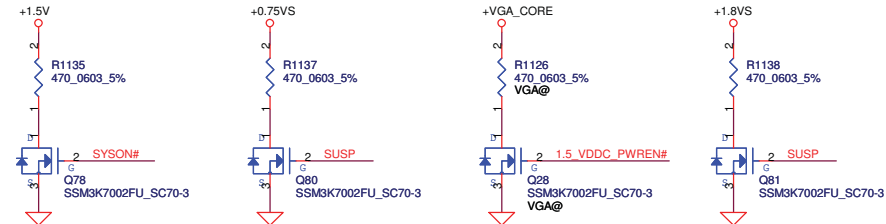
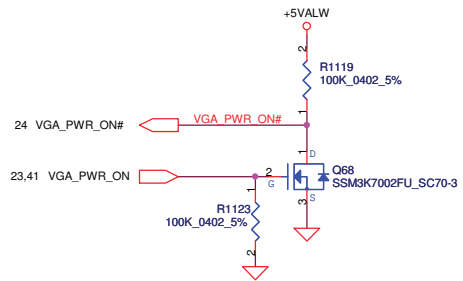
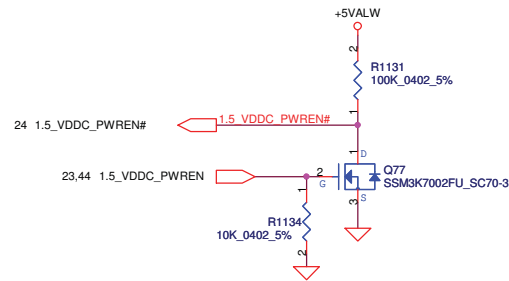
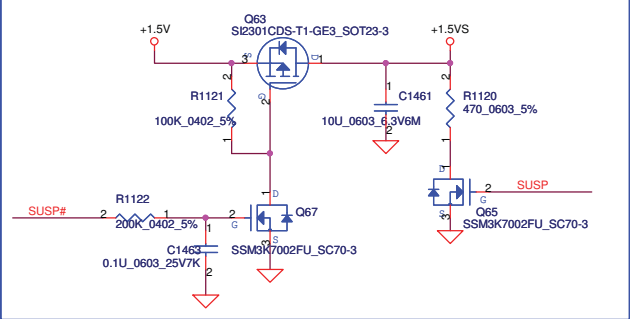
+1.1VALW TO +1.1VS



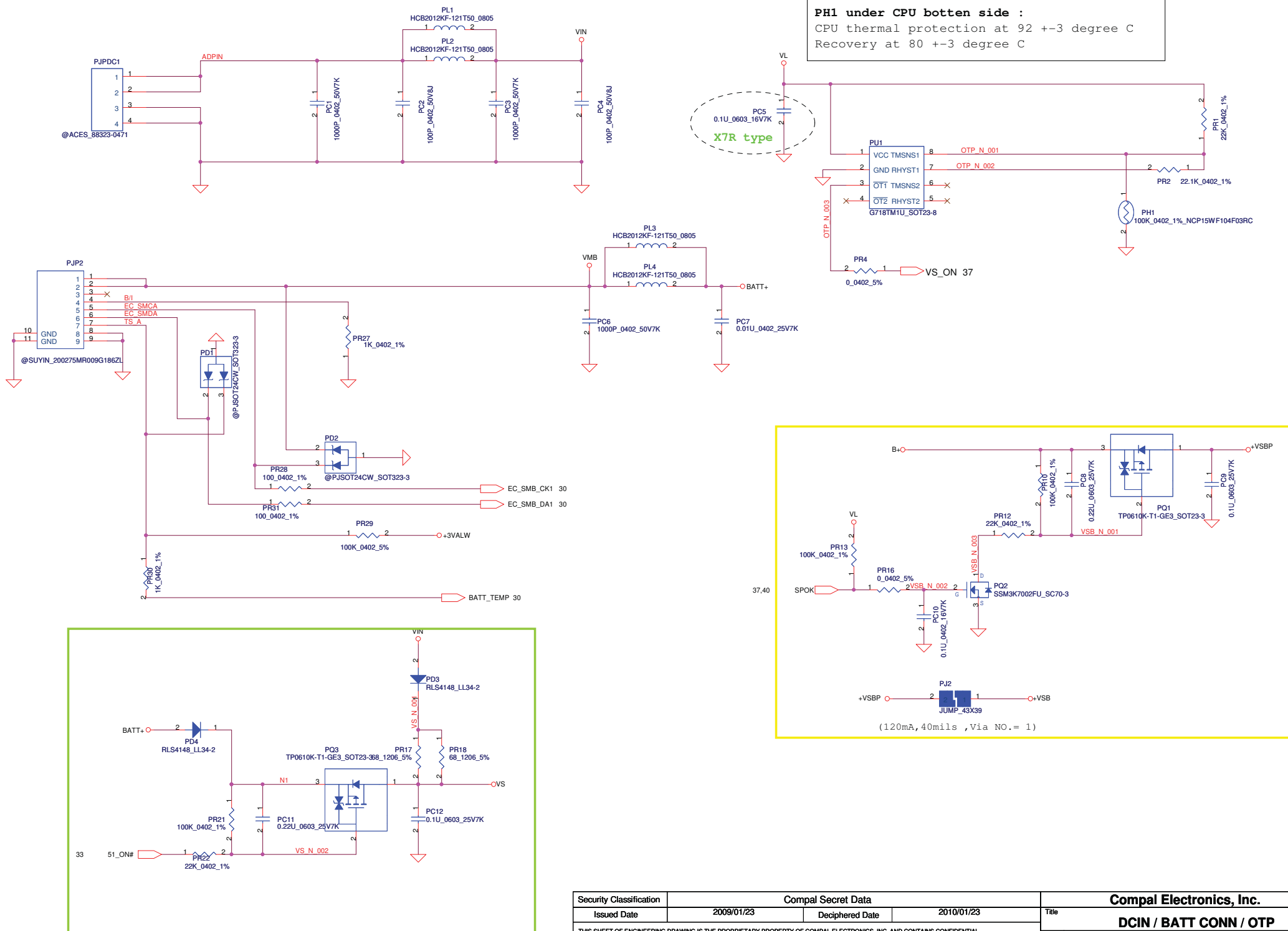
+3VALW TO +3VS

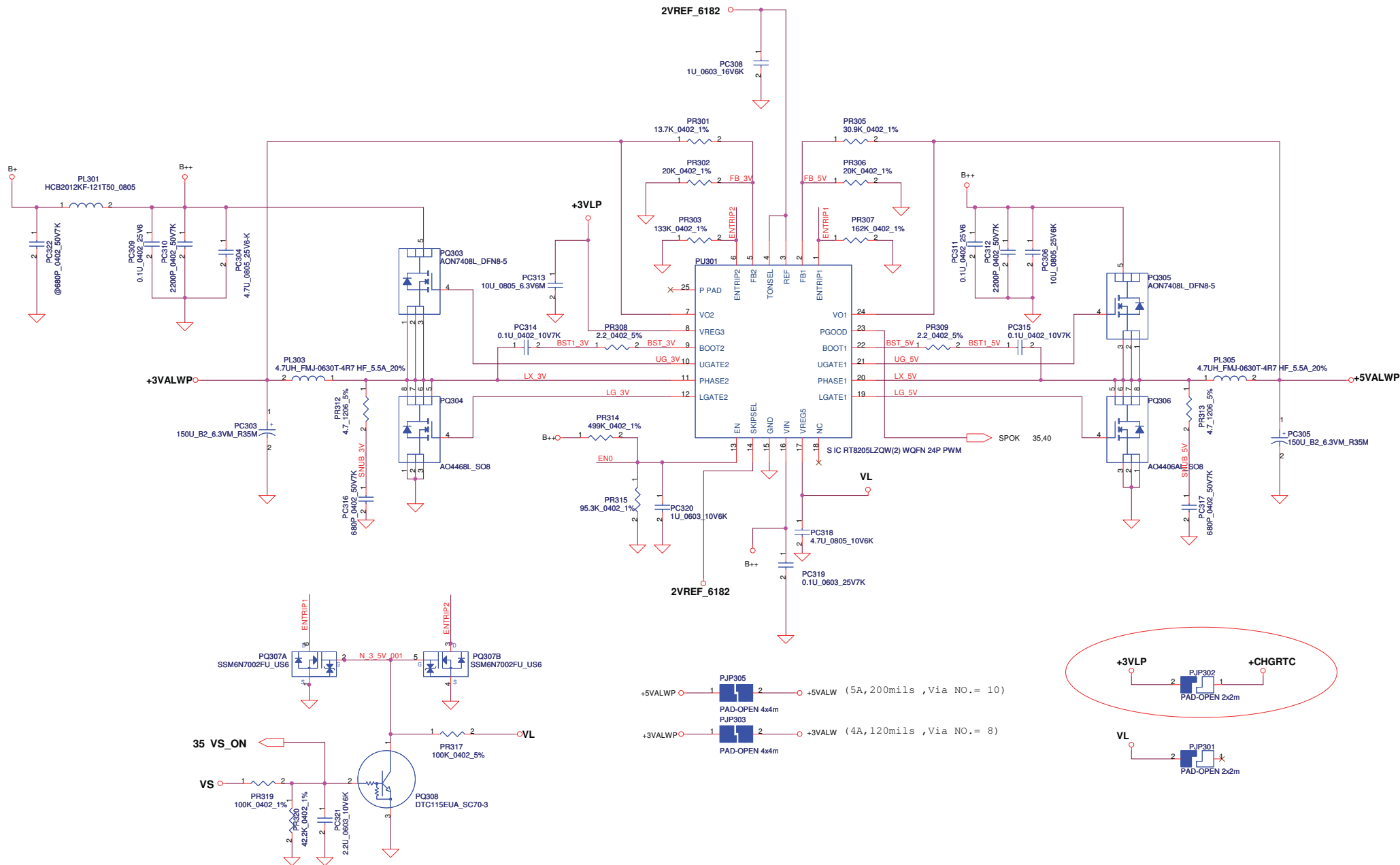


+1.5VS



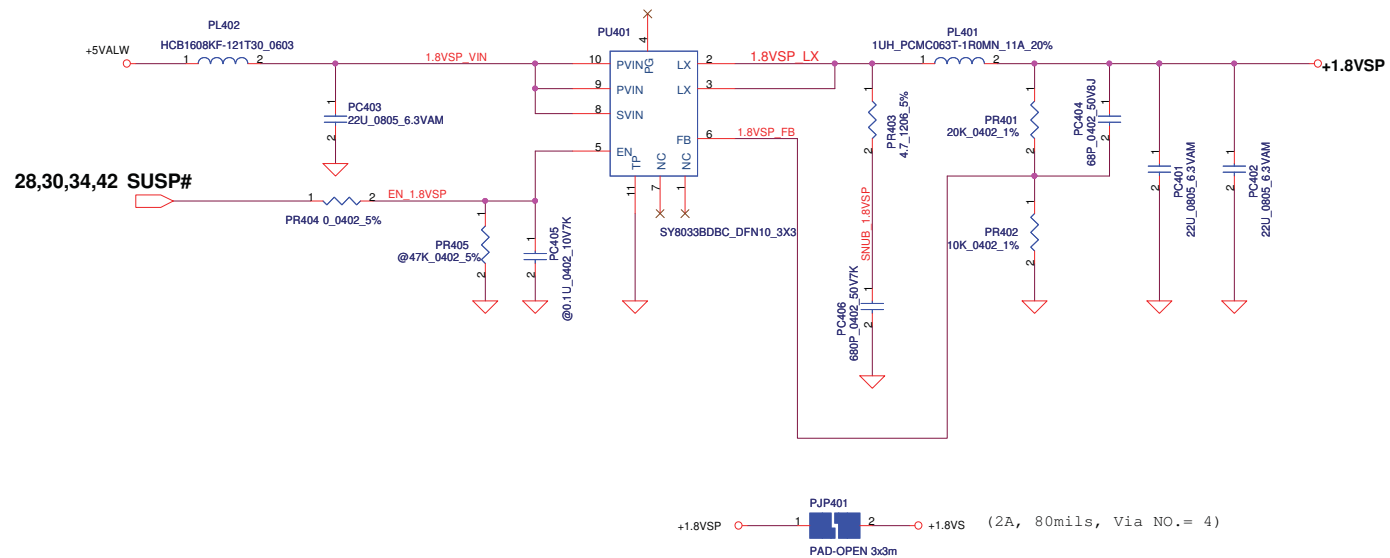
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Issued Date		2010/11/25	Deciphered Date	2011/12/31		Title		
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						Size	Document Number	Rev
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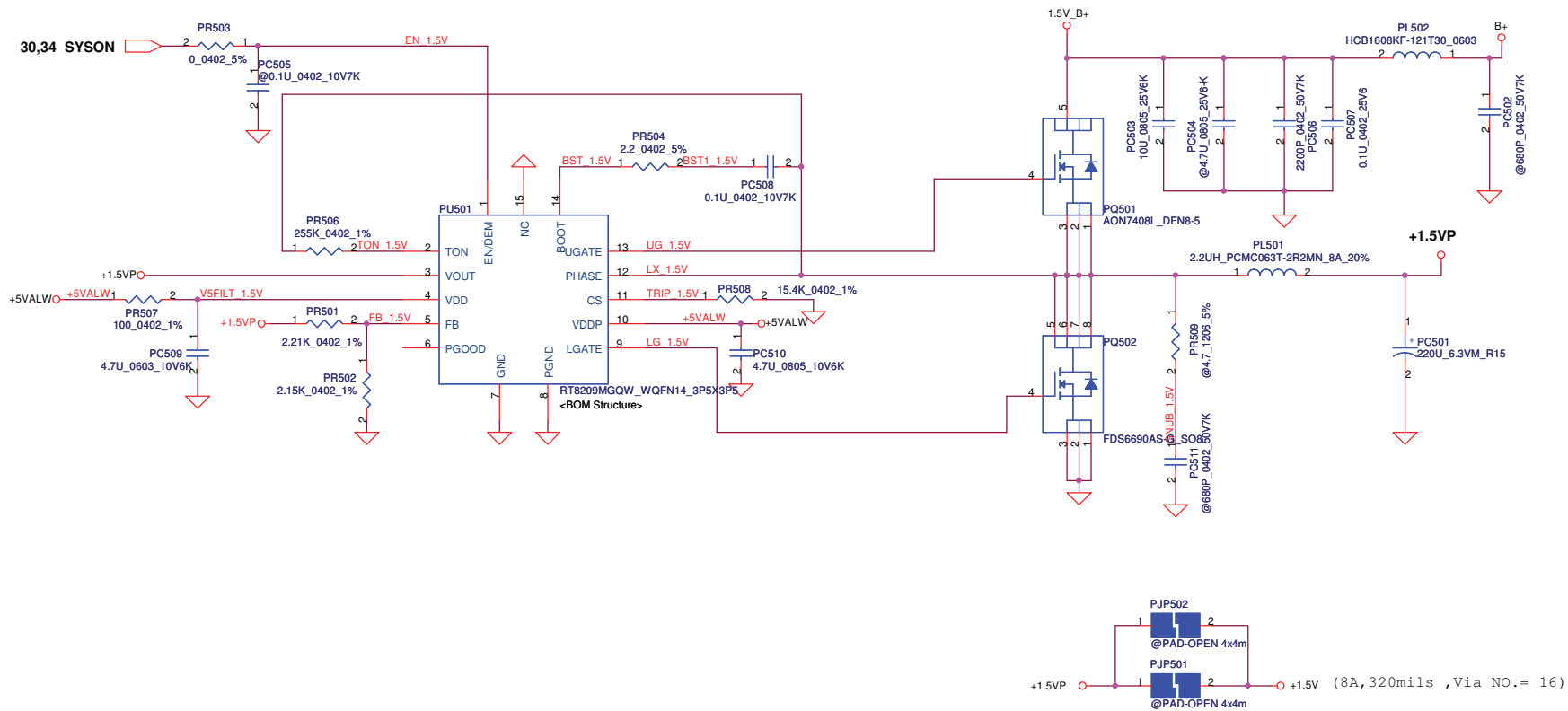
EC:+3VL, reserve PR319, install PR318, PR320 100K
 EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

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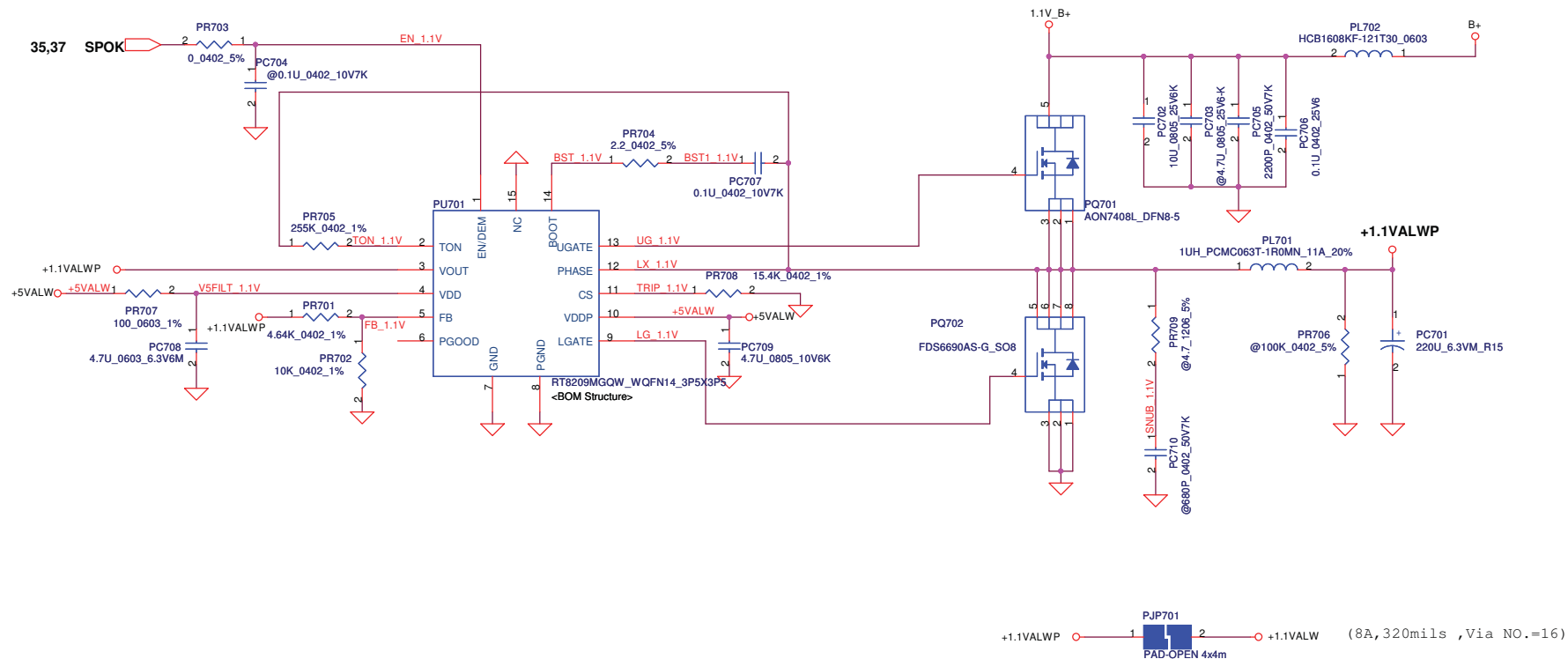


$$\langle V_o = 1.8V \rangle \quad V_{FB} = 0.6V$$

$$V_o = V_{FB} * (1 + PR401 / PR402) = 0.6 * (1 + 20K / 10K) = 1.8V$$



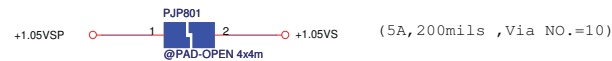
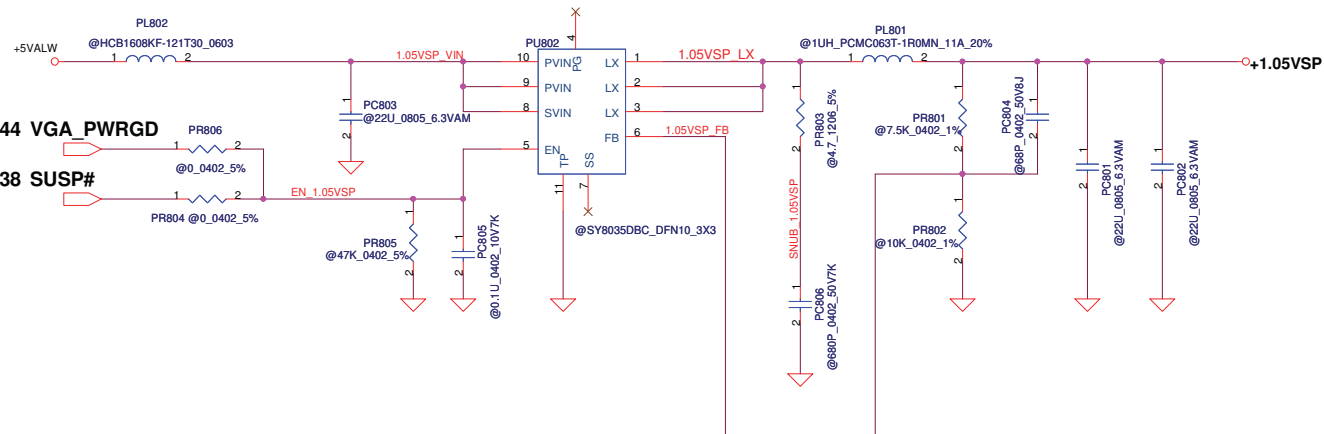
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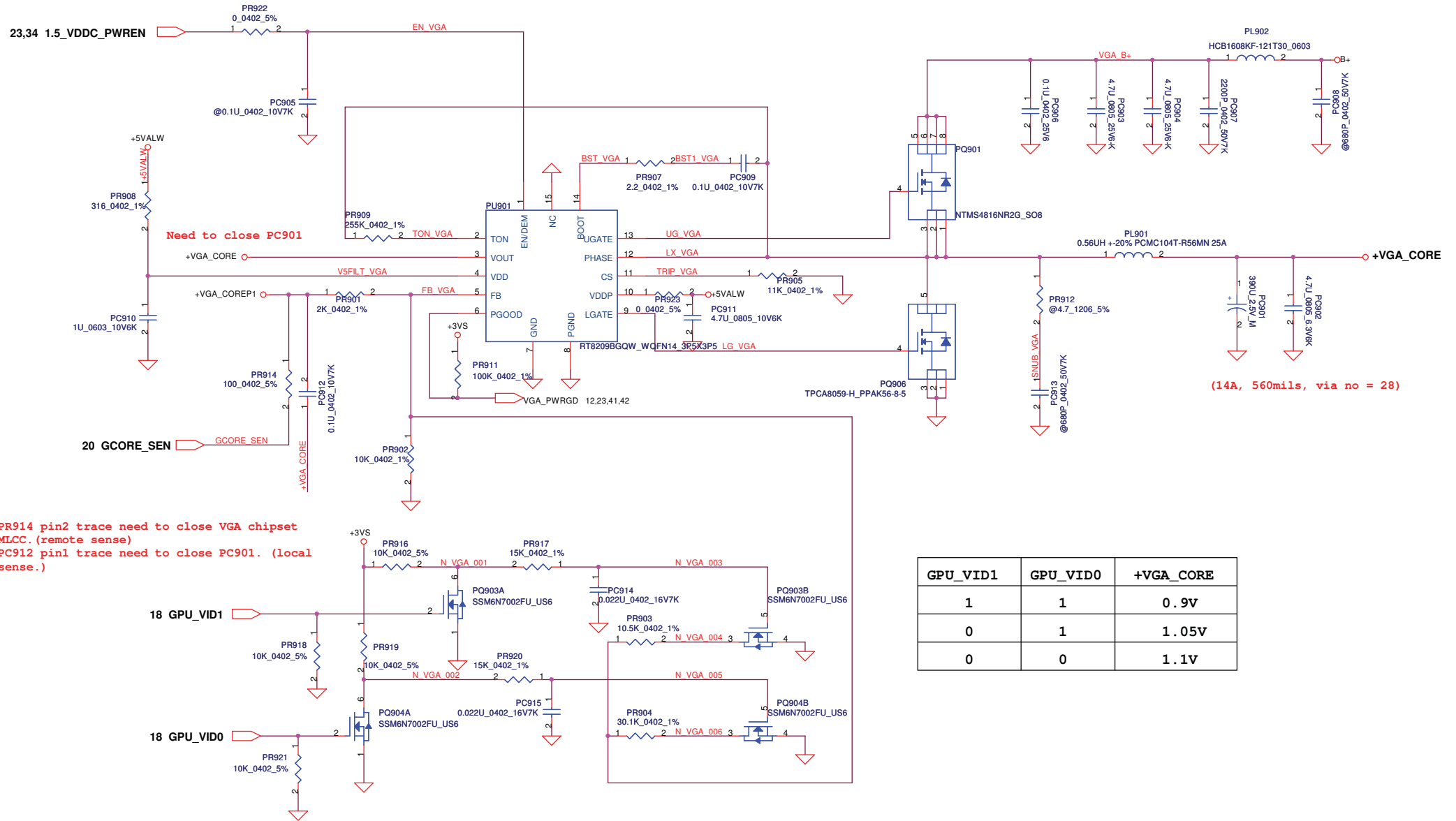
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12,23,41,44 VGA_PWRGD

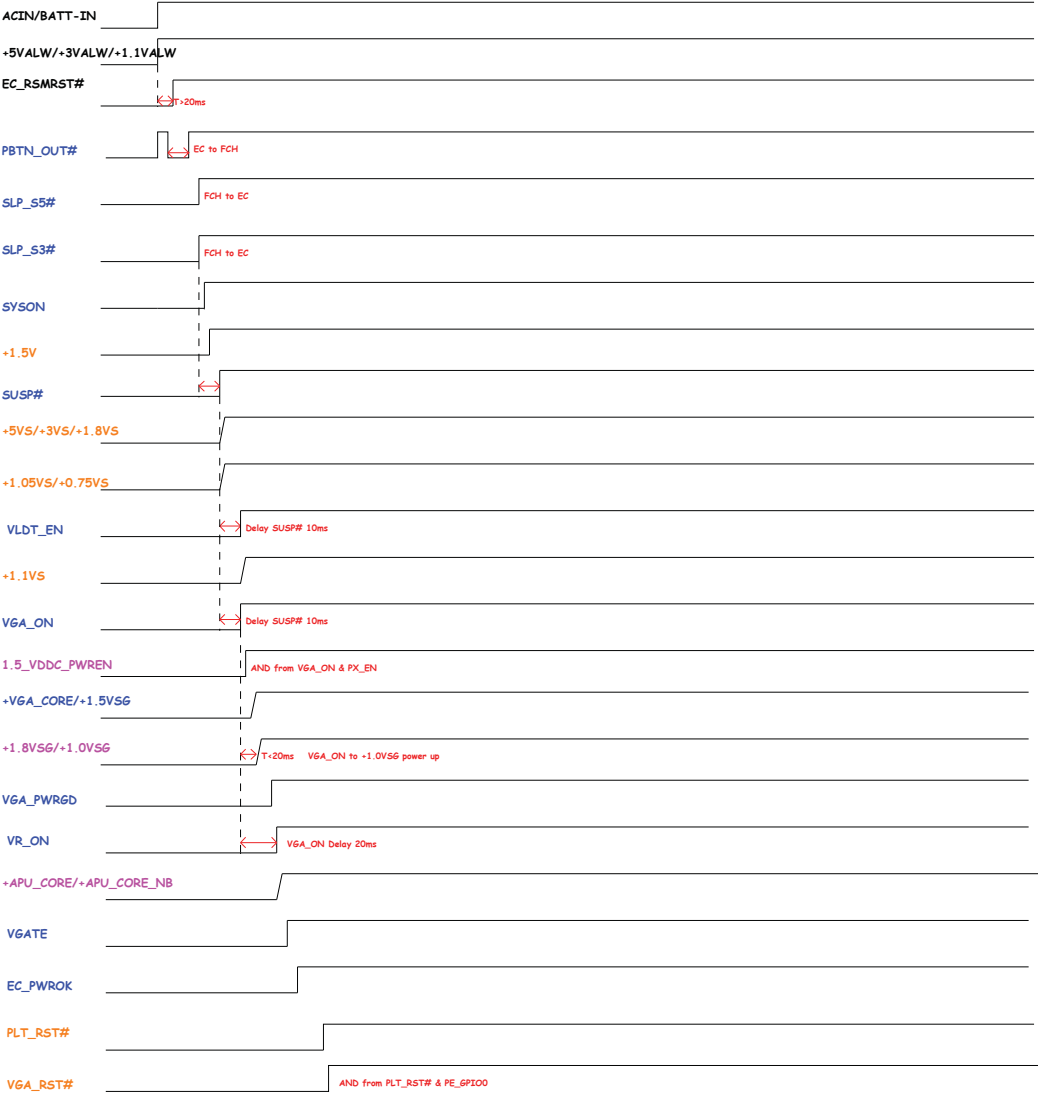
28,30,34,38 SUSP#



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POWER SEQUENCE



Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P30	KB930	2010/12/16	COMPAL	Power button no function.	Add R1621 pull up to +3VALW.	0.12
2	P31	TP button	2010/12/16	COMPAL	SW5,SW6 footprint error	Modify SW5,SW6 symbol.	0.12
3	P33	Fan Connector	2010/12/16	COMPAL	Fan no function.	Modify Fan connector pin define.	0.12
4	P35 ~ P44	Power schematic update	2010/12/16	COMPAL		Power schematic update	0.12
5	P30	KB930	2010/12/17	COMPAL	Modify board ID for ER phase.	Change R1606 from 0 ohm to 8.2K ohm.	0.12
6	P5	FCH THERMTRIP	2010/12/17	COMPAL	Modify BOM structure of thermtrip circuit. For FCH spec.	Change Q79 and R424 to unpop and change R427 to pop.	0.12
7							
8	P30	KB930	2010/12/17	COMPAL	Vendor's recommend for XCLK0 signal.	Add R1669 and C129.	0.12
9	P14	FCH SPI	2010/12/21	COMPAL	Add U11 circuit for flash BIOS crisis circuit.	Add U11 circuit.	0.12
10	P8	DDR3 80-DIMM1	2010/12/21	COMPAL	Reserve R155,R152 for DDR3 DIMM1. (SA)		0.12
11	P33	Screw hole	2010/12/22	COMPAL	Thermal issue, modify H22.	Modify H22 to 7.0.	0.13
12	P35 ~ P44	Power schematic update	2010/12/22	COMPAL		Power schematic update	0.13
13	P12	FCH RTC	2010/12/23	COMPAL	Customer requirement for clear CMOS	Change R865 to Jump.	0.13
14	P28	WLAN & LED	2010/12/23	COMPAL	For ESD solution on LED.	Add C1644-C1648.	0.13
15	P26	Audio Codec	2010/12/24	COMPAL	For EMI solution on DMIC CLK.	Change R1544 to L124.	0.13
16	P30	KB930	2010/12/24	COMPAL	For EMI solution on SPI CLK.	Change R1631 to L125 and pop R180 and C1535.	0.13
17	P14	FCH SPI	2010/12/24	COMPAL		Modify Crisis circuit.	0.13
18	P10	CRT	2010/12/24	COMPAL	For ESD solution on CRT.	Pop D1,D2,D16,D18	0.13
19	P35 ~ P44	Power schematic update	2010/12/24	COMPAL		Power schematic update	0.13
20	P25	LAN	2010/12/24	COMPAL		Reserve J1 jump for LAN power.	0.13
21	P14	FCH SPI	2010/12/25	COMPAL	For EMI requirement.	Reserve R181,C130 close to U32.	0.13
22	P25	LAN	2010/12/27	COMPAL	For LAN power discharge.	Add R1113,Q62.	0.13
23	P25	LAN	2010/12/27	COMPAL	Prevent LAN wake up signal fo floating.	Add R553 pull down to GND.	0.13
24	P25	LAN	2010/12/27	COMPAL	For ESD requirement.	Change R549,R1529,R1530,R552 to 0603 size.	0.13
25	P34	DC to DC	2010/12/27	COMPAL	For Power sequence.	Change R1103 from 100K to 47K.	0.13
26	P11	HDMI	2010/12/28	COMPAL	For EMI requirement.	Modify L11-L14 circuit and remove un-LS circuit.	0.13
27	P12,18,25	Crystal	2010/12/29	COMPAL	For Vendor recommend.	Modify C35,C66,C67,C1633,C1634.	0.2
28	P26	Audio Codec	2010/12/30	COMPAL	For EMI Requirement.	Unpop R1556,R1557,R1558,R1559.	0.2
29	P30	KB930	2010/12/31	COMPAL	Change ROM footprint.	Change U48 footprint.	0.2
30	P16	FCH Strap	2010/12/31	COMPAL	Change FCH Strap for SPI-ROM	Pop R594,R602; Unpop R601,R550.	0.2
31	P18	Seymour Strap	2011/01/10	COMPAL	For AMD requirement.	Unpop R21,R22.	0.21
32	P34	DC to DC	2011/01/11	COMPAL	For +1.8VS discharge issue.	Add Q81,R1138.	0.21
33	P13	FCH HDA/USB/ACPI	2011/02/11	COMPAL	For RSMRST pluse issue	Change R606 from 2.2k ohm to 150 ohm	0.22
34	P30	EC	2011/02/11	COMPAL	For MB Board ID	Change R1606 to 18K	0.22
35	P10	CRT	2011/02/11	COMPAL	For CRT EA AND EMI	Change L116, L117, L118 TO 80 ohm	0.22
36	P25	LAN	2011/02/11	COMPAL	For EMI request	Change D36, D37, D38, D39 footprint	0.22
37	P18	VGA	2011/02/15	COMPAL	For S3 can't resume issue	ADD R74 (1M ohm) on Y1's cap	0.22
38	P25	LAN	2011/02/15	COMPAL	Follow vendor recommend to change Crystal's cap value	Change C1633 to 15P, C1634 to 12P	0.22
39	P30	EC	2011/02/16	COMPAL	For EMI requirement	Change R180 to 39 ohm, C1535 to 33P	0.23
40	P25	LAN	2011/02/16	COMPAL	For EMI requirement	Change T51 to IH-160	0.23
41	P26	AUDIO	2011/02/17	COMPAL	For EMI requirement	Change R1556, R1557, R1558, R1559 to 0.1u caps	0.23
42	P34	DC-DC	2011/02/17	COMPAL	For EMI requirement	ADD C1505, C1523 on +5VALW	0.23
43	P32	USB	2011/02/17	COMPAL	For EMI requirement	ADD C1506 on +USB_VCCB	0.23
44	P33	PWRBTN	2011/02/17	COMPAL	For EMI requirement	ADD C1603 on ON/OFFBTN#	0.23
45	P25	LAN	2011/02/18	COMPAL	For EMI requirement	Stuff R546, R548	0.23
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