Compal Confidential

PBL22 MB Schematic Document

LA-7391P

Rev: 0.2

2011.04.07

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: ***Cover Sheet***

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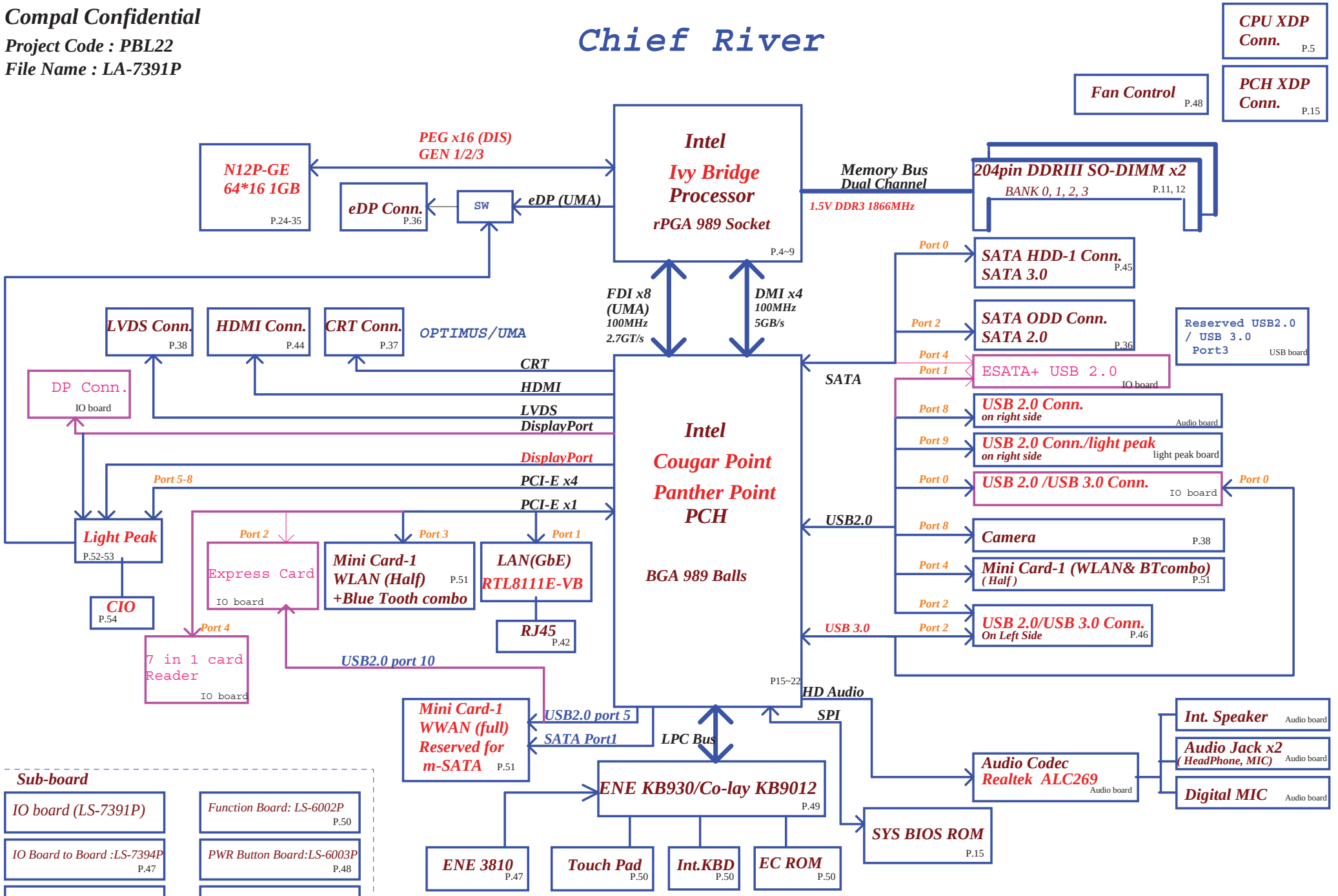
Project Code : PBL22

File Name : LA-7391P

Chief River



Sub-board

IO board (LS-7391P)	Function Board: LS-6002P P.50
IO Board to Board :LS-7394P P.47	PWR Button Board:LS-6003P P.48
Audio Board : LS-7392P USB (Port,11) P.46	USB Board : LS7395P P.46
Light Peak Board : LS-7393P USB (Port,10) P.46	FPC Cable : LF7391P P.46

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Compal Electronics, Inc.			
Title: Chief River-Block Diagram			
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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.168V	0.250 V	0.362 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SMBUS Control Table

	SOURCE	MIINI1	BATT	MINI2	EXPRESS CARD	SODIMM	DGPU Internal Thermal sensor	JXDP1 JXDP2
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	X	X	X	V	X
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	V	V	V	X	V
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	X	X	V	X

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	Debug Port
PCI3	LPC Debug Port
PCI4	None

	USB PORT#	DESTINATION
PCH	0	USB2/3 (Ext Right Side Up)
	1	ESATA (Ext Right Side Up)
	2	USB2/3 (Ext Left Side Down)
	3	USB2/3 (Ext FPC board)
	4	JMINI1 (WLAN) Bluetooth
	5	JMINI2 (WWAN)
	6	None
	7	None
	8	CAMERA
	9	JUSB3 (Ext Right Side Down)
	10	EXPRESS CARD
	11	JUSB4 (Ext Right Side Down)
	12	None
	13	None

UMA: UMA@/XDP@/UO@
OPTIMUS: XDP@/D@/UO@
DISCRETE:XDP@D@/DIS@

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD-1 WLAN	CLKOUTFLEX1	CLK_14M
	CLKOUT_PCIE2	EXPRESS CARD	CLKOUTFLEX2	27M_CLK
	CLKOUT_PCIE3	CARD READER	CLKOUTFLEX3	27M_SSC
	CLKOUT_PCIE4	Light Peak		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

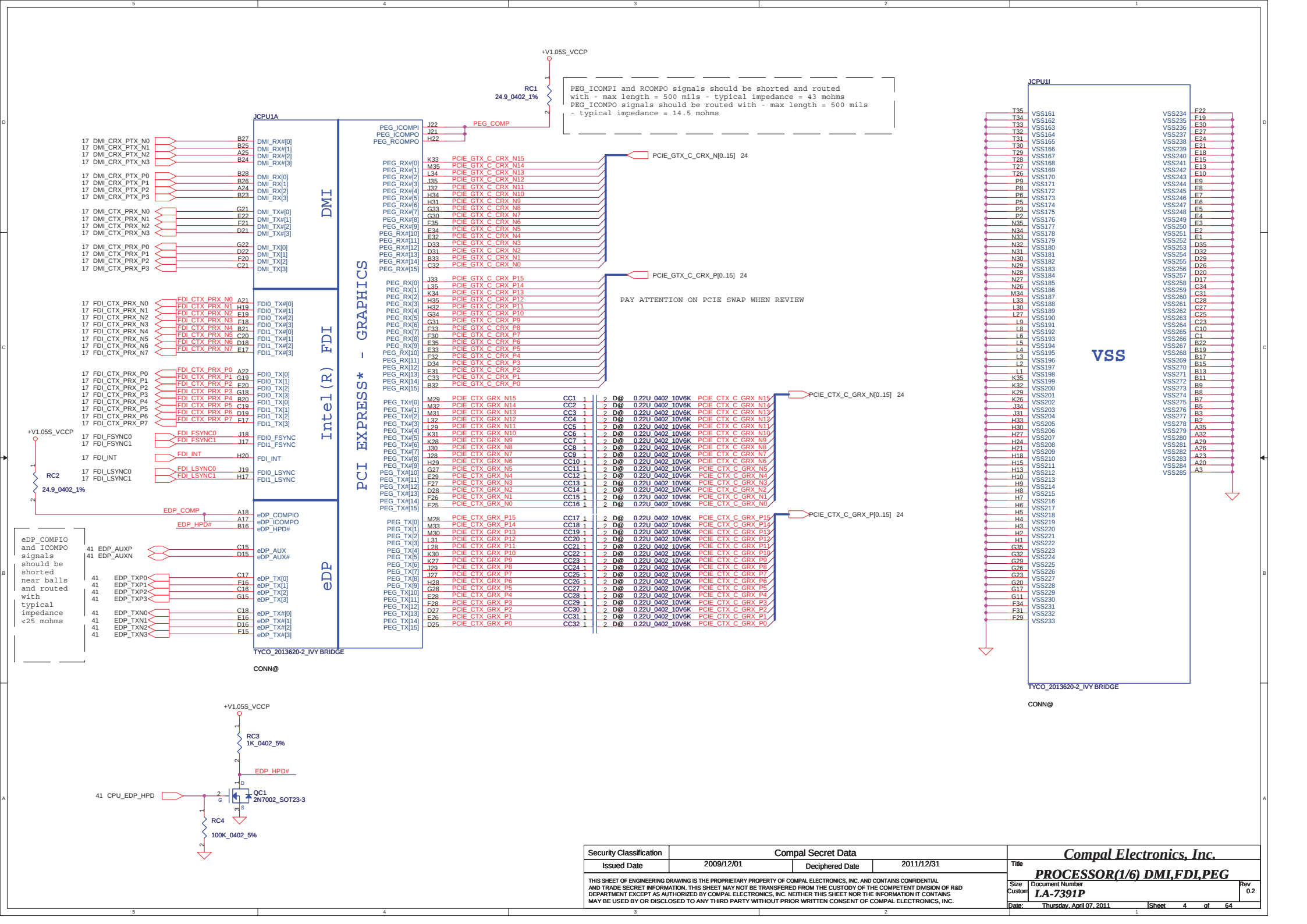
SATA	DESTINATION
SATA0	HDD
SATA1	m-SATA
SATA2	ODD
SATA3	None
SATA4	ESATA
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-1 WLAN
Lane 3	EXPRESS CARD
Lane 4	CARD READER
Lane 5	Light Peak
Lane 6	Light Peak
Lane 7	Light Peak
Lane 8	Light Peak

Symbol Note :

: means Digital Ground

: means Analog Ground



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: PROCESSOR(1/6) DMI,FDI,PEG

Size	Document Number	Rev
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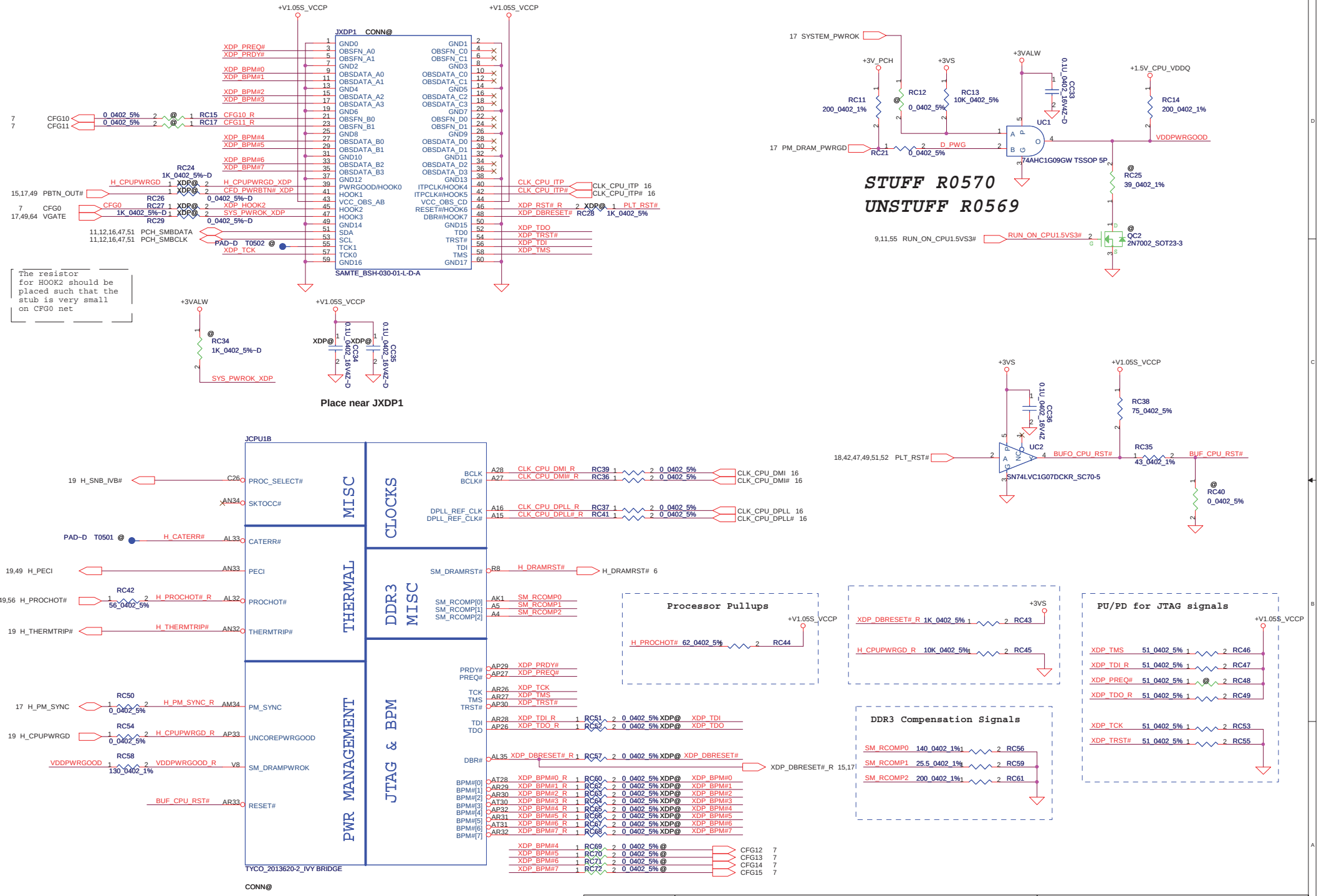

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: PROCESSOR(2/6) PM,XDP,CLK

Size	Document Number	Rev
Custom	LA-7391P	0.2

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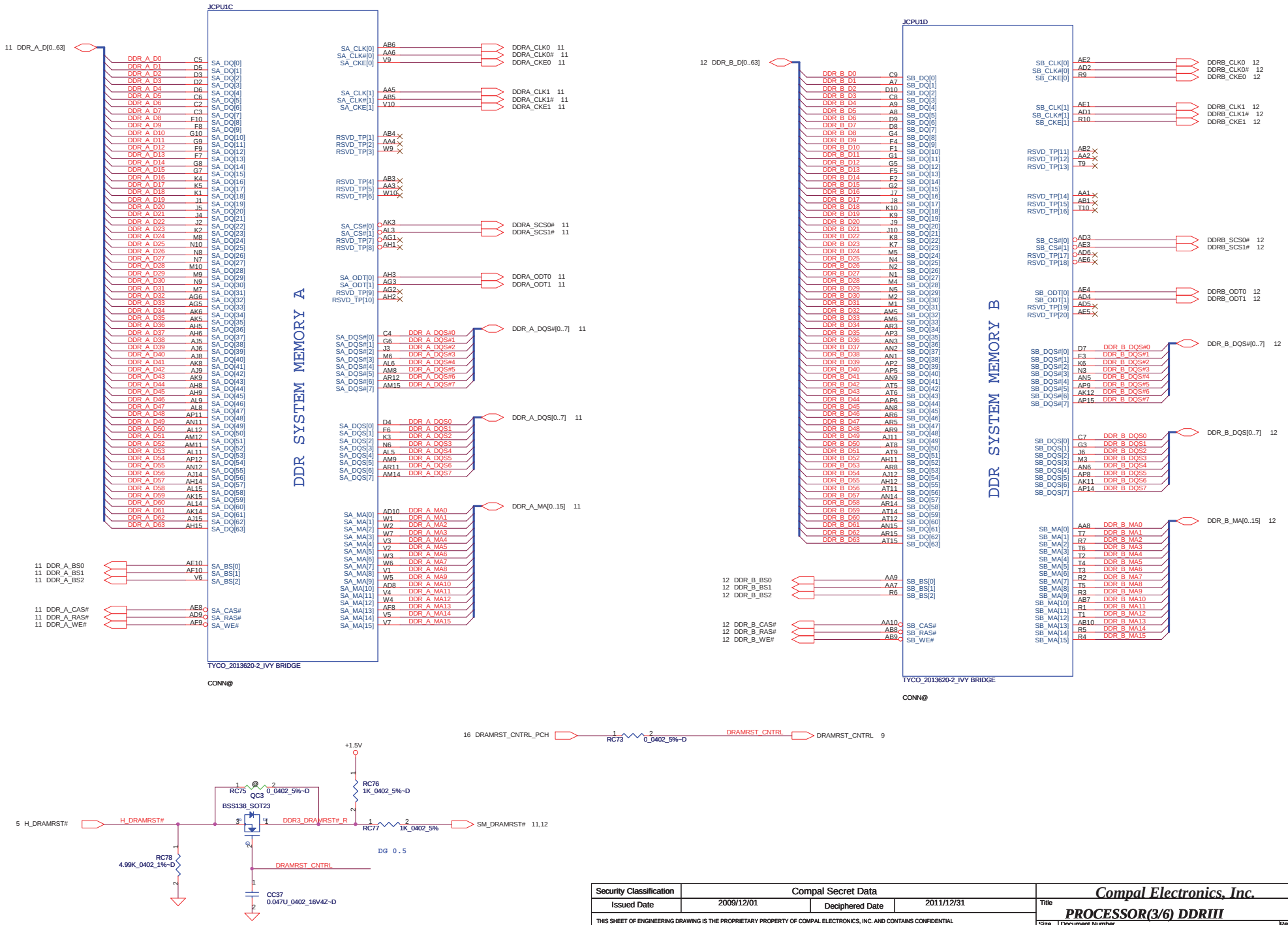

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: PROCESSOR(3/6) DDRIII

Size	Document Number	Rev
Custom	LA-7391P	0.2

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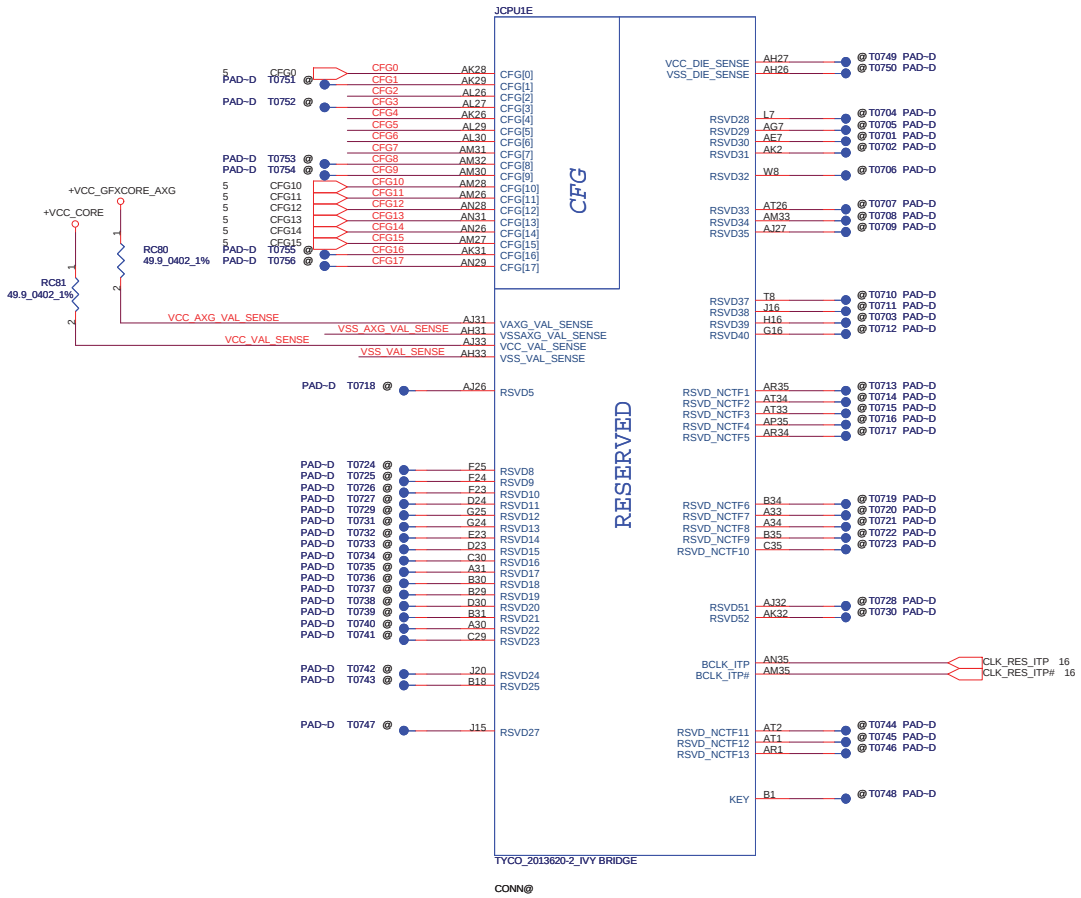
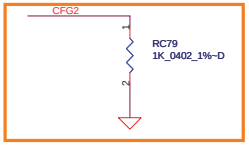
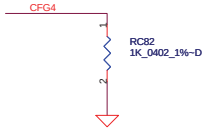
CFG Straps for Processor

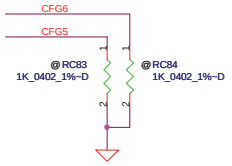




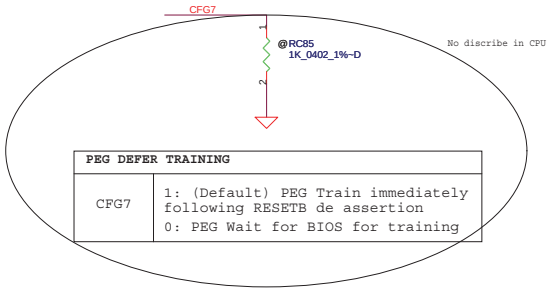
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

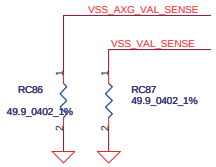


PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following RESETB de assertion 0: PEG Wait for BIOS for training

Need PWR add new circuit on 1.05V(refer CRB)



INTEL 12/28 recommand
to add RC120, RC121, RC122, RC123
Please place as close as JCPU1

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Compal Electronics, Inc.

Title: PROCESSOR(4/6) RSVD,CFG

Size	Document Number	Rev
Custom	LA-7391P	0.2

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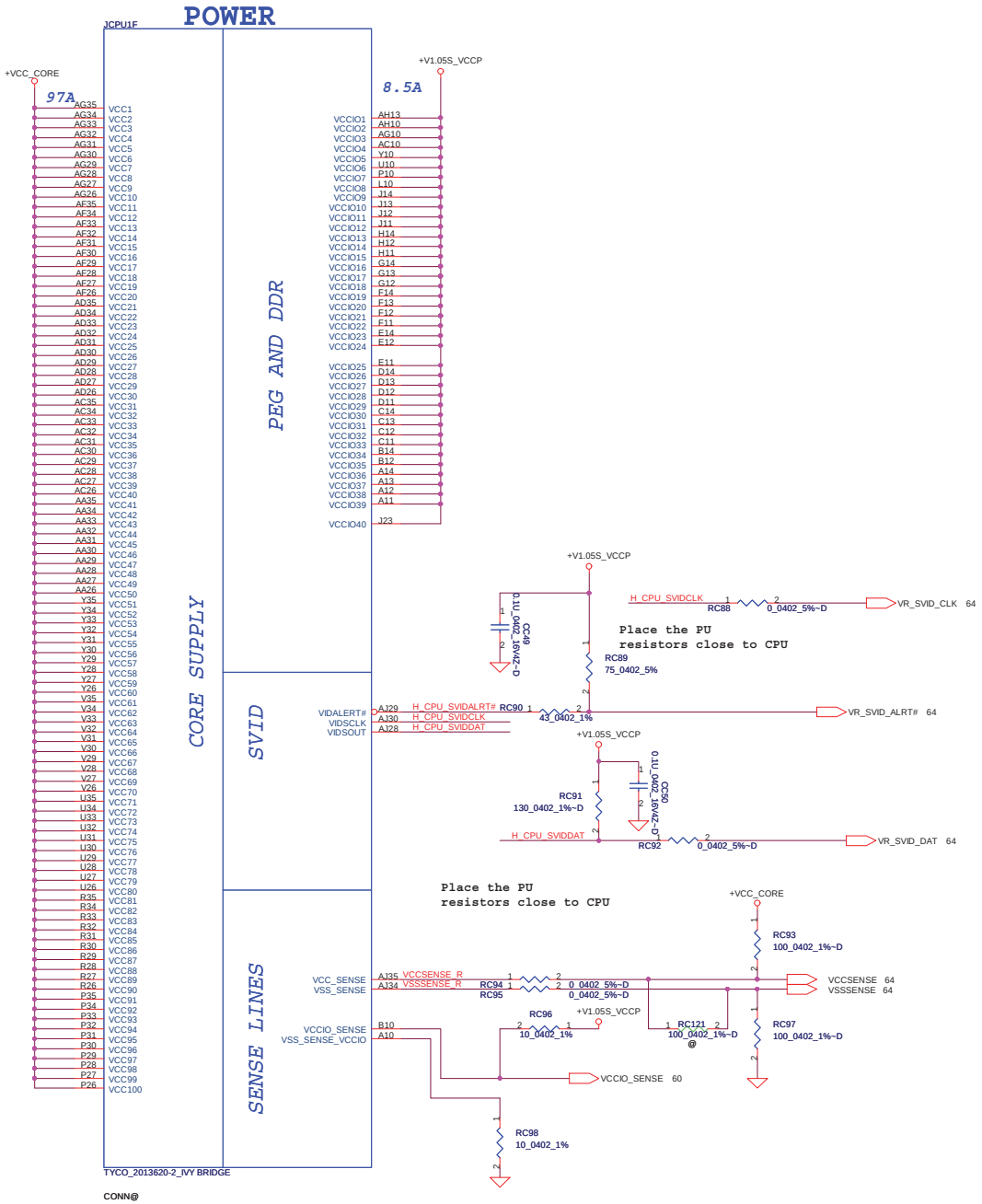

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: PROCESSOR(5/6) PWR,BYPASS

Size	Document Number	Rev
Custom	LA-7391P	0.2

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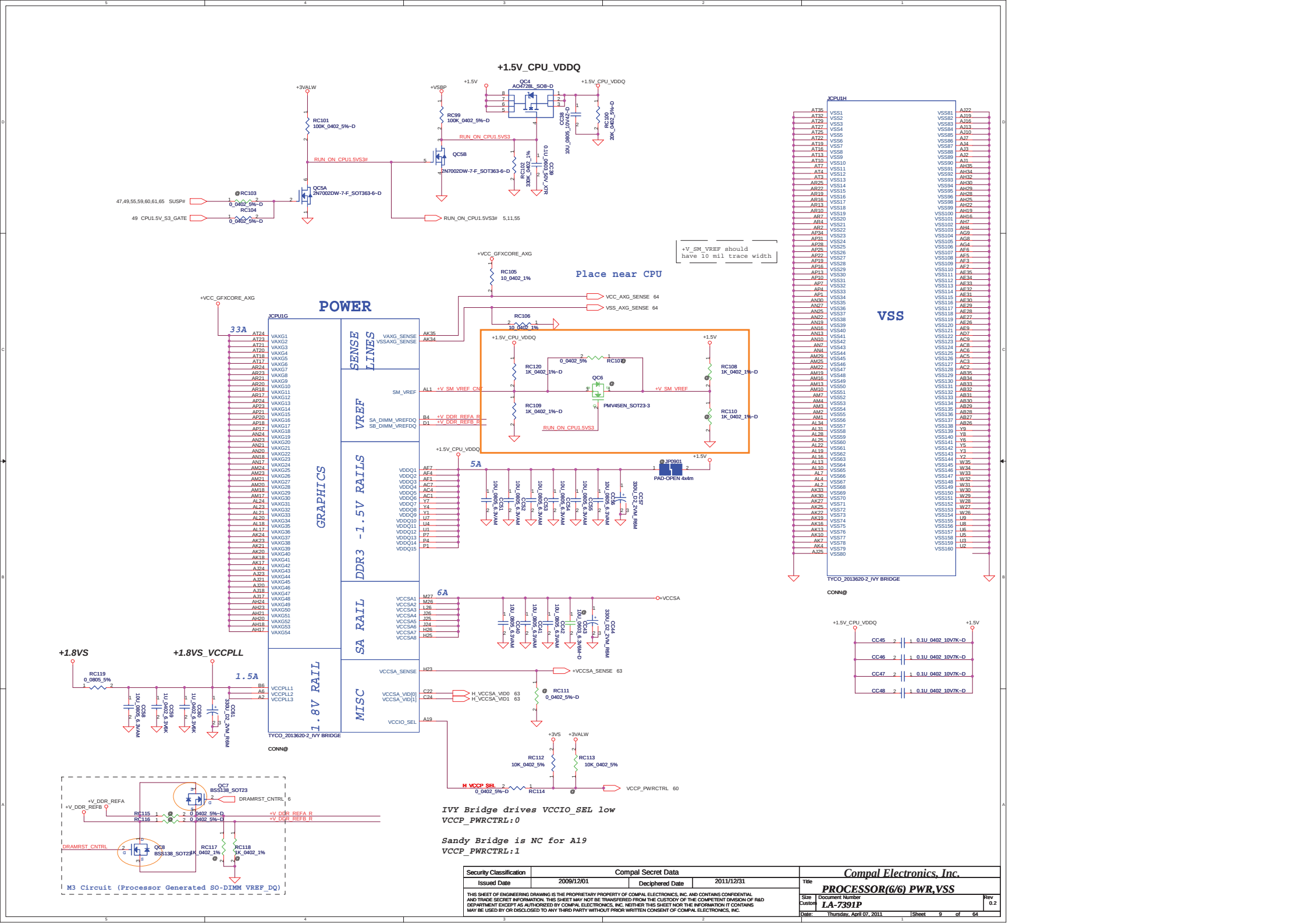

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Issued Date	2009/12/01	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: PROCESSOR(6/6) PWR,VSS

Size	Document Number	Rev
Custom	LA-7391P	0.2

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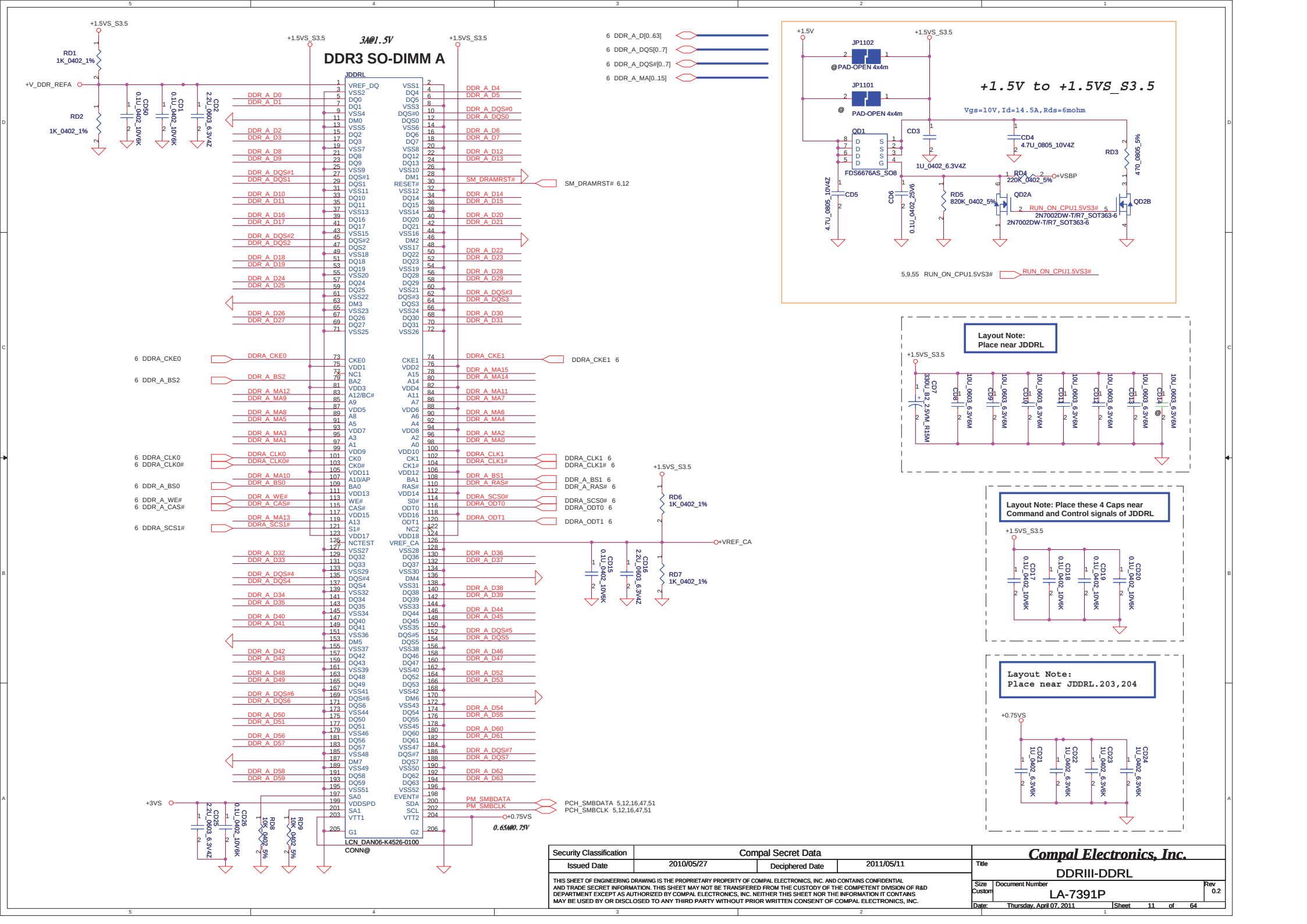
DDR3 SO-DIMM A
JDDRL
LCN_DAN06-K4526-0100
CONN@
+1.5V to +1.5VS_S3.5
Vgs=10V,Id=14.5A,Rds=6mohm
FDS6676AS_SO8
2N7002DW-T/R7_SOT363-6
Layout Note:
Place near JDDRL
Layout Note: Place these 4 Caps near
Command and Control signals of JDDRL
Layout Note:
Place near JDDRL.203,204
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2010/05/27
2011/05/11
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DDRIII-DDRL
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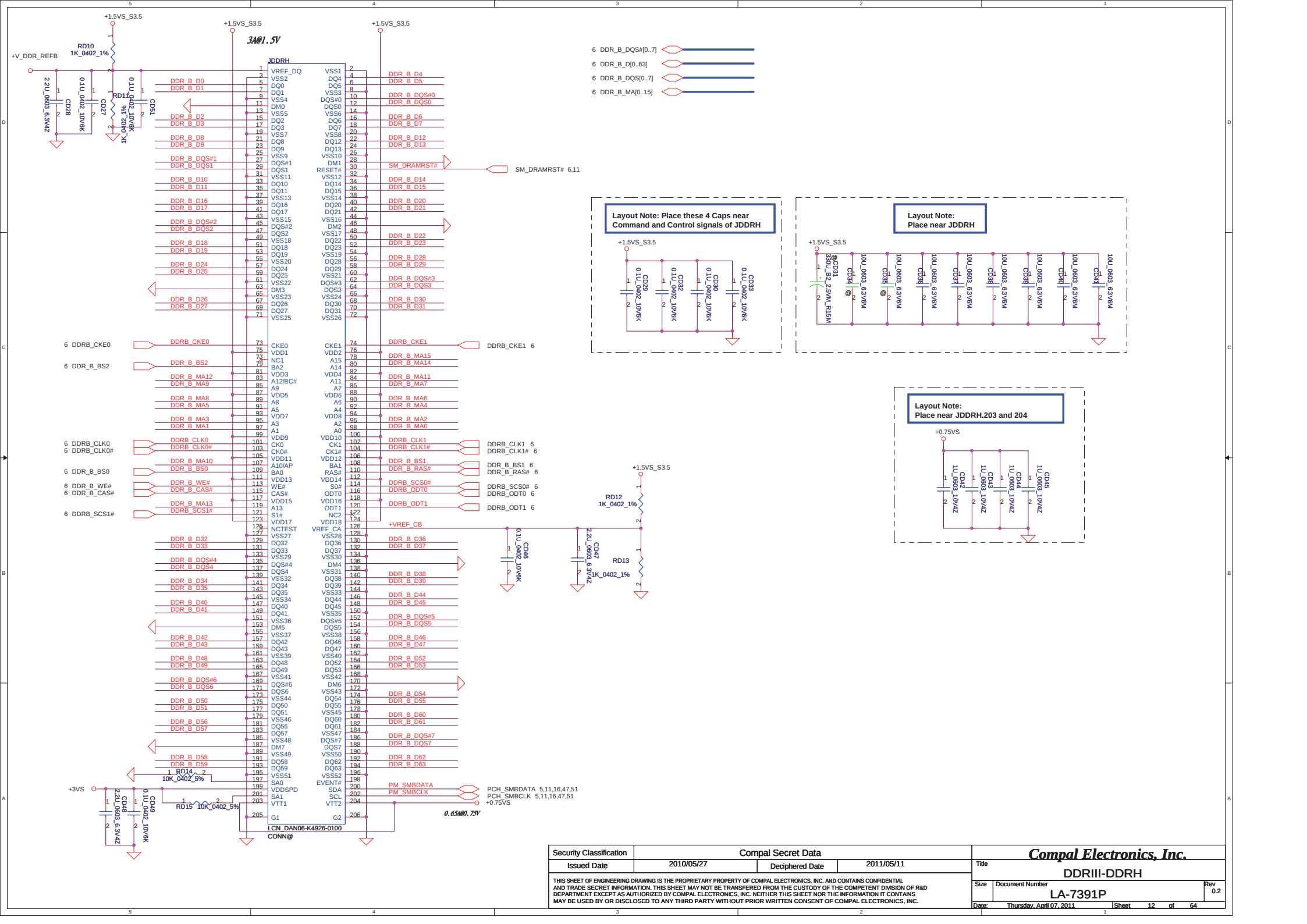

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Compal Electronics, Inc.

Title	DDRIII-DDRH	
Size	Document Number: LA-7391P	Rev: 0.2
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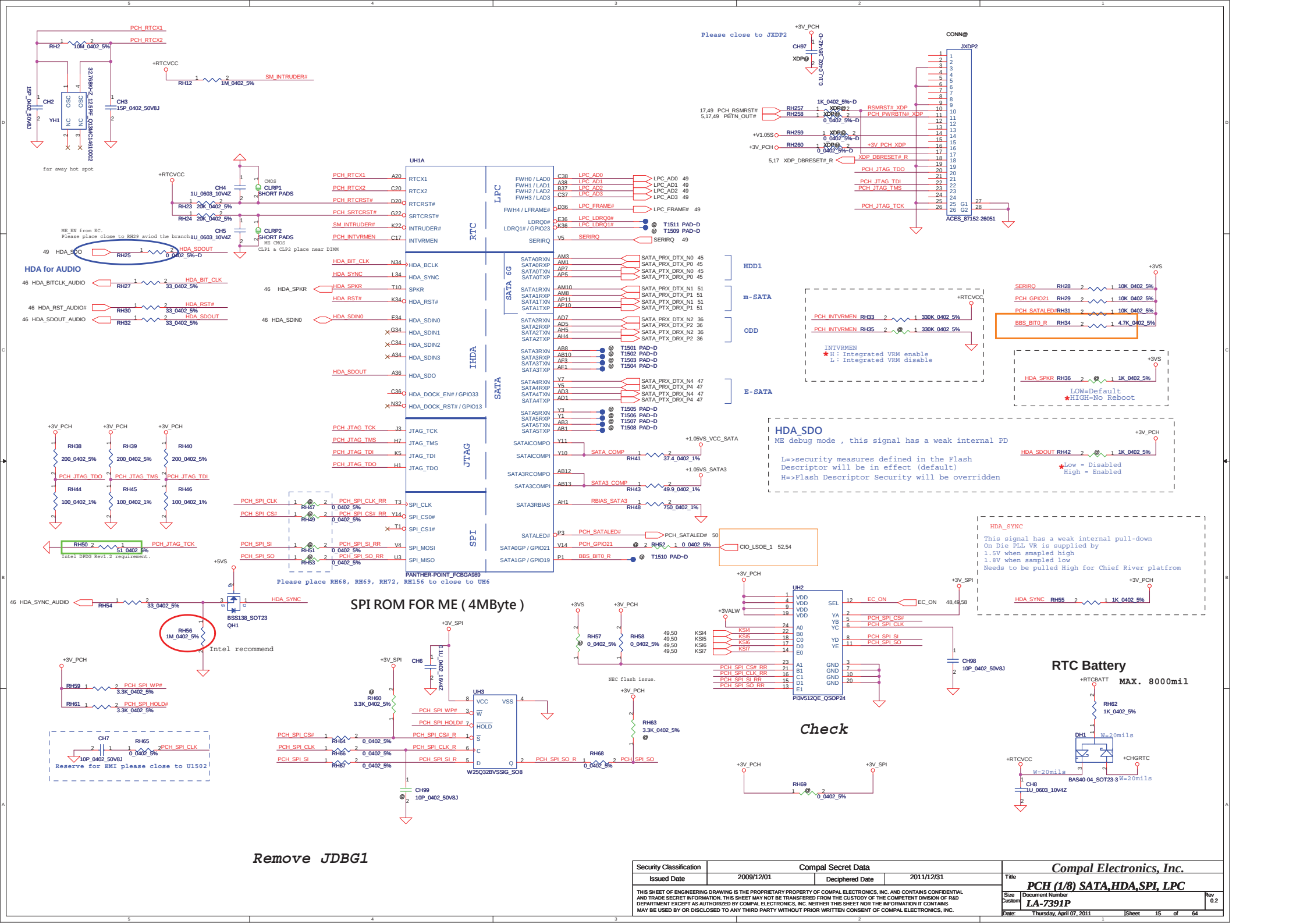

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC

Size	Document Number	Rev
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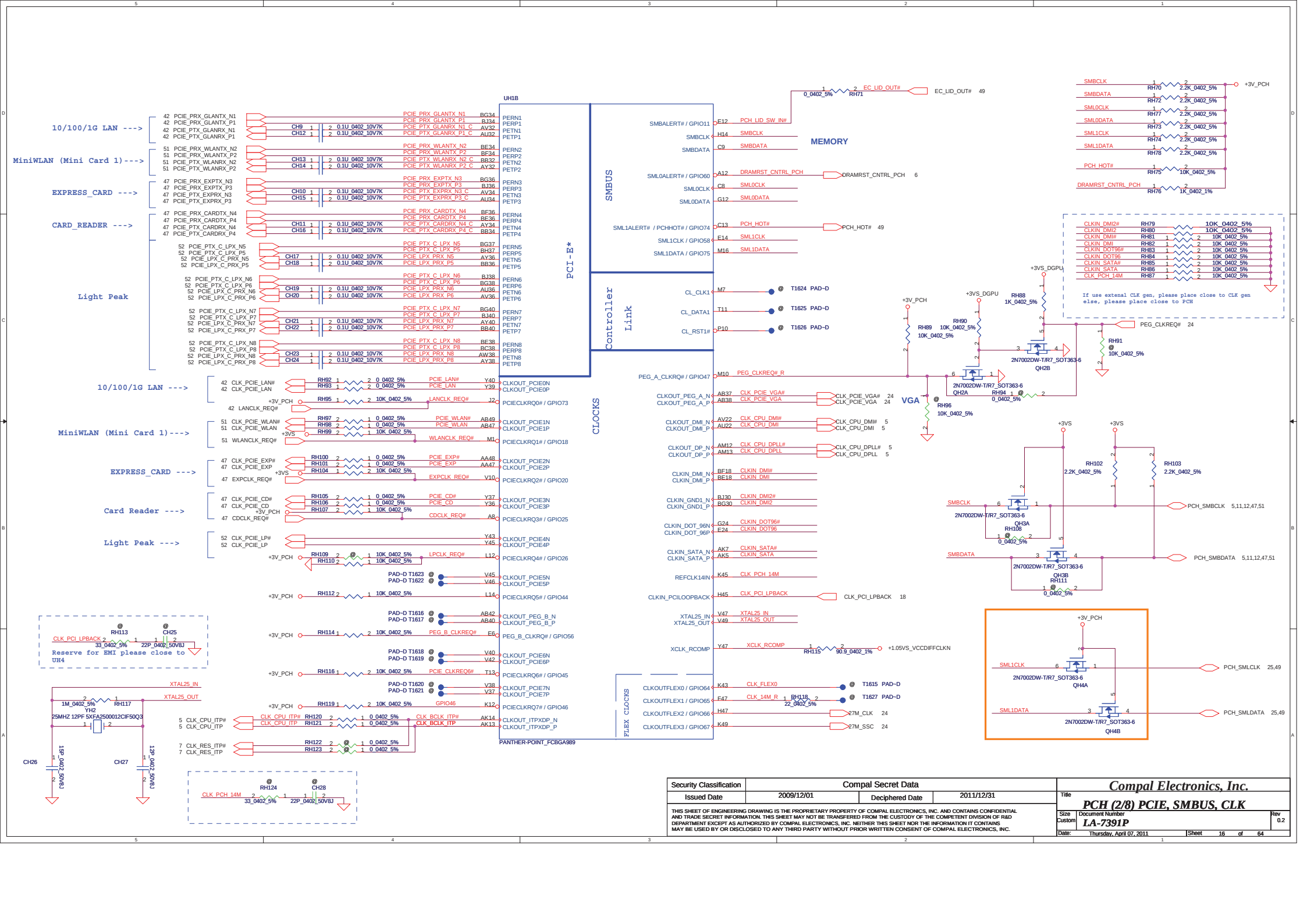
10/100/1G LAN --->
MiniWLAN (Mini Card 1)--->
EXPRESS_CARD --->
CARD_READER --->
Light Peak
10/100/1G LAN --->
MiniWLAN (Mini Card 1)--->
EXPRESS_CARD --->
Card Reader --->
Light Peak --->
UH1B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
PANTHER-POINT_FCBGA989
MEMORY
VGA
Reserve for EMI please close to UH4
If use extenal CLK gen, please place close to CLK gen else, please place close to PCH
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Title
PCH (2/8) PCIE, SMBUS, CLK
Size
Custom
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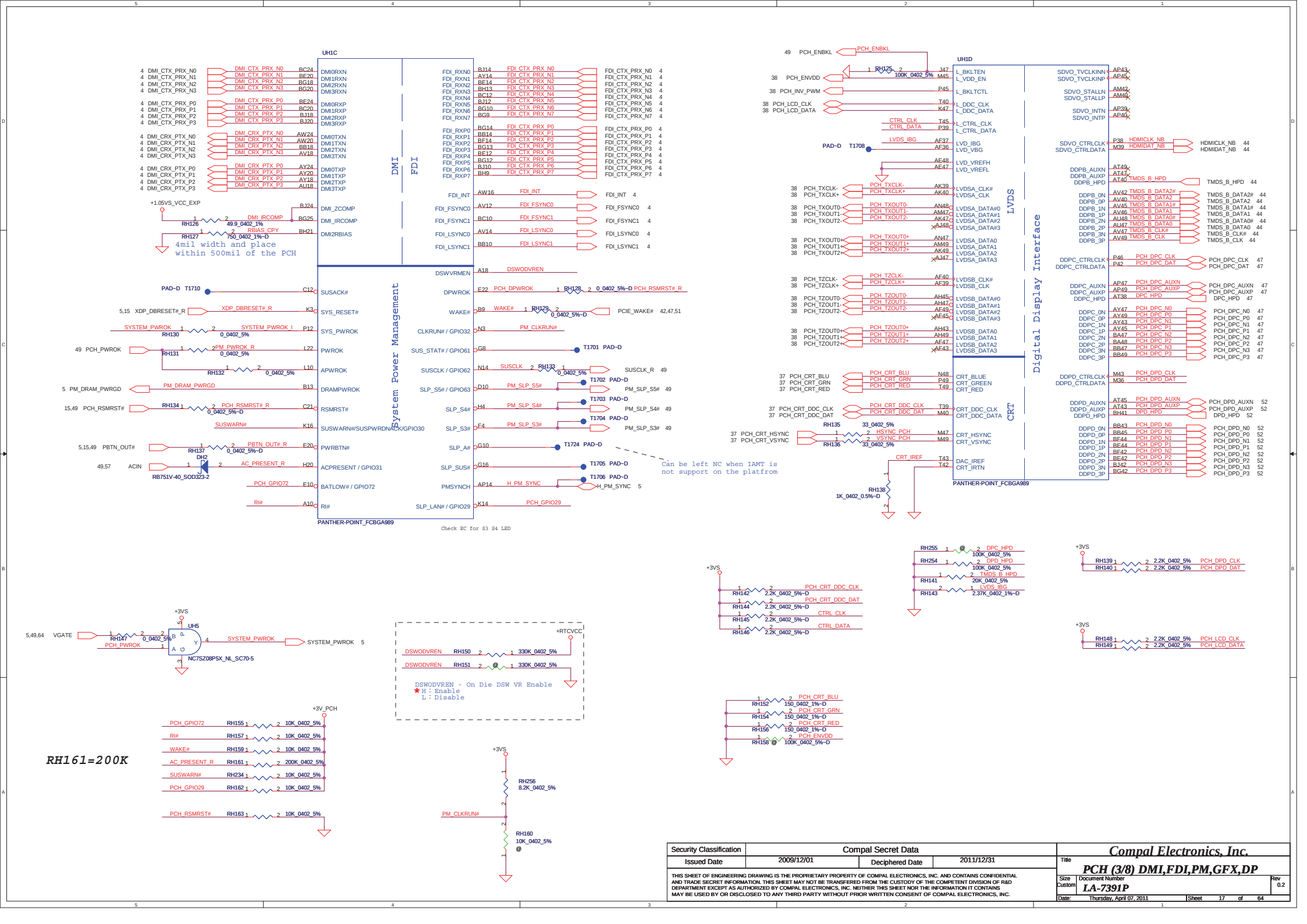

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,GFX,DP

Size	Document Number	Rev
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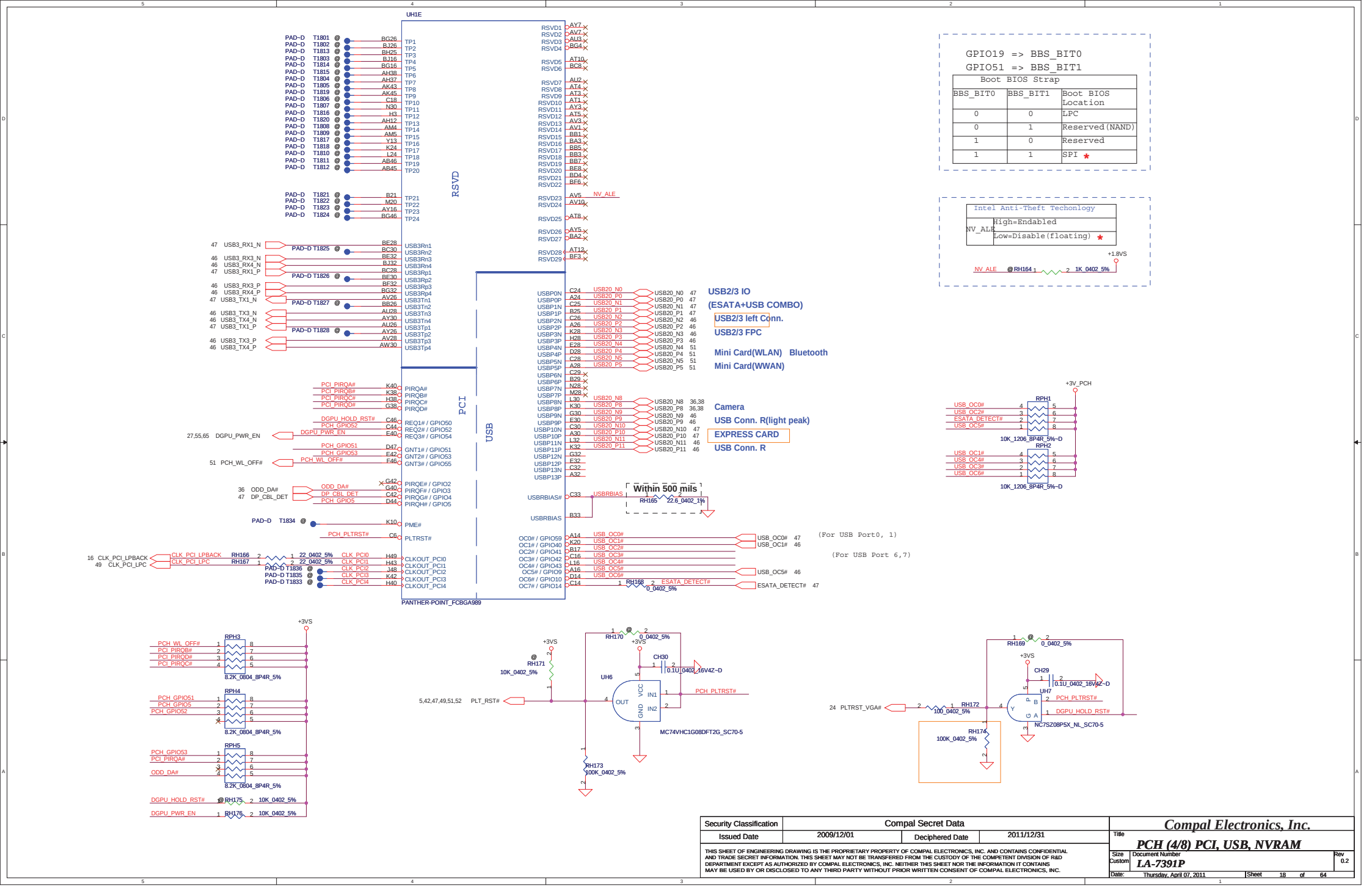

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: PCH (4/8) PCI, USB, NVRAM

Size	Document Number	Rev
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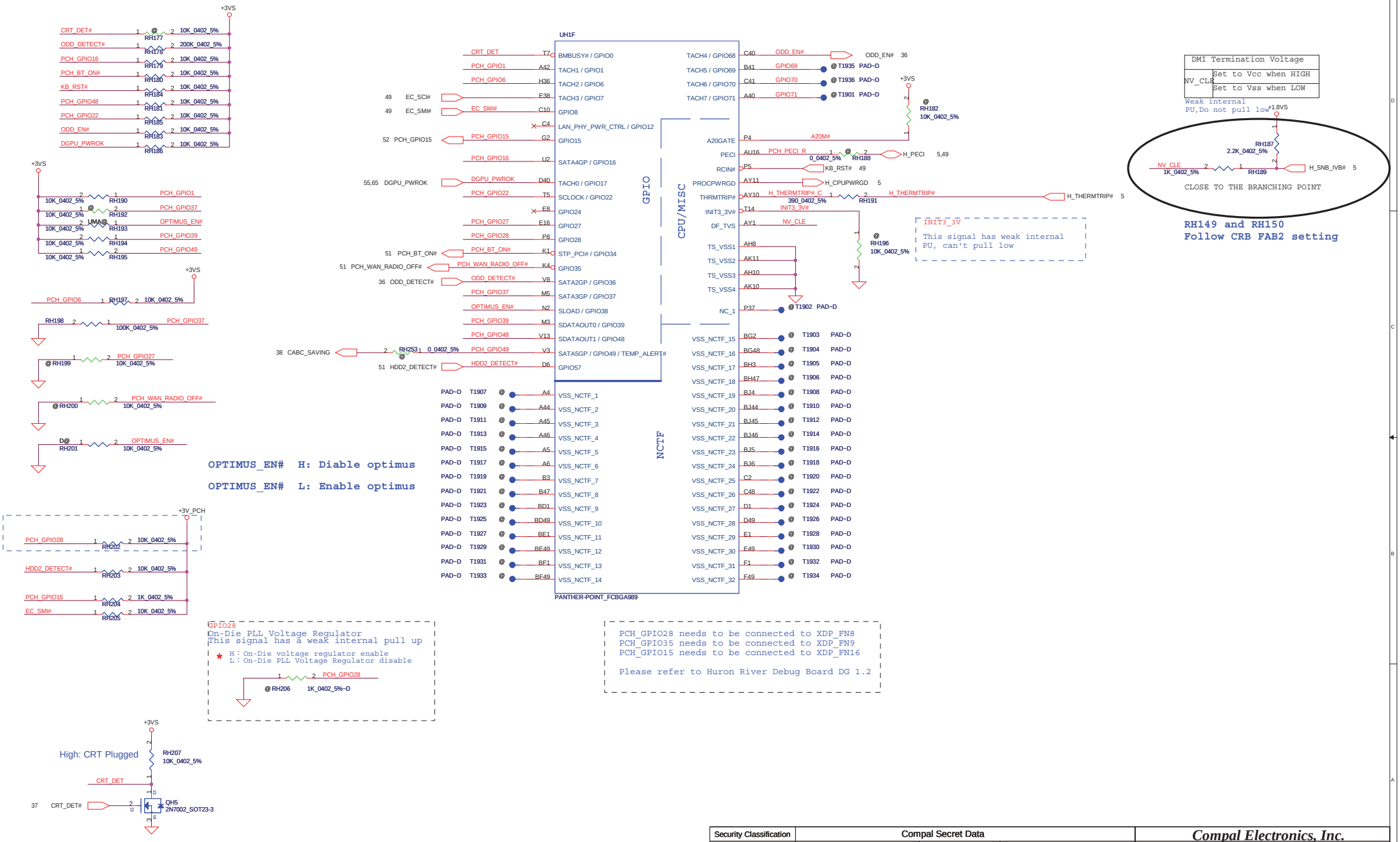

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: PCH (5/8) GPIO, CPU, MISC

Size	Document Number	Rev
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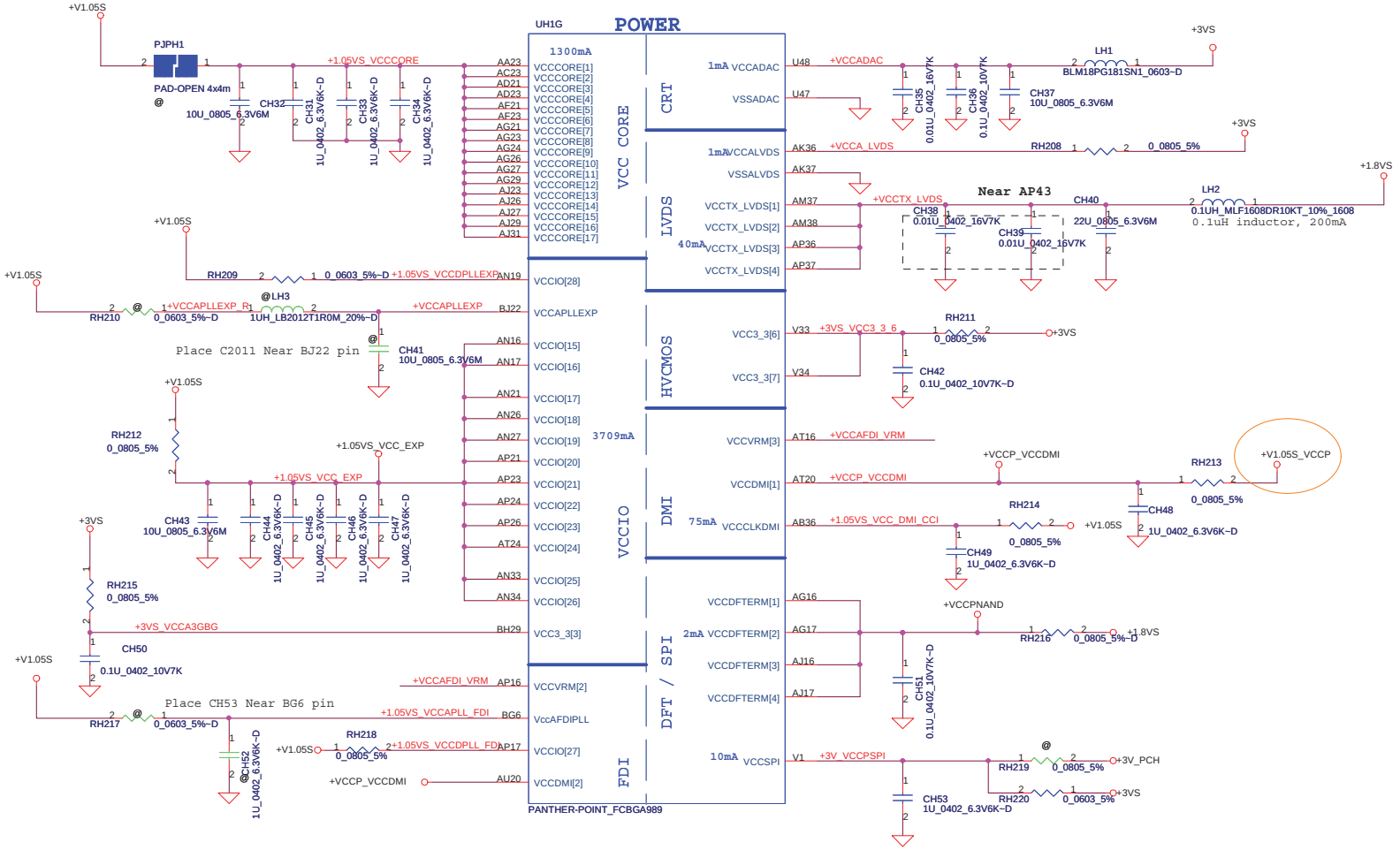
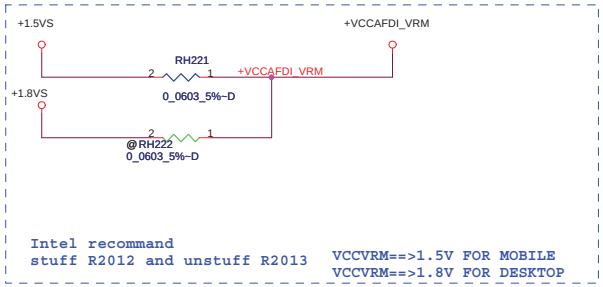


PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



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Compal Electronics, Inc.

Title: PCH (6/8) PWR

Size: Custom | Document Number: LA-7391P | Rev: 0.2

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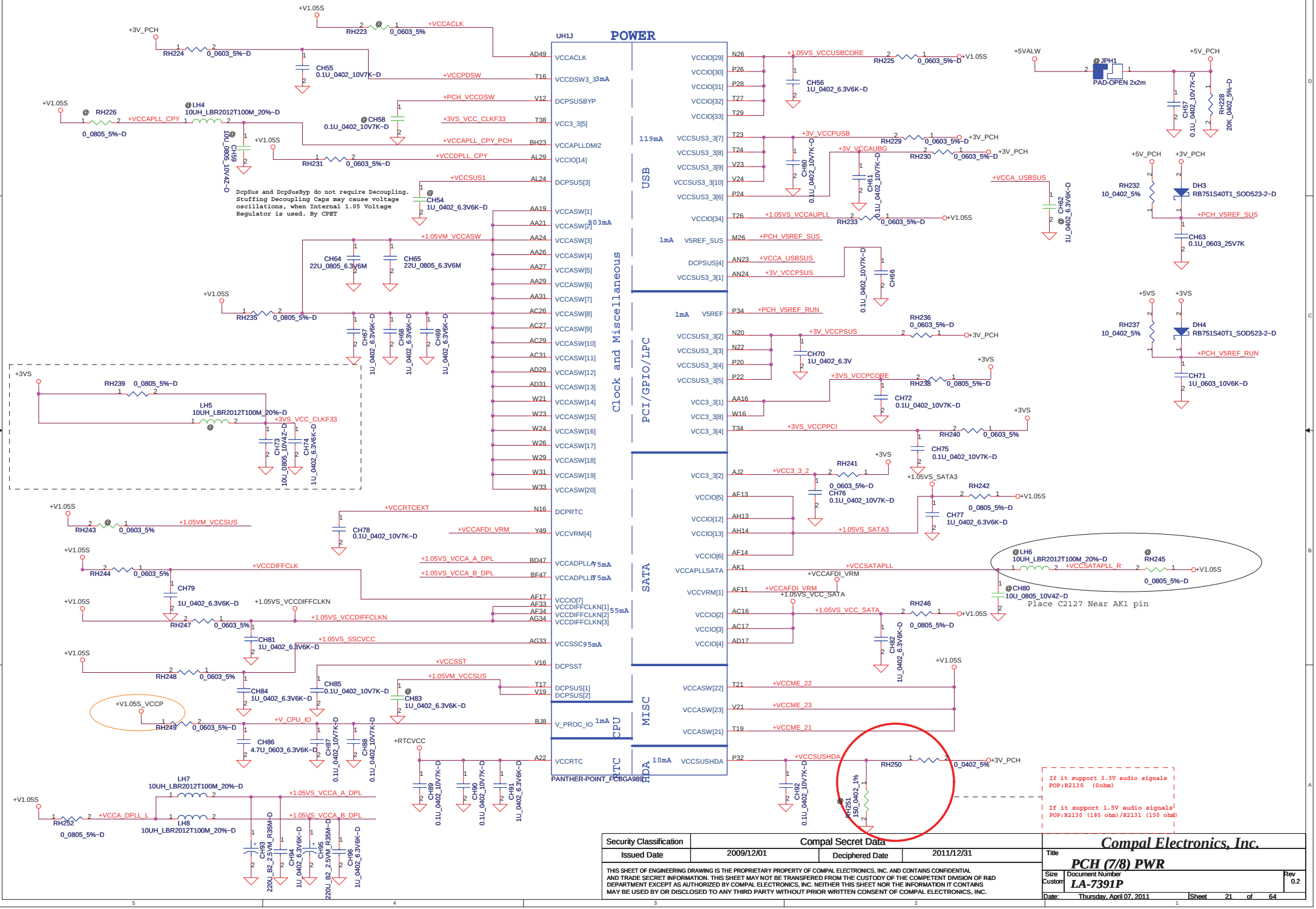

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Compal Electronics, Inc.

Title: PCH (7/8) PWR

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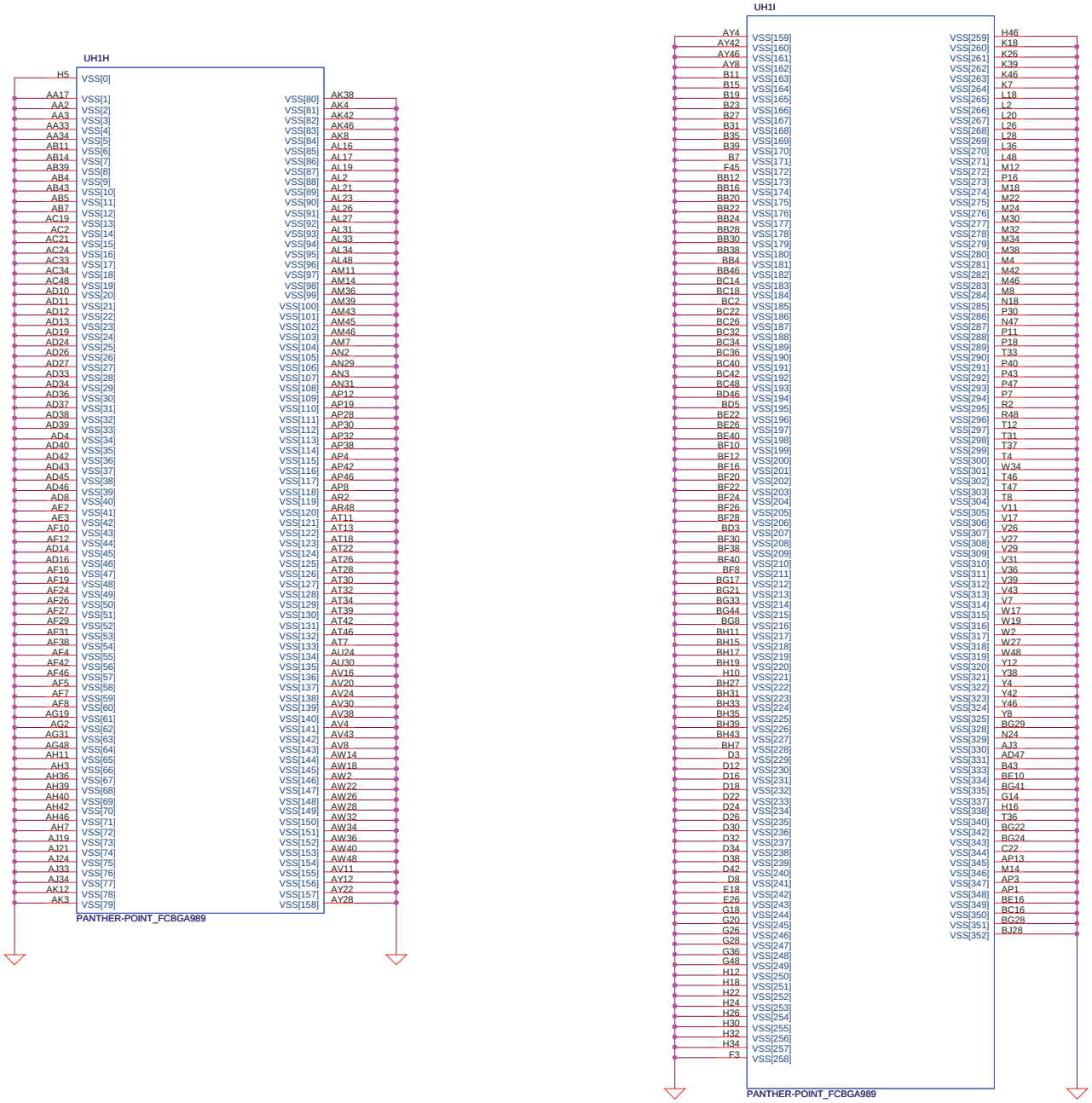

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Compal Electronics, Inc.

Title: PCH (8/8) VSS

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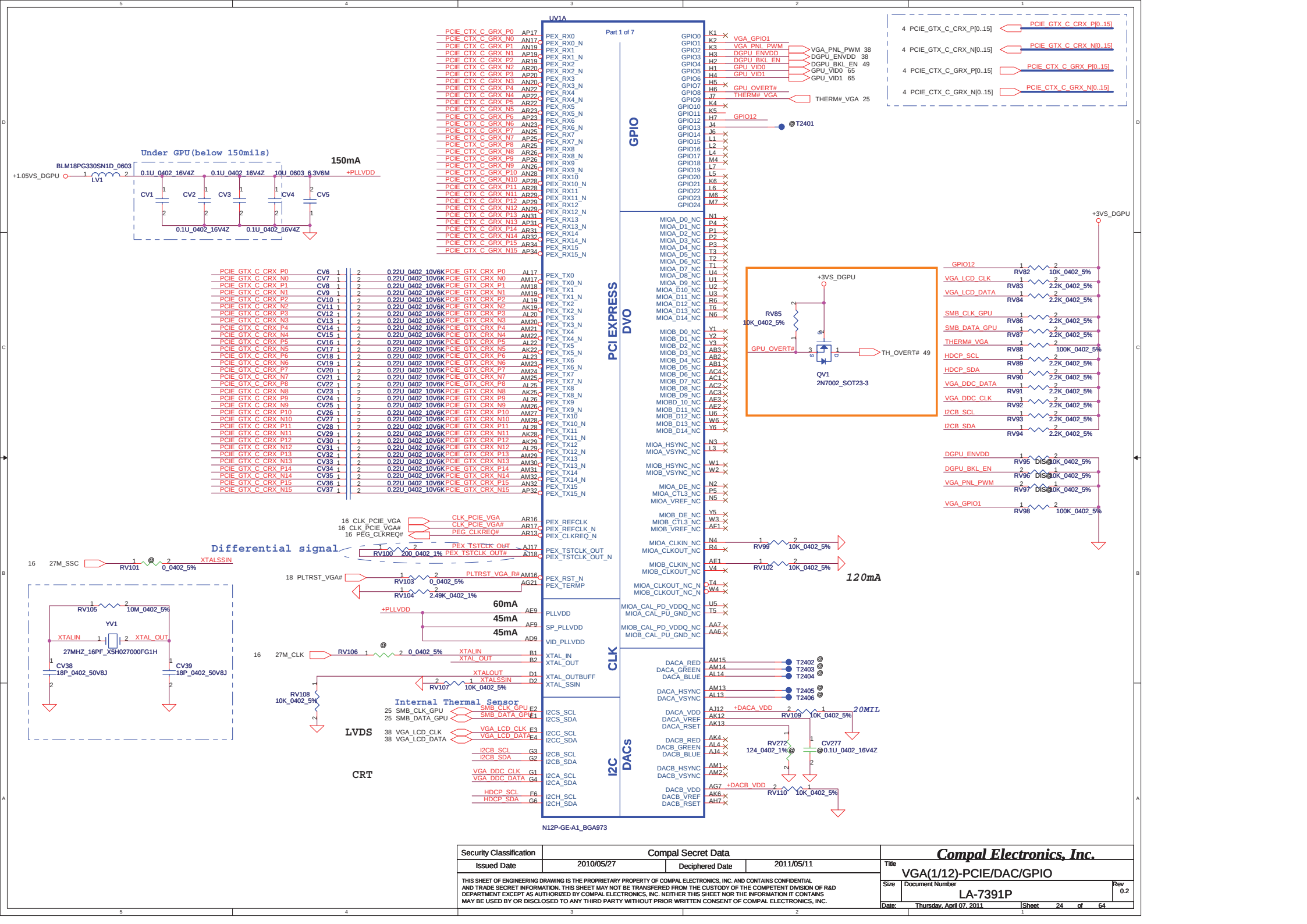

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: VGA(1/12)-PCIE/DAC/GPIO

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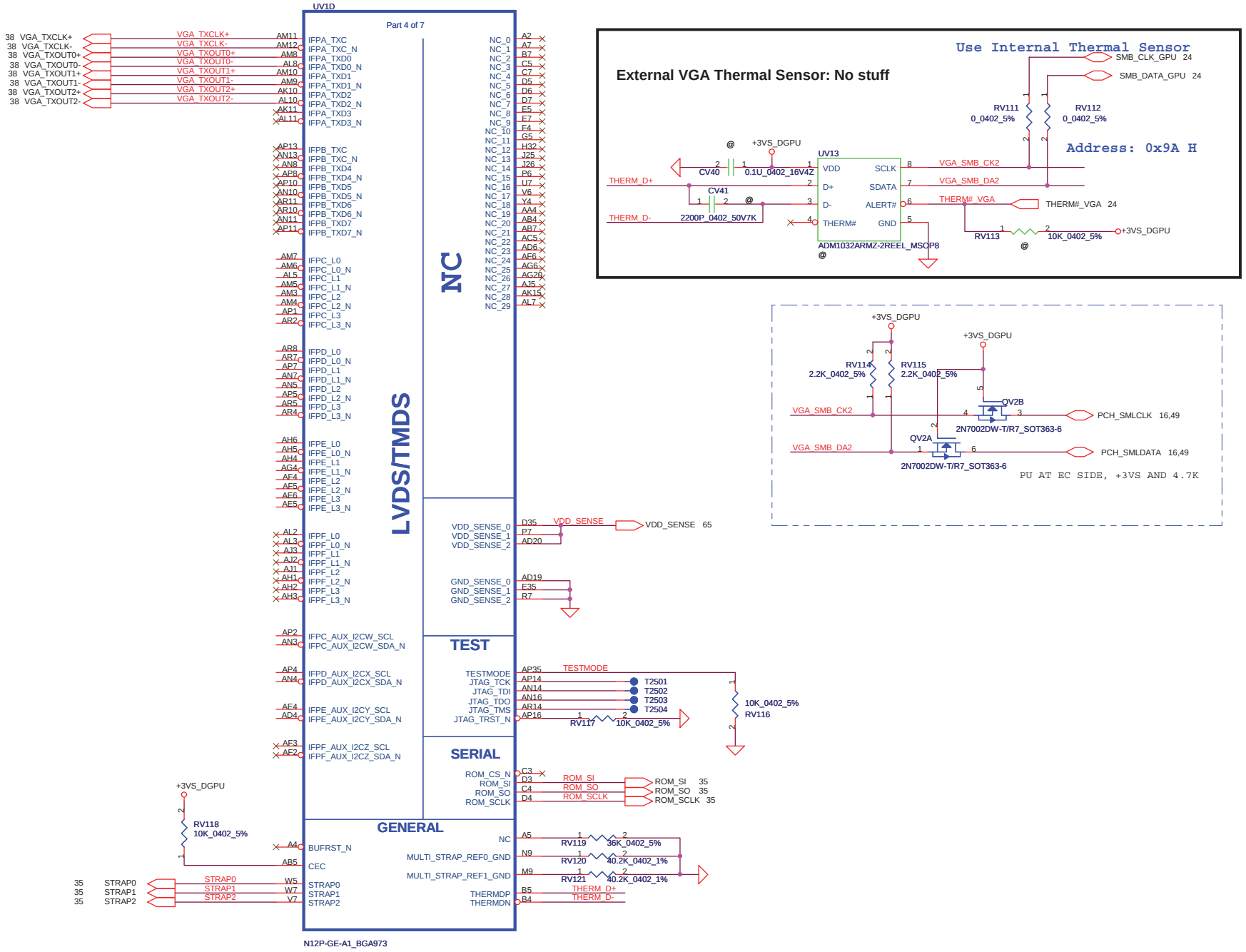

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: VGA(2/12)-LVDS/HDMI/DP/THM

Size	Document Number	Rev
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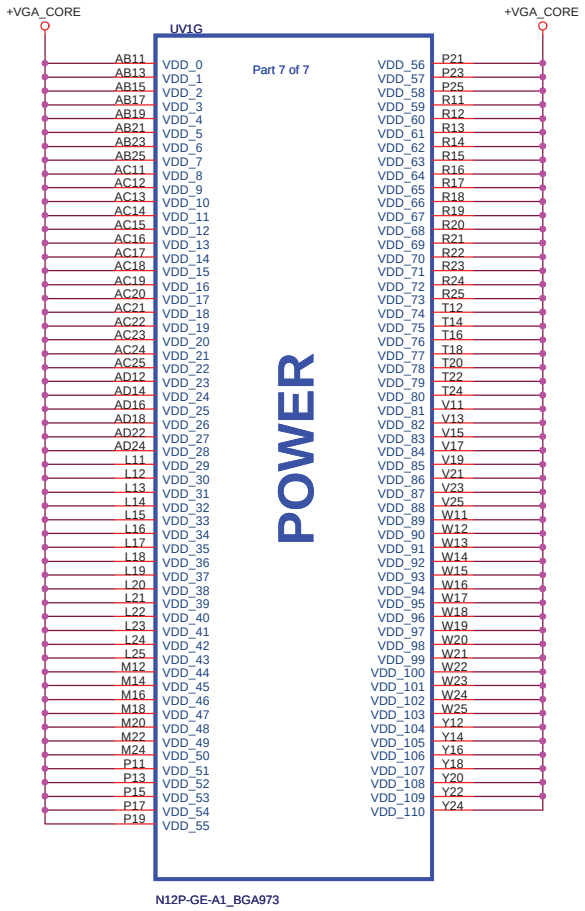

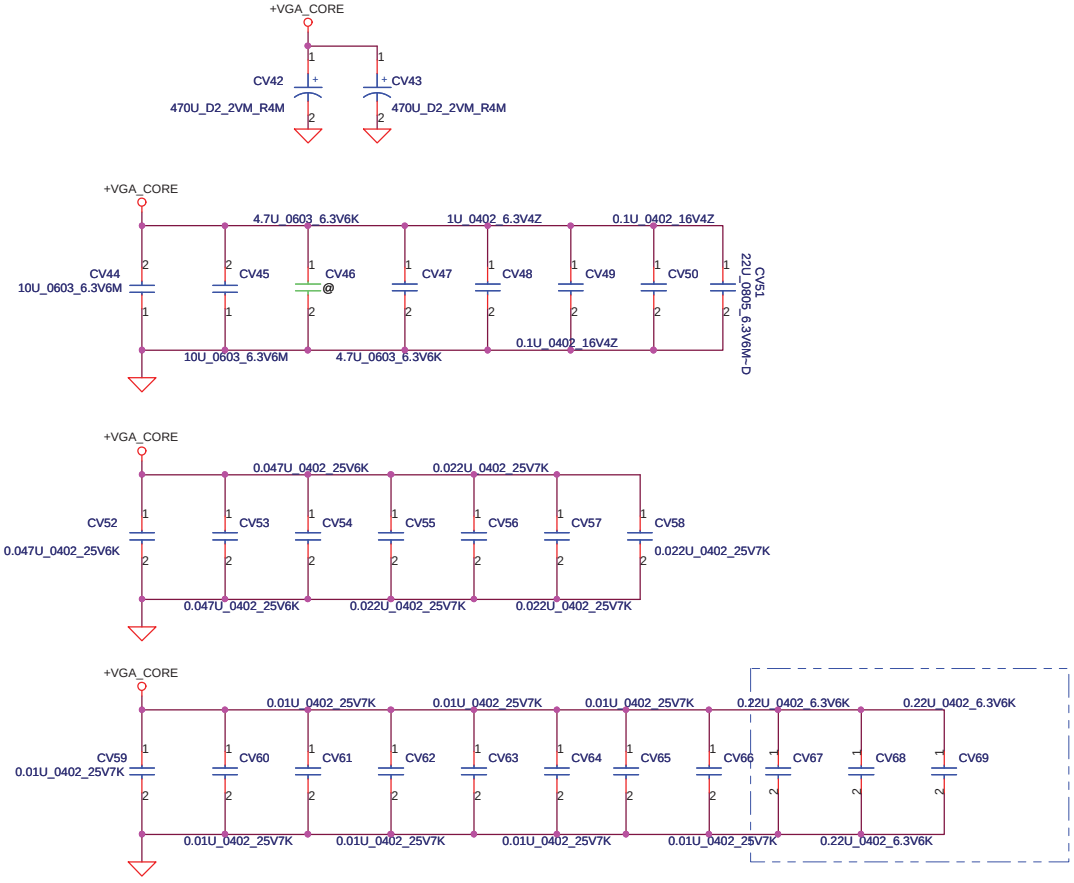

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: VGA(3/12)-VGA CORE

Size	Document Number	Rev
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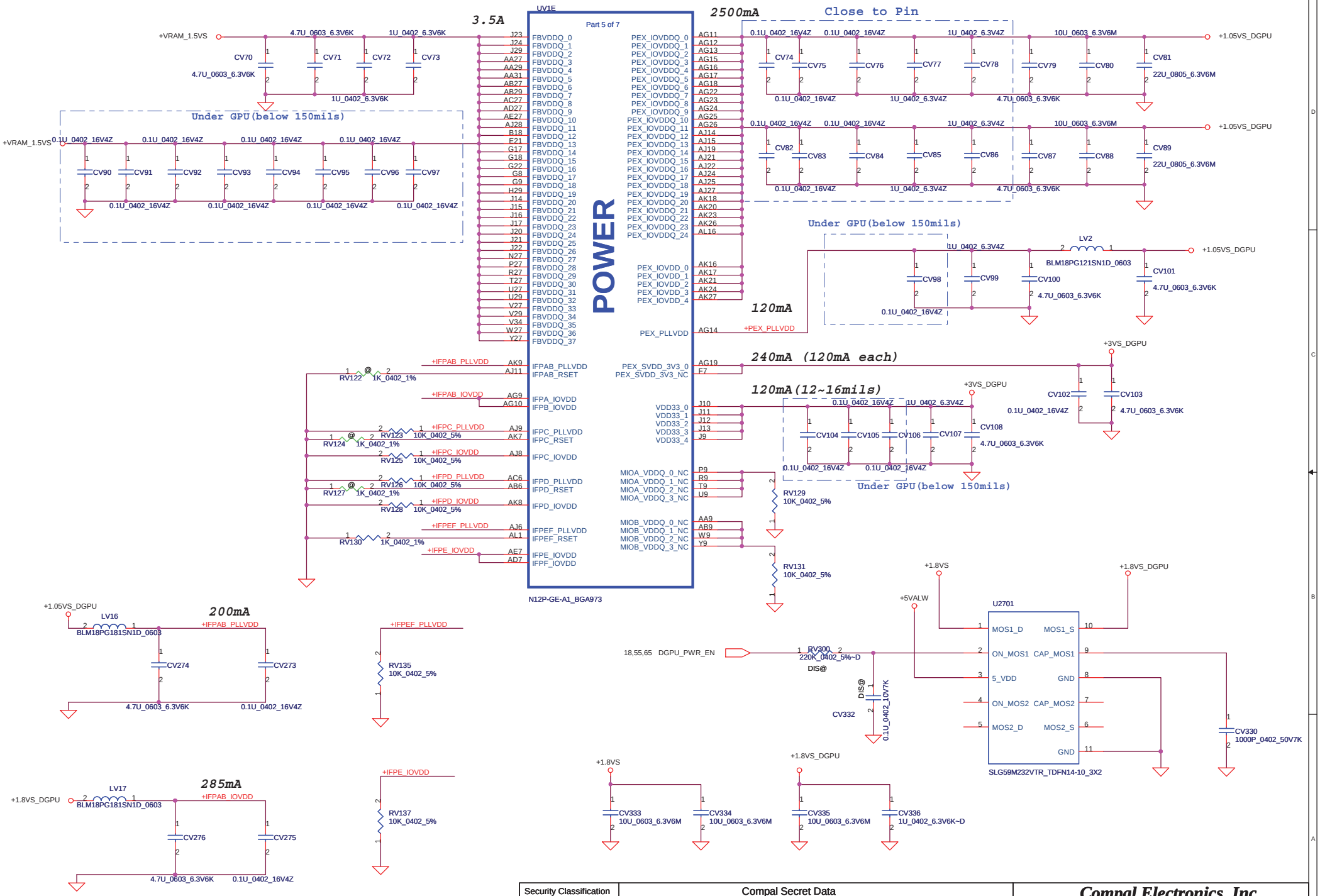

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: VGA(4/12)-POWER

Size	Document Number	Rev
	LA-7391P	0.2

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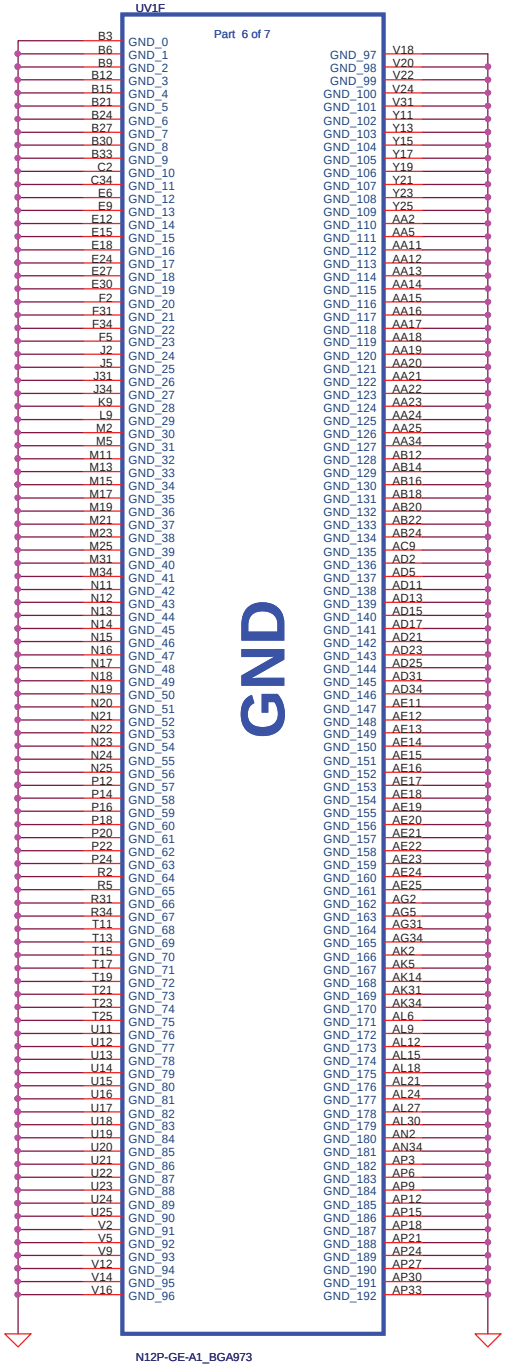


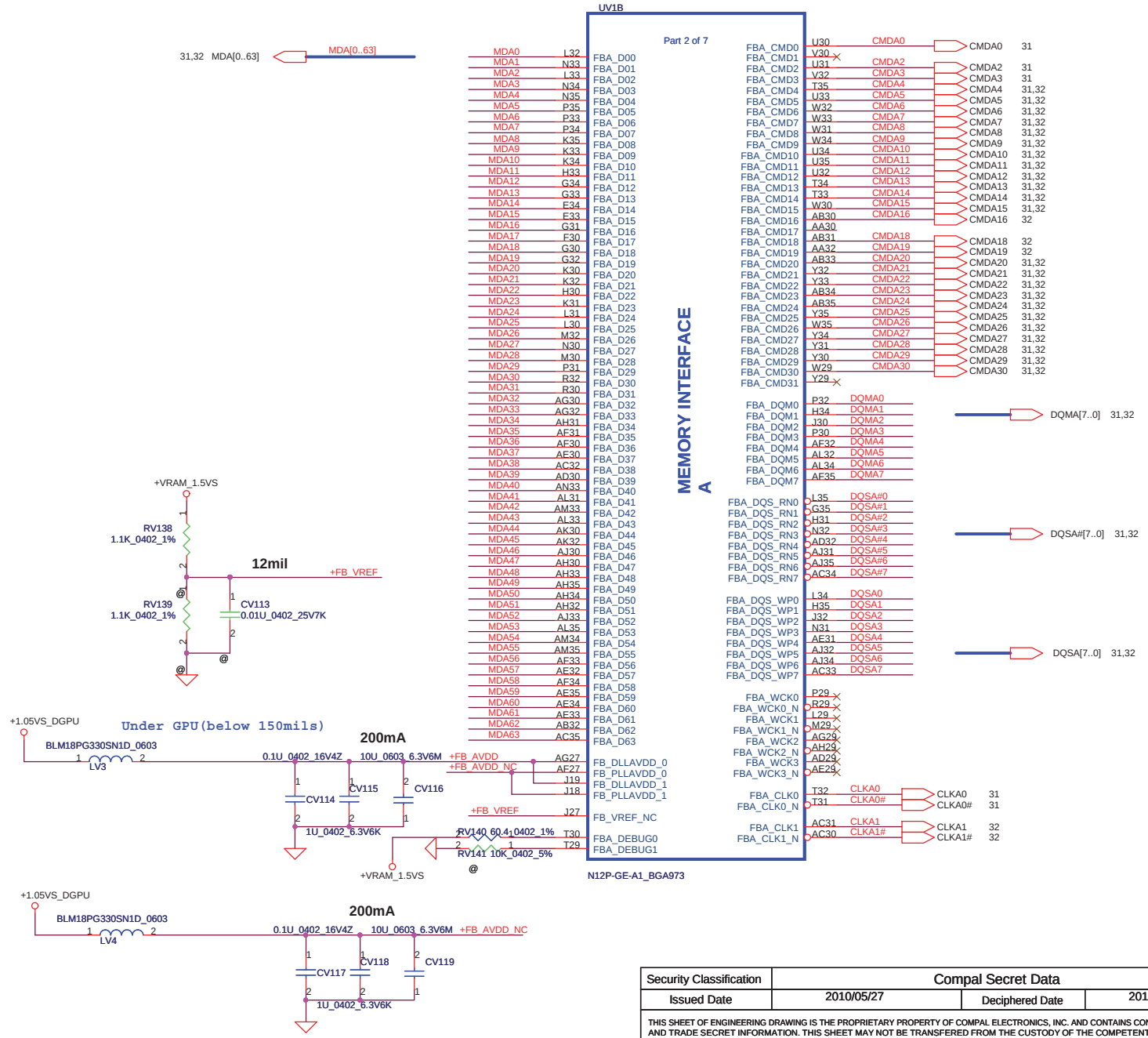
Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: VGA(5/12)-GND

Size | Document Number: LA-7391P | Rev: 0.2

Date: Thursday, April 07, 2011 | Sheet 28 of 64



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

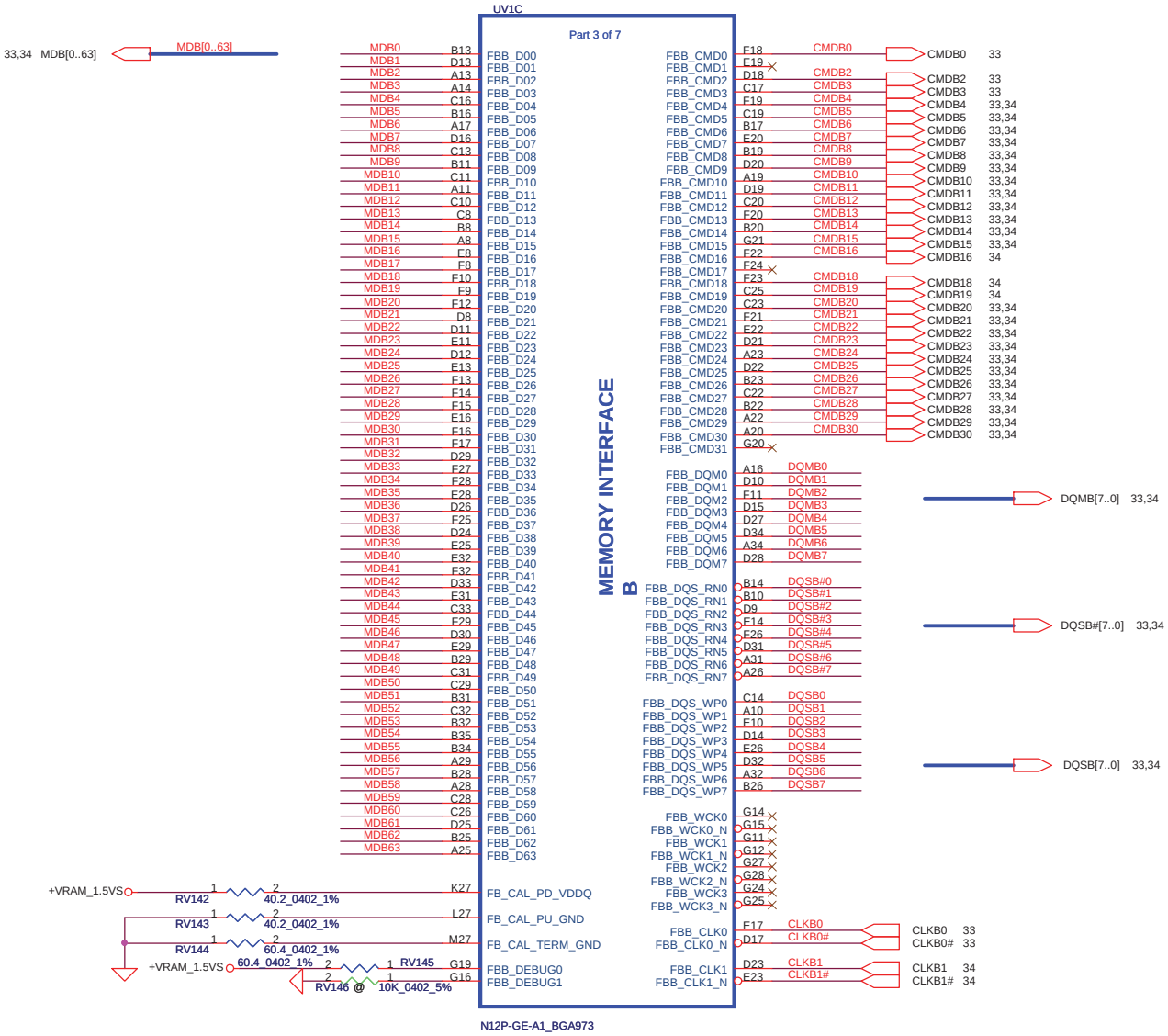
Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: VGA(6/12)-MEM Interface A

Size	Document Number	Rev
	LA-7391P	0.2

Date: Thursday, April 07, 2011 | Sheet 29 of 64



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: VGA(7/12)-MEM Interface C

Size | Document Number: LA-7391P | Rev: 0.2

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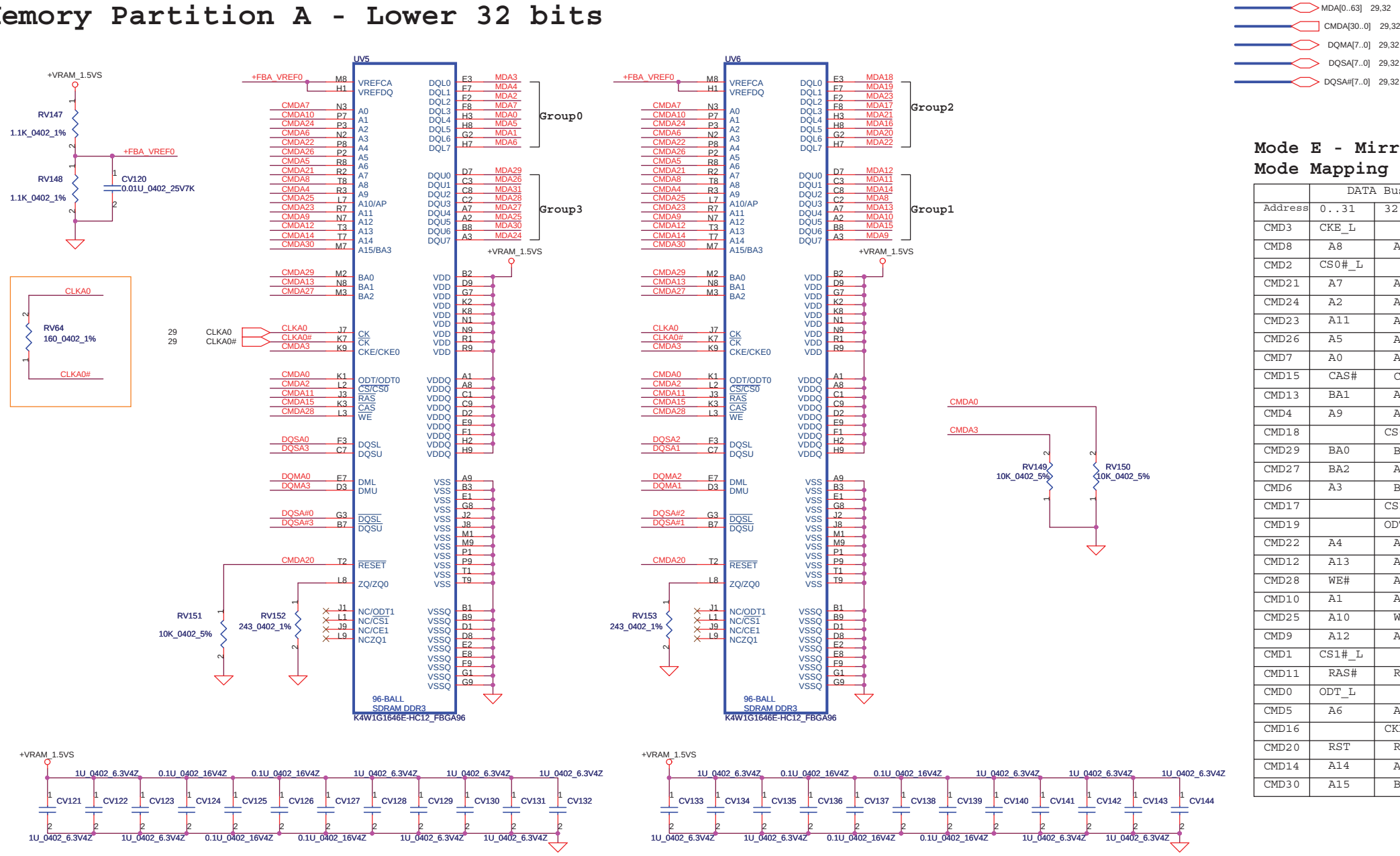
Memory Partition A - Lower 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Compal Electronics, Inc.

Title: VGA(8/12)-VRAM A Lower

Size	Document Number	Rev
	LA-7391P	0.2

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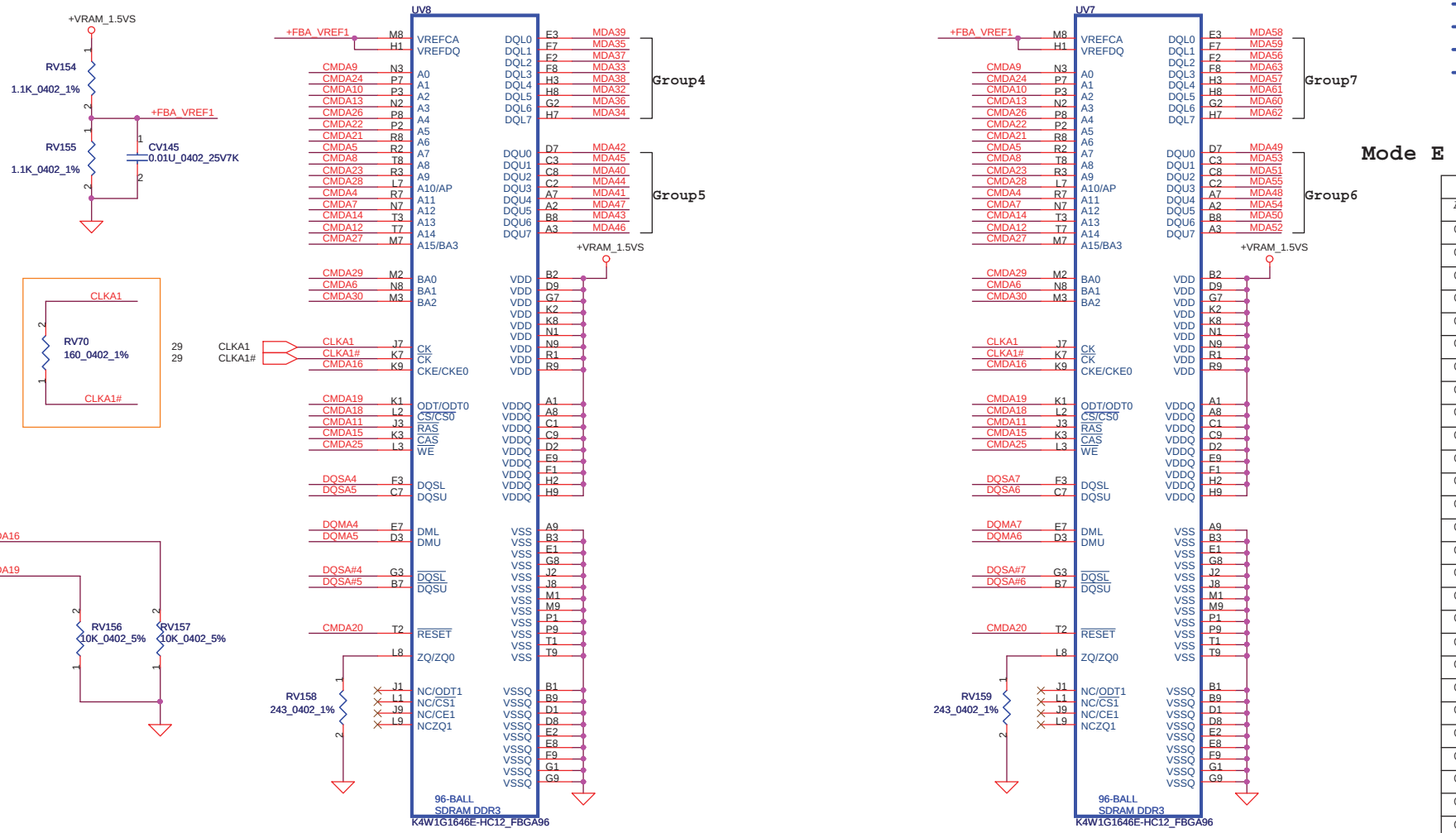
Memory Partition A - Upper 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

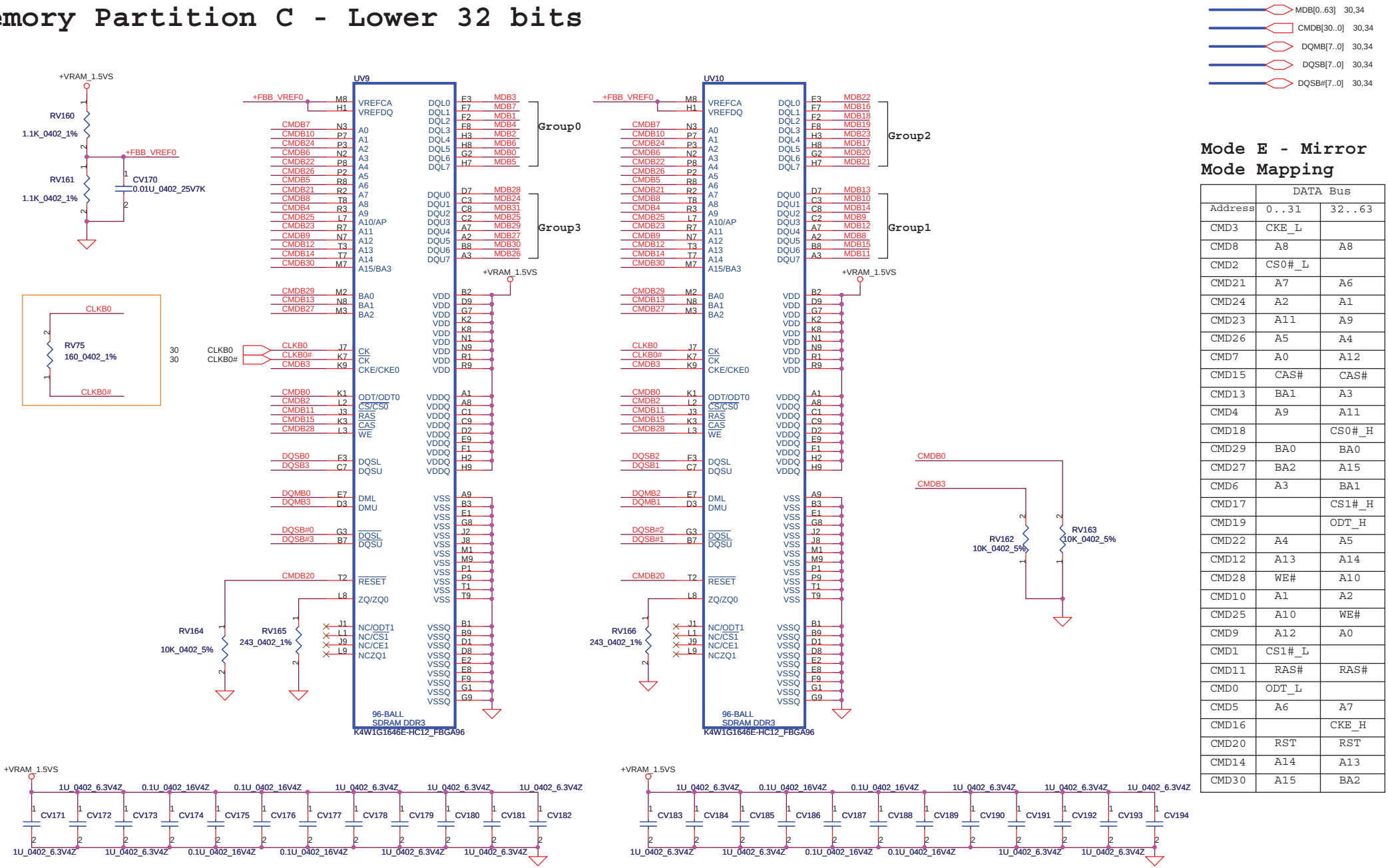
Compal Electronics, Inc.

Title: VGA(9/12)-VRAM A Upper

Size	Document Number	Rev
	LA-7391P	0.2

Date: Thursday, April 07, 2011 | Sheet 32 of 64

Memory Partition C - Lower 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: VGA(10/12)-VRAM C Lower

Size: Custom | Document Number: LA-7391P | Rev: 0.2

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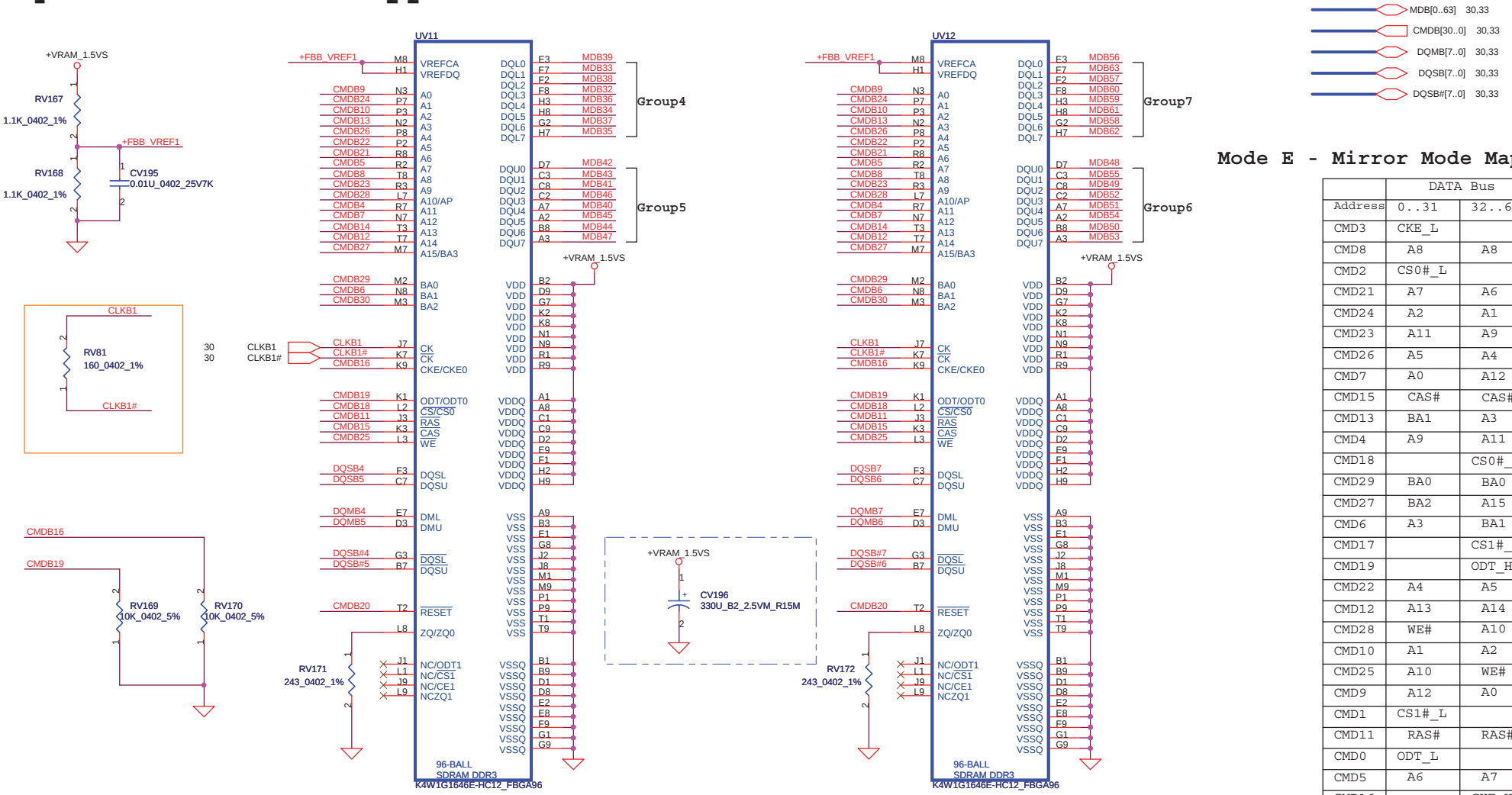
Memory Partition C - Upper 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: VGA(11/12)-VRAM C Upper

Size	Document Number	Rev
Custom	LA-7391P	0.2

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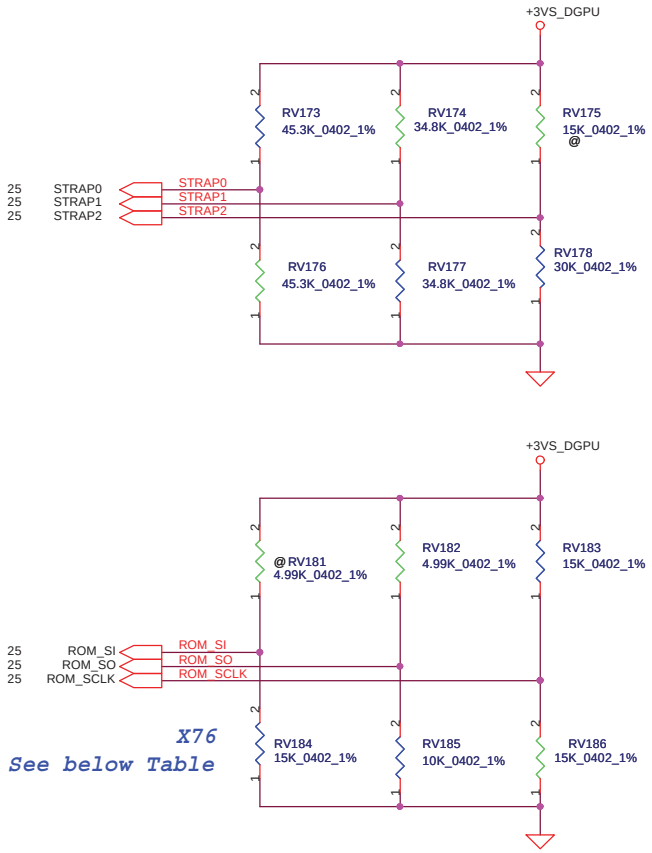


Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

ROM_SO : PL10K
Strap1 : PL35K
Strap0 : PH45K

Hynix	64Mx16 H5TQ1G63DFR-11C SA0000324E0	0010	PD 15K
	128MX16 H5TQ2G63BFR-11C SA00003YO00	0110	PD 35K
Samsung	64MX16 K4W1G1646E-HC11 SA000041T00	0011	PD 20K
	128M16 K4W2G1646C-HC11 SA000047Q00	0111	PD 45K

	DeviceID	ROM_SCLK	STRAP2
N12P-GV1		Pull up 15K	Pull down 45K
N12P-GE		Pull up 15K	Pull down 30K
N12P-GS		Pull up 15K	Pull down 25K

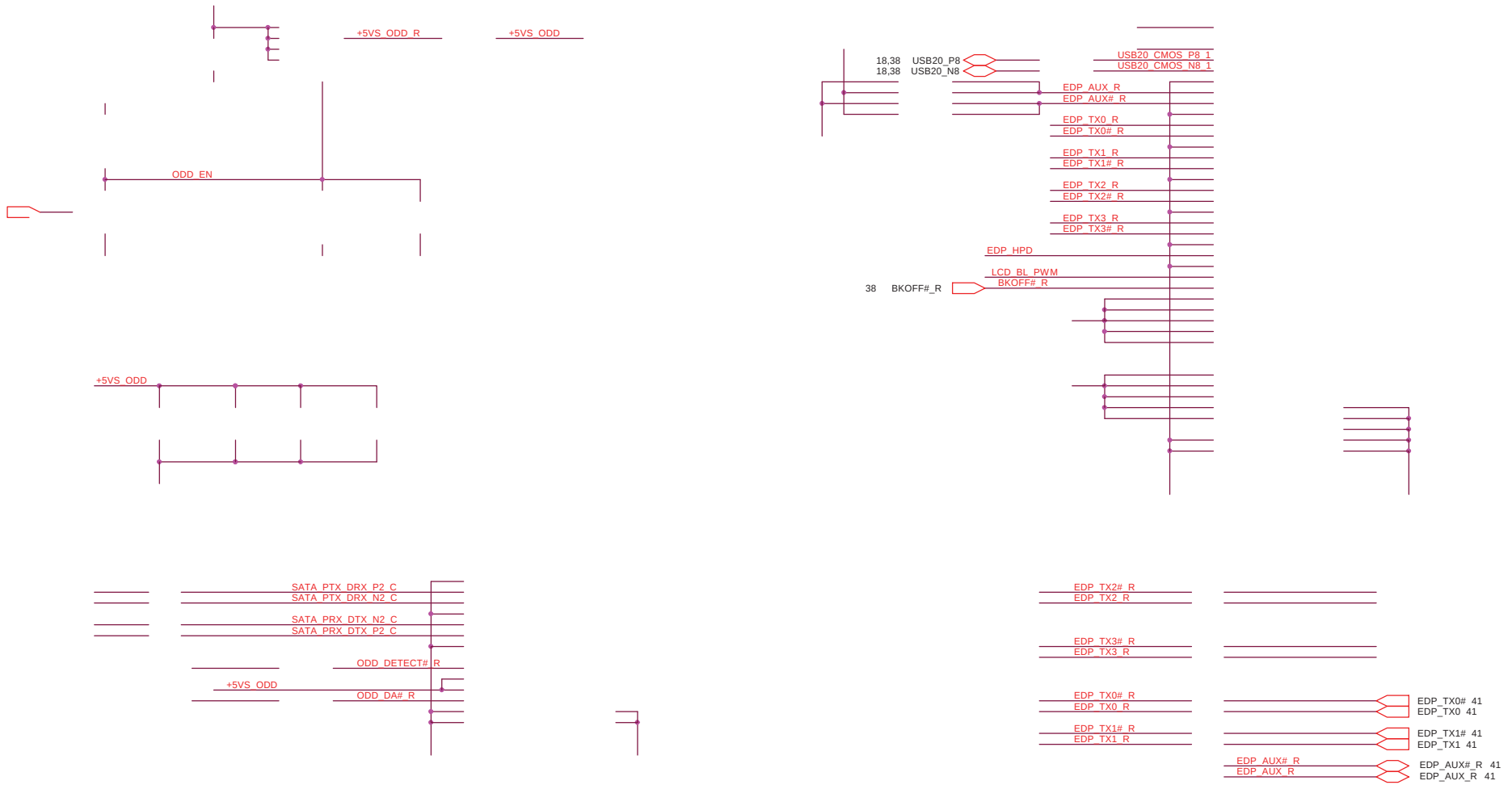
Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

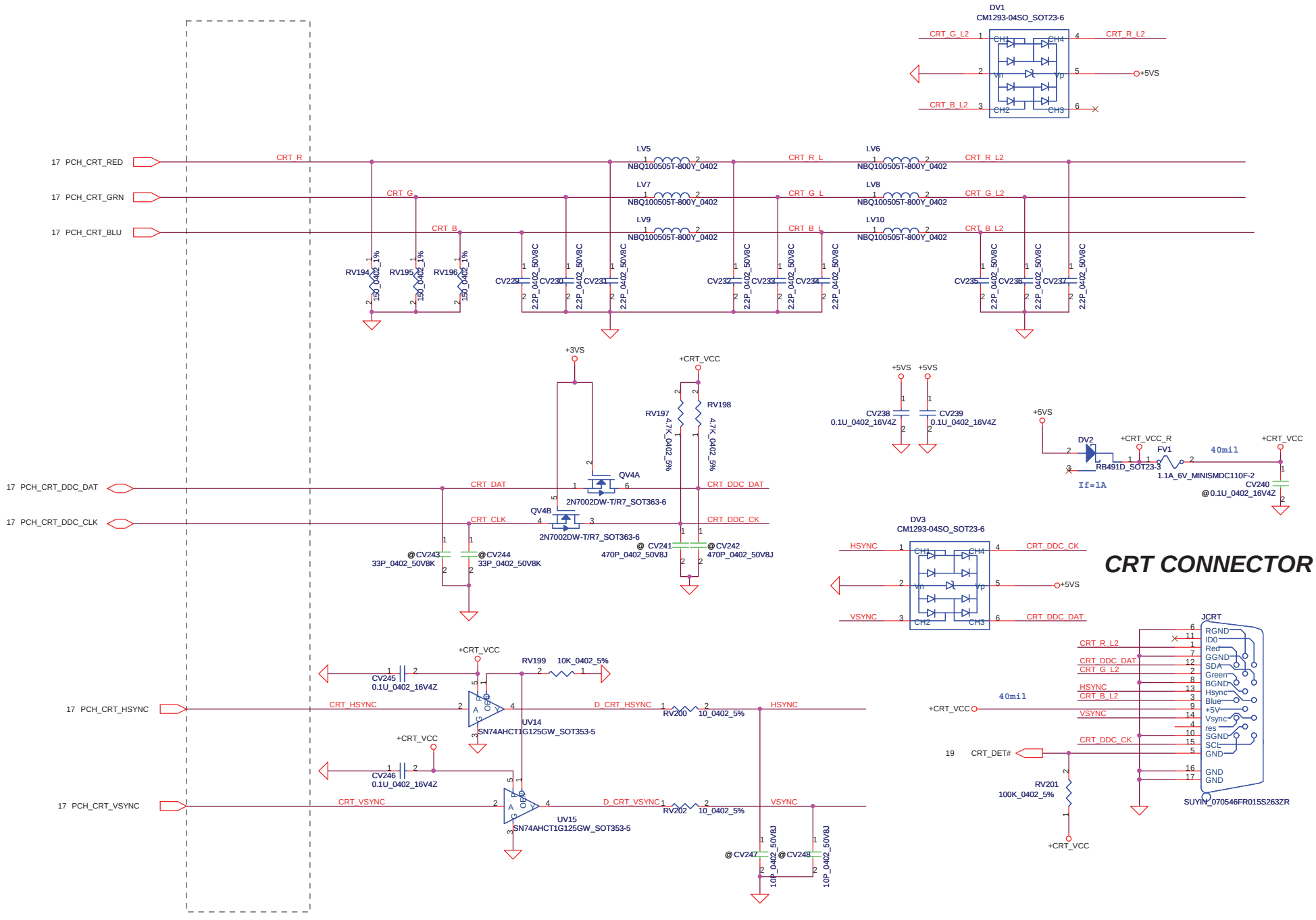
Compal Electronics, Inc.

Title: VGA(12/12)-MISC

Size: Custom | Document Number: LA-7391P | Rev: 0.2

Date: Thursday, April 07, 2011 | Sheet 35 of 64


+5VS_ODD_R
+5VS_ODD
ODD_EN
+5VS_ODD
18,38 USB20_P8
18,38 USB20_N8
USB20_CMOS_P8_1
USB20_CMOS_N8_1
EDP_AUX_R
EDP_AUX#_R
EDP_TX0_R
EDP_TX0#_R
EDP_TX1_R
EDP_TX1#_R
EDP_TX2_R
EDP_TX2#_R
EDP_TX3_R
EDP_TX3#_R
EDP_HPD
LCD_BL_PWM
38 BKOFF#_R
BKOFF#_R
SATA_PTX_DRX_P2_C
SATA_PTX_DRX_N2_C
SATA_PRX_DTX_N2_C
SATA_PRX_DTX_P2_C
ODD_DETECT#_R
+5VS_ODD
ODD_DA#_R
EDP_TX2#_R
EDP_TX2_R
EDP_TX3#_R
EDP_TX3_R
EDP_TX0#_R
EDP_TX0_R
EDP_TX1#_R
EDP_TX1_R
EDP_AUX#_R
EDP_AUX_R
EDP_TX0# 41
EDP_TX0 41
EDP_TX1# 41
EDP_TX1 41
EDP_AUX#_R 41
EDP_AUX_R 41



CRT CONNECTOR

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title	CRT		
Size	Document Number		Rev
	LA-7391P		0.2
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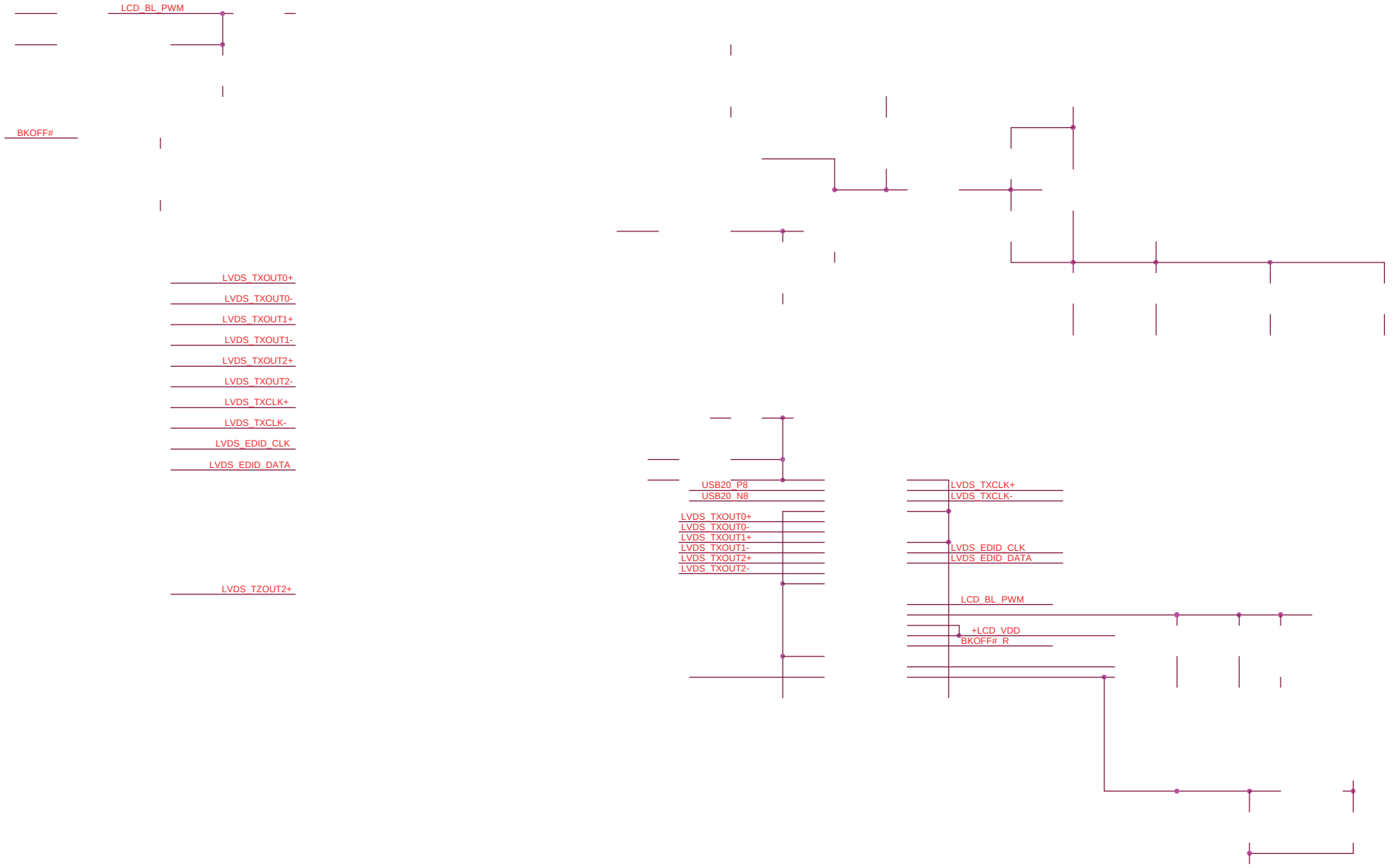
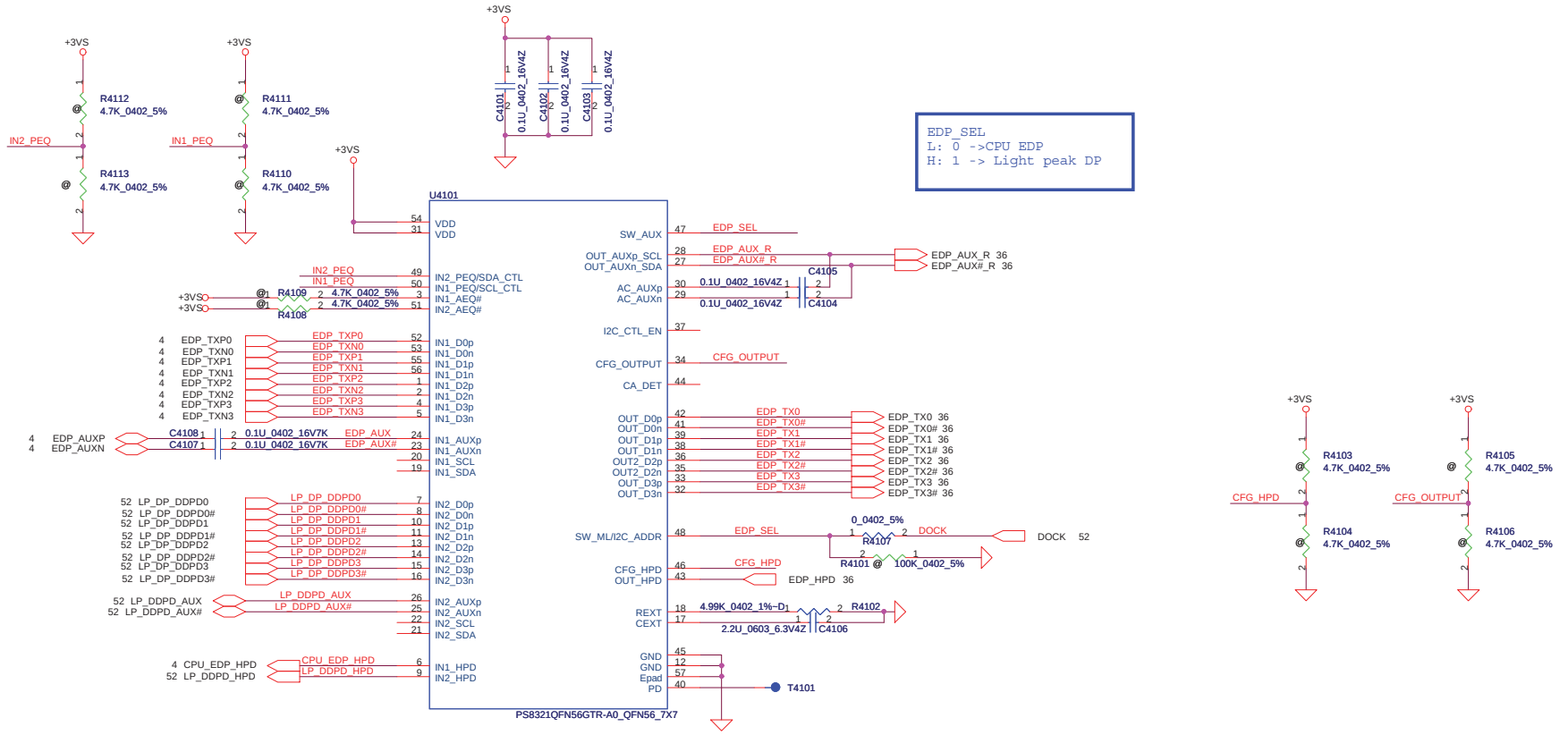

LCD_BL_PWM
BKOFF#
LVDS_TXOUT0+
LVDS_TXOUT0-
LVDS_TXOUT1+
LVDS_TXOUT1-
LVDS_TXOUT2+
LVDS_TXOUT2-
LVDS_TXCLK+
LVDS_TXCLK-
LVDS_EDID_CLK
LVDS_EDID_DATA
LVDS_TZOUT2+
USB20_P8
USB20_N8
LVDS_TXOUT0+
LVDS_TXOUT0-
LVDS_TXOUT1+
LVDS_TXOUT1-
LVDS_TXOUT2+
LVDS_TXOUT2-
LVDS_TXCLK+
LVDS_TXCLK-
LVDS_EDID_CLK
LVDS_EDID_DATA
LCD_BL_PWM
+LCD_VDD
BKOFF#_R



Security Classification	Compal Secret Data		
Issued Date	2010/04/26	Deciphered Date	2010/05/28

Compal Electronics, Inc.

Title: LP to EDP

Size	Document Number	Rev
Custom	LA-7391P	0.2

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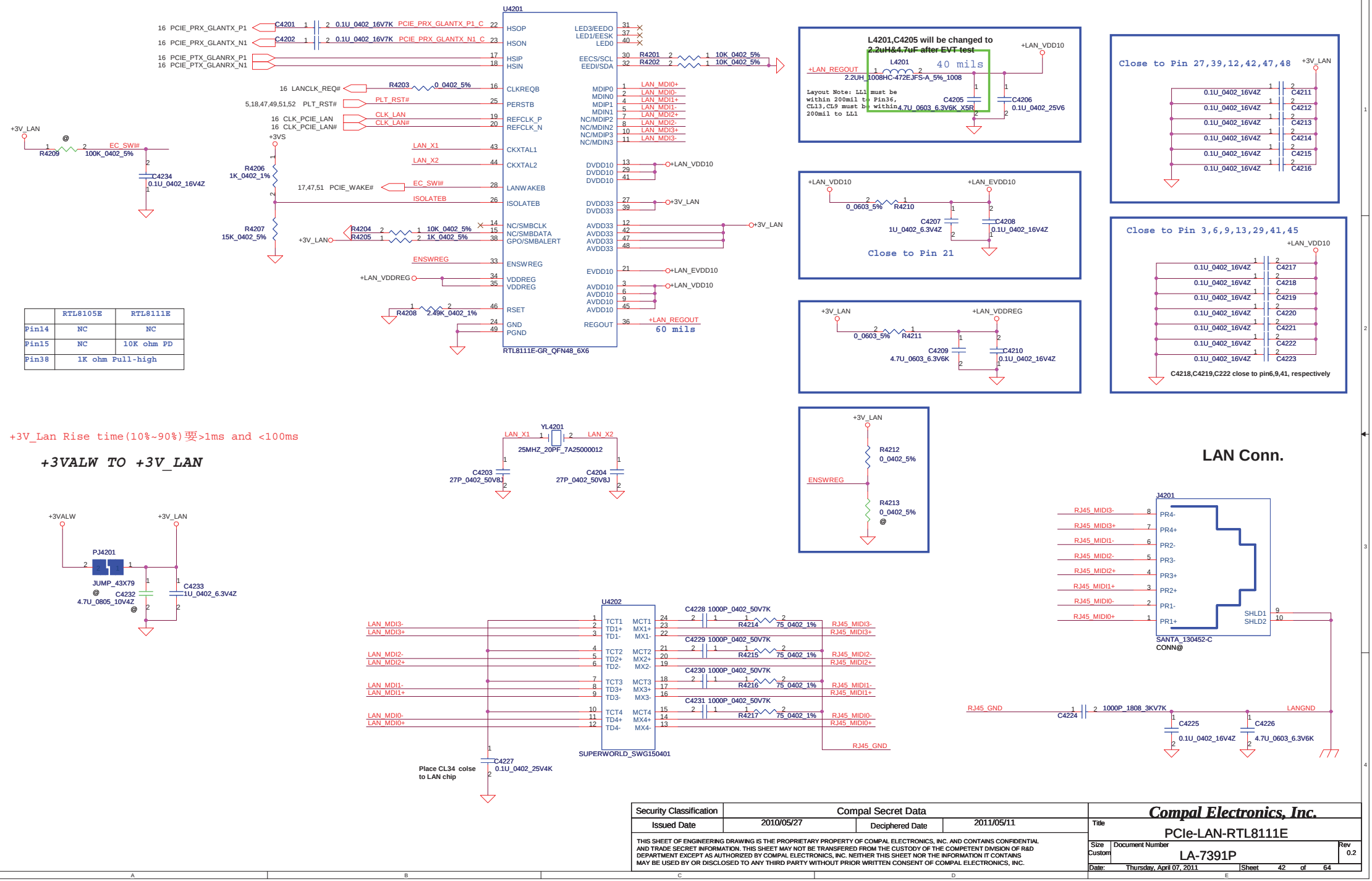


	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	

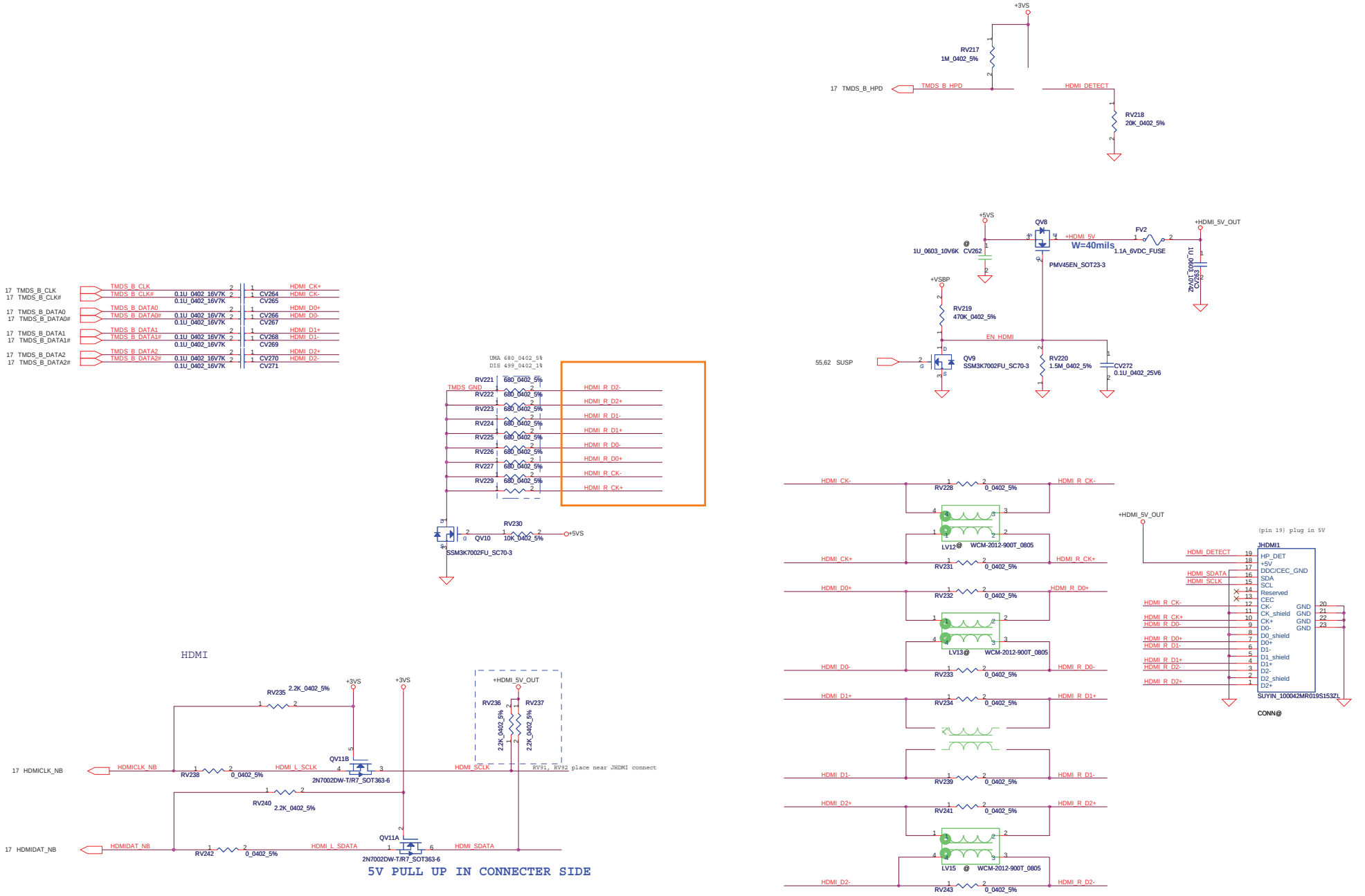
Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: PCIe-LAN-RTL8111E

Size: Custom | Document Number: LA-7391P | Rev: 0.2

Date: Thursday, April 07, 2011 | Sheet 42 of 64



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
C	LA-7391P	0.2

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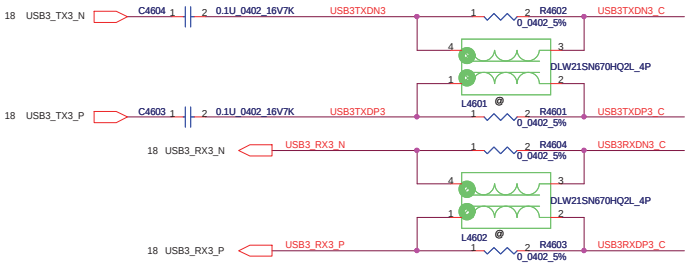
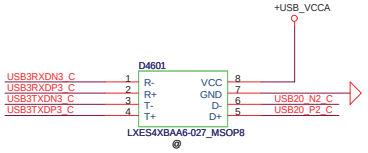
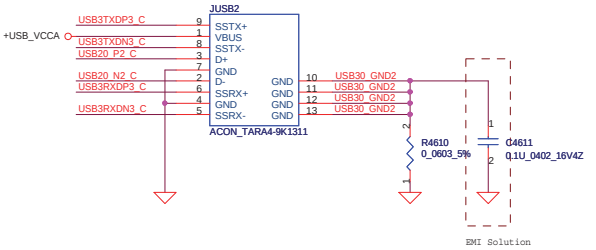
Function Board

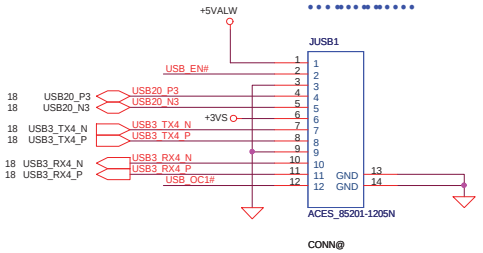
HeadPhone/LINE Out JACK

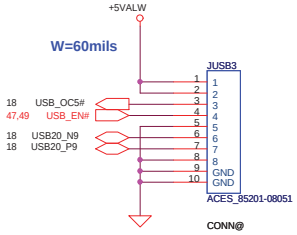
Ext.MIC/LINE IN JACK

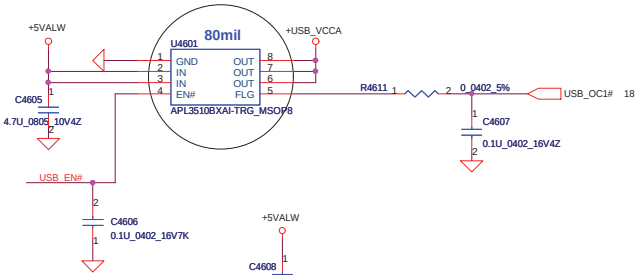


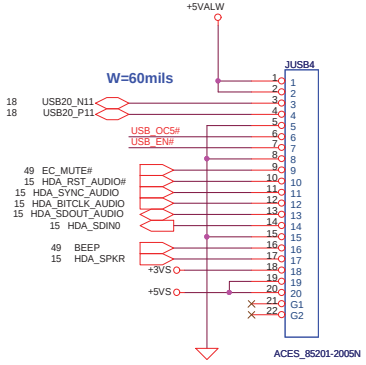


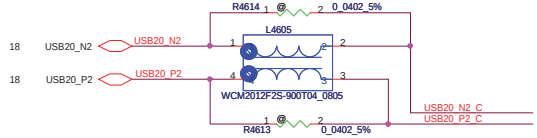












Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: USB2/USB3/AUDIO

Size	Document Number	Rev
Custom	LA-7391P	0.2

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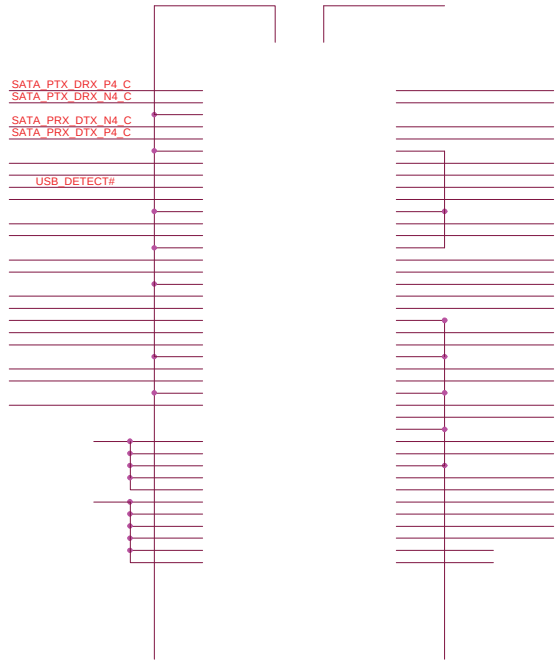
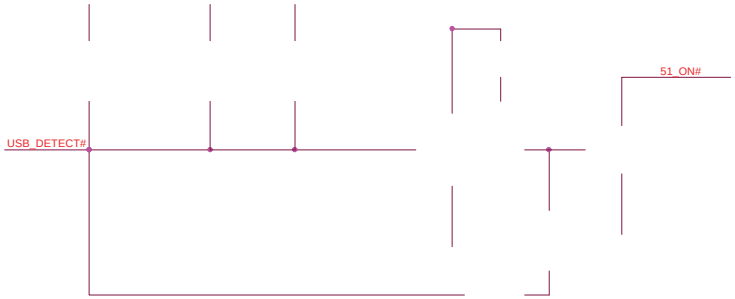
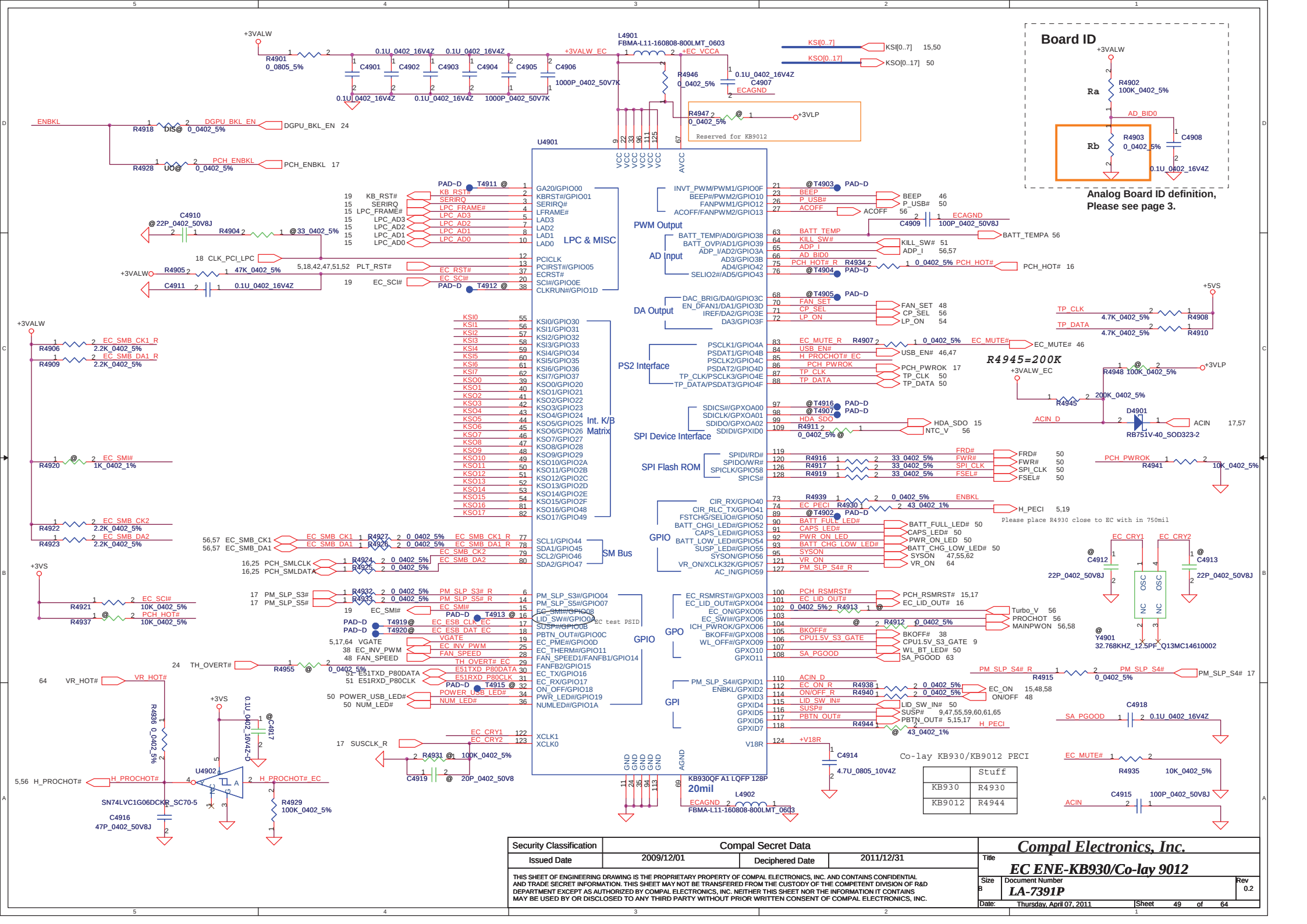
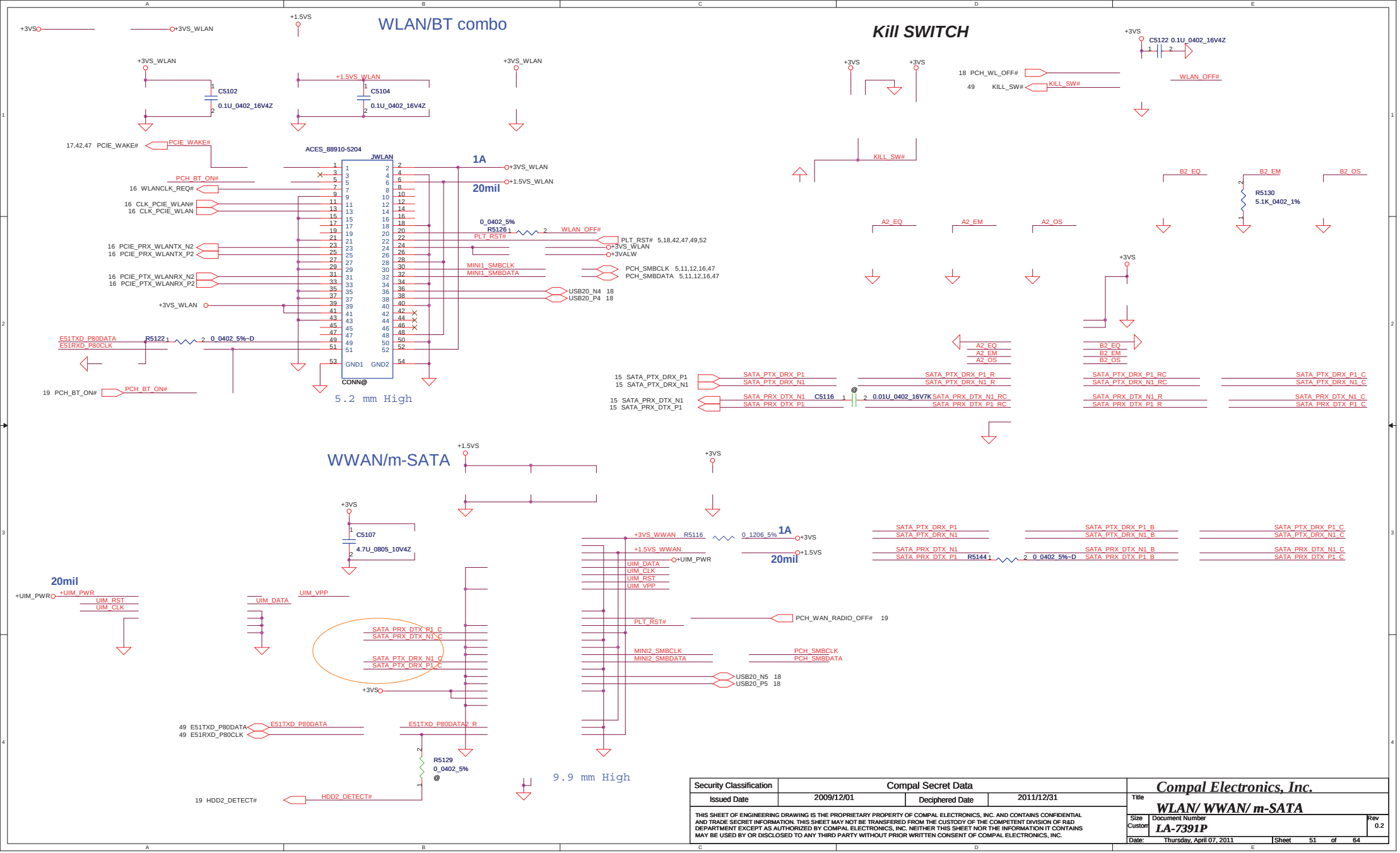

SATA_PTX_DRX_P4_C
SATA_PTX_DRX_N4_C
SATA_PRX_DTX_N4_C
SATA_PRX_DTX_P4_C
USB_DETECT#


51_ON#
USB_DETECT#


Board ID
Analog Board ID definition, Please see page 3.
U4901
KB930QF A1 LQFP 128P
20mil
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI
R4945=200K
Co-lay KB930/KB9012 PECI
KB930 R4930
KB9012 R4944
Compal Electronics, Inc.
EC ENE-KB930/Co-lay 9012
LA-7391P
Security Classification Compal Secret Data
Issued Date 2009/12/01
Deciphered Date 2011/12/31
Thursday, April 07, 2011
Sheet 49 of 64


WLAN/BT combo
Kill SWITCH
WWAN/m-SATA
ACES_88910-5204
JWLAN
CONN@
5.2 mm High
9.9 mm High
20mil
1A
C5102
0.1U_0402_16V4Z
C5104
0.1U_0402_16V4Z
C5122 0.1U_0402_16V4Z
R5126
0_0402_5%
R5122
0_0402_5%~D
R5130
5.1K_0402_1%
C5116
0.01U_0402_16V7K
C5107
4.7U_0805_10V4Z
R5129
0_0402_5%
R5116
0_1206_5%
R5144
0_0402_5%~D
Security Classification
Compal Secret Data
Issued Date
2009/12/01
Deciphered Date
2011/12/31
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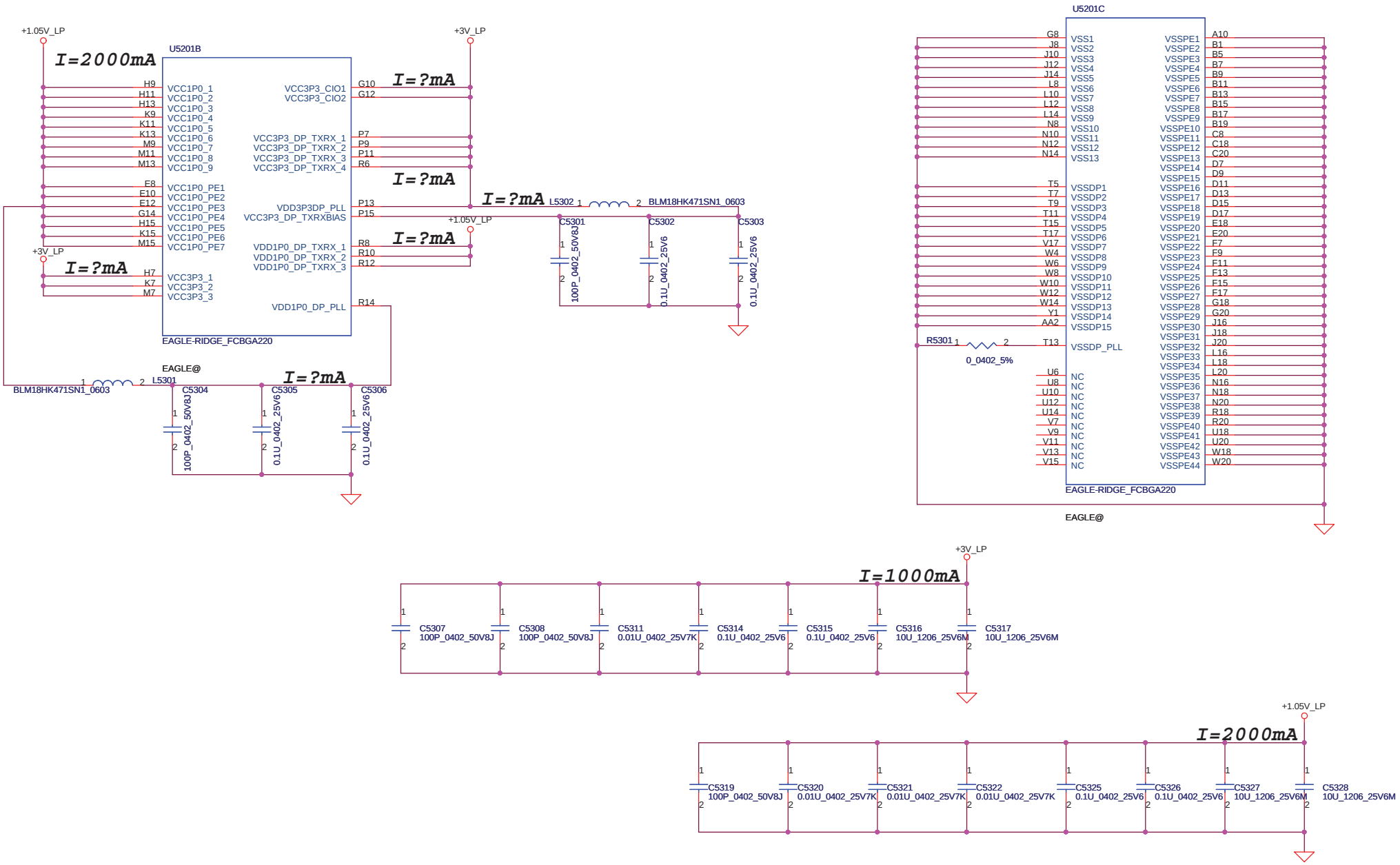
Compal Electronics, Inc.
Title
WLAN/ WWAN/ m-SATA
Size
Custom
Document Number
LA-7391P
Rev
0.2
Date: Thursday, April 07, 2011
Sheet 51 of 64



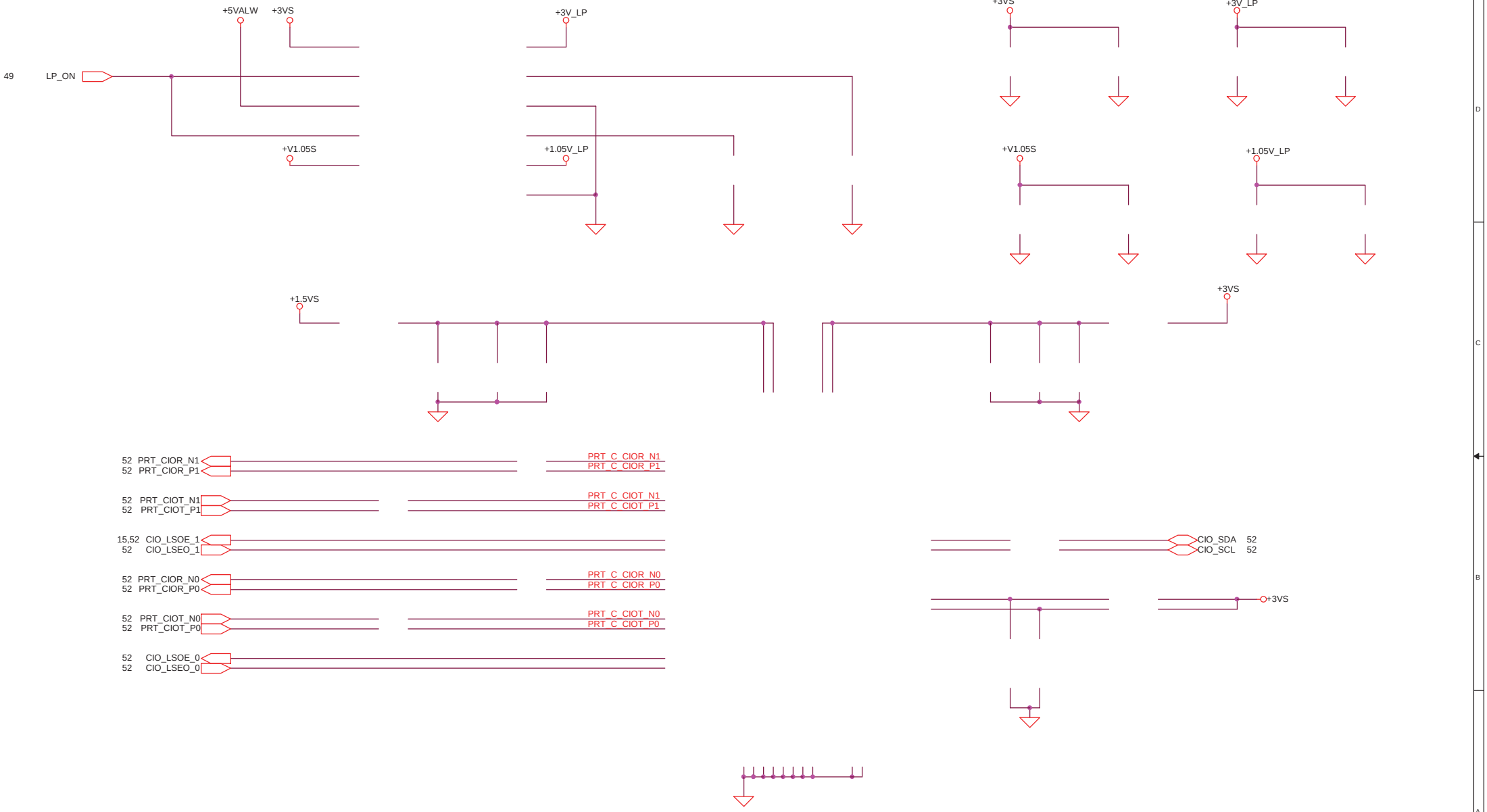
Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: **EAGLE RIDGE (PWR)**

Size	Document Number	Rev
Custom	LA-7391P	0.2

Date: Thursday, April 07, 2011 | Sheet 53 of 64



Security Classification	Compal Secret Data
	Title
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	Date: / Sheet of

DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME

need confirm: ME give us battery
connector P/N is DC040000800

90W

PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

VIN
ADPIN
+3VLP
+3VS
5,49 H_PROCHOT#
ADP_OCP_1
OTP_N_003
49 PROCHOT
MAINPWON 49,58
49,57 ADP_I
OTP_N_002
Turbo_V
ADP_OCP_2
NTC_V
CP_SEL
49

VMB
BATT+
B/I
TS_A
EC_SMDA
EC_SMCA
GND
EC_SMB_CK1 49,57
EC_SMB_DA1 49,57
+3VALW
BATT_TEMPA 49

B+
+VSBP
VL
VSB_N_001
VSB_N_003
VSB_N_002
58 POK
+CHGRTC

RTC Battery
+RTCBATT1
+RTCBATT2
+RTCBATT
Must close PBJ1
SP093MX0000
Change RTC For Cost Down

VIN
BATT+
VS_N_001
N1
VS
47,48,50 51_ON#
VS_N_002

Pre_chg
VIN
B+
49 ACOFF
+5VALW

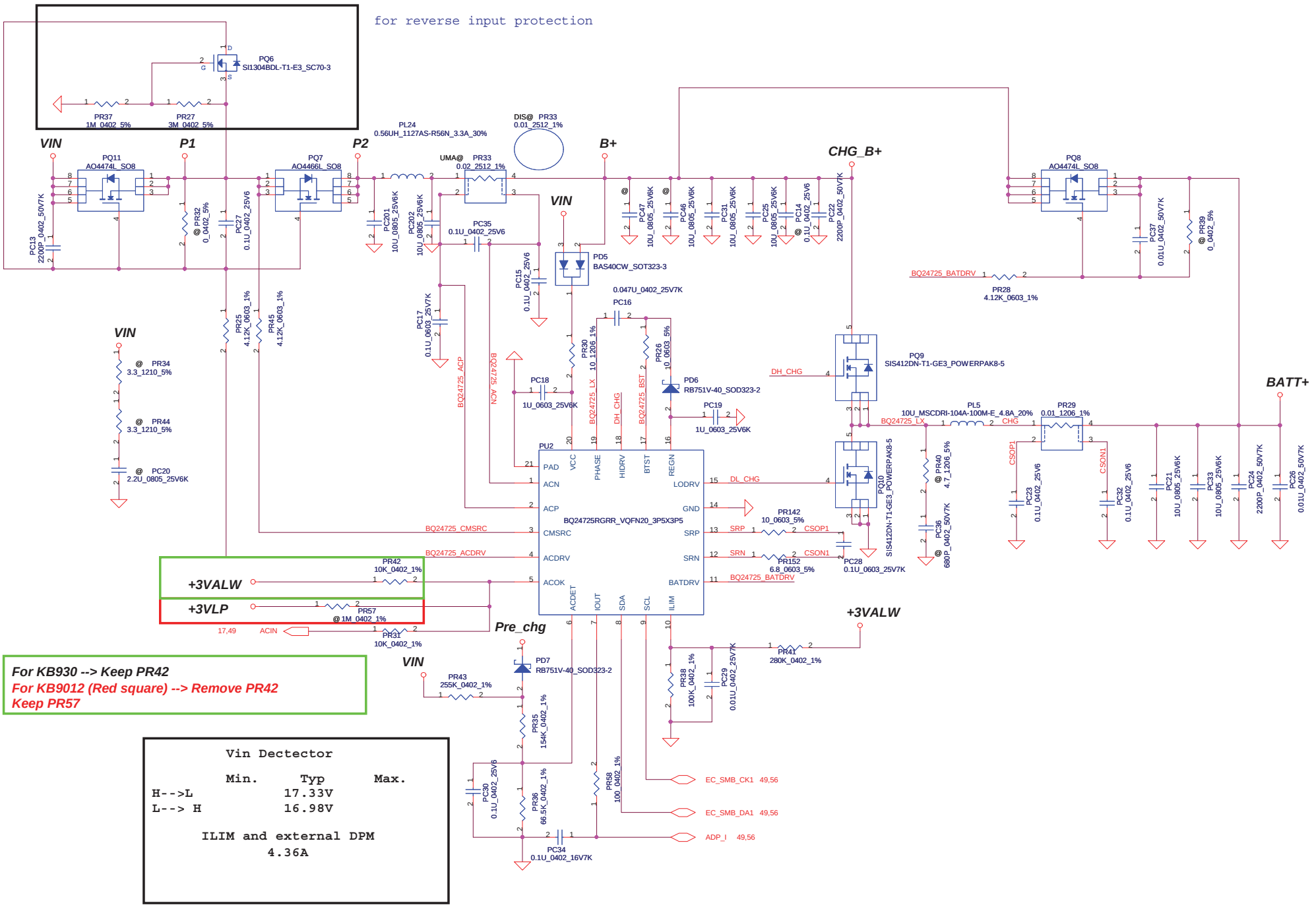
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: PWR-DCIN / BATT CONN / OTP

Size | Document Number: PBL22 LA-7391P M/B | Rev: 0.1

Date: Thursday, April 07, 2011 | Sheet 56 of 68



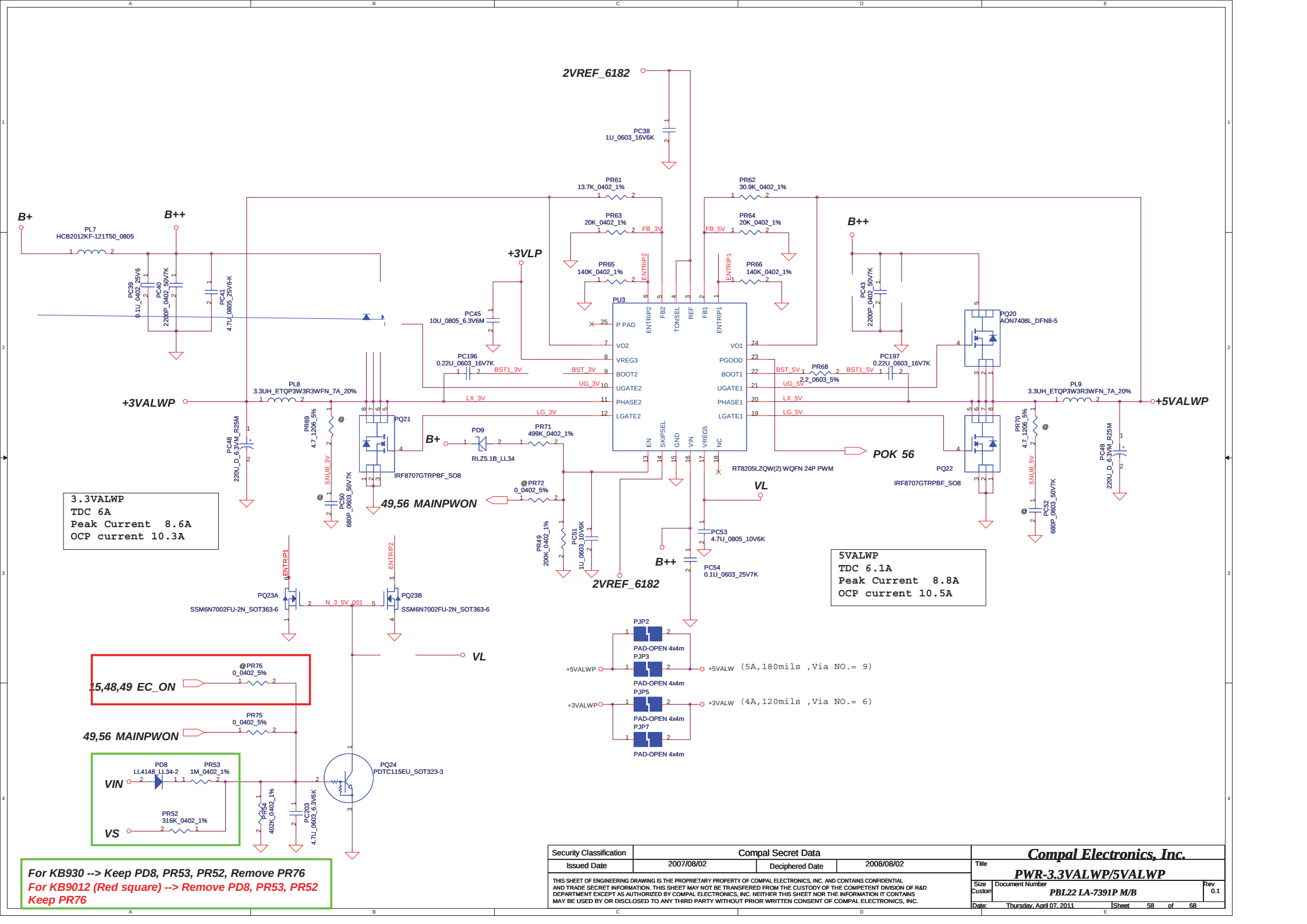
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **PWR-CHARGER**

Size	Document Number	Rev
	PBL22 LA-7391P M/B	0.1

Date: Thursday, April 07, 2011 Sheet 57 of 68


2VREF_6182
PC38 1U_0603_16V6K
PR61 13.7K_0402_1%
PR62 30.9K_0402_1%
PR63 20K_0402_1%
PR64 20K_0402_1%
PR65 140K_0402_1%
PR66 140K_0402_1%
B+
B++
PL7 HCB2012KF-121T50_0805
PC39 0.1U_0402_25V6
PC40 2200P_0402_50V7K
PC41 4.7U_0805_25V6-K
+3VLP
PC45 10U_0805_6.3V6M
PU3
P PAD
VO2
VREG3
BOOT2
UGATE2
PHASE2
LGATE2
VO1
PGOOD
BOOT1
UGATE1
PHASE1
LGATE1
EN
SKIPSEL
GND
VIN
VREG5
NC
RT8205LZQW(2) WQFN 24P PWM
PC196 0.22U_0603_16V7K
PC197 0.22U_0603_16V7K
PR68 2.2_0603_5%
PC43 2200P_0402_50V7K
PQ20 AON7408L_DFN8-5
PQ22 IRF8707GTRPBF_SO8
PL8 3.3UH_ETQP3W3R3WFN_7A_20%
PL9 3.3UH_ETQP3W3R3WFN_7A_20%
+3VALWP
+5VALWP
PC48 220U_D_6.3VM_R25M
PR69 4.7_1206_5%
PQ21 IRF8707GTRPBF_SO8
PD9 RLZ5.1B_LL34
PR71 499K_0402_1%
PR72 0_0402_5%
PC50 680P_0603_50V7K
PR70 4.7_1206_5%
PC52 680P_0603_50V7K
PC49 220U_D_6.3VM_R25M
POK 56
49,56 MAINPWON
VL
PR49 200K_0402_1%
PC51 1U_0603_10V6K
PC53 4.7U_0805_10V6K
PC54 0.1U_0603_25V7K
3.3VALWP
TDC 6A
Peak Current 8.6A
OCP current 10.3A
5VALWP
TDC 6.1A
Peak Current 8.8A
OCP current 10.5A
PQ23A SSM6N7002FU-2N_SOT363-6
PQ23B SSM6N7002FU-2N_SOT363-6
N_3_5V_001
PJP2 PAD-OPEN 4x4m
PJP3 PAD-OPEN 4x4m
PJP5 PAD-OPEN 4x4m
PJP7 PAD-OPEN 4x4m
+5VALW (5A,180mils ,Via NO.= 9)
+3VALW (4A,120mils ,Via NO.= 6)
15,48,49 EC_ON
@PR76 0_0402_5%
PR75 0_0402_5%
49,56 MAINPWON
VIN
VS
PD8 LL4148_LL34-2
PR53 1M_0402_1%
PR52 316K_0402_1%
PR54 402K_0402_1%
PC203 4.7U_0603_6.3V6K
PQ24 PDTC115EU_SOT323-3
For KB930 --> Keep PD8, PR53, PR52, Remove PR76
For KB9012 (Red square) --> Remove PD8, PR53, PR52
Keep PR76
Security Classification
Compal Secret Data
Issued Date
2007/08/02
Deciphered Date
2008/08/02
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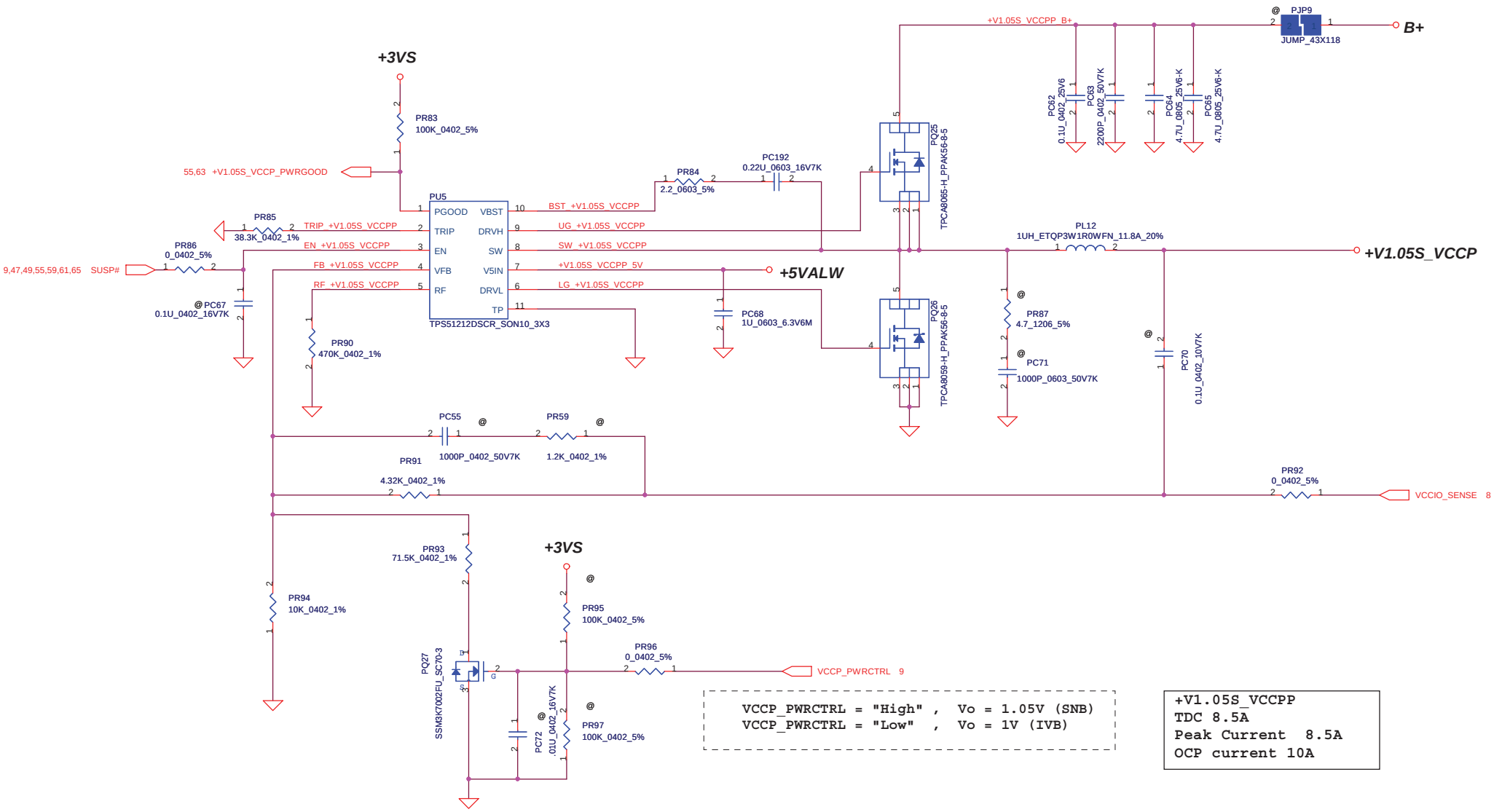
Compal Electronics, Inc.
Title
PWR-3.3VALWP/5VALWP
Size Custom
Document Number
PBL22 LA-7391P M/B
Rev 0.1
Date: Thursday, April 07, 2011
Sheet 58 of 68



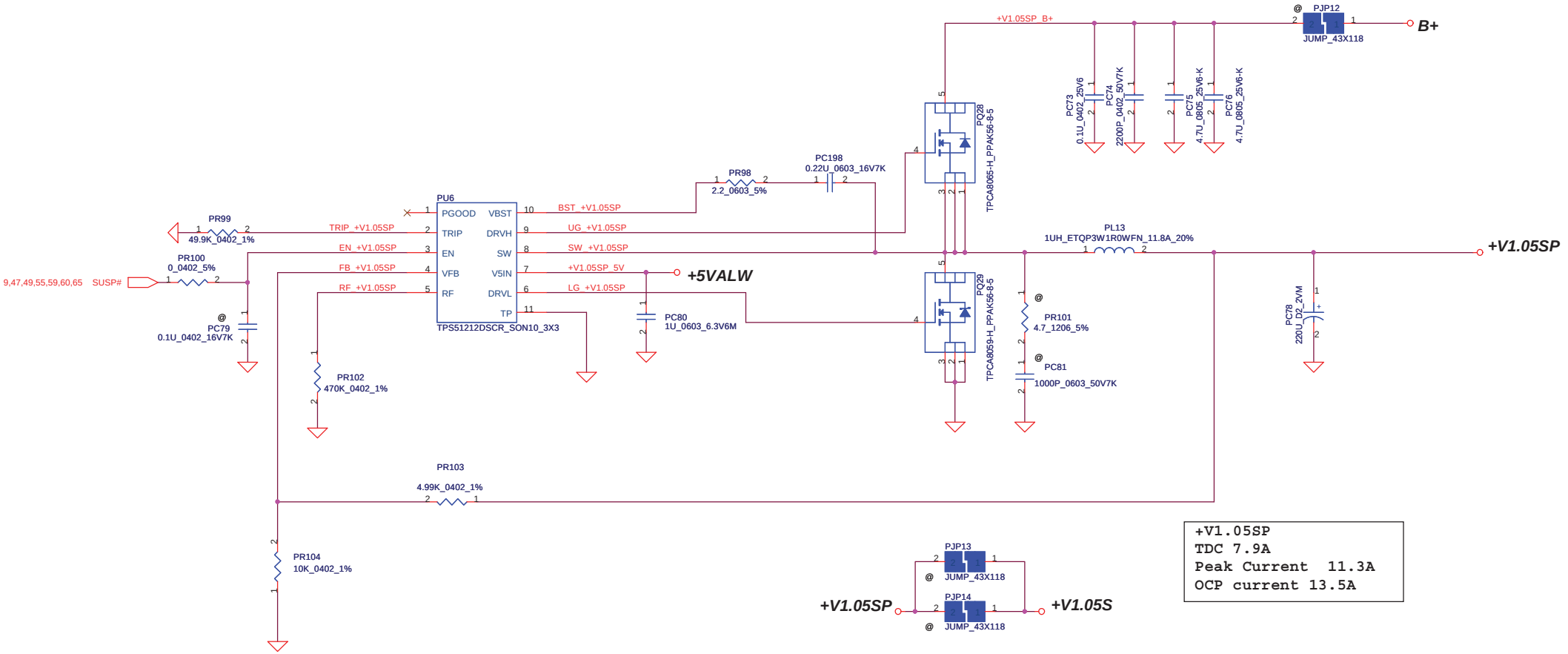
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: **PWR-V1.05S_VCCP**

Size	Document Number	Rev
Custom	PBL22 LA-7391P M/B	0.1

Date: Thursday, April 07, 2011 | Sheet 60 of 68



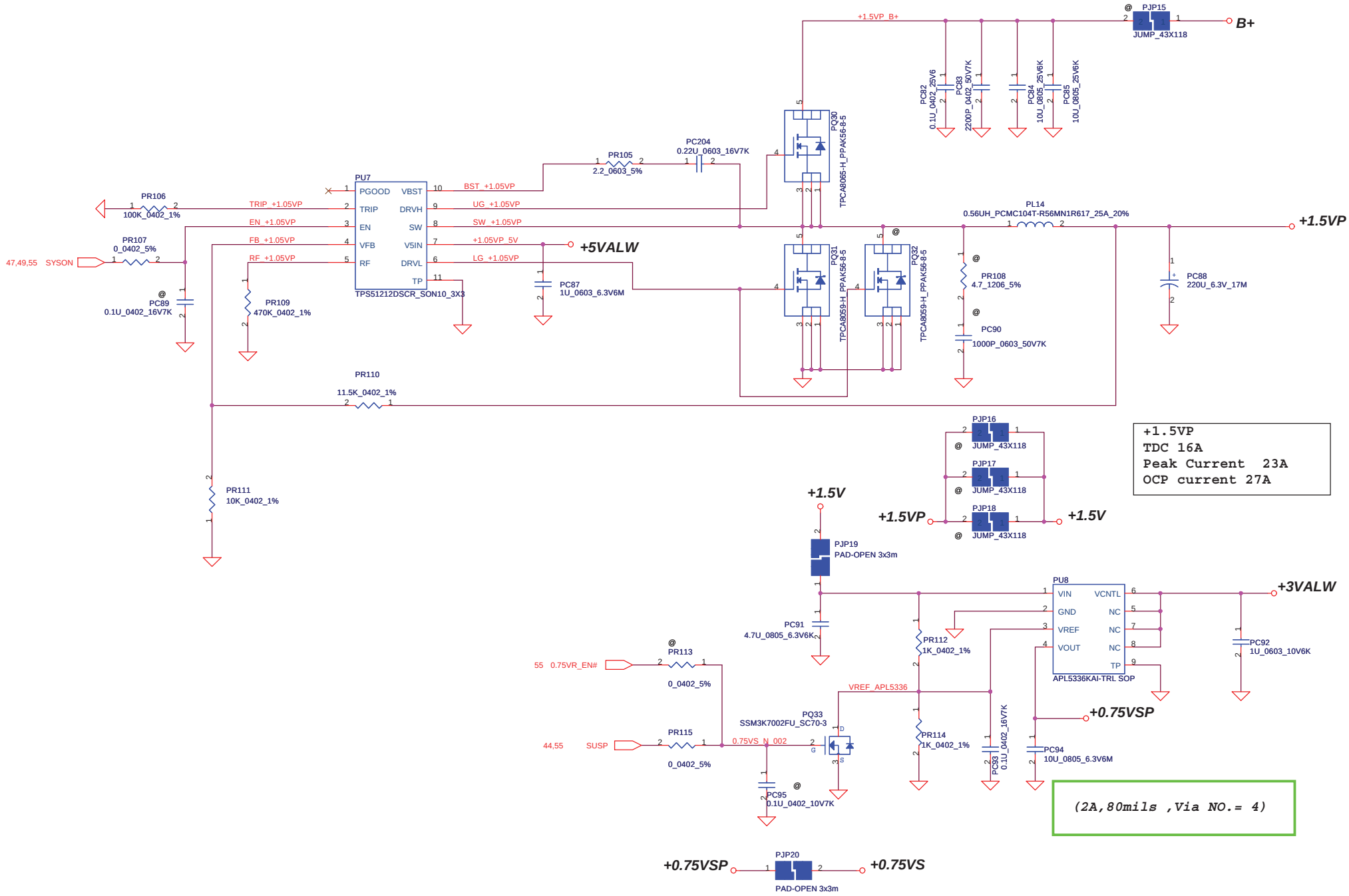
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: **PWR-V1.05SP**

Size	Document Number	Rev
Custom	PBL22 LA-7391P M/B	0.1

Date: Thursday, April 07, 2011 Sheet 61 of 68



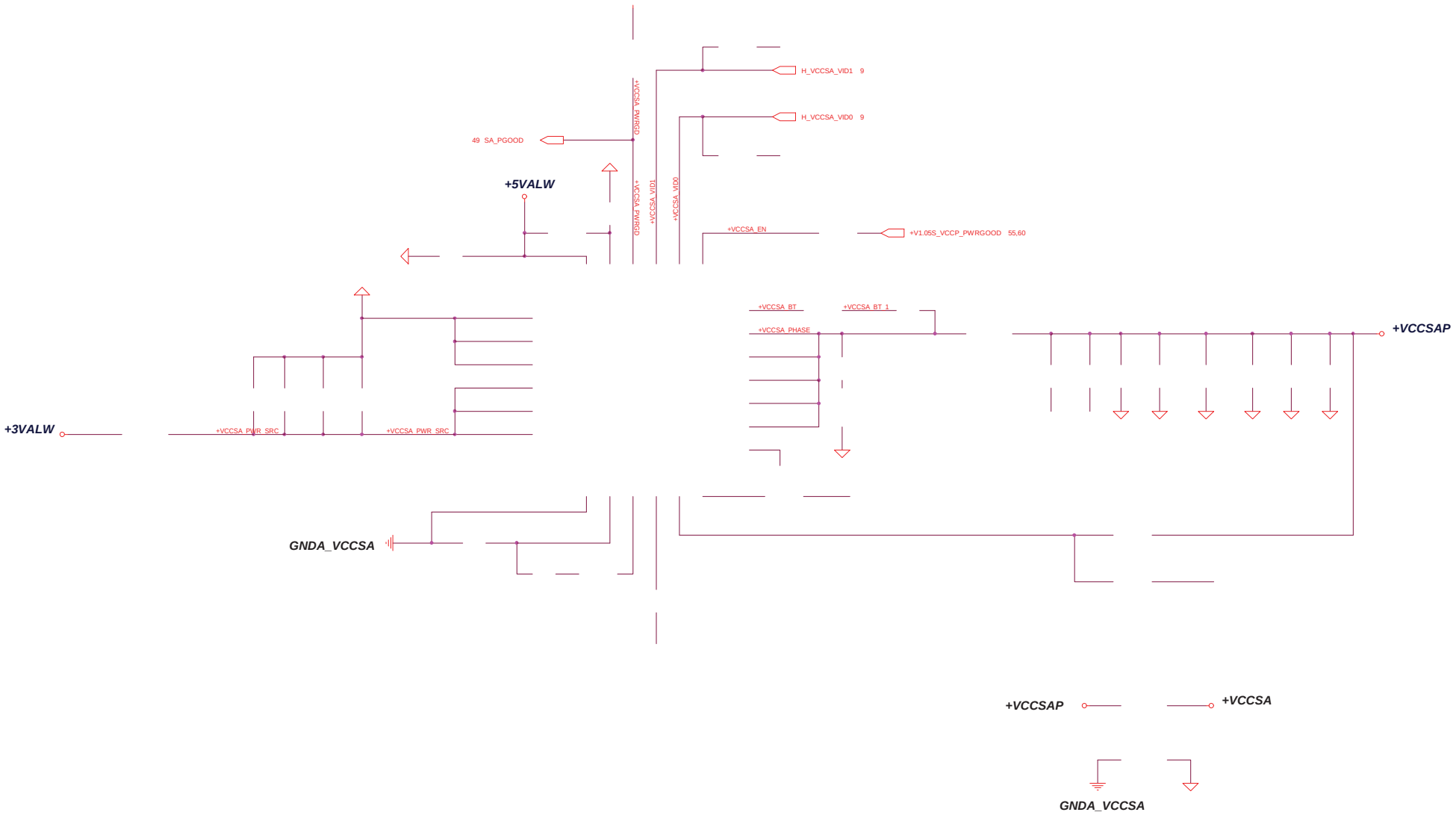
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

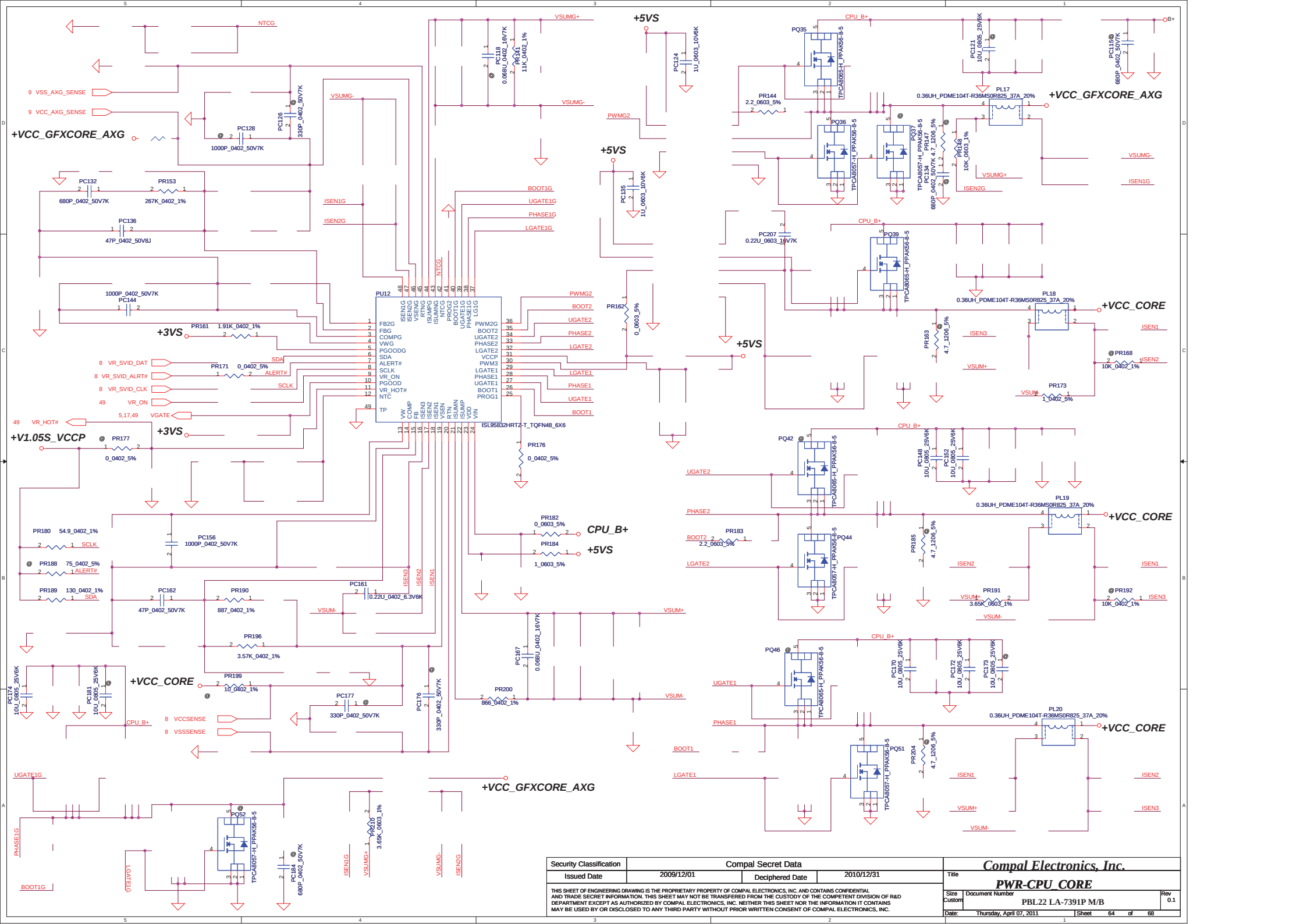
Compal Electronics, Inc.

Title: **PWR-1.5VP/0.75VSP**

Size	Document Number	Rev
Custom	PBL22 LA-7391P M/B	0.1

Date: Thursday, April 07, 2011 | Sheet 62 of 68


H_VCCSA_VID1 9
H_VCCSA_VID0 9
49 SA_PGOOD
+VCCSA_PWRGD
+VCCSA_VID1
+VCCSA_VID0
+5VALW
+VCCSA_EN
+V1.05S_VCCP_PWRGOOD 55,60
+VCCSA_BT
+VCCSA_BT_1
+VCCSA_PHASE
+VCCSAP
+3VALW
+VCCSA_PWR_SRC
+VCCSA_PWR_SRC
GNDA_VCCSA
+VCCSAP
+VCCSA
GNDA_VCCSA


+VCC_GFXCORE_AXG
+5VS
+3VS
+V1.05S_VCCP
+VCC_CORE
CPU_B+
PU12
ISL95832HRTZ-T_TQFN48_6X6
TPCA8065-H_PPAK56-8-5
TPCA8057-H_PPAK56-8-5
0.36UH_PDME104T-R36MS0R825_37A_20%
NTCG
VSUMG+
VSUMG-
PWMG2
BOOT1G
UGATE1G
PHASE1G
LGATE1G
ISEN1G
ISEN2G
BOOT2
UGATE2
PHASE2
LGATE2
SDA
SCLK
ALERT#
VGATE
VR_HOT#
VR_ON
VCCSENSE
VSSSENSE
VSUM+
VSUM-
ISEN1
ISEN2
ISEN3
Security Classification
Compal Secret Data
Issued Date
2009/12/01
Deciphered Date
2010/12/31
Compal Electronics, Inc.
PWR-CPU_CORE
PBL22 LA-7391P M/B
Rev 0.1
Thursday, April 07, 2011
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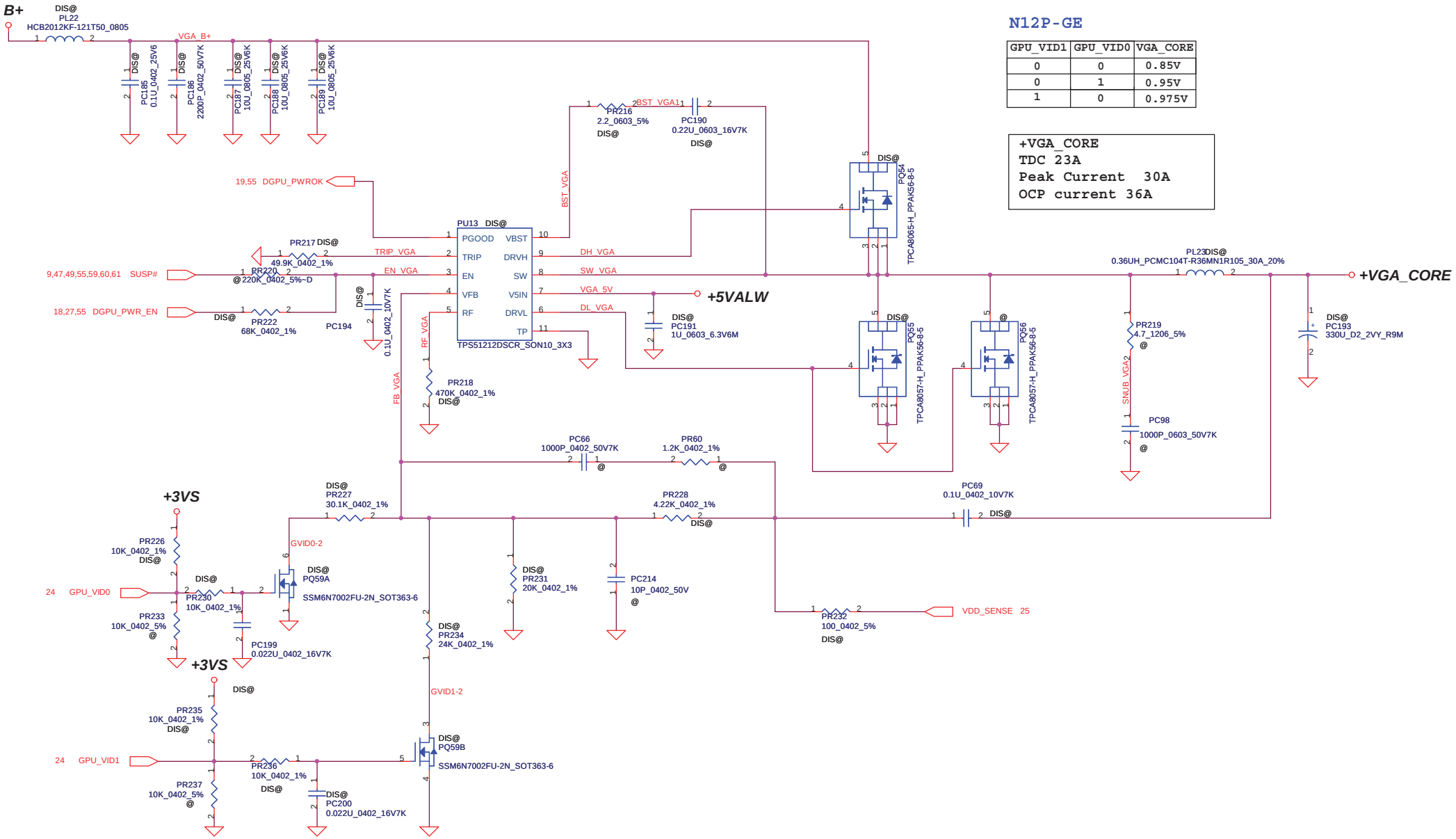


N12P-GE

GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.85V
0	1	0.95V
1	0	0.975V

+VGA_CORE
TDC 23A
Peak Current 30A
OCP current 36A

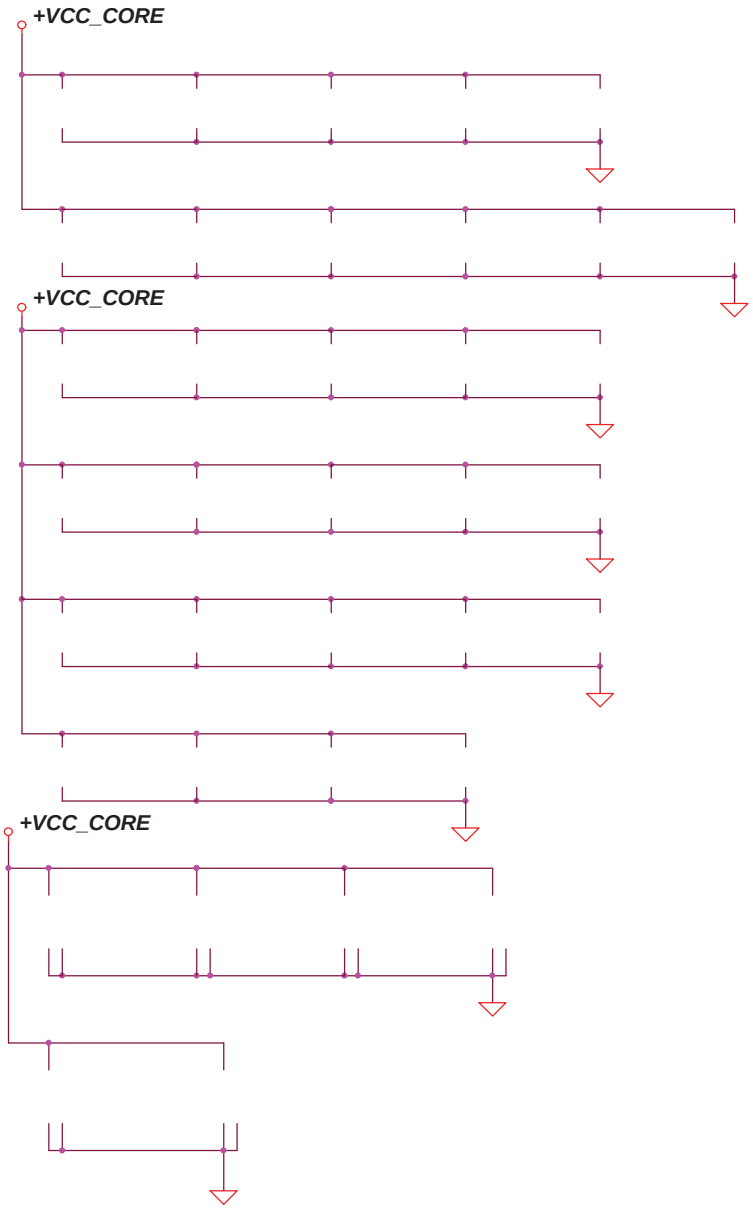
Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

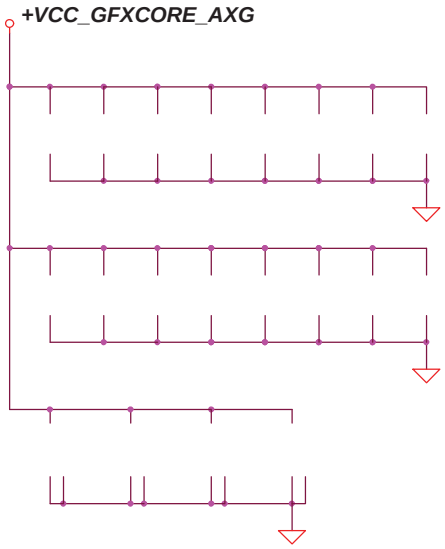
Compal Electronics, Inc.

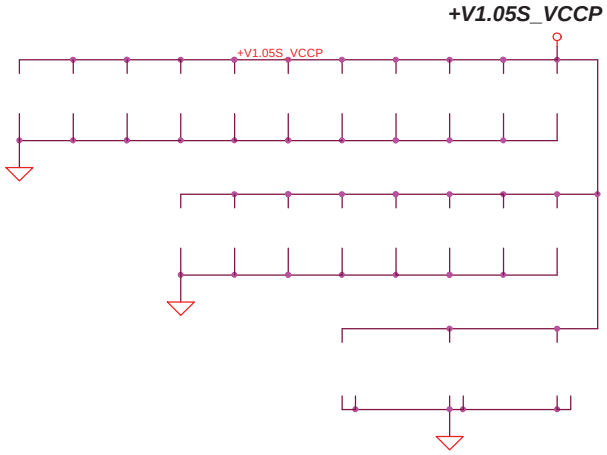
Title: PWR - VGA_COREP

Size | Document Number: PBL21 LA6771P M/B | Rev: 0.1

Date: Thursday, April 07, 2011 | Sheet 65 of 68

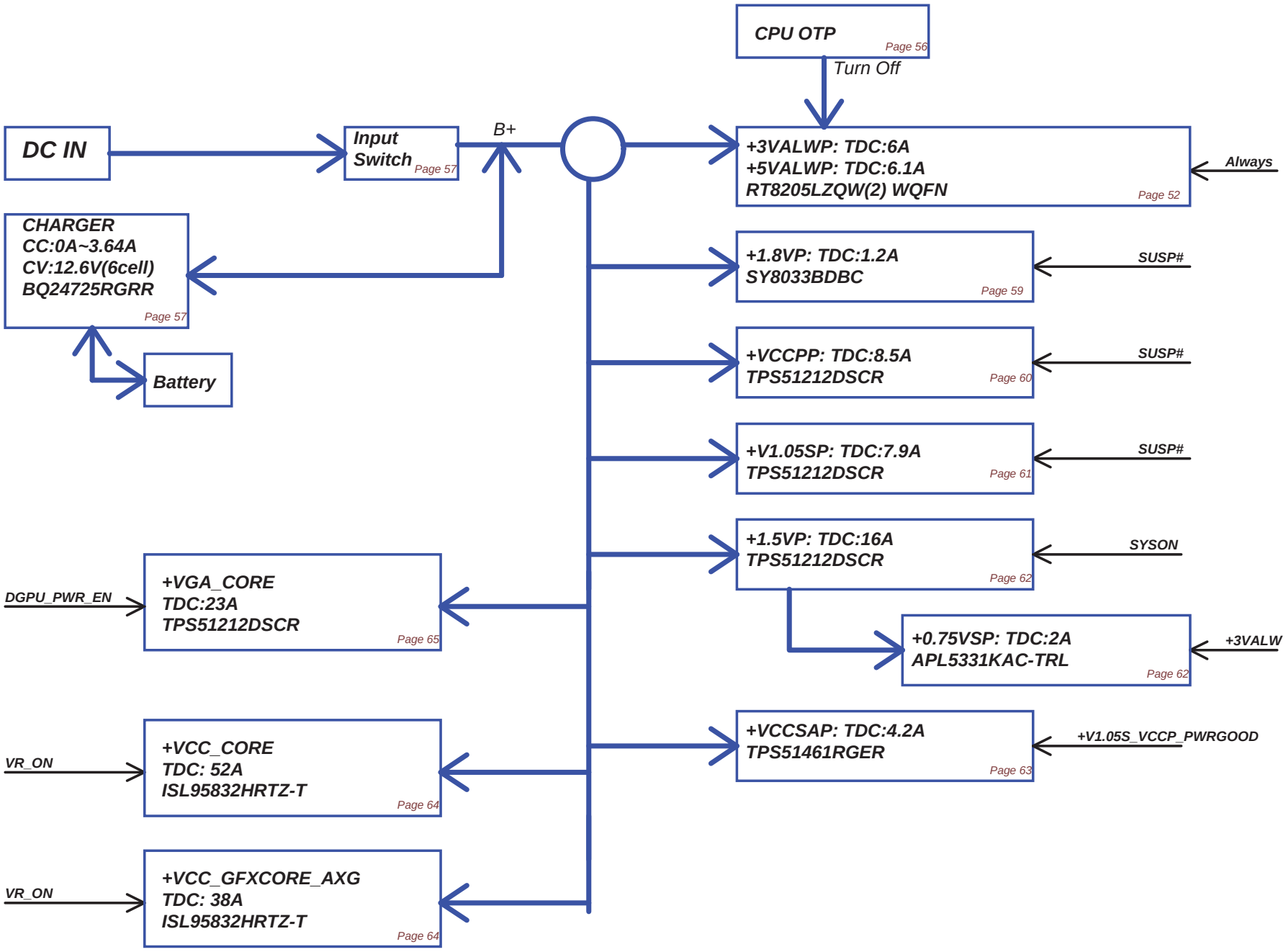

+VCC_CORE
+VCC_CORE
+VCC_CORE


+VCC_GFXCORE_AXG


+V1.05S_VCCP
+V1.05S_VCCP

Title

Power block



Security Classification	Compal Secret Data		
Issued Date	2010/08/03	Deciphered Date	2011/08/03

Compal Electronics, Inc.

Title: POWER BLOCK DIAGRAM

Size: Custom | Document Number: PBL21 LA6771P M/B | Rev: 0.1

Date: Thursday, April 07, 2011 | Sheet 67 of 68

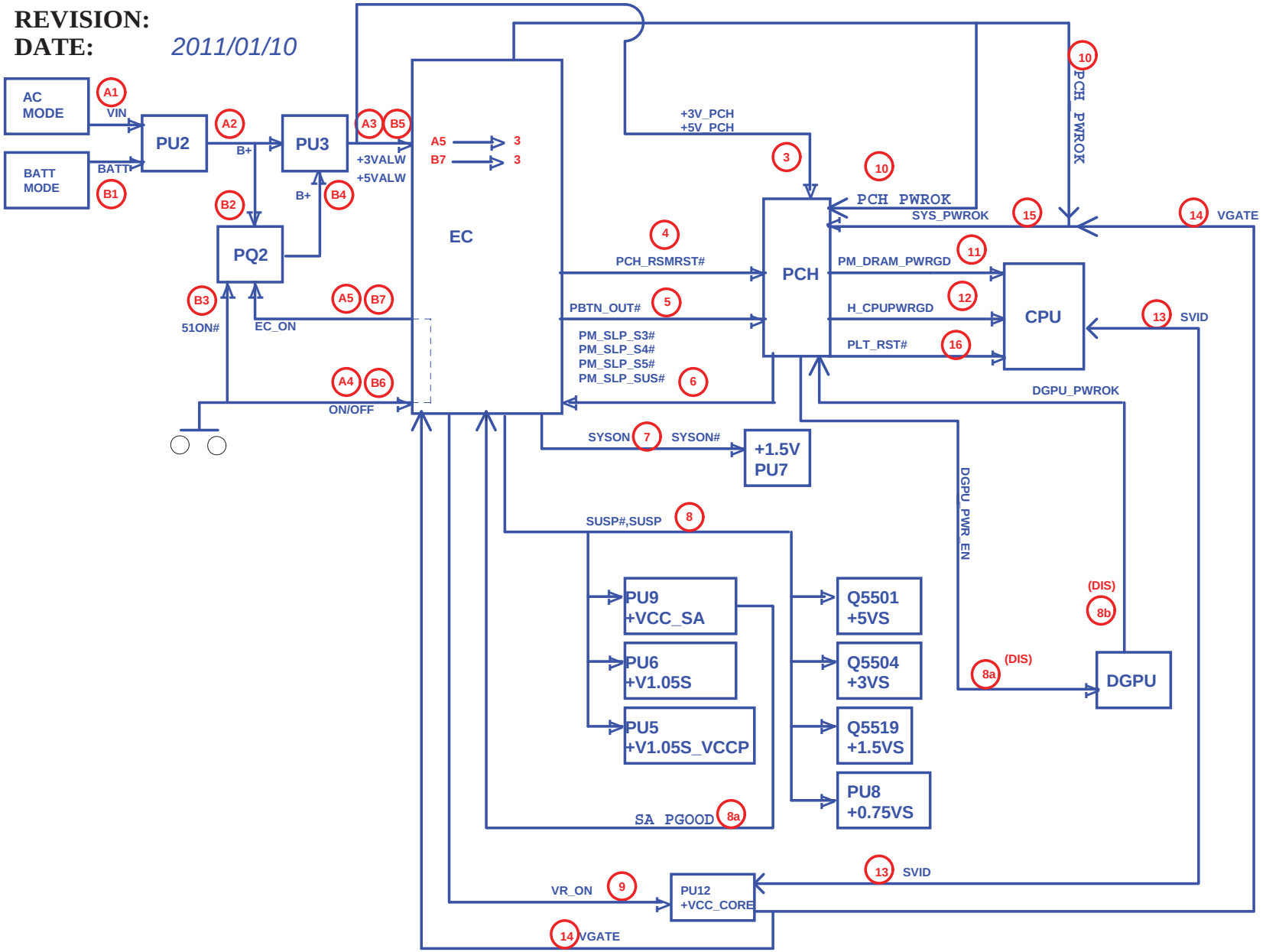
Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Compal Electronics, Inc.		
Title: PWR - PIR		
Size	Document Number: PBL21 LA6771P M/B	Rev: 0.1
Date: Thursday, April 07, 2011	Sheet 68 of 68	

COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-7391P*
REVISION:
DATE: *2011/01/10*



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/31

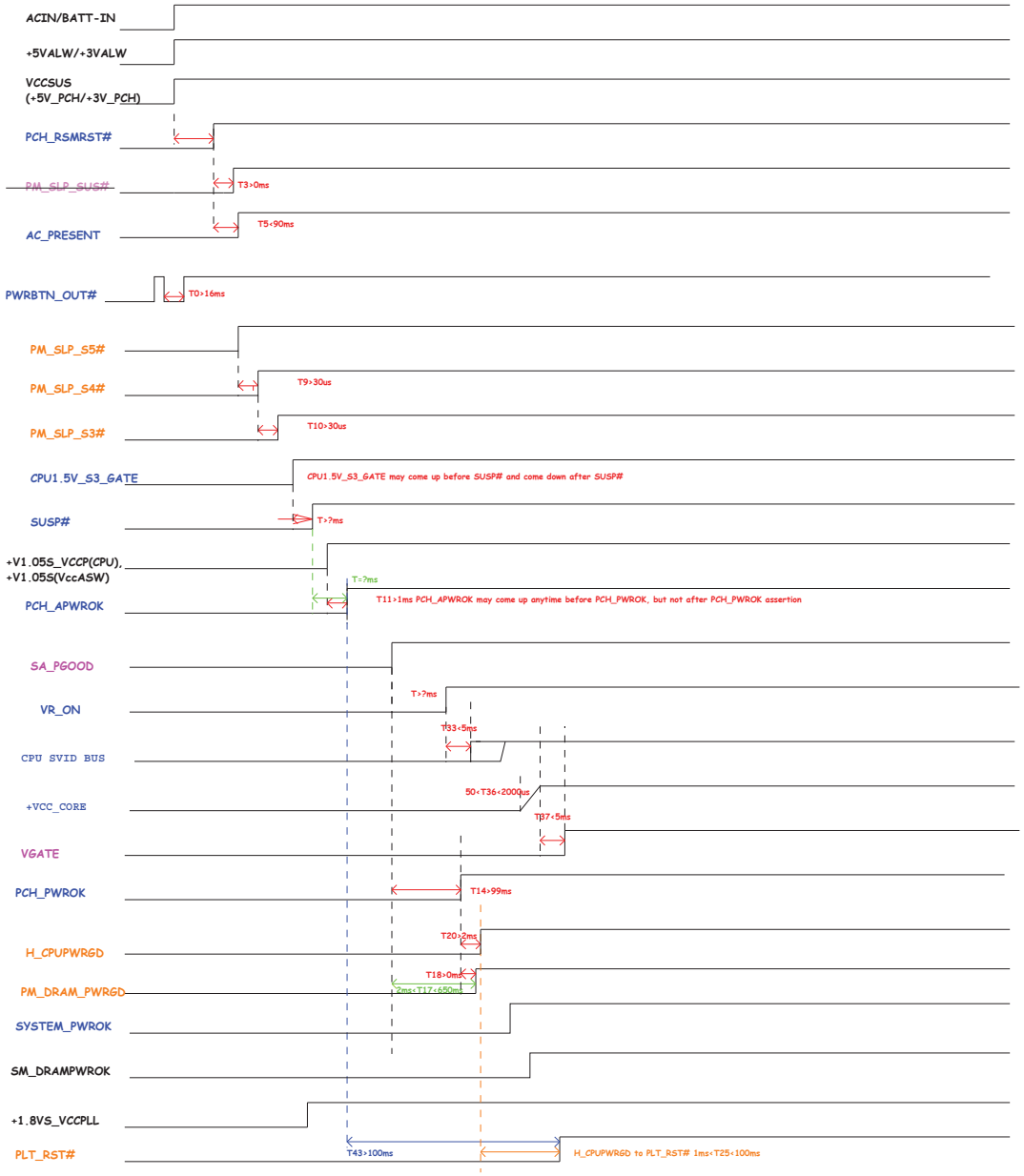
Compal Electronics, Inc.

Title: Power Sequence Block Diagram

Size	Document Number	Rev
Custom	LA-6211P	0.2

Date: Thursday, April 07, 2011 Sheet 69 of 64

Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Title: Power Sequence
Size: Document Number: LA-7391P Rev: 0.4
Date: Thursday, April 01, 2010 Sheet 31 of 36

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: EE-PIR-1

Size: Custom | Document Number: LA-7391P | Rev: 0.2

Date: Thursday, April 07, 2011 | Sheet 71 of 64