

COMPAL CONFIDENTIAL

MODEL NAME : Goliad MLK 12 UMA ENTRY  
PCB NO : LA-A972P  
BOM P/N : 4319RK31LXX  
GPIO MAP: 3.3b

Goliad MLK 12" UMA ENTRY  
Broadwell U Processor

2013-12-23  
REV : 0.2 (X01)

- @ : Nopop Component
- EMC@ : EMI, ESD and RF Component
- @EMC@ : EMI, ESD and RF Nopop Component
- CXDP@ : XDP Component
- CONN@ : Connector Component
- VPRO@ : Vpro Component
- NVPRO@ : Non-Vpro Component

Layout Dell logo



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REV: X01  
PWB: FGFC2  
DATE: 1352-01

| MB PCB      |                                        |
|-------------|----------------------------------------|
| Part Number | Description                            |
| DA800028000 | PCB 14A LA-A972P REV0 MB W/O DOCKING 2 |

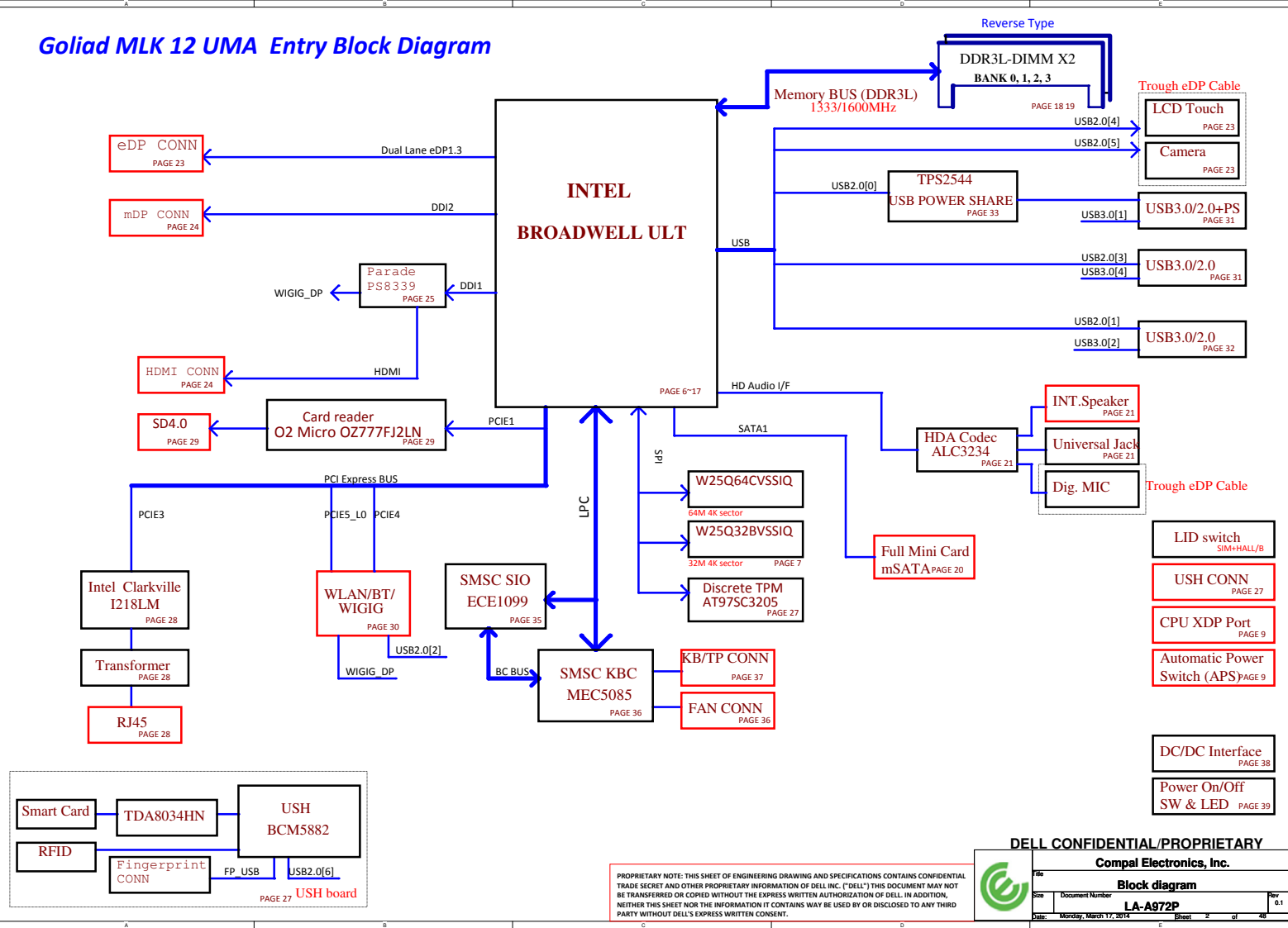
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|                          | LA-A972P               | 0.1           |
| Date                     | Monday, March 17, 2014 | Sheet 1 of 45 |

Goliad MLK 12 UMA Entry Block Diagram



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| Block diagram                 |                        |       |         |
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|                               | LA-A972P               | 6.1   |         |
| Date                          | Monday, March 17, 2014 | Sheet | 2 of 48 |

POWER STATES

| State \ Signal               | SLP S3# | SLP S4# | SLP S5# | SLP A# | ALWAYS PLANE | M PLANE | SUS PLANE | RUN PLANE | CLOCKS |
|------------------------------|---------|---------|---------|--------|--------------|---------|-----------|-----------|--------|
| S0 (Full ON) / M0            | HIGH    | HIGH    | HIGH    | HIGH   | ON           | ON      | ON        | ON        | ON     |
| S3 (Suspend to RAM) / M3     | LOW     | HIGH    | HIGH    | HIGH   | ON           | ON      | ON        | OFF       | OFF    |
| S4 (Suspend to DISK) / M3    | LOW     | LOW     | HIGH    | HIGH   | ON           | ON      | OFF       | OFF       | OFF    |
| S5 (SOFT OFF) / M3           | LOW     | LOW     | LOW     | HIGH   | ON           | ON      | OFF       | OFF       | OFF    |
| S3 (Suspend to RAM) / M-OFF  | LOW     | HIGH    | HIGH    | LOW    | ON           | OFF     | ON        | OFF       | OFF    |
| S4 (Suspend to DISK) / M-OFF | LOW     | LOW     | HIGH    | LOW    | ON           | OFF     | OFF       | OFF       | OFF    |
| S5 (SOFT OFF) / M-OFF        | LOW     | LOW     | LOW     | LOW    | ON           | OFF     | OFF       | OFF       | OFF    |

PM TABLE

| State \ power plane    | +5V_ALW<br>+3.3V_ALW<br>+3.3V_ALW_PCH<br>+3.3V_RTC_LDO | +3.3V_SUS<br>+1.35V_MEM | +5V_RUN<br>+3.3V_RUN<br>+0.675V_DDR_VTT<br>+1.05V_RUN<br>+VCC_CORE | +3.3V_M<br>+1.05V_M | +3.3V_M<br>+1.05V_M<br>(M-OFF) |
|------------------------|--------------------------------------------------------|-------------------------|--------------------------------------------------------------------|---------------------|--------------------------------|
| S0                     | ON                                                     | ON                      | ON                                                                 | ON                  | ON                             |
| S3                     | ON                                                     | ON                      | OFF                                                                | ON                  | OFF                            |
| S5 S4/AC               | ON                                                     | OFF                     | OFF                                                                | ON                  | OFF                            |
| S5 S4/AC doesn't exist | OFF                                                    | OFF                     | OFF                                                                | OFF                 | OFF                            |

| PCIE   | USB3.0   | SATA   | DESTINATION        |
|--------|----------|--------|--------------------|
|        | USB3.0 1 |        | JUSB1-->Rear left  |
|        | USB3.0 2 |        | JUSB3-->Right      |
| PCIE 1 | USB3.0 3 |        | MMI (CARD READER)  |
| PCIE 2 | USB3.0 4 |        | JUSB2-->Rear Right |
| PCIE 3 |          |        | LOM                |
| PCIE 4 |          |        | WLAN - JNGFF1      |
| PCIE 5 |          |        | WiGig - JNGFF1     |
| PCIE 6 |          | SATA 3 | NA                 |
|        |          | SATA 2 | NA                 |
|        |          | SATA 1 | JMINI3             |
|        |          | SATA 0 | NA                 |

| BDW ULT | USB PORT# | DESTINATION  |
|---------|-----------|--------------|
|         | 0         | JUSB1        |
|         | 1         | JUSB3        |
|         | 2         | WLAN + BT    |
|         | 3         | JUSB2        |
|         | 4         | Touch Screen |
|         | 5         | CAMERA       |
|         | 6         | USH          |
|         | 7         | WWAN         |

|     |   |     |
|-----|---|-----|
| USH | 0 | BIO |
|     | 1 | NA  |

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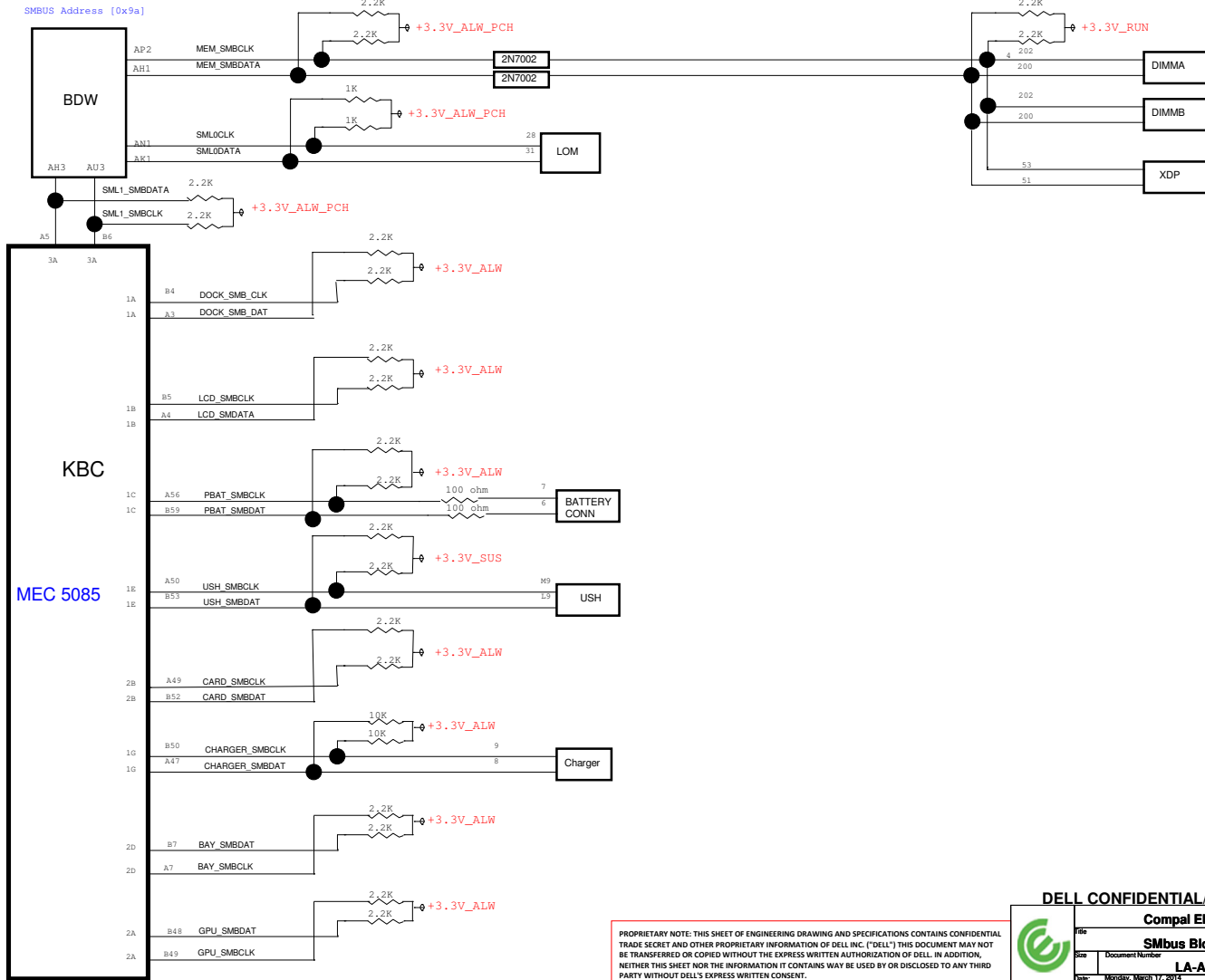


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|      |                        |          |         |
|------|------------------------|----------|---------|
| File | Port assignment        |          |         |
| Size | Document Number        | LA-A972P | Rev 0.1 |
| Date | Monday, March 17, 2014 |          |         |
|      | Sheet                  | 3        | of 40   |



SMBUS Address [0x9a]



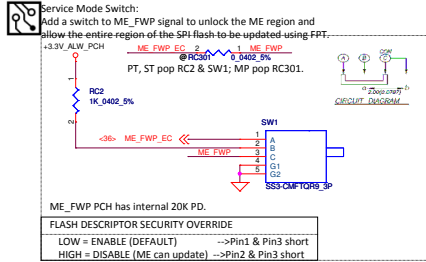
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| Date                                                                                  | Monday, March 17, 2014 | Sheet                           | 5 of 40 |

# UMA SATA port

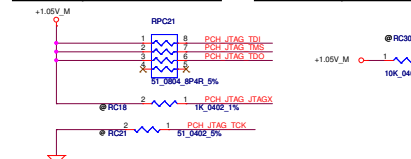
| SATA0  | SATA1 | PCB       | SATA2/PCIE6 L1                          | SATA3/PCIE6 L0                |                                                                  |
|--------|-------|-----------|-----------------------------------------|-------------------------------|------------------------------------------------------------------|
| E-Dock | mSATA | G12 UMA   | M2 3042<br>2nd PCIe Lane for PCIe Cache | M2 3042<br>(HCA & SATA-Cache) | contact to WWAN                                                  |
| NA     | mSATA | G12 Entry | NA                                      | NA                            |                                                                  |
| E-Dock | mSATA | G14 DSC   | M2 3042<br>SATA-Cache(no HCA)           | M2 3030 WIGIG                 | SATA2/PCIE6_L1 contact to WWAN<br>SATA3/PCIE6 L0 contact to WLAN |
| E-Dock | HDD   | G14 UMA   | M2 3042<br>2nd PCIe Lane for PCIe Cache | M2 3042<br>(HCA & SATA-Cache) | contact to WWAN                                                  |
| NA     | mSATA | G14D_En   | NA                                      | M2 3030 WIGIG                 | contact to WLAN                                                  |
| NA     | HDD   | G14U_En   | NA                                      | NA                            |                                                                  |



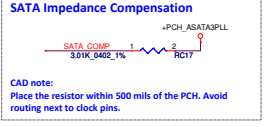
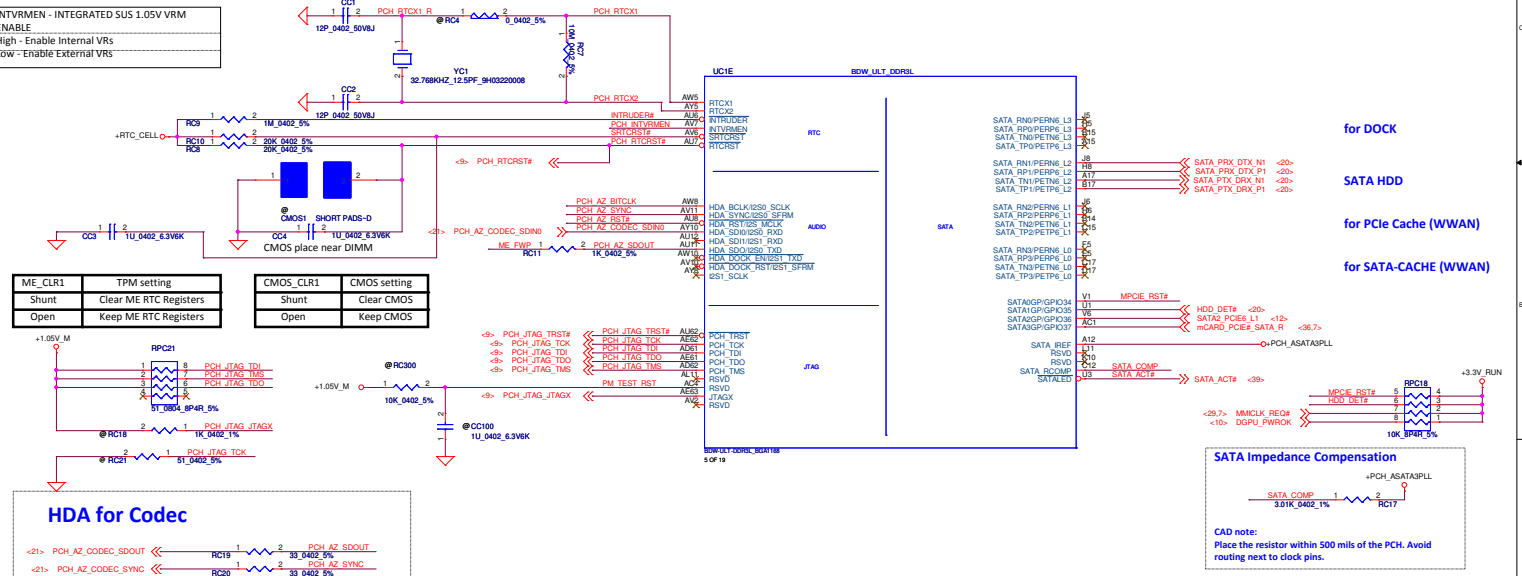
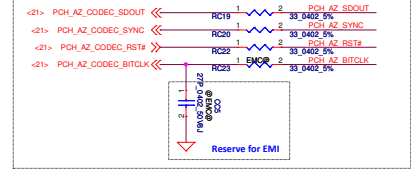
INTVRMEN - INTEGRATED SUS 1.05V VRM  
ENABLE  
High - Enable Internal VRs  
Low - Enable External VRs

ME\_CLR1  
Shunt  
Open  
Keep ME RTC Registers

CMOS\_CLR1  
Shunt  
Open  
Clear CMOS



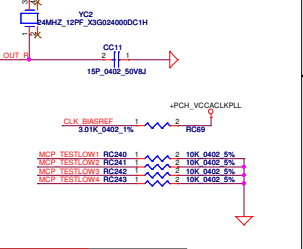
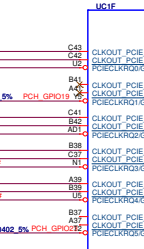
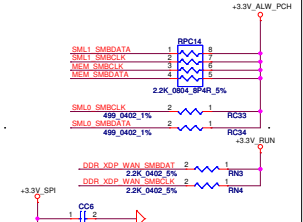
## HDA for Codec



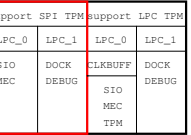
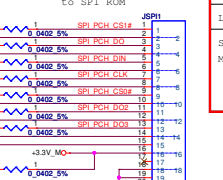
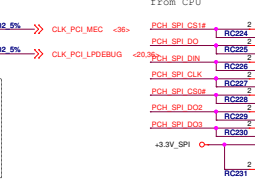
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| CPU (1/12)               |                        |
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| Date                     | Monday, March 17, 2014 |
| Sheet                    | 5 of 45                |

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The diagram shows two signal traces, PCI CLK LPC 0 and PCI CLK LPC 1, both connected to EMC0 and EMC67. Each trace has a period of 22.040 ns. Below these, two signals are shown: CLK\_PCL\_MEG and CLK\_PCL\_LDPEB, both with a period of 129.040250VUJ. These signals are connected to EMC0/CC12 and EMC0/CC13 respectively. A note at the bottom indicates 'Reserve for EMI'.



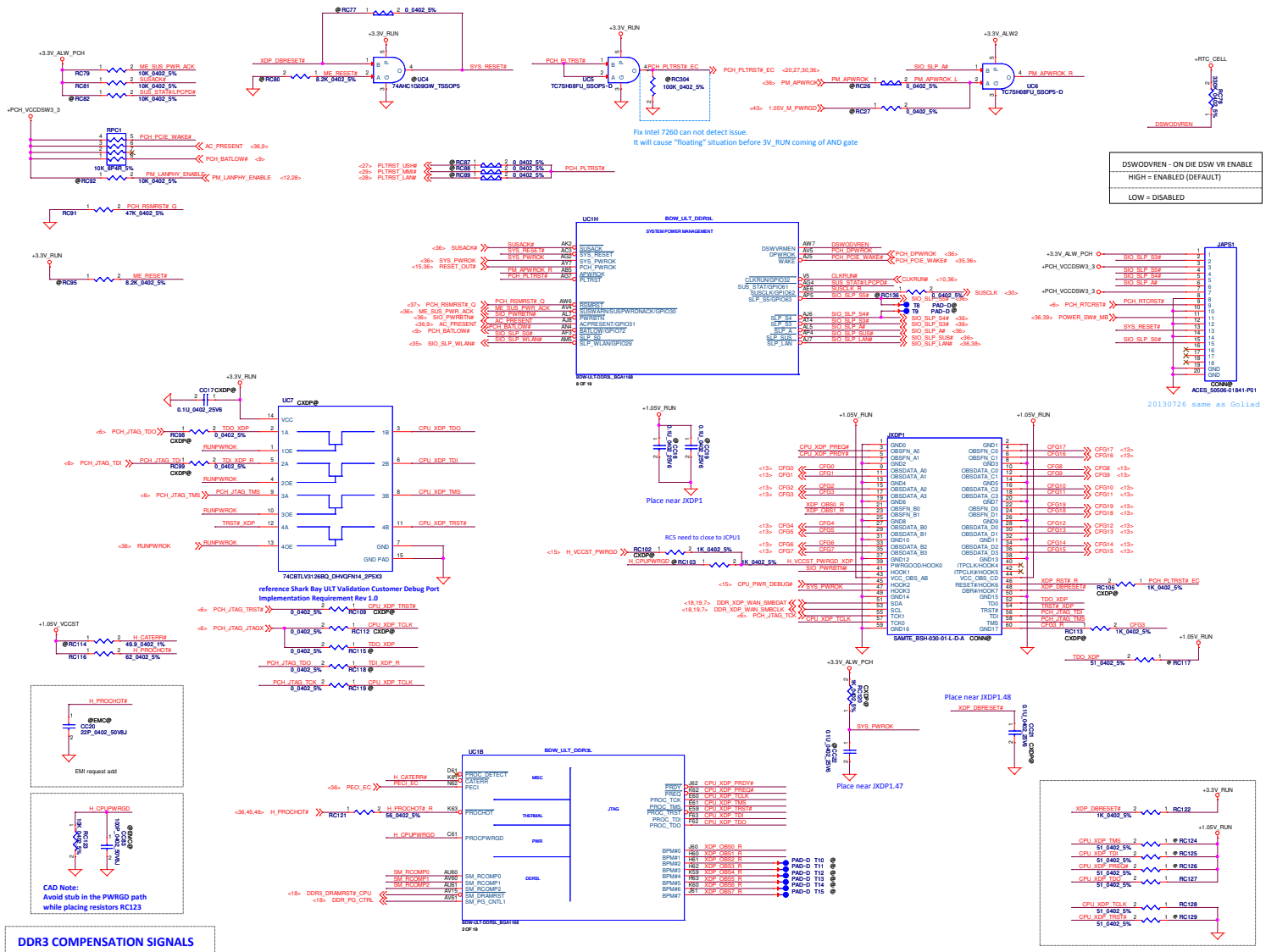
Please place RC224~RC331 with JSPI1 at the same MB side

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| <b>LA-A972P</b> |                        |                   |         |
| Date:           | Monday, March 17, 2014 | Sheet             | 7 of 48 |

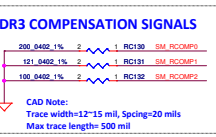
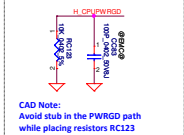
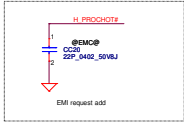




DSW00VREN - ON the DSW VR ENABLE  
HIGH = ENABLED (DEFAULT)  
LOW = DISABLED

Pin 1760 cannot not detect issue.  
It will cause "floating" situation before 3V\_RUN coming of AND gate

20130726 same as Goldid



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CPU (4/12)

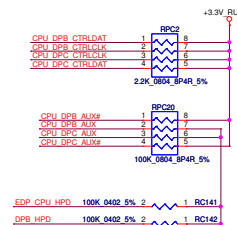
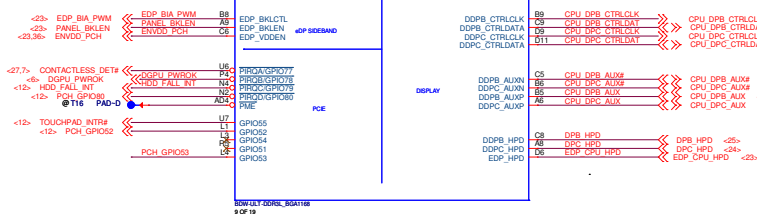
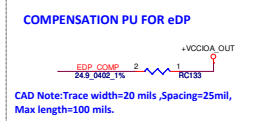
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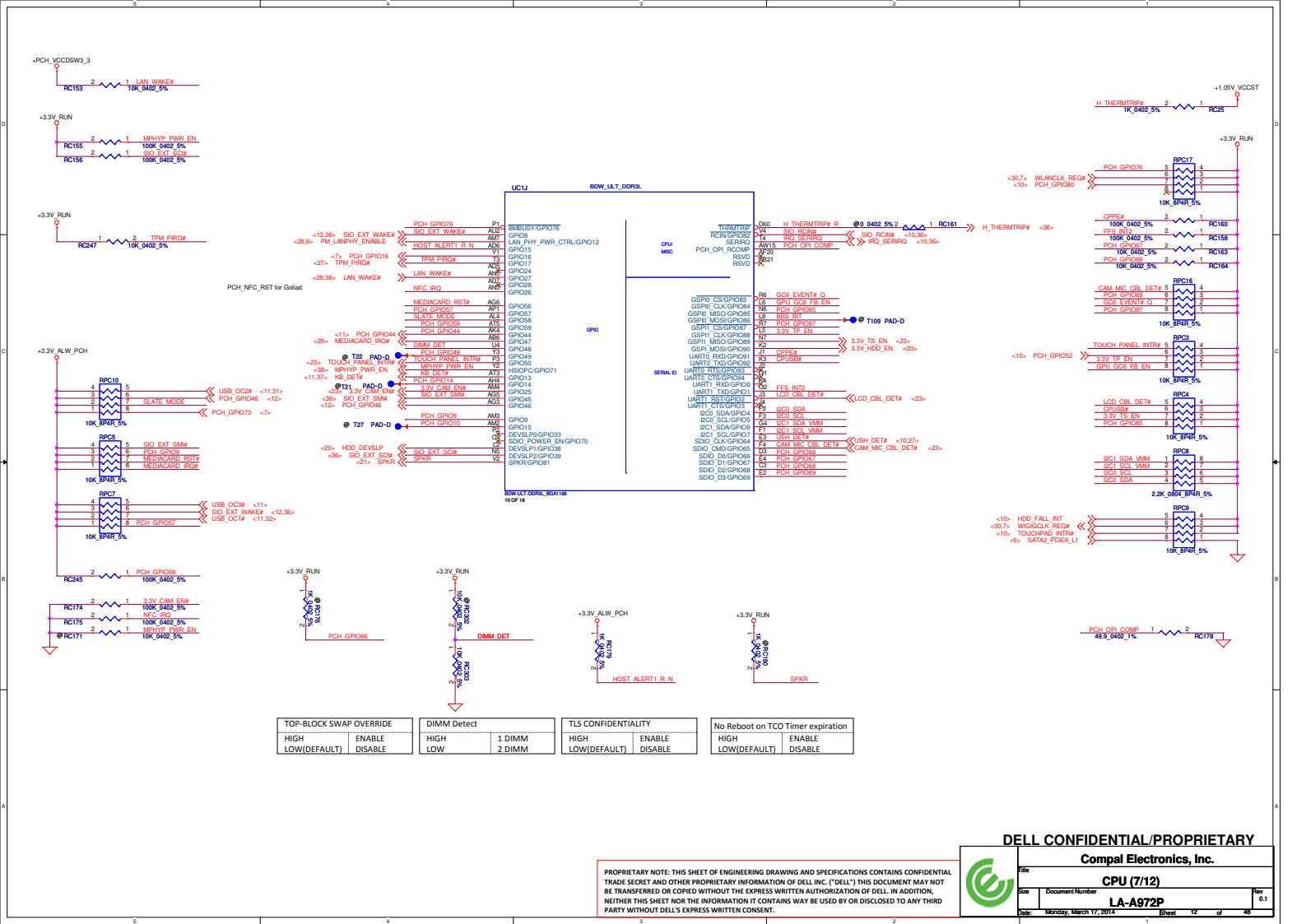
Page 9 of 46



|                                                                                       |                        |                                 |                |
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| Date                                                                                  | Monday, March 17, 2014 |                                 | Sheet 10 of 48 |

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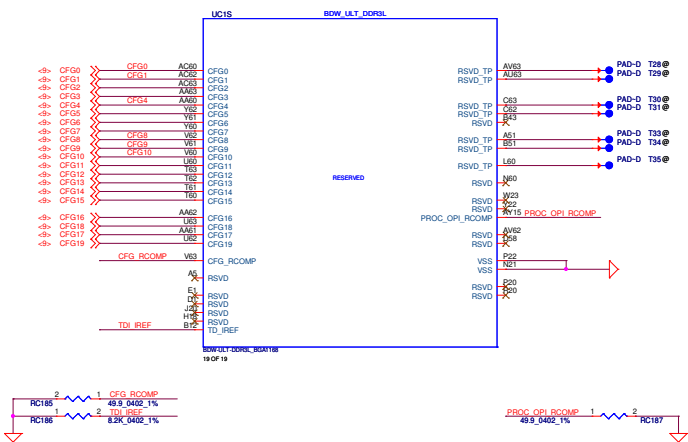


| TOP-BLOCK SWAP OVERRIDE |         | DIMM Detect |        | TLS CONFIDENTIALITY |         | No Reboot on TCO Timer expiration |         |
|-------------------------|---------|-------------|--------|---------------------|---------|-----------------------------------|---------|
| HIGH                    | ENABLE  | HIGH        | 1 DIMM | HIGH                | ENABLE  | HIGH                              | ENABLE  |
| LOW(DEFAULT)            | DISABLE | LOW         | 2 DIMM | LOW(DEFAULT)        | DISABLE | LOW(DEFAULT)                      | DISABLE |

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**LA-A972P**  
Date: Monday, March 17, 2014 Sheet 12 of 48

CFG STRAPS for CPU



| EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE |                                                           |
|-----------------------------------------------------------|-----------------------------------------------------------|
| CFG0                                                      | 1:(Default) Normal Operation; No stall<br>0:Lane Reversed |

| PCH/PCH LESS MODE SELECTION |                                                 |
|-----------------------------|-------------------------------------------------|
| CFG1                        | 1:(Default) Normal Operation<br>0:Lane Reversed |

| SAFE MODE BOOT |                                                                                                          |
|----------------|----------------------------------------------------------------------------------------------------------|
| CFG10          | 1: POWER FEATURES ACTIVATED DURING RESET<br>0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED |

| NO SVID PROTOCOL CAPABLE VR CONNECTED |                                                                                                                                        |
|---------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| CFG9                                  | 1: VRS support SVID protocol are present<br>0:No VR support SVID is present<br>The chip will not generate(OR Respond to) SVID activity |

| ALLOW THE USE OF NOA ON LOCKED UNITS |                                                                                                                                                           |
|--------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFG8                                 | 1: Enable(Default): Noa will be disable in locked units and enable in un-locked<br>0:Disable Noa will be available pegrardless of the locking of the unit |

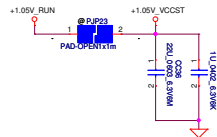
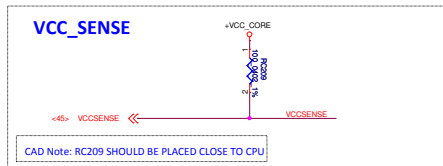
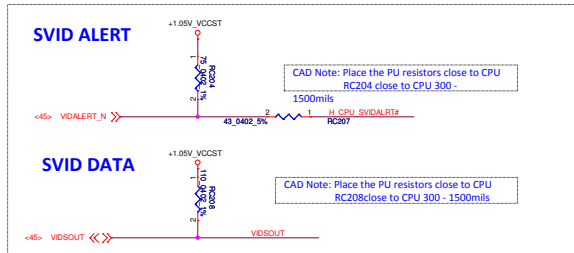
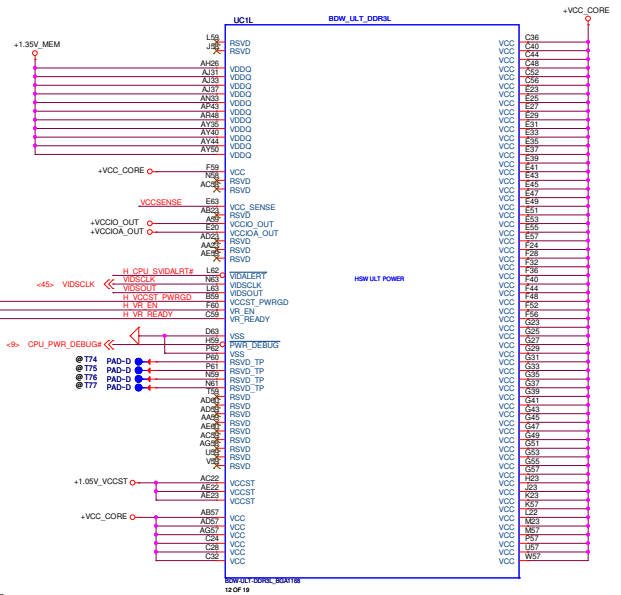
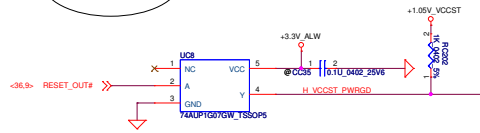
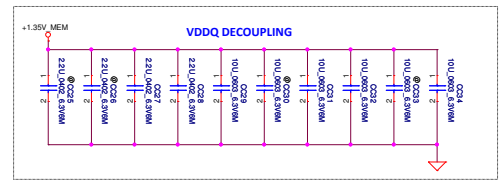
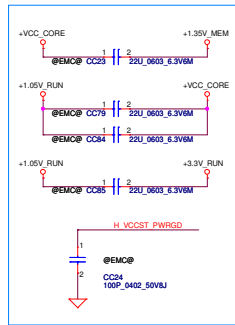
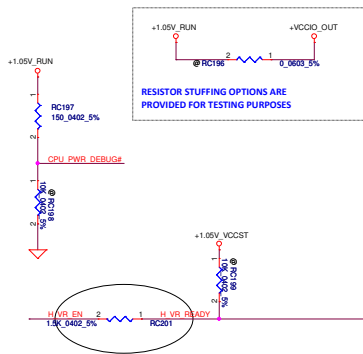
| Display Port Presence Strap |                                                                                                                                                                    |
|-----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFG4                        | 1 : Disabled; No Physical Display Port attached to Embedded Display Port<br>0 : Enabled; An external Display Port device is connected to the Embedded Display Port |

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| Date                     | Monday, March 17, 2014 |
| Sheet                    | 13 of 46               |

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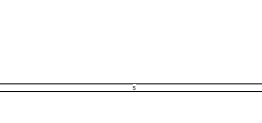
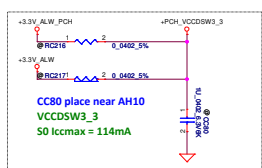
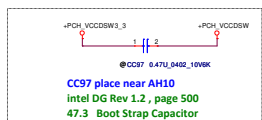
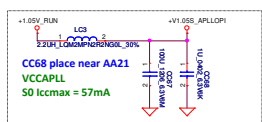
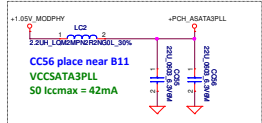
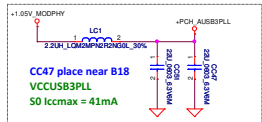
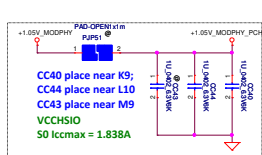
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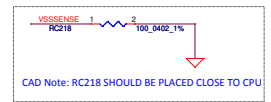
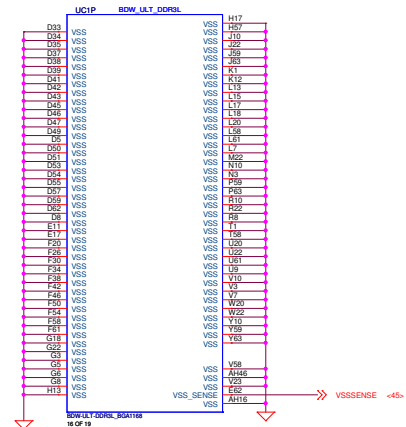
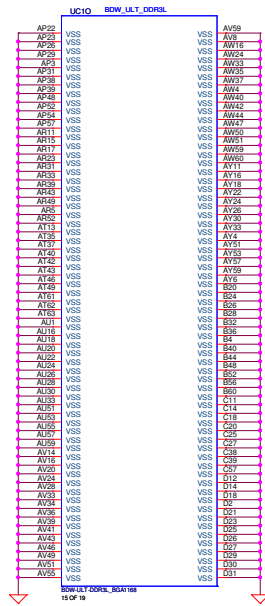
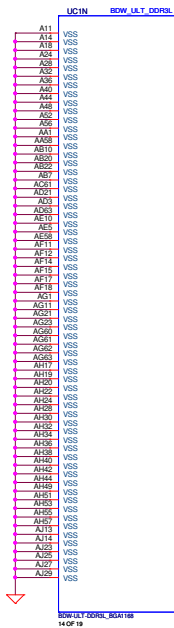
CPU (10/12)

LA-A972P

Date: Monday, March 17, 2014 Sheet 15 of 45

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| CPU (12/12)              |                        |
| File                     | Document Number        |
| LA-A972P                 |                        |
| Date                     | Monday, March 17, 2014 |
| Sheet                    | 17 of 48               |

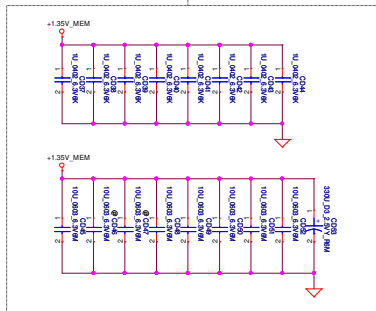
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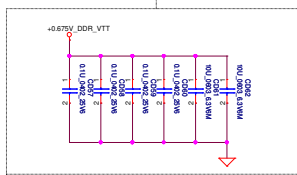
# H=4mm Reverse Type

DDR\_B\_D0[4:7] <<>  
DDR\_B\_D0[4:7] <<>  
DDR\_B\_D0[4:7] <<>  
DDR\_B\_Map[1:1] <<>

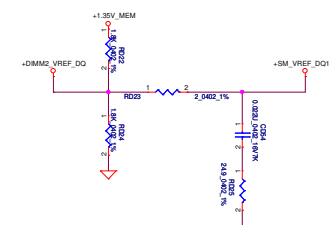
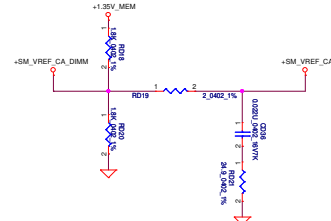
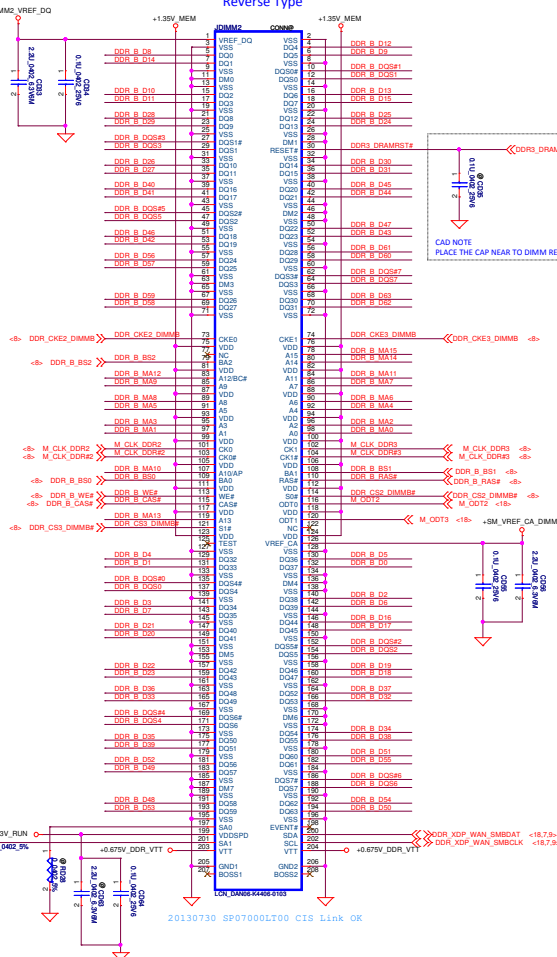
Layout Note:  
Place near JDIMM2



Layout Note:  
Place near JDIMM2.203,204



Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket



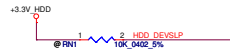
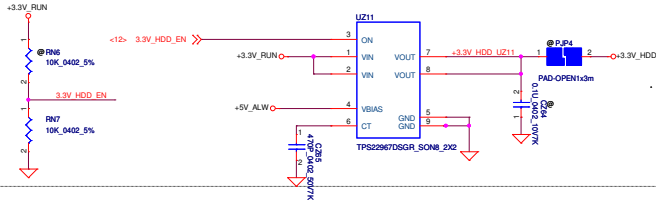
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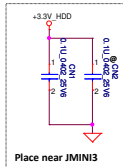
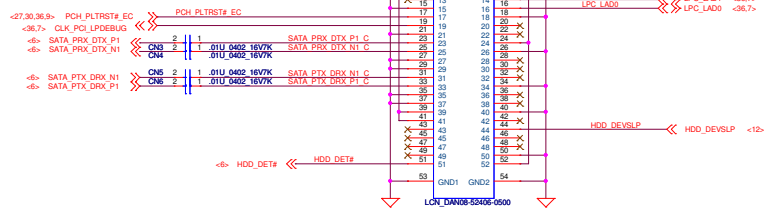
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|------------|----------|-----|---|
| DDR3L      | LA-A972P | 1   | 1 |
| Doc Number | LA-A972P | 1   | 1 |
| Rev        | 1        | 1   | 1 |

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## +3.3V\_HDD source



## Mini mSATA H=4



Place near JMINI3

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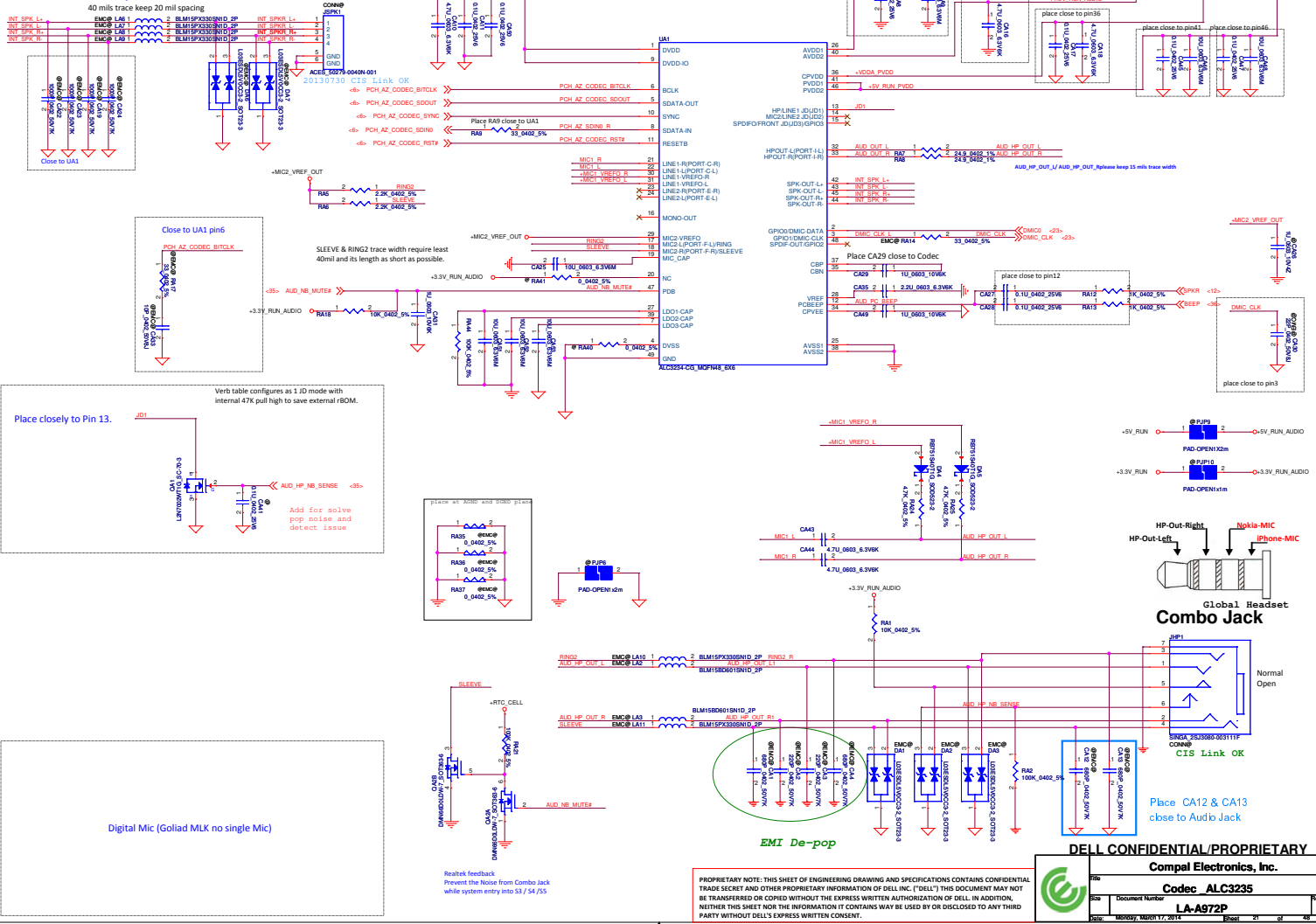
| HDD CONN |                        |
|----------|------------------------|
| Size     | Document Number        |
| LA-A972P | Rev 0.1                |
| Date     | Monday, March 17, 2014 |
| Sheet    | 20 of 25               |

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40 mils trace keep 20 mil spacing

40 mils trace keep 20 mil spacing



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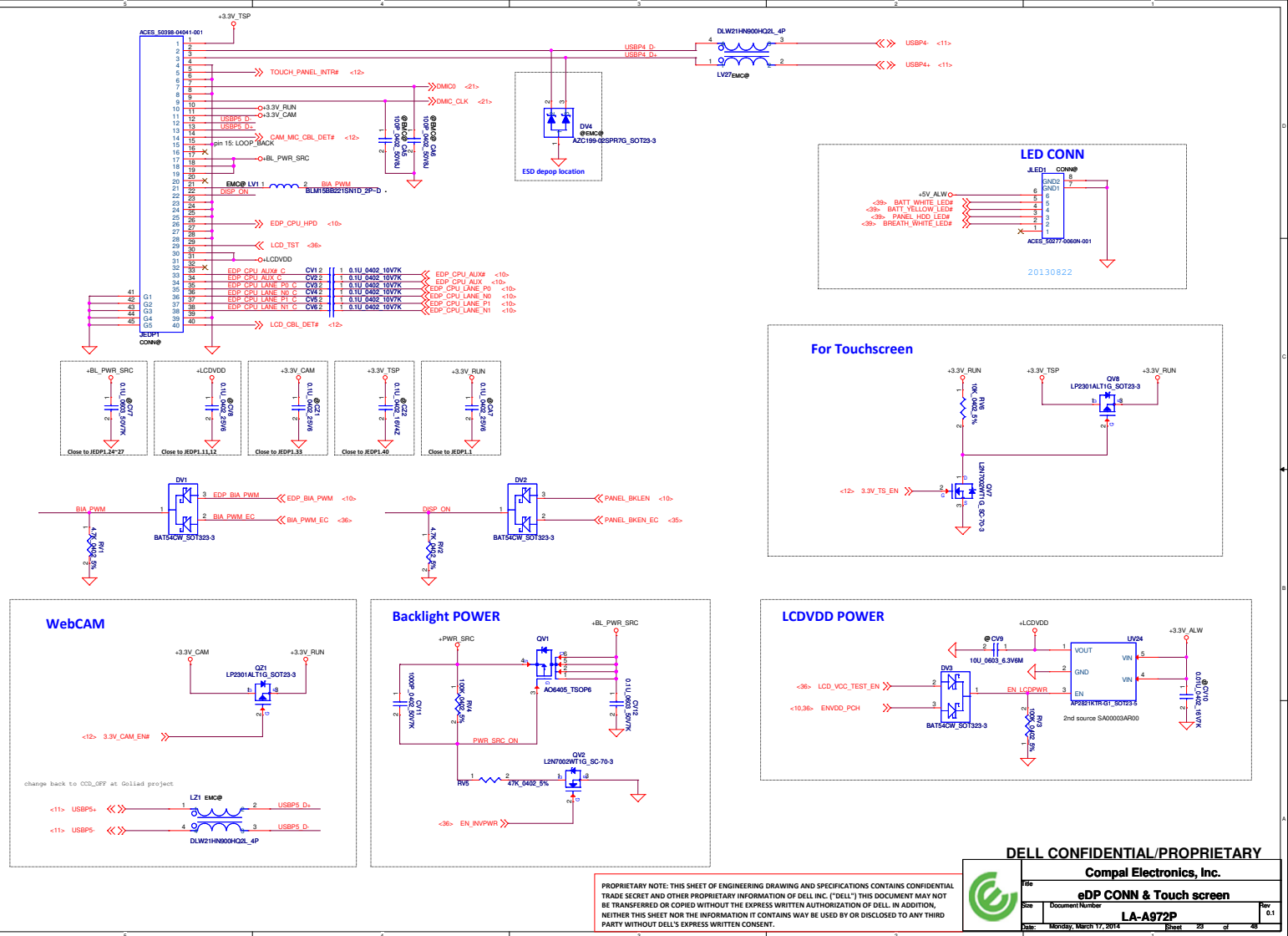
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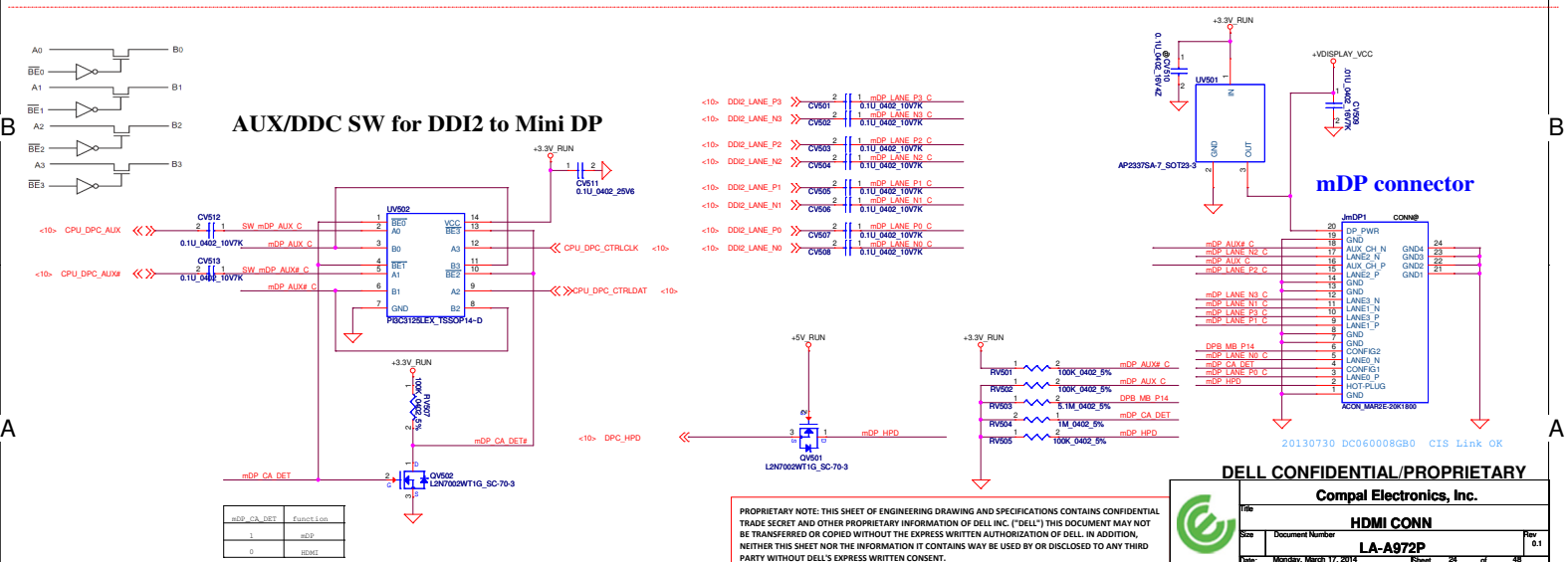
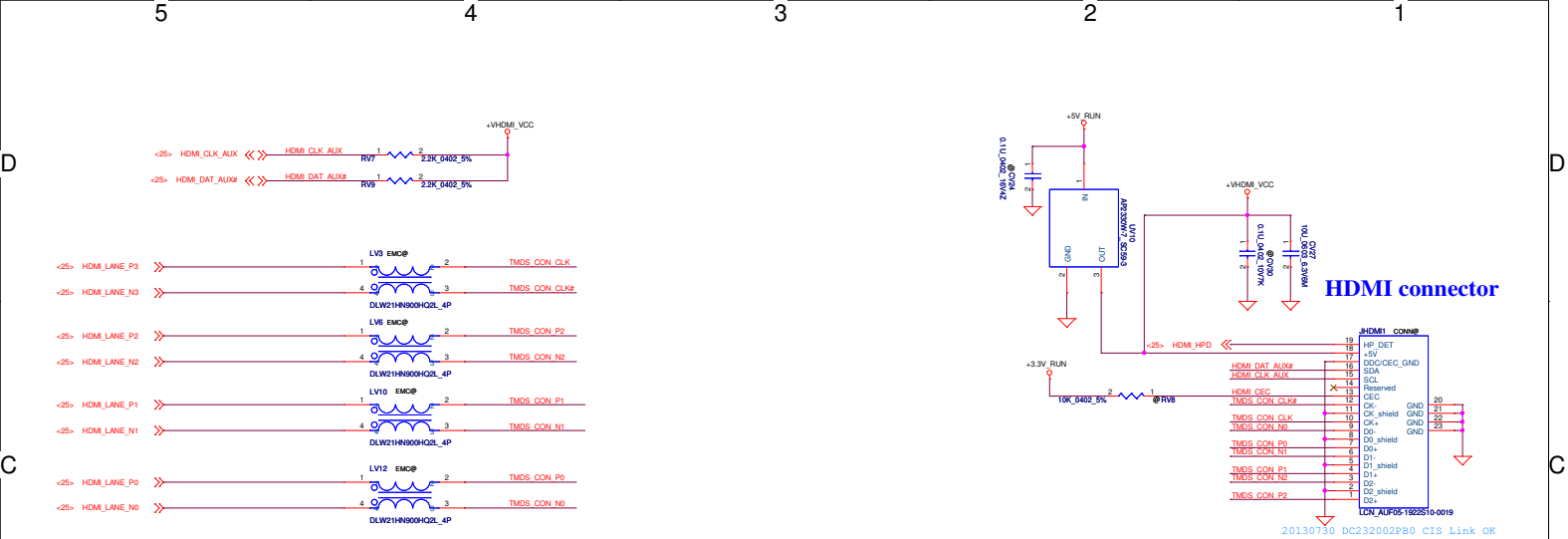
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| DP 1.2 MST HUB                |                        |       |          |
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|                               | LA-A972P               | 0.1   |          |
| Date                          | Monday, March 17, 2014 | Sheet | 22 of 48 |







|   |   |   |   |   |
|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 |
| D |   |   |   | D |
| C |   |   |   | C |
| B |   |   |   | B |
| A |   |   |   | A |

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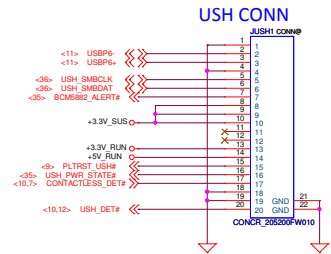
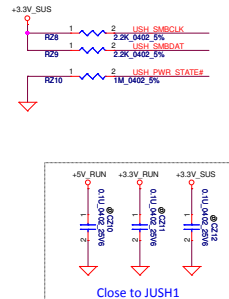
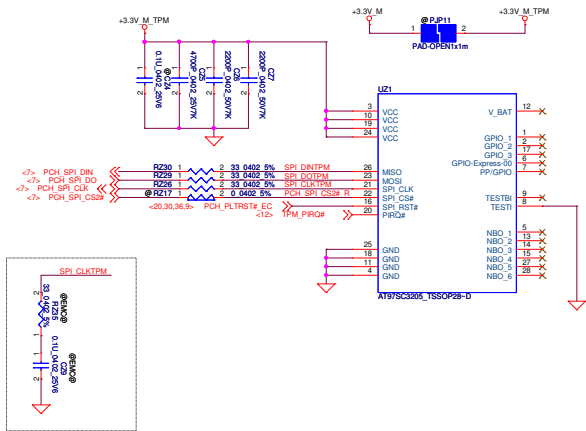
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**DP to VGA & VGA Conn**

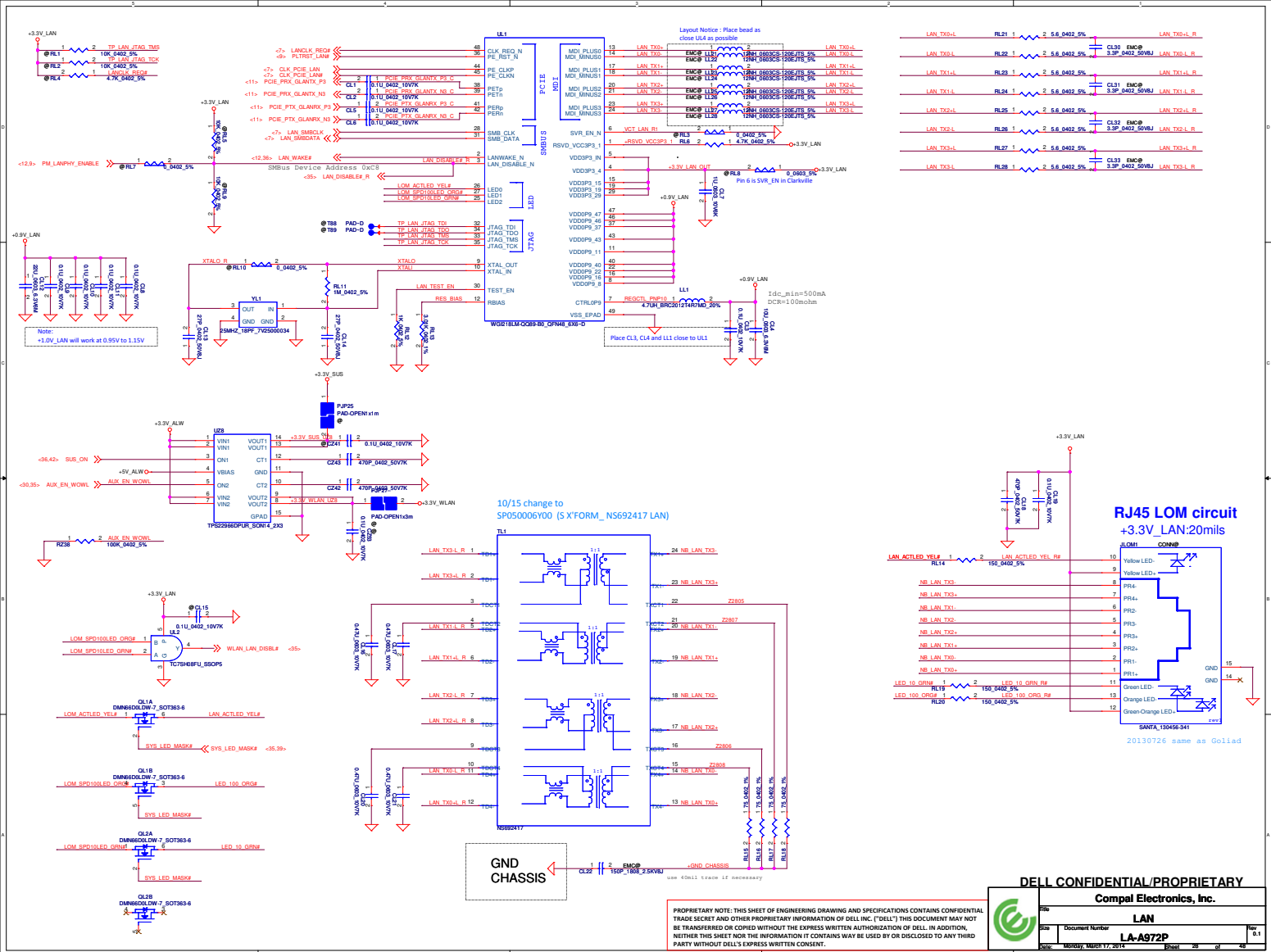
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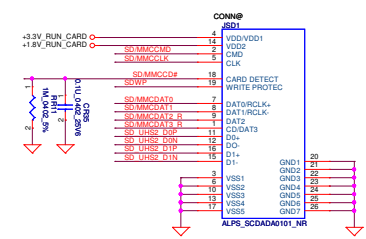
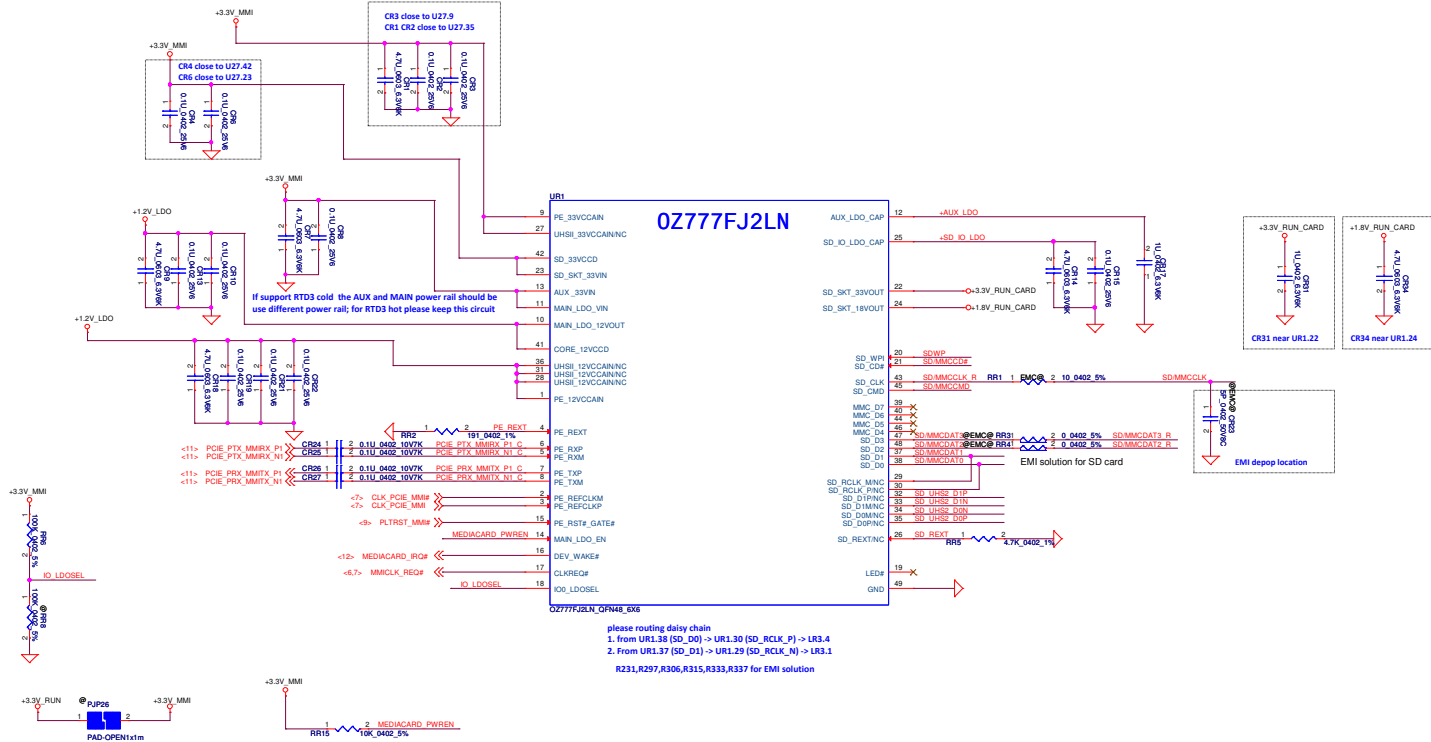
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| USH & TPM                     |  |  |  |
| LA-A972P                      |  |  |  |
| Date: Monday, March 17, 2014  |  |  |  |
| Sheet 27 of 48                |  |  |  |

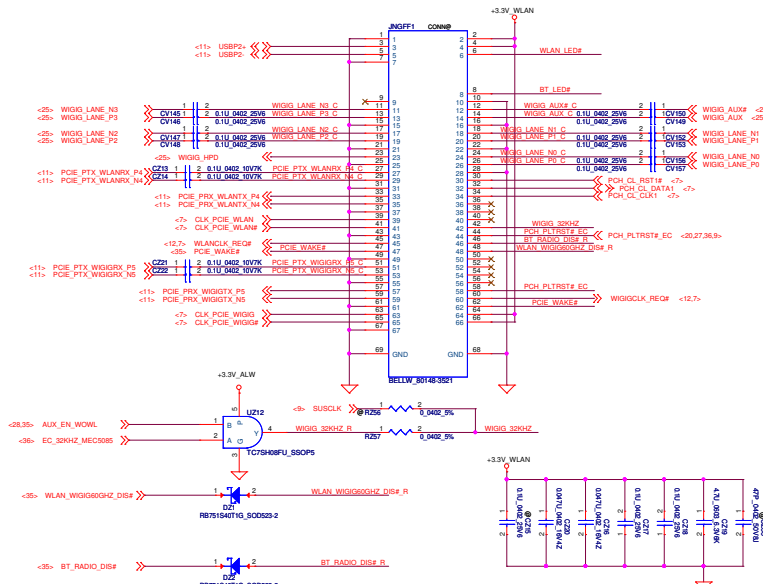




20130726 SP070011100 CIS Link OK

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| Card Reader                   |                 |
| File                          | Document Number |
| LA-A972P                      | Rev 0.1         |
| Date                          | Sheet           |
| Monday, March 17, 2014        | 29 of 48        |

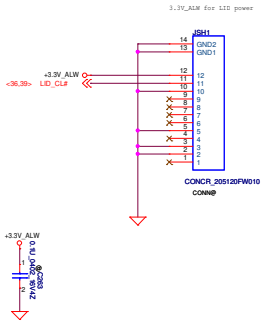
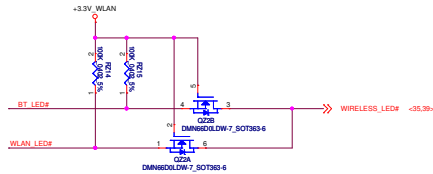
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| STATE # | CONFIG_0 | CONFIG_1 | CONFIG_2 | CONFIG_3 | Module Type |
|---------|----------|----------|----------|----------|-------------|
| 0       | GND      | GND      | GND      | GND      | SSD-SATA    |
| 1       | GND      | HIGH     | GND      | GND      | SSD-PCIe    |
| 8       | HIGH     | GND      | GND      | GND      | WWAN        |
| 14      | HIGH     | GND      | HIGH     | HIGH     | HCA-PCIe    |
| 15      | HIGH     | HIGH     | HIGH     | HIGH     | NA          |

| Power Rating TBD |                   |               |           |        |
|------------------|-------------------|---------------|-----------|--------|
| PWR Rail         | Voltage Tolerance | Primary Power | Aux Power |        |
| +3.3V            |                   | Peak          | Normal    | Normal |

LED control circuit



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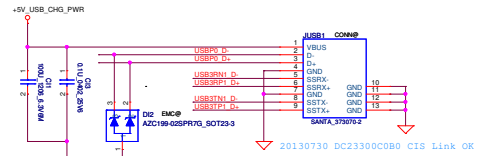
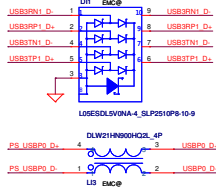
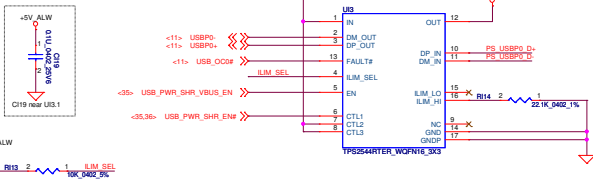
Compal Electronics, Inc.

NGFF Card

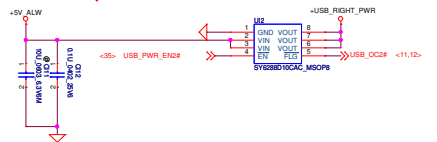
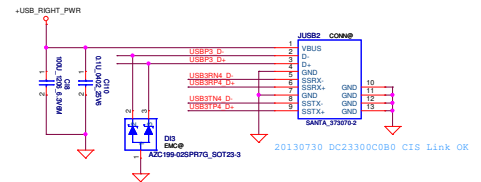
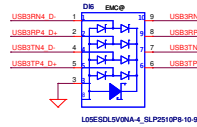
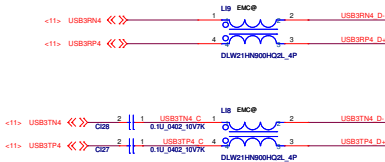
LA-A972P

Monday, March 17, 2014

30 of 40



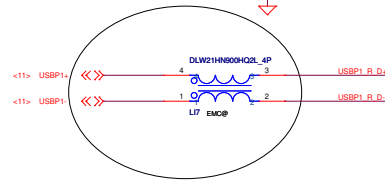
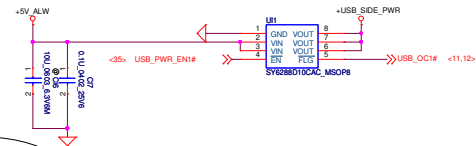
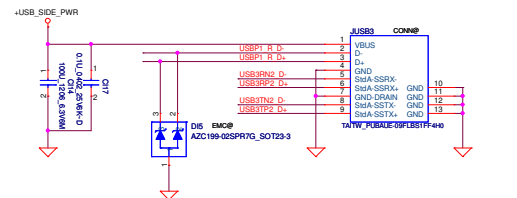
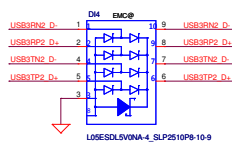
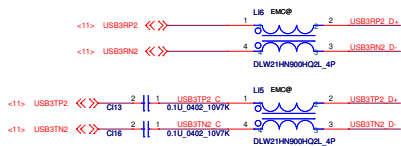
| PCB       | USB2 0  | USB2 3   |
|-----------|---------|----------|
| G12 UMA   | USB3102 | NX3DV221 |
| G12 Entry | NA      | NA       |
| G14 DSC   | USB3102 | NX3DV221 |
| G14 UMA   | USB3102 | NX3DV221 |
| G14D_En   | NA      | NA       |
| G14U_En   | NA      | NA       |



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| Rev | Doc Number | Rev |
|-----|------------|-----|
| 1   | LA-A972P   | 1   |
| Rev | Doc Number | Rev |
| 1   | LA-A972P   | 1   |



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USB SW

LA-A972P

Date: Monday, March 17, 2014 Sheet 32 of 45 Rev 0.1

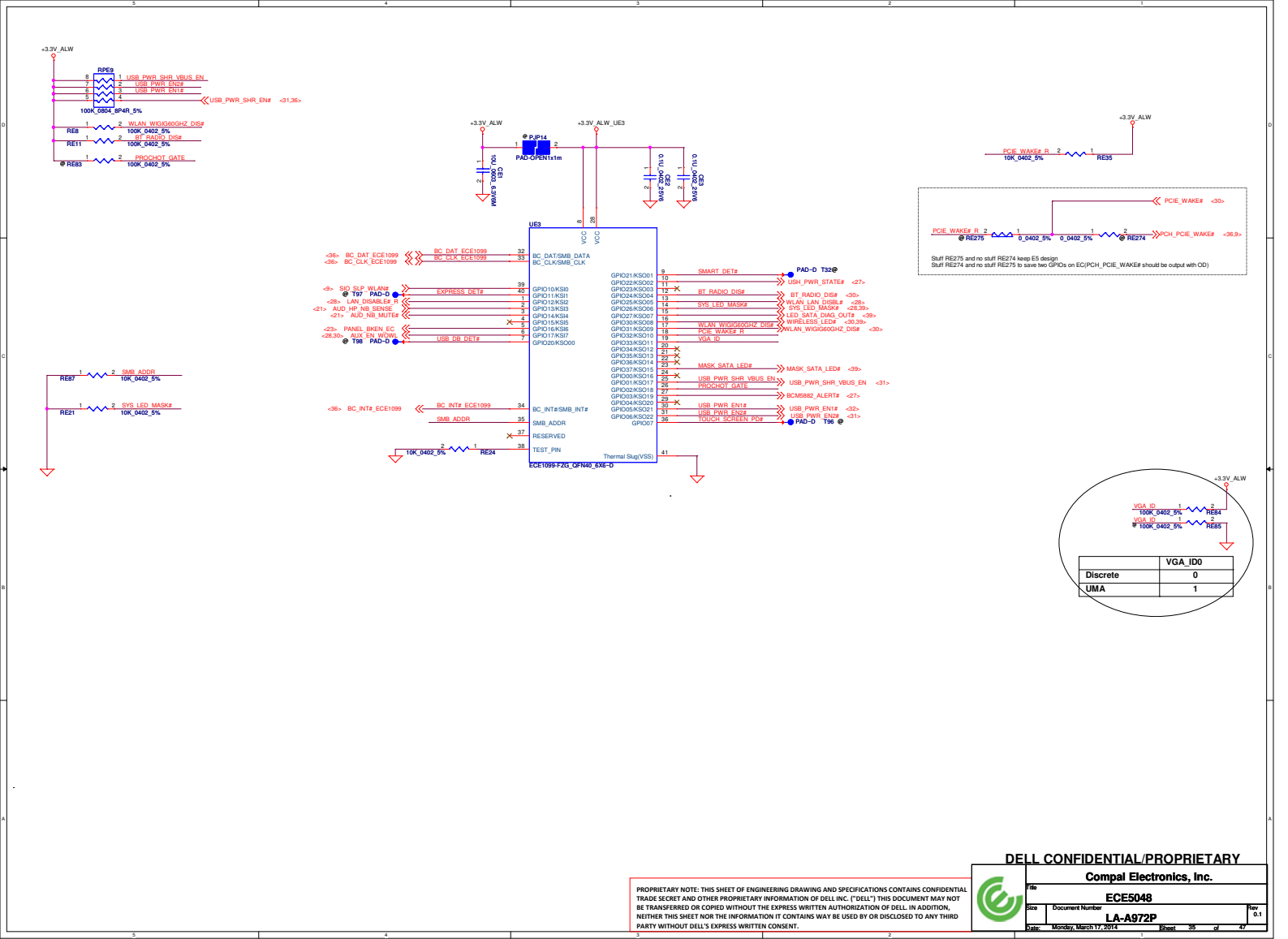
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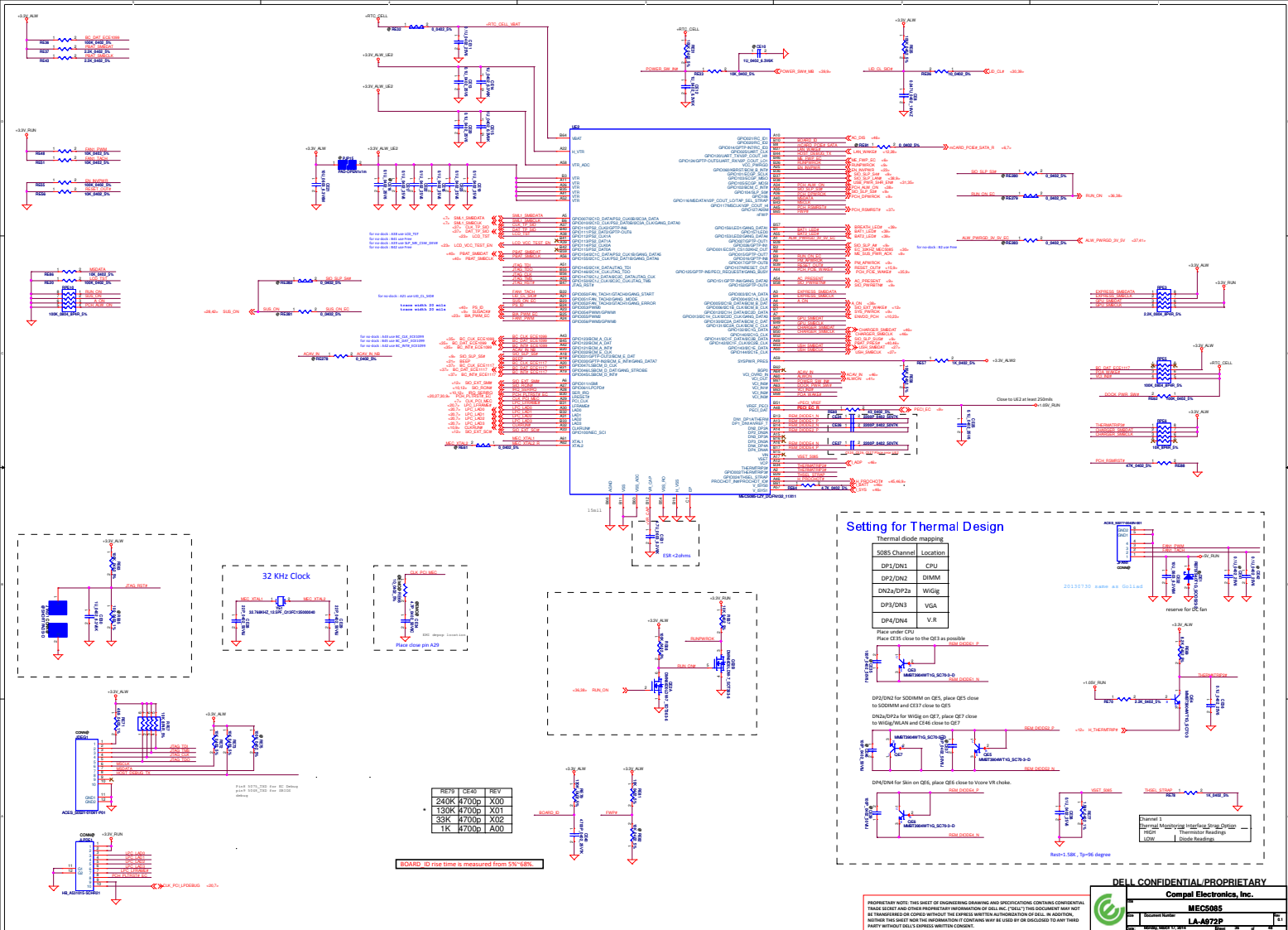
# NFC on USH/B

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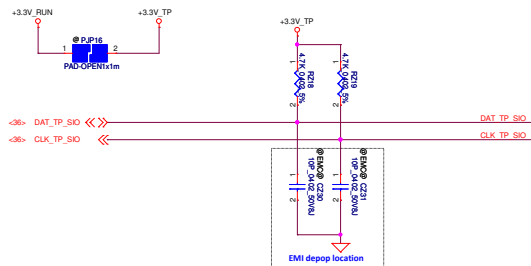
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| NFC                           |                        |  |                |
| Size                          | Document Number        |  | Rev            |
|                               | LA-A972P               |  | 0.1            |
| Date                          | Monday, March 17, 2014 |  | Sheet 33 of 45 |

|                                                                                       |                        |                 |                |
|---------------------------------------------------------------------------------------|------------------------|-----------------|----------------|
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| <b>Compal Electronics, Inc.</b>                                                       |                        |                 |                |
|  | Title                  |                 |                |
|                                                                                       | <b>E-Dock</b>          |                 |                |
|                                                                                       | Size                   | Document Number | Rev            |
|                                                                                       |                        | <b>LA-A972P</b> | <b>0.1</b>     |
| Date:                                                                                 | Monday, March 17, 2014 |                 | Sheet 34 of 48 |

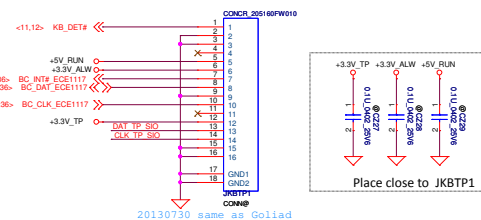




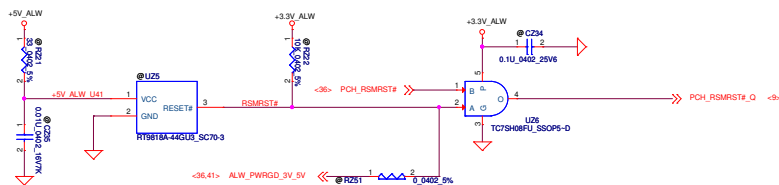
## Touch Pad



## Keyboard



## RSMRST circuit



### @HCP Cable

| Part Number | Description                      |
|-------------|----------------------------------|
| DC50100790  | 9-COMM SET 14A MB-ESP-LED-CAMERA |

### @HCP TS Cable

| Part Number | Description                         |
|-------------|-------------------------------------|
| DC50100790  | 9-COMM SET 14A MB-ESP-LED-CAMERA-TS |

### @DC-IN Cable

| Part Number | Description                            |
|-------------|----------------------------------------|
| DC30100M700 | COMM SET 0VW DC3ACB-MB 20W1003-038110P |

### @RTC BATT

| Part Number | Description                            |
|-------------|----------------------------------------|
| DC30100M700 | COMM SET 0VW DC3ACB-MB 20W1003-038110P |

### @FAN

| Part Number | Description                          |
|-------------|--------------------------------------|
| DC28A000800 | FAN SET DAQ20 DC5V AB74058B-MB3 A20A |

### @USH Board FFC

| Part Number | Description                        |
|-------------|------------------------------------|
| NRX0001K000 | FFC 12P G P0.5 PAD=0.3 47MM MB-USB |

### @VBTP FFC

| Part Number | Description                        |
|-------------|------------------------------------|
| NRX0001K000 | FFC 12P G P0.5 PAD=0.3 52MM MB-USB |

### @NFC Board FFC

| Part Number | Description                          |
|-------------|--------------------------------------|
| NRX0001K000 | FFC 12P G P0.5 PAD=0.3 40.5MM MB-USB |

### @BFP FFC

| Part Number | Description                         |
|-------------|-------------------------------------|
| NRX0001K000 | FFC 12P G P0.5 PAD=0.3 22.5MM MB-FP |

### @SIM+HMB FFC

| Part Number | Description                              |
|-------------|------------------------------------------|
| NRX0001K000 | FFC 12P G P0.5 PAD=0.3 73.5MM MB-SIM+HMB |

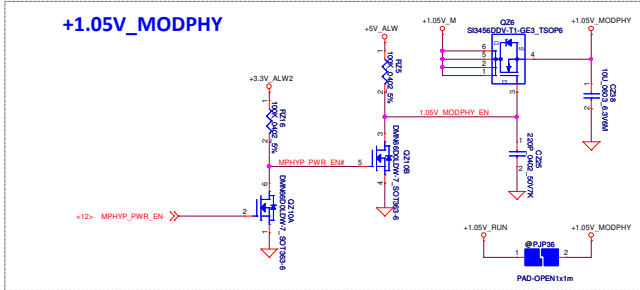
### @Speaker

| Part Number | Description                 |
|-------------|-----------------------------|
| PR210003001 | SPK PACK 2.5W 2.0W 4 OHM PD |

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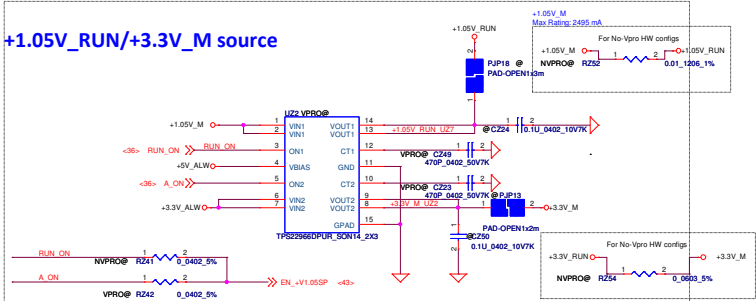
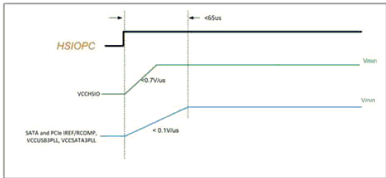
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|--------------------------|------------------------|
| Keyboard                 |                        |
| Size                     | Document Number        |
| LA-A972P                 | Rev 0.1                |
| Date                     | Monday, March 17, 2014 |
| Sheet                    | 37 of 46               |

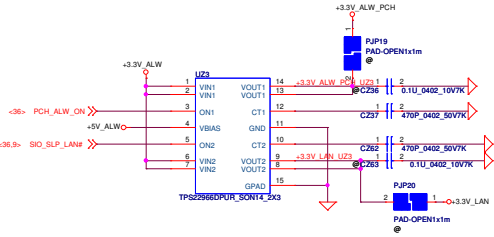


if support MODPHY off keep DSC solution  
MODPHY timing spec 0.7V/us and <65us

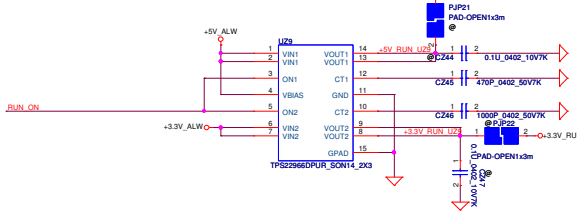
Figure 5-6. Sequencing Requirements between HSIOPC and LPT-LP 1.05V rails and COMP/IREF signals



### +3.3V\_ALW\_PCH/+3.3V\_LAN source



### +3.3V\_RUN/+5V\_RUN source



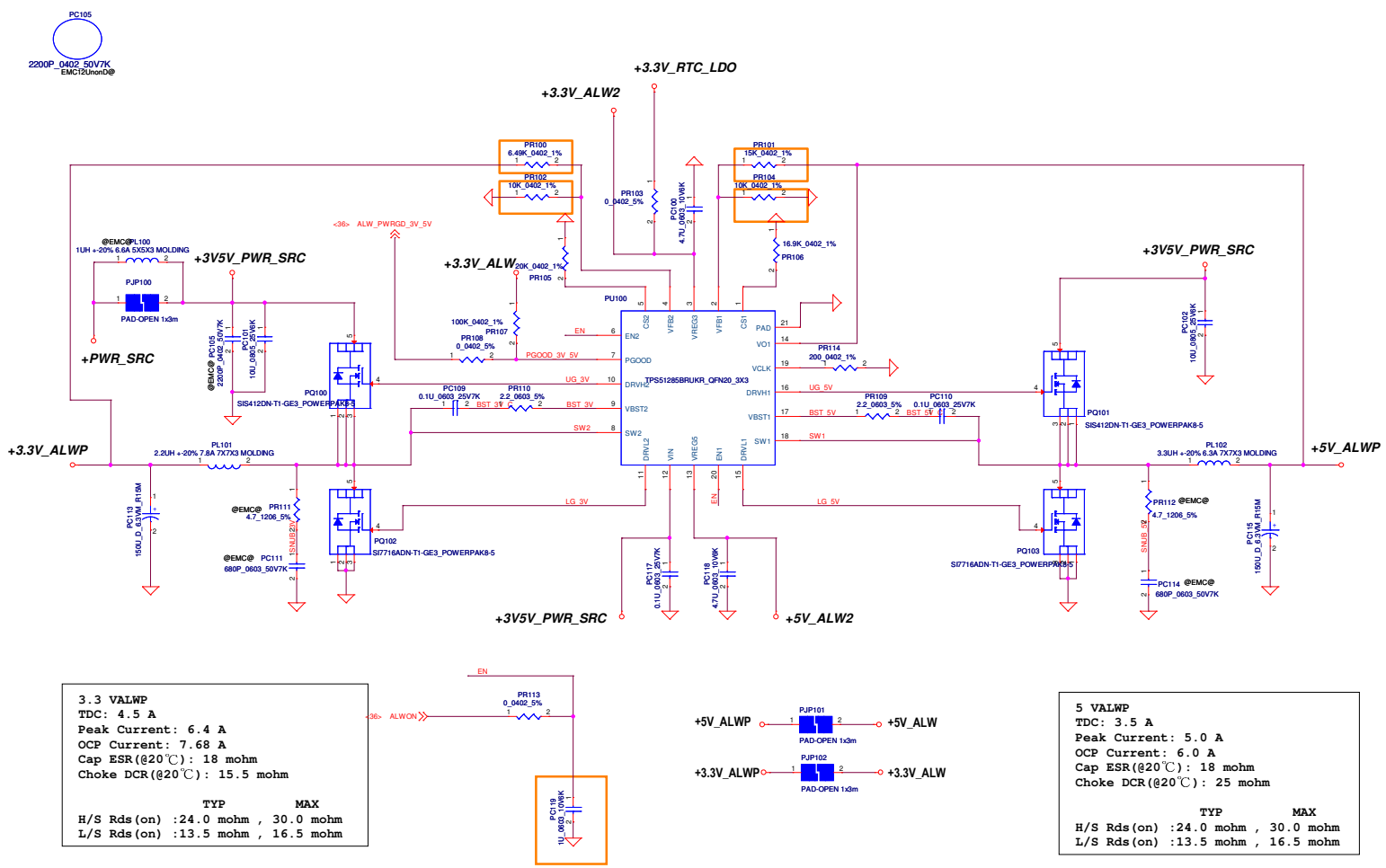
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| Power control |                        |       |          |
|---------------|------------------------|-------|----------|
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| Date          | Monday, March 17, 2014 | Sheet | 38 of 48 |







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|                                                                                       |                                 |                 |     |       |
|---------------------------------------------------------------------------------------|---------------------------------|-----------------|-----|-------|
|  | <b>Compal Electronics, Inc.</b> |                 |     |       |
|                                                                                       | <b>+5V_ALW/3.3V_ALW</b>         |                 |     |       |
|                                                                                       | Size                            | Document Number |     | Rev   |
|                                                                                       | <b>LA-A902P</b>                 |                 | 0.1 |       |
| Date: <b>Monday, March 17, 2014</b>                                                   |                                 | Sheet           | 41  | of 47 |



PC300



2200P\_0402\_50V7K  
EMC12UonD@

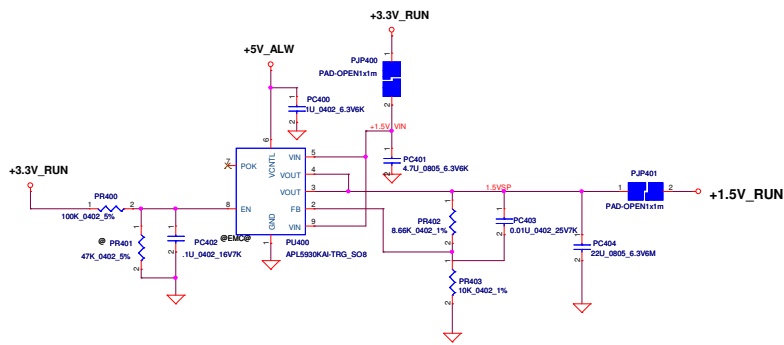


+1.05V M

9.1

Sheet 43 of 47

+1.5V\_RUN  
TDC: 0.47 A  
Peak Current: 0.67 A

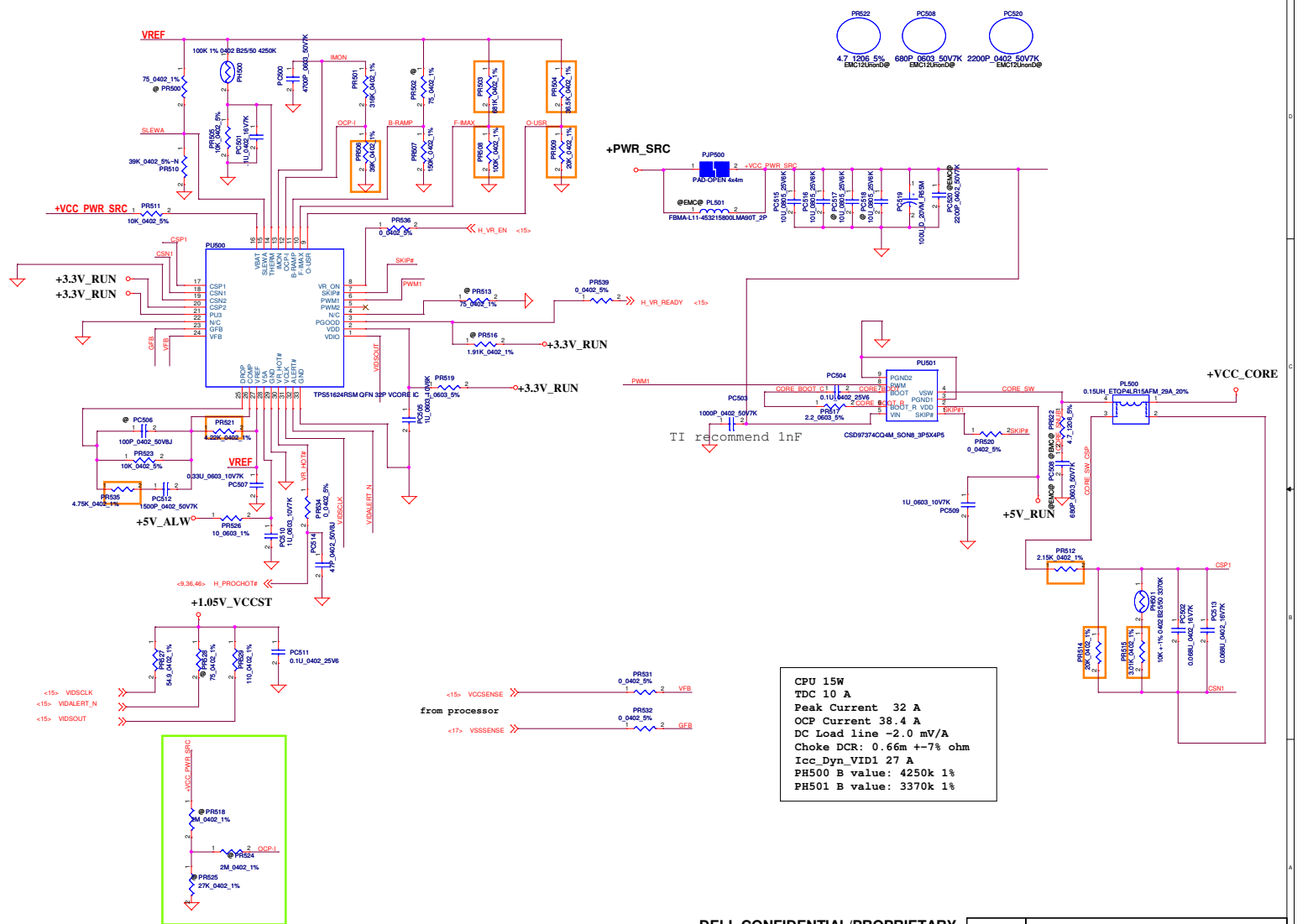


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| Size                     | Document Number        | Rev            |
|                          | LA-A902P               | 0.1            |
| Date                     | Monday, March 17, 2014 | Sheet 44 of 47 |



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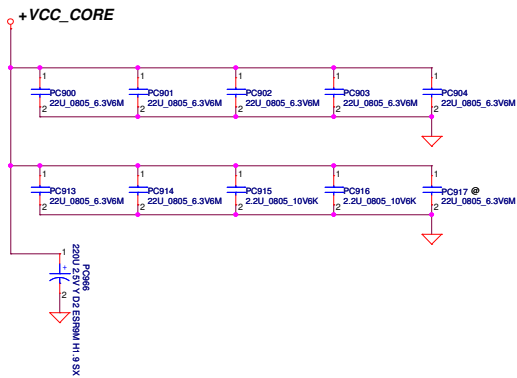
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+VCC CORE

LA-A902P

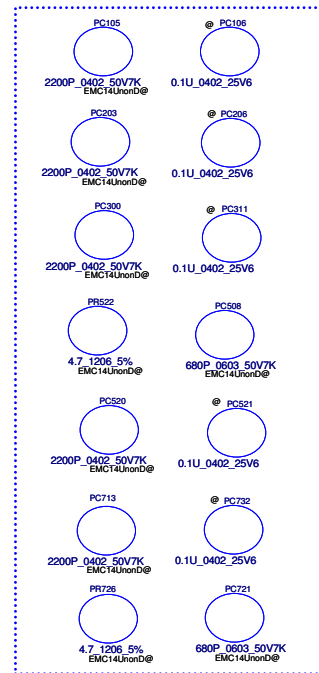
Doc: Monday, March 17, 2014 Sheet 46 of 47 Rev 0.1

|                                                                                       |                                    |                                 |              |                |
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|  | <b>Compal Electronics, Inc.</b>    |                                 |              |                |
|                                                                                       | File _____                         |                                 |              |                |
|                                                                                       | <b>Charger</b>                     |                                 |              |                |
|                                                                                       | Size _____                         | Document Number <b>LA-A902P</b> |              | Rev <b>0.1</b> |
|                                                                                       | Date <b>Monday, March 17, 2014</b> | Sheet <b>48</b>                 | of <b>47</b> |                |



Based on \_RF Cheng. Hill  
鄭智仁(11257) for PT 20131107

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| Size                                                                                  | Document Number        | Rev   |          |
|                                                                                       | LA-A902P               | 0.1   |          |
| Date                                                                                  | Monday, March 17, 2014 | Sheet | 47 of 47 |

Version Change List (P. I. R. List)

| Item | Page#      | Title                            | Date  | Request<br>Owner | Issue Description                       | Solution Description                                                                                                                      | Rev. |
|------|------------|----------------------------------|-------|------------------|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|------|
| 1    | 47         | VCC_CORE                         | 10/8  | Compal           | To prevent acoustic noise issue         | Remove PC923, PC924, PC925, PC926, PC927, PC928, PC929, PC930, PC931, PC940, PC941, PC943, PC946, PC947, PC948<br>Add PC966               | X01  |
| 2    | 42         | 1.35V_MEN                        | 10/8  | RICHTEK          | To prevent IC damage                    | Add PR204                                                                                                                                 | X01  |
| 3    | 46         | Charger                          | 10/8  | Compal           | Fine tune divider voltage               | Change PR715, PR729 to 154k                                                                                                               | X01  |
| 4    | 41, 43, 44 | +1.05V_M<br>+1.5V_RUN<br>+3V/+5V | 10/22 | Compal           | To improve the ability of anti-noise    | Change PR307 to 7.5k<br>Change PR310, PR102, PR104, PR403 to 10k<br>Change PR100 to 6.49k<br>Change PR101 to 15k<br>Change PR402 to 8.66k | X01  |
| 5    | 45         | VCC_CORE                         | 10/31 | Compal           | Fine tune IMON                          | Add PR518, PR524, PR525                                                                                                                   | X01  |
| 6    | ALL        | ALL                              | 10/31 | Compal           | RF request                              | Pop PR522, PC508, PR726, PC721, PC713, PL501, PC520                                                                                       | X01  |
| 7    | 46         | Charger                          | 12/05 | Compal           | Has the same behavior with dock circuit | Add PQ711                                                                                                                                 | X01  |
| 8    | 46         | Charger                          | 12/05 | Compal           | To add 2nd source                       | Remove PQ702 Add PQ709, PQ710                                                                                                             | X01  |
| 9    | 46         | Charger                          | 12/05 | Compal           | To reduce leakage current               | Remove PD701 Add PD704, PD705                                                                                                             | X01  |
| 10   | 46         | Charger                          | 3/03  | Compal           | To set OVP level                        | Remove PR729                                                                                                                              | X02  |
| 11   | 46         | Charger                          | 3/03  | Compal           | To set IC function                      | Remove PC720 Add PR788, PR799                                                                                                             | X02  |
| 12   | 40         | DCIN                             | 3/03  | Compal           | For ME change request                   | Change PBATT1                                                                                                                             | X02  |
| 13   | 40         | DCIN                             | 3/03  | Compal           | For EMC change request                  | Add PD5 PC20 PC21 PC22 Remove PC11                                                                                                        | X02  |
|      |            |                                  |       |                  |                                         |                                                                                                                                           |      |
|      |            |                                  |       |                  |                                         |                                                                                                                                           |      |

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LA-A902P

Monday, March 17, 2014 48 of 48

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| Item | Page#       | Title | Date       | Request Owner | Issue Description                                        | Solution Description                                                                                                                                                                                                                                                                                                                                                                                                                         | Rev.      |
|------|-------------|-------|------------|---------------|----------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| 1    | 6           | HW    | 2013/10/8  | COMPAL        | Follow intel reference circuit.                          | Add CC100, RC300 on CPU pin AC4, net name is PM_TEST_RST                                                                                                                                                                                                                                                                                                                                                                                     | 0.2 (X01) |
| 2    | 27          | HW    | 2013/10/8  | COMPAL        | Dell drop POA function.                                  | Change JUSH1 from 26 pin to 20 pin, pin define follow E5                                                                                                                                                                                                                                                                                                                                                                                     | 0.2 (X01) |
| 3    | 36          | HW    | 2013/10/8  | COMPAL        | Dell drop POA function.                                  | remove POA_WAKE# off page symbol<br>remove POA_ON/OFF#,make UE2.B62 to be NC pin                                                                                                                                                                                                                                                                                                                                                             | 0.2 (X01) |
| 4    | 22          | HW    | 2013/10/9  | COMPAL        |                                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                              | 0.2 (X01) |
| 5    | 24          | HW    | 2013/10/9  | COMPAL        | correct HDMI schematic error.                            | swap HDMI LANE0 & LANE2 BUS                                                                                                                                                                                                                                                                                                                                                                                                                  | 0.2 (X01) |
| 6    | 23          | HW    | 2013/10/9  | COMPAL        | Follow EMC suggestion                                    | Change LI1,LI2,LI3,LI4,LI5,LI6,LI7,LI8,LI9,LV3,LV6,LV10,LV12,LV27<br>From SM070003K00 (S COM FI_CHILISIN CMMI21T-900Y-N)<br>To SM070003Y00 (S COM FI_MURATA DLW21HN900HQ2L)                                                                                                                                                                                                                                                                  | 0.2 (X01) |
| 7    | 9           | HW    | 2013/10/9  | COMPAL        | reserved for S3 within 2s , system shutdown issue debug. | add RC26, reserved RC27.                                                                                                                                                                                                                                                                                                                                                                                                                     | 0.2 (X01) |
| 8    | 36          | HW    | 2013/10/9  | COMPAL        | board ID change.                                         | RE79 change to 130K                                                                                                                                                                                                                                                                                                                                                                                                                          | 0.2 (X01) |
| 9    | 24          | HW    | 2013/10/9  | COMPAL        | SATA circuit issue                                       | Swap mSATA P & N                                                                                                                                                                                                                                                                                                                                                                                                                             | 0.2 (X01) |
| 10   | 36          | HW    | 2013/10/14 | COMPAL        | follow intel latest design guide.                        | pop RE56 and change from 8.2K to 10K , it's RESET_OUT# pull down resistor                                                                                                                                                                                                                                                                                                                                                                    | 0.2 (X01) |
| 11   | 7           | HW    | 2013/10/16 | COMPAL        | RF requirement.                                          | add CC14, CC15 and move CC12, CC13 to behind the resistor (RC72)                                                                                                                                                                                                                                                                                                                                                                             | 0.2 (X01) |
| 12   | 20,23,31,32 | HW    | 2013/10/17 | COMPAL        | follow ESD recommend list.                               | change all ESD diode CPN<br>change DI2, DI3, DI5, DV4 from SCA00001100(S ZEN ROW PJDL05C 3P C/A SOT23) to SC600001600(S DIO ROW AZCI199-02S.R7G C/C SOT23 ESD)<br>change DI1,DI6,DI4 from SC300002800(S DIO(BR) TVWDF1004AD0 DFN ESD) to SC300002C00(S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD)<br>change DA1,DA2,DA3,DA6,DA7 from SCA00001L00(S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD) to SCA00002900(S ZEN ROW L03ESDL5V0CC3-2 C/A SOT-23 ESD) | 0.2 (X01) |
| 13   | 38          | HW    | 2013/10/17 | COMPAL        | power doesn't split VPRO & NPRO BOM.                     | add RZ41, RZ42, reserve it for VPRO & NVPRO option.                                                                                                                                                                                                                                                                                                                                                                                          | 0.2 (X01) |
| 14   | 39          | HW    | 2013/10/17 | COMPAL        | SSI design will cause LED behavior error.                | QL1 Pin2,5 & QL2 Pin2 change from MASK_BASE_LEDS# to SYS_LED_MASK#                                                                                                                                                                                                                                                                                                                                                                           | 0.2 (X01) |

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Doc. **LA-A972P**

Date: Monday, March 17, 2014 Sheet 69 of 76

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| Item | Page#        | Title | Date       | Request Owner | Issue Description                                           | Solution Description                                                                                                                                                                                                | Rev.      |
|------|--------------|-------|------------|---------------|-------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| 15   | 20           | HW    | 2013/10/17 | COMPAL        | To solve Line-on HDD dirty shut down issue.                 | UZ8 Pin2 change from +3.3V_ALW to 3.3V_RUN                                                                                                                                                                          | 0.2 (X01) |
| 16   | 28, 36, 38   | HW    | 2013/10/17 | COMPAL        | follow Dell requirement.                                    | Add back SUS_ON, change control pin from SUS_ON to SIO_SLP_S4#<br>1. UZ8.3 from SIO_SLP_S4# to SUS_ON<br>2. UE2.B23 -- SUS_ON_EC , RPE10.2 -- SUS_ON<br>3. add RE282, RE281, RE280, RE279<br>4. UE2.B9 -- RUN_ON_EC | 0.2 (X01) |
| 17   | 12           | HW    | 2013/10/24 | COMPAL        |                                                             |                                                                                                                                                                                                                     | 0.2 (X01) |
| 18   | 6            | HW    | 2013/10/24 | COMPAL        | debug usage.                                                | add RC301                                                                                                                                                                                                           | 0.2 (X01) |
| 19   | 9            | HW    | 2013/10/28 | COMPAL        | reserve it to prevent PCH_PLTRST# floating when power on    | add RC304, 100K pull down, on PCH_PLTRST#_EC                                                                                                                                                                        | 0.2 (X01) |
| 20   | 6, 7, 22, 28 | HW    | 2013/10/23 | COMPAL        | follow xtal vender suggest                                  | 1 CC1 &CC2 change from 18PF to 3PF<br>2 CC8 & CC11 change from 18PF to 15PF<br>3 CL13 & CL14 change from 33PF to 27PF<br>4 RV81 change from 0 ohm to 2.2K & CV113 change to 18PF                                    | 0.2 (X01) |
| 21   | 23           | HW    | 2013/10/29 | COMPAL        | it's designed for E5 Goliad, E6 GMLK doesn't need.          | remove RZ1                                                                                                                                                                                                          | 0.2 (X01) |
| 22   | 30           | HW    | 2013/10/29 | COMPAL        |                                                             |                                                                                                                                                                                                                     | 0.2 (X01) |
| 23   | 12           | HW    | 2013/10/29 | COMPAL        | To solve backdrive issue.                                   | Change TPM_PIRQ# pull up ( RC247) to +3.3V_RUN from +3.3V_ALW_PCH                                                                                                                                                   | 0.2 (X01) |
| 24   | 30           | HW    | 2013/10/30 | COMPAL        | Dell doesn't support MODPHY.                                | add PJP36, depop Q26, QZ10, RZ16, RZ5, CZ25, CZ38                                                                                                                                                                   | 0.2 (X01) |
| 25   | 7            | HW    | 2013/11/2  | COMPAL        | SMBUS Pull High                                             | Add RN3&RN4 pull high to +3.3V_RUN for DDR_XDP_WAN_SMBDAT/SMBCLK                                                                                                                                                    | 0.2 (X01) |
| 26   | 21           | HW    | 2013/11/2  | COMPAL        | EMC request.                                                | Add RA42, RA43.                                                                                                                                                                                                     | 0.2 (X01) |
| 27   | 21           | HW    | 2013/11/05 | COMPAL        | follow vender suggestion. It's for 15KV ESD fail issue.     | add CA12, CA13<br>change DA1, DA2, DA3, DA4 from GNDA to GND                                                                                                                                                        | 0.2 (X01) |
| 28   | 12           | HW    | 2013/11/05 | COMPAL        | GPIO 14 is sus power well, it has risk to cause back drive. | move TPM_PIRQ# from PCH_GPIO14 to PCH_GPIO17, add T21 on PCH_GPIO14                                                                                                                                                 | 0.2 (X01) |
| 39   | 21           | HW    | 2013/12/17 | COMPAL        |                                                             |                                                                                                                                                                                                                     | 0.3 (X01) |
| 40   | 22           | HW    | 2013/12/17 | COMPAL        |                                                             |                                                                                                                                                                                                                     | 0.3 (X01) |

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LA-A972P

Monday, March 17, 2014

Sheet 81 of 70

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| <i>Item</i> | <i>Page#</i> | <i>Title</i> | <i>Date</i> | <i>Request Owner</i> | <i>Issue Description</i>        | <i>Solution Description</i>                         | <i>Rev.</i> |
|-------------|--------------|--------------|-------------|----------------------|---------------------------------|-----------------------------------------------------|-------------|
| D<br>29     | 22           | HW           | 2013/12/17  | COMPAL               |                                 |                                                     | 0.3 (X01)   |
| E<br>30     | 22           | HW           | 2013/12/17  | COMPAL               | Base on Pre-PT RSMRST EA result | 1.POP RE88,UZ6,RE51<br>2.remove QZ12,RZ48,RZ49,RZ50 | 0.3 (X01)   |
| F<br>31     | 22           | HW           | 2013/12/17  | COMPAL               |                                 |                                                     | 0.3 (X01)   |
| G<br>32     | 7            | HW           | 2013/12/27  | COMPAL               | Intel recommend                 | Change RC33, RC34 from 1k to 499 ohm                | 0.3 (X01)   |
| H           |              |              |             |                      |                                 |                                                     |             |
| I           |              |              |             |                      |                                 |                                                     |             |
| J           |              |              |             |                      |                                 |                                                     |             |
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| A           |              |              |             |                      |                                 |                                                     |             |

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**EE P.I.R (3/3)**  
 Doc # \_\_\_\_\_  
 Date: Monday, March 17, 2014    Sheet 68 of 70

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