Compal Confidential

NAWE6 Schematics Document

AMD Danube

Champlain Processor with RS880M/SB820/Park VGA

2010-02-24

LA5754 REV: 0.2

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Issued Date	2008/10/06	Deciphered Date	2010/03/12	Title	Cover Page
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				Date: Monday, March 01, 2010	Sheet 1 of 47

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Model Name : AMD Danube + Park

ZZZ1 LA5754P DAZ@ DA80000IP00

POWER BD: (ZZZ2 LS-5758P @ DA40000TD00)
POWER BTN
NOVO BTN
POWER MANAGE BTN

CAP SENSOR BD: (ZZZ3 4 layer LS5756P @ DA40000T300)
VOLUME UP
VOLUME DOWN
MUTE
AUDIO ENHANCE
BUTTON & LED

CARD READER BD: (ZZZ4 LS5753P @ DA40000Q210)
RTS5159
HP JACK
MIC JACK

Danube

VRAM 512MB 64M16 x 4 page 18

DDR3

ATI M93-S3 Park - S3 uFCBGA-631 Page 13,14,15,16,17

PCI-Express x 16 Gen2

AMD S1G4 Processor uPGA-638 Package Champlain page 4,5,6,7

Hyper Transport Link 16 x 16

Memory BUS(DDR3) Dual Channel 1.5V DDRIII 800~1333MHz

204pin DDRIII-SO-DIMM X2 BANK 0, 1, 2, 3 page 8,9

ATI RS880M uFCBGA-528 page 10,11,12,13

Thermal Sensor ADM1032 page 6

Clock Generator ICS9LPRS488 page 19

LVDS page 27

CRT page 25

HDMI Conn. page 26

A link Express2 Gen1

ATI SB820M uFCBGA-605 page 20,21,22,23,24

page 37	page 37	page 27	page 37	page 28	page 28	page 28
USB PORT (LEFT)	USB conn (Right)	CMOS Camera	Bluetooth Conn <Option>	Mini card (WL)X1	3G/GPS WWAN <Option>	New Card
USB port 0	USB port 12	USB port 5	USB port 6	USB port 11	USB port 10	USB port 7

3.3V 48MHz USB

S-ATA Gen2

3.3V 24.576MHz/48Mhz HD Audio

New Card WLAN page 28 — GPP3

3G/WWAN MINI Card page 28 — GPP2 — SIM Card page28 — USB (WWAN)

MINI Card WLAN page 28 — GPP1

LAN(GbE) Atheros AR8151/8152 page 29 — GPP0 — RJ45 page 30

SATA HDD Conn. page 32 — port 0

CDROM Conn. page 32 — port 1

ESATA & USB Combine CON — USB port 4 — page28

LPC BUS

ENE KB926 page 34

Touch Pad page 35

Int.KBD page 35

BIOS page 34

Audio Codec Realtec ALC259 page33

Analog MIC_Int page33

2Channel Speaker page33

USB port 2 — Card Reader / Audio Jack SB CONN page38
RTS5159-GR MS/MS pro/SD/SD pro/mmc/XD
HP X 1+ MIC_Ext X1

LED page 36

LID SW / IO BD page 32

Power On/Off CKT. page 32

DC/DC Interface CKT. page 38

Fan Control page 31

Power Circuit page 39,40,41,42,43,44,45,46,47,48,49

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date 2009/10/06	Title: Block Diagrams

Size: B	Document Number: NAWE6 LA-5754P		Rev: 0.2
Date: Monday, March 01, 2010	Sheet 2 of 47		

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+0.75VS	+0.75VS LDO power rail for DDR3 VTT	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
EMC1402-1 (CPU)	100_1100b	4CH
EMC1412-A (GPU)	111_1100b	7CH
EMC1403-2 (DDR,WWAN)	100_1101b	4DH

SB820 SM Bus 0 address

Device	Address	HEX
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2
DDR DIMM1	1001 000Xb	90
DDR DIMM2	1001 010Xb	94

SB820 SM Bus 1 address

Device	Address

BOM Config

UMA only SKU: UMA@
DIS ONLY (Park S3): DIS@
EXT CLK Mode:EXT@
INT CLK mode:INT@
LAN GIGA: 8151@
LAN 100: 8152@
CMOS@
BT@
3G@
S@
H@

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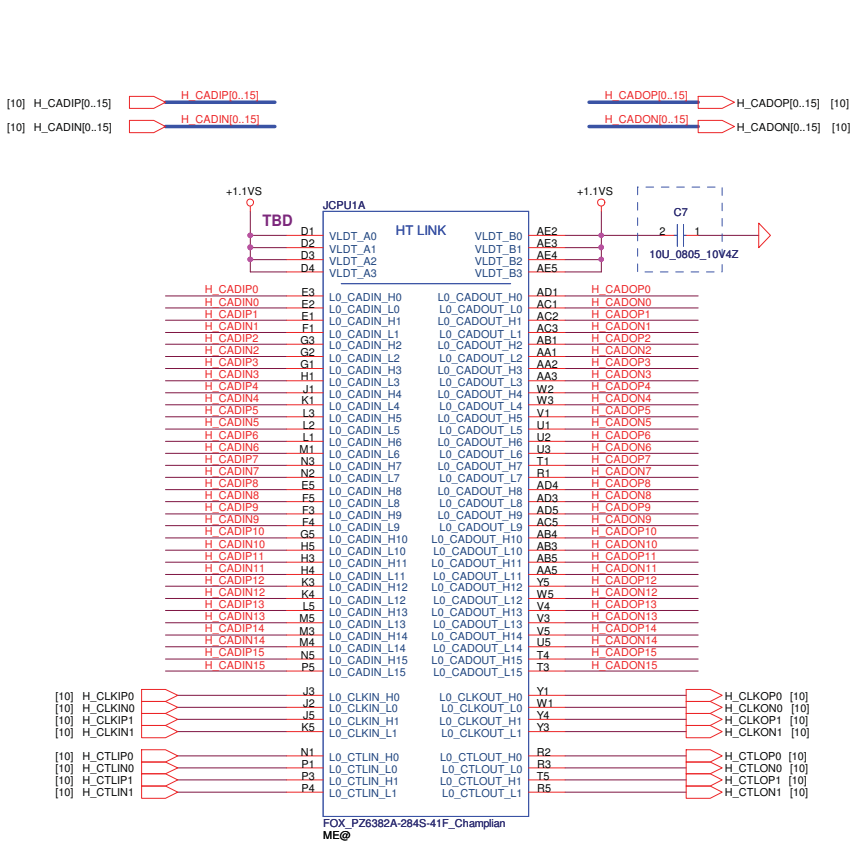
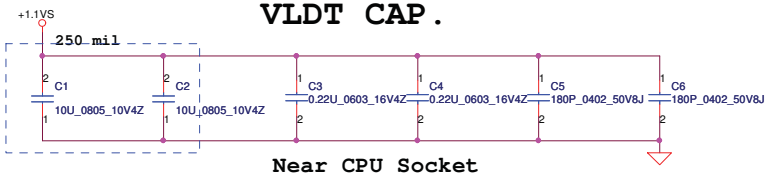
			Size: B; Document Number: NAWE6 LA-5754P; Rev: 0.2
			Date: Monday, March 01, 2010; Sheet 3 of 47





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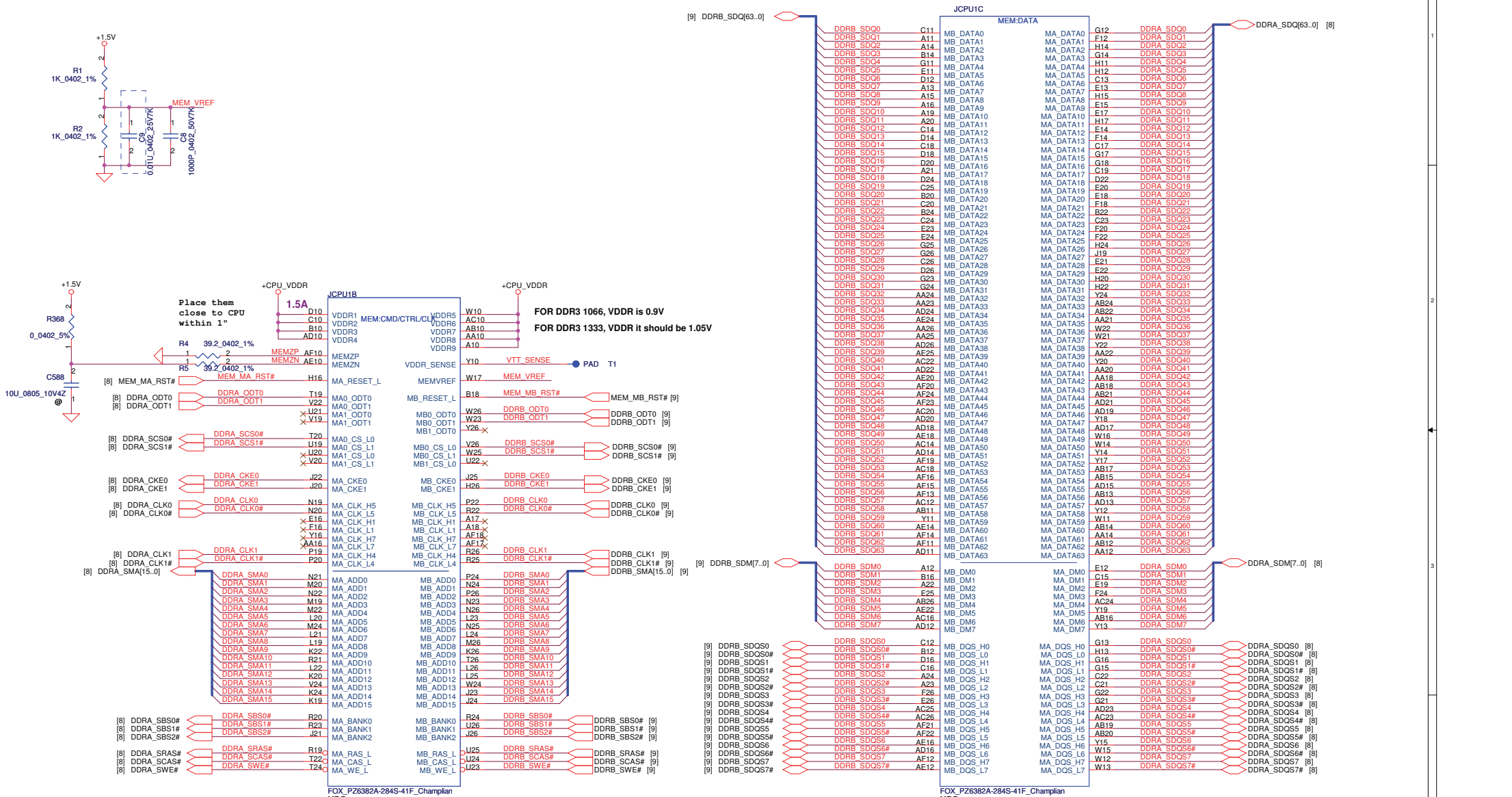
Issued Date	2008/10/06	Deciphered Date 2010/03/12	Title AMD CPU S1G4 HT I/F
Size Custom	Document Number NAWE6 LA-5754P		Rev 0.2
Date: Monday, March 01, 2010	Sheet 4 of 47		

Processor DDR3 Memory Interface



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Title: AMD CPU S1G4 DDRII I/F

Size: Custom	Document Number: NAWE6 LA-5754P	Rev: 0.2
Date: Monday, March 01, 2010	Sheet 5 of 47	

Champlain: C1E
C1E: LDT_REQ# no connect
CLMC: LDT_REQ# connect to NB

LDT_RES# / MEMHOT#
no support in S1g4

VDDA=0.25A

FOX_PZ6382A-284S-41F_Champlian
ME@

PROCHOT:
Input: For HTC Function
Output: Over Temperature Condition

For SCAN connect use

TI
TMP411ADGKR MSOP 8P
SA00002DE10
Address: 100 1100

EMC1402-1
(SA00001Z700)
Address 100_1100b
S IC EMC1402-1-ACZL-TR MSOP 8P SENSOR

EMC1402-1-ACZL-TR-MSOP-8P

CPU internal thermal sensor

FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V

2.09V for Gate

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Title: AMD CPU S1G4 CTRL

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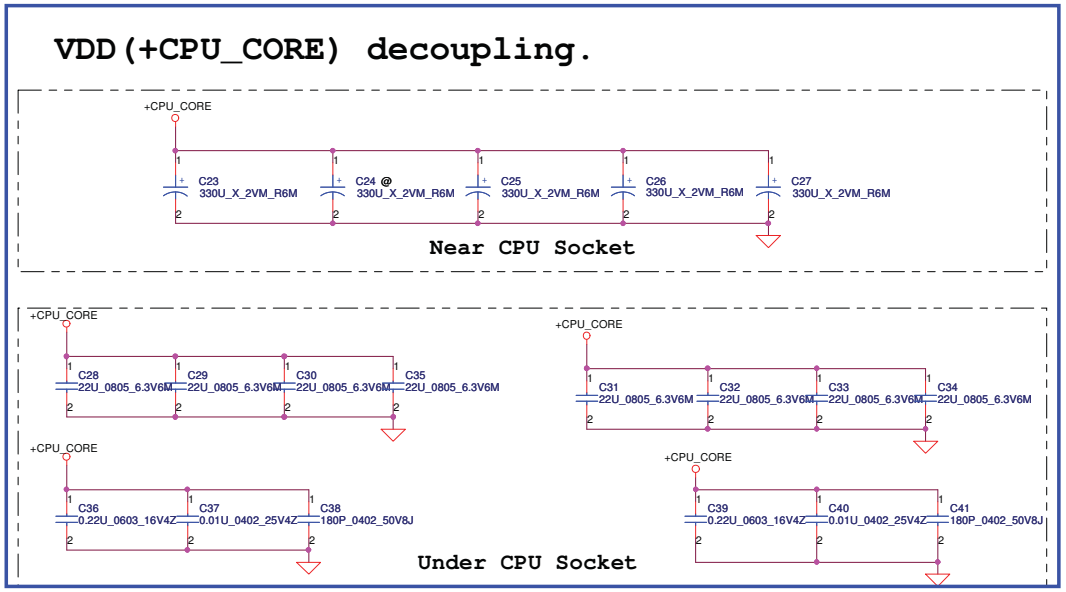
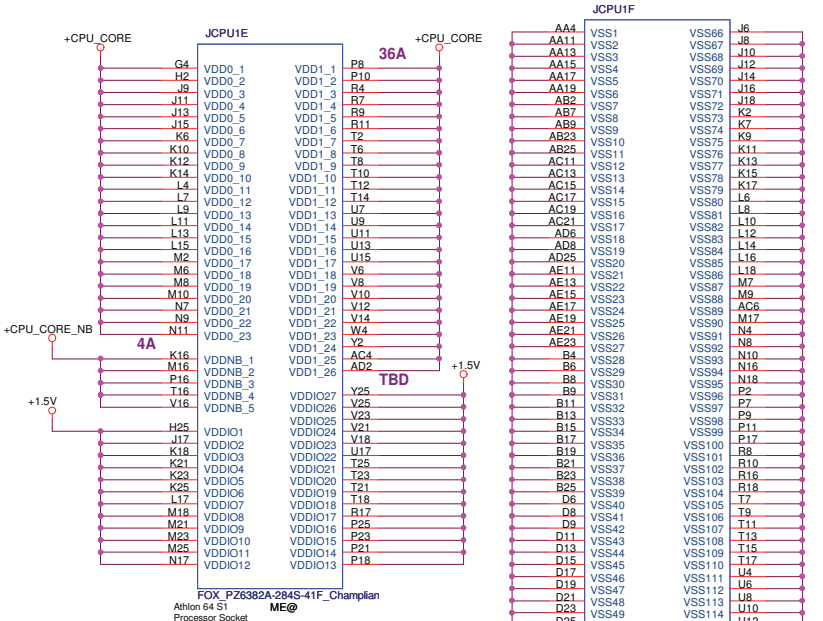
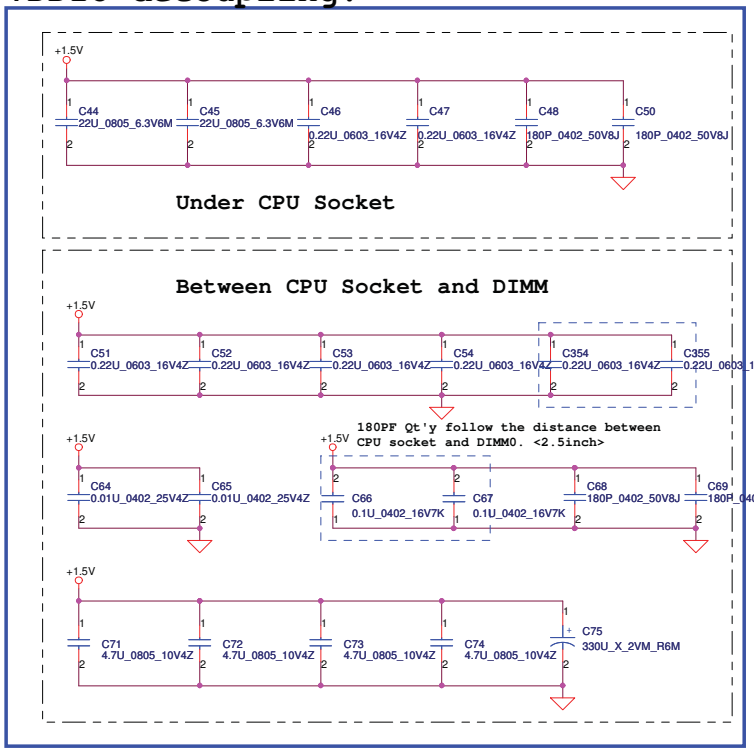
Date: Tuesday, March 02, 2010 | Sheet 6 of 47

VDD(+CPU_CORE) decoupling.

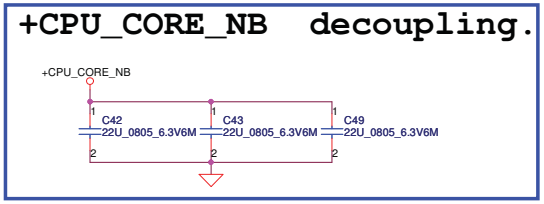




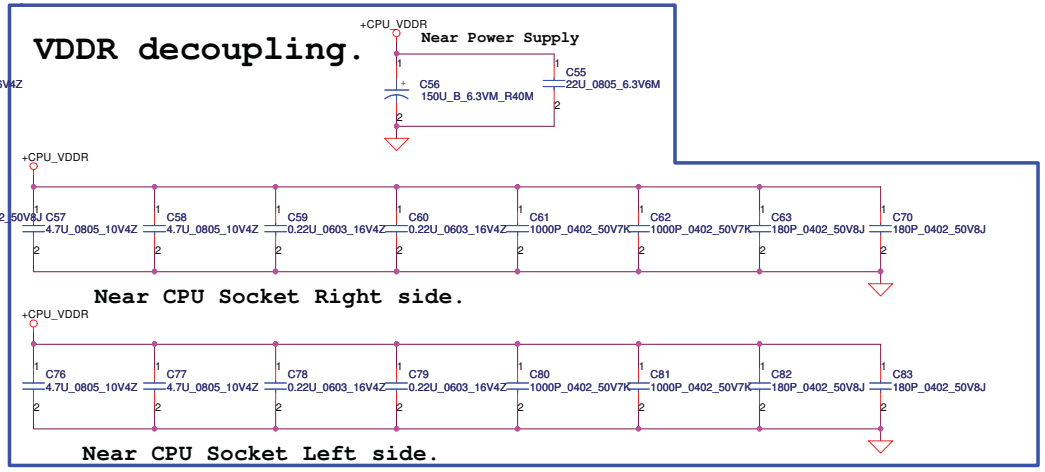
VDDIO decoupling.



+CPU_CORE_NB decoupling.



VDDR decoupling.



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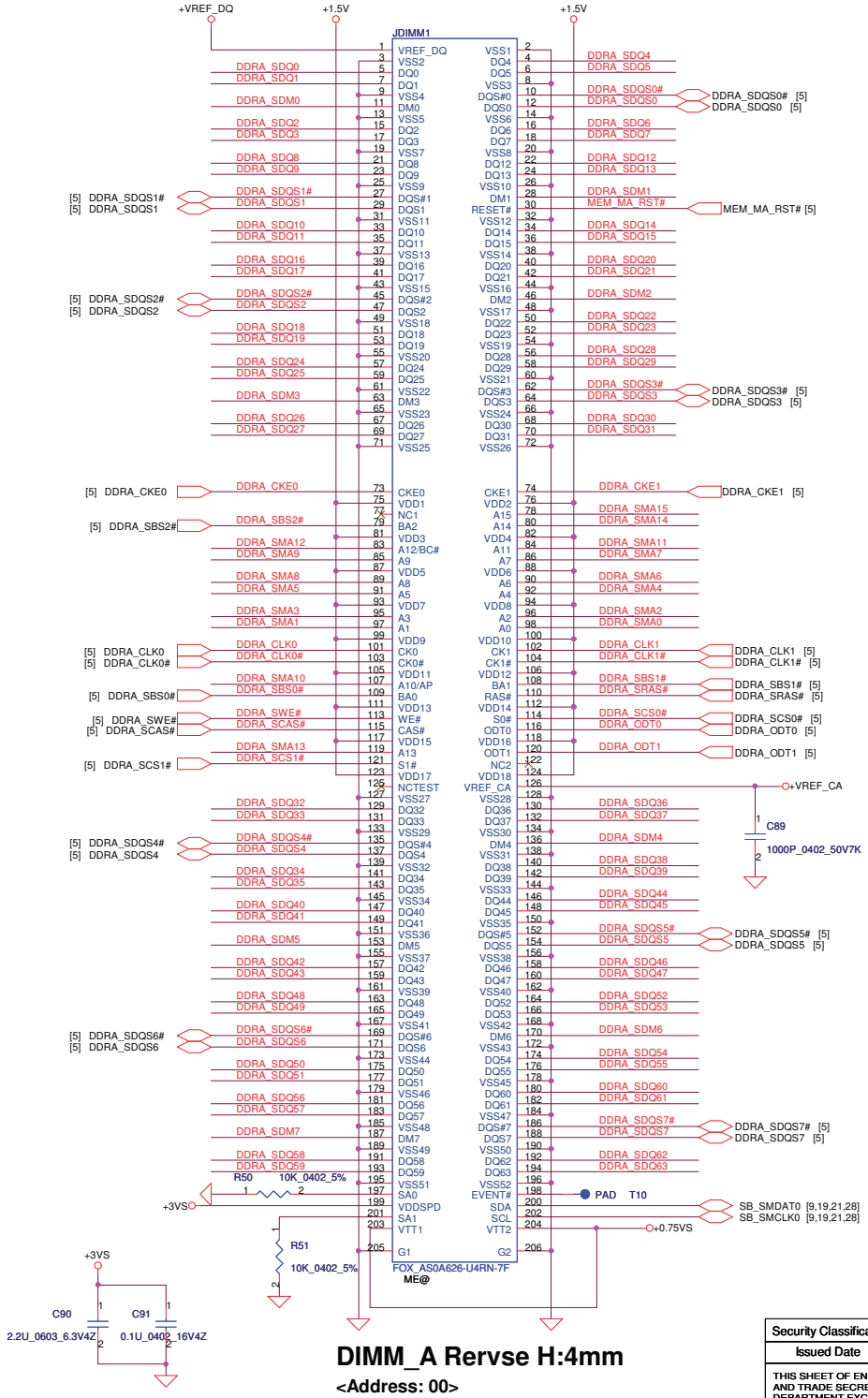
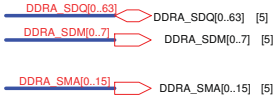
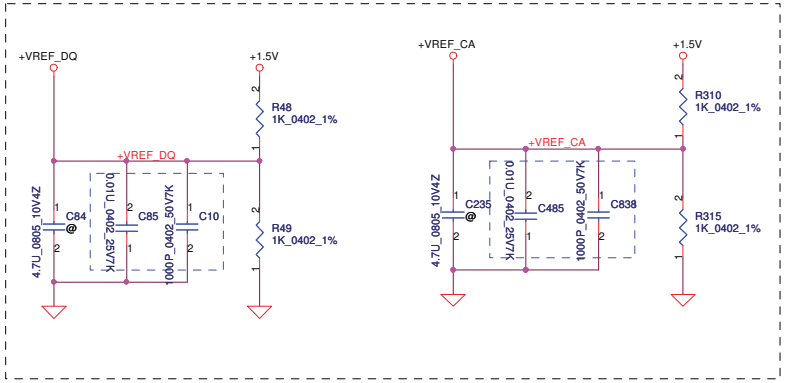
Title: AMD CPU S1G4 PWR & GND

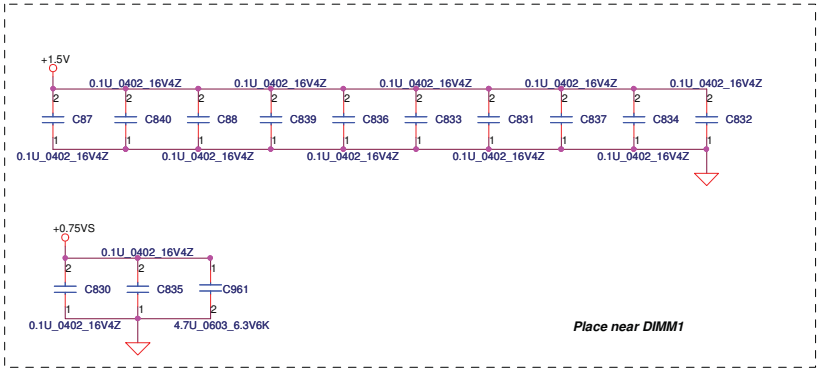
Size: Custom | Document Number: NAWE6 LA-5754P | Rev: 0.2

Date: Monday, March 01, 2010 | Sheet 7 of 47









DIMM_A Rervse H:4mm

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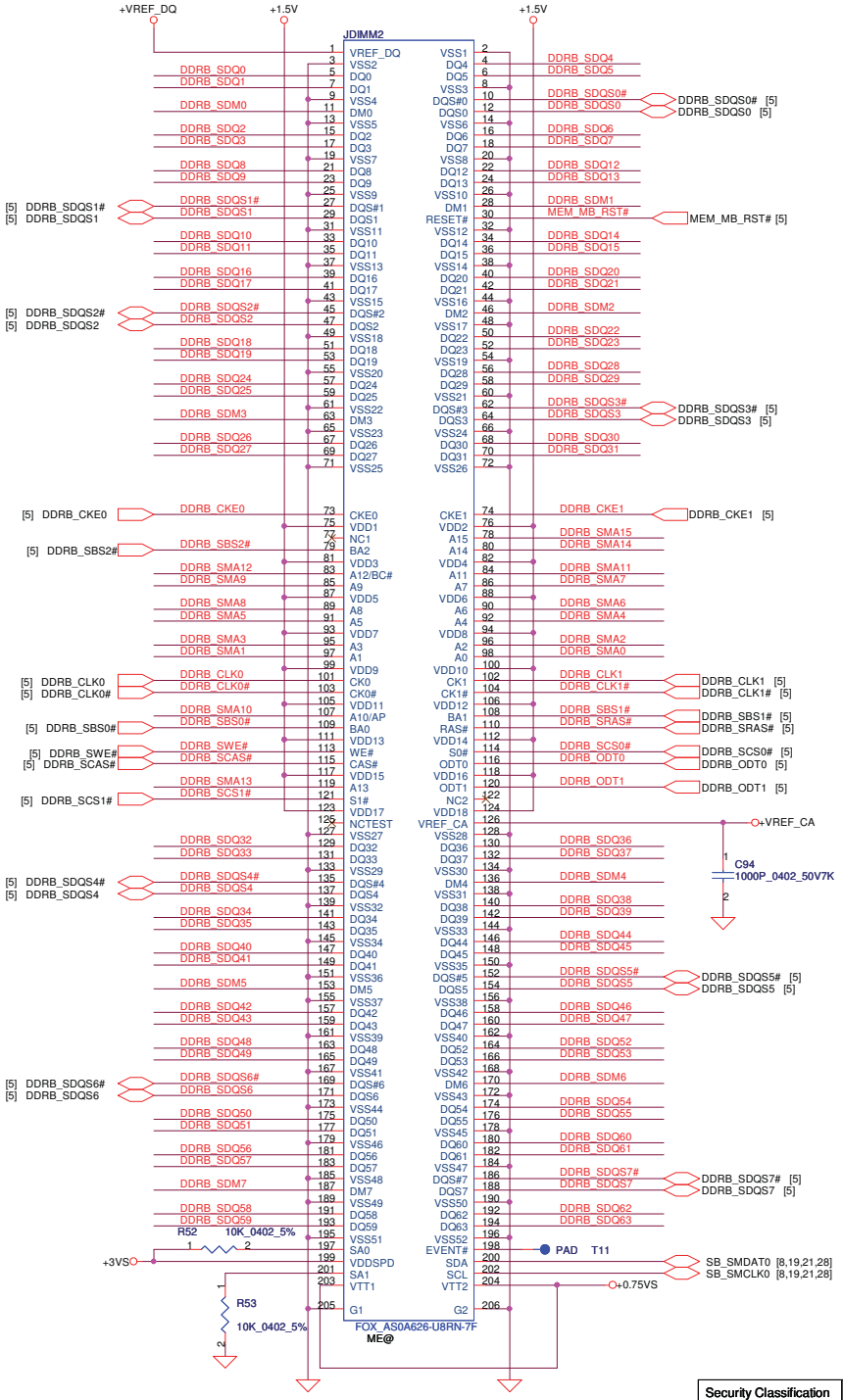
Title: DDRII SO-DIMM 1

Size: Custom | Document Number: NAWE6 LA-5754P | Rev: 0.2

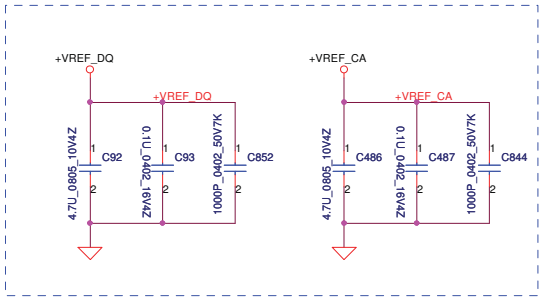
Date: Monday, March 01, 2010 | Sheet 8 of 47

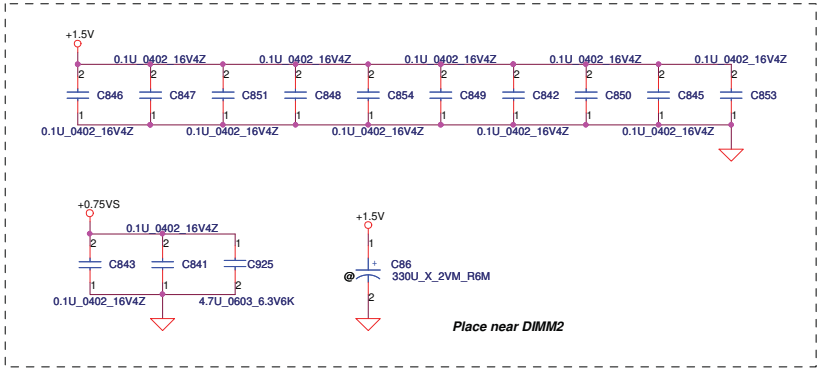


DDRB_SDQ[0..63] → DDRB_SDQ[0..63] [5]

DDRB_SDM[0..7] → DDRB_SDM[0..7] [5]

DDRB_SMA[0..15] → DDRB_SMA[0..15] [5]





DIMM_B Reverse H:8mm

<Address: 01>

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Title: DDRII SO-DIMM 2

Size: Custom | Document Number: NAWE6 LA-5754P | Rev: 0.2

Date: Monday, March 01, 2010 | Sheet 9 of 47

[13] PCIE_GTX_C_MRX_P[0..15] → PCIE_GTX_C_MRX_P[0..15]
[13] PCIE_GTX_C_MRX_N[0..15] → PCIE_GTX_C_MRX_N[0..15]

PCIE_MTX_C_GRX_P[0..15] → PCIE_MTX_C_GRX_P[0..15] [13]
PCIE_MTX_C_GRX_N[0..15] → PCIE_MTX_C_GRX_N[0..15] [13]

UMA HDMI

PCIE_MTX_GRX_P0	C488 1	2	UMA@ 0.1U_0402_16V7K	UMA_HDMI_P0 [26]
PCIE_MTX_GRX_N0	C489 1	2	UMA@ 0.1U_0402_16V7K	UMA_HDMI_N0 [26]
PCIE_MTX_GRX_P1	C491 1	2	UMA@ 0.1U_0402_16V7K	UMA_HDMI_P1 [26]
PCIE_MTX_GRX_N1	C490 1	2	UMA@ 0.1U_0402_16V7K	UMA_HDMI_N1 [26]
PCIE_MTX_GRX_P2	C497 1	2	UMA@ 0.1U_0402_16V7K	UMA_HDMI_P2 [26]
PCIE_MTX_GRX_N2	C500 1	2	UMA@ 0.1U_0402_16V7K	UMA_HDMI_N2 [26]
PCIE_MTX_GRX_P3	C499 1	2	UMA@ 0.1U_0402_16V7K	UMA_HDMI_P3 [26]
PCIE_MTX_GRX_N3	C498 1	2	UMA@ 0.1U_0402_16V7K	UMA_HDMI_N3 [26]

Cap close NB

U3B

PCIE_GTX_C_MRX_P0	D4	GFX_RX0P	PART 2 OF 6	GFX_TX0P	A5	PCIE_MTX_GRX_P0	C95 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P0
PCIE_GTX_C_MRX_N0	C4	GFX_RX0N		GFX_TX0N	B5	PCIE_MTX_GRX_N0	C96 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N0
PCIE_GTX_C_MRX_P1	A3	GFX_RX1P		GFX_TX1P	A4	PCIE_MTX_GRX_P1	C97 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P1
PCIE_GTX_C_MRX_N1	B3	GFX_RX1N		GFX_TX1N	B4	PCIE_MTX_GRX_N1	C98 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N1
PCIE_GTX_C_MRX_P2	C2	GFX_RX2P		GFX_TX2P	C3	PCIE_MTX_GRX_P2	C99 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P2
PCIE_GTX_C_MRX_N2	C1	GFX_RX2N		GFX_TX2N	B2	PCIE_MTX_GRX_N2	C100 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N2
PCIE_GTX_C_MRX_P3	E5	GFX_RX3P		GFX_TX3P	D1	PCIE_MTX_GRX_P3	C101 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P3
PCIE_GTX_C_MRX_N3	F5	GFX_RX3N		GFX_TX3N	D2	PCIE_MTX_GRX_N3	C102 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N3
PCIE_GTX_C_MRX_P4	G5	GFX_RX4P		GFX_TX4P	E2	PCIE_MTX_GRX_P4	C103 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P4
PCIE_GTX_C_MRX_N4	G6	GFX_RX4N		GFX_TX4N	E1	PCIE_MTX_GRX_N4	C104 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N4
PCIE_GTX_C_MRX_P5	H5	GFX_RX5P		GFX_TX5P	F4	PCIE_MTX_GRX_P5	C105 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P5
PCIE_GTX_C_MRX_N5	H6	GFX_RX5N		GFX_TX5N	F3	PCIE_MTX_GRX_N5	C106 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N5
PCIE_GTX_C_MRX_P6	J6	GFX_RX6P		GFX_TX6P	F1	PCIE_MTX_GRX_P6	C107 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P6
PCIE_GTX_C_MRX_N6	J5	GFX_RX6N		GFX_TX6N	F2	PCIE_MTX_GRX_N6	C108 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N6
PCIE_GTX_C_MRX_P7	J7	GFX_RX7P		GFX_TX7P	H4	PCIE_MTX_GRX_P7	C109 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P7
PCIE_GTX_C_MRX_N7	J8	GFX_RX7N		GFX_TX7N	H3	PCIE_MTX_GRX_N7	C110 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N7
PCIE_GTX_C_MRX_P8	L5	GFX_RX8P		GFX_TX8P	H1	PCIE_MTX_GRX_P8	C111 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P8
PCIE_GTX_C_MRX_N8	L6	GFX_RX8N		GFX_TX8N	H2	PCIE_MTX_GRX_N8	C112 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N8
PCIE_GTX_C_MRX_P9	M8	GFX_RX9P		GFX_TX9P	J2	PCIE_MTX_GRX_P9	C113 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P9
PCIE_GTX_C_MRX_N9	L8	GFX_RX9N		GFX_TX9N	J1	PCIE_MTX_GRX_N9	C114 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N9
PCIE_GTX_C_MRX_P10	P7	GFX_RX10P	PCIE I/F GFX	GFX_TX10P	K4	PCIE_MTX_GRX_P10	C115 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P10
PCIE_GTX_C_MRX_N10	M7	GFX_RX10N		GFX_TX10N	K3	PCIE_MTX_GRX_N10	C116 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N10
PCIE_GTX_C_MRX_P11	P5	GFX_RX11P		GFX_TX11P	K1	PCIE_MTX_GRX_P11	C117 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P11
PCIE_GTX_C_MRX_N11	M5	GFX_RX11N		GFX_TX11N	K2	PCIE_MTX_GRX_N11	C118 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N11
PCIE_GTX_C_MRX_P12	R8	GFX_RX12P		GFX_TX12P	M4	PCIE_MTX_GRX_P12	C119 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P12
PCIE_GTX_C_MRX_N12	P8	GFX_RX12N		GFX_TX12N	M3	PCIE_MTX_GRX_N12	C120 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N12
PCIE_GTX_C_MRX_P13	R6	GFX_RX13P		GFX_TX13P	M1	PCIE_MTX_GRX_P13	C121 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P13
PCIE_GTX_C_MRX_N13	R5	GFX_RX13N		GFX_TX13N	M2	PCIE_MTX_GRX_N13	C122 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N13
PCIE_GTX_C_MRX_P14	P4	GFX_RX14P		GFX_TX14P	N2	PCIE_MTX_GRX_P14	C123 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P14
PCIE_GTX_C_MRX_N14	P3	GFX_RX14N		GFX_TX14N	N1	PCIE_MTX_GRX_N14	C124 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N14
PCIE_GTX_C_MRX_P15	T4	GFX_RX15P		GFX_TX15P	P1	PCIE_MTX_GRX_P15	C125 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_P15
PCIE_GTX_C_MRX_N15	T3	GFX_RX15N		GFX_TX15N	P2	PCIE_MTX_GRX_N15	C126 1	2 DIS@ 0.1U_0402_16V7K PCIE_MTX_C_GRX_N15

	AE3	GPP_RX0P		GPP_TX0P	AC1			
	AD4	GPP_RX0N		GPP_TX0N	AC2			
[28] PCIE_PTX_C_IRX_P1	AE2	GPP_RX1P		GPP_TX1P	AB4	PCIE_ITX_PRX_P1	C201 1	2 0.1U_0402_16V7K PCIE_ITX_C_PRX_P1 [28] WLAN
[28] PCIE_PTX_C_IRX_N1	AD3	GPP_RX1N		GPP_TX1N	AB3	PCIE_ITX_PRX_N1	C200 1	2 0.1U_0402_16V7K PCIE_ITX_C_PRX_N1 [28] WLAN
[29] PCIE_PTX_C_IRX_P2	AD1	GPP_RX2P		GPP_TX2P	AA2	PCIE_ITX_PRX_P2	C482 1	2 0.1U_0402_16V7K PCIE_ITX_C_PRX_P2 [29] GLAN
[29] PCIE_PTX_C_IRX_N2	AD2	GPP_RX2N	PCIE I/F GPP	GPP_TX2N	AA1	PCIE_ITX_PRX_N2	C481 1	2 0.1U_0402_16V7K PCIE_ITX_C_PRX_N2 [29] GLAN
[28] PCIE_PTX_C_IRX_P3	V5	GPP_RX3P		GPP_TX3P	Y1	PCIE_ITX_PRX_P3	C484 1	2 3G@ 0.1U_0402_16V7K PCIE_ITX_C_PRX_P3 [28] WWAN
[28] PCIE_PTX_C_IRX_N3	W5	GPP_RX3N		GPP_TX3N	Y2	PCIE_ITX_PRX_N3	C483 1	2 3G@ 0.1U_0402_16V7K PCIE_ITX_C_PRX_N3 [28] WWAN
	U5	GPP_RX4P		GPP_TX4P	Y4			
	U6	GPP_RX4N		GPP_TX4N	Y3			
	U8	GPP_RX5P		GPP_TX5P	V1			
	U7	GPP_RX5N		GPP_TX5N	V2			

[20] SB_RX0P	AA8	SB_RX0P		SB_TX0P	AD7	SB_TX0P_C	C133 1	2 0.1U_0402_16V7K SB_TX0P [20]
[20] SB_RX0N	Y8	SB_RX0N		SB_TX0N	AE7	SB_TX0N_C	C134 1	2 0.1U_0402_16V7K SB_TX0N [20]
[20] SB_RX1P	AA7	SB_RX1P		SB_TX1P	AE6	SB_TX1P_C	C135 1	2 0.1U_0402_16V7K SB_TX1P [20]
[20] SB_RX1N	Y7	SB_RX1N		SB_TX1N	AD6	SB_TX1N_C	C136 1	2 0.1U_0402_16V7K SB_TX1N [20]
[20] SB_RX2P	AA5	SB_RX2P	PCIE I/F SB	SB_TX2P	AB6	SB_TX2P_C	C137 1	2 0.1U_0402_16V7K SB_TX2P [20]
[20] SB_RX2N	AA6	SB_RX2N		SB_TX2N	AC6	SB_TX2N_C	C138 1	2 0.1U_0402_16V7K SB_TX2N [20]
[20] SB_RX3P	W5	SB_RX3P		SB_TX3P	AD5	SB_TX3P_C	C139 1	2 0.1U_0402_16V7K SB_TX3P [20]
[20] SB_RX3N	Y5	SB_RX3N		SB_TX3N	AE5	SB_TX3N_C	C140 1	2 0.1U_0402_16V7K SB_TX3N [20]

PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)

AC8 — R59 1 2 1.27K_0402_1%
AB8 — R58 1 2 2K_0402_1%
+1.1VS

RS880M_FCBGA528

RS880 A11(SA000032710)

[4] H_CADOP[0..15] → H_CADOP[0..15]
[4] H_CADON[0..15] → H_CADON[0..15]
H_CADIP[0..15] → H_CADIP[0..15] [4]
H_CADIN[0..15] → H_CADIN[0..15] [4]

U3A

H_CADOP0	Y25	HT_RXCAD0P	PART 1 OF 6	HT_TXCAD0P	D24	H_CADIP0	
H_CADON0	Y24	HT_RXCAD0N		HT_TXCAD0N	D25	H_CADIN0	
H_CADOP1	V22	HT_RXCAD1P		HT_TXCAD1P	E24	H_CADIP1	
H_CADON1	V23	HT_RXCAD1N		HT_TXCAD1N	E25	H_CADIN1	
H_CADOP2	V25	HT_RXCAD2P		HT_TXCAD2P	F24	H_CADIP2	
H_CADON2	V24	HT_RXCAD2N		HT_TXCAD2N	F25	H_CADIN2	
H_CADOP3	U24	HT_RXCAD3P		HT_TXCAD3P	F23	H_CADIP3	
H_CADON3	U25	HT_RXCAD3N		HT_TXCAD3N	F22	H_CADIN3	
H_CADOP4	T25	HT_RXCAD4P		HT_TXCAD4P	H23	H_CADIP4	
H_CADON4	T24	HT_RXCAD4N		HT_TXCAD4N	H22	H_CADIN4	
H_CADOP5	P22	HT_RXCAD5P		HT_TXCAD5P	J25	H_CADIP5	
H_CADON5	P23	HT_RXCAD5N		HT_TXCAD5N	J24	H_CADIN5	
H_CADOP6	P25	HT_RXCAD6P		HT_TXCAD6P	K24	H_CADIP6	
H_CADON6	P24	HT_RXCAD6N		HT_TXCAD6N	K25	H_CADIN6	
H_CADOP7	N24	HT_RXCAD7P		HT_TXCAD7P	K23	H_CADIP7	
H_CADON7	N25	HT_RXCAD7N		HT_TXCAD7N	K22	H_CADIN7	
H_CADOP8	AC24	HT_RXCAD8P	HYPER TRANSPORT CPU I/F	HT_TXCAD8P	F21	H_CADIP8	
H_CADON8	AC25	HT_RXCAD8N		HT_TXCAD8N	G21	H_CADIN8	
H_CADOP9	AB25	HT_RXCAD9P		HT_TXCAD9P	G20	H_CADIP9	
H_CADON9	AB24	HT_RXCAD9N		HT_TXCAD9N	H21	H_CADIN9	
H_CADOP10	AA24	HT_RXCAD10P		HT_TXCAD10P	J20	H_CADIP10	
H_CADON10	AA25	HT_RXCAD10N		HT_TXCAD10N	J21	H_CADIN10	
H_CADOP11	Y22	HT_RXCAD11P		HT_TXCAD11P	J18	H_CADIP11	
H_CADON11	Y23	HT_RXCAD11N		HT_TXCAD11N	K17	H_CADIN11	
H_CADOP12	W21	HT_RXCAD12P		HT_TXCAD12P	L19	H_CADIP12	
H_CADON12	W20	HT_RXCAD12N		HT_TXCAD12N	J19	H_CADIN12	
H_CADOP13	V21	HT_RXCAD13P		HT_TXCAD13P	M19	H_CADIP13	
H_CADON13	V20	HT_RXCAD13N		HT_TXCAD13N	L18	H_CADIN13	
H_CADOP14	U20	HT_RXCAD14P		HT_TXCAD14P	M21	H_CADIP14	
H_CADON14	U21	HT_RXCAD14N		HT_TXCAD14N	P21	H_CADIN14	
H_CADOP15	U19	HT_RXCAD15P		HT_TXCAD15P	P18	H_CADIP15	
H_CADON15	U18	HT_RXCAD15N		HT_TXCAD15N	M18	H_CADIN15	

[4] H_CLKOP0	T22	HT_RXCLK0P		HT_TXCLK0P	H24	H_CLKIP0 [4]
[4] H_CLKON0	T23	HT_RXCLK0N		HT_TXCLK0N	H25	H_CLKIN0 [4]
[4] H_CLKOP1	AB23	HT_RXCLK1P		HT_TXCLK1P	L21	H_CLKIP1 [4]
[4] H_CLKON1	AA22	HT_RXCLK1N		HT_TXCLK1N	L20	H_CLKIN1 [4]
[4] H_CTLOP0	H_CTLOP0 M22	HT_RXCTL0P		HT_TXCTL0P	M24	H_CTLIP0 [4]
[4] H_CTLON0	H_CTLON0 M23	HT_RXCTL0N		HT_TXCTL0N	M25	H_CTLIN0 [4]
[4] H_CTLOP1	H_CTLOP1 R21	HT_RXCTL1P		HT_TXCTL1P	P19	H_CTLIP1 [4]
[4] H_CTLON1	H_CTLON1 R20	HT_RXCTL1N		HT_TXCTL1N	R18	H_CTLIN1 [4]

1 R60 2 — HT_RXCALP C23 — HT_RXCALN A24 — 301_0402_1%
Place within 1" layout 1:2

HT_RXCALP
HT_RXCALN

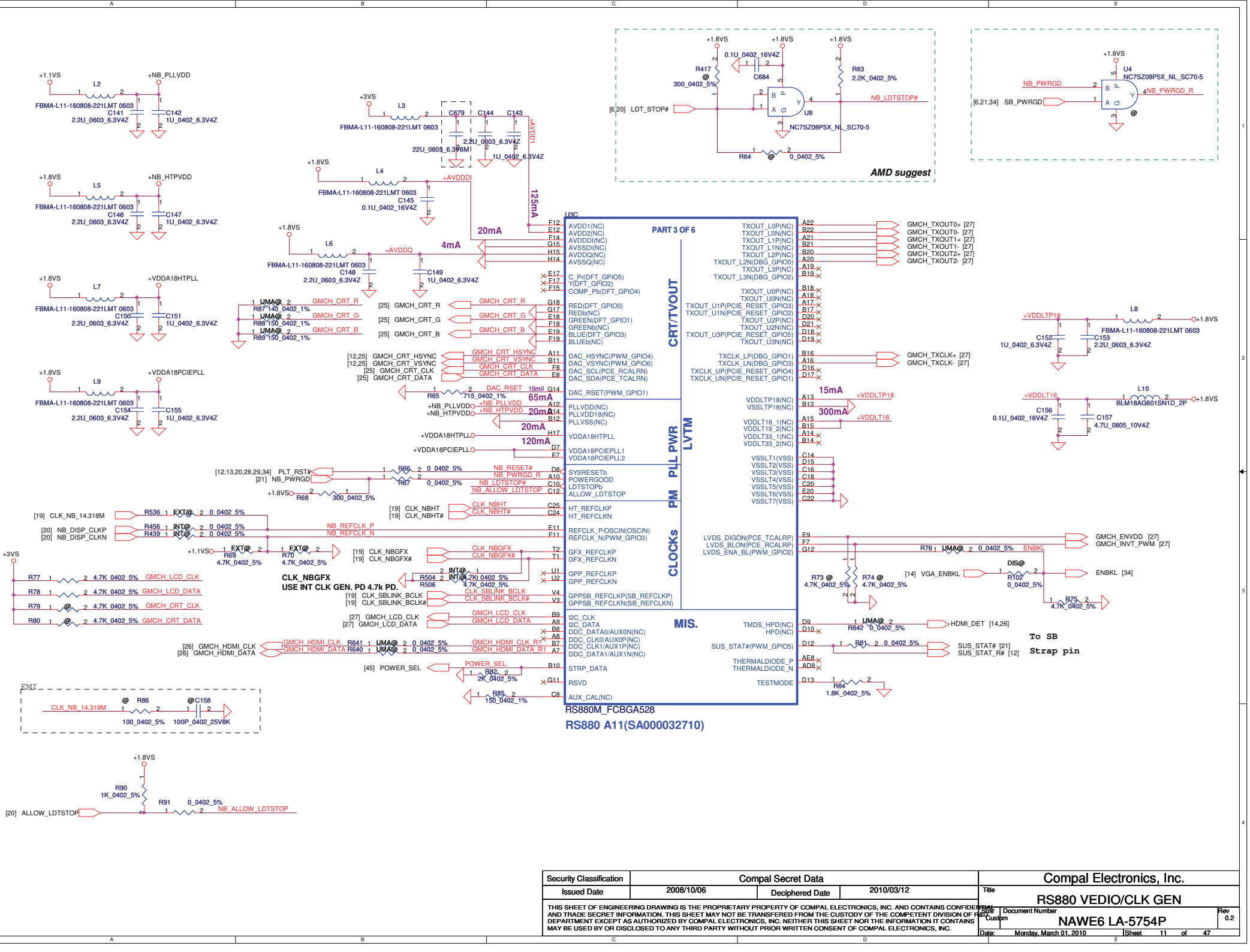
HT_TXCALP B24 — R61 2 — HT_TXCALN B25 — 301_0402_1%
Place within 1" layout 1:2

RS880M_FCBGA528

RS880 A11(SA000032710)

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date 2010/03/12	Title RS880-HT/PCIE

Size Custom	Document Number NAWE6 LA-5754P		Rev 0.2
Date: Monday, March 01, 2010	Sheet 10 of 47		



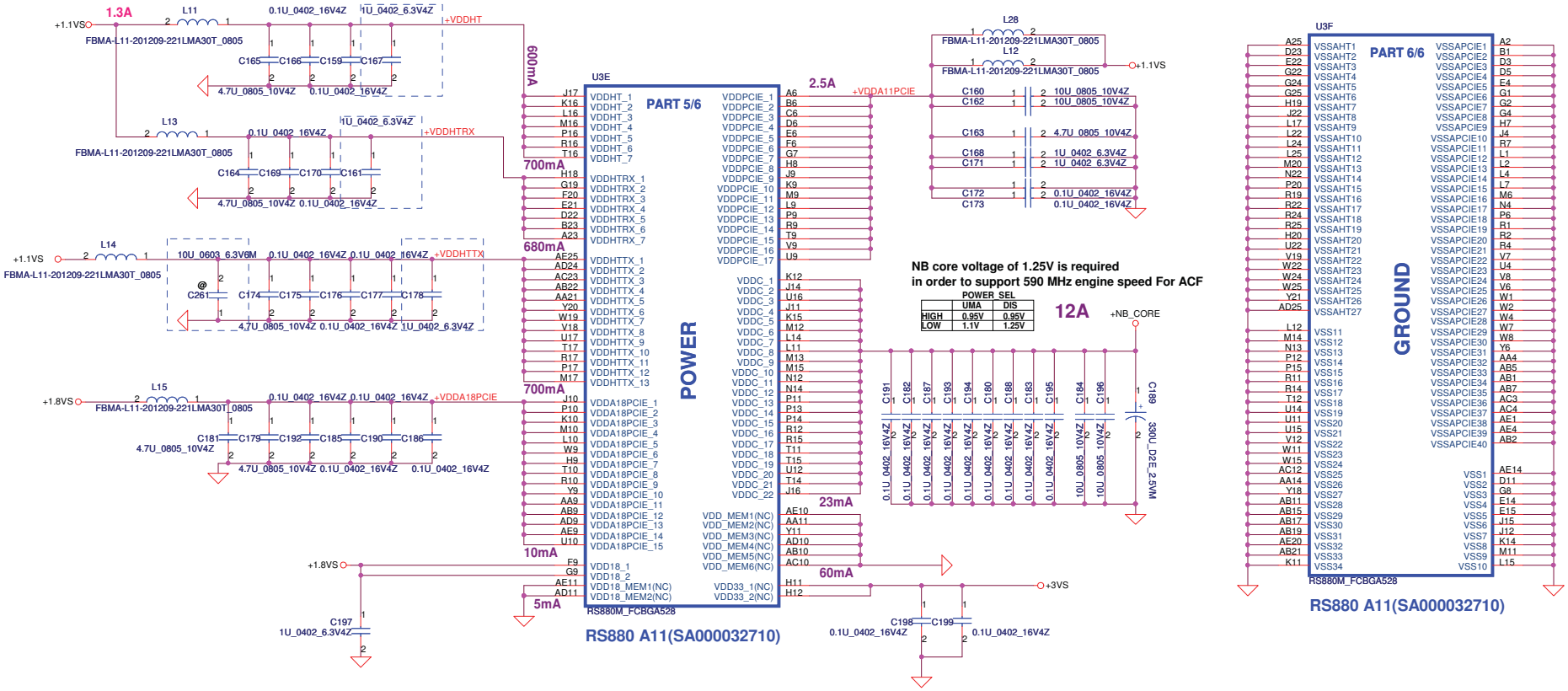
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

Title: RS880 VEDIO/CLK GEN

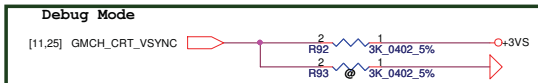
Size: B (Custom) | Document Number: NAWE6 LA-5754P | Rev: 0.2

Date: Monday, March 01, 2010 | Sheet 11 of 47

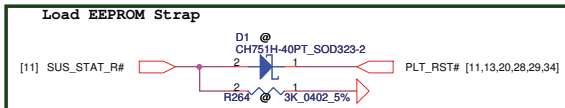


Side port and Strap setting

Debug Mode



Load EEPROM Strap



Enable Side Port Memory

DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

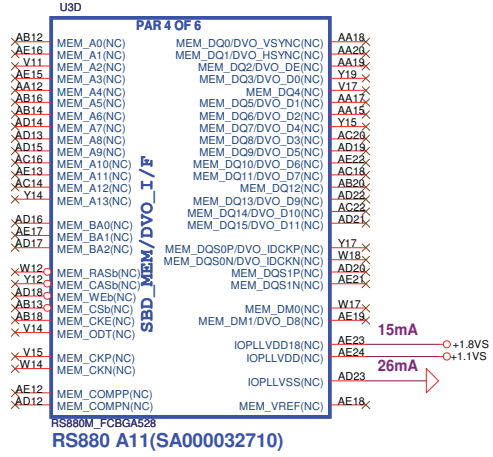
```
Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable
0 : Enable
```

DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
```

Enable Side Port Memory

```
RS880: HSYNC#
0:   Enable        Register Readback of strap:
1 :  Disable       NB_CLKCFG:CLK_TOP_SPARE_D[1]
```



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

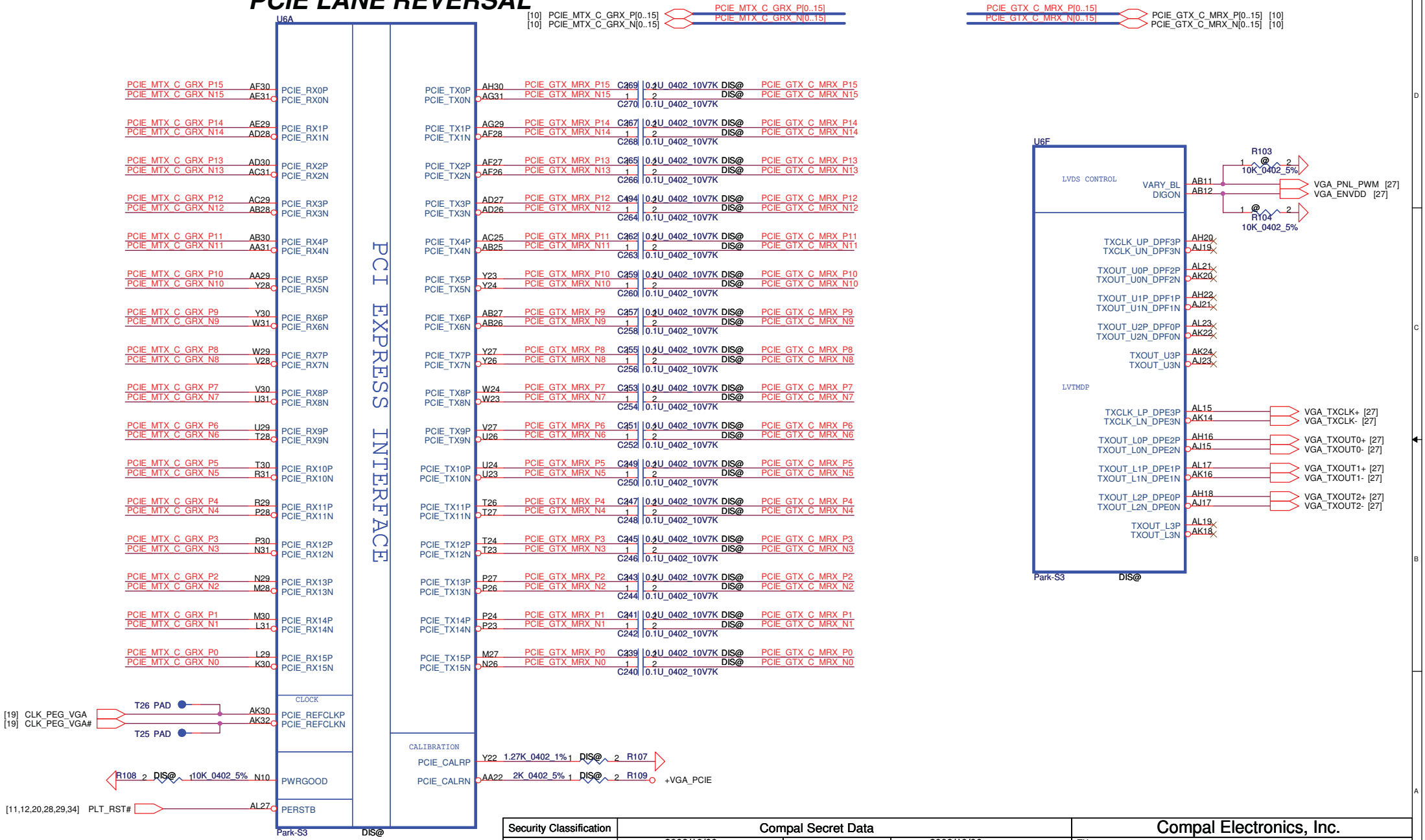
Compal Electronics, Inc.

Title: RS880 PWR/GND

Size: Custom | Document Number: NAWE6 LA-5754P | Rev: 0.2

Date: Monday, March 01, 2010 | Sheet 12 of 47

PCIE LANE REVERSAL



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: PARK-S3 PCIE/LVDS

Size	Document Number	Rev
Custom	NAWE6 LA-5754P	0.2

Date: Tuesday, March 02, 2010 Sheet 13 of 47

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	0
	GPIO8		0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
	H2SYNC		0
	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

STRAPS

GPU_GPIO0 R111 10K 0402 5%
GPU_GPIO1 R112 10K 0402 5%
GPU_GPIO2 R113 10K 0402 5%
GPU_GPIO8 R114 10K 0402 5%
GPU_GPIO9 R115 10K 0402 5%
GPU_GPIO11 R117 10K 0402 5%
GPU_GPIO12 R118 10K 0402 5%
GPU_GPIO13 R119 10K 0402 5%
VGA_CRT_HSYNC R120 10K 0402 5%
VGA_CRT_VSYNC R121 10K 0402 5%
VGA_CRT_VSYNC2 R122 10K 0402 5%
VGA_CRT_HSYNC2 R123 10K 0402 5%

VGA Thermal Sensor ADM1032 Closed to GPU

EMC1412-A (SA00003Y40L)
Address 1111_100xb
S IC EMC1412-A-ACZL-TR MSOP 8P SENSOR

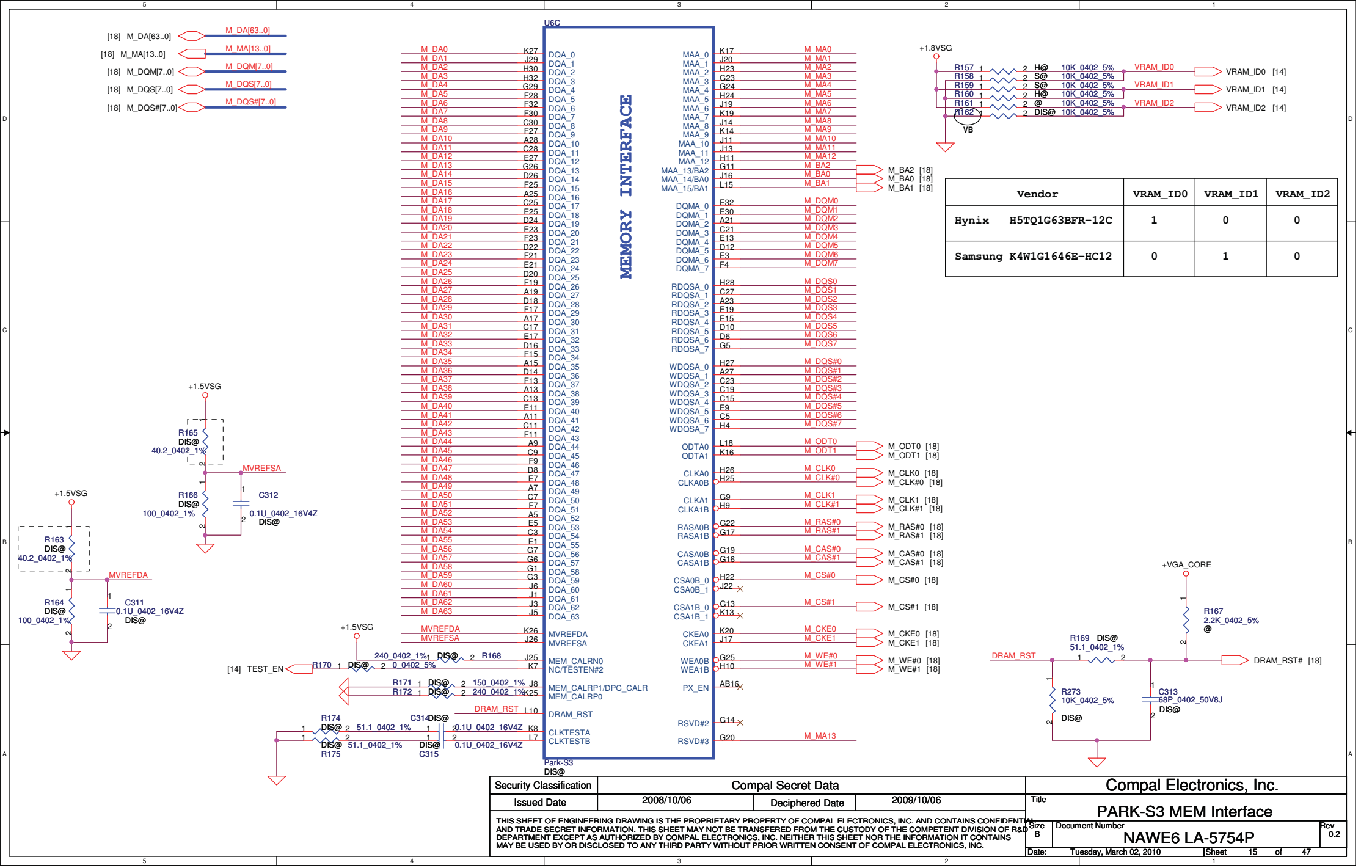
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: PARK-S3 Main Generic/MSIC

Size	Document Number	Rev
C	NAWE6 LA-5754P	0.2

Date: Tuesday, March 02, 2010 Sheet 14 of 47



Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix H5TQ1G63BFR-12C	1	0	0
Samsung K4W1G1646E-HC12	0	1	0

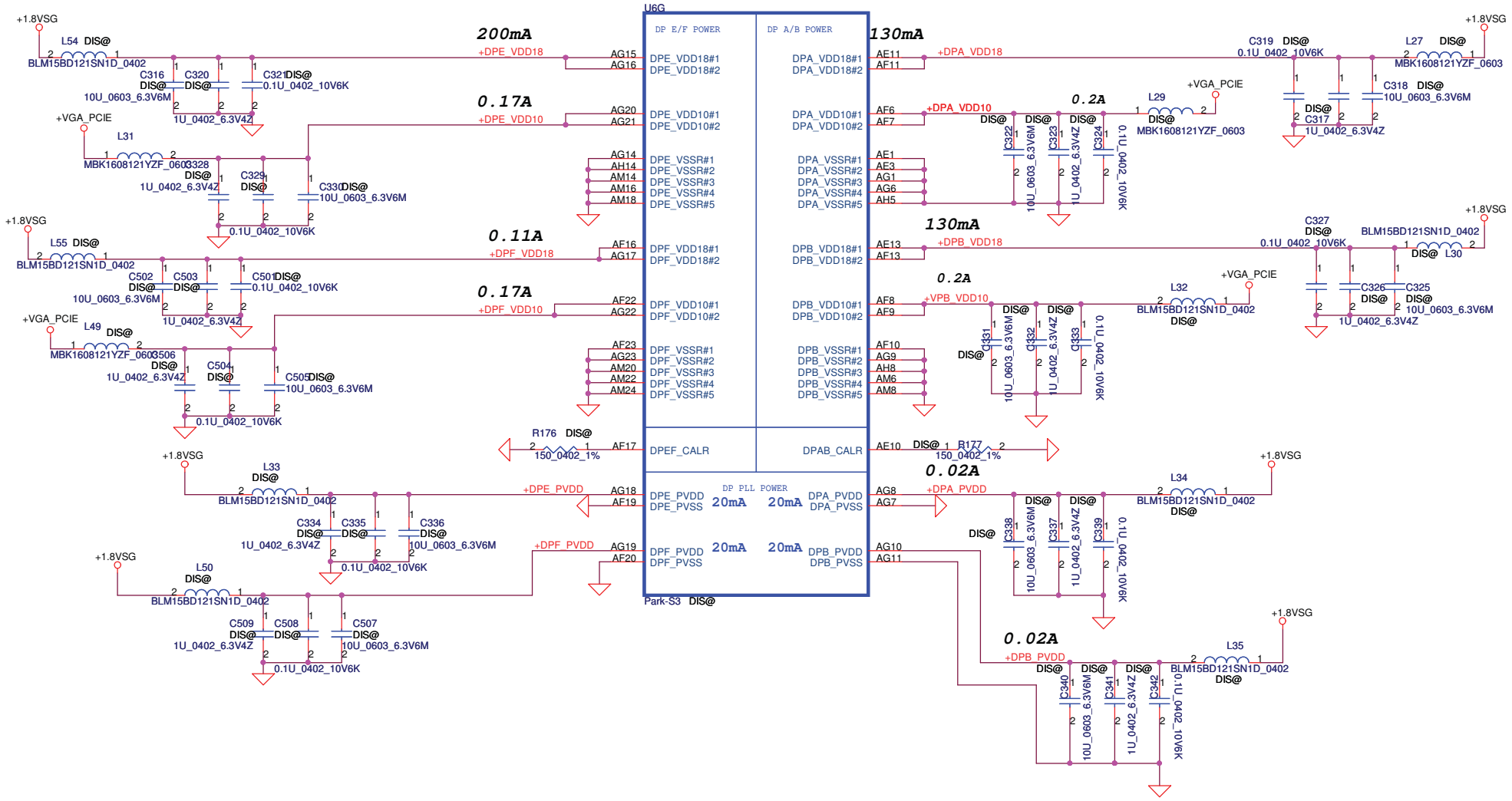
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Title: PARK-S3 MEM Interface

Size: B | Document Number: NAWE6 LA-5754P | Rev: 0.2

Date: Tuesday, March 02, 2010 | Sheet 15 of 47

DPE_VDD10 DPF_VDD10	Park-S3: TMDS/DP=110mA@1.0V : LVDS=120mA@1.0V



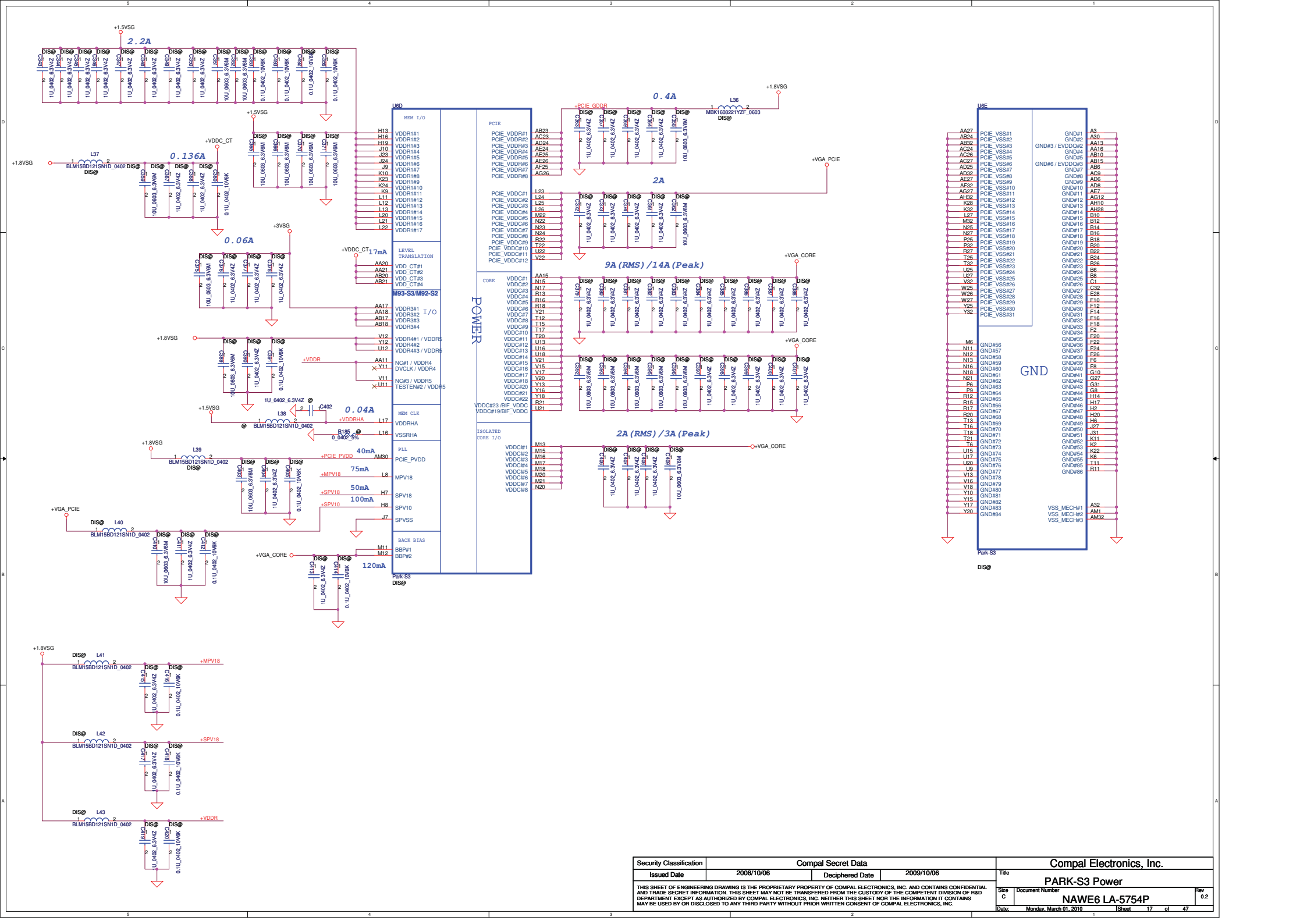
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: PARK-S3 DPX Power

Size: B | Document Number: NAWE6 LA-5754P | Rev: 0.2

Date: Monday, March 01, 2010 | Sheet 16 of 47



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

Title: PARK-S3 Power

Size	Document Number	Rev
C	NAWE6 LA-5754P	0.2

Date: Monday, March 01, 2010 Sheet 17 of 47

[15] M_DA[63..0] → M_DA[63..0]
[15] M_MA[13..0] → M_MA[13..0]
[15] M_DQM[7..0] → M_DQM[7..0]
[15] M_DQS[7..0] → M_DQS[7..0]
[15] M_DQS#[7..0] → M_DQS#[7..0]

X76-H Hynix X76H@ X76223381.02
X76-S Samsung X76S@ X76223381.01

U9 SAMSUNG VRAM S@
U10 SAMSUNG VRAM S@
U11 SAMSUNG VRAM S@
U12 SAMSUNG VRAM S@

100-BALL SDRAM DDR3 64MX16 H5TQ1G63BFR-12C FBGA H@

R189 240_0402_1% DIS@
R190 240_0402_1% DIS@
R191 240_0402_1% DIS@
R192 240_0402_1% DIS@

R193 4.99K_0402_1% DIS@ — VREFD_Q1
R194 4.99K_0402_1% DIS@ — VREFC_A1
R195 4.99K_0402_1% DIS@ — VREFC_A2
R196 4.99K_0402_1% DIS@ — VREFD_Q2
R197 4.99K_0402_1% DIS@ — VREFC_A3
R198 4.99K_0402_1% DIS@ — VREFD_Q3
R199 4.99K_0402_1% DIS@ — VREFC_A4
R200 4.99K_0402_1% DIS@ — VREFD_Q4
R201 4.99K_0402_1% DIS@
R202 4.99K_0402_1% DIS@
R203 4.99K_0402_1% DIS@
R204 4.99K_0402_1% DIS@
R205 4.99K_0402_1% DIS@
R206 4.99K_0402_1% DIS@
R207 4.99K_0402_1% DIS@
R208 4.99K_0402_1% DIS@
C421–C426 0.1U_0402_10V6K DIS@

M_CLK0 R209 56_0402_1%
M_CLK#0 R211 56_0402_1%
C455 0.01U_0402_16V7K DIS@
M_CLK1 R210 56_0402_1%
M_CLK#1 R212 56_0402_1%
C456 0.01U_0402_16V7K DIS@

C446 C429 C447 C448 C449 C430 10U_0603_6.3V6M DIS@

C431–C439 1U_0402_6.3V4Z DIS@
C440–C445 1U_0402_6.3V4Z DIS@

VRAM P/N :
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

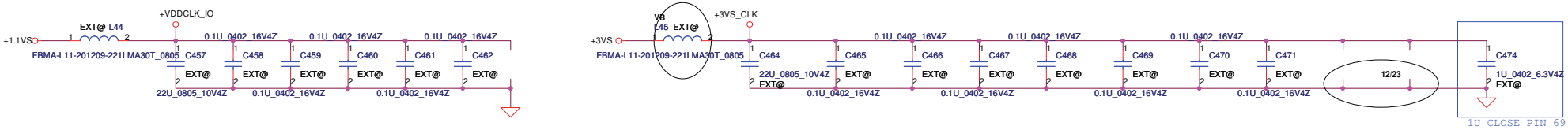
Compal Electronics, Inc.

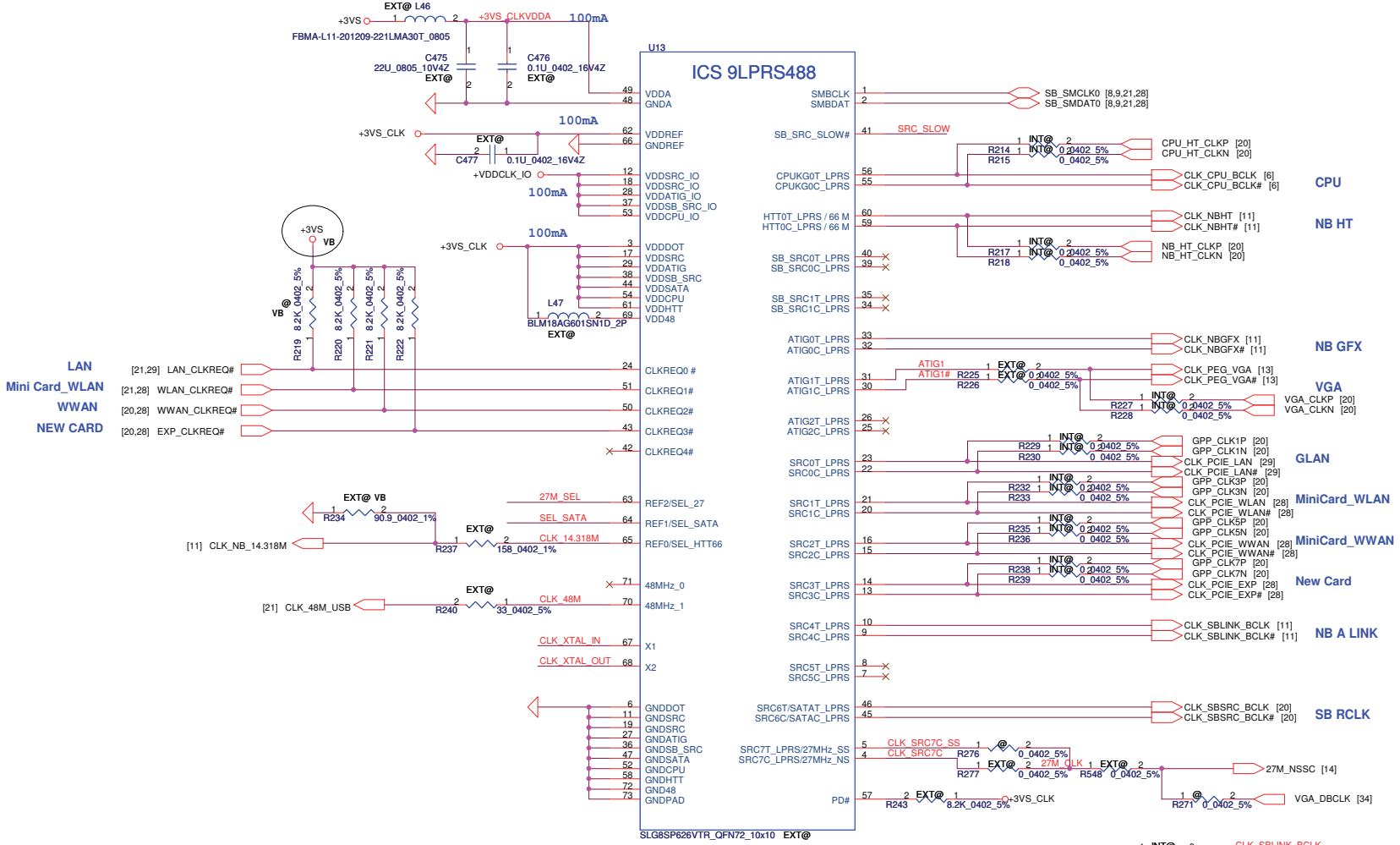
Title: PARK-S3 DDR3 VRAM

Size	Document Number	Rev
C	NAWE6 LA-5754P	0.2

Date: Monday, March 01, 2010 Sheet 18 of 47

Check Timing +1.1VS <50us +3VS for EXT CLKGEN satable





	CLK_NB_14.318M
RS780	1.1V 158R/90.0R

27M_SEL	1 *	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC_7 output
SEL_HTT66	1	single-ended 66MHz HTT output
	0 *	differential 100MHz HTT output
SEL_SATA	1	NON SPREAD 100M_SATA SRC6 output
	0 *	SPREAD 100M_SATA SRC6 output

* default

1st (SILEGO) : SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN

2nd (ICS) : SA000023H10 S IC ICS9LPRS488CKLFT MLF 72P CLK GEN

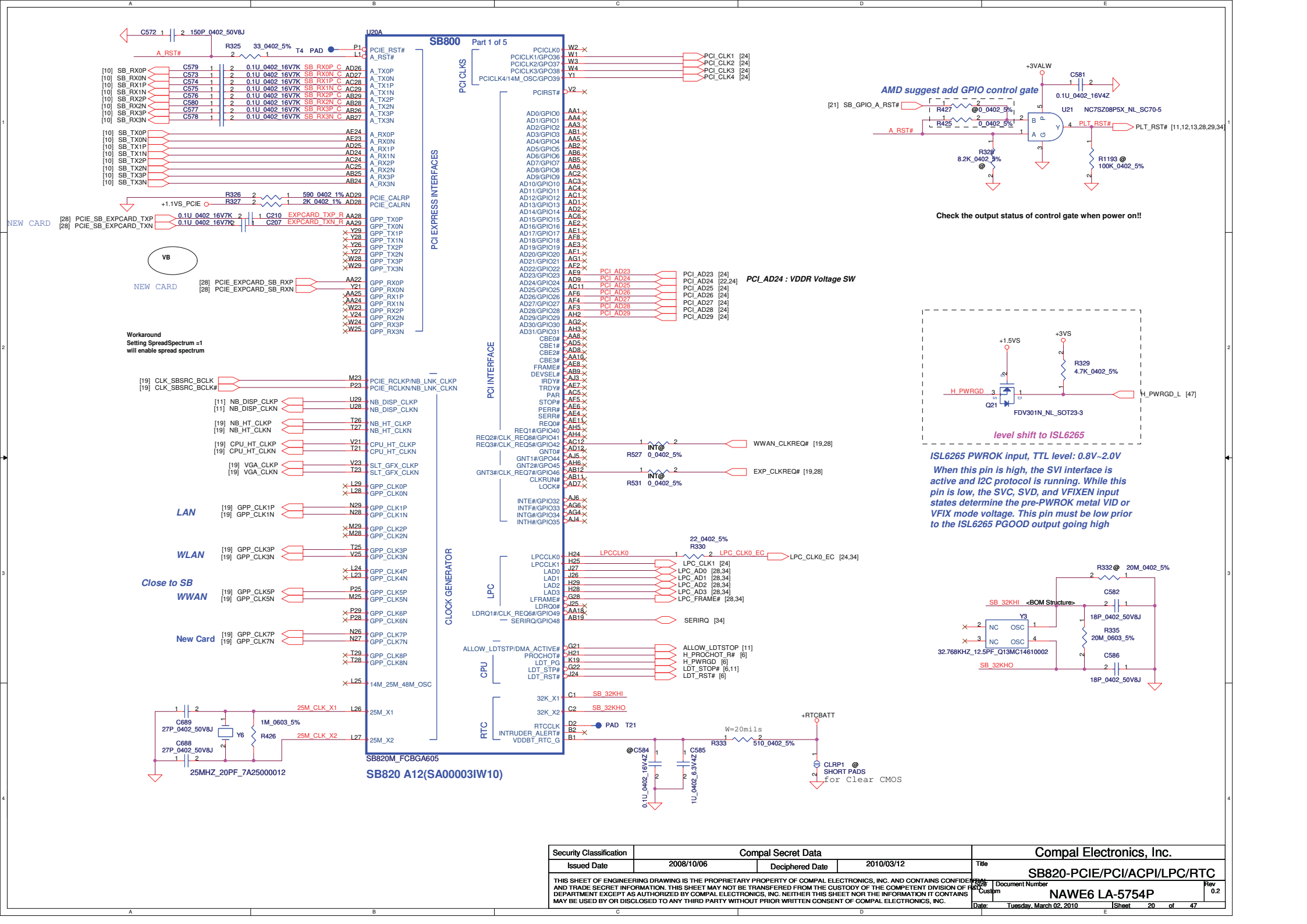
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

Title: Clock generator

Size: B2B Custom | Document Number: NAWE6 LA-5754P | Rev: 0.2

Date: Tuesday, March 02, 2010 | Sheet 19 of 47



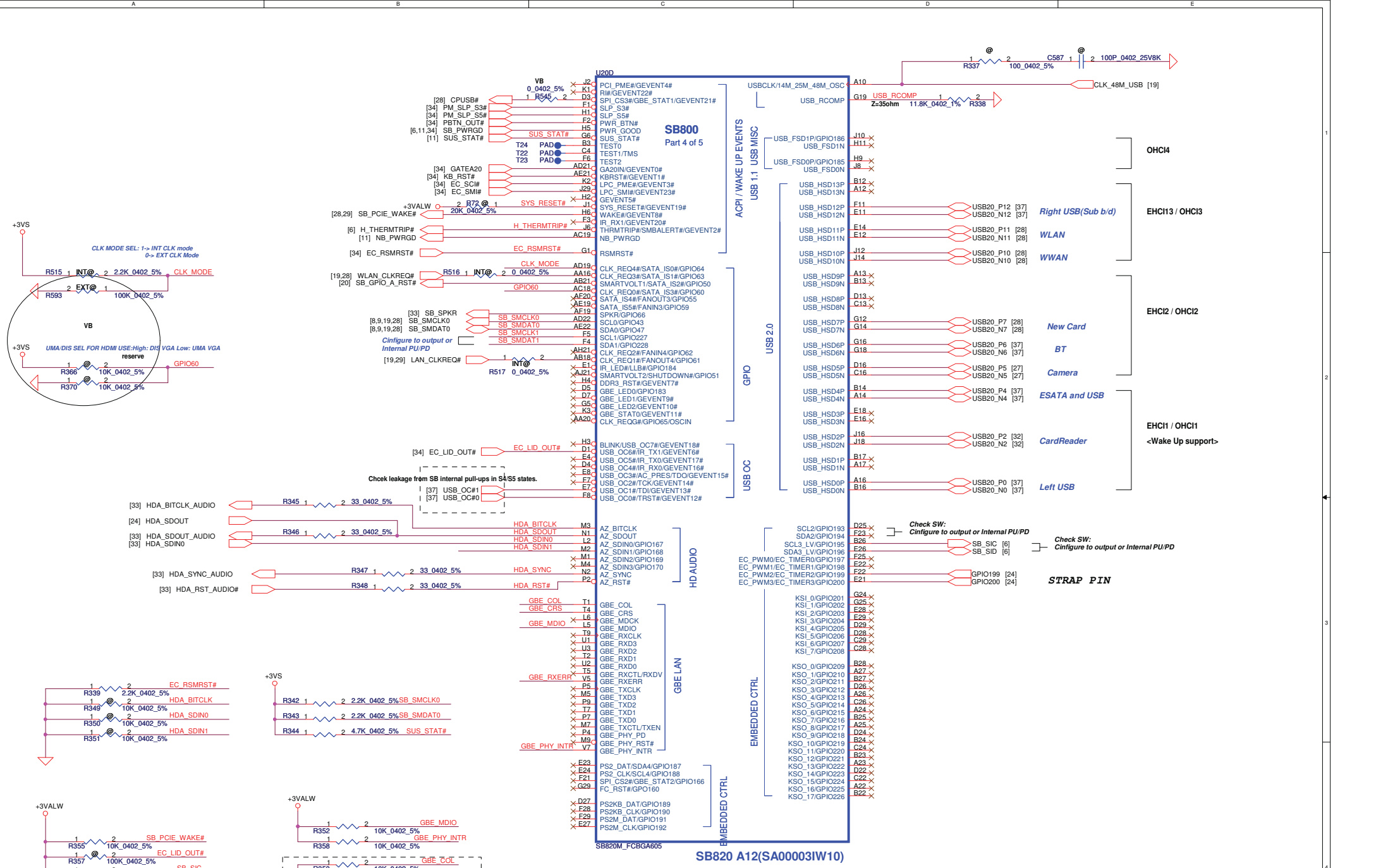
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

Title: SB820-PCIE/PCI/ACPI/LPC/RTC

Size	Document Number	Rev
B2B Custom	NAWE6 LA-5754P	0.2

Date: Tuesday, March 02, 2010 | Sheet 20 of 47



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

Title: SB820 USB/HD audio

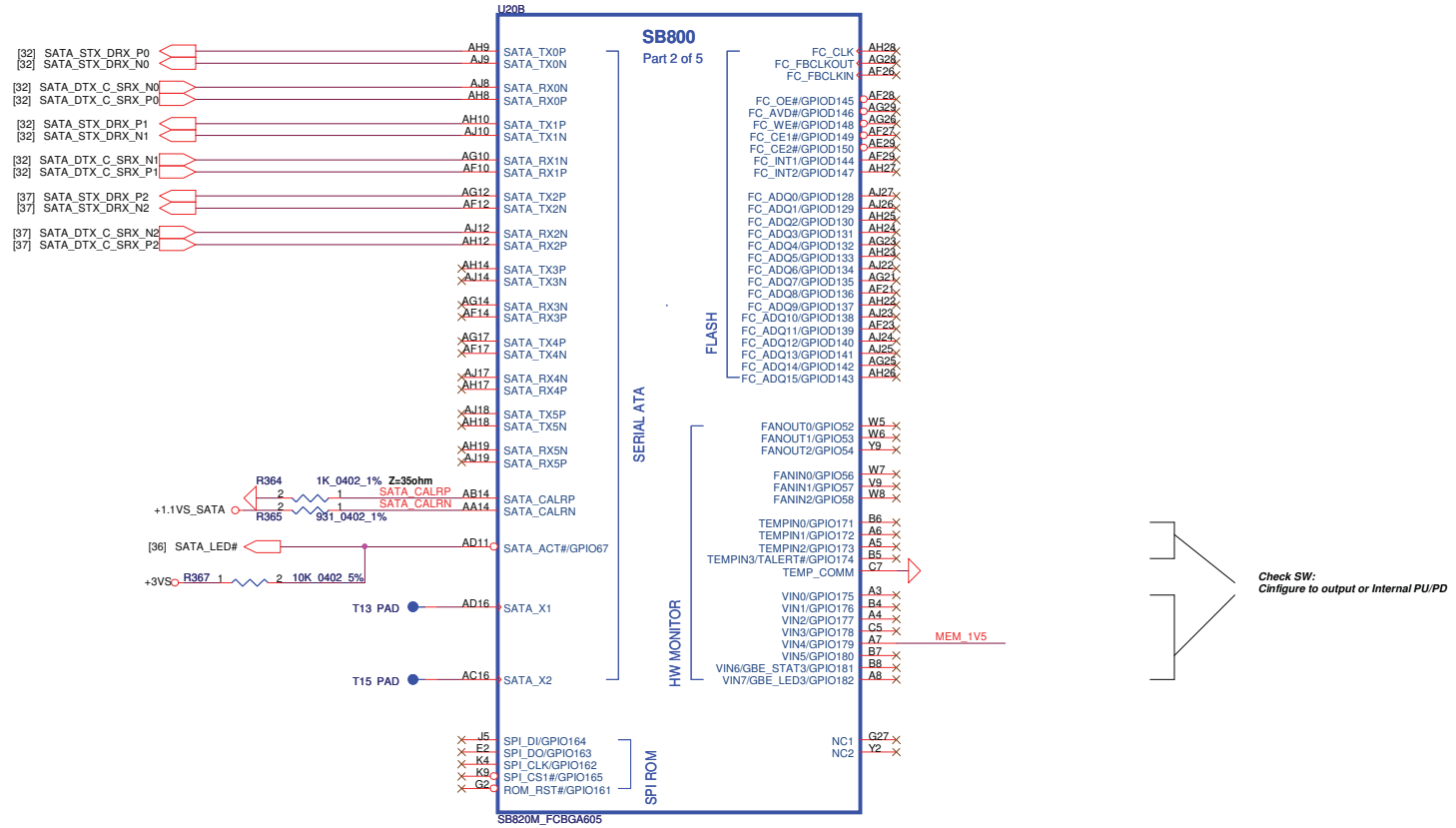
Size: Custom | Document Number: NAWE6 LA-5754P | Rev: 0.2

Date: Tuesday, March 02, 2010 | Sheet 21 of 47

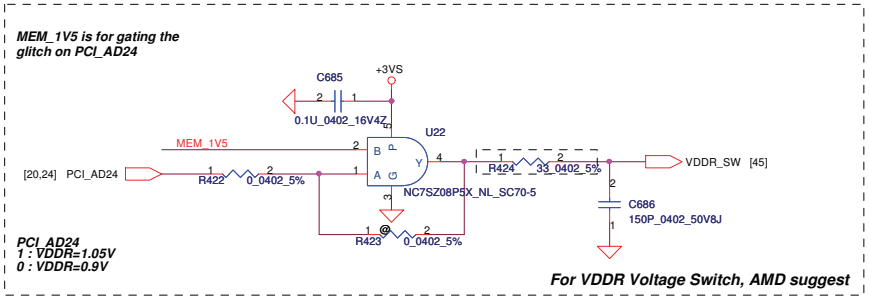
HDD

ODD

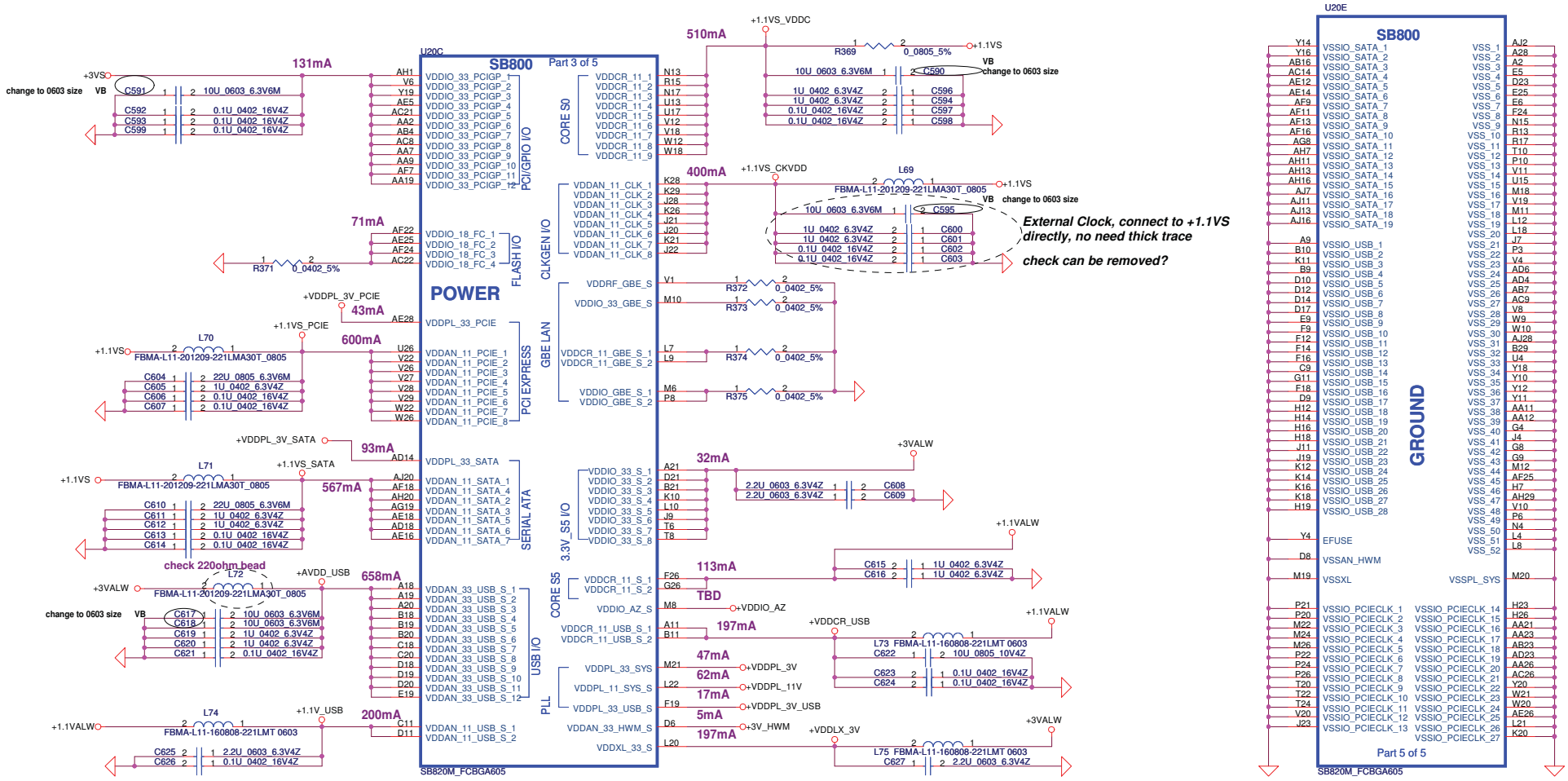
e-SATA



SB820 A12(SA00003IW10)



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date 2010/03/12	Title: SB820 SATA/IDE/SPI
Size: B2B Custom	Document Number: NAWE6 LA-5754P		Rev: 0.2
Date: Monday, March 01, 2010	Sheet 22 of 47		



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

Title: SB820 power/GND

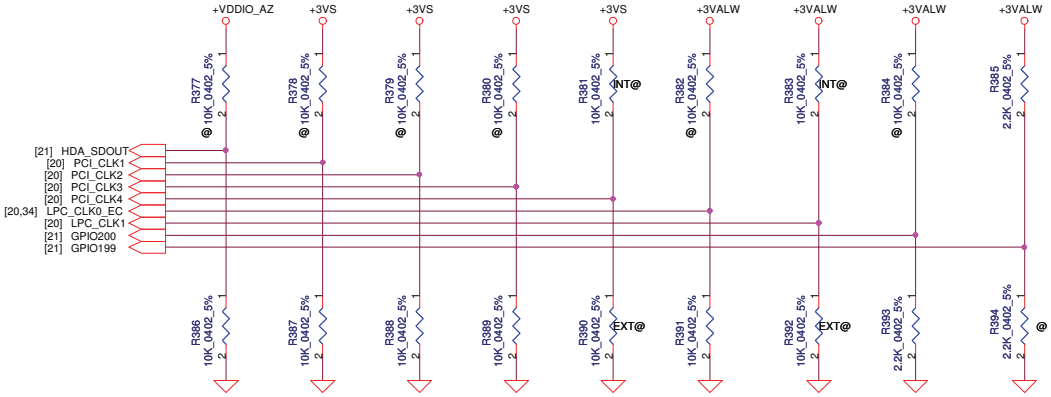
Size: Custom | Document Number: NAWE6 LA-5754P | Rev: 0.2

Date: Tuesday, March 02, 2010 | Sheet 23 of 47

REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LCP_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	CPU/HT CLK SEL Enable	EC ENABLE	CLOCKGEN ENABLE	H,H = Reserved H,L = SPI ROM **L,H = LPC ROM (Default L,NC)** L,L = FWH ROM
PULL LOW	Performance MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER DISABLE DEFAULT	IGNORE DEBUG STRAP DEFAULT	CPU/HT CLK SEL Disable DEFAULT	EC DISABLE DEFAULT	CLOCKGEN DISABLE DEFAULT	



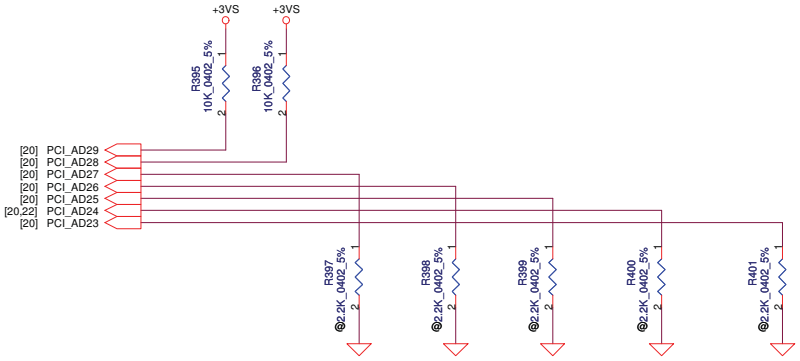
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH		USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW		BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

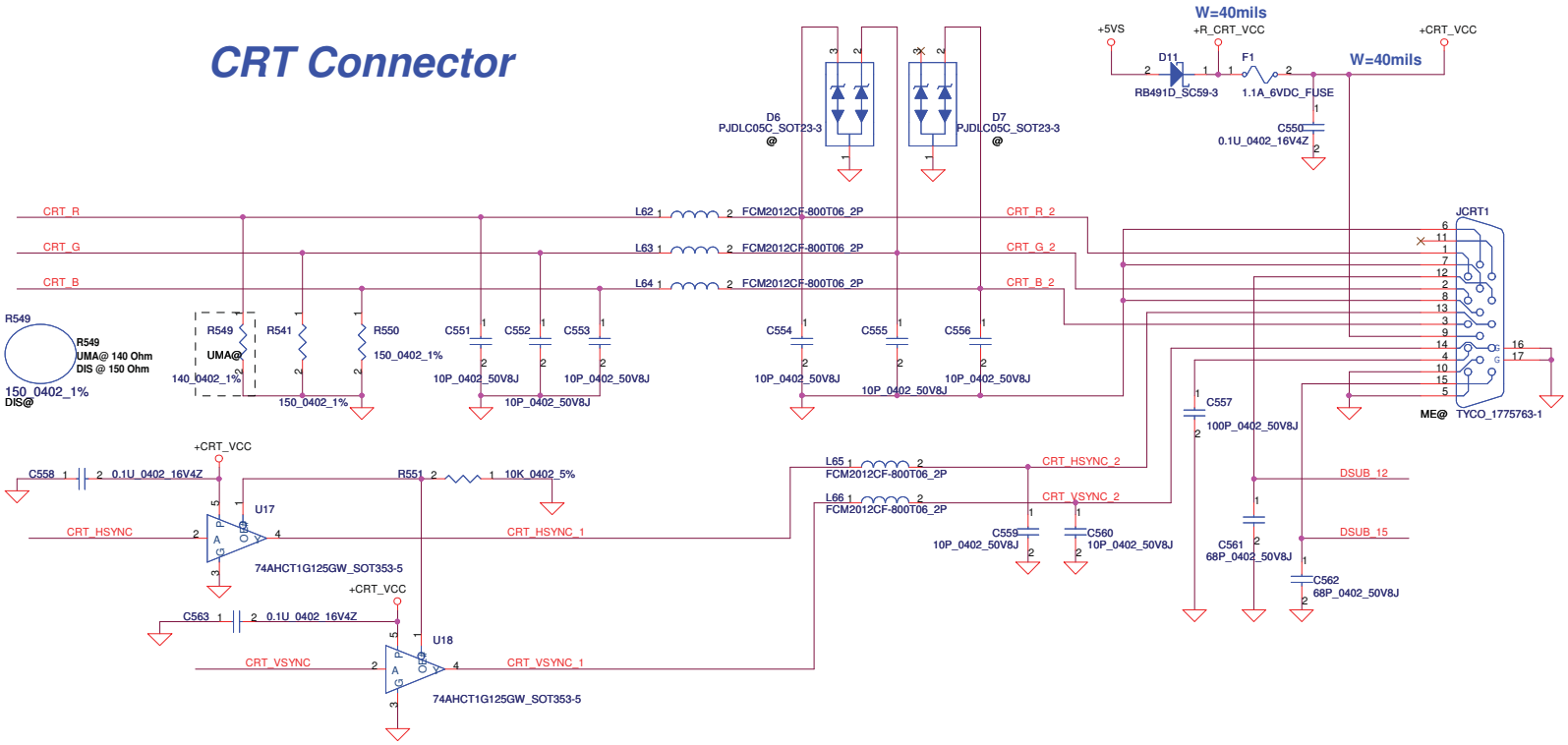
Check AD29,AD28 strap function

check default



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date 2010/03/12	Title SB820 STRAPS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size Custom / Document Number NAWE6 LA-5754P / Rev 0.2
			Date: Monday, March 01, 2010 / Sheet 24 of 47

CRT Connector



For UMA Only

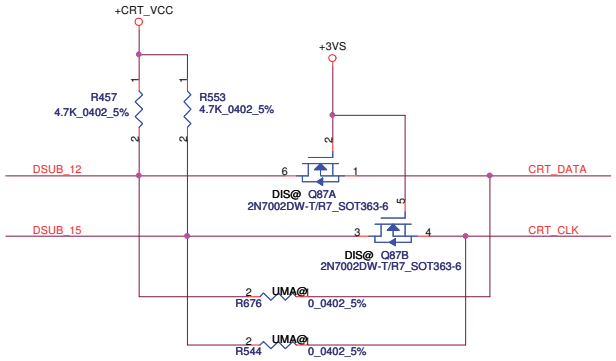
[11] GMCH_CRT_R	GMCH_CRT_R	R677	UMA@	0_0402_5%	CRT_R
[11] GMCH_CRT_G	GMCH_CRT_G	R542	UMA@	0_0402_5%	CRT_G
[11] GMCH_CRT_B	GMCH_CRT_B	R679	UMA@	0_0402_5%	CRT_B
[11,12] GMCH_CRT_HSYNC	GMCH_CRT_HSYNC	R547	UMA@	0_0402_5%	CRT_HSYNC
[11,12] GMCH_CRT_VSYNC	GMCH_CRT_VSYNC	R543	UMA@	0_0402_5%	CRT_VSYNC
[11] GMCH_CRT_DATA	GMCH_CRT_DATA	R546	UMA@	0_0402_5%	CRT_DATA
[11] GMCH_CRT_CLK	GMCH_CRT_CLK	R678	UMA@	0_0402_5%	CRT_CLK

For VGA Only

[14] VGA_CRT_R	VGA_CRT_R	R539	DIS@	0_0402_5%	CRT_R
[14] VGA_CRT_G	VGA_CRT_G	R552	DIS@	0_0402_5%	CRT_G
[14] VGA_CRT_B	VGA_CRT_B	R554	DIS@	0_0402_5%	CRT_B
[14] VGA_CRT_HSYNC	VGA_CRT_HSYNC	R535	DIS@	0_0402_5%	CRT_HSYNC
[14] VGA_CRT_VSYNC	VGA_CRT_VSYNC	R557	DIS@	0_0402_5%	CRT_VSYNC
[14] VGA_CRT_DATA	VGA_CRT_DATA	R538	DIS@	0_0402_5%	CRT_DATA
[14] VGA_CRT_CLK	VGA_CRT_CLK	R556	DIS@	0_0402_5%	CRT_CLK

NOTE:
IF RS880M ONLY(NO MXM SUPPORT),
DAC_SDAT AND DAC_SCL DON'T
NEED LEVEL SHIFT, PU TO +5V DIRECTLY.
DAC_SDAT AND DAC_SCL ARE 5V TOLERANCE.

Close to Conn side



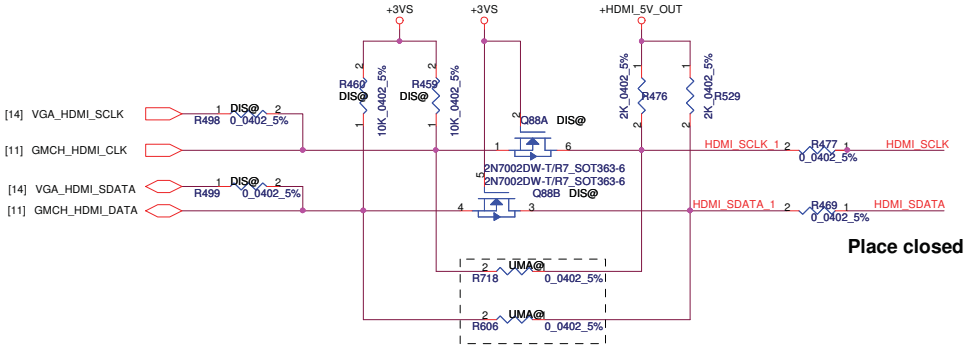
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

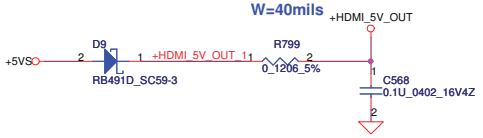
Title: CRT Connector

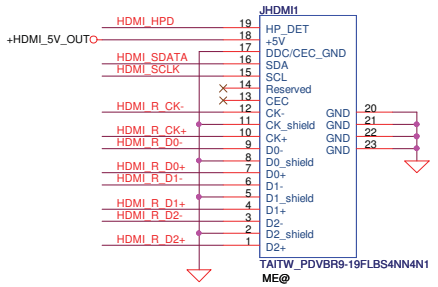
Size: B | Document Number: NAWE6 LA-5754P | Rev: 0.2

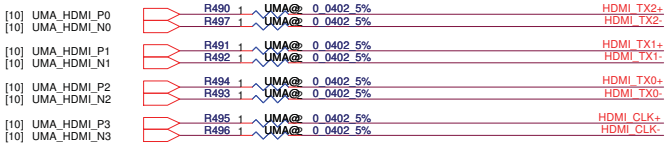
Date: Monday, March 01, 2010 | Sheet 25 of 47

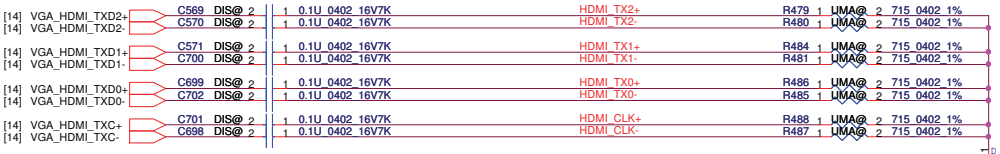


Place closed to JHDMI1

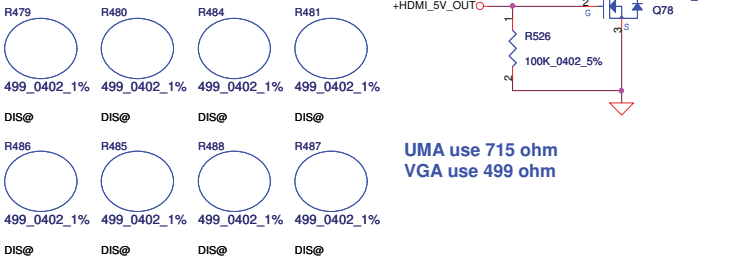




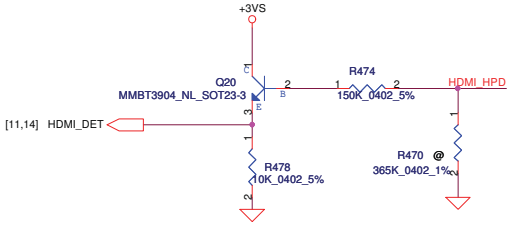


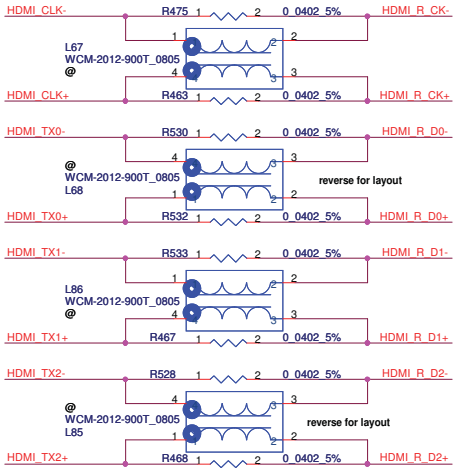


Place closed to JHDMI1



UMA use 715 ohm
VGA use 499 ohm





Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

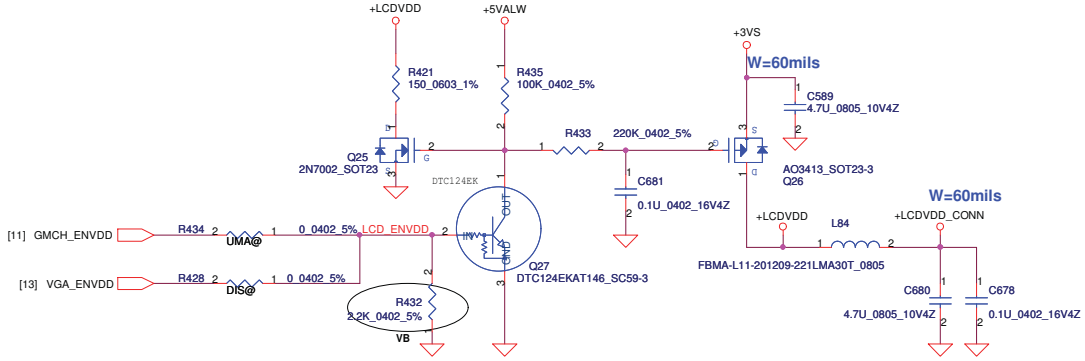
Compal Electronics, Inc.

Title: HDMI Connector

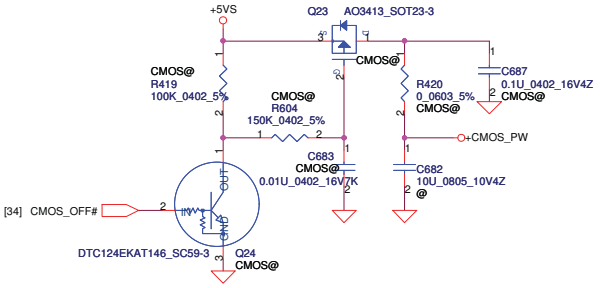
Size: Custom | Document Number: NAWE6 LA-5754P | Rev: 0.2

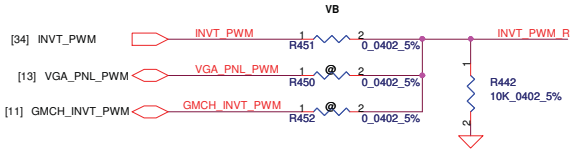
Date: Monday, March 01, 2010 | Sheet 26 of 47

LCD POWER CIRCUIT

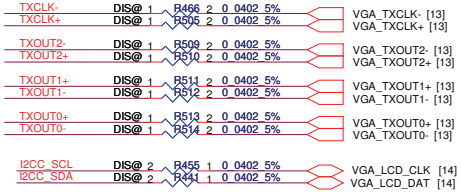


CMOS Camera

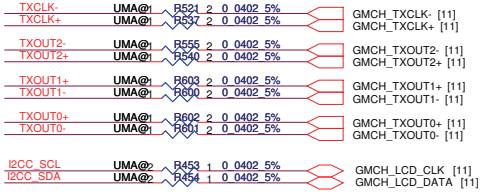


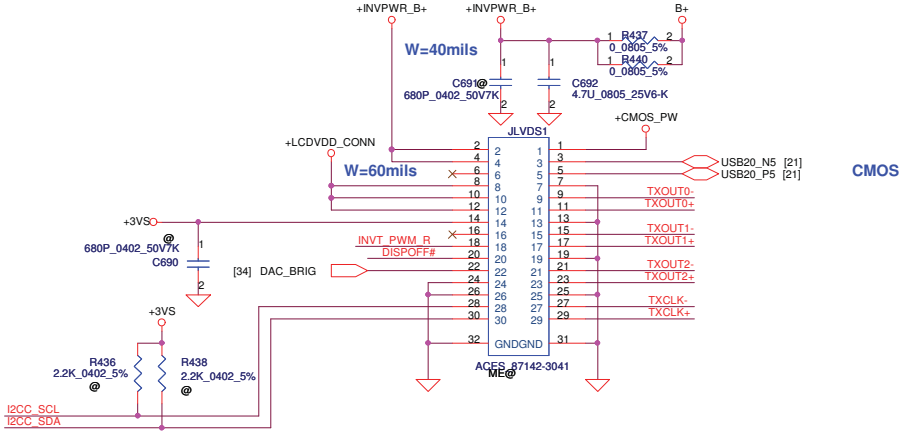


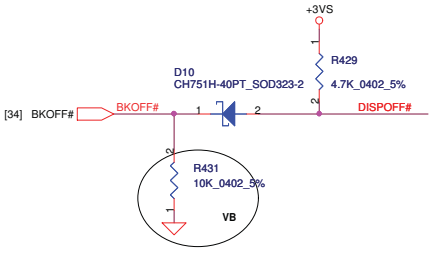
VGA ONLY

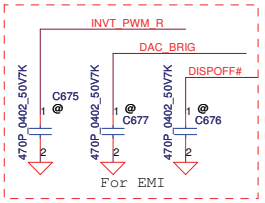


UMA ONLY





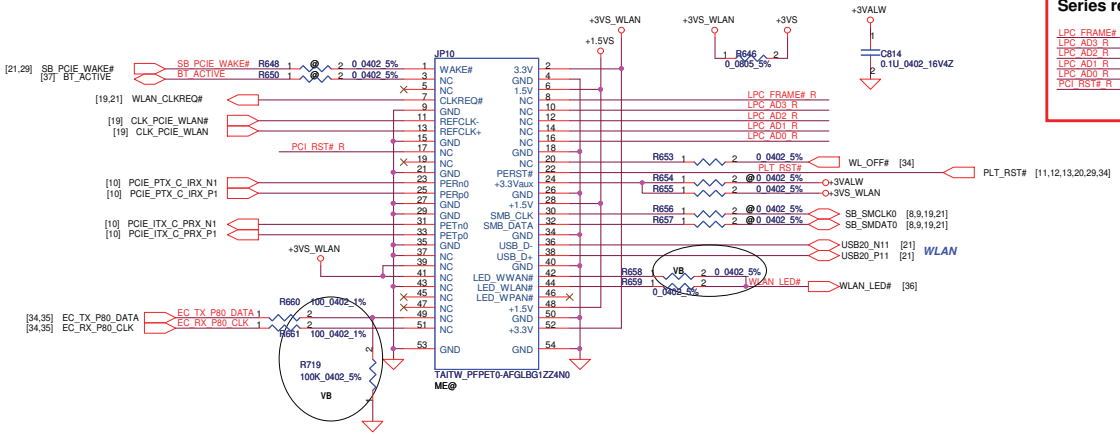




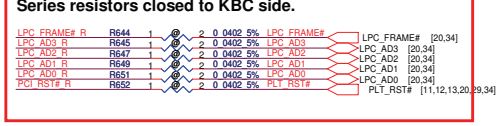
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: LVDS/CAMERA			
Size: Custom	Document Number: NAWE6 LA-5754P		Rev: 0.2
Date: Tuesday, March 02, 2010	Sheet 27 of 47		

Mini-Express Card for WLAN/WiMAX(Half)

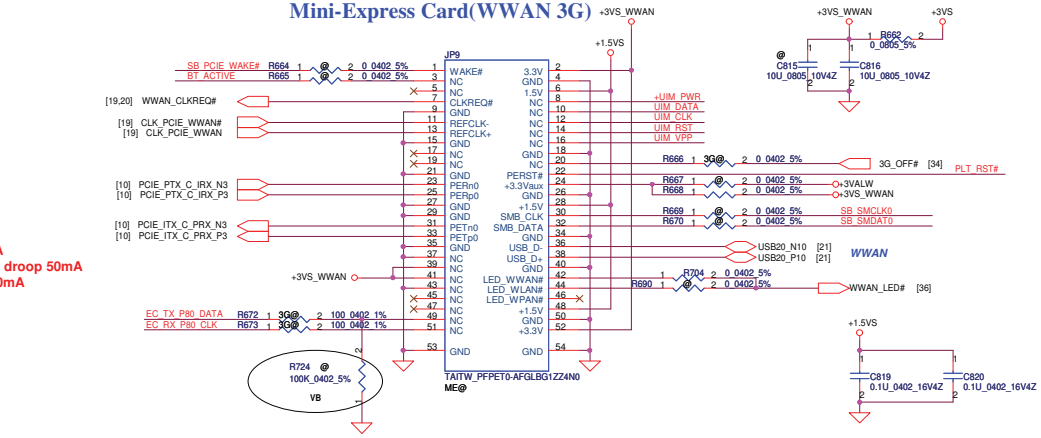


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

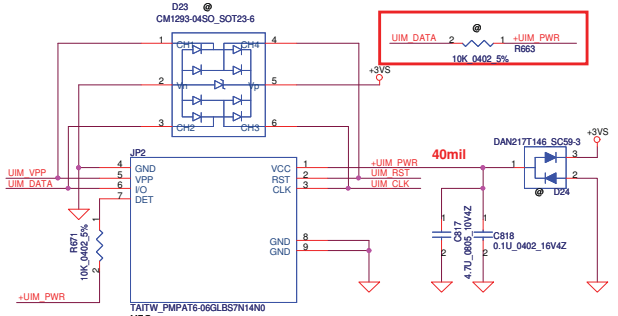


Mini-Express Card for WWAN(Full)

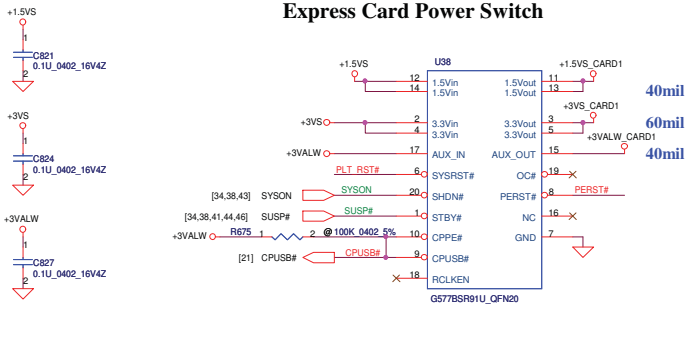
Mini-Express Card(WWAN 3G)



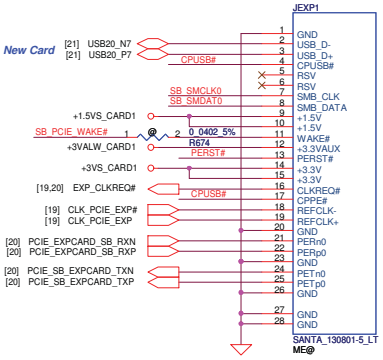
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA



Express Card Power Switch

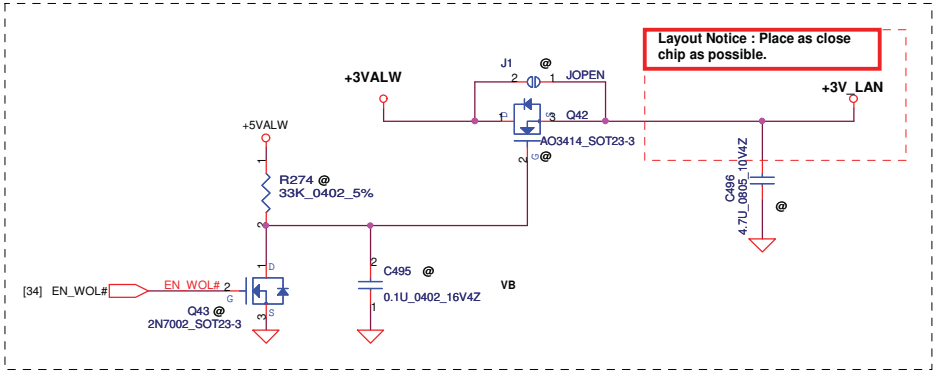


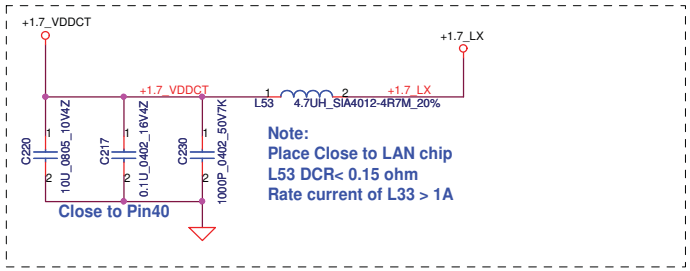
New Card 34mm Socket (Left/TOP)



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

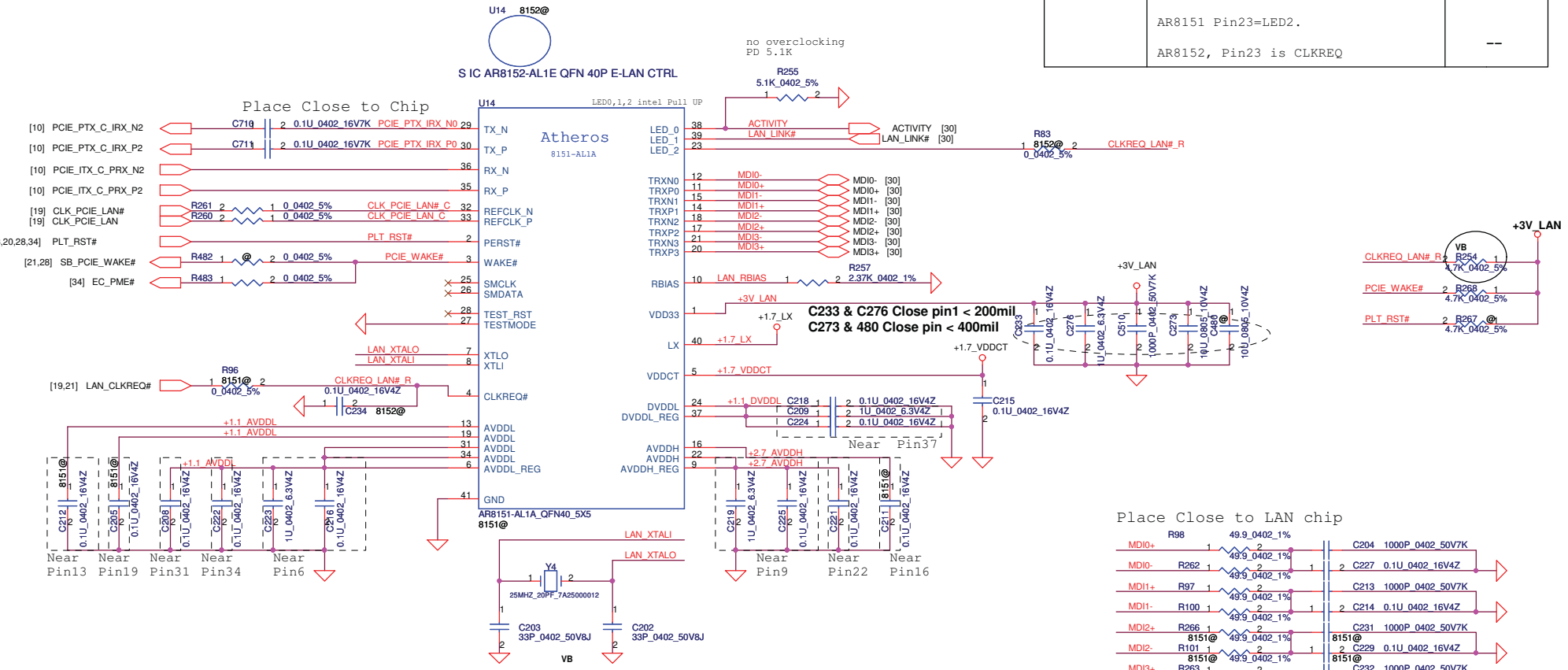
Compal Electronics, Inc.			
Title	Mini-Card/Nwe Card/SIM		
Size	Document Number	NAWE6 LA-5754P	Rev 0.2
Date: Tuesday, March 02, 2010	Sheet 28 of 47		





Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable ★	H
	H:SWR Switch mode regulator Select ★ AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--



8152 no mount MDI3+,MDI3-,MDI2-,MDI2+ resister and cap

For AR8152, pin23 is the LDO output. Mount C234 and no mount R96.close to this pin4

For AR8151, pin4 is the CLKREQn pin, mount R96 and no mount C234.close to this pin4

Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

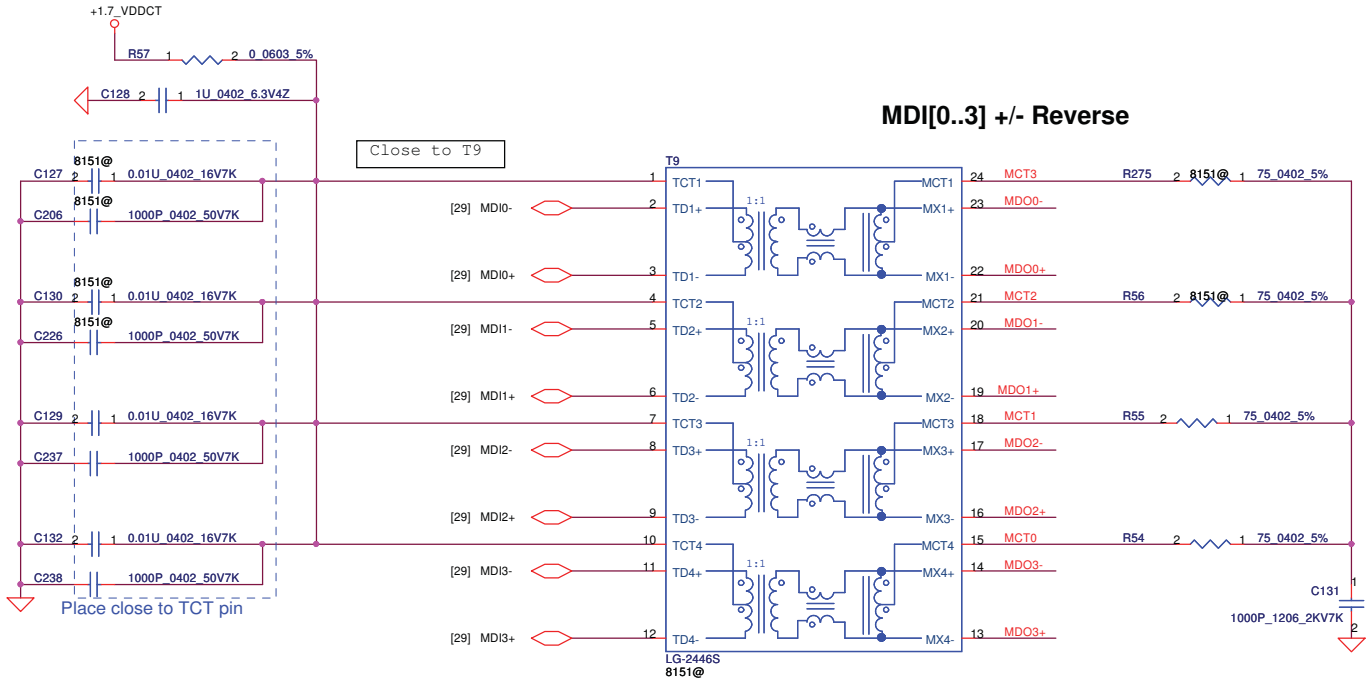
Compal Electronics, Inc.

Title: LAN-AR8151/8152

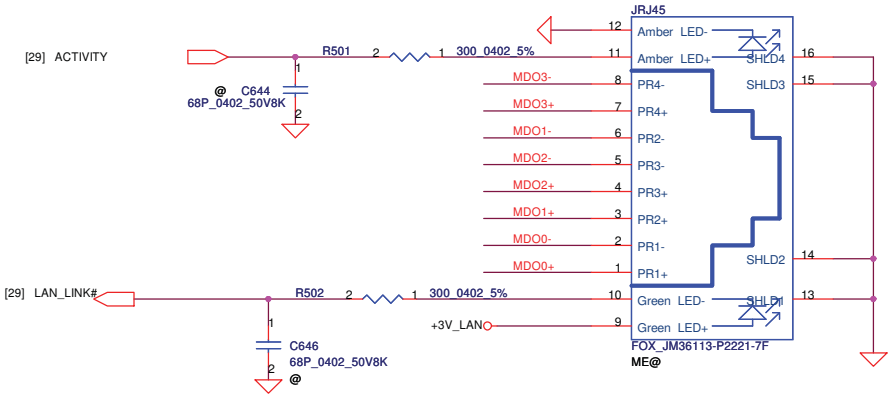
Size: Custom | Document Number: NAWE6 LA-5754P | Rev: 0.2

Date: Tuesday, March 02, 2010 | Sheet 29 of 47

MDI[0..3] +/- Reverse



RJ45 Conn.



Security Classification	Compal Secret Data		
Issued Date	2009/03/20	Deciphered Date	2010/03/20

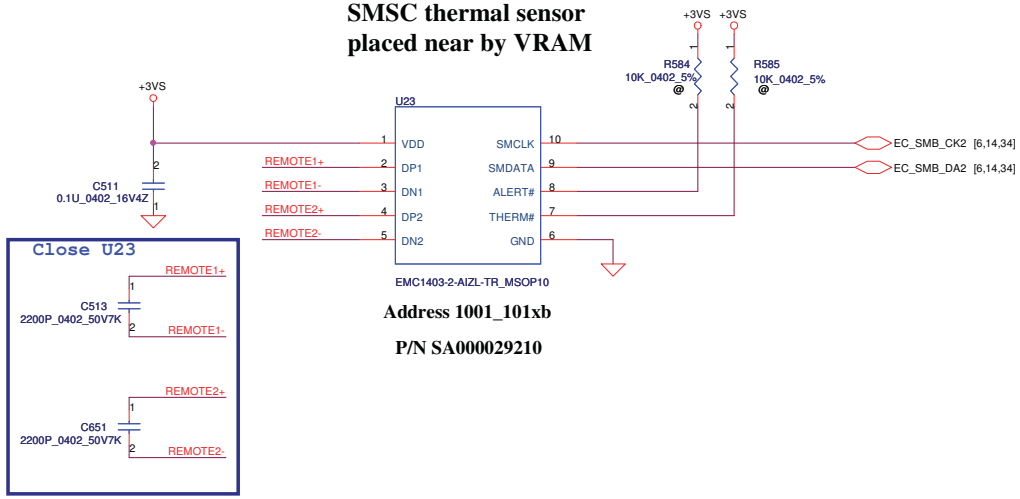
Compal Electronics, Inc.

Title: **LAN_Transformer**

Size	Document Number	Rev
Custom	NAWE6 LA-5754P	0.2

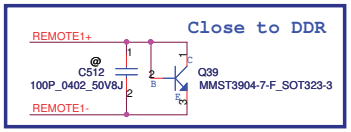
Date: Monday, March 01, 2010 Sheet 30 of 47

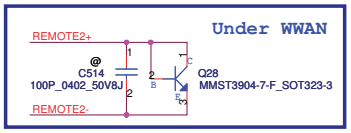
SMSC thermal sensor placed near by VRAM



Address 1001_101xb

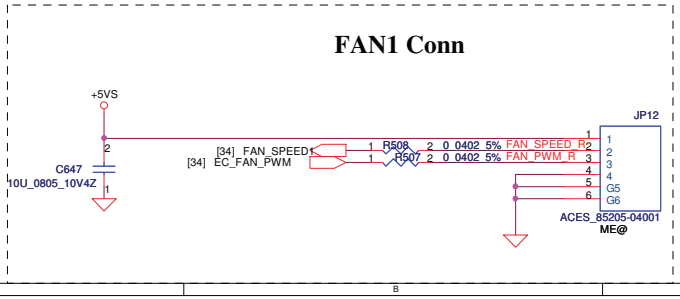
P/N SA000029210





REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

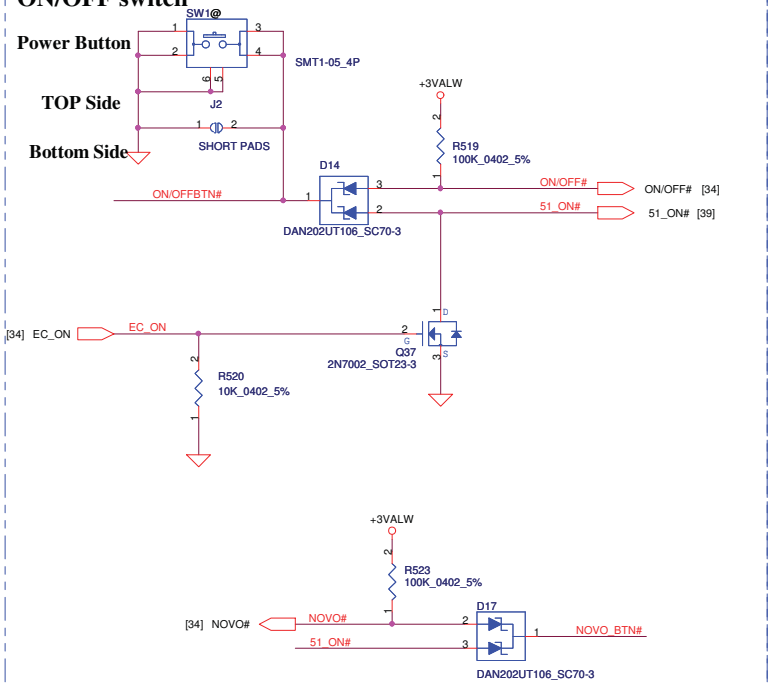
Compal Electronics, Inc.

Title: EMC1403_sensor/FAN

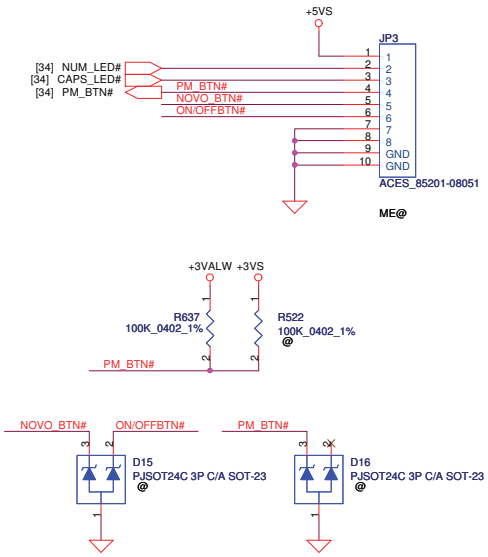
Size: B | Document Number: NAWE6 LA-5754P | Rev: 0.2

Date: Monday, March 01, 2010 | Sheet 31 of 47

ON/OFF switch

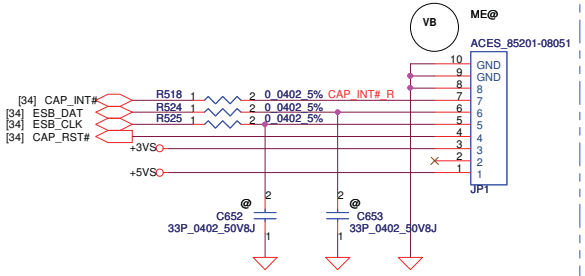


Power Bottom Board Conn. 8pin

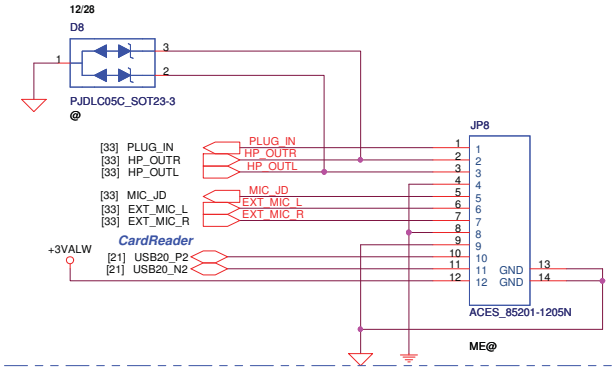


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

Cap Sensor Board Conn. 8pin

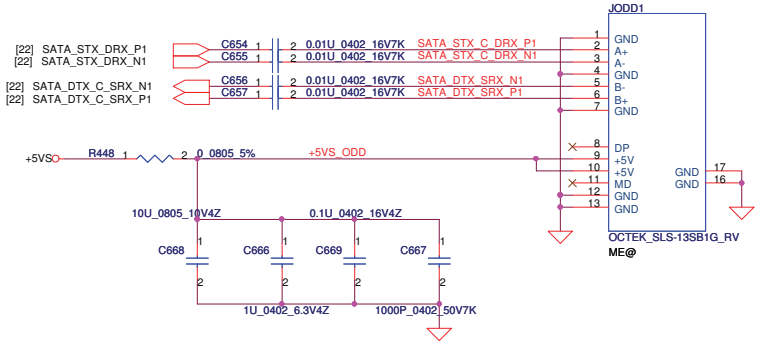


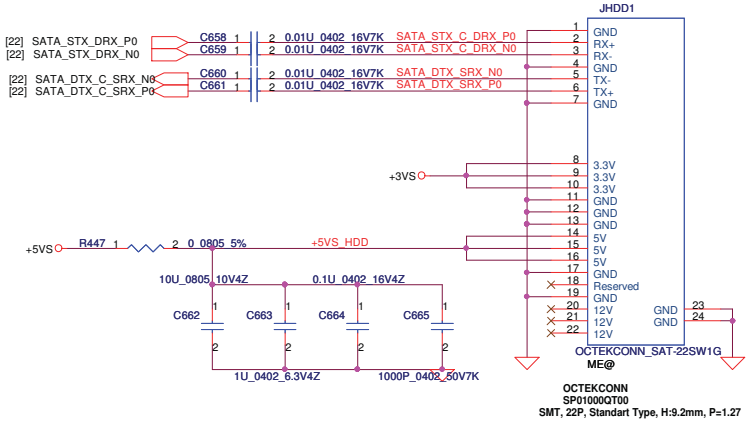
Card Reader/Audio Jack SB CONN



SATA HDD Conn.

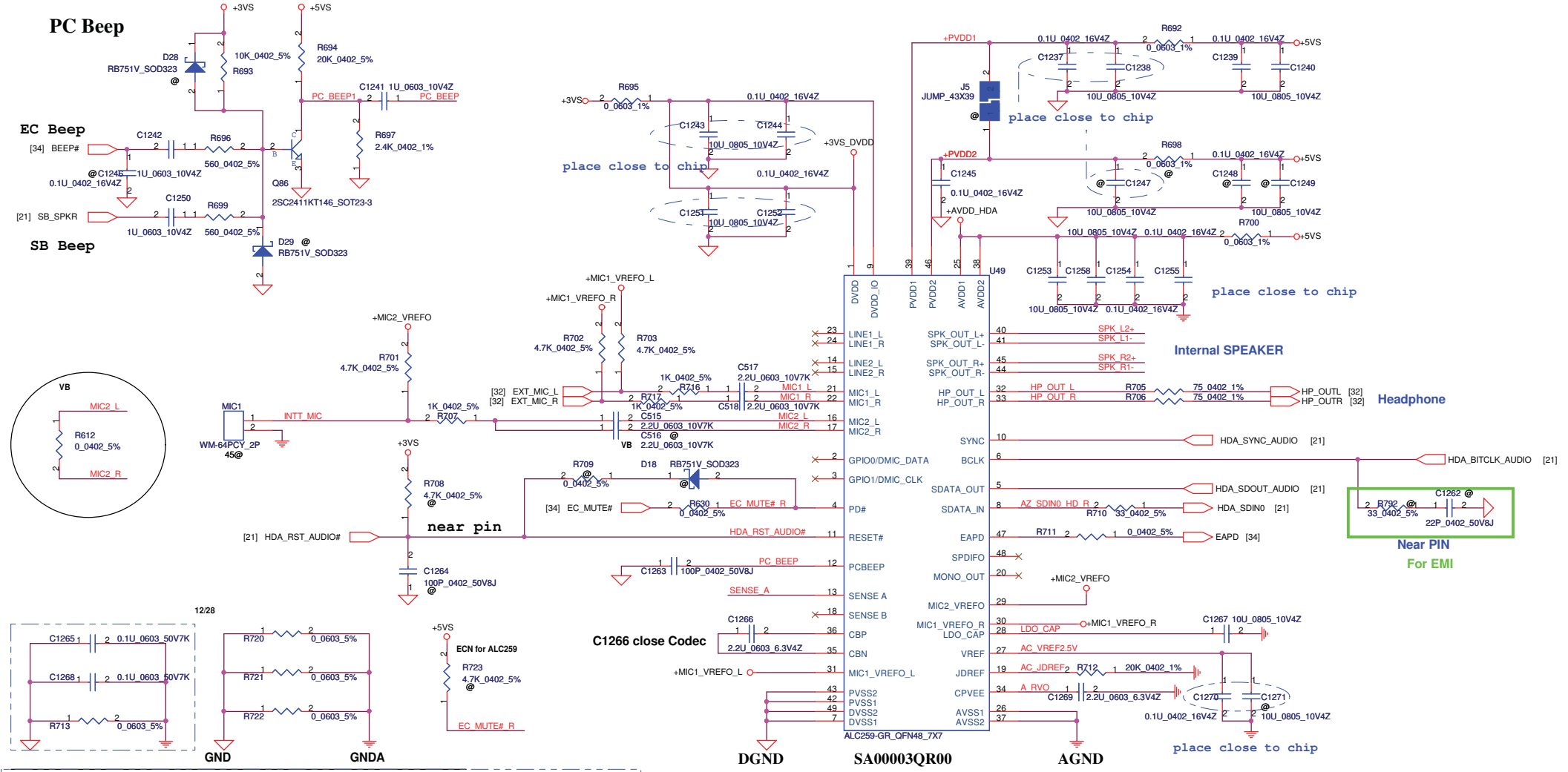
SATA ODD Conn.





Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: HDD/ODD Connector			
Size: Custom	Document Number: NAWE6 LA-5754P		Rev: 0.2
Date: Tuesday, March 02, 2010	Sheet 32 of 47		



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	

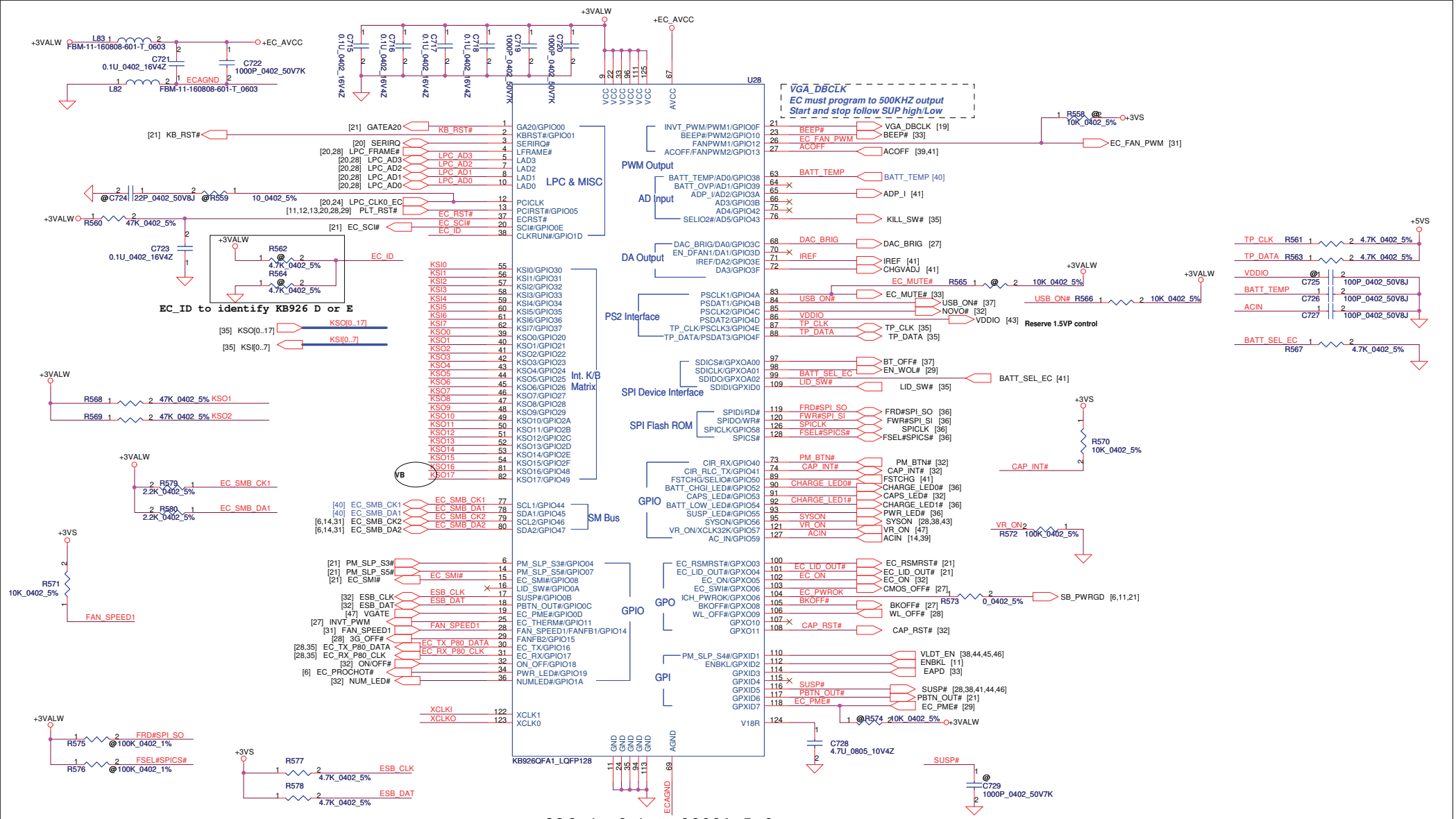
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: ALC259 Codec

Size: Custom | Document Number: NAWE6 LA-5754P | Rev: 0.2

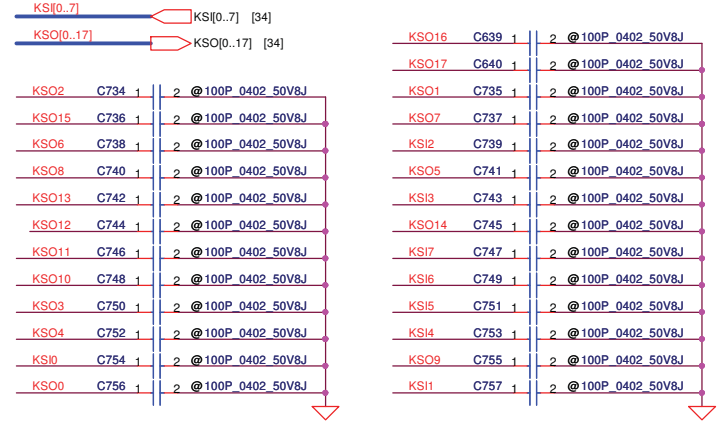
Date: Tuesday, March 02, 2010 | Sheet 33 of 47



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

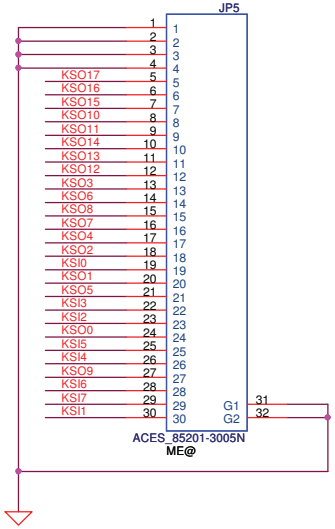
Compal Electronics, Inc.			
Title: BIOS & EC I/O Port			
Size: C (Custom)	Document Number: NAWE6 LA-5754P		Rev: 0.2
Date: Tuesday, March 02, 2010	Sheet: 34 of 47		

INT_KBD Conn.

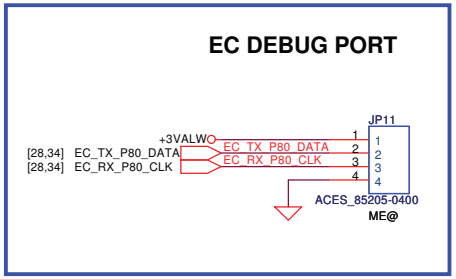


CONN PIN define need double check

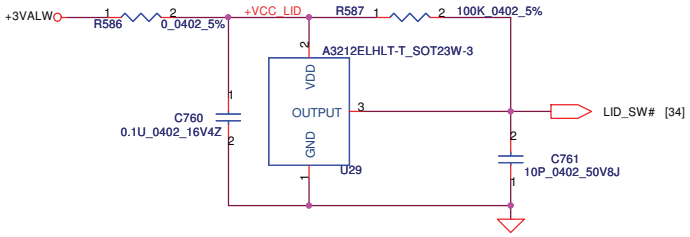
reversal of NIWE1



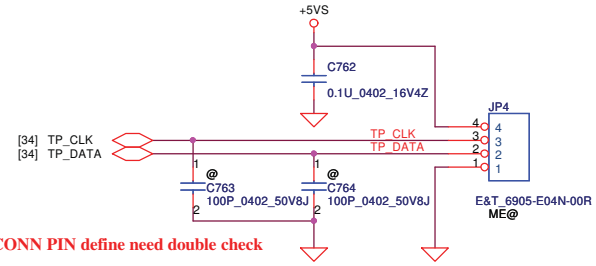
EC DEBUG PORT



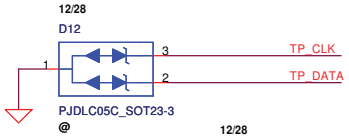
Lid Switch



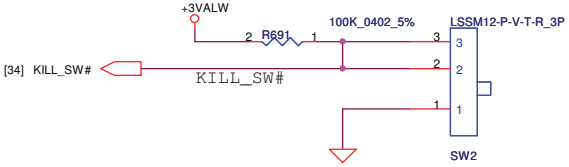
To TP/B Conn.



CONN PIN define need double check



Kill Switch



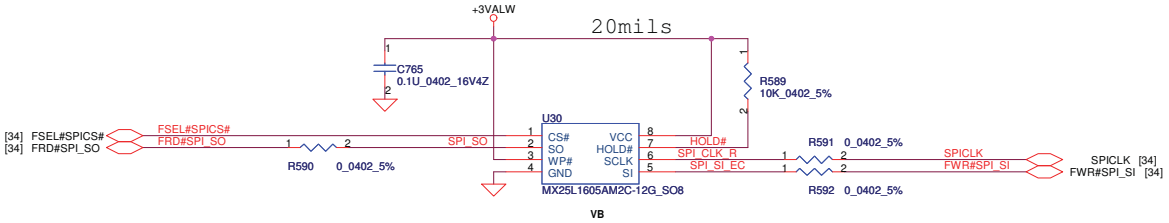
Kill

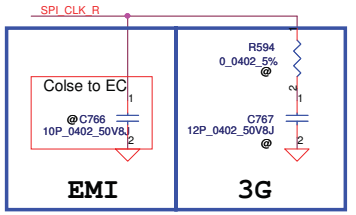
STATUS	
1,2(LOW)	OFF
2,3(HI)	ON

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

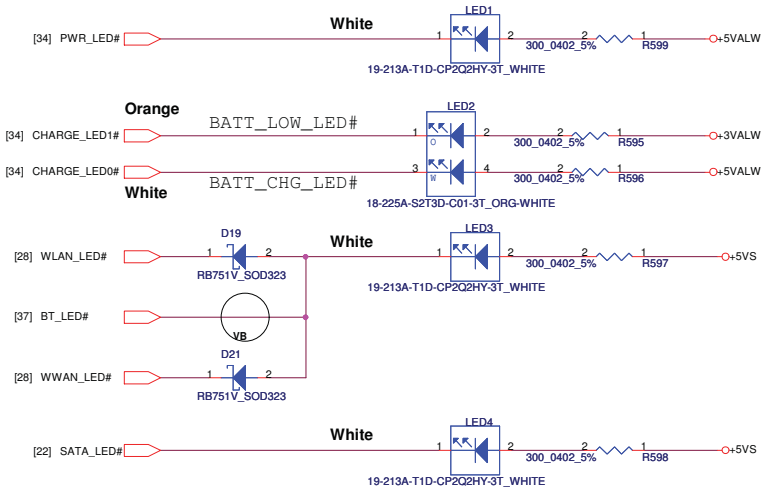
Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: B	Document Number: NAWE6 LA-5754P		Rev: 0.2
Date: Monday, March 01, 2010		Sheet 35 of 47	

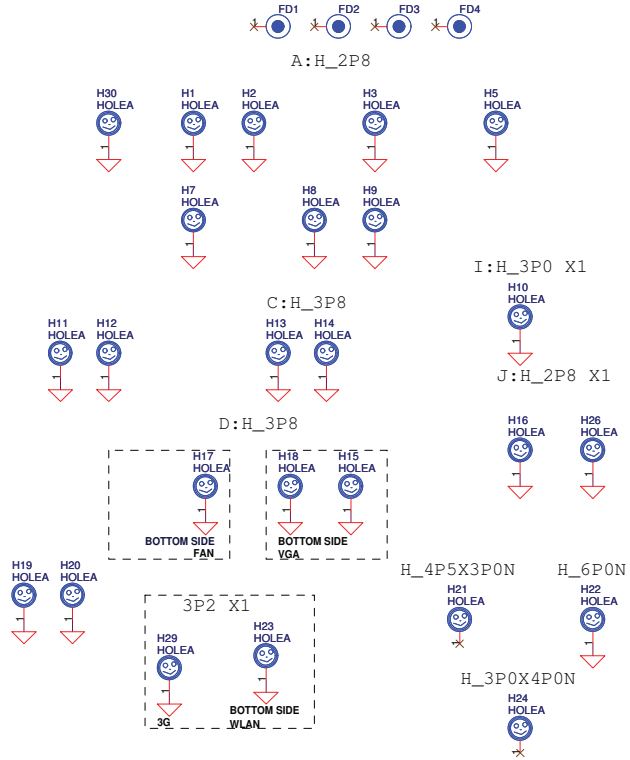
SA00002TO00 pakage 200mil
S IC FL 16MBIT MX25L1605AM2C-12G SO8 ROM

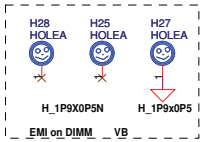




LED







Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

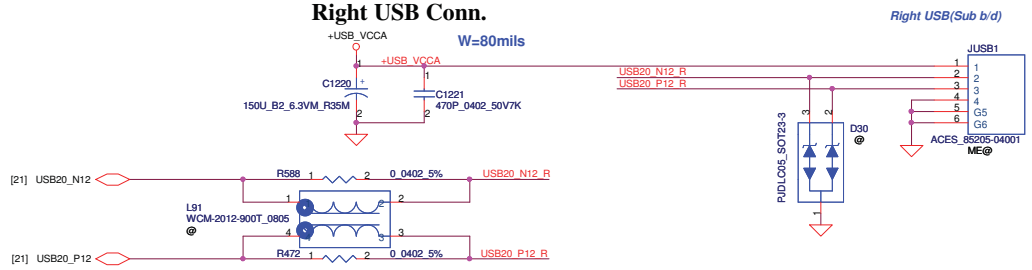
Compal Electronics, Inc.

Title: LED/EC SPI ROM

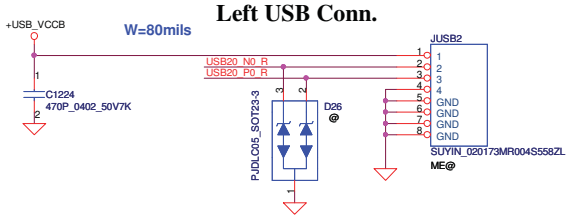
Size: B | Document Number: NAWE6 LA-5754P | Rev: 0.2

Date: Tuesday, March 02, 2010 | Sheet 36 of 47

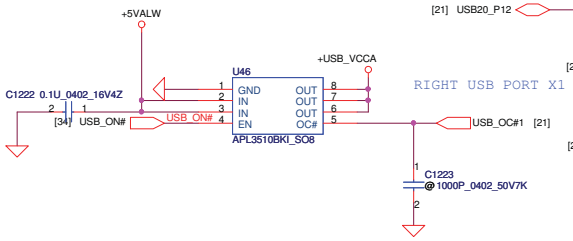
Right USB Conn.



Left USB Conn.

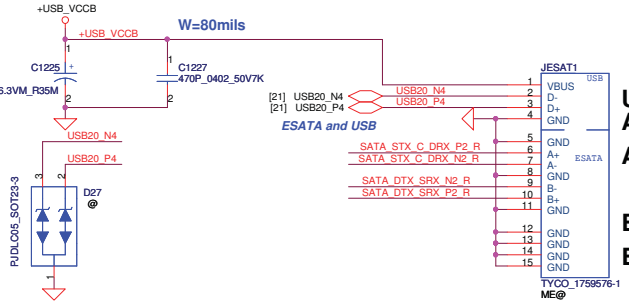


RIGHT USB PORT X1

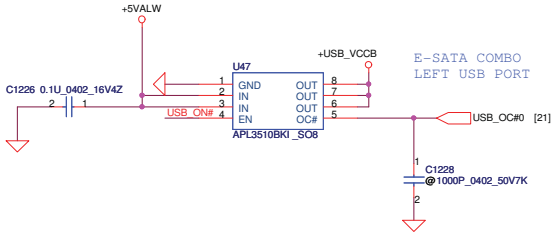


USB power switch need update symbol
to SA000039E00(Low enable)

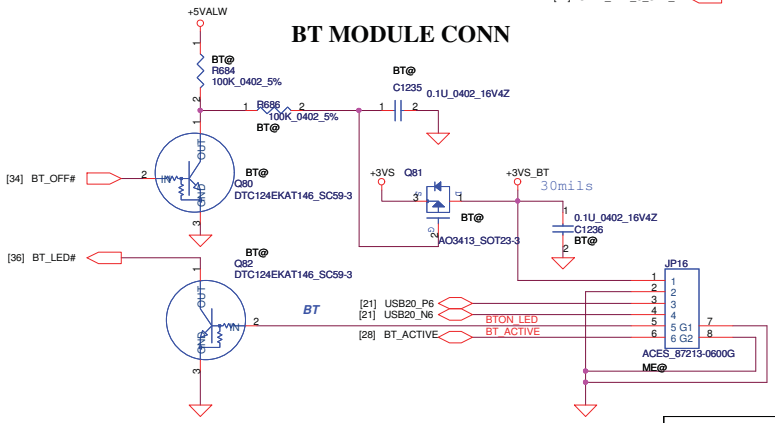
ESATA and USB Conn.

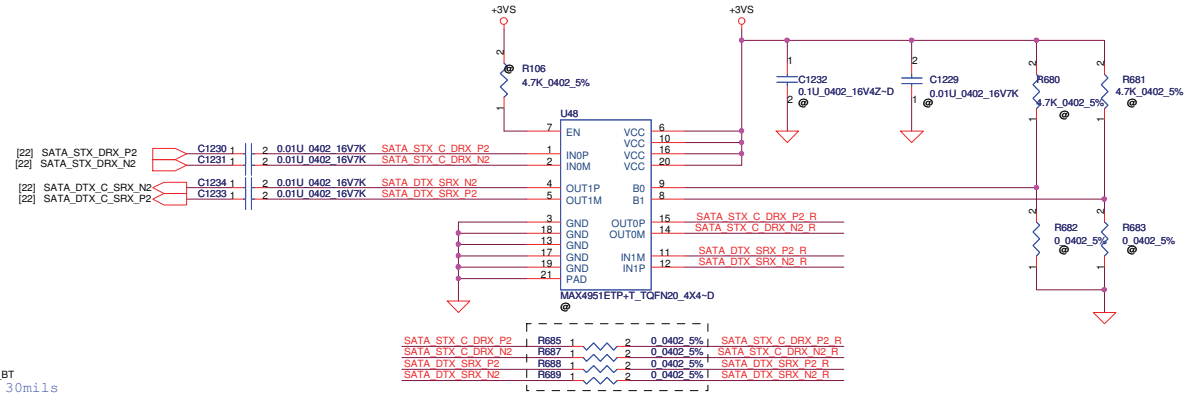


E-SATA COMBO LEFT USB PORT



BT MODULE CONN





Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

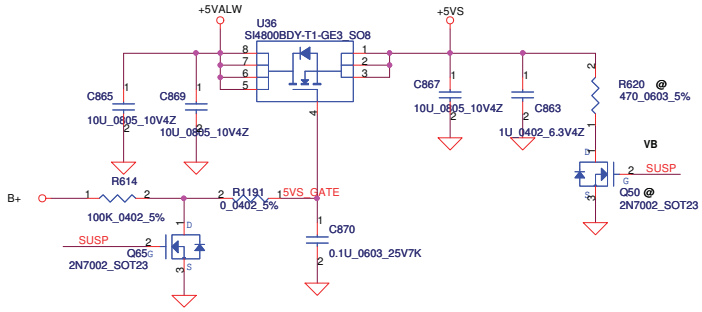
Compal Electronics, Inc.

Title: USB ports/BT/E-SATA

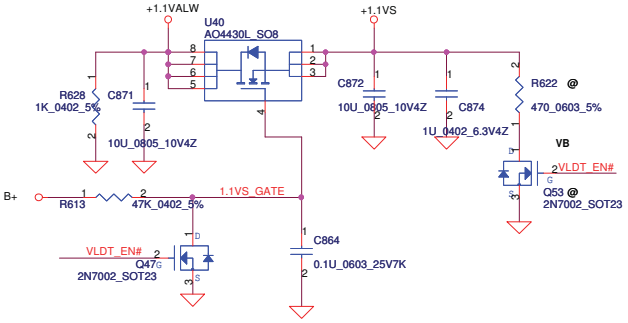
Size	Document Number	Rev
Custom	NAWE6 LA-5754P	0.2

Date: Monday, March 01, 2010 | Sheet 37 of 47

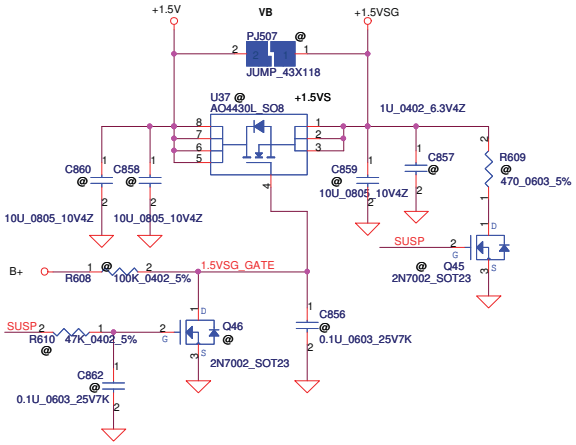
+5VALW TO +5VS



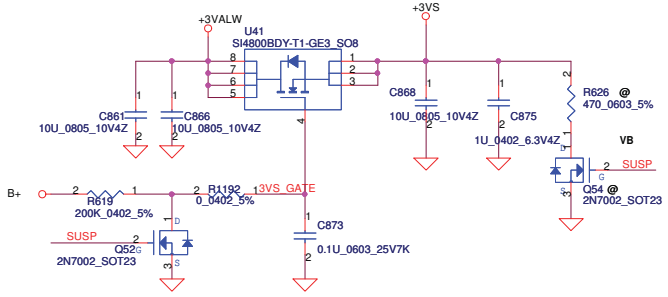
+1.1VALW TO +1.1VS (NB HT)

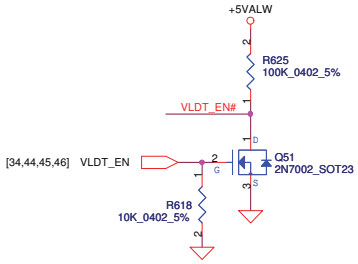


+1.5V to +1.5VSG

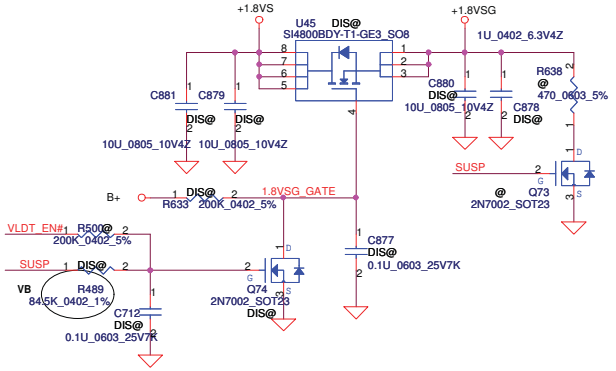


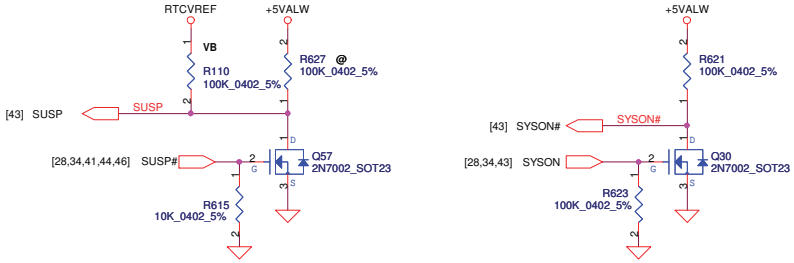
+3VALW TO +3VS



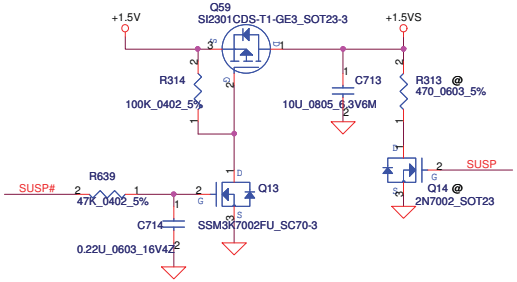


+1.8VS to +1.8VSG

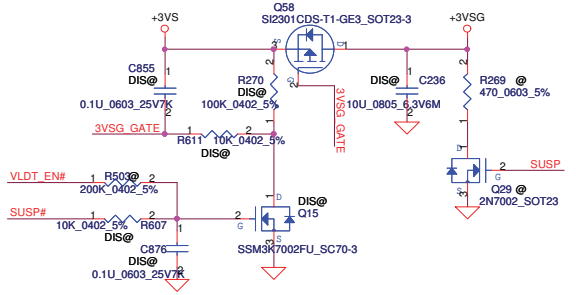


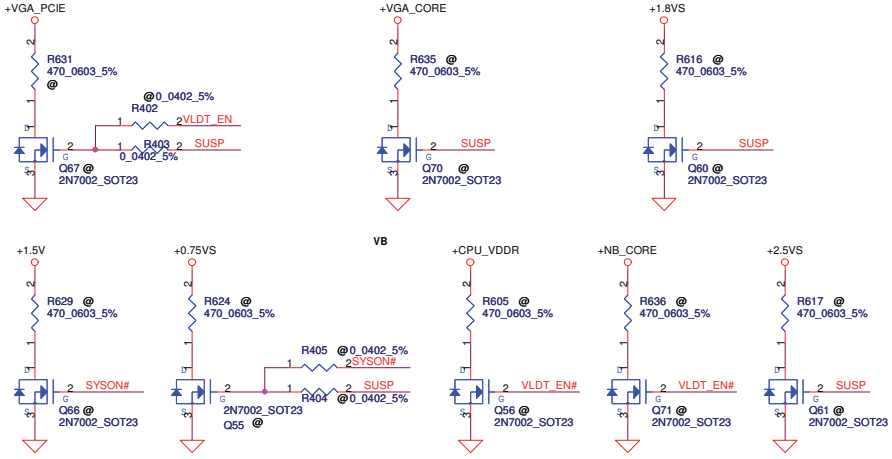


+1.5VS



+3VSG





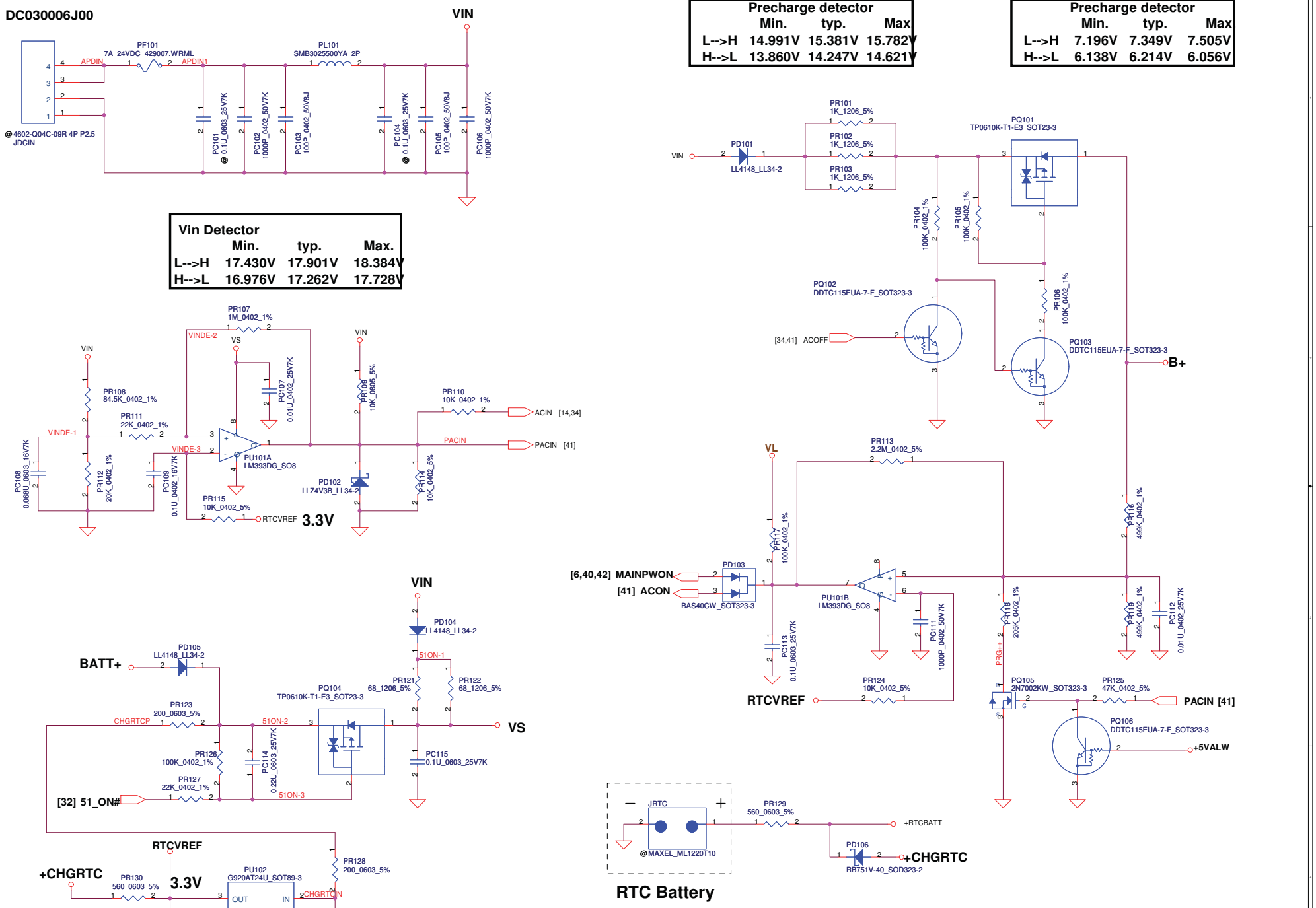
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: NAWE6 LA-5754P | Rev: 0.2

Date: Tuesday, March 02, 2010 | Sheet 38 of 47



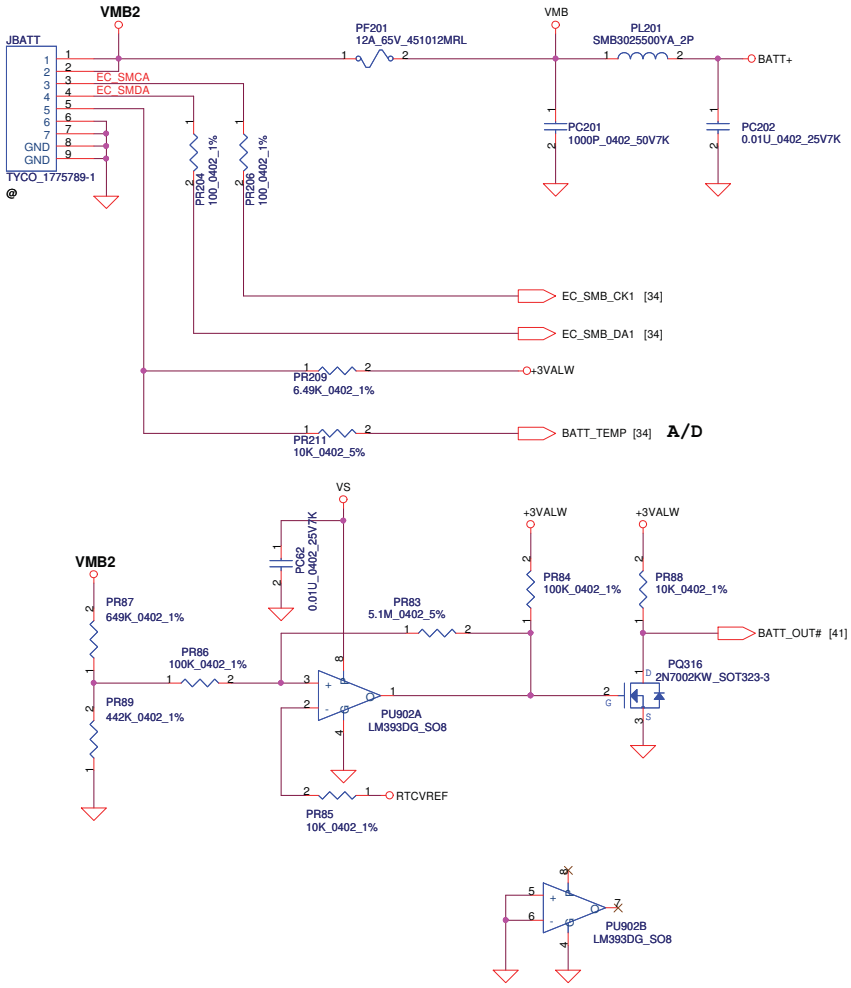
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

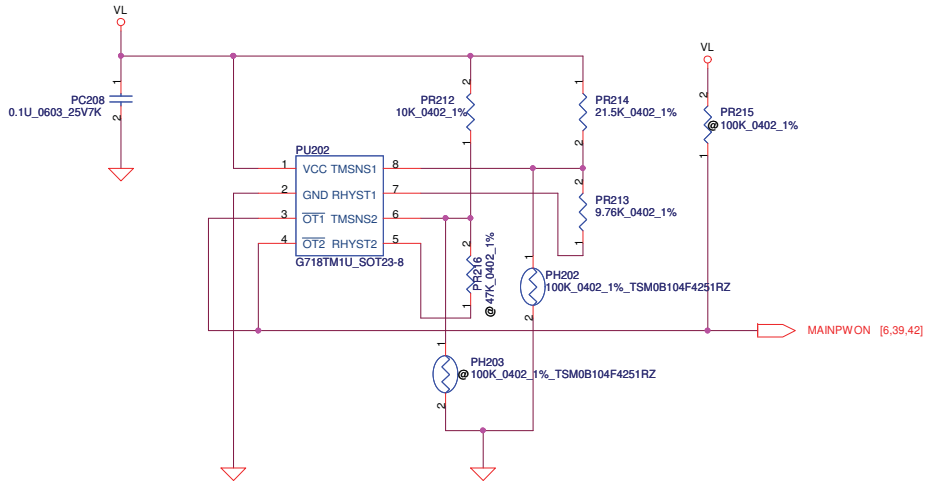
Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom		0.1

Date: Monday, March 01, 2010 Sheet 39 of 47



PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



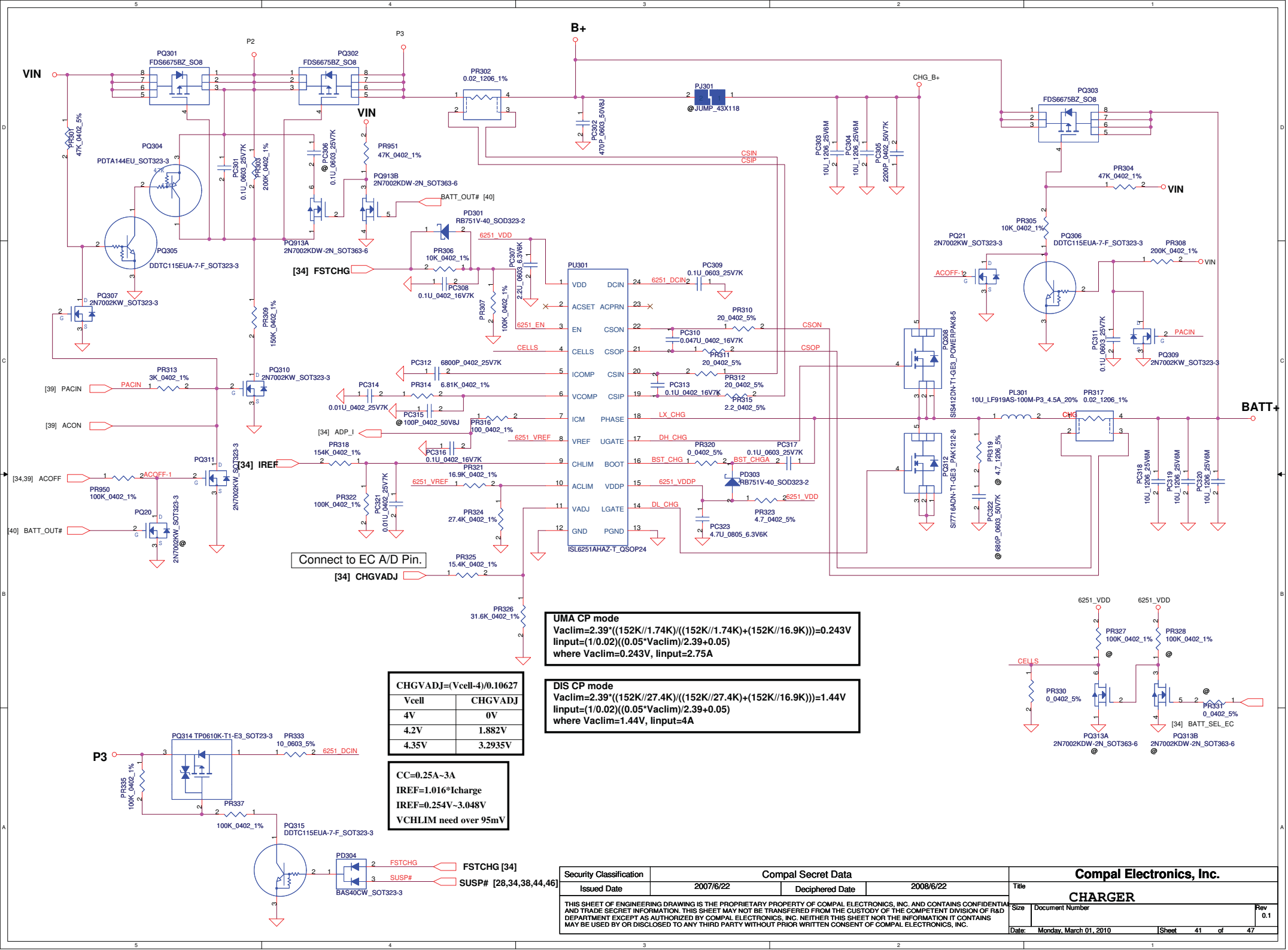
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		0.1

Date: Monday, March 01, 2010 Sheet 40 of 47



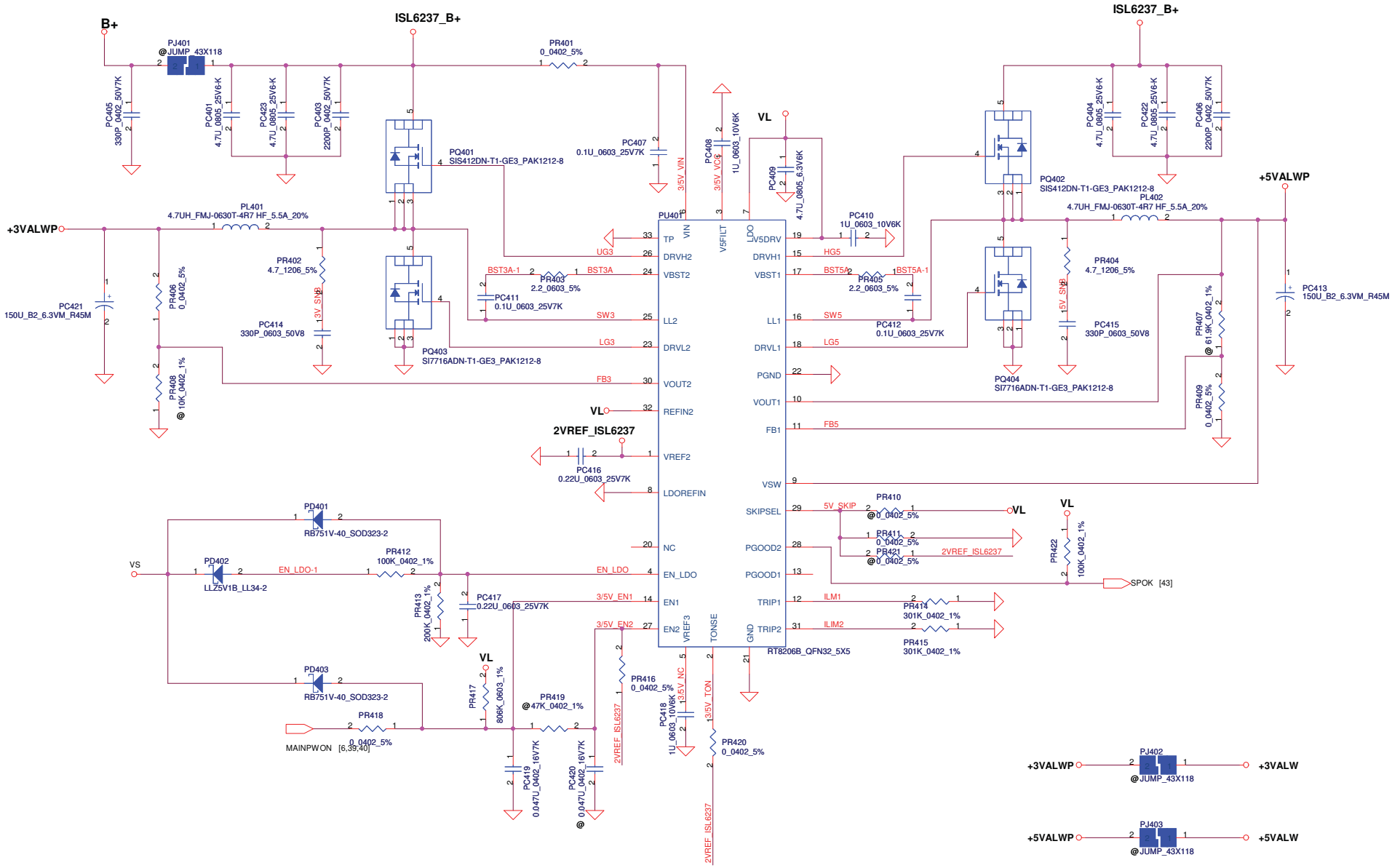
Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title: CHARGER

Size | Document Number | Rev 0.1

Date: Monday, March 01, 2010 | Sheet 41 of 47



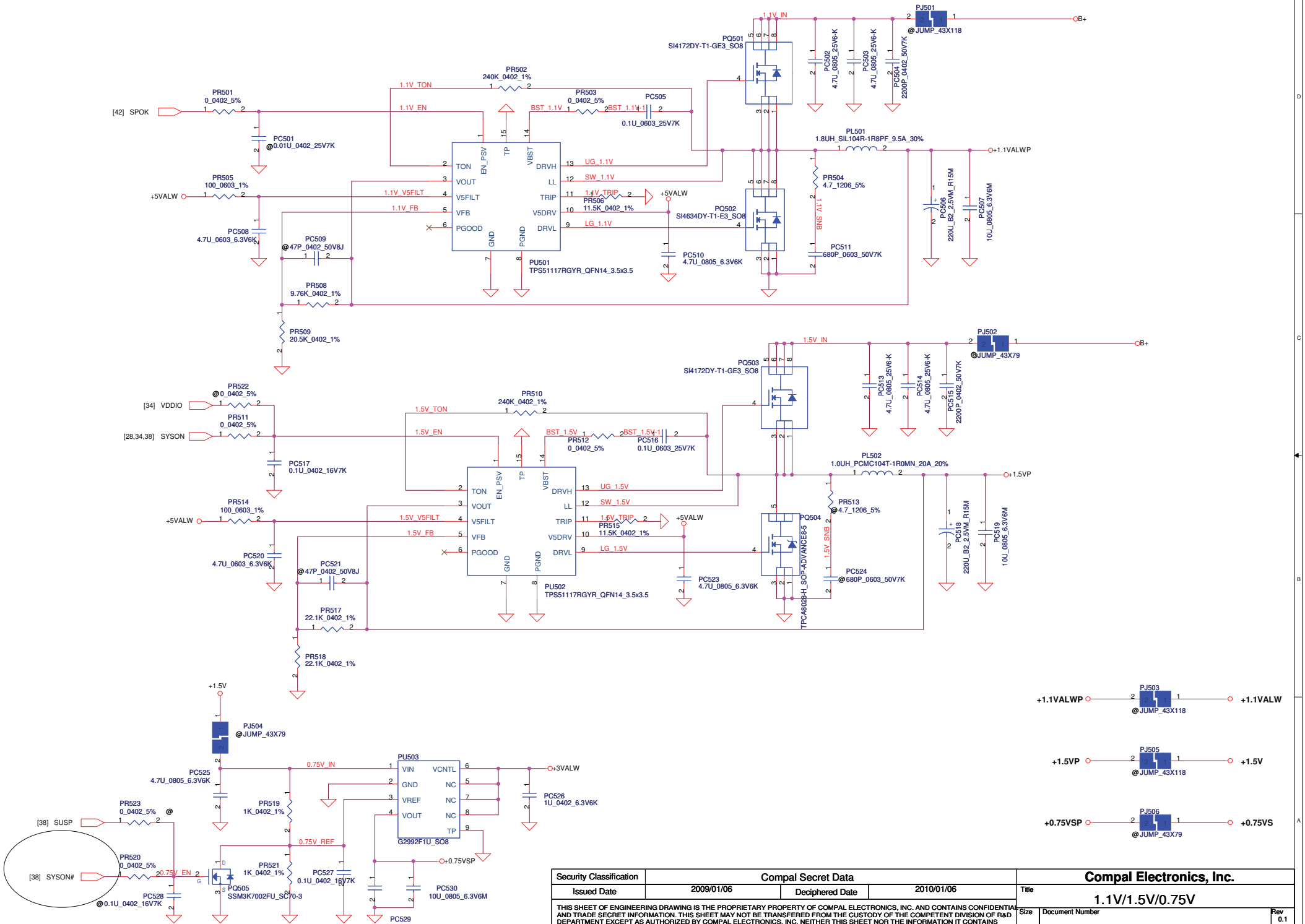
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size	Document Number	Rev
Custom		0.1

Date: Monday, March 01, 2010 | Sheet 42 of 47



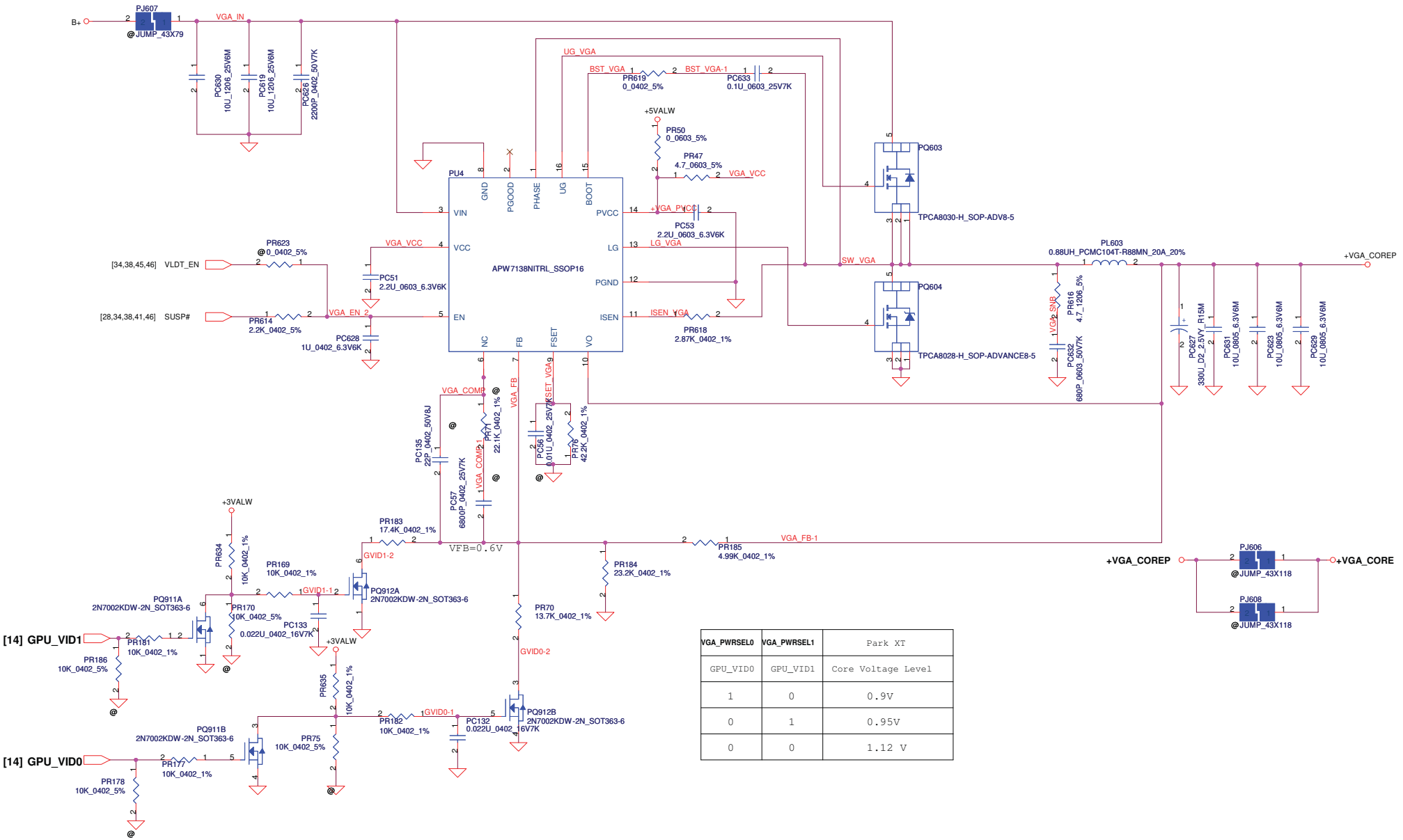
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: 1.1V/1.5V/0.75V

Size | Document Number | Rev 0.1

Date: Monday, March 01, 2010 | Sheet 43 of 47



VGA_PWRSEL0	VGA_PWRSEL1	Park XT
GPU_VID0	GPU_VID1	Core Voltage Level
1	0	0.9V
0	1	0.95V
0	0	1.12 V

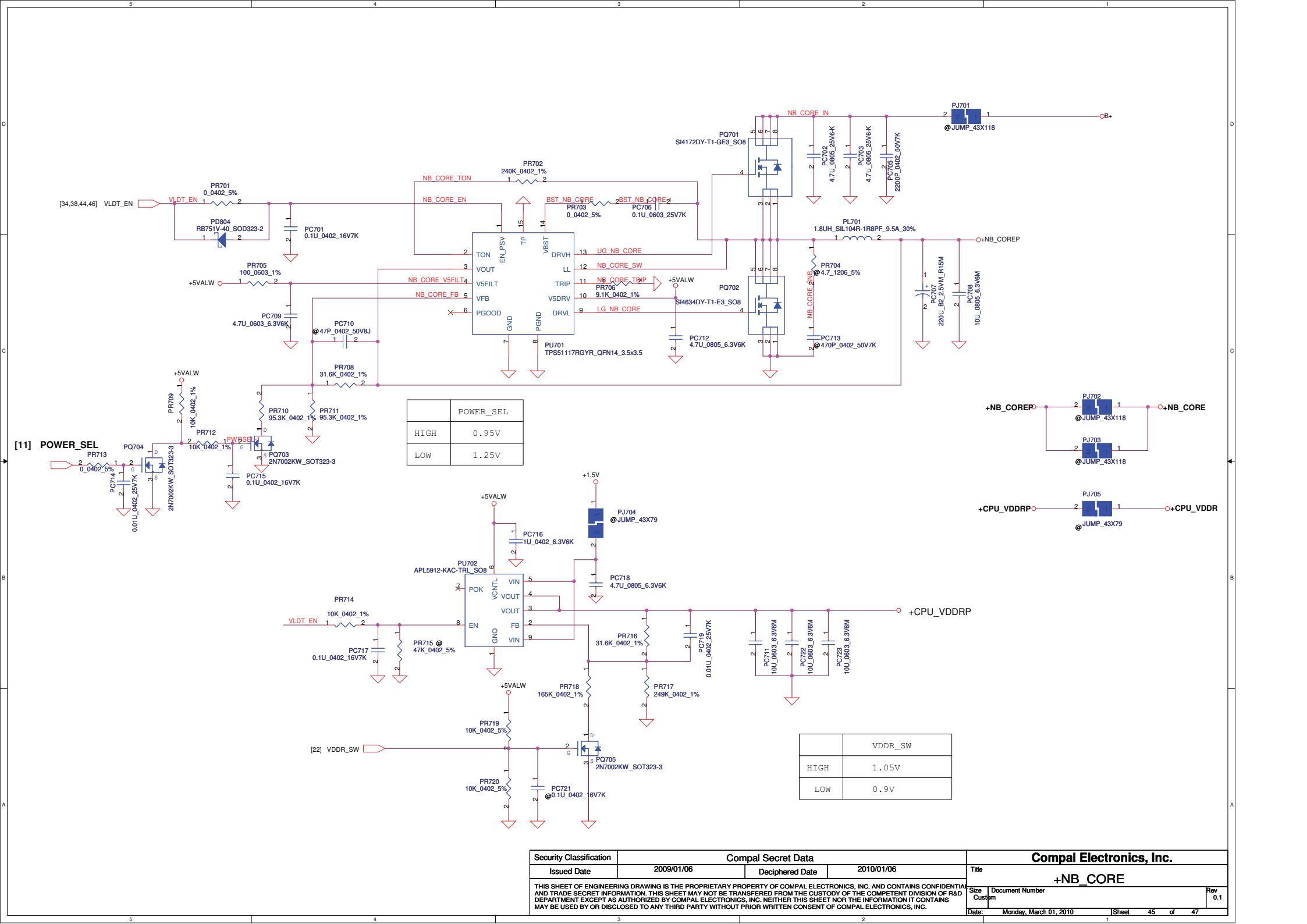
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: 1.5V/VGA_CORE

Size	Document Number	Rev
		0.1

Date: Monday, March 01, 2010 | Sheet 44 of 47


[11] POWER_SEL
[34,38,44,46] VLDT_EN
[22] VDDR_SW
NB_CORE_IN
B+
+NB_COREP
+NB_CORE
+CPU_VDDRP
+CPU_VDDR
+5VALW
+1.5V
PU701 TPS51117RGYR_QFN14_3.5x3.5
PU702 APL5912-KAC-TRL_SO8
PQ701 SI4172DY-T1-GE3_SO8
PQ702 SI4634DY-T1-E3_SO8
PQ703 2N7002KW_SOT323-3
PQ704 2N7002KW_SOT323-3
PQ705 2N7002KW_SOT323-3
PL701 1.8UH_SIL104R-1R8PF_9.5A_30%
PJ701 @JUMP_43X118
PJ702 @JUMP_43X118
PJ703 @JUMP_43X118
PJ704 @JUMP_43X79
PJ705 @JUMP_43X79
POWER_SEL
HIGH 0.95V
LOW 1.25V
VDDR_SW
HIGH 1.05V
LOW 0.9V
Security Classification
Compal Secret Data
Issued Date 2009/01/06
Deciphered Date 2010/01/06
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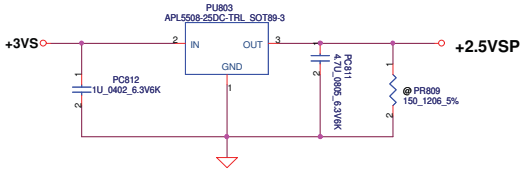
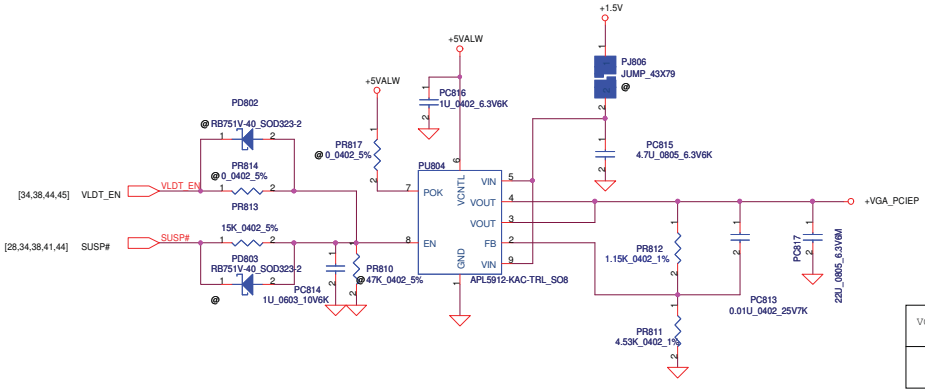
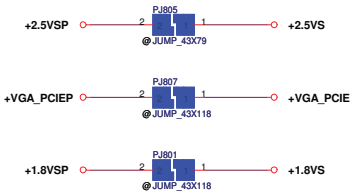
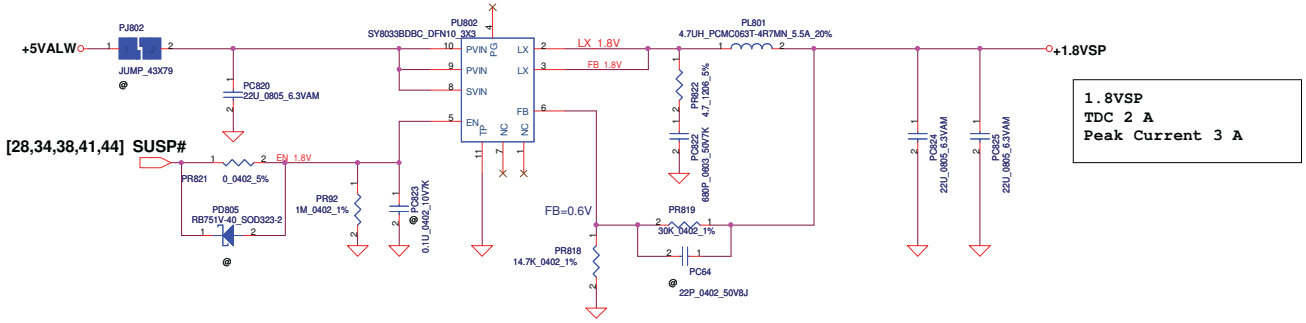
Compal Electronics, Inc.
Title +NB_CORE
Size Custom
Document Number
Rev 0.1
Date: Monday, March 01, 2010
Sheet 45 of 47





VGA_PCIE	1.0V	1.1 V
PR811	4.53K	3K





1.8VSP
TDC 2 A
Peak Current 3 A

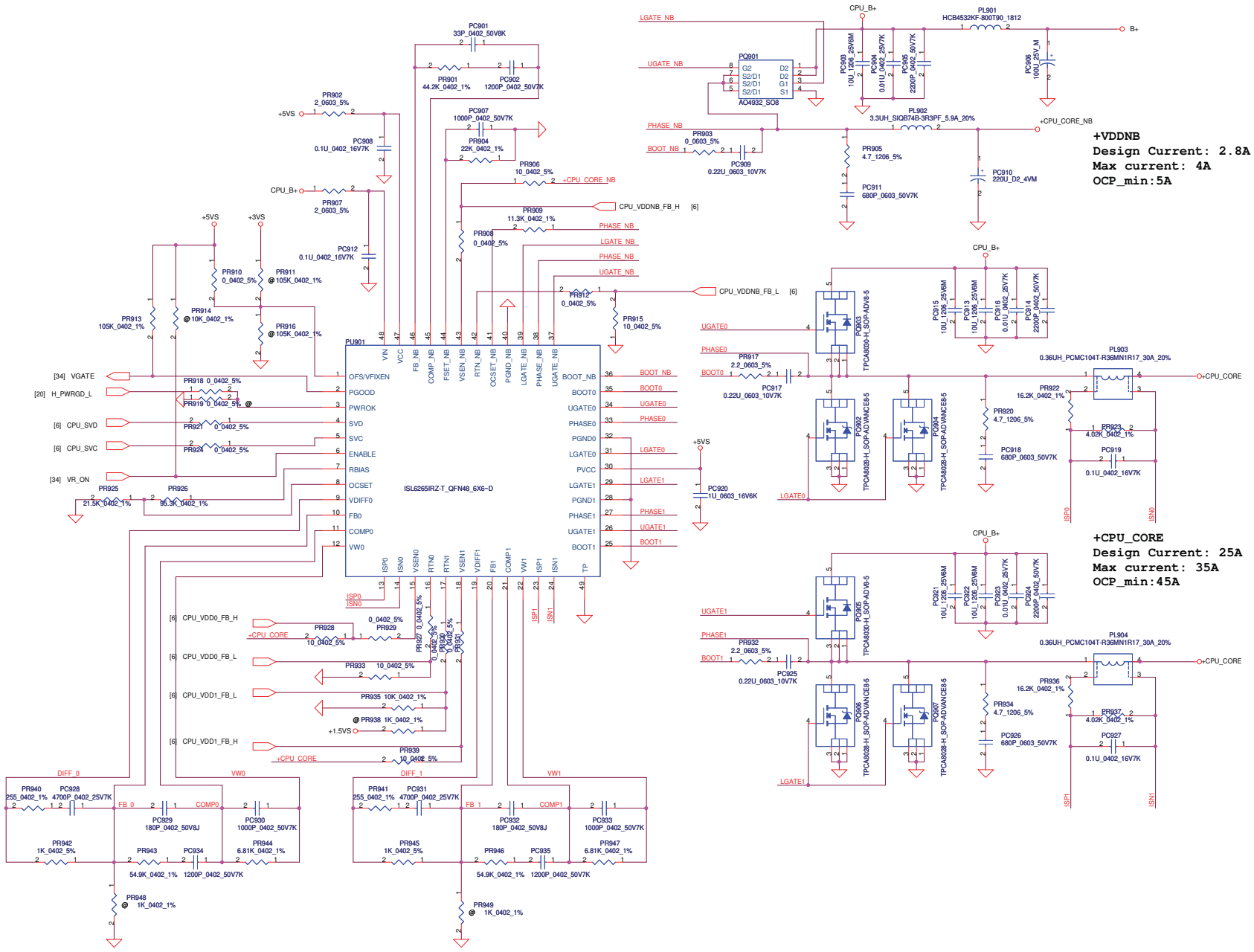
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: 2.5VS/PCIE/1.8VS

Size | Document Number | Rev 0.1

Date: Monday, March 01, 2010 | Sheet 46 of 47



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Date: Monday, March 01, 2010 Sheet 47 of 47