

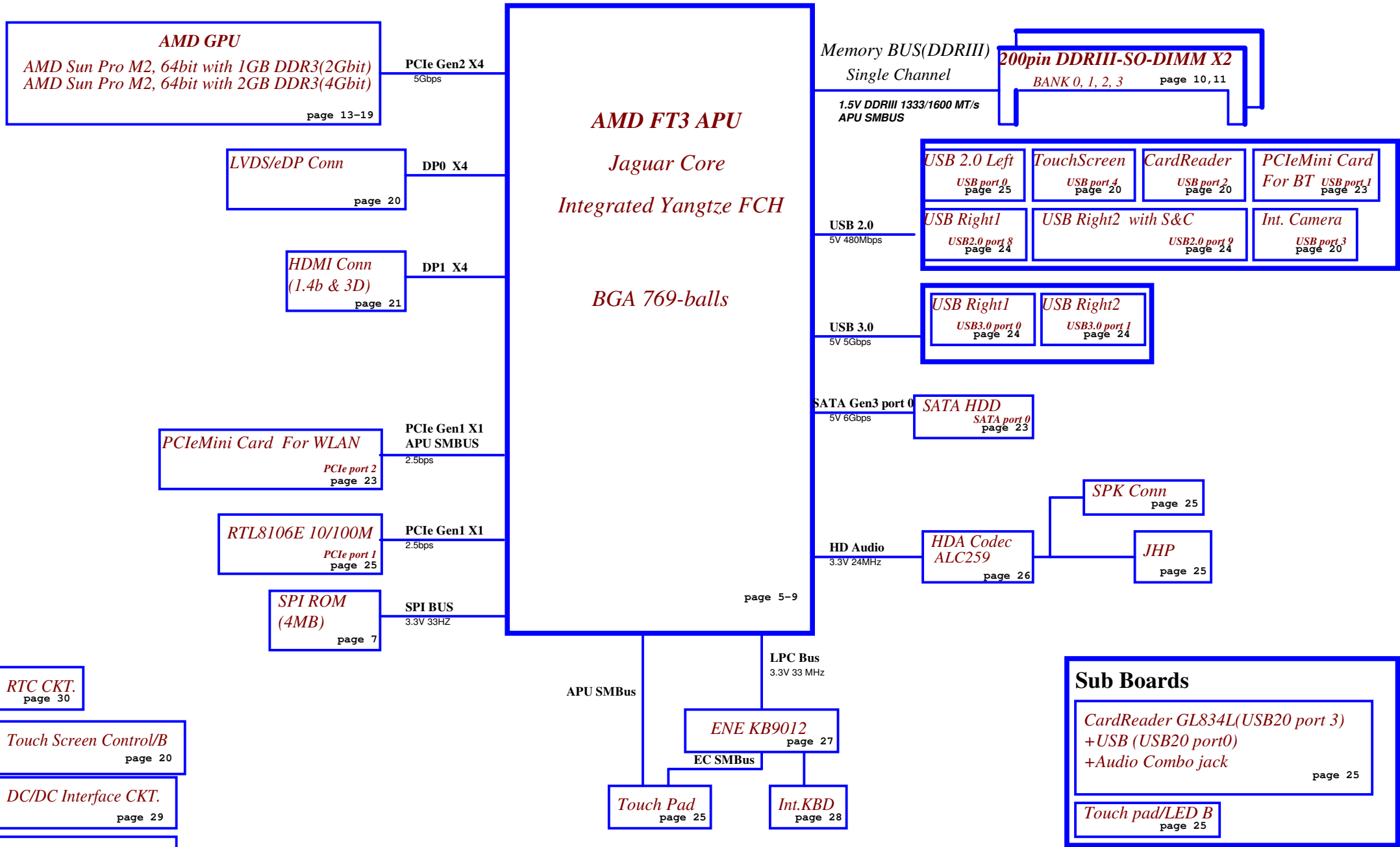
ZRMAE/ZEMAE

Juno/Iakros 10AN/10ANG

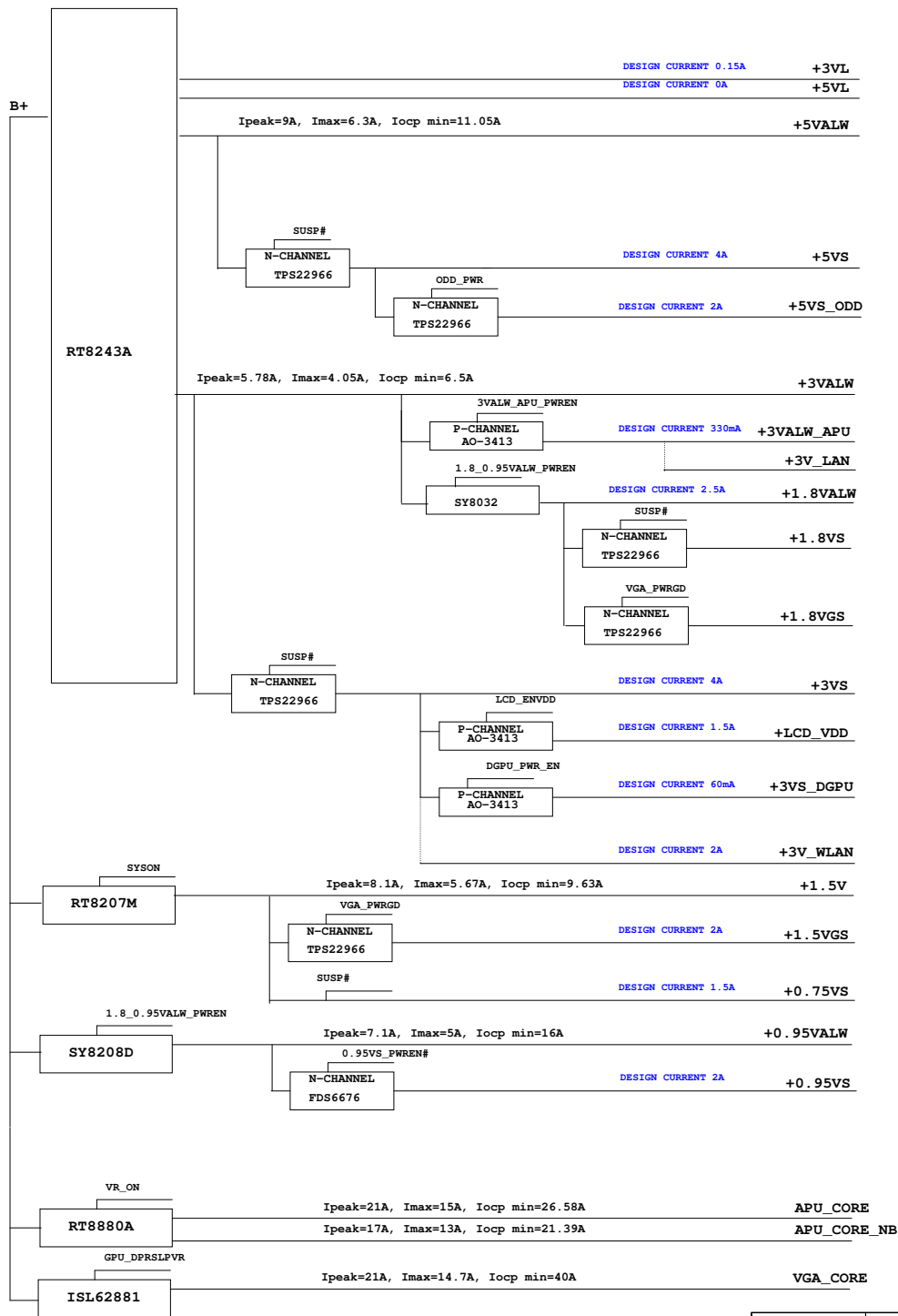
LA-A551P REV 1.0 Schematic

AMD KABINI Quad Core 25W for UMA+DIS
AMD KABINI Quad Core 15W
2013-07-05 Rev 1.0

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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.8VALW +0.95VALW +VSB	+1.5V	+5VS +3VS +0.95VS +1.8VS +1.5VS +0.75VS +APU_CORE +APU_CORE_NB
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

UMA

BTO Option Table

Function	APU	
description	CPU A4-5000	CPU A6-5200
explain	15W 4C	25W 4C
BTO	A4R1@	A6R1@

Function	GPU	EC			LVDS-eDP		Camera & Mic			KB Light
description	Sun-Pro M2	9012	885		LVDS-eDP		Camera & Mic			KB Light
explain	VGA	9012	w/	w/ EMI	LVDS	eDP	Camera & Mic			KB Light
BTO	VGA@	9012@	885@	885_EMI@	LVDS@	IEDP@	CAM@	CAM@EMI@	@CAM@EMI@	KBL@

Function	LAN	S&C		Size		Codec	Touch Screen	
description	8106E	TI solution		Size		ALC259	Touch Screen	
explain	8106E	TPS2546	TPS2544	14"	15"	ALC259	W/ Touch	W/O EMI Touch
BTO	8106E@	2546@	2544@	14@	15@	259@	Touch_EMI@	@Touch_EMI@

Function	EMI/ESD/RF part				
description	EMI/ESD/RF part				
explain	EMI/ESD/RF part				
BTO	EMI@	@EMI@	ESD@	@ESD@	@RF@

APU SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM A	A0H	1010 0000 b
+3VS	DDR SO-DIMM B	A2H	1010 0010 b
+3VS	WLAN		

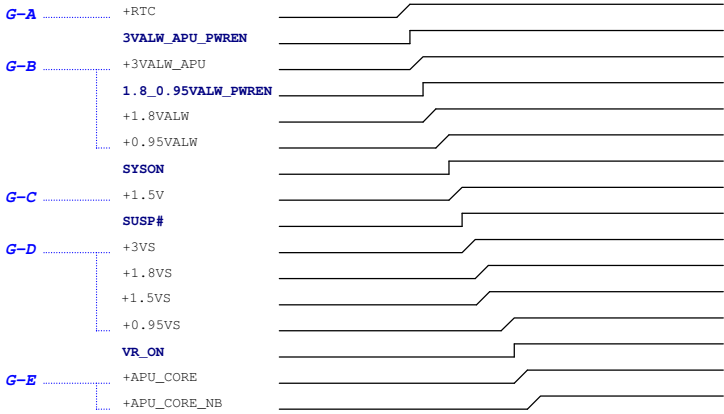
EC SM Bus1 Address

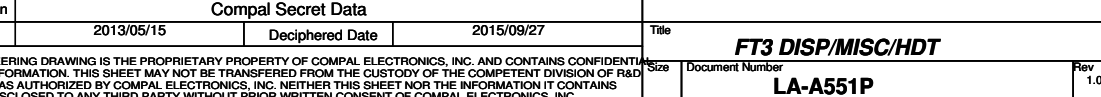
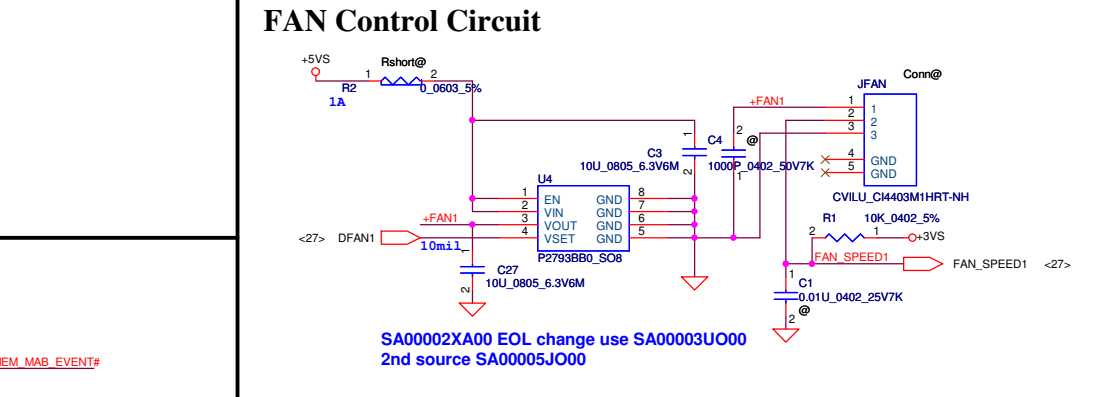
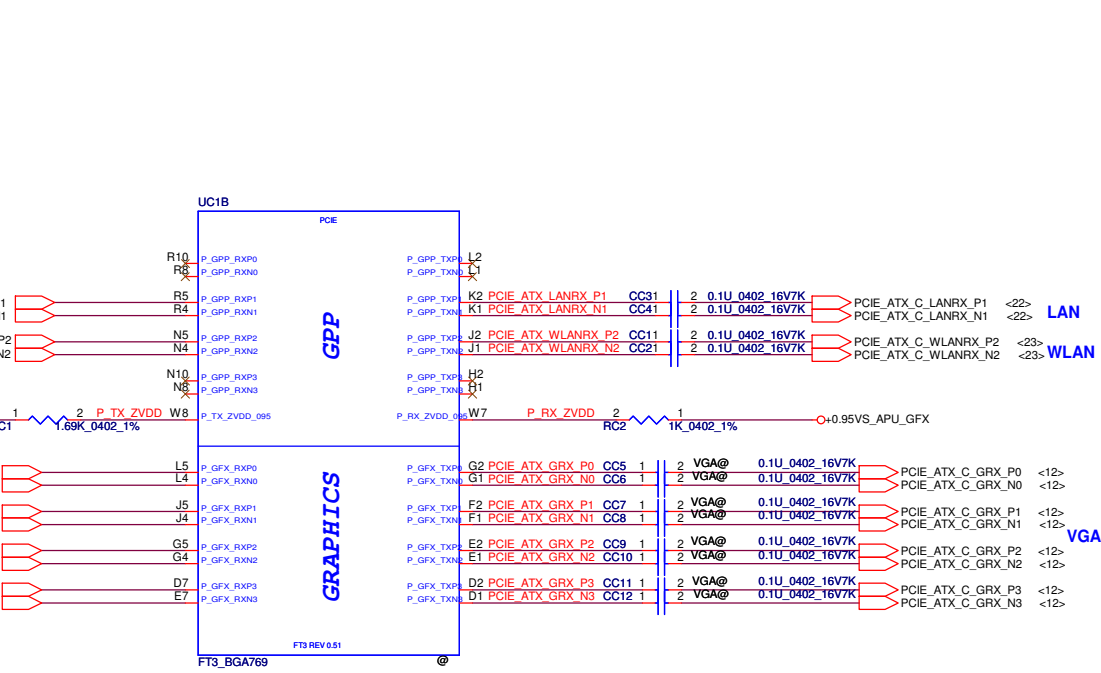
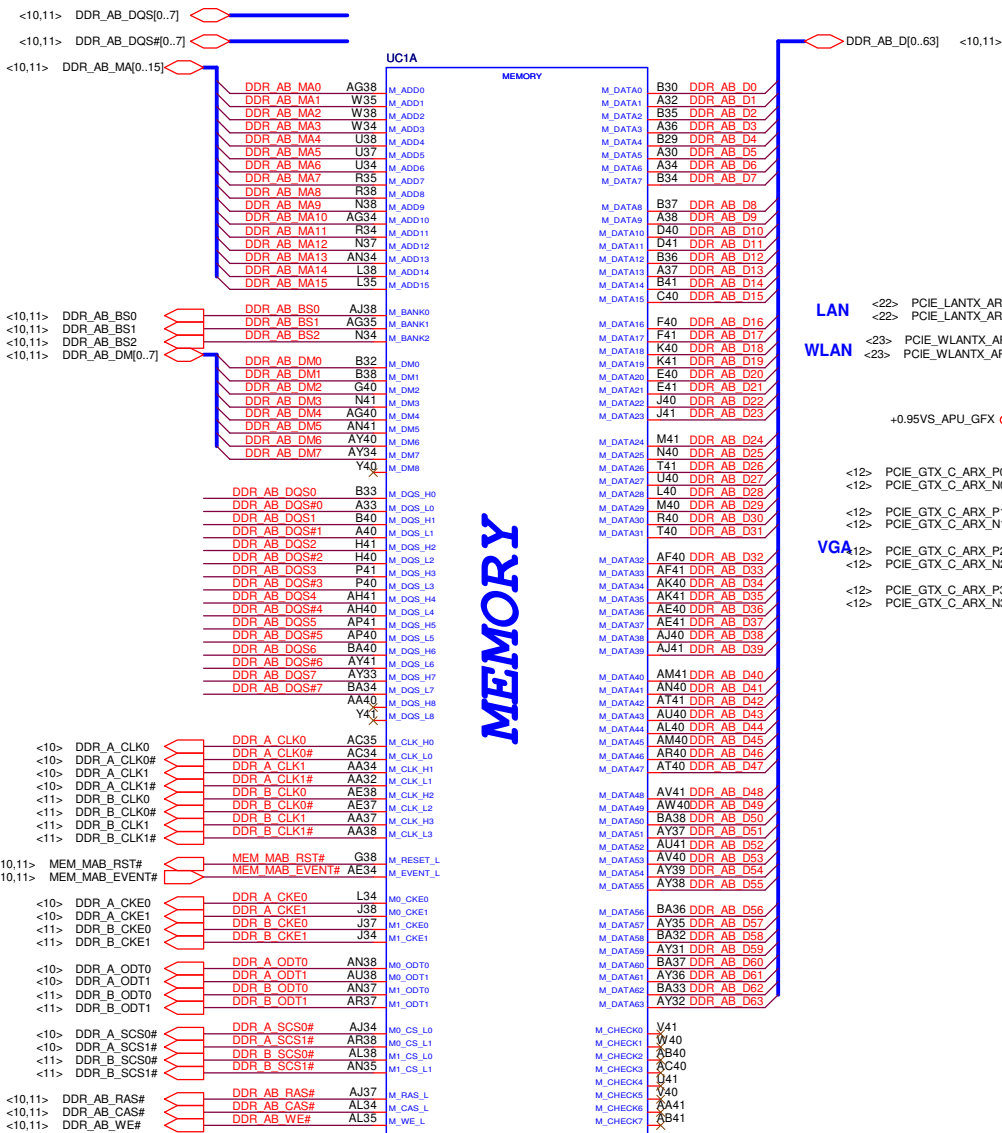
EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16H	0001 0110 b	+3VS	VGA thermal	82H	1000 0010 b
+3VL	Charger	12H	0001 0010 b	+3VS	APU thermal	98H	1001 1000 b

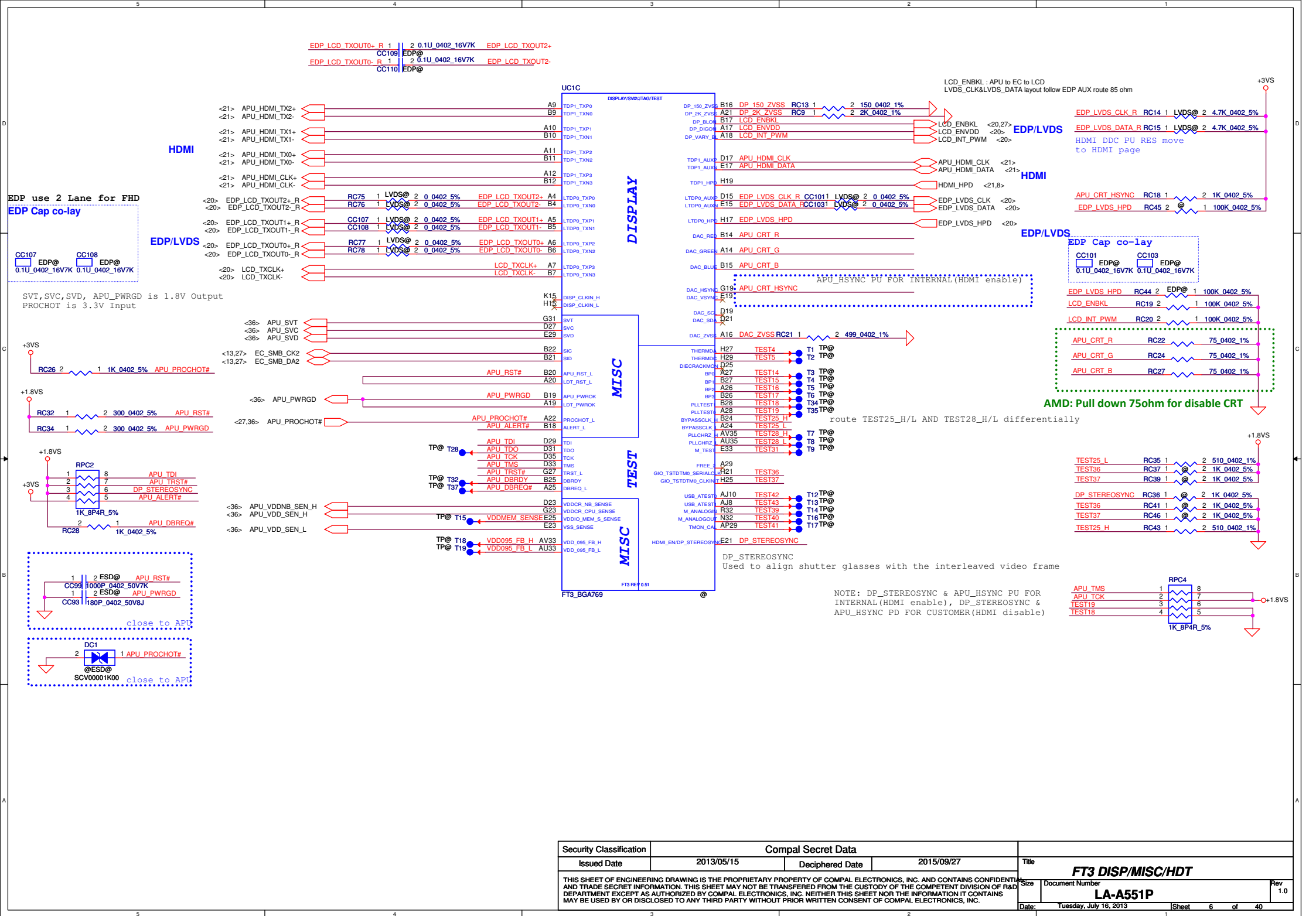
STATE	SIGNAL	SLP_S3#	SLP_S5#
Full ON		HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH
S4 (Suspend to Disk)		LOW	HIGH
S5 (Soft OFF)		LOW	LOW
G3		LOW	LOW

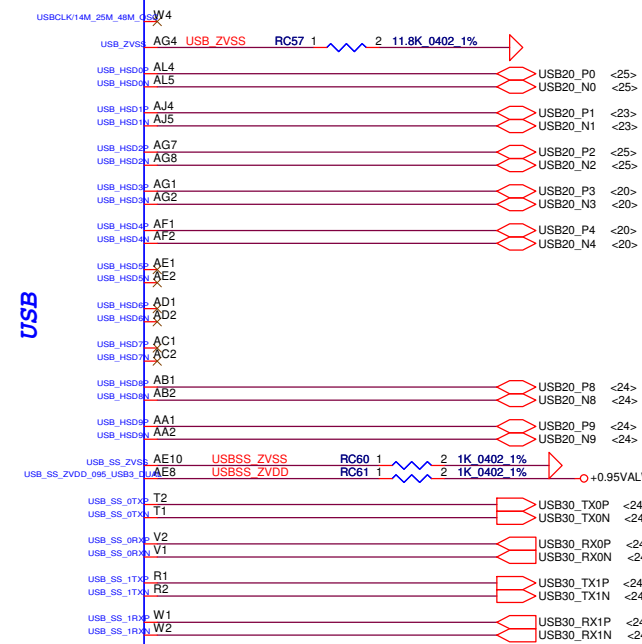
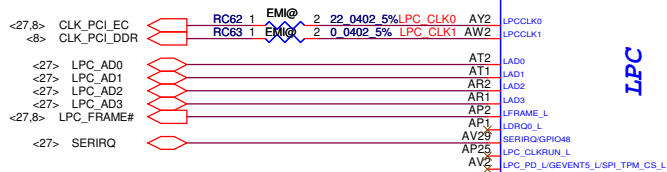
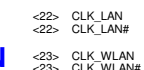
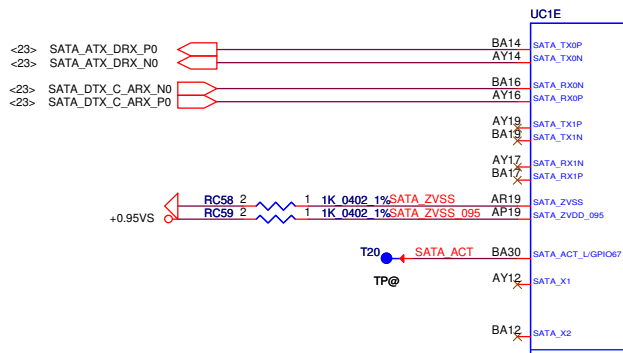
APU POWER SEQUENCE





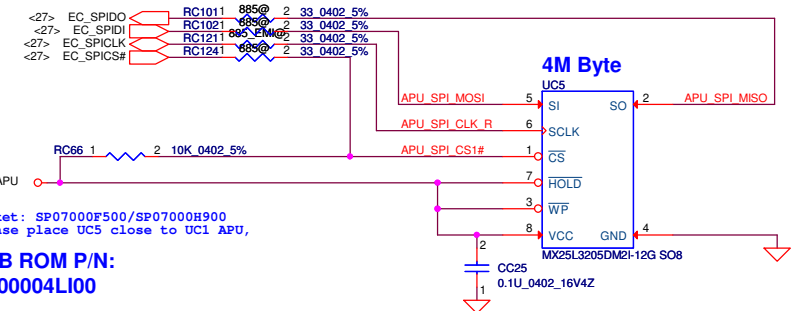
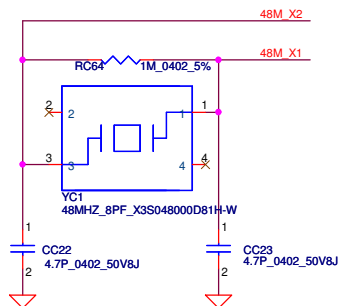
Security Classification		Compal Secret Data		Title	
Issued Date	2013/05/15	Deciphered Date	2015/09/27	FT3 DISP/MISC/HDT	
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24> **USB2.0-Right2**

<24>
<24> **USB3.0-Right2**

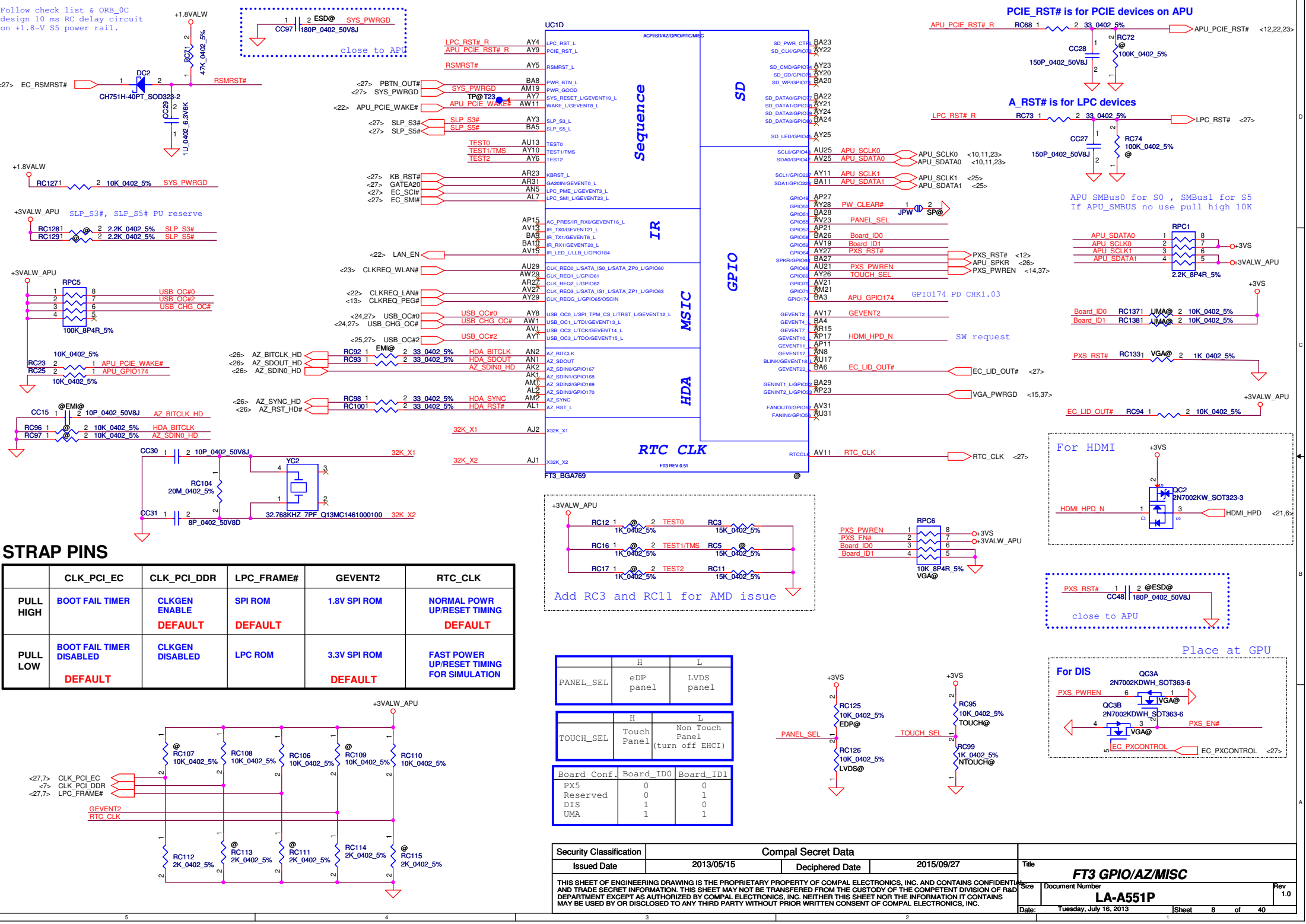


Socket: SP07000F500/SP07000H900
Please place UC5 close to UC1 APU,

**4MB ROM P/N:
SA00004LI00**

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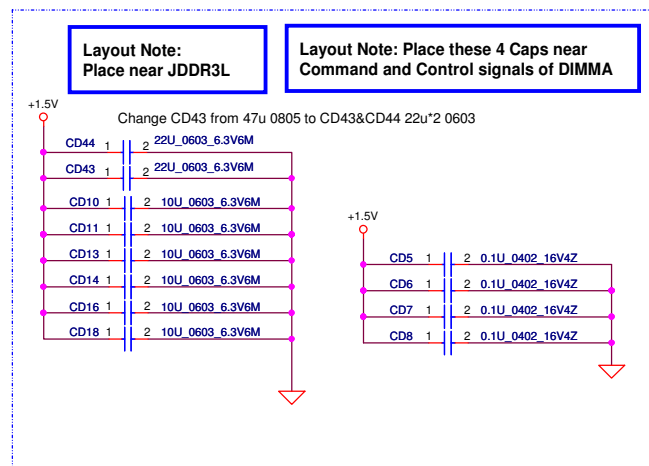
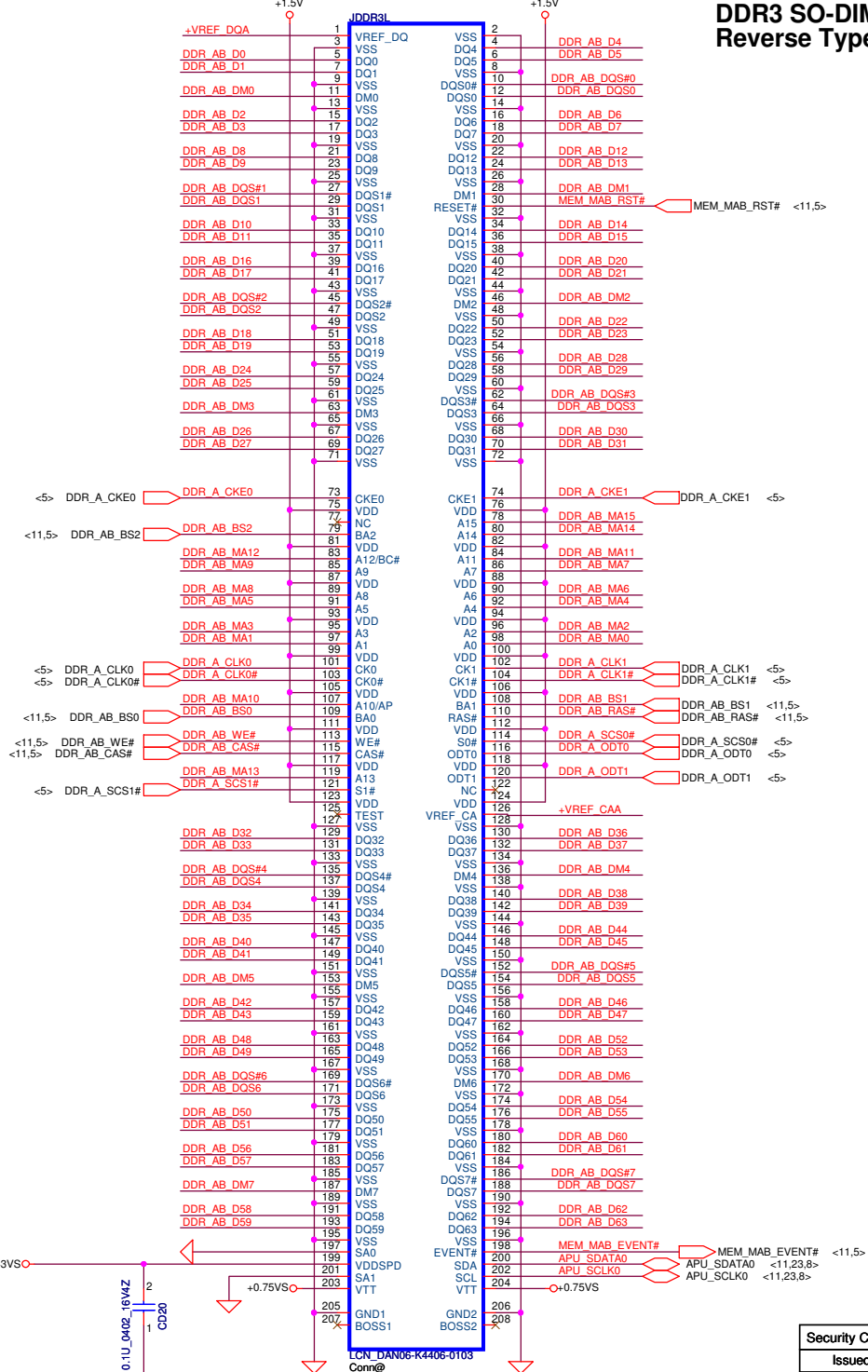
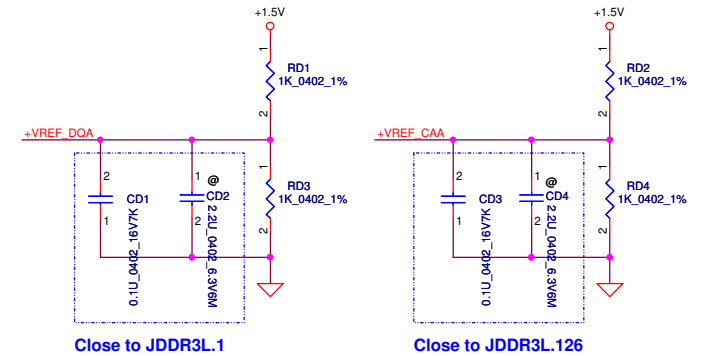
Follow check list & ORB_OC design 10 ms RC delay circuit on +1.8-V S5 power rail.



DDR3 SO-DIMM A Reverse Type

DDR_AB_DQS[0..7] <11,5>
DDR_AB_DQS#[0..7] <11,5>
DDR_AB_DM[0..7] <11,5>
DDR_AB_MA[0..15] <11,5>

SO-DIMM VREF

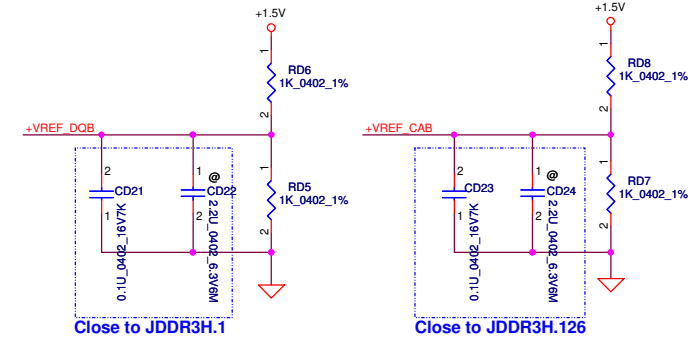


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DDR3 SO-DIMM B Standard Type

DDR_AB_DQS[0..7] <10,5>
DDR_AB_DQS[0..7] <10,5>
DDR_AB_D[0..63] <10,5>
DDR_AB_DM[0..7] <10,5>
DDR_AB_MA[0..15] <10,5>

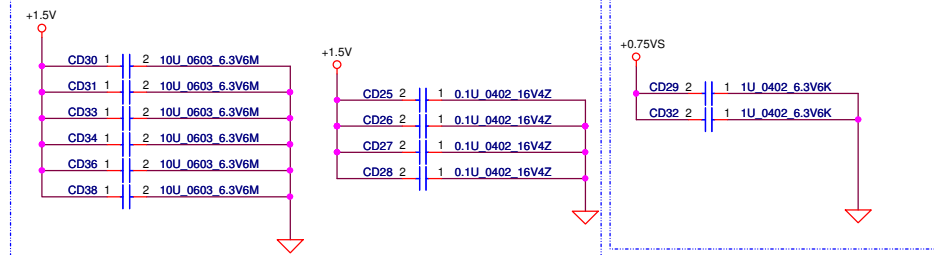
SO-DIMM VREF



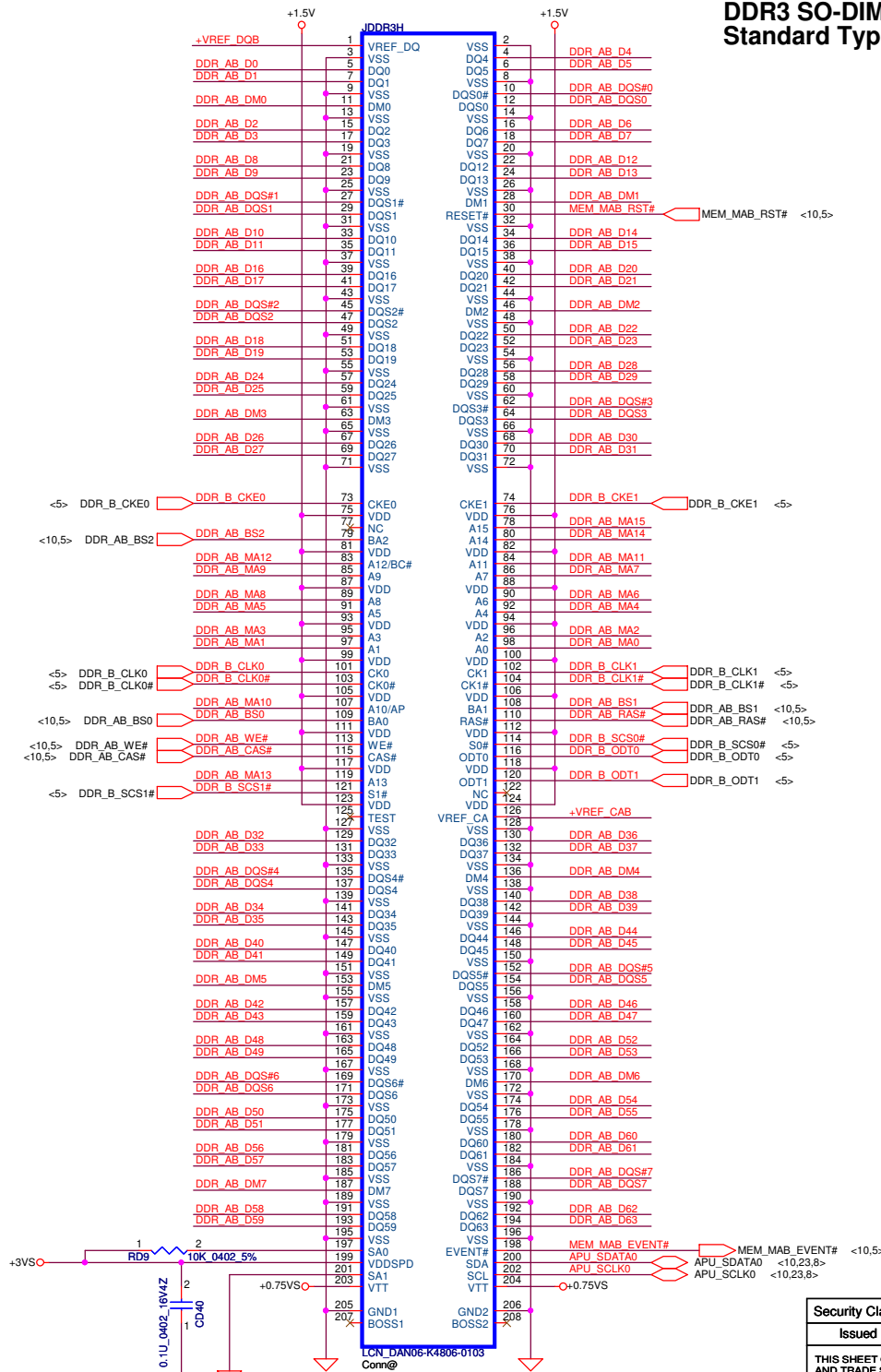
Layout Note:
Place near JDDR3H

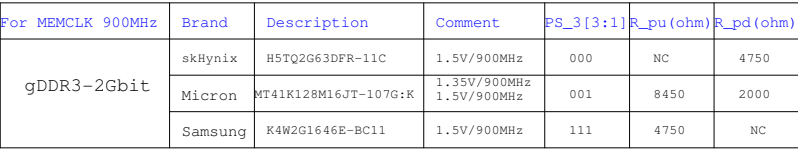
Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

Layout Note:
Place near JDDRH.203 and 204

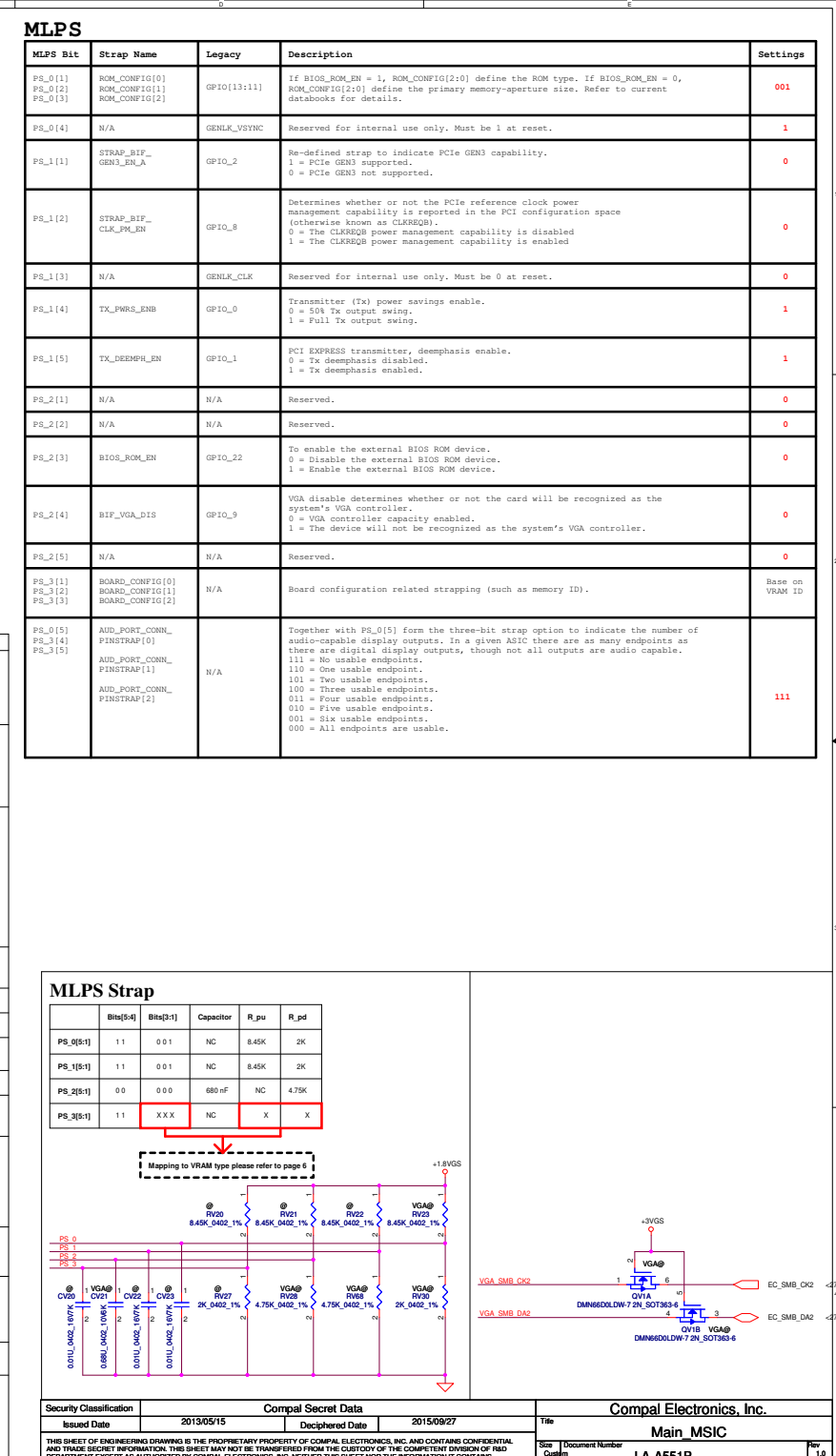


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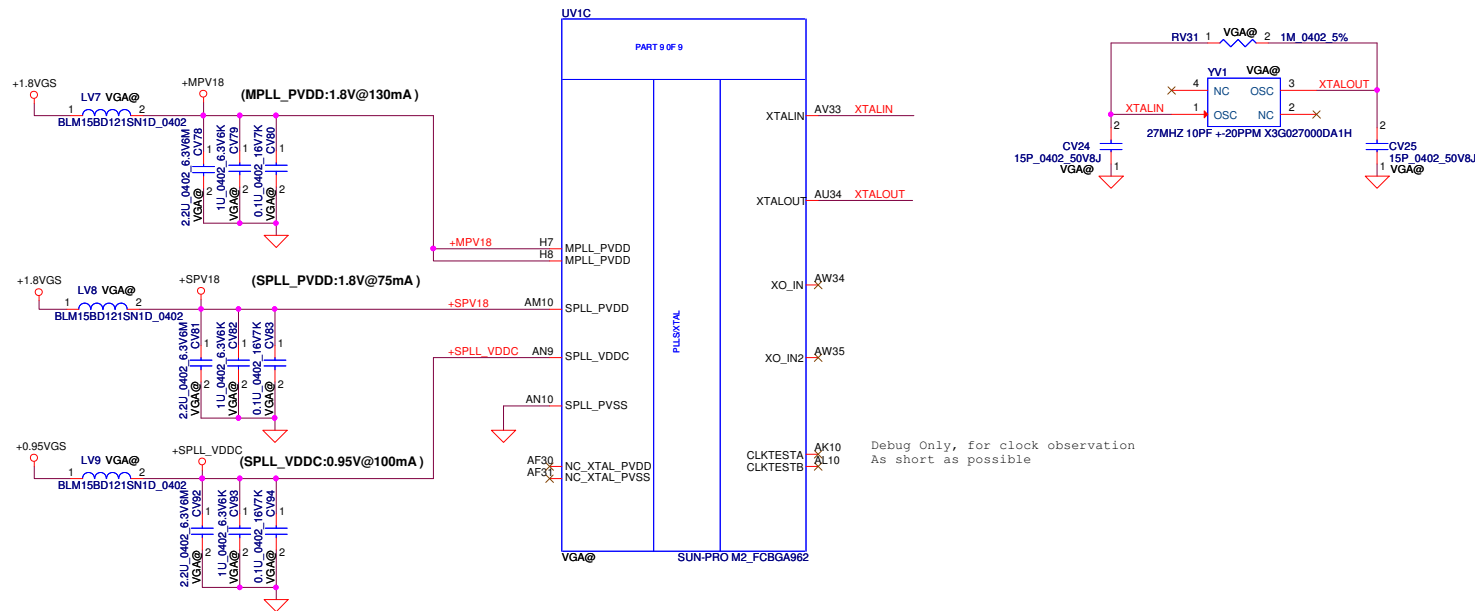
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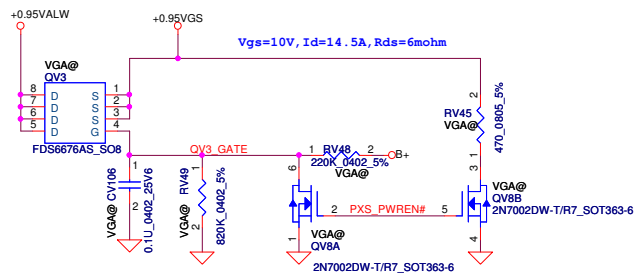
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

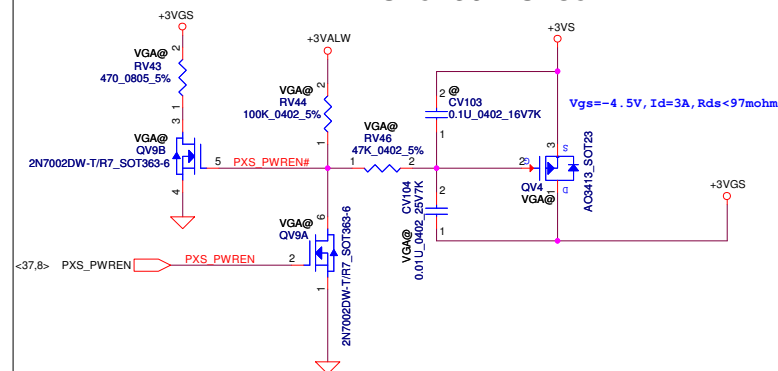
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1



+0.95VS to +0.95VGS



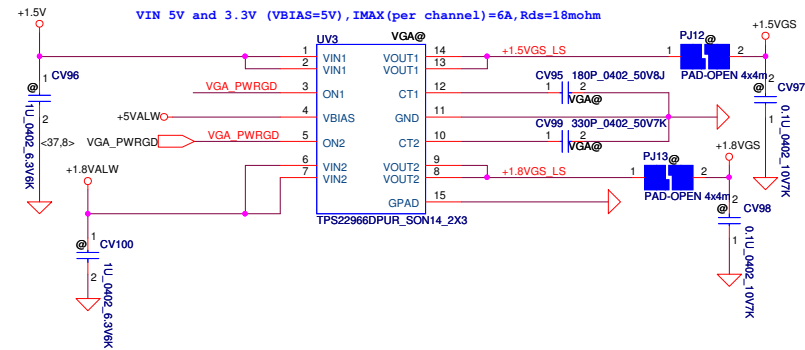
+3VS to +3VGS



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Only for Kabini

+1.8VALW to +1.8VGS
+1.5V to +1.5VGS

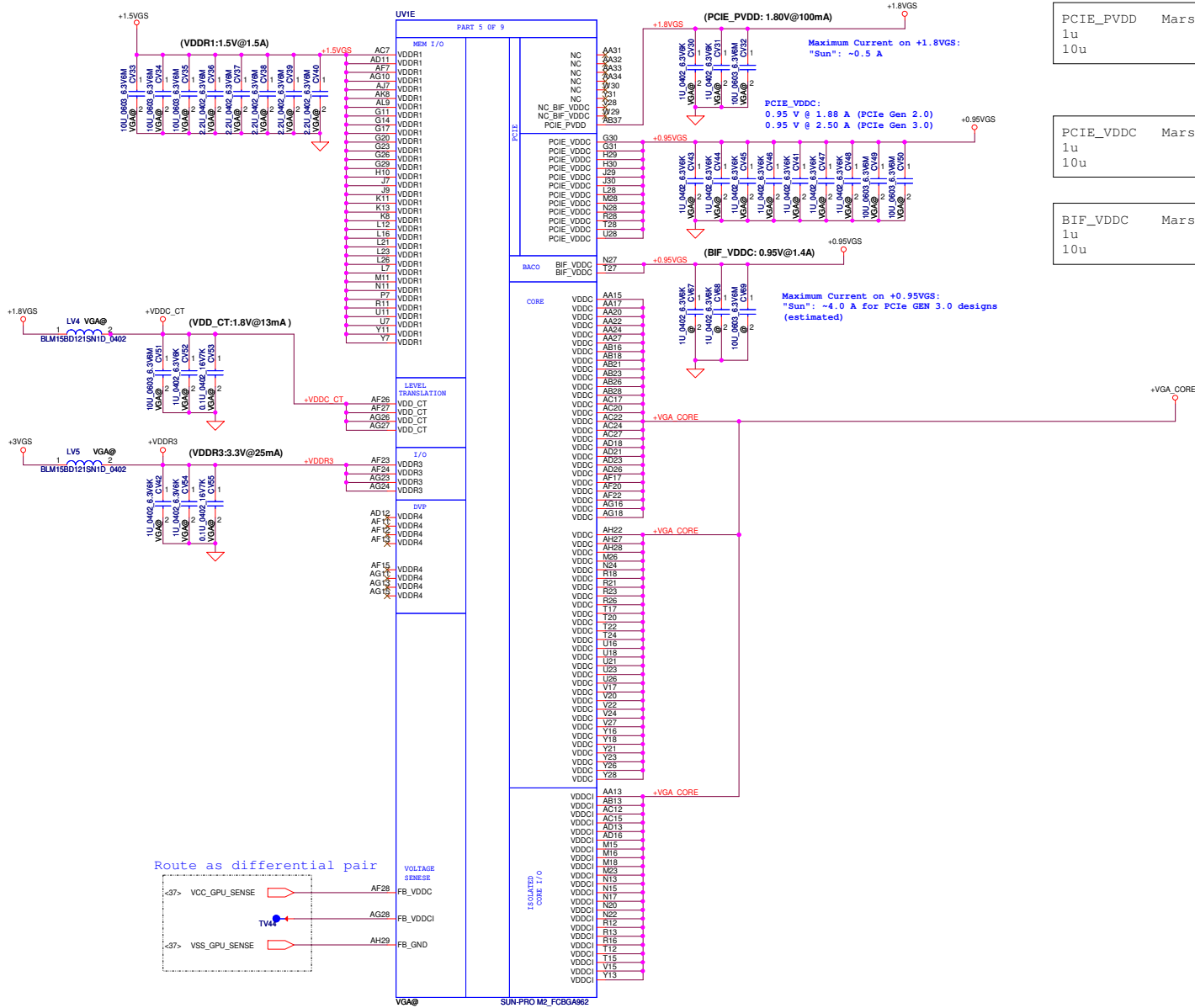


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VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	0
2.2u	5	5
10u	3	3

VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDDR3	Mars	check list	Design
120ohm	1		1
1u	3		2
10u	1		0
0.1u	0		1

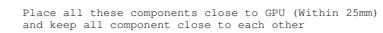
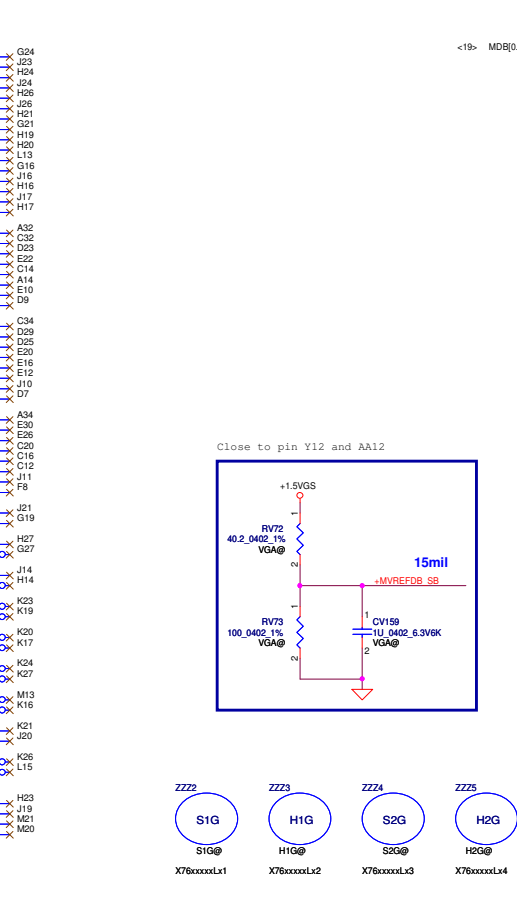


PCIE_PVDD	MarsCRB	Design
1u	2	2
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	7
10u	2	2

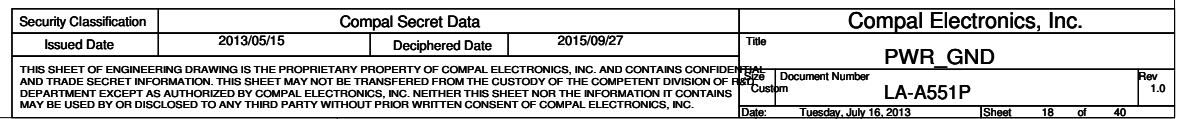
BIF_VDDC	Mars	check list	Design
1u	1		1
10u	1		1

Need check all power current and decoupling capacitors after got SUN databook and reference schematic.

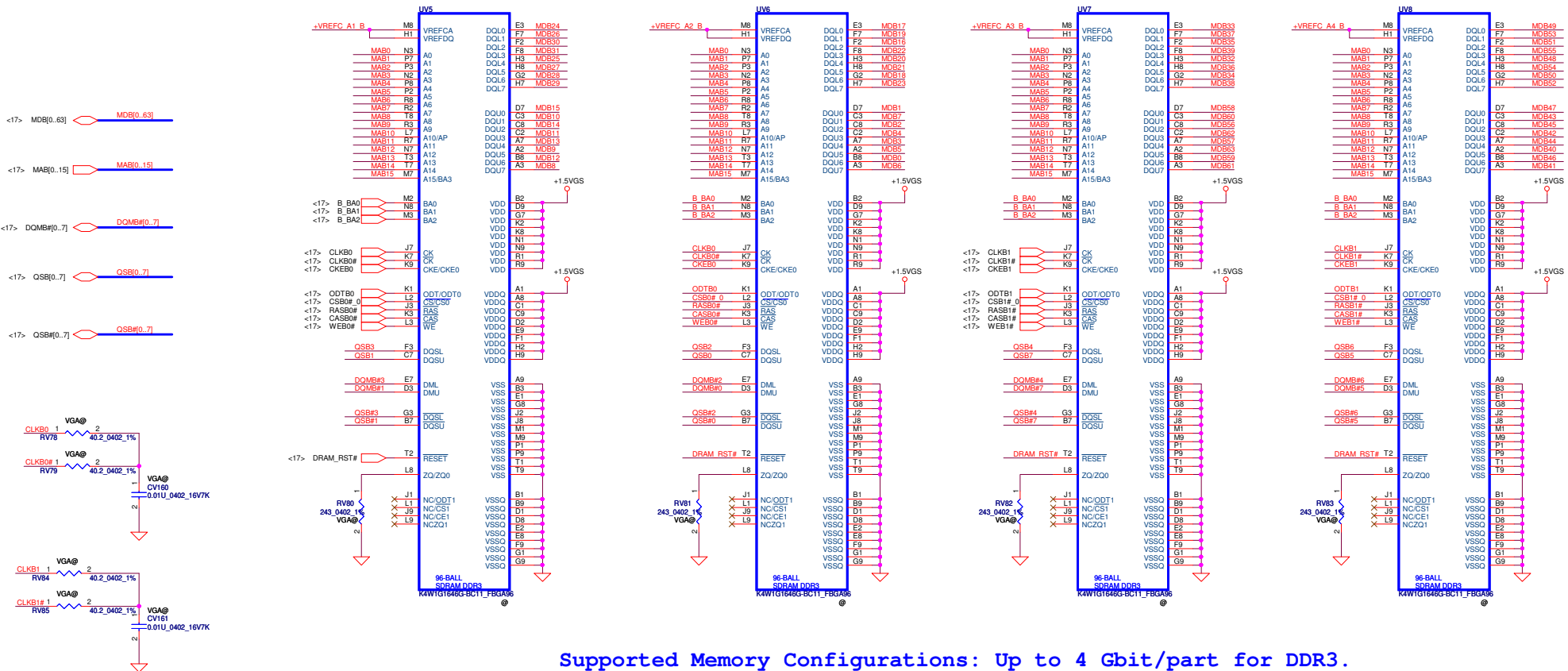


R_{pu} & R_{pd} resistor:
0402 1% resistors are required.

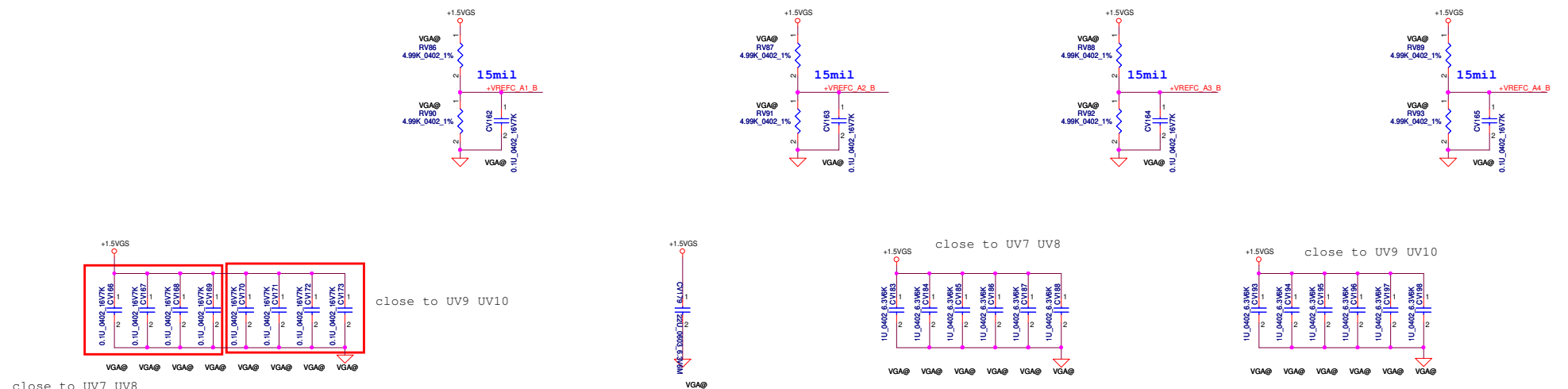
GPU Type	Memory Bus Width	VRAM Vendor	Compal P/N	Manufacturer P/N	X76 P/N	Size per part	Configuration	Total Memory Size/Qty	PS_3[3]	PS_3[2]	PS_3[1]	R_pu	R_pd
SUN PRO-M2	64bit	Samsung	SA000068U20	K4W2G1646E-BC1A		2Gbit	128M*16	1GB/4pcs	0	0	0	RV20 NC	RV27 4.75K
SUN PRO-M2	64bit	Micron	SA00005XB00	MT41K128M16JT-107G:K		2Gbit	128M*16	1GB/4pcs	0	0	1	RV20 8.45K	RV27 2K
SUN PRO-M2	64bit	Samsung	SA00005SH00	K4W2G1646E-BC11		2Gbit	128M*16	1GB/4pcs	0	1	0	RV20 4.53K	RV27 2K
SUN PRO-M3	64bit	Micron	SA00006D530	MT41K256M16HA-107G:E		4Gbit	128M*16	2GB/4pcs	1	1	0	RV20 3.4K	RV27 10K
SUN PRO-M4	64bit	Samsung	SA000068R20	K4W4G1646B-HC11		4Gbit	128M*16	2GB/4pcs	1	1	1	RV20 4.75K	RV27 NC



CHANNEL B: 512MB/1024MB DDR3



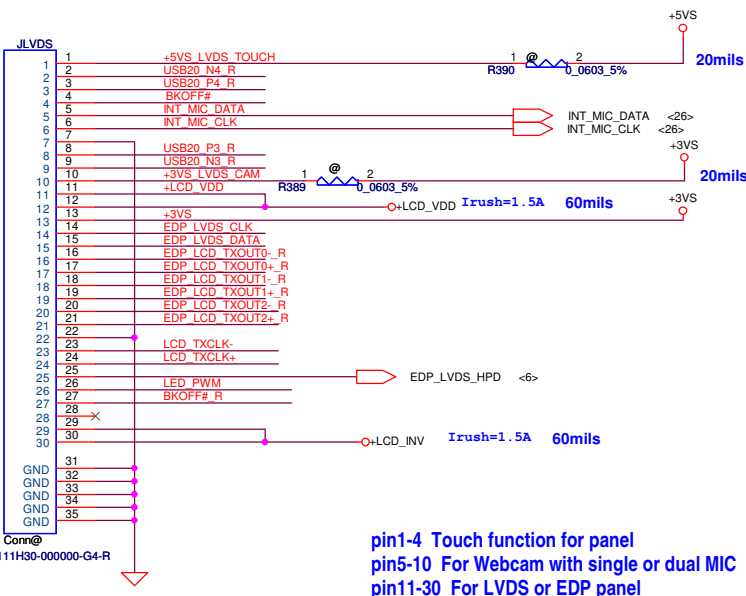
Supported Memory Configurations: Up to 4 Gbit/part for DDR3.



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Issued Date	2013/05/15	Deciphered Date	2015/09/27	VRAM Channel B
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<6> EDP_LCD_TXOUT0+_R EDP_LCD_TXOUT0+_R
 <6> EDP_LCD_TXOUT0-_R EDP_LCD_TXOUT0-_R
 <6> EDP_LCD_TXOUT1+_R EDP_LCD_TXOUT1+_R
 <6> EDP_LCD_TXOUT1-_R EDP_LCD_TXOUT1-_R
 <6> EDP_LCD_TXOUT2+_R EDP_LCD_TXOUT2+_R
 <6> EDP_LCD_TXOUT2-_R EDP_LCD_TXOUT2-_R
 <6> LCD_TXCLK+ LCD_TXCLK+
 <6> LCD_TXCLK- LCD_TXCLK-
 <6> EDP_LVDS_CLK EDP_LVDS_CLK
 <6> EDP_LVDS_DATA EDP_LVDS_DATA

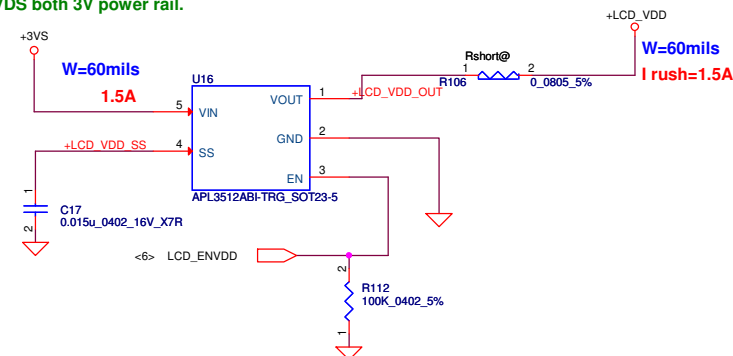
If it's EPD, they're become
 LCD_TXOUT2+_R = EDP_TX0+
 LCD_TXOUT2-_R = EDP_TX0-
 LCD_TXOUT1+_R = EDP_TX1+
 LCD_TXOUT1-_R = EDP_TX1-
 LVDS_CLK = EDP_AUXP
 LVDS_DATA = EDP_AUXN



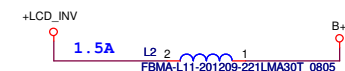
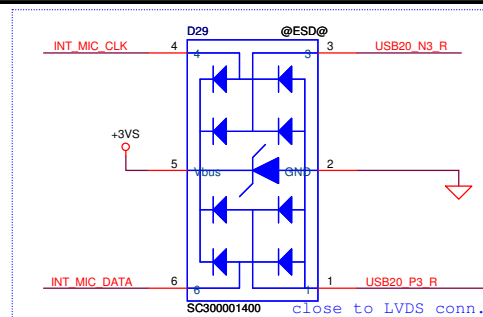
pin1-4 Touch function for panel
 pin5-10 For Webcam with single or dual MIC
 pin11-30 For LVDS or EDP panel

LCD_VDD

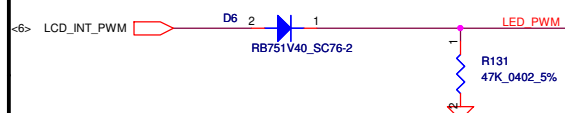
Need check eDP&LVDS both 3V power rail.



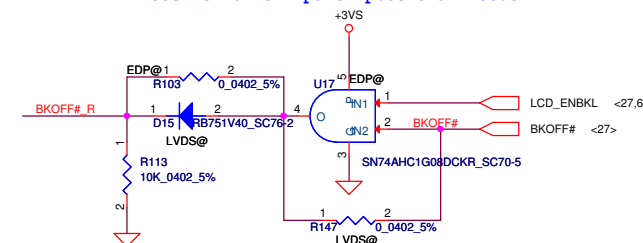
LCD_INV



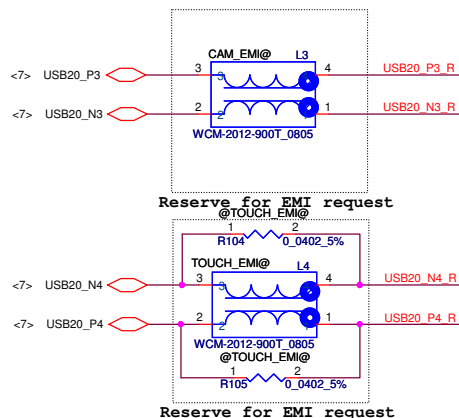
LCD Control



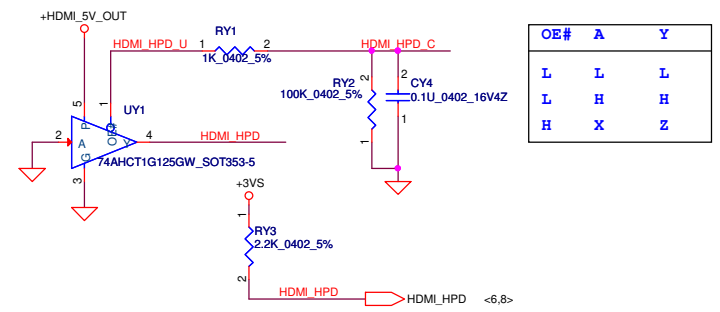
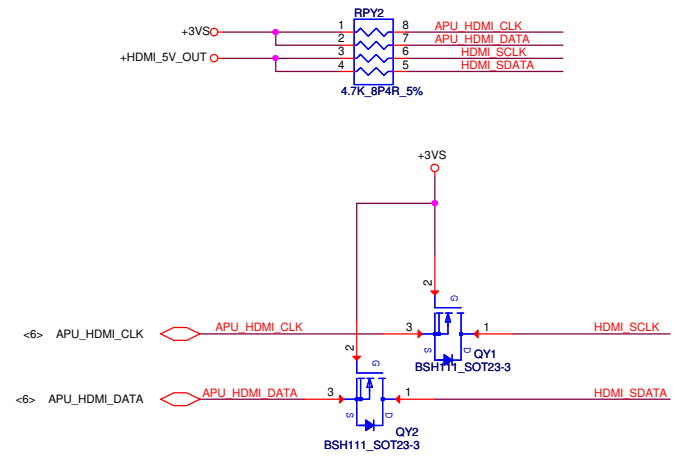
Reserve for eDP panel potential issue



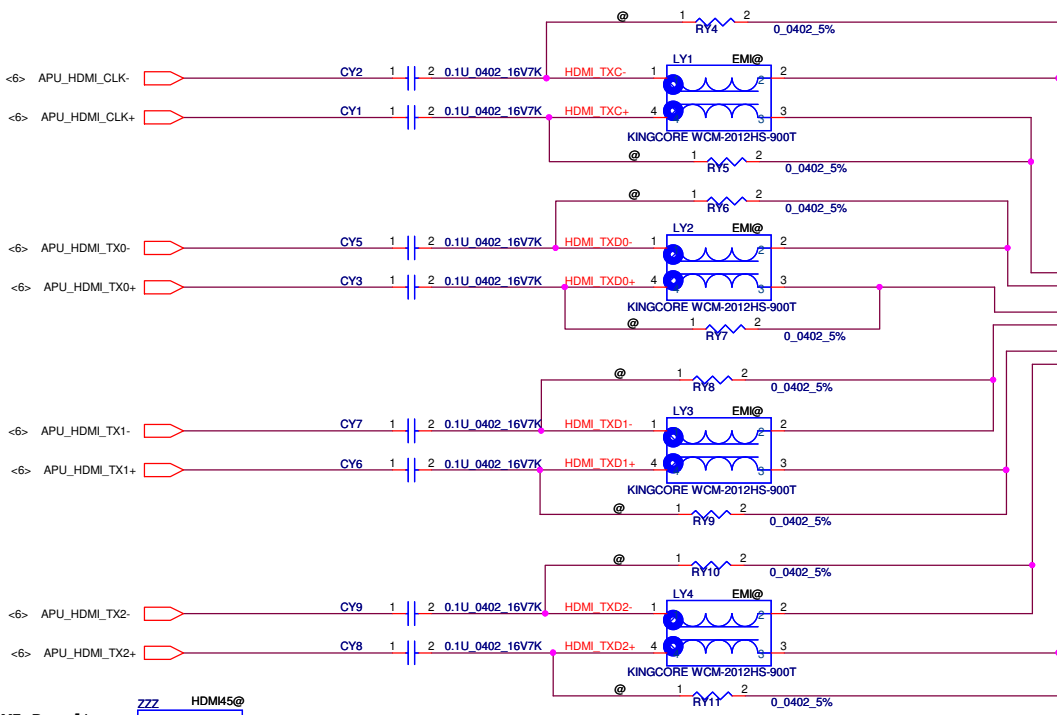
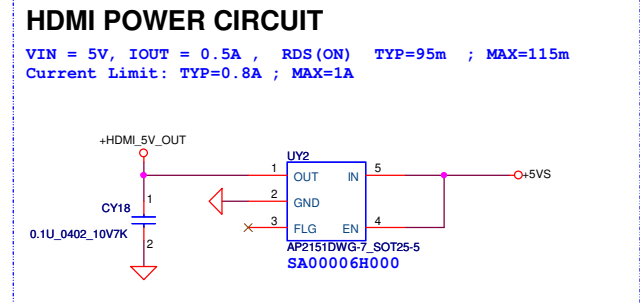
Camera & Touch Screen



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Issued Date	2013/05/15	Deciphered Date	2015/09/27	Title	LVDS/EDP W/ CAMERA	
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					LA-A551P	0.2
				Date	Tuesday, July 16, 2013	Sheet 20 of 40

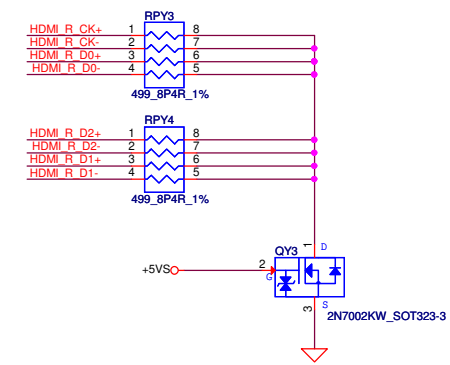
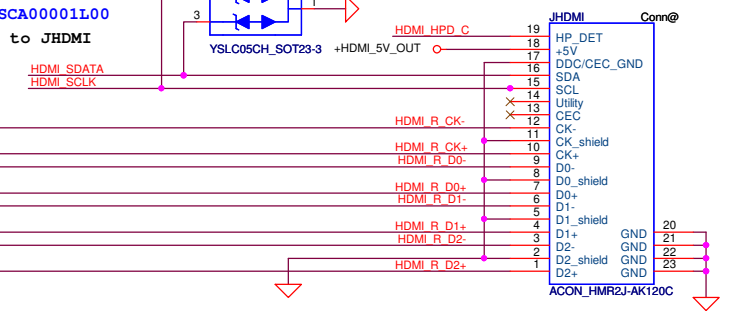


OE#	A	Y
L	L	L
L	H	H
H	X	Z



Main: SCA00000U10
2nd: SCA00001L00
Close to JHDMI

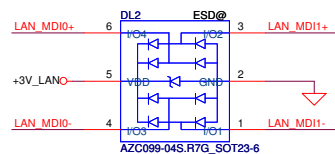
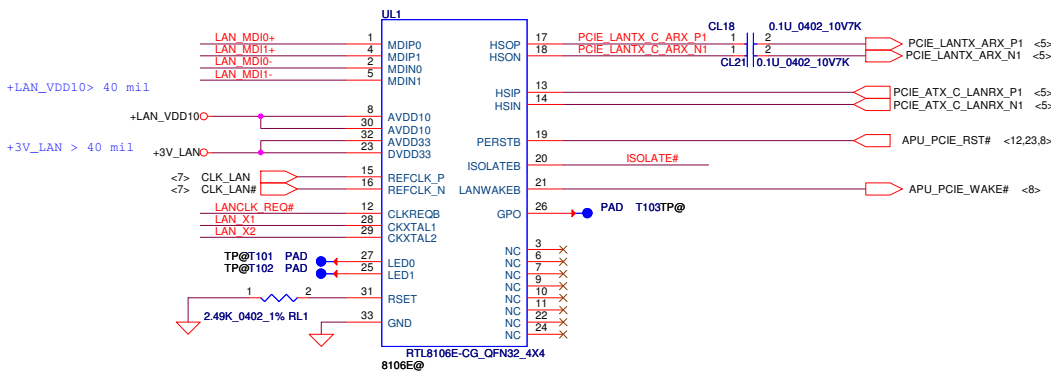
HDMI Connector



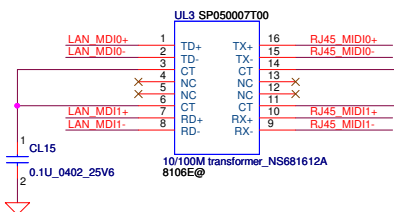
HDMI Royalty
RO0000003HMM
HDMI W/Logo + HDCP
HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HMM

please manually load
this virtual material to 45@ BOM

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2013/05/15		Deciphered Date		2015/09/27		Title	
										HDMI W/O CEC	
										LA-A551P	
										Date: Tuesday, July 16, 2013	
										Sheet 21 of 40	



main: SP050007T00
2nd: SP050007K00
3rd: SP050006H00



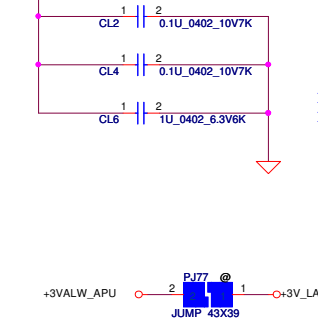
2013/5/3 EMI request change CL17 BOM structure to EMI@
2013/6/7 ESD request reserve DL14
2013/6/7 ESD request add DL5

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

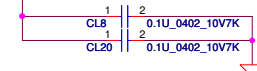
*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

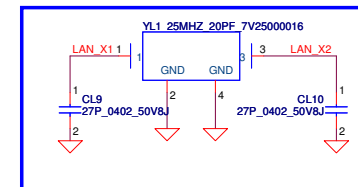
CL2,CL4 close to pin 8,30 respectively
CL6 close to pin 30



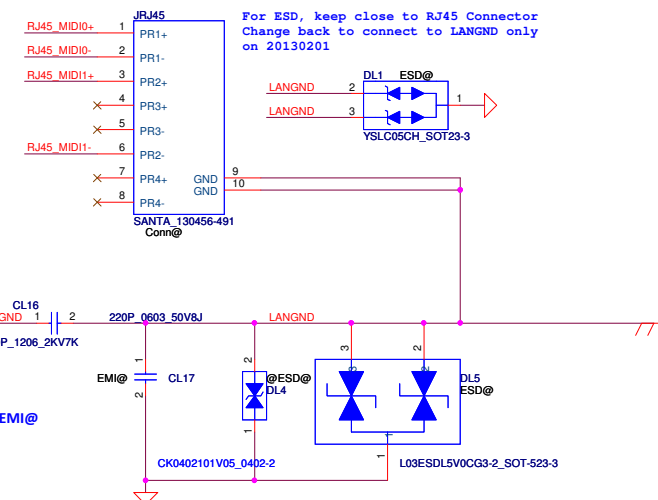
CL8 close to Pin32
CL20 close to Pin23



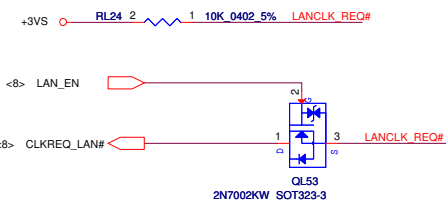
Keep de-coupling capacitors close to RTL8106E within 200 mil



For ESD, keep close to RJ45 Connector
Change back to connect to LANGND only on 20130201

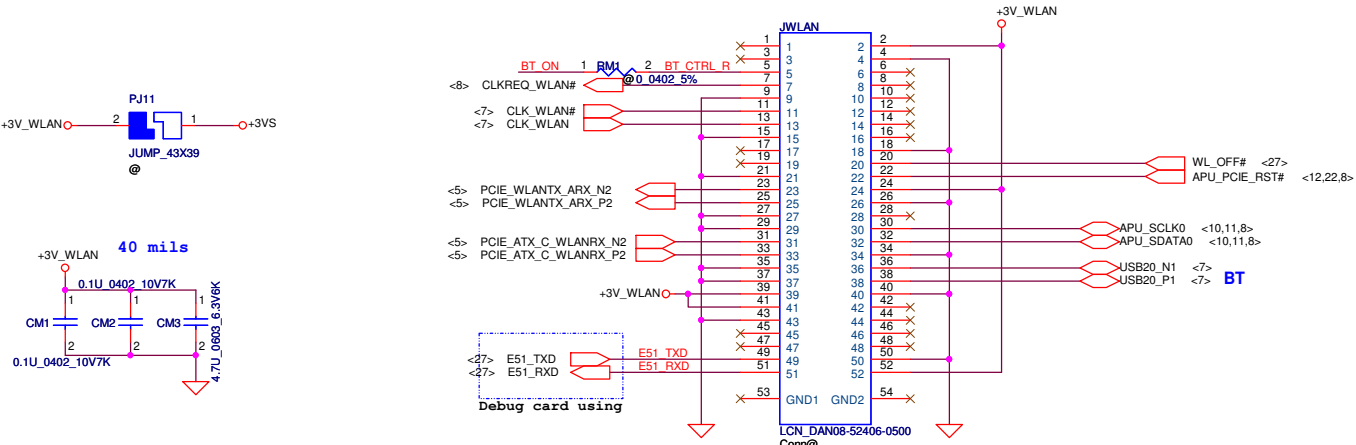


For LAN function



	Sx Enable Wake up	Sx Disable Wake up
WOL_EN#	LOW	HIGH

Slot 1 Half PCIe Mini Card-WLAN



WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L

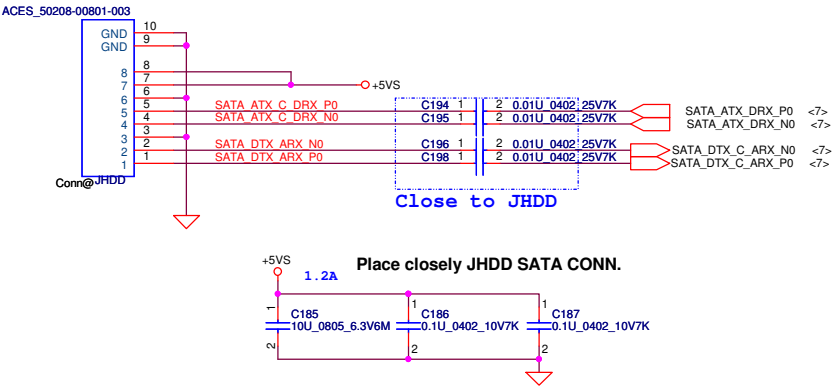
From EC

<27> BT_ON

BT_ON 1 RM2 2 E51_RXD 1K 0402 5%

For isolate BT_CTRL and
Compal Debug Card.

SATA HDD Conn.

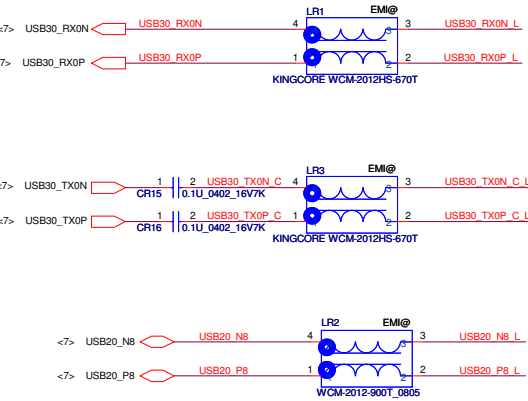


USB Sleep & Charge

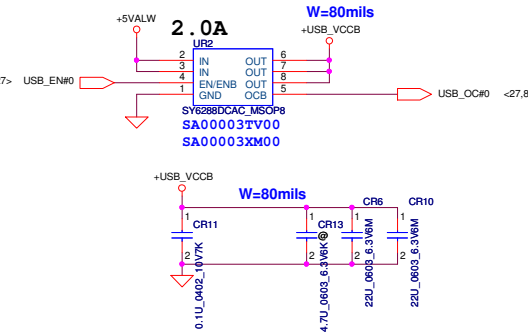
State table for TPS2546RTER

CB0	CB1	CB2	ILIM_SEL	Mode	STATUS
0	1	1	1	Auto/Alternate	Auto-detection charger mode for Apple device(2A,1A). Resistor dividers are connected to DP/DM. Including DCP
1	1	1	0	SDP	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	1	1	CDP	USB pass-through mode with CDP emulation. DP/DM are connected to TDP/TDM

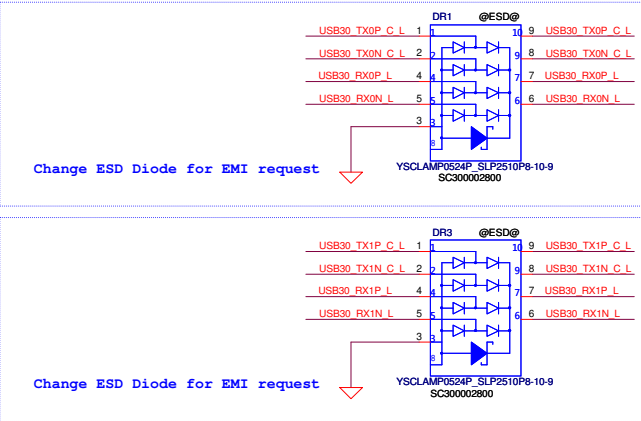
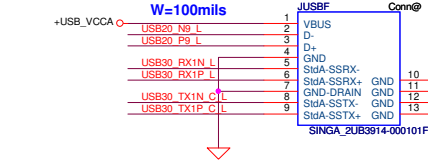
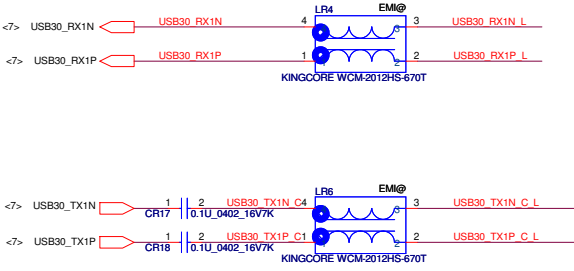
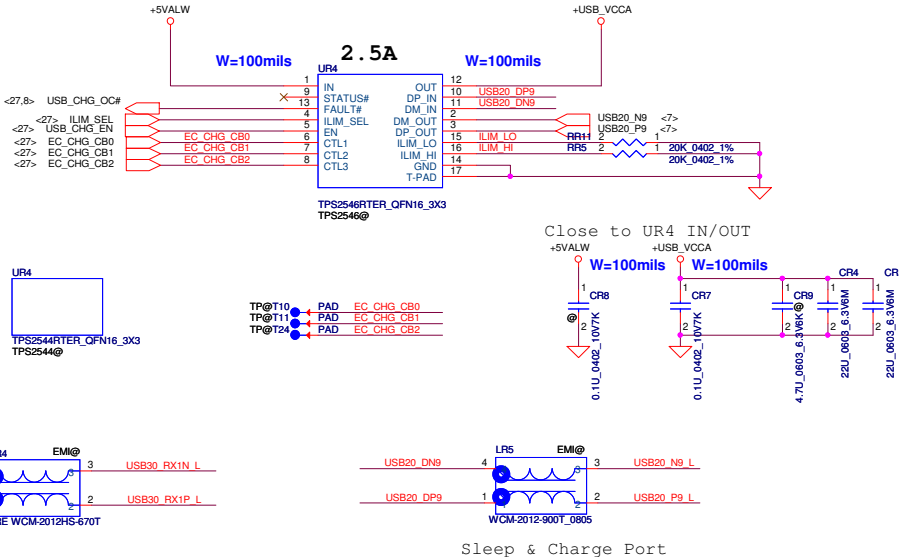
Right side USB 3.0 x 1



USB POWER SWITCH



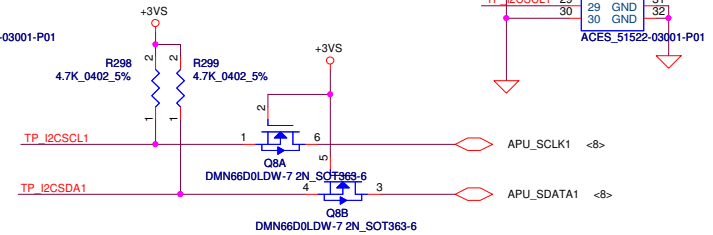
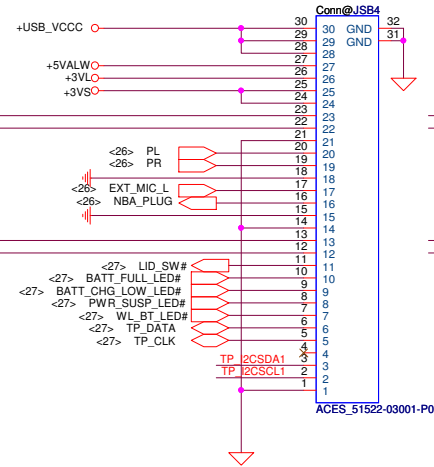
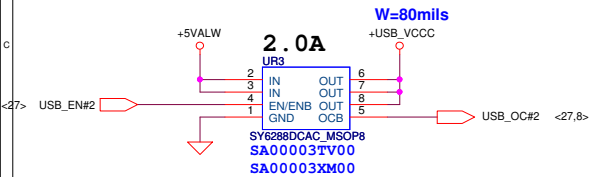
Right side USB 3.0 x 1 W/ Sleep&Charge



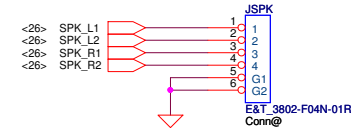
Small board Conn

Close to JSB5

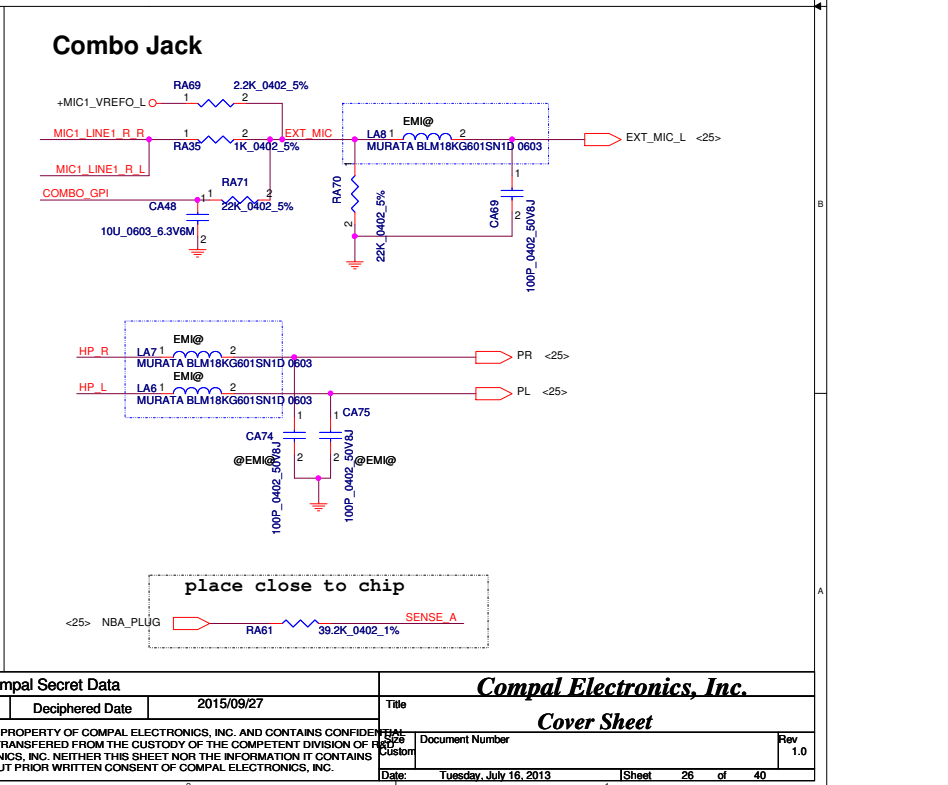
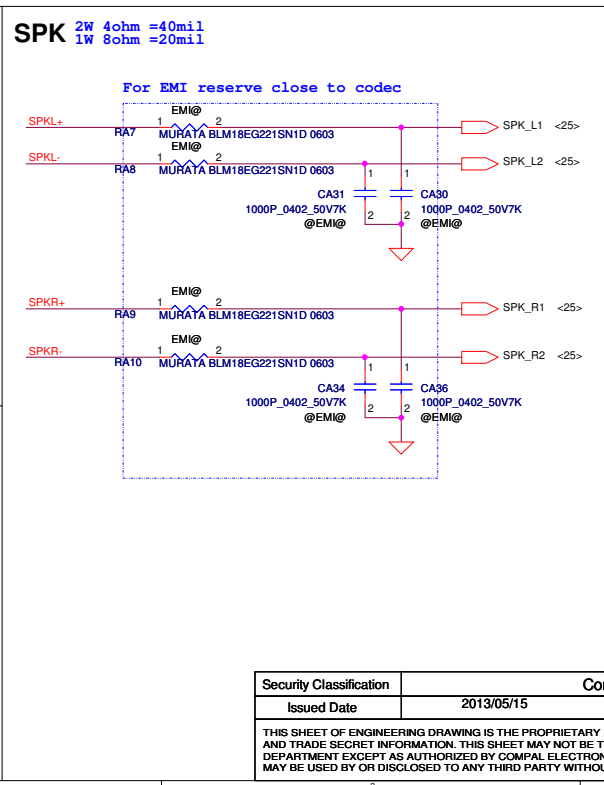
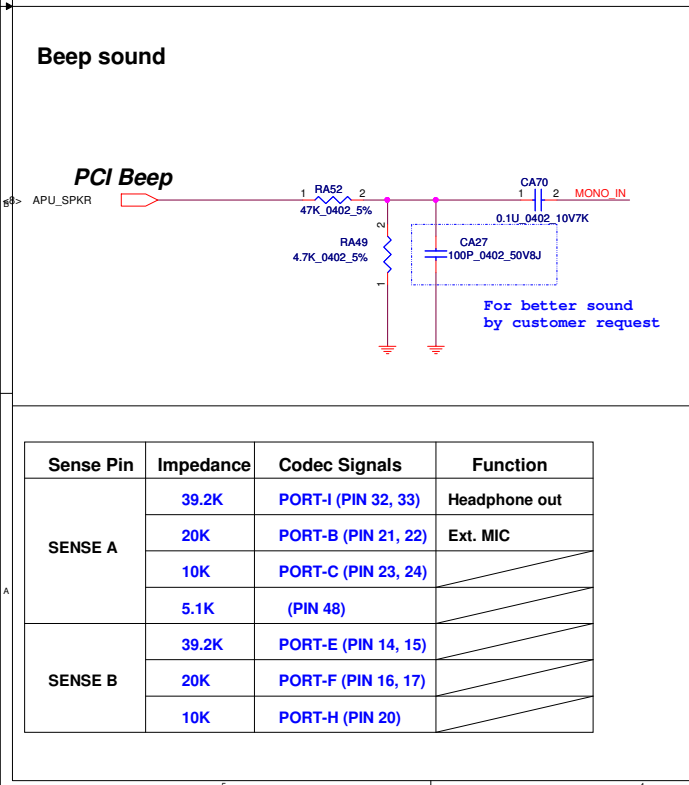
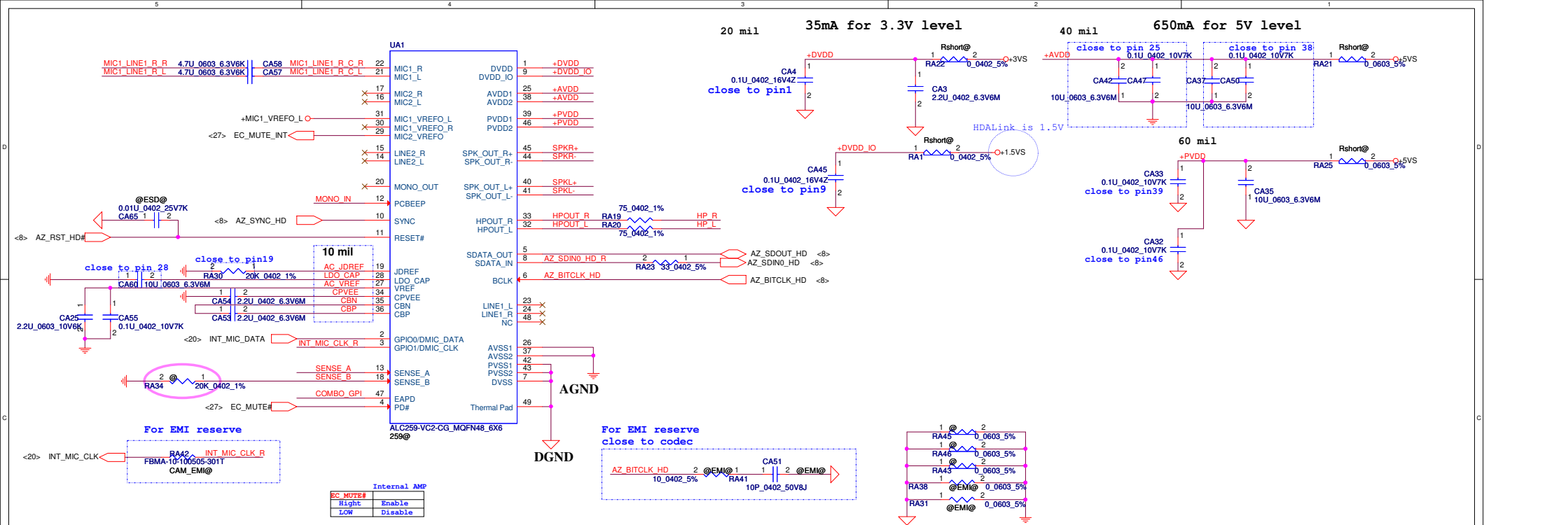
Left USB 2.0 x 1



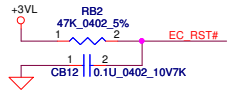
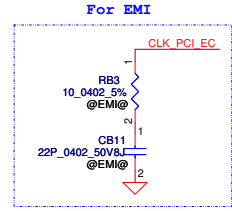
SPK Conn.



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				Custom	LA-A551P	1.0
				Date:	Tuesday, July 16, 2013	Sheet 25 of 40

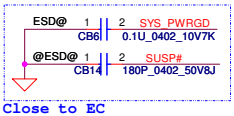
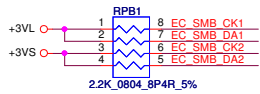


20130417 Note. 2013 ENE EC change version
A3 (SA000040B20) to A4 (SA000040B30)

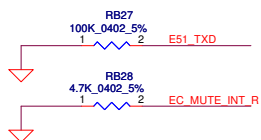


SMBUS1->BATT, Smart Charger
SMBUS2->G-Sensor, GPU Thermal Sensor,
APU Thermal Sensor

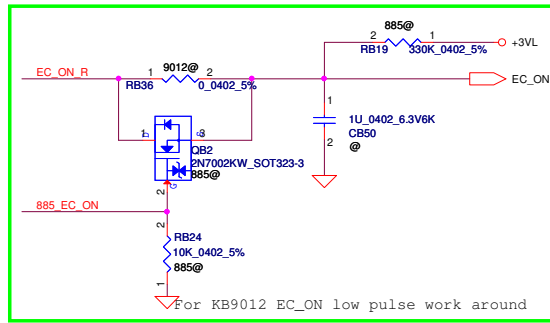
EC SMBus2 for S0, SMBus1 for S5



Close to EC



P.32_SYS_PWRGD OD/L
for 1.8V PU APU



For KB9012 EC_ON low pulse work around

PC & MISC

Int. K/B
Matrix

SPI Device Interface

SPI Flash ROM

SPI Bus

GPIO

GPI

GPIO

GPIO

GPIO

GPIO

GPIO

PWM Output

AD Input

DA Output

PS2 Interface

SPI Device Interface

SPI Flash ROM

GPIO

GPI

GPIO

GPIO

GPIO

GPIO

AD Input

DA Output

PS2 Interface

SPI Device Interface

SPI Flash ROM

GPIO

GPI

GPIO

GPIO

GPIO

GPIO

GPIO

AD Input

DA Output

PS2 Interface

SPI Device Interface

SPI Flash ROM

GPIO

GPI

GPIO

GPIO

GPIO

GPIO

GPIO

AD Input

DA Output

PS2 Interface

SPI Device Interface

SPI Flash ROM

GPIO

GPI

GPIO

GPIO

GPIO

GPIO

GPIO

AD Input

DA Output

PS2 Interface

SPI Device Interface

SPI Flash ROM

GPIO

GPI

GPIO

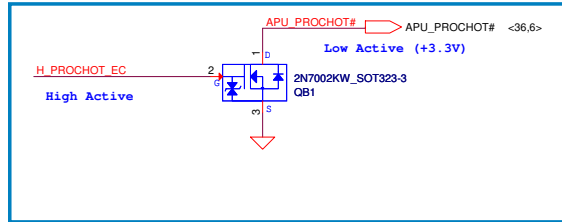
GPIO

GPIO

GPIO

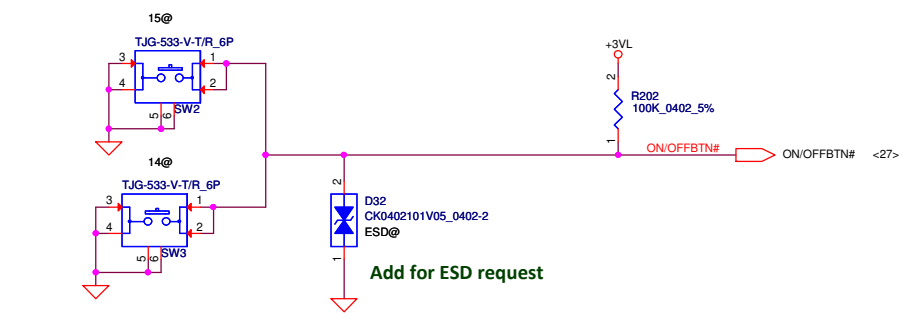
GPIO

Voltage Comparator Pins FOR 9012 A3			
VCIN0 pin109	>1.2V	<1.2V	
VCOUT0 pin104	HIGH	LOW	
VCOUT1 pin103	LOW	HIGH	

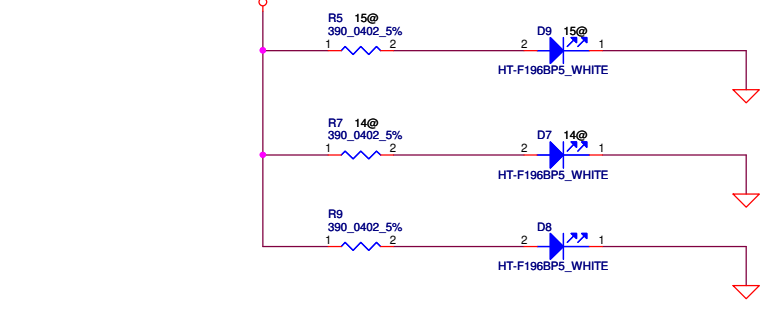


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2013/05/15				LPC-EC-KB9012			
Deciphered Date				2015/09/27				LA-A551P			
Title				20130417 Note. 2013 ENE EC change version				Rev 1.0			
Document Number				27				Tuesday, July 16, 2013			
Date				2013/05/15				Sheet 27 of 40			

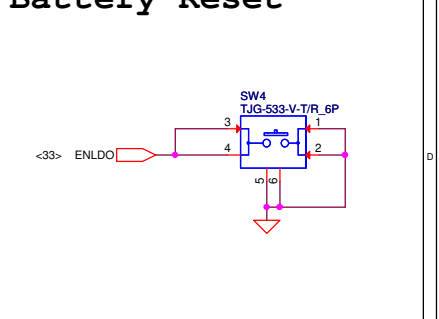
Power Button



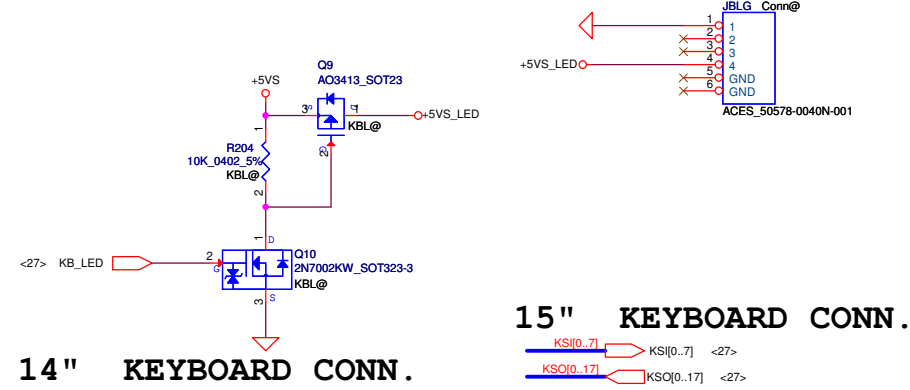
POWER LED



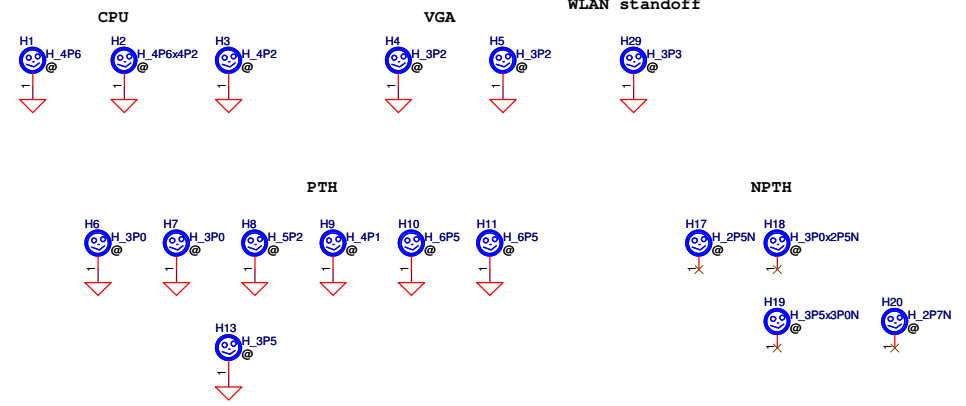
Battery Reset



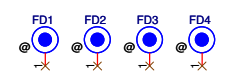
Keyboard LED



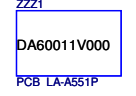
Screw Hole



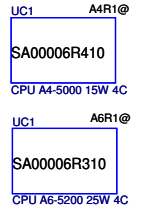
PCB Fedical Mark PAD



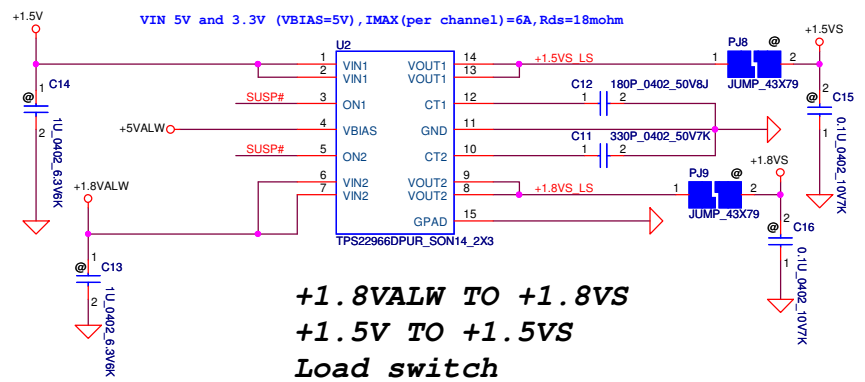
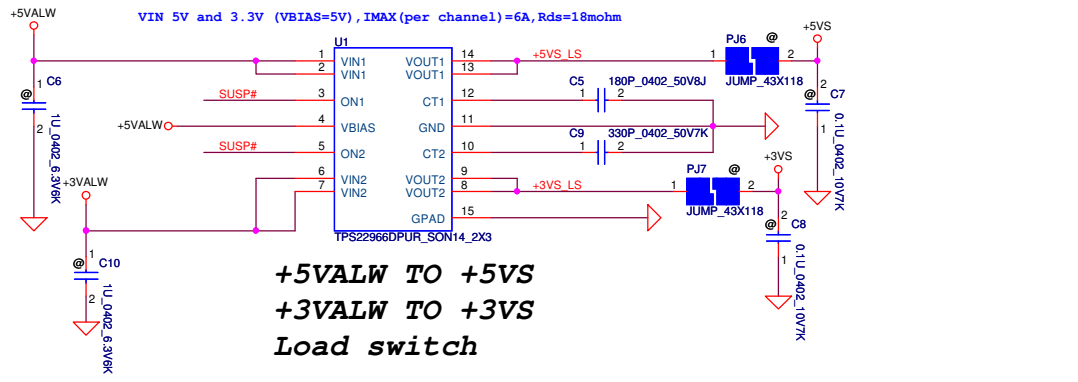
ISPD



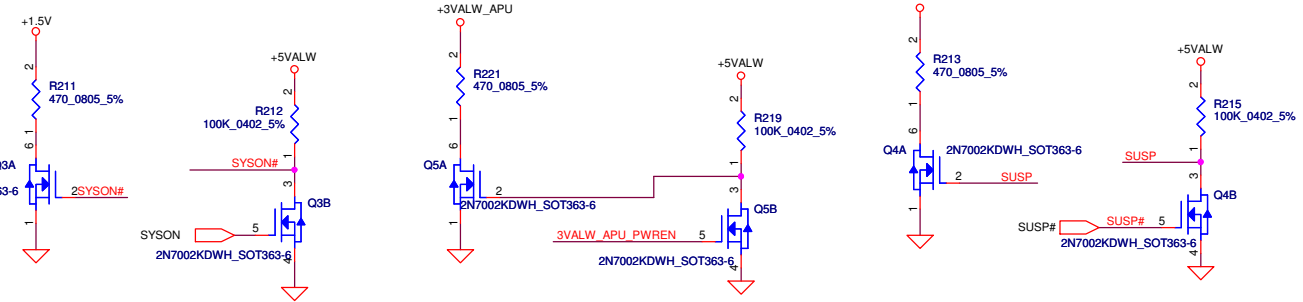
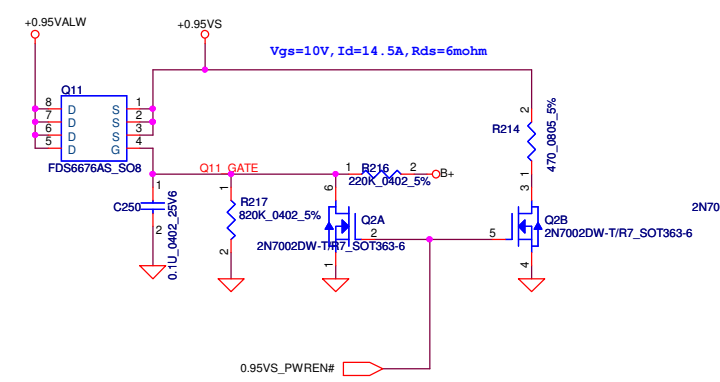
APU PR sample



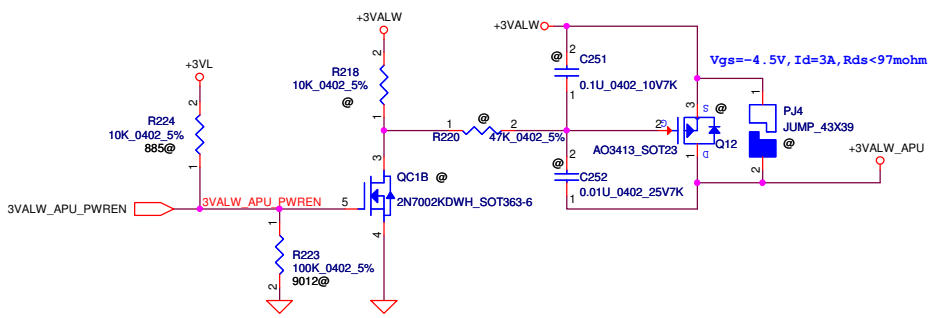
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/05/15	Deciphered Date	2015/09/27	Title	
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+0.95VALW to +0.95VS



+3VALW to +3VALW_FCH

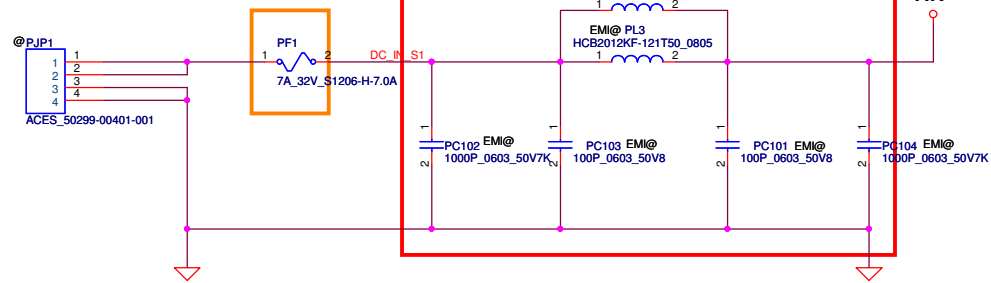


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				LA-A551P	
				Date	Tuesday, July 16, 2013
				Sheet	29 of 40

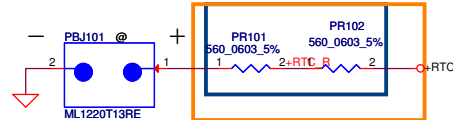
EMI Part (47.1)

Other component (37.1)

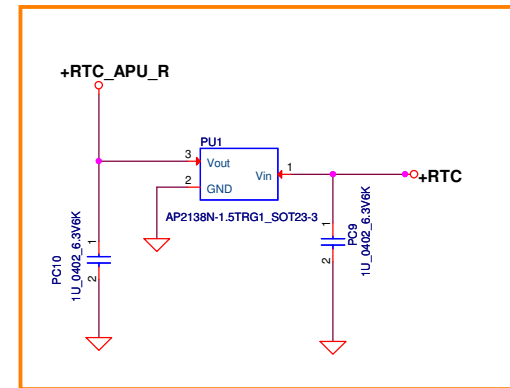
A51 need add fuse



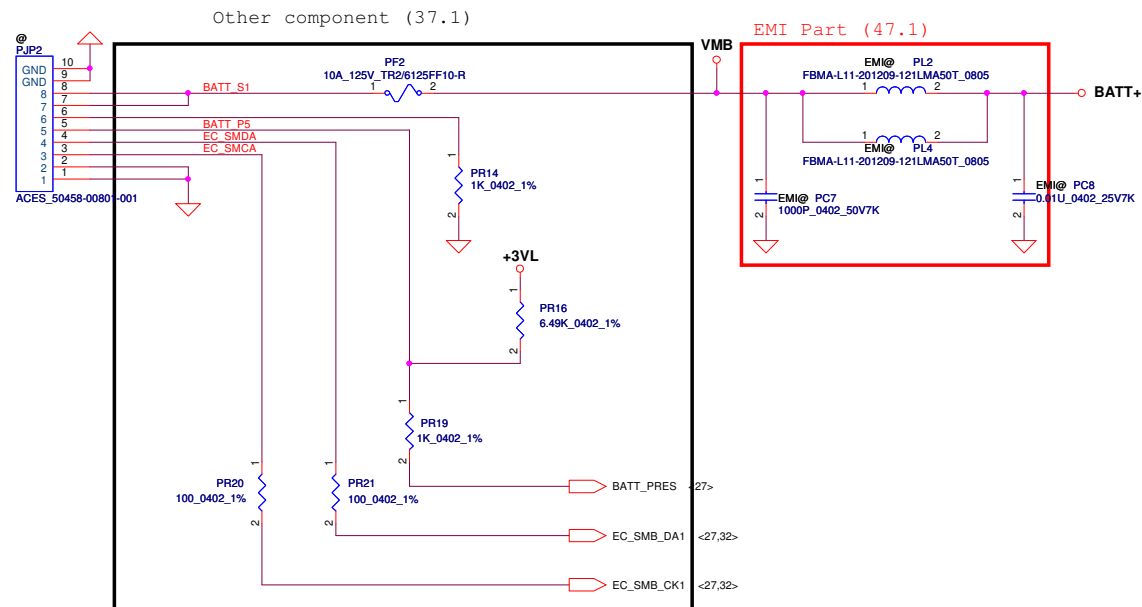
For ML1220 RTC (38.2)



For RTC (38.2)

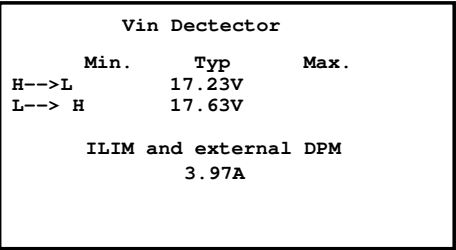


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Date:				Rev 0.1
Sheet 30 of 40				Document Number LA-A551P



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				Rev	0.1
				Sheet	31 of 40

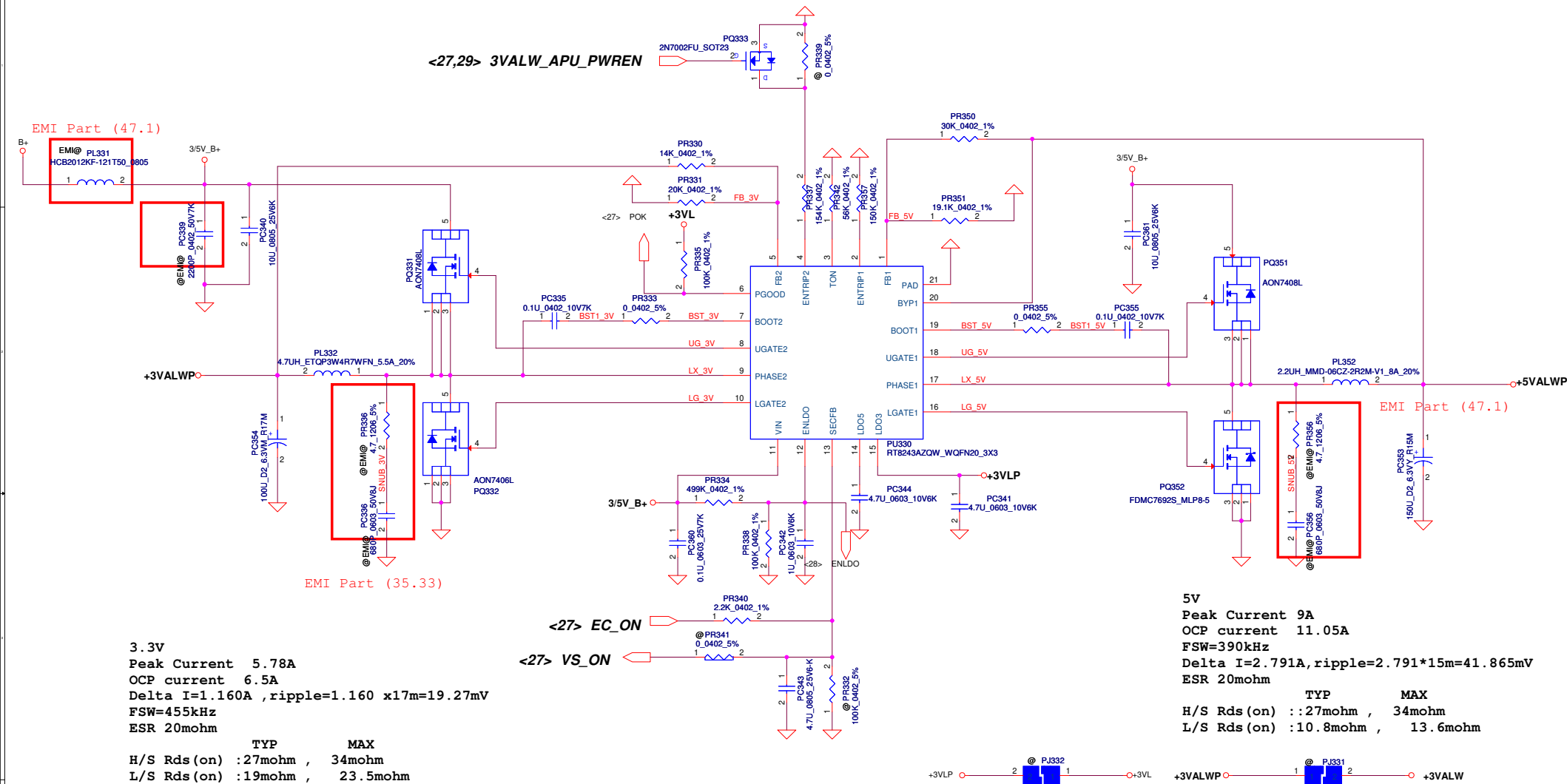
Charger controller (40.1), Support component (40.2)

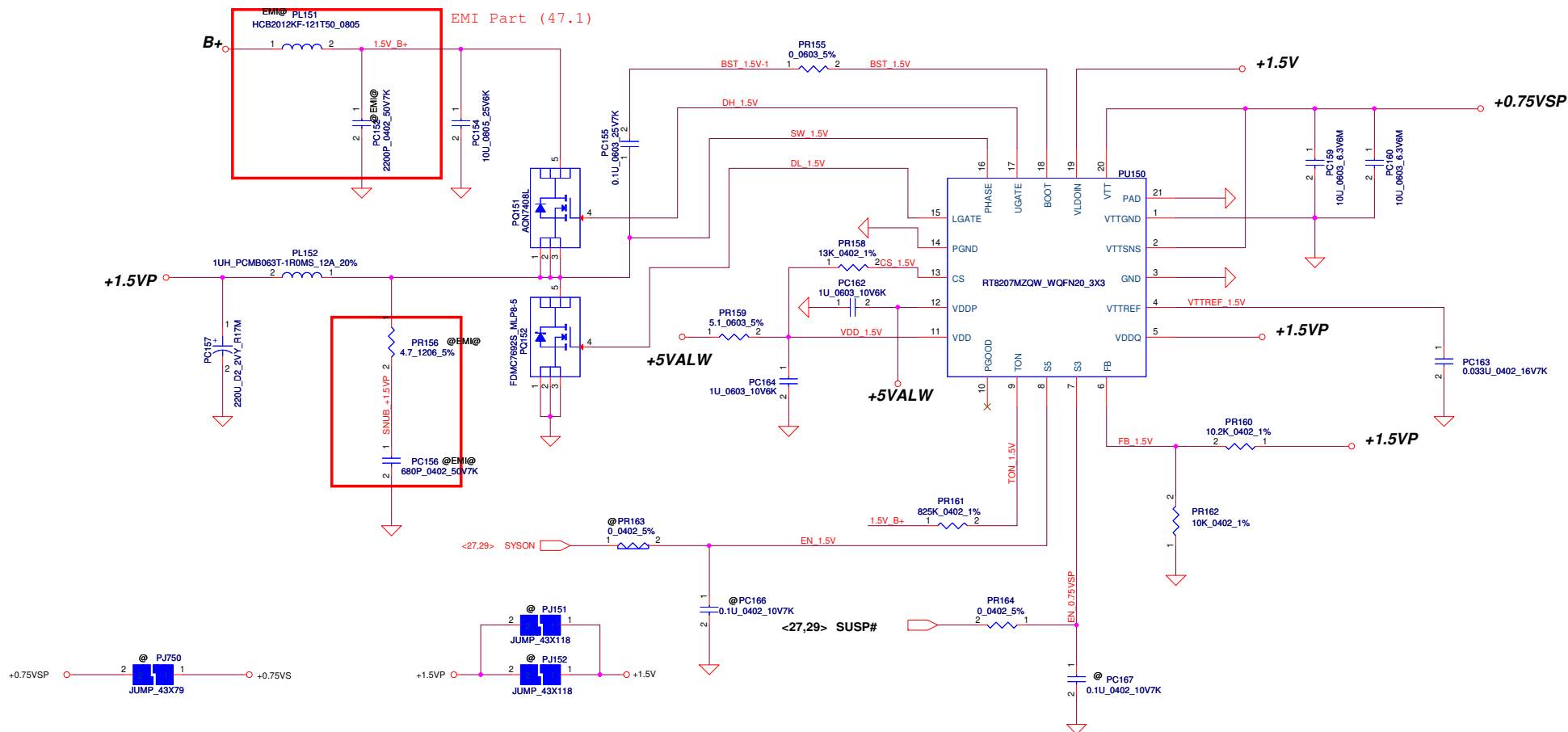


For A51 ADP_V function

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/09/27	Deciphered Date	2015/09/27	Title	CHARGER	
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				Custom	LA-A551P	0.1
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<27,29> 3VALW_APU_PWREN





1.5V
Peak Current 8.1A
OCP current 9.63A
FSW=500kHz
DCR 8.3 ~ 10mohm

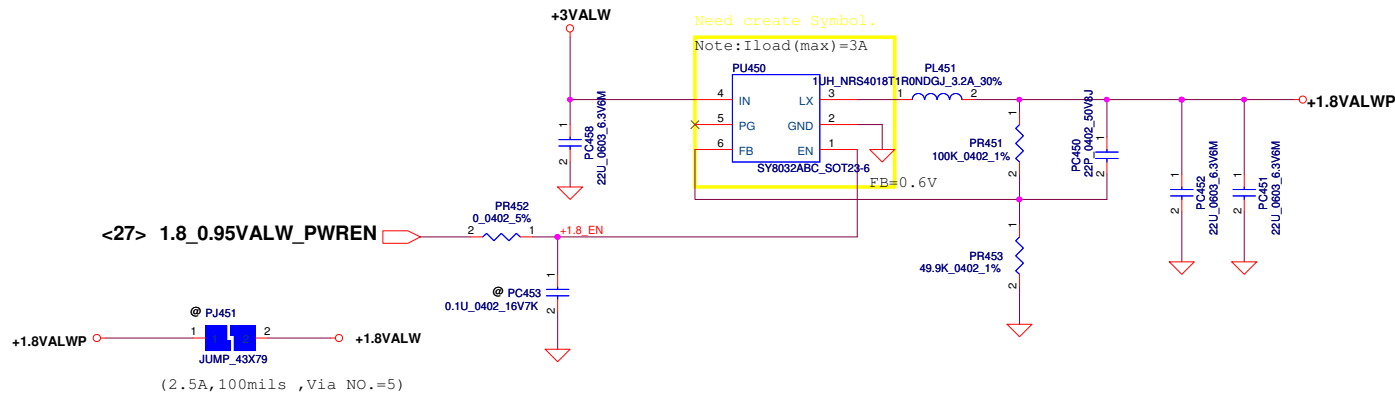
	TYP	MAX
H/S Rds(on)	: 27mohm	, 34mohm
L/S Rds(on)	: 10.8mohm	, 13.6mohm

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title	1.5VP/0.75VSP/1.8VSP	
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				Custom	LA-A551P	0.1
Date:	Sheet		34	of	40	

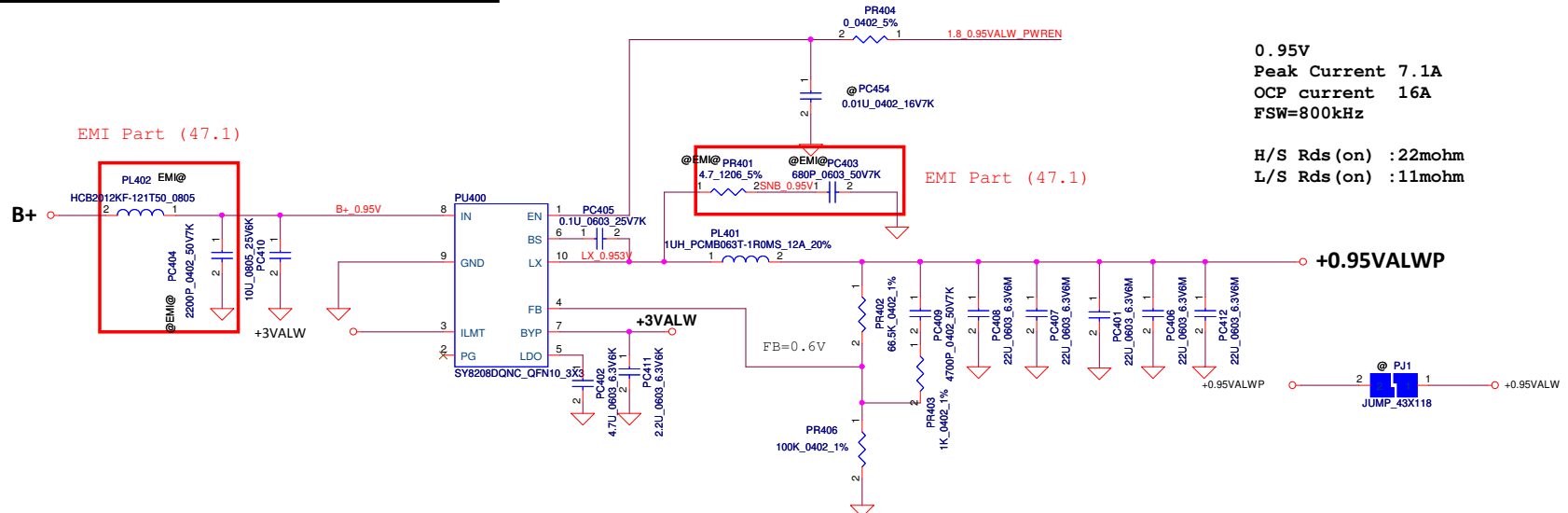
1.8V controller (35.15), Support component (35.16)



1.8V
Peak Current 2.5A
OCP current 3.5A
FSW=800kHz

H/S Rds(on) :100mohm ,
L/S Rds(on) :80mohm ,

0.95V controller (35.27), Support component (35.28)



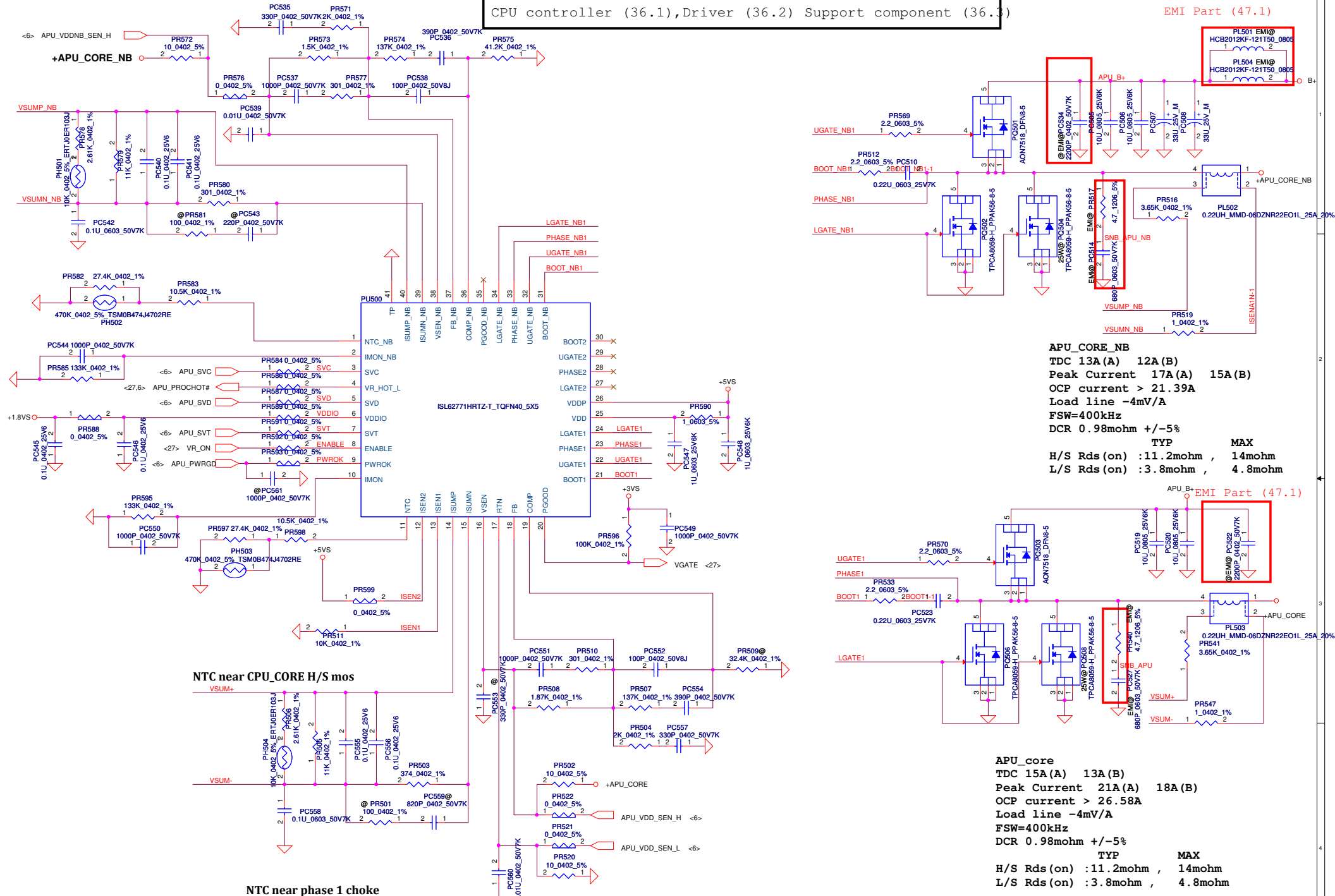
0.95V
Peak Current 7.1A
OCP current 16A
FSW=800kHz

H/S Rds(on) :22mohm
L/S Rds(on) :11mohm

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						Size		Document Number		ZRM AE		Rev 0.1	
						Custom							
						Date:		Tuesday, July 16, 2013		Sheet		35 of 40	

CPU controller (36.1),Driver (36.2) Support component (36.3)

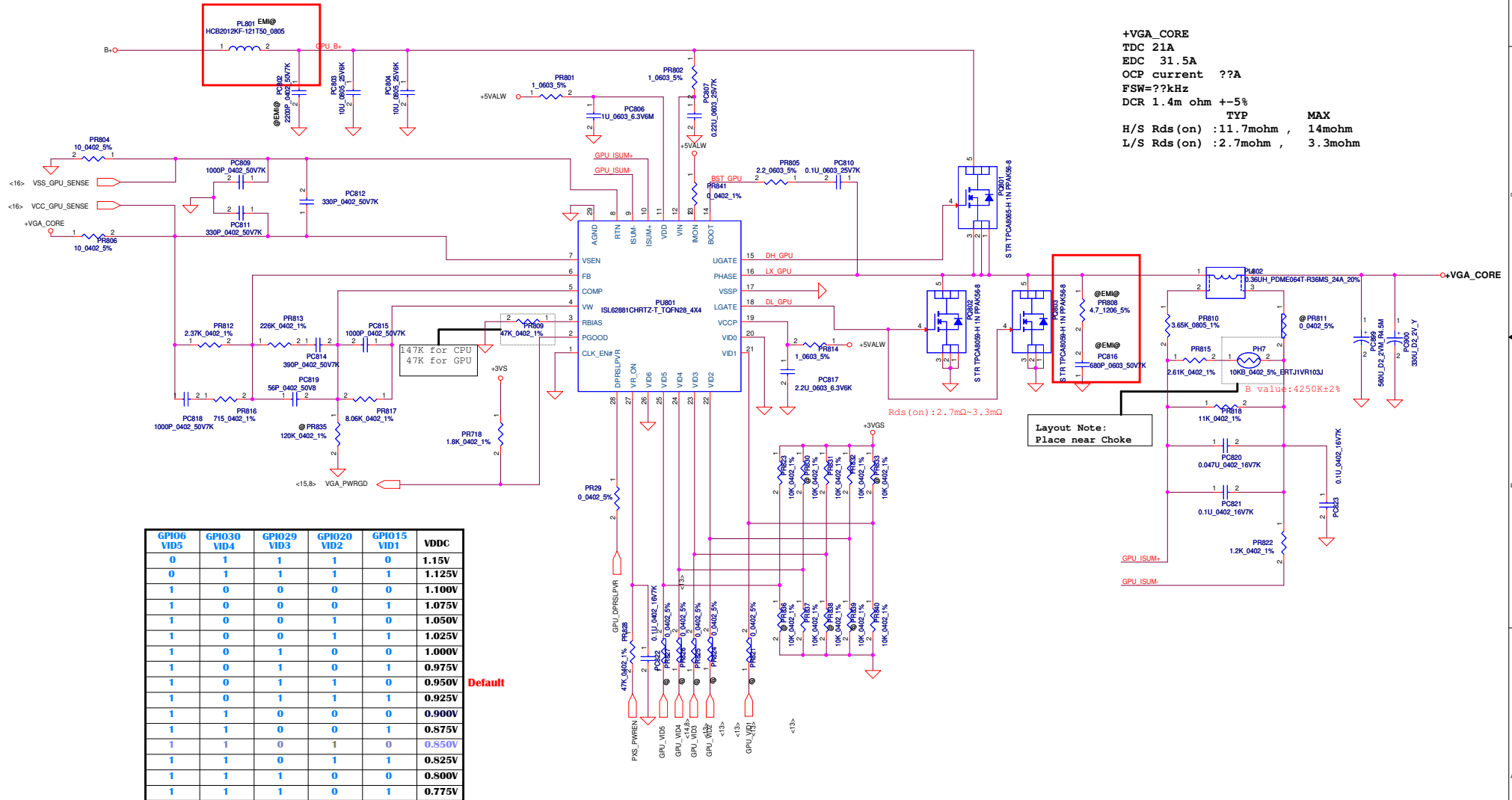
EMI Part (47.1)



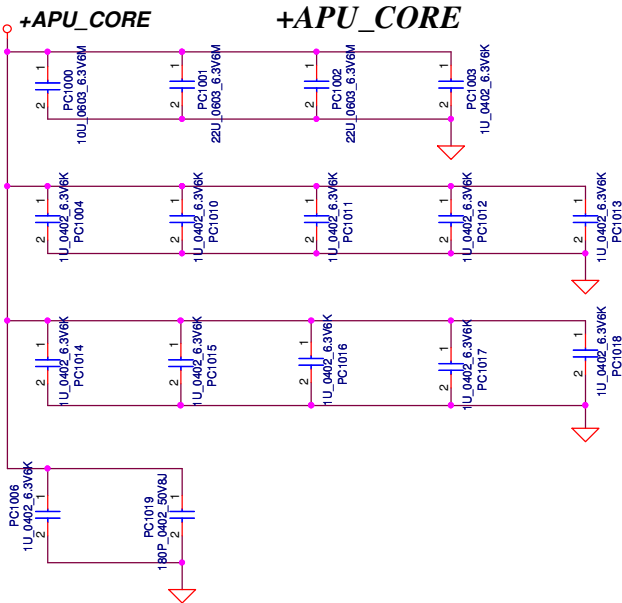
Security Classification		Compal Secret Data		Title	
Issued Date	2012/09/27	Deciphered Date		+CPU_CORE/VDDNB	
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				Date	Rev
				Tuesday, July 16, 2013	1.0
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VGA controller (43.1),Driver (43.2) Support component (43.3)

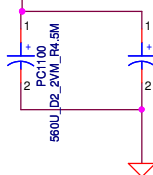
EMI Part (47.1)



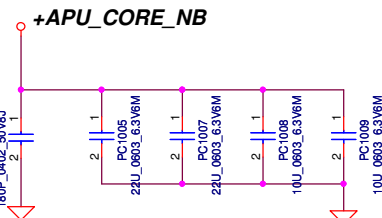
CPU_Core output CAP (Including MLCC) 36.4



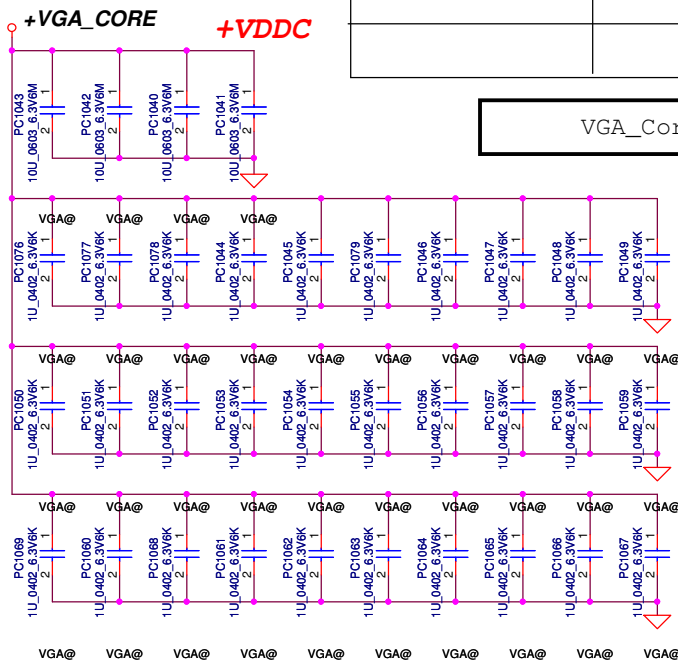
+APU_CORE



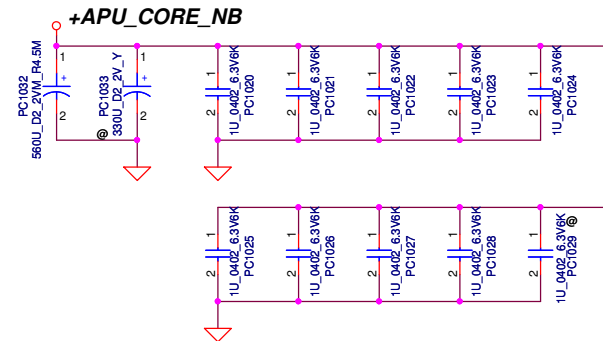
+APU_CORE_NB



+VGA_CORE



GFX output CAP (Including MLCC) 36.5



kABINI	560uF*4.5m	330uF	22uF (0603)	10uF (0603)	1u (0402)	180P (0402)
VDD	1	1	2	1	12	1
VDD_NB	1		2	2	9	1

VGA_Core output CAP (Including MLCC 43.9)

Version change list (P.I.R. List)

Page 1 of 1
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
------	-------------------	-----	-------------	------	-------

Item	Time (When)	Page (Where)	Location / Discription (How / What)	Request (Who)	for design change
1	DVT--2013/05/03	P32-PWR-CHARGER	PR248/Remove 10K	PWR	double count for parts
2	DVT--2013/05/03	P33-PWR-3VALW/5VALW	PR337 PR357/change to 107K 150K	PWR	For 3/5 V OCP Setting
3	DVT--2013/05/03	P34-PWR-+1.5VP/0.75VSP	PR158/ change to 15K	PWR	For 1.5 V OCP Setting
4	DVT--2013/05/03	P34-PWR-+1.5VP/0.75VSP	PC157 / change to 220U	PWR	for design change
5	DVT--2013/05/03	P34-PWR-+1.5VP/0.75VSP	PL152 / change PN	PWR	Common with PL401(1UH)
6	DVT--2013/05/03	P35-PWR_+1.8VALWP/+0.95VALWP	PR405 /Remove 10K	PWR	EC pull low 10k
7	DVT--2013/05/03	P36-PWR-CPU_CORE/VDDNBP	PQ504 PQ508 / Remove TPCA8059	PWR	For 15W APU
8	DVT--2013/05/07	P38-PWR-PROCESSOR DECOUPLING	PC1044,PC1045,PC1046,PC1047,PC1048, PC1049,PC1050,PC1051,PC1052,PC1053, PC1054,PC1055,PC1056,PC1057,PC1058, PC1059,PC1060,PC1061,PC1062,PC1063, PC1064,PC1065,PC1066,PC1067,PC1068, PC1069, PC1076, PC1077,PC1078,PC1079	PWR	Remove VGA MLCC
9	DVT--2013/05/07	P38-PWR-PROCESSOR DECOUPLING	PC1040,PC1041,PC1042,PC1043	PWR	Remove VGA MLCC
10	PVT--2013/06/10	P38-PWR-PROCESSOR DECOUPLING	PC1006/add 1U	PWR	for APU Transient test
11	PVT--2013/06/10	P38-PWR-PROCESSOR DECOUPLING	PC1001,PC1002/change 22U	PWR	for APU Transient test
12	PVT--2013/06/10	P38-PWR-PROCESSOR DECOUPLING	PC1101/change 330U	PWR	for APU Transient test
13	PVT--2013/06/10	P35-PWR_+1.8VALWP/+0.95VALWP	PC412/add 22U	PWR	for 0.95v Ripple
14	PVT--2013/06/10	P33-PWR-3VALW/5VALW	PC353 / change to 150U	PWR	for 3/5V design change
15	PVT--2013/06/10	P33-PWR-3VALW/5VALW	PC354 / change to 100U	PWR	for 3/5V design change
16	PVT--2013/06/10	P33-PWR-3VALW/5VALW	PC343/ add 4.7U	PWR	for 3/5V design change
17	PVT--2013/06/10	P36-PWR-CPU_CORE/VDDNBP	PC540 PC555/ change to 0.1U	PWR	for APU Transient test
18	PVT--2013/06/17	P33-PWR-3VALW/5VALW	PR337/change to 154K	PWR	for 3V OCP Setting
19	PVT--2013/06/17	P36-PWR-CPU_CORE/VDDNBP	PC538,PC552/ change to SE071101J80	PWR	SE068101K80 - X1 Code
20	PreMP--2013/07/15	P38-PWR-PROCESSOR DECOUPLING	PC1005 PC1007/change 22U	PWR	for APU_NB Transient test

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Size	Custom	Document Number	ZRMAE	Rev	1.0
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HW PIR (Product Improve Record)

ZEMAE LA-A551P SCHEMATIC CHANGE
LIST
REVISION CHANGE: 0.1 to 0.2

NO.	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	05/29	P24.	Delete RR2,RR3,RR7,RR6,RR12,RB7 for USB trace.	Part conut reduce
2.	05/29	P24.	Change CR13 to 0603.	HW4 Common design
3.	05/29	P24.	Delete SLP_CHG_CB0 & SLLP_CHG_CB1 from APU.	Reduce reserve
4.	05/29	P24,27,28.	EC_CHG_CB2(GPIO1A) move to GPIO12 ` ADD NUM_LED#(JKB5.1 to JUB1.36)	Design change
5.	05/30	P08.	Add QC2 and connect HDMI_HDP_N to HDMI_HDP.	For HDMI utility
6.	05/30	P08.	Delete T24,T25,T27	For RTC issue
7.	05/30	P08.	Add RC3 15K pull down and reserve RC12,RC16,RC17 pull +3VALW_APU and RC5,RC11 pull gnd.	For RTC issue
8.	06/03	P24.	Change CR3&CR2 47u 0805 to CR6&CR10 and CR4&CR5 22u 0603	For hight limit
9.	06/03	P10.	Change CD43 from 47u 0805 to CD43&CD44 22u*2 0603	For hight limit
10.	06/03	P09.	Change CC14 from 47u 0805 to CC14&CC16 22u*2 0603	For hight limit
11.	06/07	P22.	Reserve varistor DL14 for LANGND to DGND	For ESD request
12.	06/07	P22.	Add diode DL5 for LANGND to DGND	For ESD request
13.	06/07	P26.	Remove RA18 and RA24	Remove reserve 0 ohm
14.	06/07	P25.	Add C18 0.1uF 0402 on +USB_VCCC close to JSB5	For EMI request
15.	06/10	P20.	Change C17 form 1500P to 0.015uF	For LCD sequence
16.	06/10	P25.	Remove 0ohm for 14 and 15 and add LR10 and LR9	For part count reduce
17.	06/11	P26.	Change LA7 and LA6 form 0402 to 0603 size	For EMI request
18.	06/11	P25.	Swap LR7/LR8 pin1&4 and pin3&2	For layout smooth
19.	06/11	P24.	Add test point for S&C IC T10&T11&T24	For NPI debug
20.	06/13	P28.	Change H4&H5 form H_3P3 to H_3P2	For ME limite
21.	06/14	P21.	Colay RY4,RY5,RY6,RY7,RY8,RY9,RY10,RY11 with HDMI chock	For EMI request

ZEMAE LA-A551P SCHEMATIC CHANGE
LIST
REVISION CHANGE: 0.2 to 1.0

NO.	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	07/05	A11	Change R2,R130,RC116,RC117,RC119,RC120,R106,RA22,RA25,RA1,RA21,LA8 to shortpad	MP Part reduce
2.	07/05	P28	Delete SW5	Remove debug part
3.	07/05	P29	Reserve QC1B	Remove non-used part
4.	07/05	P06	Add APU_CRT_R/G/B pull 75ohm to GND	For disable CRT
5.	07/05	P08	Change CC31 form 10P to 8PF	XTRAL PPM fine tune
6.	07/08	P28	Change H20 screw hole to 2.7mm from 2.8mm	ME change
7.	07/08	P08	Add RC11 15K pull GND	AMD request
8.	07/08	P26	Change LA8 shortpad form 0402 to 0603	EMI request
9.	07/11	P28	Change C24 100pF cap to D32 100p varistor	ESD request
10.	07/15	P24	Update PCB footprint	DFB request

Title		
HW PIR		
Size	Document Number	Rev
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