Model Name : JE50-HR/SJV50-HR
Compal Project Name : P5WE0/P5WS0
File Name : LA-6902P

Compal Confidential

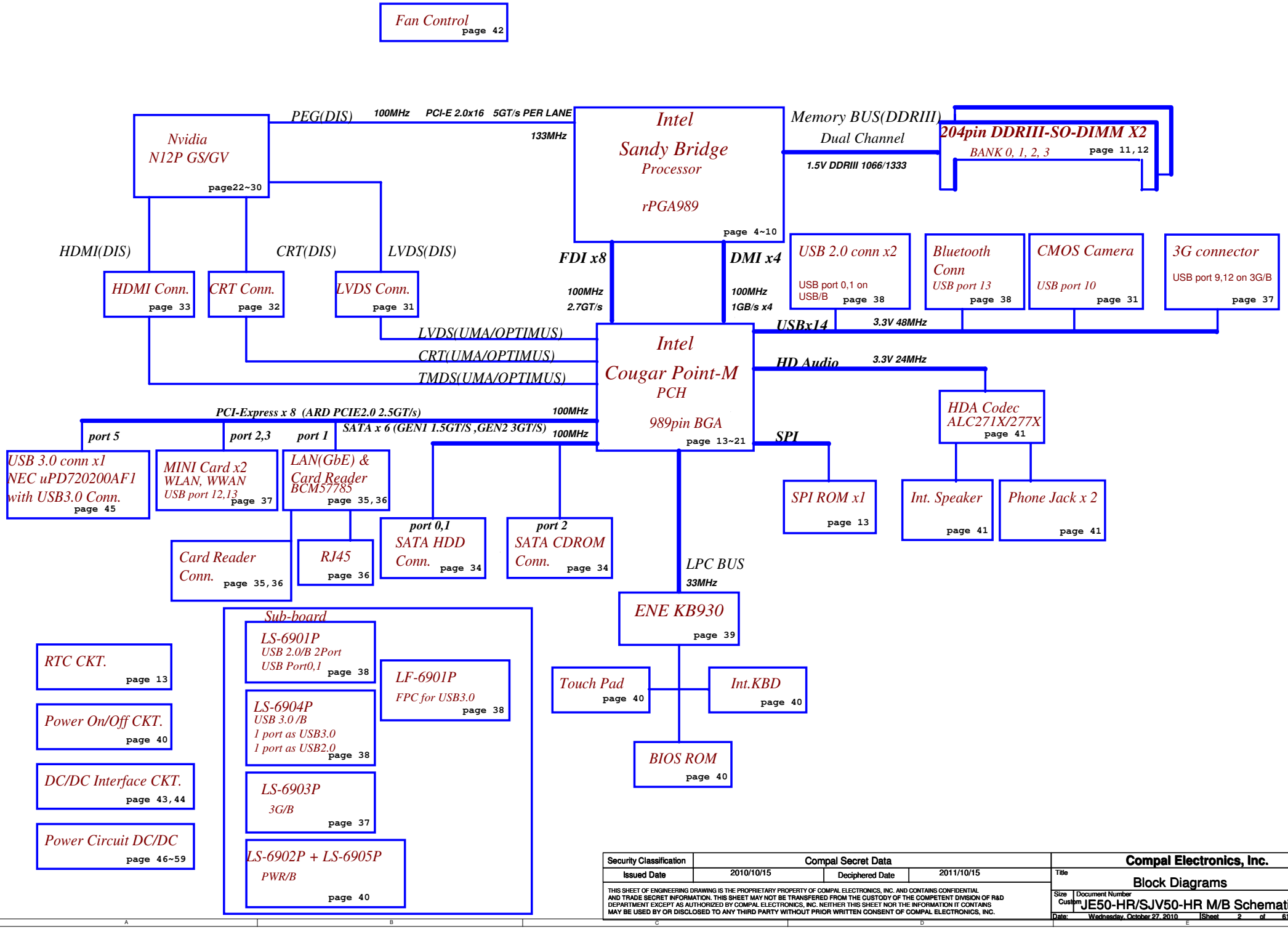
JE50-HR/SJV50-HR(P5WE0/P5WS0) M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
Nvidia N12P GS/GV

2010-10-19

REV:0.1

Compal Electronics, Inc.			
Title: Cover Page			
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: 0.4
Date: Wednesday, October 27, 2010	Sheet 1 of 61		



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Title: Block Diagrams

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

3G & BT & USB30 & USB20 Config

3G SKU: 3G@ USB30 SKU: USB30@ OPTMIUS SKU: OPT@

BT SKU: BT@ USB20 SKU: USB20@ Non-OPTMIUS SKU: NOPT@

LAN Chip A0 version: A0@ N12P-GS: GS@

LAN chip B0 Version: B0@ N12P-GV: GV@

BOM Config

UMA Only: BT@/3G@/USB30@/UMA@/UMAO@/NOPT@/A0@

OPTIMUS(N12P-GS): BT@/3G@/USB30@/UMA@/DIS@/X76@/OPT@/A0@/GS@

DIS Only(N12P-GS): BT@/3G@/USB30@/DISO@/DIS@/X76@/NOPT@/A0@/GS@

OPTIMUS(N12P-GV): BT@/3G@/USB30@/UMA@/DIS@/X76@/OPT@/A0@/GV@

DIS Only(N12P-GV): BT@/3G@/USB30@/DISO@/DIS@/X76@/NOPT@/A0@/GV@

VRAM P/N :

64*16

Samsung : SA000035700

Hynix : SA000032400/SA0000324C0

128*16

Samsung : SA00003MQ40

Hynix : SA00003VS00

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

EVT
EVT2
DVT
PVT
Pre-MP

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
UMA with OPTIMUS	UMA@
Dis with OPTIMUS	DIS@
DIS Only	DISO@
OPTIMUS	OPT@
Non-OPTIMUS	NOPT@
3G	3G@
Blue Tooth	BT@
USB2.0	USB20@
USB3.0	USB30@
VRAM	X76@
Connector	CONN@
Unpop	@
LAN Chip A0 version	A0@
LAN Chip B0 version	B0@
N12P-GS	GS@
N12P-GV	GV@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB/B (Right Side)
	UHCI1	2	USB3.0 colay USB2.0 Conn.
		3	USB/B Colay USB3.0
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card 1(WLAN)
		9	3G/B(WWAN)
	UHCI5	10	Camera
		11	Mini Card 2(Reserved)
	UHCI6	12	3G/B(SIM Card)
		13	BlueTooth

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Compal Electronics, Inc.

Title: Notes List

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ZZZ
DA60000KC00

JCPU1A

DMI

Intel(R) FDI

PCI EXPRESS* - GRAPHICS

eDP

Sandy Bridge_rPGA_Rev0p61
CONN@

+1.05VS_VTT

R517
24.9_0402_1%

PEG_COMP

PEG_ICOMPI and PEG_RCOMPO signals should be shorted and routed,
max length = 500 mils,trace width=4mils
PEG_ICOMPO signals should be routed with - max length = 500 mils,trace width=12mils
spacing =15mils

PEG_GTX_HRX_N[0..15] 22
PEG_GTX_HRX_P[0..15] 22
PEG_HTX_C_GRX_N[0..15] 22
PEG_HTX_C_GRX_P[0..15] 22

+1.05VS_VTT

R145
24.9_0402_1%

EDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls,
Trace Width for EDP_COMPIO=4mils,
EDP_ICOMPO=12mils,
and both length less than 500 mils...
should not be left floating
,even if disable eDP function...

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

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Issued Date	2010/10/15	Deciphered Date	2011/10/15

Title	PROCESSOR(1/7) DMI,FDI,PEG		
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: 0.4
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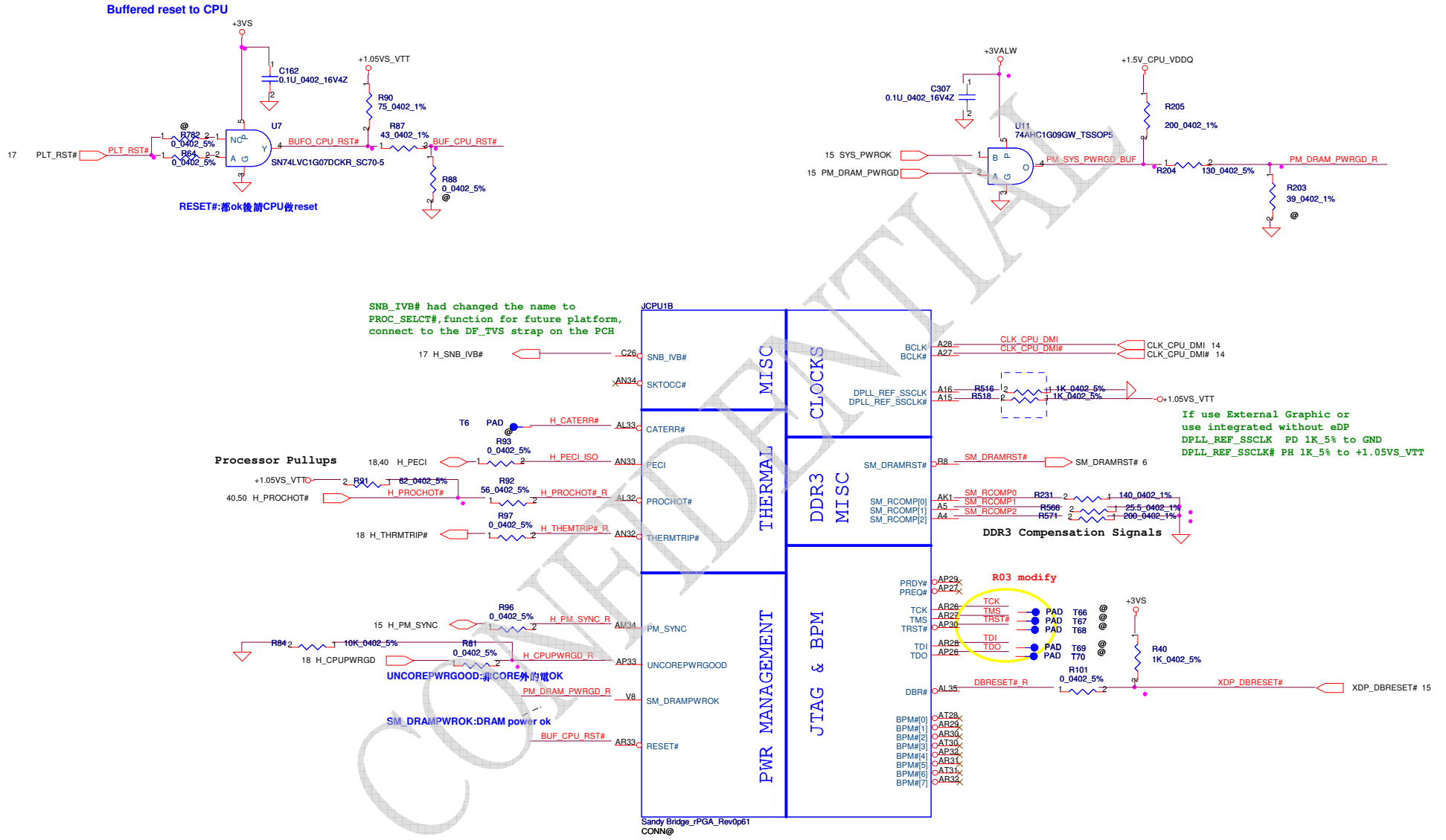


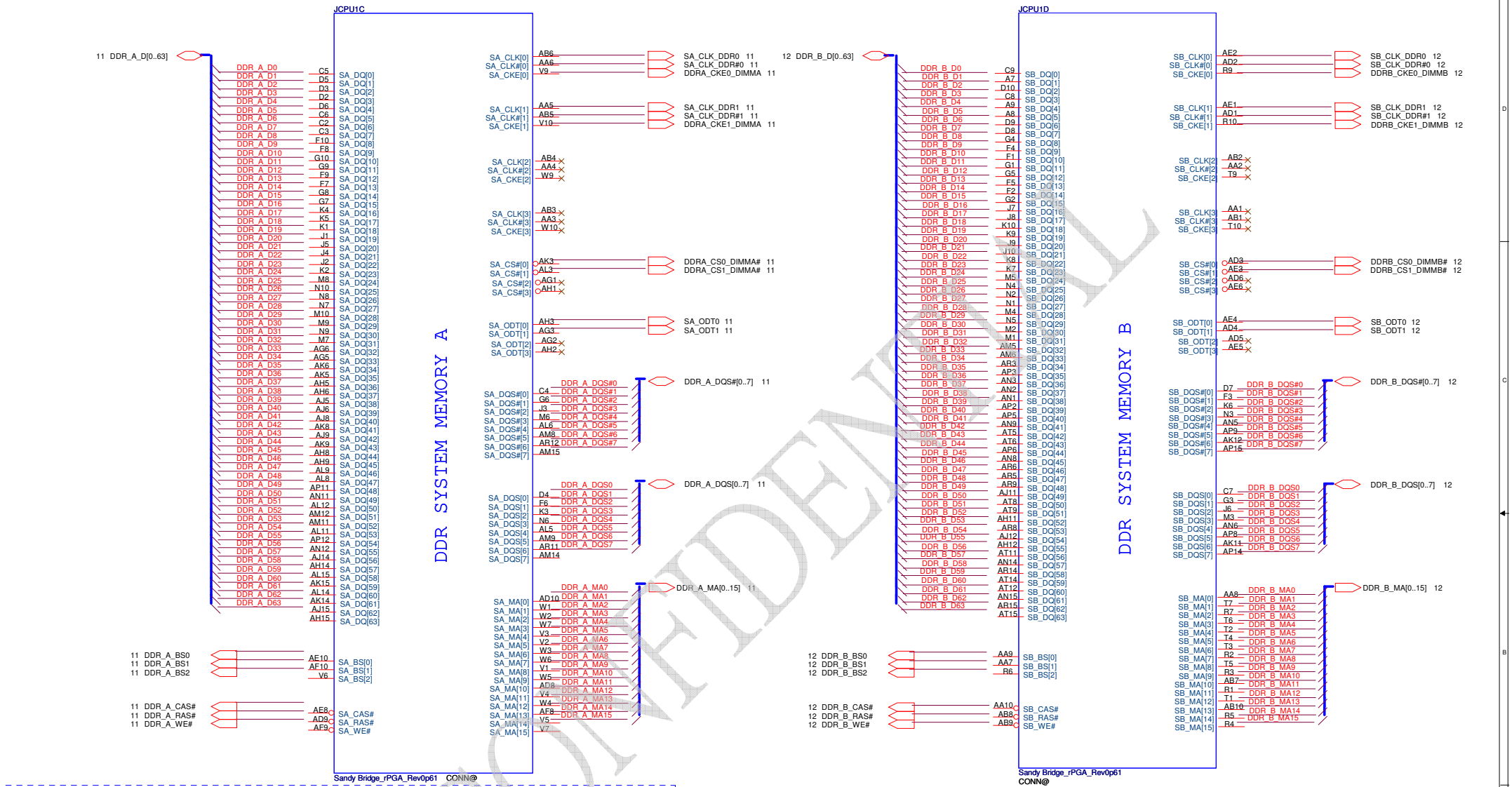
Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

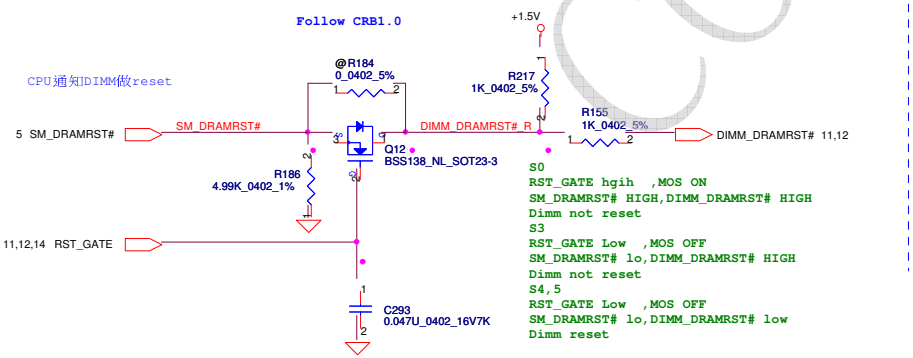
Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

Date: Wednesday, October 27, 2010 | Sheet 5 of 61





Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

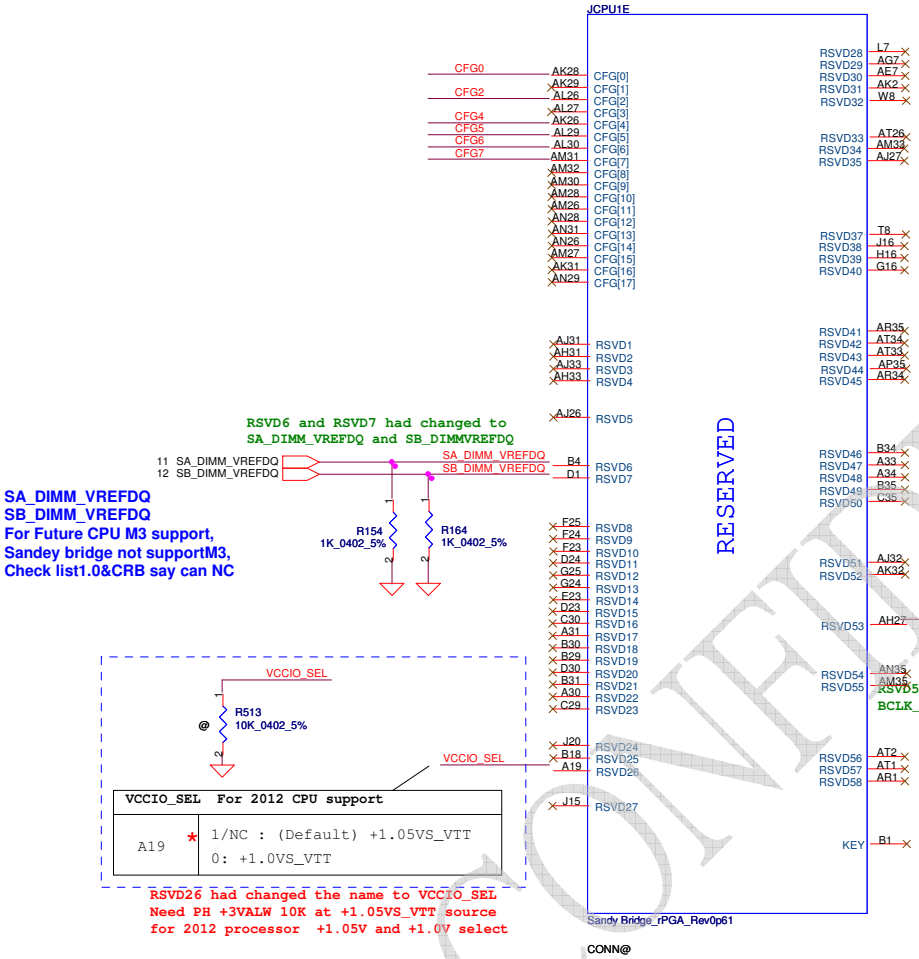
Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

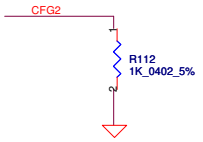
Size	Document Number	Rev
Custom	JE50-HR/SJV50-HR M/B Schematics	0.4

Date: Wednesday, October 27, 2010 Sheet 6 of 61

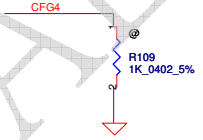
CFG Straps for Processor



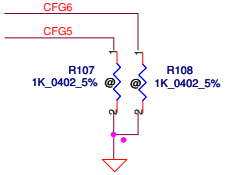
VCCIO_SEL For 2012 CPU support		
A19	*	1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT



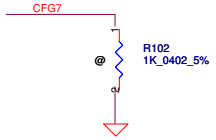
PEG Static Lane Reversal - CFG2 is for the 16x		
CFG2	*	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap		
CFG4	*	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps		
CFG[6:5]	*	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

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POWER

SV type CPU

QC 94A
DC 53A

JCPU1F

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

8.5A

+CPU_CORE

INTEL Recommend
4*470uF,16*22uF and 10*10uF
from PDDG 1.0

Follow Power Suggestion ,
place 3-pin Cap for CPU_CORE

PAW00
use 470uF*2
330uF*3

+1.05VS_VTT

INTEL Recommend
2*330uF,12*22uF
from PDDG 1.0

R02 modify

ME interefer,not pop!!

H_CPU_SVIDALRT#
H_CPU_SVIDCLK
H_CPU_SVIDDAT

VIDALERT#
VIDSCLK
VIDSOUT

VR_SVID_ALRT# 55
VR_SVID_CLK 55
VR_SVID_DAT 55

Place the PU
resistors close to VR

Place the PU
resistors close to CPU

VCCSENSE_R
VSSSENSE_R

VCC_SENSE
VSS_SENSE

VCCSENSE 55
VSSSENSE 55

VSSIO_SENSE
VCCIO_SENSE 53

VSS_SENSE
change to
VSS_SENSE_VCCIO

Should change to connect form
power cirucit & layout differential
with VCCIO_SENSE.

Sandy Bridge rPGA_Rev0p61

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

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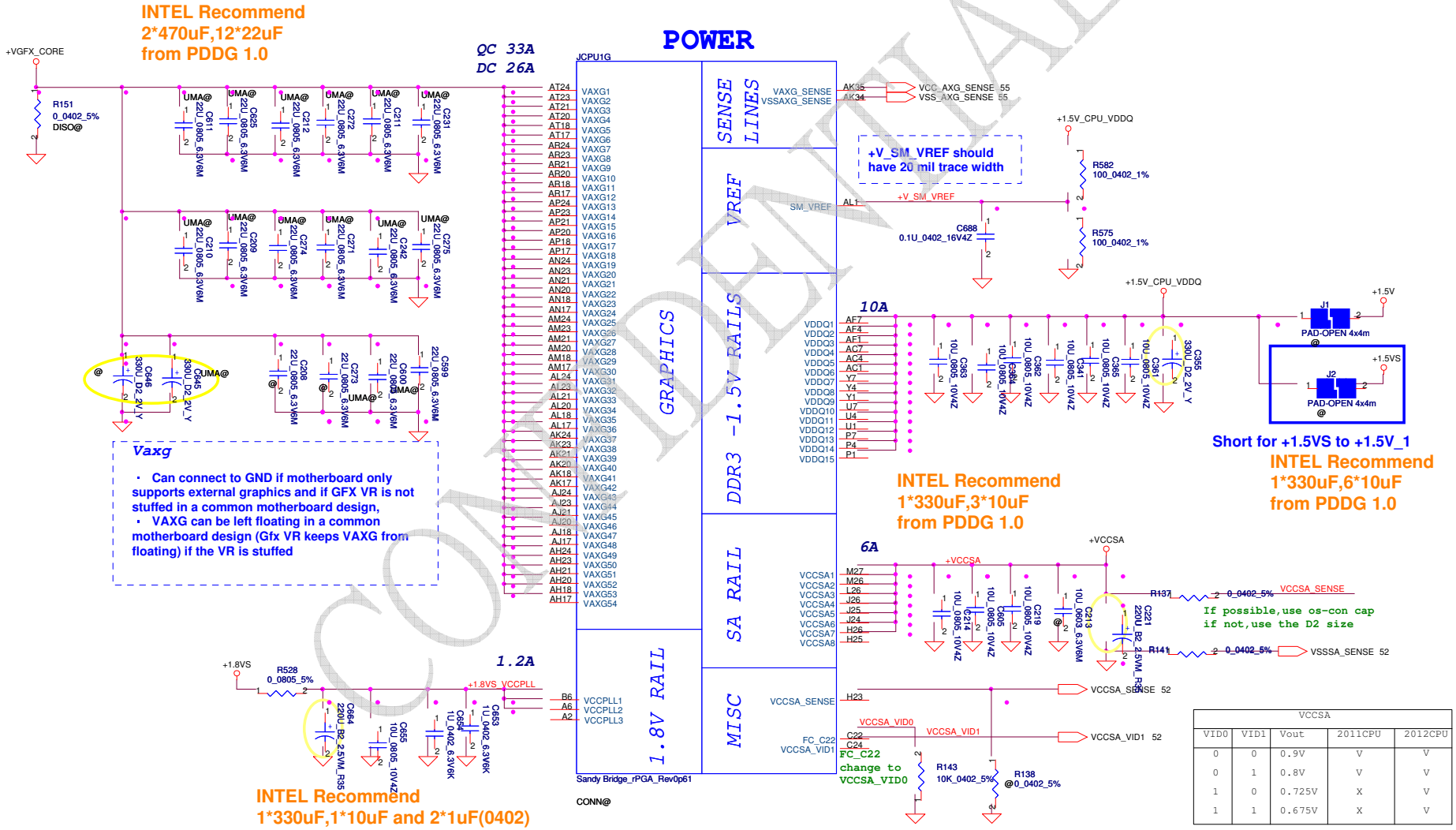
POWER



VCCSA				
VID0	VID1	Vout	2011CPU	2012CPU
0	0	0.9V	V	V
0	1	0.8V	V	V
1	0	0.725V	X	V
1	1	0.675V	X	V

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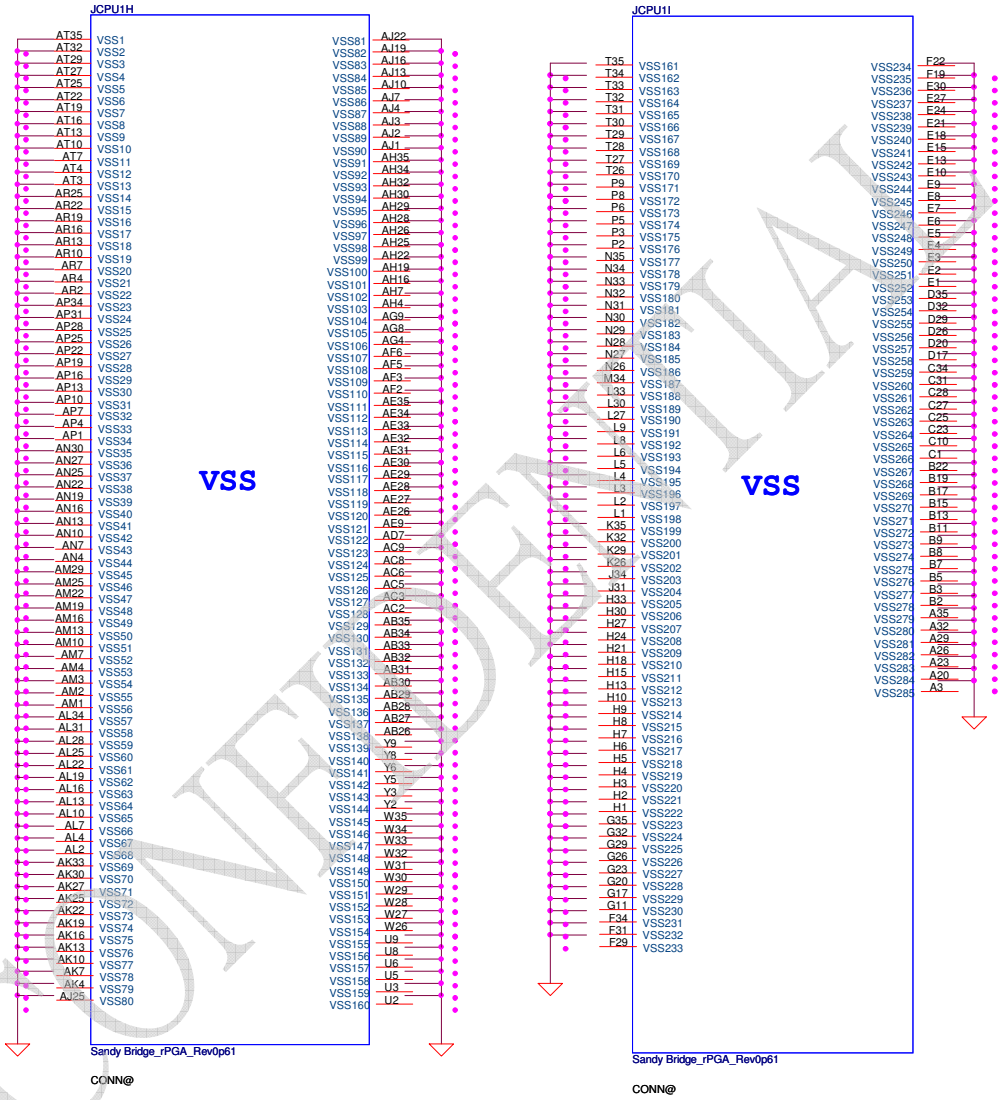
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.			
Title: PROCESSOR(6/7) PWR			
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: 0.4
Date: Wednesday, October 27, 2010		Sheet 9 of 61	



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Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

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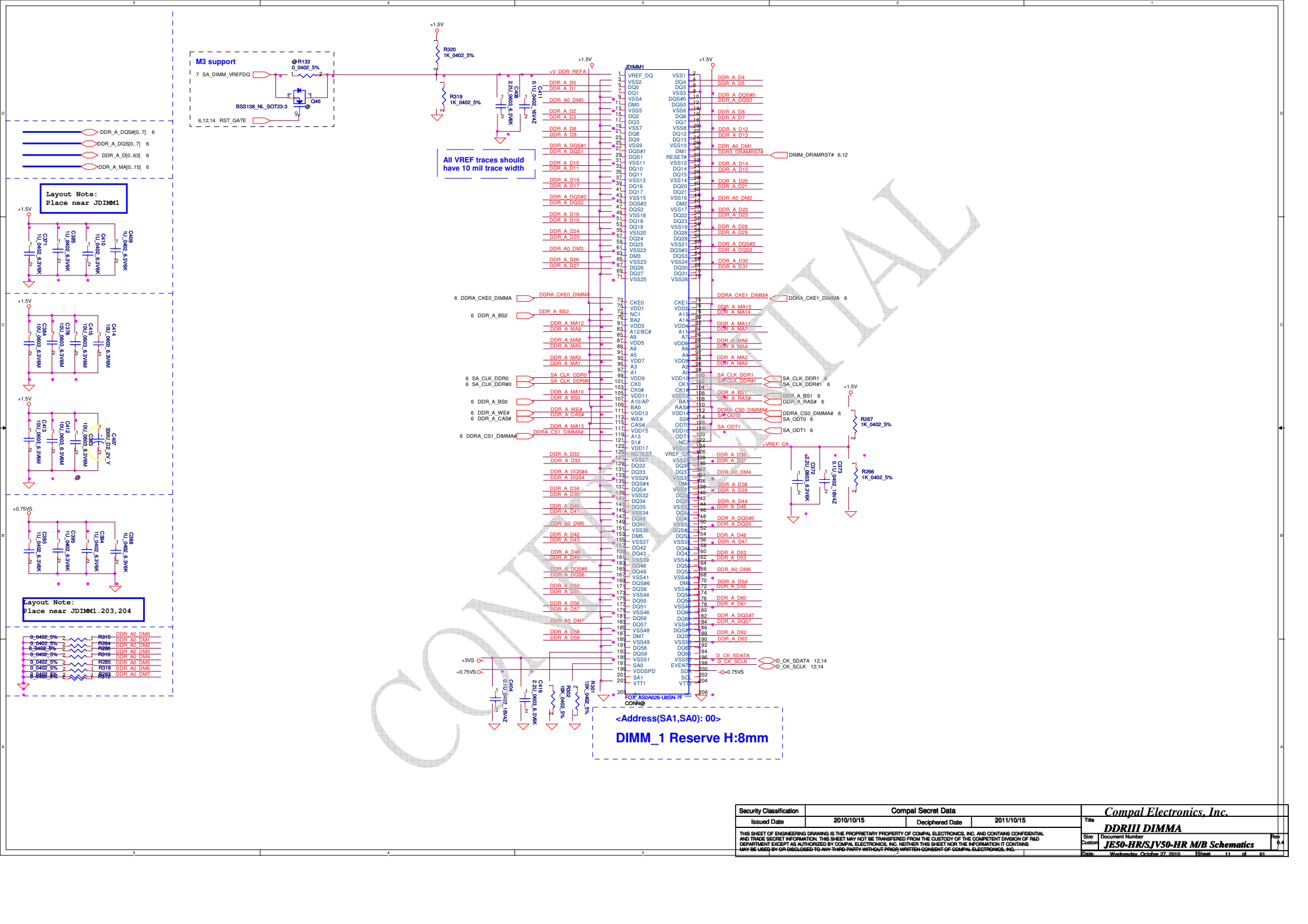
Date: Wednesday, October 27, 2010 | Sheet 10 of 61



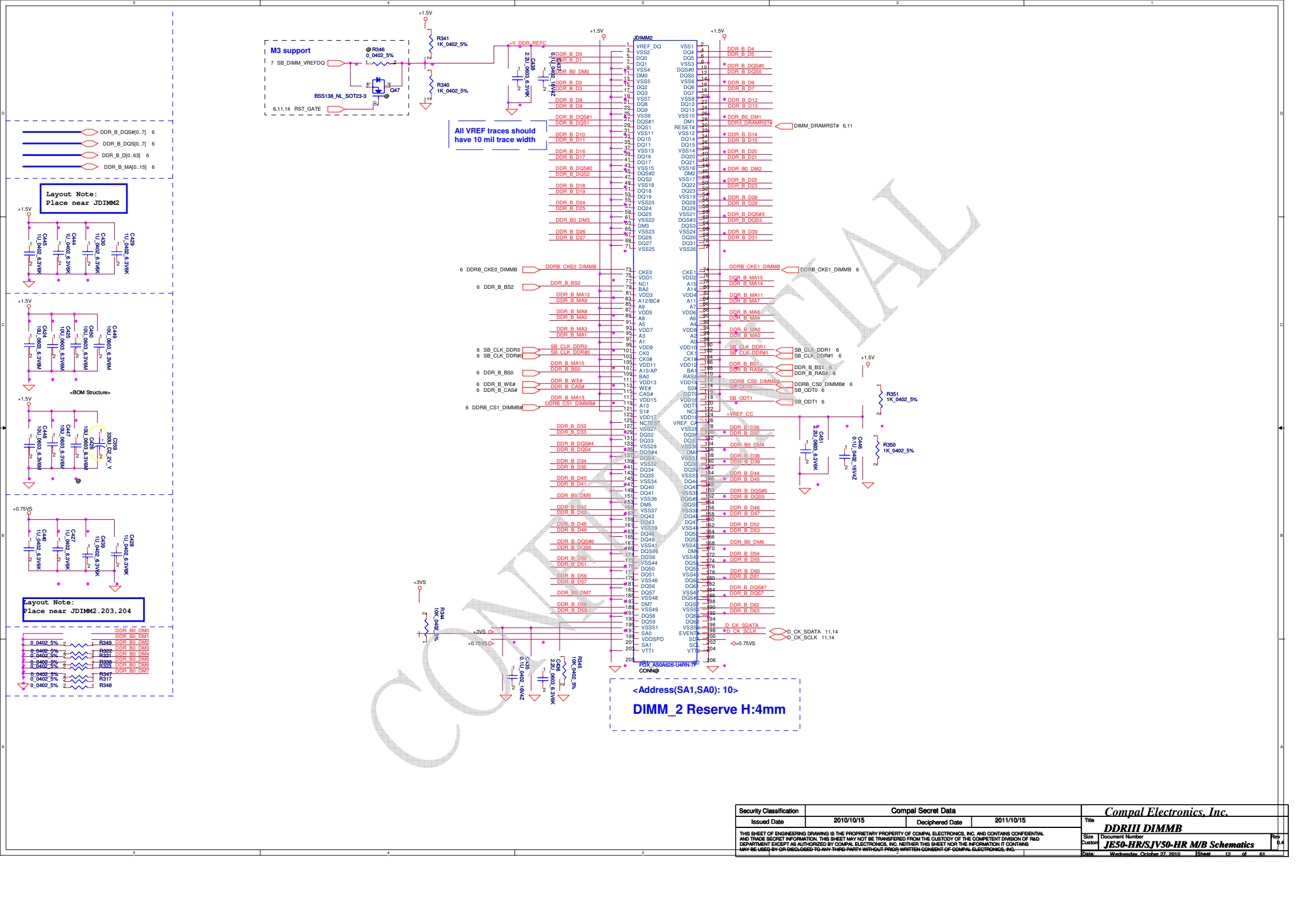
Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: DDRIII DIMMA

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

Date: Wednesday, October 27, 2010 | Sheet 11 of 61



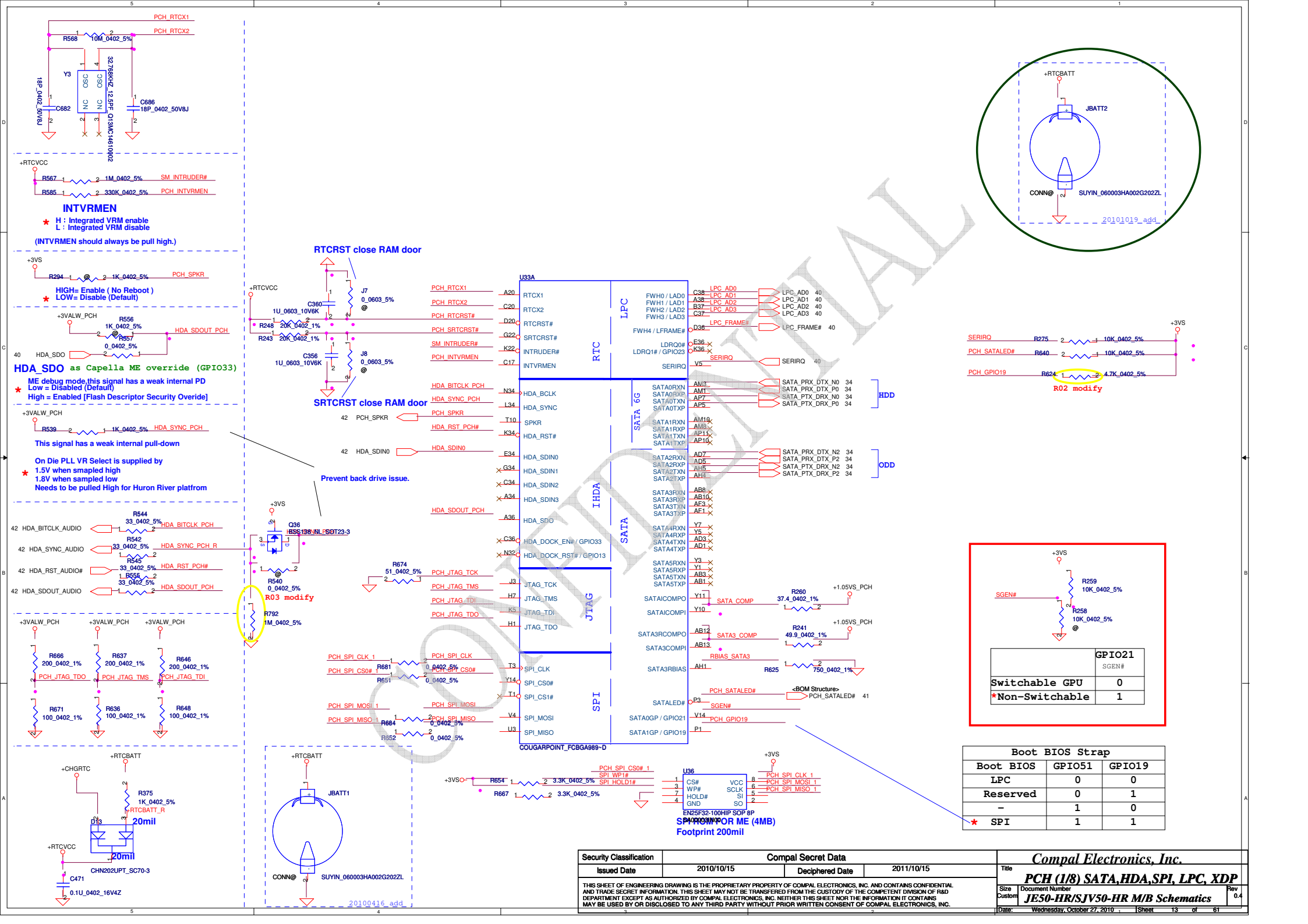
Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: DDRIII DIMMB

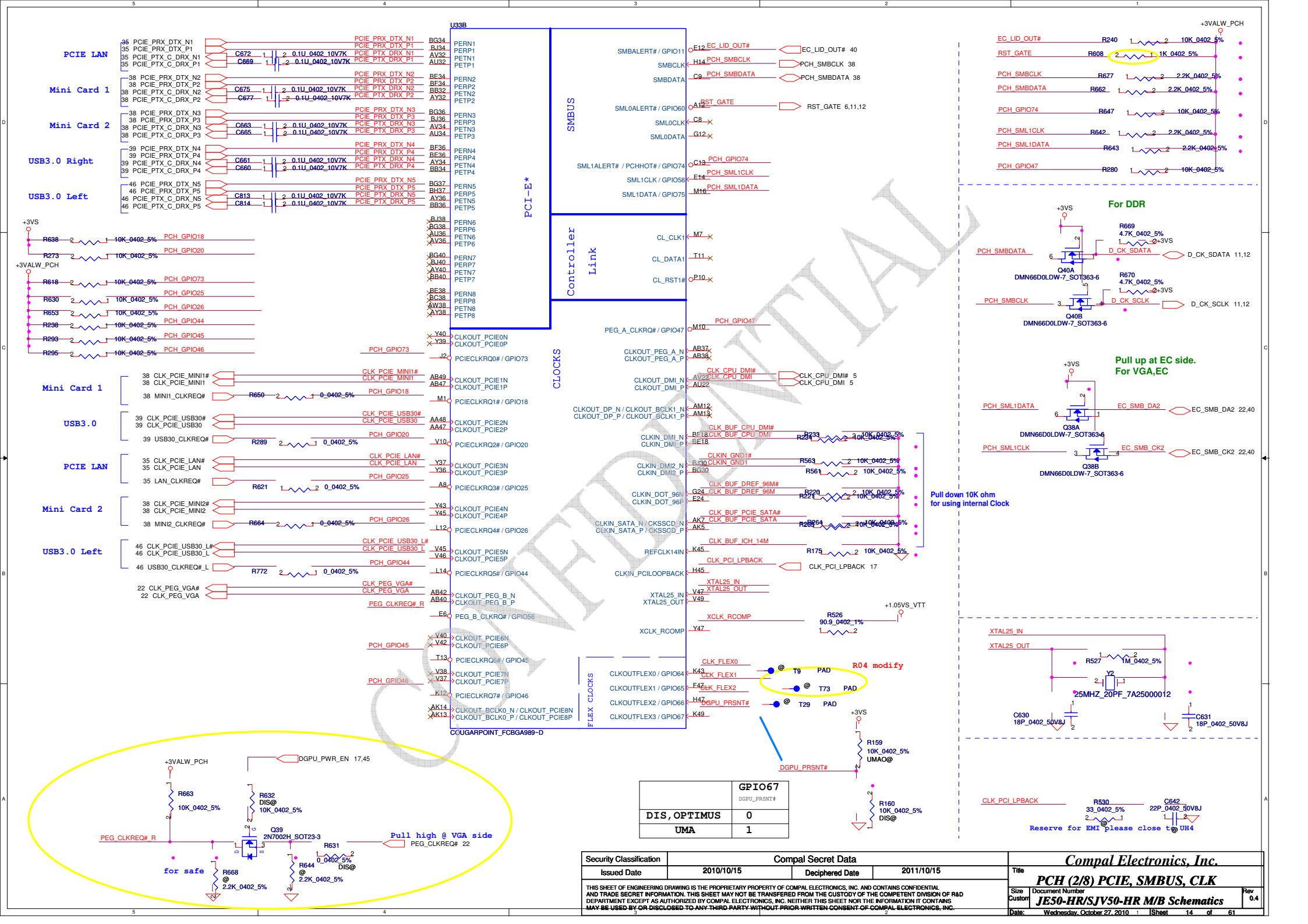
Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

Date: Wednesday, October 27, 2010 | Sheet 12 of 61



Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Title	Compal Electronics, Inc.		
	PCH (1/8) SATA,HDA,SPI, LPC, XDP		
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: 0.4
Date: Wednesday, October 27, 2010	Sheet 13 of 61		



	GPIO67 DGPU_PRSNT#
DIS,OPTIMUS	0
UMA	1

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

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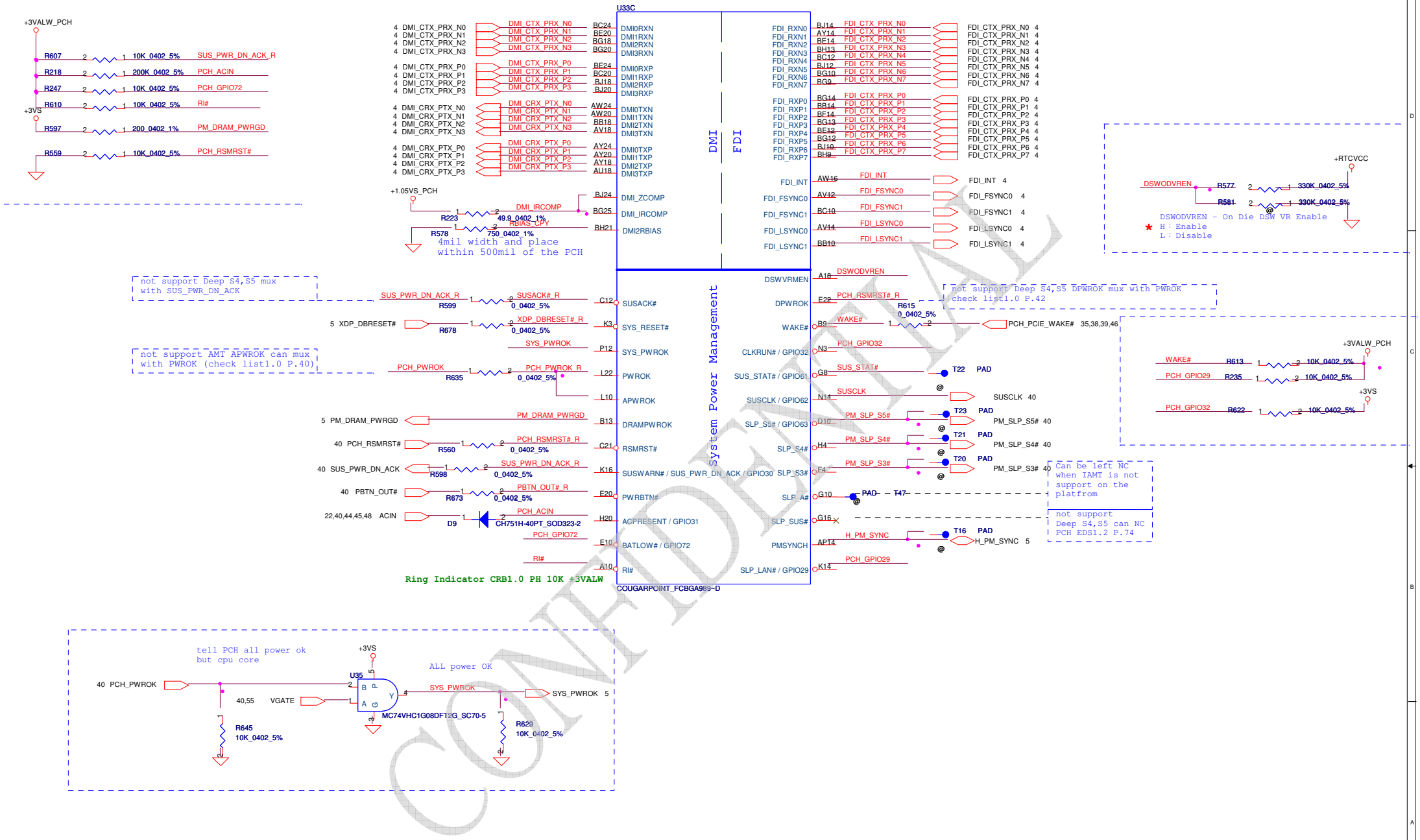
Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

Date: Wednesday, October 27, 2010 | Sheet 14 of 61



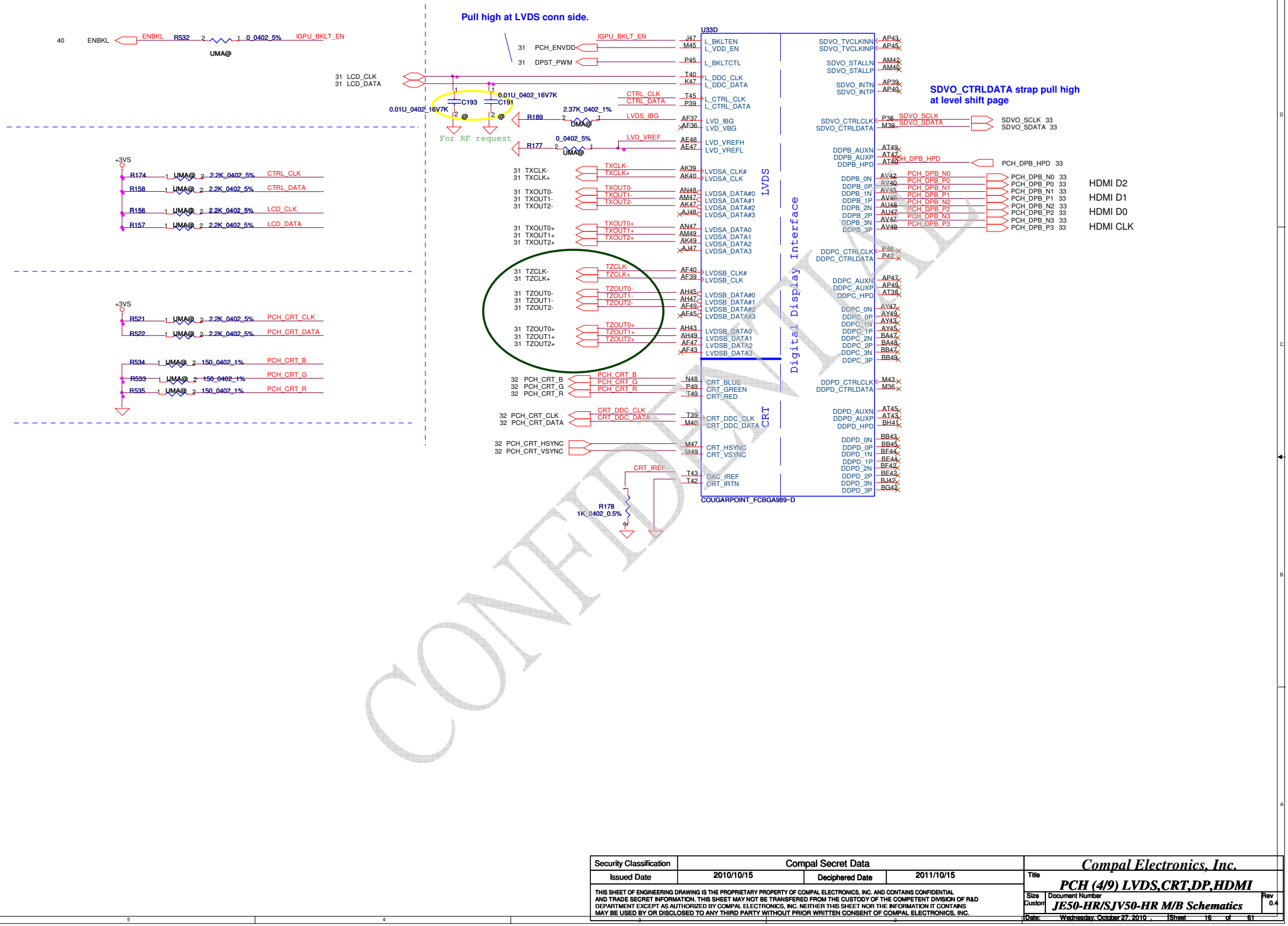
Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

Date: Wednesday, October 27, 2010 | Sheet 15 of 61



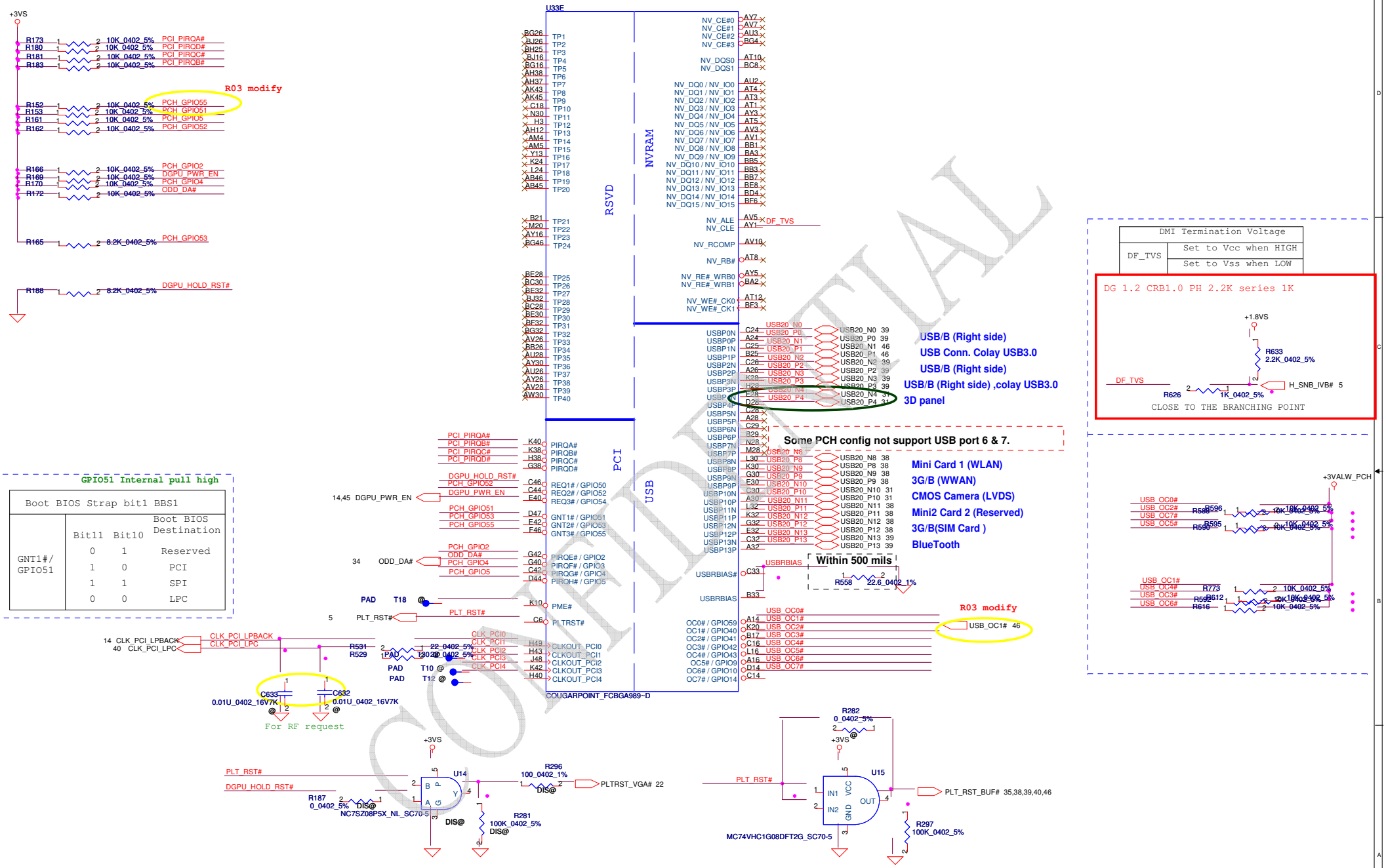
Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size	Document Number	Rev
Custom	JE50-HR/SJV50-HR M/B Schematics	0.4

Date: Wednesday, October 27, 2010 Sheet 16 of 61



Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

Date: Wednesday, October 27, 2010 | Sheet 17 of 61

HDA_SYNC PH(PLL =+1.5VS)

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R272 1 @ 2 1K_0402_5% PCH_GPIO28
+3VALW_PCH R768 1 2 4.7K_0402_5%

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70

R661 1 2 10K_0402_5% PCH_GPIO27

+3VS
R623 1 NOPT@ 2 10K_0402_5% OPTIMUS_EN#
R639 1 OPT@ 2 10K_0402_5%

	GPIO38 OPTIMUS_EN#
* OPTIMUS	0
Non-OPTIMUS	1

+3VS
R04 modify
R277 1 2 200K_0402_5% WWAN_OFF#
R276 1 2 10K_0402_5% PCH_GPIO0
R546 1 2 10K_0402_5% PCH_GPIO1
R191 1 2 10K_0402_5% DGPU_HPD_INT#
R641 1 2 10K_0402_5% PCH_GPIO16
R194 1 2 10K_0402_5% DGPU_PWROK
R290 1 2 10K_0402_5% PCH_GPIO22
R649 1 2 10K_0402_5% PCH_GPIO39
R04 modify
R291 1 2 200K_0402_5% ODD_DETECT#
R619 1 2 10K_0402_5% BT_ON#
R292 1 2 10K_0402_5% PCH_GPIO48
R274 1 2 10K_0402_5% WL_OFF#

+3VALW_PCH
R262 1 2 10K_0402_5% PCH_GPIO24
R620 1 2 10K_0402_5% PCH_GPIO12
R672 1 2 1K_0402_5% SMIB
R263 1 2 10K_0402_5% PCH_GPIO57

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.

CRB1.0 PH10K to +3VALW

U33F

PCH_GPIO0	T7	BMBUSY# / GPIO0		TACH4 / GPIO68	C40
PCH_GPIO1	A42	TACH1 / GPIO1		TACH5 / GPIO69	B41
DGPU_HPD_INT#	H36	TACH2 / GPIO6		TACH6 / GPIO70	C41
40 EC_SCI# EC_SCI#	E38	TACH3 / GPIO7		TACH7 / GPIO71	A40
40 EC_SMI# EC_SMI#	C10	GPIO8			
PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12			
39,46 SMIB SMIB	G2	GPIO15		A20GATE	P4
PCH_GPIO16	U2	SATA4GP / GPIO16		PECI	AH16
54 VGA_PWROK R193 1 2 0_0402_5% DGPU_PWROK	D40	TACH0 / GPIO17		RCIN#	P5
PCH_GPIO22	T5	SCLOCK / GPIO22		PROCPWRGD	AY11
PCH_GPIO24	E8	GPIO24 / MEM_LED		THRMTRIP#	AY10
PCH_GPIO27	E16	GPIO27		INIT3_3V#	T14
PCH_GPIO28	P8	GPIO28			
38,39 BT_ON# BT_ON#	K1	STP_PCI# / GPIO34			
	K4	GPIO35		NC_1	AH8
34 ODD_DETECT# ODD_DETECT#	V8	SATA2GP / GPIO36		NC_2	AK11
R03 modify 38 WWAN_OFF# WWAN_OFF#	M5	SATA3GP / GPIO37		NC_3	AH10
OPTIMUS_EN#	N2	SLOAD / GPIO38		NC_4	AK10
PCH_GPIO39	M3	SDATAOUT0 / GPIO39		NC_5	P37
PCH_GPIO48	V13	SDATAOUT1 / GPIO48			
R03 modify 38 WL_OFF# WL_OFF#	V3	SATA5GP / GPIO49			
PCH_GPIO57	D6	GPIO57			

GPIO
CPU/MISC
NCTF

PAD T61	A4	VSS_NCTF_1		VSS_NCTF_15	BG2 T58 PAD
PAD T46	A44	VSS_NCTF_2		VSS_NCTF_16	BG48 T39 PAD
PAD T44	A45	VSS_NCTF_3		VSS_NCTF_17	BH3 T59 PAD
PAD T41	A46	VSS_NCTF_4		VSS_NCTF_18	BH47 T40 PAD
PAD T52	A5	VSS_NCTF_5		VSS_NCTF_19	BJ4 T60 PAD
PAD T51	A6	VSS_NCTF_6		VSS_NCTF_20	BJ44 T45 PAD
PAD T64	B3	VSS_NCTF_7		VSS_NCTF_21	BJ45 T43 PAD
PAD T37	B47	VSS_NCTF_8		VSS_NCTF_22	BJ46 T42 PAD
PAD T55	BD1	VSS_NCTF_9		VSS_NCTF_23	BJ5 T50 PAD
PAD T34	BD49	VSS_NCTF_10		VSS_NCTF_24	BJ6 T49 PAD
PAD T56	BE1	VSS_NCTF_11		VSS_NCTF_25	C2 T65 PAD
PAD T35	BE49	VSS_NCTF_12		VSS_NCTF_26	C48 T38 PAD
PAD T57	BF1	VSS_NCTF_13		VSS_NCTF_27	D1 T63 PAD
PAD T36	BF49	VSS_NCTF_14		VSS_NCTF_28	D49 T32 PAD
				VSS_NCTF_29	E1 T54 PAD
				VSS_NCTF_30	F49 T33 PAD
				VSS_NCTF_31	F1 T53 PAD
				VSS_NCTF_32	F49 T31 PAD

COUGARPOINT_FCBGA989~D

ODD_EN# 34

+3VS
R278 10K_0402_5%
GATEA20 40
PECI CPU-EC
PCH_PECI_R 1 2 0_0402_5%@R239 H_PECI 5,40
CTRL+ALT+DEL
EC_KBRST# 40
non CPU power ok
H_CPUPWRGD 5
PCH_THRMTRIP#_R R627 1 2 390_0402_5% H_THRMTRIP# H_THRMTRIP# 5
130 degree shut sown

INIT3_3V Checklist1.0 P.59
This signal has weak internal PU, can't pull low,leave NC

TS_VSS1~4
PD to GND

+3VS
ODD_EN# R771 2 10K_0402_5%
EC_KBRST# R279 1 2 10K_0402_5%

R02 modify
+3VS
R554 10K_0402_5% PCH_GPIO69
R548 10K_0402_5% PCH_GPIO70
R553 10K_0402_5%
R549 10K_0402_5%

R02 modify
+3VS
R550 10K_0402_5% PCH_GPIO71
X76@
R551 10K_0402_5% X76@

Project ID	GPIO69	GPIO70
* P5WE0	0	0
P7YE0	0	0
x	1	0
x	1	1

	GPIO71 PCH_GPIO71
*VRAM 800 MHz	0
VRAM 900 MHz	1

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

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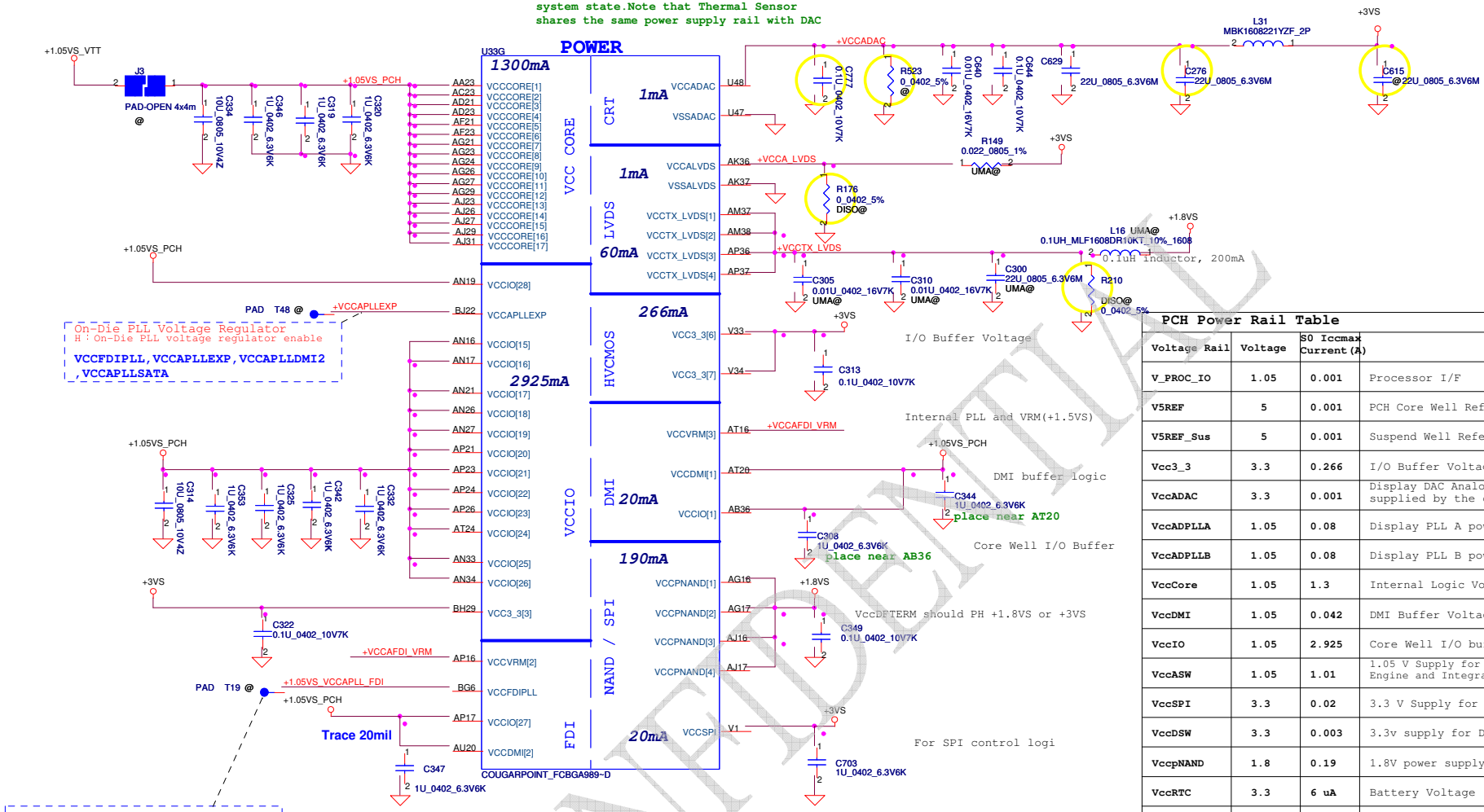
+VCCADAC should be powered up during S0 system state.Note that Thermal Sensor shares the same power supply rail with DAC



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: PCH (7/9) PWR

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Have internal VRM

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

POWER

U33J

+3VS
R150 0_0805_5%
L14 10UH_LB2012T100MR_20%
+3VS_VCC_CLKF33
C277 10U_0805_10V4Z
C304 1U_0402_6.3V6K

+1.05V analog internal clock PLL Can NC
+1.05VS_PCH
R167 0_0603_5%
+VCCACLK

Not support Deep S4,S5 connect to +3VALW
+3VALW_PCH
C340 0.1U_0402_10V7K

PAD T17 @ +PCH_VCCDSW
+3VS_VCC_CLKF33

suppied by internal 1.05V VR must NC
PAD T11 @ +VCCAPLL_CPY_PCH
+1.05VS_RCH
PAD T13 @ +VCCSUS1

GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA

AD49 VCCACLK
T16 VCCDSW3_3
V12 DCPSUSBYP
T38 VCC3_3[5]
BH23 VCCAPLLDMI2
AL29 VCCIO[14]
AL24 DCPSUS[3]

3mA
119mA
1010mA
1mA

USB
Clock and Miscellaneous
PCI/GPIO/LPC

+1.05VS_PCH
L12 10UH_LB2012T100MR_20%
+1.05VS_VCCA_A_DPL
C279 220U_B2_2.5VM_R35
C296 1U_0402_6.3V6K
L11 10UH_LB2012T100MR_20%
+1.05VS_VCCA_B_DPL
C278 220U_B2_2.5VM_R35
C295 1U_0402_6.3V6K
SGA00001700
220U 2.5V M B2
ESR 35mohm@100Khz

+1.05VS_PCH
C336 22U_0805_6.3V6M
C335 22U_0805_6.3V6M
C326 1U_0402_6.3V6K
C327 1U_0402_6.3V6K
C316 1U_0402_6.3V6K

AA19 VCCASW[1]
AA21 VCCASW[2]
AA24 VCCASW[3]
AA26 VCCASW[4]
AA27 VCCASW[5]
AA29 VCCASW[6]
AA31 VCCASW[7]
AC26 VCCASW[8]
AC27 VCCASW[9]
AC29 VCCASW[10]
AC31 VCCASW[11]
AD29 VCCASW[12]
AD31 VCCASW[13]
W21 VCCASW[14]
W23 VCCASW[15]
W24 VCCASW[16]
W26 VCCASW[17]
W29 VCCASW[18]
W31 VCCASW[19]
W33 VCCASW[20]

+VCCRTCEXT
C348 0.1U_0402_10V7K
+VCCAFDI_VRM
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL

N16 DCPRTC
Y49 VCCVRM[4]
BD47 VCCADPLLA
BF47 VCCADPLLB

80mA
80mA
SATA

+1.05VS_PCH
C311 1U_0402_6.3V6K Place near AF17
C312 1U_0402_6.3V6K Place near AG33
C317 1U_0402_6.3V6K Place near AF33, AF34,AG34

AF17 VCCIO[7]
AF33 VCCIO[8]
AF34 VCCIO[9]
AG34 VCCIO[11]
AG33 VCCIO[10]

55mA
95mA

+VCCSST
C354 0.1U_0402_10V7K
+1.05VM_VCCSUS

V16 DCPSST
T17 DCPSUS[1]
V19 DCPSUS[2]

PAD T15 @
suppied by internal 1.05V VR Must NC

1mA
CPU
MISC

BJ8 V_PROC_IO

+1.05VS_PCH
C700 4.7U_0603_6.3V6K
C684 0.1U_0402_10V7K
C693 0.1U_0402_10V7K
Place near BJ8

+RTCVCC
A22 VCCRTC
C331 1U_0402_6.3V6K
C685 0.1U_0402_10V7K
C687 0.1U_0402_10V7K

RTC
SUS
10mA

COUGARPOINT_FCBGA989~D

+1.05VS_PCH
C321 1U_0402_6.3V6K

T23 VCCSUS3_3[7]
T24 VCCSUS3_3[8]
V23 VCCSUS3_3[9]
V24 VCCSUS3_3[10]
P24 VCCSUS3_3[6]
+3VALW_PCH
C330 0.1U_0402_10V7K Place near J24
C333 0.1U_0402_10V7K Place near J24

T26 VCCIO[34]
+1.05VS_PCH
M26 V5REF_SUS
+PCH_V5REF_SUS
AN23 DCPSUS[4]
+VCCA_USBSUS
AN24 VCCSUS3_3[1]
+3VALW_PCH
@ F14 PAD
Supplied by internal 1.05V VR Must NC

P34 V5REF
+PCH_V5REF_RUN
N20 VCCSUS3_3[2]
N22 VCCSUS3_3[3]
P20 VCCSUS3_3[4]
P22 VCCSUS3_3[5]
+3V_VCCPSUS
+3VALW_PCH
C352 1U_0402_6.3V6K

AA16 VCC3_3[1]
W16 VCC3_3[8]
T34 VCC3_3[4]
+3VS
C704 0.1U_0402_10V7K Place near J2
C343 0.1U_0402_10V7K Place near AA16,W16
C309 0.1U_0402_10V7K Place near J24

AJ2 VCC3_3[2]
+1.05VS_PCH
AF13 VCCIO[5]
AH13 VCCIO[12]
AH14 VCCIO[13]
AF14 VCCIO[6]
C350 1U_0402_6.3V6K

AK1 VCCAPLLSATA
+VCCSATAPLL
@ T62 PAD
+VCCAFDI_VRM
AF11 VCCVRM[1]
+VCCAFDI_VRM

GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA

AC16 VCCIO[2]
AC17 VCCIO[3]
AD17 VCCIO[4]
+1.05VS_PCH
C351 1U_0402_6.3V6K

T21 VCCASW[22]
V21 VCCASW[23]
T19 VCCASW[21]
+VCCME_22
+VCCME_23
+VCCME_21
R237 0_0603_5%
R224 0_0603_5%
R236 0_0603_5%
+1.05VS_PCH
+3VALW_PCH
Need +3VALW and 0.1U close PCH

P32 VCCSUSHDA
+VCCSUSHDA
R206 0_0603_5%
C315 1U_0402_16V4Z

+5VALW_PCH
+3VALW_PCH
R202 100_0402_1%
D8 CH751H-40PT_SOD323-2
+PCH_V5REF_SUS
C318 0.1U_0603_25V7K

+5VS
+3VS
R148 100_0402_1%
D7 CH751H-40PT_SOD323-2
+PCH_V5REF_RUN
C244 1U_0603_10V6K

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Title: PCH (8/9) PWR

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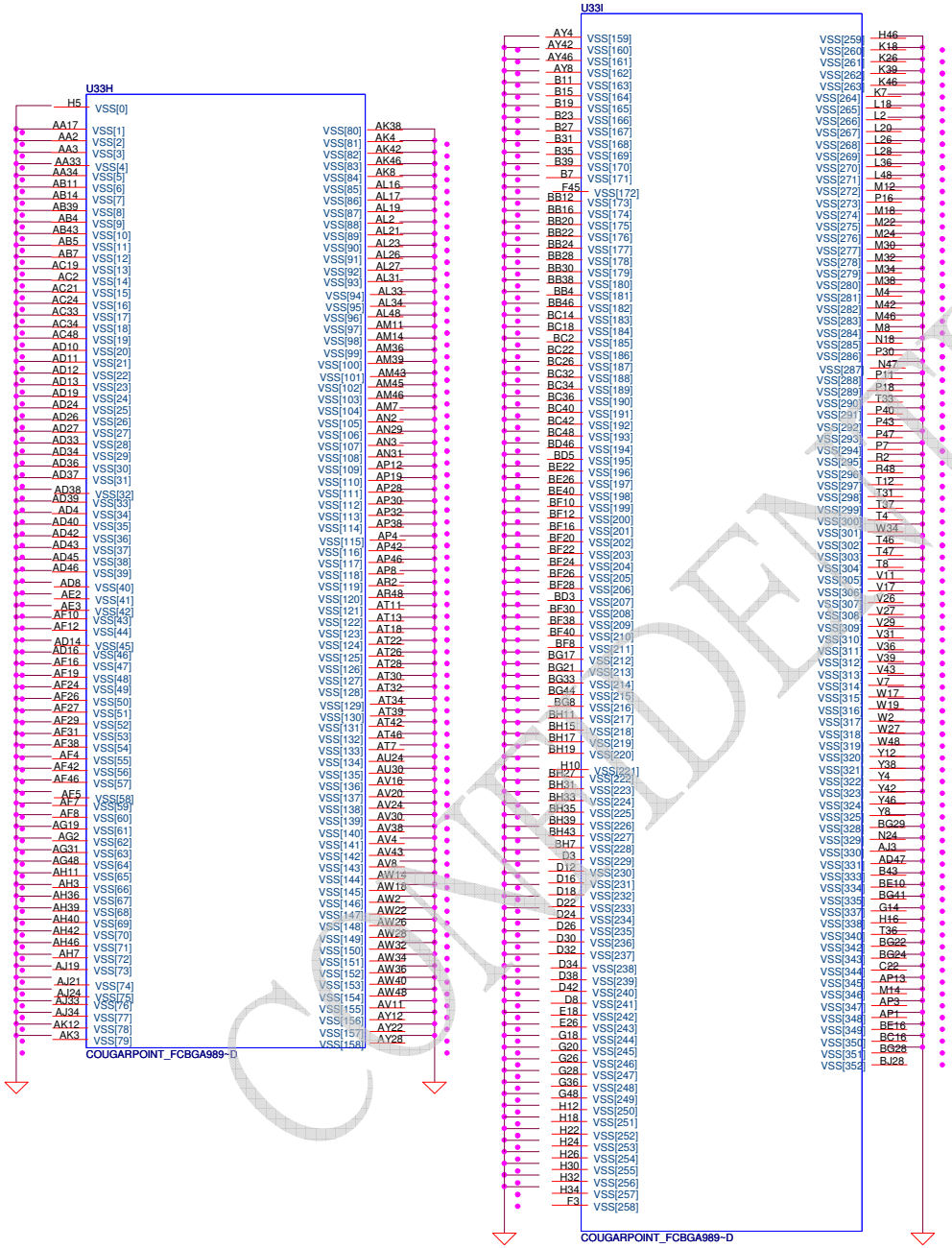

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: PCH (9/9) VSS

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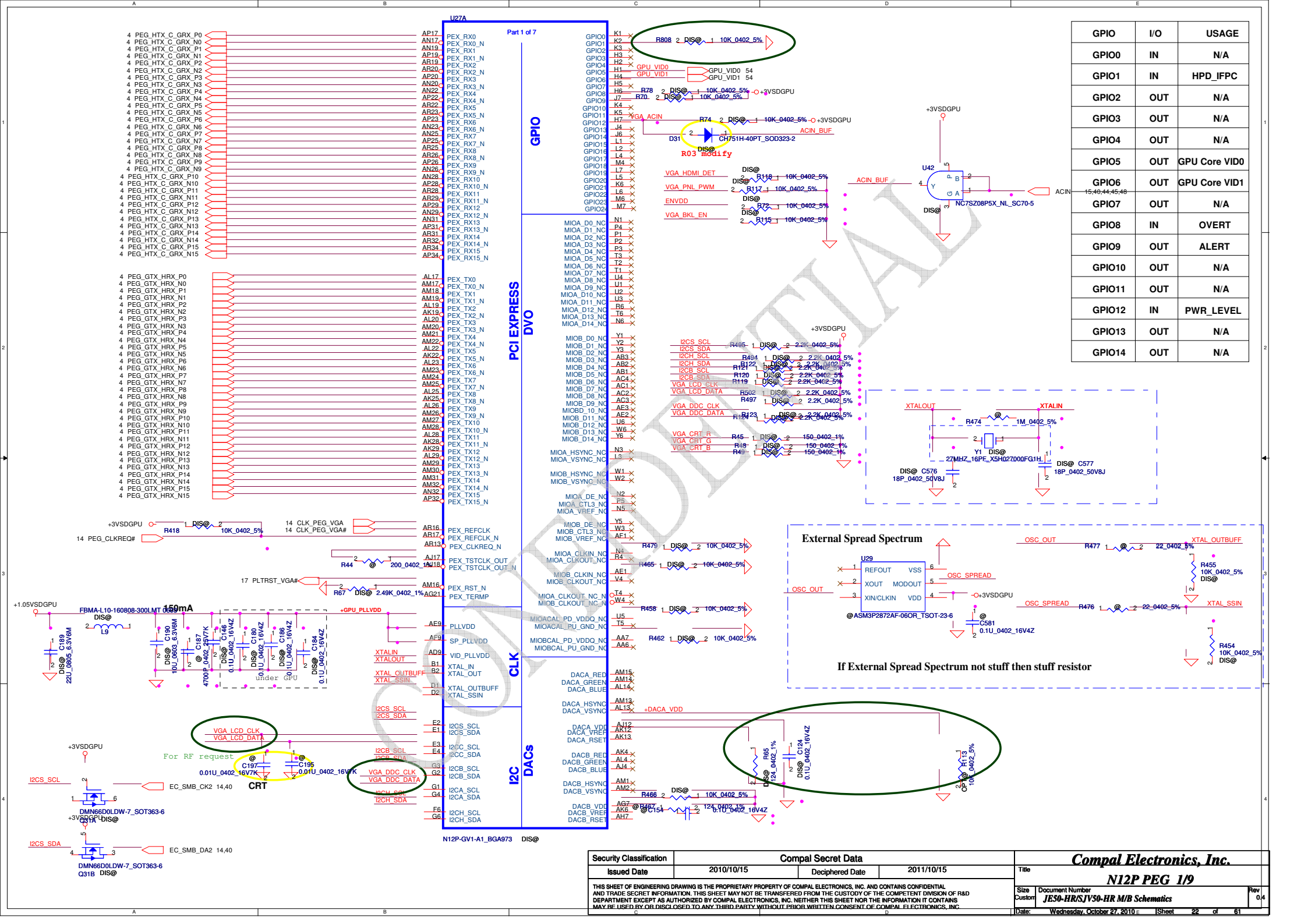

GPIO	I/O	USAGE
GPIO0	IN	N/A
GPIO1	IN	HPD_IFPC
GPIO2	OUT	N/A
GPIO3	OUT	N/A
GPIO4	OUT	N/A
GPIO5	OUT	GPU Core VID0
GPIO6	OUT	GPU Core VID1
GPIO7	OUT	N/A
GPIO8	IN	OVERT
GPIO9	OUT	ALERT
GPIO10	OUT	N/A
GPIO11	OUT	N/A
GPIO12	IN	PWR_LEVEL
GPIO13	OUT	N/A
GPIO14	OUT	N/A

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: N12P PEG 1/9

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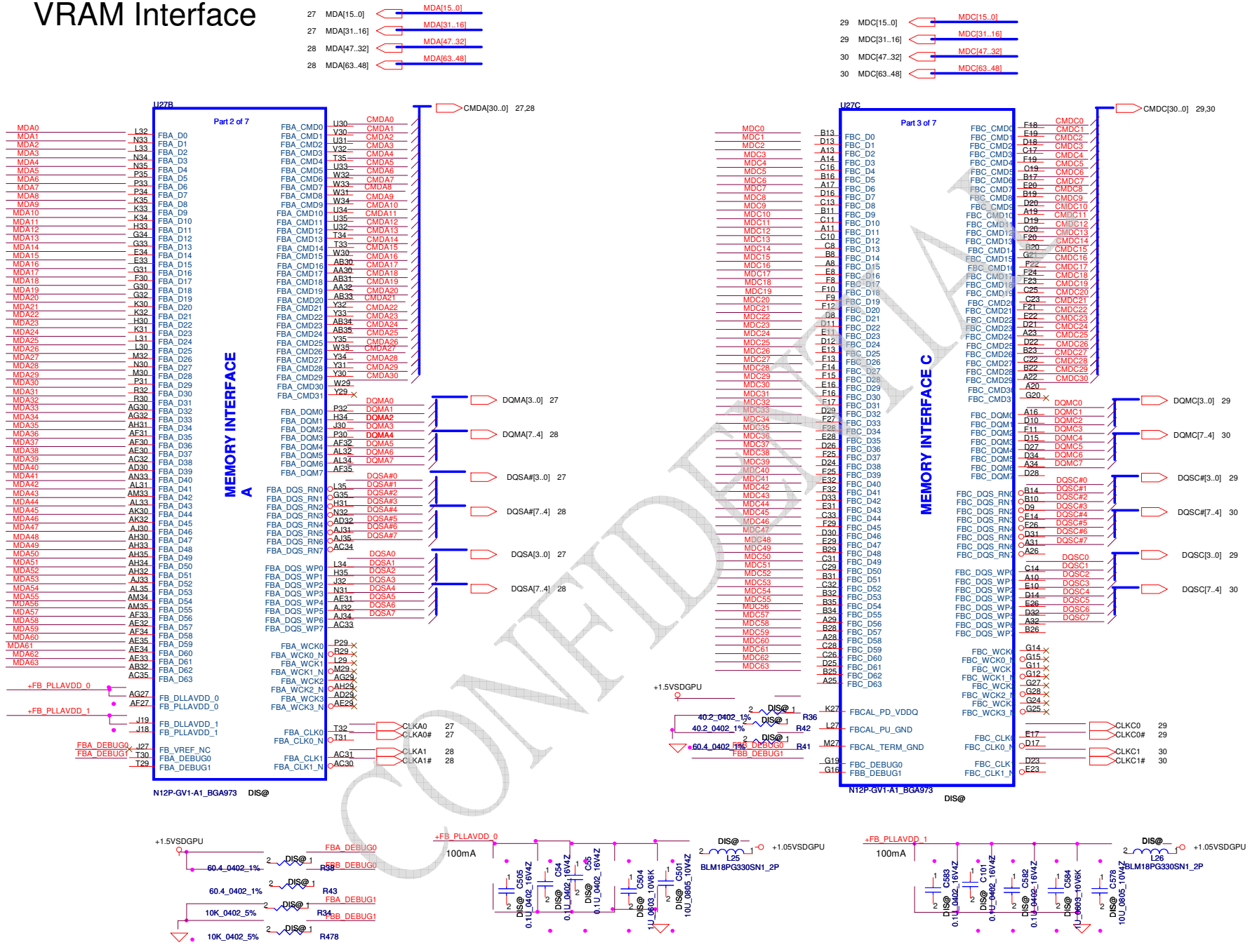
VRAM Interface



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Title: N12P VRAM 2/9			
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: 0.4
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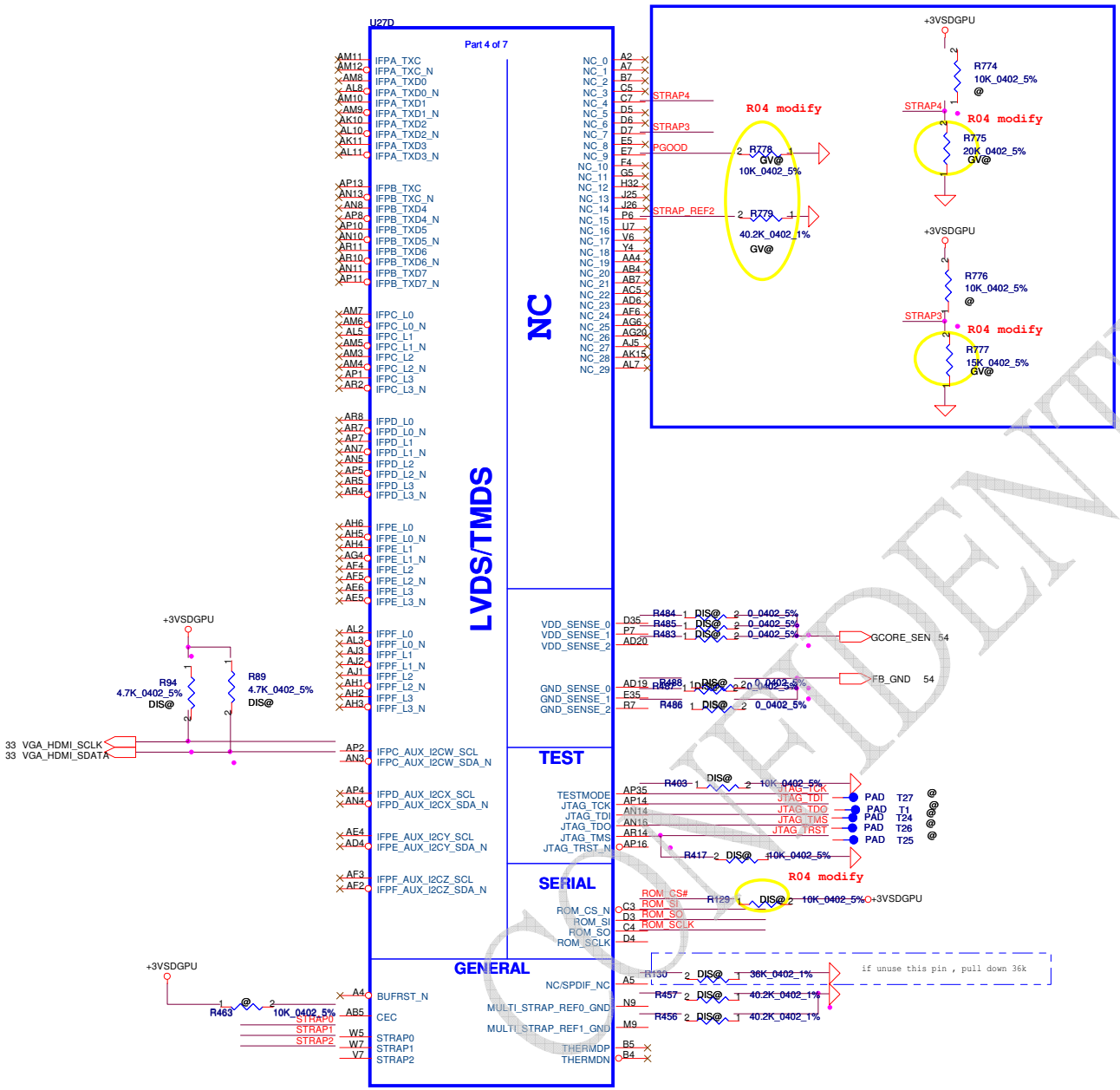
For GB2-128 & GB2b-128 colayout....

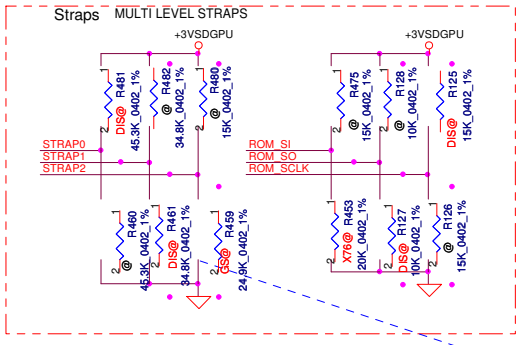


For N12P-GV ES strap table

Frenq.	N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK	strap3	strap4
800 MHz	64MX16 Hynix SA000032420	H 45K	L 35K	H 45K	L 15K	H 10K	H 15K	L 15K	L 20K
900 MHz	64MX16 Hynix SA000041S40	H 45K	L 35K	H 45K	L 15K	H 10K	H 15K	L 15K	L 20K
900 MHz	64MX16 Samsung SA00004GS10	H 45K	L 35K	H 45K	L 25K	H 10K	H 15K	L 15K	L 20K
800 MHz	128MX16 Samsung SA00003MQ60	H 45K	L 35K	H 45K	L 45K	H 10K	H 15K	L 15K	L 20K
800 MHz	128MX16 Hynix SA00003VS10	H 45K	L 35K	H 45K	L 35K	H 10K	H 15K	L 15K	L 20K

For N12P-GV A1 strap table

Frenq.	N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK	strap3	strap4
800 MHz	64MX16 Hynix SA000032420	H 45K	L 35K	L 5K	L 15K	H 10K	H 5K	L 15K	L 20K
900 MHz	64MX16 Hynix SA000041S40	H 45K	L 35K	L 5K	L 15K	H 10K	H 5K	L 15K	L 20K
900 MHz	64MX16 Samsung SA00004GS10	H 45K	L 35K	L 5K	L 25K	H 10K	H 5K	L 15K	L 20K
800 MHz	128MX16 Samsung SA00003MQ60	H 45K	L 35K	L 5K	L 45K	H 10K	H 5K	L 15K	L 20K
800 MHz	128MX16 Hynix SA00003VS10	H 45K	L 35K	L 5K	L 35K	H 10K	H 5K	L 15K	L 20K



For N12P-GS strap table (strap 3 and strap4 left NC)

Frenq.	N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
800 MHz	64MX16 Hynix SA000032420	H 45K	L 35K	L 25K	L 5K	L 10K	H 15K
900 MHz	64MX16 Hynix SA000041S40	H 45K	L 35K	L 25K	L 15K	L 10K	H 15K
900 MHz	64MX16 Samsung SA00004GS10	H 45K	L 35K	L 25K	L 20K	L 10K	H 15K
800 MHz	128MX16 Samsung SA00003MQ60	H 45K	L 35K	L 25K	L 45K	L 10K	H 15K
800 MHz	128MX16 Hynix SA00003VS10	H 45K	L 35K	L 25K	L 35K	L 10K	H 15K

GV@ R459 45.3K 0402_1%

Strap 2 for GV1, Pull low 45K Ohm

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Compal Electronics, Inc.

Title: N12P LVDS 3/9

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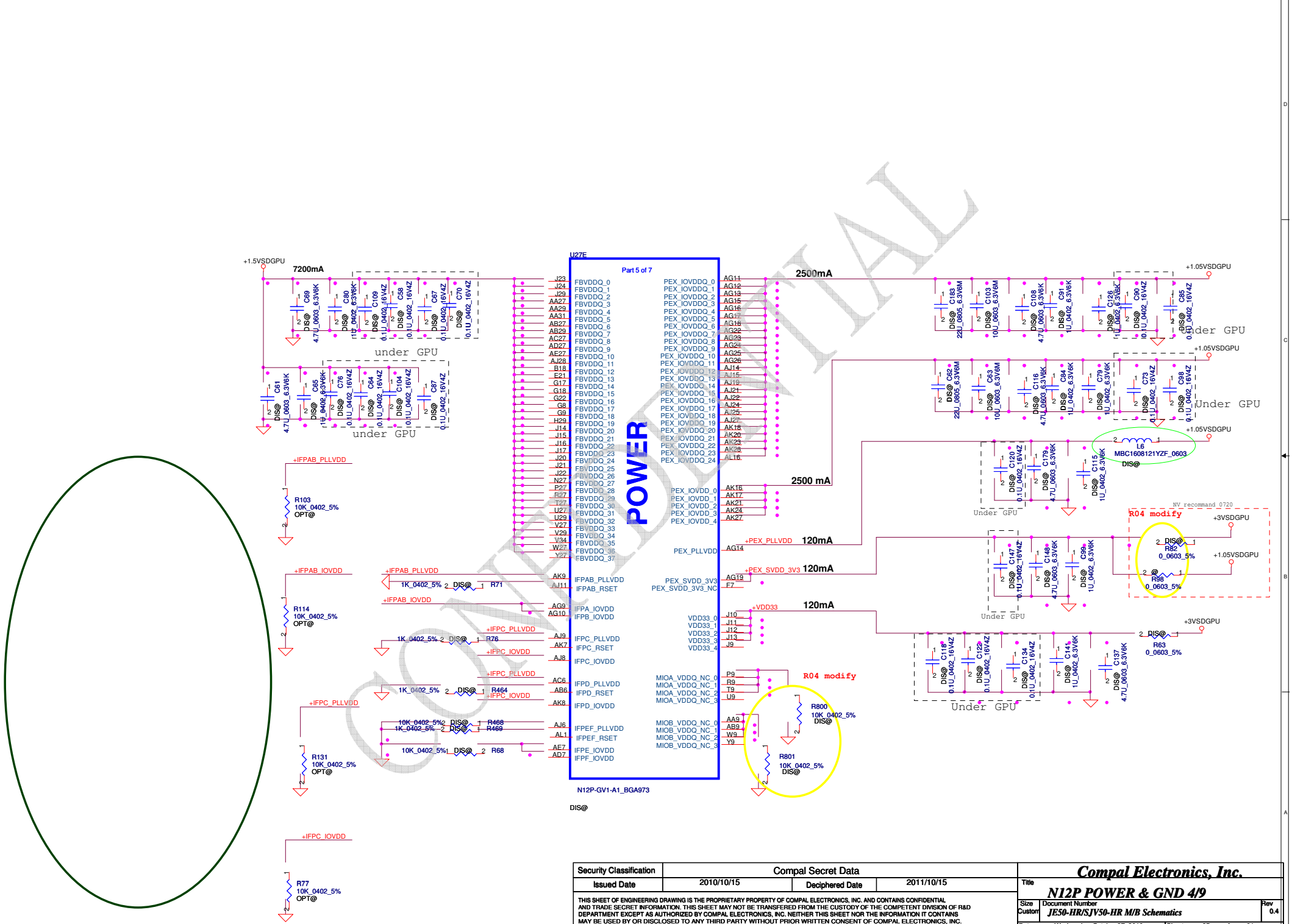

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: **N12P POWER & GND 4/9**

Size	Document Number	Rev
Custom	JE50-HR/SJV50-HR M/B Schematics	0.4

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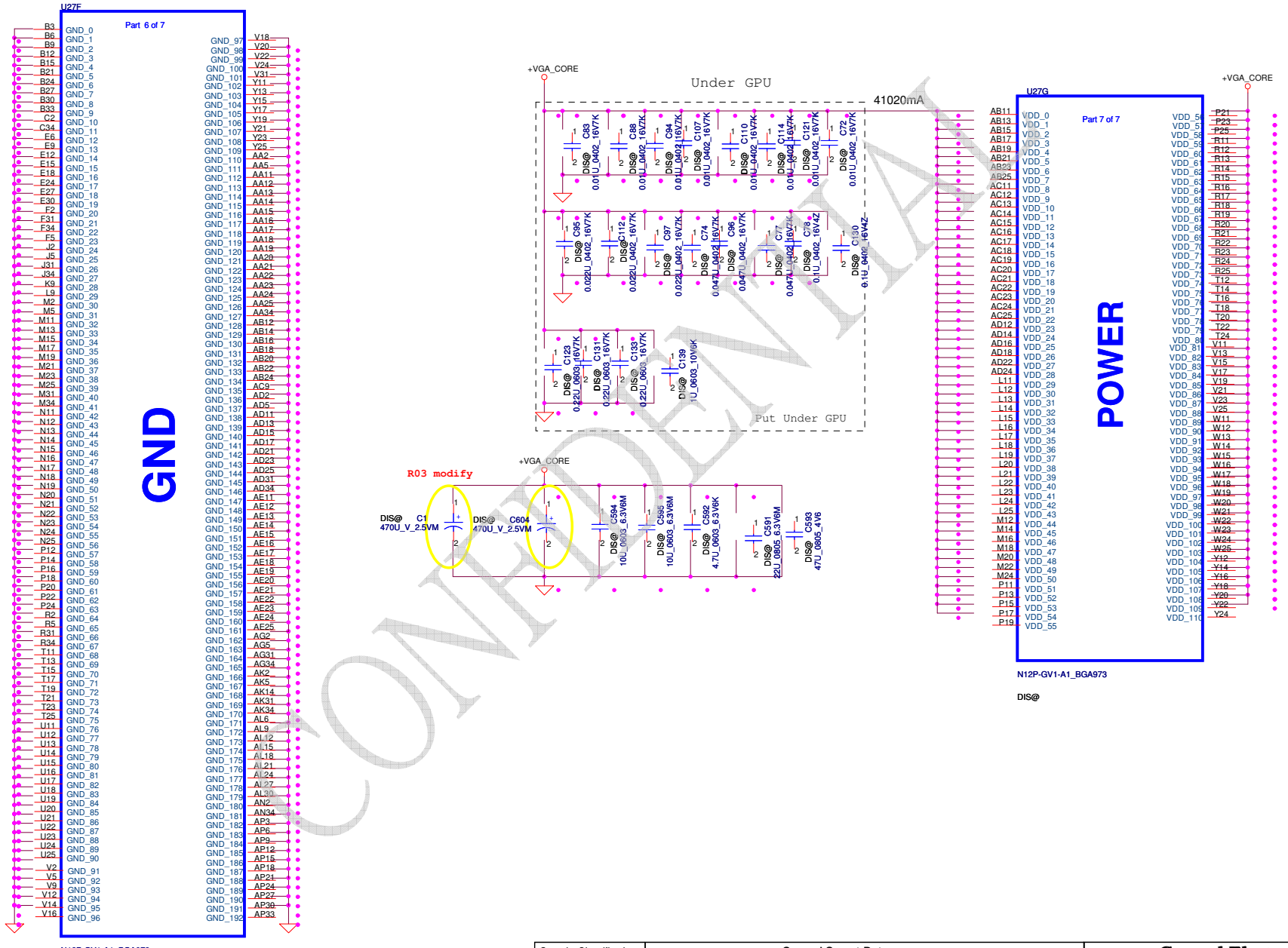

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: **N12P POWER & GND 5/9**

Size	Document Number	Rev
Custom	JE50-HR/SJV50-HR M/B Schematics	0.4

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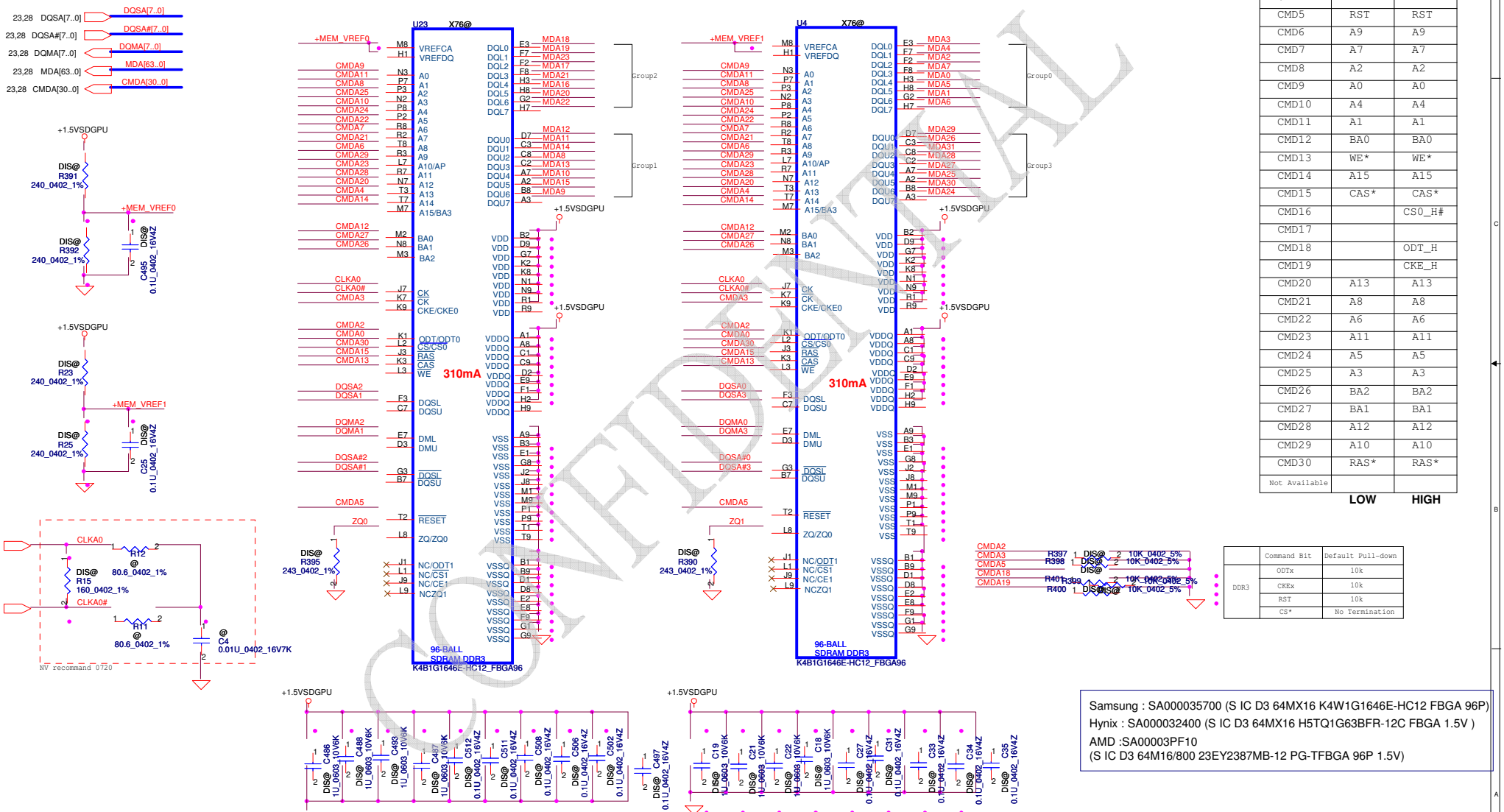
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

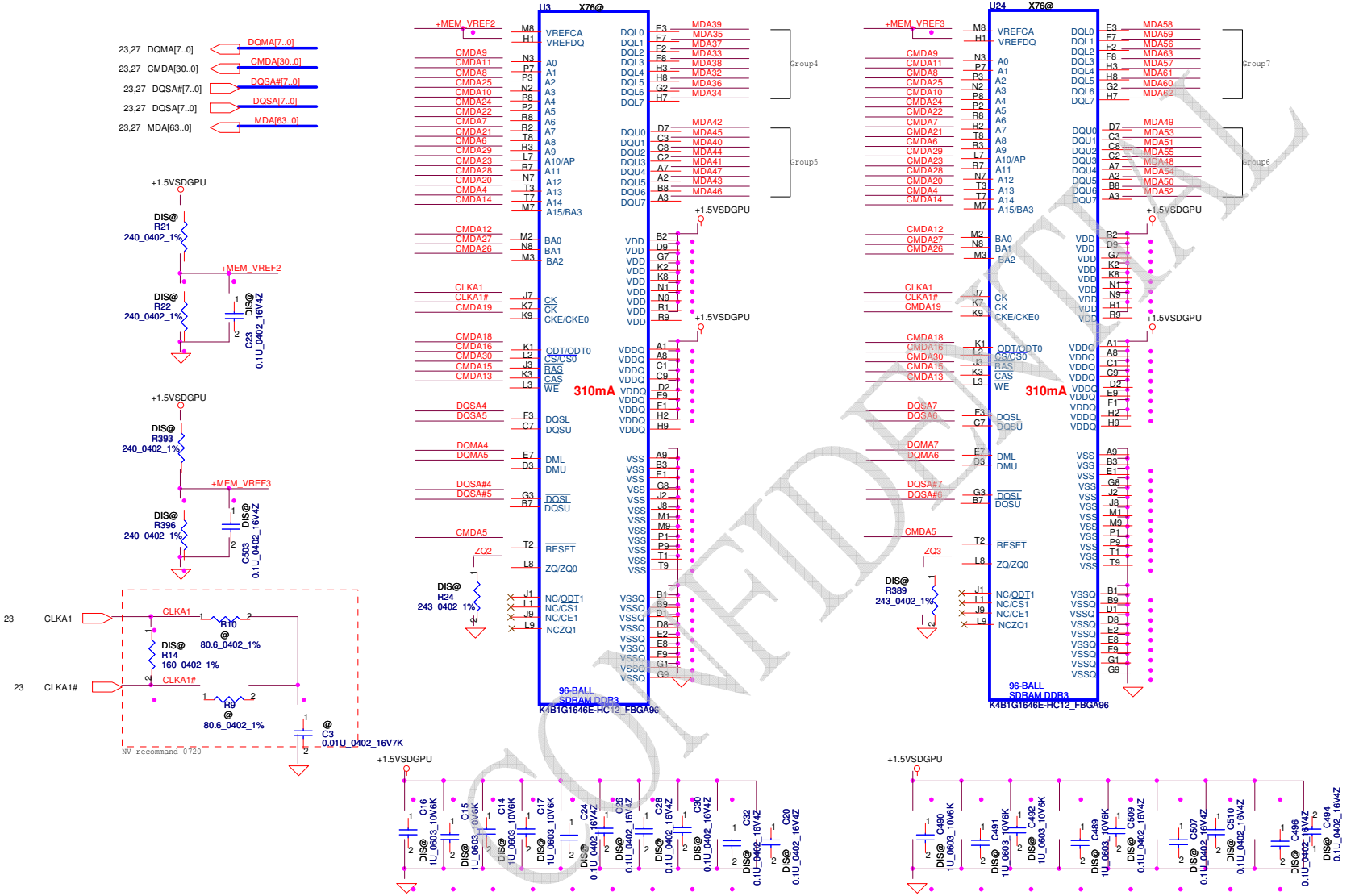
Title: N12P DDR3 6/9

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

Date: Wednesday, October 27, 2010 | Sheet 27 of 61

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

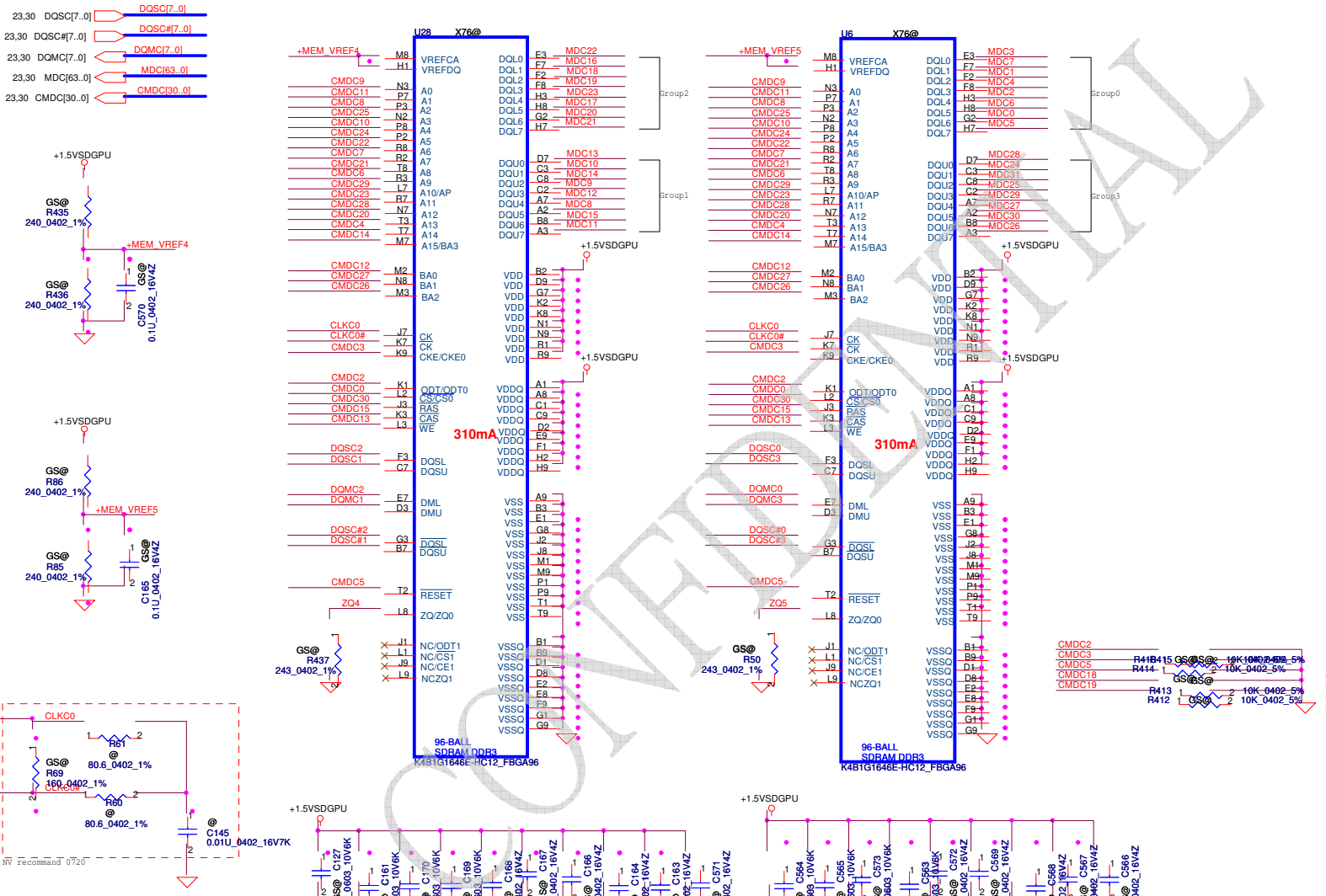
Title: N12P DDR3 7/9

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

Date: Wednesday, October 27, 2010 | Sheet 28 of 61

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

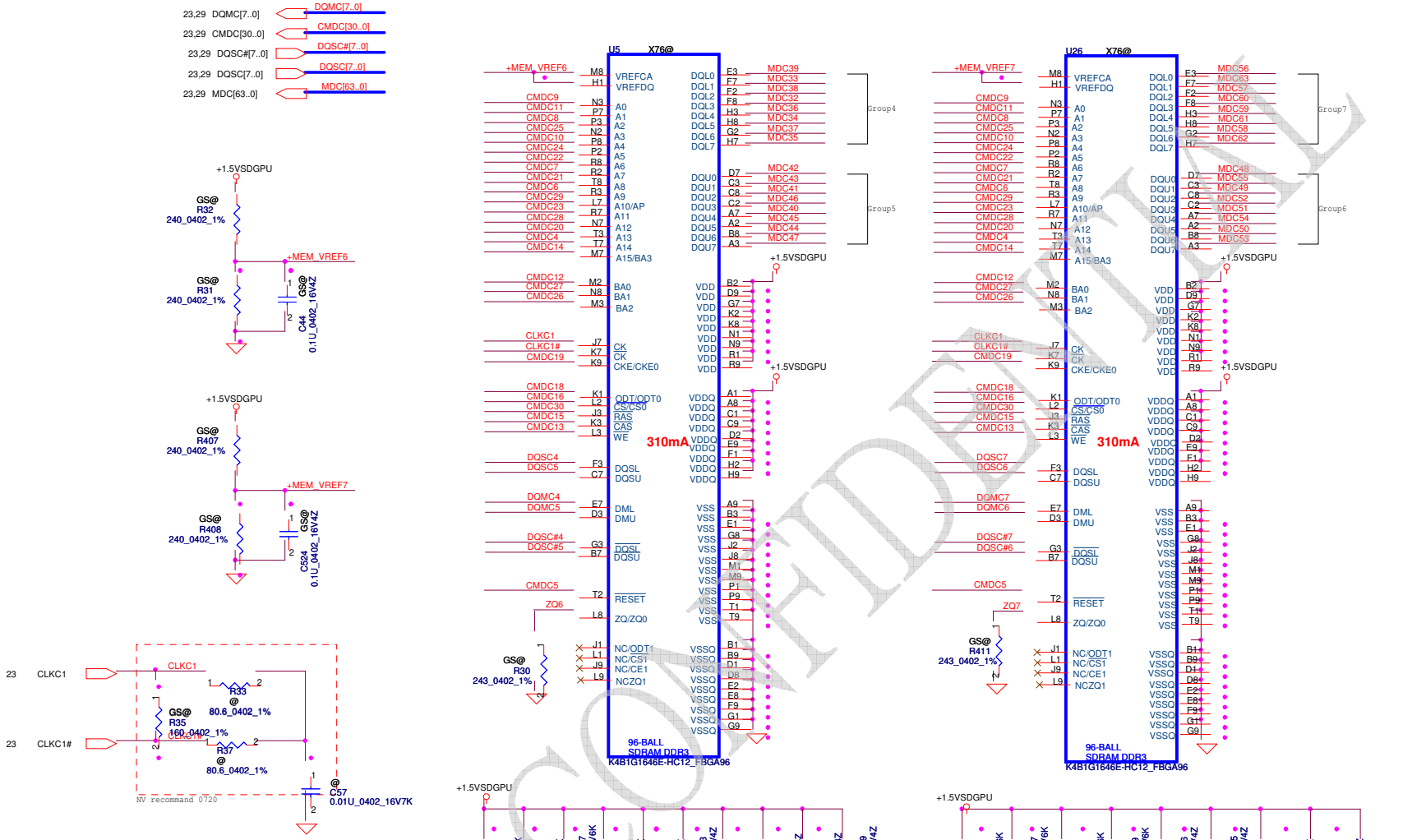
Title: N12P DDR3 8/9

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

Date: Wednesday, October 27, 2010 | Sheet 29 of 61

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: N12P DDR3 9/9

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

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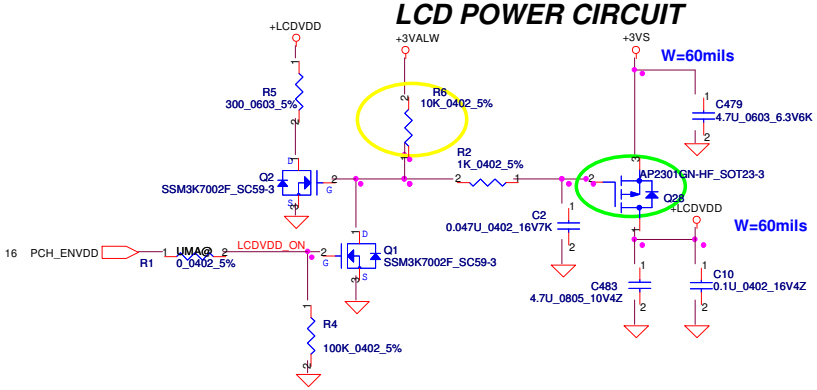
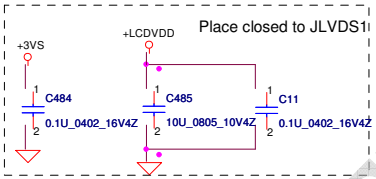
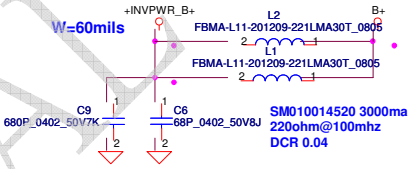
LCD POWER CIRCUIT

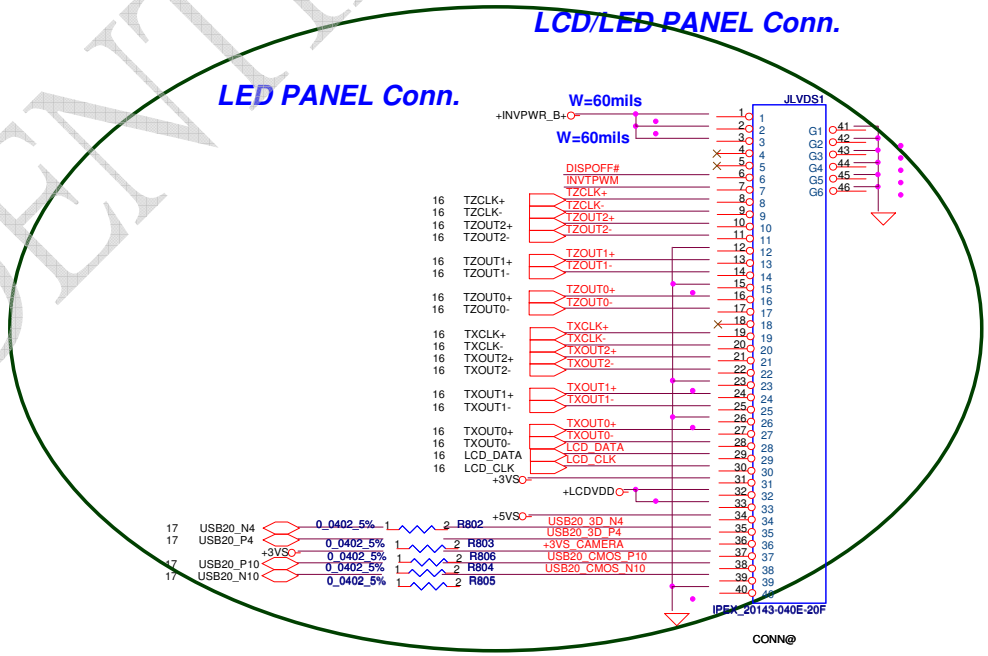


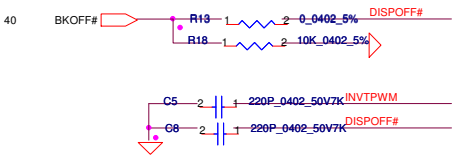


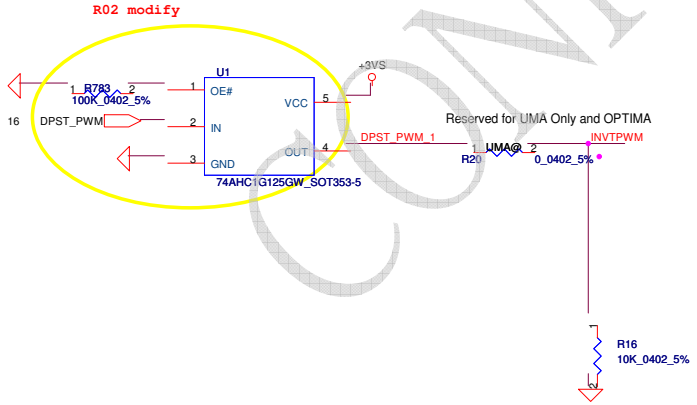


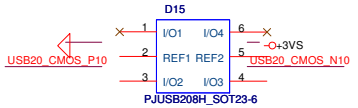
LCD/LED PANEL Conn.

LED PANEL Conn.









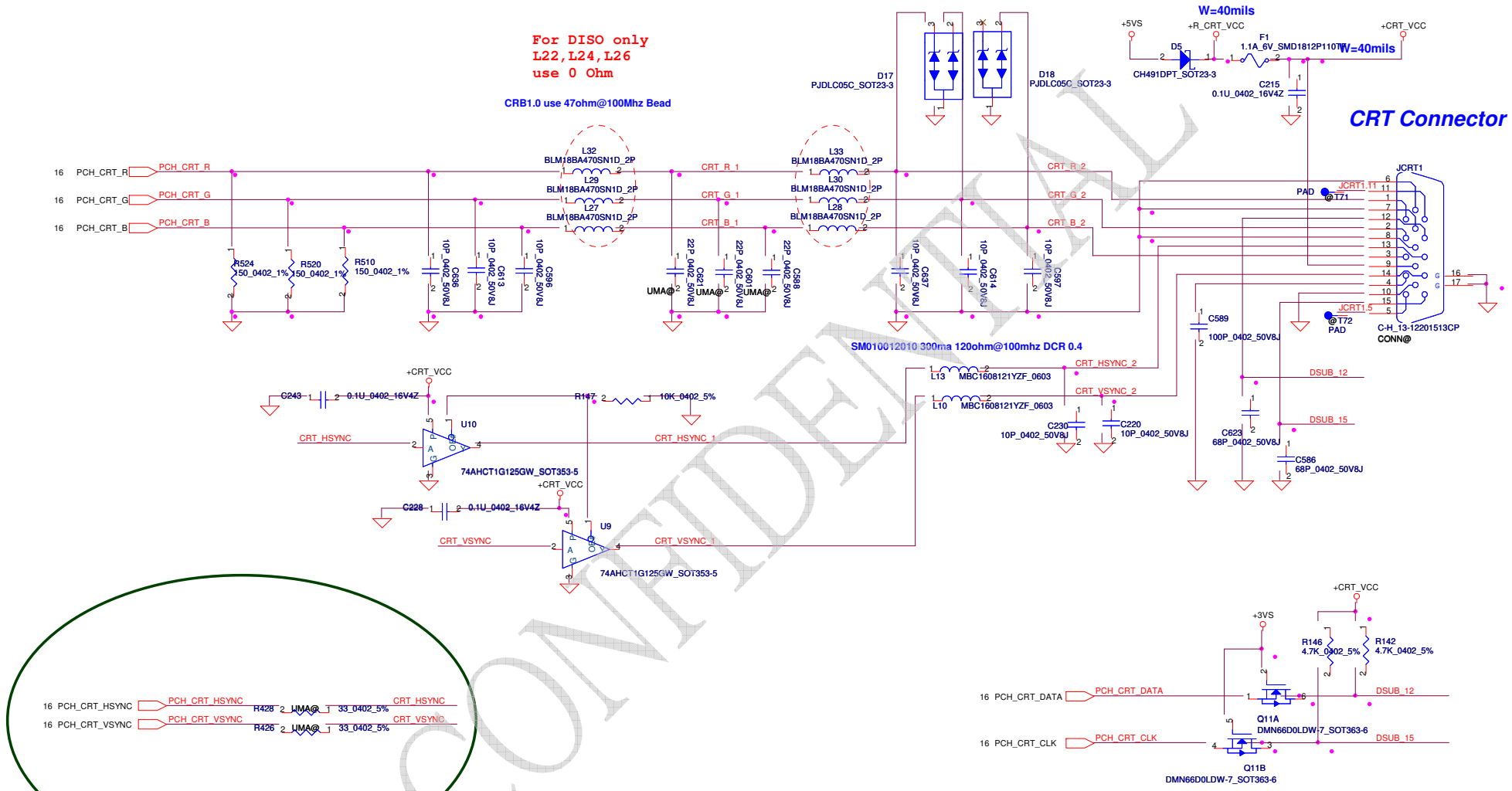
Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

Date: Wednesday, October 27, 2010 | Sheet 31 of 61



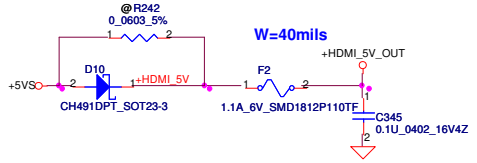
Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

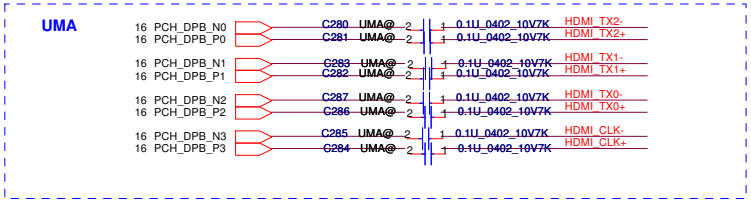
Compal Electronics, Inc.

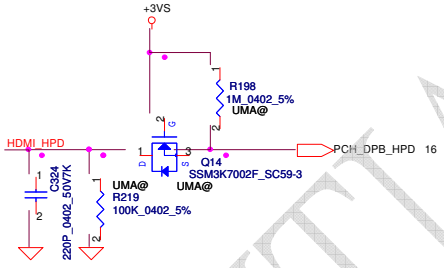
Title: CRT Connector

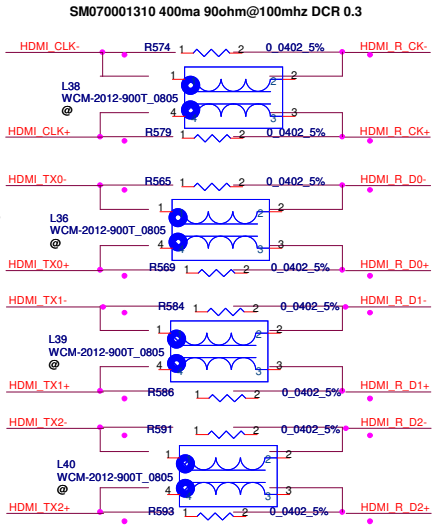
Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

Date: Wednesday, October 27, 2010 | Sheet 32 of 61

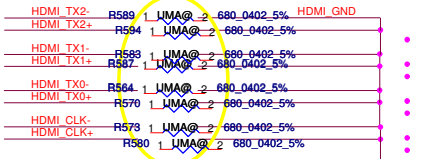




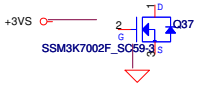




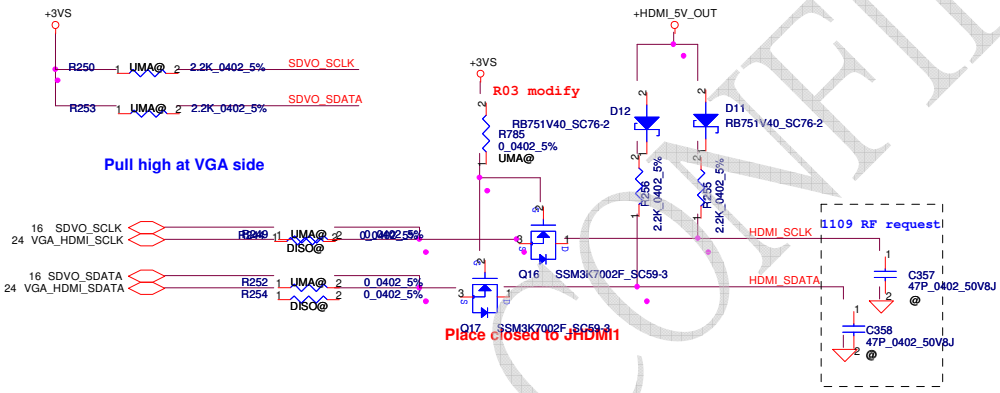
R03 modify



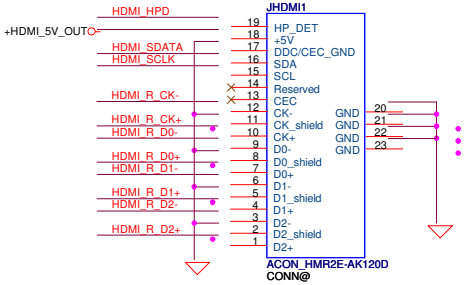
INTEL use 680 Ohm for terminationn in DG 1.5



NV use 499 Ohm for terminationn



HDMI connector



Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: HDMI Conn

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 1.0

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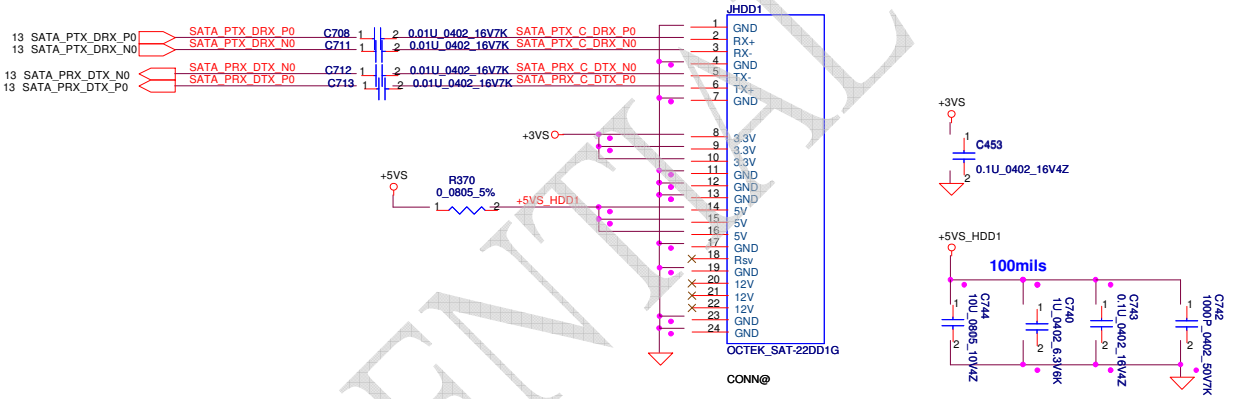
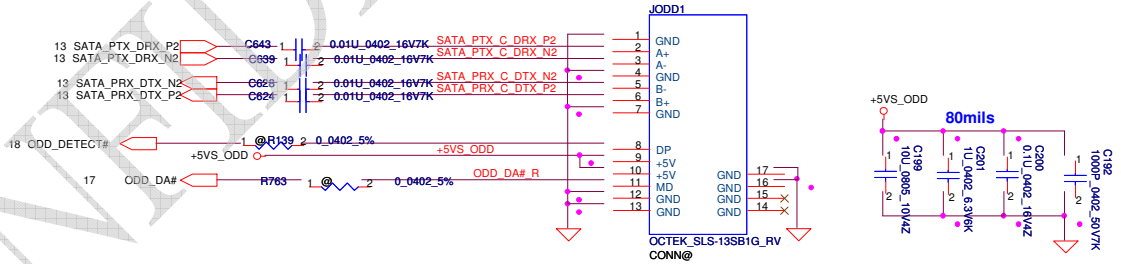
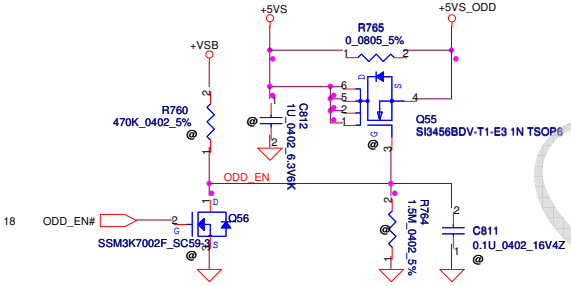
SATA HDD1 Conn.



SATA ODD Conn.





Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: HDD & ODD Connector

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

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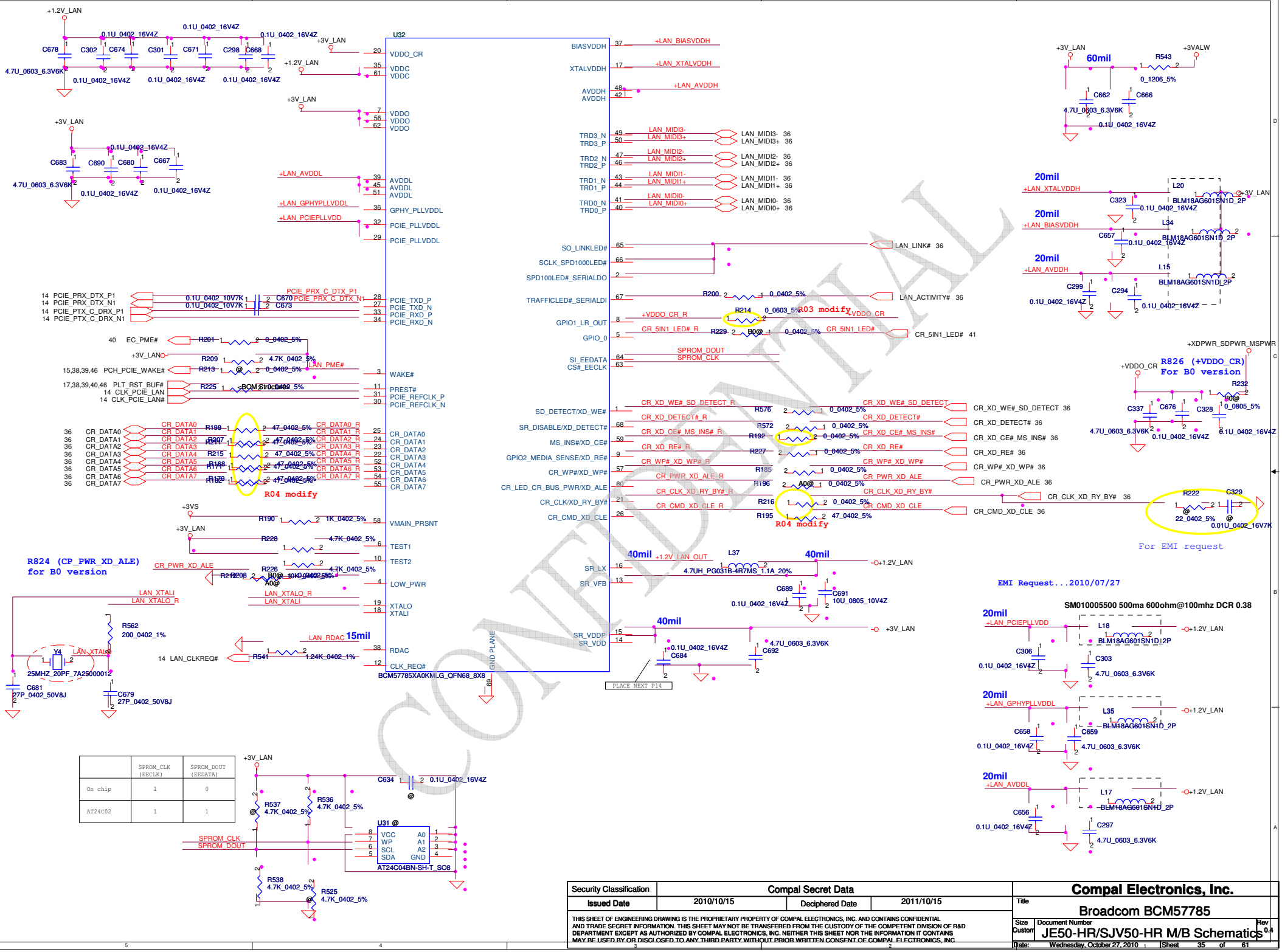

	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: Broadcom BCM57785

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

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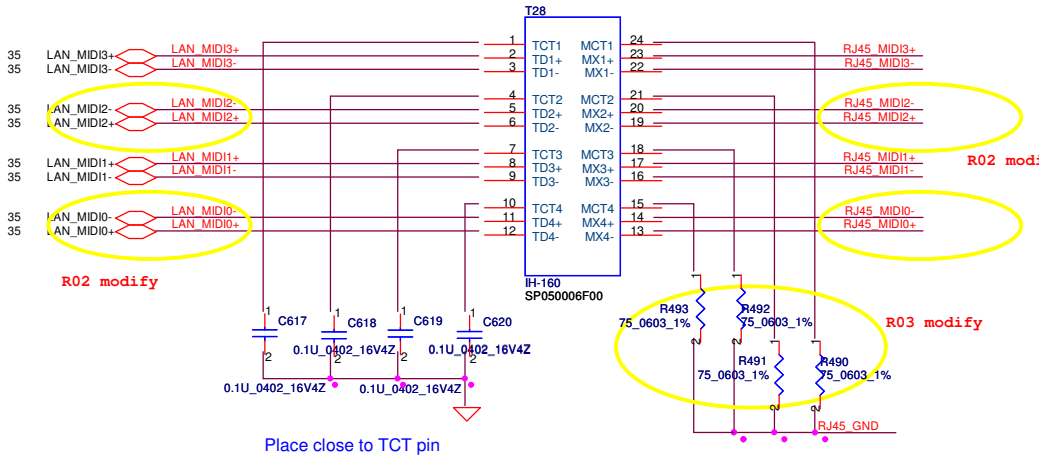
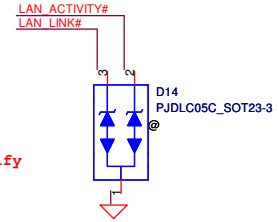
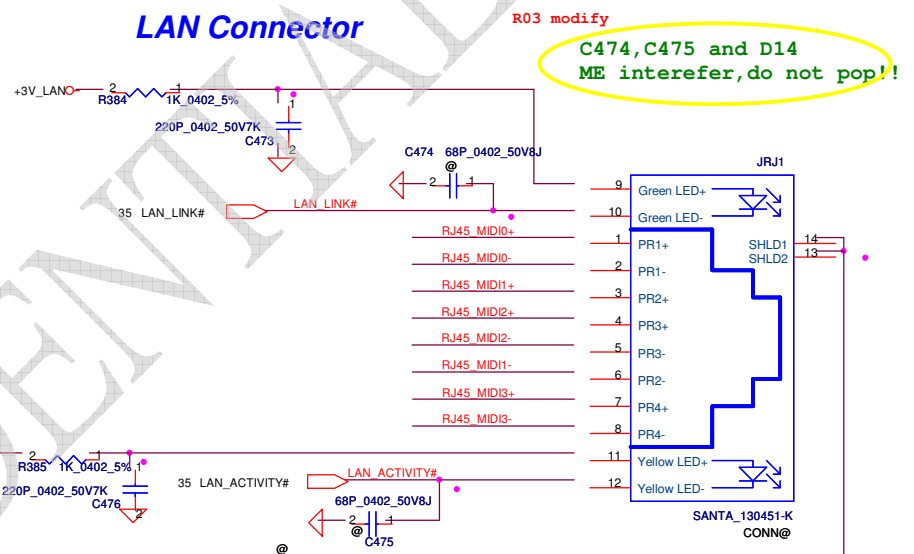


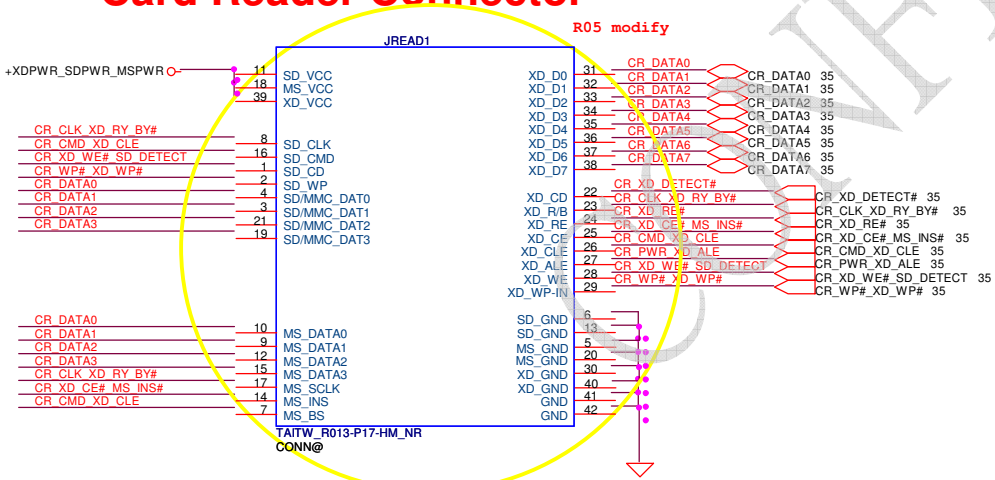


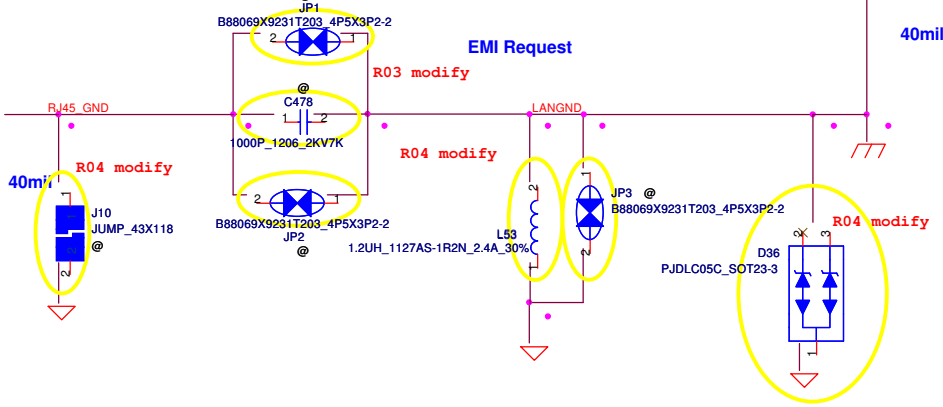
BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00

LAN Connector



Card Reader Connector





Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

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Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: RTS5138 Card Reader

Size	Document Number	Rev
Custom	JE50-HR/SJV50-HR M/B Schematics	0.4

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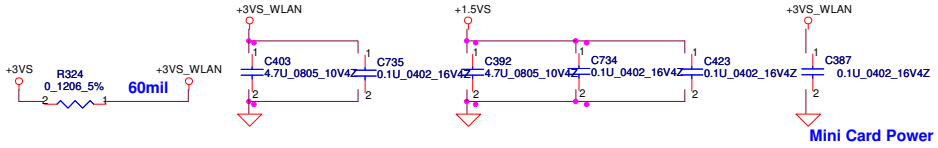
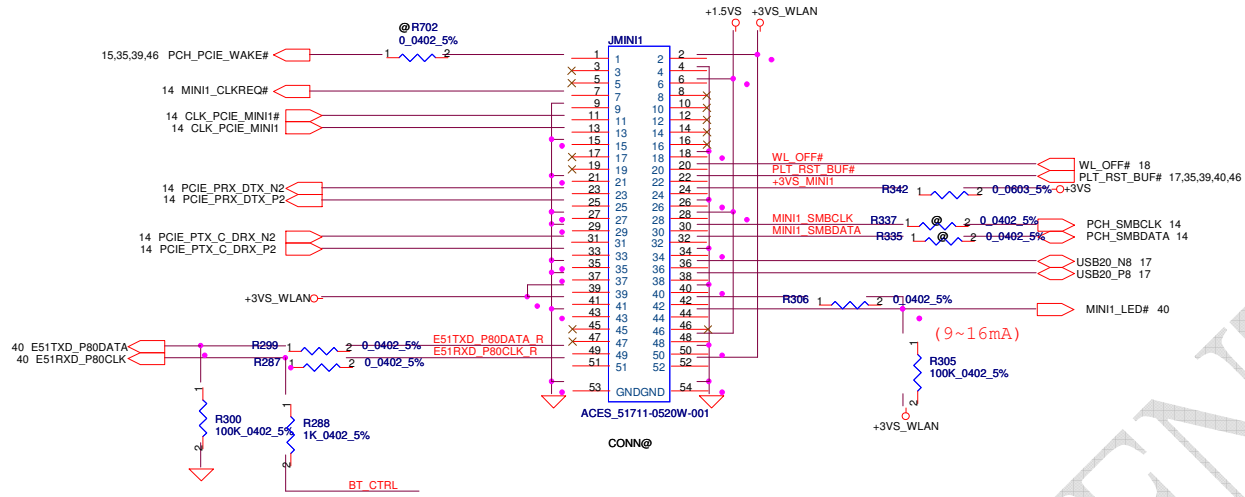
For Wireless LAN

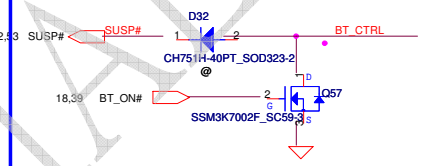


Mini Card Power Rating

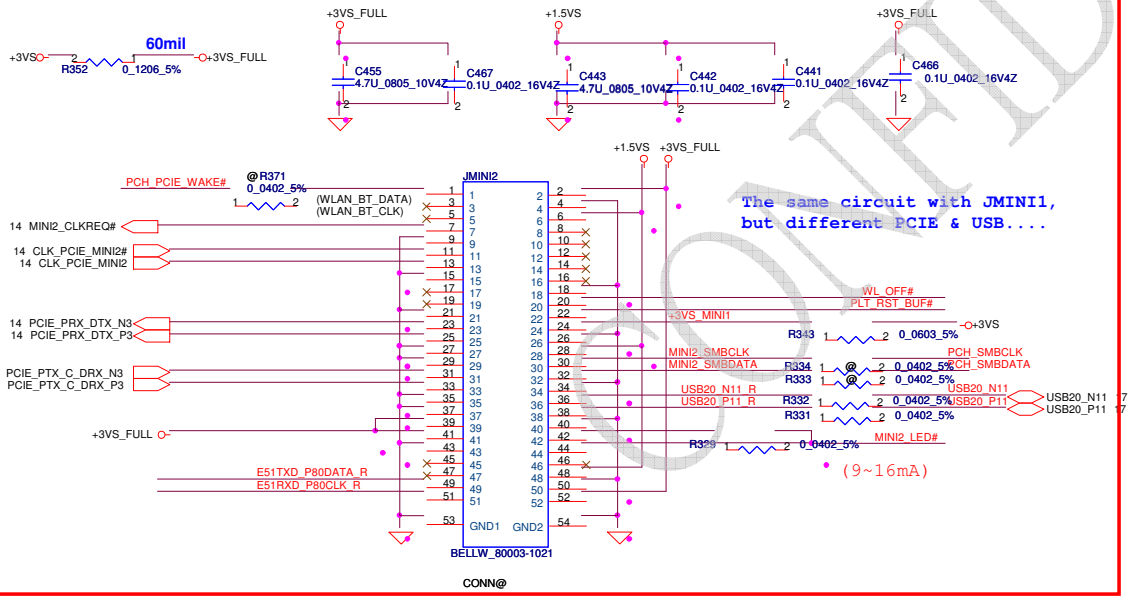


WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H



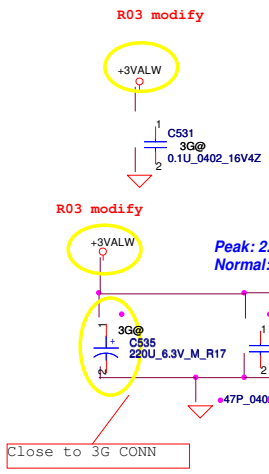
Reserve

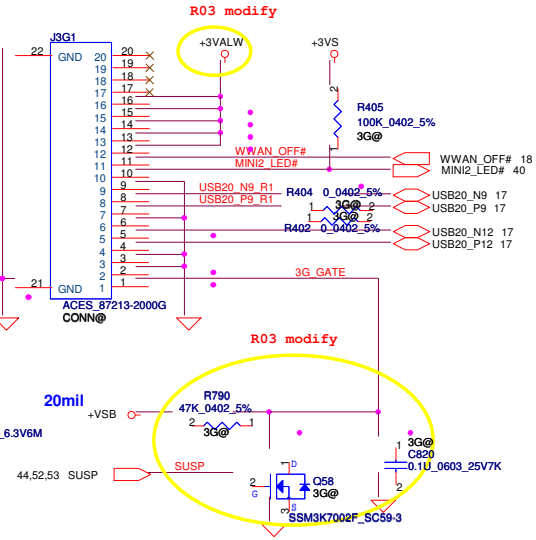


The same circuit with JMINI1, but different PCIE & USB....

For 3G / GPS

To 3G Module Connect





Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: MINI CARD (WLAN & TV-Tuner)

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

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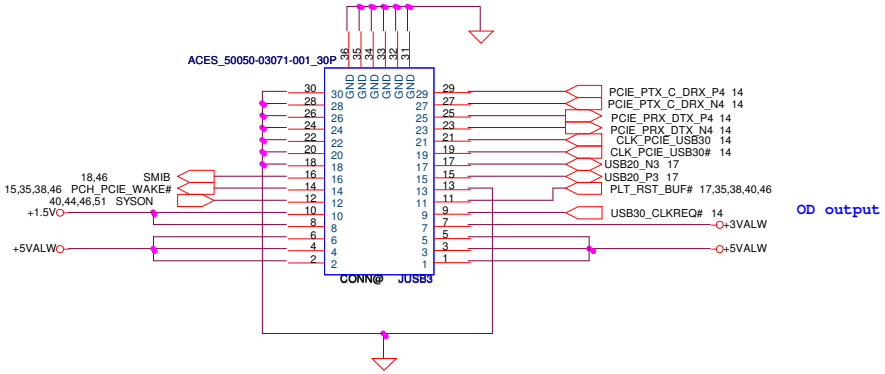
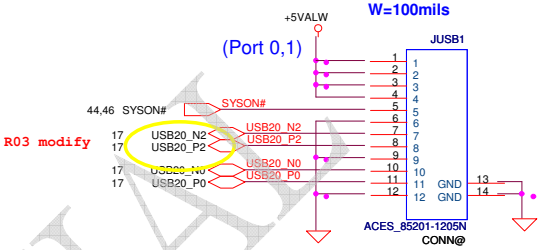
USB3.0 Conn.

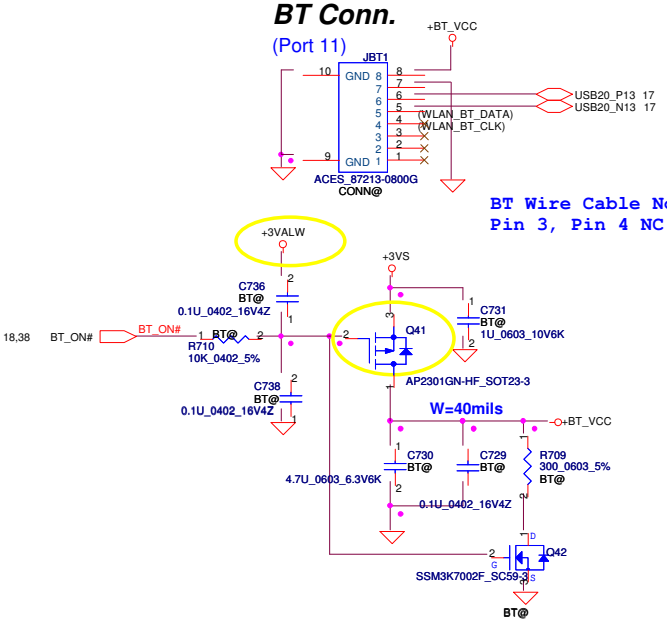


OD output

USB/B Conn.



BT Conn.



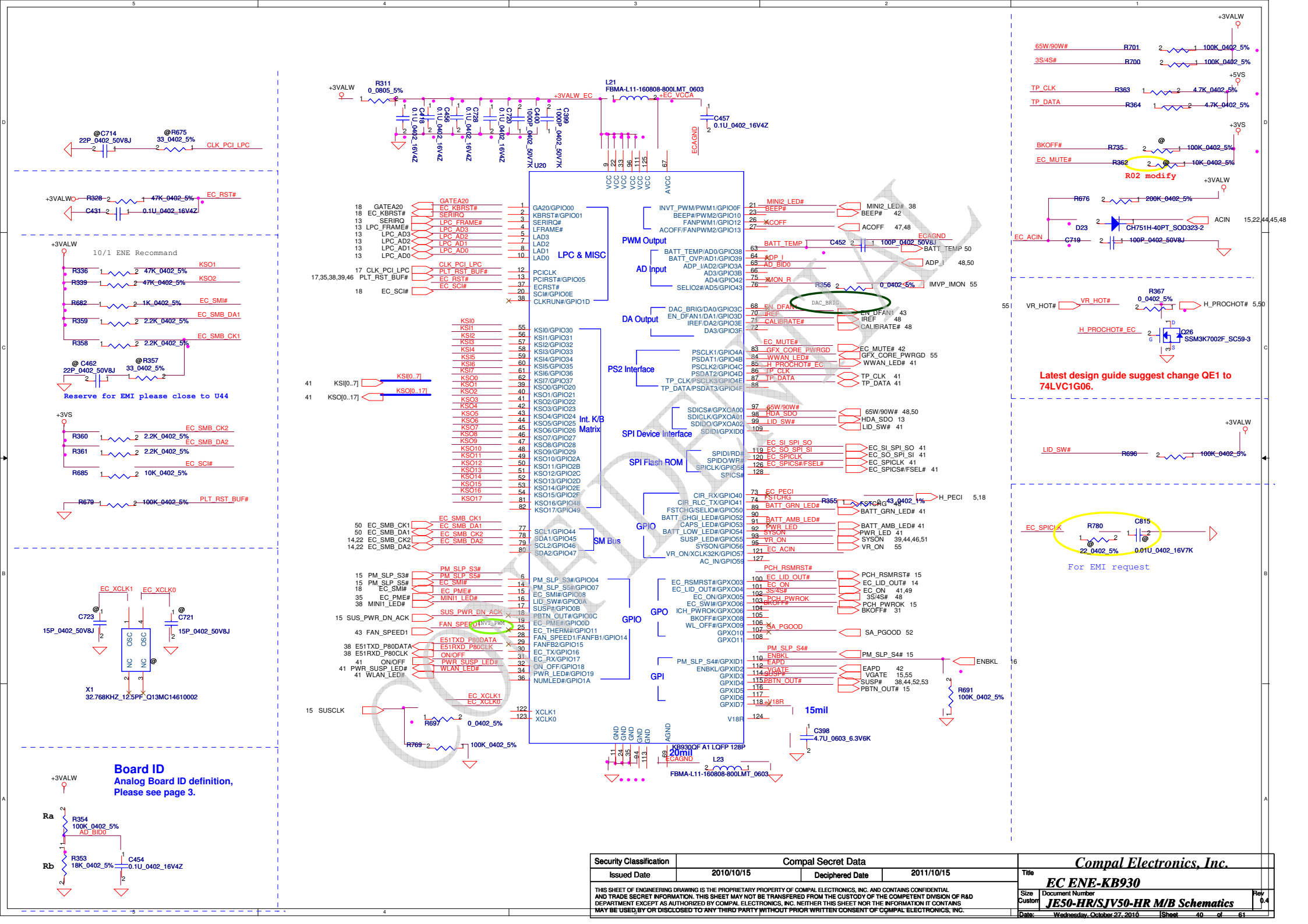
Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: USB / BT / USBB

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

Date: Wednesday, October 27, 2010 | Sheet 39 of 61


Board ID
Analog Board ID definition,
Please see page 3.
Reserve for EMI please close to U44
10/1 ENE Recommand
Latest design guide suggest change QE1 to 74LVC1G06.
For EMI request
R02 modify
15mil
20mil
KB930QF A1 LQFP 128P
X1
32.768KHZ_12.5PF_Q13MC14610002
Security Classification
Compal Secret Data
Issued Date
2010/10/15
Deciphered Date
2011/10/15
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Document Number
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Rev
0.4
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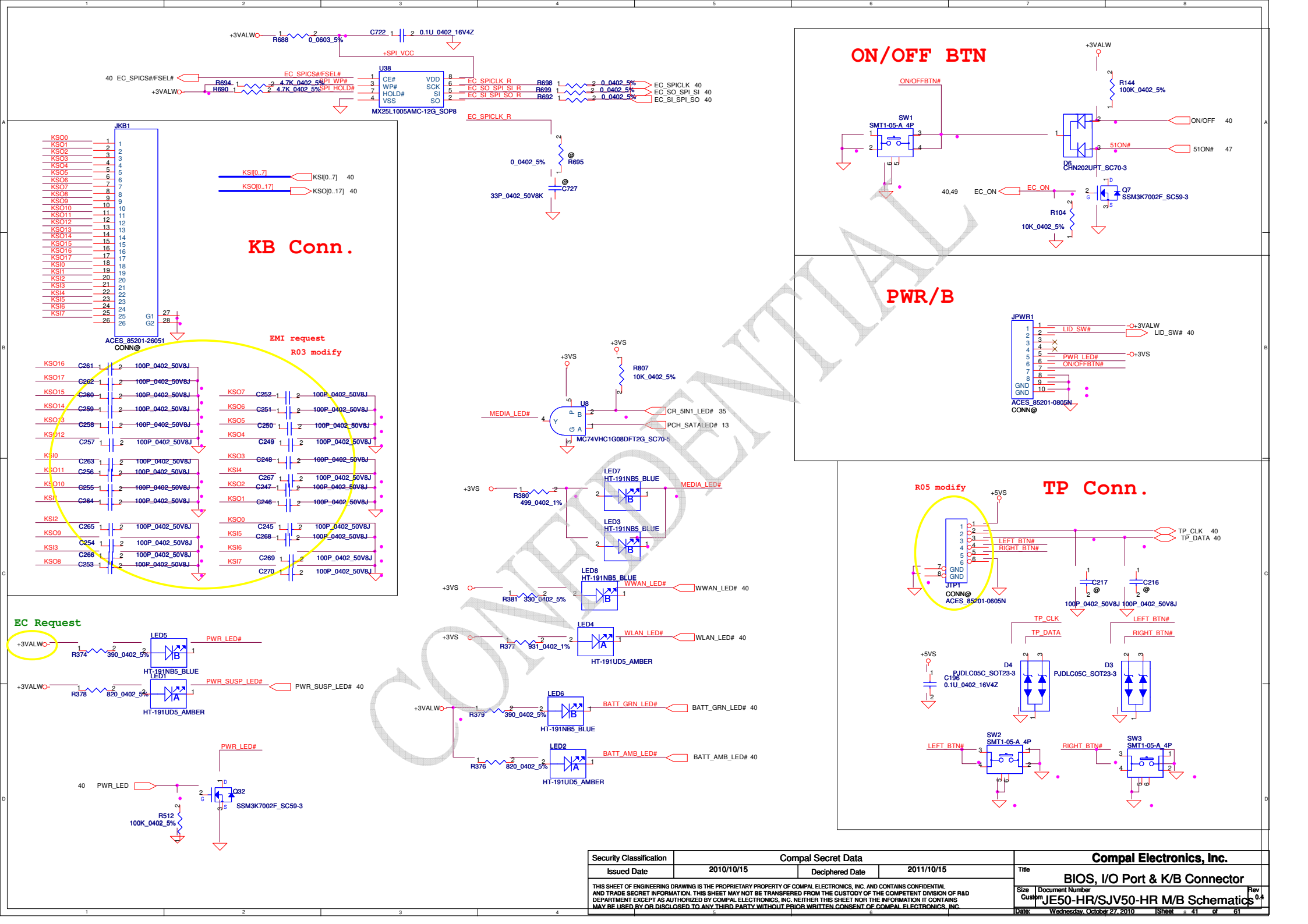

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

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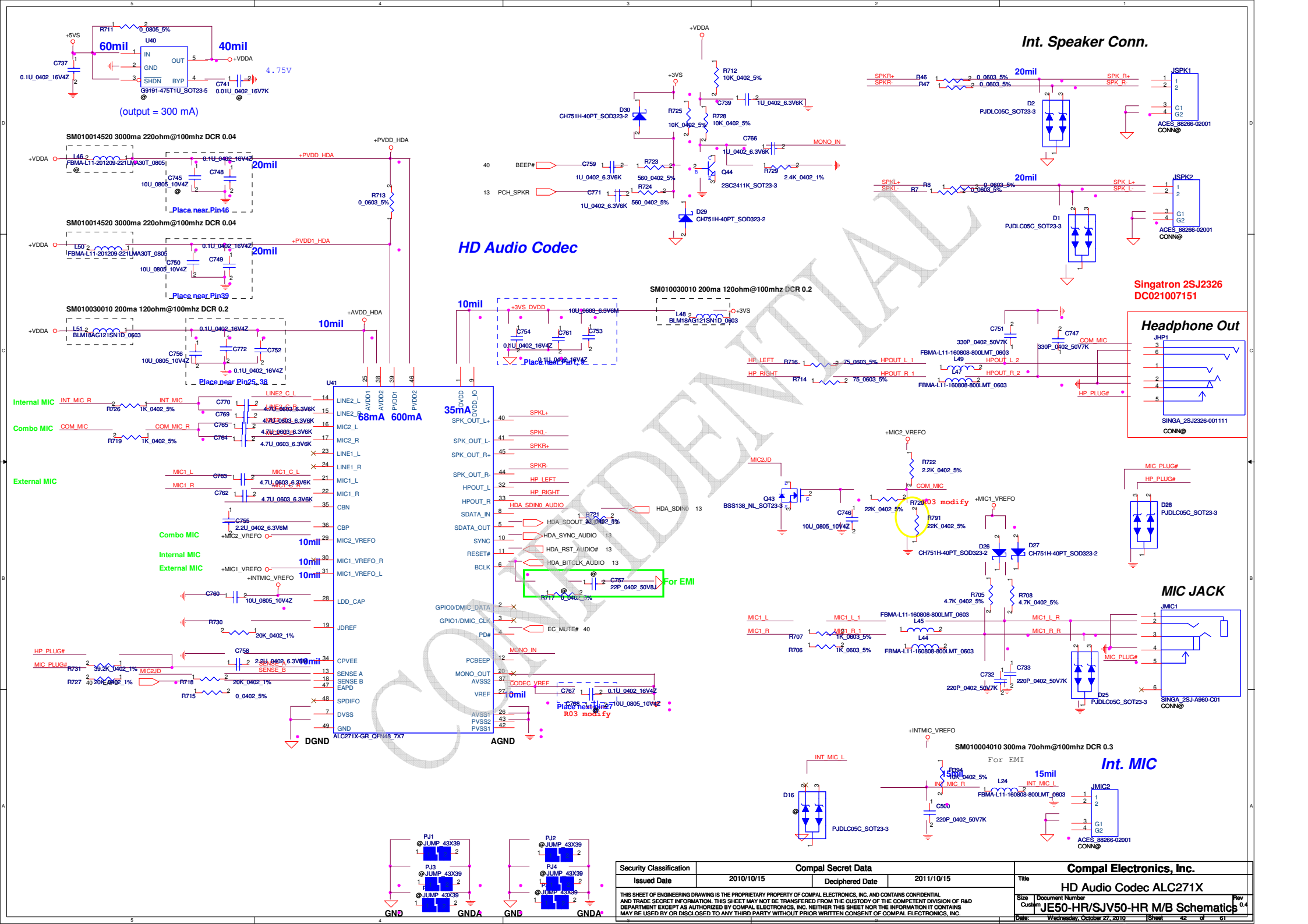

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Compal Electronics, Inc.

Title: HD Audio Codec ALC271X

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FAN Stand-Off

JUSB3 Stand-Off

H1 H_3P4 H2 H_3P4 H3 H_3P4 H4 H_3P4 H5 H_3P4 H6 H_3P4 H7 H_3P4

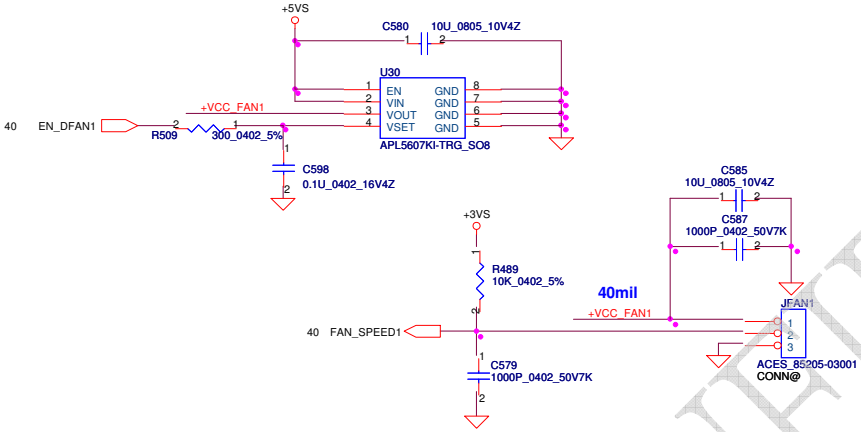
H8 H_3P0 H9 H_3P0 H10 H_3P0 H11 H_3P0 H12 H_3P0 H13 H_3P0 H14 H_3P0 H15 H_3P0 H16 H_3P0 H17 H_3P0 H18 H_3P0

H19 H_4P0 H20 H_4P0

H21 H_4P2 H22 H_4P2 H23 H_4P2 H24 H_4P2

H25 H_7P0N H26 H_3P0N H27 H_3P5X3P0N

FAN1 Conn



FD1 FIDUCIAL_C40M80 FD3 FIDUCIAL_C40M80 FD2 FIDUCIAL_C40M80 FD4 FIDUCIAL_C40M80

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: FAN & Screw Hole

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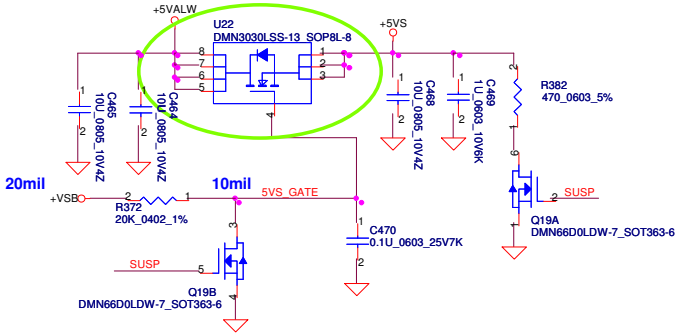
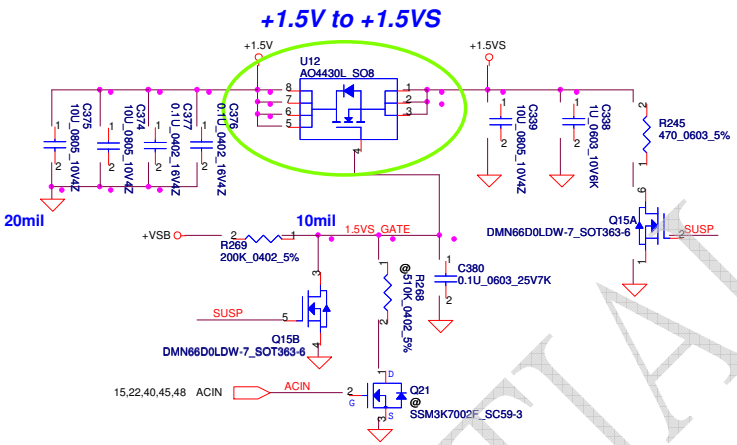
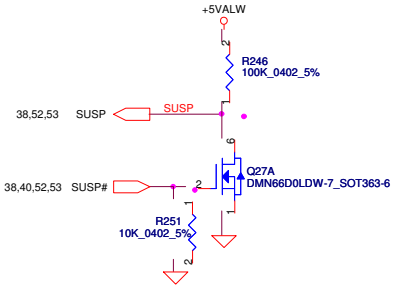
+5VALW TO +5VS

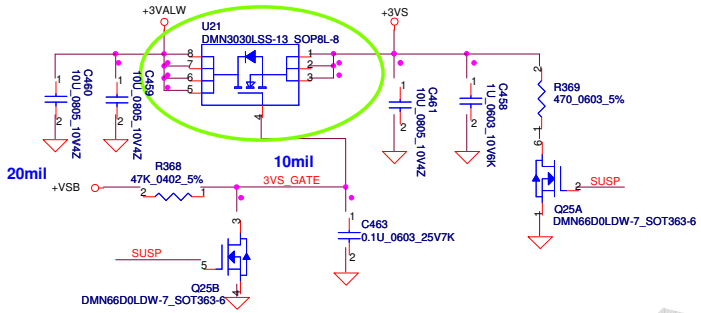


+1.5V to +1.5VS

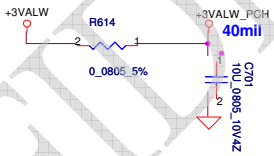


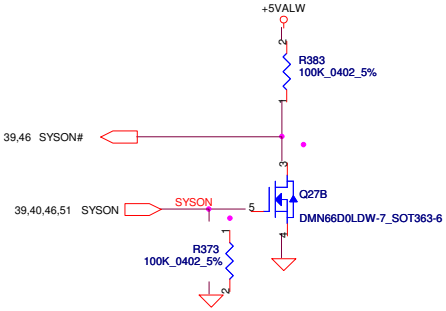


+3VALW TO +3VS

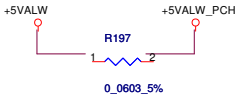


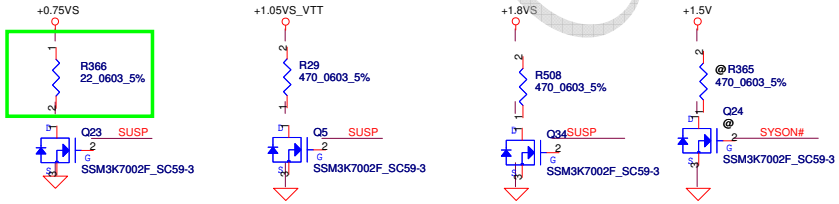
+3VALW TO +3VALW_PCH(PCH AUX Power)





+5VALW TO +5VALW_PCH(PCH AUX Power)





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Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

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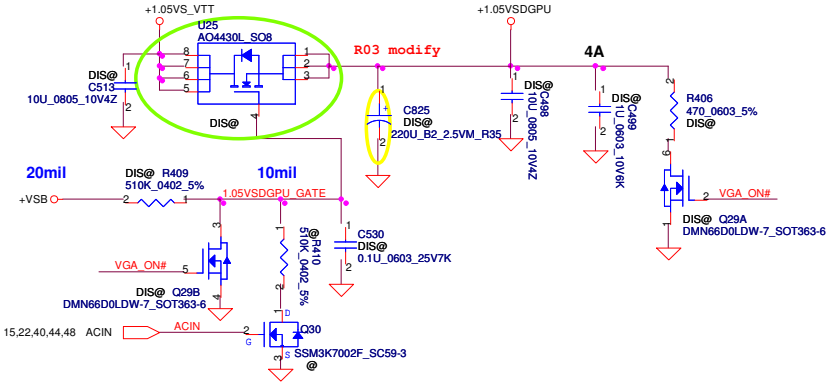
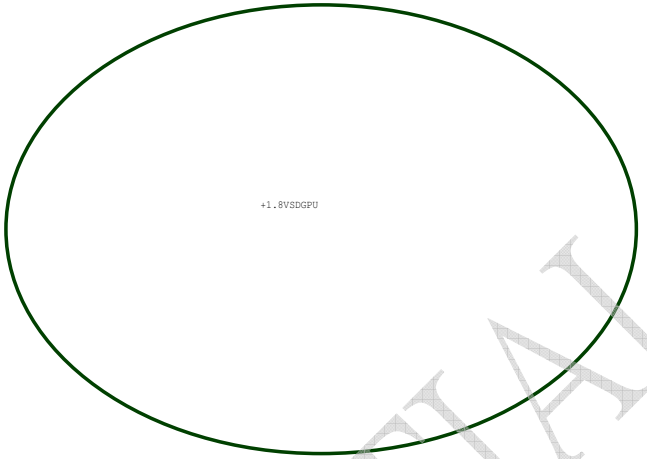
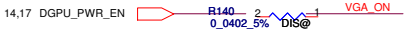
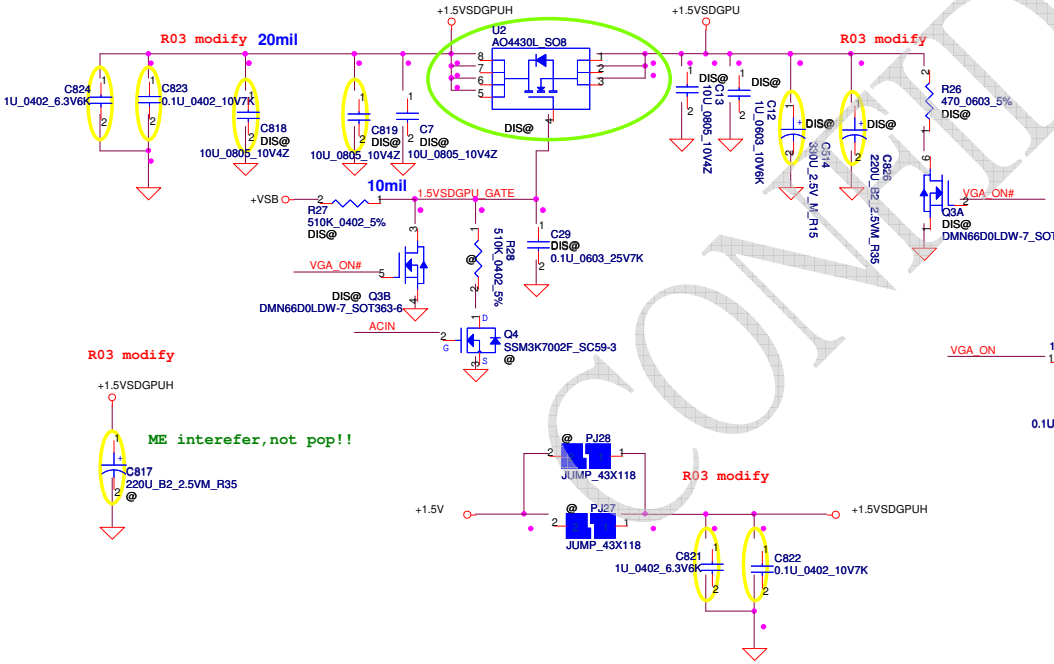
+1.05VS_VTT to +1.05VSDGPU for GPU



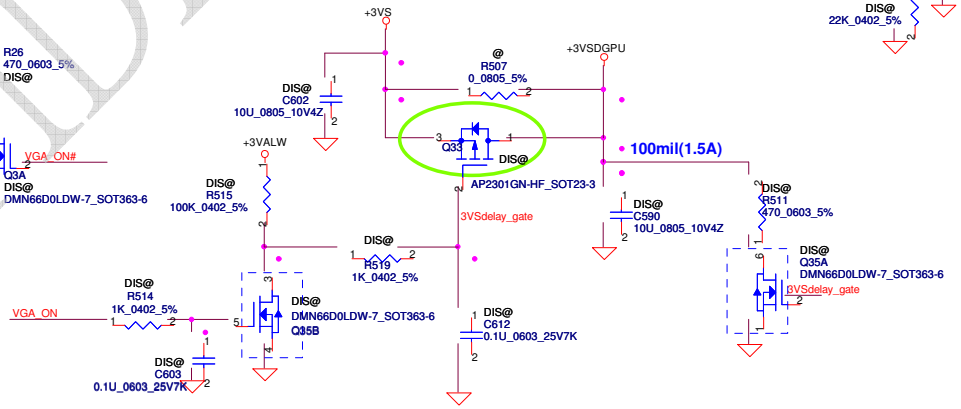


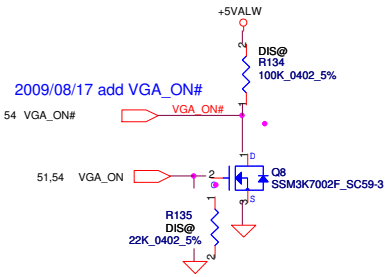


+1.5VSDGPUH to +1.5VSDGPU for GPU



+3VS to +3VSDGPU for GPU





Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

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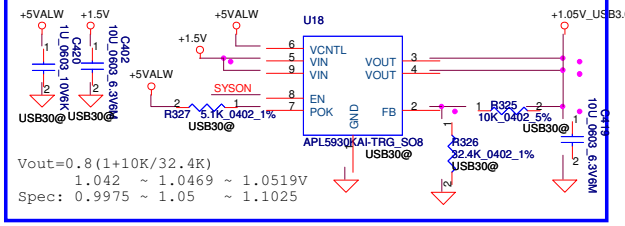
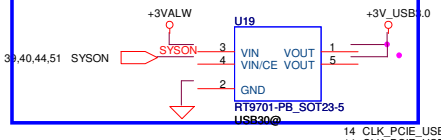
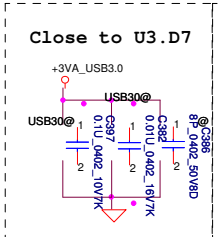
+1.5V to +1.05V Transfer



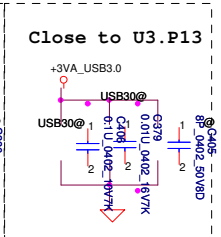
+3VALW to +3V Transfer

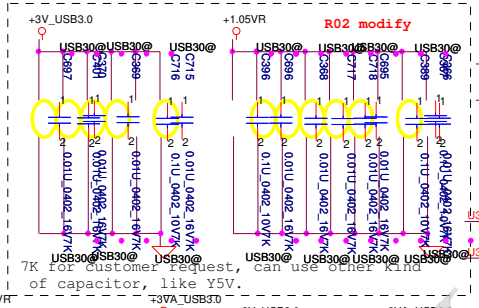


Close to U3.D7

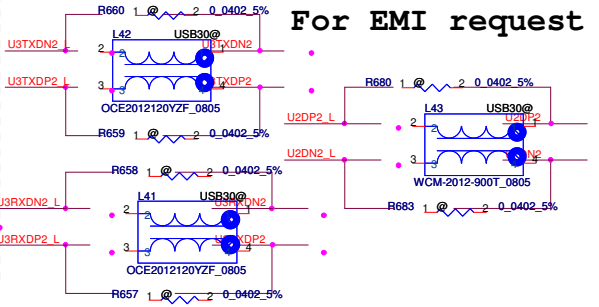


Close to U3.P13

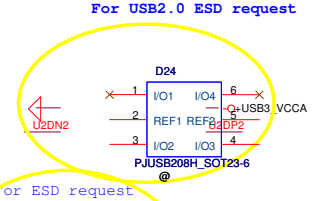


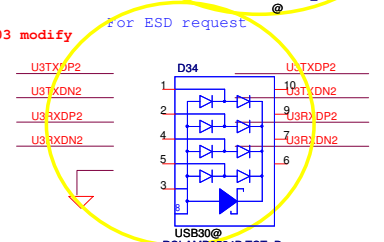


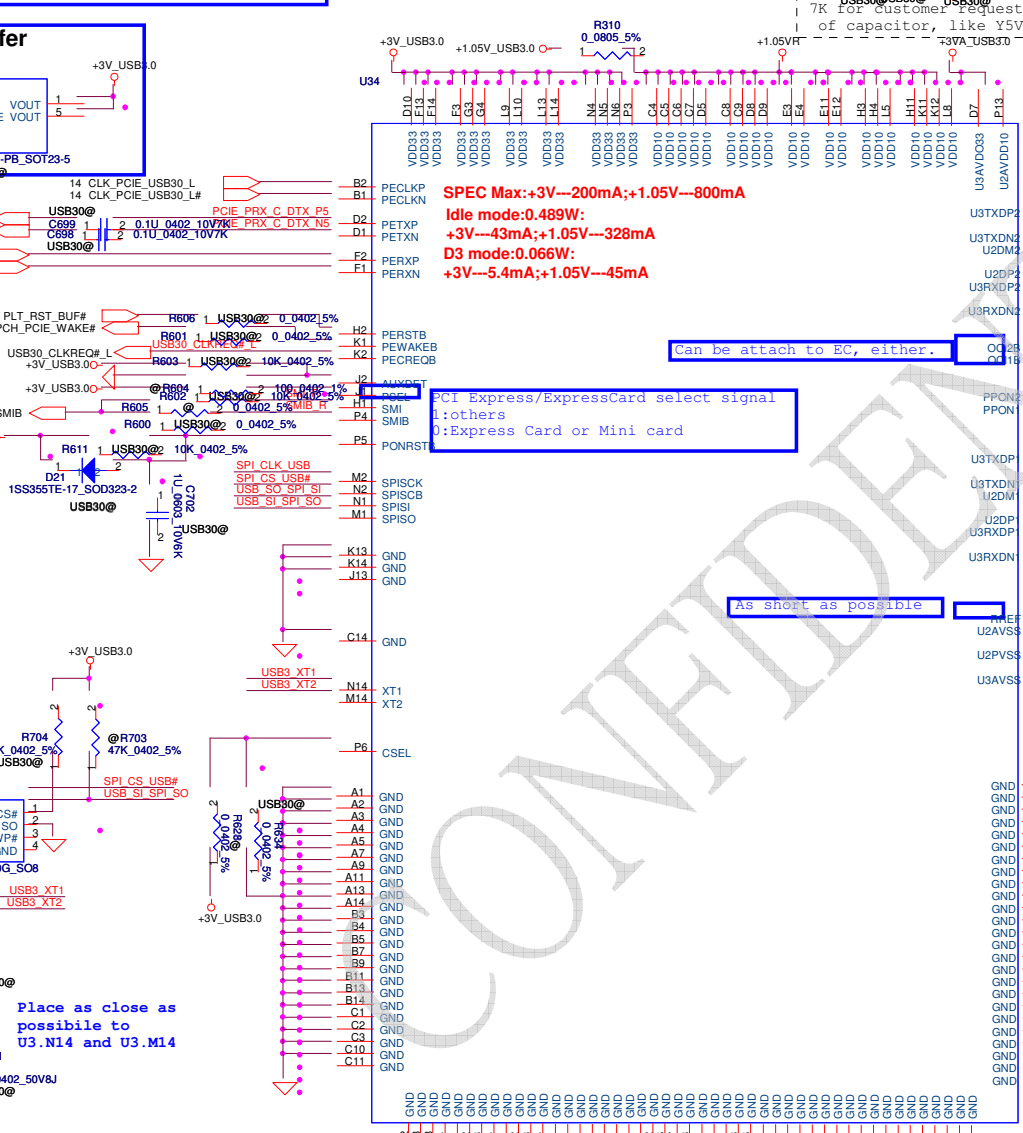
For EMI request



For USB2.0 ESD request







Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

Security Classification	Compal Secret Data		
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Title: USB3.0 PD720200

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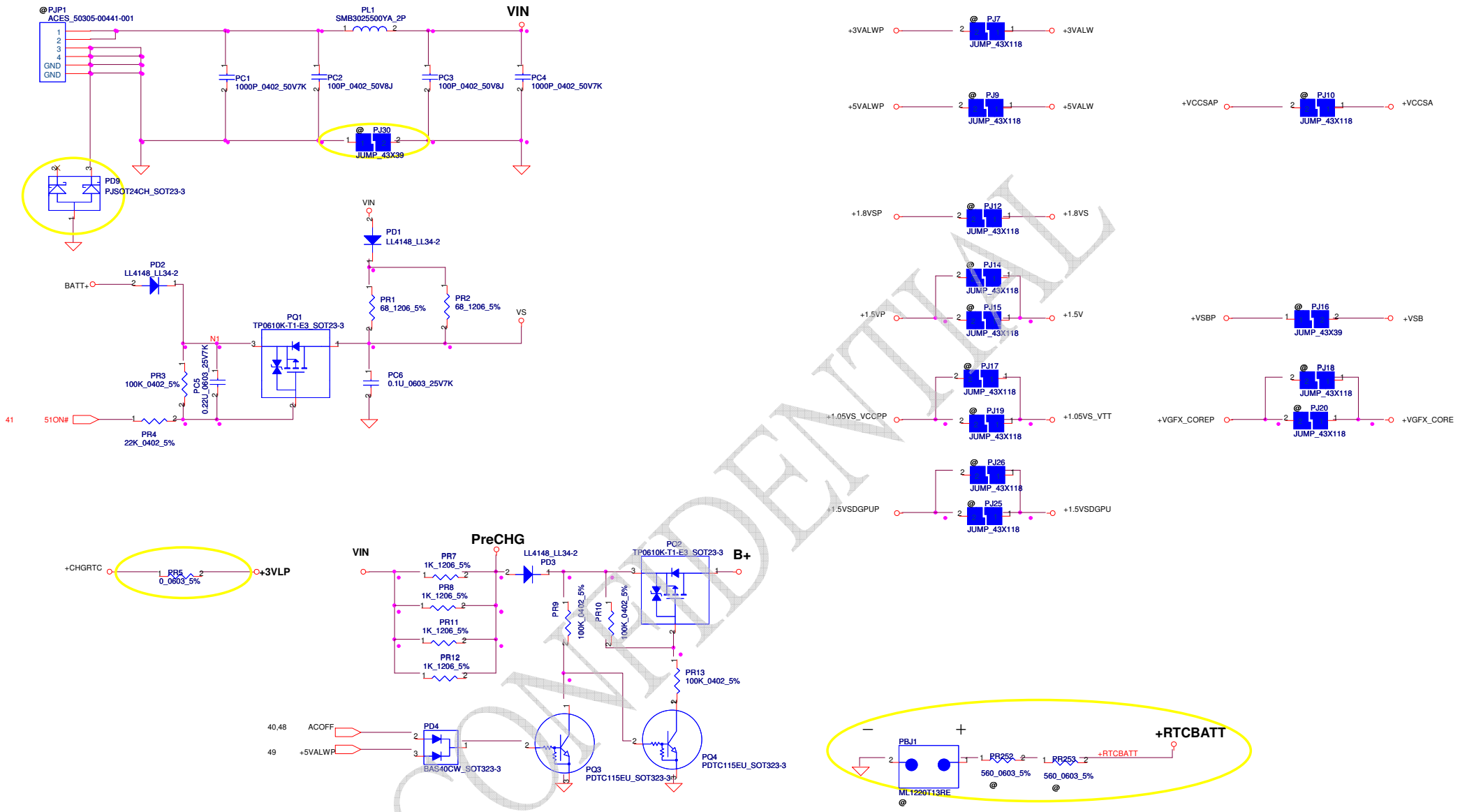

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

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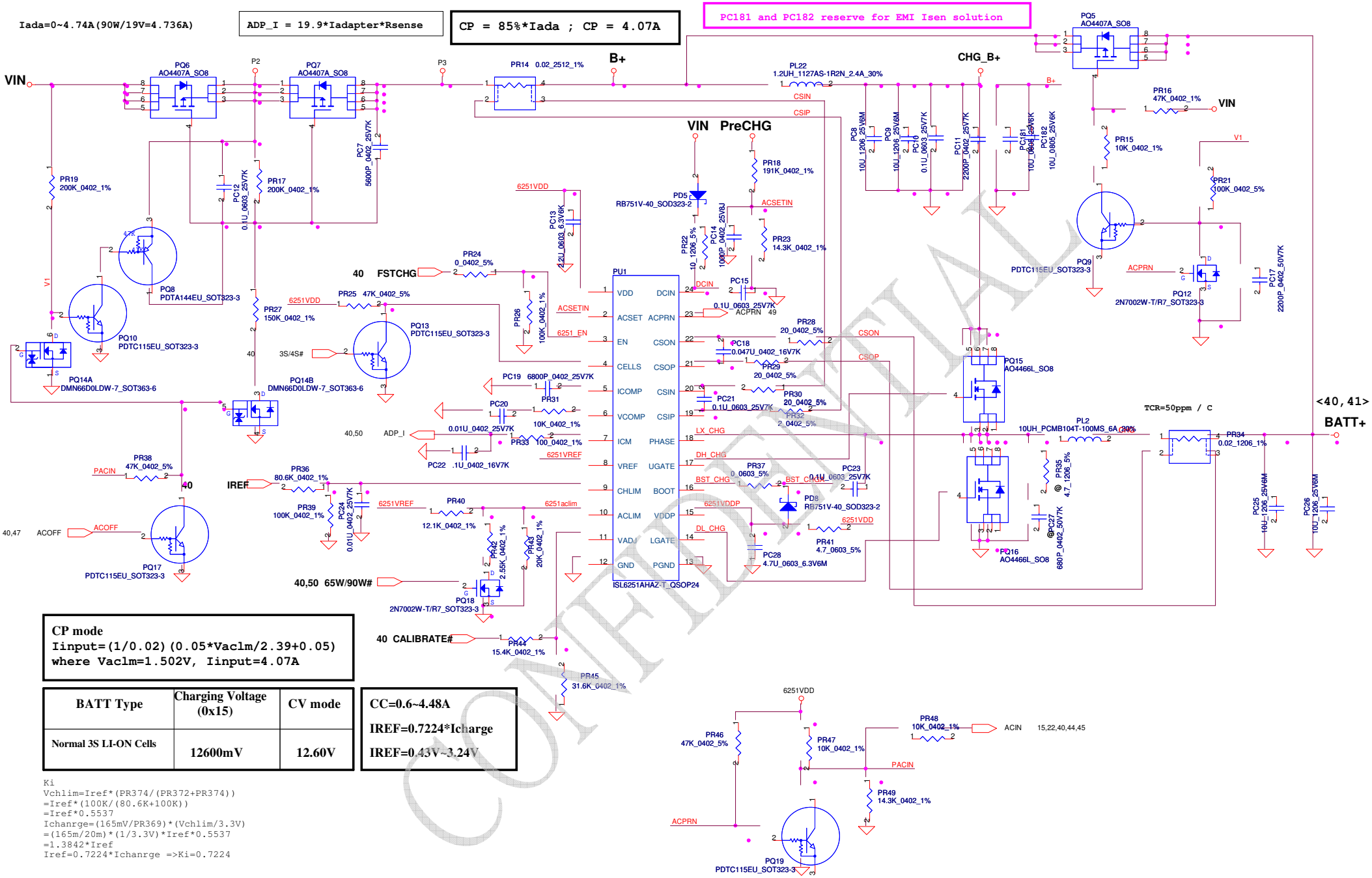
Iada=0~4.74A(90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A

PC181 and PC182 reserve for EMI Isen solution



CP mode

Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)

where Vaclm=1.502V, Iinput=4.07A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: PWR-CHARGER

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

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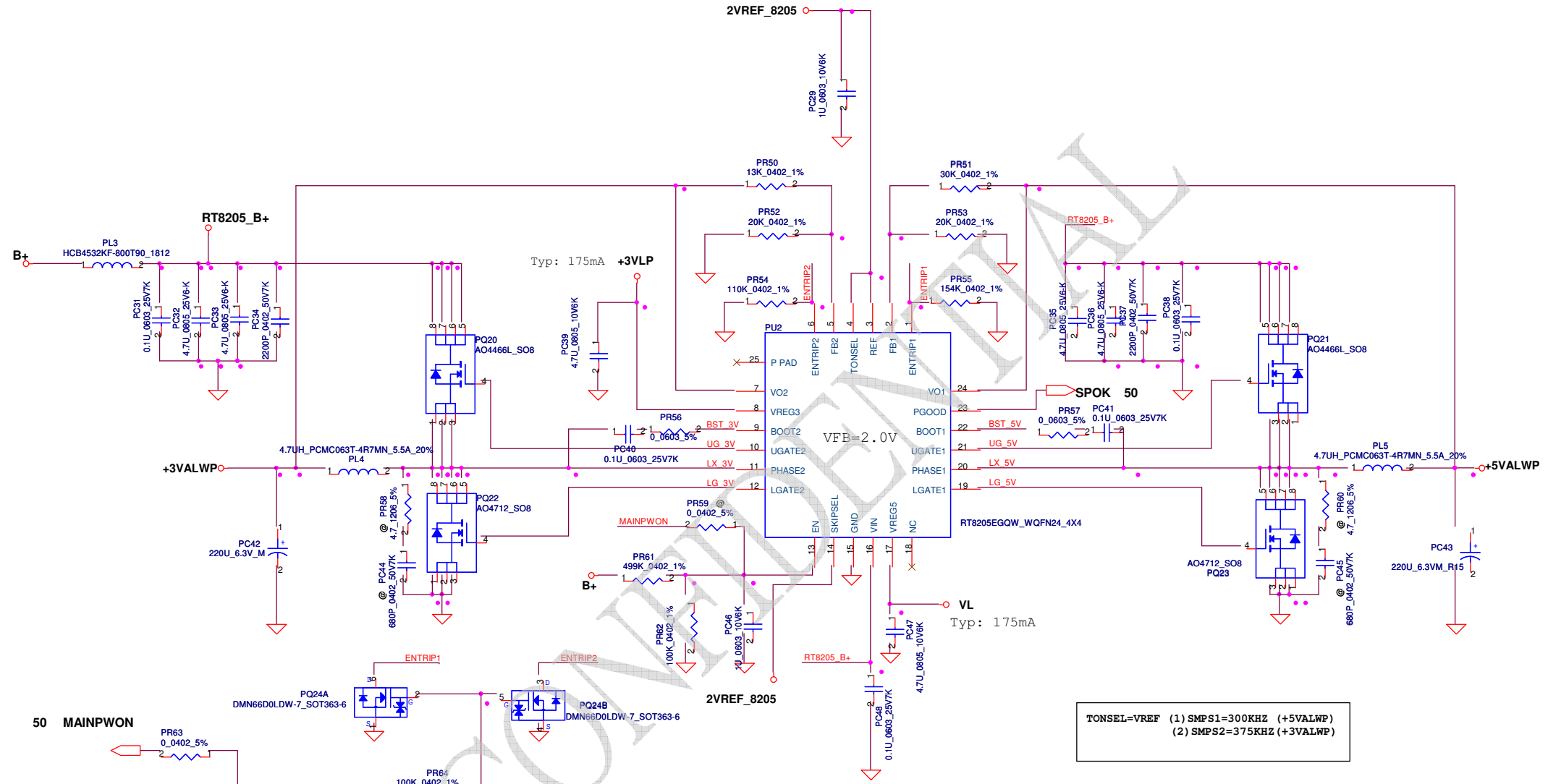

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

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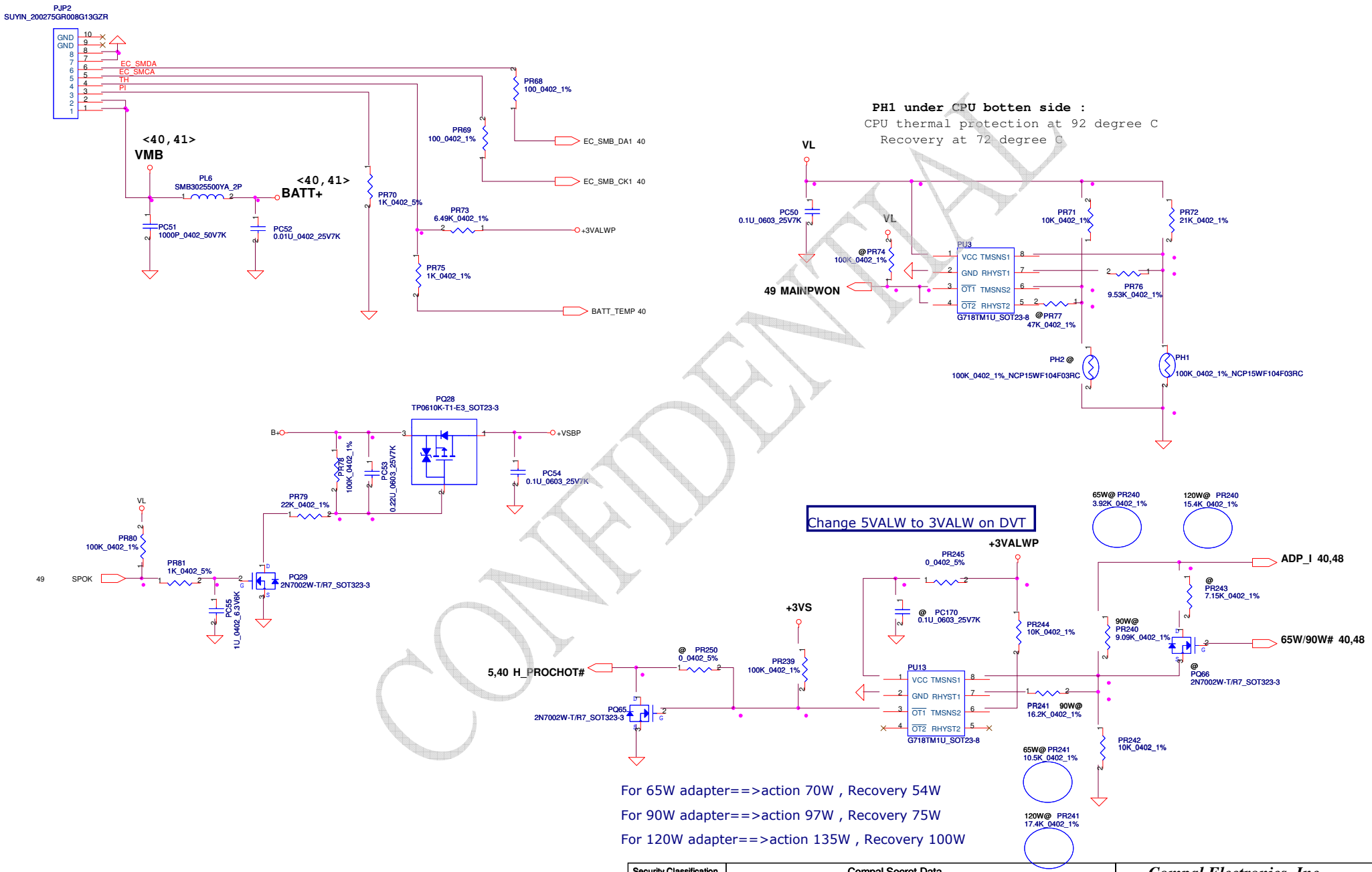

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

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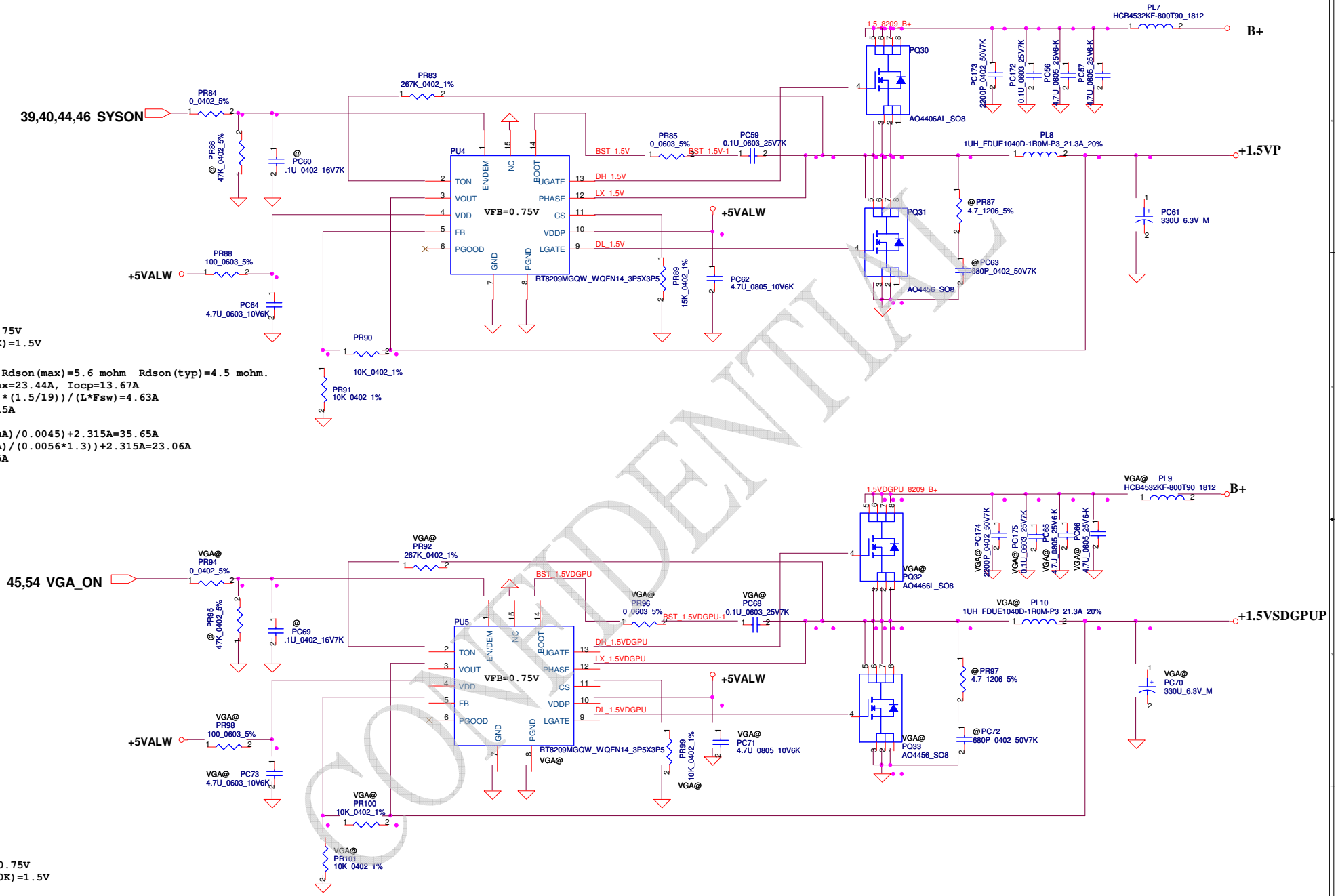

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: PWR-+1.5VP/+1.5VSDGPU

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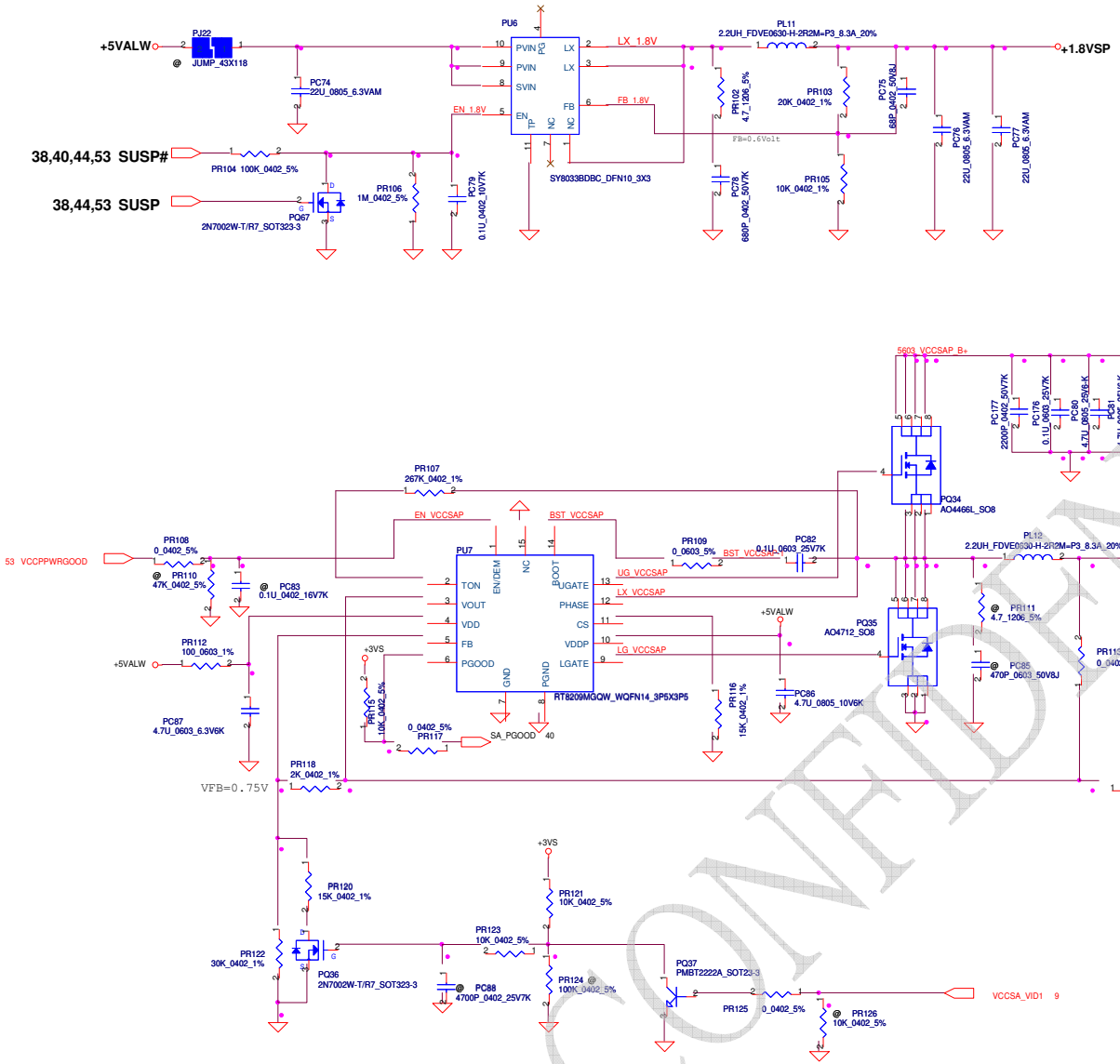
1.8VSP
Ipeak=3.35A ; 1.2Ipeak=4.02 ;Imax=2.345A
Vout=0.6*(1+(20K/10K))=1.8V



VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

<Vo=0.9V> VFB=0.75V
V=0.75*(1+2K/10K)=0.9V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=18 mohm Rdson(typ)=15 mohm.
Ipeak=6A, Imax=4.2A, Iocp=7.2A
Delta I=((19-0.9)*(0.9/19))/(L*Fsw)=1.31A
=>1/2Delta I=0.655A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.015)+0.655A=11.48A
Iocpmin=((15K*9uA)/(0.018*1.2))+0.655A=7.27A
Iocp=7.27A~11.48A

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.
Title: PWR +VCCSAP
Size: C
Document Number: JE50-HR/SJV50-HR M/B Schematics
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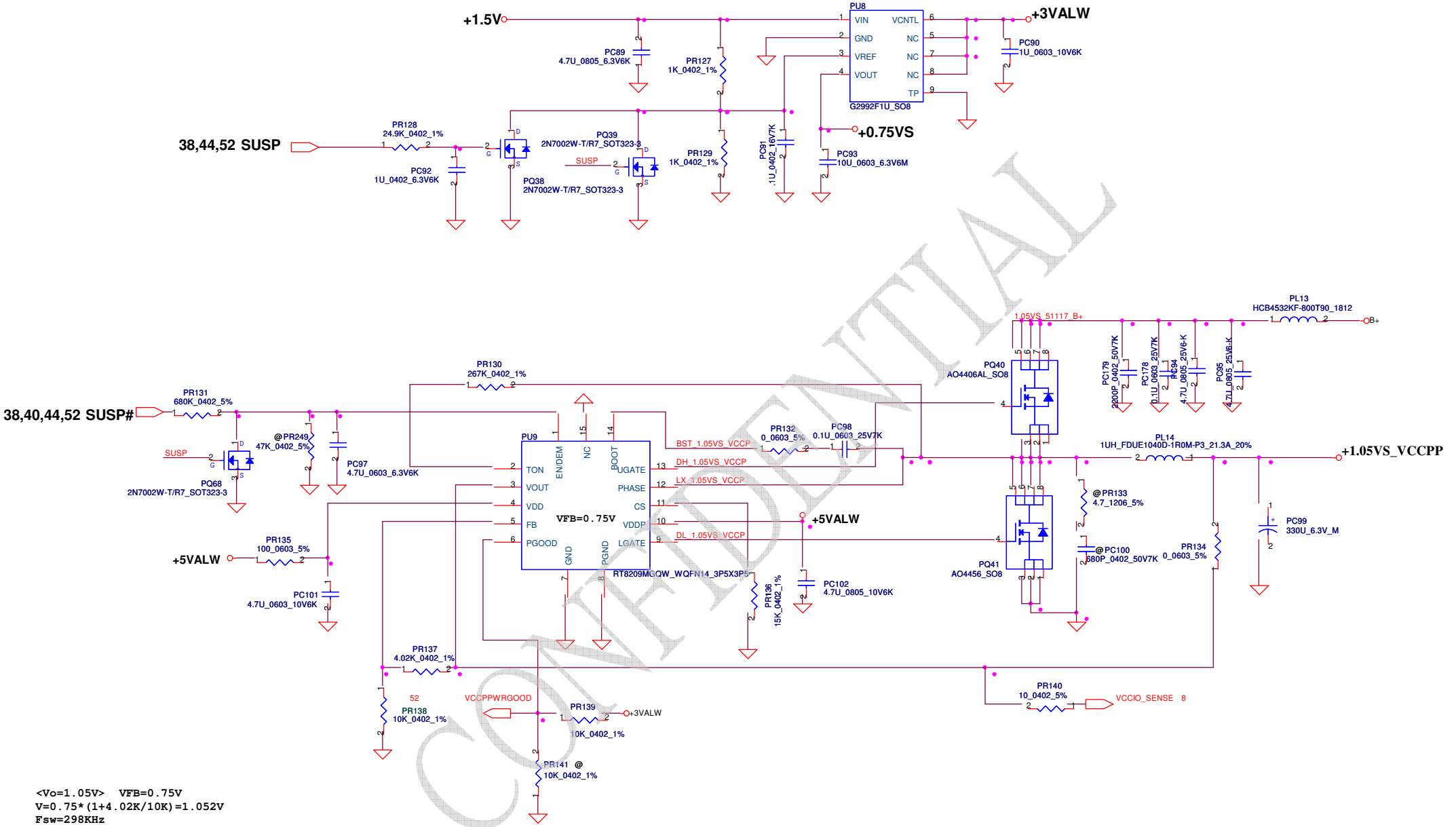

<Vo=1.05V> VFB=0.75V
V=0.75*(1+4.02K/10K)=1.052V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=12.866A, Imax=9A, Iocp=15.439A
Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=3.33A
=>1/2Delta I=1.665A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+1.665A=37.62A
Iocpmin=((15K*9uA)/(0.0056*1.3))+1.665A=23.02A
Iocp=23.02A~37.62A

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/+0.75VSP

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.4

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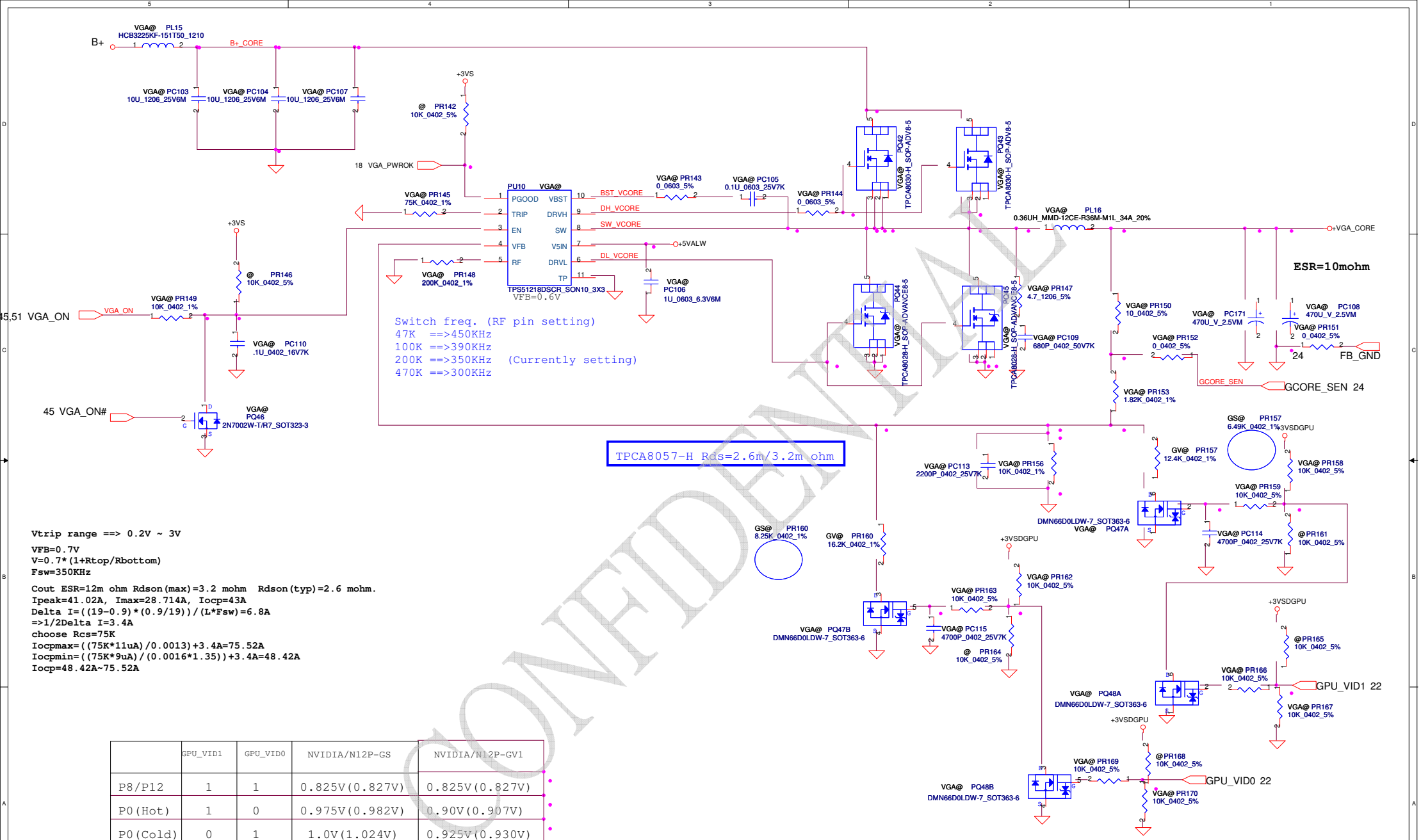

Vtrip range ==> 0.2V ~ 3V

VFB=0.7V
V=0.7*(1+Rtop/Rbottom)
Fsw=350KHz

Cout ESR=12m ohm Rdson(max)=3.2 mohm Rdson(typ)=2.6 mohm.
Ipeak=41.02A, Imax=28.714A, Iocp=43A
Delta I=((19-0.9)*(0.9/19))/(L*Fsw)=6.8A
=>1/2Delta I=3.4A
choose Rcs=75K
Iocpmax=((75K*11uA)/0.0013)+3.4A=75.52A
Iocpmin=((75K*9uA)/(0.0016*1.35))+3.4A=48.42A
Iocp=48.42A~75.52A

	GPU_VID1	GPU_VID0	NVIDIA/N12P-GS	NVIDIA/N12P-GV1
P8/P12	1	1	0.825V(0.827V)	0.825V(0.827V)
P0(Hot)	1	0	0.975V(0.982V)	0.90V(0.907V)
P0(Cold)	0	1	1.0V(1.024V)	0.925V(0.930V)
	0	0	----	----

Security Classification	Compal Secret Data	AP	
Issued Date	2010/10/15	Deciphered Date	2011/10/15

Compal Electronics, Inc.

Title: **+VGA_COREP**

Size	Document Number	Rev
Custom	P5WE0	0.4

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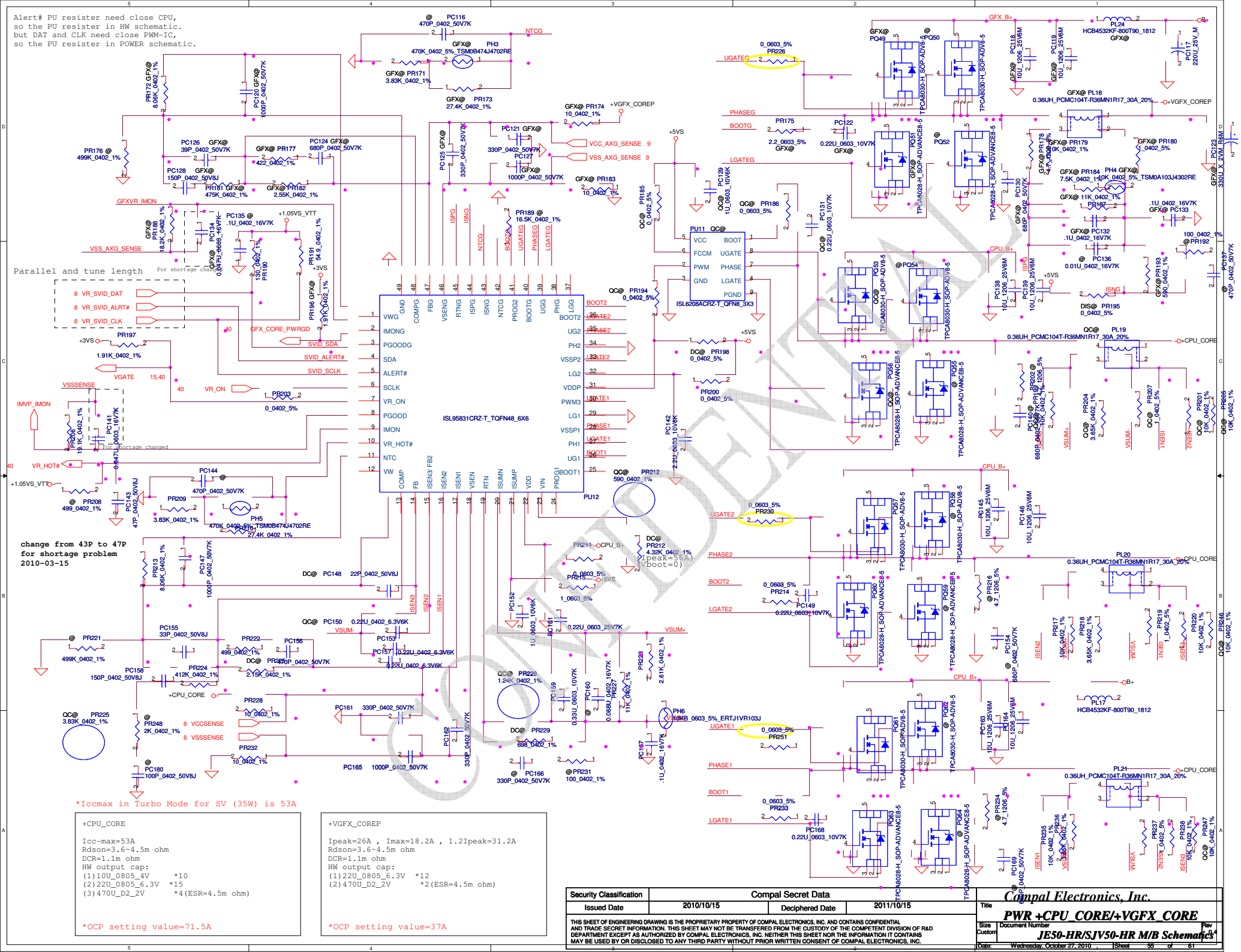
Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.
Parallel and tune length
change from 43P to 47P
for shortage problem
2010-03-15
ISL95831CRZ-T_TQFN48_6X6
ISL6208ACRZ-T_QFN8_3X3
*Iccmax in Turbo Mode for SV (35W) is 53A
+CPU_CORE
Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)10U_0805_4V *10
(2)22U_0805_6.3V *15
(3)470U_D2_2V *4(ESR=4.5m ohm)
*OCP setting value=71.5A
+VGFX_COREP
Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)22U_0805_6.3V *12
(2)470U_D2_2V *2(ESR=4.5m ohm)
*OCP setting value=37A
Security Classification
Compal Secret Data
Issued Date
2010/10/15
Deciphered Date
2011/10/15
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Compal Electronics, Inc.
Title
PWR +CPU_CORE/+VGFX_CORE
Size
Custom
Document Number
JE50-HR/SJV50-HR M/B Schematics
Rev
0.4
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Version change list (P.I.R. List) for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Shut down for PWM3 pin floating	IF the PWM3 no used, please pull high it for +5VS and not floating	0.1	P.55	(1)Add PR638(0_0603_5%) between PWM3 and +5VS (2)connect the ISNG to +5VS	2010-03-29	DVT
2	OVP problem with PWR and HW side	If the HW side is 0V, through the jumper will cause the sense pin to over the votage setting and it may happen OVP problem.	0.1	P.55	Change the +VGFX_CORE to +VGFX_COREP	2010-03-29	DVT
3							

COMPAL ELECTRONICS		
Title <Title>	PIR POWER1	
Size A	Document Number PAW00(LA-6361P)	Rev 0.1
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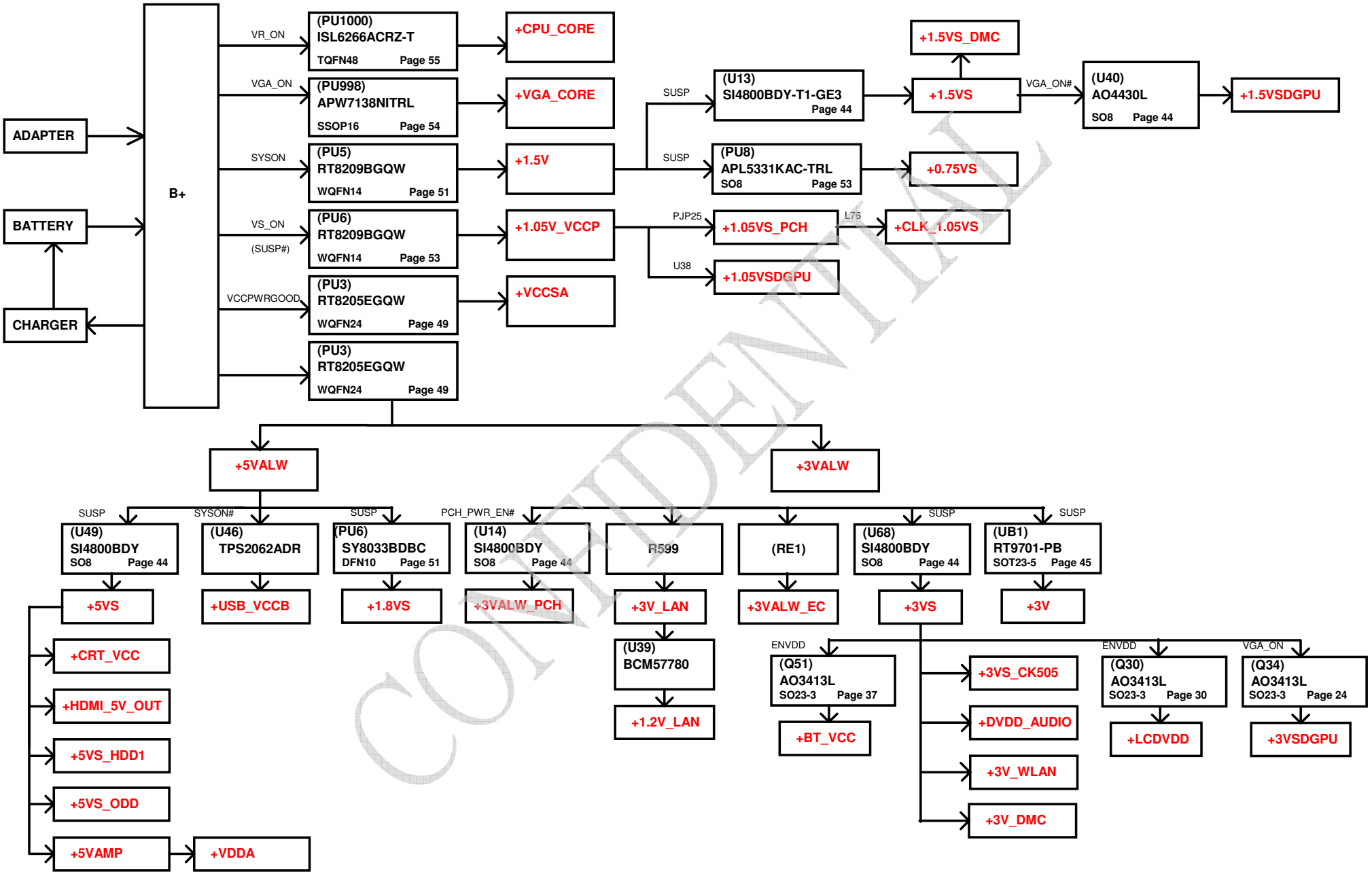

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Issued Date	2010/10/15	Deciphered Date	2011/10/15

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Title: Power Rail

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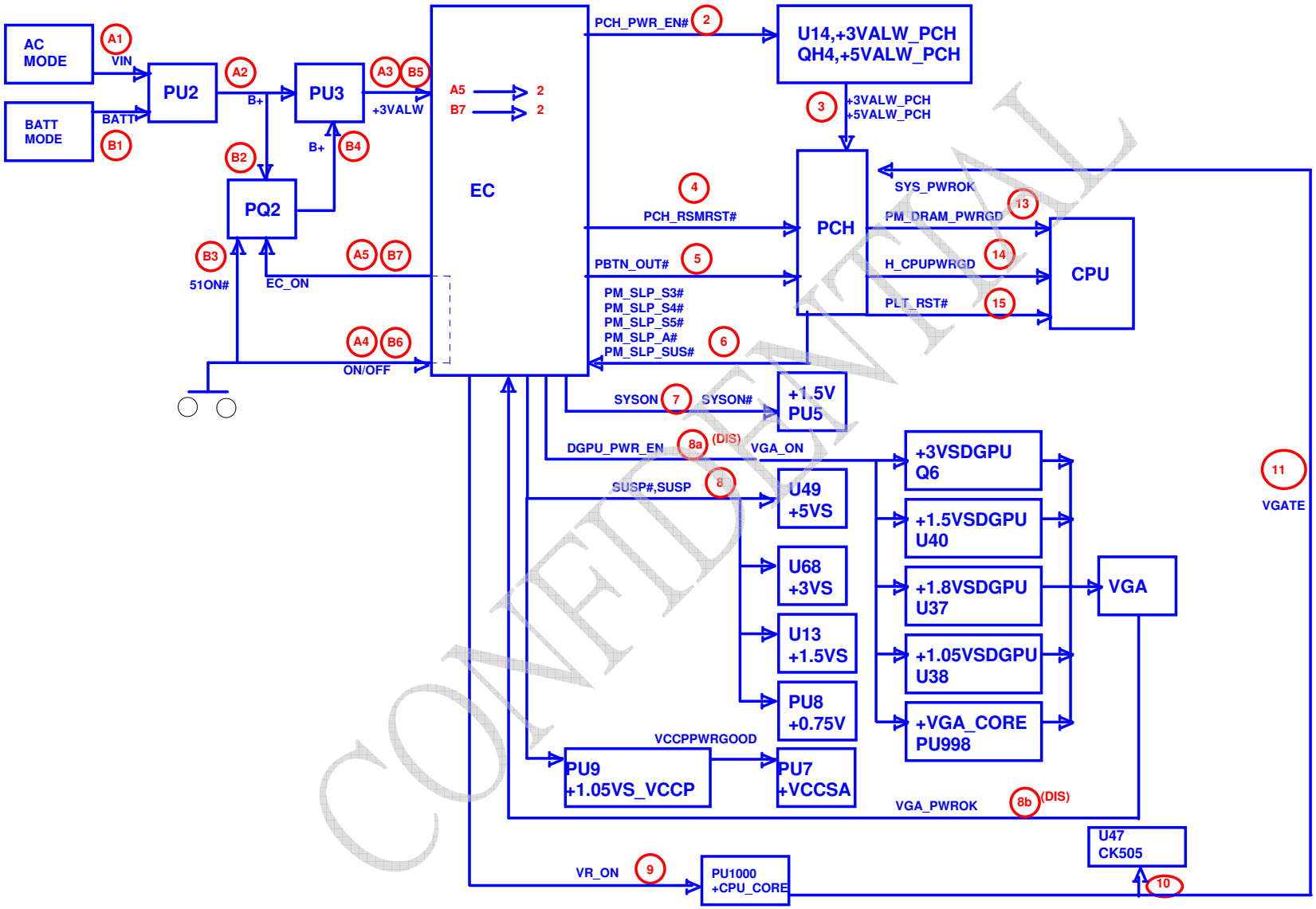

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

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Title: Power sequence

Size	Document Number	Rev
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Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P.18	PCH_GPIO71	09/01	SW	For identofy VRAM 900 or 800 MHz		0.2
2	P.31	DPST buffer	09/03	HW	Change U1 from NOT gate to Buffer		0.2
3	P.39	EC_MUTE# pull high	09/03	HW	Change EC_MUTE# Pull high from +3VALW to +3VS		0.2
4	P.40	TP Conn. Reverse	09/03	HW	TP Mudule change,so reverse TP pin		0.2
5	P.13	R624 pop @	09/03	HW	Already pull high R655~		0.2
6	P.45	Change Cap from 0.1u to 0.01u	09/03	HW	C696,C368,C717,C718,C695,C366,C697, C401,C370,C369,C715 change to 0.01U Follow Vendor Suggest ..		0.2
7	P.35	Change 0 Ohm to 47 Ohm	09/04	Broadcom	R199,R207,R211,R215,R168,R171,R179, R182,R195,R216,R192 change to 47 Ohm Follow Vendor Suggest ..		0.2
8	P.5		09/17	HW	CPU XDP socket take off		0.2
9	P.40		09/17	HW	TP pin reverse		0.2
10	P.13		09/17	HW	R624 change to 4.7K		0.2
11	P.45		09/17	HW	OCI2B(R313) place @ for BOM		0.2
12	P.33		09/17	HW	HDMI output from PCH (by UMA)		0.2
13	P.35		09/17	HW	switch the LAN MIDI0 and MIDI2 pin		0.2
14	P.17,35 ,37,38, 39,45		09/17	HW	Change IO port PLT_RST# to PLT_RST_BUF#		0.2
15	P.18		09/17	HW	OPTIMUS_EN# pull high, pull low resistor value both change to 10K		0.2
16	P.24		09/20	HW	modify the VRAM strap pin ROM_SI pull low resistor for implement VRAM 900MHz		0.3
17	P.33		09/23	HW	Add R784 and R785 for DDC pull high...		0.3
18	P.44		09/23	HW	Add C818 and C819 for coupling noise from other spare trace...		0.3
19	P.45		09/23	HW	Add R786,R787,R788 and R789 pull down from vendor's suggestion..		0.3
20	P.37		09/23	HW	Add C820,R790 and Q58 for 3G/B and change source voltage from +3VS to +3VALW..		0.3
21	P.45		09/23	HW	Add C821,C822,C823,C824 for +1.5V... and move the PJ26 & PJ27 between 1.5V to 1.5VSDGPUH		0.3
22	P.46		09/24	HW	Change JUSB5 to USB2.0 Conn. Add D34 as ESD Diode for USB3.0		0.3

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Title: EE P.I.R (1)

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Version Change List (P. I. R. List) Page 2

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
23	P.41		09/24	HW	Add R791 pull down 22k Ohm to ground Vendor's request...		0.3
24	P.22		09/24	HW	Add D31 to connect to ACIN Vendor's request...		0.3
25	P.36		09/29	HW	Add JP1,JP2 and JP3 for 家電下鄉 ESD protection		0.3
26	P.36		09/29	ME	Update the JREAD1 symbol		0.3
27	P.13		09/29	HW	Add R792 follow DG1.5		0.3
28	P.33		09/29	HW	Change HDMI termination R to 680 Ohm		0.3
29	P.44		09/29	HW	Add C825 fro +1.05VSDGPU		0.3
30	P.17,38 ,45		09/30	HW	Change the M/B to USB port to port 1 Sub/B to port 0 and port 2		0.3
31	P.5		10/04	HW	Add test point for TCK,TMS, TRST#,TDO,TDI		0.3
32	P.17,18		10/04	HW	WWAN_OFF# from GPIO51 to GPIO37 WL_OFF# from GPIO55 to GPIO49		0.3
33	P.17,45		10/04	HW	M/B USB port from port 2 change to port1		0.3
34	P.26		10/04	HW	C1 and C604 chaneg to 470uF		0.3
35	P.36		10/04	HW	Add C827 as DGND and RJ45_GND bridge		0.3
36	P.36		10/04	HW	Change R490,R491,R492 and R493 to 0603 package		0.3
37	P.35		10/04	HW	Chaneg R214 to 0603 package		0.3
38	P.35		10/04	HW	Chaneg R192,R195,R199,R207,R211 ,R215,R168,R171,R179,R182 to 0 Ohm		0.3
39	P.40		10/04	HW	follow broadcom suggestion,add R496		0.3
40	P.40		10/04	HW	Add keyboard cap for EMI		0.3
41	P.44		10/04	HW	Add C826 for +1.5VSDGPU		0.3
42	P.37		10/05	HW	Add RTS5138 circuit		0.4
43	P.13		10/12	HW	Add D35 ,R799 and C838 for changing the RTC to samll size... and can be charged!!		0.4
44	P.14		10/12	HW	Add CLK_SD_48M for Card Reader 5138		0.4
45	P.24		10/12	HW	Pop R129 follow NV suggestion		0.4
46	P.25		10/12	HW	Pop R82 and De-pop R92 follow NV suggestion		0.4
47	P.25		10/12	HW	Add R800 and R801 10K Ohm pull down follow NV suggestion		0.4
48	P.24		10/12	HW	Change R775,R777,R778 and R779 to GV@		0.4

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Title: EE P.I.R (2)

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Security Classification	Compal Secret Data		
Issued Date	2010/10/15	Deciphered Date	2011/10/15

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Title: EE P.I.R (3)

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