Compal Confidential

Q5WV8 Schematics Document

AMD "Comal" Platform

AMD Trinity APU / Hudson M3 FCH / ATI Thames XT

2012-01-05A

LA-8331P REV: 0.4

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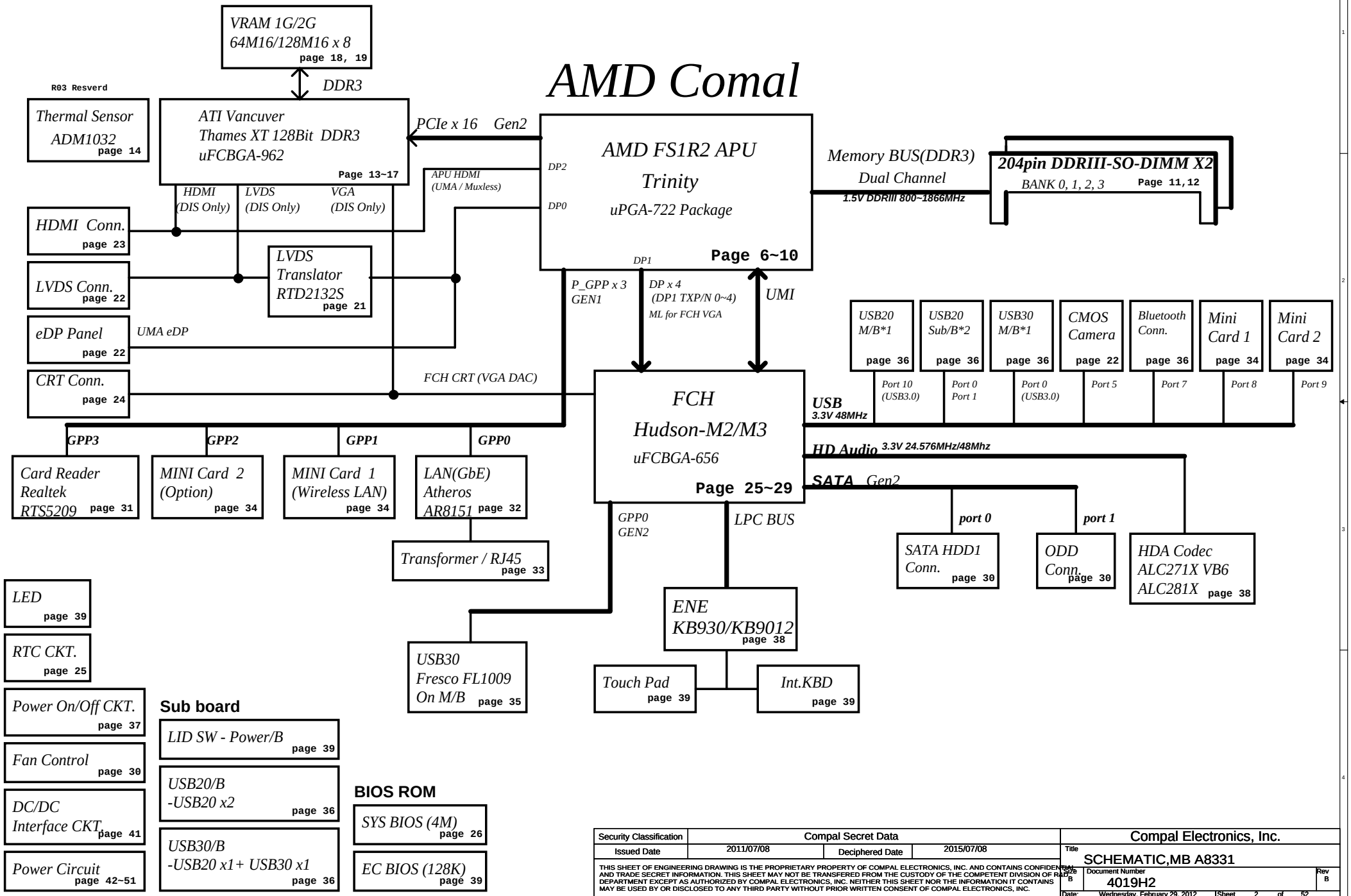
Model Name : Q5WV8



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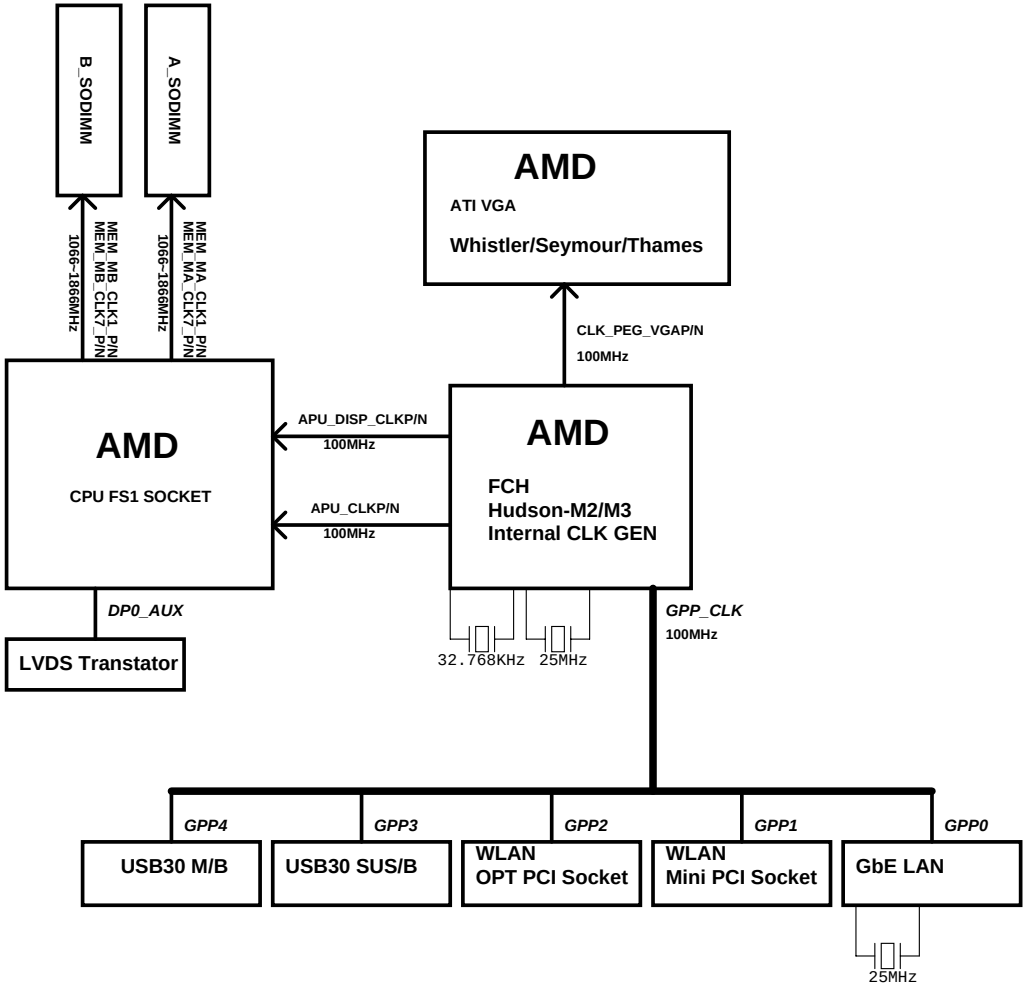
CLOCK DISTRIBUTION



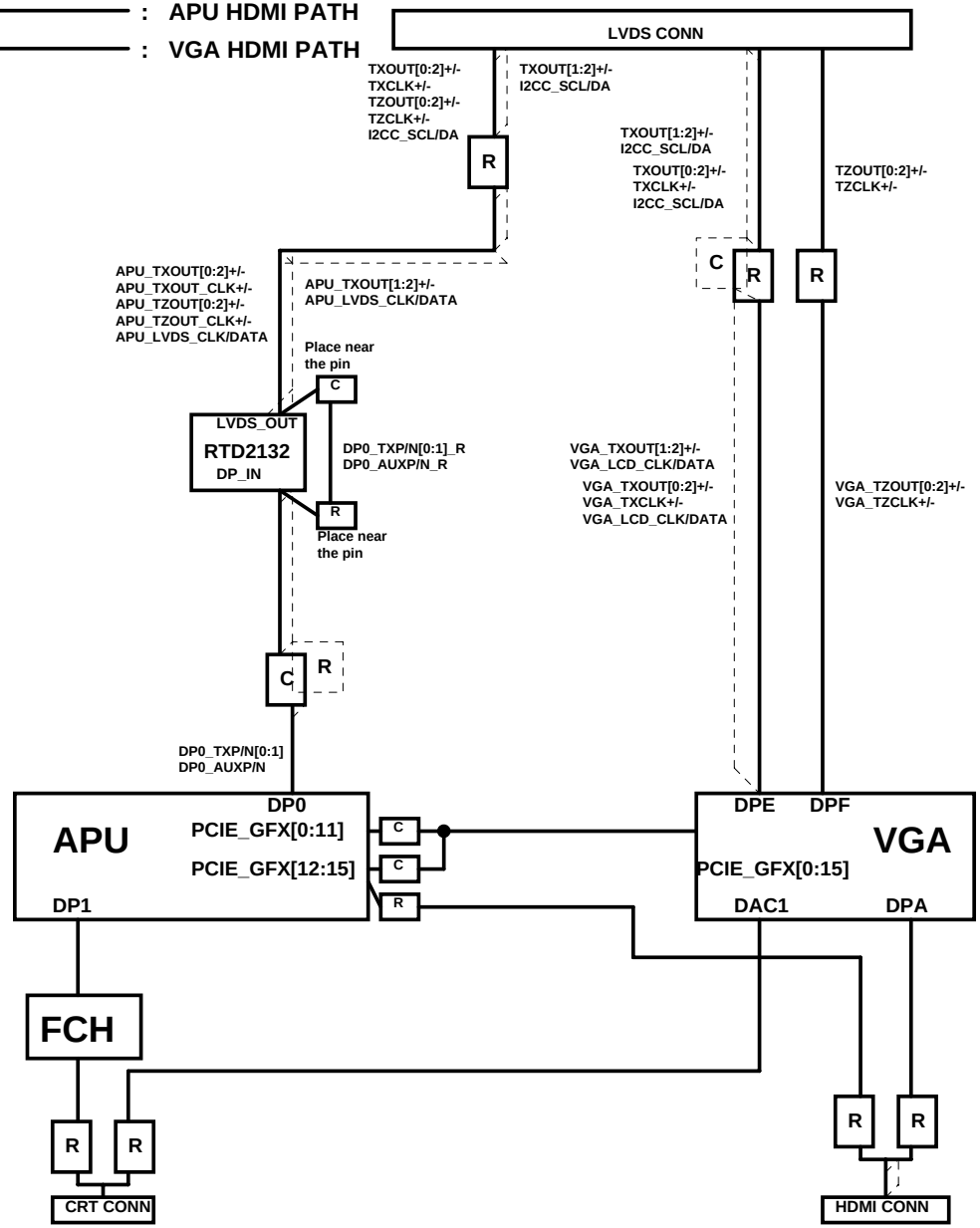
DISPLAY DISTRIBUTION

: LVDS PATH

, : eDP PATH

: APU HDMI PATH

: VGA HDMI PATH



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

ZZZ
PCB
Part Number = DA60000QV00
PCB 0OH LA-8331P REV0 M/B

ZZZ2
X76
Part Number = X76356BOL02
TMSSAM2G@

ZZZ3
X76
Part Number = X76356BOL03
SEYHYN1G@

ZZZ1
X76
Part Number = X76356BOL01
TMSHYN2G@

ZZZ4
X76
Part Number = X76356BOL04
SEYSAM1G@

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	EVT
1	EVT2
2	DVT
3	
4	
5	
6	
7	

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (VGA)	1001 101X b	9AH
SB-TSI (APU)	1001 100X b	98H
LVDS TR(RTD-2132S)	1010 100X b	A8H
VGA Internal Thermal	1000 001X b	82H

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	90
DDR DIMM2	1101 001X b	94

FCH SM Bus 1 address

Device	Address	HEX

BOM Option Table

BOM Config

BOM Structure	Description	UMA	Thames	EVT2 UMA	DVT UMA-LVDS	DVT UMA-eDP	DVT PX5 1G-LVDS	DVT PX5 1G-eDP	DVT PX5 2G-LVDS		
M2@	Use Hudson-M2			V							
M3@	Use Hudson-M3	V	V		V	V	V	V	V		
930@	Use EC 930	V	V								
9012@	Use EC 9012			V	V	V	V	V	V		
UMA@	Display output from APU (UMA only or PX)	V	V	V	V	V	V	V	V		
DISO@	Display output from VGA (DIS only)										
VGALVDS@	VGA output LVDS (DIS only)										
VGA@	Use VGA (PX or DIS only)		V				V	V	V		
THA@	VGA: Thames		V				V	V	V		
SEY@	VGA: Seymour										
128@	Use VRAM channel A&B		V				V	V	V		
PX@	PX function		V				V	V	V		
BACO@	BACO function (PX4.0)		V								
NOBACO@	Without BACO function (DISO and PX5.0)						V	V	V		
TL@	LVDS Translator (for LVDS)	V	V	V	V		V		V		
EDP@	Use eDP Panel					V		V			
APUEDP@	APU output eDP					V		V			
VGAEDP@	VGA output eDP (DIS only)										
271@	Realtek ALC271x VB6	V	V	V	V	V	V	V	V		
281@	Realtek ALC281x										
ZERO@	ZERO Power ODD function										
FL@	Fresco FL1009 USB3.0 Controller			V							
8151@	LAN Atheros AR8151 10/100/1000M LAN			V	V	V	V	V	V		
8152@	LAN Atheros AR8152 10/100M LAN										
X76@	VRAM ID Table (Load By X76J)										
CONN@	Connector (Control by ME)										

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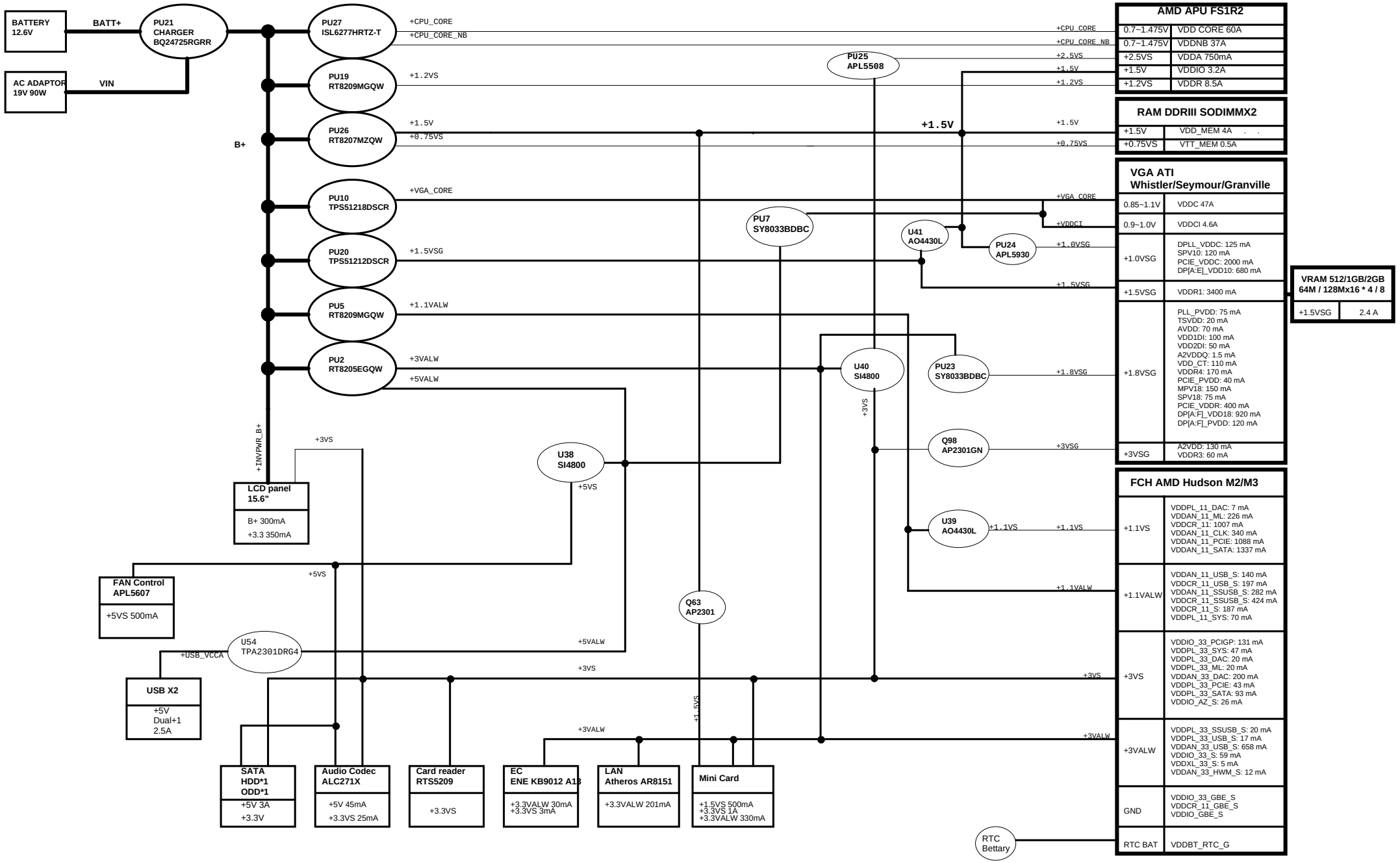

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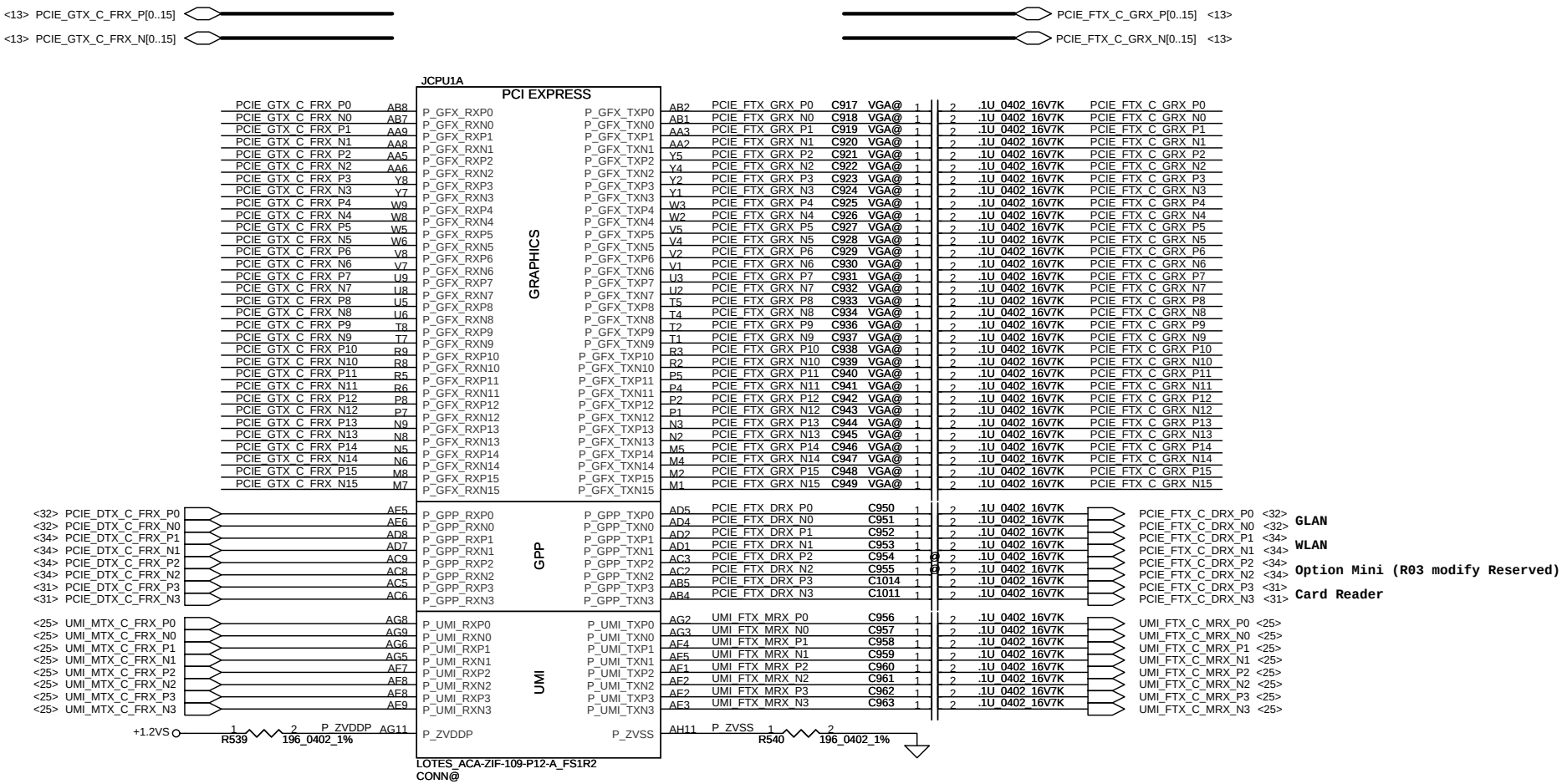

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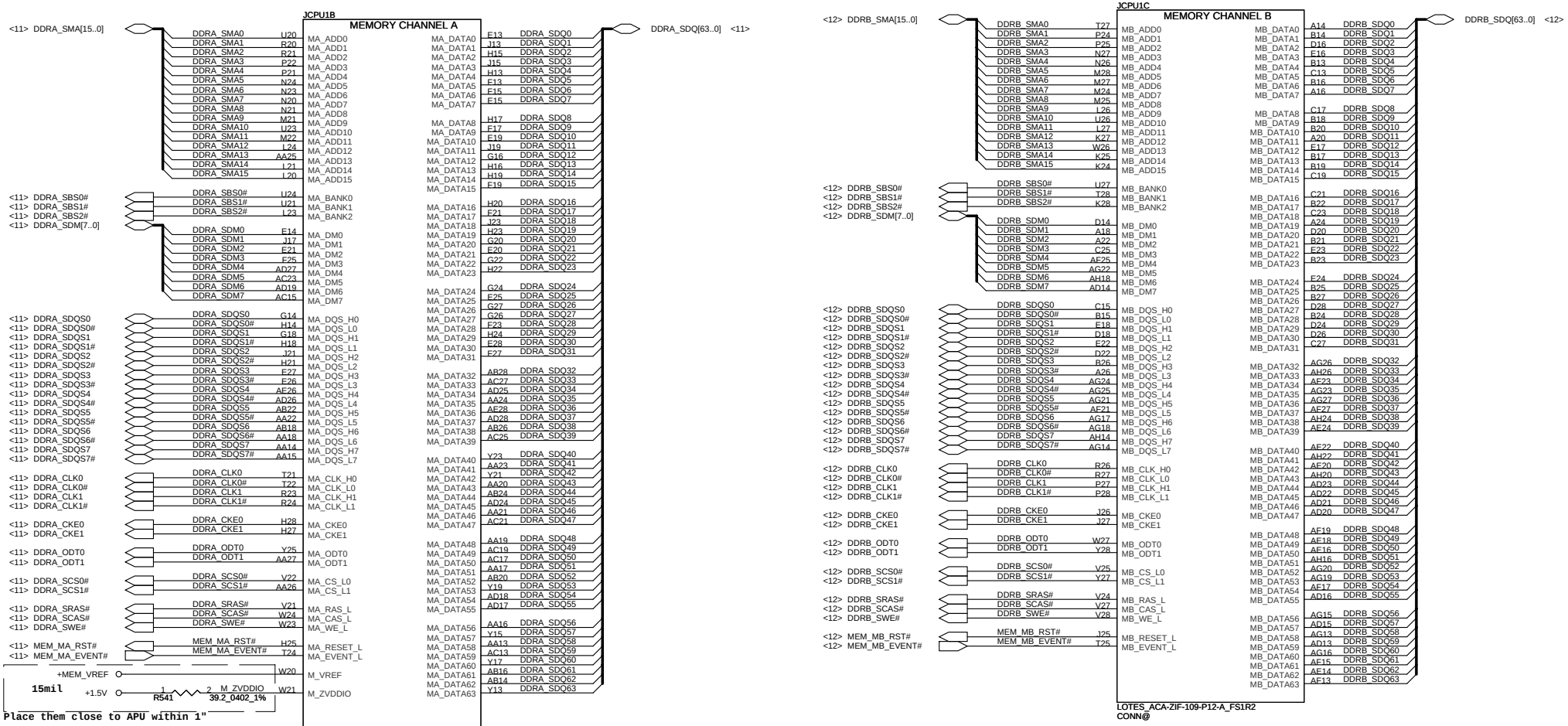

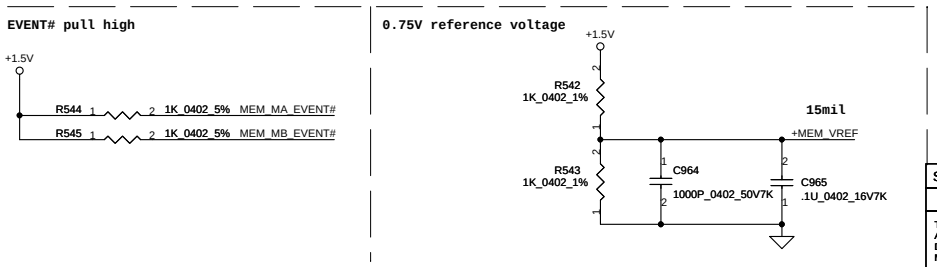

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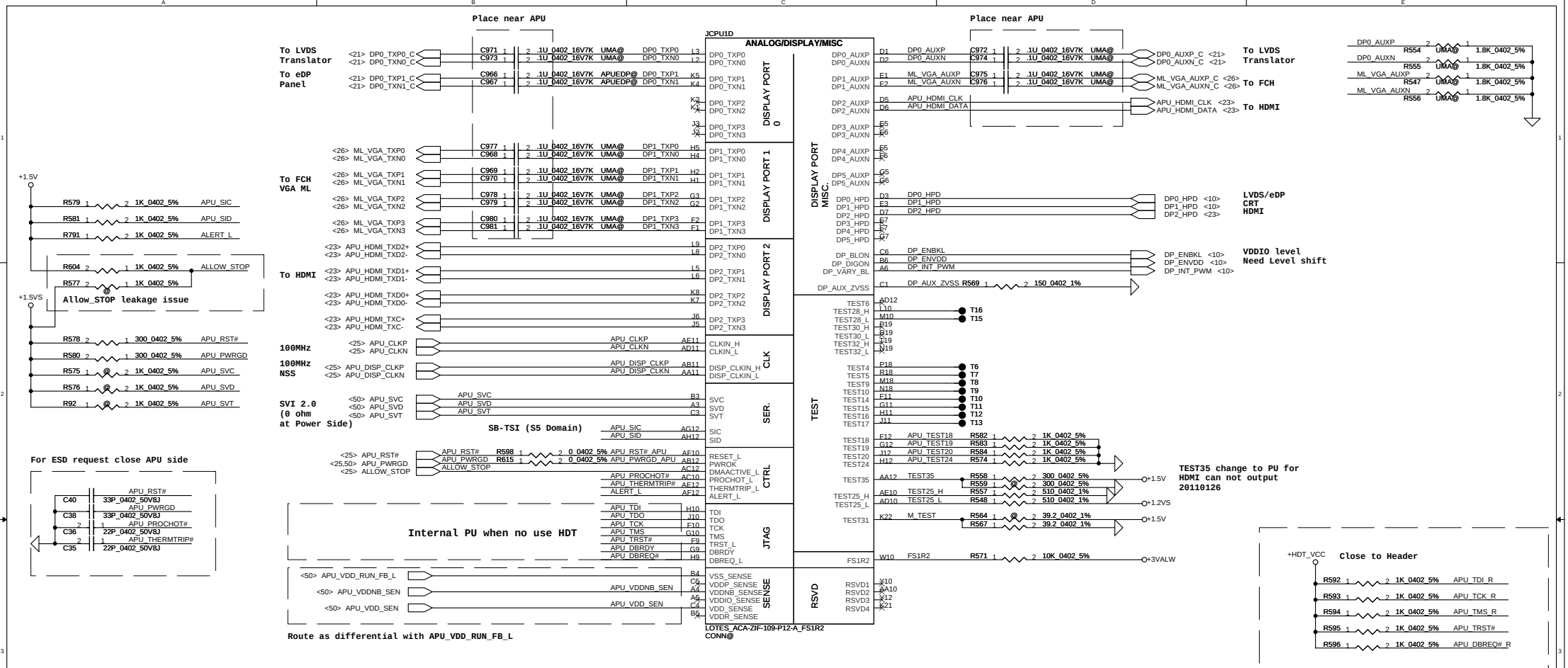


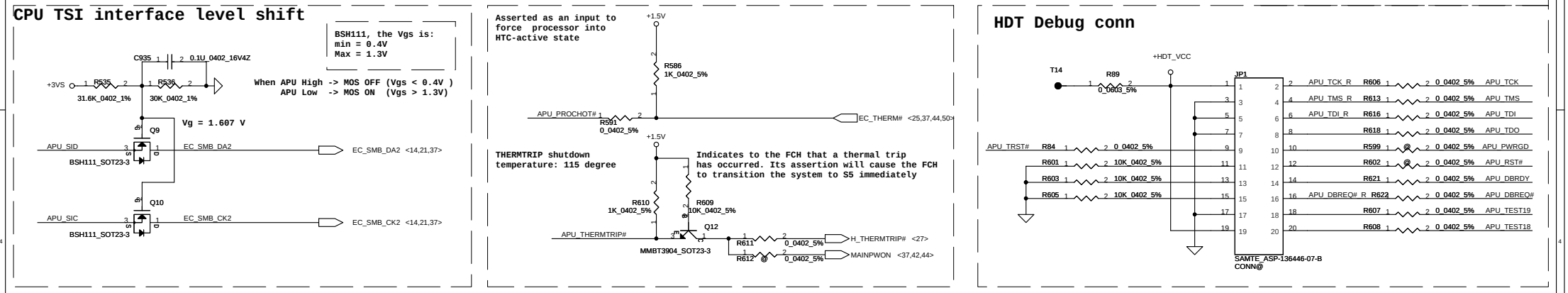
CPU TSI interface level shift

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

When APU High -> MOS OFF (Vgs < 0.4V)
APU Low -> MOS ON (Vgs > 1.3V)

Vg = 1.607 V

HDT Debug conn



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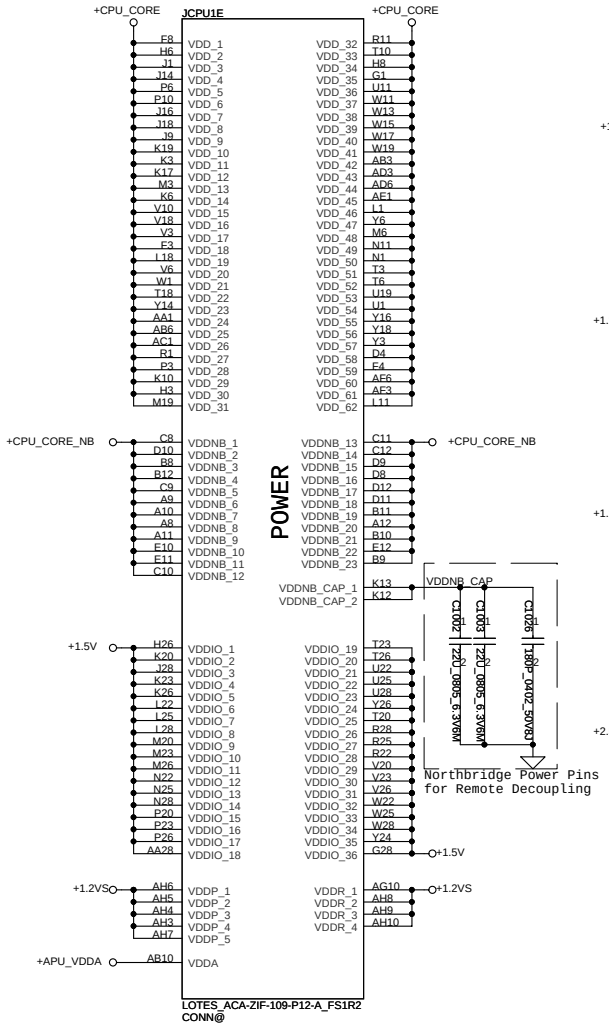
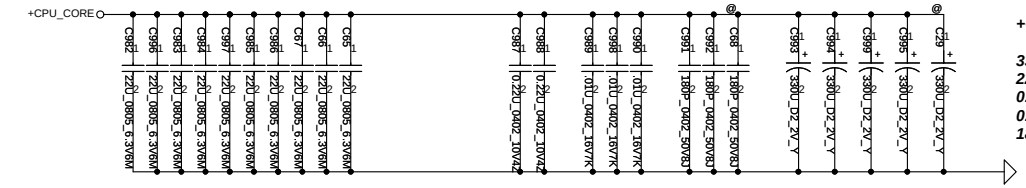
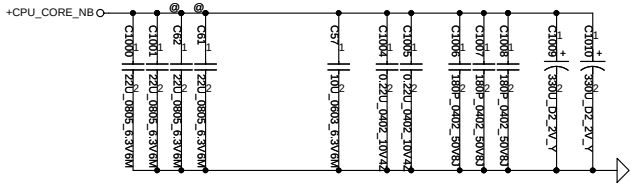
Power Name	Consumption
VDD +CPU_CORE	60A
VDDNB +CPU_CORE_NB	37A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.75A





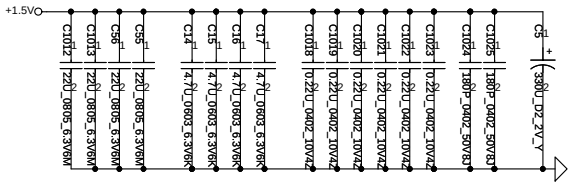
+CPU_CORE Decoupling

330uF x 3@ x2
22uF x 10 @ x5
0.22uF x2
0.01uF x3
180pF x2 @ x1



+CPU_CORE_NB Decoupling

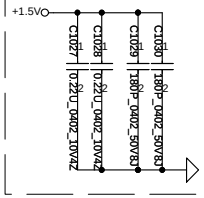
330uF x2
22uF x2 @ x5
10uF x1
0.22uF x2
180pF x3

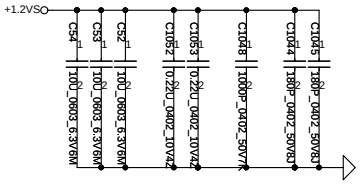


+1.5V / VDDIO Decoupling

330uF x1
22uF x4
4.7uF x4
0.22uF x6
180pF x1 @x1

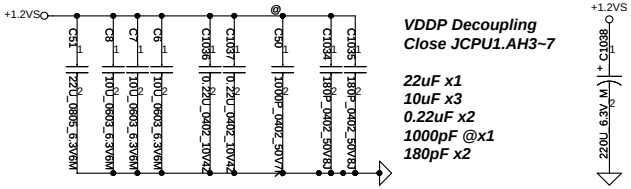
Decoupling between CPU and DIMMs
across VDDIO and VSS split





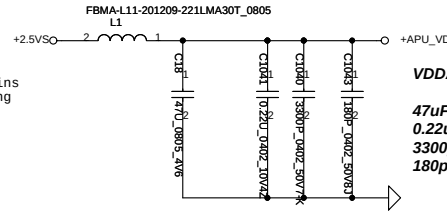
VDDR Decoupling
Close JCPU1.AG10,AH8,AH9,AH10

10uF x3
0.22uF x2
1000pF x1
180pF x2



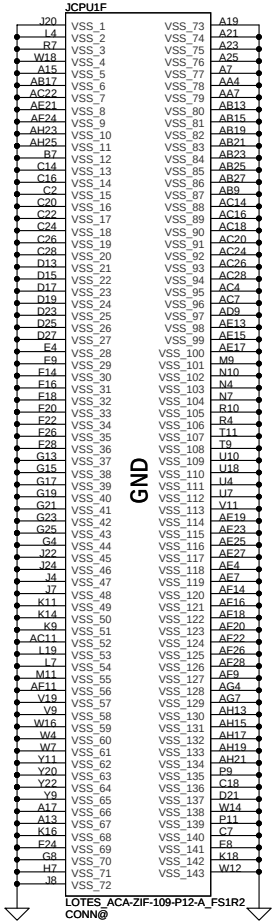
VDDP Decoupling
Close JCPU1.AH3~7

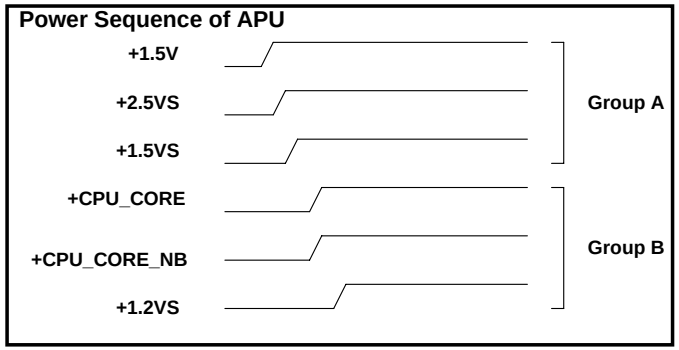
22uF x1
10uF x3
0.22uF x2
1000pF @x1
180pF x2



VDDA Decoupling

47uF x1
0.22uF x1
3300pF x1
180pF x1





Decoupling Caps.

Pop / @	330uF	220uF	47uF	22uF	10uF	4.7uF	0.22uF	0.01uF	3300pF	1nF	180pF
Pumori 2.0			0	19/11	7	5	17	3	1	1 / 1	13/3
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2
P5WS5	7 / 2	1	1	13	3	8	19	3	1	4	16

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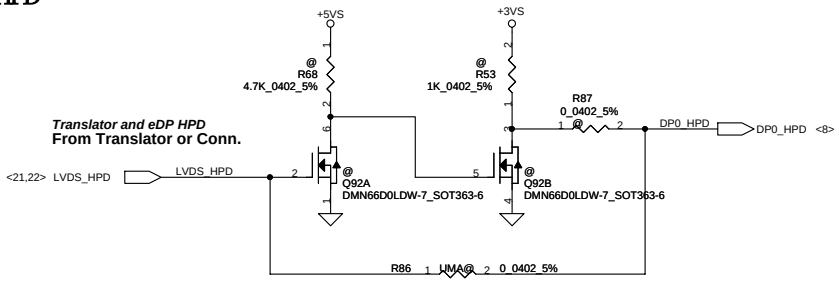
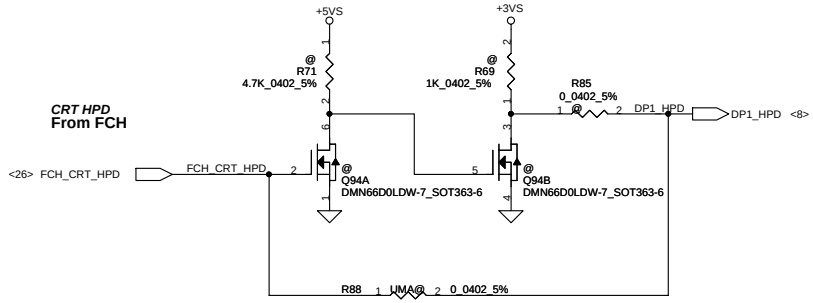
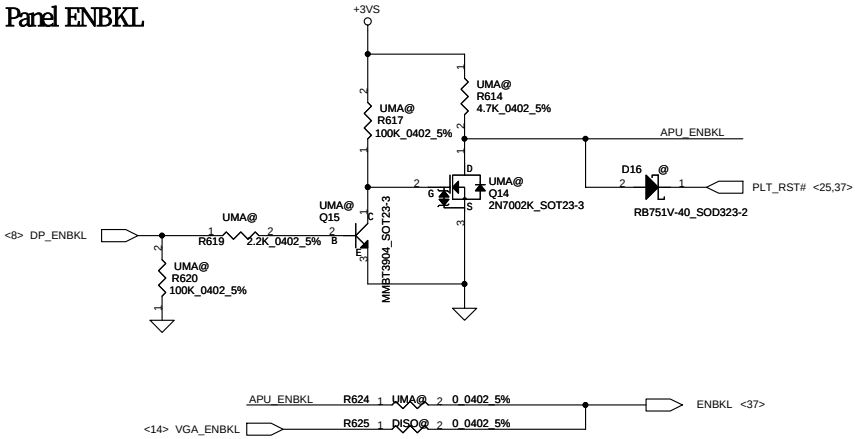
HPD

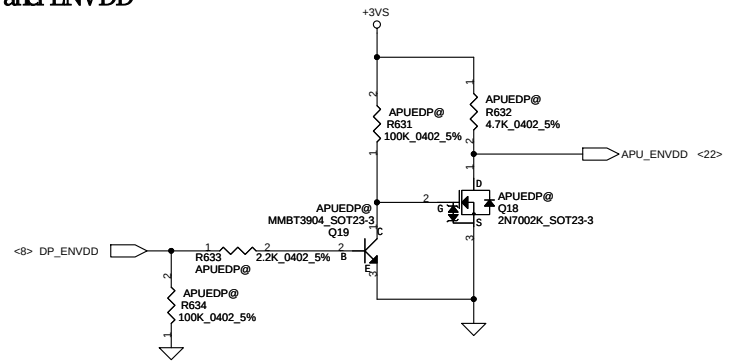




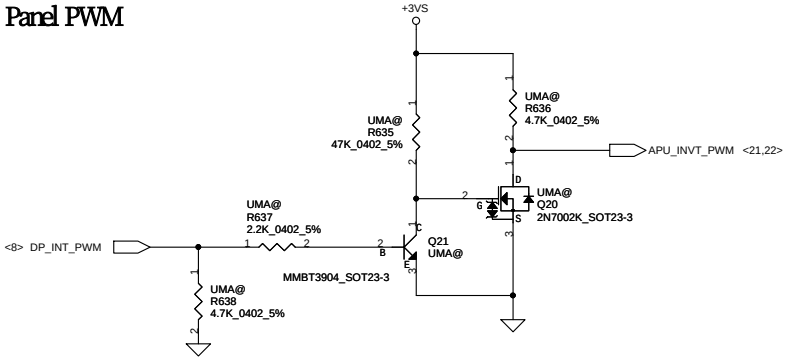
Panel ENBKL



Panel ENVDD



Panel PWM



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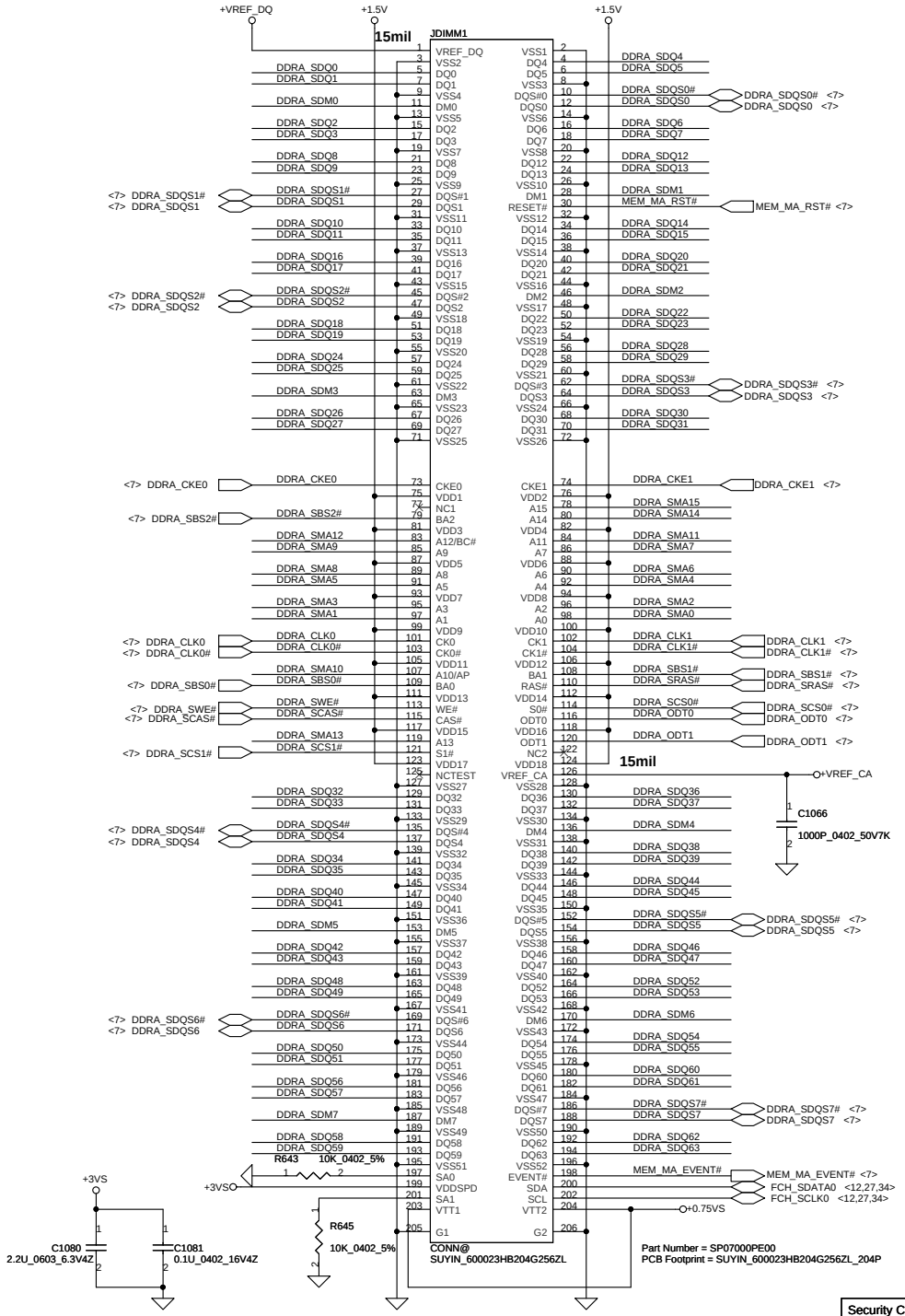
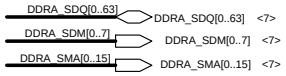
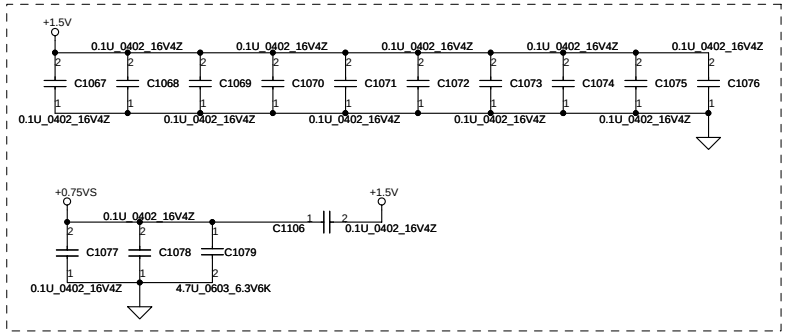
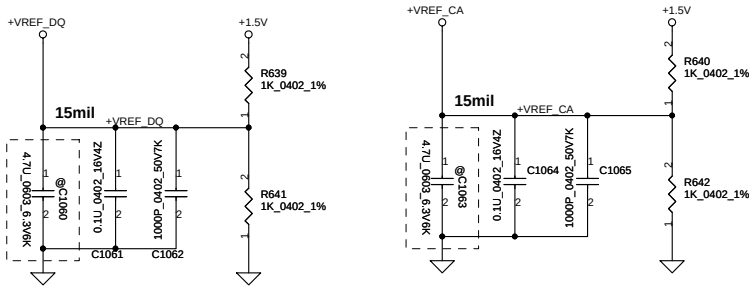
				Date: Wednesday, February 29, 2012; Sheet 10 of 52





Place near DIMM1





DIMM_A STD H:8mm

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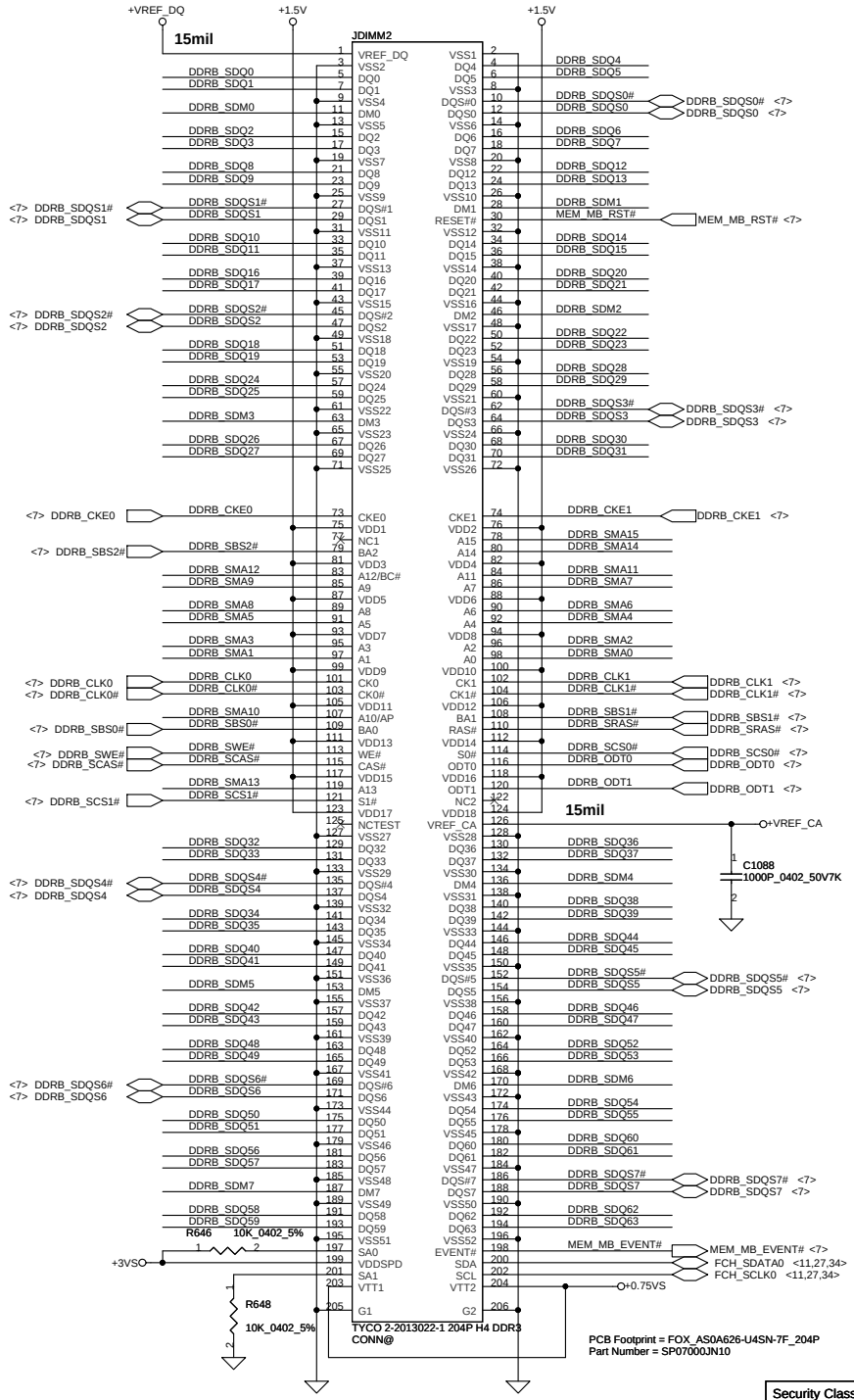
				Date: Wednesday, February 29, 2012 / Sheet 11 of 52



DIMM_B STD H:4mm

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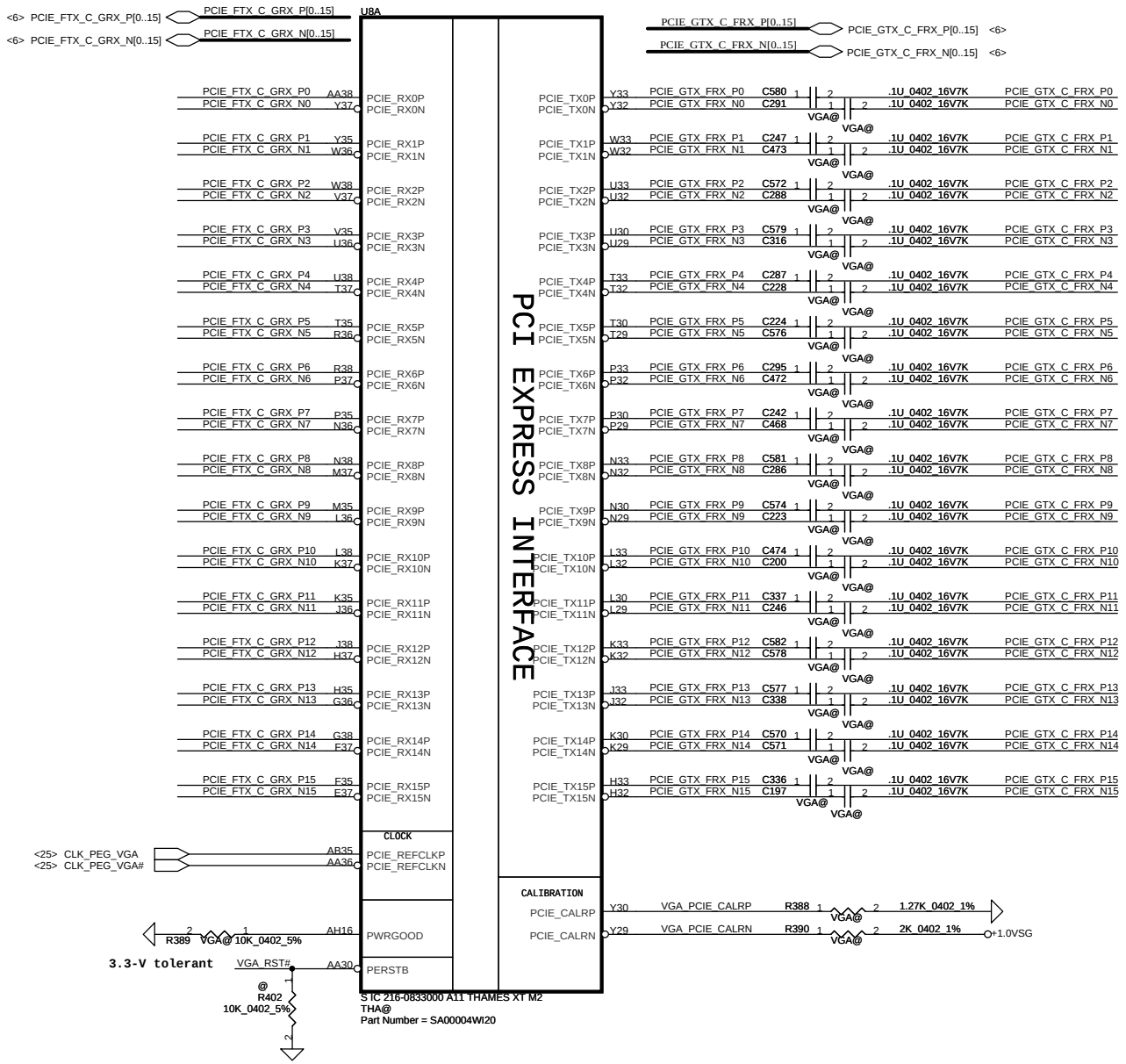
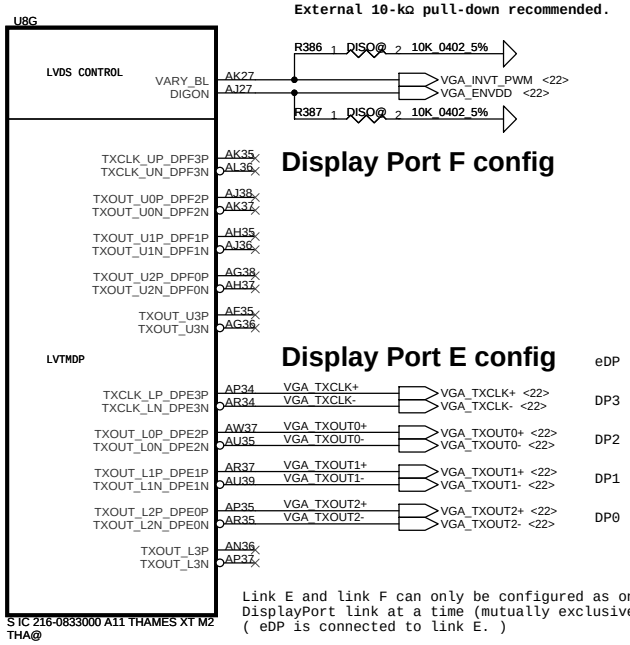
GFX PCIE LANE REVERSAL

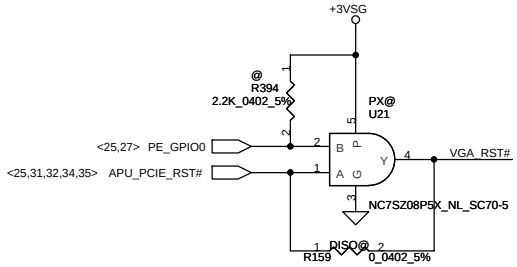


<DIGON>
Controls panel digital power on/off.
Active High
External 10-kΩ pull-down recommended.

<VARY_BL>
LCD PWM (pulse width modulated)
output to adjust LCD brightness
Active High
External 10-kΩ pull-down recommended.



Link E and link F can only be configured as one DisplayPort link at a time (mutually exclusive). (eDP is connected to link E.)



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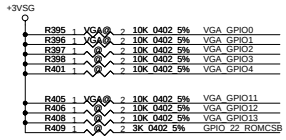
Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis diabled 1: Tx de-emphasis enabled	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. CONFIG[3:0] 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 256 MB 001 * 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (Internal PD) 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI



GPIO5 fast-power reduction:
HW control will casue display disturb
should use SW method control
GPIO6 voltage control signal ,No use can NC

Move to
DDCCLK_AUX3P,DDCDATA_AUX3N

Global Swap Lock on
Multiple GPUs

DISCRETE ONLY
PD 100K at EC side

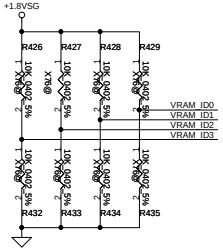
R02 modify, R03 modify BOM

VGA_SMB_DA2 R469 VGA@ 0_0402_5%
VGA_SMB_CK2 R527 VGA@ 0_0402_5%

<10> VGA_ENBKL
GPIO7 Controls backlight onoff.
Active High ,need external PD
if GPIO22 High ,GPIO 11-13->CFG[0:2]
Config ROM type ,GPU has internal PD
GPIO6,15,16,20
Voltage control signal
GPIO6,15 no use can NC
Thermal monitor interrupt
Critical temperature fault
Reserved
External BIOS device
ON(1)OFF(0) inter PD
Internal Debug
no use can floating
ON(1)OFF(0)
Stereo Sync
no use can NC
For ATI Cross fire
no use can NC

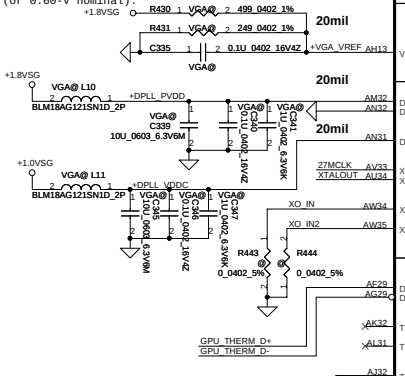
<49> GPU_VID0
<45> VDDCI_VID
<22> VGA_EDP_HPD
<49> GPU_VID1

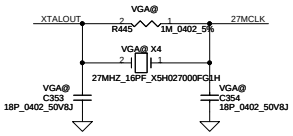
VRAM ID

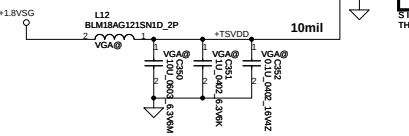


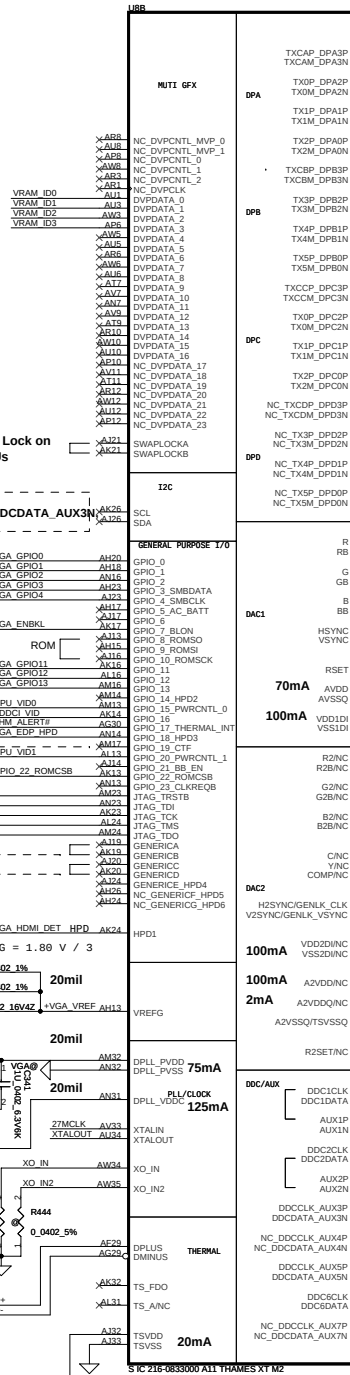
DVPDATA	ID3	ID2	ID1	ID0	Van SPD Name
00h	0	0	0	0	SAM 933 K4W1G1646G-BC11 64Mx16
01h	0	0	0	1	SAM 933 K4W2G1646C-HC11 128Mx16
02h	0	0	1	0	
03h	0	0	1	1	
04h	0	1	0	0	AMD 900 23EY2387MB11 64Mx16
05h	0	1	0	1	AMD 900 23EY4187MA11 128Mx16
06h	0	1	1	0	
07h	0	1	1	1	
08h	1	0	0	0	HYN 900 H5TQ1G63DFR-11C
09h	1	0	0	1	HYN 900 H5TQ2G63BFR-11C
0Ah	1	0	1	0	
0Bh	1	0	1	1	
0Ch	1	1	0	0	MIC 900 MT41J64M16JT-107G:G
0Dh	1	1	0	1	MIC 900 MT41J128M16HA-107G:D
0Eh	1	1	1	0	
0Fh	1	1	1	1	

VREFG:Use a voltage divider to set VREFG = 1.80 V / 3
(or 0.60-V nominal).

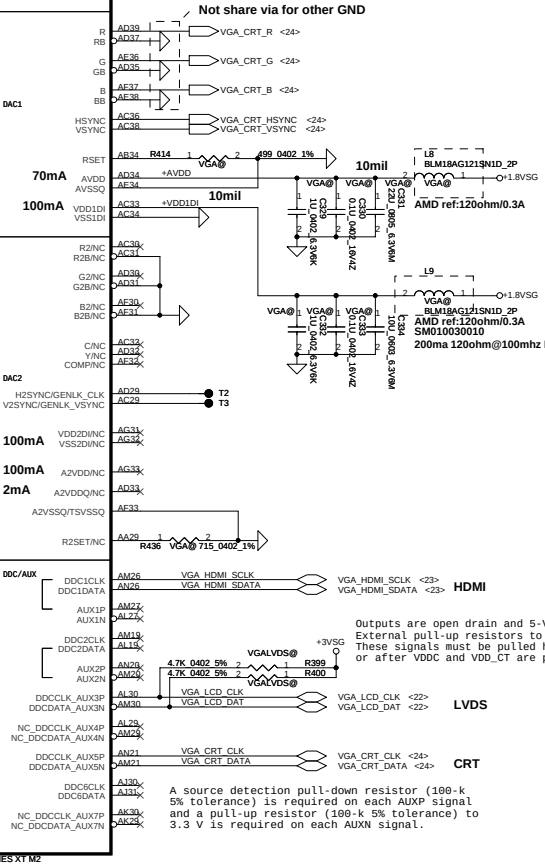








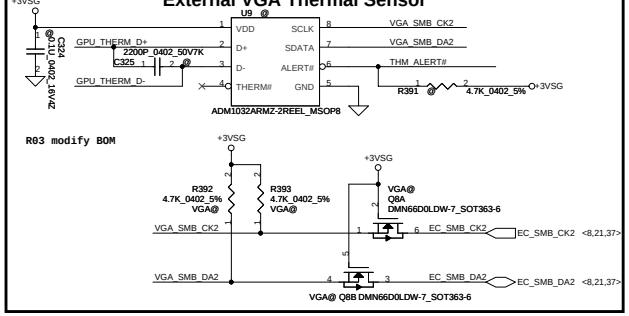
Not share via for other GND

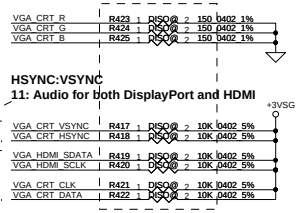


Outputs are open drain and 5-V tolerant.
External pull-up resistors to 3.3 V or 5 V are required.
These signals must be pulled high (to 3.3 V or 5 V) before
or after VDDC and VDD_CT are powered up.

A source detection pull-down resistor (100-k
5% tolerance) is required on each AUXP signal
and a pull-up resistor (100-k 5% tolerance) to
3.3 V is required on each AUXN signal.

External VGA Thermal Sensor





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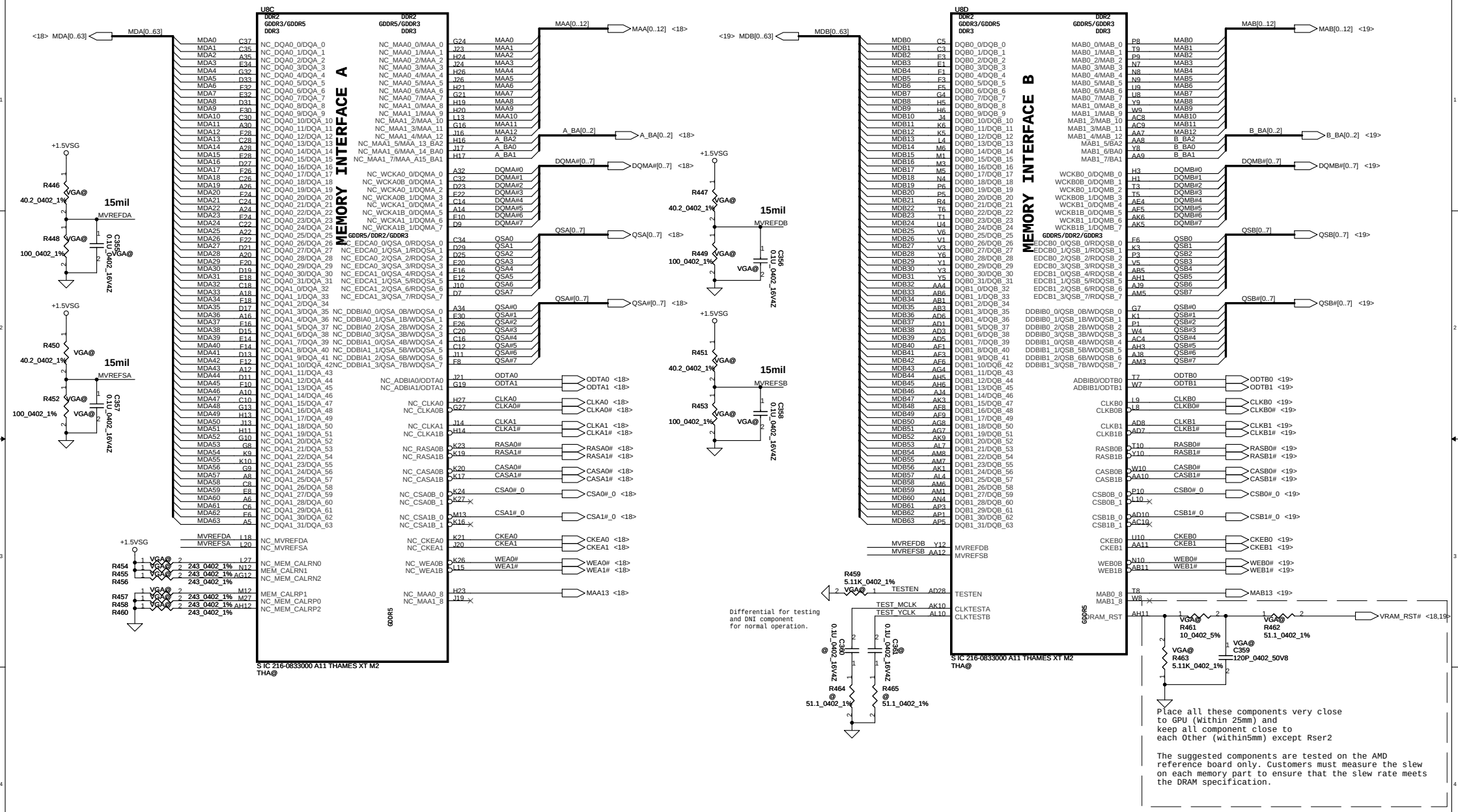

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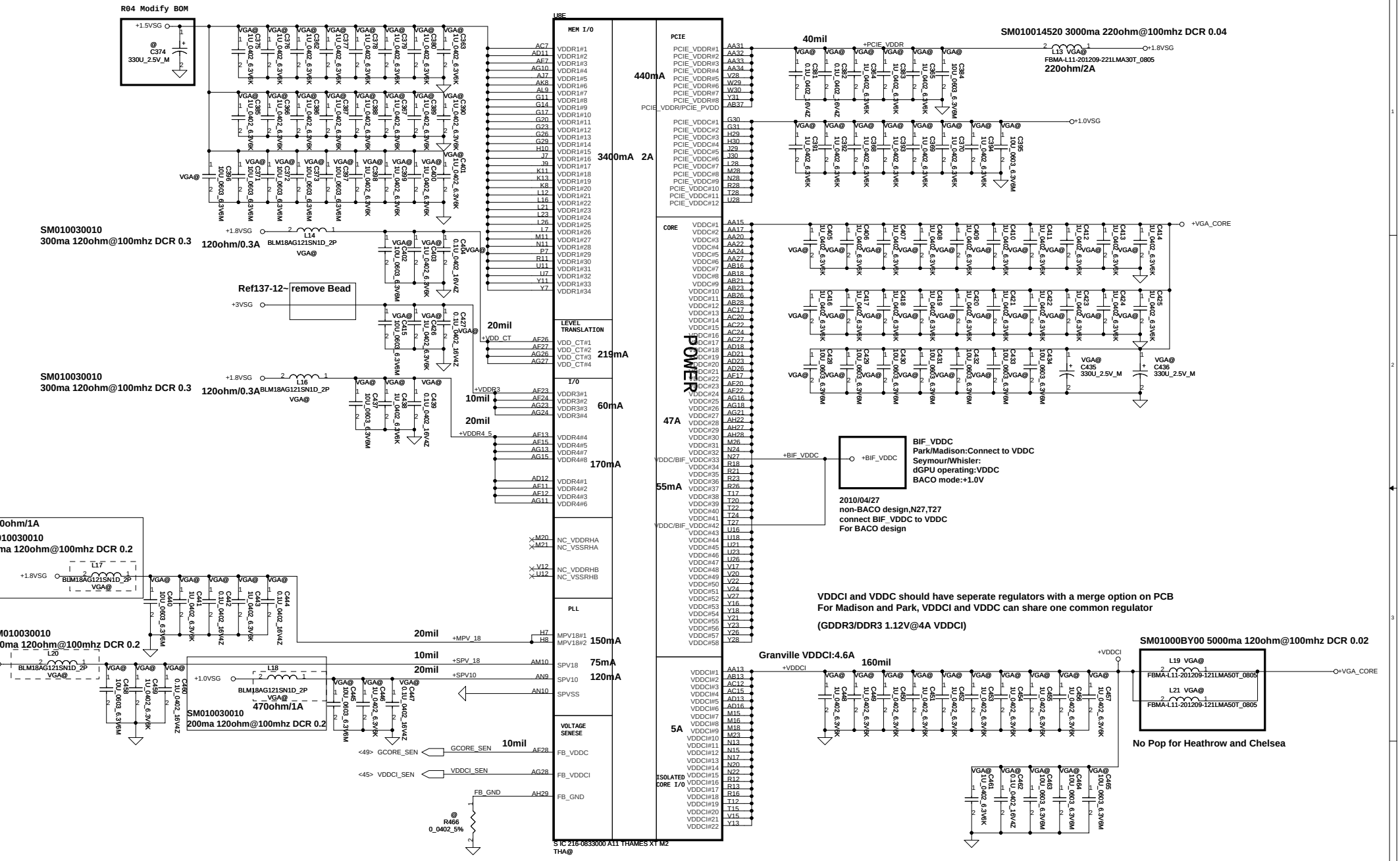

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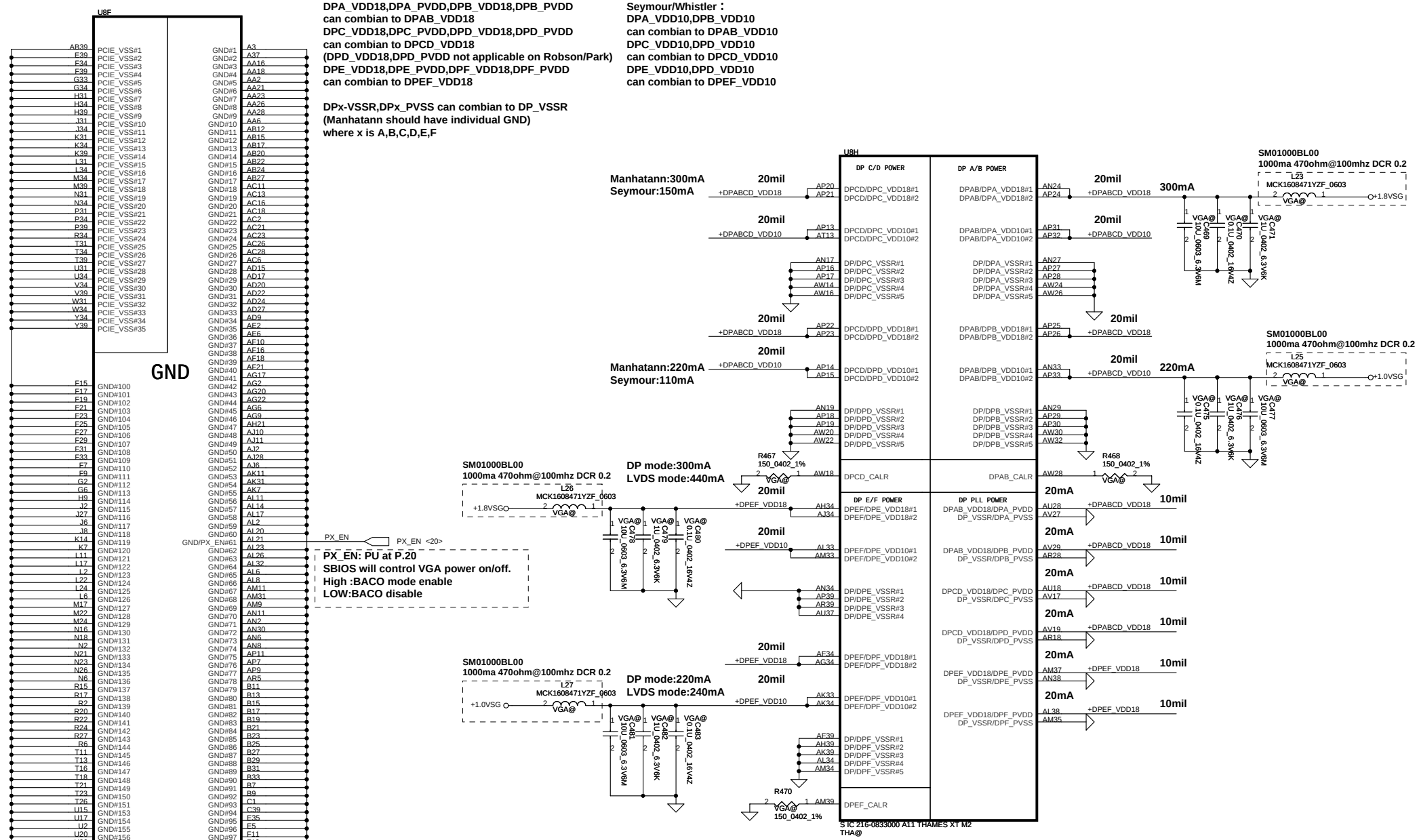

DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhatann should have individual GND)
where x is A,B,C,D,E,F

Seymour/Whistler：
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10

PX_EN: PU at P.20
SBIOS will control VGA power on/off.
High :BACO mode enable
LOW:BACO disable

Park/Madison :AL21left NC

Seymour/Whistler:
AL21:PX_EN
use to control discreate GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC

REF137-13 update

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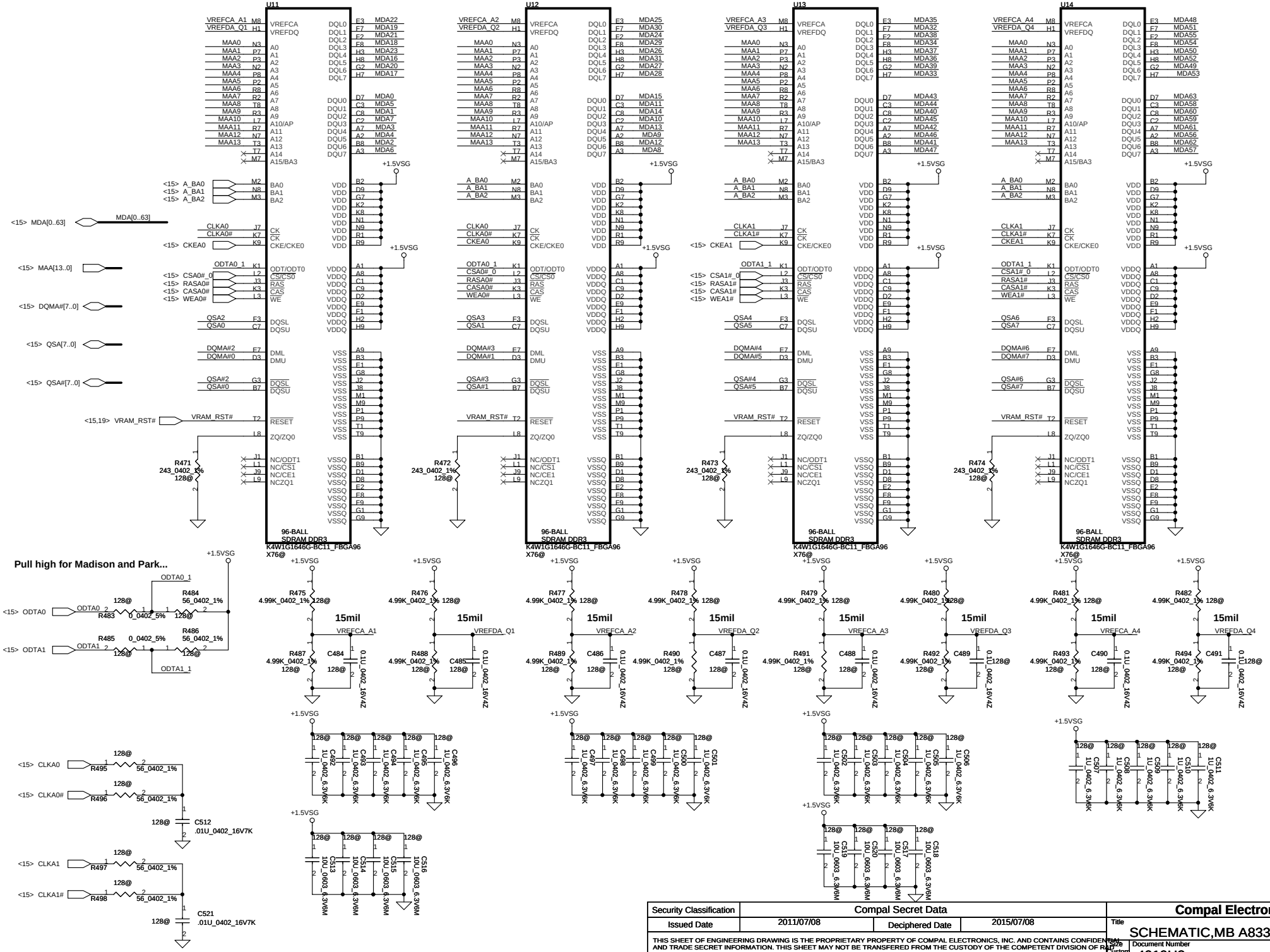

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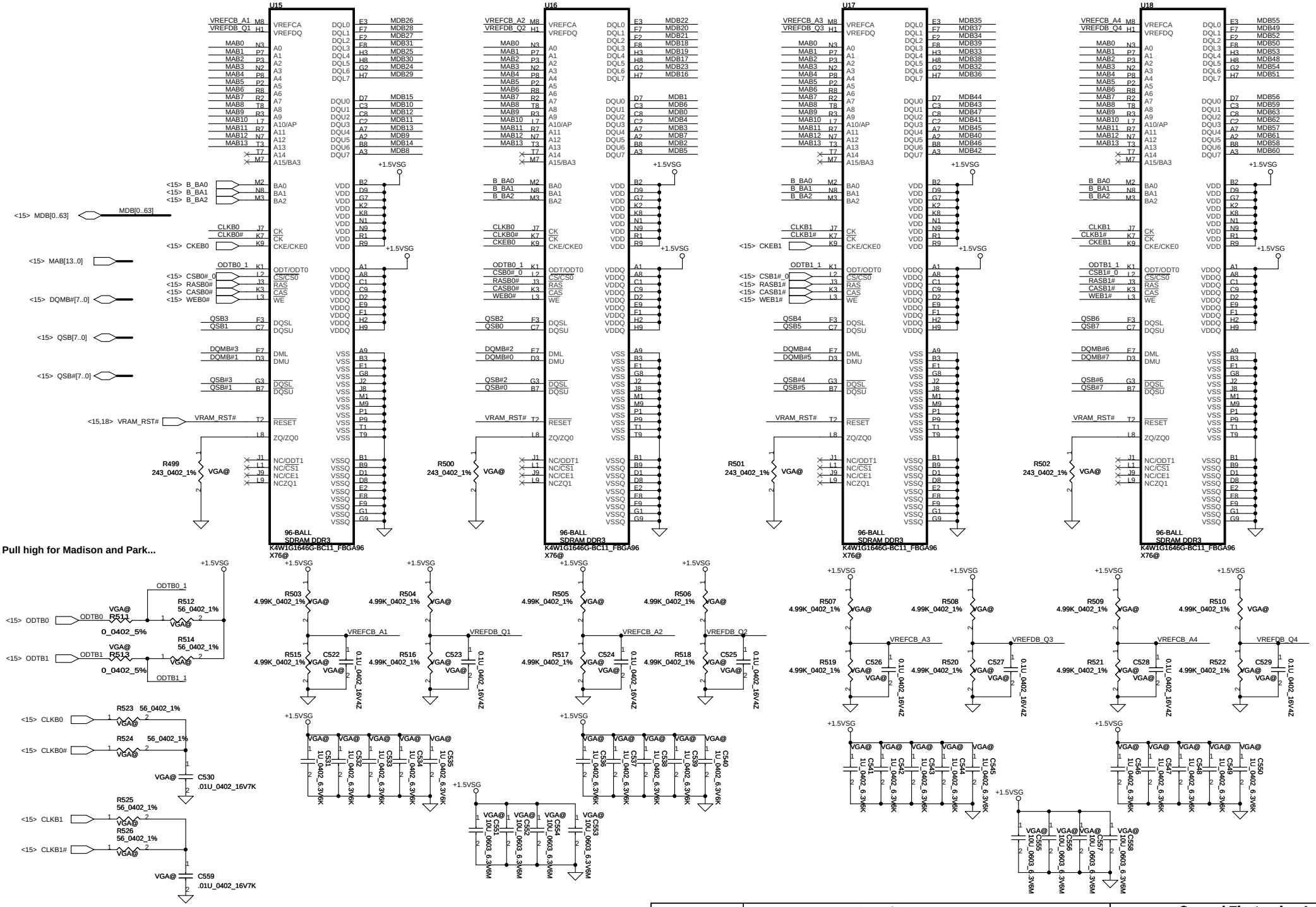

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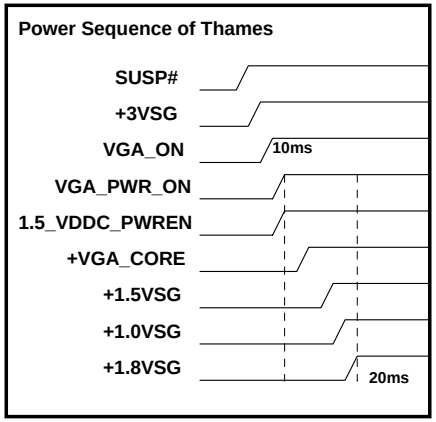
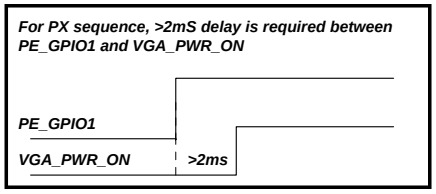
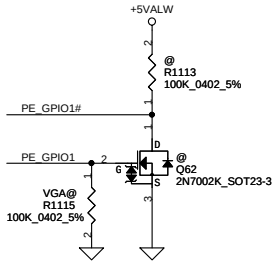


VGA Muxless and Dis only Status Mapping table			
	Dis only	Muxless High performance GPU	Muxless Power-saving GPU
VGA_PWR_ON	1	1	0
1.5_VDDC_PWREN	1	1	0
+3.3VSG	ON	ON	OFF
+1.8VSG	ON	ON	OFF
+1.0VSG	ON	ON	OFF
+VGA_CORE	ON	ON	OFF
+1.5VSG	ON	ON	OFF
+BIF_VDDC	+VGA_CORE	+VGA_CORE	OFF

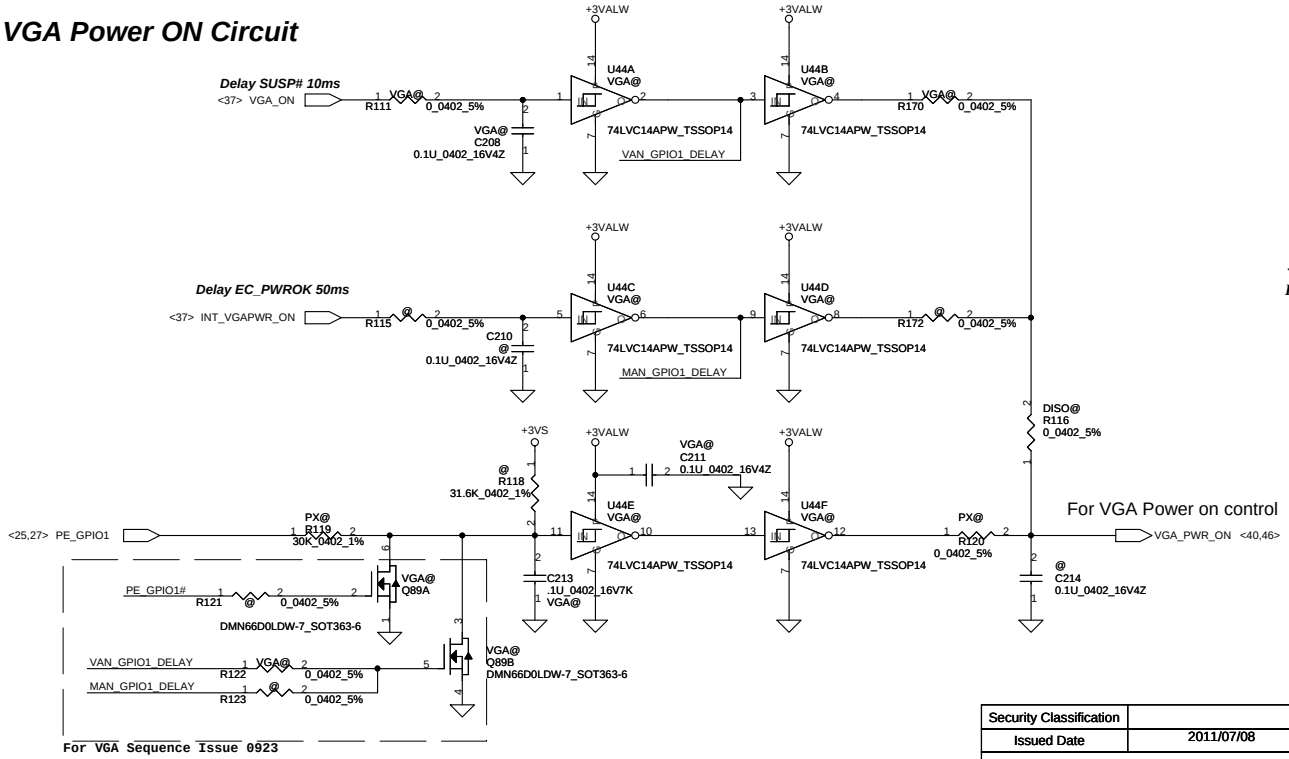
VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

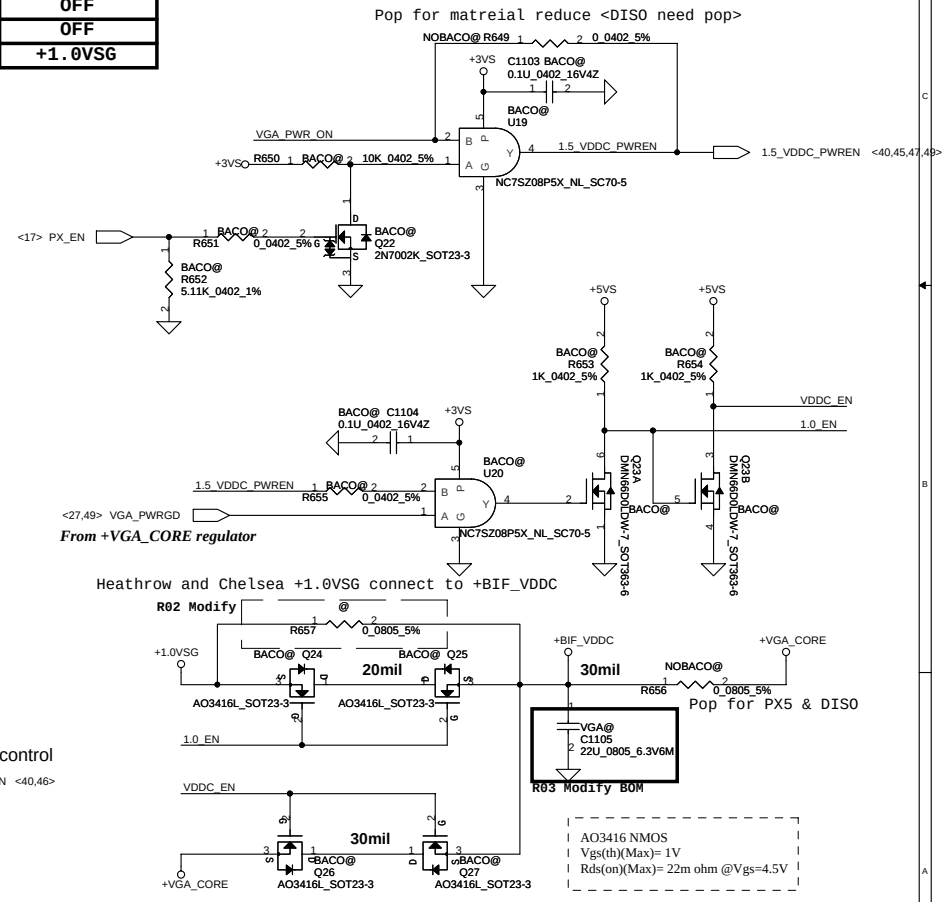
VGA Power Enable Signal Mapping table		
	Graville	Whistler and Seymour
VGA_PWR_ON source signal	INT_VGAPWR_ON	VGA_ON
+3.3VSG	VGA_PWR_ON	SUSP#
+1.8VSG	VGA_PWR_ON	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON	VGA_PWR_ON
+VDDCI	VGA_PWR_ON	Combine with +VGA_CORE
+VGA_CORE	VGA_PWR_ON	1.5_VDDC_PWREN
+1.5VSG	VGA_PWR_ON	1.5_VDDC_PWREN





VGA Power ON Circuit





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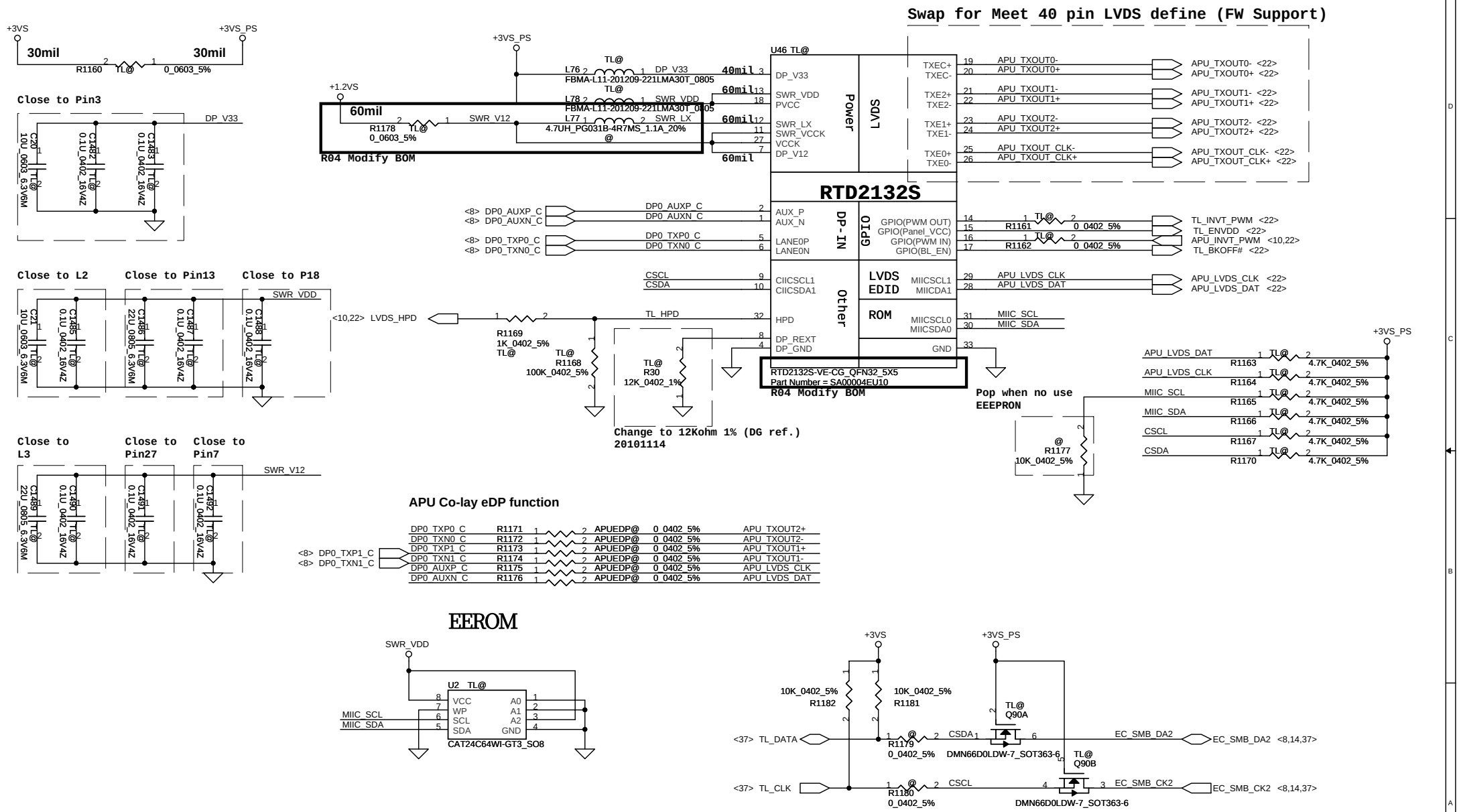

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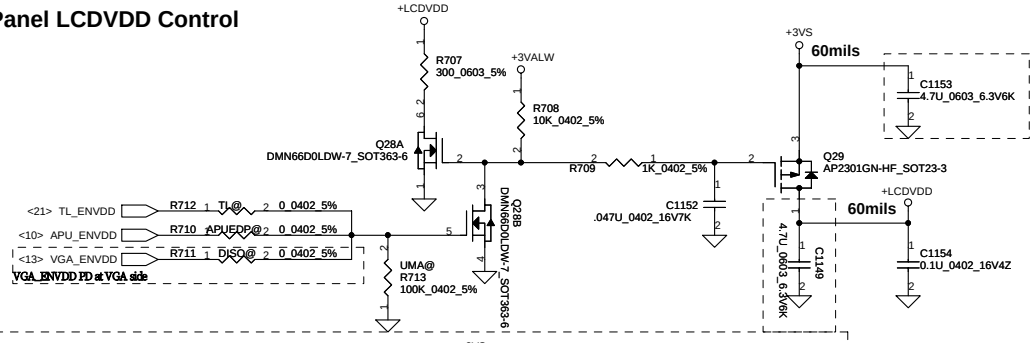
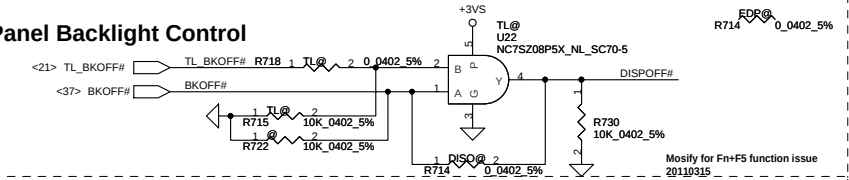
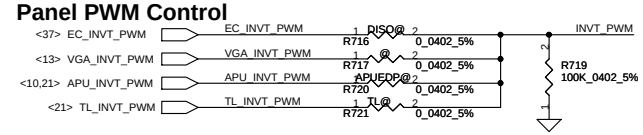
Panel LCDVDD Control



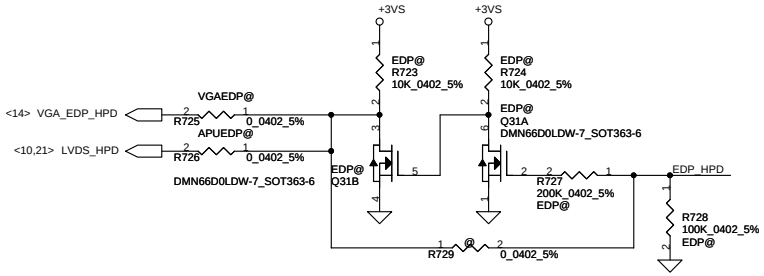
Panel Backlight Control

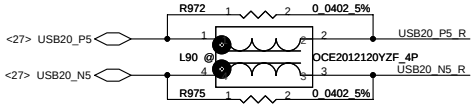


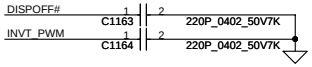
Panel PWM Control

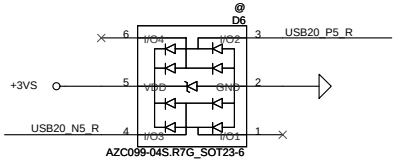


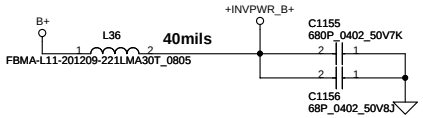
eDP HDP for APU and VGA







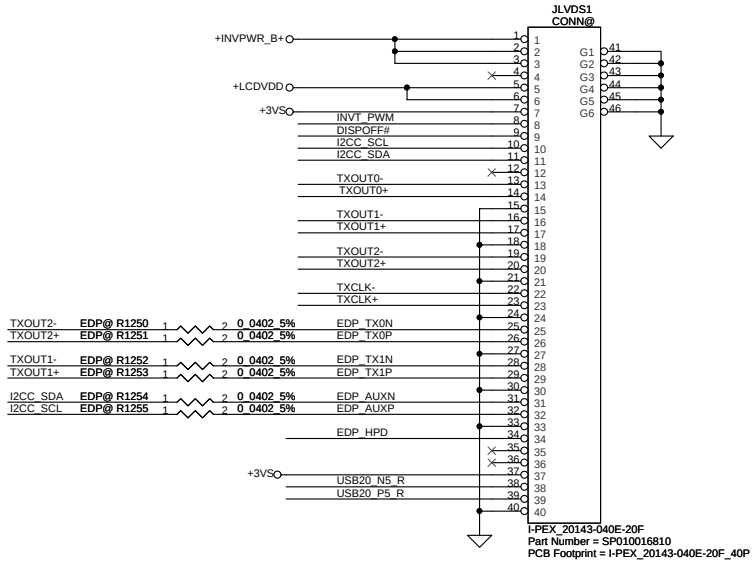




UMA/DIS LVDS/eDP Mapping table

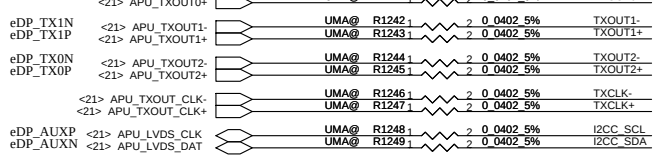
UMA		DIS		Panel
LVDS	eDP	LVDS	eDP	Conn.
APU_TXOUT0+ APU_TXOUT0-		VGA_TXOUT0+ VGA_TXOUT0-		TXOUT0+ TXOUT0-
APU_TXOUT1+ APU_TXOUT1-	DP0_TXP1_R DP0_TXN1_R	VGA_TXOUT1+ VGA_TXOUT1-	eDP_TX1P eDP_TX1N	TXOUT1+ TXOUT1-
APU_TXOUT2+ APU_TXOUT2-	DP0_TXP0_R DP0_TXN0_R	VGA_TXOUT2+ VGA_TXOUT2-	eDP_TX0P eDP_TX0N	TXOUT2+ TXOUT2-
APU_TXOUT_CLK+ APU_TXOUT_CLK-		VGA_TXCLK+ VGA_TXCLK-		TXCLK+ TXCLK-
APU_TZOUT0+ APU_TZOUT0-		VGA_TZOUT0+ VGA_TZOUT0-		TZOUT0+ TZOUT0-
APU_TZOUT1+ APU_TZOUT1-		VGA_TZOUT1+ VGA_TZOUT1-		TZOUT1+ TZOUT1-
APU_TZOUT2+ APU_TZOUT2-		VGA_TZOUT2+ VGA_TZOUT2-		TZOUT2+ TZOUT2-
APU_TZOUT_CLK+ APU_TZOUT_CLK-		VGA_TZCLK+ VGA_TZCLK-		TZCLK+ TZCLK-
APU_LVDS_CLK APU_LVDS_DAT	DP0_AUXP_R DP0_AUXN_R	VGA_LCD_CLK VGA_LCD_DATA	eDP_AUXP eDP_AUXN	I2CC_SCL I2CC_SDA

LCD/LED PANEL Conn.

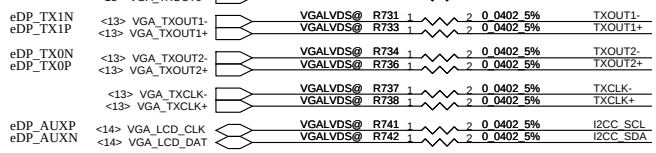


Place near LVDS Conn

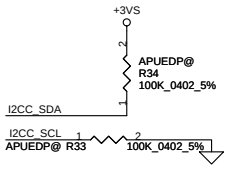
Translator LVDS Output



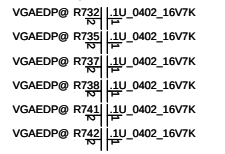
VGA LVDS Output



DG ref. Need close to eDP Conn.
201011251400



VGA Co-lay eDP function



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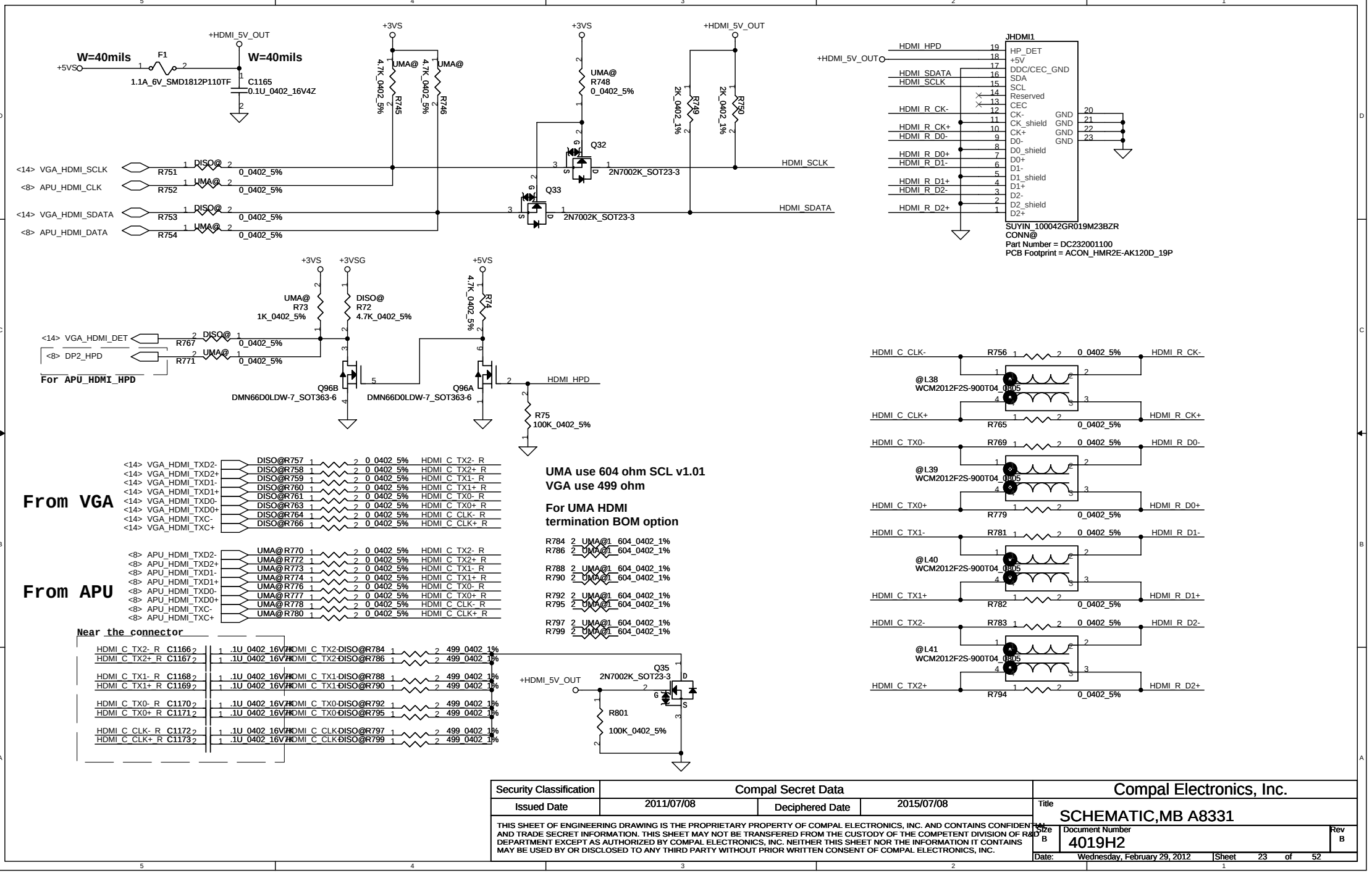

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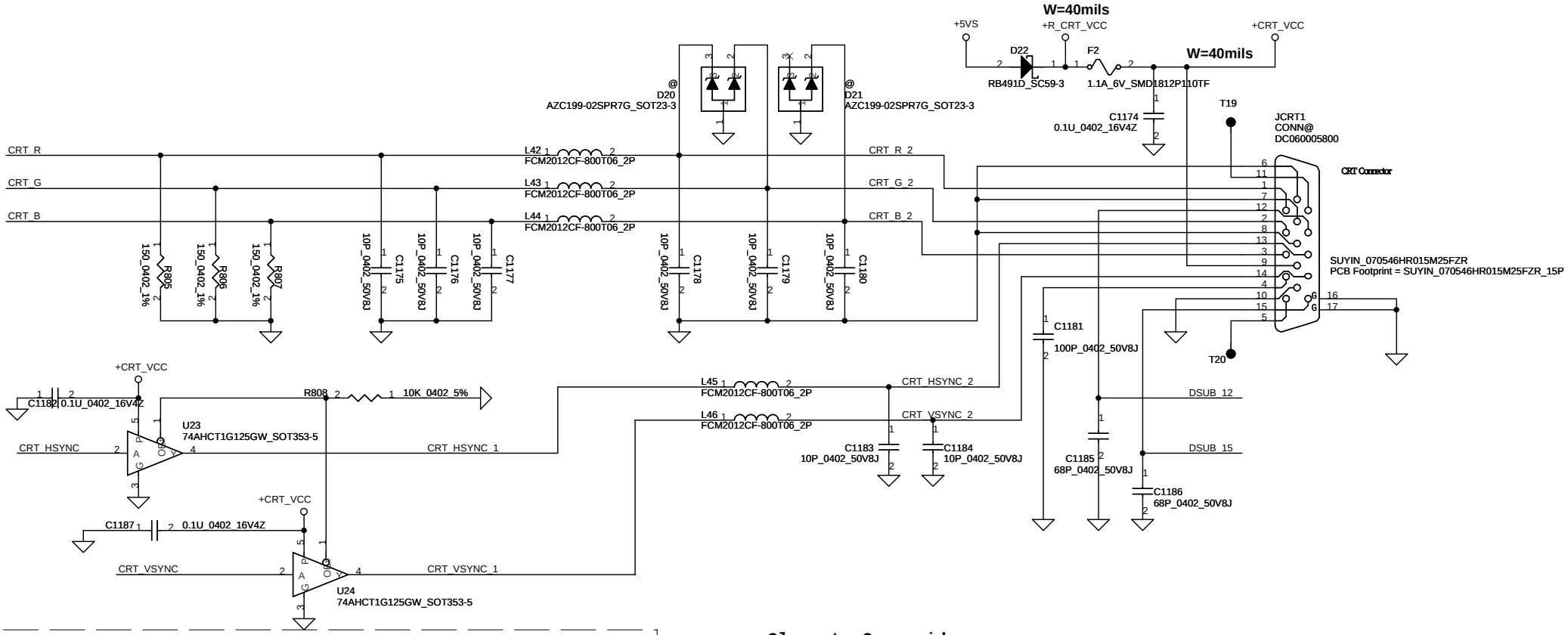


Use common via

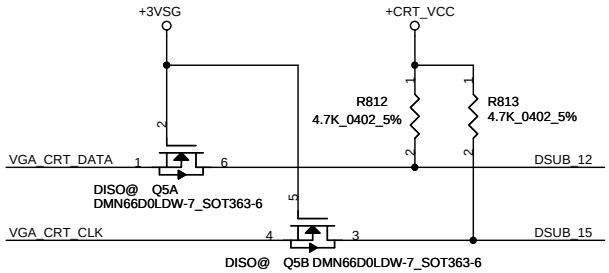
From FCH

<26> FCH_CRT_R	FCH_CRT_R	R809	UMA@	0_0402_5%	CRT_R
<26> FCH_CRT_G	FCH_CRT_G	R810	UMA@	0_0402_5%	CRT_G
<26> FCH_CRT_B	FCH_CRT_B	R811	UMA@	0_0402_5%	CRT_B
<26> FCH_CRT_HSYNC	FCH_CRT_HSYNC	R814	UMA@	0_0402_5%	CRT_HSYNC
<26> FCH_CRT_VSYNC	FCH_CRT_VSYNC	R815	UMA@	0_0402_5%	CRT_VSYNC
<26> FCH_CRT_DDC_SDA	FCH_CRT_DDC_SDA	R816	UMA@	0_0402_5%	DSUB_12
<26> FCH_CRT_DDC_SCL	FCH_CRT_DDC_SCL	R817	UMA@	0_0402_5%	DSUB_15

From VGA

<14> VGA_CRT_R	VGA_CRT_R	R818	DISO@	0_0402_5%	CRT_R
<14> VGA_CRT_G	VGA_CRT_G	R819	DISO@	0_0402_5%	CRT_G
<14> VGA_CRT_B	VGA_CRT_B	R820	DISO@	0_0402_5%	CRT_B
<14> VGA_CRT_HSYNC	VGA_CRT_HSYNC	R821	DISO@	0_0402_5%	CRT_HSYNC
<14> VGA_CRT_VSYNC	VGA_CRT_VSYNC	R822	DISO@	0_0402_5%	CRT_VSYNC
<14> VGA_CRT_DATA	VGA_CRT_DATA				
<14> VGA_CRT_CLK	VGA_CRT_CLK				

Close to Conn side



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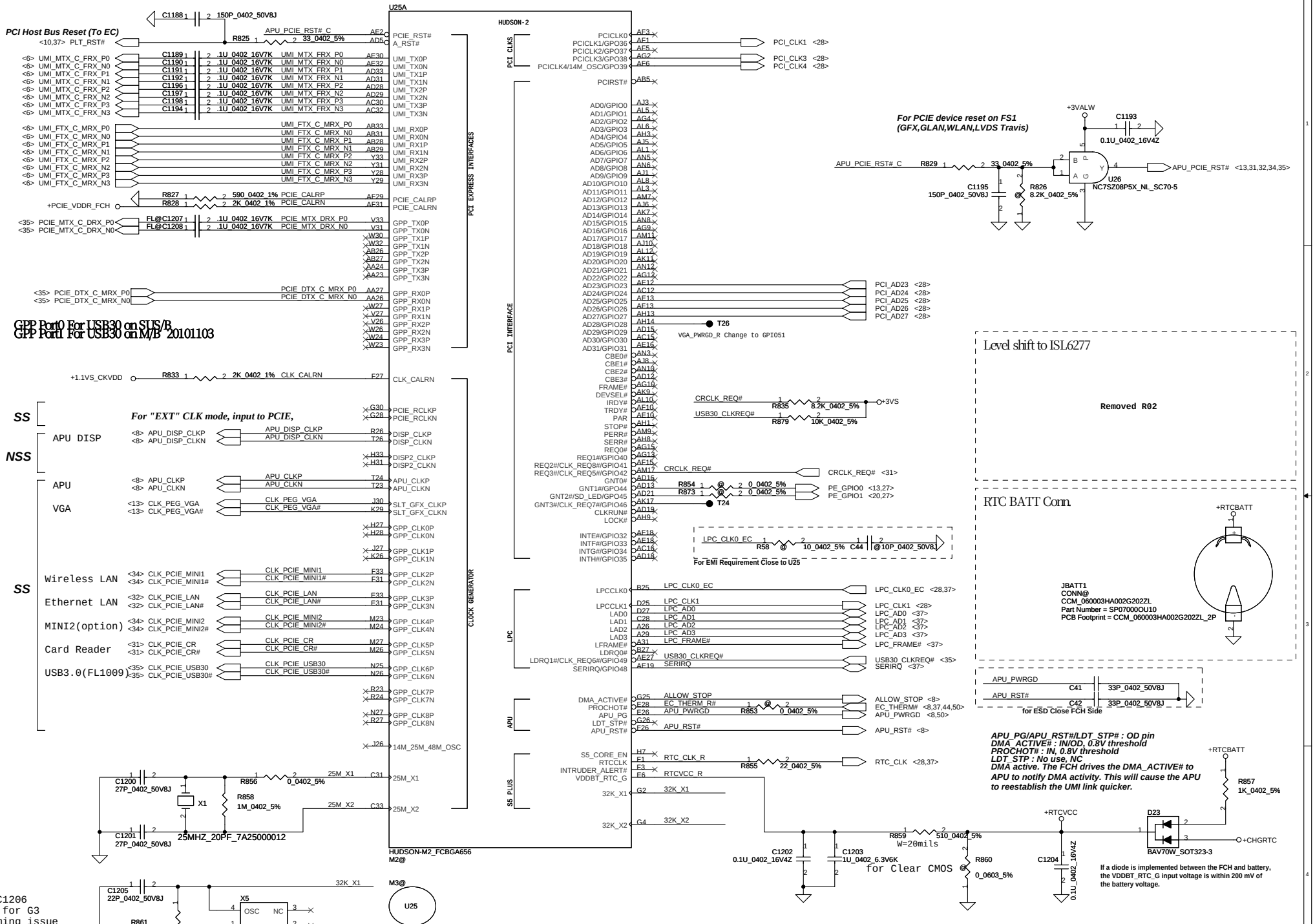

C1205,C1206
Change for G3
RTC timing issue
<improve amplitude>
R03 Modify to 22pF
follow Vender suggest

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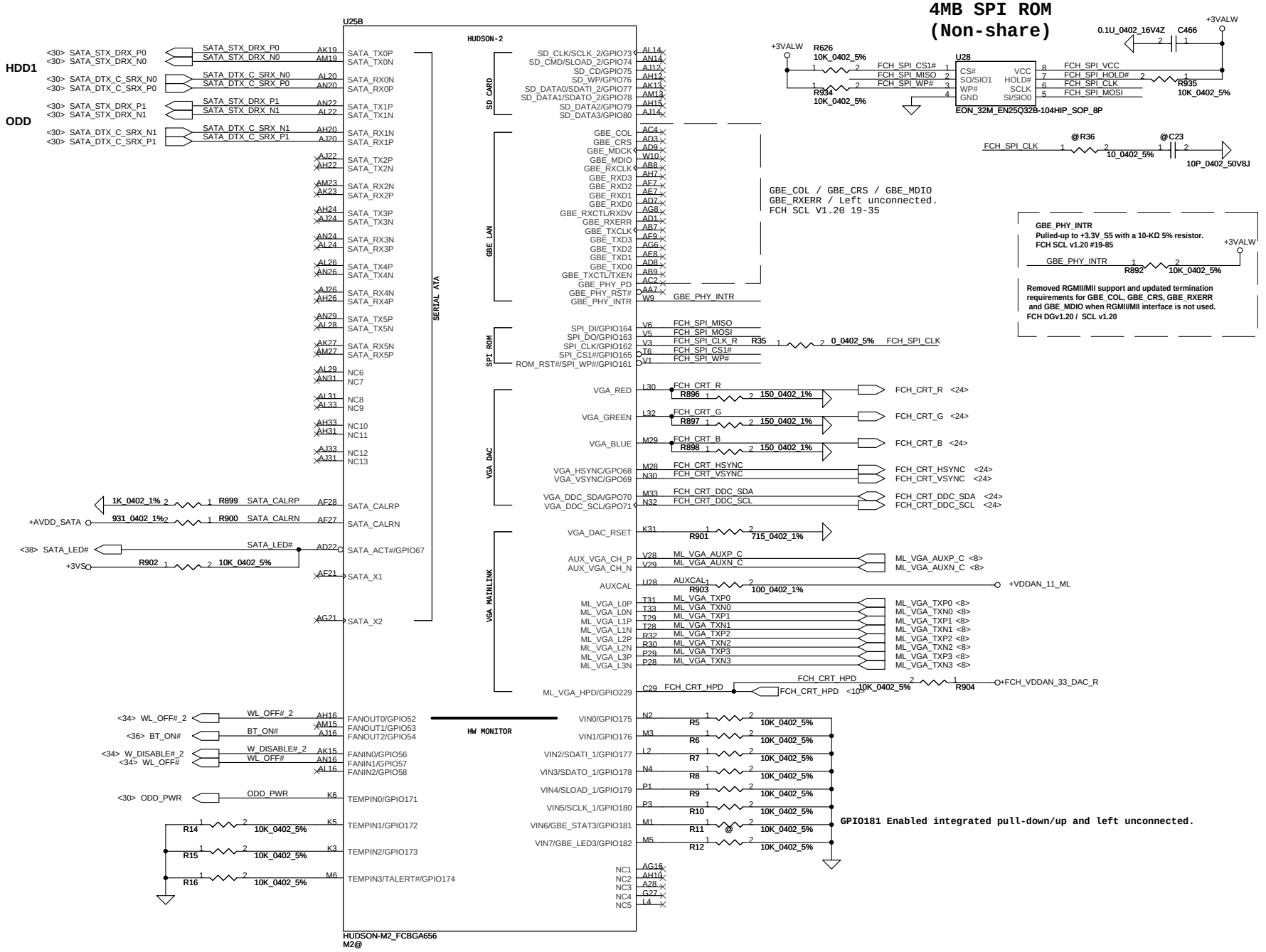
4MB SPI ROM (Non-share)



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FCH_PCIE_RST# IS FOR PCIE DEVICES ON Hudson-M2/M3

FL@ C1211 150P_0402_50V8J

R03 modify
Update BOM Structure

U25D

HUDSON-2

<35> FCH_PCIE_RST# — R837 33_0402_5% — FCH_PCIE_RST# R — AB6
<37> EC_LID_OUT# — EC_LID_OUT# — R2
W7
<37> SLP_S3# — SLP_S3# — T3
<37> SLP_S5# — SLP_S5# — W2
<37> PBTN_OUT# — PBTN_OUT# — J4
<37> FCH_PWRGD — FCH_PWRGD — N7
TEST0 — T9
TEST1 — T10
TEST2 — V9
<37> EC_GA20 — EC_GA20 — AF22
<37> EC_KBRST# — EC_KBRST# — AG19
<37> EC_SCI# — EC_SCI# — R9
<37> EC_SMI# — EC_SMI# — C26
T5
SYS_RESET# — U4
<32,34,35> FCH_PCIE_WAKE# — FCH_PCIE_WAKE# — K1
V7
<8> H_THERMTRIP# — H_THERMTRIP# — B10
WD_PWRGD — AF19
<37> EC_RSMRST# — EC_RSMRST# — U2
<34> MINI2_CLKREQ# — MINI2_CLKREQ# — AG24
<32> LAN_CLKREQ# — LAN_CLKREQ# — AE24
AF26
AE22
AH17
AG18
<39> FCH_SPKR — FCH_SPKR — AE24
<11,12,34> FCH_SCLK0 — FCH_SCLK0 — AD26
<11,12,34> FCH_SDATA0 — FCH_SDATA0 — AD25
R03 modify for TP 6P/8P
<38> FCH_SCLK1 — FCH_SCLK1 — T7
<38> FCH_SDATA1 — FCH_SDATA1 — R7
<34> MINI1_CLKREQ# — MINI1_CLKREQ# — AG25
AG22
J2
VGA_PWRGD_R — AG26
V8
W8
Y6
V10
AA8
AF25
<35> SMIB — ODD_DA# 1 — M7
R8
T1
<30> ODD_PLUG# — R78 2_0402_5% — 2ZERO@ — T32 — P6
E5
CARD_DET_FCH — P5
<36> USB_OC1# — USB_OC1# — J7
<36> USB_OC0# — USB_OC0# — T8
<39> HDA_BITCLK_AUDIO — R866 33_0402_5% — HDA_BITCLK — AB3
<39> HDA_SDOUT_AUDIO — R867 33_0402_5% — HDA_SDOUT — AB1
<39> HDA_SDIN0 — HDA_SDIN0 — AA2
HDA_SDIN1 — Y5
HDA_SDIN2 — Y3
HDA_SDIN3 — Y1
<39> HDA_SYNC_AUDIO — R868 33_0402_5% — HDA_SYNC — AD6
<39> HDA_RST_AUDIO# — R869 33_0402_5% — HDA_RST# — AE4
FCH_GPIO187 — K19
FCH_GPIO188 — H19
FCH_GPIO166 — J21
R03 modify for Resverd
FCH_GPIO189 — D21
FCH_GPIO190 — C20
<13,25> PE_GPIO0 — 0_0402_5% — R842 — D23
<20,25> PE_GPIO1 — 0_0402_5% — R843 — C22
E21
E20
E20
A22
E18
A20
J18
H18
G18
B21
K18
D19
A18
C18
B19
B17
A24
D17

R03 modify
remove D44/D45

HUDSON-M2_FCBGA656
M2@

THERMTRIP:
Need level shift from +3VALW to +1.5V
Note: Ensure FCH internal pull-up resistor to +3.3V S5 is disabled to prevent leakage when APU is powered down.

SM bus 0-->S0 PWR domain
SM bus 1-->S5 PWR domain

FCH GEVENT (S5 domain)
with isolation circuit to avoid leakage

+3VS +3VS
ZERO@ R954 10K_0402_5%
<30> ODD_DA# — Q84 2N7002K_SOT23-3 ZERO@ — ODD_DA# 1

+3VS +3VS
R955 10K_0402_5%
<31> CARD_DET — Q85 2N7002K_SOT23-3 — CARD_DET_FCH

33ohm termination
resistor at CODEC side

+3VALW
R54 100K_0402_5% — USB_OC1#
R871 10K_0402_5% — H_THERMTRIP#
R874 2.2K_0402_5% — FCH_SCLK1
R876 2.2K_0402_5% — FCH_SDATA1
R877 100K_0402_5% — EC_LID_OUT#
R878 10K_0402_5% — FCH_PCIE_WAKE#
R18 10K_0402_5% — SYS_RESET#
R37 10K_0402_5% — SMIB
R942 8.2K_0402_5% — LAN_CLKREQ#

For FCH internal debug use
R887 2.2K_0402_5% — TEST0
R889 2.2K_0402_5% — TEST1
R890 2.2K_0402_5% — TEST2

+3VS
R880 2.2K_0402_5% — FCH_SCLK0
R881 2.2K_0402_5% — FCH_SDATA0
R882 8.2K_0402_5% — MINI1_CLKREQ#
R883 8.2K_0402_5% — MINI2_CLKREQ#
R862 10K_0402_5% — WD_PWRGD
R940 8.2K_0402_5% — LAN_CLKREQ#
R884 2.2K_0402_5% — EC_RSMRST#
R885 10K_0402_5% — HDA_BITCLK
R886 10K_0402_5% — HDA_SDIN0
R888 10K_0402_5% — HDA_SDIN1
R891 10K_0402_5% — HDA_SDIN2
R893 10K_0402_5% — HDA_SDIN3

R03 modify

+3VALW
EDP@ R65 2.2K_0402_5%
M2@ R49 2.2K_0402_5%
PX@ R47 2.2K_0402_5%
VGA@ R45 2.2K_0402_5%
R43 2.2K_0402_5%
FCH_GPIO189
FCH_GPIO190
FCH_GPIO188
FCH_GPIO187
FCH_GPIO166
R51 100K_0402_5%
R50 100K_0402_5%
R48 100K_0402_5%
R46 100K_0402_5%
R44 100K_0402_5%

Project SKU ID	Value	
GPIO189 (use VGA)	Low (UMA)	High (VGA)
GPIO190 (use PX)	Low (noPX)	High (PX)
GPIO188 (USB2/3)	High (2.0)	Low (3.0)
GPIO187 (LVDS/eDP)	Low (LVDS)	High (eDP)
GPIO166 (Resverd)		

USB MISC
USB_RCOMP — R863 11.8K_0402_1%
USB 1.1
USB_FSD1P/GPIO186 — USB_FSD1N
USB_FSD0P/GPIO185 — USB_FSD0N
USB_HSD13P — USB_HSD13N
USB_HSD12P — USB_HSD12N
USB_HSD11P — USB_HSD11N
USB_HSD10P — USB_HSD10N
USB_HSD9P — USB_HSD9N
USB_HSD8P — USB_HSD8N
USB_HSD7P — USB_HSD7N
USB_HSD6P — USB_HSD6N
USB_HSD5P — USB_HSD5N
USB_HSD4P — USB_HSD4N
USB_HSD3P — USB_HSD3N
USB_HSD2P — USB_HSD2N
USB_HSD1P — USB_HSD1N
USB_HSD0P — USB_HSD0N
USB 2.0
USB_CLKRN/14M_25M_48M_OSC
USB_CLKRP
USB_HSD13P — USB30_P10 — USB30_P10 <36>
USB_HSD13N — USB30_N10 — USB30_N10 <36>
USB_HSD9P — USB20_P9 — USB20_P9 <34>
USB_HSD9N — USB20_N9 — USB20_N9 <34>
USB_HSD8P — USB20_P8 — USB20_P8 <34>
USB_HSD8N — USB20_N8 — USB20_N8 <34>
USB_HSD7P — USB20_P7 — USB20_P7 <36>
USB_HSD7N — USB20_N7 — USB20_N7 <36>
USB_HSD5P — USB20_P5 — USB20_P5 <22>
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USB_HSD1N — USB20_N1 — USB20_N1 <36>
USB_HSD0P — USB20_P0 — USB20_P0 <36>
USB_HSD0N — USB20_N0 — USB20_N0 <36>
USB 3.0
USBSS_CALRP — USBSS_CALRP — R864 1K_0402_1% — +FCH_VDD_11_SSUSB_S
USBSS_CALRN — USBSS_CALRN — R865 1K_0402_1%
USB_SS_TX3P — USB_SS_TX3N
USB_SS_RX3P — USB_SS_RX3N
USB_SS_TX2P — USB30_MTX_DRX_P2 — USB30_MTX_DRX_P2 <36>
USB_SS_TX2N — USB30_MTX_DRX_N2 — USB30_MTX_DRX_N2 <36>
USB_SS_RX2P — USB30_MRX_DTX_P2 — USB30_MRX_DTX_P2 <36>
USB_SS_RX2N — USB30_MRX_DTX_N2 — USB30_MRX_DTX_N2 <36>
USB_SS_TX1P — USB30_MTX_DRX_P1 — USB30_MTX_DRX_P1 <36>
USB_SS_TX1N — USB30_MTX_DRX_N1 — USB30_MTX_DRX_N1 <36>
USB_SS_RX1P — USB30_MRX_DTX_P1 — USB30_MRX_DTX_P1 <36>
USB_SS_RX1N — USB30_MRX_DTX_N1 — USB30_MRX_DTX_N1 <36>
USB_SS_TX0P — USB30_MTX_DRX_P0 — C39 M3@ — .1U_0402_16V7K — USB30TXP <35,36>
USB_SS_TX0N — USB30_MTX_DRX_N0 — C37 M3@ — .1U_0402_16V7K — USB30TXN <35,36>
USB_SS_RX0P — USB30_MRX_DTX_P0 — USB30_MRX_DTX_P0 <36>
USB_SS_RX0N — USB30_MRX_DTX_N0 — USB30_MRX_DTX_N0 <36>
HD AUDIO
EMBEDDED CTRL
SCL2/GPIO193 — R870 10K_0402_5%
SDA2/GPIO194 — R872 10K_0402_5%
SCL3_LV/GPIO195 — R90 10K_0402_5%
SDA3_LV/GPIO196 — R91 10K_0402_5%
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199 — EC_PWM2 — EC_PWM2 <28>
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208

ACPI / WAKE UP EVENTS
GPIO
USB OC

Hudson-M2/M3
EHCI CTL
DEV 20, Fn 5
<Disable CTL>

30 Pin Sub board USB3.0 Conn — Hudson-M2 EHCI CTL DEV 22, Fn 2 <Disable CTL of M2> — Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0
30 Pin Sub board USB3.0 Conn
On board USB Conn
Mini2-Option — Hudson-M2/M3 EHCI CTL DEV 19, Fn 2
Mini1-WLAN
BT
Camera
Hudson-M2/M3 EHCI CTL DEV 18, Fn 2 <Support Wakeup>
For Right Side USB2.0 Port
Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0
30 Pin Sub board USB3.0 Conn
30 Pin Sub board USB3.0 Conn
On board USB Conn

For PCIE device reset on FS1
(GFX,GLAN,WLAN,LVDS Travis)

+3VALW
@C1199 0.1U_0402_16V4Z
@U27 NC7SZ08P5X_NL_SC70-5
<20,49> VGA_PWRGD — VGA_PWRGD — R830 0_0402_5% — VGA_PWRGD_R
R831 @100K_0402_5%
R832 0_0402_5%

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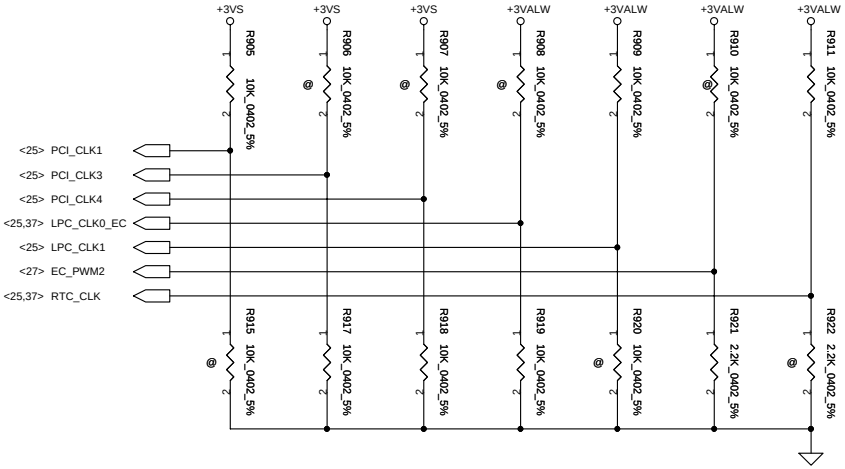
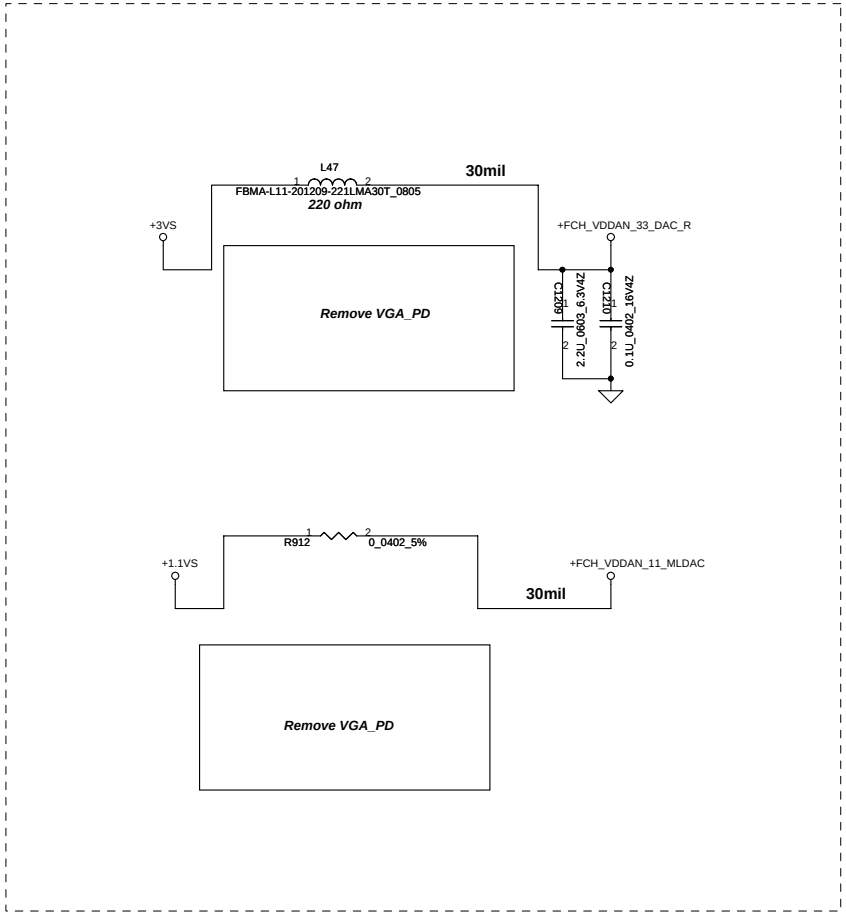
STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



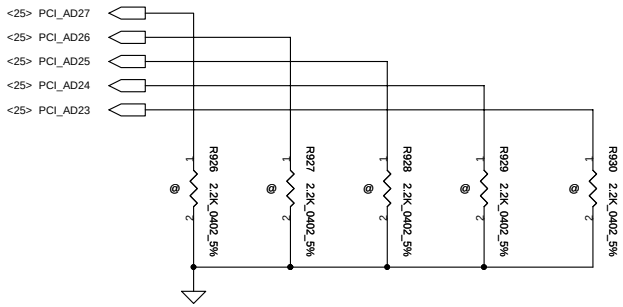


DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26

	PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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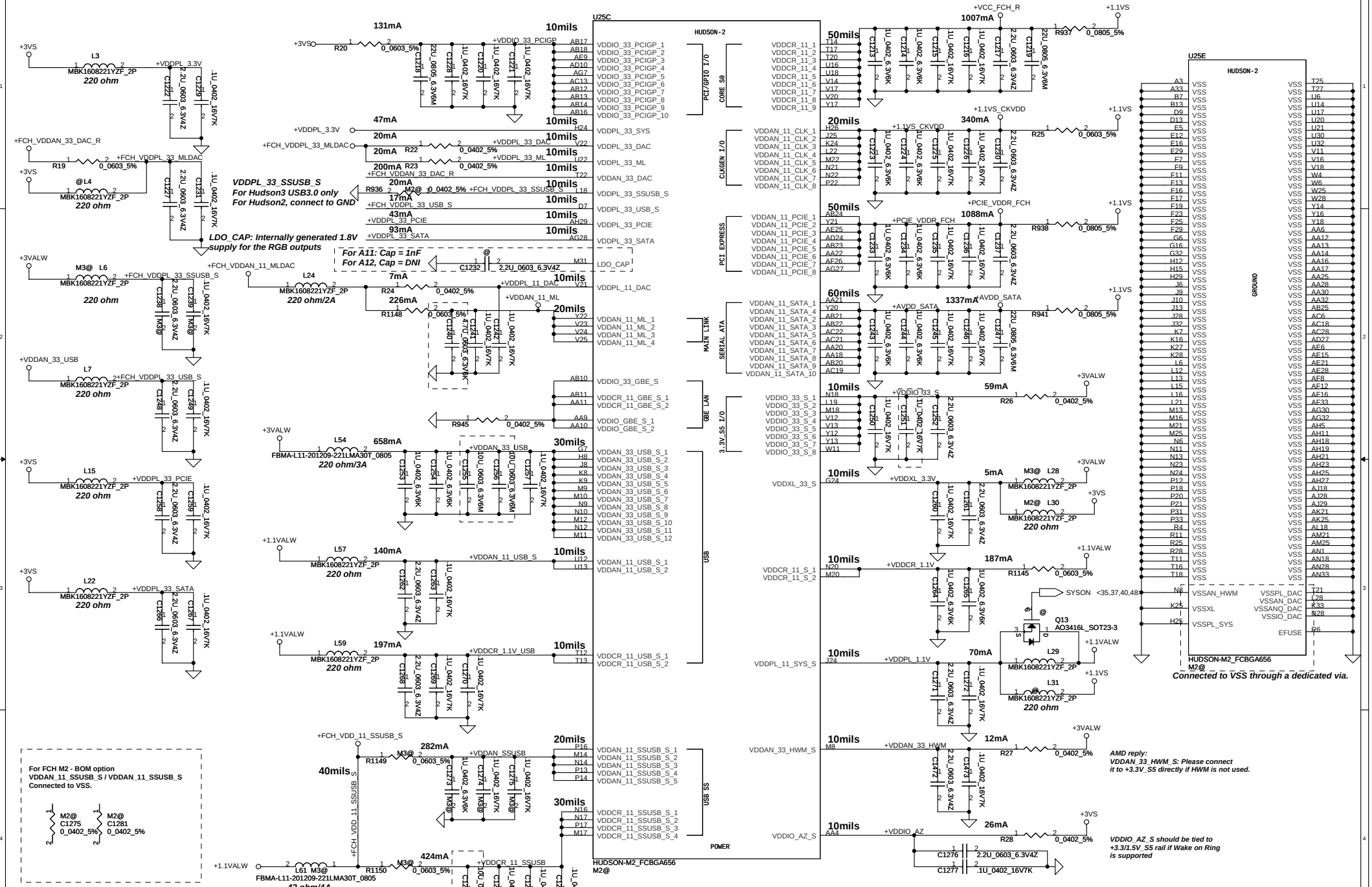

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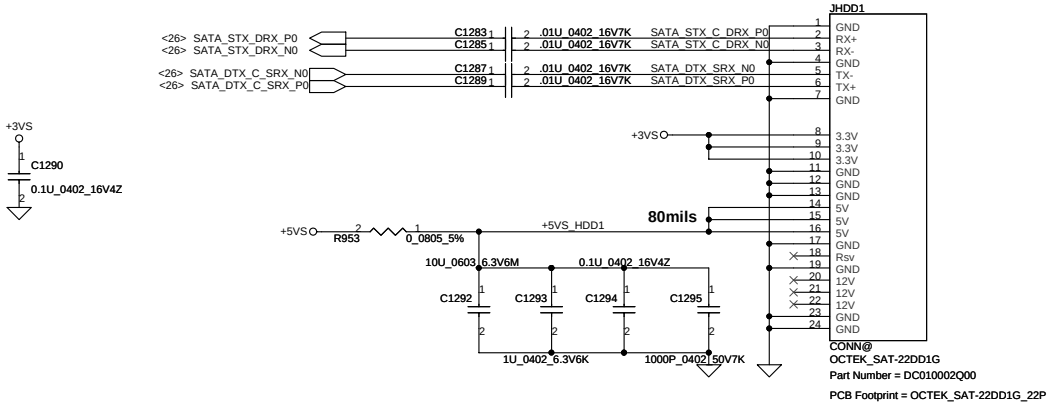
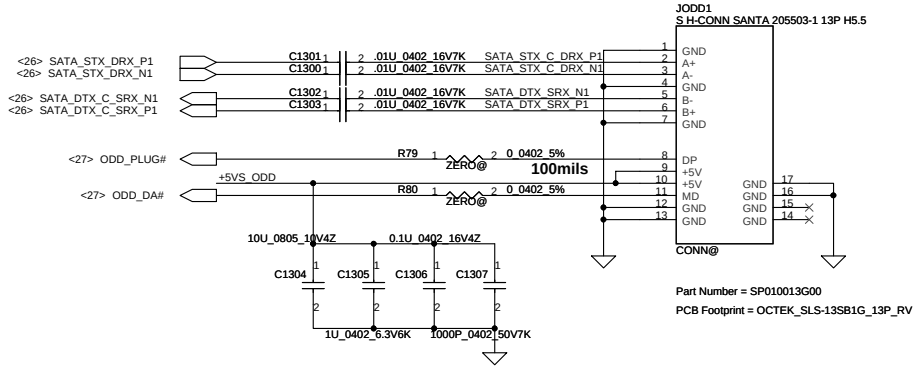
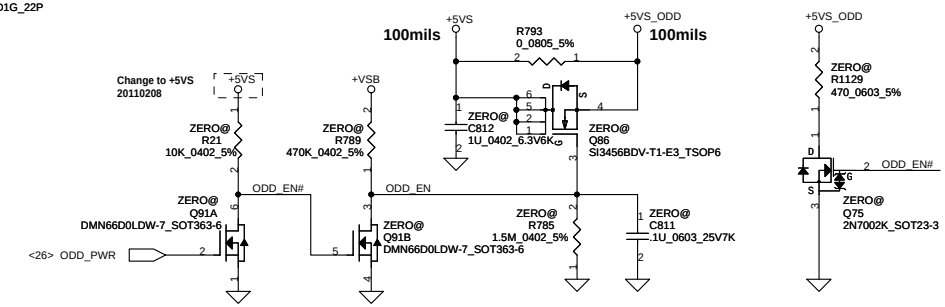
SATA HDD1 Conn.

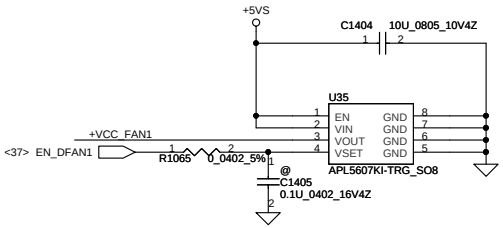


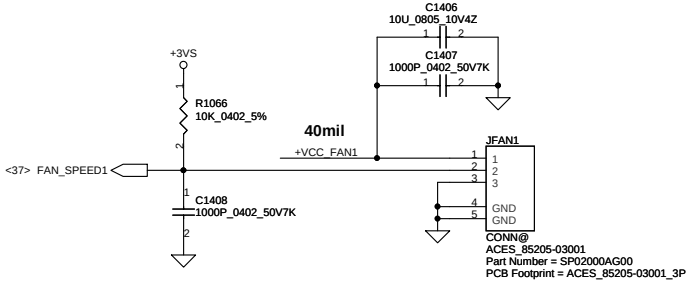
SATA ODD Conn.





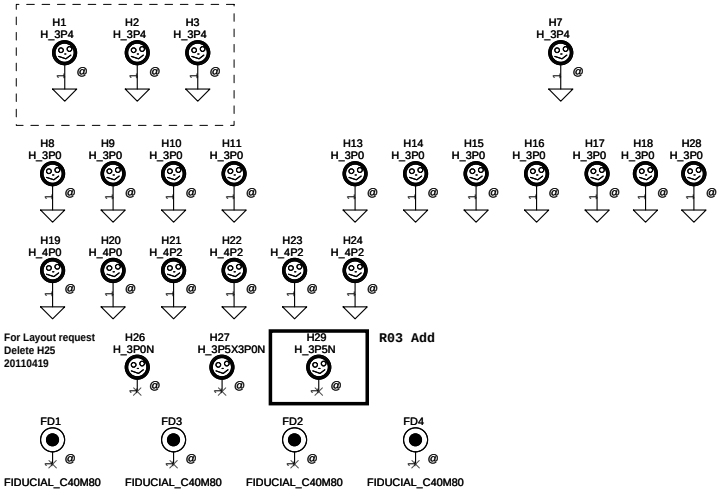
FAN





Screw Hole Follow P5WE0

FAN Stand-Off



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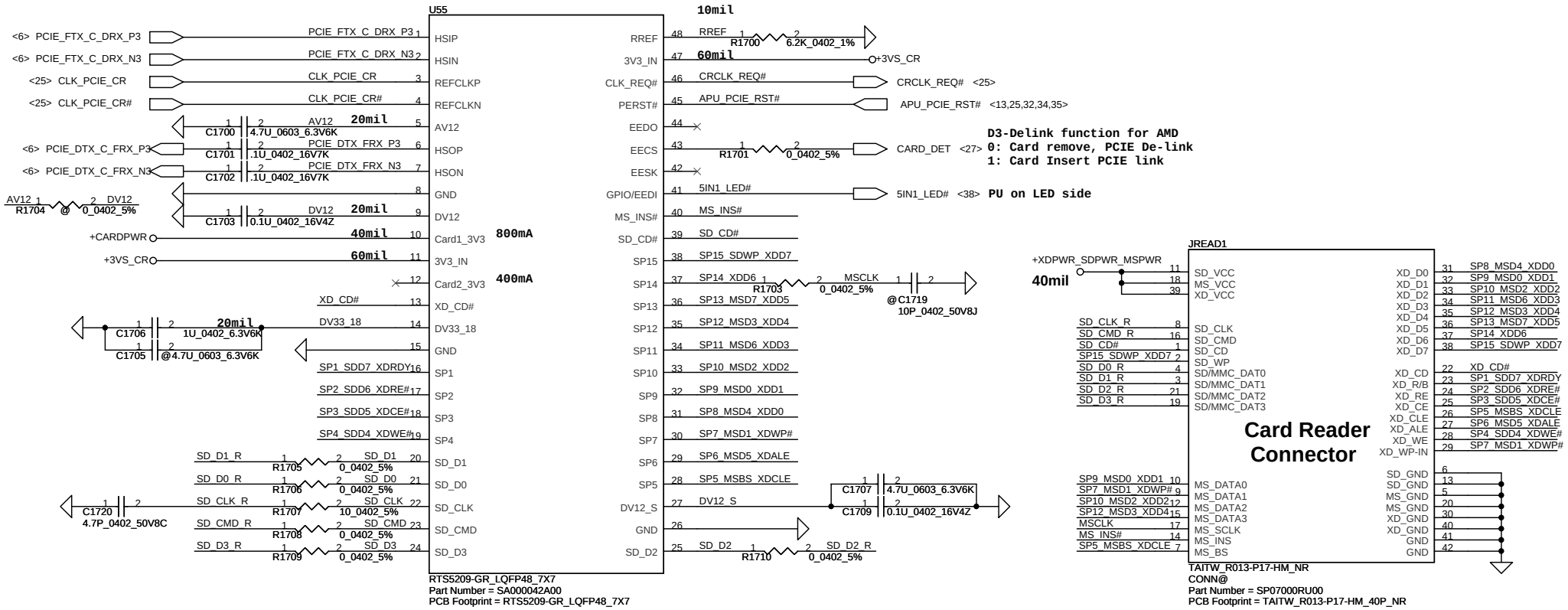

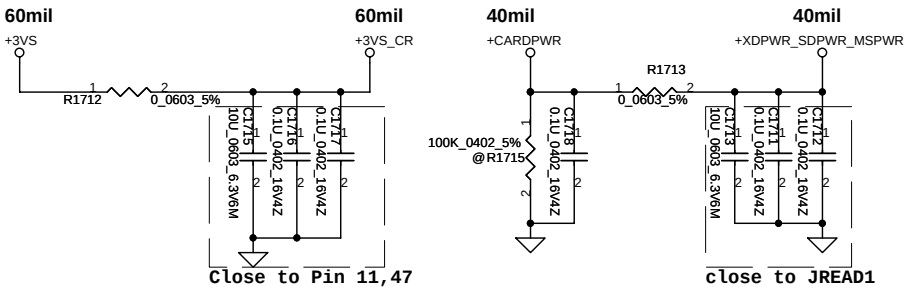

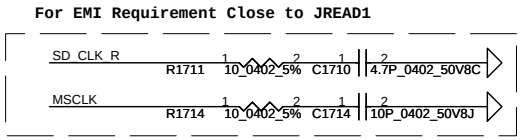

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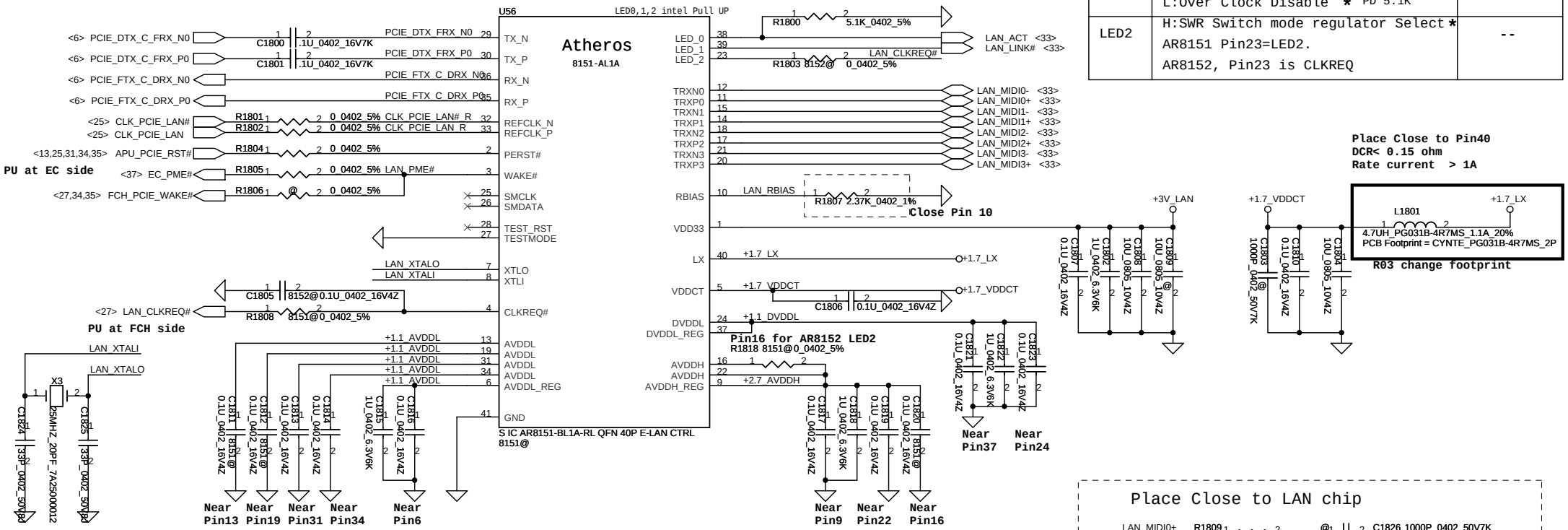
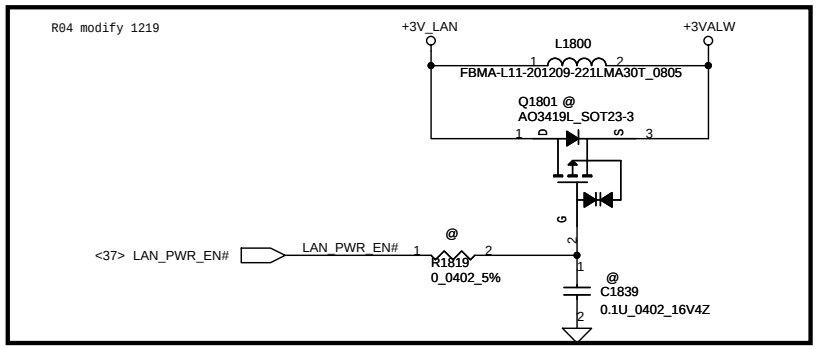
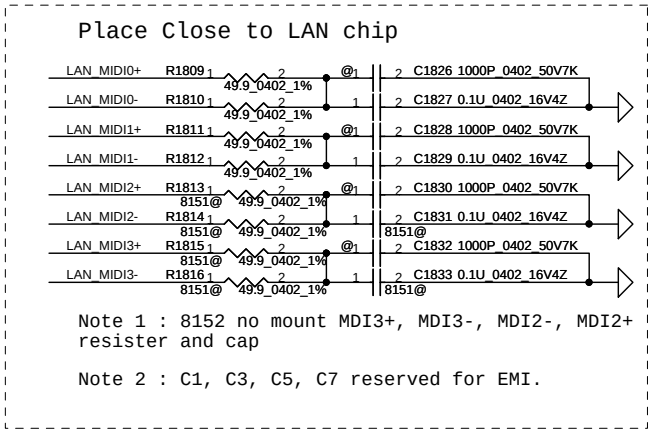
Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable * PD 5.1K	H
LED2	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--







	Pin4	Configure R1808	Configure C1805		Pin23	Configure R1803
AR8152	VDDCT_REG		*		CLKREQn	*
AR8151	CLKREQn	*			LED[2]	

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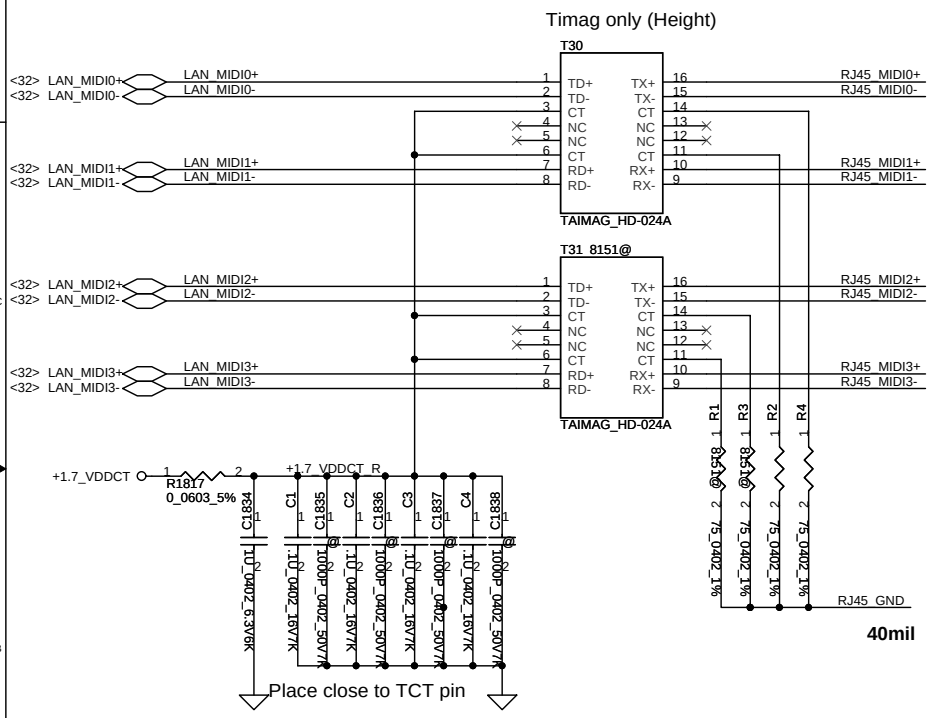

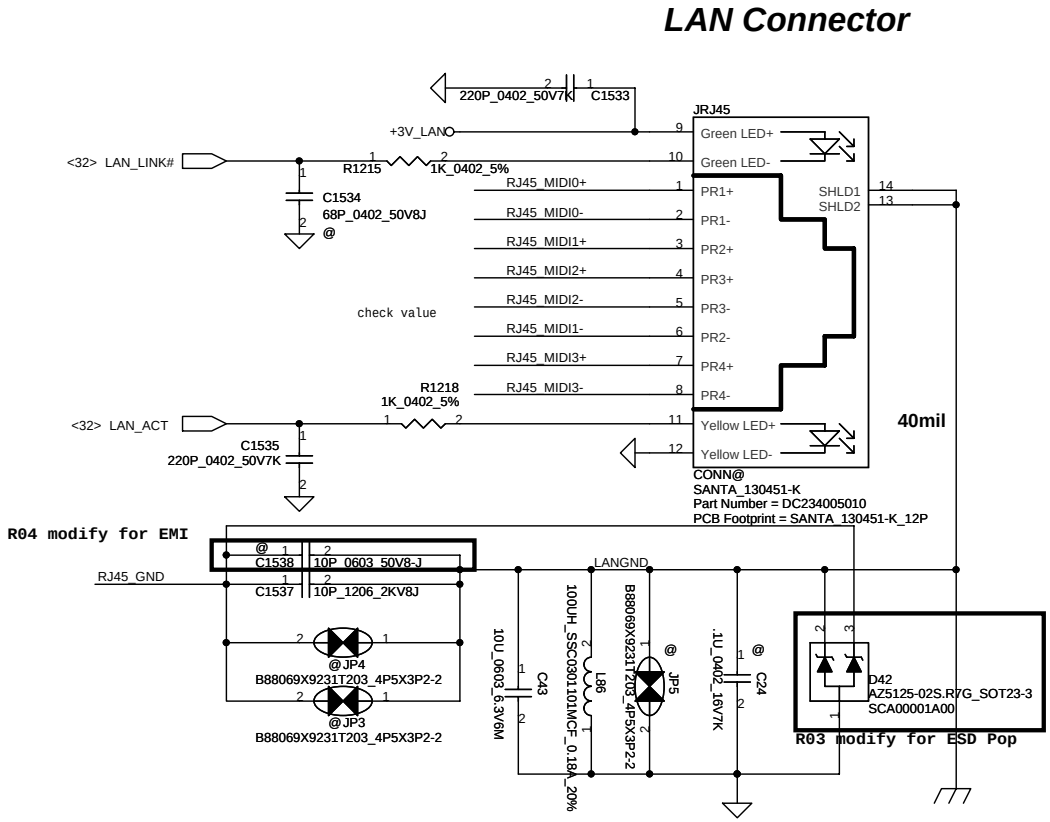

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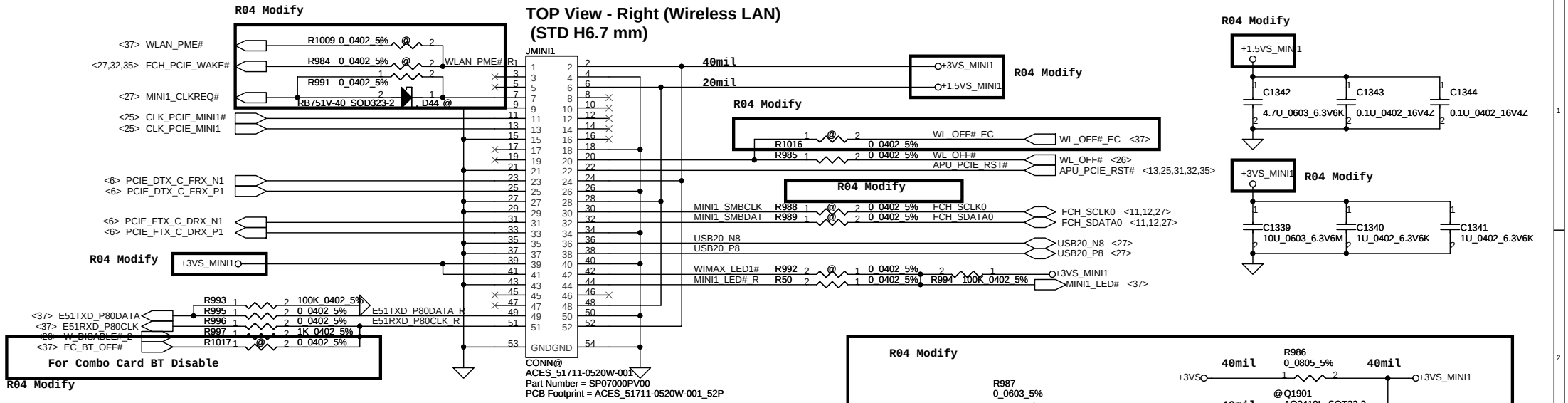
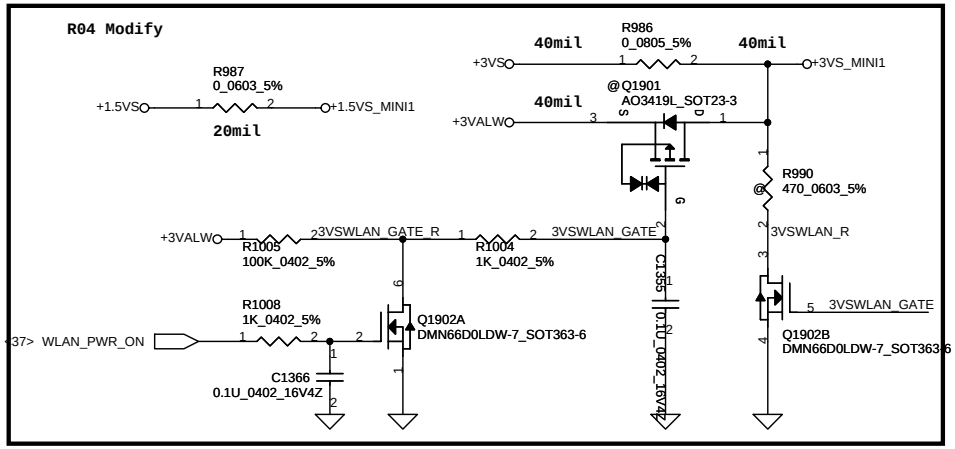
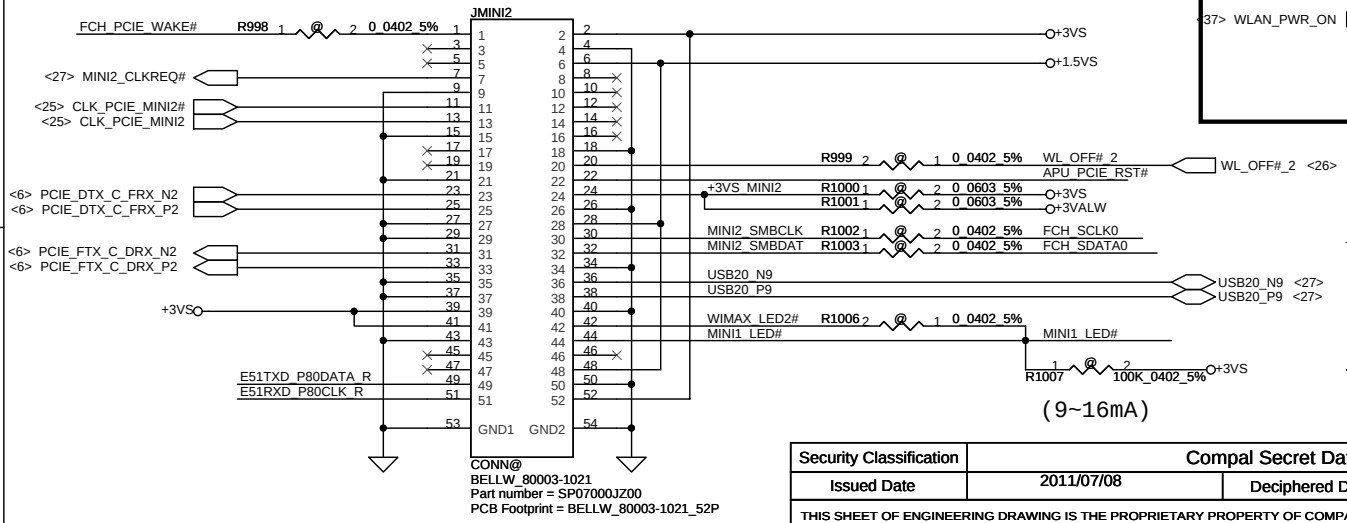
TOP View - Right (Wireless LAN) (STD H6.7 mm)

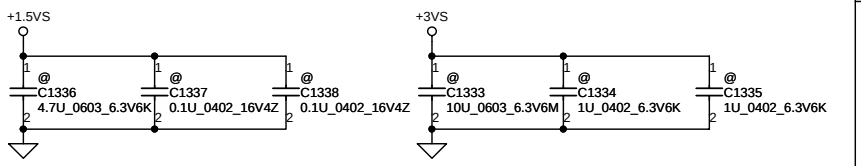




TOP View - Left (Option) (STD H5.7mm)



(9~16mA)



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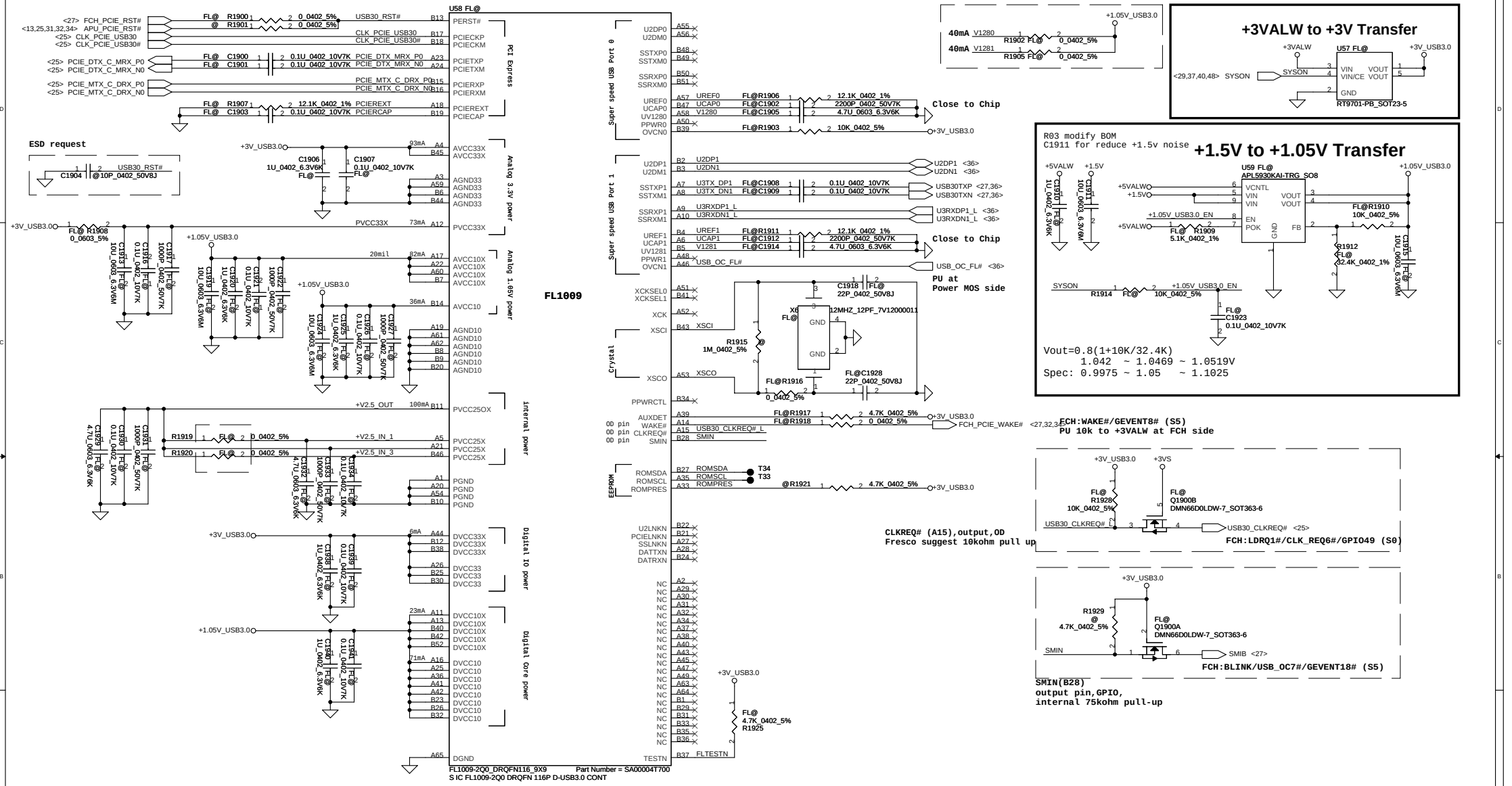

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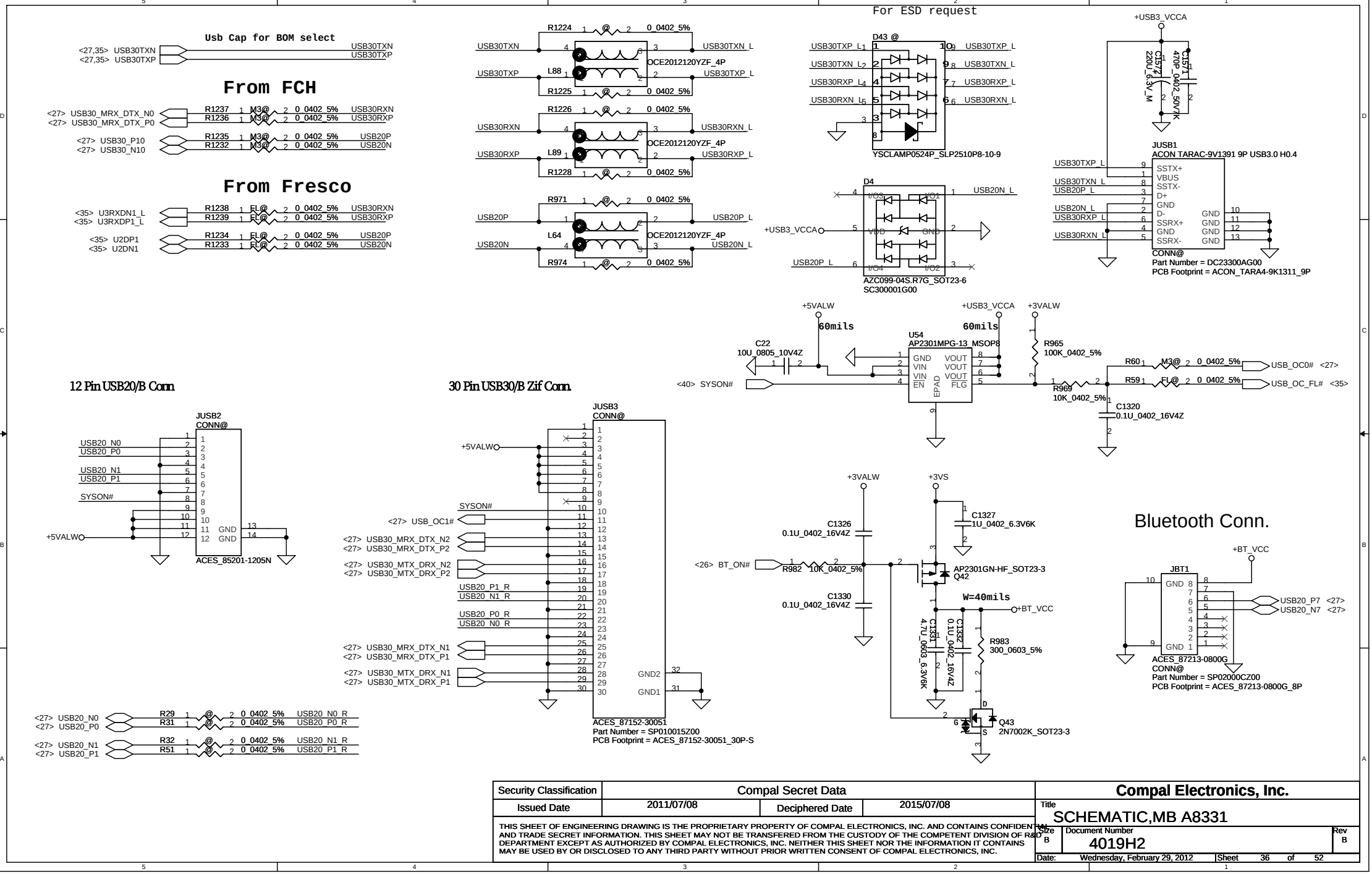

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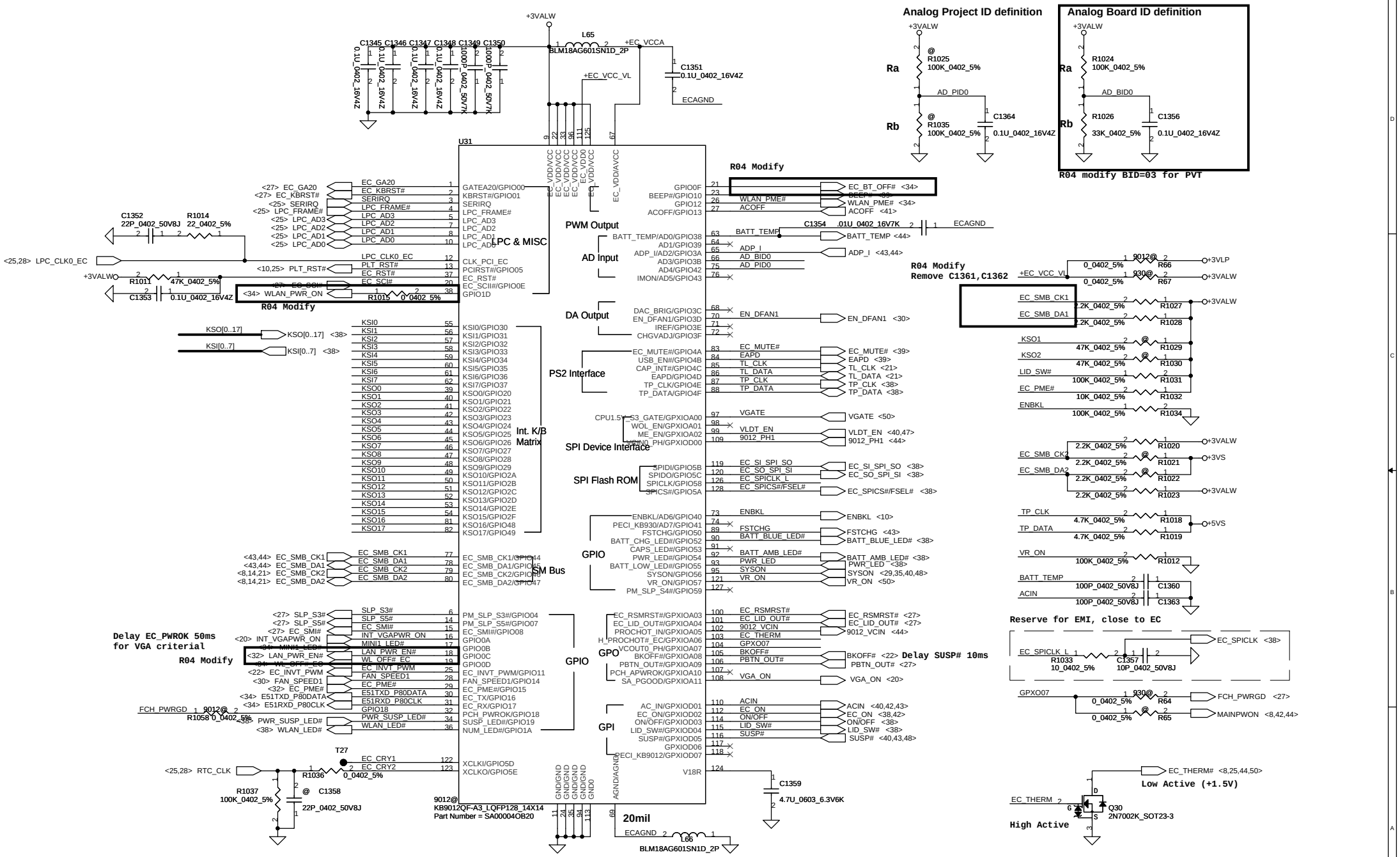

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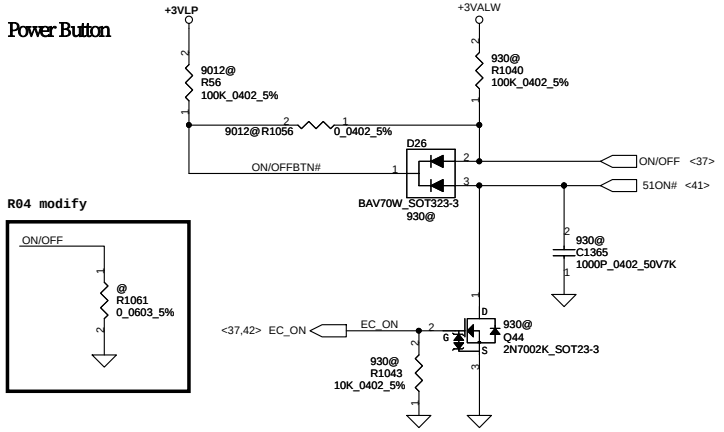
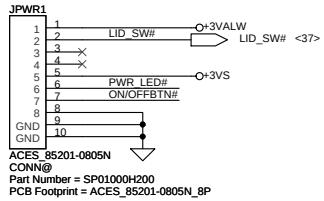
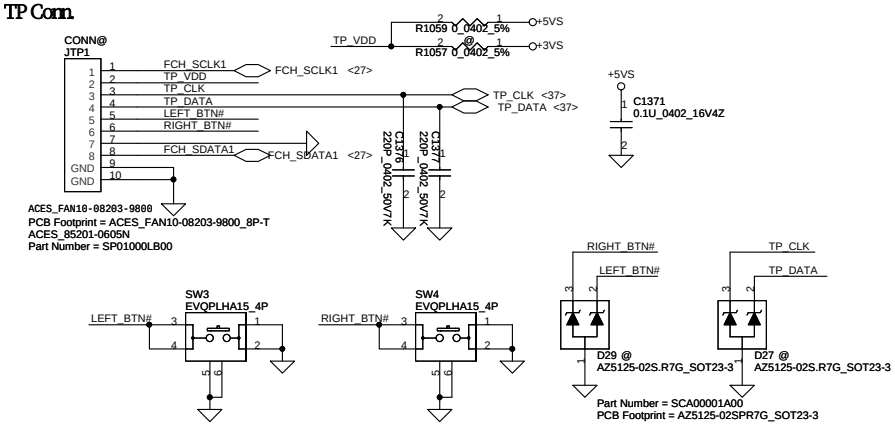
Power Button



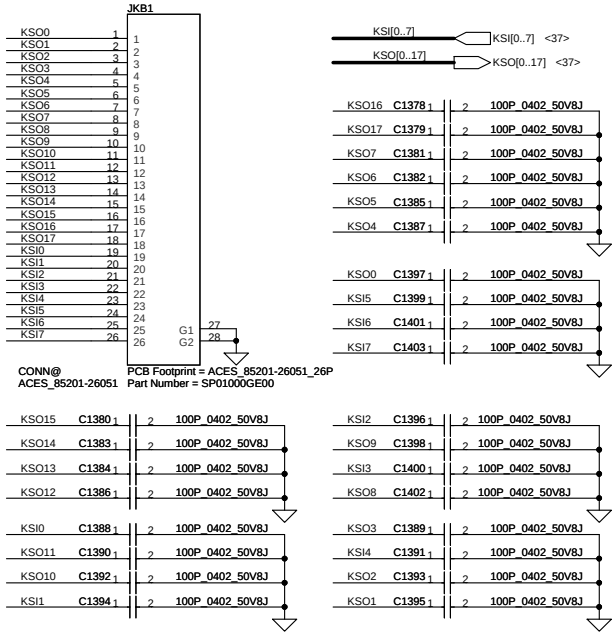
POWER/B



TP Conn.



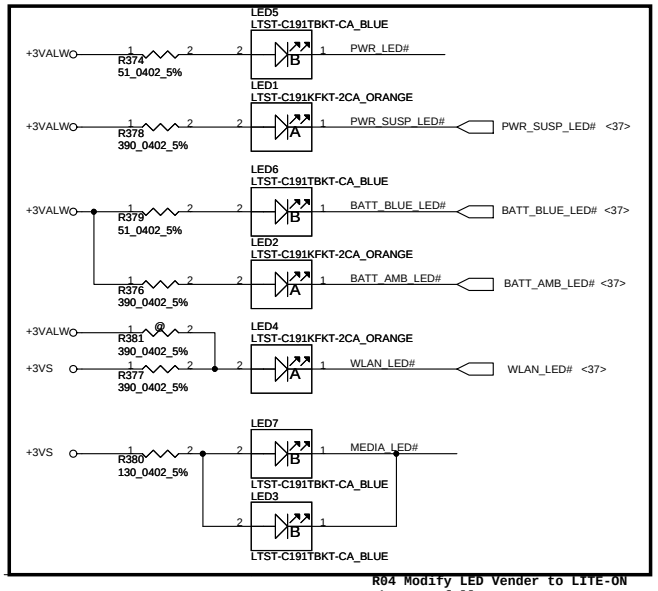
KB Conn.



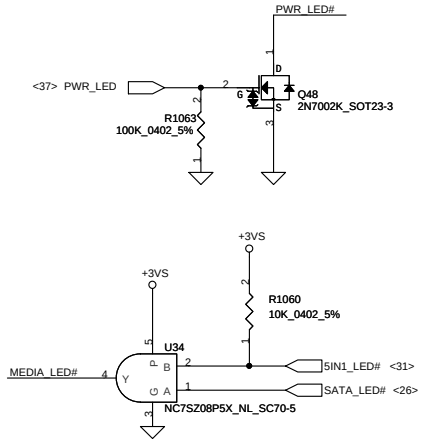
LED

LED Status	Power/SUS		Battery		3G / WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber		Amber		

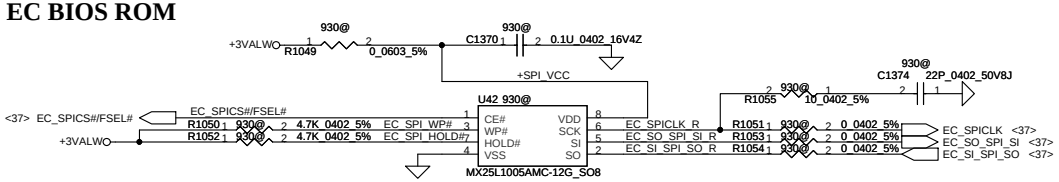
removed



R04 Modify LED Vender to LITE-ON
Change R follow Q5WVH



EC BIOS ROM



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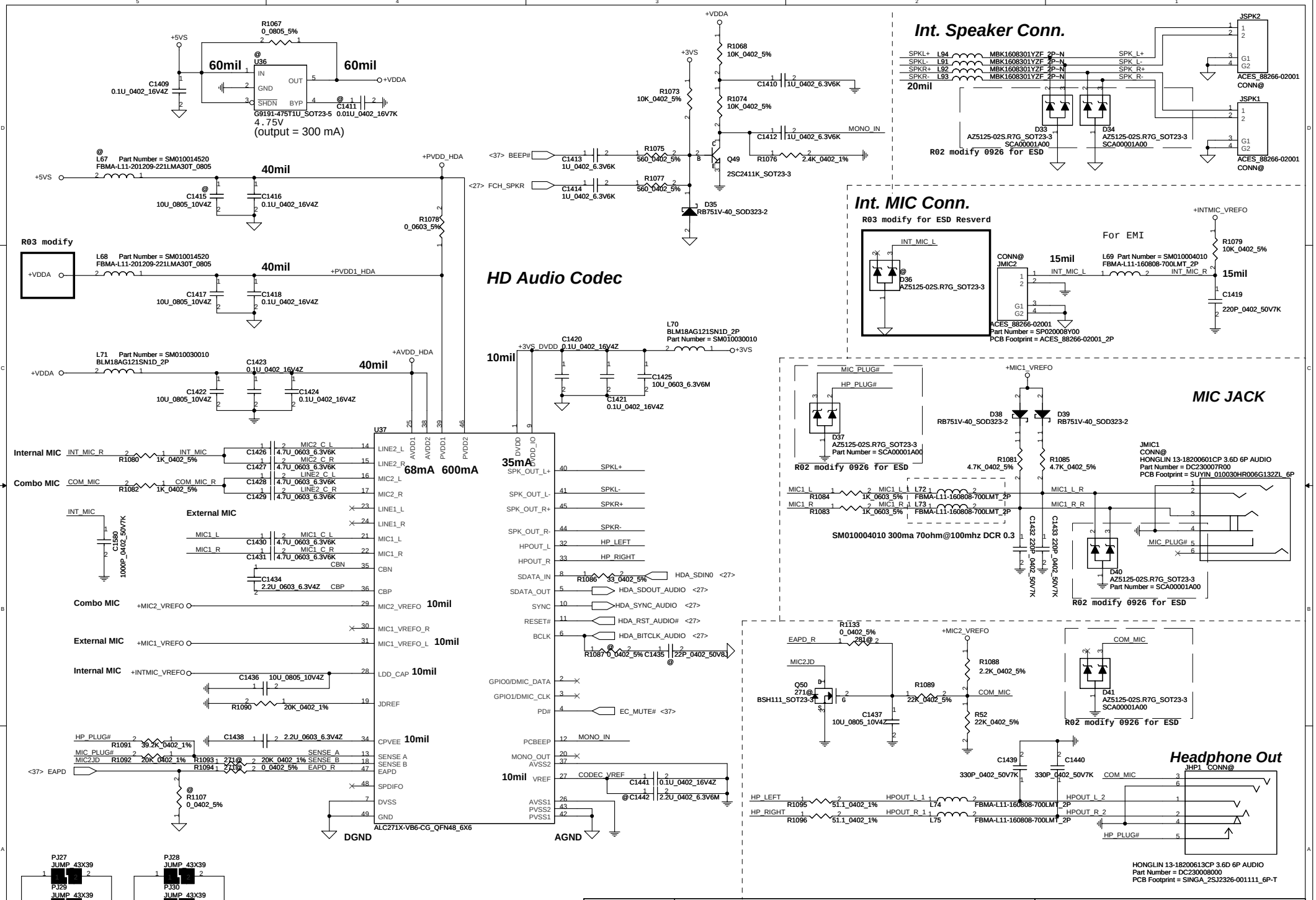
Int. Speaker Conn.
Int. MIC Conn.
HD Audio Codec
MIC JACK
Headphone Out
R03 modify
R02 modify 0926 for ESD
U37
ALC271X-VB6-CG_QFN48_6X6
DGND
AGND
G9191-475T1U_SOT23-5
4.75V
(output = 300 mA)
SM010004010 300ma 70ohm@100mhz DCR 0.3
HONGLIN 13-18200601CP 3.6D 6P AUDIO
HONGLIN 13-18200613CP 3.6D 6P AUDIO
Internal MIC
Combo MIC
External MIC
68mA 600mA
35mA
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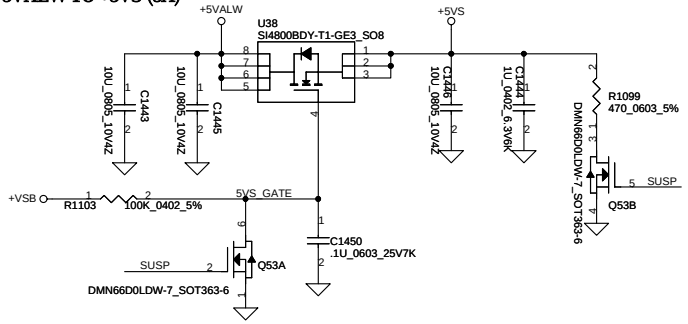
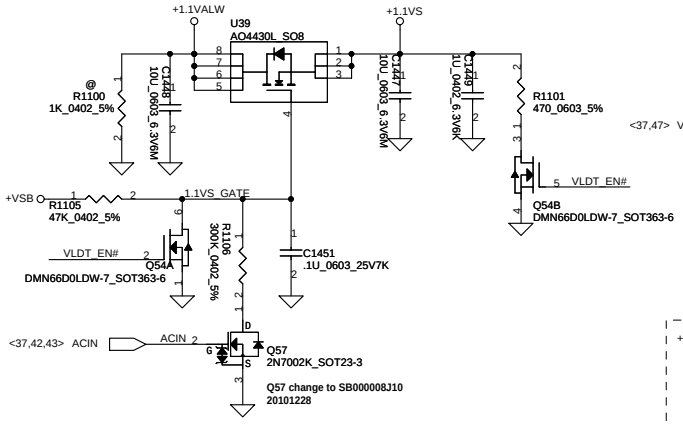
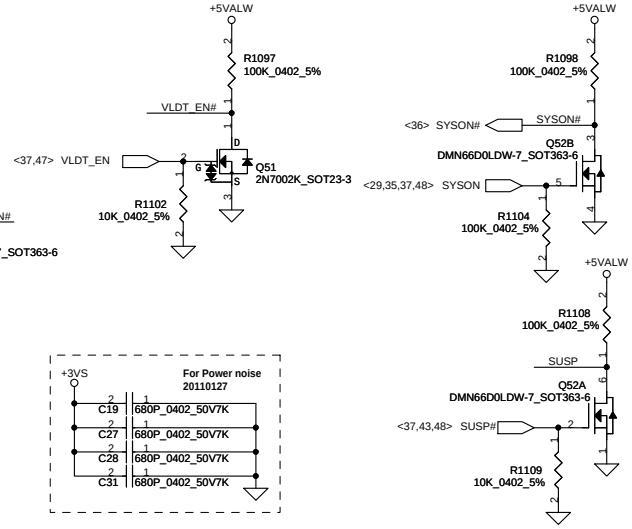
+5VALW TO +5VS (5A)

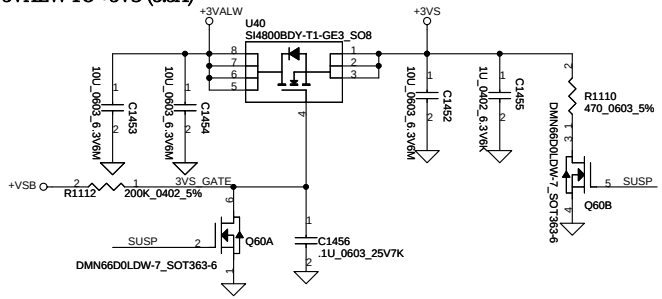


+1.1VALW TO +1.1VS (1.1A)

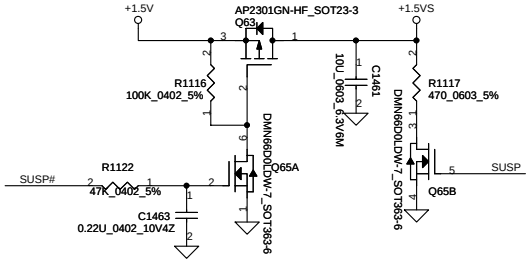




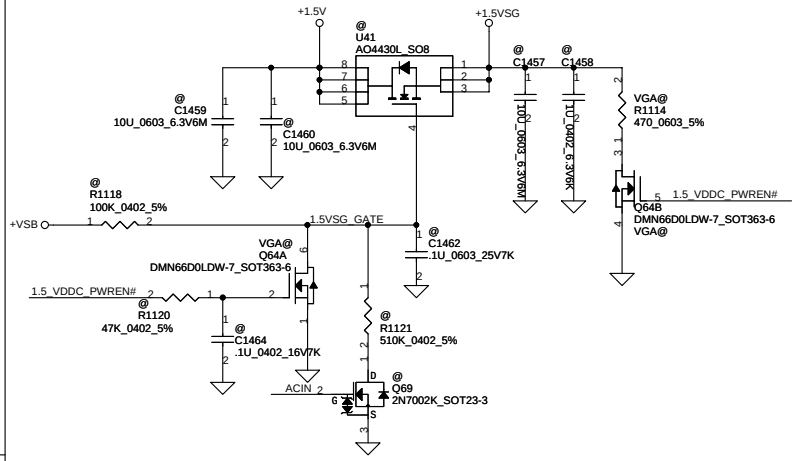
+3VALW TO +3VS (3.3A)

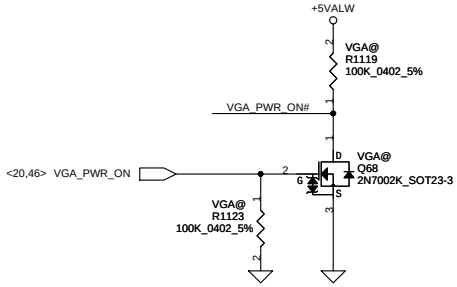


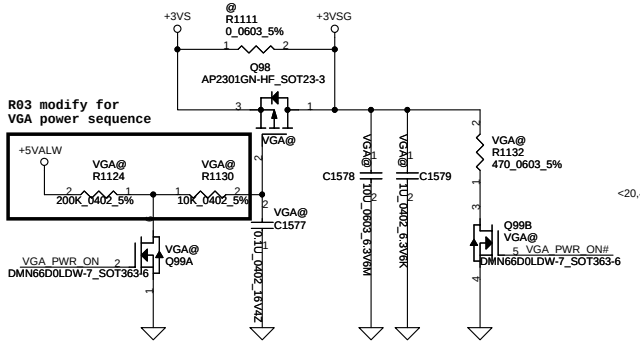
+1.5V TO +1.5VS (1.5A)

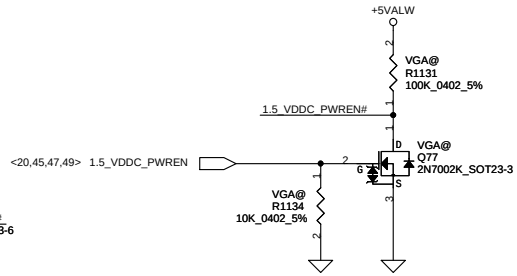


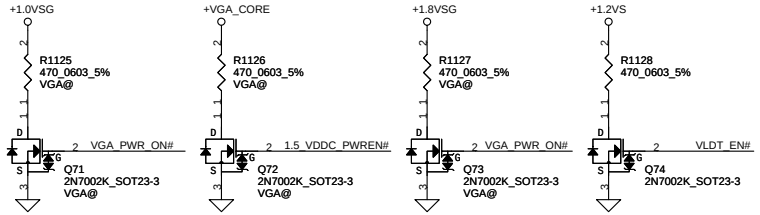
VGA Power *+1.5V to +1.5VSG (1.5A)*

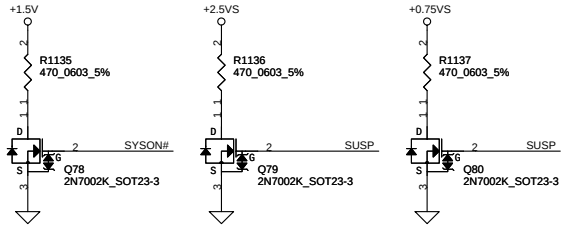












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Part Number = SP02000VQ00
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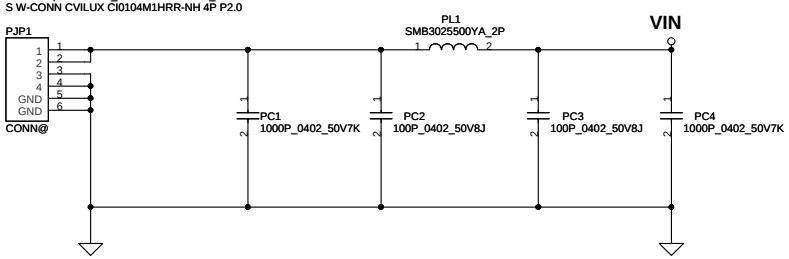
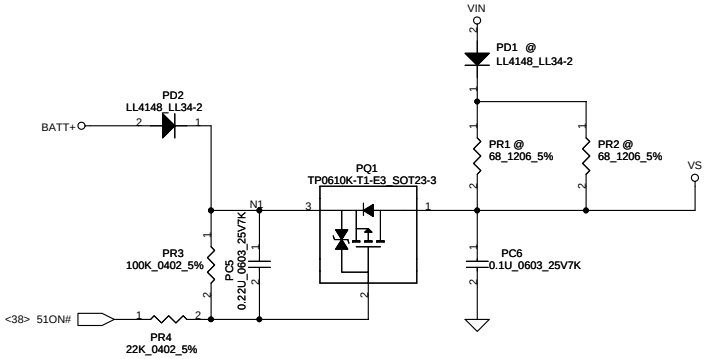
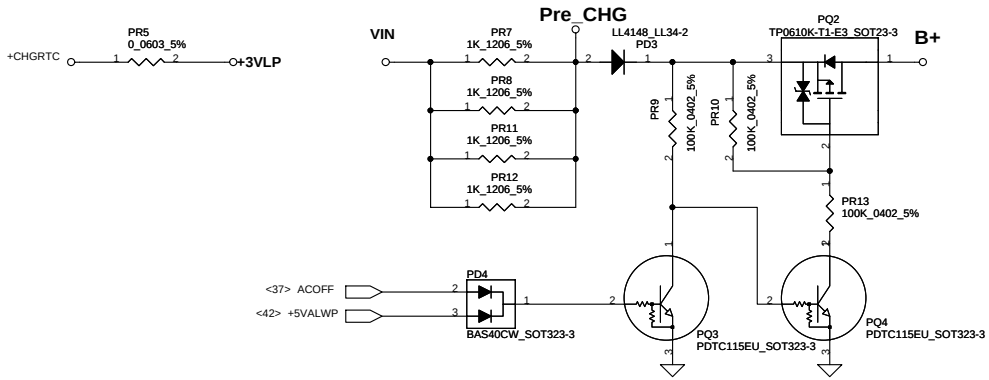
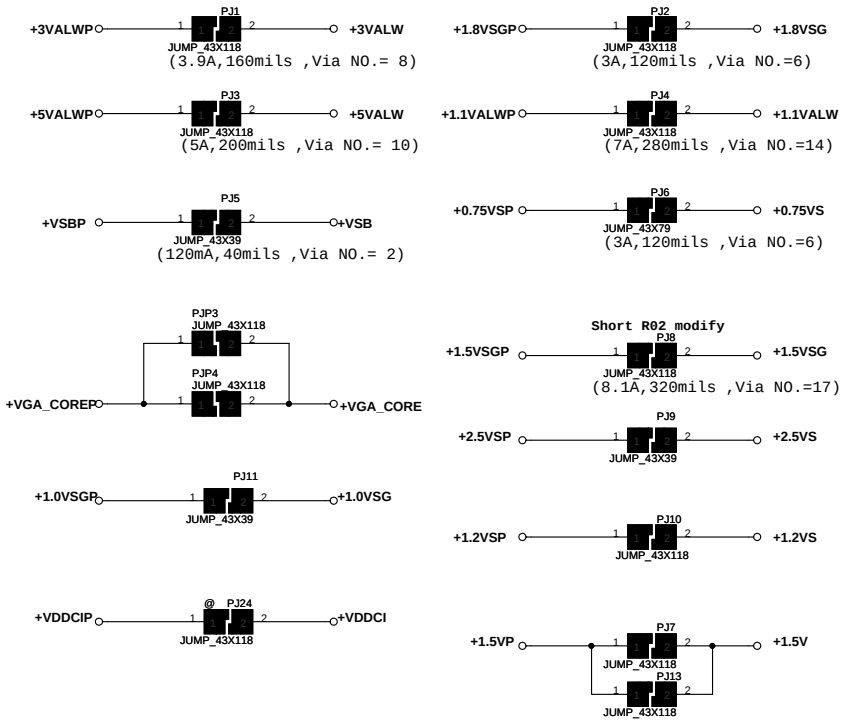
S W-CONN CVILUX CI0104M1HRR-NH 4P P2.0









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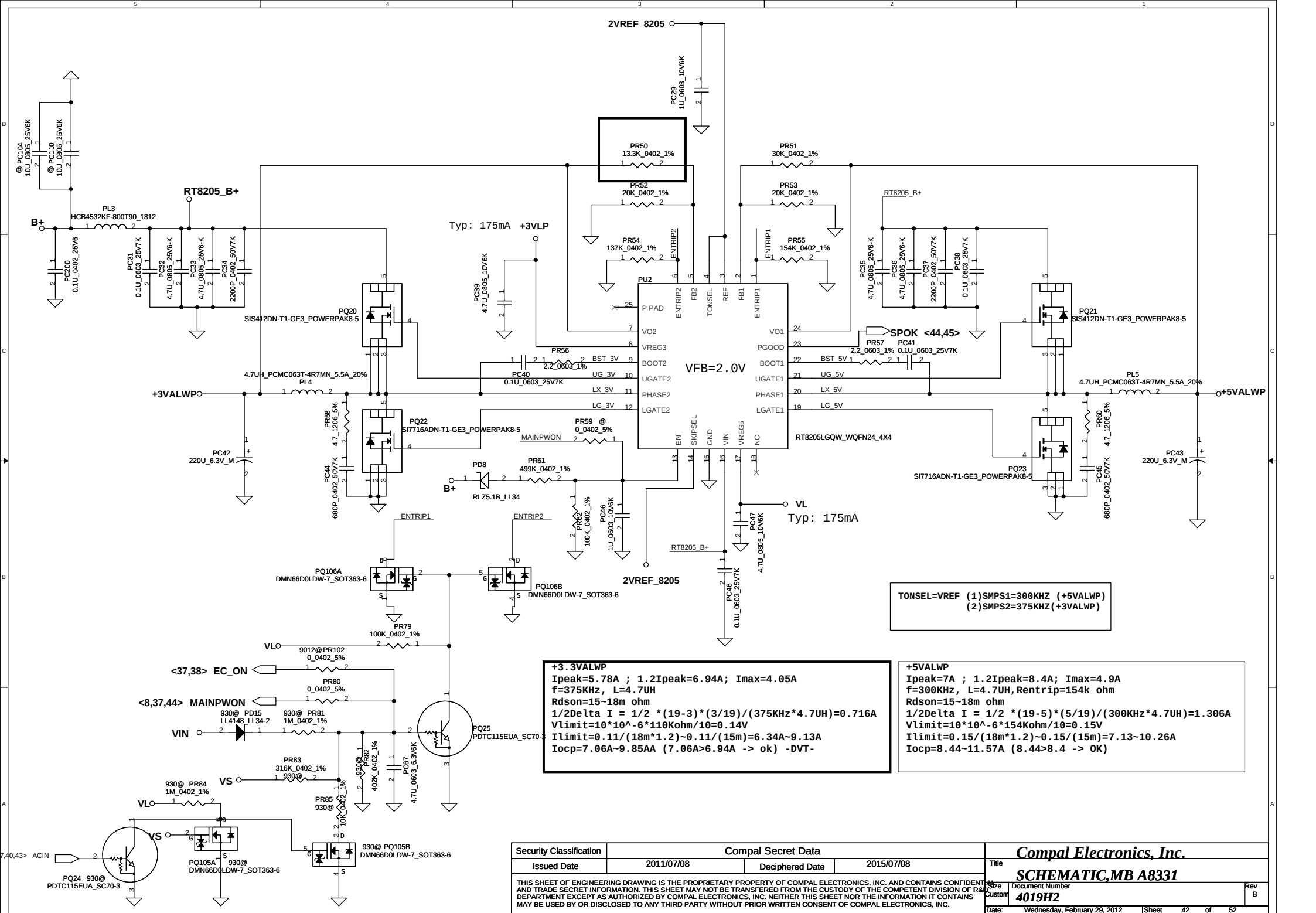

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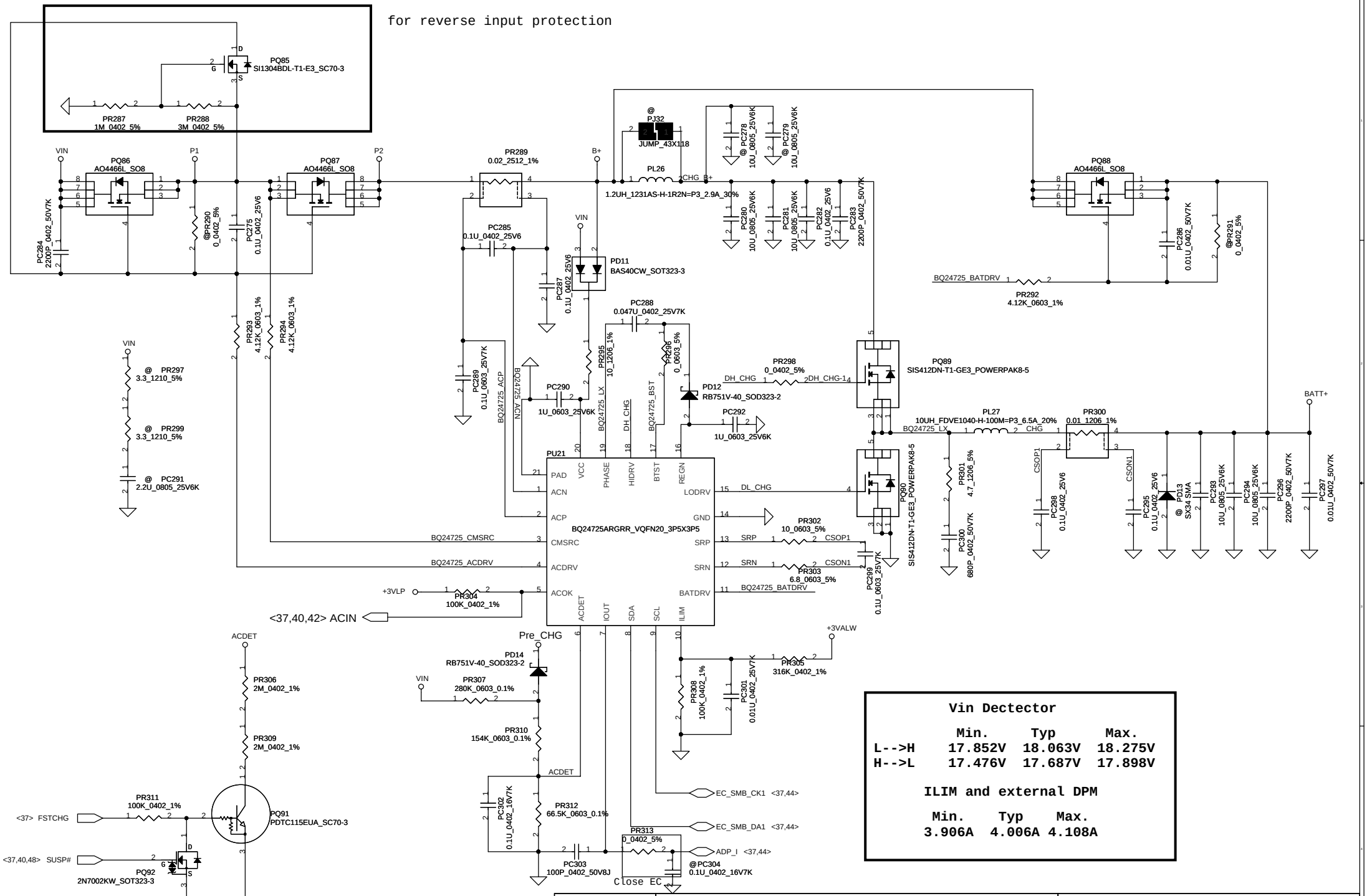

Vin Dectector

	Min.	Typ	Max.
L-->H	17.852V	18.063V	18.275V
H-->L	17.476V	17.687V	17.898V

ILIM and external DPM

Min.	Typ	Max.
3.906A	4.006A	4.108A

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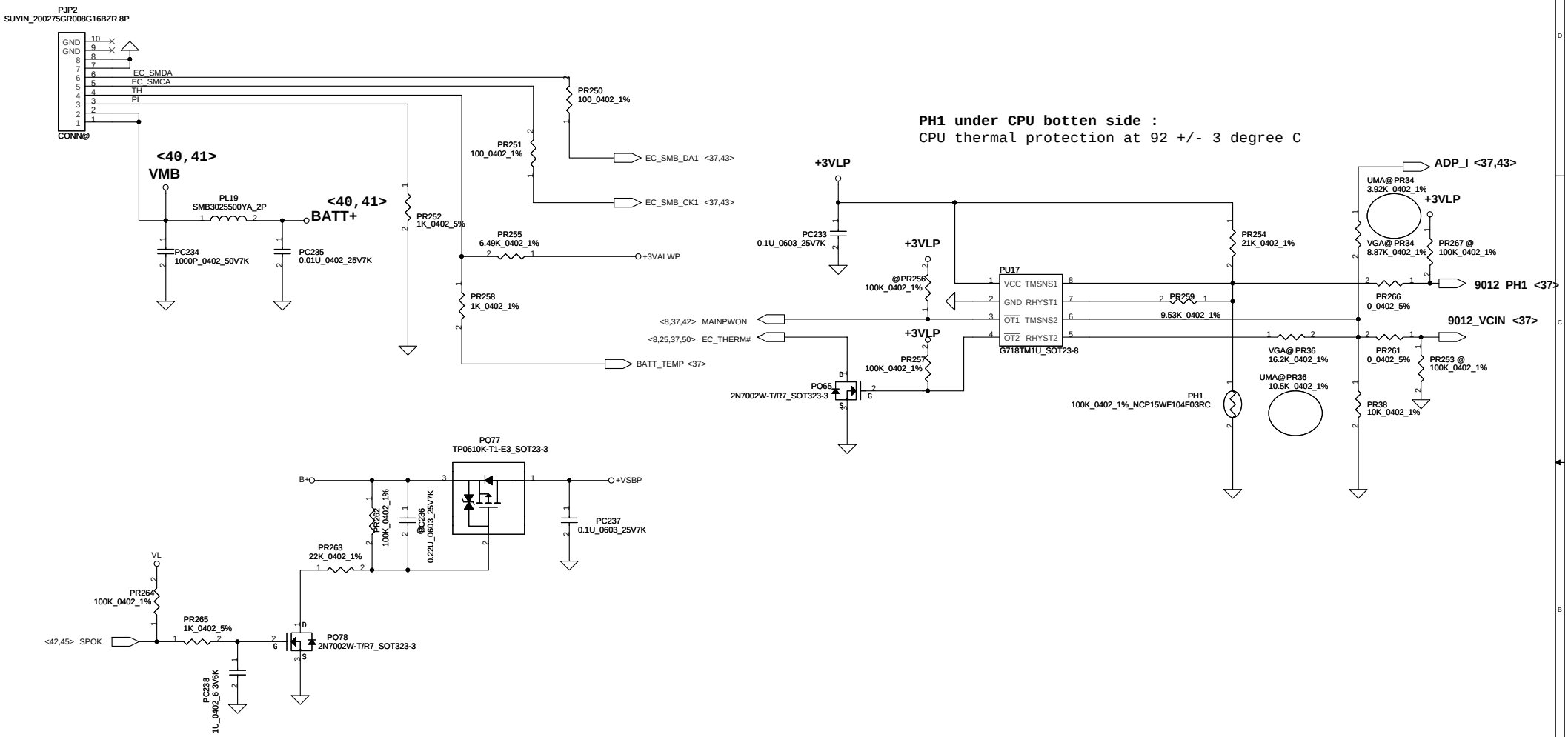

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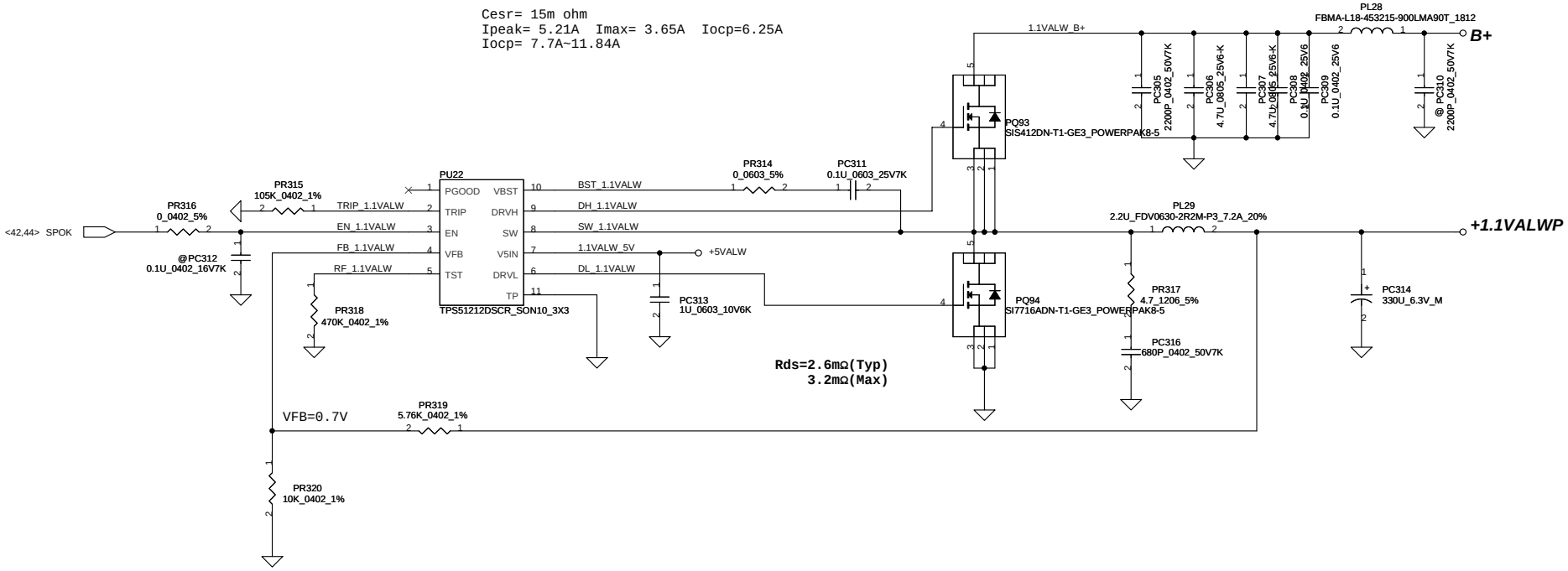
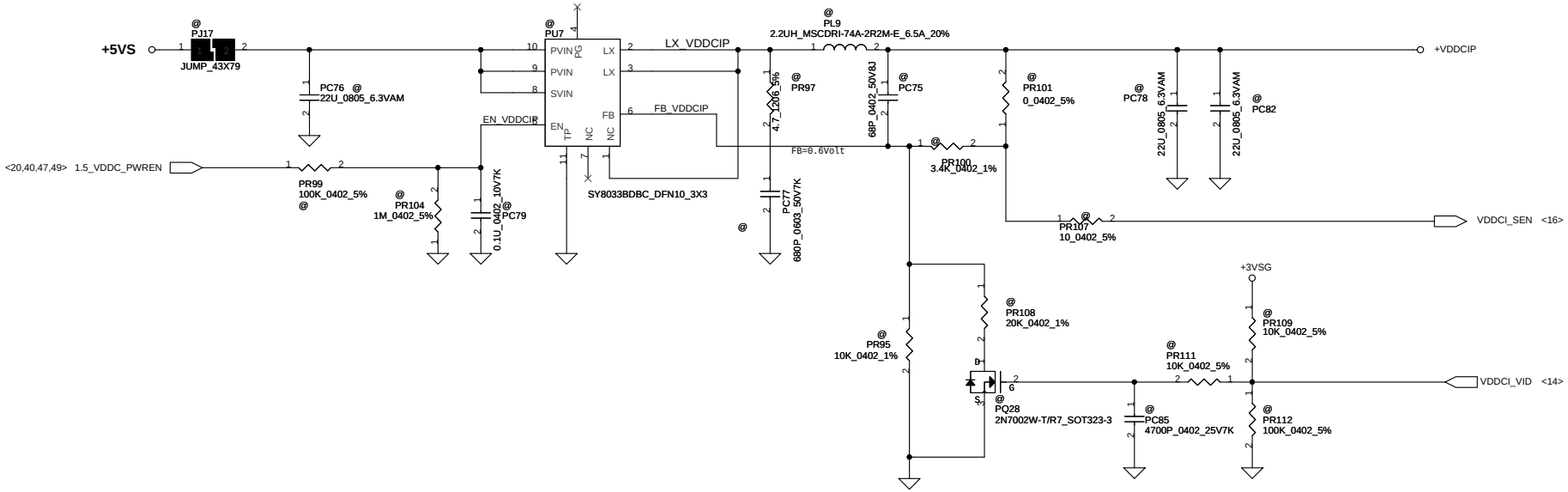
VFB= 0.7V
Vo=VFB*(1+5.76K/10K)= 1.1V
Freq= 266~314KHz , 290KHz(typ)

Cesr= 15m ohm
Ipeak= 5.21A Imax= 3.65A Iocp=6.25A
Iocp= 7.7A~11.84A





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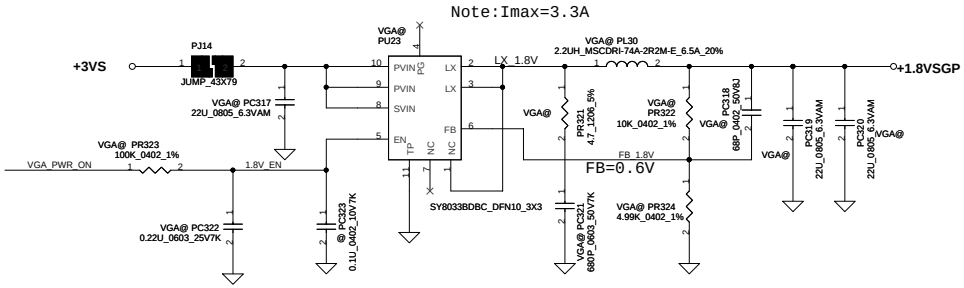

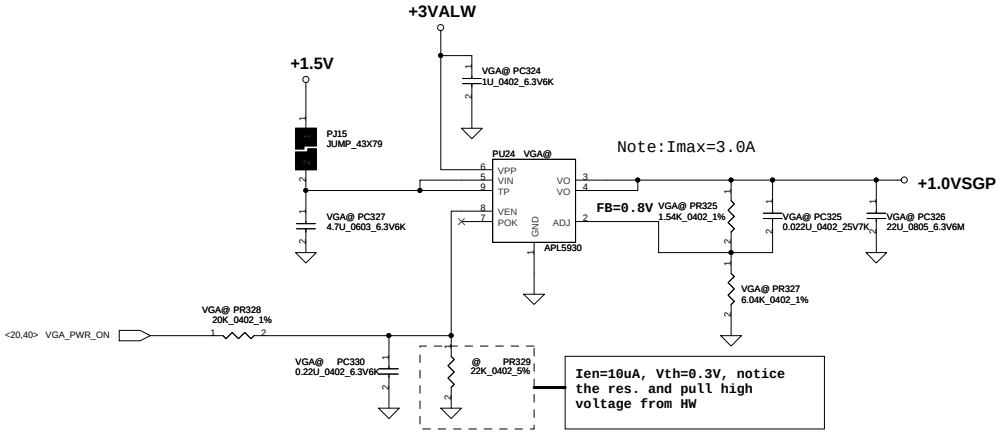

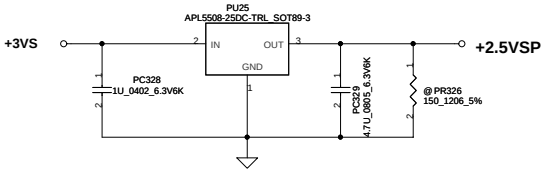

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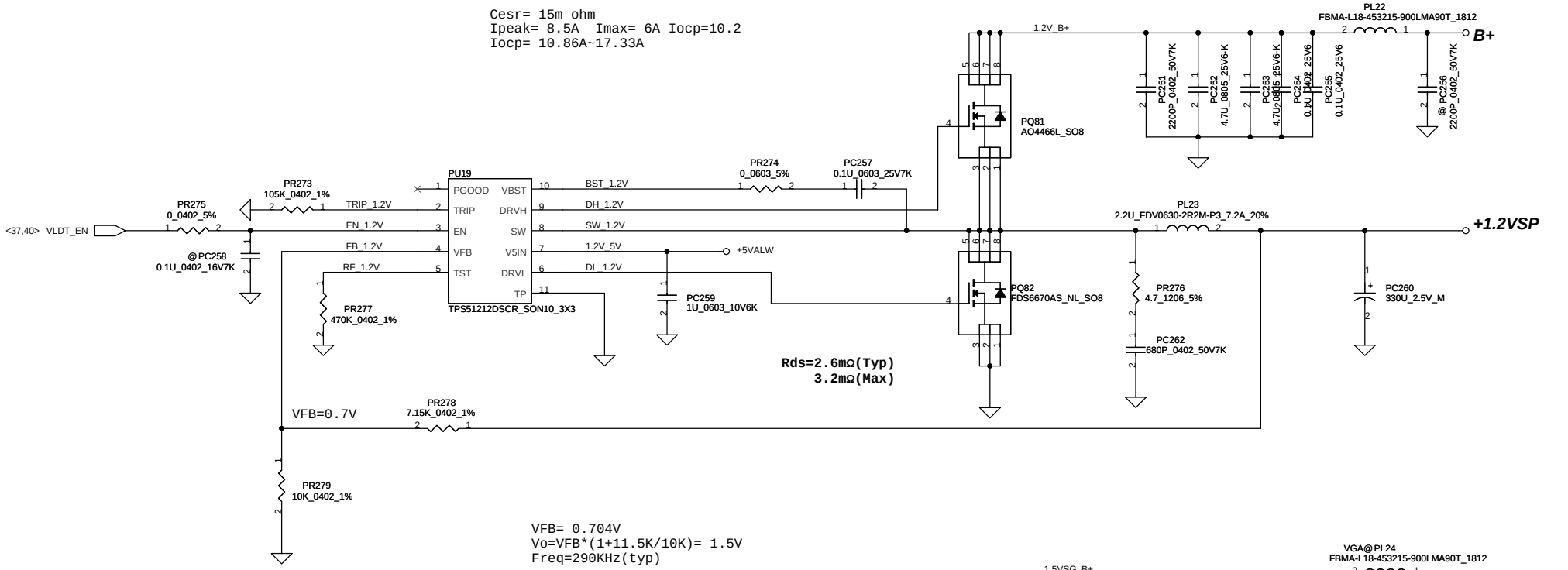
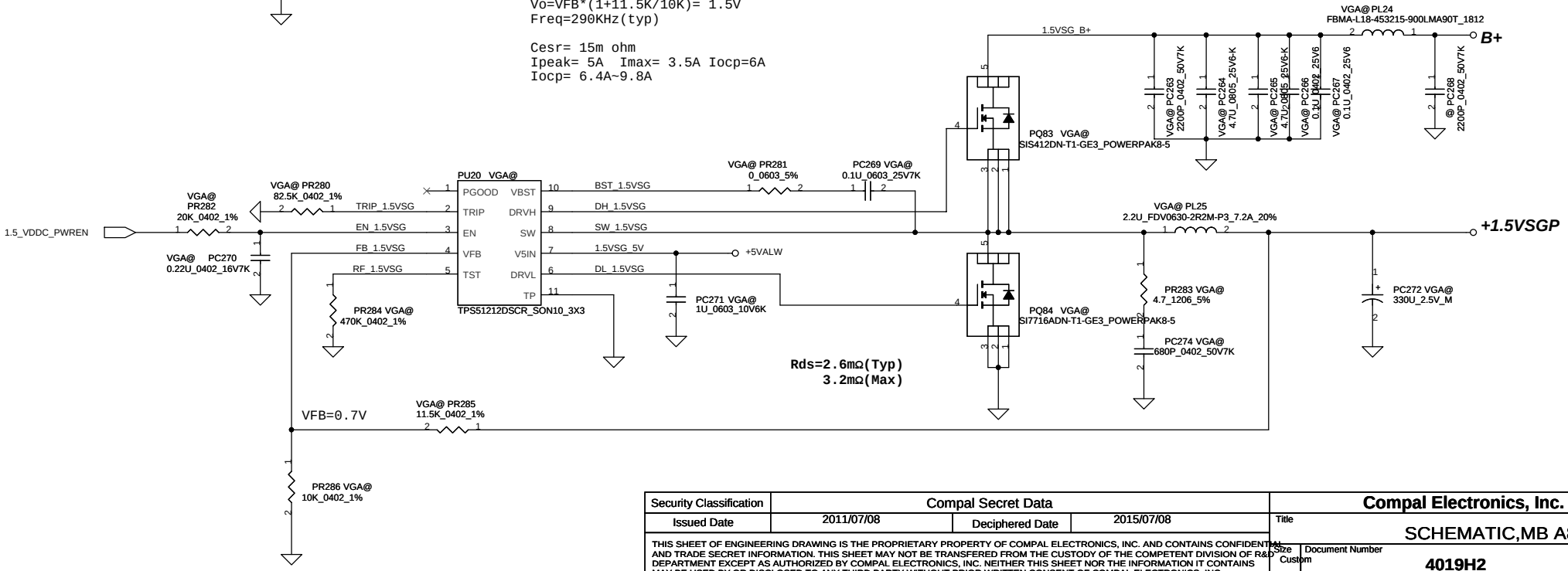
VFB= 0.7V
Vo=VFB*(1+7.15K/10K)= 1.2V
Freq= 266~314KHz , 290KHz(typ)

Cesr= 15m ohm
Ipeak= 8.5A Imax= 6A Iocp=10.2
Iocp= 10.86A~17.33A



VFB= 0.704V
Vo=VFB*(1+11.5K/10K)= 1.5V
Freq=290KHz(typ)

Cesr= 15m ohm
Ipeak= 5A Imax= 3.5A Iocp=6A
Iocp= 6.4A~9.8A



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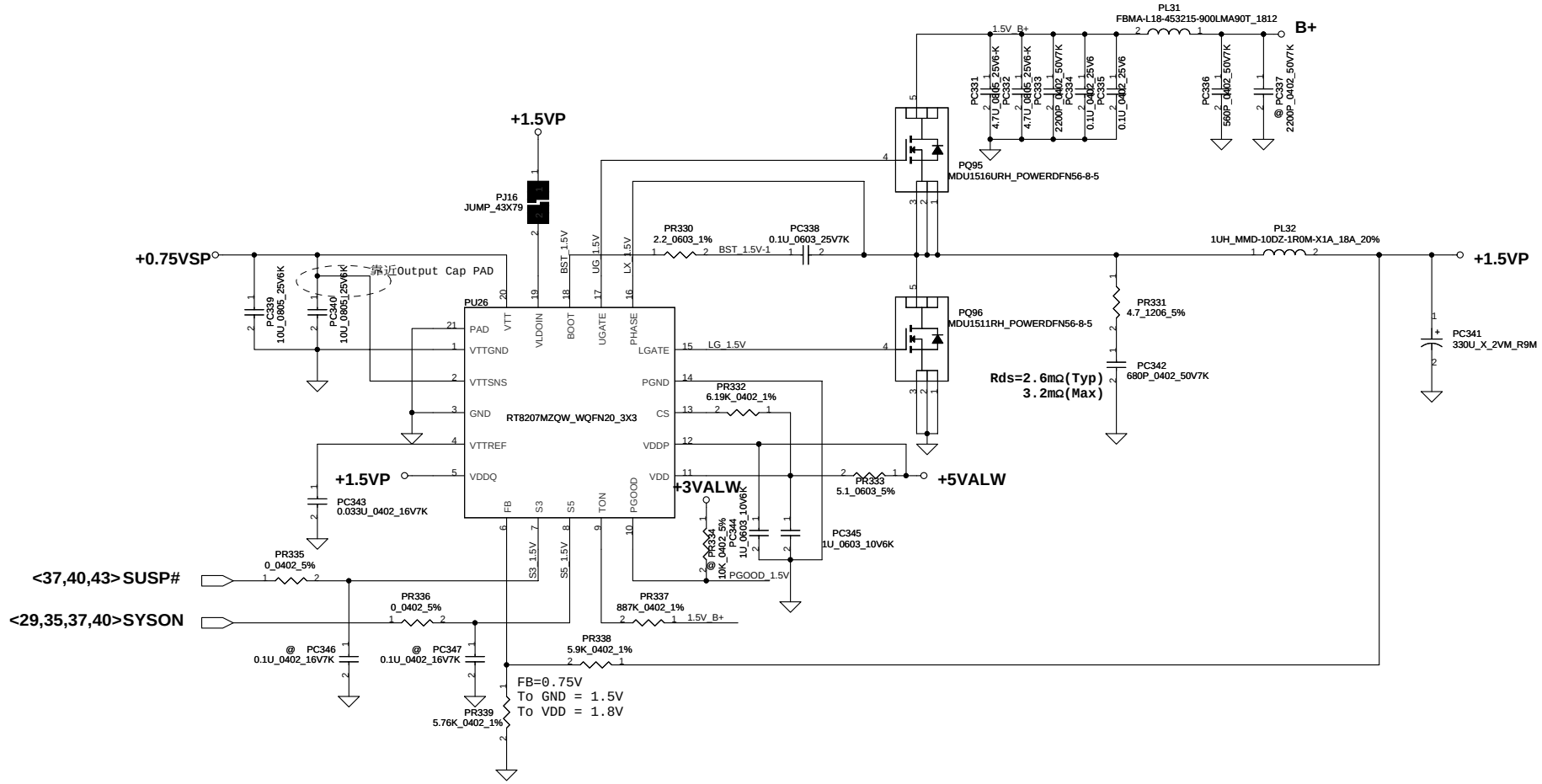

VFB= 0.75V
Ipeak= 15A Imax= 10.5A Iocp=18A
Iocp= 17.24A~25.47A

STATE	S3	S5	1.5VP	0.75VSP
S0	Hi	Hi	On	On
S3	Lo	Hi	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)
Note: S3 - sleep ; S5 - power off				

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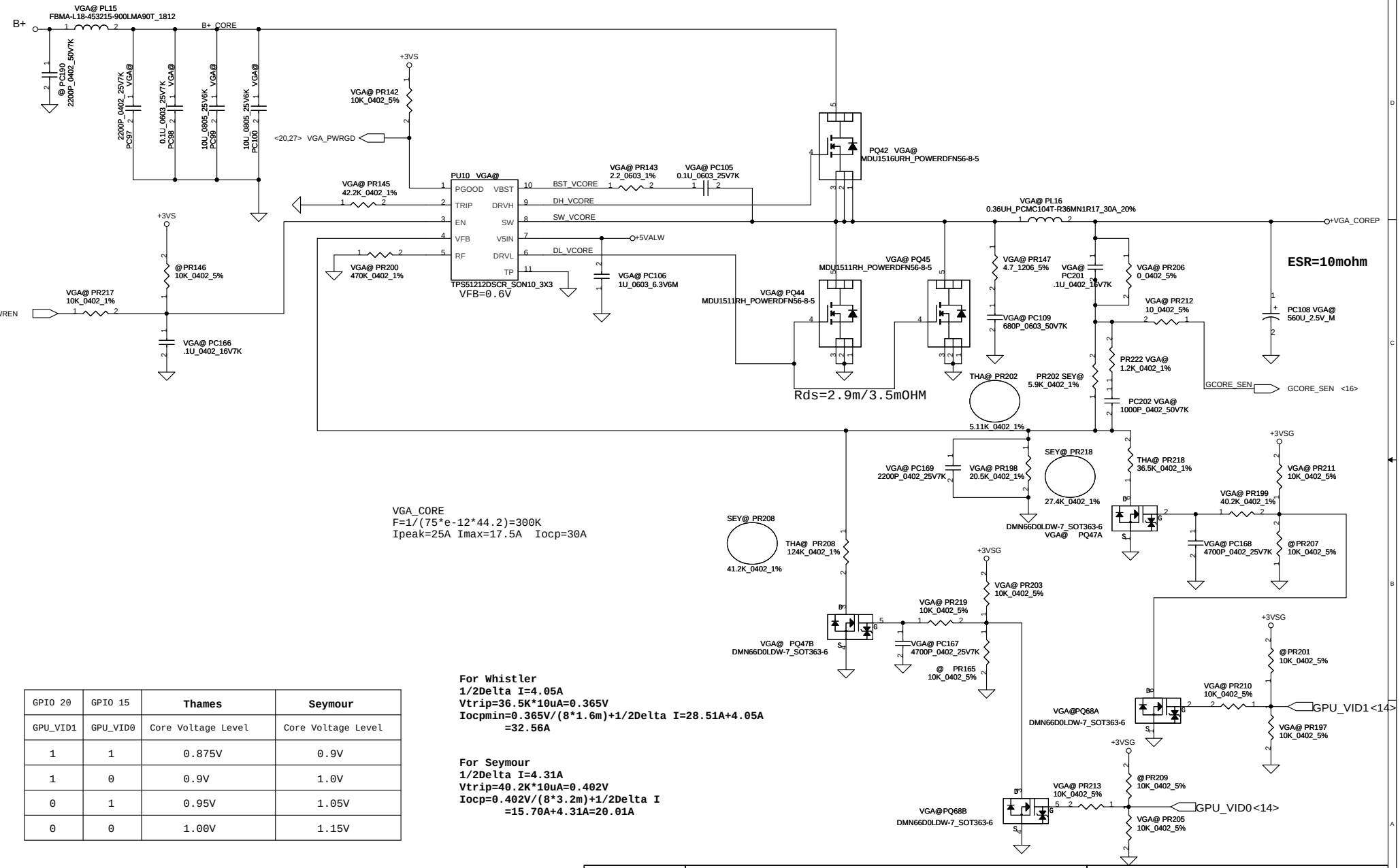

VGA_CORE
F=1/(75*e-12*44.2)=300K
Ipeak=25A Imax=17.5A Iocp=30A

GPIO 20	GPIO 15	Thames	Seymour
GPU_VID1	GPU_VID0	Core Voltage Level	Core Voltage Level
1	1	0.875V	0.9V
1	0	0.9V	1.0V
0	1	0.95V	1.05V
0	0	1.00V	1.15V

For Whistler
1/2Delta I=4.05A
Vtrip=36.5K*10uA=0.365V
Iocpmin=0.365V/(8*1.6m)+1/2Delta I=28.51A+4.05A
=32.56A

For Seymour
1/2Delta I=4.31A
Vtrip=40.2K*10uA=0.402V
Iocp=0.402V/(8*3.2m)+1/2Delta I
=15.70A+4.31A=20.01A

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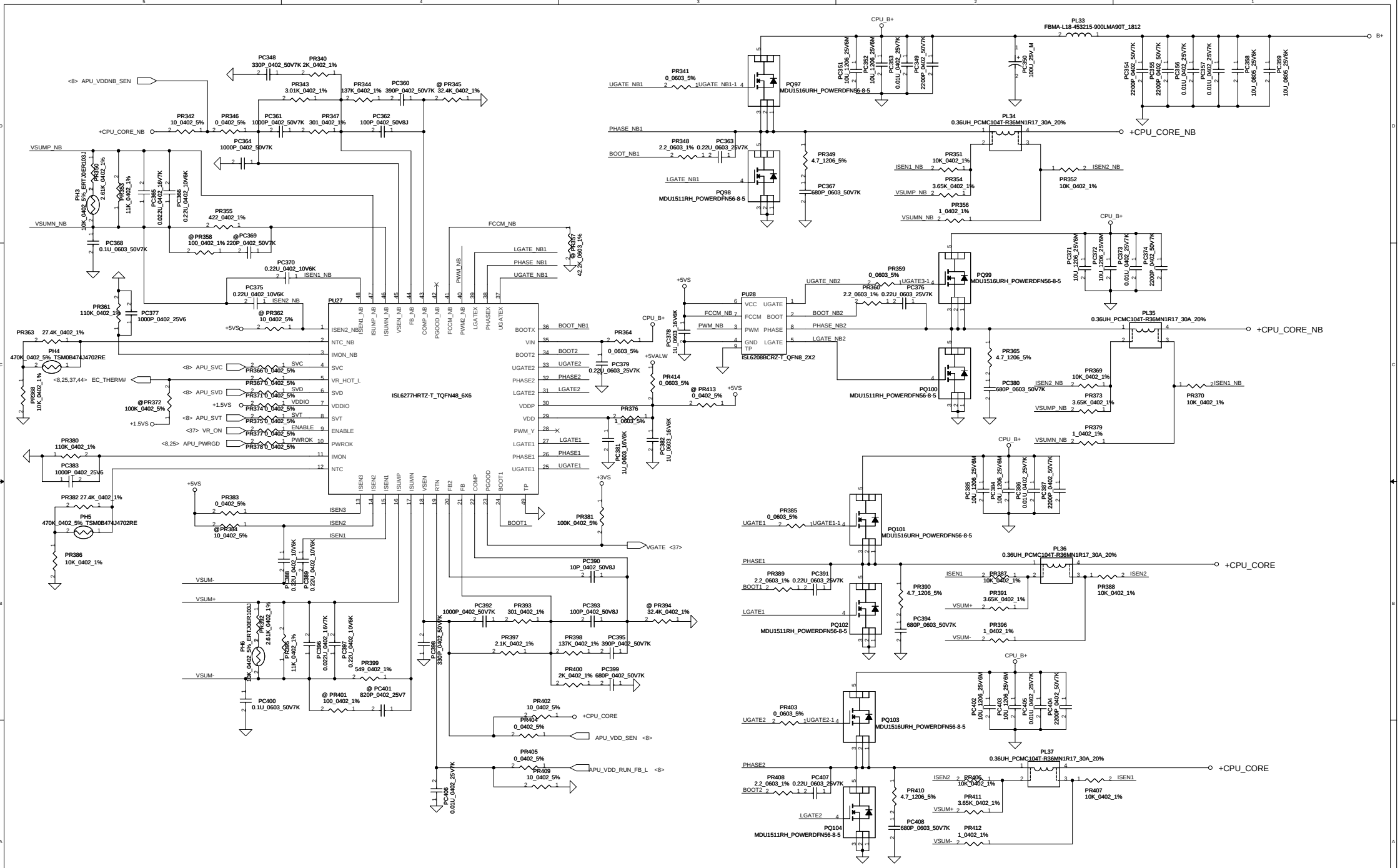

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							

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Version change list (P.I.R. List)

EVT Stage (0.1~0.2)

0817 Pop C1025 180p for VDDIO (SCL v1.02)
Change D16,D17 to SCS00000Z00

0818 Change Q50 from BSH138 to BSH111
Unpop R1100 for +1.1VALW
Add D26 BOM Structure for 930@
unpop D4 for USB issue

0903 1.Change Card Reader Controller to RTS5209
2.Change LAN to Atheros AR8151
3.Removed D17

0904 Add Mini2 Debug Port

0905 1.Add Fresco FL1009 USB3.0 Controller
P20. BACO BIFVDDC update
P25. remove Q25 APU power ok

0915 1.Remove EC X2

0916 1.Add C1361/C1362 10pF for EMI
2.Change D27/D29 footprint to AZ5125
3.Add R402 10k for reserved
4.Add R469/R527 for VGA Internal Thermal Senser

0926 1.Change D4 to SC300001G00 for ESD request
2.Change D33/D34/D37/D40/D41 to SCA00001A00 for ESD request

DVT Stage (0.2~0.3)

1.Unpop C954, C955 for Mini2 reserved.
2.Remove R587, R588, Q11 for no need level shift.
3.Pop R469, R527
Unpop U9, R391, C352, C324
for VGA Internal Thermal Interface.
4.Unpop C374 330uF for Use discrete +1.5VSG circuit.
5.Add R1169 1k for RTS2132 Vender suggestion.
6.Reserved R1177 for option EEPROM.
7.Add R1178 for RTS2132 discrete +1.2VS power.
8.Reserved SMBUS(TL_CLK/TL_DATA) to EC for EEEPROM option.
9.Reserved BACO circuit and pop C1105.
10.Change D4, D6 to AZC099 for ESD reserved.
11.Change D20, D21 to AZC199-02SPR7G for ESD reserved.
12.Remove D44, D45 for no need.
13.Change C1211, R837 BOM to TL@.
14.Change JTP1 to 6P/8P co-lay footprint for WIN8.
15.Add SMBUS(FCH_SCLK1/FCH_SDATA1) for JTP1.
16.Reserved GPIO166 for future used.
17.Add H29 for ME update.
18.Add C1719, C1720 10pF for RTD5209 EMI request.
19.Change L1801 footprint.
20.Pop D42 and change to SCA00001A00 for ESD.
21.Change C1537 to 10pF 2KV for EMI/ESD.
22.Unpop C1336, C1337, C1338, C1333, C1334, C1335
for MINI2 Reserved.
23.Modify C1911 always pop for noise reduce.
24.Modify R60 to M3@.
25.Change Board ID to "02" for DVT.
26.Add Q30 for EC_THERM reverse for EC common code.
27.Change 9012_PH2 netname to 9012_VCIN for VC function.
28.Unpop R65 for External OTP.
29.Change L68 +5VS to +VDDA.
30.Chnage R1124 to 200k, R1130 to 10k for VGA Power Sequence.
31.Pop R997 for W/L BT combo card BT ON/OFF
32.Change U28 SPI ROM from MXIC to EON

PVT Stage

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