

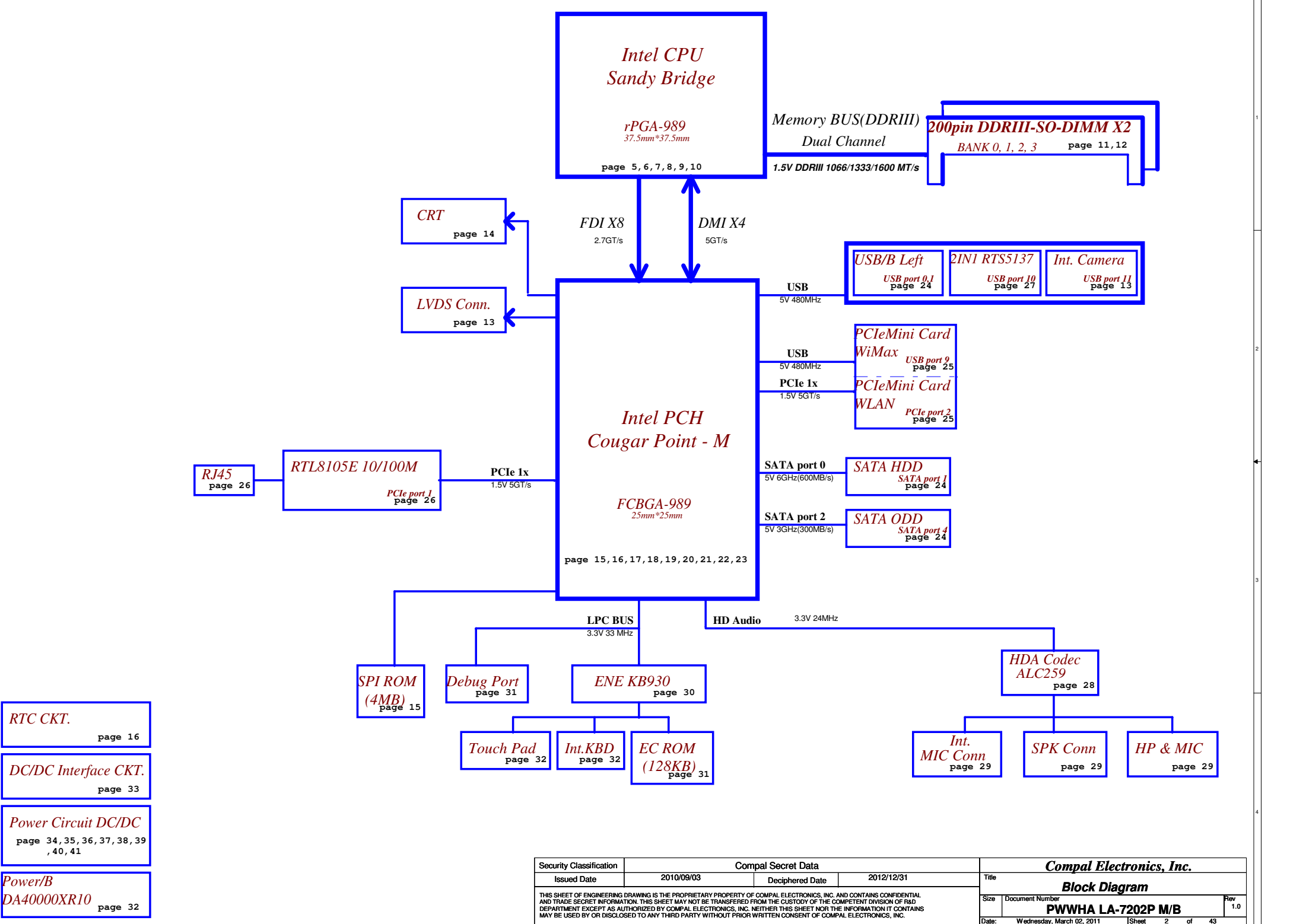
PWWHA

Delhi 10R

LA-7202P REV 1.0 Schematic

Intel Processor (Sandy Bridge) / PCH (Cougar Point)
2011-02-08 Rev 1.0

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				Size B	Document Number PWWHA LA-7202P M/B
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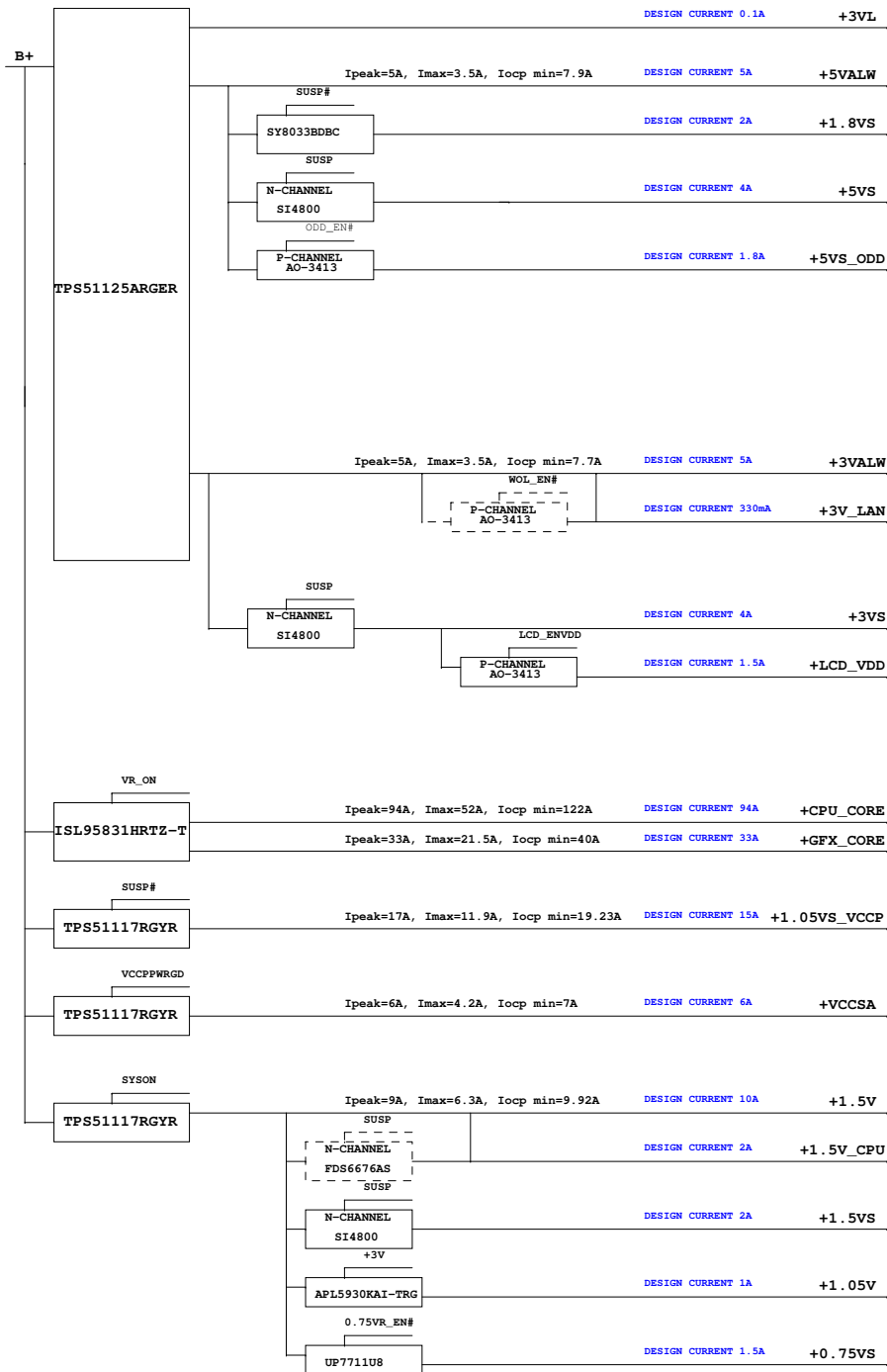
RTC CKT.
page 16

DC/DC Interface CKT.
page 33

Power Circuit DC/DC
page 34, 35, 36, 37, 38, 39, 40, 41

Power/B
DA40000XR10
page 32

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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +GFX_CORE
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	WLAN/WIMAX		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

EC SM Bus2 Address

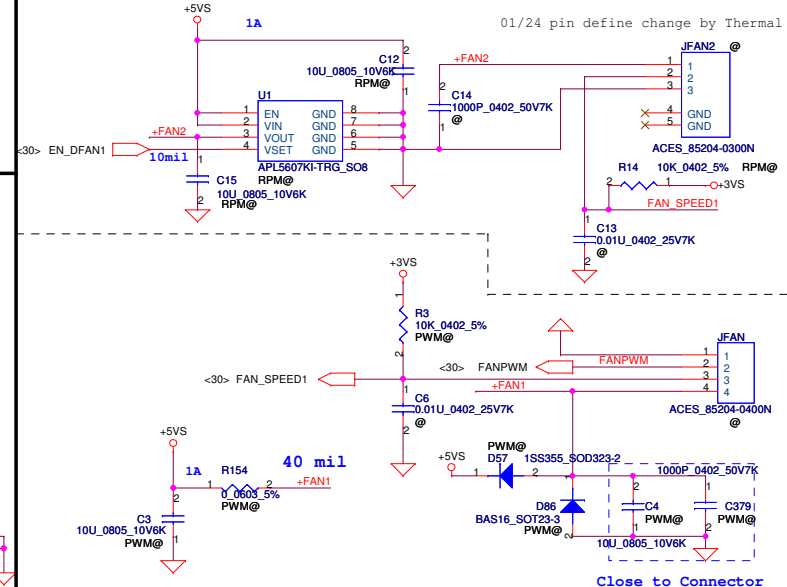
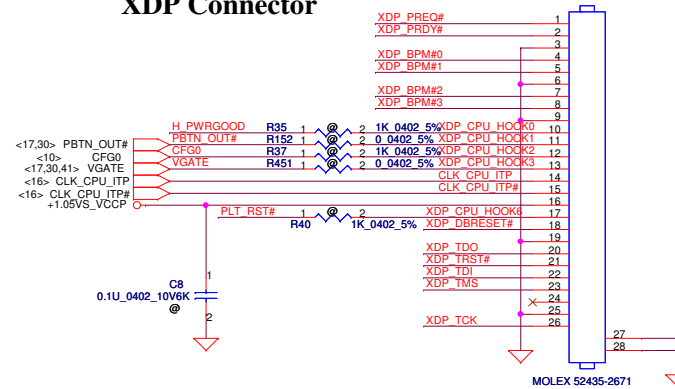
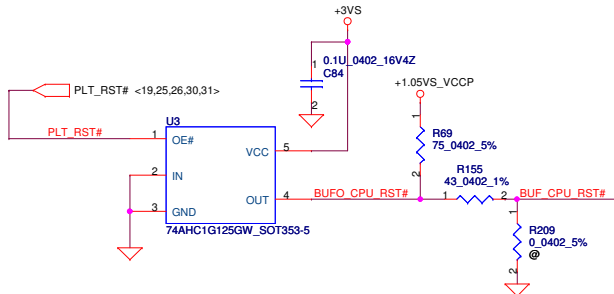
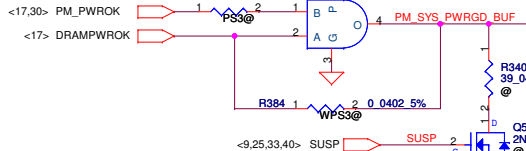
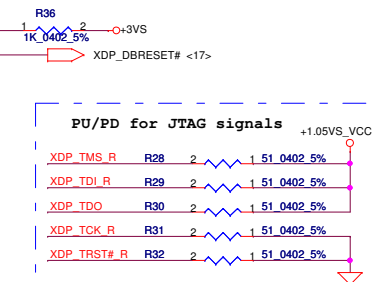
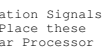
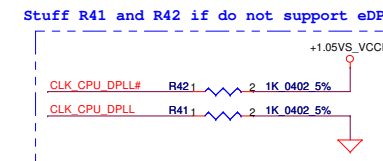
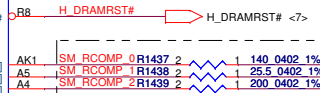
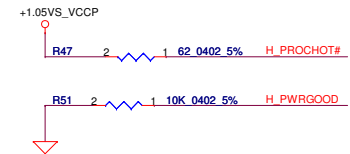
Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b

BTO Option Table

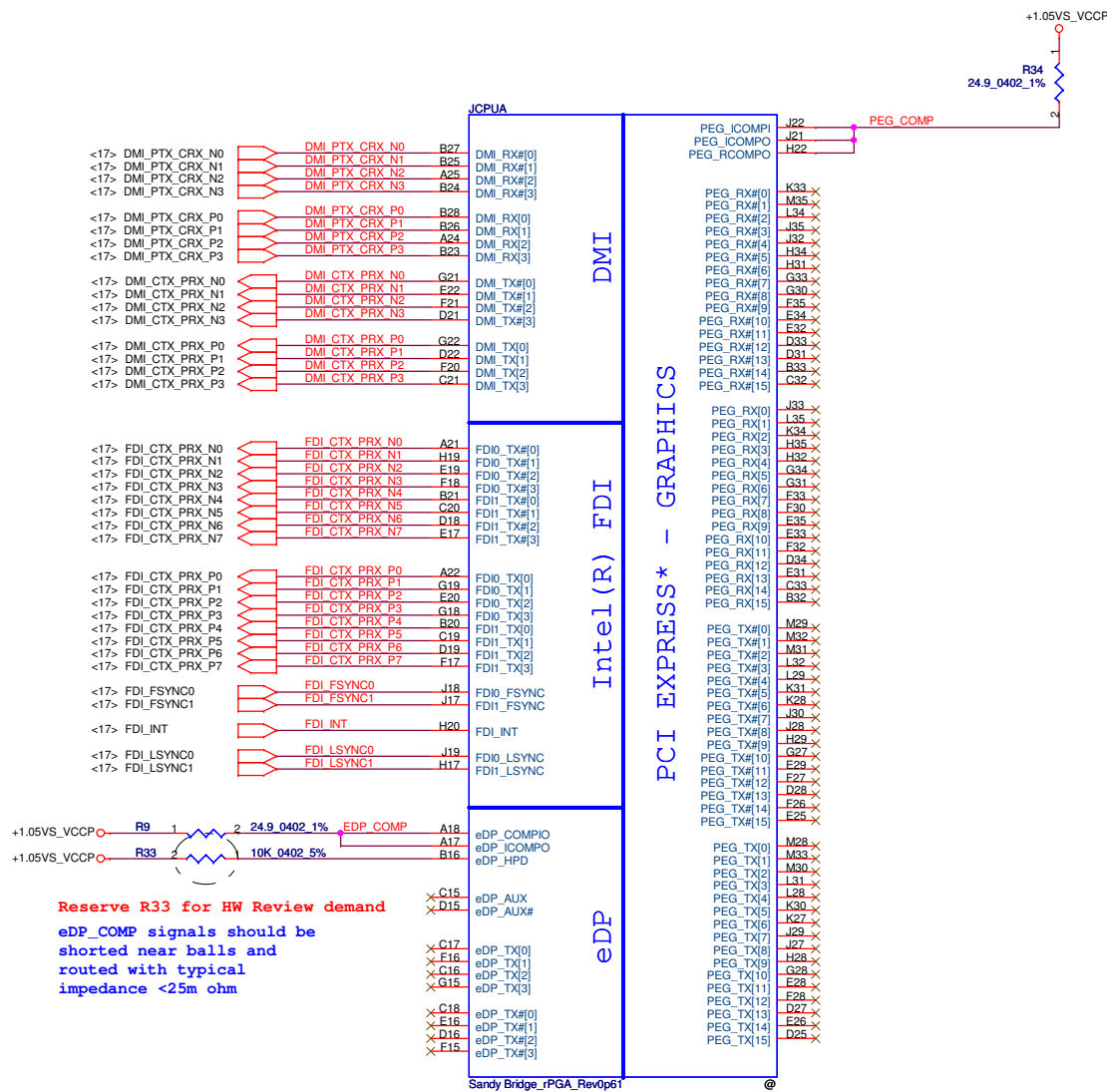
Function	MINI PCI-E SLOT	LAN		Camera & Mic	FAN		S3 Power Saving		Load Power Switch	
description	SLOT1	LAN		Camera & Mic	FAN		S3 Power Saving		Load Power Switch	
explain	WIMAX	10/100M	Giga	Camera & Mic	PWM	RPM	1.5V	1.5VS	Old Sch.	New Sch.
BTO	WIMAX@	8105E@	8111E@	CAM@	PWM@	RPM@	WPS3@	PS3@	OLS@	NLS@

STATE SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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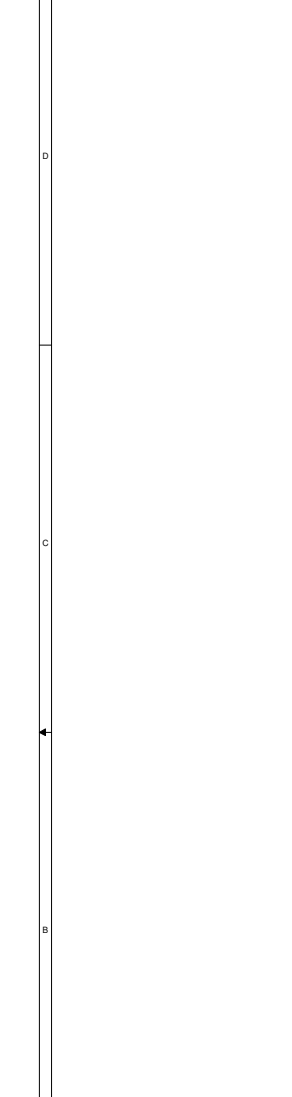
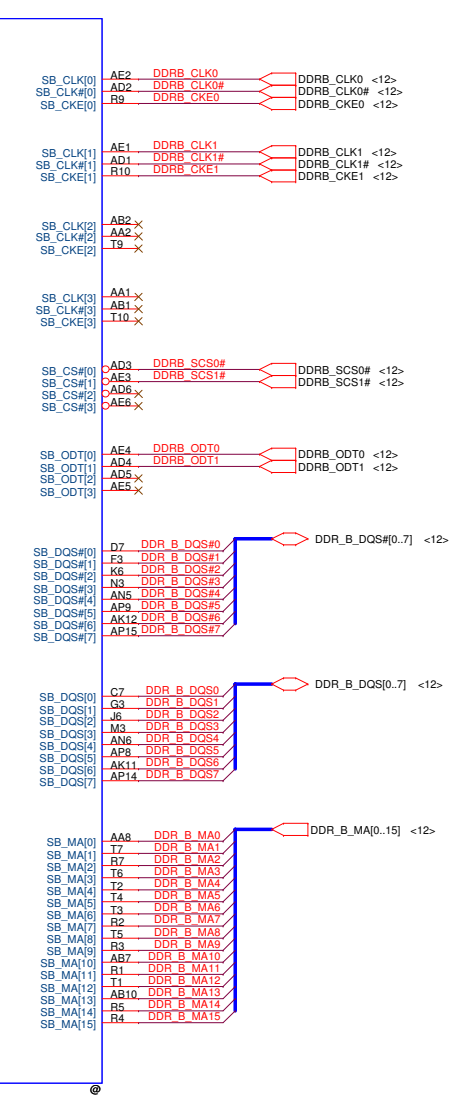
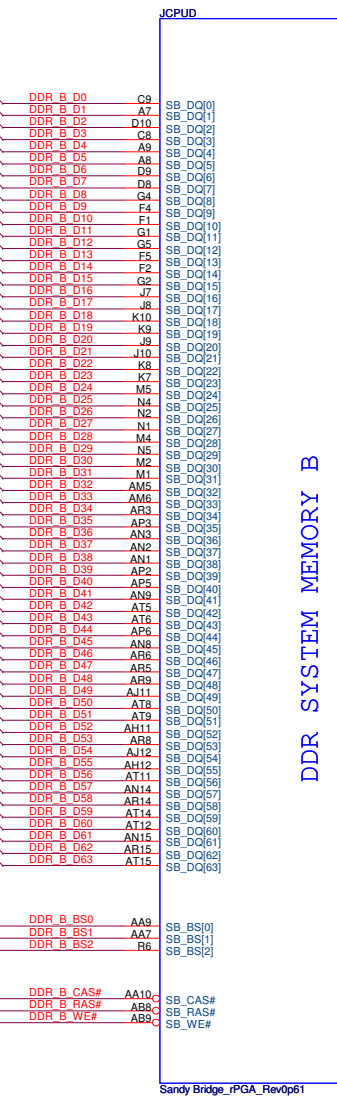
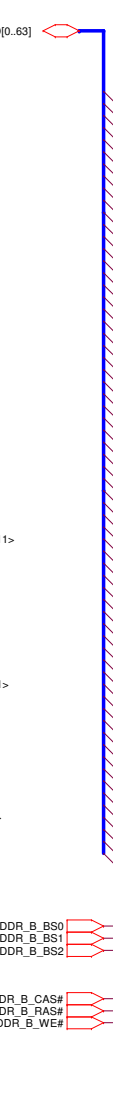
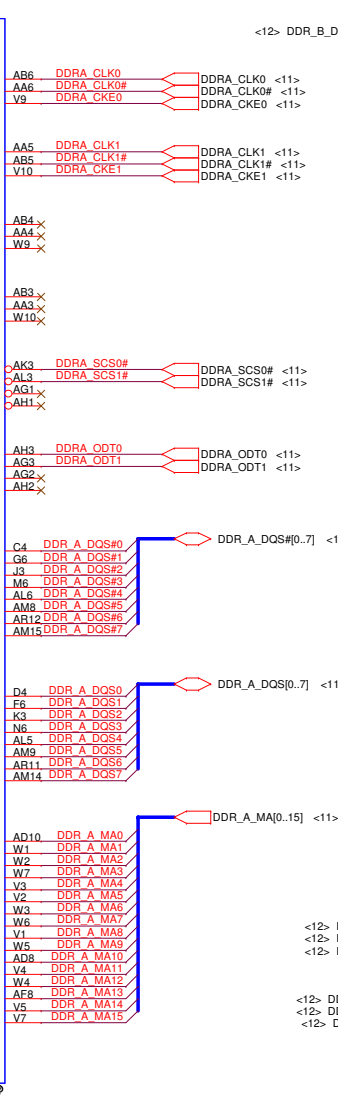
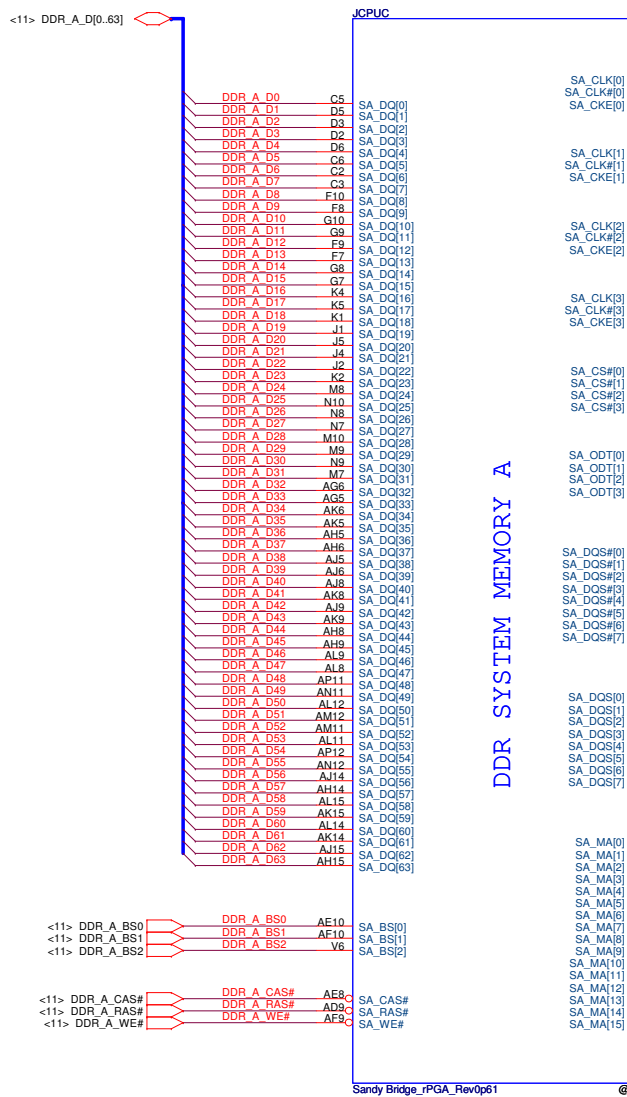
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PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)

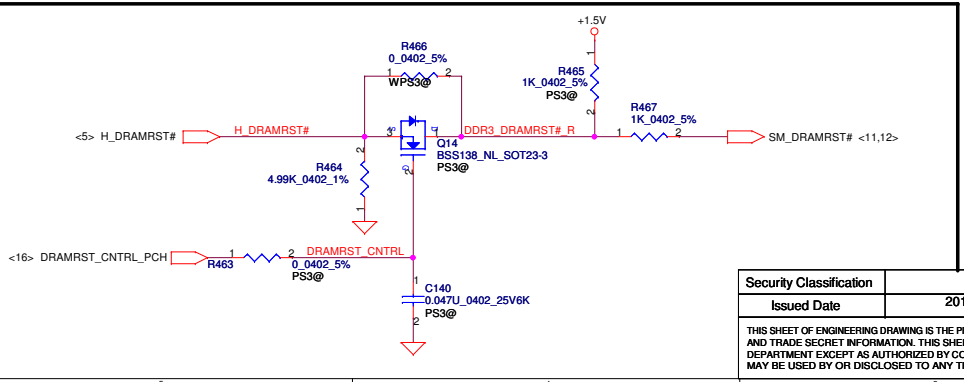
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)

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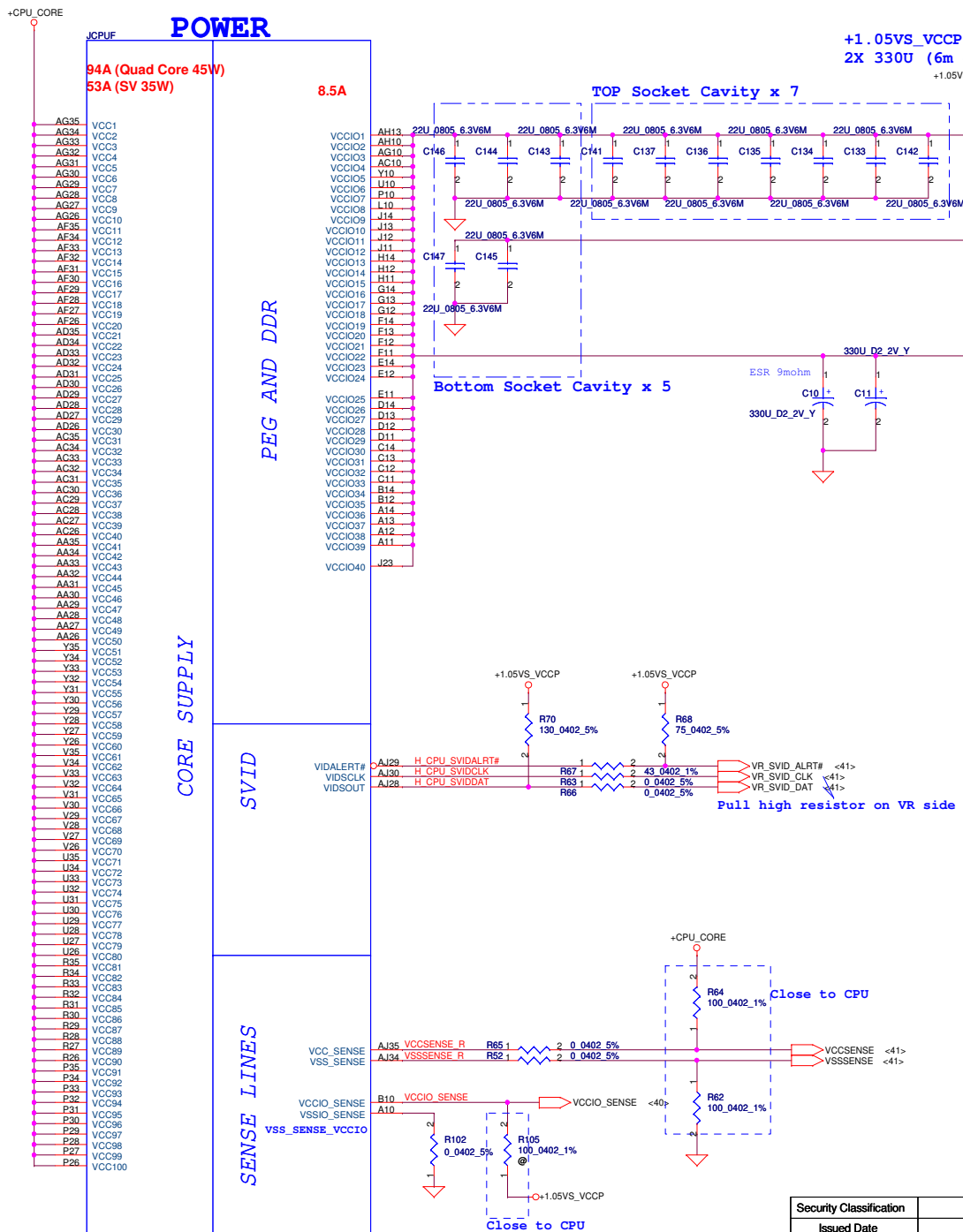


DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

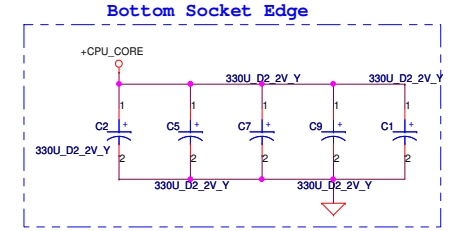
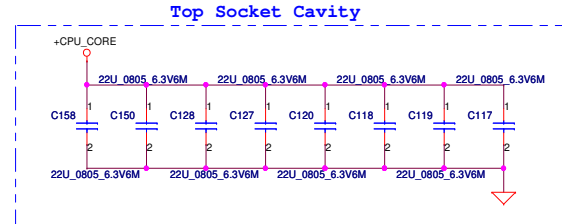
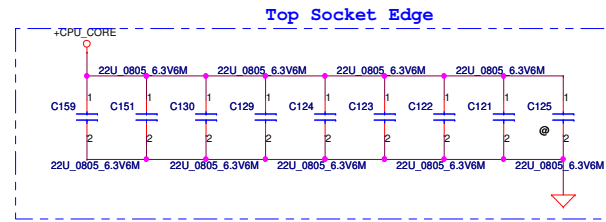
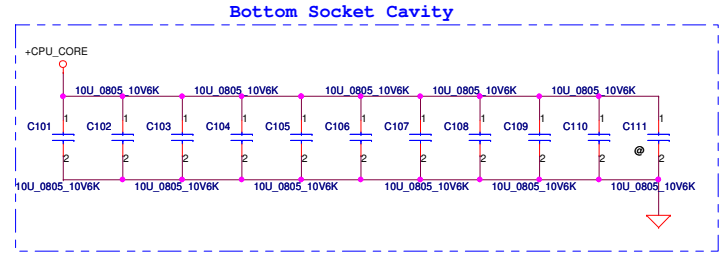


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+1.05VS_VCCP Decoupling:
2X 330U (6m ohm), 12X 22U

+CPU_CORE Decoupling:
4X 470U (4m ohm), 16X 22U, 10X 10U



Pull high resistor on VR side

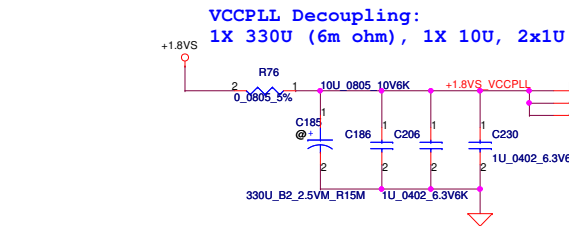
Close to CPU

Close to CPU

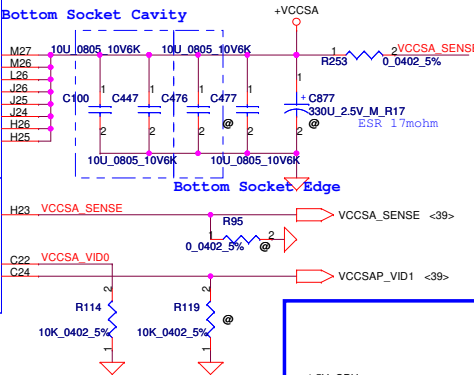
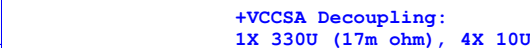
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				2012/12/31				Size Document Number			
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+GFX_CORE
Change C873 from 330uF to 560uF for power issue



.8V RAIL		GRAPHICS	
MISC	SA RAIL	DDR3 -1.5V RAILS	VREF
VCCSA_SENSE VCCSA_YID0 FC_C22 VCCSA_VID1	6A VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8	5A VDDQ01 VDDQ02 VDDQ03 VDDQ04 VDDQ05 VDDQ06 VDDQ07 VDDQ08 VDDQ09 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15	SENSE LINES VAXG_SENSE VSSAXG_SENSE SM_VREF



VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.75 V
1	1	0.65 V

IF MPS30, short PJ30.

1.5V_CPU

PS30

C213 1 2 0.1U 0402 16V4Z

C212 1 2 0.1U 0402 16V4Z

C211 1 2 0.1U 0402 16V4Z

C210 1 2 0.1U 0402 16V4Z

1.5V

Vgs=10V, Id=14.5A, Rds=6mohm

470_0805_5%

R449

C179 10U_0805_10V4K

FDS6676AS_S08

Q46B

2N7002DW-T/R7_SOT363-6

SUSP

Q46A

2N7002DW-T/R7_SOT363-6

420K_0402_5%

R420

820K_0402_5%

R455

220K_0402_5%

VSB

1.5V

JUMP_43X118

C33

1 S @ 8

2 S @ 7

3 S @ 6

4 G @ 5

D

D

D

D

D

D

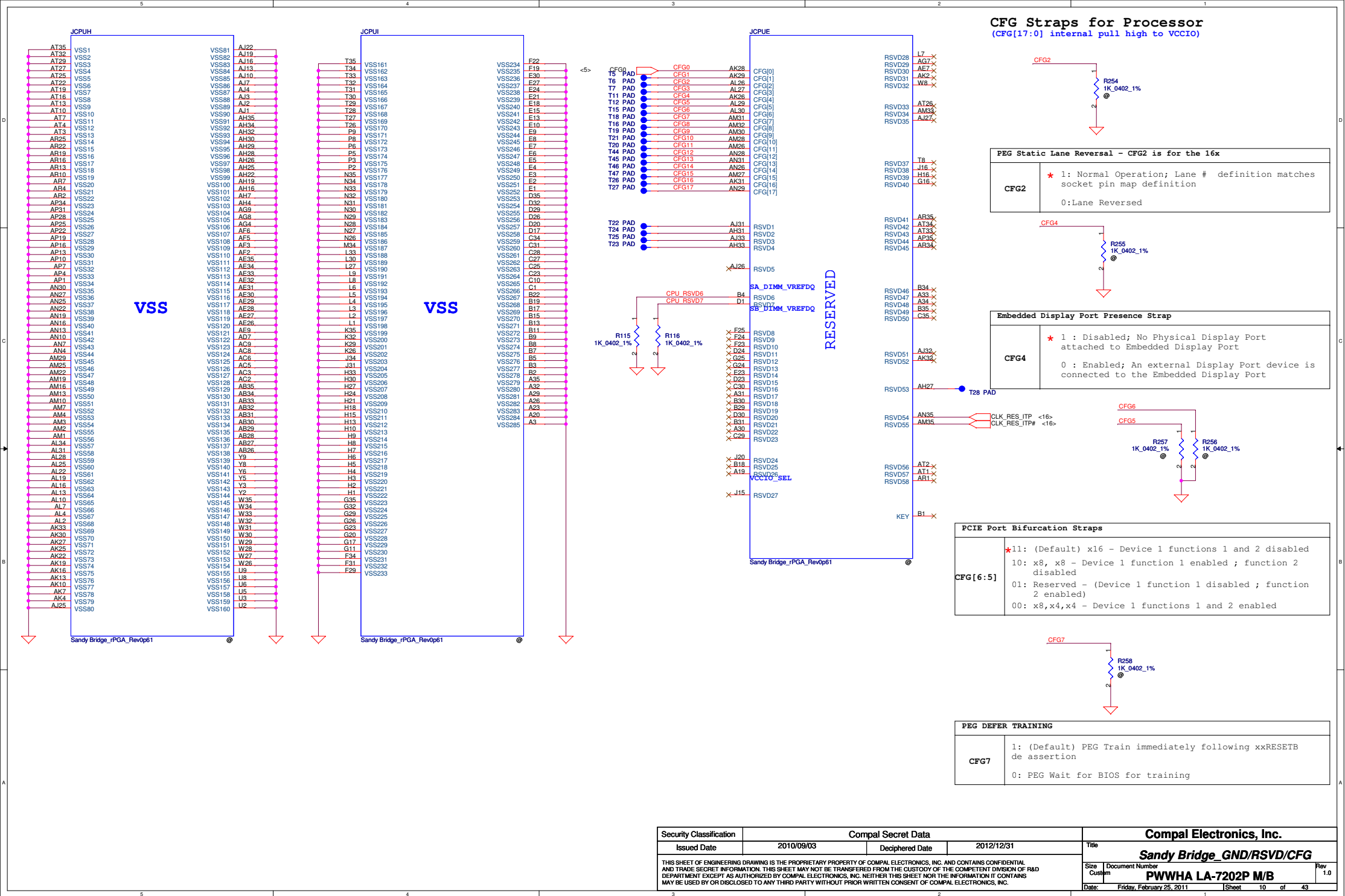
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RUN_ON_CPU1.5VS3

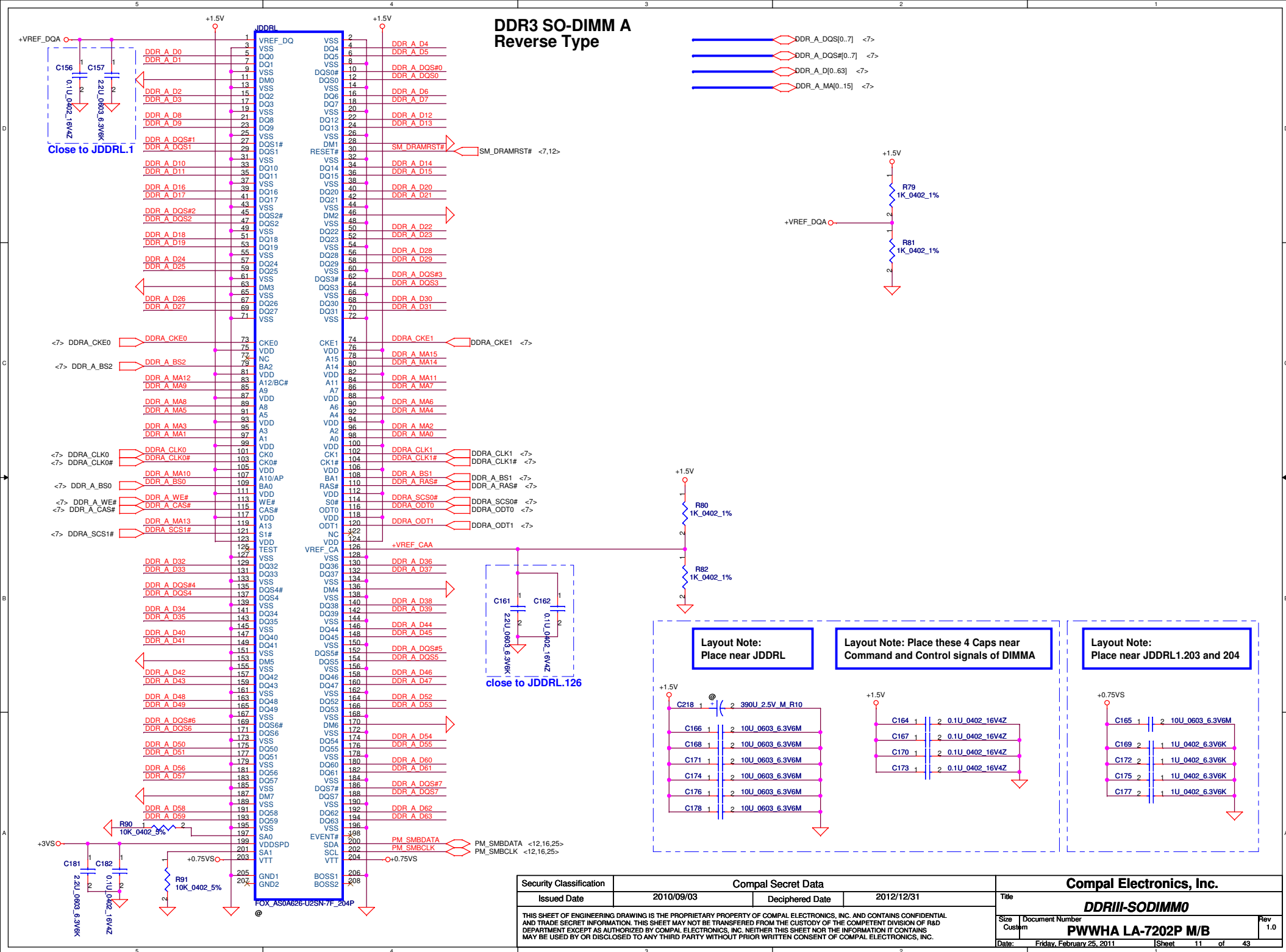
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<5.25,33>

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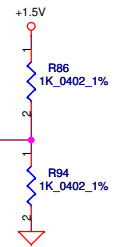
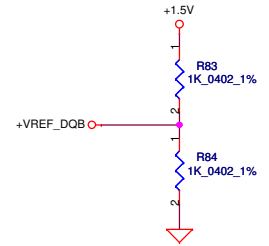
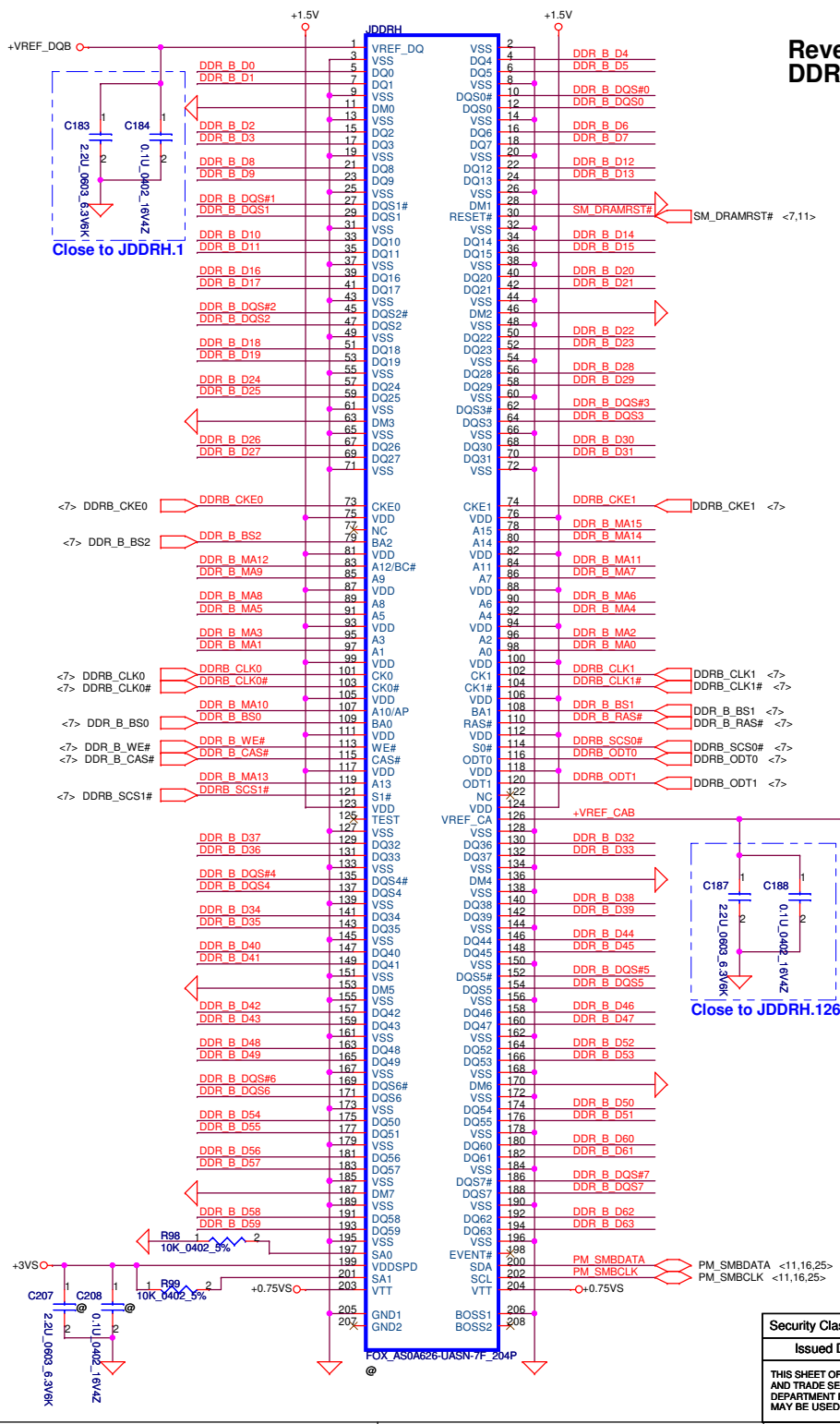


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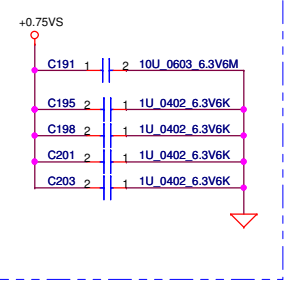
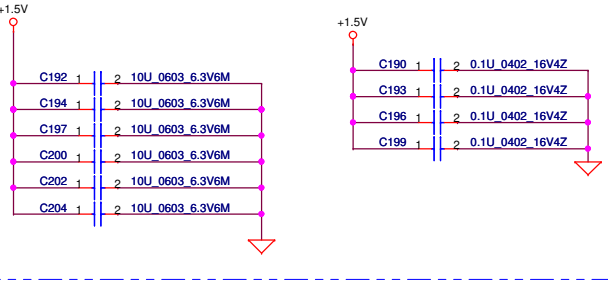
Reverse Type DDR3 SO-DIMM B



Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

Layout Note:
Place near JDDRH.203 and 204



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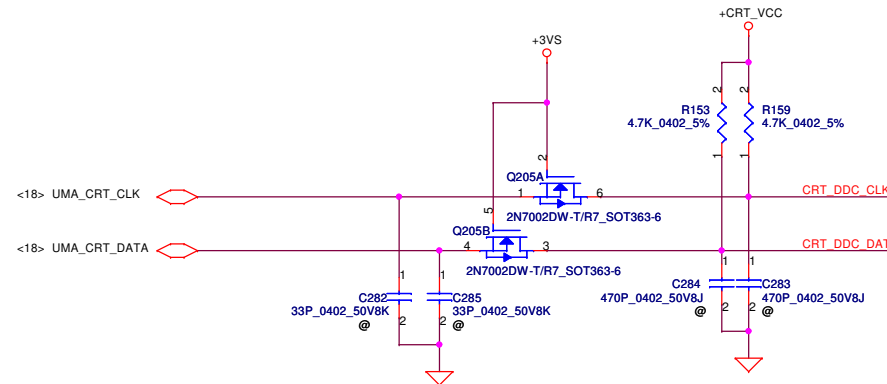
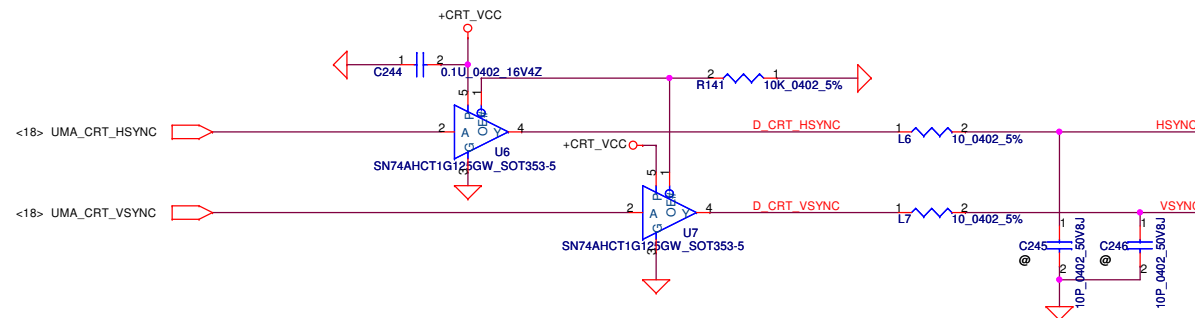
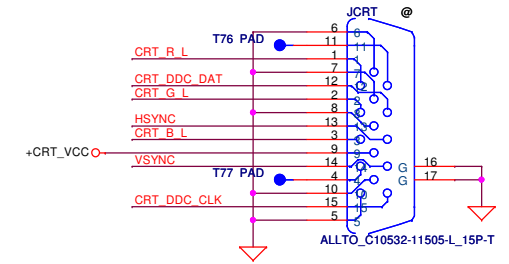
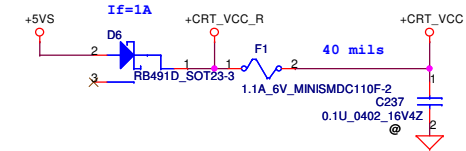
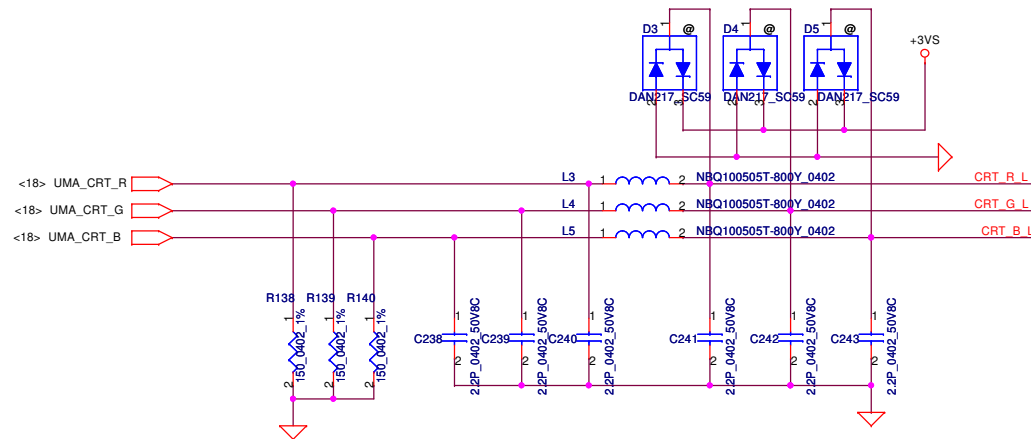


LCD/PANEL BD. Conn.



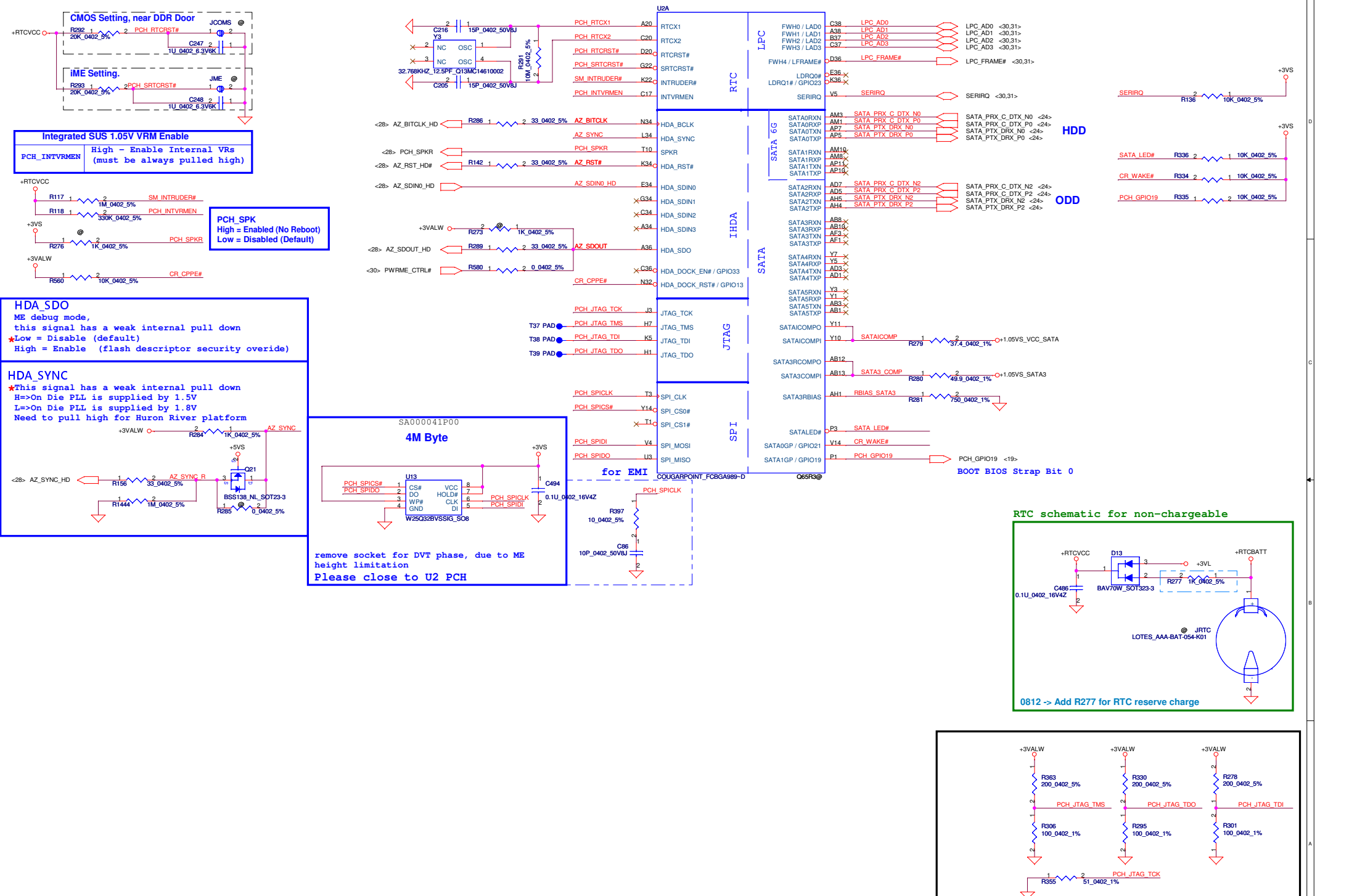
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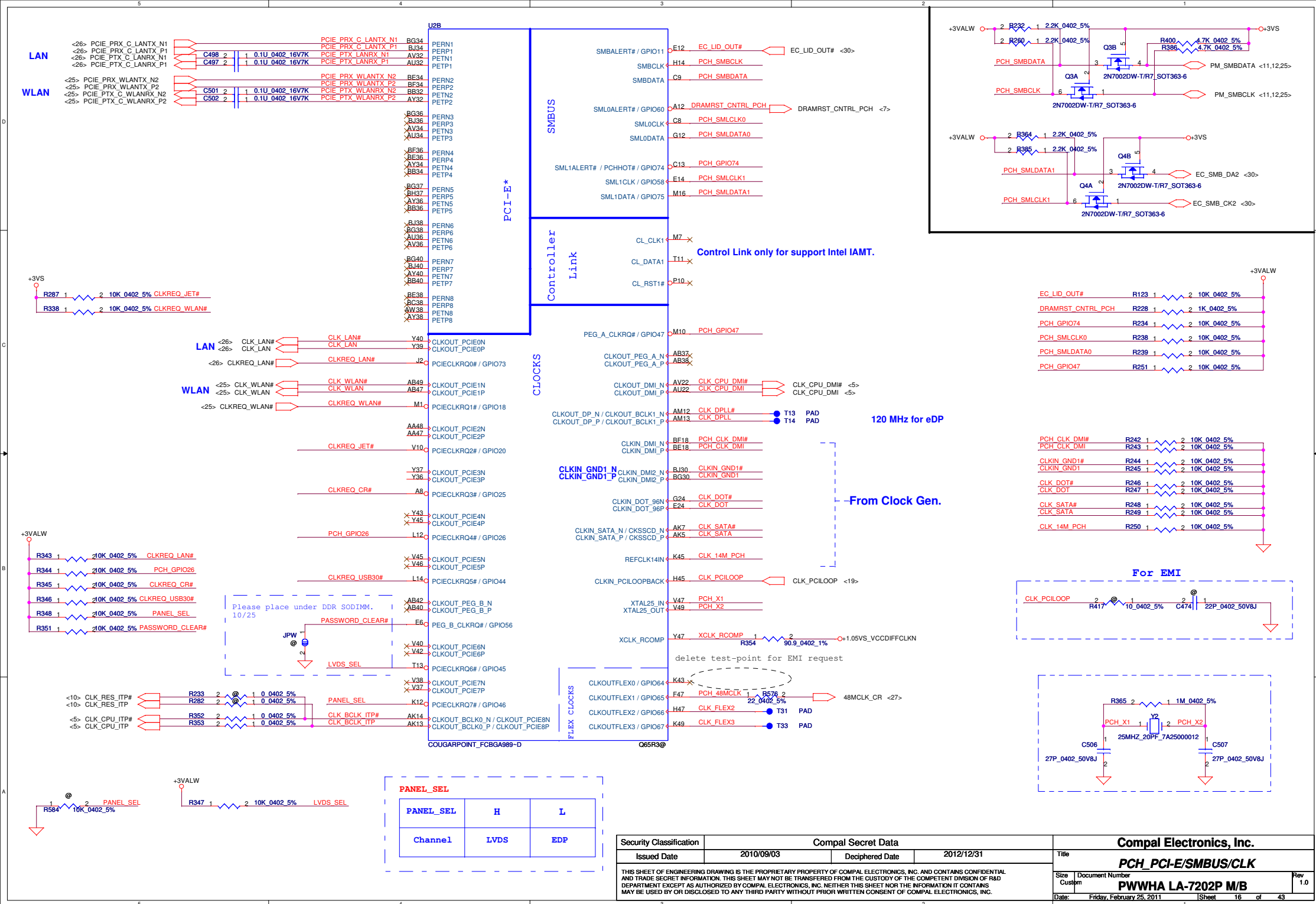
CRT CONNECTOR

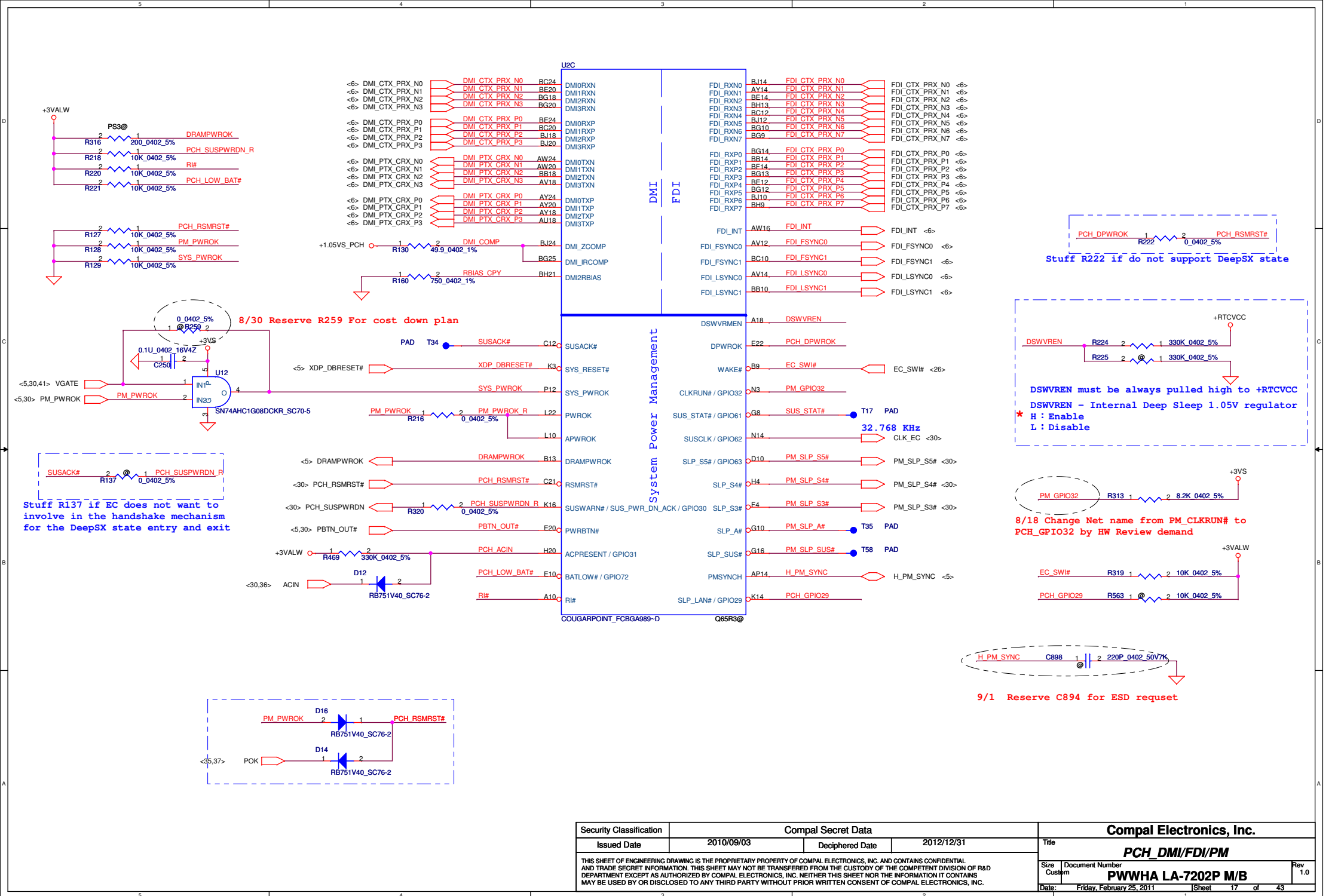


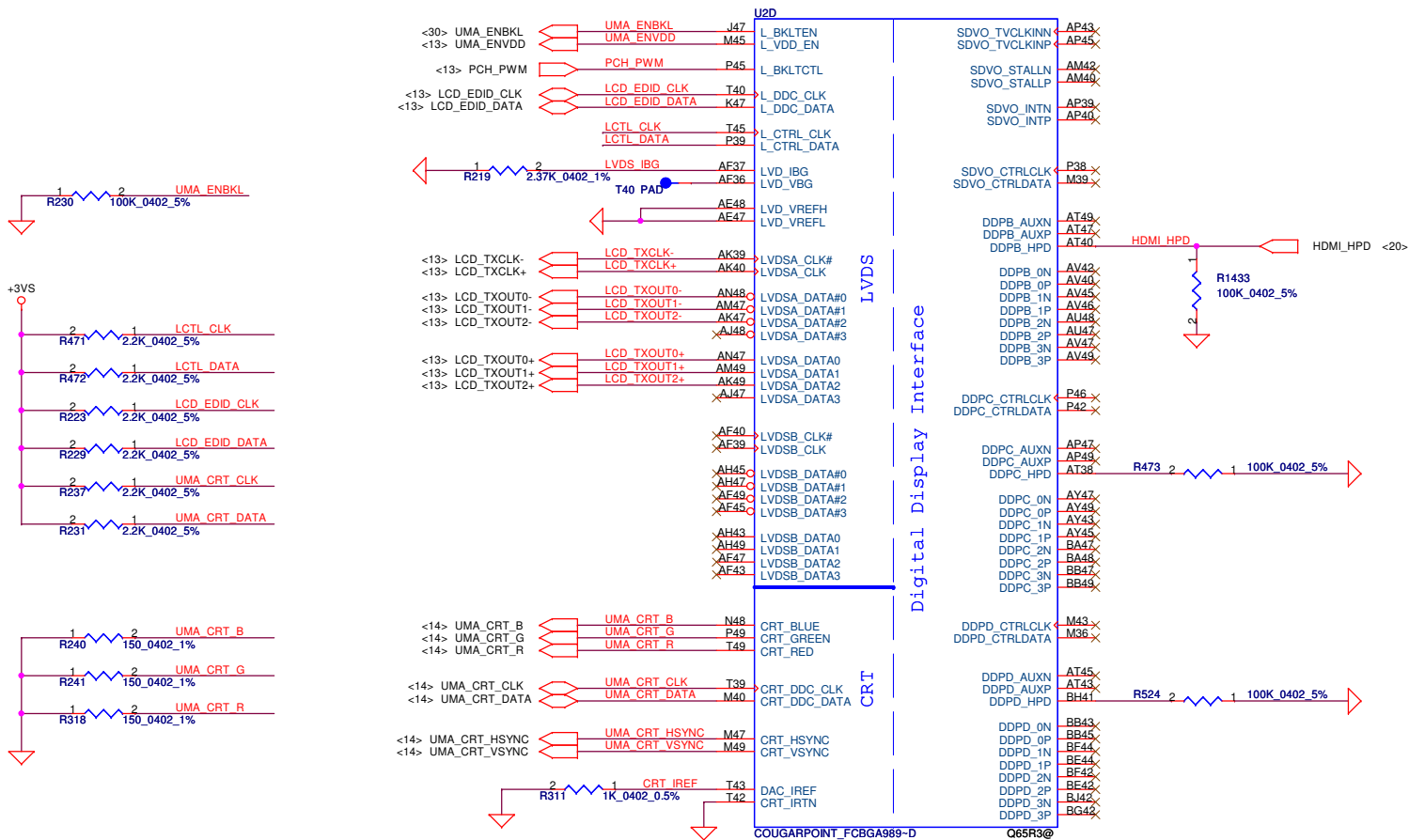
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Issued Date				2010/09/03		Deciphered Date		2012/12/31		Title	
										CRT	
										PWWHA LA-7202P M/B	
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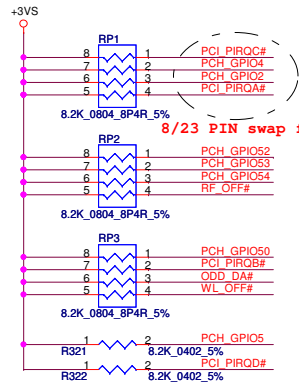




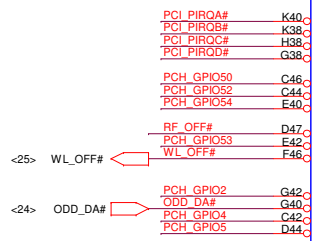




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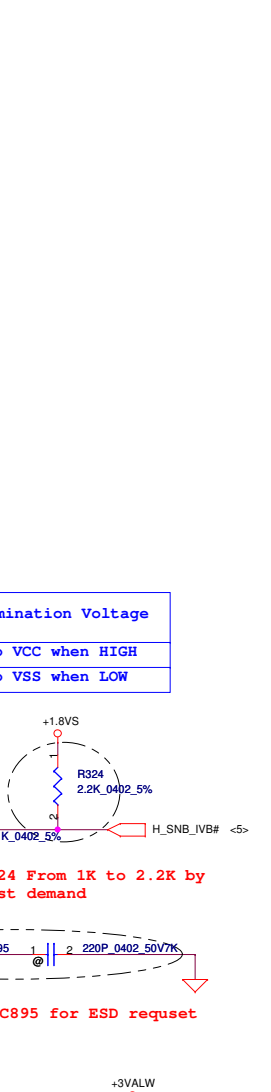
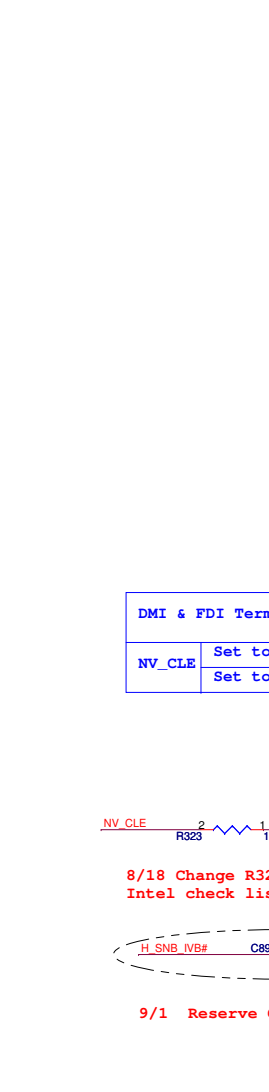
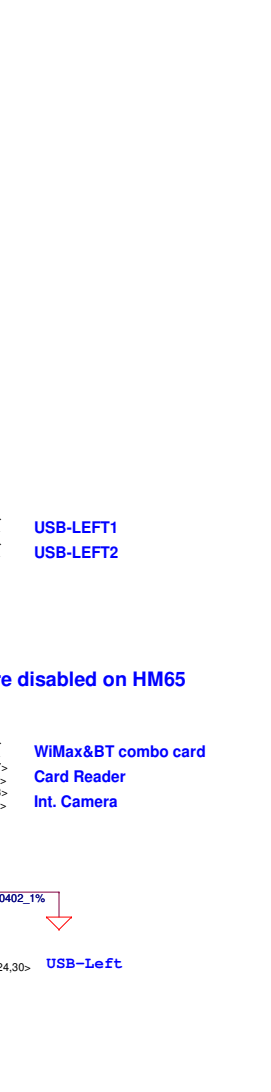
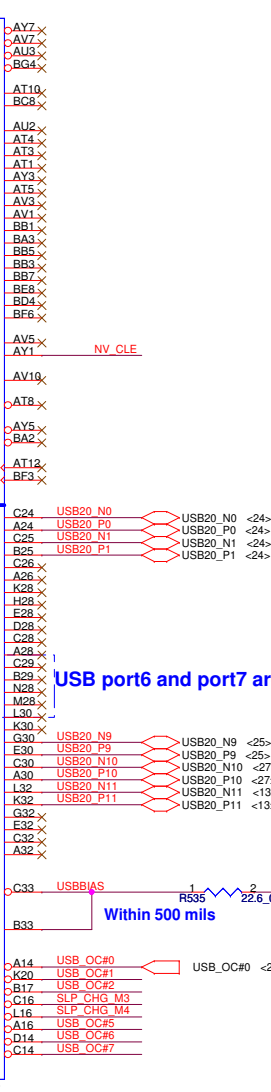
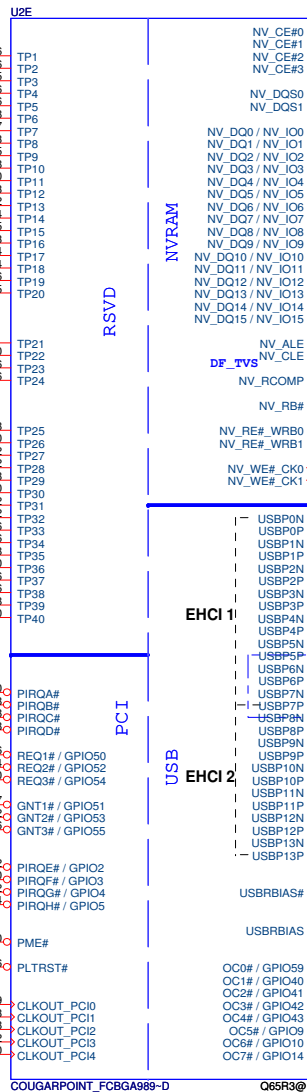


8/23 PIN swap for layout request

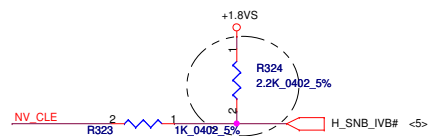


Boot BIOS Strap		
RF_OFF#	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *

A16 Swap Override Strap	
WL_OFF#	Low= A16 swap override Enable High= A16 swap override Disable
1	0



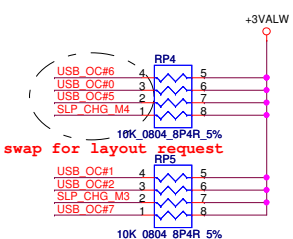
DMI & FDI Termination Voltage	
NV_CLE	Set to VCC when HIGH Set to VSS when LOW



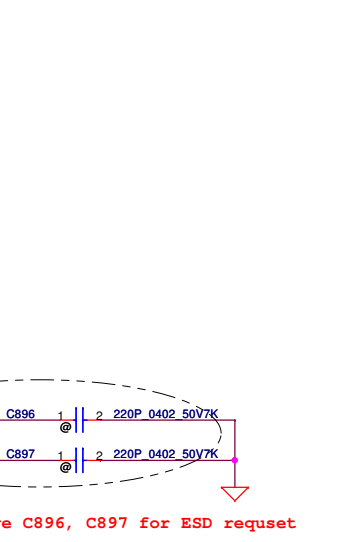
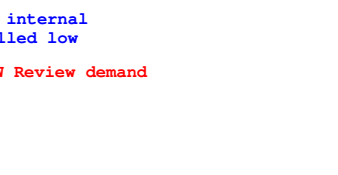
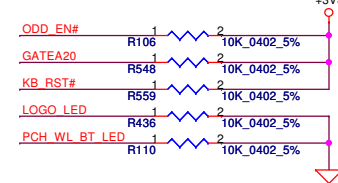
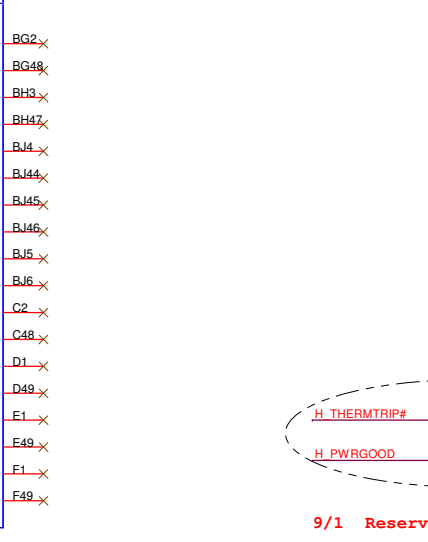
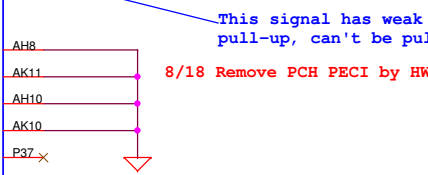
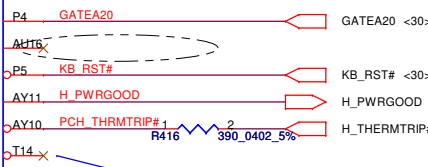
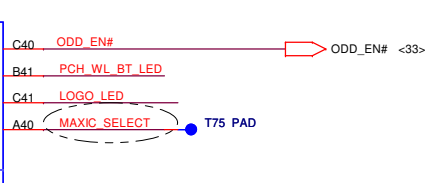
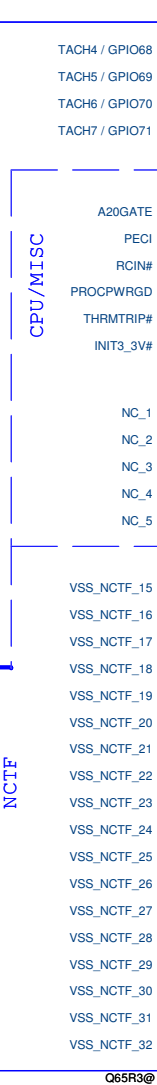
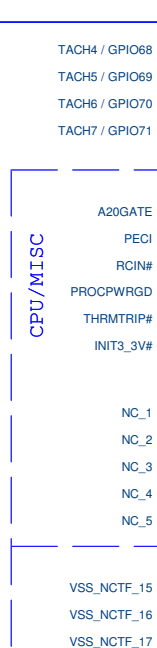
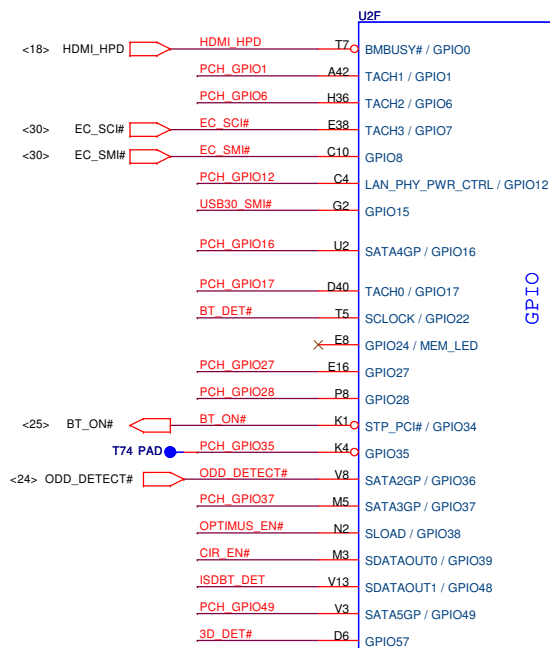
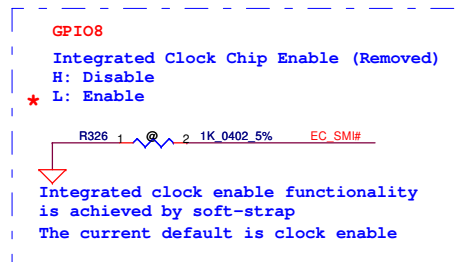
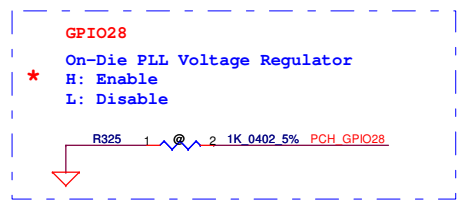
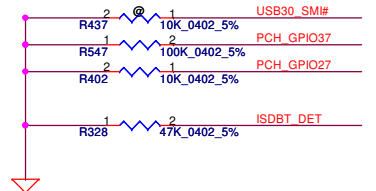
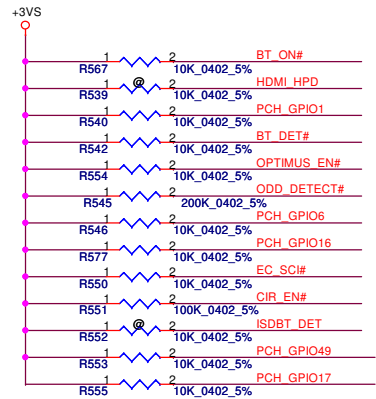
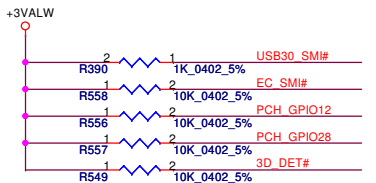
8/18 Change R324 From 1K to 2.2K by Intel check list demand



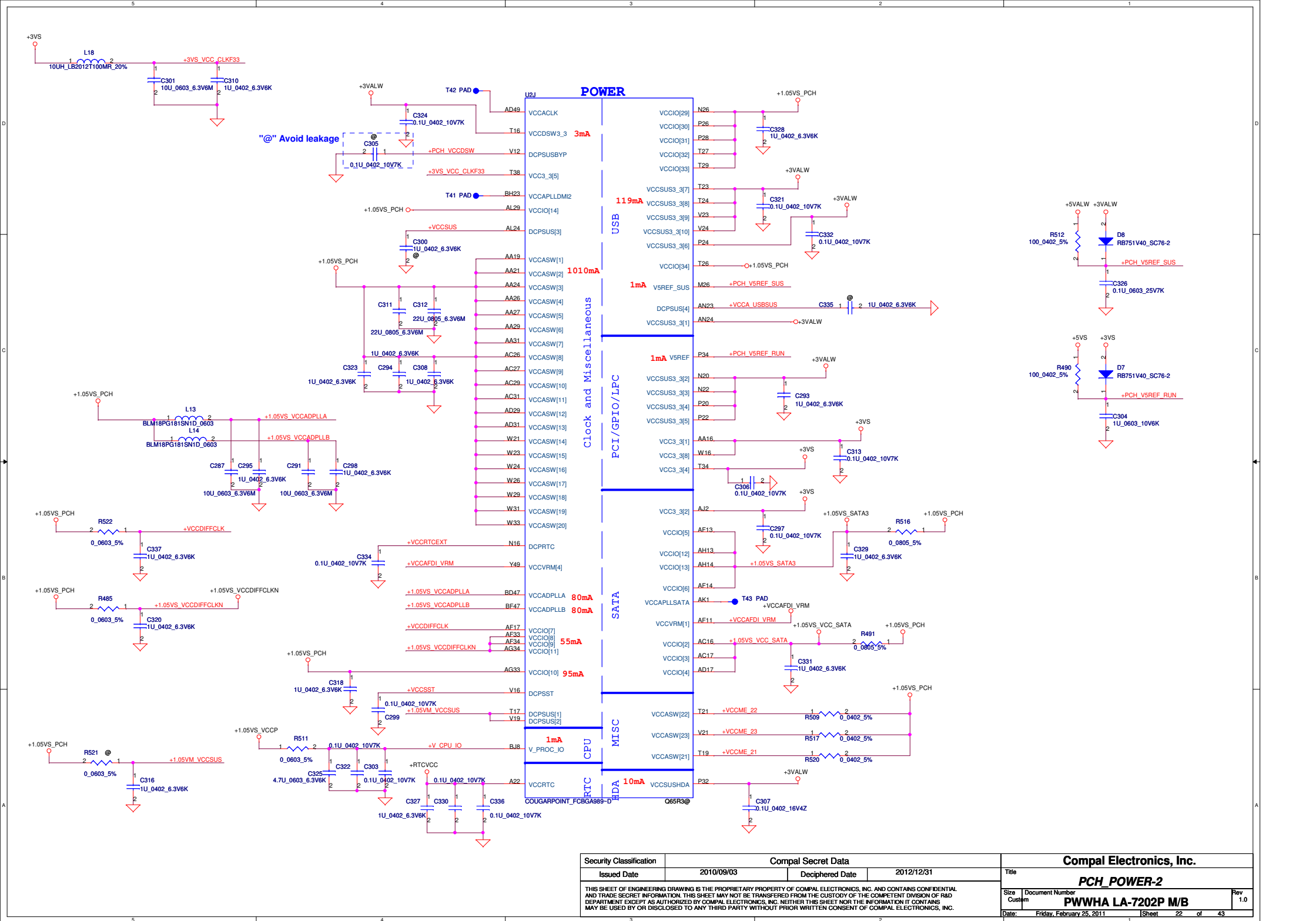
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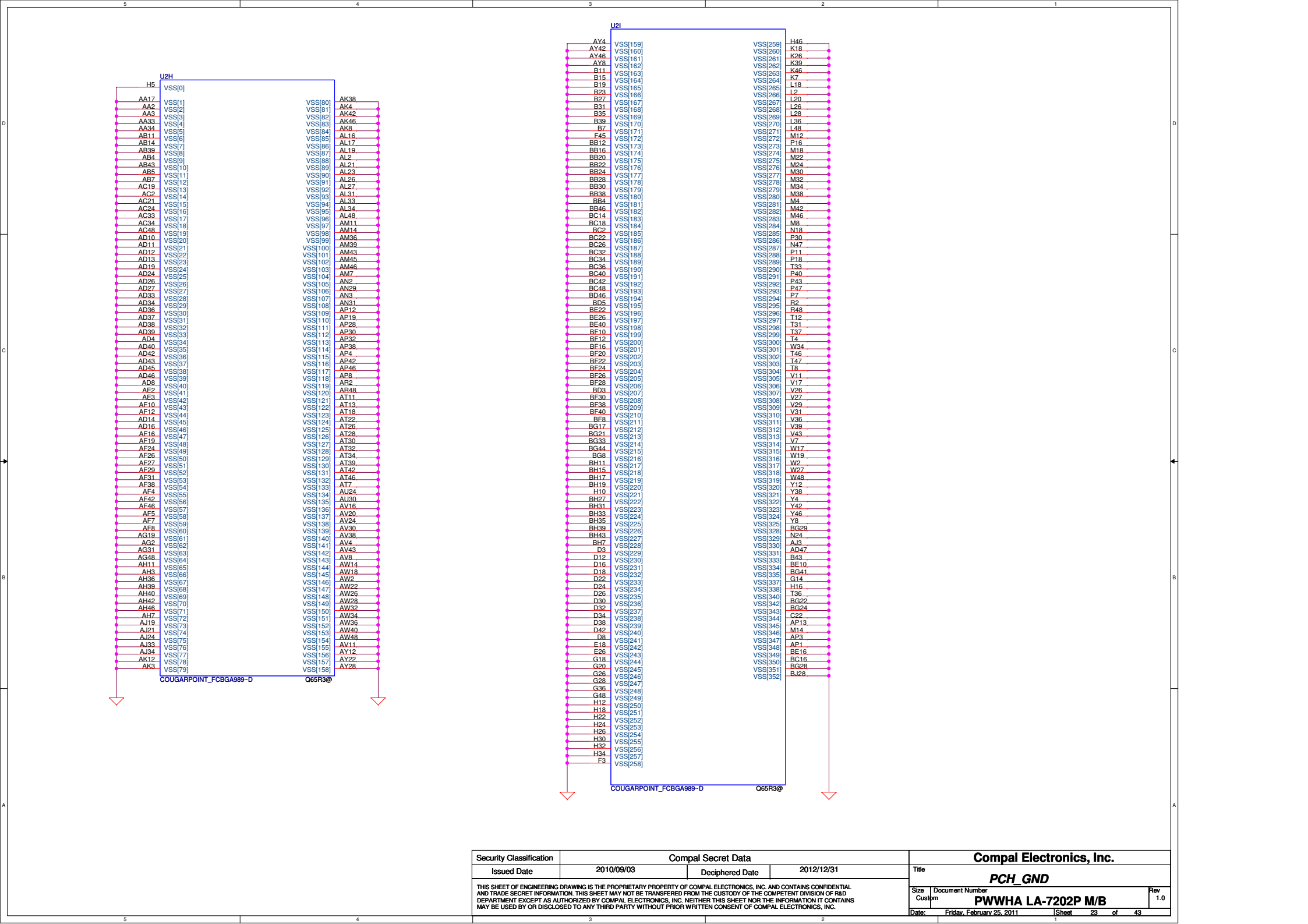


8/23 PIN swap for layout request

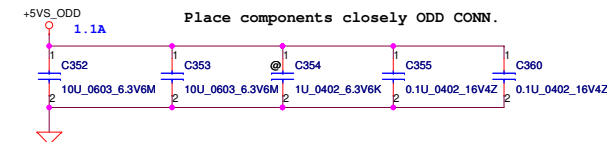
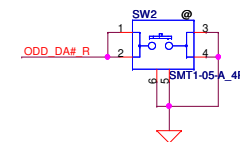


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Size B	Document Number	PWWHA LA-7202P M/B		Rev	1.0
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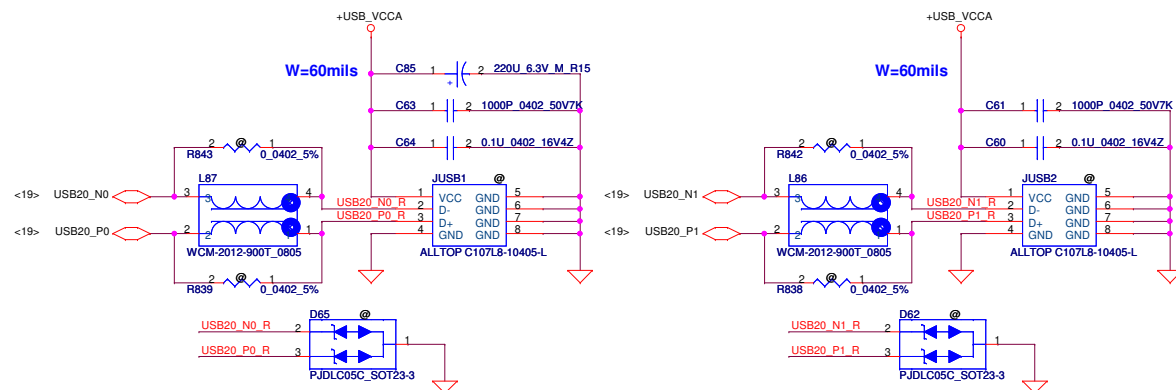
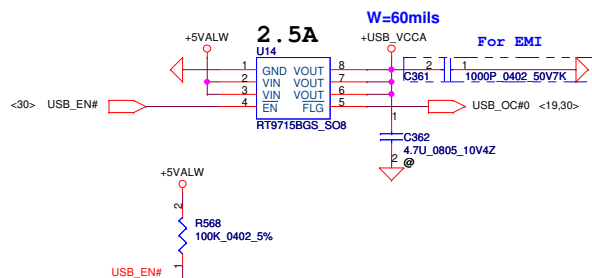




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Size		Document Number		Rev	
Custom		PWWHA LA-7202P M/B		1.0	
Date:		Friday, February 25, 2011		Sheet	23 of 43

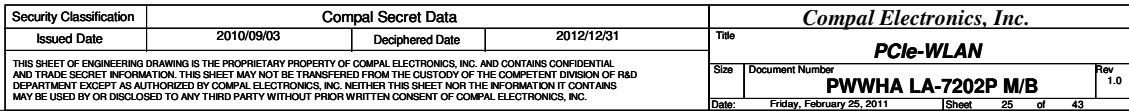
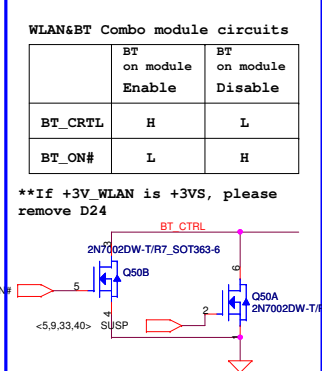


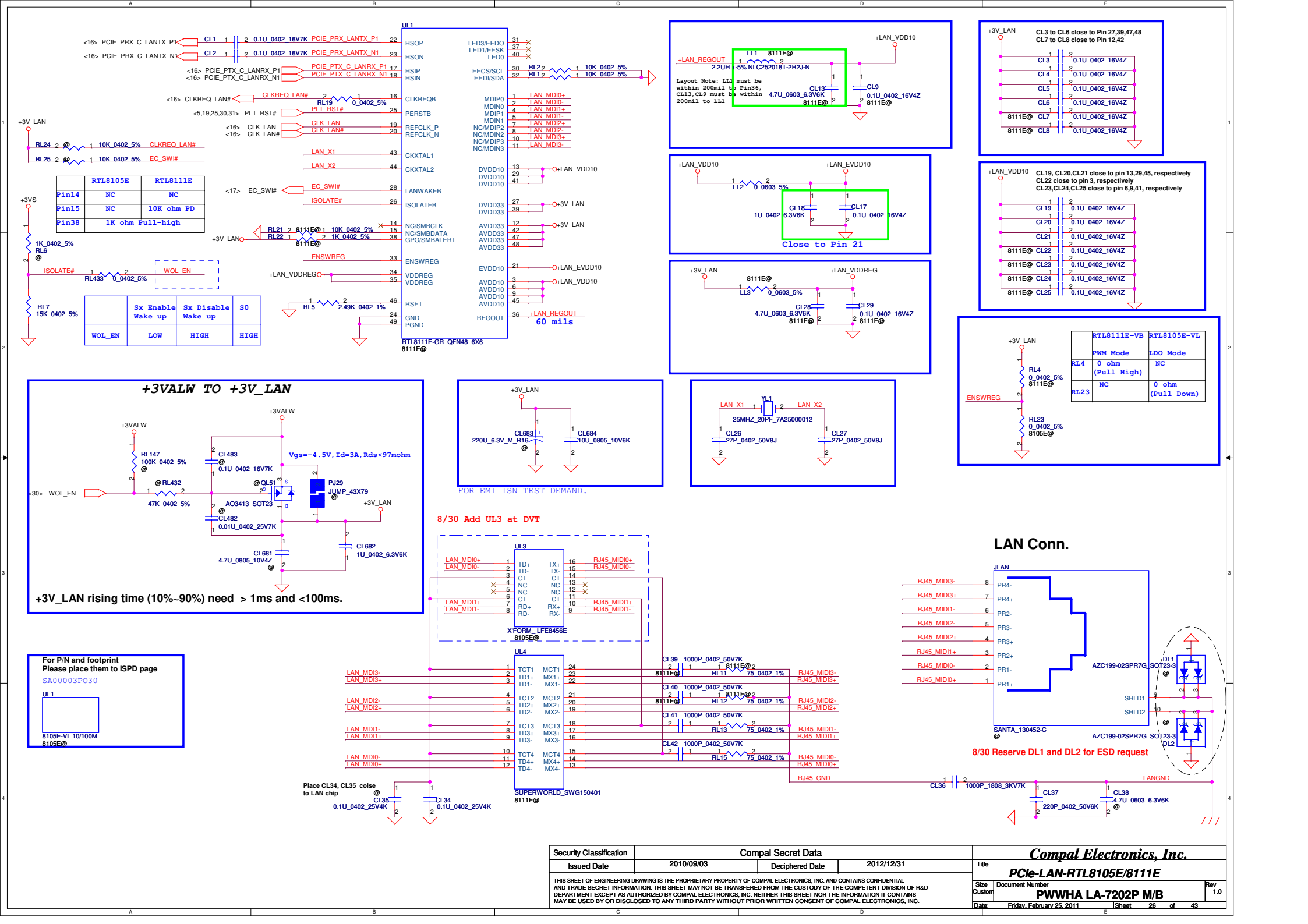
USB Conn. Left Side

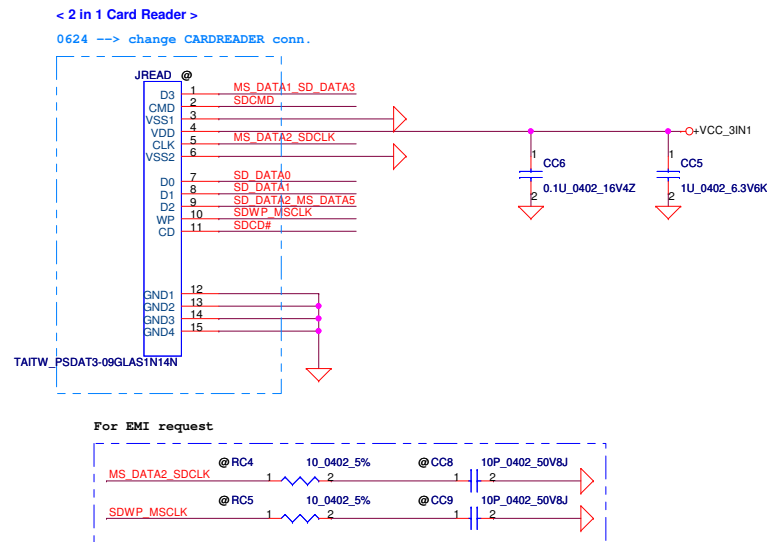
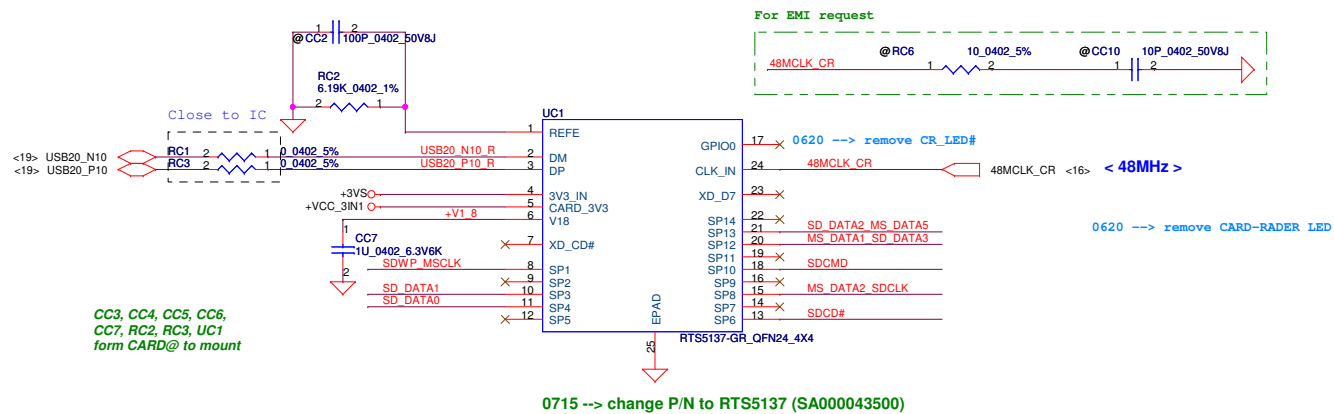


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				SATA-HDD/ODD/USB		
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Short PJ27 for Wimax
Short PJ26 for WLAN







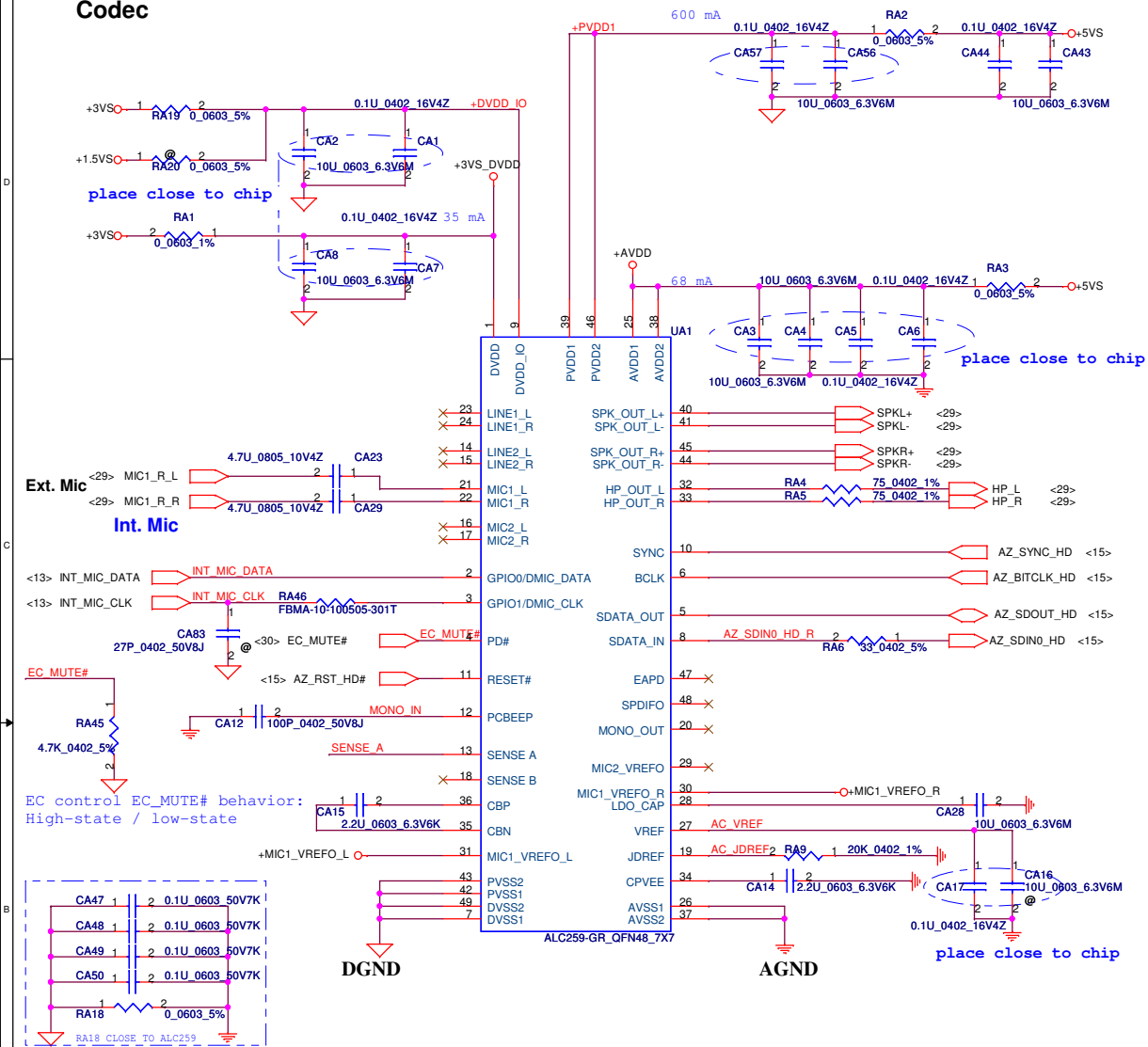
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Issued Date	2010/09/03	Deciphered Date	2012/12/31	PCle-CardReader RTS5137	
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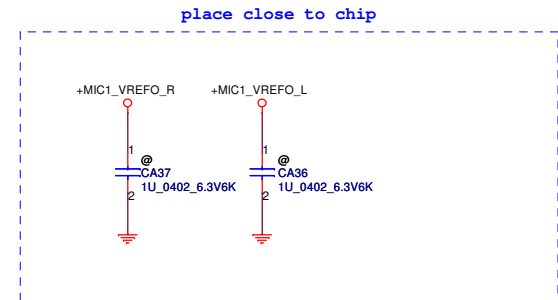
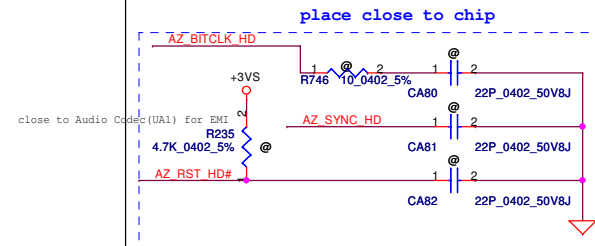
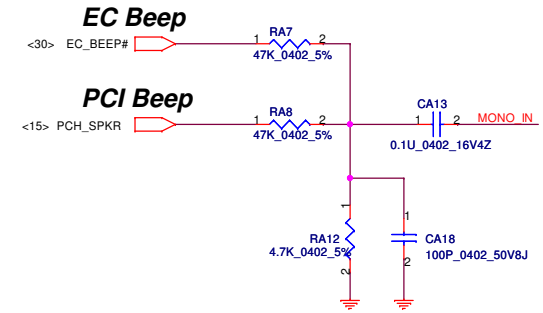
PCle-CardReader RTS5137

PWWHA LA-7202P M/B

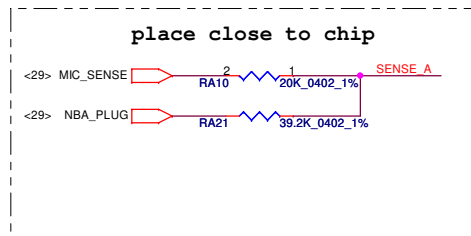
Codec



Beep sound

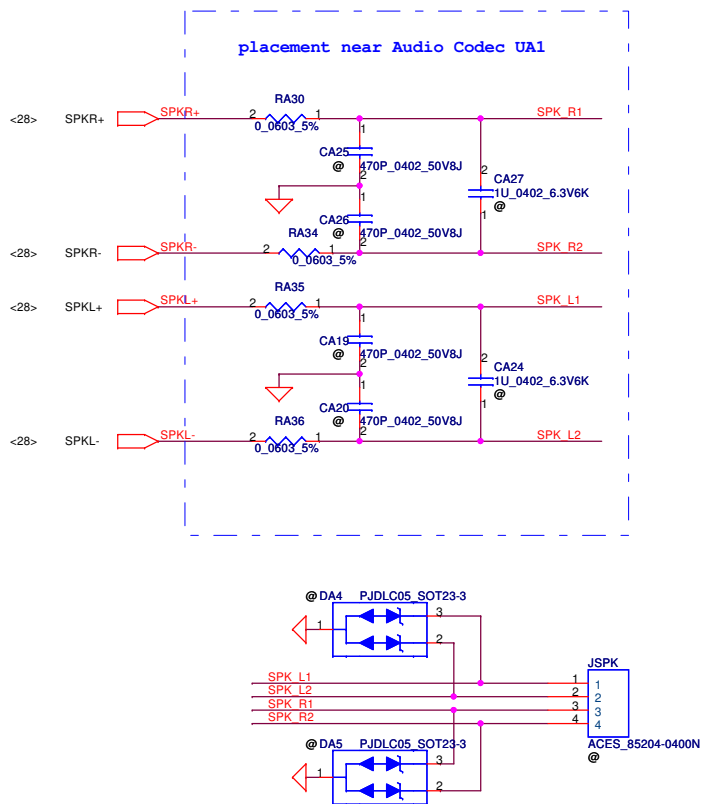


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
SENSE B	5.1K	(PIN 48)	
	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 20)	

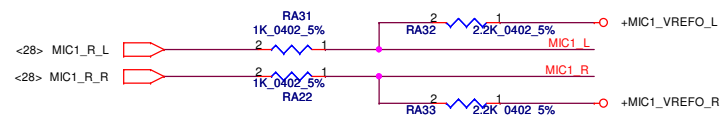


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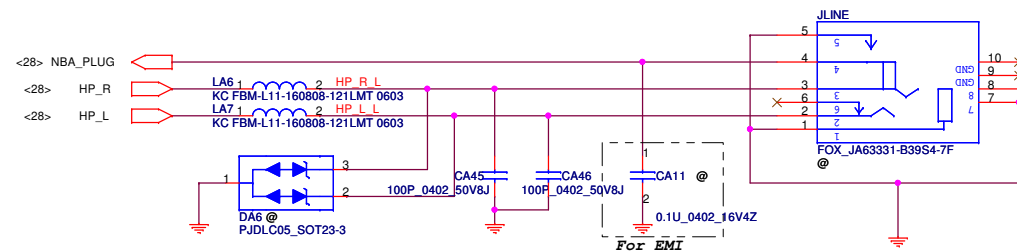
Speaker Connector



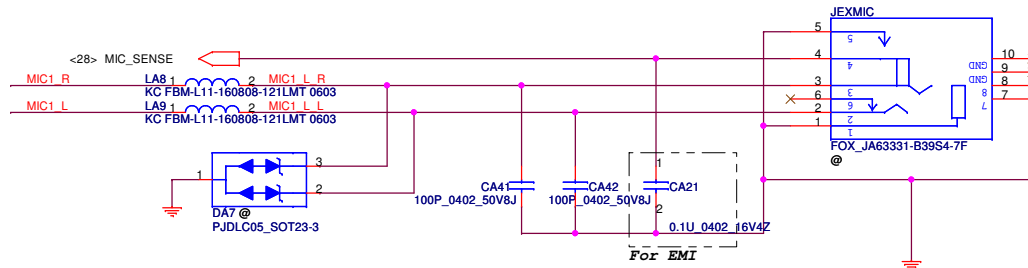
Ext. Mic



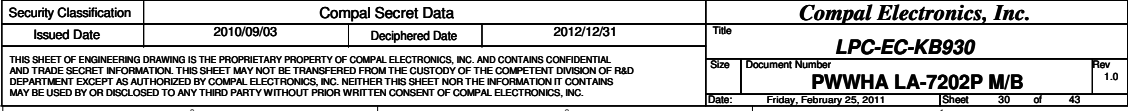
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK



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[illegible]

PCB Debug Port

The diagram illustrates the PCB debug port circuit. It features a central component labeled 'H7' with pins 0 through 10. Pin 6 is connected to +3VS. Pin 7 is connected to SERIRQ through a resistor R392 (22_0402_5%). Pin 8 is connected to LPC_AD3. Pin 9 is connected to LPC_AD1. Pin 10 is connected to LPC_FRAME#. Pin 5 is connected to PLT_RST# through a resistor R393 (22_0402_5%). Pin 4 is connected to LPC_AD2. Pin 3 is connected to LPC_AD0. Pin 2 is connected to LPC_AD0. Pin 1 is connected to CLK_PCI_DDR. Pin 0 is connected to a ground symbol. A dashed box labeled 'For EMI' contains a network of components: a resistor R393 (22_0402_5%), a capacitor C457 (22P_0402_50V8J), and a ground symbol. The text 'Place the PAD under DDR DIMM.' is written above the H7 component.

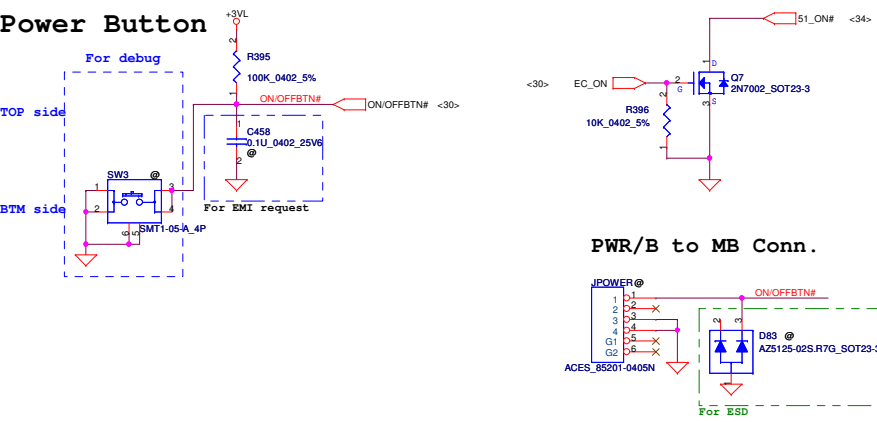
[illegible]

KSO16	1	2
KSO17	C401	100P_0402_50VB8J
	C402	100P_0402_50VB8J
KSO2	C404	100P_0402_50VB8J
KSO1	C405	100P_0402_50VB8J
KSO0	C406	100P_0402_50VB8J
KSO4	C407	100P_0402_50VB8J
KSO3	C408	100P_0402_50VB8J
KSO5	C409	100P_0402_50VB8J
KSO14	C410	100P_0402_50VB8J
KSO6	C411	100P_0402_50VB8J
KSO7	C412	100P_0402_50VB8J
KSO13	C413	100P_0402_50VB8J
KSO8	C415	100P_0402_50VB8J
KSO9	C416	100P_0402_50VB8J
KSO10	C417	100P_0402_50VB8J
KSO11	C418	100P_0402_50VB8J
KSO12	C419	100P_0402_50VB8J
KSO15	C420	100P_0402_50VB8J
KS17	C421	100P_0402_50VB8J
KS12	C422	100P_0402_50VB8J
KS13	C423	100P_0402_50VB8J
KS14	C424	100P_0402_50VB8J
KS10	C425	100P_0402_50VB8J
KS15	C427	100P_0402_50VB8J
KS16	C429	100P_0402_50VB8J
KS11	C431	100P_0402_50VB8J
CAPS_LED#	C433	100P_0402_50VB8J
NUM_LED#	C435	100P_0402_50VB8J

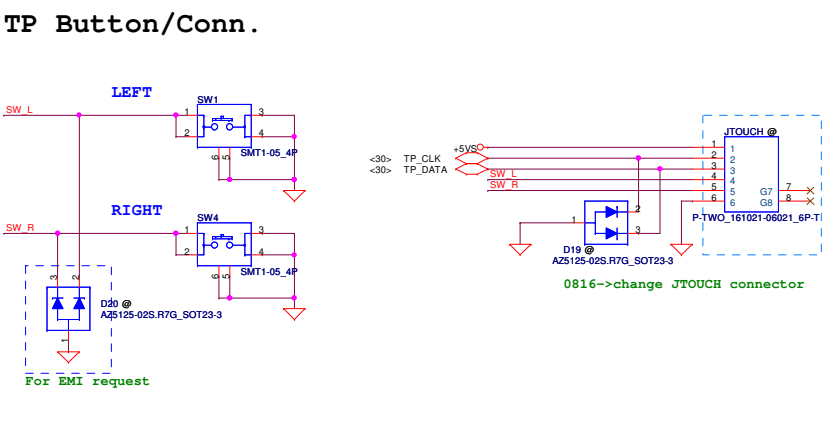
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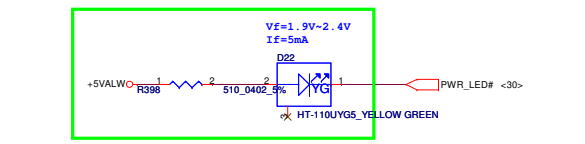
Power Button



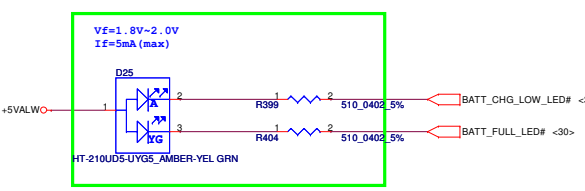
TP Button/Conn.



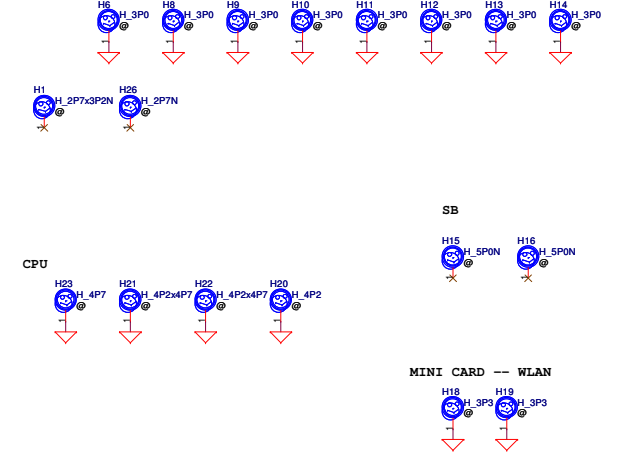
POWER/SUSPEND LED



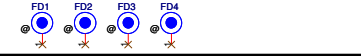
BATT CHARGE/FULL LED



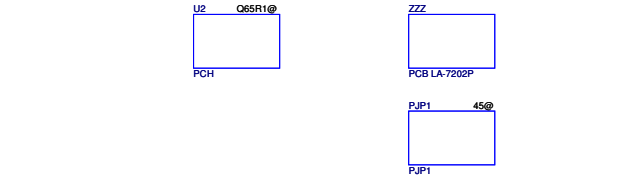
Screw Hole



PCB Fedical Mark PAD

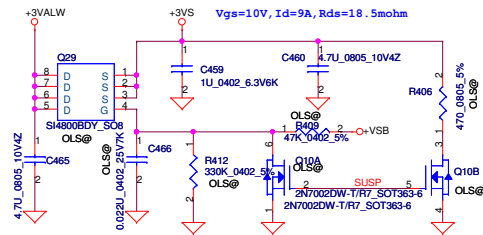


ISPD

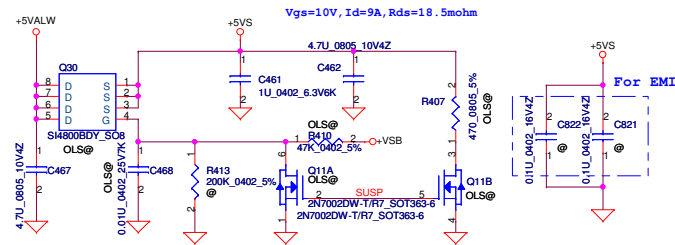


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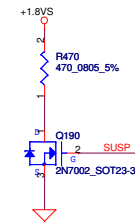
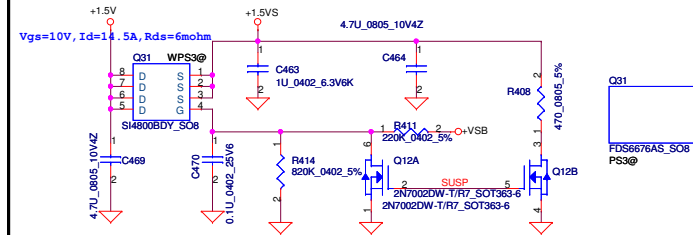
+3VALW TO +3VS



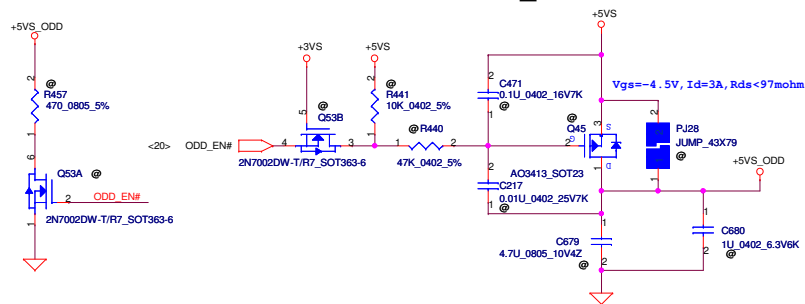
+5VALW TO +5VS



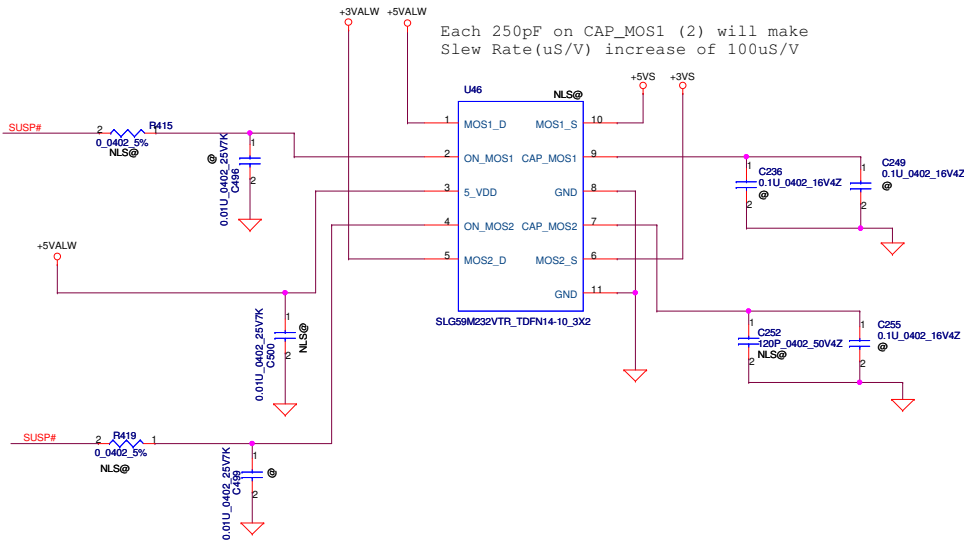
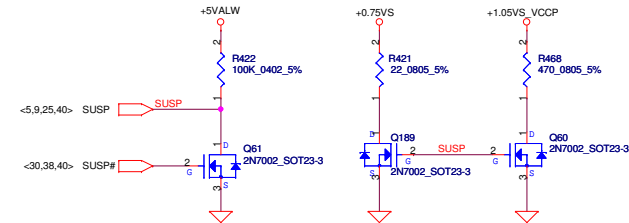
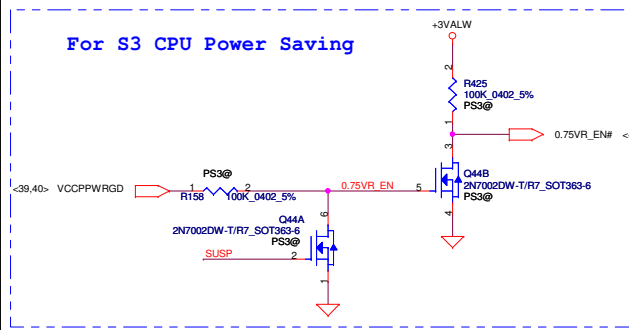
+1.5V to +1.5VS



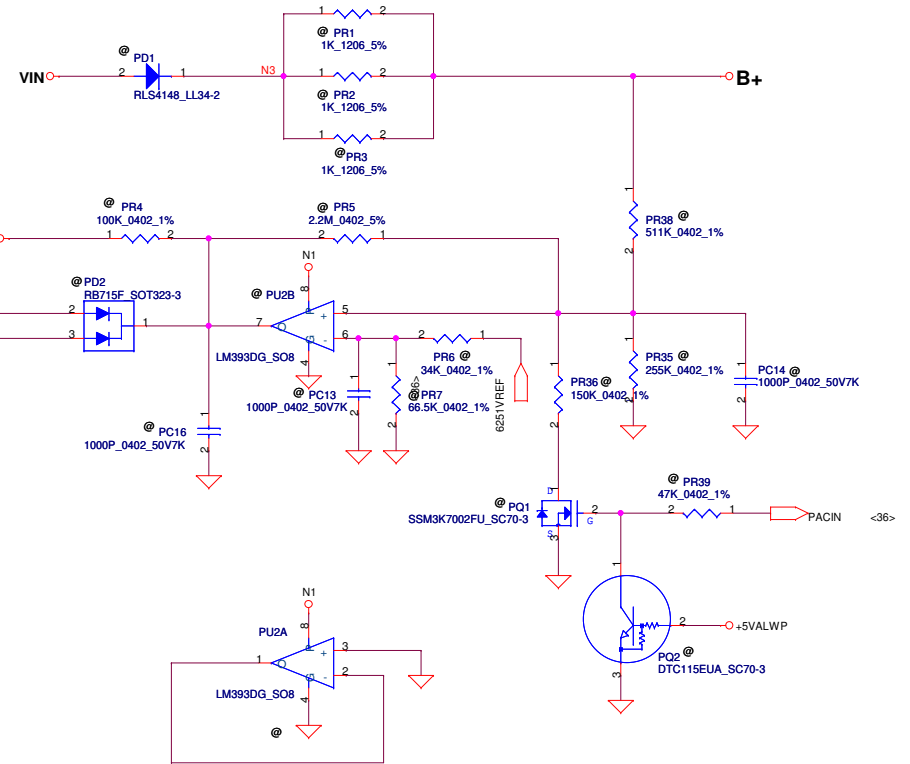
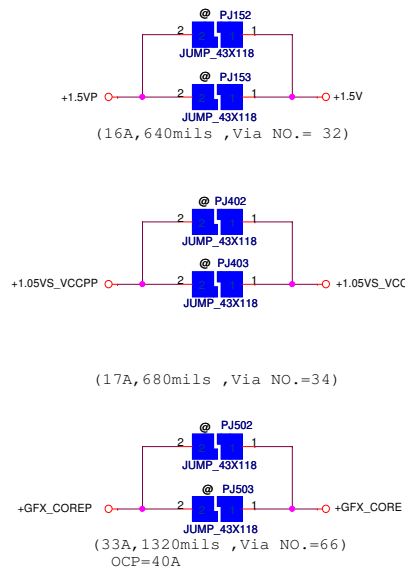
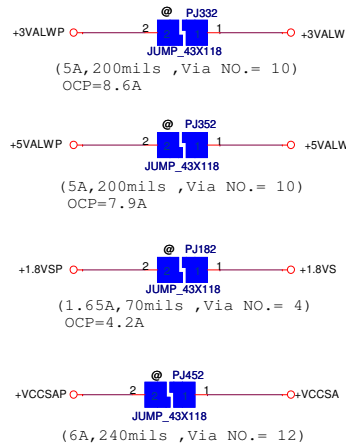
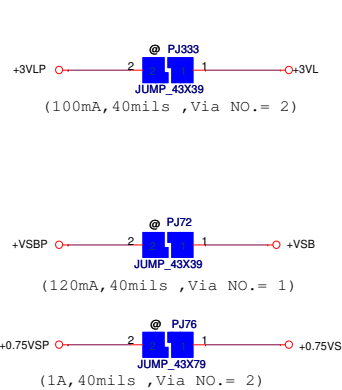
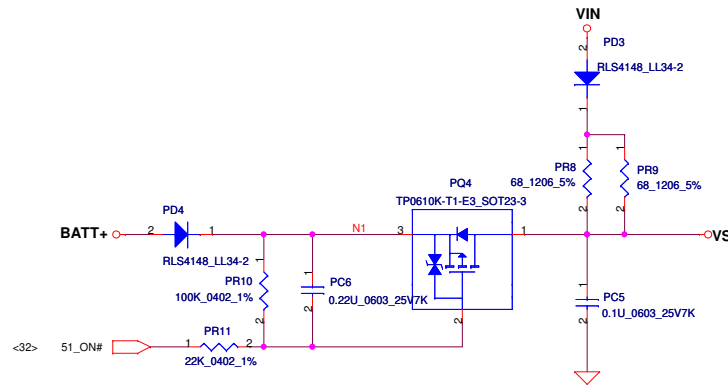
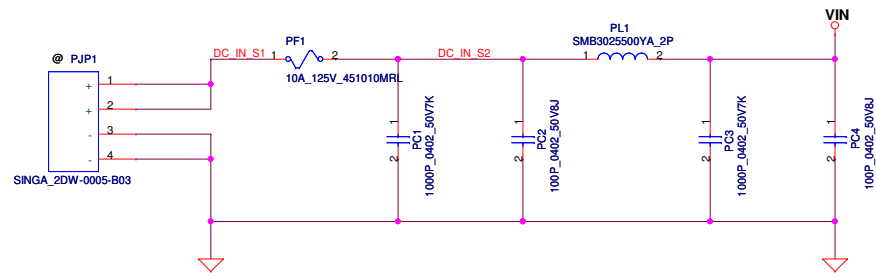
+5VS TO +5VS_ODD



For S3 CPU Power Saving



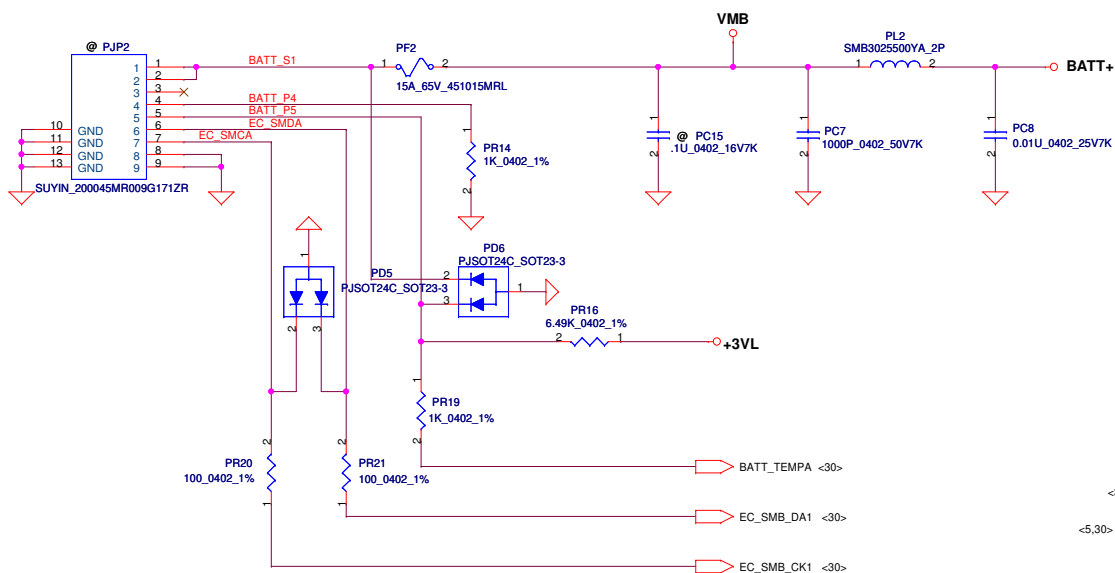
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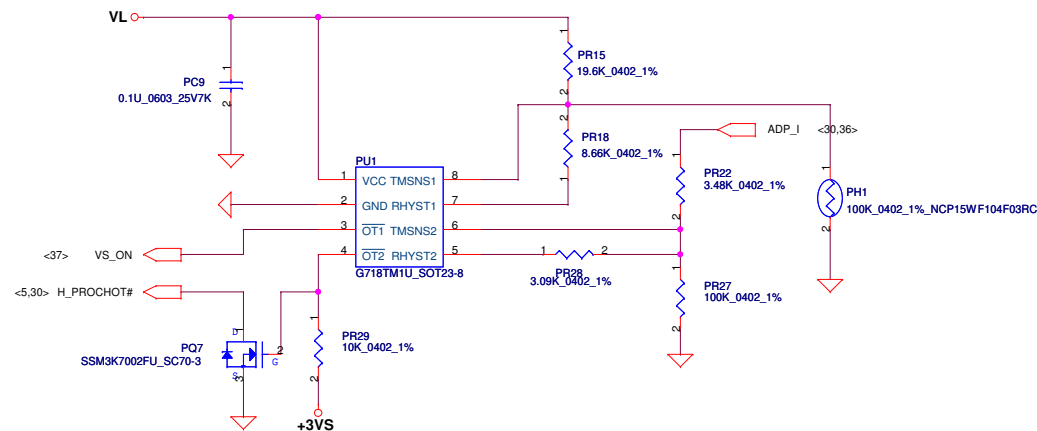
ACIN			
	Precharge detector		
	Min.	typ.	Max.
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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Deciphered Date				2012/12/31				DCIN/VIN DETECTOR			
Size				Document Number				PWWHA LA-7202 M/B			
Date				Friday, February 25, 2011				Sheet 34 of 43			
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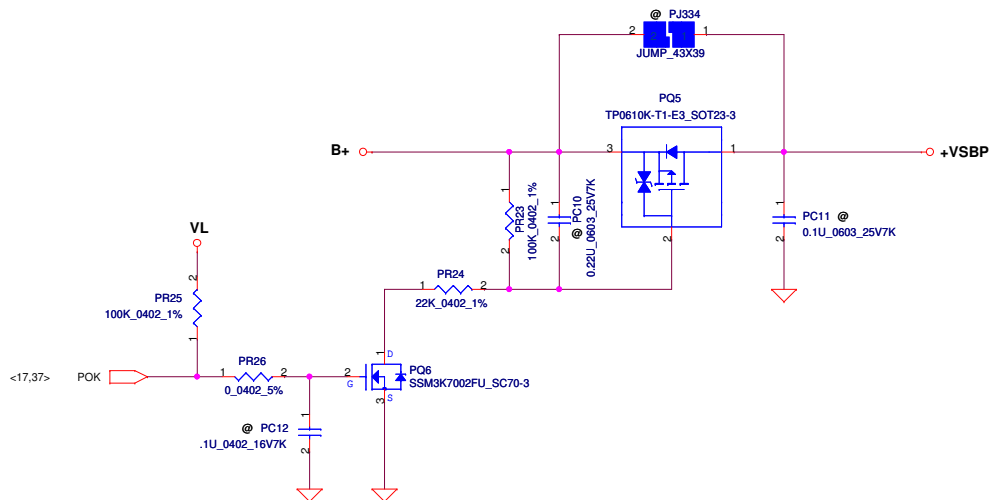
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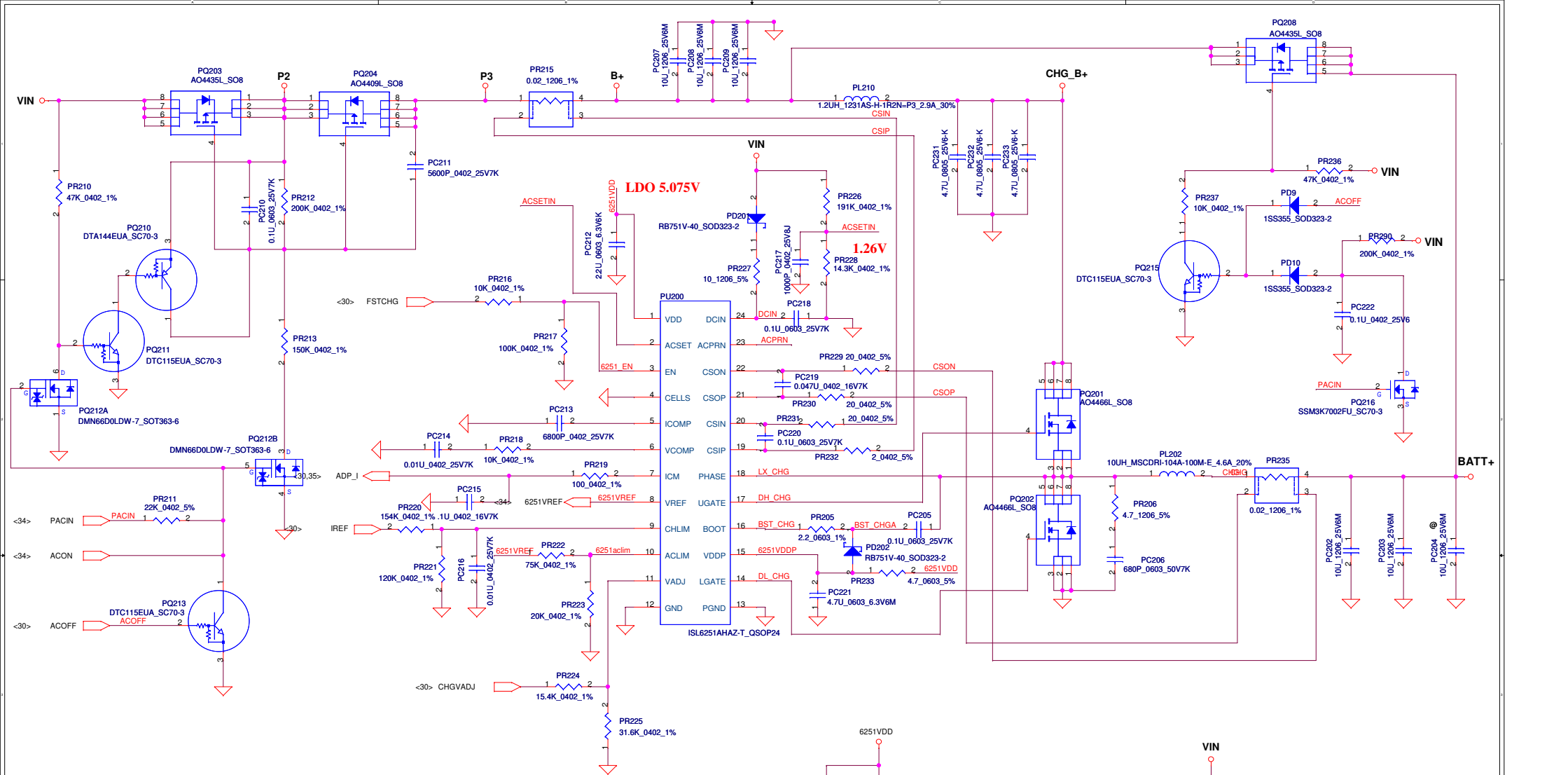


PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C



Adapter	Throttle Watt	Recovery Watt	Throttle Point	Recovery Point
65W_UMA	71.25W	62.4W	1.48V	1.308V
75W_DIS	85.5W	72W	1.78V	1.5V
75W_QCore	85.5W	72W	1.78V	1.5V





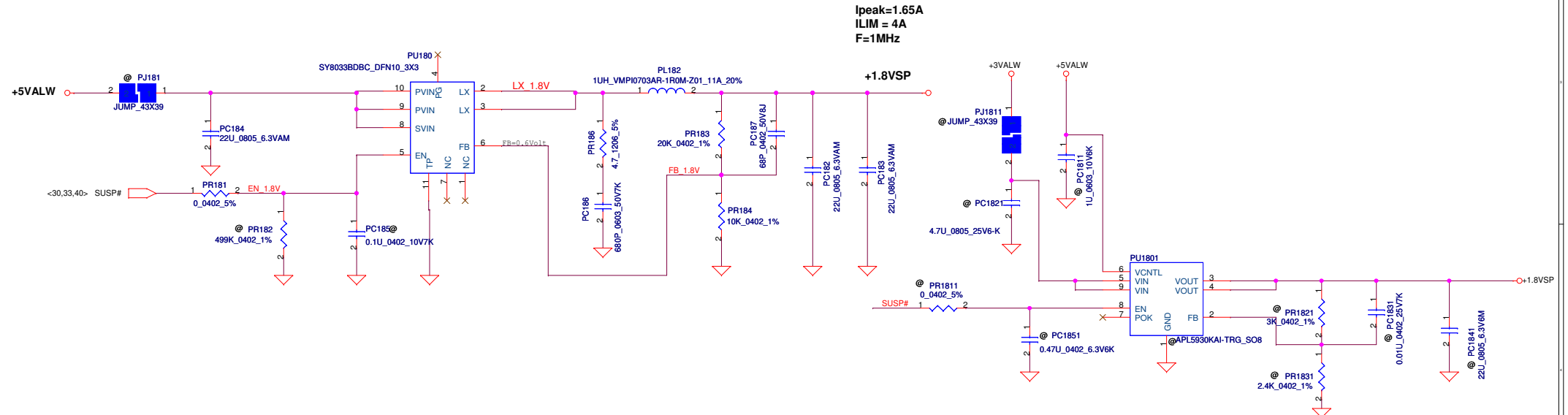
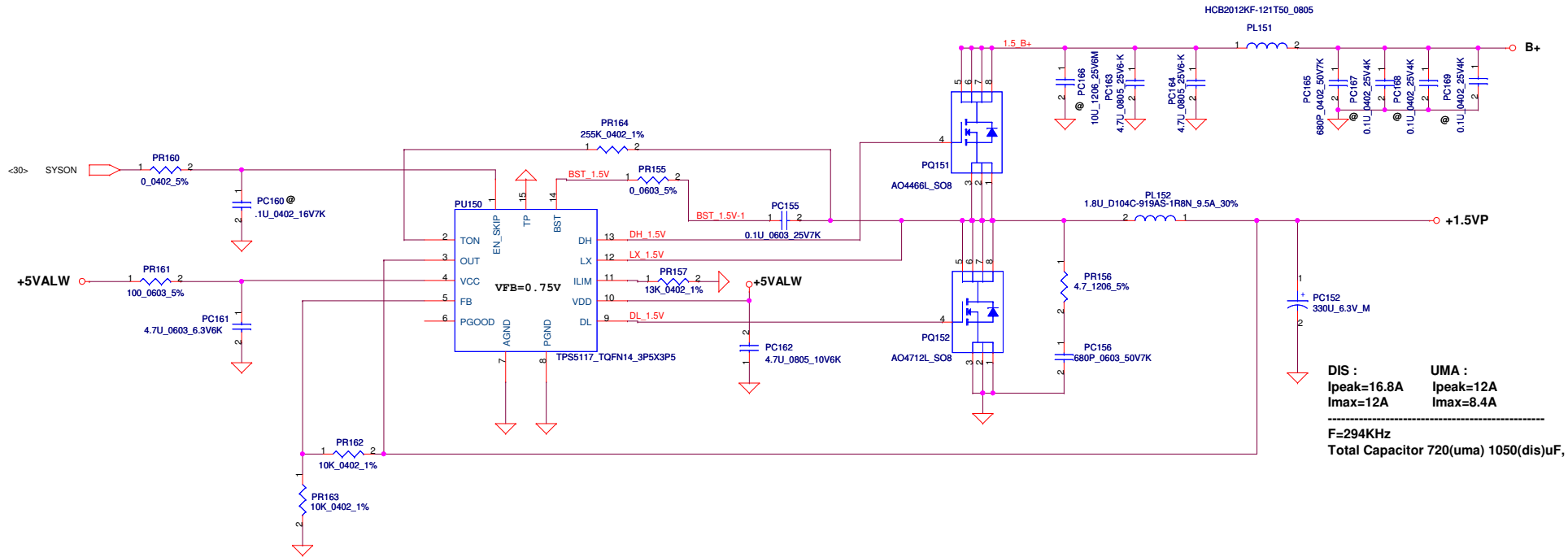
CC=0.25A~3A
 IREF=1.016*Icharge
 IREF=0.254V~3.048V
 VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

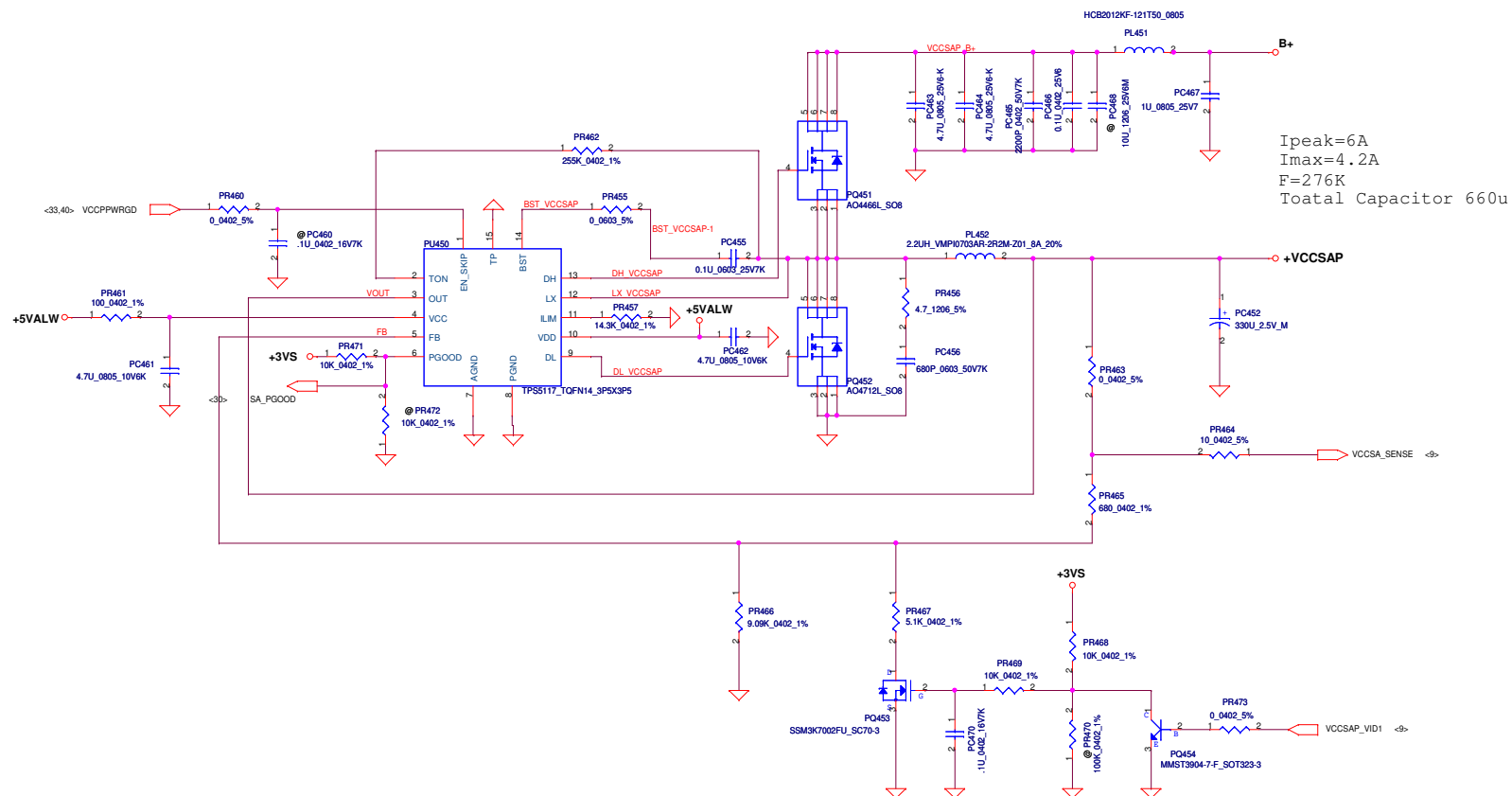
CP mode	
Iada=0~3.42A (65W)	CP= 92%*Iada; CP=3.147A
VacLim=1.08V (65W)	PR222=75k PR223=20k PR215=0.02
Iada=0~3.947A (75W)	CP= 92%*Iada; CP=3.63A
VacLim=0.736V (75W)	PR222=24k PR223=20k PR215=0.02

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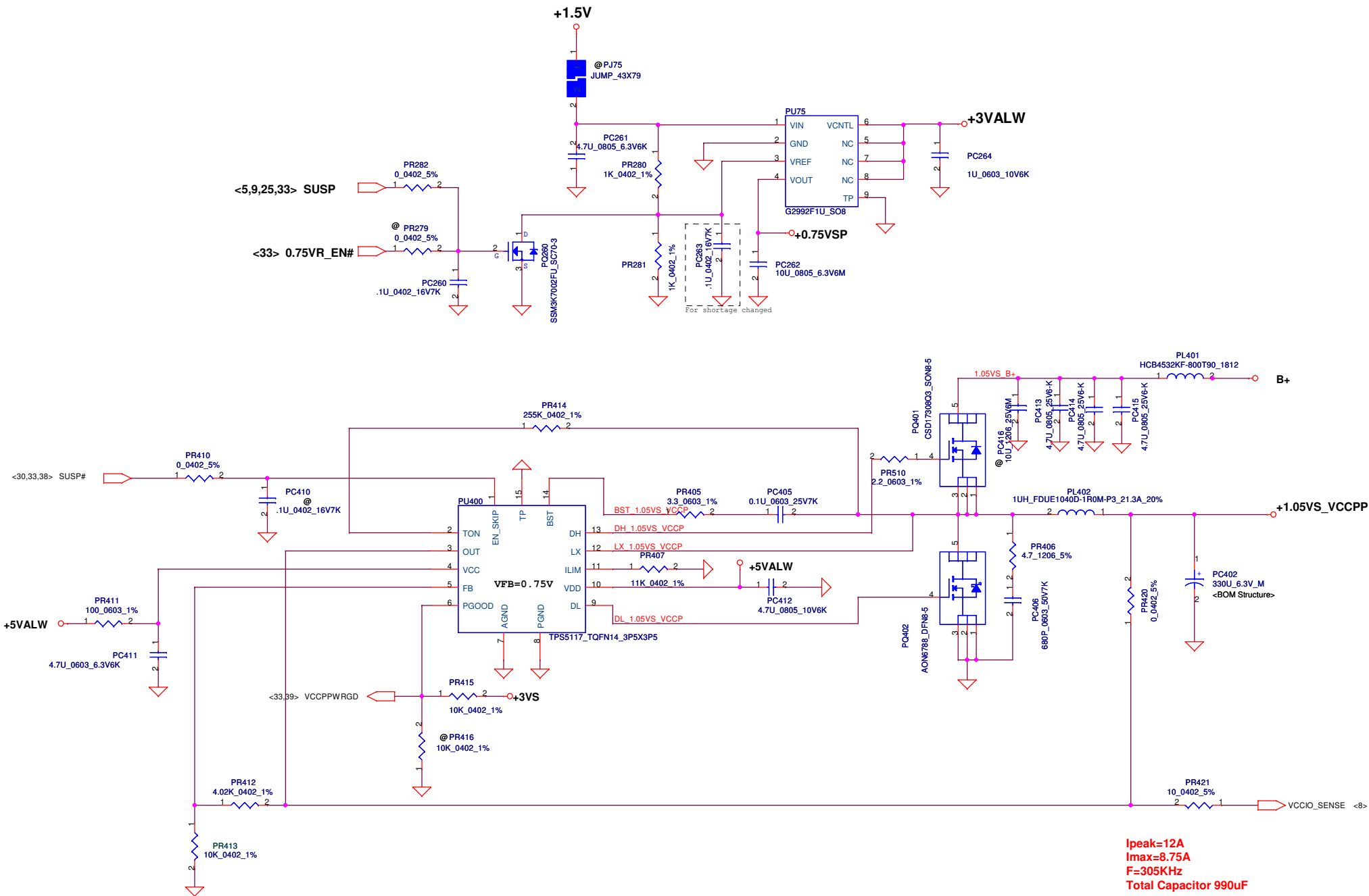
Compal Electronics, Inc.			
Title CHARGER			
Size	Document Number	PWWHA LA-7202 M/B	
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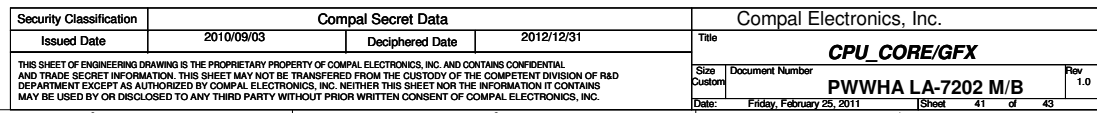
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title	+1.5VP/+1.8VSP
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VID1	+VCCSAP
1	0.8V
0	0.9V



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				Size Custom	Document Number
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PAGE	MODIFICATION LIST	PURPOSE
2010/12/31 (PVT) P36 Charger	Change PQ203,PQ208 to AO4435L	Cost down
2010/12/31 (PVT) P36 Charger	add PQ207,PQ208,PQ209 10u	EMI command
2010/12/31 (PVT) P36 Charger	add snubber PR206,PC206	EMI command
2010/12/31 (PVT) P36 Charger	change boost to 2.2 ohm PR205	EMI command
2010/12/31 (PVT) P35 +3VALW/+5VALW	add snubber PR336,PC336,PR356,PC336	EMI command
2010/12/31 (PVT) P37 +1.5VP/+1.8VSP	add snubber PR156,PC156	EMI command
2010/12/31 (PVT) P37 +1.5VP/+1.8VSP	add PC165 for MEI	EMI command
2010/12/31 (PVT) P37 +VCCSA	add snubber PR456,PC456	EMI command
2010/12/31 (PVT) P37 +VCCSA	change output capacitor PC452 to OS-con	cost down
2010/12/31 (PVT) P37 +VCCSA	change choke PL452 to molding	cost down
2010/12/31 (PVT) P38 +1.05VS/+0.75	add snubber PC406 PR406	EMI command
2010/12/31 (PVT) P38 +1.05VS/+0.75	change 0.75V enable PR279 tp PR282	HW command
2010/12/31 (PVT) P39 +CPU_CORE	change PC549,PC515,PC525,PC 505 to correct rating	design change
2010/12/31 (PVT) P39 +CPU_CORE	change PL502,PL503,PL504 to DCR 5%	design change
2010/12/31 (PVT) P39 +CPU_CORE	change PC568 PC 566 to 5.8mmm capacitor	design change
2010/12/31 (PVT) P39 +CPU_CORE	change PL551 for load line adjust	design change
2010/12/31 (PVT) P39 +CPU_CORE	change PR560 for program temperture	design change
2010/12/31 (PVT) P39 +CPU_CORE	change PC502,PC531,PC532 for burn-in shun down	design change

Title <Title>		
Size A	Document Number PWVHA LA-7202P M/B	Rev 1.0
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HW PIR (Product Improve Record)

PWWHA LA-7202P SCHEMATIC CHANGE LIST

REVISION CHANGE: 1.0

GERBER-OUT DATE: 2011/02/18

MODIFICATION LIST				PURPOSE
NO	DATE	PAGE		
1)	01/24	05	modify FAN with BTO item PWM and RPM	For HW BTO item
2)	01/24	05	modify RPM FAN connector pin define	Request from thermal team
3)	02/14	30	co-lay KB9012	For BTO item
4)	02/15	24	Add C450	For ESD request

Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		HW-PIR	
2010/08/03		2012/12/31			
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				Document Number PWWHA LA-7202P M/B	
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