Compal Confidential

PAU30 M/B Schematics Document

Intel Arrandale Processo SV with DDRIII + Ibex Peak-M

2010-11-22

REV:1.0

ZZZ
DAZ@
DAZ0F900100
PCB PAU30 LA-6392P LS-6391P/6392P/6393P/6394P

ZZZ1
DA1@
DA80000KE10
PCB 0F9 LA-6392P REV1 M/B

ZZZ2
DA2@
DA20000KT10
PCB 0F9 LS-6391P REV1 POWER_BTN/B

ZZZ3
DA2@
DA20000KU10
PCB 0F9 LS-6392P REV1 SWITCH/B

ZZZ4
DA2@
DA20000KV10
PCB 0F9 LS-6393P REV1 LED/B

ZZZ5
DA2@
DA20000LE10
PCB 0F9 LS-6394P REV1 LID SWITCH/B

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Title: Cover Page

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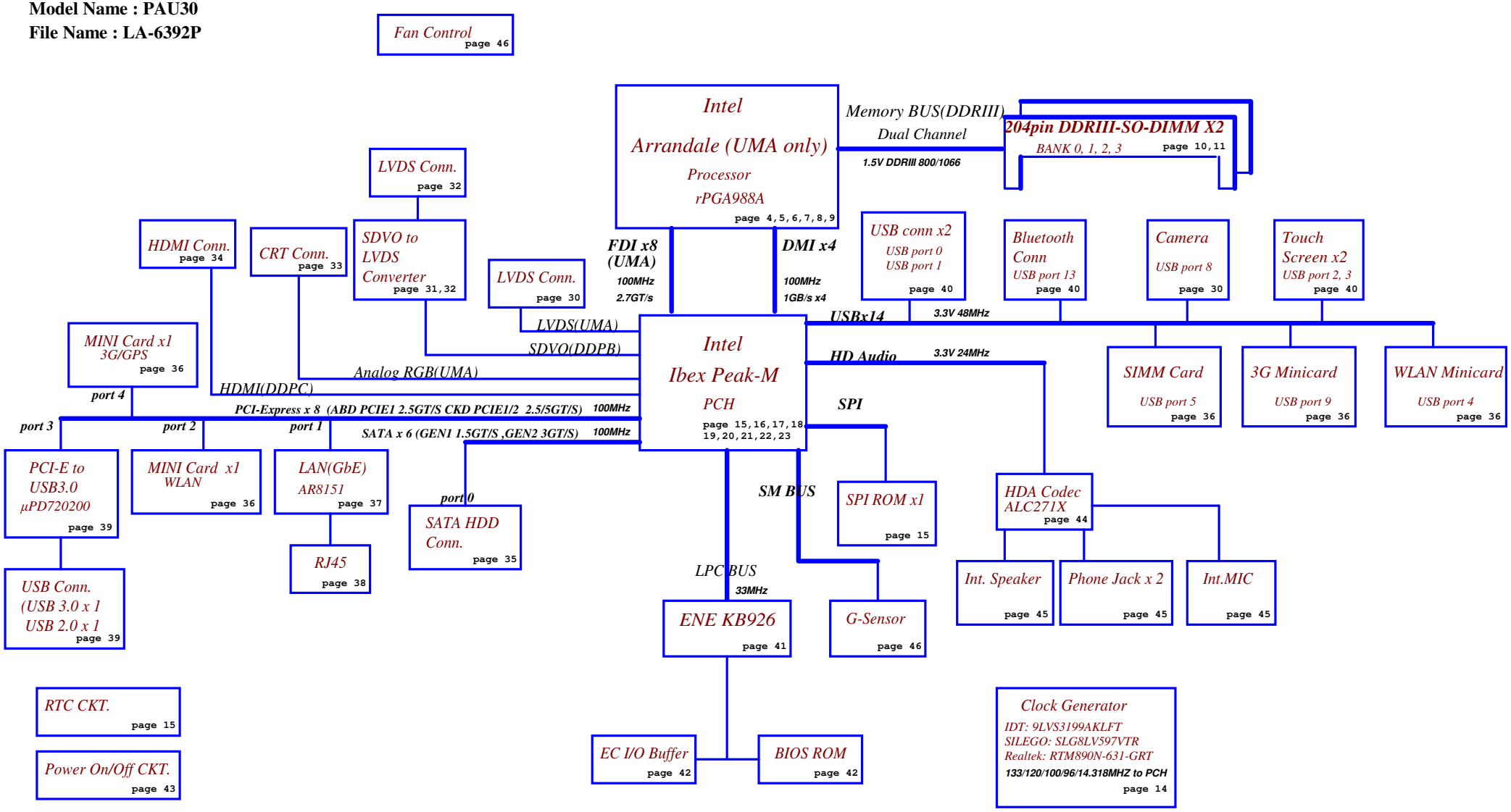
Model Name : PAU30
File Name : LA-6392P



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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

43level BOM Config

P/N	Des.	BOM Config
431954BOL01	SMT MB A6392 PAU30 W/3G	DAZ@

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
VRAM	
VRAM	X76@
Connector	CONN@
Ventura	VENTURA@
Blue Tooth	BT@
Unpop	@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/Touch Screen2
		3	USB/Touch Screen1
	UHCI2	4	Mini Card(WLAN)
		5	SIMM CARD
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Camera
		9	Mini Card(3G)
	UHCI5	10	
		11	
	UHCI6	12	
		13	Blue Tooth

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Title	Notes List		
Size B	Document Number PAU30 M/B LA-6392P Schematic		Rev 0.1
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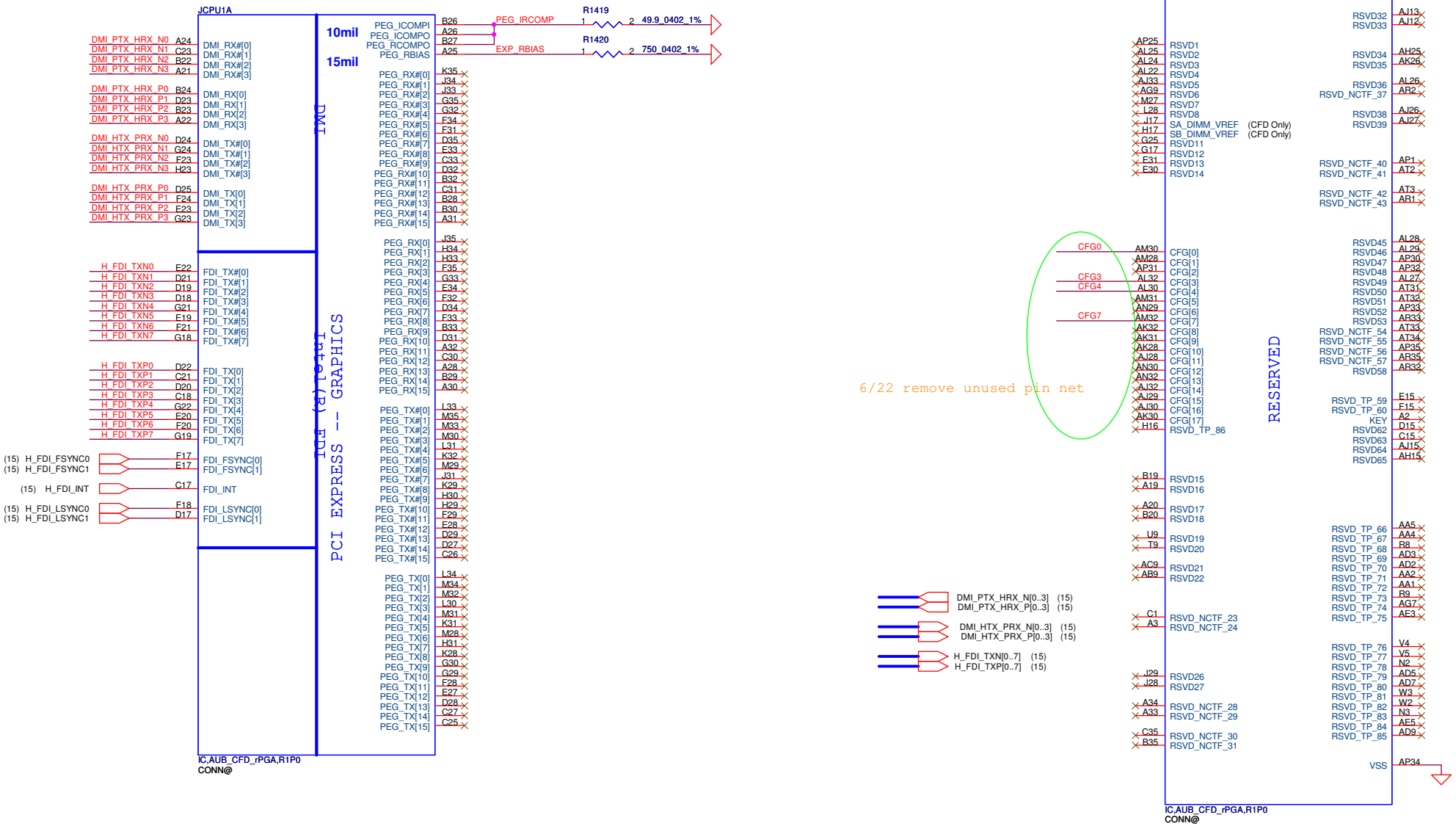

eDP Signals Mapping

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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Title: PROCESSOR (1/6) DMI,FDI,PEG

Size	Document Number	Rev
B	PAU30 M/B LA-6392P Schematic	1.0

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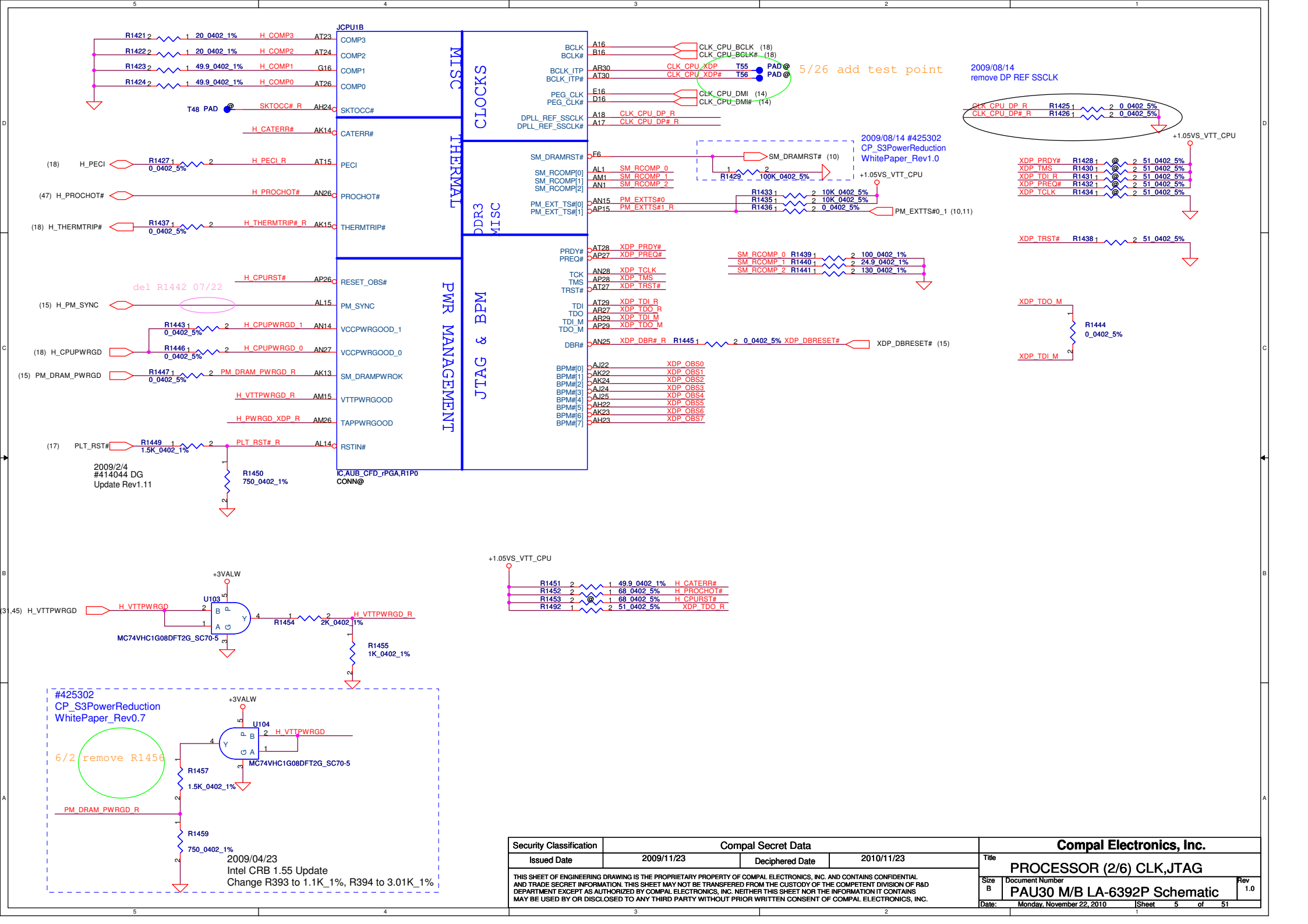

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Compal Electronics, Inc.

Title: PROCESSOR (2/6) CLK,JTAG

Size	Document Number	Rev
B	PAU30 M/B LA-6392P Schematic	1.0

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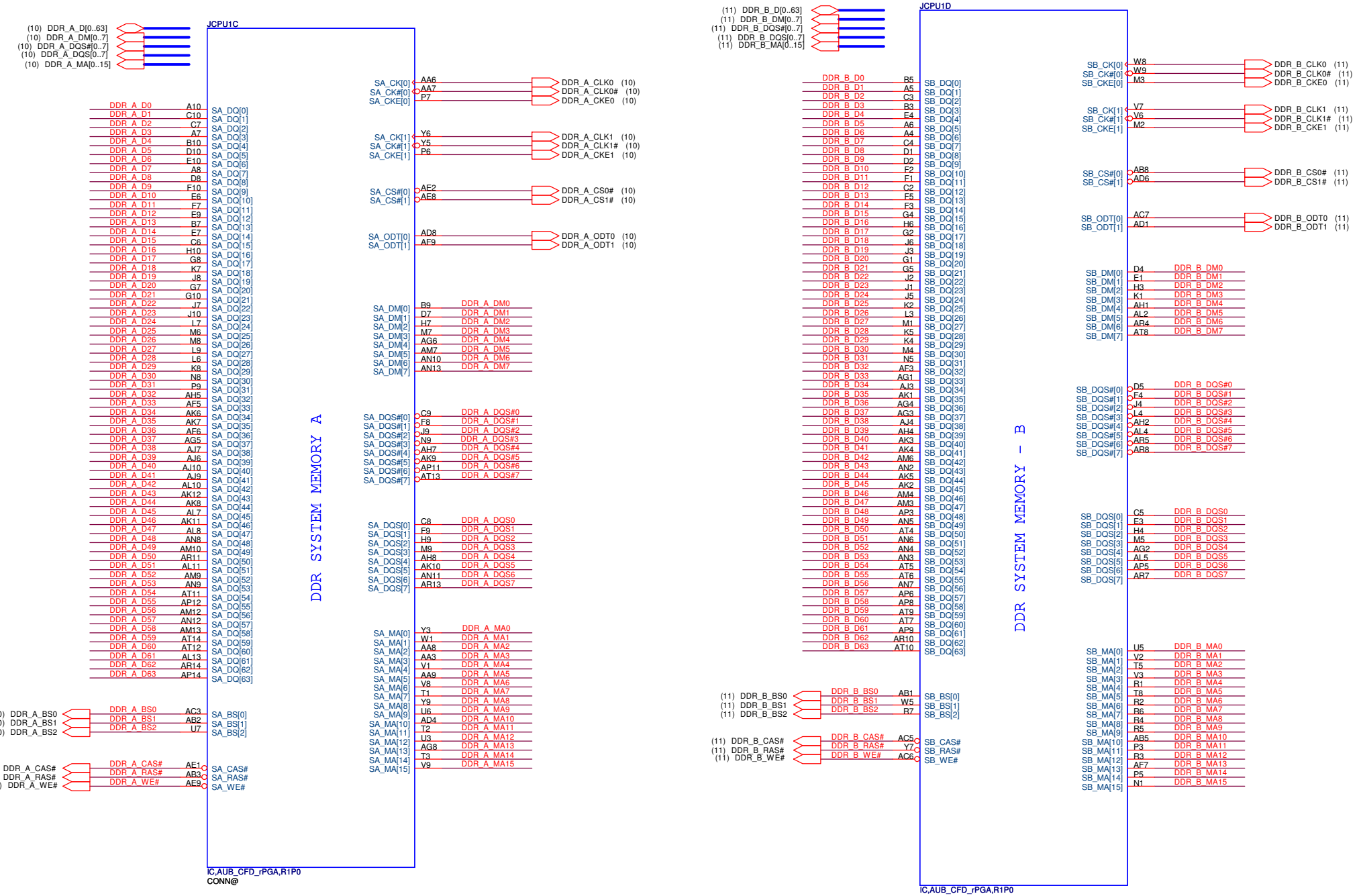

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Title: PROCESSOR (3/6) DDRIII

Size	Document Number	Rev
B	PAU30 M/B LA-6392P Schematic	1.0

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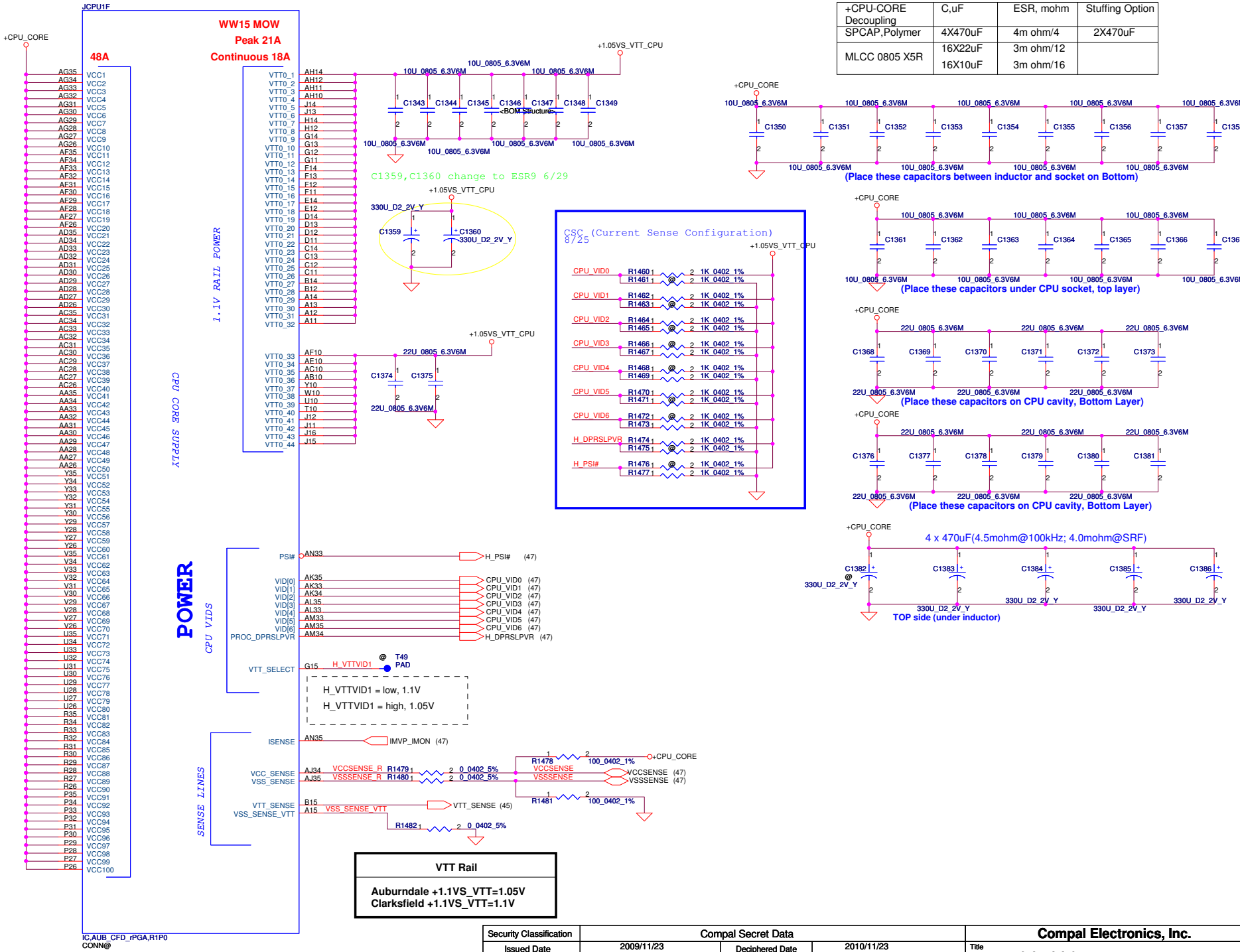

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

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Compal Electronics, Inc.

Title: PROCESSOR (4/6) PWR,Bypass

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 1.0

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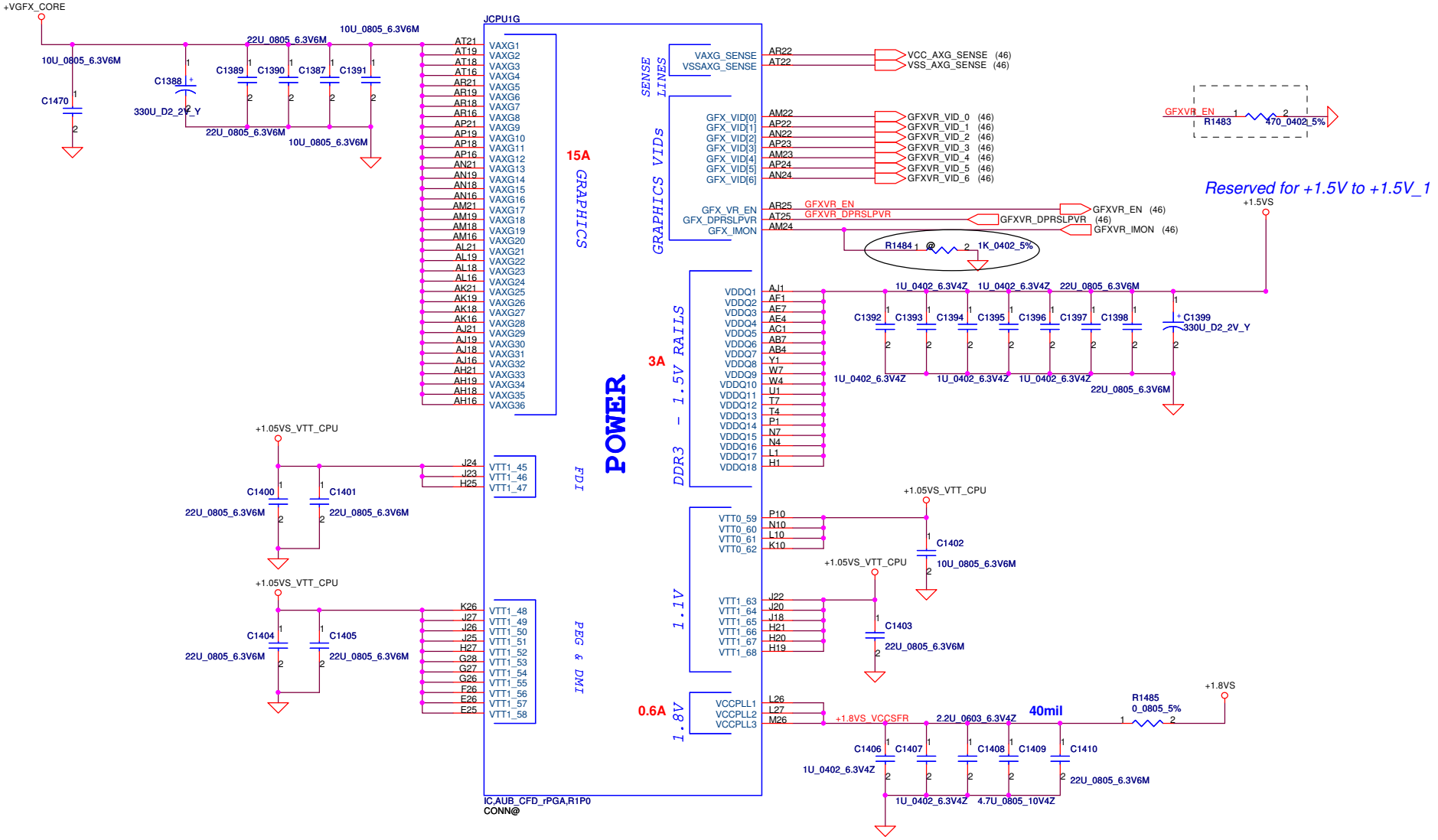

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Compal Electronics, Inc.

Title: PROCESSOR (5/6) PWR

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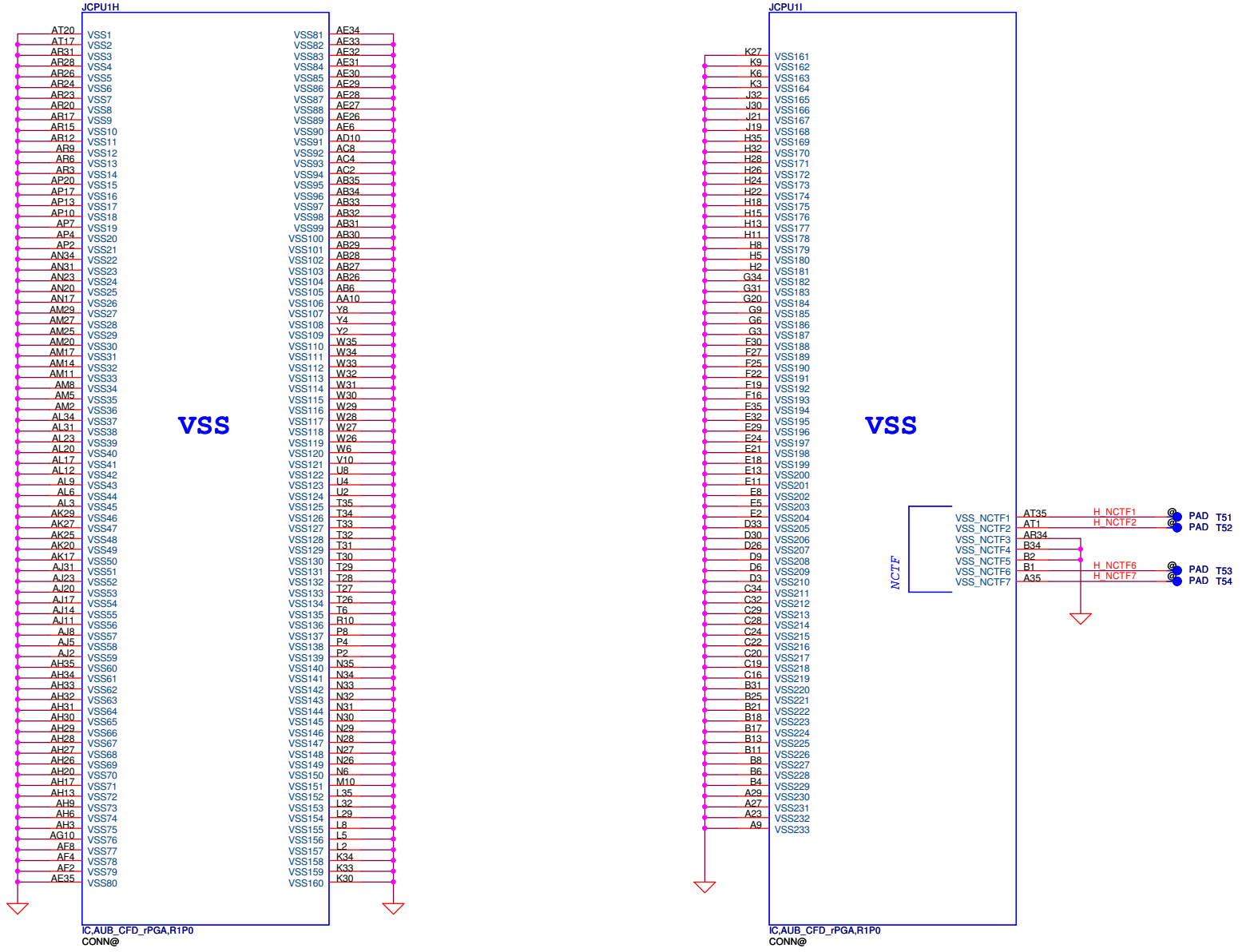

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Title: PROCESSOR (6/6) VSS

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DIMMA VREFDQ M1 Circuit

+1.5V

R1493 1K_0402_1%

+DIMM_VREFDQA

20mil

R1494 1K_0402_1%

DIMMA & DIMMB VREFCA circuit

+1.5V

R1495 1K_0402_1%

+DIMM_VREFCA

20mil

R1496 1K_0402_1%

(6) DDR_A_DQS#[0..7]

(6) DDR_A_D[0..63]

(6) DDR_A_DM[0..7]

(6) DDR_A_DQS[0..7]

(6) DDR_A_MA[0..15]

#425302
CP_S3PowerReduction
WhitePaper_Rev1.0

R1497 0_0402_5%

R1498 1K_0402_1%

Q107 BSS138LT1G_SOT23-3 <BOM Structure>

(5) SM_DRAMRST#

DIMM_DRAMRST#

DIMM_DRAMRST# (11)

(18) RST_GATE

RST_GATE

C1435 0.047U_0402_16V7K

+DIMM_VREFDQA

C1434 0.1U_0402_16V4Z

C1433 2.2U_0603_6.3V4Z

JDIMM1

		VREF_DQ	1	2	VSS1		
	DDR_A_D0	VSS2	3	4	DQ4	DDR_A_D4	
	DDR_A_D1	DQ0	5	6	DQ5	DDR_A_D5	
		DQ1	7	8	VSS3		
	DDR_A_DM0	VSS4	9	10	DQS#0	DDR_A_DQS#0	
		DM0	11	12	DQS0	DDR_A_DQS0	
	DDR_A_D2	VSS5	13	14	VSS6		
	DDR_A_D3	DQ2	15	16	DQ6	DDR_A_D6	
		DQ3	17	18	DQ7	DDR_A_D7	
	DDR_A_D8	VSS7	19	20	VSS8		
	DDR_A_D9	DQ8	21	22	DQ12	DDR_A_D12	
		DQ9	23	24	DQ13	DDR_A_D13	
	DDR_A_DQS#1	VSS9	25	26	VSS10		
	DDR_A_DQS1	DQS#1	27	28	DM1	DDR_A_DM1	
		DQS1	29	30	RESET#	DIMM_DRAMRST#	
	DDR_A_D10	VSS11	31	32	VSS12		
	DDR_A_D11	DQ10	33	34	DQ14	DDR_A_D14	
		DQ11	35	36	DQ15	DDR_A_D15	
	DDR_A_D16	VSS13	37	38	VSS14		
	DDR_A_D17	DQ16	39	40	DQ20	DDR_A_D20	
		DQ17	41	42	DQ21	DDR_A_D21	
	DDR_A_DQS#2	VSS15	43	44	VSS16		
	DDR_A_DQS2	DQS#2	45	46	DM2	DDR_A_DM2	
		DQS2	47	48	VSS17		
	DDR_A_D18	VSS18	49	50	DQ22	DDR_A_D22	
	DDR_A_D19	DQ18	51	52	DQ23	DDR_A_D23	
		DQ19	53	54	VSS19		
	DDR_A_D24	VSS20	55	56	DQ28	DDR_A_D28	
	DDR_A_D25	DQ24	57	58	DQ29	DDR_A_D29	
		DQ25	59	60	VSS21		
	DDR_A_DM3	VSS22	61	62	DQS#3	DDR_A_DQS#3	
		DM3	63	64	DQS3	DDR_A_DQS3	
	DDR_A_D26	VSS23	65	66	VSS24		
	DDR_A_D27	DQ26	67	68	DQ30	DDR_A_D30	
		DQ27	69	70	DQ31	DDR_A_D31	
		VSS25	71	72	VSS26		
(6) DDR_A_CKE0	DDR_A_CKE0	CKE0	73	74	CKE1	DDR_A_CKE1	DDR_A_CKE1 (6)
		VDD1	75	76	VDD2		
(6) DDR_A_BS2	DDR_A_BS2	NC1	77	78	A15	DDR_A_MA15	
		BA2	79	80	A14	DDR_A_MA14	
	DDR_A_MA12	VDD3	81	82	VDD4		
	DDR_A_MA9	A12/BC#	83	84	A11	DDR_A_MA11	
		A9	85	86	A7	DDR_A_MA7	
	DDR_A_MA8	VDD5	87	88	VDD6		
	DDR_A_MA5	A8	89	90	A6	DDR_A_MA6	
		A5	91	92	A4	DDR_A_MA4	
	DDR_A_MA3	VDD7	93	94	VDD8		
	DDR_A_MA1	A3	95	96	A2	DDR_A_MA2	
		A1	97	98	A0	DDR_A_MA0	
		VDD9	99	100	VDD10		
(6) DDR_A_CLK0	DDR_A_CLK0	CK0	101	102	CK1	DDR_A_CLK1	DDR_A_CLK1 (6)
(6) DDR_A_CLK0#	DDR_A_CLK0#	CK0#	103	104	CK1#	DDR_A_CLK1#	DDR_A_CLK1# (6)
		VDD11	105	106	VDD12		
	DDR_A_MA10	A10/AP	107	108	BA1	DDR_A_BS1	DDR_A_BS1 (6)
(6) DDR_A_BS0	DDR_A_BS0	BA0	109	110	RAS#	DDR_A_RAS#	DDR_A_RAS# (6)
		VDD13	111	112	VDD14		
(6) DDR_A_WE#	DDR_A_WE#	WE#	113	114	S0#	DDR_A_CS0#	DDR_A_CS0# (6)
(6) DDR_A_CAS#	DDR_A_CAS#	CAS#	115	116	ODT0	DDR_A_ODT0	DDR_A_ODT0 (6)
		VDD15	117	118	VDD16		
	DDR_A_MA13	A13	119	120	ODT1	DDR_A_ODT1	DDR_A_ODT1 (6)
(6) DDR_A_CS1#	DDR_A_CS1#	S1#	121	122	NC2		
		VDD17	123	124	VDD18		
		NCTEST	125	126	VREF_CA	DDR_VREF_CA_DIMMA	
	DDR_A_D32	VSS27	127	128	VSS28	DDR_A_D36	
	DDR_A_D33	DQ32	129	130	DQ36	DDR_A_D37	
		DQ33	131	132	DQ37		
	DDR_A_DQS#4	VSS29	133	134	VSS30		
	DDR_A_DQS4	DQS#4	135	136	DM4	DDR_A_DM4	
		DQS4	137	138	VSS31		
	DDR_A_D34	VSS32	139	140	DQ38	DDR_A_D38	
	DDR_A_D35	DQ34	141	142	DQ39	DDR_A_D39	
		DQ35	143	144	VSS33		
	DDR_A_D40	VSS34	145	146	DQ44	DDR_A_D44	
	DDR_A_D41	DQ40	147	148	DQ45	DDR_A_D45	
		DQ41	149	150	VSS35		
	DDR_A_DM5	VSS36	151	152	DQS#5	DDR_A_DQS#5	
		DM5	153	154	DQS5	DDR_A_DQS5	
	DDR_A_D42	VSS37	155	156	VSS38		
	DDR_A_D43	DQ42	157	158	DQ46	DDR_A_D46	
		DQ43	159	160	DQ47	DDR_A_D47	
	DDR_A_D48	VSS39	161	162	VSS40		
	DDR_A_D49	DQ48	163	164	DQ52	DDR_A_D52	
		DQ49	165	166	DQ53	DDR_A_D53	
	DDR_A_DQS#6	VSS41	167	168	VSS42		
	DDR_A_DQS6	DQS#6	169	170	DM6	DDR_A_DM6	
		DQS6	171	172	VSS43		
	DDR_A_D50	VSS44	173	174	DQ54	DDR_A_D54	
	DDR_A_D51	DQ50	175	176	DQ55	DDR_A_D55	
		DQ51	177	178	VSS45		
	DDR_A_D56	VSS46	179	180	DQ60	DDR_A_D60	
	DDR_A_D57	DQ56	181	182	DQ61	DDR_A_D61	
		DQ57	183	184	VSS47		
	DDR_A_DM7	VSS48	185	186	DQS#7	DDR_A_DQS#7	
		DM7	187	188	DQS7	DDR_A_DQS7	
	DDR_A_D58	VSS49	189	190	VSS50		
	DDR_A_D59	DQ58	191	192	DQ62	DDR_A_D62	
		DQ59	193	194	DQ63	DDR_A_D63	
		VSS51	195	196	VSS52		
		SA0	197	198	EVENT#	PM_EXTTS#0_1	PM_EXTTS#0_1 (5,11)
		VDDSPD	199	200	SDA	D_CK_SDATA	D_CK_SDATA (11,12,14,28,38)
		SA1	201	202	SCL	D_CK_SCLK	D_CK_SCLK (11,12,14,28,38)
		VTT1	203	204	VTT2	+0.75VS	
		G1	205	206	G2		

FOX_AS0A626-U4RN-7F

CONN@

+1.5V

+3VS

R1499 10K_0402_5%

C1449 2.2U_0603_6.3V4Z

C1450 0.1U_0402_16V4Z

R1500 10K_0402_5%

+DIMM_VREFCA

C1436 2.2U_0603_6.3V4Z

C1437 0.1U_0402_16V4Z

20mil

DDR_VREF_CA_DIMMA

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V

C1438 10U_0805_6.3V6M

C1439 10U_0805_6.3V6M

C1440 10U_0805_6.3V6M

C1441 10U_0805_6.3V6M

C1442 10U_0805_6.3V6M

C1443 10U_0805_6.3V6M

C1444 0.1U_0402_16V4Z

C1445 0.1U_0402_16V4Z

C1446 0.1U_0402_16V4Z

C1447 0.1U_0402_16V4Z

C1448 330U_D2_2V_Y

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

+0.75VS

C1451 1U_0402_6.3V4Z

C1452 1U_0402_6.3V4Z

C1453 1U_0402_6.3V4Z

C1454 1U_0402_6.3V4Z

C1455 10U_0805_6.3V6M

DDR3 SO-DIMM A
H=8mm

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Issued Date	2009/11/23	Deciphered Date	2010/11/23

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Compal Electronics, Inc.

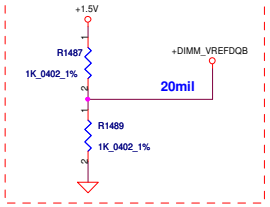
Title: DDRIII-SODIMM SLOT1

Size	Document Number	Rev
C	PAU30 M/B LA-6392P Schematic	1.0

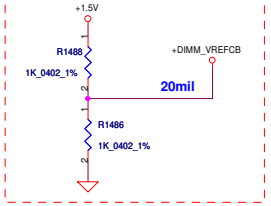
Date: Monday, November 22, 2010 Sheet 10 of 51

(6) DDR_B_DQS#[0..7]
(6) DDR_B_D[0..63]
(6) DDR_B_DM[0..7]
(6) DDR_B_DQS[0..7]
(6) DDR_B_MA[0..15]

DIMMB VREFDQ M1 Circuit

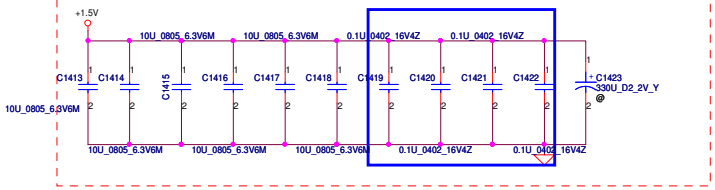


DIMMB VREFDQ CA Circuit

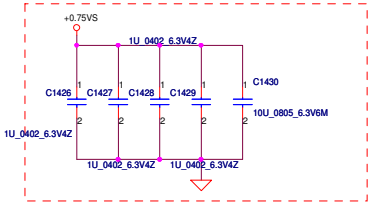


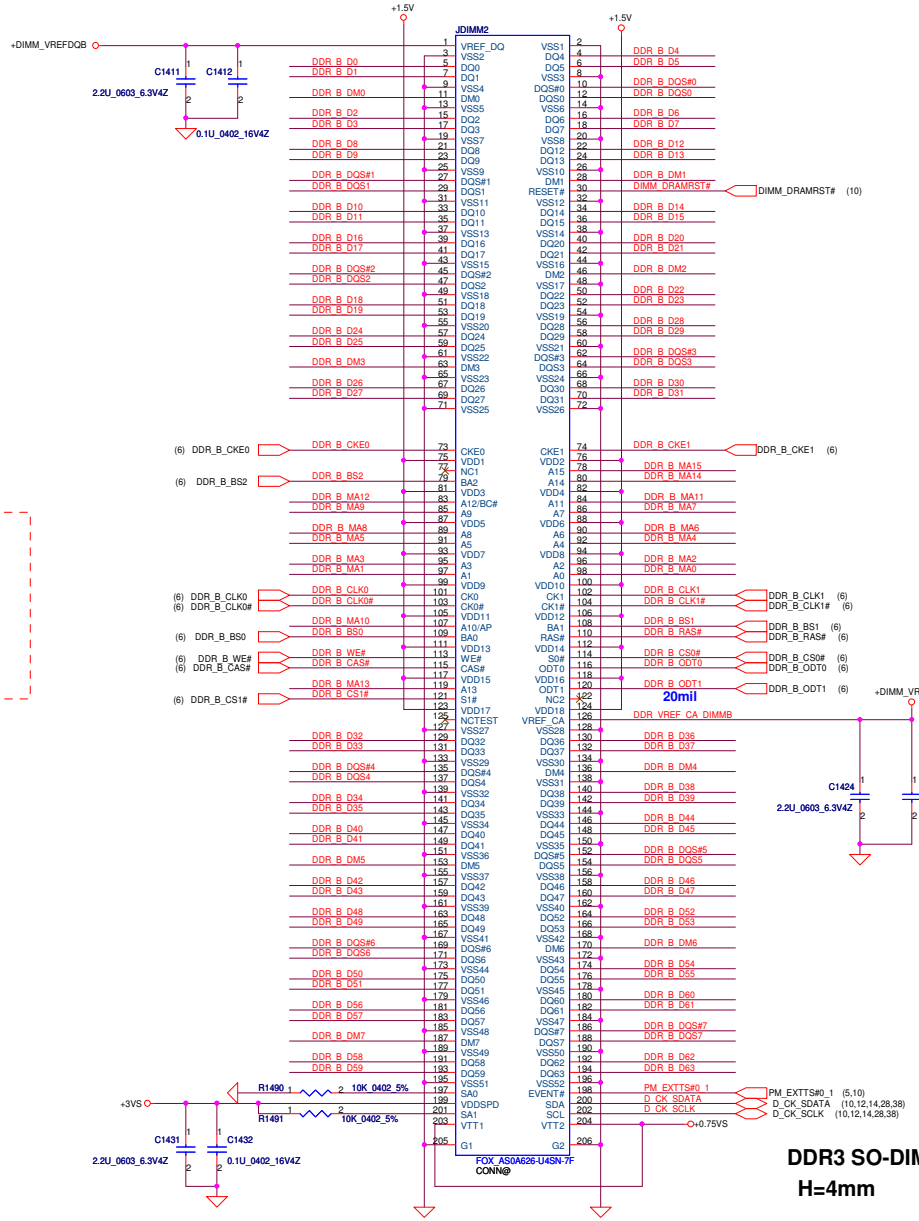
Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB



Layout Note:
Place near JDIMM2.203 & JDIMM2.204





DDR3 SO-DIMM B
H=4mm

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Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

Size	Document Number	Rev
C	PAU30 M/B LA-6392P Schematic	1.0

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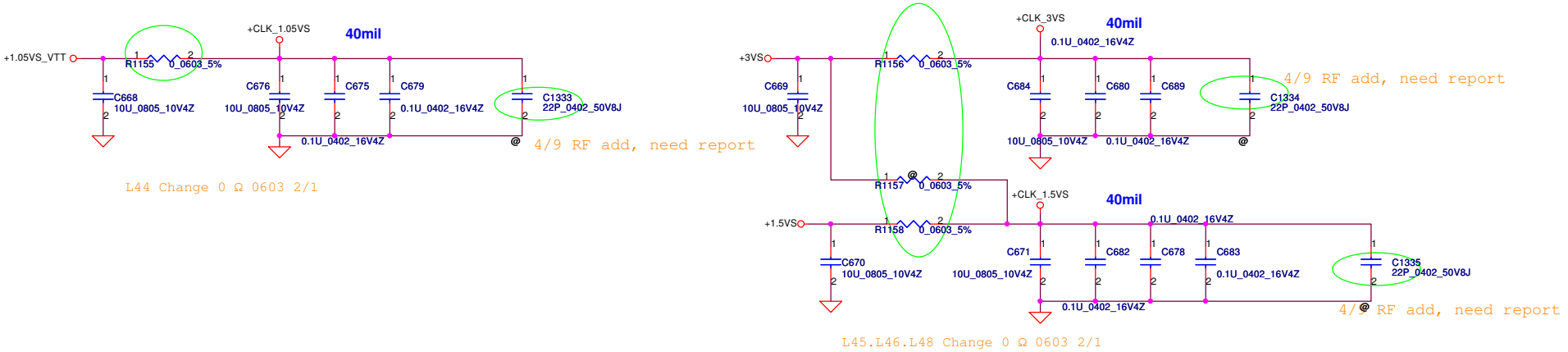
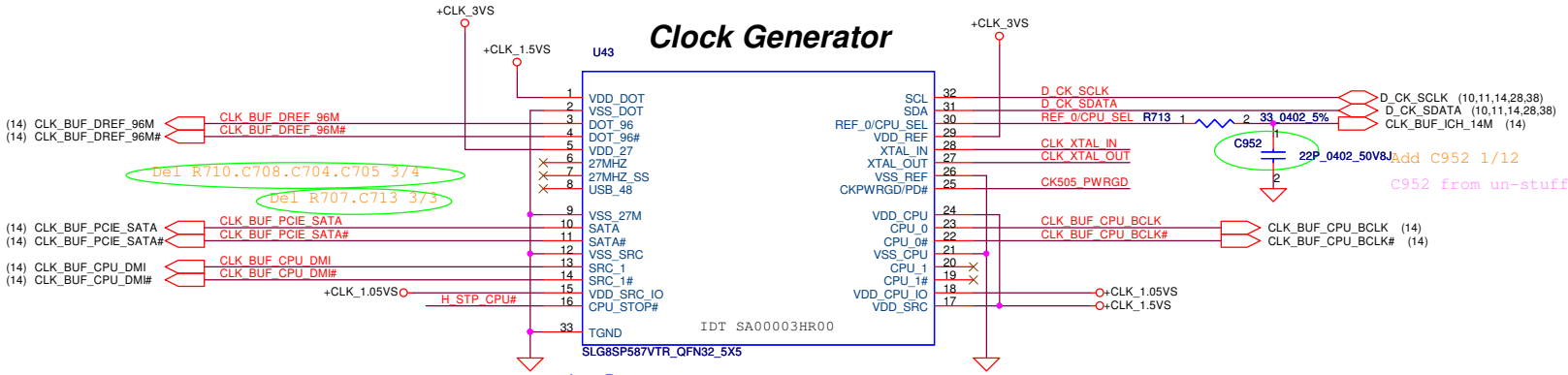


Clock Generator



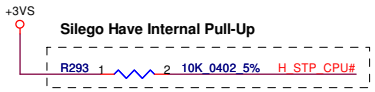
Low Power:

IDT: 9LVS3199AKLFT, SA00003HR00

Realtek: RTM890N-631-GRT, SA00003HQ00

Silego: SLG8LV597VTR , SA00003MF00

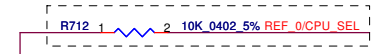
IDT 9LVS3199AKLFT NC



Silego Have Internal Pull-Up

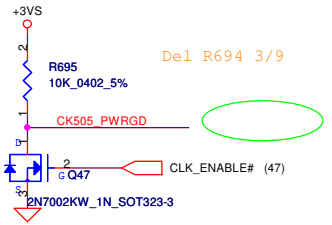
IDT Have Internal Pull-Down

FOR Realtek

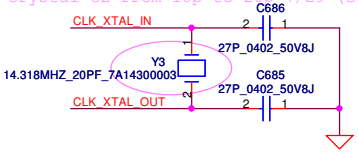


PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

Move Q50 and Q51 to PCH Side 1/12



change Crystal CL from 16p to 20p 7/29 (sourcer suggestion)



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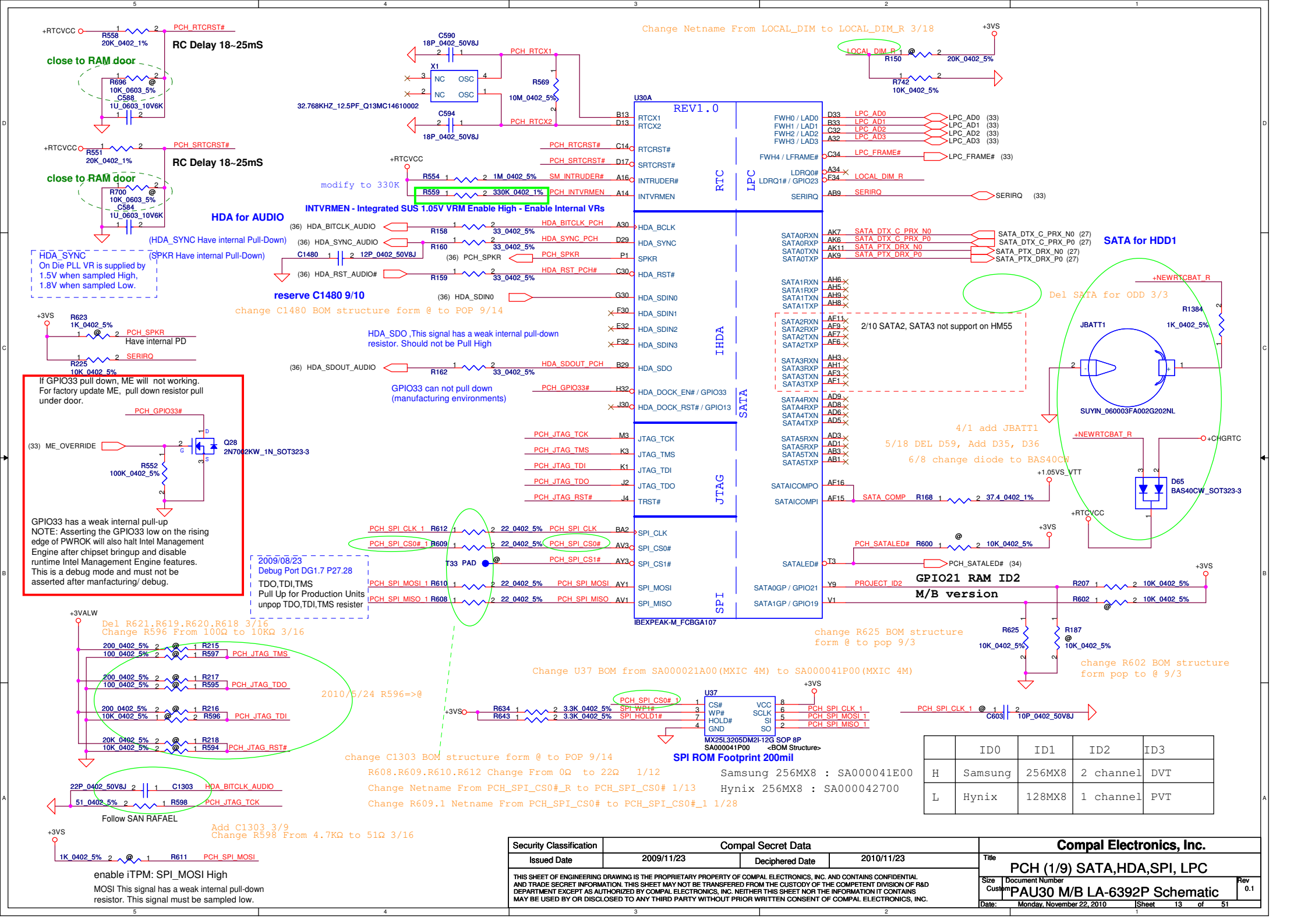
Compal Electronics, Inc.

Title: Clock Generator (CK505)

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 12 of 51



	ID0	ID1	ID2	ID3
H	Samsung	256MX8	2 channel	DVT
L	Hynix	128MX8	1 channel	PVT

Security Classification	Compal Secret Data		
Issued Date	2009/11/23	Deciphered Date	2010/11/23

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Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

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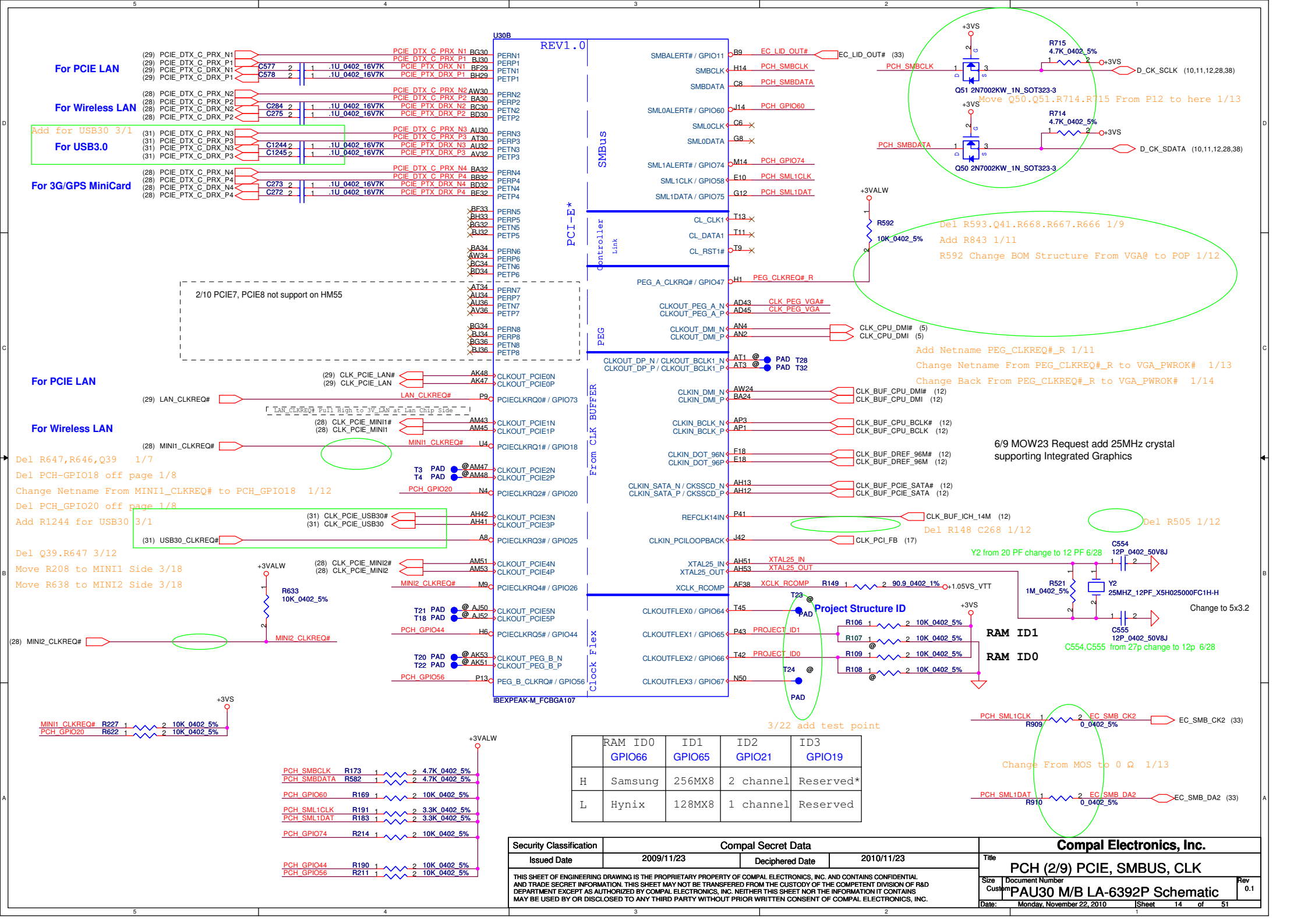

	RAM ID0 GPIO66	ID1 GPIO65	ID2 GPIO21	ID3 GPIO19
H	Samsung	256MX8	2 channel	Reserved*
L	Hynix	128MX8	1 channel	Reserved

Security Classification	Compal Secret Data		
Issued Date	2009/11/23	Deciphered Date	2010/11/23

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Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

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(4) DMI_HTX_PRX_N[0..3] DMI_HTX_PRX_N[0..3]
(4) DMI_HTX_PRX_P[0..3] DMI_HTX_PRX_P[0..3]
(4) DMI_PTX_HRX_N[0..3] DMI_PTX_HRX_N[0..3]
(4) DMI_PTX_HRX_P[0..3] DMI_PTX_HRX_P[0..3]

(4) H_FDI_TXN[0..7] H_FDI_TXN[0..7]
(4) H_FDI_TXP[0..7] H_FDI_TXP[0..7]

+3VS
@ R604 1 2 8.2K_0402_5% PM_CLKRUN#
R791 2 1 1K_0402_5% XDP_DBRESET#

+3VALW
R599 1 2 10K_0402_5% SUS_PWR_DN_ACK
R584 1 2 8.2K_0402_5% PCH_GPIO72
R178 1 2 10K_0402_5% EC_SWI#
R188 1 2 10K_0402_5% PCH_PCIE_WAKE#
@ R198 1 2 10K_0402_5% PM_SLP_LAN#

+1.05VS_VTT
R163 49.9_0402_1% 1 2 DMI_COMP

09/09/14 WW37 PCH WAKE# PU 10K

U30C

DMI_HTX_PRX_N0	BC24	DMI0RXN	
DMI_HTX_PRX_N1	BJ22	DMI1RXN	
DMI_HTX_PRX_N2	AW20	DMI2RXN	
DMI_HTX_PRX_N3	BJ20	DMI3RXN	
DMI_HTX_PRX_P0	BD24	DMI0RXP	
DMI_HTX_PRX_P1	BG22	DMI1RXP	
DMI_HTX_PRX_P2	BA20	DMI2RXP	
DMI_HTX_PRX_P3	BG20	DMI3RXP	
DMI_PTX_HRX_N0	BE22	DMI0TXN	
DMI_PTX_HRX_N1	BF21	DMI1TXN	
DMI_PTX_HRX_N2	BD20	DMI2TXN	
DMI_PTX_HRX_N3	BE18	DMI3TXN	
DMI_PTX_HRX_P0	BD22	DMI0TXP	
DMI_PTX_HRX_P1	BH21	DMI1TXP	
DMI_PTX_HRX_P2	BC20	DMI2TXP	
DMI_PTX_HRX_P3	BD18	DMI3TXP	
	BH25	DMI_ZCOMP	
	BF25	DMI_IRCOMP	

DMI

FDI_RXN0	BA18	H_FDI_TXN0	
FDI_RXN1	BH17	H_FDI_TXN1	
FDI_RXN2	BD16	H_FDI_TXN2	
FDI_RXN3	BJ16	H_FDI_TXN3	
FDI_RXN4	BA16	H_FDI_TXN4	
FDI_RXN5	BE14	H_FDI_TXN5	
FDI_RXN6	BA14	H_FDI_TXN6	
FDI_RXN7	BC12	H_FDI_TXN7	
FDI_RXP0	BB18	H_FDI_TXP0	
FDI_RXP1	BF17	H_FDI_TXP1	
FDI_RXP2	BC16	H_FDI_TXP2	
FDI_RXP3	BG16	H_FDI_TXP3	
FDI_RXP4	AW16	H_FDI_TXP4	
FDI_RXP5	BD14	H_FDI_TXP5	
FDI_RXP6	BB14	H_FDI_TXP6	
FDI_RXP7	BD12	H_FDI_TXP7	
FDI_INT	BJ14	H_FDI_INT (4)	
FDI_FSYNC0	BF13	H_FDI_FSYNC0 (4)	
FDI_FSYNC1	BH13	H_FDI_FSYNC1 (4)	
FDI_LSYNC0	BJ12	H_FDI_LSYNC0 (4)	
FDI_LSYNC1	BG14	H_FDI_LSYNC1 (4)	

FDI

REV1.0

System Power Management

(5) XDP_DBRESET#	XDP_DBRESET#	T6	SYS_RESET#
	SYS_PWROK	M6	SYS_PWROK
	PWROK	B17	PWROK
3/22 add R1358	R1358 1 2 0_0402_5% MEPWROK	K5	MEPWROK
	LAN_RST#	A10	LAN_RST#
(5) PM_DRAM_PWRGD		D9	DRAMPWROK
	PCH_RSMRST#	C16	RSMRST#
(33) SUS_PWR_DN_ACK	SUS_PWR_DN_ACK	M1	SUS_PWR_DN_ACK / GPIO30
+3VALW @ R230 10K_0402_5% (33) PBTN_OUT#	PBTN_OUT#	P5	PWRBTN#
(33) EC_ACIN R908 2 1 0_0402_5%	PCH_ACIN	P7	ACPRESENT / GPIO31
	PCH_GPIO72	A6	BATLOW# / GPIO72
(33) EC_SWI#	EC_SWI#	F14	RI#

WAKE#	J12	PCH_PCIE_WAKE#	PCH_PCIE_WAKE# (28,29,31)
CLKRUN# / GPIO32	Y1	PM_CLKRUN#	R1371 1K_0402_5%
SUS_STAT# / GPIO61	P8	PCH_GPIO61 @	PAD T7
SUSCLK / GPIO62	F3	PCH_GPIO62 @	PAD T31
SLP_S5# / GPIO63	E4		PM_SLP_S5# (33)
SLP_S4#	H7		PM_SLP_S4# (33)
SLP_S3#	P12		PM_SLP_S3# (33)
SLP_M#	K8	PM_SLP_M# @	PAD T8
TP23	N2	PM_SLP_DSW# @	PAD T29
PMSYNCH	BJ10		H_PM_SYNC (5)
SLP_LAN# / GPIO29	F6	PM_SLP_LAN#	

IBEXPEAK-M_FCBGA107

Change D24 to 0Ω 1/12

Change From +3V to +3VALW 1/8

R645 2 1 @ 0_0402_5%
Q38 MMBT3906_SOT23-3
PCH_RSMRST# 1 3 EC_RSMRST# (33)
R656 10K_0402_5%
R644 1 2 4.7K_0402_5% +3VALW
D27A BAV99DW-7_SOT363
D27B BAV99DW-7_SOT363
R655 2.2K_0402_5%

PWROK R1348 1 2 22_0402_5%
Add R911 1/13
Add R1348 3/18
SYS_PWROK R911 1 2 22_0402_5% PWROK_R

+3VS
U40
MC74VHC1G08DFT2G_SC70-5
EC_PWROK EC_PWROK (33)
VGATE VGATE (47)

4/15 change pull down connect to PWROK_R

PWROK_R R181 1 2 10K_0402_5%
EC_PWROK R676 1 2 10K_0402_5%
LAN_RST# R184 1 2 10K_0402_5%

No used Integrated LAN,
connecting LAN_RST# to GND

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Compal Electronics, Inc.

Title: PCH (3/9) DMI, FDI, PM

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

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IGPU_BKLT_EN Pull down 100K at EC Side

PCH_ENVDD Pull down 100k at JLVDS1 Side

PCH_LCD_CLK and PCH_LCD_DATA Pull high 4.7K at JLVDS1 Side

U30D

IGPU_BKLT_EN T48 L_BKLTEN
(22) PCH_ENVDD T47 L_VDD_EN
(22) DPST_PWM Y48 L_BKLTCTL
(22) PCH_LCD_CLK PCH_LCD_CLK AB48 L_DDC_CLK
(22) PCH_LCD_DATA PCH_LCD_DATA Y45 L_DDC_DATA
LCTLA_CLK AB46 L_CTRL_CLK
LCTLB_DATA V48 L_CTRL_DATA
R145 2.37K_0402_1% LVDS_IBG AP39 LVD_IBG
AP41 LVD_VBG
R141 0_0402_5% LVD_VREF AT43 LVD_VREFH
AT42 LVD_VREFL

(22) PCH_TXCLK- PCH_TXCLK- AV53 LVDSA_CLK#
(22) PCH_TXCLK+ PCH_TXCLK+ AV51 LVDSA_CLK
(22) PCH_TXOUT0- PCH_TXOUT0- BB47 LVDSA_DATA#0
(22) PCH_TXOUT1- PCH_TXOUT1- BA52 LVDSA_DATA#1
(22) PCH_TXOUT2- PCH_TXOUT2- AY48 LVDSA_DATA#2
AV47 LVDSA_DATA#3
(22) PCH_TXOUT0+ PCH_TXOUT0+ BB48 LVDSA_DATA0
(22) PCH_TXOUT1+ PCH_TXOUT1+ BA50 LVDSA_DATA1
(22) PCH_TXOUT2+ PCH_TXOUT2+ AY49 LVDSA_DATA2
AV48 LVDSA_DATA3
AP48 LVDSB_CLK#
AP47 LVDSB_CLK
AY53 LVDSB_DATA#0
AT49 LVDSB_DATA#1
AU52 LVDSB_DATA#2
AT53 LVDSB_DATA#3
AY51 LVDSB_DATA0
AT48 LVDSB_DATA1
AU50 LVDSB_DATA2
AT51 LVDSB_DATA3

LVDS

(25) PCH_CRT_B PCH_CRT_B AA52 CRT_BLUE
(25) PCH_CRT_G PCH_CRT_G AB53 CRT_GREEN
(25) PCH_CRT_R PCH_CRT_R AD53 CRT_RED
(25) PCH_CRT_CLK PCH_CRT_CLK V51 CRT_DDC_CLK
(25) PCH_CRT_DATA PCH_CRT_DATA V53 CRT_DDC_DATA
R974 22_0402_5% PCH_CRT_HSYNC_R Y53 CRT_HSYNC
R975 22_0402_5% PCH_CRT_VSYNC_R Y51 CRT_VSYNC
CRT_IREF AD48 DAC_IREF
AB51 CRT_IRTN

CRT

Digital Display Interface

SDVO_TVCLKINN BJ46
SDVO_TVCLKINP BG46
SDVO_STALLN BJ48 → SDVOB_STALL- (24)
SDVO_STALLP BG48 → SDVOB_STALL+ (24)
SDVO_INTN BF45
SDVO_INTP BH45
SDVO_CTRLCLK T51 SDVOB_SCLK → SDVOB_SCLK (24)
SDVO_CTRLDATA T53 SDVOB_SDATA → SDVOB_SDATA (24)
DDPB_AUXN BG44
DDPB_AUXP BJ44
DDPB_HPD AU38 → @ T42 PAD
DDPB_0N BD42 DDPB_0N C1004 .1U_0402_16V7K → SDVOB_R- (24)
DDPB_0P BC42 DDPB_0P C1005 .1U_0402_16V7K → SDVOB_R+ (24)
DDPB_1N BJ42 DDPB_1N C1006 .1U_0402_16V7K → SDVOB_G- (24)
DDPB_1P BG42 DDPB_1P C1007 .1U_0402_16V7K → SDVOB_G+ (24)
DDPB_2N BB40 DDPB_2N C1008 .1U_0402_16V7K → SDVOB_B- (24)
DDPB_2P BA40 DDPB_2P C1009 .1U_0402_16V7K → SDVOB_B+ (24)
DDPB_3N AW38 DDPB_3N C1010 .1U_0402_16V7K → SDVOB_CLK- (24)
DDPB_3P BA38 DDPB_3P C1011 .1U_0402_16V7K → SDVOB_CLK+ (24)

4/13 add test point

DDPC_CTRLCLK Y49 DDPC_SCLK → DDPC_SCLK (26)
DDPC_CTRLDATA AB49 DDPC_SDATA → DDPC_SDATA (26)
DDPC_AUXN BE44
DDPC_AUXP BD44
DDPC_HPD AV40 → PCH_DPC_HPD (26)
DDPC_0N BE40 DDPC_0N C1078 .1U_0402_16V7K → PCH_TMDS_D2# (26)
DDPC_0P BD40 DDPC_0P C1014 .1U_0402_16V7K → PCH_TMDS_D2 (26)
DDPC_1N BF41 DDPC_1N C1028 .1U_0402_16V7K → PCH_TMDS_D1# (26)
DDPC_1P BH41 DDPC_1P C1065 .1U_0402_16V7K → PCH_TMDS_D1 (26)
DDPC_2N BD38 DDPC_2N C1068 .1U_0402_16V7K → PCH_TMDS_D0# (26)
DDPC_2P BC38 DDPC_2P C1070 .1U_0402_16V7K → PCH_TMDS_D0 (26)
DDPC_3N BB36 DDPC_3N C1071 .1U_0402_16V7K → PCH_TMDS_CK# (26)
DDPC_3P BA36 DDPC_3P C1075 .1U_0402_16V7K → PCH_TMDS_CK (26)

DDPD_CTRLCLK U50
DDPD_CTRLDATA U52
DDPD_AUXN BC46
DDPD_AUXP BD46
DDPD_HPD AT38
DDPD_0N BJ40
DDPD_0P BG40
DDPD_1N BJ38
DDPD_1P BG38
DDPD_2N BF37
DDPD_2P BH37
DDPD_3N BE36
DDPD_3P BD36

REV1.0

iBEXPEAK-M_FCBGA107

+3VS

Del R116 R119 1/13

R117 10K_0402_5% LCTLA_CLK
R118 10K_0402_5% LCTLB_DATA
R517 2.2K_0402_5% PCH_CRT_CLK
R518 2.2K_0402_5% PCH_CRT_DATA
R1048 4.7K_0402_5% SDVOB_SCLK
R1049 4.7K_0402_5% SDVOB_SDATA

Change R1048.R1049 From 2.2KΩ to 4.7KΩ 1/18

R511 150_0402_1% PCH_CRT_B
R512 150_0402_1% PCH_CRT_G
R513 150_0402_1% PCH_CRT_R

close to PCH

Add R974.R975 1/14

(33) ENBKL ENBKL R112 0_0402_5% IGPU_BKLT_EN

R135 1K_0402_0.5%

2/3 Change to 1K_0402_0.5% from Intel Suggestion. (EDS 1.0 is incorrect)

Del U11.C230.R115.R126 1/7

Configuration Wise Pin Mapping for DDI Ports

	DDI PCH Pin Names	SDVO Mapping	HDMI/DVI Mapping	DisplayPort Mapping
PORT B	DDPB_[0]P	SDVO_RED	TMDSB_DATA2	DDPB_[0]P
	DDPB_[0]N	SDVO_RED#	TMDSB_DATA2#	DDPB_[0]N
	DDPB_[1]P	SDVO_GREEN	TMDSB_DATA1	DDPB_[1]P
	DDPB_[1]N	SDVO_GREEN#	TMDSB_DATA1#	DDPB_[1]N
	DDPB_[2]P	SDVO_BLUE	TMDSB_DATA0	DDPB_[2]P
	DDPB_[2]N	SDVO_BLUE#	TMDSB_DATA0#	DDPB_[2]N
	DDPB_[3]P	SDVO_CLK	TMDSB_CLK	DDPB_[3]P
	DDPB_[3]N	SDVO_CLK#	TMDSB_CLK#	DDPB_[3]N
	DDPB_AUXP	NA	NA	DDPB_AUXP
	DDPB_AUXN	NA	NA	DDPB_AUXN
	DDPB_HPD	NA	HDMIB_HPD	DDPB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	HDMIB_CTRLCLK	NA
	SDVO_CTRLDATA	SDVO_CTRLDATA	HDMIB_CTRLDATA	NA

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Issued Date	2009/11/23	Deciphered Date	2010/11/23

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Compal Electronics, Inc.

Title: PCH (4/9) LVDS, CRT, DPI

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 16 of 51

U30E

REV1.0

PCI_GNT[0:3]# has a weak internal pull-up

change netname PCI_PIRQE# to G_SENSOR_G

change netname PCI_PIRQG# to TOUCH_PANEL_INT2#

change netname PCI_PIRQF# to TOUCH_PANEL_INT1#

1/7

3/25 add T15

PCI_GNT2# ESI Strap (Server Only)

this signal should not be pulled low

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

2008/1/6 2009MOW01 change to 22 ohm

Add C953 1/13 RF Recommand

4/1 add two pull up resistors

Del R607 1/27

3/22 USB port0

4/8 change control board 2 to USB port 2

USB Conn. (Left Side)

USB Conn. (Left Side)

USB/Touch Screen2

USB/Touch Screen1

Mini Card 1(WLAN)

SIMM Card

6/3 DEL USB port3

EHCI 1 (Device 29)

Change usb port 1/8

2/10 USB6, USB7 not support on HM55

CMOS Camera (LVDS)

Mini Card 2 (3G/GPS)

Change Touch screen1 form USB port10 to port3 08/24

EHCI 2 (Device 26)

Del USB Port12 3/3

Bluetooth

Del R167 1/7

(For USB CONN) 1/8

(For USB 2.0 &3.0 Conn.) 3/3

OC[0..3] use for EHCI 1

OC[4..7] use for EHCI 2

Change Netname From USB_OC#x_R to USB_OC#x 1/14

6/9 add +3VALW path, reserve +3VS

4/13 add 1410

Change R614 From 0 to 22 Ohm 1/13

R614 and R590 Swap Position 1/13

NV_ALE

Enable Intel Anti-Theft Technology : 8.2K PU to +NVRAM_VCCQ

Disable Intel Anti-Theft Technology : floating(internal PD)

NV_CLE

DMI termination voltage. weak internal PU, don't PD

Del USB_OC#2_R to PCH XDP 1/7

change R1385.R1396 from 10k to 4.7k 8/2

R640 Move From P.36 to here

A16 swap overide Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default ★

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Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, VRAM

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 17 of 51

3/22 R543, R546

Change Netname From DGPU_EDIDSEL# to GPIO0 3/18

+3VS

R539 10K_0402_5% GPIO1

R603 10K_0402_5% COLOR_ENG_EN
R224 10K_0402_5% VGA_PRSNT_L#
R605 10K_0402_5% PCH_TEMP_ALERT#
R226 10K_0402_5% PCH_GPIO22
R209 10K_0402_5% PCH_GPIO39

Del R144 3/9

R206 10K_0402_5% PCH_GPIO48
R205 @ 10K_0402_5% DGPU_PWR_EN
R228 10K_0402_5% PCH_GPIO34

+3VALW

change R189 from 10k to 4.7k 8/2

R189 4.7K_0402_5% PCH_GPIO12
R229 1K_0402_5% PCH_GPIO15
10/7 Not Use PCH_GPIO15 PU 1K to +3V
R182 @ 10K_0402_5% PCH_GPIO24
R210 10K_0402_5% PCH_GPIO28
R197 10K_0402_5% PCH_GPIO57
R589 10K_0402_5% PCH_GPIO45
R586 10K_0402_5% RST_GATE

R223 @ 10K_0402_5% VGA_PRSNT_L#
R606 10K_0402_5% DGPU_HOLD_RST#
R725 10K_0402_5% DGPU_PWR_EN
R180 10K_0402_5% PCH_GPIO35
R204 @ 10K_0402_5% PCH_GPIO27

GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

CRT_DET Reserve Pull high to +3VS at U99 side

Del R143 1/14

(33) PCH_CRT_DET — PCH_CRT_DET — Y3 BMBUSY# / GPIO0
GPIO1 — C38 TACH1 / GPIO1
(33) PCH_HDMI_HPD_INT# — PCH_HDMI_HPD_INT# — D37 TACH2 / GPIO6
(33) EC_SCI# — EC_SCI# — J32 TACH3 / GPIO7
(33) EC_SMI# — EC_SMI# — F10 GPIO8
(31) PCH_GPIO12 — PCH_GPIO12 — K9 LAN_PHY_PWR_CTRL / GPIO12
(GPIO15 Have Internal Pull Down) — PCH_GPIO15 — T7 GPIO15
DGPU_HOLD_RST# — AA2 SATA4GP / GPIO16
(35) VGA_PWROK_R — VGA_PWROK_R — F38 TACH0 / GPIO17
2009/09/07 GPIO24 pull high +3V
PCH_GPIO22 — Y7 SCLOCK / GPIO22
PCH_GPIO24 — H10 GPIO24
(GPIO27 Have Internal Pull High)
PCH_GPIO27 — AB12 GPIO27
Del off page 1/8
PCH_GPIO28 — V13 GPIO28
PCH_GPIO34 — M11 STP_PCI# / GPIO34
DGPU_PWR_EN Pull Down at Page 47
PCH_GPIO35 — V6 SATACLKREQ# / GPIO35
DGPU_PWR_EN — AB7 SATA2GP / GPIO36
VGA_PRSNT_L# — AB13 SATA3GP / GPIO37
COLOR_ENG_EN — V3 SLOAD / GPIO38
PCH_GPIO39 — P3 SDATAOUT0 / GPIO39
PCH_GPIO45 — H3 PCIECLKRQ6# / GPIO45
(10) RST_GATE — RST_GATE — F1 PCIECLKRQ7# / GPIO46
PCH_GPIO48 — AB6 SDATAOUT1 / GPIO48
(33) PCH_TEMP_ALERT# — AA4 SATA5GP / GPIO49
PCH_GPIO57 — F8 GPIO57

Del VGA_PRSNT_L# off page 1/8

Del R626 3/18

U30F

MISC: BMBUSY# / GPIO0, TACH1 / GPIO1, TACH2 / GPIO6, TACH3 / GPIO7, GPIO8, LAN_PHY_PWR_CTRL / GPIO12

GPIO: GPIO15, SATA4GP / GPIO16, TACH0 / GPIO17, SCLOCK / GPIO22, GPIO24, GPIO27, GPIO28, STP_PCI# / GPIO34, SATACLKREQ# / GPIO35, SATA2GP / GPIO36, SATA3GP / GPIO37, SLOAD / GPIO38, SDATAOUT0 / GPIO39, PCIECLKRQ6# / GPIO45, PCIECLKRQ7# / GPIO46, SDATAOUT1 / GPIO48, SATA5GP / GPIO49, GPIO57

CPU: CLKOUT_PCIE6N AH45, CLKOUT_PCIE6P AH46, CLKOUT_PCIE7N AF48, CLKOUT_PCIE7P AF47, A20GATE U2 — EC_GA20 — EC_GA20 (33), CLKOUT_BCLK0_N / CLKOUT_PCIE8N AM3 — CLK_CPU_BCLK# (5), CLKOUT_BCLK0_P / CLKOUT_PCIE8P AM1 — CLK_CPU_BCLK (5), PECI BG10 — H_PECI (5), RCIN# T1 — EC_KBRST# — EC_KBRST# (33), PROCPWRGD BE10 — H_CPUPWRGD (5), THRMTRIP# BD10 — THRMTRIP_PCH# — R175 2 1 56_0402_5% — H_THERMTRIP# — H_THERMTRIP# (5); R174 2 1 56_0402_5% — +1.05VS_VTT

2009/08/23
Series resistor of 56±5%
Pull-up of 56±5% to VTT
(both these should be close to PCH)

TP1 BA22, TP2 AW22, TP3 BB22, TP4 AY45, TP5 AY46, TP6 AV43, TP7 AV45, TP8 AF13, TP9 M18, TP10 N18, TP11 AJ24, TP12 AK41, TP13 AK42, TP14 M32, TP15 N32, TP16 M30, TP17 N30, TP18 H12, TP19 AA23, NC_1 AB45, NC_2 AB38, NC_3 AB42, NC_4 AB41, NC_5 T39, INIT3_3V# P6, TP24 C10

NCTF: VSS_NCTF_1 A4 … VSS_NCTF_31 E53

RSVD

IBEXPEAK-M_FCBGA107

REV1.0

INIT3_3V
This signal has weak internal PH, can't pull low

2009/08/23
(Have internal PH,Do not pull down)

Del T27 1/14

Move R601.R624 to EC side 3/18

MAINPWON (41,42)

R570 @330_0402_5% — +1.05VS_VTT — Q33 2SC2411K_SOT23-3 @ — H_THERMTRIP#

Move R192.R153.R605 to EC side 3/18
Move R205 to Page.47 3/18
Move R124 to Page.43 3/18

VGA_PRSNT_L#	
GPIO37	Structure
0	DIS/OPT/SG
* 1	UMA Only

GPIO8
This signal has a weak internal pull up can't Pull low

GPIO27
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

Note: the internal pull-up is disabled after RSMRST# de-asserts. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.

GPIO15
* L : Intel ME Crypto Transport Layer Security(TLS) chiper suite with no confidentiality
H : Intel ME Crypto Transport Layer Security(TLS) chiper suite with confidentiality

CRB has a 1-k pull-up on this signal to +3.3VA rail.

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Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

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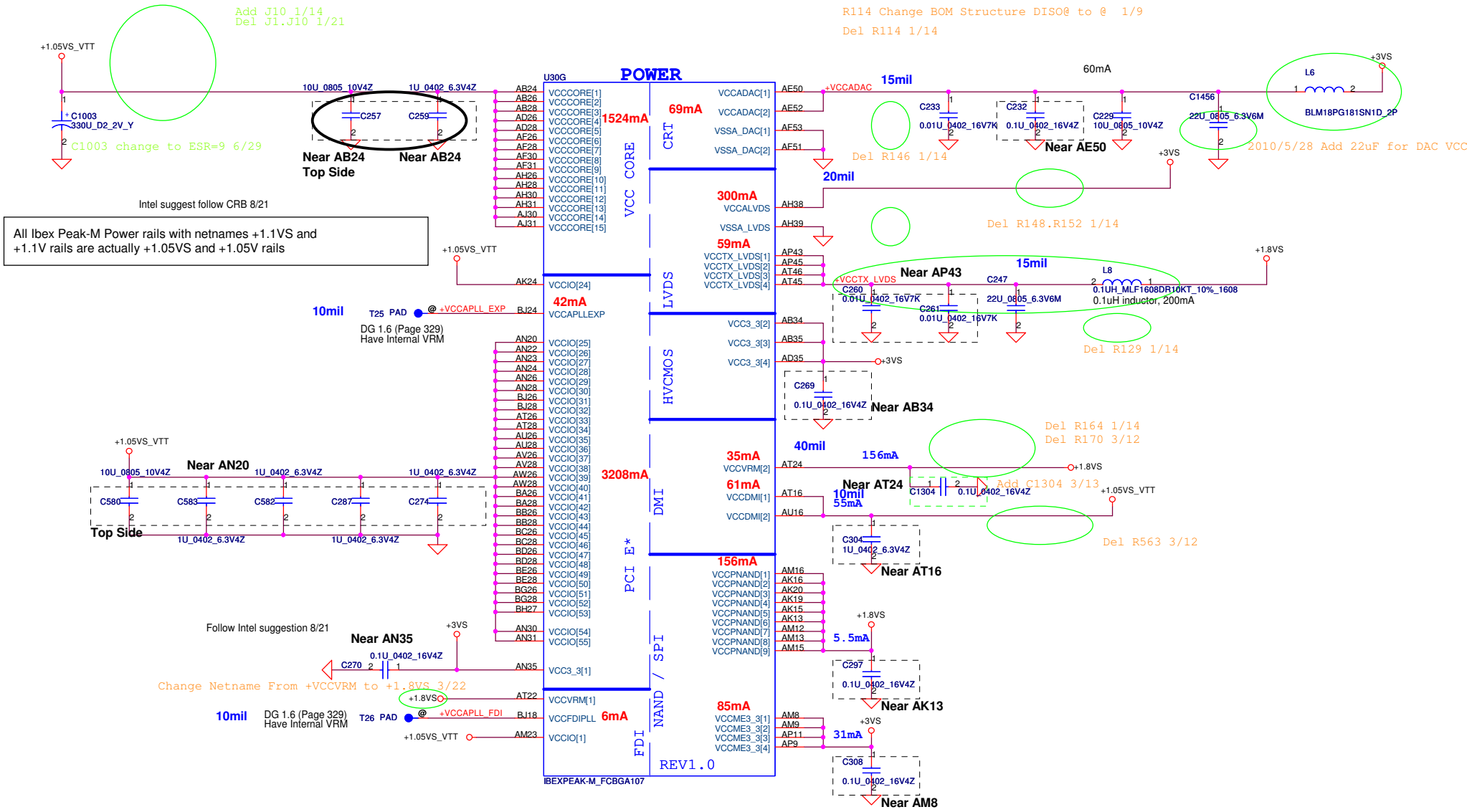

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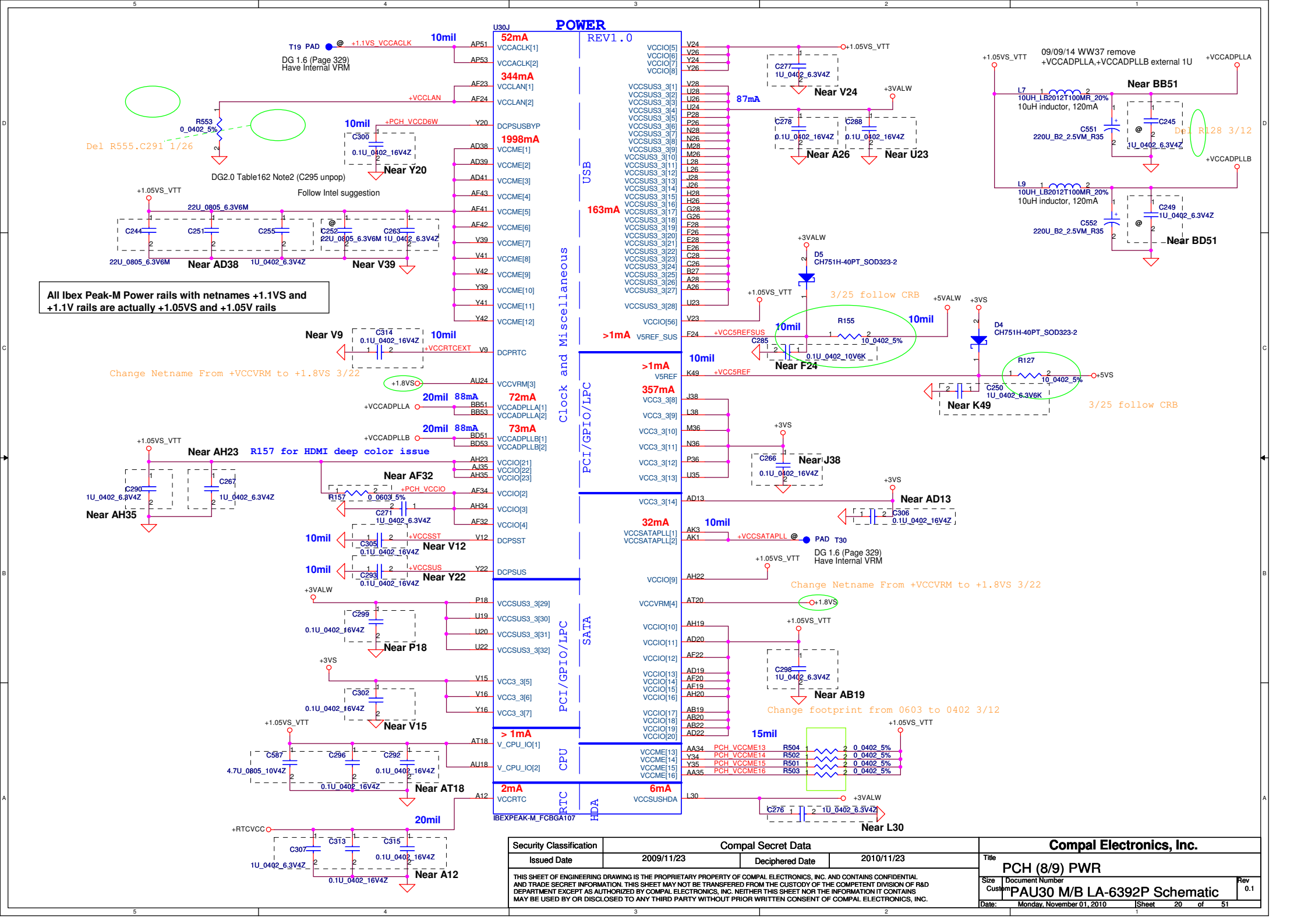
Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

Date: Tuesday, September 07, 2010 | Sheet 19 of 51



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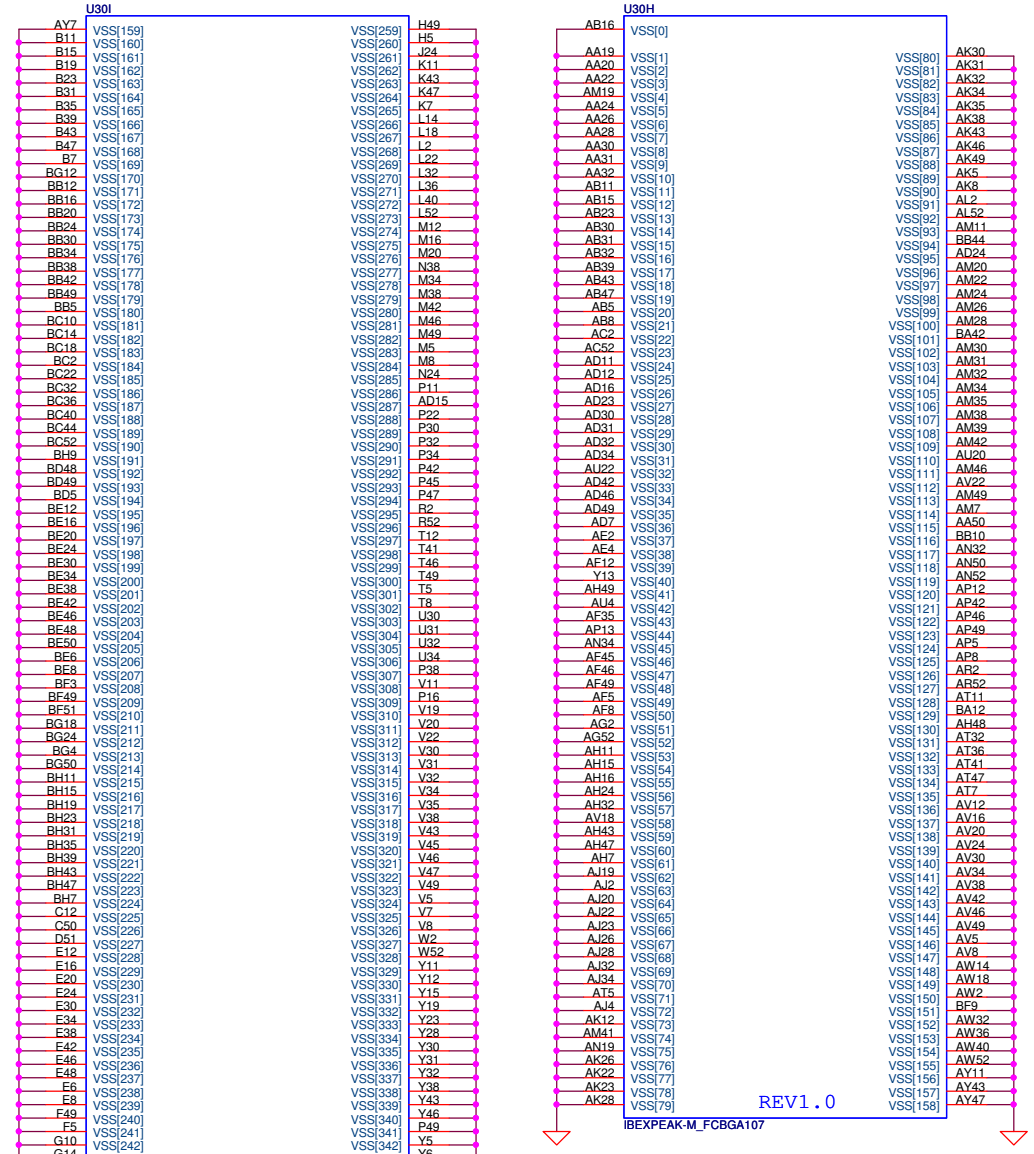
Compal Electronics, Inc.

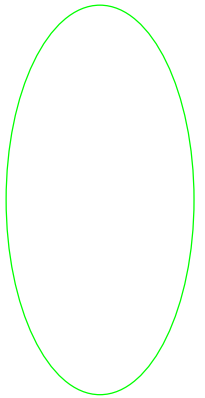
Title: PCH (8/9) PWR

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

Date: Monday, November 01, 2010 | Sheet 20 of 51



Del PCH XDP Port 1/7



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Compal Electronics, Inc.

Title: PCH (9/9) VSS & PCH XDP Port

Size	Document Number	Rev
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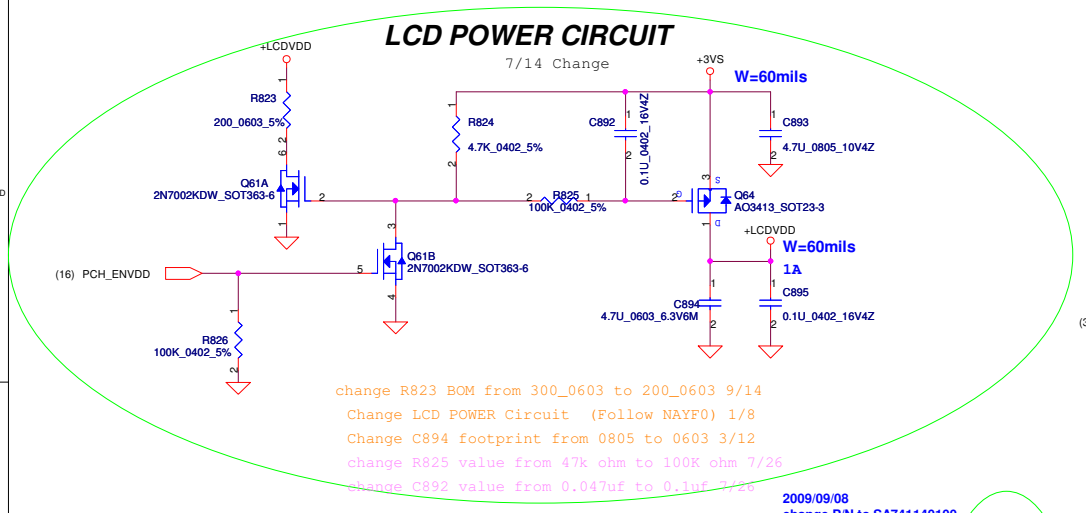
LCD POWER CIRCUIT

7/14 Change



change R823 BOM from 300_0603 to 200_0603 9/14

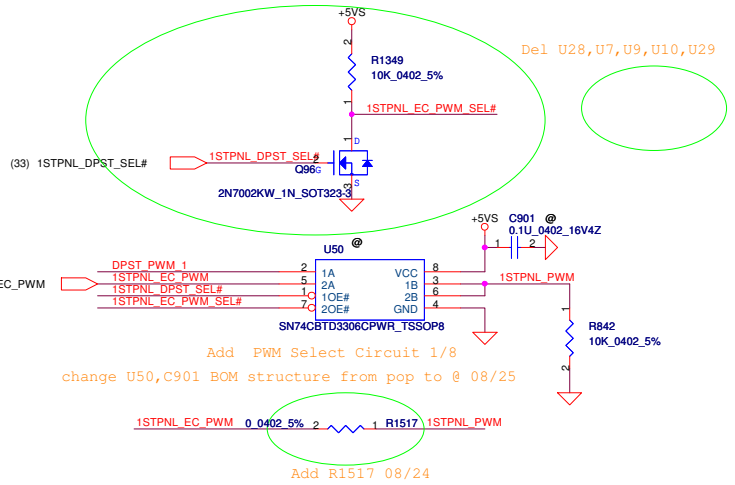
Change LCD POWER Circuit (Follow NAYF0) 1/8

Change C894 footprint from 0805 to 0603 3/12

change R825 value from 47k ohm to 100K ohm 7/26

change C892 value from 0.047uf to 0.1uf 7/26

Change 1STPNL_DPST_SEL# Circuit 3/18



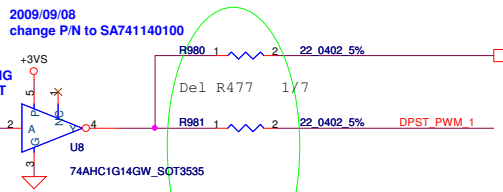
Del U28,U7,U9,U10,U29 1/7

Add PWM Select Circuit 1/8

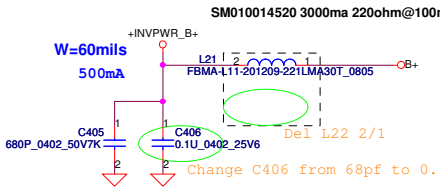
change U50,C901 BOM structure from pop to @ 08/25

Add R1517 08/24

2009/09/08
change P/N to SA741140100

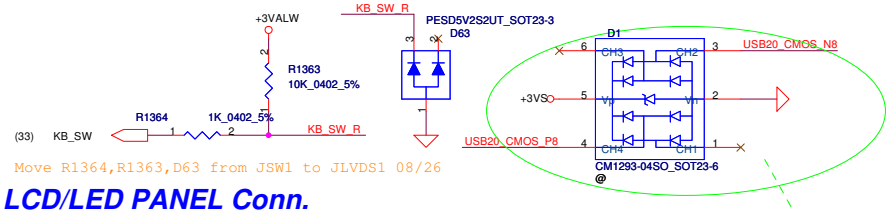


Del R477 1/7



Del L22 2/1

Change C406 from 68pf to 0.1uf 3/12



Move R1364,R1363,D63 from JSW1 to JLVDS1 08/26

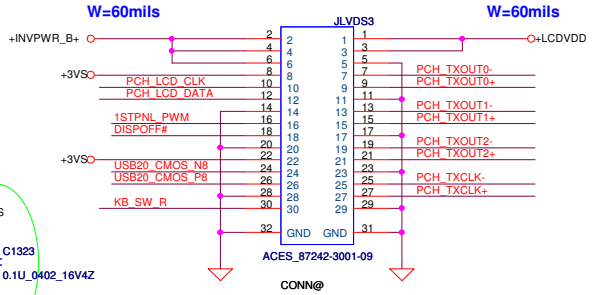
Del R476.R467.R477 1/7

Add R980.R981 1/14

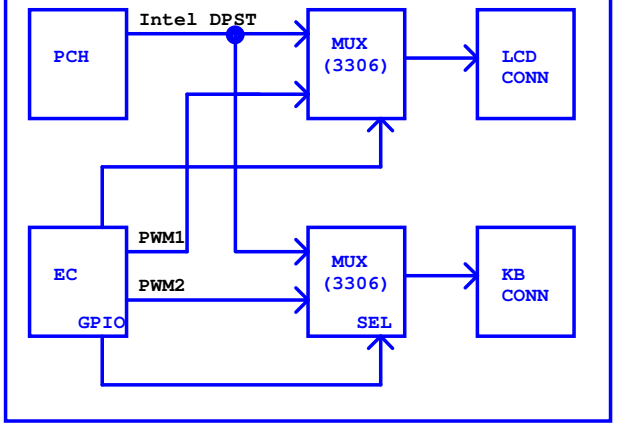
Del R466 3/4

add JLVDS3 08/26

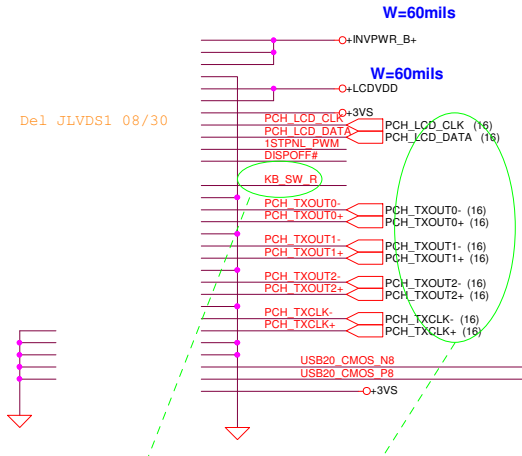
modify JLVDS3 pin define 08/27



Brightness control

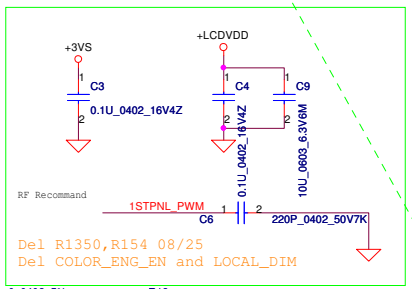


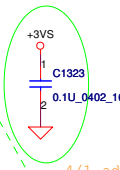
LCD/LED PANEL Conn.



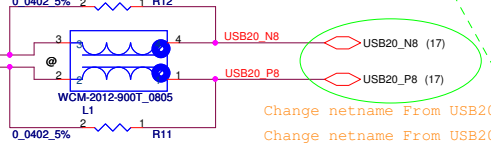
Del JLVDS1 08/30

Change JLVDS1 Singal netname 1/7



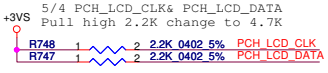


4/1 add for RF



Change netname From USB20_N8 to USB20_N3 1/8

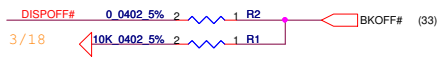
Change netname From USB20_P8 to USB20_P3 1/8



Del UMA Only ,Switchable ,DIS Only Circuit 1/7

Add R1350 3/18

Move R154 From PCH side to JLVDS side 3/18



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Issued Date	2009/11/23	Deciphered Date	2010/11/23

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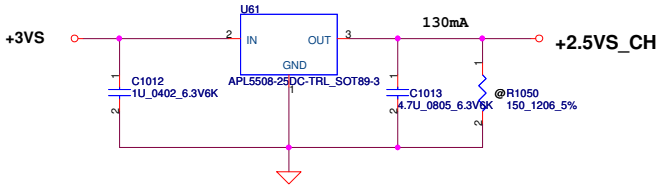
Compal Electronics, Inc.

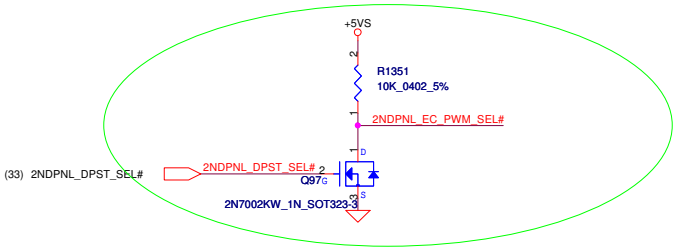
Title: LVDS Connector

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

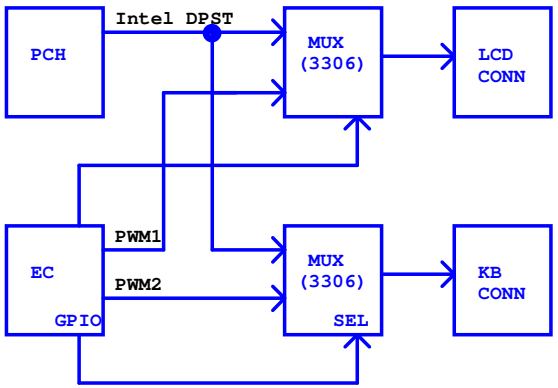
Date: Monday, November 22, 2010 | Sheet 22 of 51



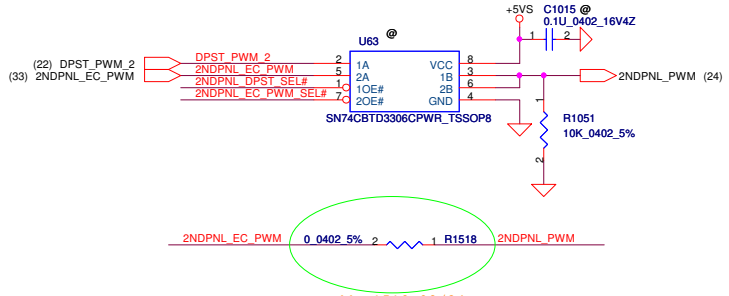
Change 2NDPNL_DPST_SEL# Circuit 3/18



Brightness control



change U63,C1015 BOM structure from pop to @ 08/25



Add R1518 08/24

Security Classification	Compal Secret Data		
Issued Date	2008/10/20	Deciphered Date	2008/10/20

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Compal Electronics, Inc.

Title: ***CH7308 SDVO to LVDS***

Size	Document Number	Rev
Custom	***PAU30 M/B LA-6392P Schematic***	1.0

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add Q83 and R1170 02/24

R1060.R1061 Change BOM Structure From POP to @ 2/23

add R1168 02/24

Change Netname From PLT_RST# to PLT_RST_BUF# 3/2

S IC EE 16K CAT24C16WI-GT3 SOIC 8P

4/1 add R1389, R1390

4/9 RF add, need report

Del L67 2/26

6/17 RF add

change BOM Structure from un-stuff to stuff 7/26

change L63,L64,L68 footprint name to R_0603 08/24

Add Q82.R1166.R1167 2/9

4/7 connect JLVDS2 pin27 to GND

Del JLVDS2 08/30

change Crystal CL from 16p to 20p 7/29 (sourcer suggestion)

Add net:COLOR_ENG_EN and LOCAL_DIM 3/16

Del R1352.R1353

Del COLOR_ENG_EN and LOCAL_DIM 8/25

4/13 ESD add D62

D62 from SC10T24C000 change to SCA00000R00 6/28

add C1471 (ESD request) 7/22

Add JLVDS4 08/26

Modify JLVDS4 pindefine 08/27

change R1065 BOM from 300_0603 to 200_0603 9/14

change SOT363-6 to SOT323-3 02/24

LCD POWER CIRCUIT

7/14 Change

Change From +3VS to +3VALW 3/26

6/8 change Q85 to BSS138

change neme from RTD_PANEL_ON to 2ND_PANEL_ENAVDD 02/24

change R1067 value from 47k ohm to 100K ohm 7/26

change C1043 value from 0.047uf to 0.1uf 7/26

Security Classification	Compal Secret Data		
Issued Date	2008/10/20	Deciphered Date	2008/10/20

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Compal Electronics, Inc.

Title: *7308 SDVO to LVDS*

Size: Custom | Document Number: *PAU30 M/B LA-6392P Schematic* | Rev: 1.0

Date: Monday, November 22, 2010 | Sheet 24 of 51

CRT Connector

Change ESD protect circuit (follow NAV50) 3/12
Close to CRT CONN for ESD.

5/26 change to fuse

W=40mils

W=30mils

Change L30,L32,L34 from SM01000HJ00 to SHI0000A800 11/01

Change L30,L32,L34 P/N form SM01000HI00 to SM01000HJ00(bead 60 ohm) 9/9

Del L77.L78.L79.C571.C564.C561 3/4
NV DG RGB recommended one pi filter

Change from Inductor to Bead 60 ohm 7/26

Change BOM Structure from un-pop to pop 7/26

Change BOM Structure from POP to @ 9/9

SM010012010 300ma 120ohm@100mhz DCR 0.4

3/22 add R1359, update net CRT_DET#

5/24 Change CRT connet to PCH

Security Classification	Compal Secret Data		
Issued Date	2009/11/23	Deciphered Date	2010/11/23

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Compal Electronics, Inc.

Title: CRT Connector

Size: B | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

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5/26 add RT9701 for HDMI VCC

U105 RT9701-PB_SOT23-5

Q98 SI3456BDV-T1-E3_TSOP6

W=40mils

F2 1.1A_6VDC_FUSE

C295 0.1U_0402_16V4Z

R1360 10K_0402_5%

R425 510K_0402_5%

C1310 0.1U_0603_25V7K

R1365 47K_0402_5%

Change +5VS to +HDMI_5V_OUT Circuit 3/18

3/25 add R1360, Q99, R1365

6/3 temprately restore Q99

change R1365 value from 10K to 47K ohm 7/27

Q99A 2N7002KDWH_SOT363-6

Q99B 2N7002KDWH_SOT363-6

Change HPD Circuit 1/8

R832 Change From 10k to 0 3/4

C896 Change From 0.1u to 220P 3/4

2009/04/30
add C101 & R145

R831 10K_0402_5%

Q65 2N7002KW_1N_SOT323-3

C896 220P_0402_50V7K

R832 0_0402_5%

R833 100K_0402_5%

HDMI connector

JHDMI1 SUYIN_100042GR019M23DZL

CONN@

4/13 change HDMI footprint

U32 ASM1442 PN: SA00003GT00

ASM1442T_QFN48_7X7

Vendor Recommand : CFG SETTING 000

change R238,R629,R232 BOM structure
from pop to @ 9/9

change R561,R557 BOM structure
from pop to @ 9/9

Connection to 3.4K external resistor.

CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

R234 from 100ohm change to 100K 6/28

SM070001310 400ma 90ohm@100mhz DCR 0.3

L37 WCM-2012-900T_0805

L36 WCM-2012-900T_0805

L38 WCM-2012-900T_0805

L39 WCM-2012-900T_0805

6/3 swap for layout

5/24 DEL HDMI from VGA

R171 4.7K_0402_5%

R172 4.7K_0402_5%

C592 C607 C600 C331 C608 C591 C602 0.1U_0402_16V4Z

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Compal Electronics, Inc.

Title: HDMI Conn

Size: C | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.1

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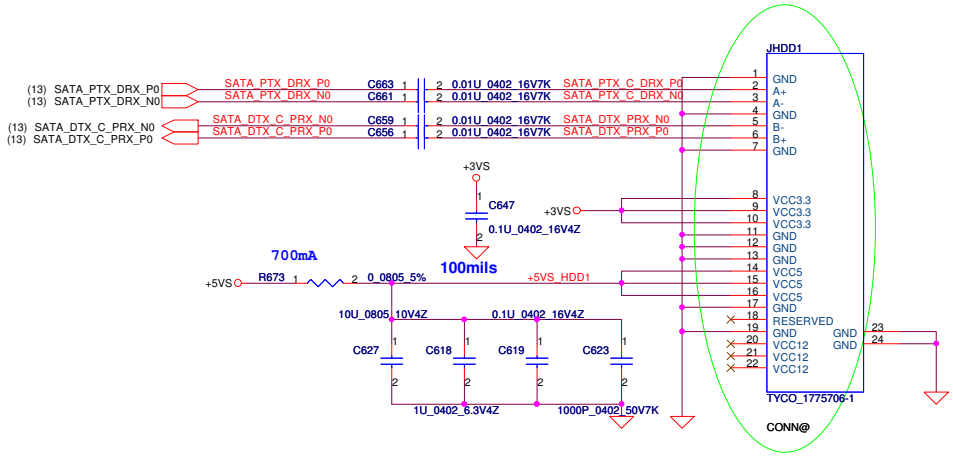
CL 4.0 mm

SATA HDD1 Conn.



6/8 change HDD symbol

change HDD symbol 8/26

Security Classification	Compal Secret Data		
Issued Date	2009/11/23	Deciphered Date	2010/11/23

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Compal Electronics, Inc.

Title: ***HDD & ODD Connector***

Size: Custom | Document Number: ***PAU30 M/B LA-6392P Schematic*** | Rev: 0.1

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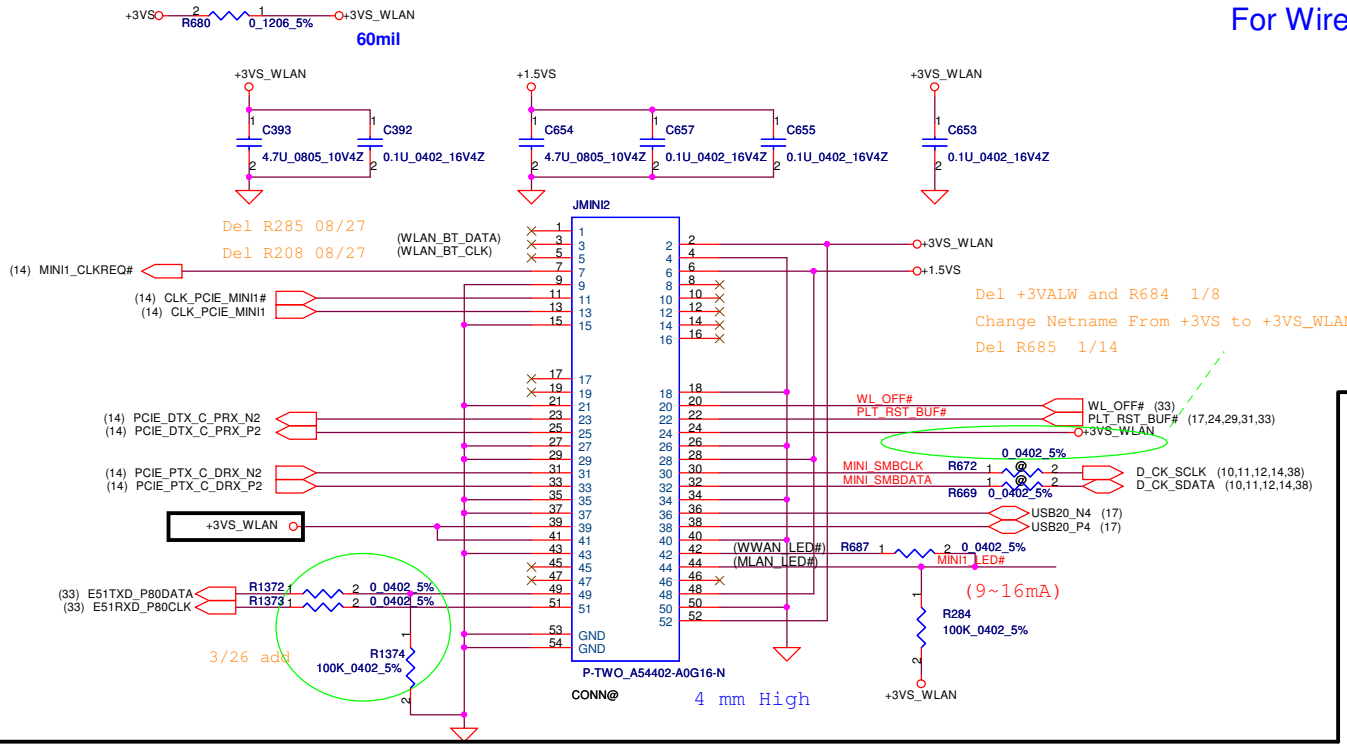
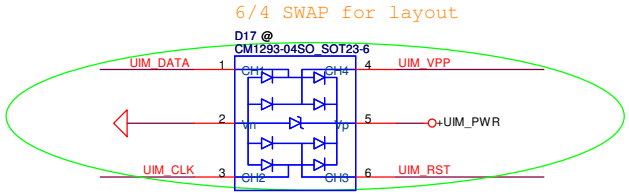
For Wireless LAN (Half Card)



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

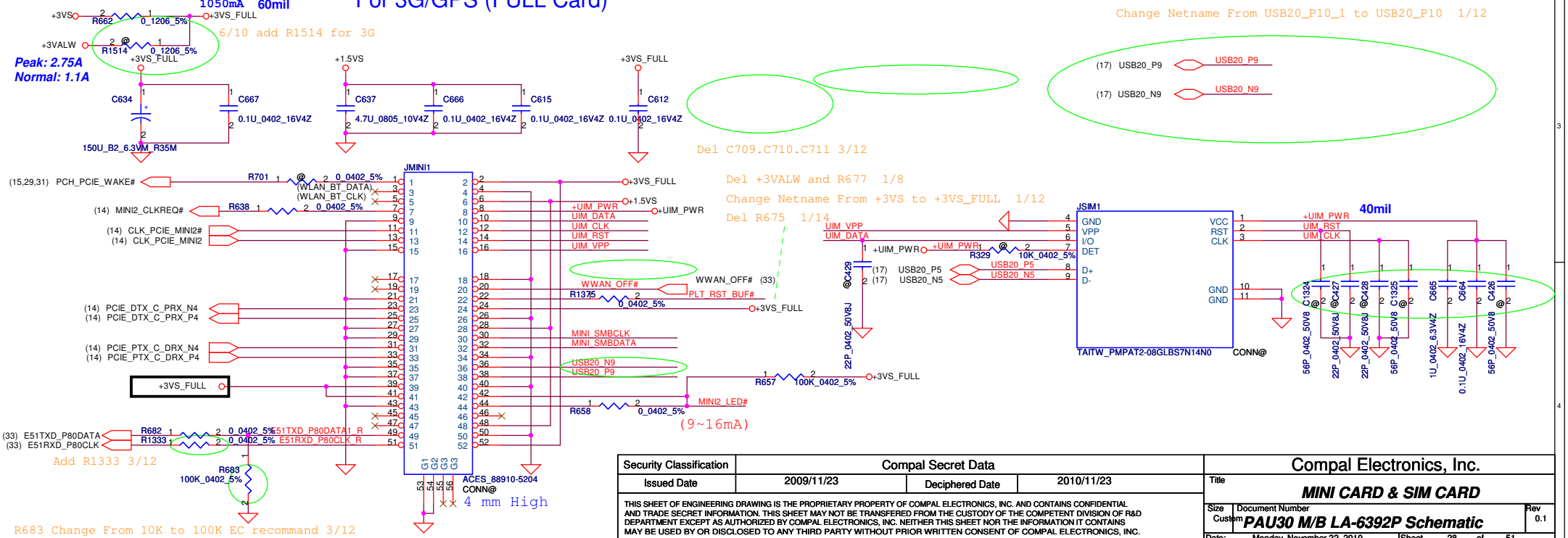
For SIMM CARD



Del L41.R661.R663 1/14
Change Netname From USB20_N10_1 to USB20_N10 1/12
Change Netname From USB20_P10_1 to USB20_P10 1/12

(17) USB20_P9 — USB20_P9
(17) USB20_N9 — USB20_N9

For 3G/GPS (FULL Card)



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Compal Electronics, Inc.

Title: **MINI CARD & SIM CARD**

Size: Custom | Document Number: **PAU30 M/B LA-6392P Schematic** | Rev: 0.1

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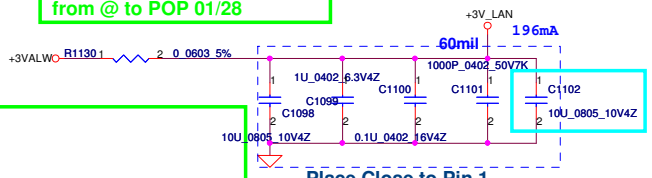
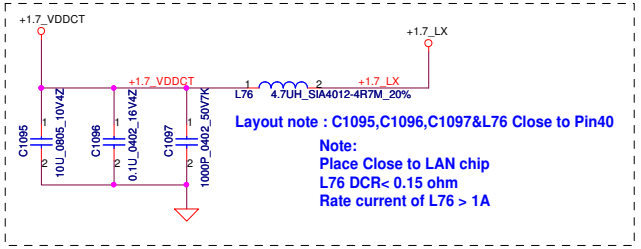
LAN Power Circuit & Refer NTUC0

change R362 BOM structure
from @ to POP 01/28



Place Close to Pin 1
Refer CRB

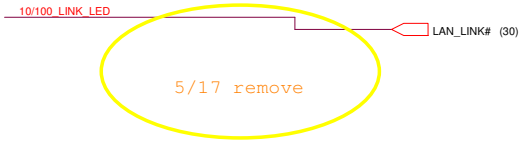
Del Q21,R363,C273
(WOL function) 01/28

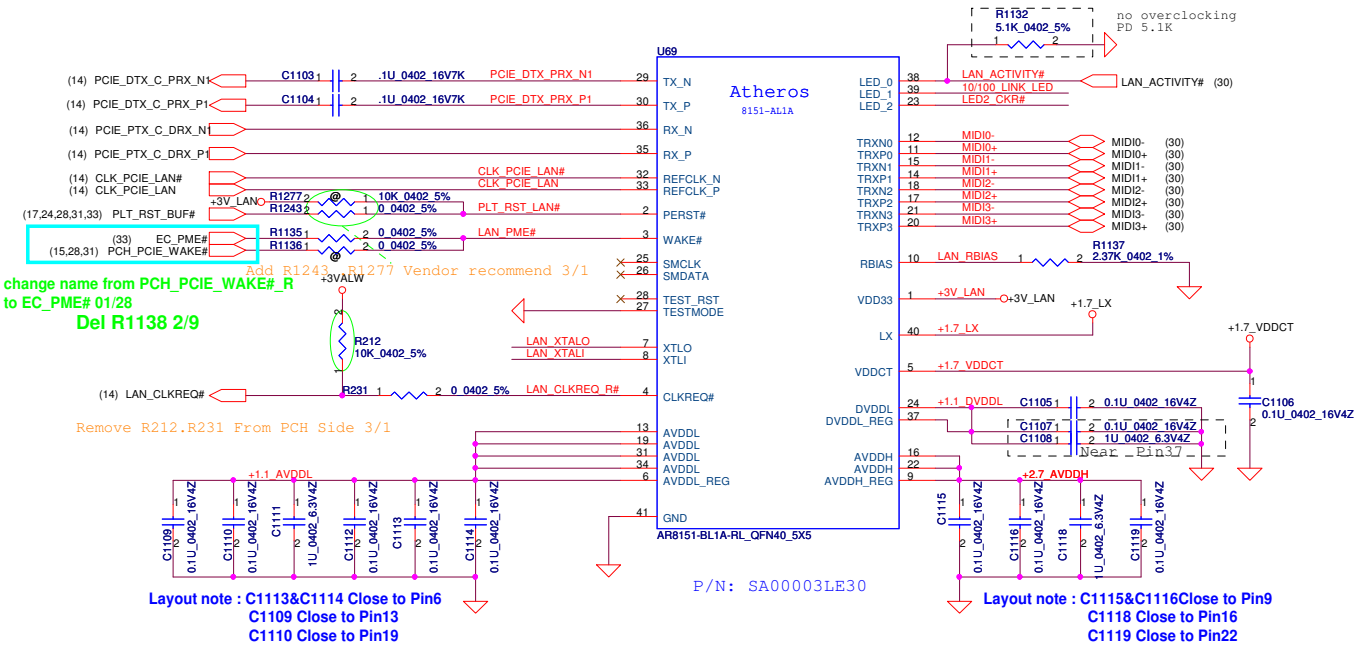


Layout note : C1095,C1096,C1097&L76 Close to Pin40

Note:
Place Close to LAN chip
L76 DCR< 0.15 ohm
Rate current of L76 > 1A

10/22 Remove R364



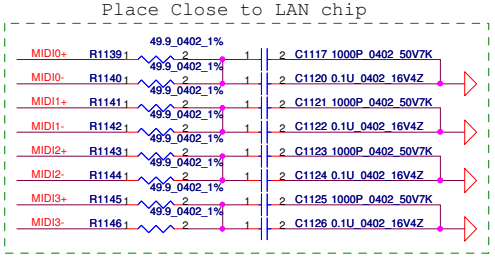


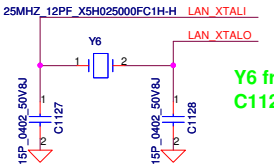
Layout note : C1113&C1114 Close to Pin6
C1109 Close to Pin13
C1110 Close to Pin19
C1111 Close to Pin31
C1112 Close to Pin34

Layout note : C1115&C1116Close to Pin9
C1118 Close to Pin16
C1119 Close to Pin22

10/22 Change R376 from mount to @
11/02 Change R373 from mount to @
11/02 Delete Q3(@),R375(@),R377(@)
11/09 Delete R373(@),R376(@)

Place Close to LAN chip





Y6 from 20 pf change to 12 pf 6/28
C1127,C1128 from 27p change to 15p 6/28

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Issued Date	2009/10/10	Deciphered Date	2010/10/10

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Compal Electronics, Inc.

Title: LAN AR8151

Size: Custom | Document Number: PAU30 M/B LA-6392P Schematic | Rev: 0.3

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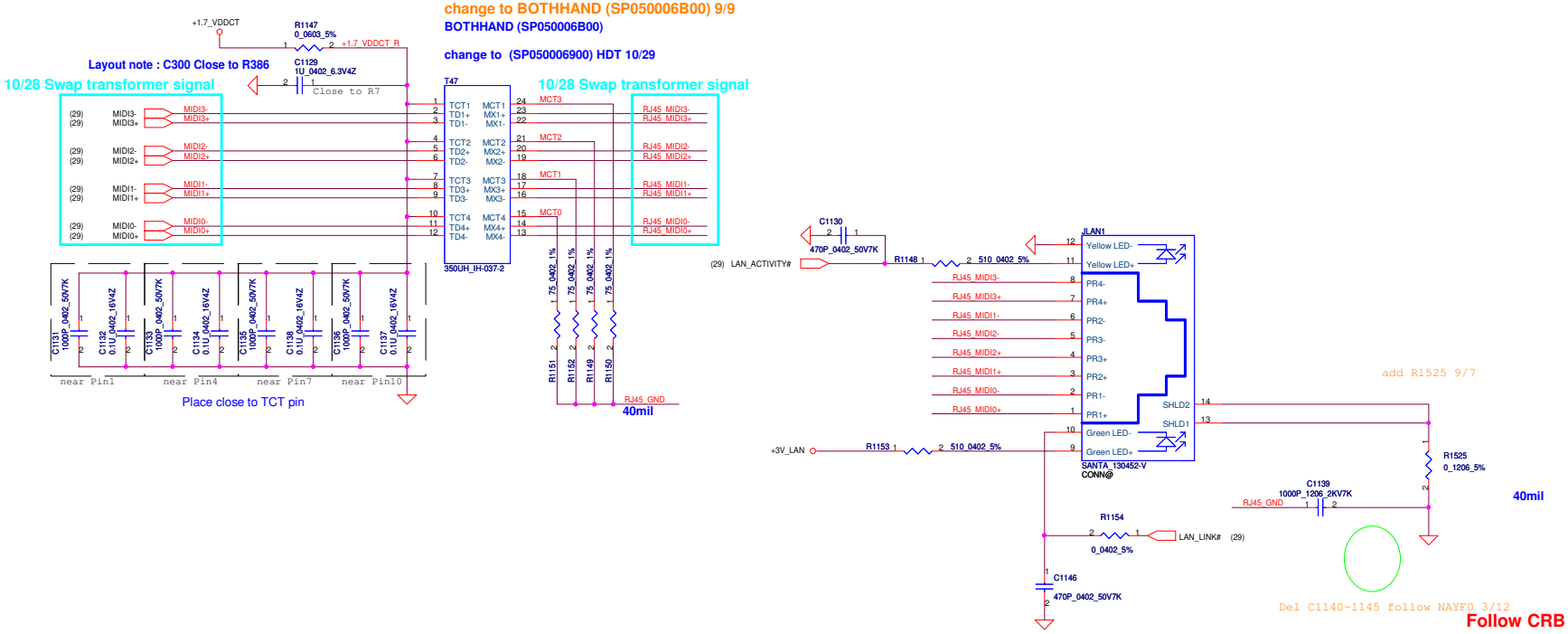
Copy NIMUA

change transformer P/N from TAIMAG(SP050004M00)
change to BOTHHAND (SP050006B00) 9/9
BOTHHAND (SP050006B00)

change to (SP050006900) HDT 10/29



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Issued Date	2009/10/10	Deciphered Date	2010/10/10

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Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size	Document Number	Rev
	PAU30 M/B LA-6392P Schematic	0.3

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6/8 add 100uF
C1461 chang to 150U 6/30

C1285,C1286 from 12p change to 15p 6/28
R1263 from 100ohm change to 430ohm 6/28

change U92 P/N from SA000033W10 to SA000048H00 10/22

6/9 change U95 to MX25L512EMC

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

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Title: **USB3.0 PD720200**

Size	Document Number	Rev
C	PAU30 M/B LA-6392P Schematic	0.1

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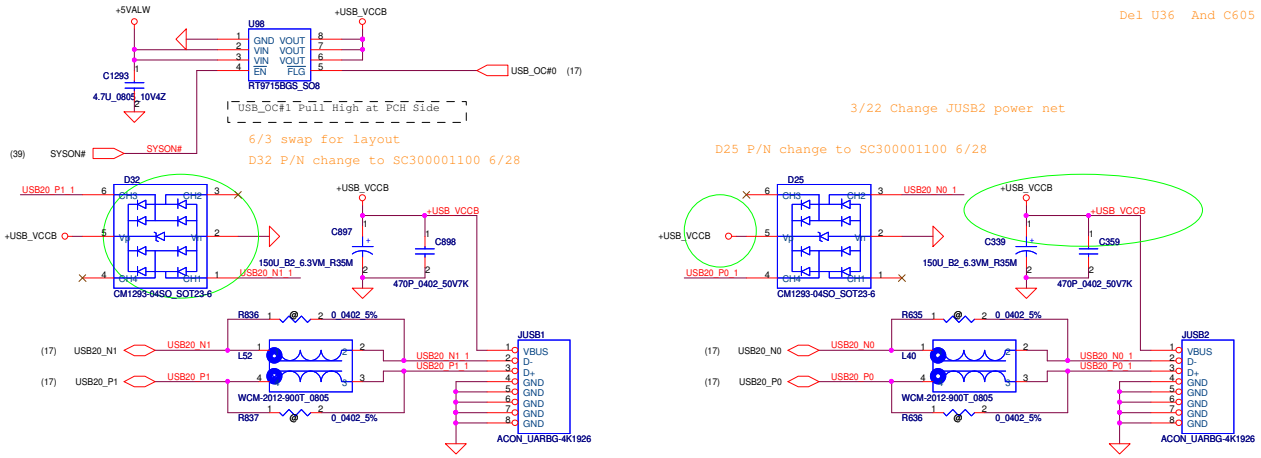
Left

R640 Move to P.17 1/12
Del R639 And C614 1/8
Del U36 And C605 3/3

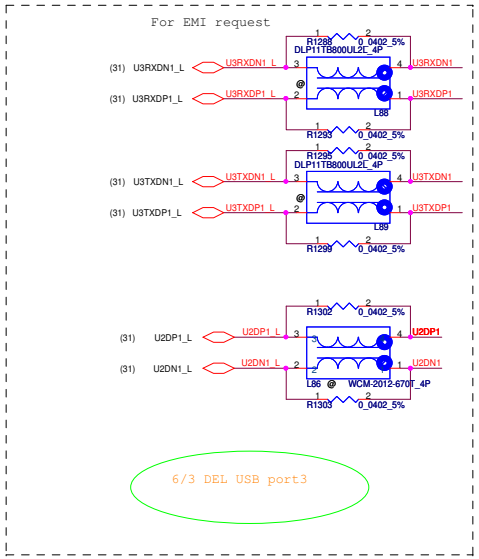
3/22 Change JUSB2 power net

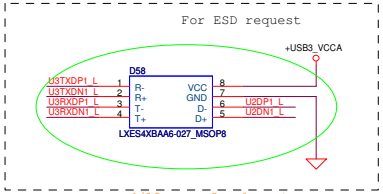
D25 P/N change to SC300001100 6/28

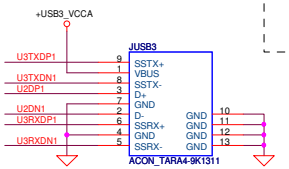
6/3 swap for layout
D32 P/N change to SC300001100 6/28



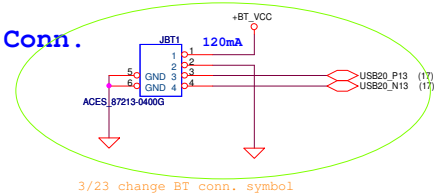
Right

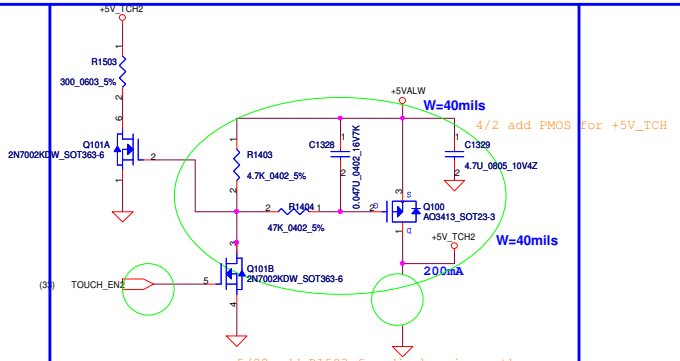


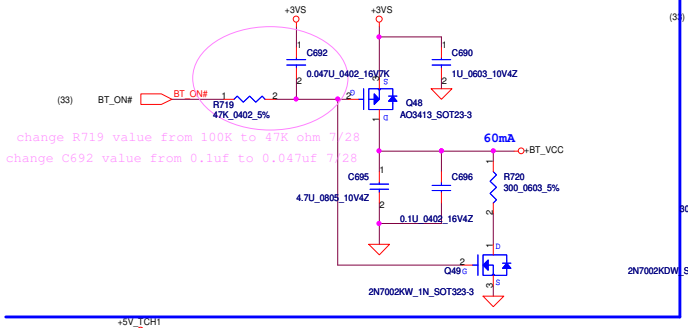


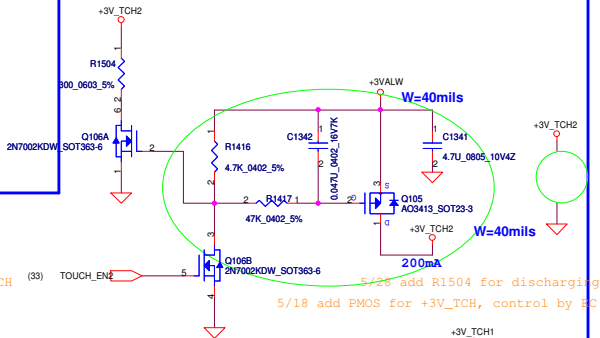


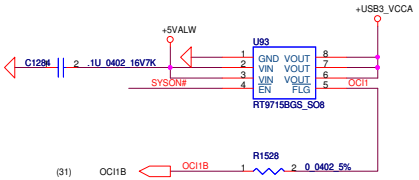
BT Conn.

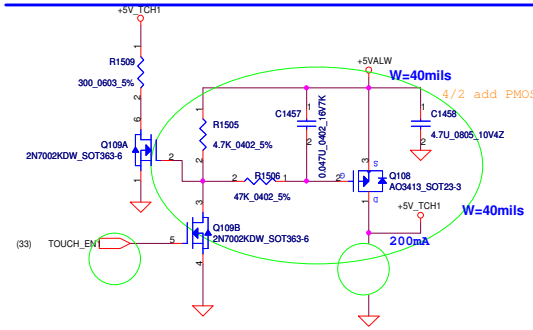


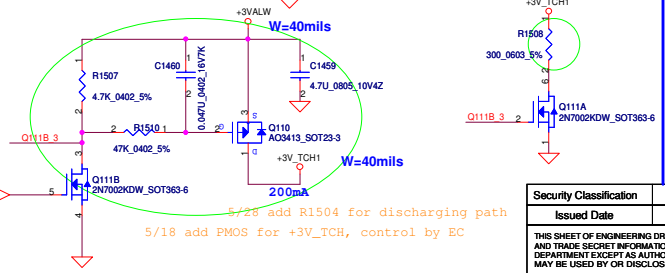


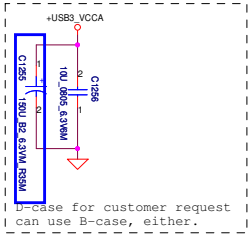












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Compal Electronics, Inc.

Title: **USB / BT / LAN CON**

Size	Document Number	Rev
C	**PAU30 M/B LA-6392P Schematic**	0.1

Date: Monday, November 22, 2010 Sheet 32 of 51

SM010015410 300ma 80ohm@100mhz DCR 0.3

For EC Tools

Change From RAM door to 3G door 1/14

Place on 3G door

4/7 move from PCH

R299.R302 Change BOM Structure POP to @ 1/13

Del R711.C688 1/13

Change Netname From PLT_RST# to PLT_RST_BUF# 3/2

Add HV_15V_EN 9/1

Change HV_15V_EN from pin 82 to pin 85 9/3

3/22 DEL R298,R295, R300

Add R1354.R1355 3/18

Del R301.R296 3/12

4/20 Change AC_OFF connect to pin36

Add R1305.R1306 3/2

Change L49 to R982 1/14

Change H_PROCHOT_# From Pin76 to Pin 68 (follow NELA0) 3/18

Remove Netname: EC_PWM_2 From Pin 21 to Pin34 3/2

Change R292 value from 8.2K to 18K 9/03

Del C395 3/12

Change HV_15V_EN from pin 82 to pin 85 9/3

Change R292 value from 18K to 33K 10/29

EC_ID: HIGH is D3 ; LOW is E0

3/29 remove cap

change C699&C700 value from 15pf to 22pf 7/27

4/7 change PANEL_THRM_ALERT# to pin 115

Board ID definition, Please see page 3.

Board ID definition, Please see page 3.

U45 KB926QFE0_LQFP128_14X14 SA00001J5A0

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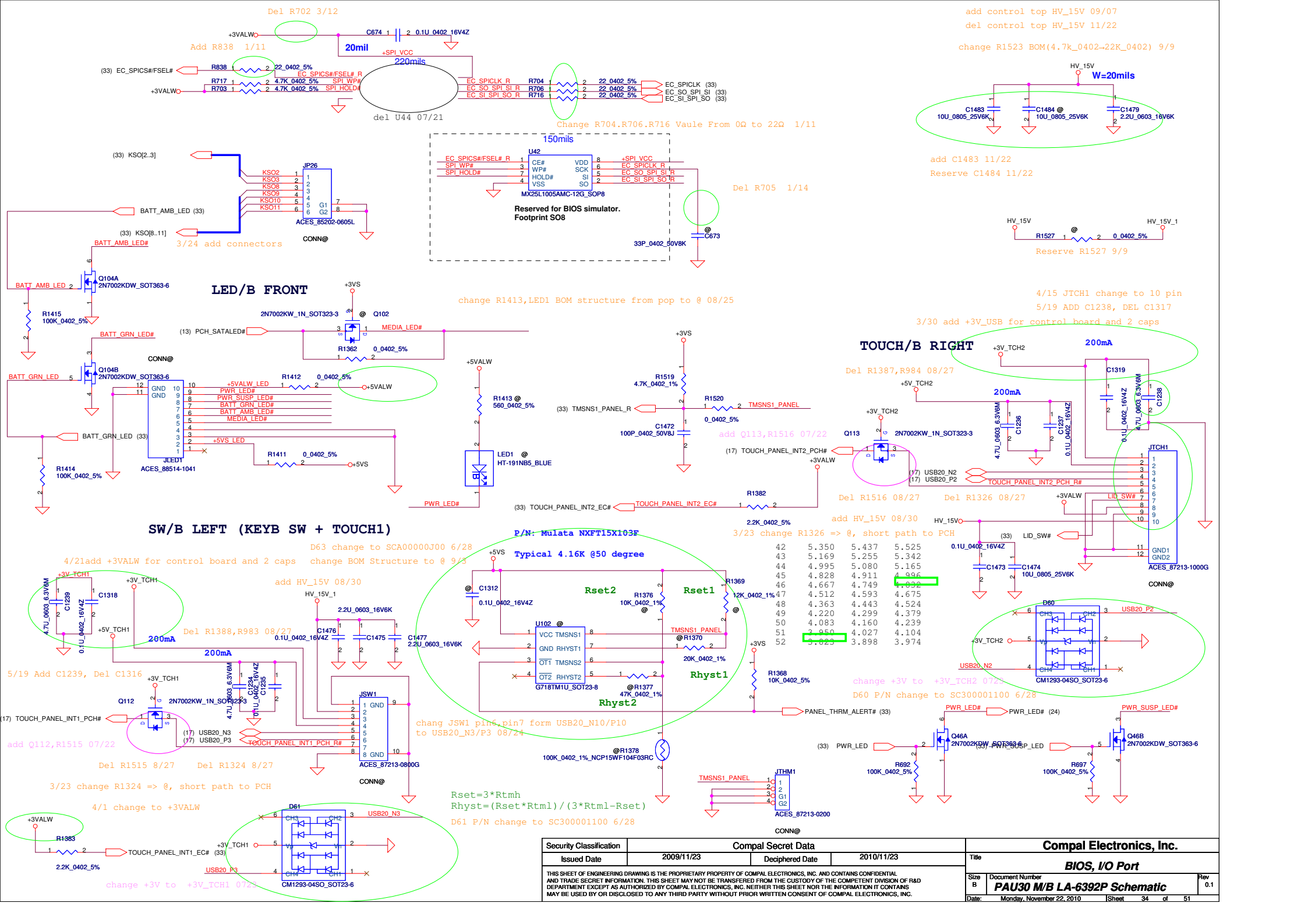
Compal Electronics, Inc.

Title: **EC ENE KB926**

Size: B | Document Number: **PAU30 M/B LA-6392P Schematic** | Rev: 0.1

Date: Monday, November 22, 2010 | Sheet 33 of 51



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: ***BIOS, I/O Port***

Size	Document Number	Rev
B	***PAU30 M/B LA-6392P Schematic***	0.1

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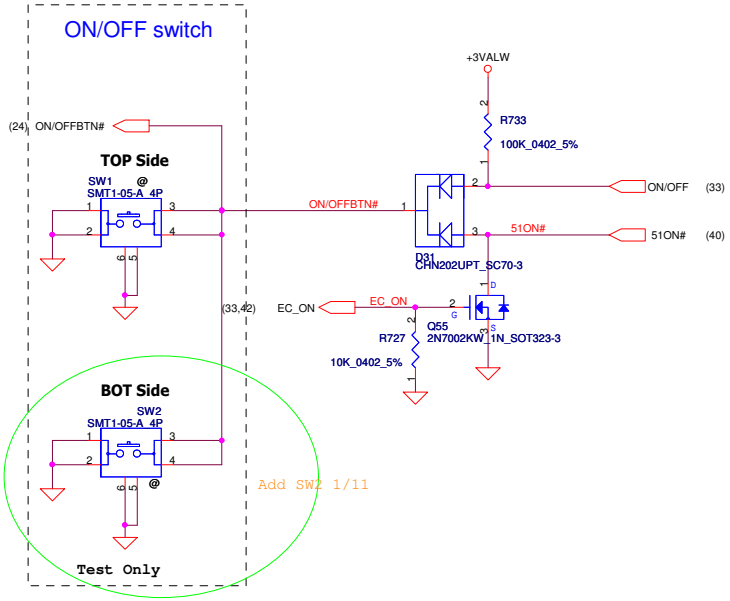
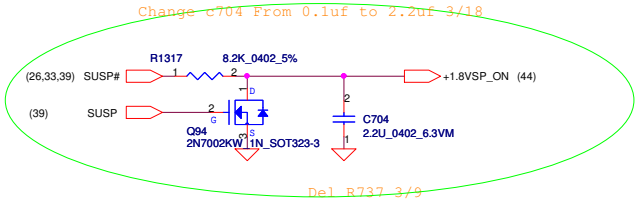
Power Button



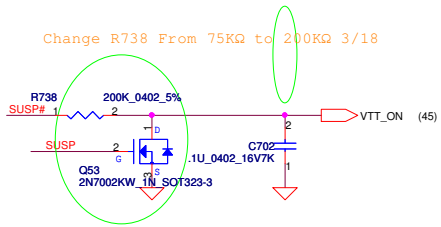
Power ON Circuit

Change R1317 From 1KΩ to 8.2KΩ 3/18
Change c704 From 0.1uf to 2.2uf 3/18

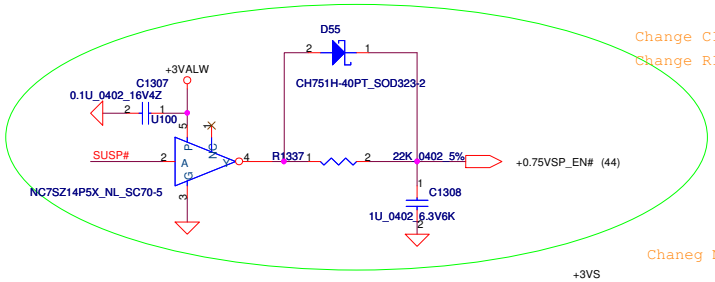


Del R737 3/9

Change R738 From 75KΩ to 200KΩ 3/18



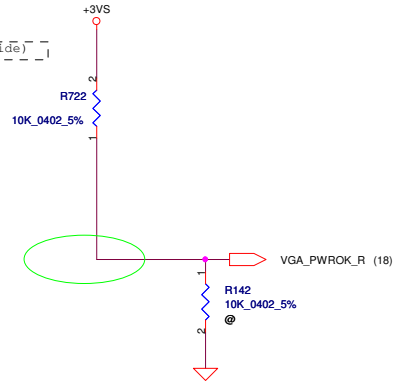
Add +0.75VSP_EN Circuit 3/13
Change +3VS to +3VALW 3/16



Change C1308 From 0.1uf to 1uf 3/18
Change R1337 From 1KΩ to 22KΩ 3/18

Chaneg Netname From VGA_PWROK# to PEG_CLKREQ#_R 3/18

VGA_PWROK is Open-Drain (Pull high at HW side)



Del U46.R734.R1159.R739.R740.D45.R729.R730.D46 3/9

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Issued Date	2009/11/23	Deciphered Date	2010/11/23

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Compal Electronics, Inc.

Title: **Power OK**

Size: B | Document Number: **PAU30 M/B LA-6392P Schematic** | Rev: 0.1

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Del ALC272 circuit 3/12

+VDDA
R1071 10K_0402_5%
+3VS
C1047 4.7U_0603_6.3V6M
D43 CH751H-40PT_SOD323-2
R1076 10K_0402_5%
R1073 10K_0402_5%
C1051 1U_0402_6.3V4Z
MONO_IN
(33) BEEP#
C1052 1U_0402_6.3V4Z
R1074 560_0402_5%
Q75 2SC2411KT146_SOT23-3 <BOM Structure>
R1075 2.4K_0402_1%
(13) PCH_SPKR
C1053 1U_0402_6.3V4Z
R1077 560_0402_5%
D33 CH751H-40PT_SOD323-2

R1072 FBMA-L11-201209-221LMA30T_0805
+5VS
0.1U_0402_16V4Z
C1048
C1049 0.1U_0402_16V4Z
60mil
40mil
U66 G9191-475T1U_SOT23-5
IN GND SHDN OUT BYP
+VDDA 4.75V
C1050 0.01U_0402_25V7K
(output = 300 mA)

L69 0_0603_5%
PVDD1_AUDIO
+5VS
C1054 0.1U_0402_16V4Z
C1055 10U_0603_6.3V6M
C1056 0.1U_0402_16V4Z
C1057 10U_0603_6.3V6M

L71 0_0603_5%
PVDD2_AUDIO
+5VS
C1066 0.1U_0402_16V4Z
C1067 10U_0603_6.3V6M
C1069 10U_0603_6.3V6M

+VDDA
0.1U_0402_16V4Z
40mil
C1061 10U_0805_10V4Z
C1062
C1063
0.1U_0402_16V4Z
PVDD1_AUDIO
+VDDA
PVDD2_AUDIO
+3VS_DVDD
L70 BLM18PG181SN1D_2P
+3VS
C1058 0.1U_0402_16V4Z
C1059 0.1U_0402_16V4Z
C1060 10U_0805_10V4Z

U90 ALC271X-GR_QFN48_7X7
AVDD1 AVDD2 PVDD1 PVDD2 DVDD DVDD_IO
LINE2_L LINE2_R MIC2_L MIC2_R LINE1_L LINE1_R MIC1_L MIC1_R CBN CBP MIC2_VREFO MIC1_VREFO_R MIC1_VREFO_L LDD_CAP JDREF CPVEE SENSE A SENSE B EAPD SPDIFO DVSS GND
SPK_OUT_L+ SPK_OUT_L- SPK_OUT_R+ SPK_OUT_R- HPOUT_L HPOUT_R SDATA_IN SDATA_OUT SYNC RESET# BCLK GPIO0/DMIC_DATA GPIO1/DMIC_CLK PD# PCBEEP MONO_OUT AVSS2 VREF AVSS1 PVSS2 PVSS1

Del R1100.R1080.R1081.R1084 3/17

(37) MIC1_L
(37) MIC1_R
C1072 4.7U_0805_6.3V6K
C1073 4.7U_0805_6.3V6K
C1064 2.2U_0402_6.3VM
Del R1092.1088 3/17
MIC1_VREFO_R 10mil
MIC1_VREFO_L 10mil
MIC1_VREFO 10mil
C1074 10U_0603_6.3V6M
R1083 20K_0402_1%
JDREF 10mil
C1079 2.2U_0402_6.3VM
CPVEE 10mil
SENSE_A
(37) HP_PLUG#
(37) MIC_PLUG#
R1091 39.2K +-1% 0402
R1093 20K_0402_1%
(33) EAPD
(37) SPDIF
R1095 0_0402_5%
EAPD_R
SPDIF
Change Netname From SENSE_B to CPVEE 3/18

HP_LEFT
HP_RIGHT
HDA_SDIN0_AUDIO
HDA_SDOUT_AUDIO
HDA_SYNC_AUDIO
HDA_RST_AUDIO#
HDA_BITCLK_AUDIO
DMIC_DATA
DMIC_CLK
EC_MUTE_CODEC#
MONO_IN
CODEC_VREF
C1080 @ C1081 0.1U_0402_16V4Z 10U_0805_10V4Z
PVSS2
PVSS1
R1086 33_0402_5%
C1481 12P_0402_50V8J
R1526 @ 10K_0402_5%
R1098 0_0402_5%
+5VS
reserve R1526 9/8

(37) SPKL+
(37) SPKL-
(37) SPKR+
(37) SPKR-
(37) HP_LEFT
(37) HP_RIGHT
(13) HDA_SDIN0
(13) HDA_SDOUT_AUDIO
(13) HDA_SYNC_AUDIO
(13) HDA_RST_AUDIO#
(13) HDA_BITCLK_AUDIO
EC_MUTE# (33)

change C1481 BOM structure form @ to POP 9/14
reserve C1481 9/10
Change MIC from Analog MIC to Digital MIC 3/12

R1320.R1321.C1076.C1077 Close to Codec
Digital MIC
change R1320 & R1321 value from 22 ohm to 33 ohm 7/26
+3VS
JDMIC1 ACES_87213-0400G
DMIC_CLK
DMIC_DATA
R1320 33_0402_5%
R1321 33_0402_5%
D34 PJDLC05C
C1077 33P_0402_50V8J
C1076 220P_0402_50V8J
CONN@
change C1077 value from 22pf to 33pf and stuff 7/26
D34 P/N change to SCA00000T00 6/28

Change U90 from SA00003LA00 to SA00003LA10 10/26
271X change 271X-VB3 10/26

C1482 @ 0.1U_0402_16V4Z
+5VS
R1529 @ 10K_0402_5%
U106 74AHCT1G125GW_SOT353-5
(33) EC_MUTE#
EC_MUTE#
EC_MUTE_CODEC#
R1131 4.7K_0402_5%
R1133 @ 4.7K_0402_5%
Reserve C1428,U106,R1529,R1133 10/22
Add R1131 10/22

Change R1105.R1106.R1107 footprint From 0805 to 0603 3/18
R1105 @ 0_0603_5%
R1106 0_0603_5%
R1107 0_0603_5%
GND GNDA GND GNDA

Need update this table

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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Issued Date: 2008/08/10 Deciphered Date: 2009/08/10
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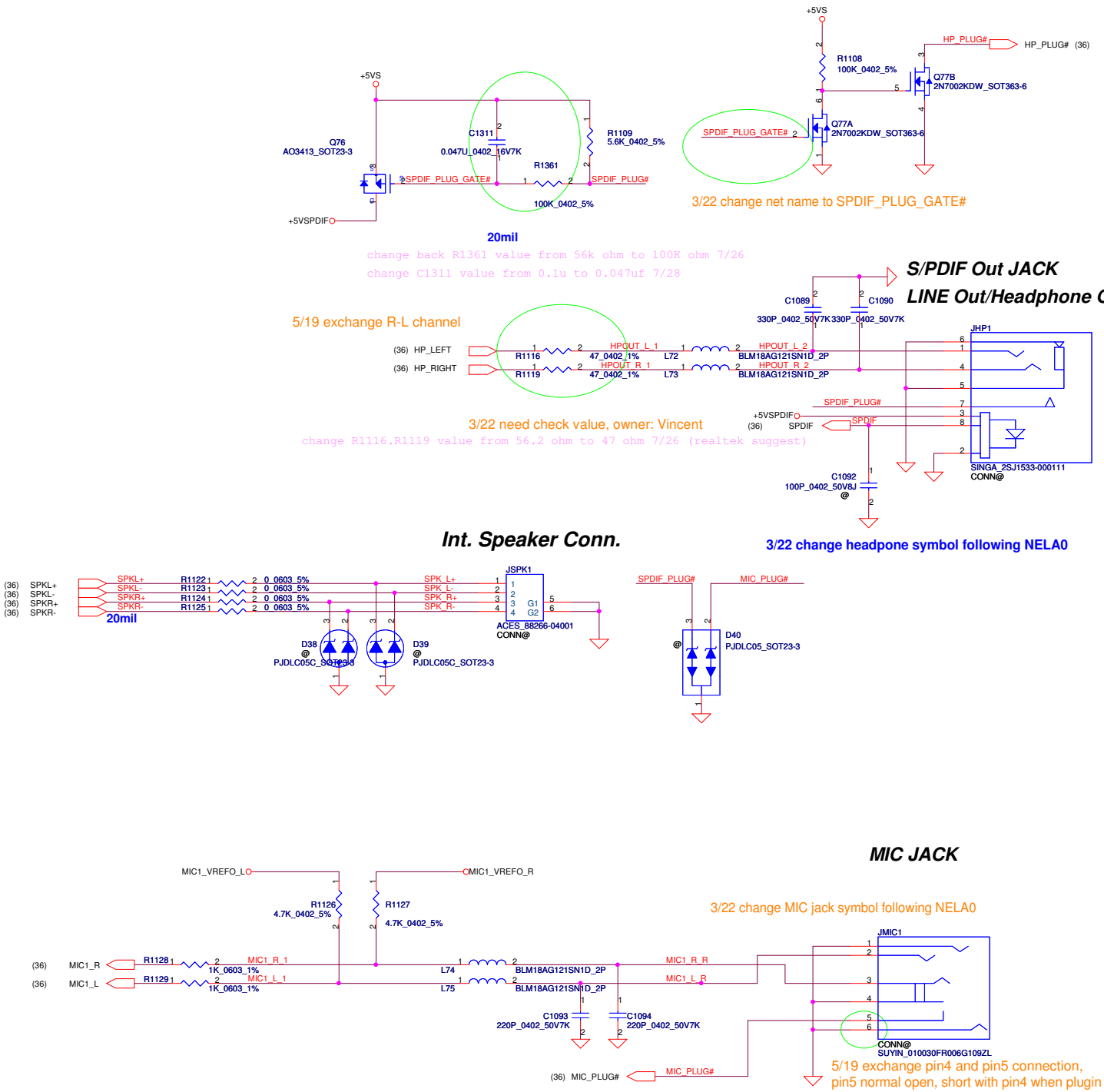
Compal Electronics, Inc.
Title: HD Audio Codec ALC271X
Size: C Document Number: PAU30 M/B LA-6392P Schematic Rev: 0.2
Date: Monday, November 22, 2010 Sheet 36 of 51



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Compal Electronics, Inc.

Title: ***Amplifier & Audio Jack***

Size	Document Number	Rev
B	***PAU30 M/B LA-6392P Schematic***	0.2

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Change D66 BOM structure form @ to POP 10/29
reserve D66 10/26

FAN1 Conn

D66
CH491DPT_SOT23-3
@

R417
0_0603_5%
+5VS
+VCC_FAN1

C500
10U_0805_10V4Z

Change R417 BOM structure form POP to @ 10/29

2009/12/18
+5VS
D18
1SS355_SOD323-2
@
D20
1SS355_SOD323-2
@

5/18 DEL D19, ADD D20

C518
10U_0805_10V4Z
C516
1000P_0402_50V7K

+3VS
R429
10K_0402_5%
40mil
+VCC_FAN1
(33) FAN_SPEED1
(33) FANPWM
C515
1000P_0402_50V7K

JFAN1
G1
G2
ACES_85204-04001
CONN@

5/18 change footprint

H1 H_3P2 @
H2 H_3P2 @
H3 H_3P2 @
H4 H_3P2 @
H5 H_3P2 @
H6 H_3P2 @
H7 H_3P2 @
H8 H_3P2 @
H9 H_3P2 @
H10 H_3P2 @
H11 H_3P2 @
H12 H_3P2 @
H13 H_3P2 @
H14 H_3P2 @
H15 H_3P2 @
H16 H_3P2 @
H17 H_3P2 @
H18 H_3P2 @
H19 H_2P8 @
H20 H_3P2 @
H22 H_4P0 @
H24 H_4P2X4P7 @
H25 H_4P2 @
H26 H_4P7 @
H27 H_4P2X4P7 @
H28 H_2P8 @
H31 H_4P0X4P6 @
H32 H_3P2 @
H33 H_3P2 @

add H32,H33 7/12

modify 03/24

FD4 @ FIDUCIAL_C40M80
FD2 @ FIDUCIAL_C40M80
FD1 @ FIDUCIAL_C40M80
FD3 @ FIDUCIAL_C40M80

Add G-Sensor Circuit 1/12

LIS33DE ST G-SENSOR

+3VS
C899 10U_0603_6.3V6M GSEN@
C900 0.1U_0402_16V4Z GSEN@
+3VS
R839 4.7K_0402_5%
GSEN@

4/6 add

U49
VDD
VDD_IO
CS
SDA/SDI/SDO
SCL/SPC
SDO/SA0
NC_1
NC_2
INT_1
INT_2
GND_1
GND_2
GND_3
GND_4
RSVD_1
RSVD_2
LIS331DLTR_LGA16_3X3
GSEN@

R1405 0_0402_5%
GSEN@
G_SENSOR_INT#
G_SENSOR_INT# (17)

(10,11,12,14,28) D_CK_SDATA
(10,11,12,14,28) D_CK_SCLK

R839 Change From 3.4K to 4.7K 3/4

6/17 DEL R912.R913

U? LIS33DE P/N SA00003VT00

Del Q63.R840.R841 1/13

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Compal Electronics, Inc.

Title: *FAN & G-Sensor & Screw Hole*

Size	Document Number	Rev
B	*PAU30 M/B LA-6392P Schematic*	0.1

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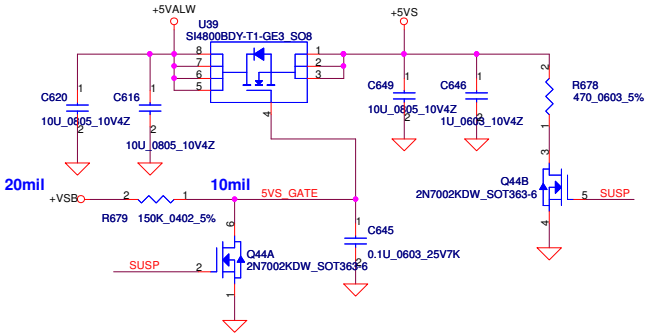
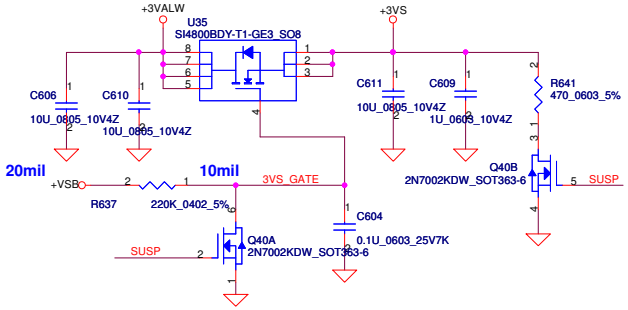
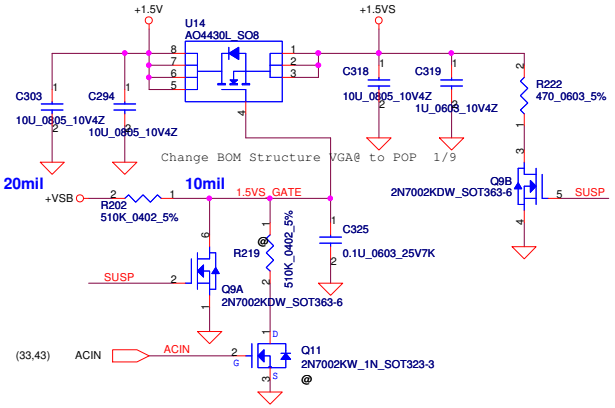
+5VALW TO +5VS

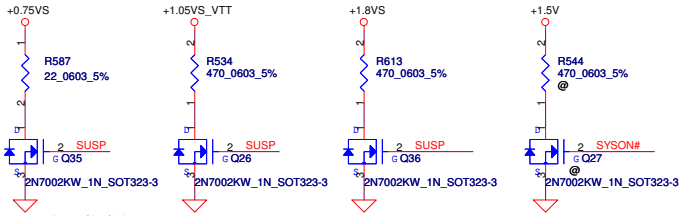


+3VALW TO +3VS



+1.5V to +1.5VS

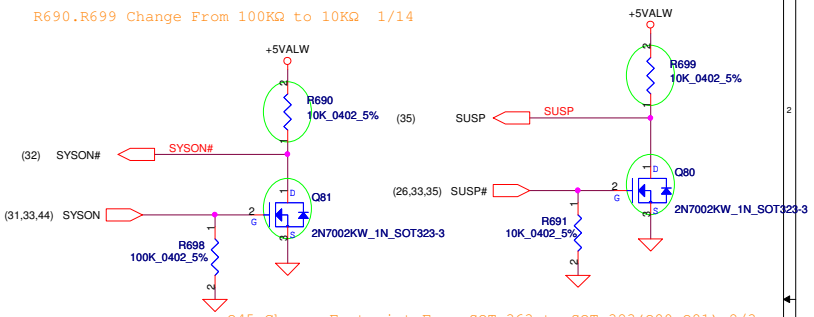




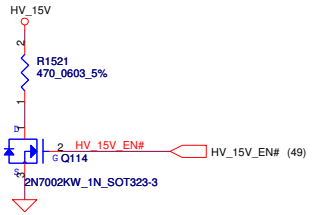
2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge

Del +3VLAWS to +3V 1/8
Del +5VLAWS to +5V 1/8

R690.R699 Change From 100KΩ to 10KΩ 1/14



Q45 Change Footprint From SOT-363 to SOT-323(Q80,Q81) 2/3



4/6 remove

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Compal Electronics, Inc.

Title: ***DC Interface***

Size	Document Number	Rev
B	***PAU30 M/B LA-6392P Schematic***	0.1

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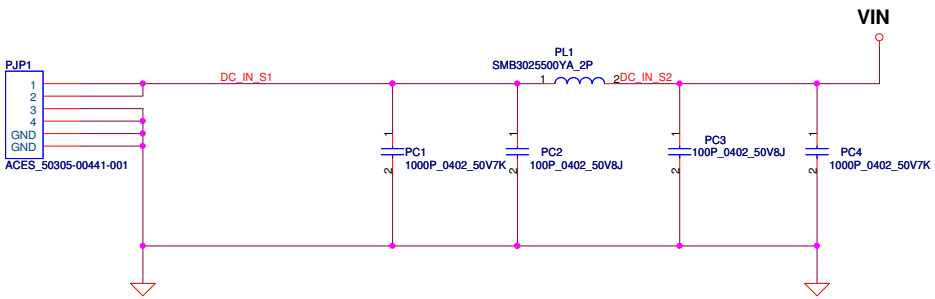

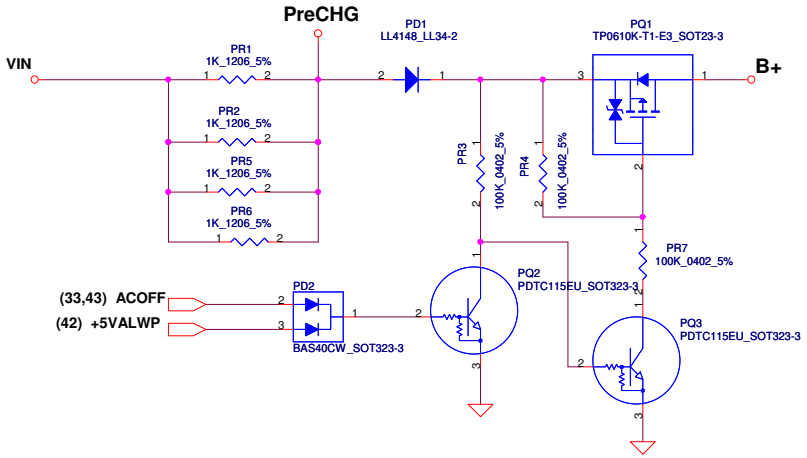

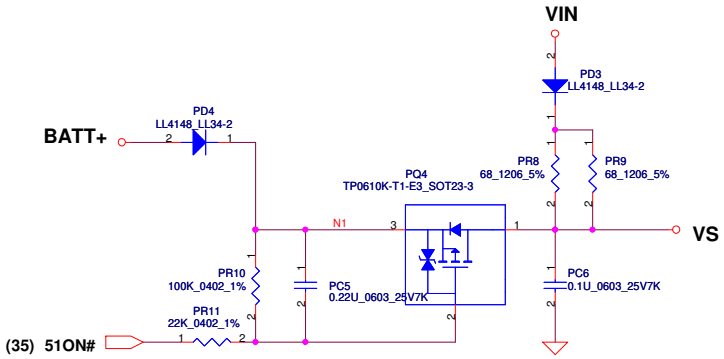

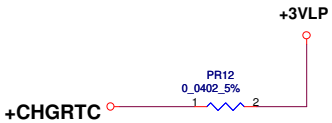

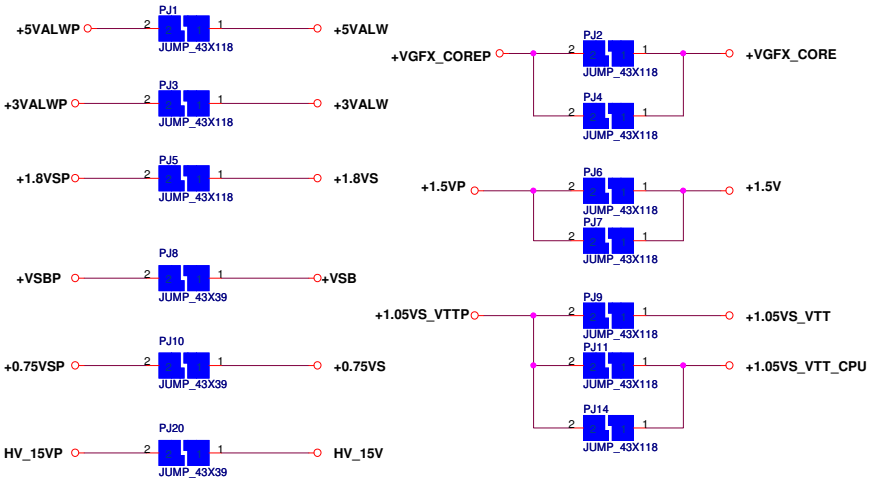

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Issued Date	2009/11/23	Deciphered Date	2010/11/23

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Compal Electronics, Inc.

Title: **DCIN & PRECHARGE**

Size	Document Number	Rev
Custom	SR40 Schematic	0.1

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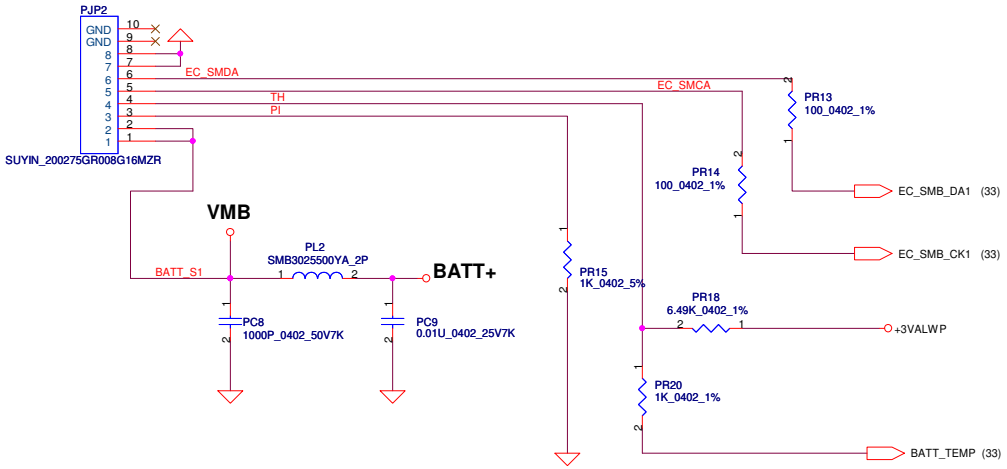
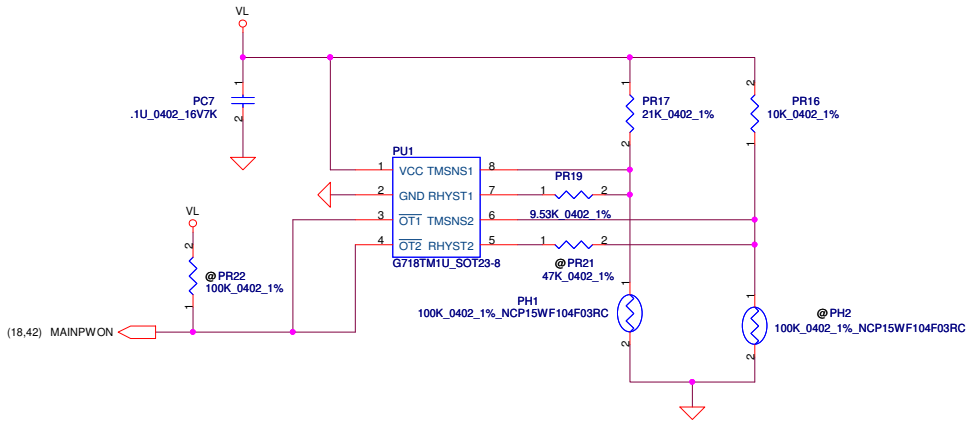
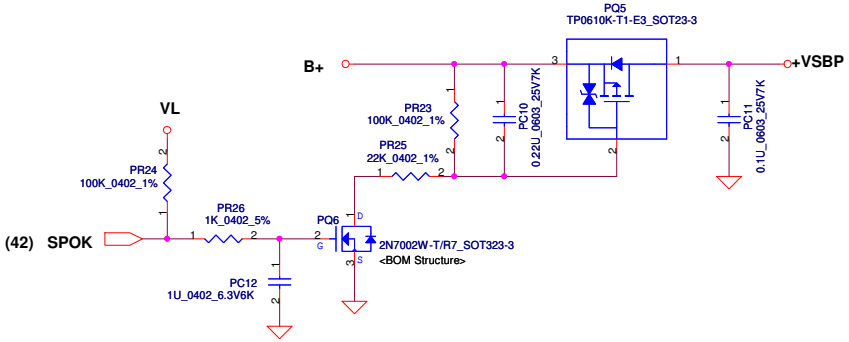


PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





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Compal Electronics, Inc.

Title: **BATTERY CONN / OTP**

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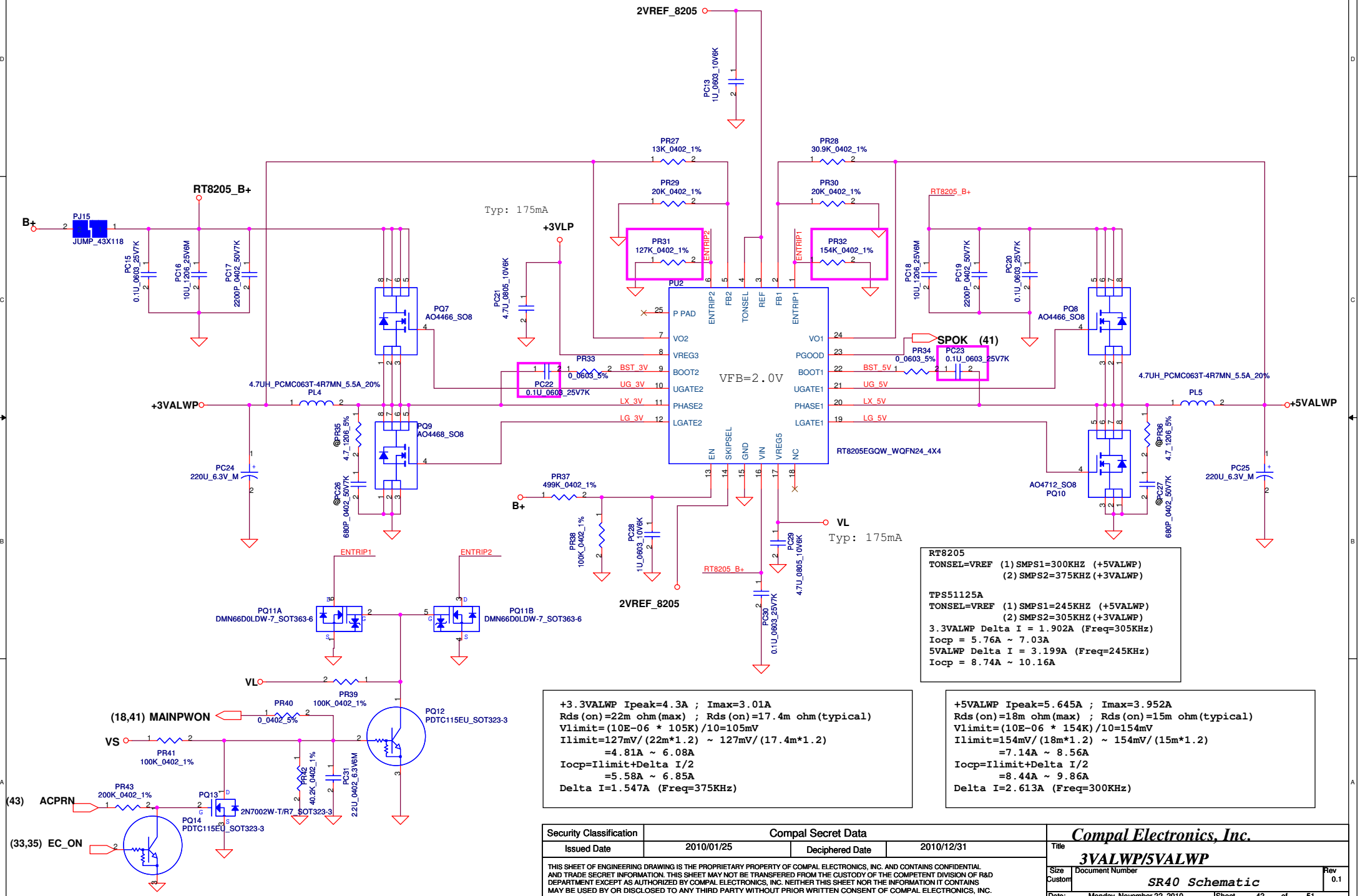
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



RT8205
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ(+3VALWP)

TPS51125A
TONSEL=VREF (1)SMPS1=245KHZ (+5VALWP)
(2)SMPS2=305KHZ(+3VALWP)
3.3VALWP Delta I = 1.902A (Freq=305KHz)
Iocp = 5.76A ~ 7.03A
5VALWP Delta I = 3.199A (Freq=245KHz)
Iocp = 8.74A ~ 10.16A

+3.3VALWP Ipeak=4.3A ; Imax=3.01A
Rds(on)=22m ohm(max) ; Rds(on)=17.4m ohm(typical)
Vlimit=(10E-06 * 105K)/10=105mV
Ilimit=127mV/(22m*1.2) ~ 127mV/(17.4m*1.2)
=4.81A ~ 6.08A
Iocp=Ilimit+Delta I/2
=5.58A ~ 6.85A
Delta I=1.547A (Freq=375KHz)

+5VALWP Ipeak=5.645A ; Imax=3.952A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(10E-06 * 154K)/10=154mV
Ilimit=154mV/(18m*1.2) ~ 154mV/(15m*1.2)
=7.14A ~ 8.56A
Iocp=Ilimit+Delta I/2
=8.44A ~ 9.86A
Delta I=2.613A (Freq=300KHz)

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Issued Date	2010/01/25	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	SR40 Schematic	0.1

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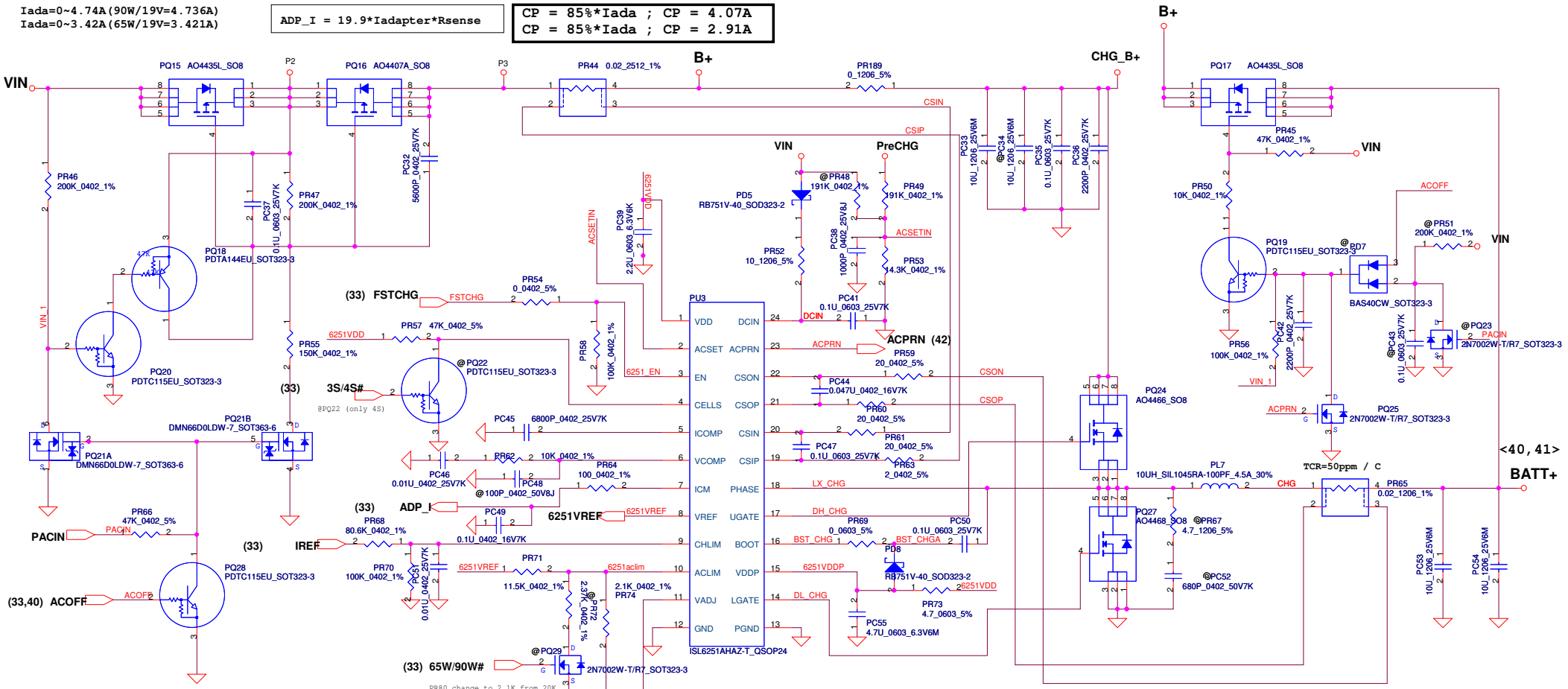
Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(65W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A
where Vaclm=0.392V, Iinput=2.91A

CC=0.6~4.48A
Iref=0.7224*Ichanrge
kI=0.7224
IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

BATT Type	Charging Voltage (0x15)	CV mode
Normal 4S LI-ON Cells	16800mV	16.80V

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Issued Date	2007/09/20	Deciphered Date	2008/09/20

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Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: SR40 Schematic | Rev: 0.1

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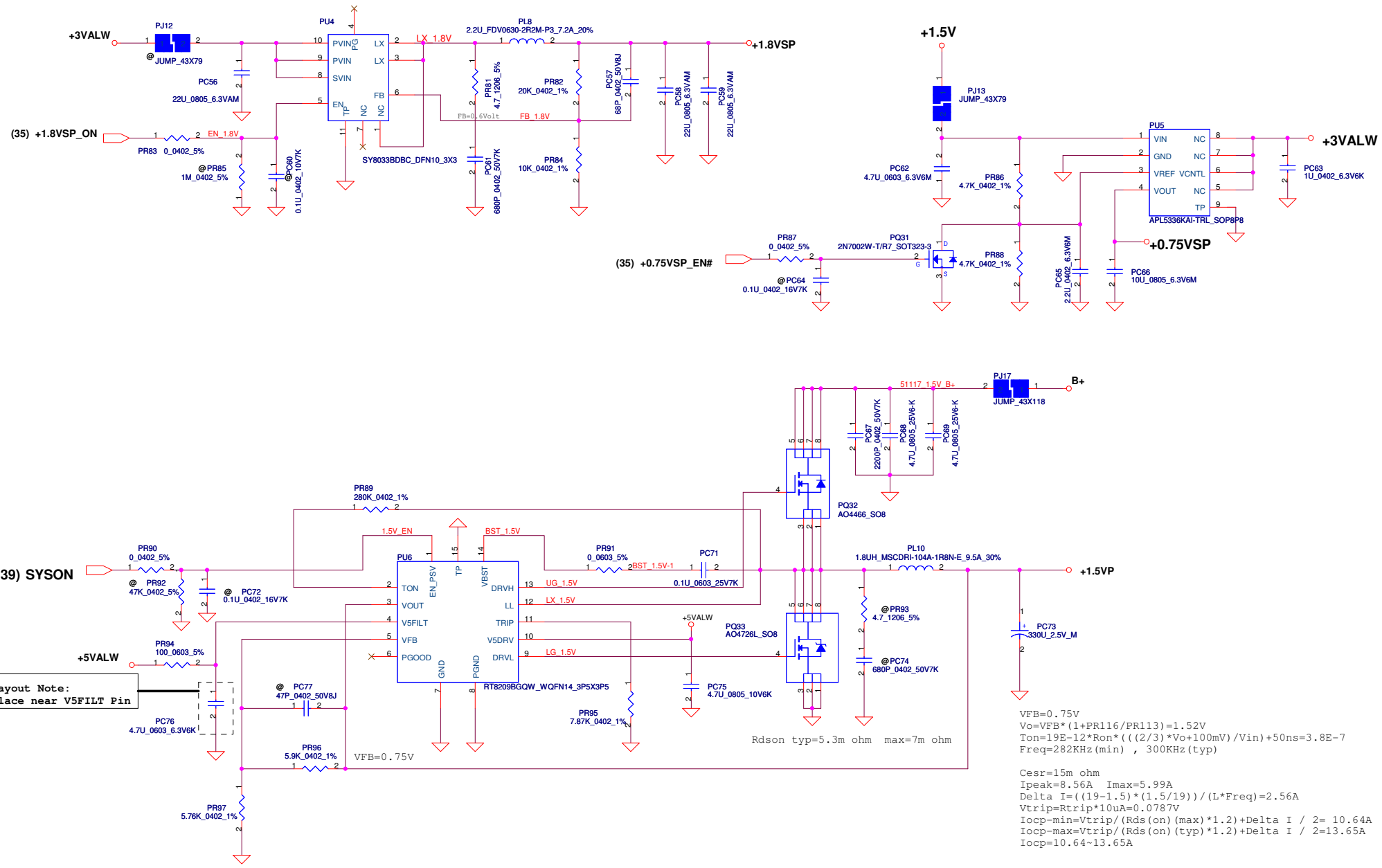
Note:Iload(max)=3.5A



VFB=0.75V
Vo=VFB*(1+PR116/PR113)=1.52V
Ton=19E-12*Ron*(((2/3)*Vo+100mV)/Vin)+50ns=3.8E-7
Freq=282KHz(min) , 300KHz(typ)

Cesr=15m ohm
Ipeak=8.56A Imax=5.99A
Delta I=((19-1.5)*(1.5/19))/(L*Freq)=2.56A
Vtrip=Rtrip*10uA=0.0787V
Iocp-min=Vtrip/(Rds(on)(max)*1.2)+Delta I / 2= 10.64A
Iocp-max=Vtrip/(Rds(on)(typ)*1.2)+Delta I / 2=13.65A
Iocp=10.64~13.65A

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

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Compal Electronics, Inc.

Title: **+1.8VSP/+1.5VP/+0.75VSP**

Size	Document Number	Rev
Custom	*SR40 Schematic*	0.1

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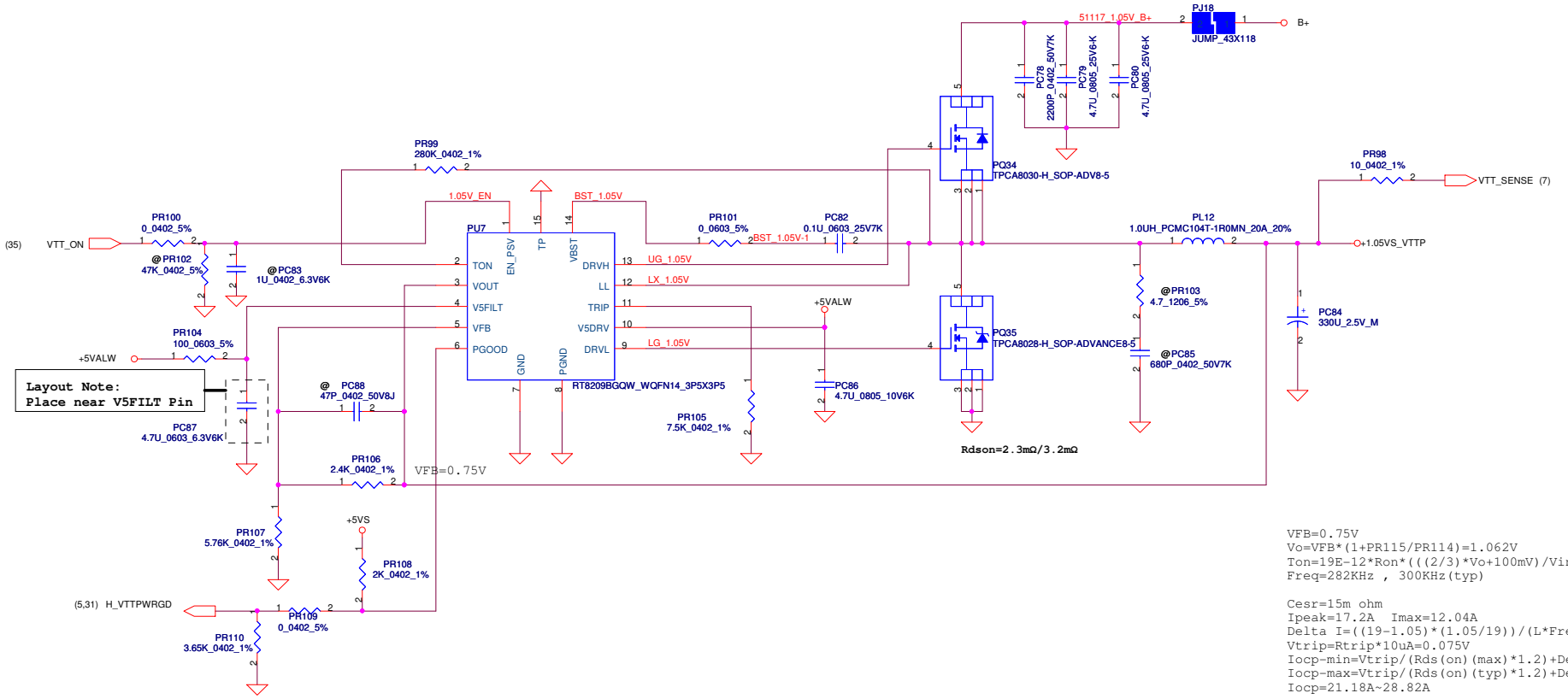

VFB=0.75V
Vo=VFB*(1+PR115/PR114)=1.062V
Ton=19E-12*Ron*(((2/3)*Vo+100mV)/Vin)+50ns=2.74E-07
Freq=282KHz , 300KHz(typ)

Cesr=15m ohm
Ipeak=17.2A Imax=12.04A
Delta I=((19-1.05)*(1.05/19))/(L*Freq)=3.306A
Vtrip=Rtrip*10uA=0.075V
Iocp-min=Vtrip/(Rds(on)(max)*1.2)+Delta I / 2= 21.18A
Iocp-max=Vtrip/(Rds(on)(typ)*1.2)+Delta I / 2=28.82A
Iocp=21.18A~28.82A

Security Classification	Compal Secret Data		
Issued Date	2009/11/23	Deciphered Date	2010/11/23

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Compal Electronics, Inc.

Title: **+1.05VS_VTTP**

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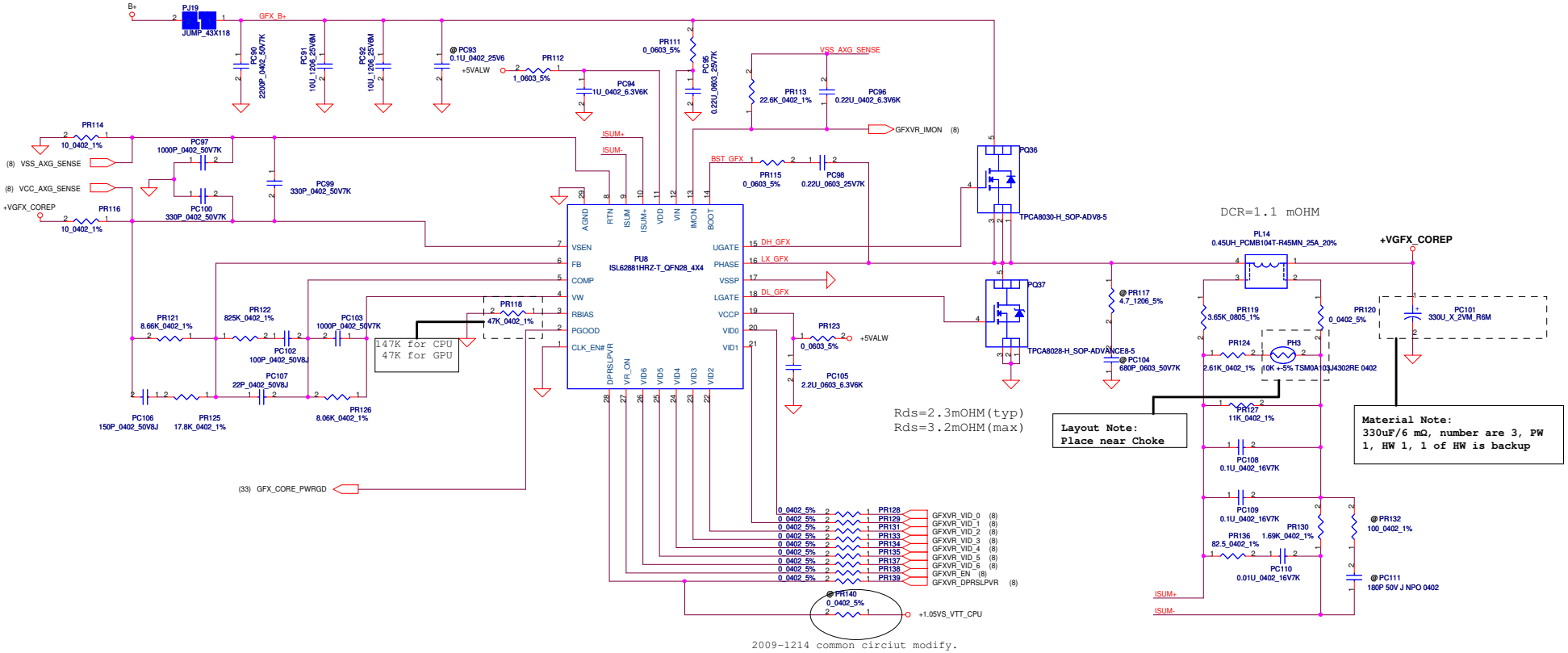
Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR127 // (PR124+PH3)=5.875k ohm
Rsum=PR119=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR121=2.87k ohm, Ri=PR130=562 ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A

Vvid = 1.25
LL = 7m ohm
Iccaxg = 22A
Icctdc_axg = 12 A
Iccaxg_dyn 19 A



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/4/15	Deciphered Date	2010/04/15
Title	GFX_COREP		
Size C	Document Number SR40 Schematic		Rev 0.1
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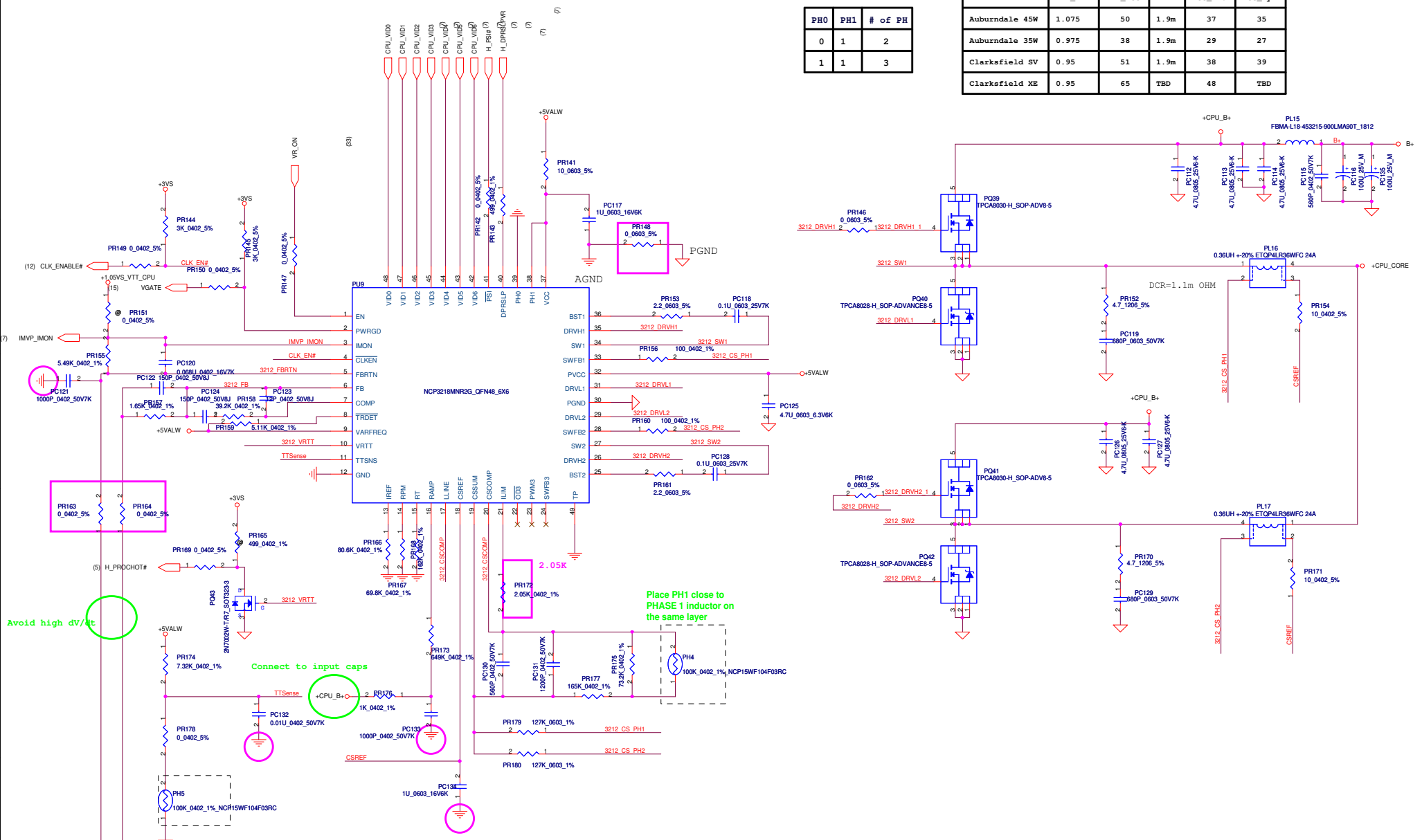
PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Ipeak = 38A, Imax = 29A
Delta I = 8.56A
RILIM = Vdroop/ILIM = Iocp*Ro/20uA
RILIM = 2.05K ohm, Iocp = 43A, Ro = LL = 1.9m ohm
Rcs = (PH4*PR175)/(PH4+PR175) + PR177 = 207K ohm
Ro = Rcs*Rsense / PR179
Ro = LL = 1.9m ohm, Rcs = 207K ohm, Rsense = DCR = 1.1m ohm, so PR179 = 137K ohm

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Issued Date	2009/02/04	Deciphered Date	2010/02/04

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Compal Electronics, Inc.			
Title	CPU_CORE		
Size C	Document Number SR40 Schematic		Rev 0.1
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	change bead to jamp	6 layers change to 8 layers, so change bead to jamp	0.1	50	1 del PC14 SE074681K80 (S CER CAP 680P 50V K X7R 0402) 2 del PL3 SM010016380 (FBMA-L11-322513-201LMA40T)	2010-0617	to DVT
2	change bead to jamp	6 layers change to 8 layers, so change bead to jamp	0.1	51	del PL6 SM010016380 (FBMA-L11-322513-201LMA40T)	2010-0617	to DVT
3	change bead to jamp	6 layers change to 8 layers, so change bead to jamp	0.1	52	1 del PC70 SE074561K80 (S CER CAP 560P 50V K X7R 0402) 2 del PL9 SM010016380 (FBMA-L11-322513-201LMA40T)	2010-0617	to DVT
4	change bead to jamp	6 layers change to 8 layers, so change bead to jamp	0.1	53	1 del PC81 SE074561K80 (S CER CAP 560P 50V K X7R 0402) 2 del PL11 SM010020720 (FBMA-L18-453215-900LMA90T)	2010-0617	to DVT
5	change bead to jamp	6 layers change to 8 layers, so change bead to jamp	0.1	54	1 del PC89 SE074561K80 (S CER CAP 560P 50V K X7R 0402) 2 del PL13 SM010016380 (FBMA-L11-322513-201LMA40T)	2010-0617	to DVT
6	change main souce	cost down	0.1	54	Chnage PQ36 from SB000008L80(S TR SI7686DP-T1-E3 1N POWERPAK SO8) to SB00000HL00(S TR TPCA8030-H 1N SOP-ADV) change PQ37 from SB000009F80(S TR AO4456 1N SO8) to SB00000GL00(S TR TPCA8028-H 1N SOP ADVANCE) Del PQ38 SB000009F80(S TR AO4456 1N SO8)	2010-0617	to DVT
7	reduce components quantity	cost down	0.1	53	Chnage PR104 from SD014100080(S RES 1/10W 100 +-5% 0603) to SD013100080 (S RES 1/10W 100 +-1% 0603)	2010-0624	to DVT
8	reduce components quantity	cost down	0.1	52	Chnage PR94 from SD014100080(S RES 1/10W 100 +-5% 0603) to SD013100080 (S RES 1/10W 100 +-1% 0603)	2010-0624	to DVT
9	change main souce	cost down	0.1	51	Chnage PQ15, PQ17 from SB00000DL00(S TR AO4407A 1P SO8) to SB00000DJ10 (S TR AO4435L 1P SO8)	2010-0624	to DVT
10	change main souce	cost down	0.1	51	Chnage PQ27 from SB00000CG00(S TR AO4466 1N SO8) to SB000009580 (S TR AO4468 1N SO8)	2010-0624	to DVT
11	change main souce	cost down	0.1	50	Chnage PQ9 from SB00000AJ00(S TR AO4712 1N SO8) to SB000009580 (S TR AO4468 1N SO8)	2010-0624	to DVT
12	adjust OCP setting	Because Rds(on) change to 22m(MAX) and 17.4m(TYP) ohm of low side MOS, so change OCP setting	0.1	50	Chnage PR31 from SD034105380(S RES 1/16W 105K +-1% 0402) to SD034127380 (S RES 1/16W 127K +-1% 0402)	2010-0624	to DVT
13	change main souce	ISL62881C has hang up issue, so change to ISL62881.	0.2	54	Chnage PU8 from SA000043N00(S IC ISL62881CHRZ-T QFN 28P PWM) to SA000030200 (S IC ISL62881HRZ-T QFN 28P PWM)	2010-0713	to DVT
14	adjust resistance value	adjust resistance value for ISL62881	0.2	54	Chnage PR113 from SD034750180(S RES 1/16W 7.5K +-1% 0402) to SD034226280 (S RES 1/16W 22.6K +-1% 0402)	2010-0713	to DVT
15	adjust resistance value	adjust resistance value for ISL62881	0.2	54	Chnage PR121 from SD034287180(S RES 1/16W 2.87K +-1% 0402) to SD034866180 (S RES 1/16W 8.66K +-1% 0402)	2010-0713	to DVT
16	adjust resistance value	adjust resistance value for ISL62881	0.2	54	Chnage PR130 from SD000009380(S RES 1/16W 562 +-1% 0402) to SD00000JB80 (S RES 1/16W 1.69K +-1% 0402)	2010-0713	to DVT
17	add resistance	pop resistance for ISL62881	0.2	54	add PR136 SD034825A80(S RES 1/16W 82.5 +-1% 0402)	2010-0713	to DVT
18	add cup.	pop Cup. for ISL62881	0.2	54	add PC110 SE076103K80(S CER CAP .01U 16V K X7R 0402)	2010-0713	to DVT
19	adjust capacitor	Because ME height limit, so change to 8 height capacitor.	0.2	55	Chnage PC116 from SF22004M210(S ELE CAP 220U 25V M 8X10.2 CE-AX) to SF000000S80 (S ELE CAP 100U 25V M 6.3X7.7 CE-LX)	2010-0713	to DVT
20	add cup.	Because ME height limit, so add an 8 height capacitor.	0.2	55	Add PC135 SF000000S80 (S ELE CAP 100U 25V M 6.3X7.7 CE-LX)	2010-0713	to DVT
21	adjust resistance value	adjust resistance value for CPU loadline	0.2	55	Chnage PR179 and PR180 from SD014137380(S RES 1/10W 137K +-1% 0603) to SD014127380(S RES 1/10W 127K +-1% 0603)	2010-0715	to DVT
22	adjust resistance value	adjust resistance value for +5Valwp to 5.1V	0.2	50	Chnage PR28 from SD034300280(S RES 1/16W 30K +-1% 0402) to SD034309280(S RES 1/16W 30.9K +-1% 0402)	2010-0723	to DVT

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Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number | Rev: 0.1

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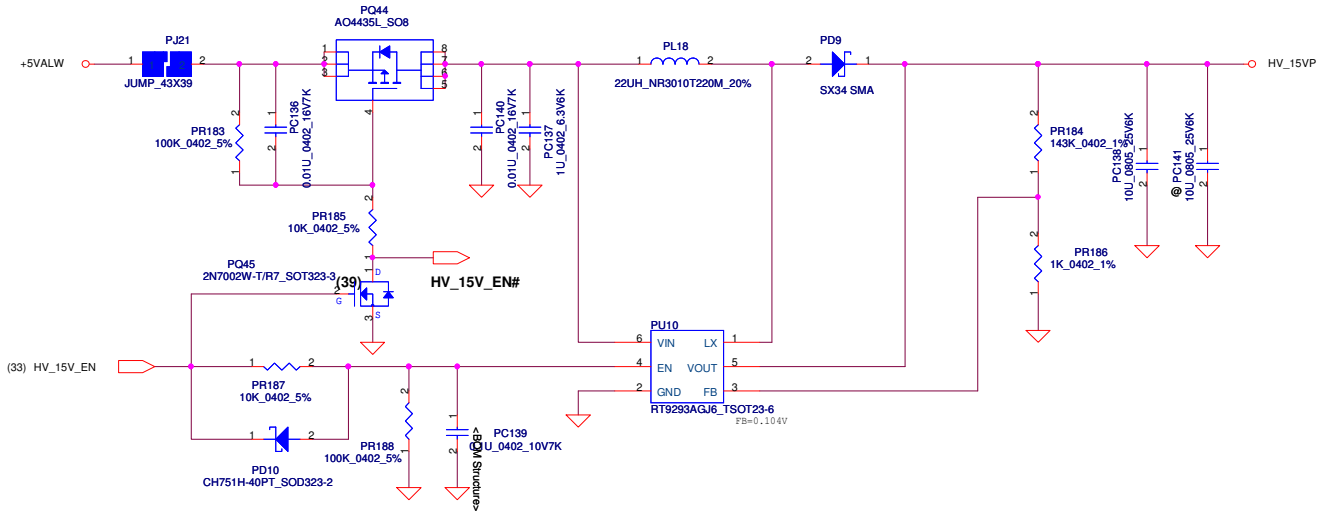

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Compal Electronics, Inc.

Title: 12V

Size	Document Number	Rev
		0.3

Date: Monday, November 22, 2010 | Sheet 49 of 51

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	EMI reguest reserve 0 ohm	EMI reguest reserve 0 ohm for EMI ISN test	0.3	43	change PJ16 to SD011000080(S RES 1/4W 0 +-5% 1206)	2010-0907	PVT
2	Add boost resister	EMI reguest add boost resister for EMI test	0.3	47	change PR153 and PR161 form SD013000080 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)	2010-0907	PVT
3	Add snubber	EMI reguest add snubber for EMI test	0.3	47	Add PR152 and PR170 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC119 and PC129 SE025681K80(S CER CAP 680P 50V K X7R 0603)	2010-0907	PVT
4	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PU10 SA00004DD00(S IC RT9293AGJ6 TSOT-23 6P BOOST) Add PL18 SHI00005P00(S INDUC_ 22UH +-20% NR3010T220M)	2010-0907	PVT
5	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PD9 SCSSSM24A20(S DIO SSM24APT SMA-S) Add PQ44 SB00000DJ10(S TR AO4435L 1P SO8) Add PQ45 SB000006800(S TR 2N7002W T/R7 1N SOT-323)	2010-0907	PVT
6	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PD10 SC1H751H010(S DIO CH751H-40PT SOD323) Add PR183, PR188 SD028100380(S RES 1/16W 100K +-5% 0402) Add PR185, PR187 SD028100280(S RES 1/16W 10K +-5% 0402)	2010-0907	PVT
7	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PC136, PC140 SE076103K80(S CER CAP .01U 16V K X7R 0402) Add PC137 SE000000U00(S CER CAP 1U 16V K X5R 0402) Add PC139 SE102104K00(S CER CAP 0.1U 10V +-10% X7R 0402)	2010-0907	PVT
8	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PR184 SD034143380(S RES 1/16W 143K +-1% 0402) Add PR186 SD034100180(S RES 1/16W 1K +-1% 0402)	2010-0907	PVT
9	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PC138 SE00000QK00(S CER CAP 10U 25V K X5R 0805 H1.25)	2010-0907	PVT
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Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

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Title: PIR (PWR)

Size	Document Number	Rev
Custom		0.1

Date: Thursday, October 28, 2010 Sheet 50 of 51

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1			0.1	48			
2			0.1	50			
3			0.1	51			
4			0.1	51			
5			0.1	52			
6			0.1	53			
7			0.1	46			
8			0.1	47			
9			0.1	52			
10			0.1	48			
11			0.1	52			
12			0.1	52			
13			0.2	46			
14			0.2	51			
15			0.2	52			
16			0.2	53			
17			0.2	52			
18			0.2	50			
19			0.2	55			
20			0.2	53			
21			0.2	55			
22			0.2	48			
23			0.2	52			

Security Classification	Compal Secret Data		
Issued Date	2009/11/23	Deciphered Date	2010/11/23

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Title: PIR (PWR)

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