


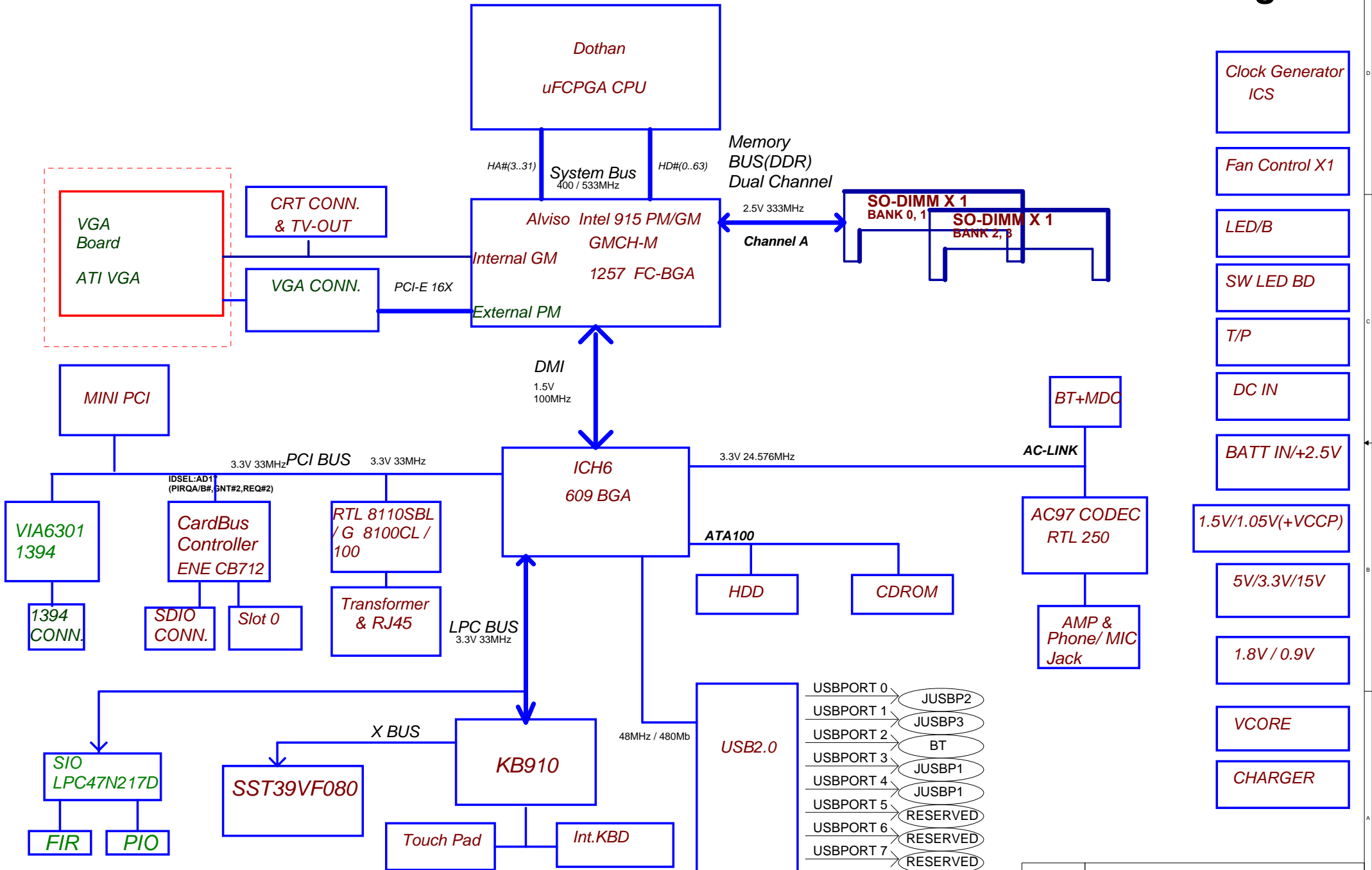
Project Code : AL50/1

Date : 2004-06-02

Revision : 0.2

AL50/1 Intel Sonoma platform Used the Alvisio and I CH6-M

	<b>Compal Electronics, Inc.</b>		
	Title		
	<b>Function</b>		
	Size	Document Number	Rev
	<b>LA-2361</b>	0.0	
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# I2C / SMBUS ADDRESSING

## External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD17	0	F
CARD BUS	AD20	1	A
Cardreader			B
1394	AD16	2	E
Wireless LAN(MINI PCI)	AD18	3	G,H

@ Depop

1@ EAL51

2@ EAL50

1@ EAL51 VALUE (DELETE SIO/1394)

Power Management table

Signal			+CPU_CORE +VCCP +5VS +3VS +2.5VS +1.8VS +1.25VS +1.5VS
State	+12VALW +3VALW +5VALW	+2.5V +3V +5V +12V	
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

Ceramic Capacitor Spec Guide:

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7
CODE	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R

8	9	A	B	C	D	E	F	G
NP0	C0G		BJ	CH	CJ	CK	SH	SJ

H	I	J	
UJ	UK	SL	

Tolerance:

Symbol	A	B	C	D	F	G	H	J
CODE	+/-0.05PF	+/-0.1PF	+/-0.25PF	+/-0.5PF	+/-1PF	+/-2%	+/-3%	+/-5%

K	M	N	P	Q	V	X	Z	
+/-10%	+/-20%	+/-30%	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	


SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	THERMAL SENSOR (LM75)	SODIMM	CLK CHIP	MINI PCI	LCD	VGA Thermal ADM1032
SMB_EC_CK1 SMB_EC_DA1	PC87591L	✓	✓	✓	✗	✗	✗	✗	✗	✗	✗
SMB_EC_CK2 SMB_EC_DA2	PC87591L	✗	✗	✗	✓	✓	✗	✗	✗	✗	✓
ICH_SMBCLK ICH_SMBDATA	ICH6-M	✗	✗	✗	✗	✗	✓	✓	✗	✗	✗
LCD_DDCCLK LCD_DDCDATA	Alviso GM-GP	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗

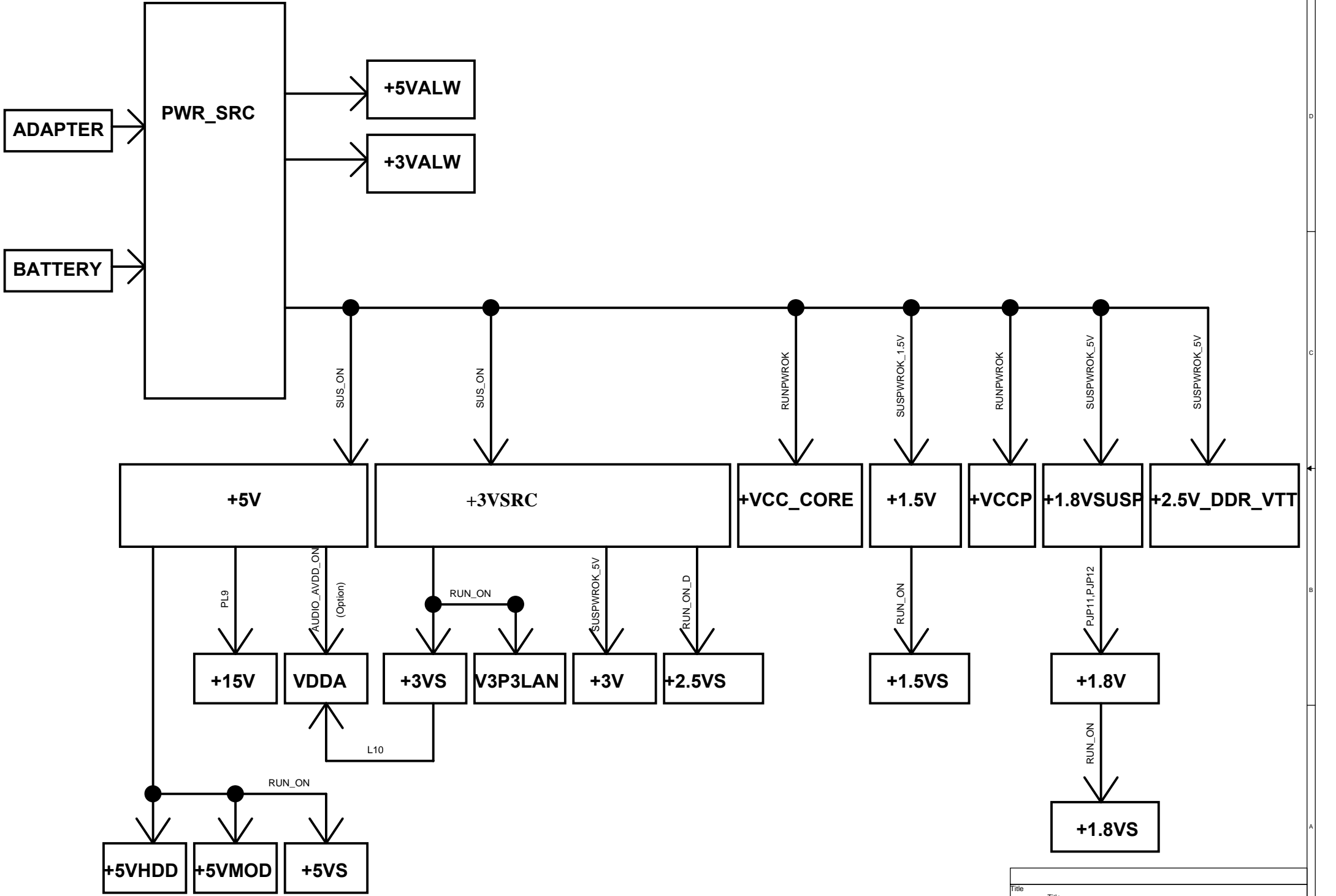
	PCB Rev	Data
Bringup-Build SST-Build	0.1	
PT-Build		
ST-Build		
QT-Build		

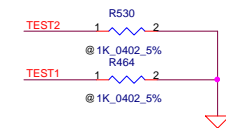
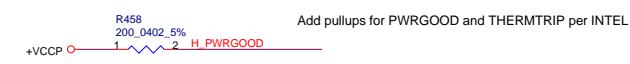
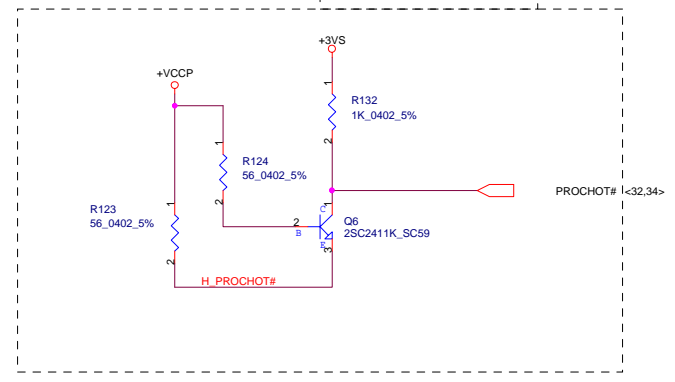
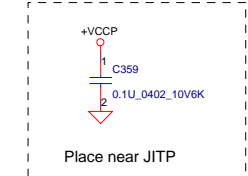
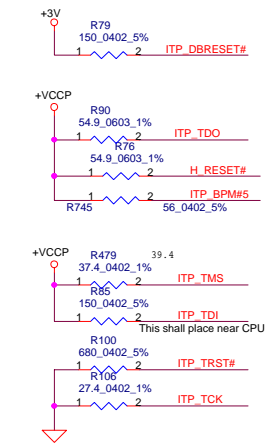
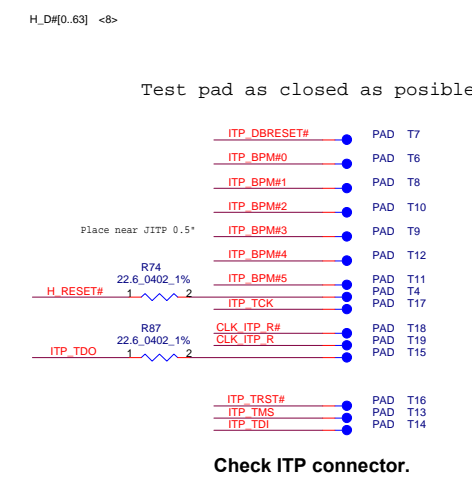
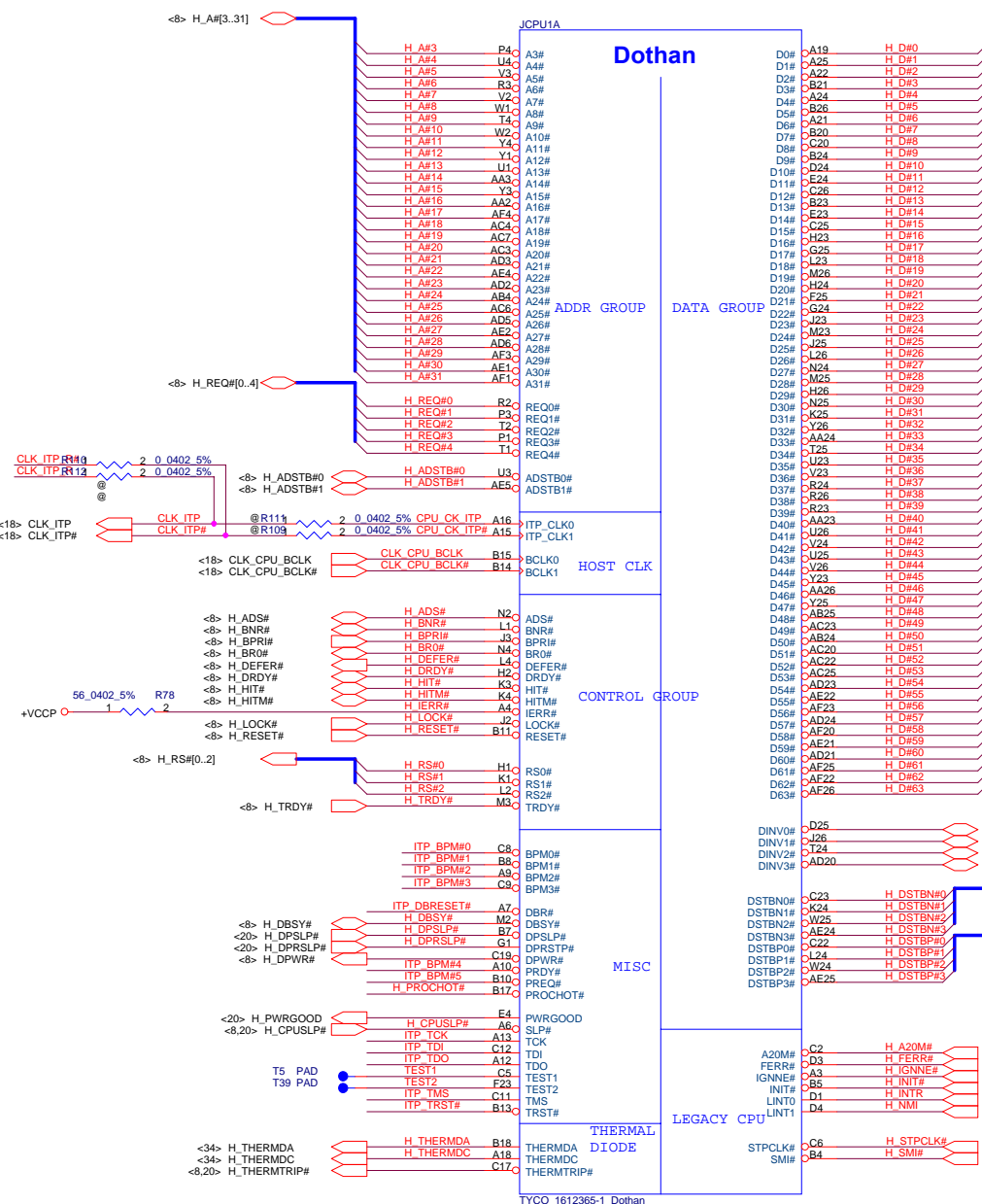
SCHEMATICS VERSION LIST

VERSION	ISSUE DATE	REMARK
0.0A		First Release



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Title: **Dothan Processor(1/2)**

Size: **LA-2361**

Document Number: **LA-2361**

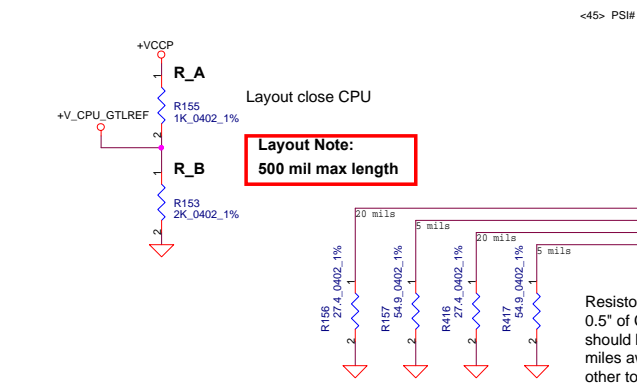
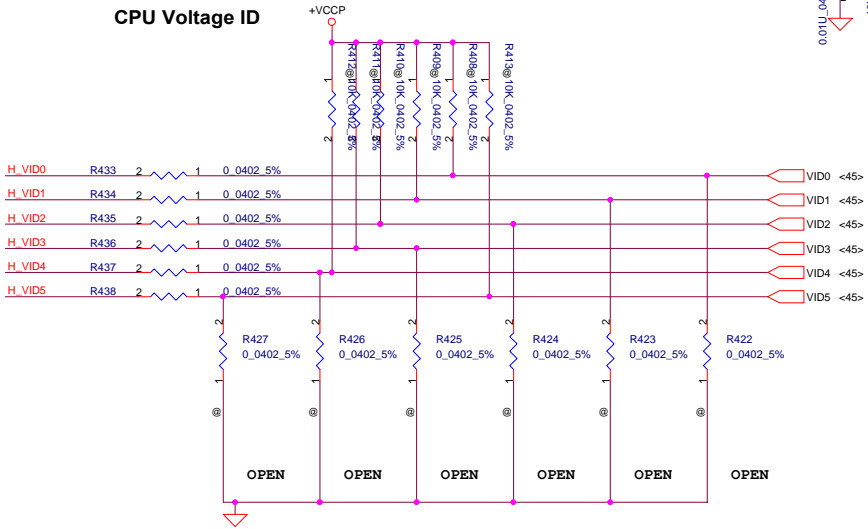
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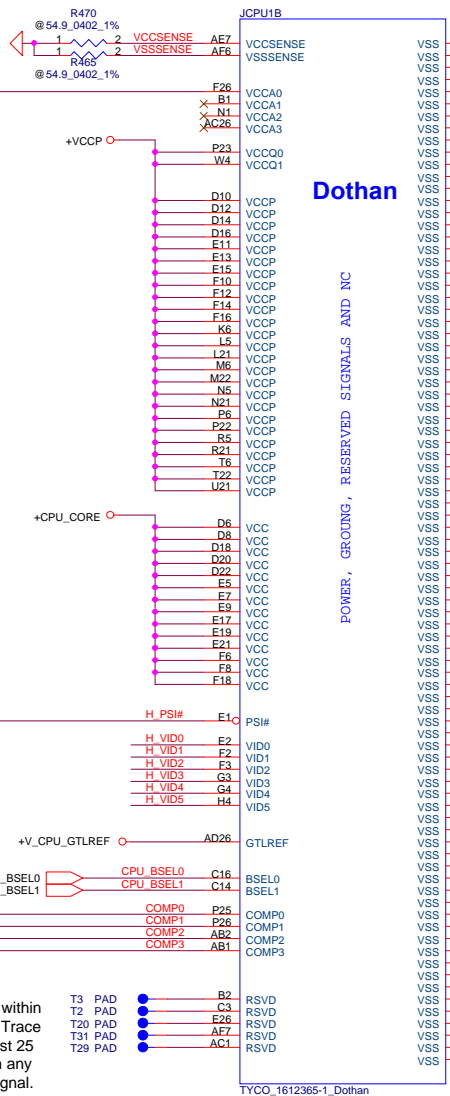
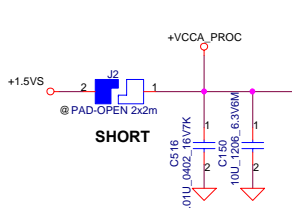
Rev 0.0

For test only ,Cmos output

CPU Voltage ID

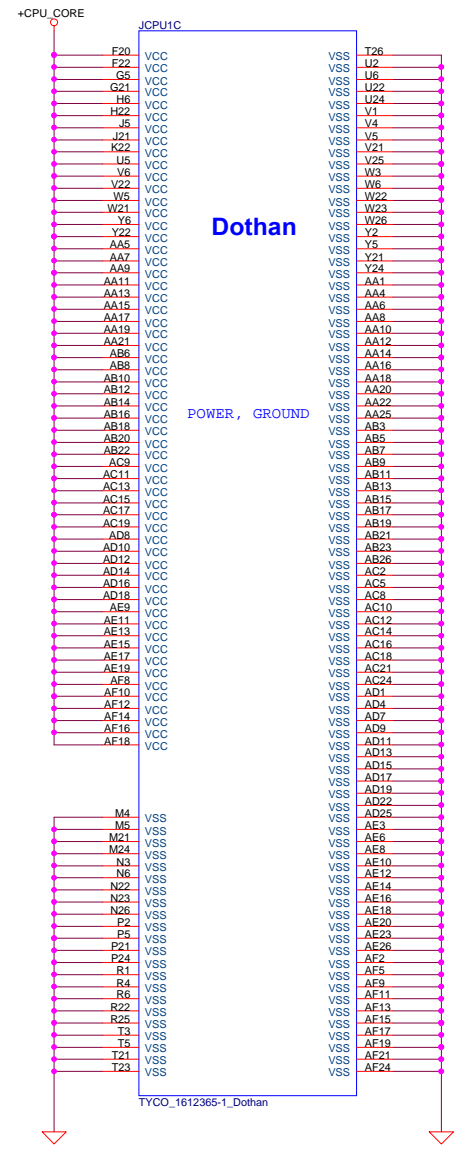


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 miles away from any other toggling signal.



Dothan

POWER, GROUND, RESERVED SIGNALS AND NC



Dothan

POWER, GROUND

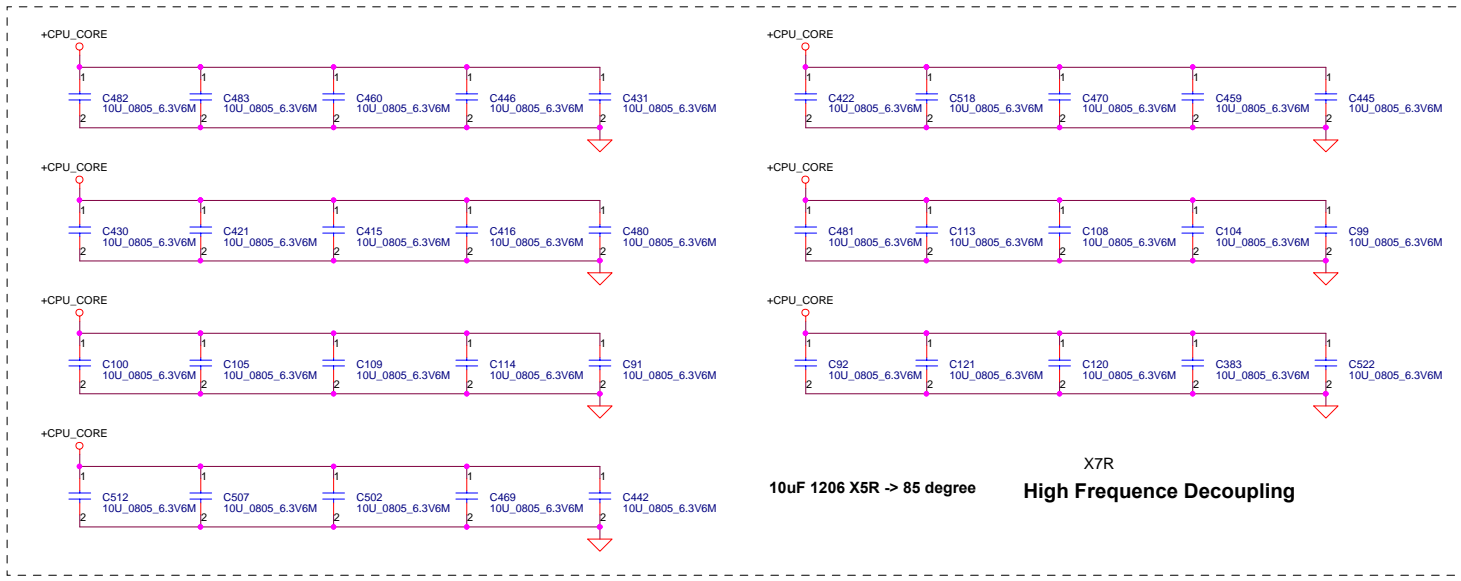
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**Dothan Processor(2/2)**

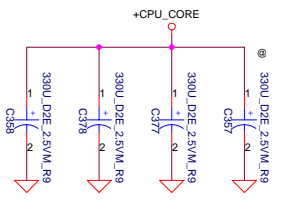
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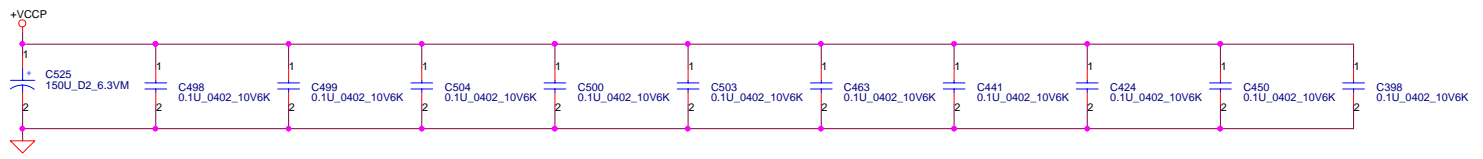


10uF 1206 X5R -> 85 degree X7R  
**High Frequency Decoupling**


**Near VCORE regulator.**



ESR <= 3m ohm  
 Capacitor > 880 uF

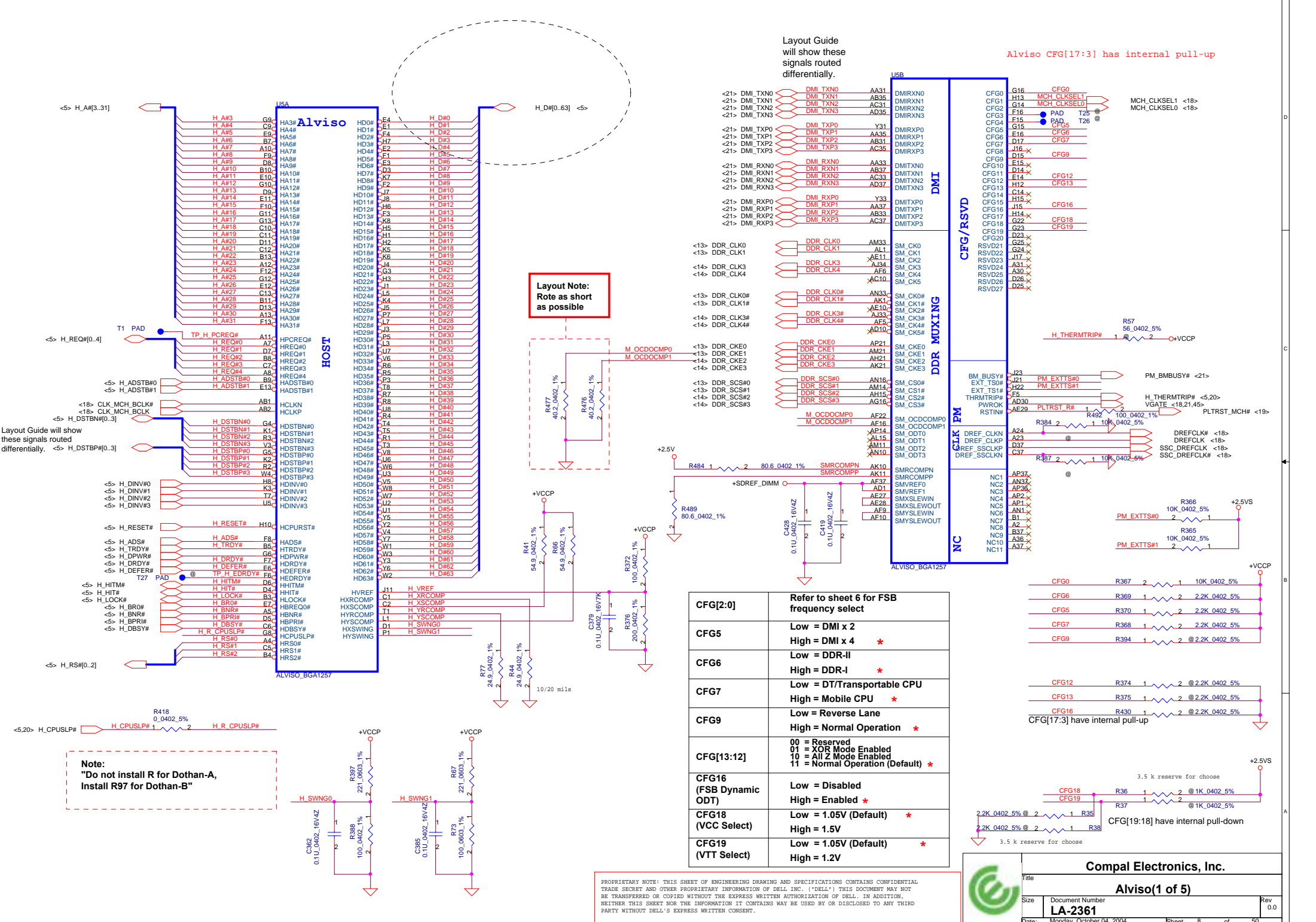


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		<b>Dothan Bypass</b>	
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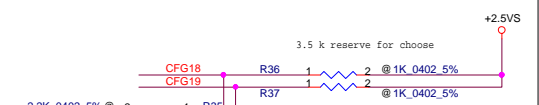
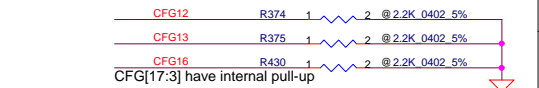
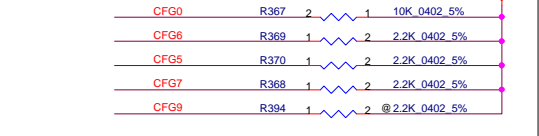
Layout Guide will show these signals routed differentially.

Alviso CFG[17:3] has internal pull-up



**Layout Note:**  
Route as short as possible

CFG2:0]	Refer to sheet 6 for FSB frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	High = DDR-II *
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	High = Normal Operation *
CFG13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V



Layout Guide will show these signals routed differentially.

**Note:**  
"Do not install R for Dothan-A, Install R97 for Dothan-B"

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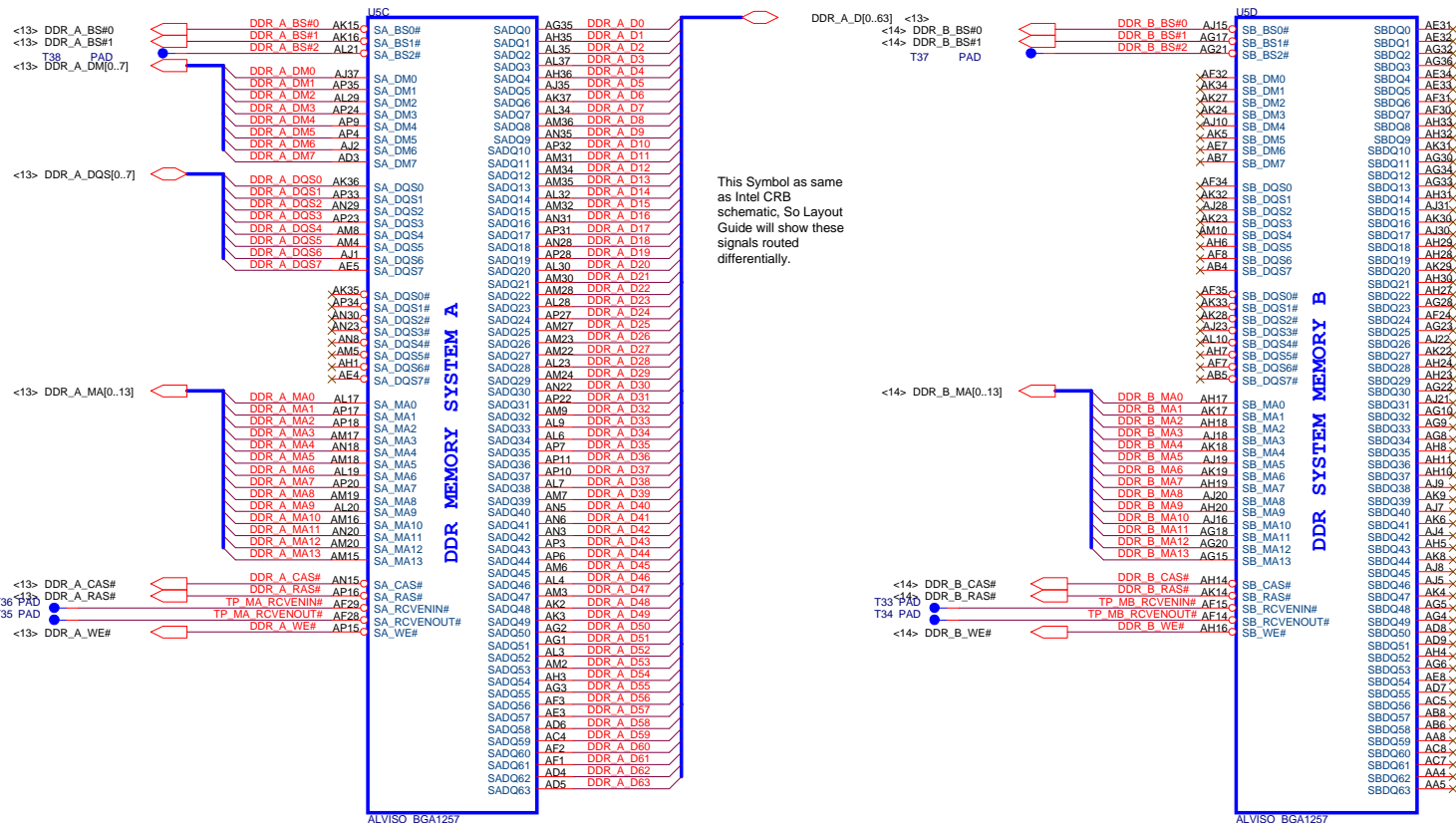
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**Alviso (1 of 5)**

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**DDR MEMORY SYSTEM A**  
 ALVISO\_BGA1257

**DDR SYSTEM MEMORY B**  
 ALVISO\_BGA1257

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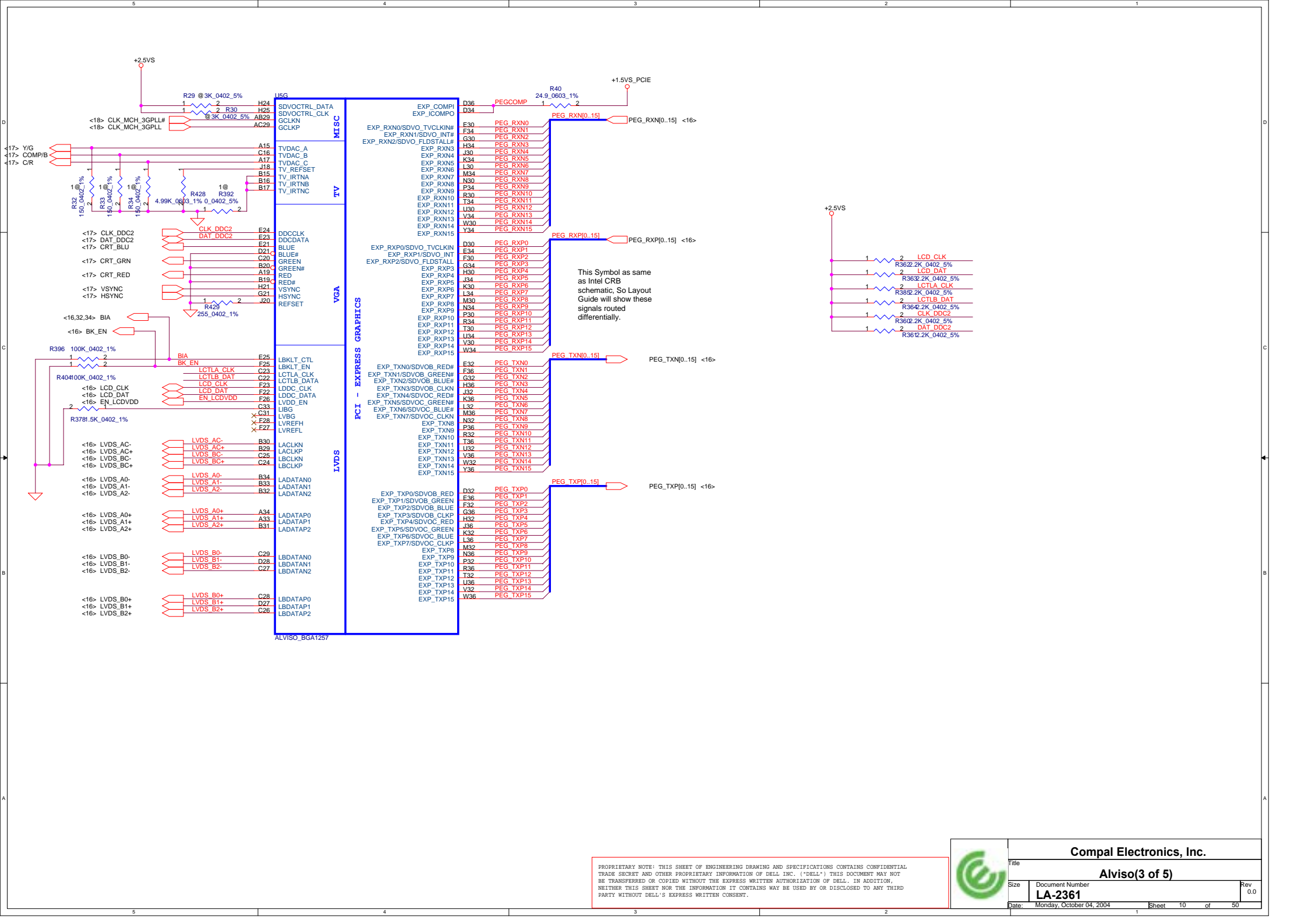
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Alviso (2 of 5)



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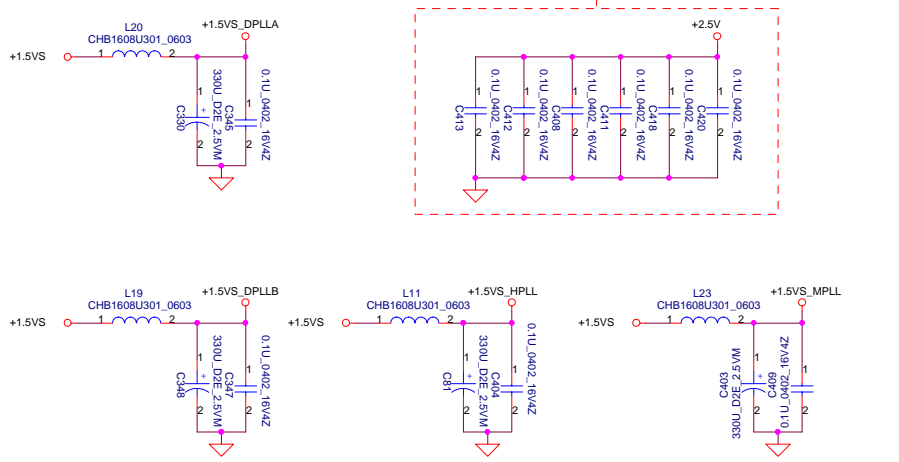
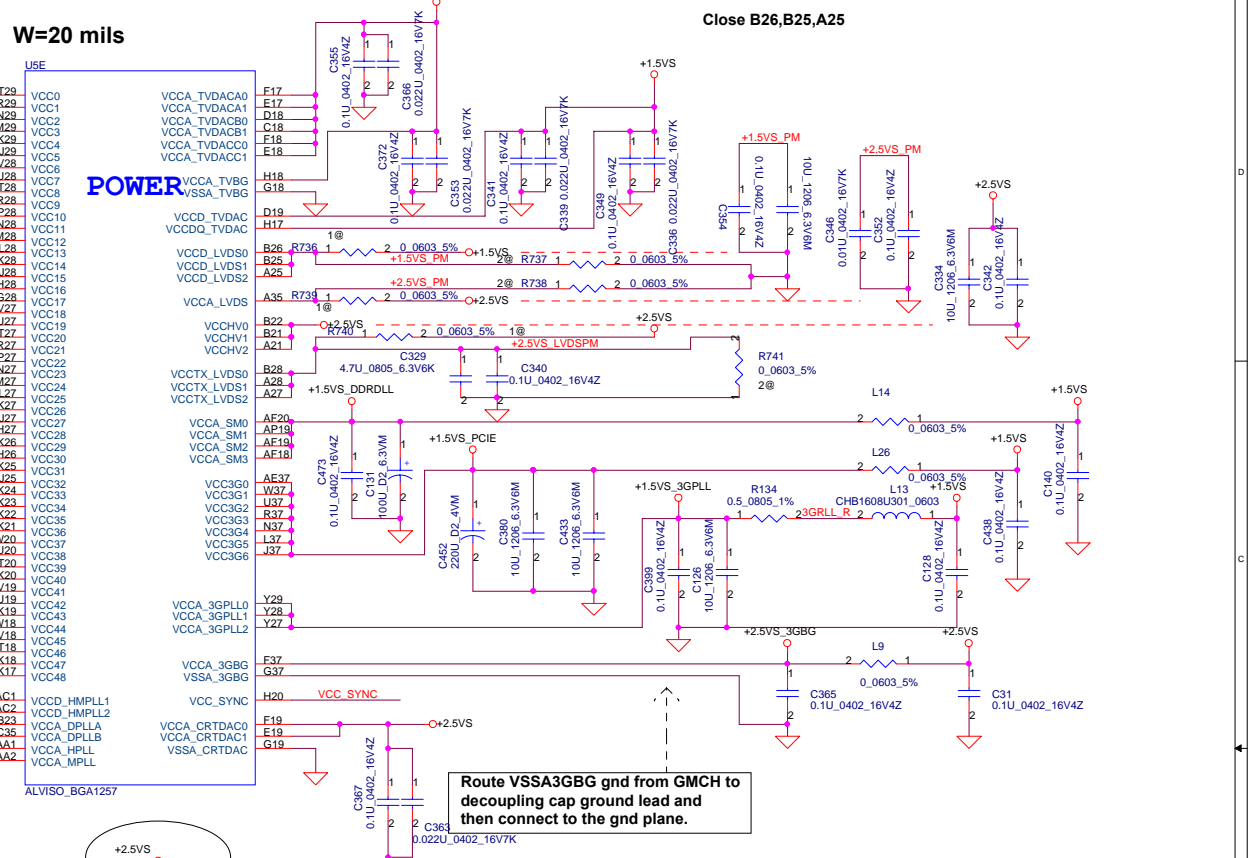
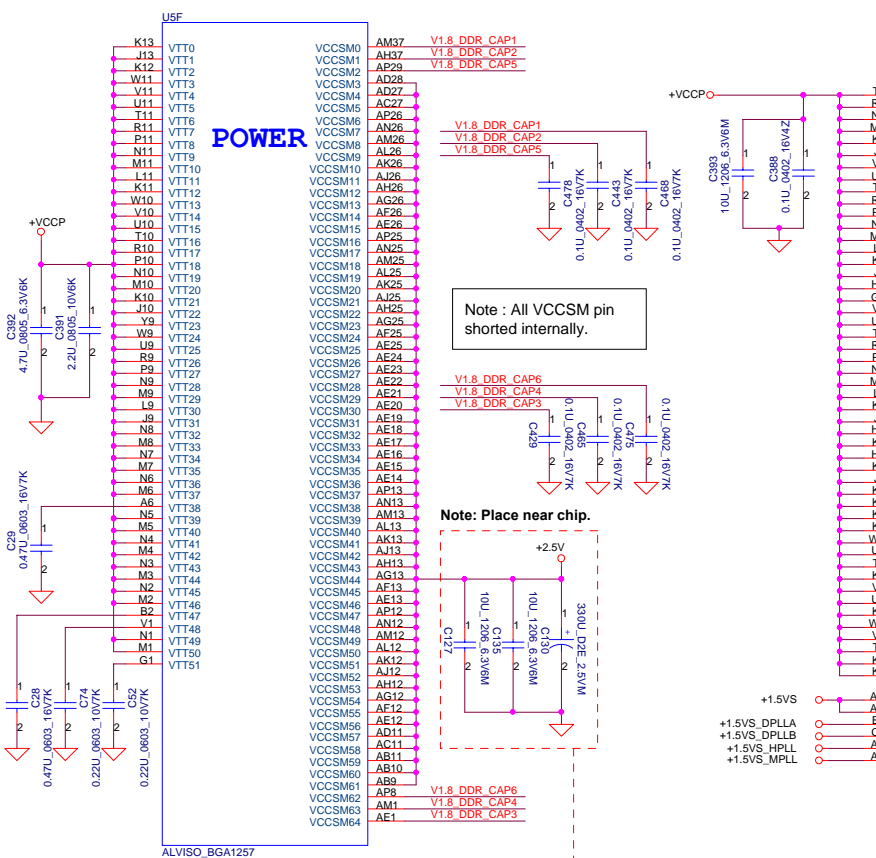


ALVISO\_BGA1257

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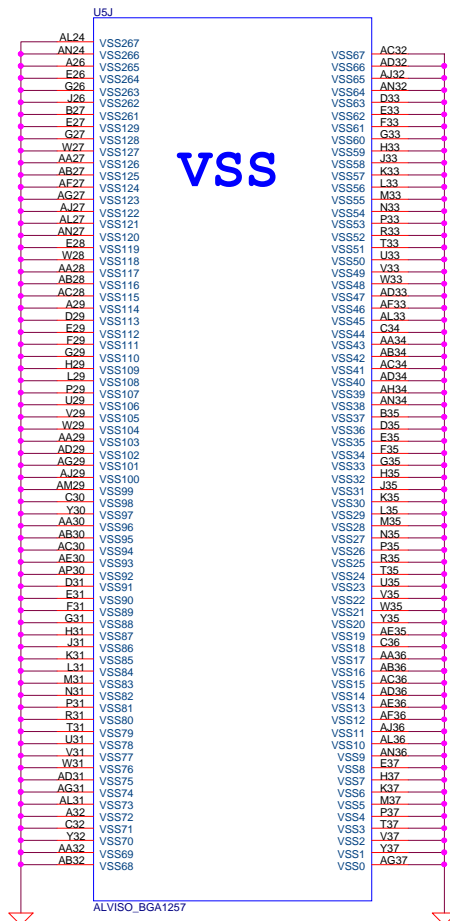
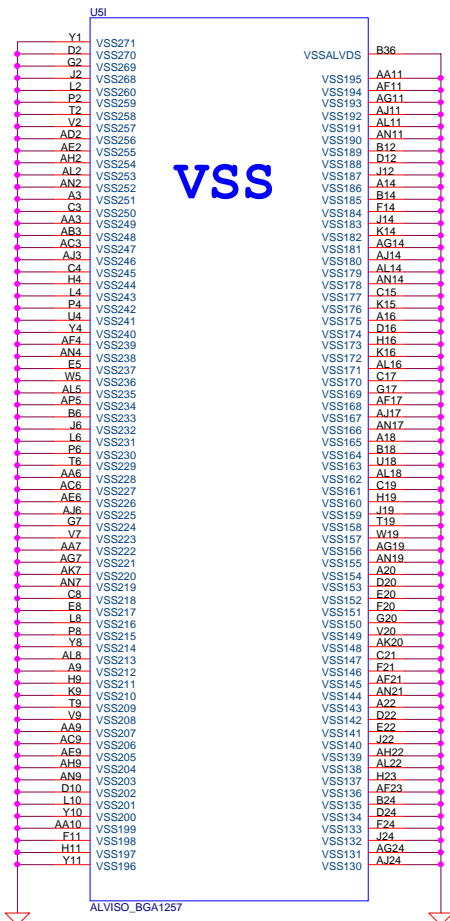
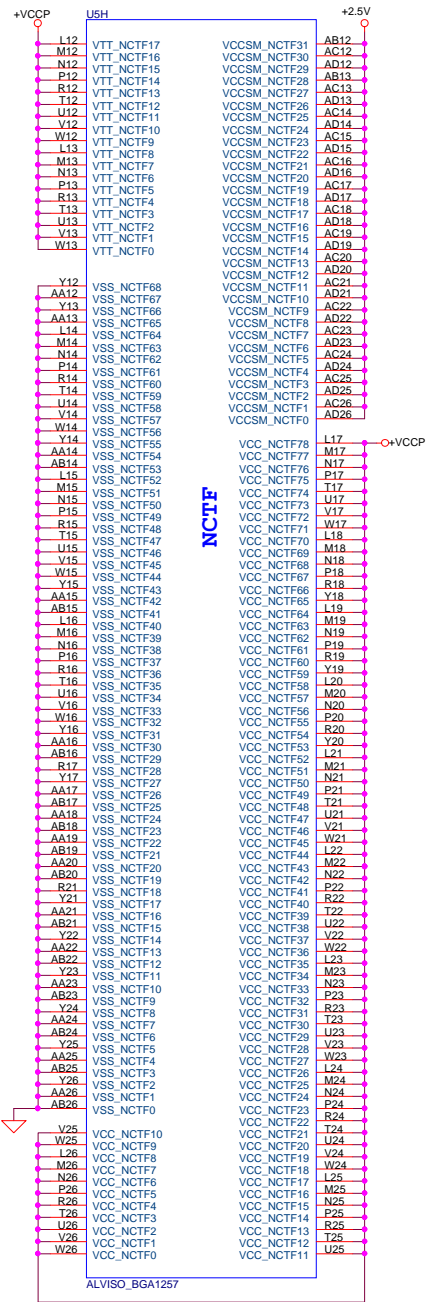


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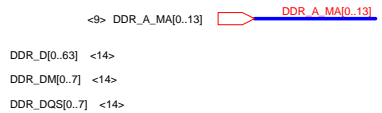
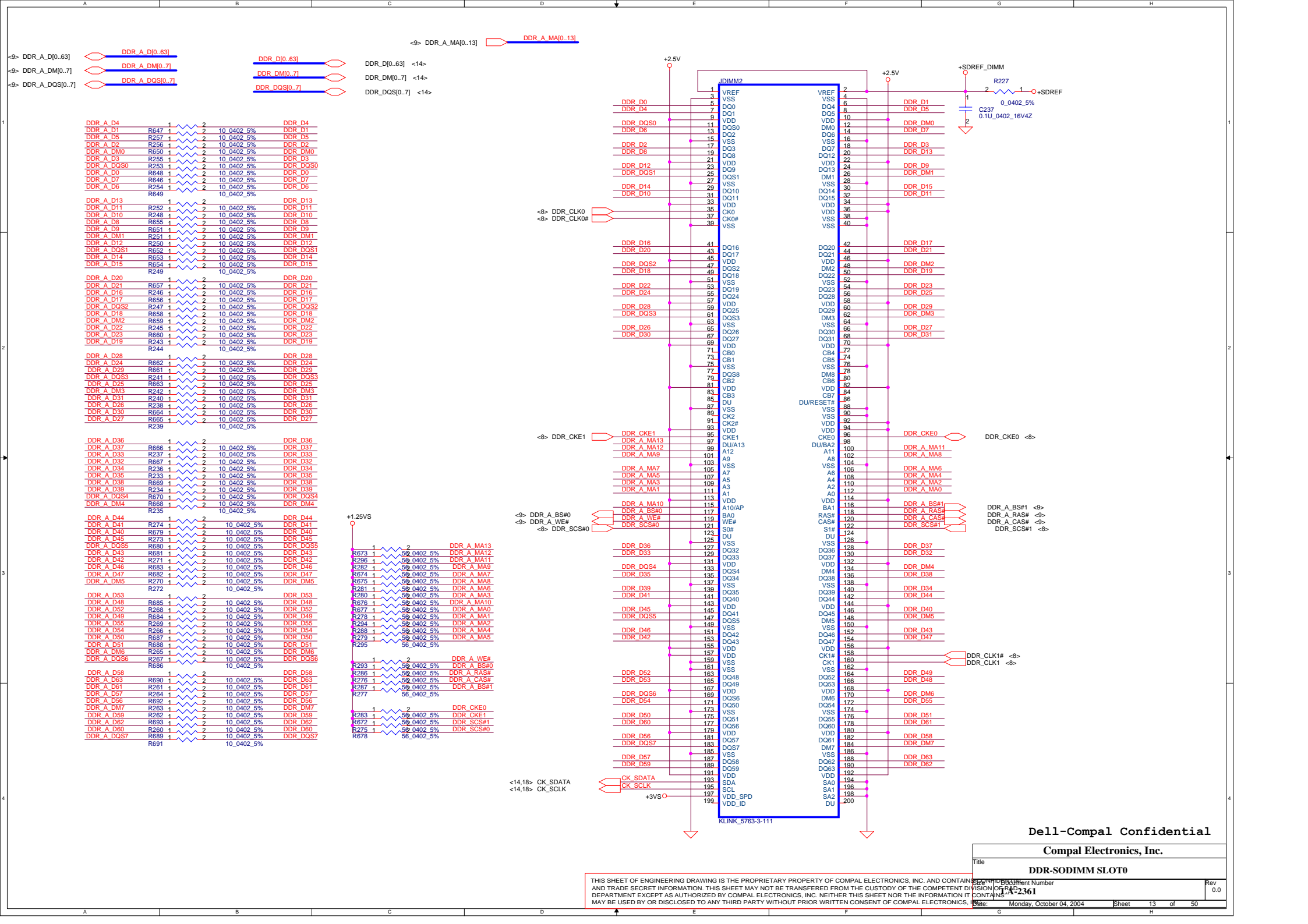
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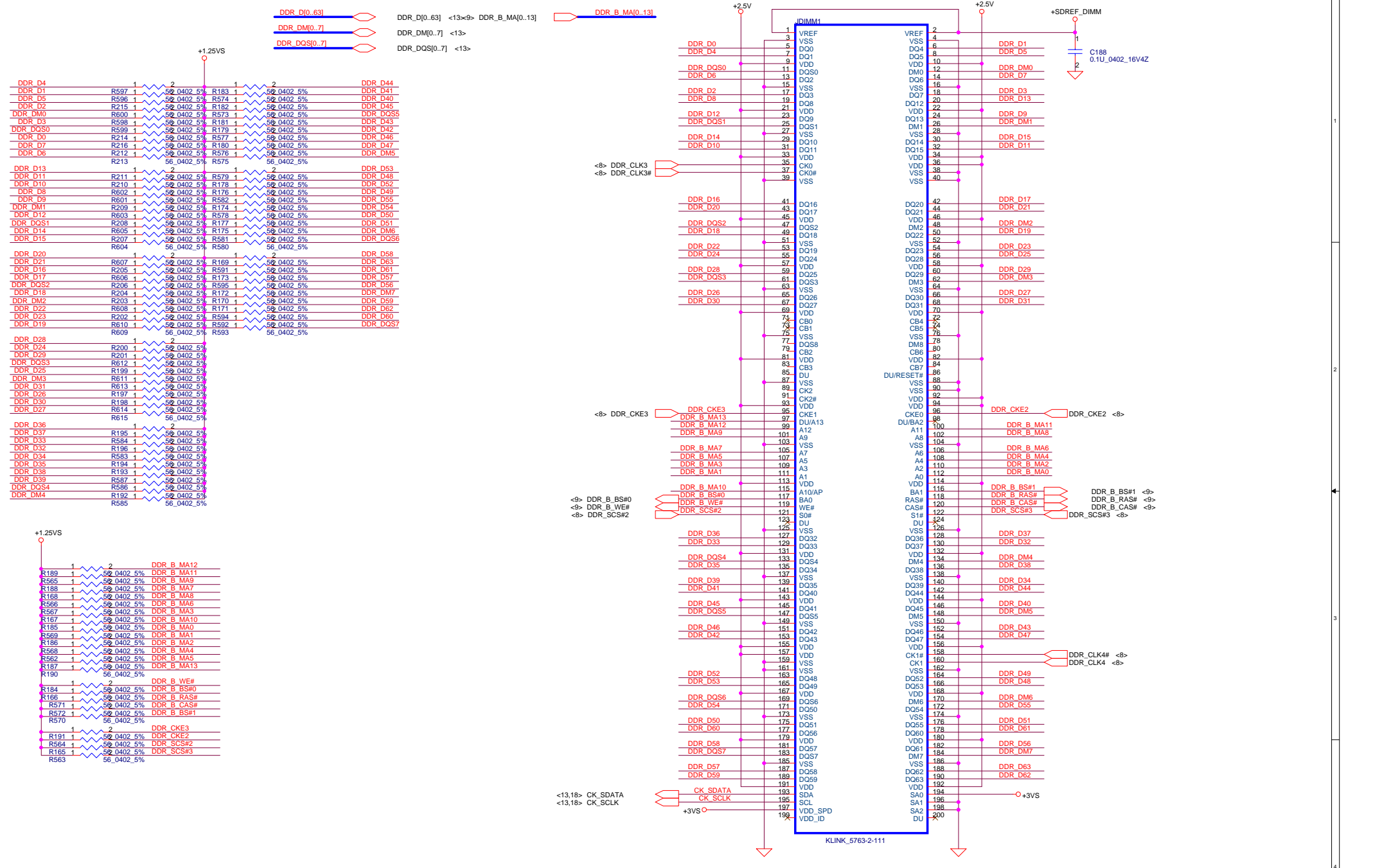
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DDR A D5	R257	1	2	10	0.402	5%	DDR D5
DDR A D2	R256	1	2	10	0.402	5%	DDR D2
DDR A DM0	R650	1	2	10	0.402	5%	DDR DM0
DDR A D3	R255	1	2	10	0.402	5%	DDR D3
DDR A DQ50	R253	1	2	10	0.402	5%	DDR DQ50
DDR A D0	R648	1	2	10	0.402	5%	DDR D0
DDR A D7	R646	1	2	10	0.402	5%	DDR D7
DDR A D6	R254	1	2	10	0.402	5%	DDR D6
DDR A D13	R649	1	2	10	0.402	5%	DDR D13
DDR A D11	R252	1	2	10	0.402	5%	DDR D11
DDR A D10	R248	1	2	10	0.402	5%	DDR D10
DDR A D8	R655	1	2	10	0.402	5%	DDR D8
DDR A D9	R651	1	2	10	0.402	5%	DDR D9
DDR A DM1	R251	1	2	10	0.402	5%	DDR DM1
DDR A D12	R250	1	2	10	0.402	5%	DDR D12
DDR A DQ51	R652	1	2	10	0.402	5%	DDR DQ51
DDR A D14	R653	1	2	10	0.402	5%	DDR D14
DDR A D15	R654	1	2	10	0.402	5%	DDR D15
DDR A D20	R249	1	2	10	0.402	5%	DDR D20
DDR A D21	R657	1	2	10	0.402	5%	DDR D21
DDR A D16	R246	1	2	10	0.402	5%	DDR D16
DDR A D17	R656	1	2	10	0.402	5%	DDR D17
DDR A DQ52	R247	1	2	10	0.402	5%	DDR DQ52
DDR A D18	R658	1	2	10	0.402	5%	DDR D18
DDR A DM2	R659	1	2	10	0.402	5%	DDR DM2
DDR A D22	R245	1	2	10	0.402	5%	DDR D22
DDR A D23	R660	1	2	10	0.402	5%	DDR D23
DDR A D19	R243	1	2	10	0.402	5%	DDR D19
DDR A D24	R244	1	2	10	0.402	5%	DDR D24
DDR A D28	R662	1	2	10	0.402	5%	DDR D28
DDR A D29	R661	1	2	10	0.402	5%	DDR D29
DDR A DQ53	R241	1	2	10	0.402	5%	DDR DQ53
DDR A D25	R663	1	2	10	0.402	5%	DDR D25
DDR A DM3	R242	1	2	10	0.402	5%	DDR DM3
DDR A D31	R240	1	2	10	0.402	5%	DDR D31
DDR A D26	R238	1	2	10	0.402	5%	DDR D26
DDR A D30	R664	1	2	10	0.402	5%	DDR D30
DDR A D27	R665	1	2	10	0.402	5%	DDR D27
DDR A D36	R666	1	2	10	0.402	5%	DDR D36
DDR A D37	R237	1	2	10	0.402	5%	DDR D37
DDR A D32	R667	1	2	10	0.402	5%	DDR D32
DDR A D34	R236	1	2	10	0.402	5%	DDR D34
DDR A D35	R233	1	2	10	0.402	5%	DDR D35
DDR A D38	R669	1	2	10	0.402	5%	DDR D38
DDR A D39	R234	1	2	10	0.402	5%	DDR D39
DDR A DQ54	R670	1	2	10	0.402	5%	DDR DQ54
DDR A DM4	R668	1	2	10	0.402	5%	DDR DM4
DDR A D44	R235	1	2	10	0.402	5%	DDR D44
DDR A D41	R274	1	2	10	0.402	5%	DDR D41
DDR A D40	R679	1	2	10	0.402	5%	DDR D40
DDR A D45	R273	1	2	10	0.402	5%	DDR D45
DDR A DQ55	R680	1	2	10	0.402	5%	DDR DQ55
DDR A D43	R681	1	2	10	0.402	5%	DDR D43
DDR A D42	R271	1	2	10	0.402	5%	DDR D42
DDR A D46	R683	1	2	10	0.402	5%	DDR D46
DDR A D47	R682	1	2	10	0.402	5%	DDR D47
DDR A DM5	R270	1	2	10	0.402	5%	DDR DM5
DDR A D53	R272	1	2	10	0.402	5%	DDR D53
DDR A D48	R685	1	2	10	0.402	5%	DDR D48
DDR A D52	R268	1	2	10	0.402	5%	DDR D52
DDR A D49	R684	1	2	10	0.402	5%	DDR D49
DDR A D55	R269	1	2	10	0.402	5%	DDR D55
DDR A D54	R266	1	2	10	0.402	5%	DDR D54
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DDR A D51	R688	1	2	10	0.402	5%	DDR D51
DDR A DM6	R265	1	2	10	0.402	5%	DDR DM6
DDR A DQ56	R267	1	2	10	0.402	5%	DDR DQ56
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DDR A D63	R690	1	2	10	0.402	5%	DDR D63
DDR A D61	R261	1	2	10	0.402	5%	DDR D61
DDR A D57	R264	1	2	10	0.402	5%	DDR D57
DDR A D56	R692	1	2	10	0.402	5%	DDR D56
DDR A DM7	R263	1	2	10	0.402	5%	DDR DM7
DDR A D59	R262	1	2	10	0.402	5%	DDR D59
DDR A D62	R693	1	2	10	0.402	5%	DDR D62
DDR A D60	R260	1	2	10	0.402	5%	DDR D60
DDR A DQ57	R689	1	2	10	0.402	5%	DDR DQ57
DDR A D67	R691	1	2	10	0.402	5%	DDR D67

R673	1	2	10	0.402	5%	DDR A MA13
R674	1	2	10	0.402	5%	DDR A MA12
R296	1	2	10	0.402	5%	DDR A MA11
R282	1	2	10	0.402	5%	DDR A MA9
R674	1	2	10	0.402	5%	DDR A MA7
R675	1	2	10	0.402	5%	DDR A MA8
R281	1	2	10	0.402	5%	DDR A MA6
R280	1	2	10	0.402	5%	DDR A MA3
R676	1	2	10	0.402	5%	DDR A MA10
R677	1	2	10	0.402	5%	DDR A MA0
R278	1	2	10	0.402	5%	DDR A MA1
R294	1	2	10	0.402	5%	DDR A MA2
R288	1	2	10	0.402	5%	DDR A MA4
R279	1	2	10	0.402	5%	DDR A MA5
R295	1	2	10	0.402	5%	DDR A MA5
R293	1	2	10	0.402	5%	DDR A WE#
R286	1	2	10	0.402	5%	DDR A RAS#
R276	1	2	10	0.402	5%	DDR A CAS#
R287	1	2	10	0.402	5%	DDR A BS#1
R277	1	2	10	0.402	5%	DDR A BS#1
R283	1	2	10	0.402	5%	DDR A WE#
R672	1	2	10	0.402	5%	DDR A S#0
R275	1	2	10	0.402	5%	DDR A S#0
R678	1	2	10	0.402	5%	DDR A S#0



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 DDR-SODIMM SLOT0



Dell-Compal Confidential

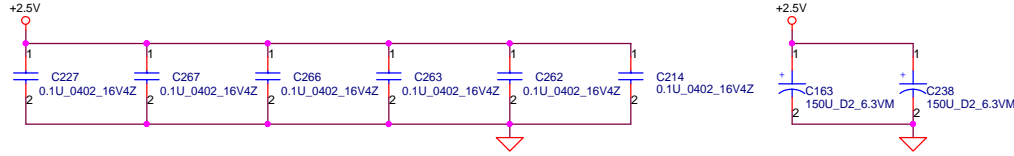
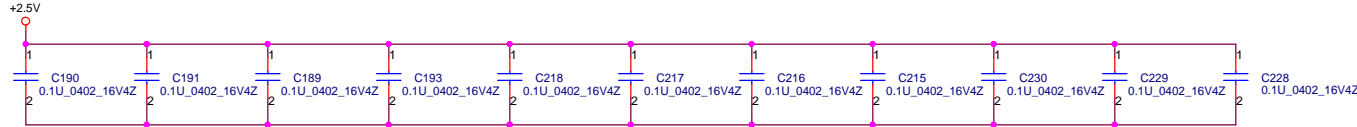
Compal Electronics, Inc.

Title: **DDR-SODIMM SLOT1**

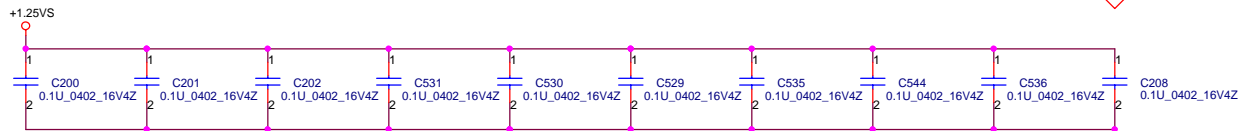
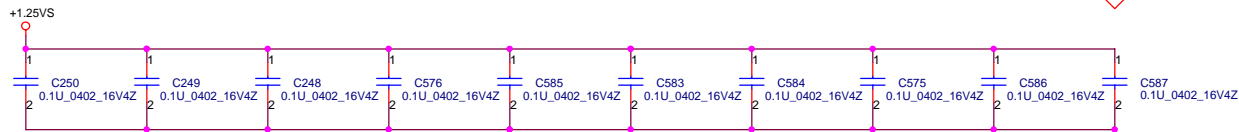
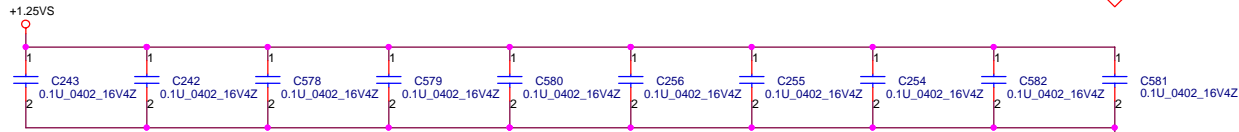
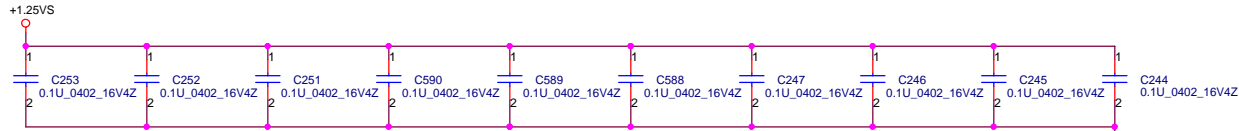
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Document Number: **2361**  
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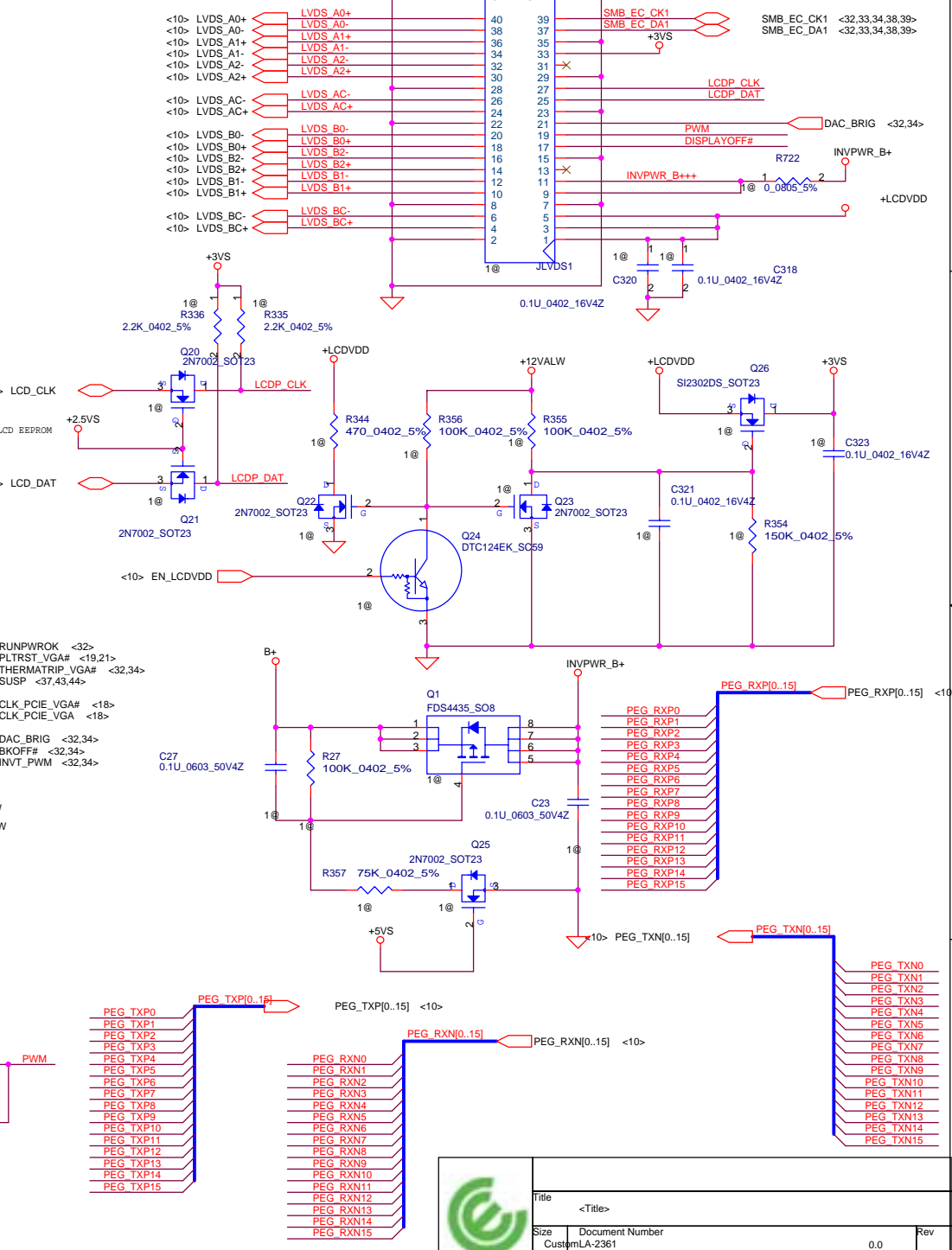
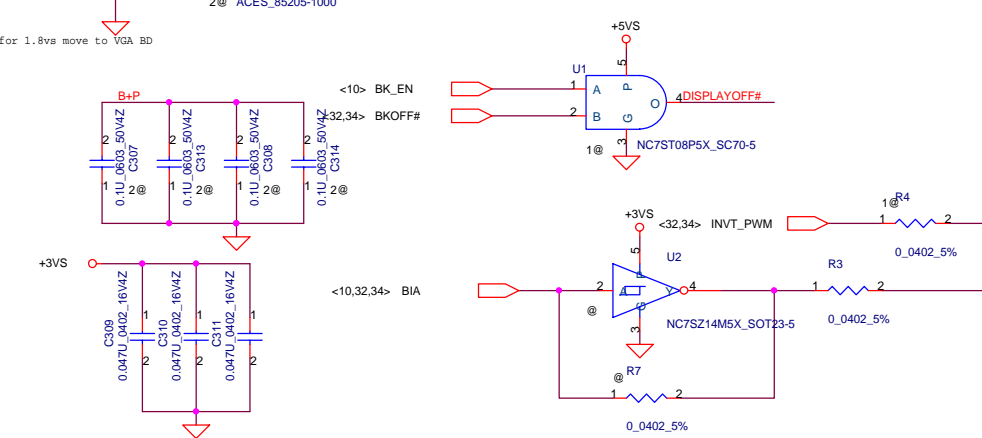
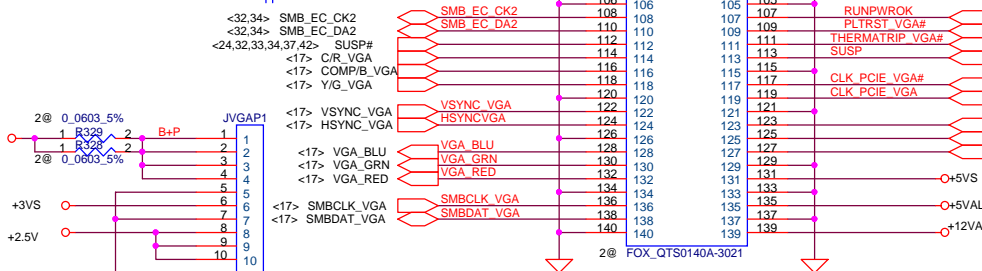
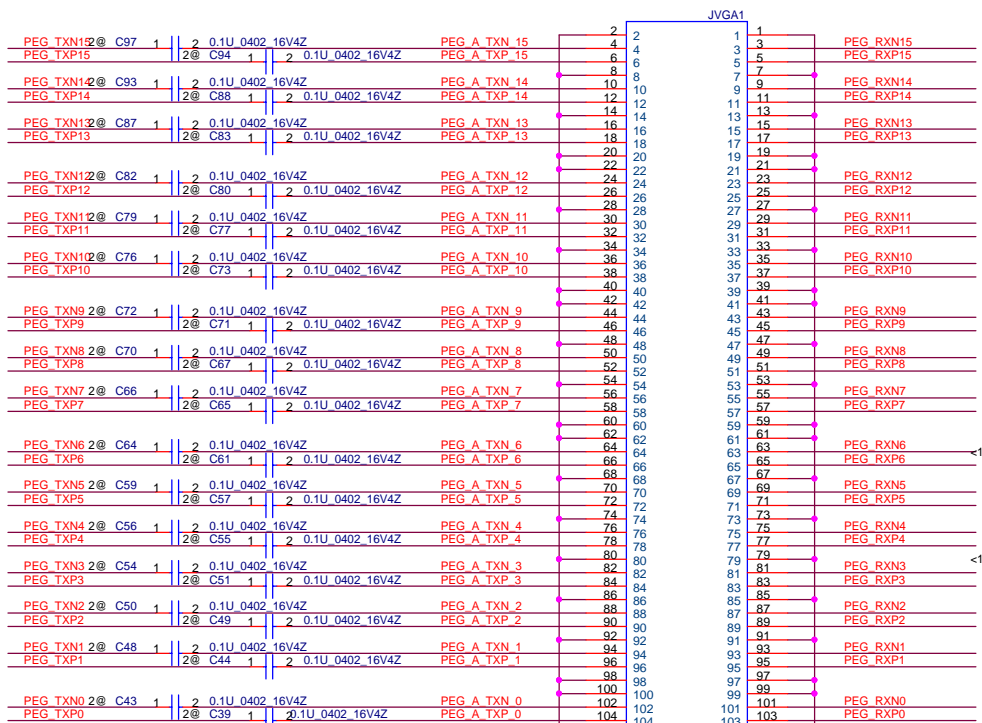
**Layout note :**  
Distribute as close as possible to DDR-SODIMM.



**Layout note :**  
Place one cap close to every 2 pull up resistors termination to +1.25V

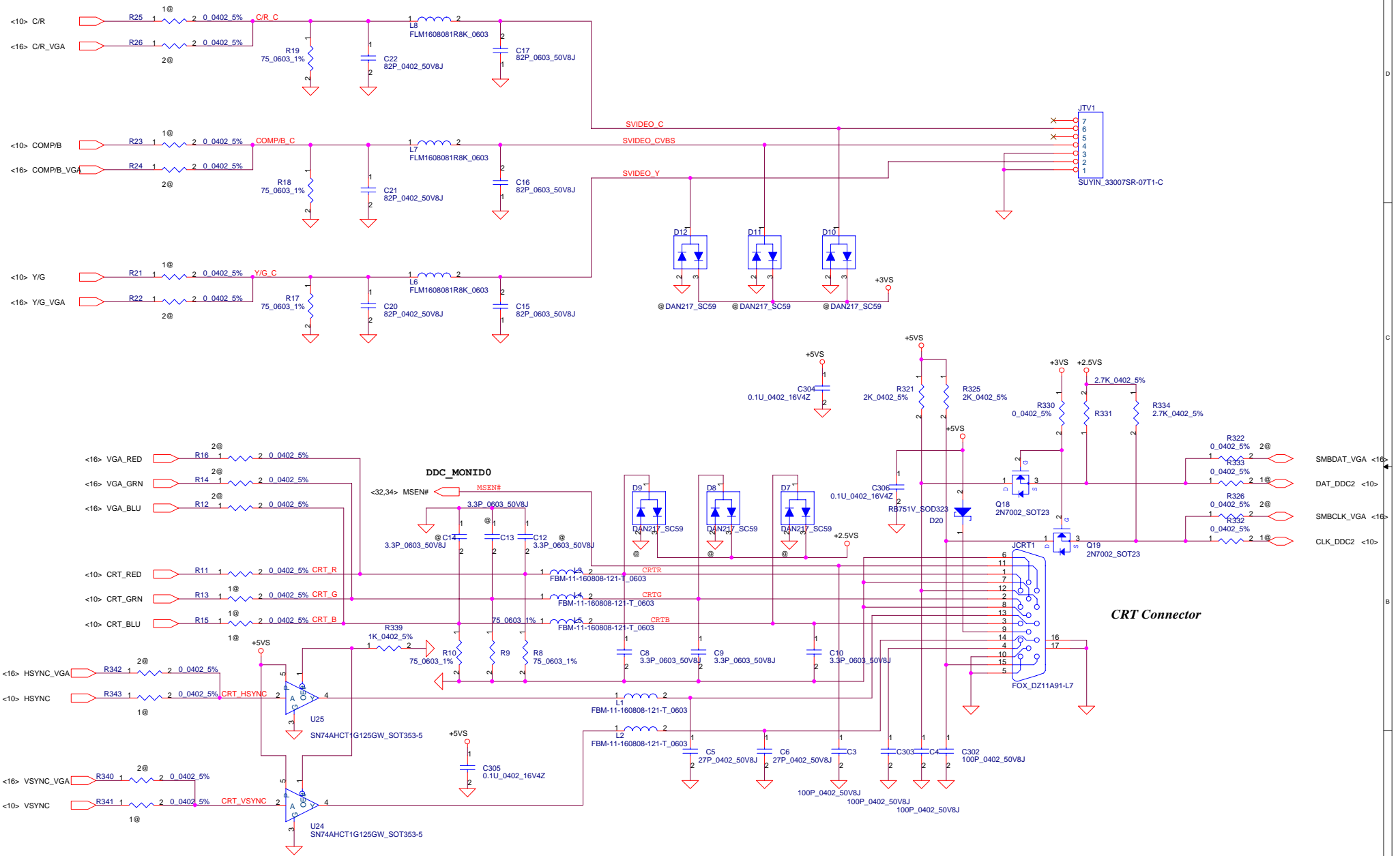


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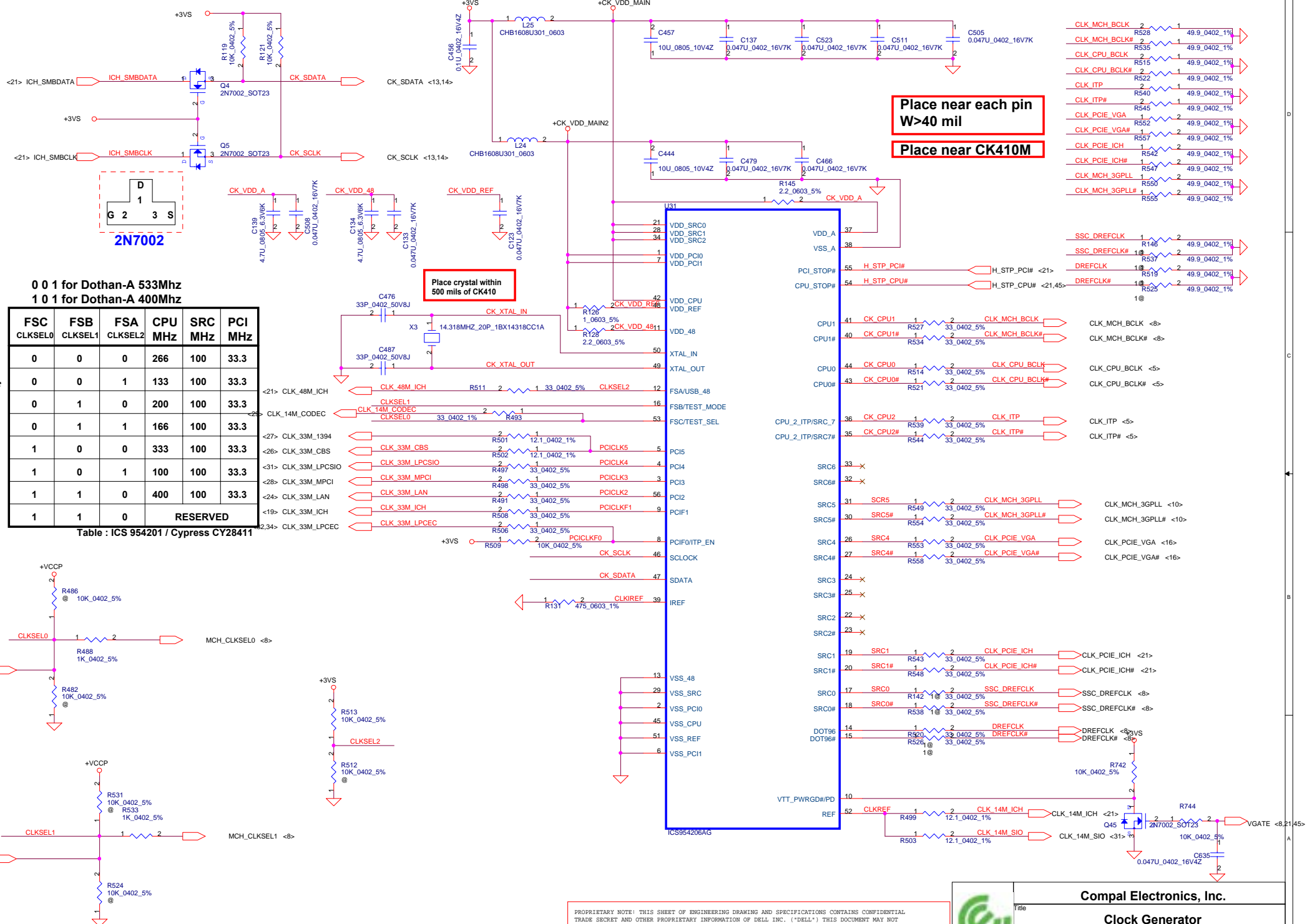
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		<b>TV_OUT and CRT connector</b> <b>LA-2361</b>	
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0 0 1 for Dothan-A 533Mhz  
1 0 1 for Dothan-A 400Mhz

FSC	FSB	FSA	CPU	SRC	PCI
CLKSEL0	CLKSEL1	CLKSEL2	MHZ	MHZ	MHZ
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	0	<b>RESERVED</b>		

Table : ICS 954201 / Cypress CY28411



Place near each pin  
W>40 mil

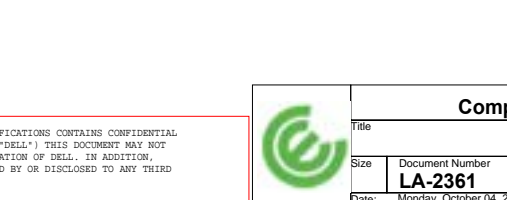
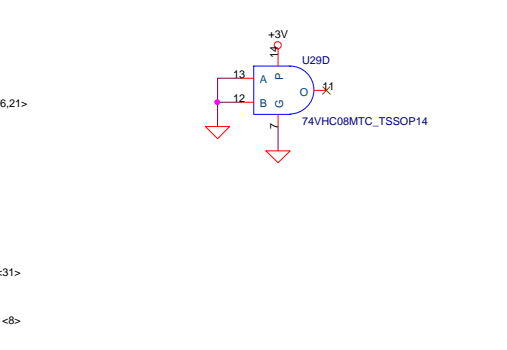
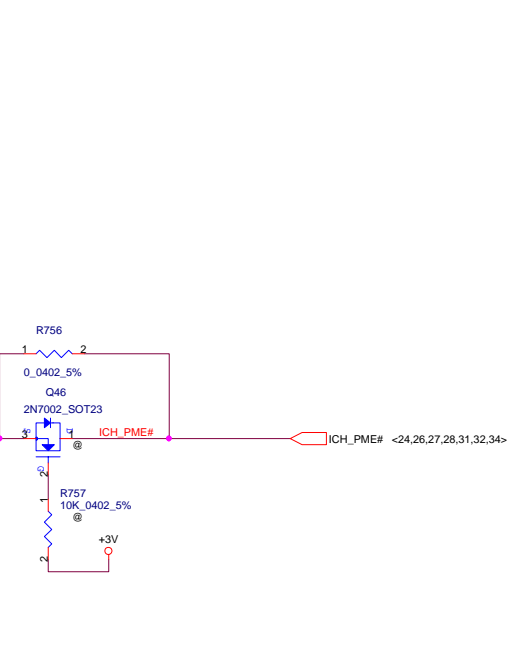
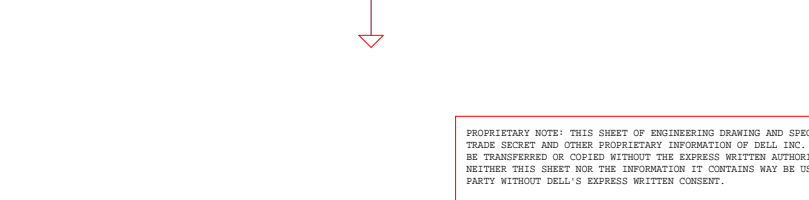
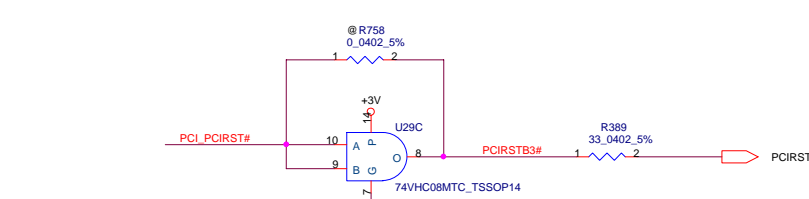
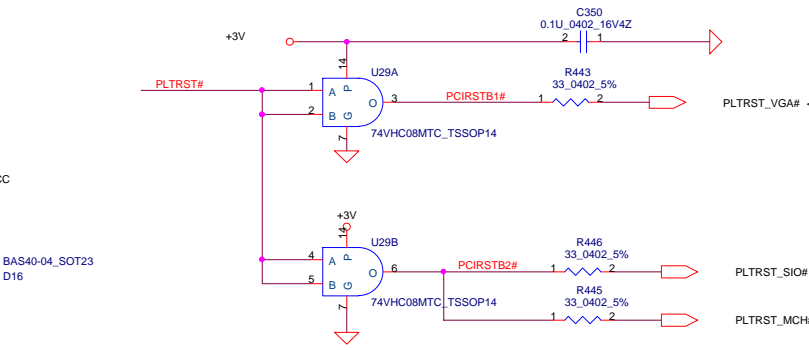
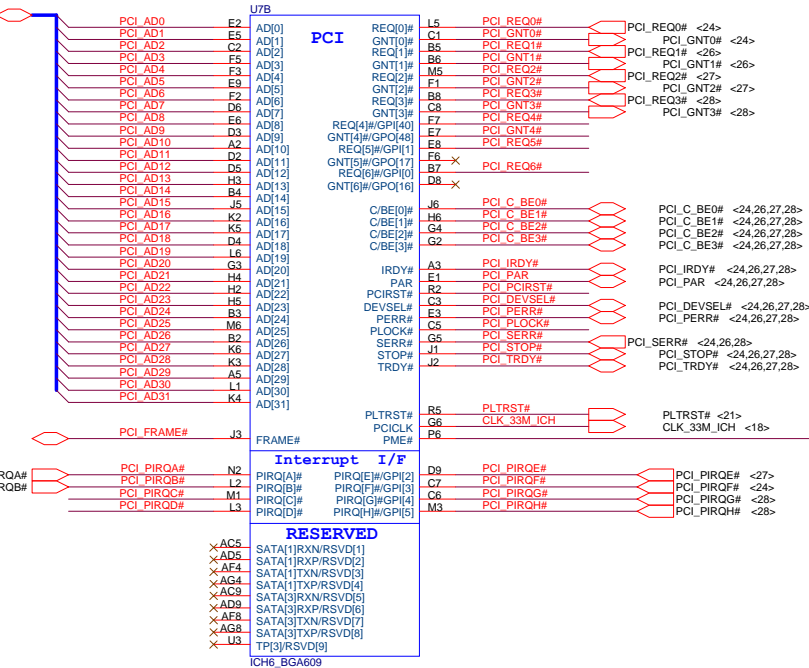
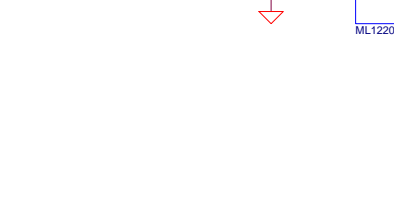
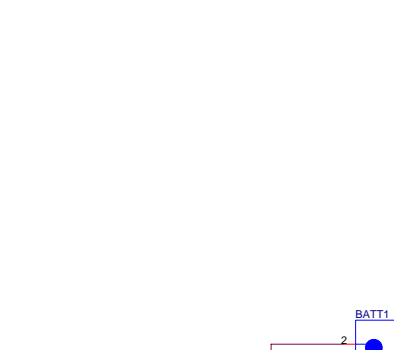
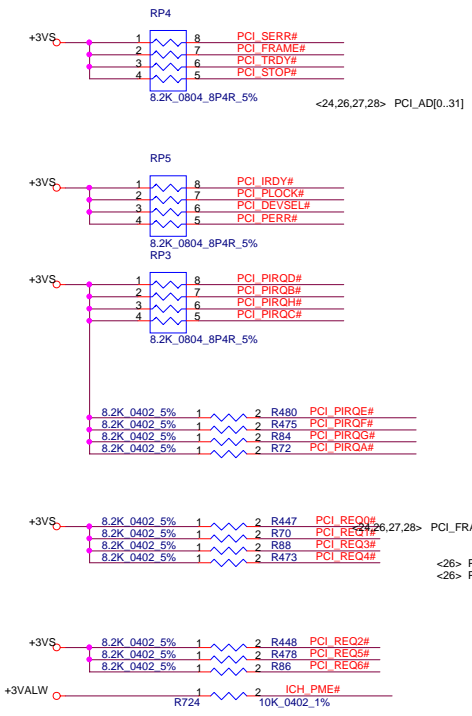
Place near CK410M

Place crystal within  
500 mils of CK410

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<b>Clock Generator</b>		
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COMPAL ELECTRONICS, INC.

Title: ICH6(1/4)

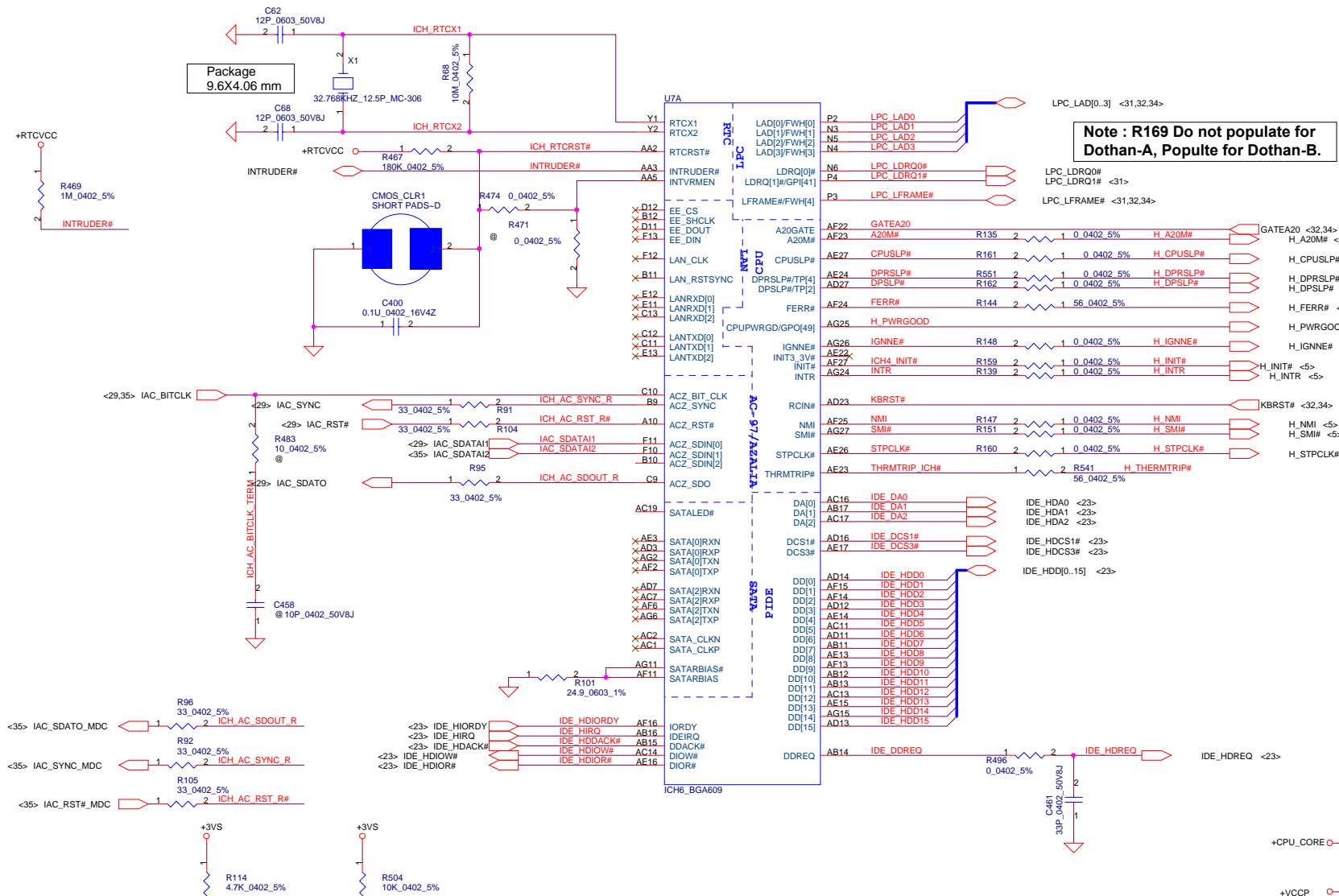
Size: Document Number LA-2361

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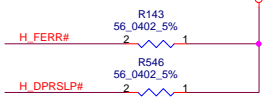
Rev: 0.0

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Package  
9.6X4.06 mm

**Note : R169 Do not populate for Dothan-A, Populte for Dothan-B.**



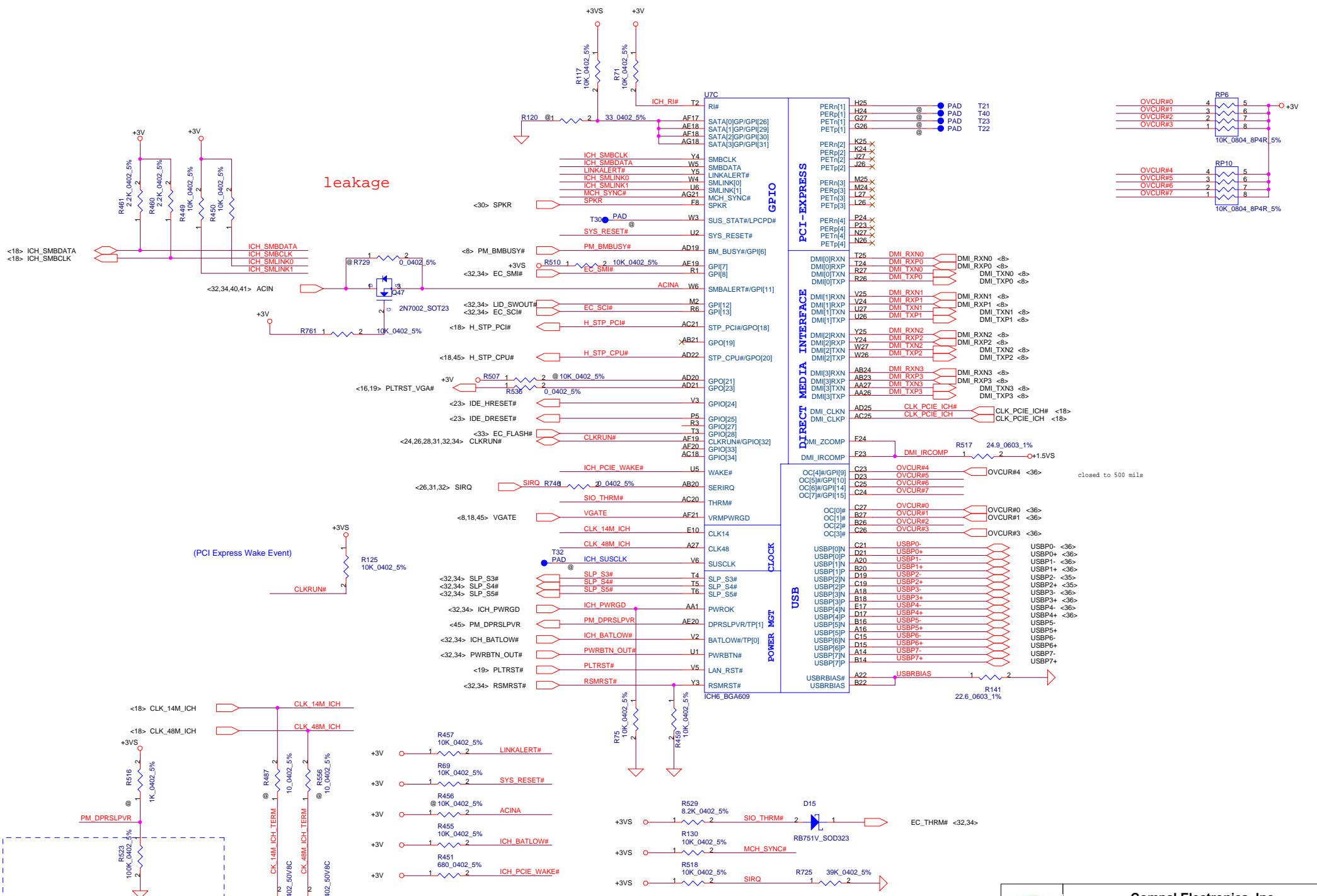
**Note : R423 must be stuff for Dothan-A, no-stuff for Dothan-B.**

**Note : R168 populate 56 ohm for Dothan-A, Populte zero ohm for Dothan-B.**

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<b>Compal Electronics, Inc.</b>			
Title	<b>ICH6(2/4)</b>		
Size	Document Number	Rev	
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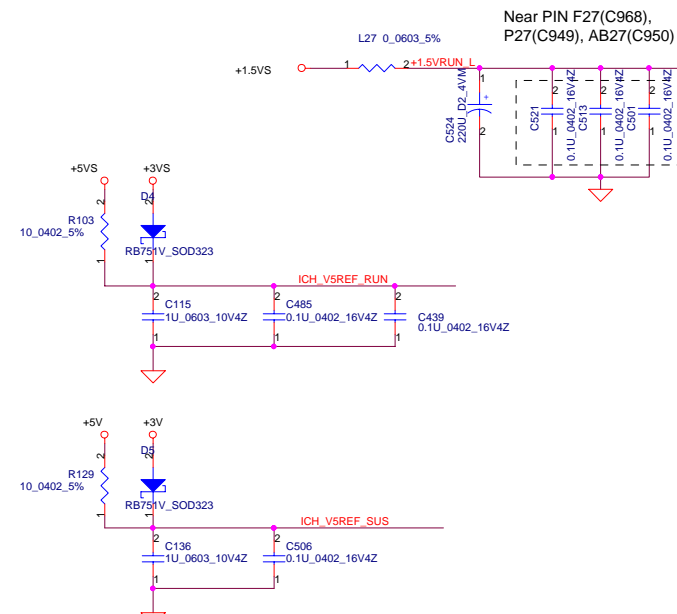
leakage

(PCI Express Wake Event)

May need pulldown for DPRSLPVR in case the ICH6m does not set this value in time for boot.

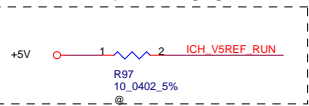
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Title		<b>ICH6(3/4)</b>
Size	Document Number	Rev
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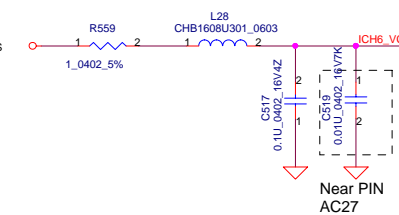
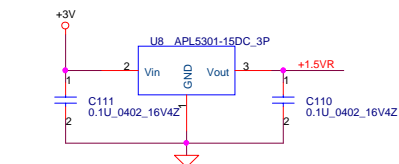


Replacing by this circuit?

Note: Intel will update design guide.



+5VALW @



Near PIN F27(C968), P27(C949), AB27(C950)

Near PIN AG5

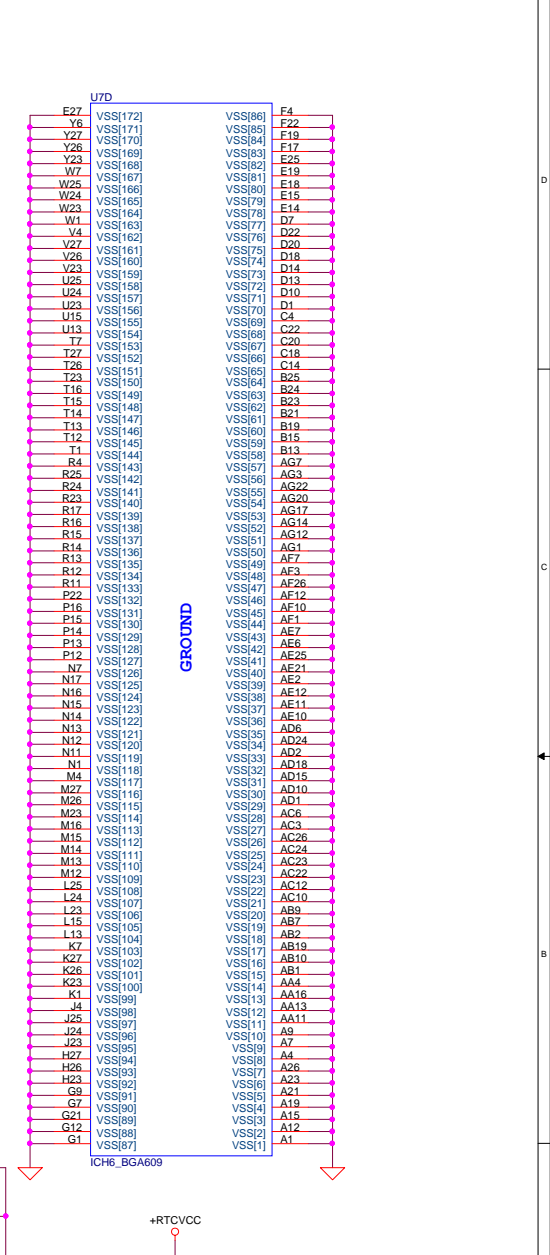
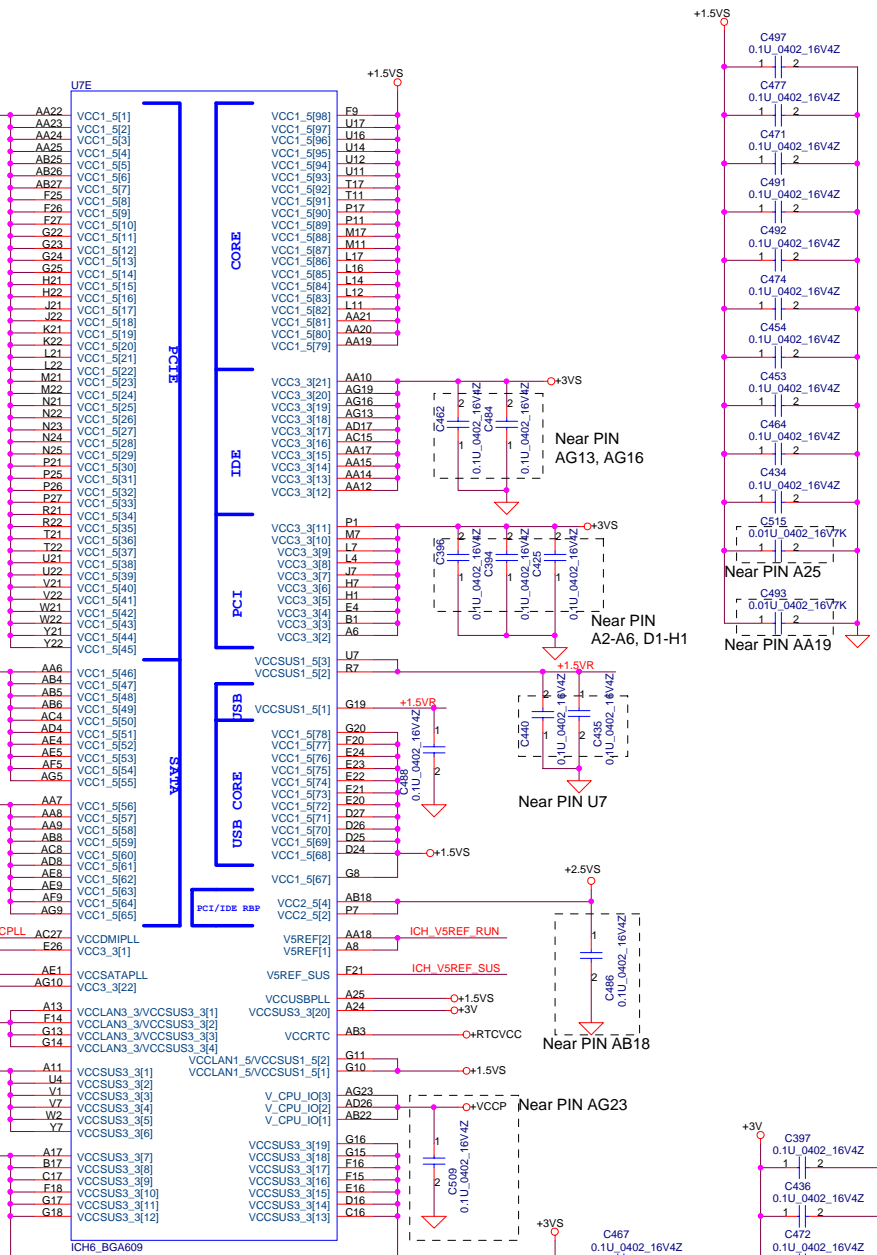
Near PIN AG9

Near PIN E26, E27

Near PIN AE1

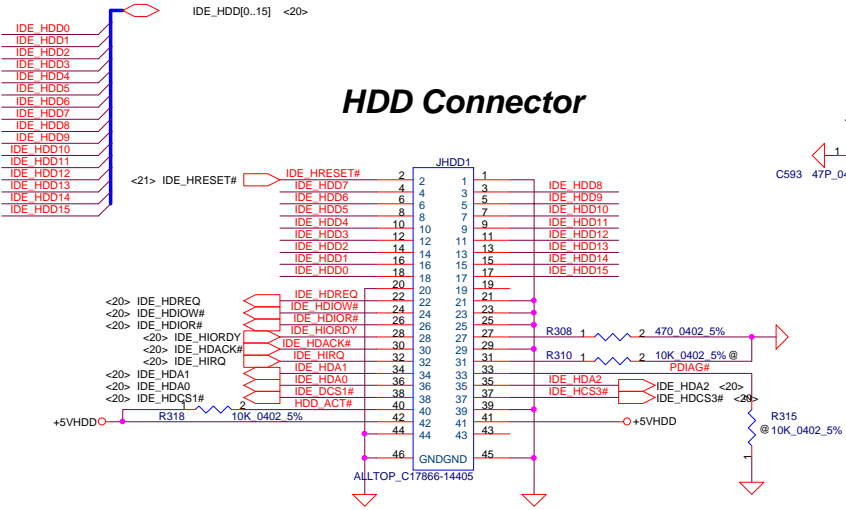
Near PIN A17

Near PIN AC27



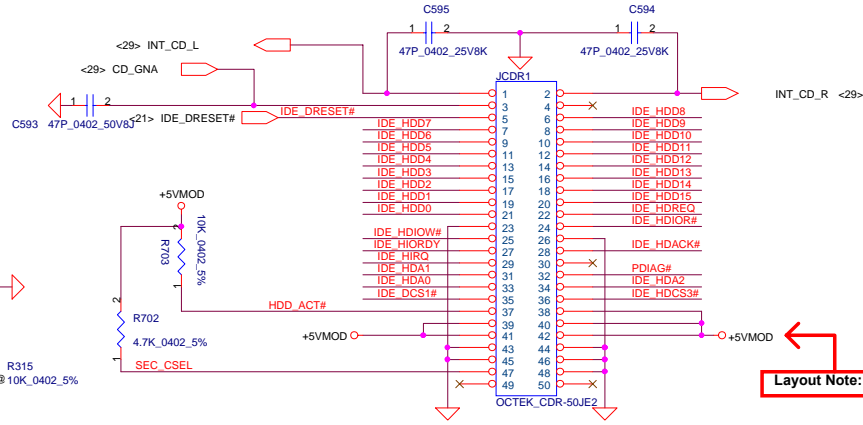
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		<b>ICH6(4/4)</b>	
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### HDD Connector

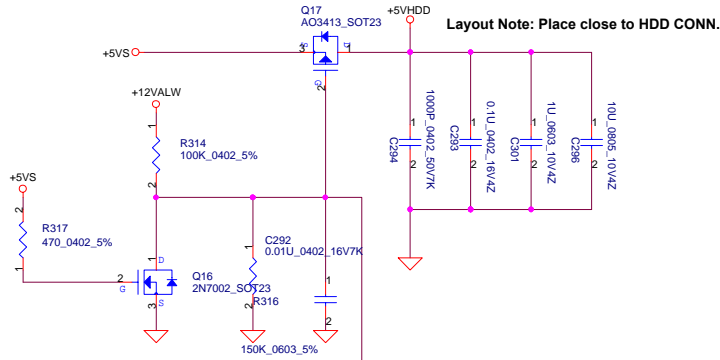
### CD-ROM Connector



Layout Note: W=80 mils

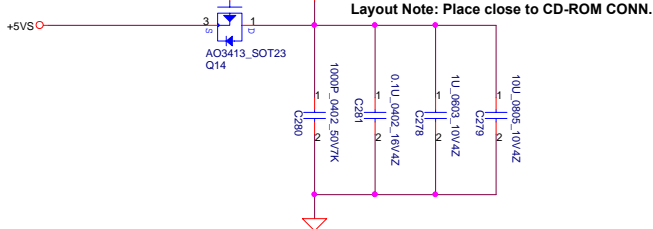
IRQ how to assign

#### +5VHDD Source



Layout Note: Place close to HDD CONN.

#### +5VMOD Source



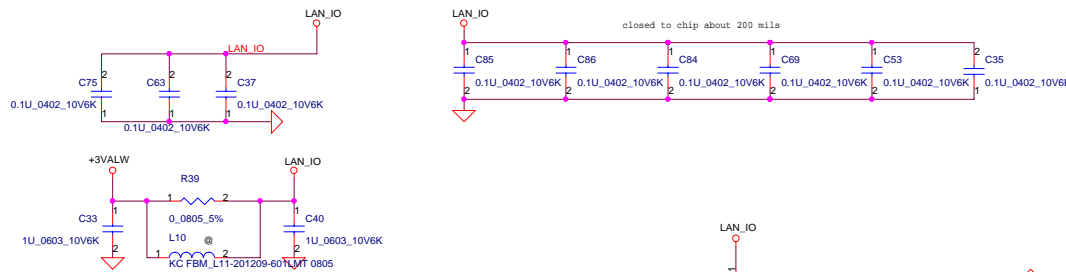
Layout Note: Place close to CD-ROM CONN.



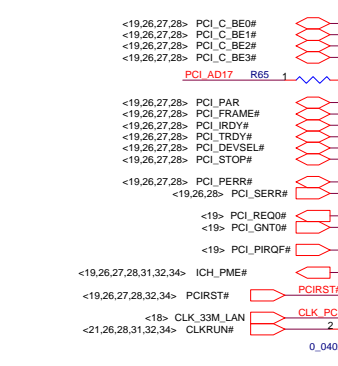
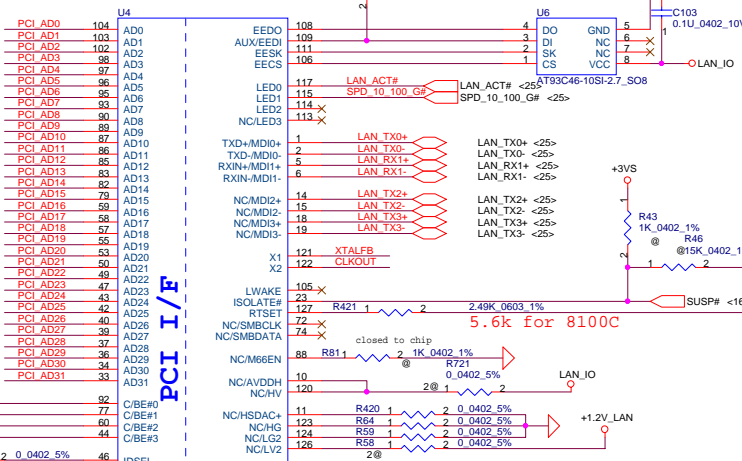
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Title <b>SATA to PATA BRIDGE &amp; CD-ROM CONN.</b>			
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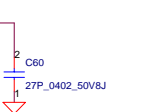
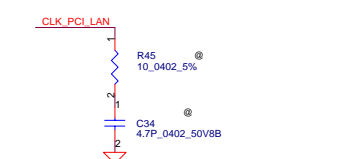
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PCI I/F

LAN I/F

Power

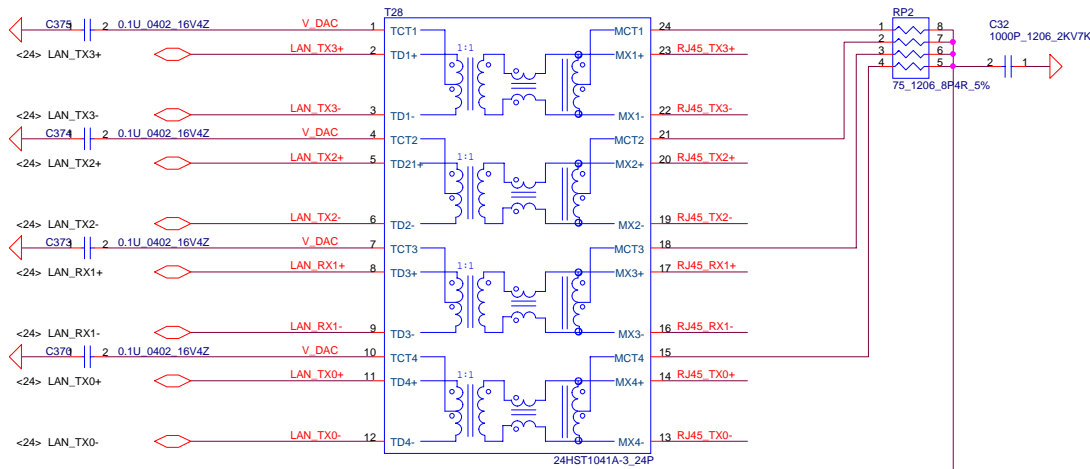


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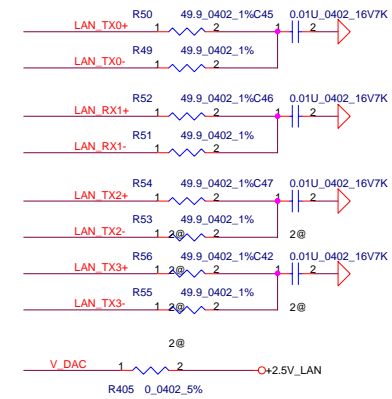
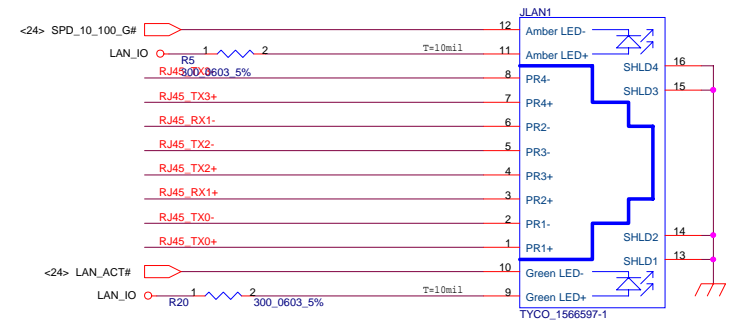
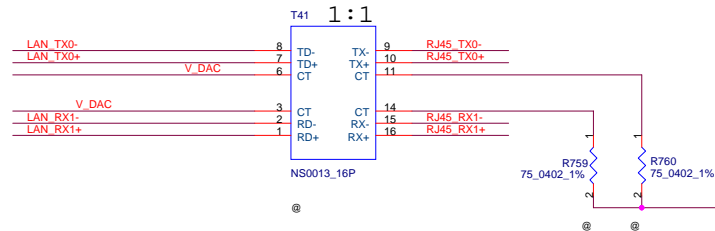




RTL8110SBL used the 24HST1041A-3\_24P  
 RTL8100CL used the 24ST0023-3\_24P

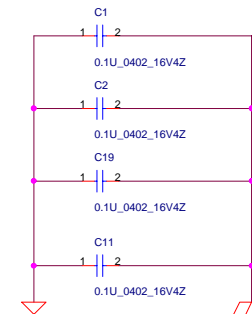
Layout Note  
 24HST1041A-3 pls close to conn.

Termination plane should be copied to chassis ground  
 and also depends on safety concern



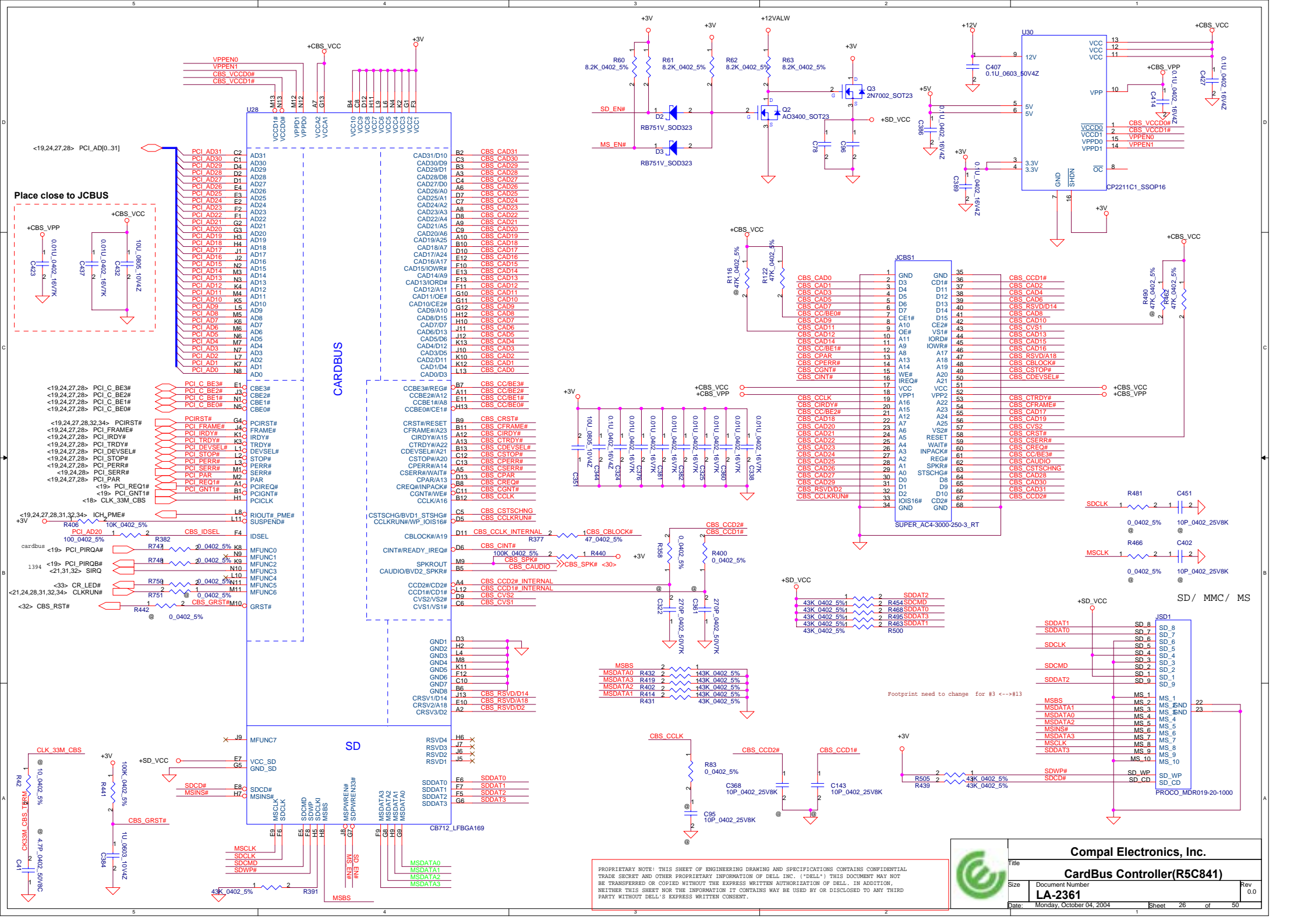
Termination plane should be copied to chassis ground  
 and also depends on safety concern

Please close to LAN IC



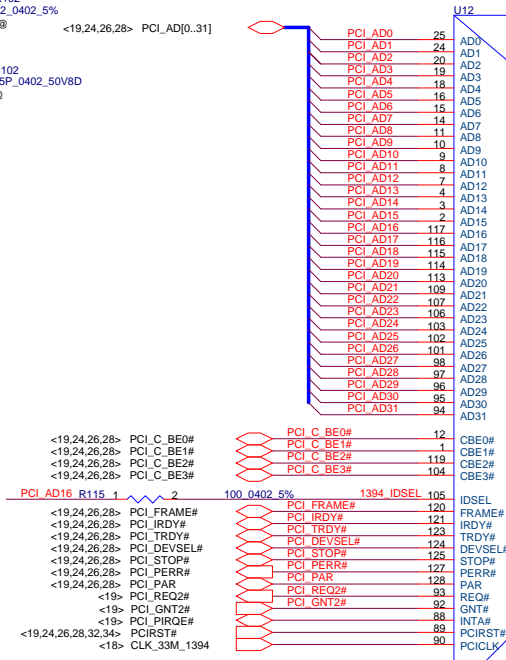
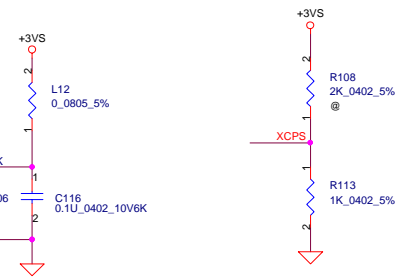
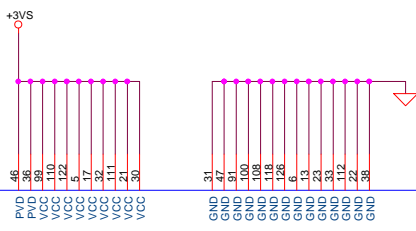
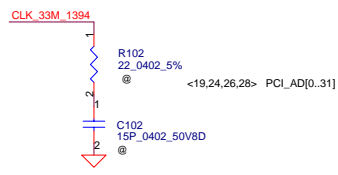
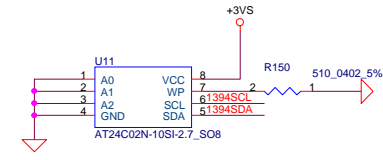
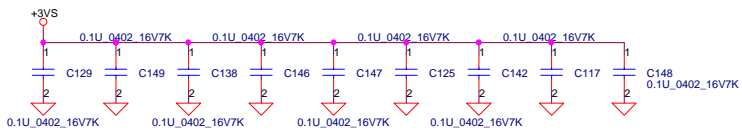
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		<b>LAN CONTROLLER</b>	
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		<b>Compal Electronics, Inc.</b>	
		<b>CardBus Controller(R5C841)</b>	
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# Power

# IEEE 1394

# VT6301S

# PCI Bus

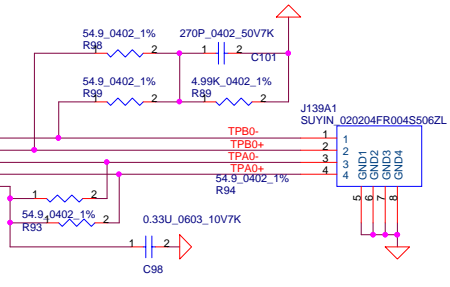
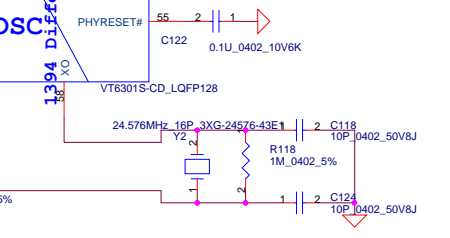
## EEPROM I/F

## PM & Test


## 1394 Differential Pairs

## NC

## OSC



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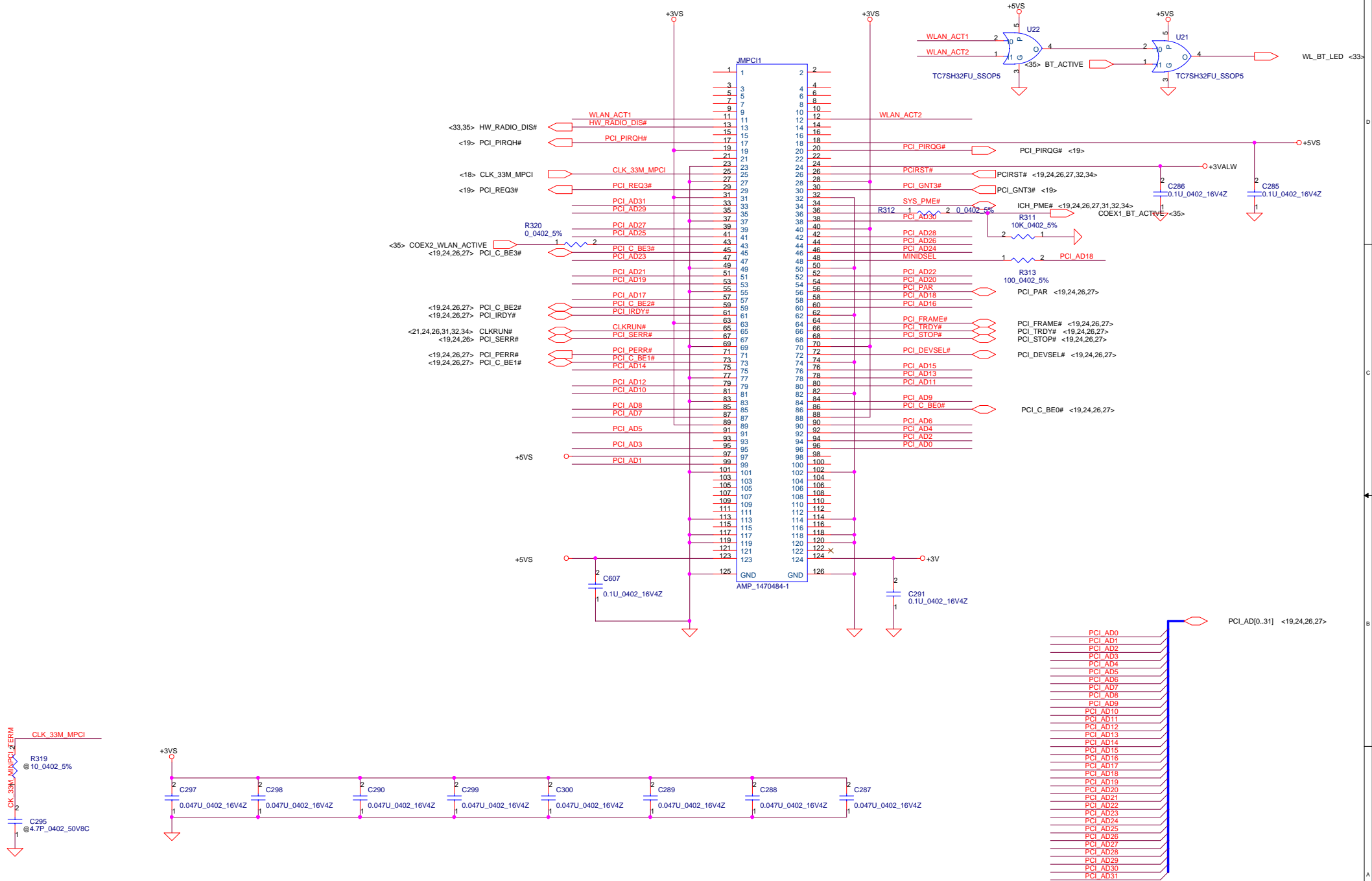


**Compal Electronics, Inc.**


**VIA 6301S 1394 chip**

LA-2361

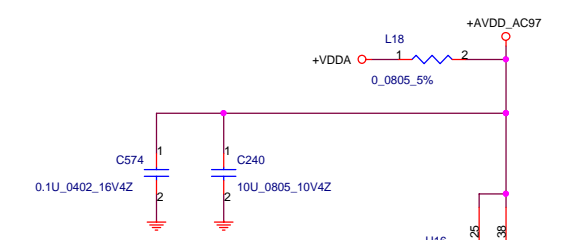
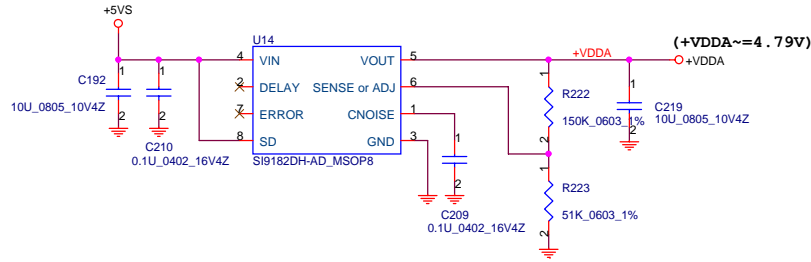
Title		Rev 0.0	
Size	Document Number	Date: Monday, October 04, 2004	
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		<b>Compal Electronics, Inc.</b>	
		<b>MINIPCI</b>	
Title Size Date:	Document Number <b>LA-2361</b> Monday, October 04, 2004	Rev 0.0	Sheet 28 of 50

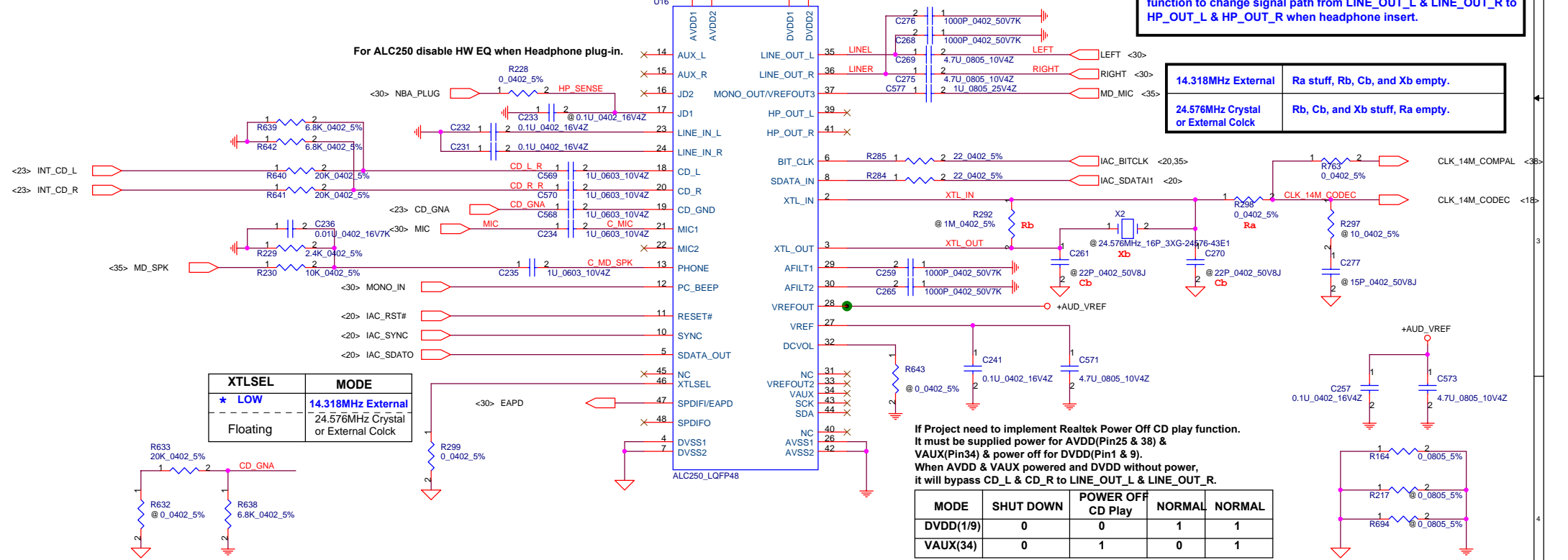
# AC97 Codec



When Project need implement Headphone channel output from Audio Codec pin 39 & 41, it must have another driver to support JD function to change signal path from LINE\_OUT\_L & LINE\_OUT\_R to HP\_OUT\_L & HP\_OUT\_R when headphone insert.

For ALC250 disable HW EQ when Headphone plug-in.

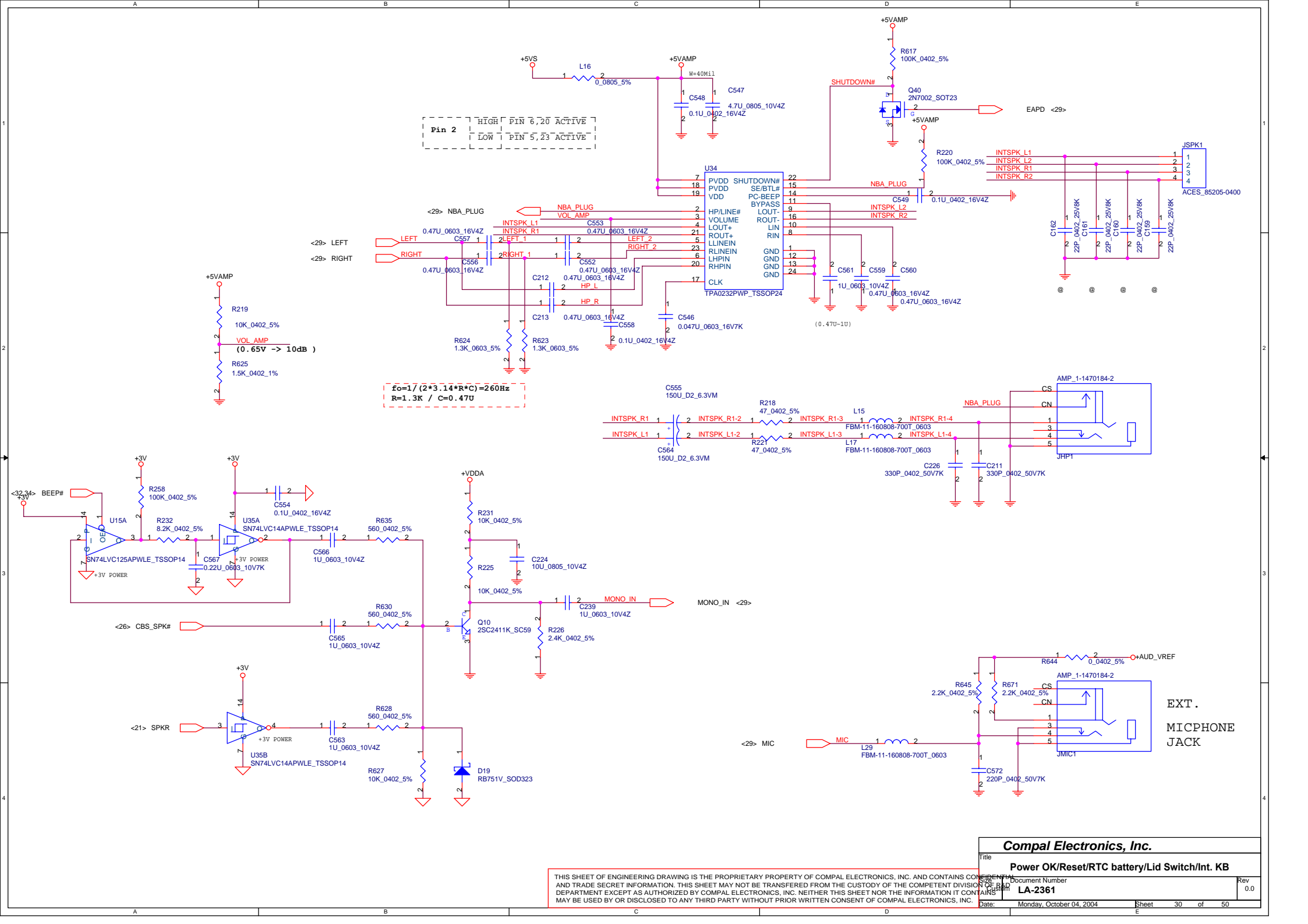
14.318MHz External or External Colck	Ra stuff, Rb, Cb, and Xb empty.
24.576MHz Crystal or External Colck	Rb, Cb, and Xb stuff, Ra empty.



XTLSEL	MODE
* LOW	14.318MHz External
Floating	24.576MHz Crystal or External Colck

If Project need to implement Realtek Power Off CD play function. It must be supplied power for AVDD(Pin25 & 38) & VAUX(Pin34) & power off for DVDD(Pin1 & 9). When AVDD & VAUX powered and DVDD without power, it will bypass CD\_L & CD\_R to LINE\_OUT\_L & LINE\_OUT\_R.

MODE	SHUT DOWN	POWER OFF CD Play	NORMAL	NORMAL
DVDD(1/9)	0	0	1	1
VAUX(34)	0	1	0	1



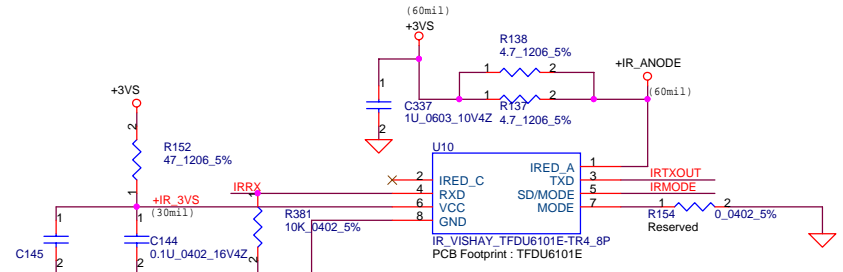
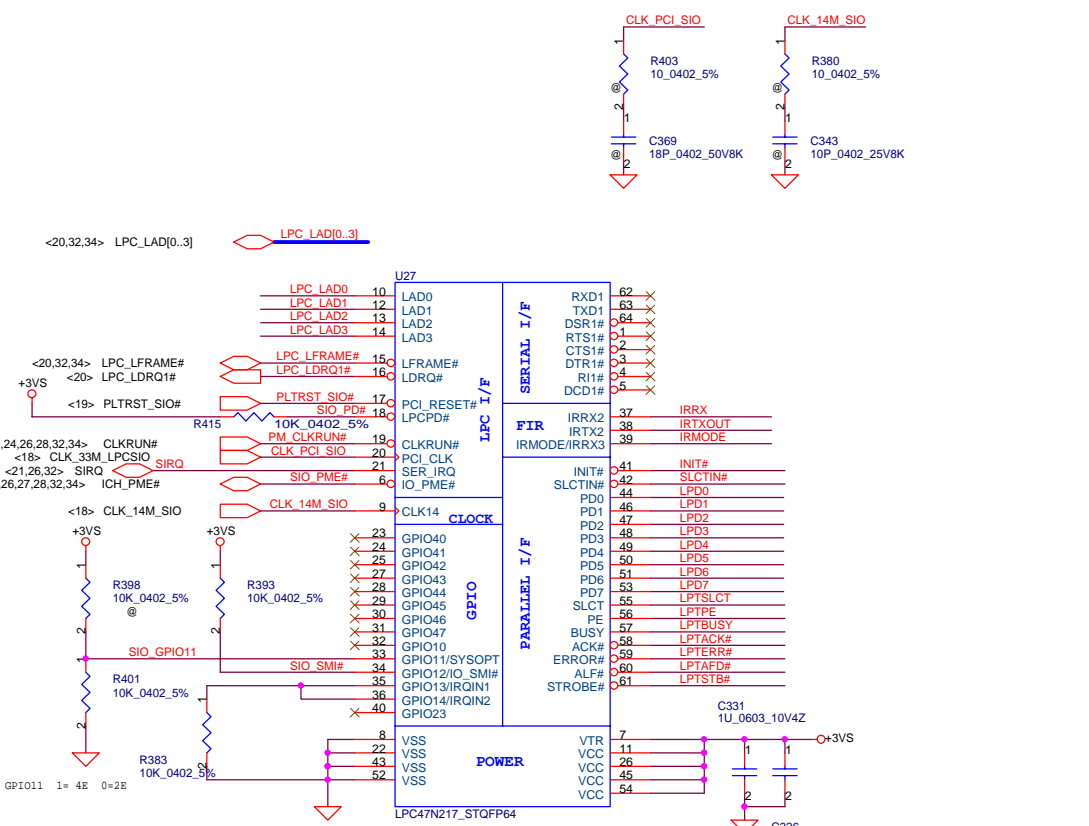
Pin 2 HIGH PIN 6, 20 ACTIVE  
LOW PIN 5, 23 ACTIVE

$$f_0 = 1 / (2 * 3.14 * R * C) = 260 \text{ Hz}$$

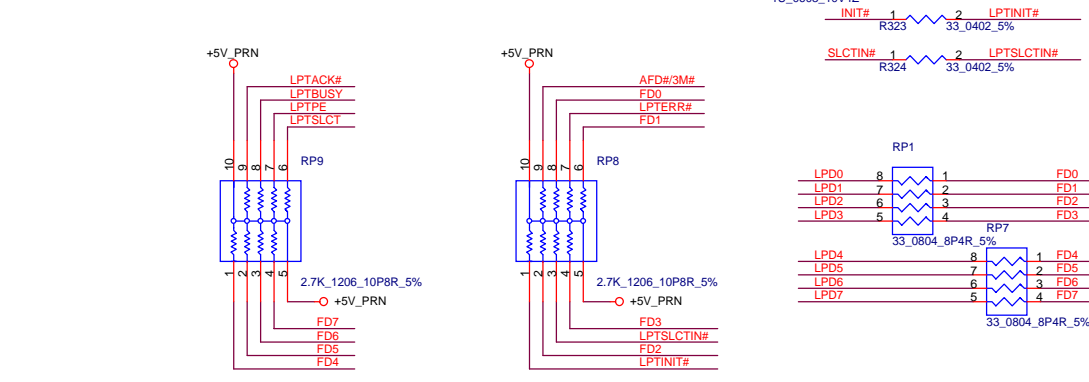
$$R = 1.3 \text{ K} / C = 0.47 \text{ U}$$

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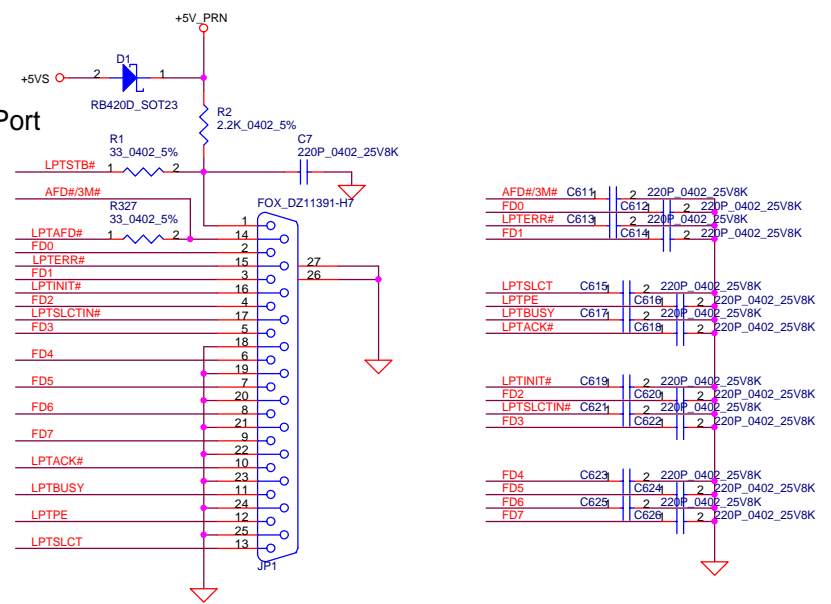
# FIR Module



SD/MODE: SHUTDOWN MODE, HIGH ACTIVE  
MODE: HIGH/LOW SPEED SELECT

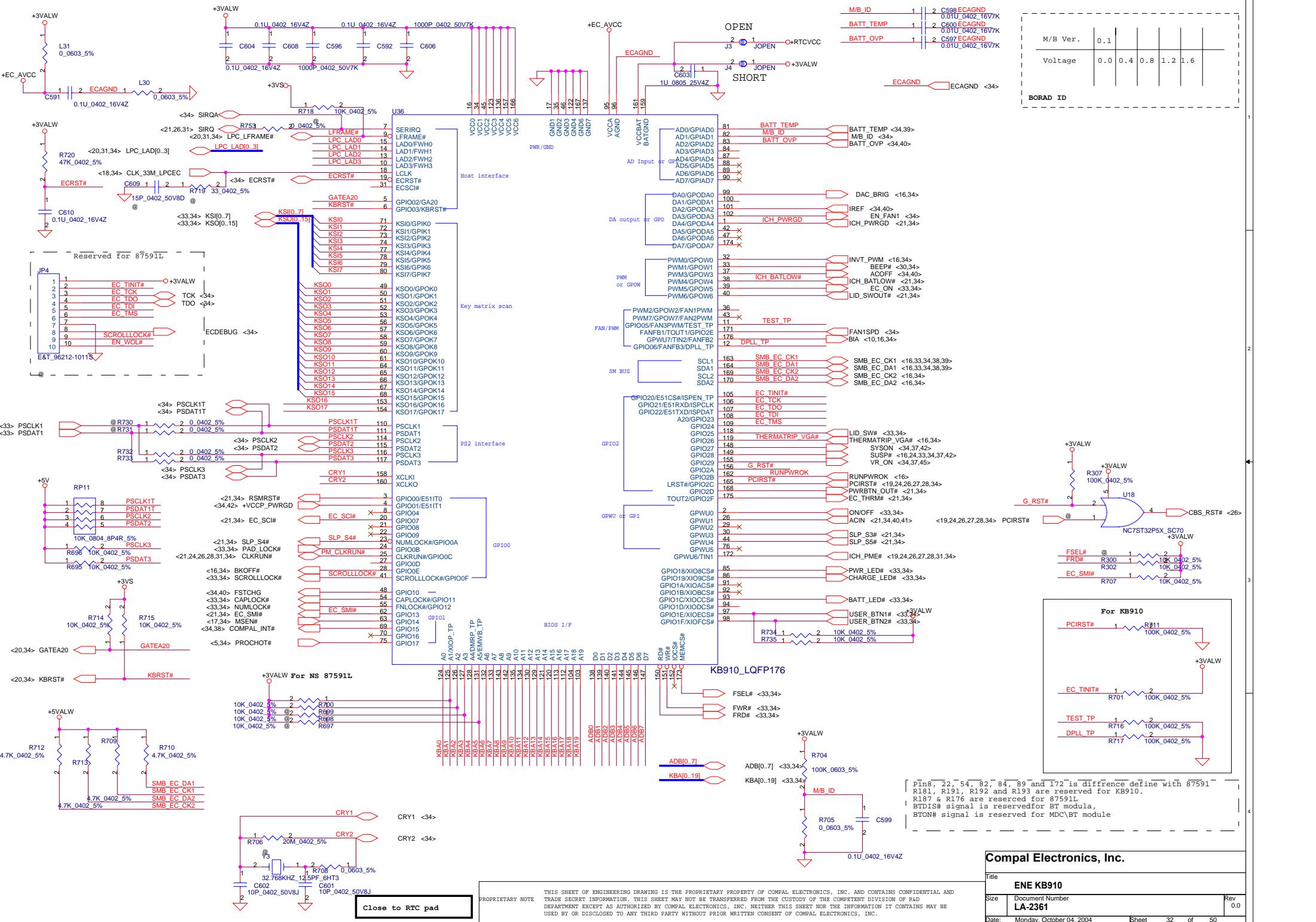


## Parallel Port



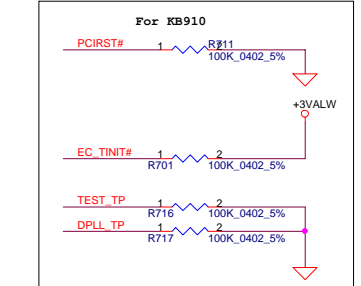
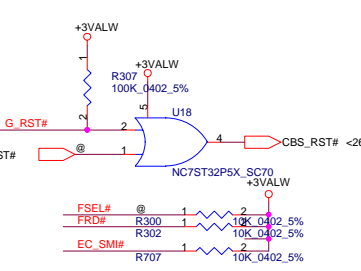
<b>Compal Electronics, Inc.</b>	
Title	<b>SUPER I/O LPC47N217</b>
Document Number	<b>LA-2361</b>
Date: Monday, October 04, 2004	Sheet 31 of 50

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M/B Ver.	0.1				
Voltage	0.0	0.4	0.8	1.2	1.6

BORAD ID



Pin8, 22, 54, 82, 84, 89 and I72 is difference define with 87591  
 R181, R191, R192 and R193 are reserved for KB910.  
 R187 & R176 are reserved for 87591L.  
 BTDISH signal is reserved for BT module.  
 BTON# signal is reserved for MDC/BT module

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Title	ENE KB910		
Size	Document Number	LA-2361	Rev 0.0
Date:	Monday, October 04, 2004	Sheet	32 of 50

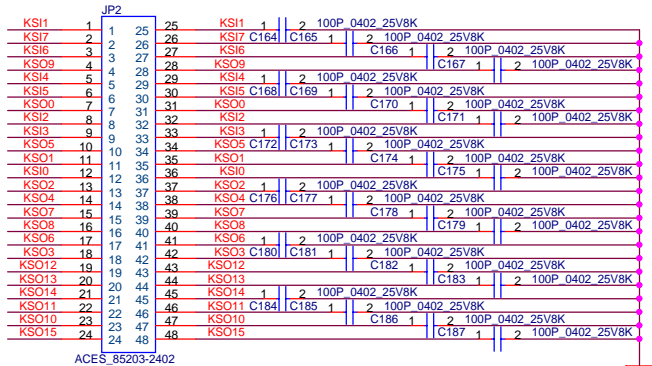
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Close to RTC pad

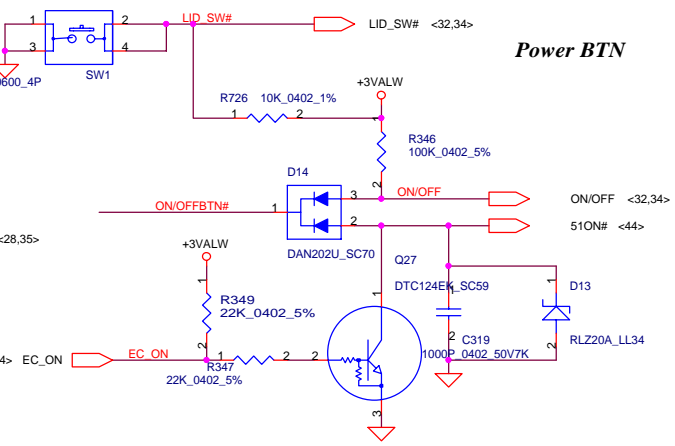
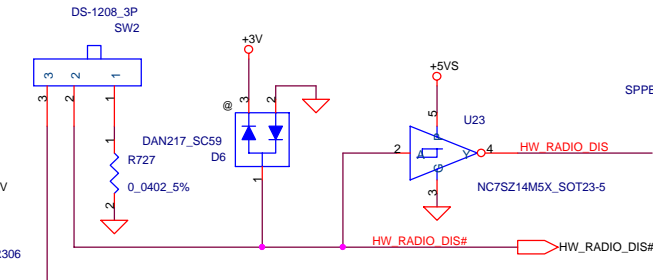


<32,34> KSI[0..7]  
<32,34> KSO[0..15]

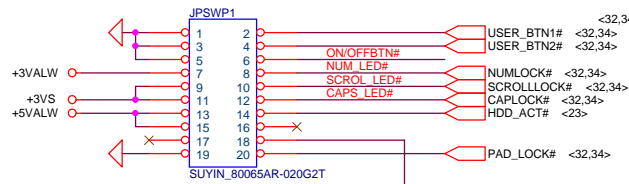
# KeyBoard



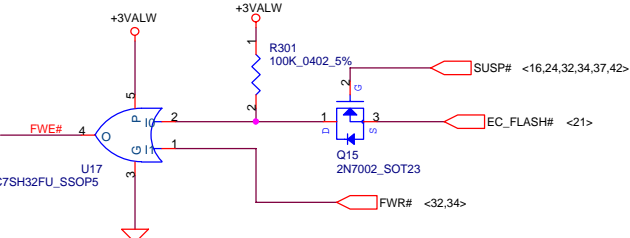
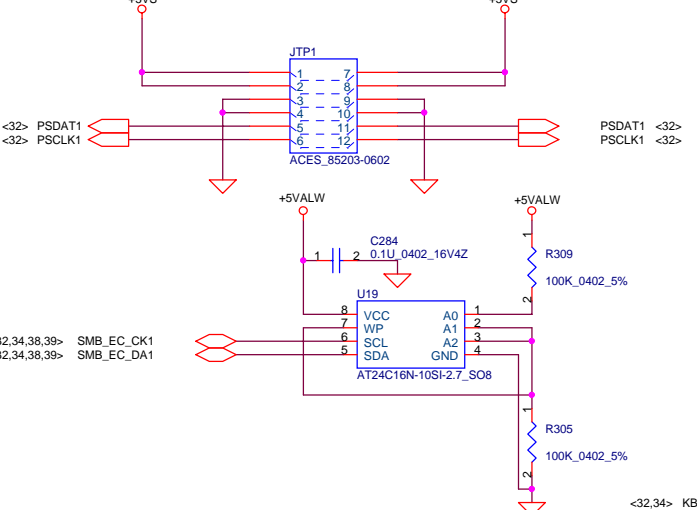
# Killer switch



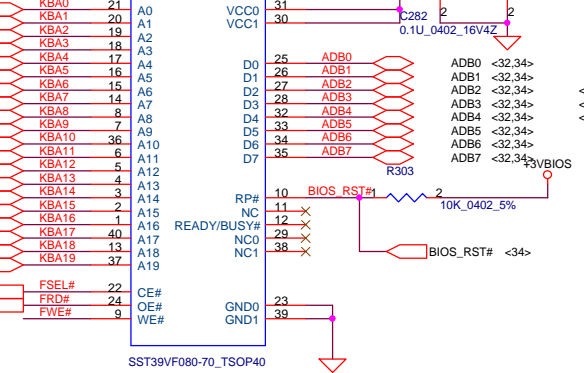
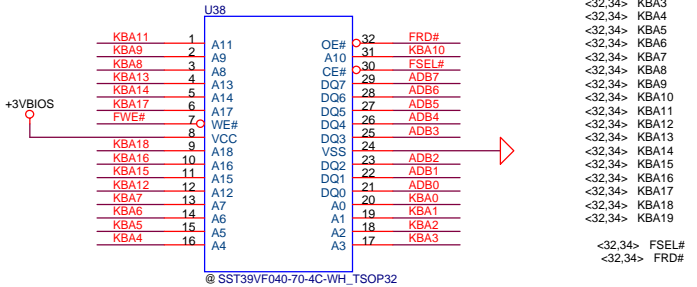
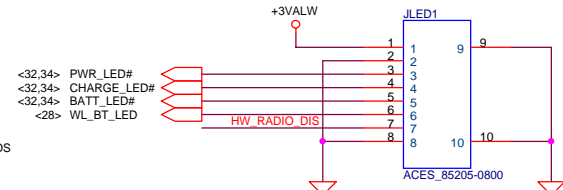
# SW Board



# T/P

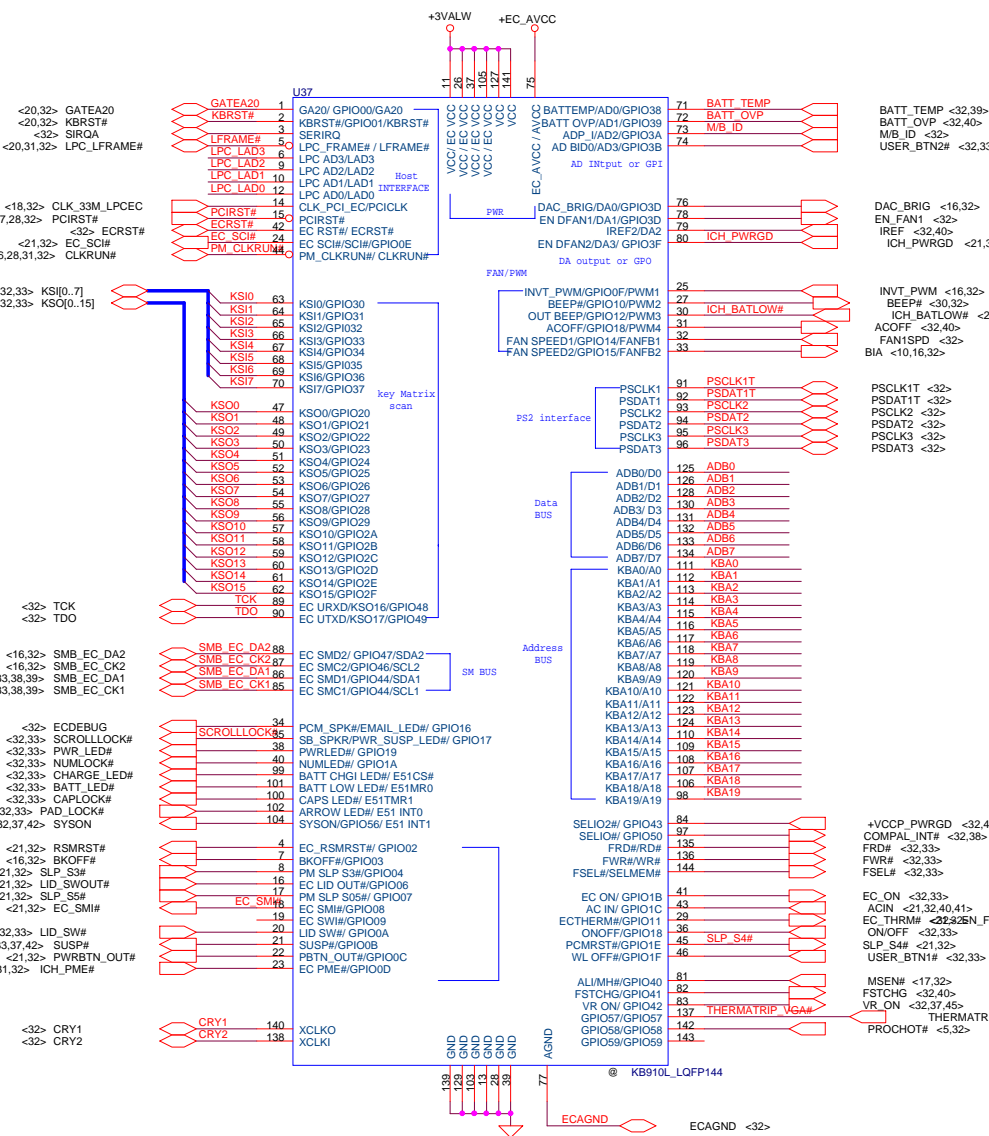


# LED Board

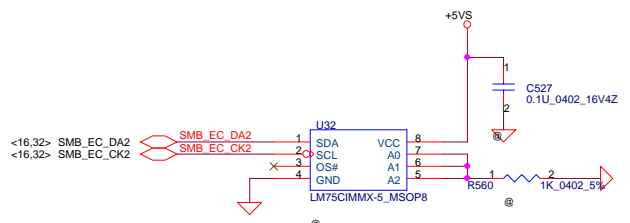
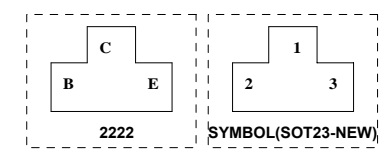
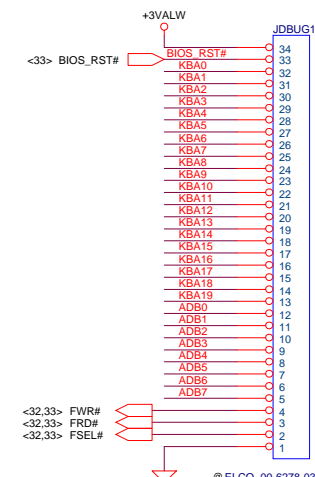


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<20,31,32> LPC\_LAD[0..3]



ADB[0..7] <32,33>  
KBA[0..19] <32,33>



BATT\_TEMP <32,39>  
BATT\_OVP <32,40>  
MB\_ID <32,40>  
USER\_BTN2# <32,33>

DAC\_BRIG <16,32>  
EN\_FAN1 <32>  
IREF <32,40>  
EN\_DFAN2/DA3/GPIO3F <32,33>

INVT\_PWM <16,32>  
BEEP# <30,32>  
ICH\_BATLOW# <21,32>  
ACOFF/GPIO10/PWM4 <32,33>  
FAN1SPD <32>  
FAN\_SPEED1/GPIO14/FANF81 <32,33>  
FAN\_SPEED2/GPIO15/FANF82 <32,33>

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PSDAT1T <32>  
PSCLK2 <32>  
PSDAT2 <32>  
PSCLK3 <32>  
PSDAT3 <32>

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ADB1 <32>  
ADB2 <32>  
ADB3 <32>  
ADB4 <32>  
ADB5 <32>  
ADB6 <32>  
ADB7 <32>

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KBA5/A5 <32,33>  
KBA6/A6 <32,33>  
KBA7/A7 <32,33>  
KBA8/A8 <32,33>  
KBA9/A9 <32,33>  
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KBA17/A17 <32,33>  
KBA18/A18 <32,33>  
KBA19/A19 <32,33>

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EC\_SMC2/GPIO46/SCL2 <32,33>  
EC\_SMD1/GPIO44/SDA1 <32,33>  
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SB\_SPKR/PWR\_SUSP\_LED#/GPIO17 <32,33>  
PWR\_LED#/GPIO19 <32,33>  
NUMLED#/GPIO1A <32,33>  
BATT\_CHG\_LED#/E51CS# <32,33>  
BATT\_LOW\_LED#/E51MR0 <32,33>  
CAPS\_LED#/E51TR1 <32,33>  
ARROW\_LED#/E51INT0 <32,33>  
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SELIO1/GPIO50 <32,33>  
FRD#/GPIO3 <32,33>  
FWR#/WR# <32,33>  
FSEL#/SELMEM# <32,33>

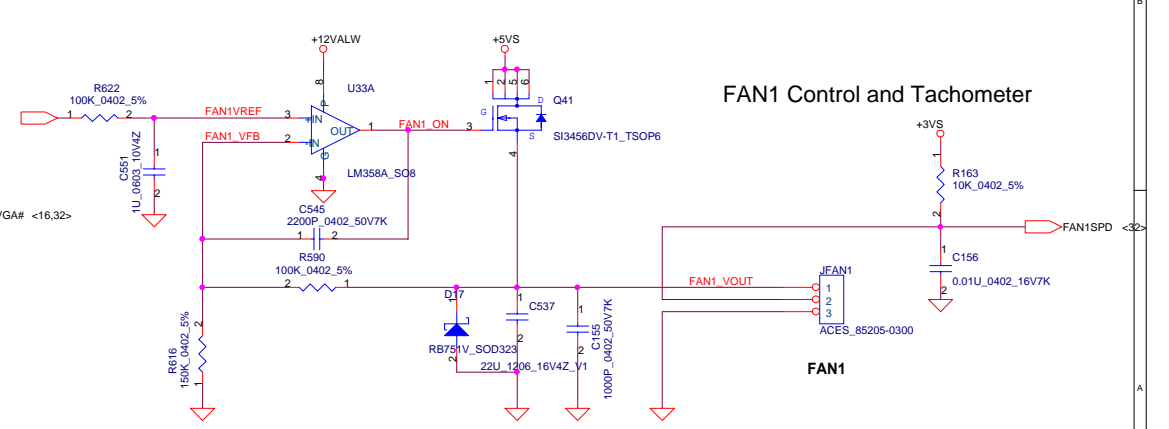
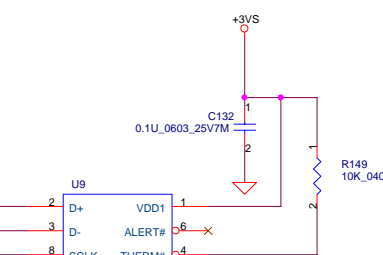
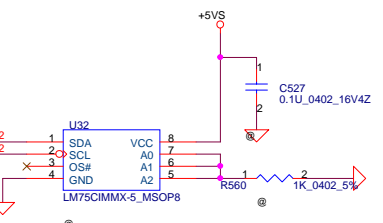
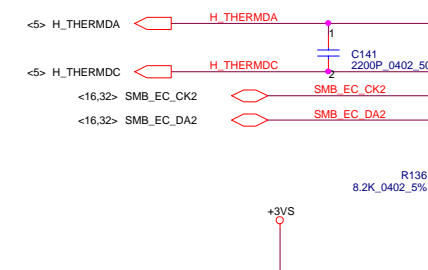
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AC\_IN/GPIO1C <32,33>  
ECTHERM#/GPIO11 <32,33>  
ONOFF/GPIO18 <32,33>  
PCMRST#/GPIO1E <32,33>  
WL\_OFF#/GPIO1F <32,33>

ALIMH#/GPIO40 <32,33>  
FSTCHG#/GPIO41 <32,33>  
VR\_ON/GPIO42 <32,33>  
GPIO57/GPIO57 <32,33>  
GPIO58/GPIO58 <32,33>  
GPIO59/GPIO59 <32,33>

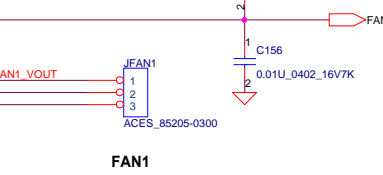
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FWR# <32,33>  
FSEL# <32,33>

EC\_ON <32,33>  
AC\_IN <32,33>  
ECTHERM# <32,33>  
ON/OFF <32,33>  
SLP\_S4# <32,33>  
USER\_BTN1# <32,33>

MSEN# <17,32>  
FSTCHG# <32,40>  
VR\_ON <32,37,45>  
THERMATRIP\_VGA# <16,32>  
PROCHOT# <5,32>



### FAN1 Control and Tachometer



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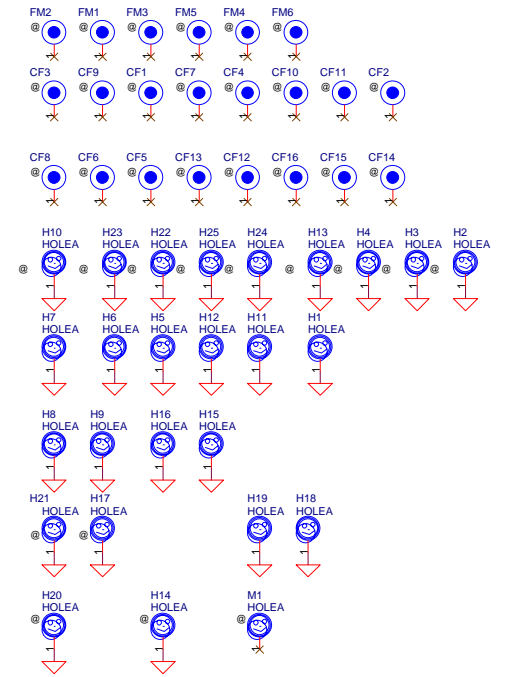
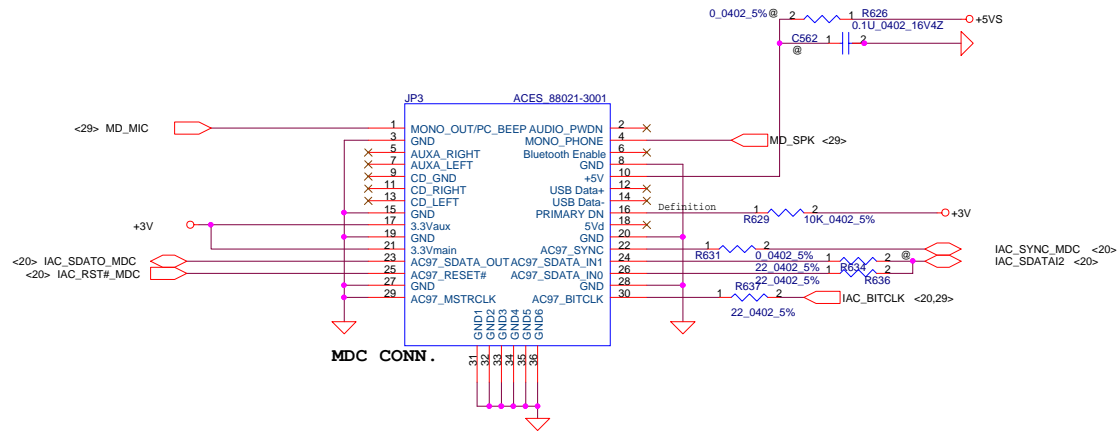
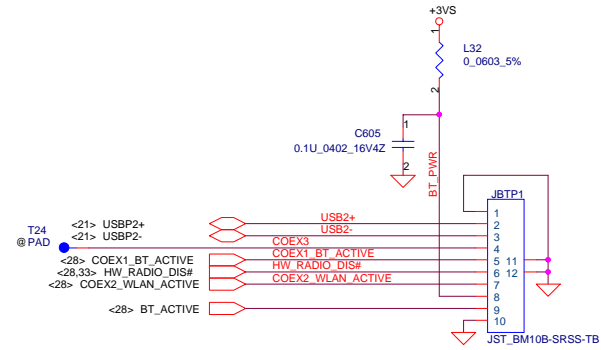
Compal Electronics, Inc.

Thermal sensor and Fan

LA-2361

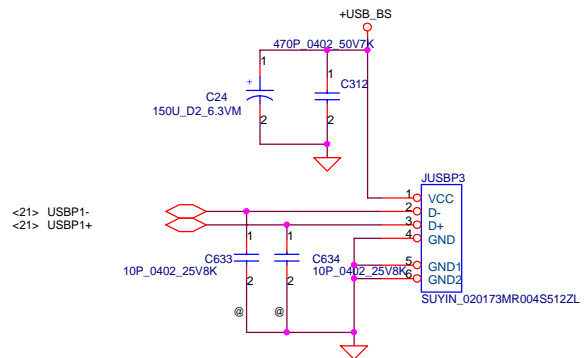
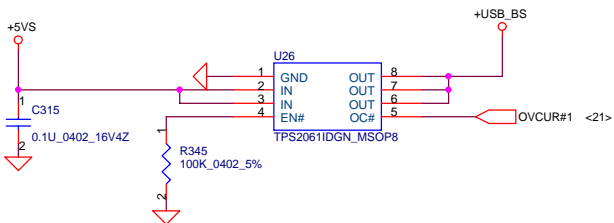
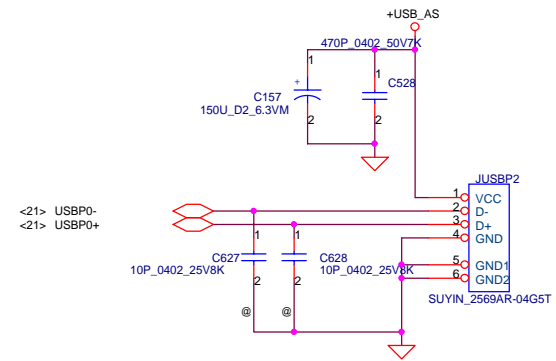
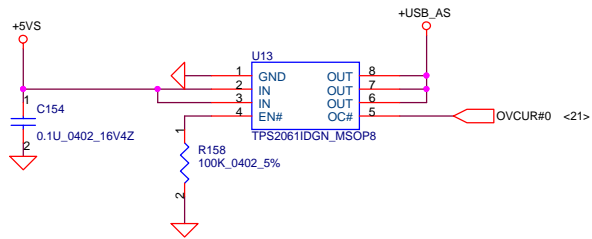
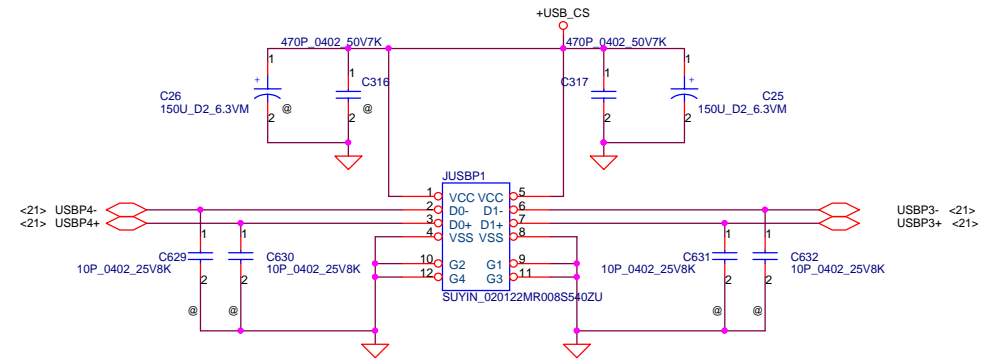
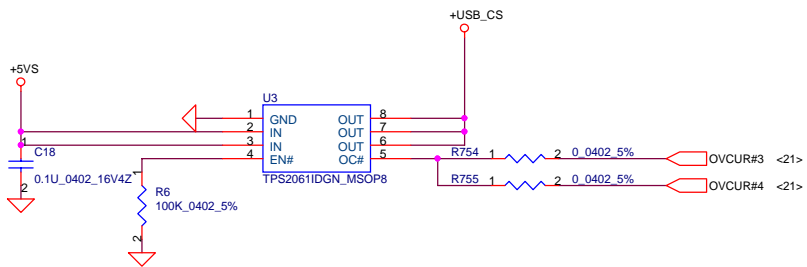
Monday, October 04, 2004

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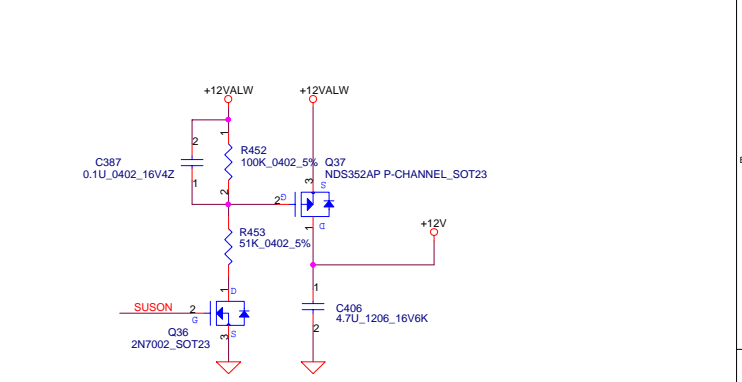
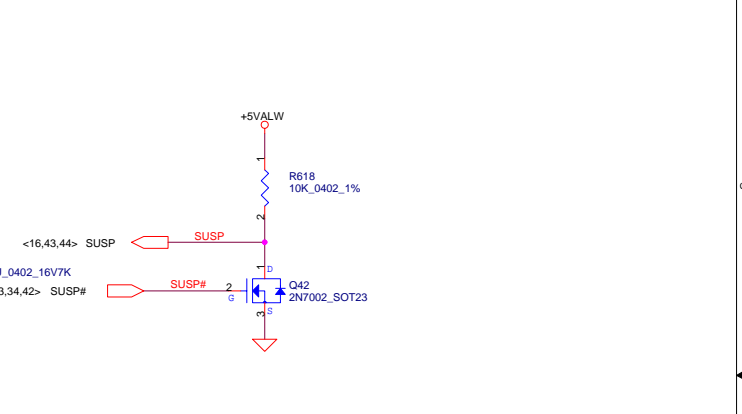
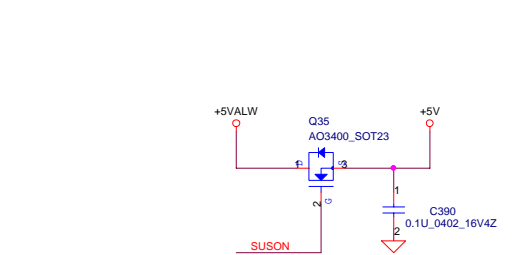
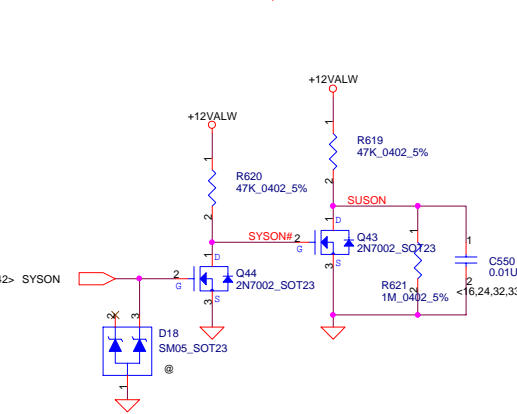
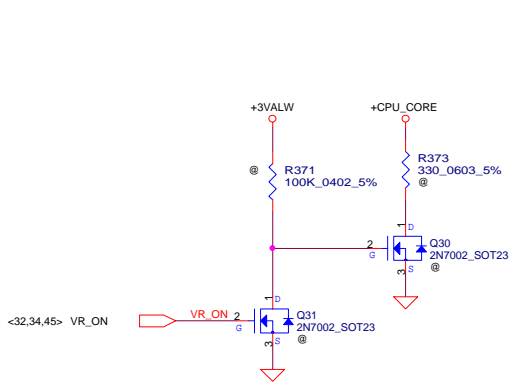
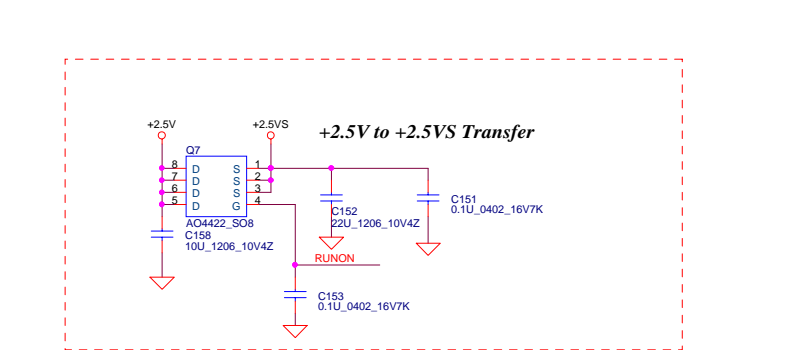
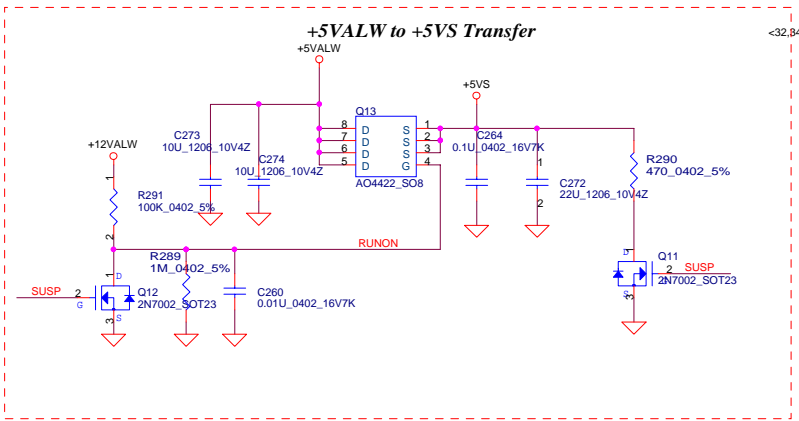
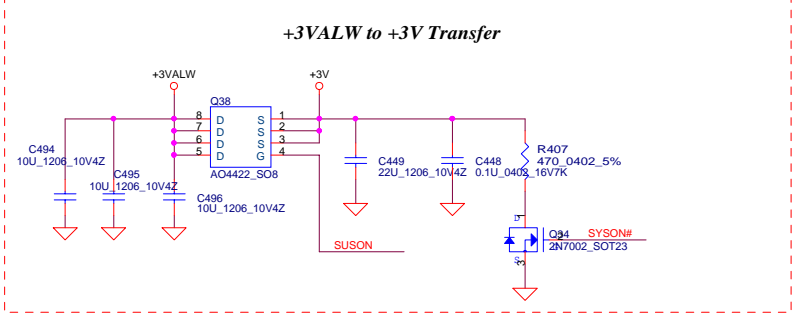
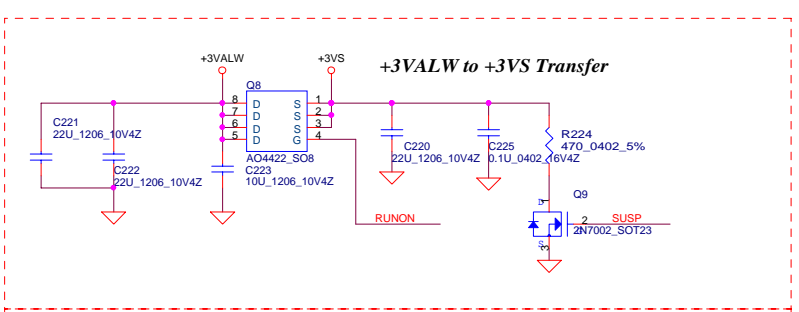


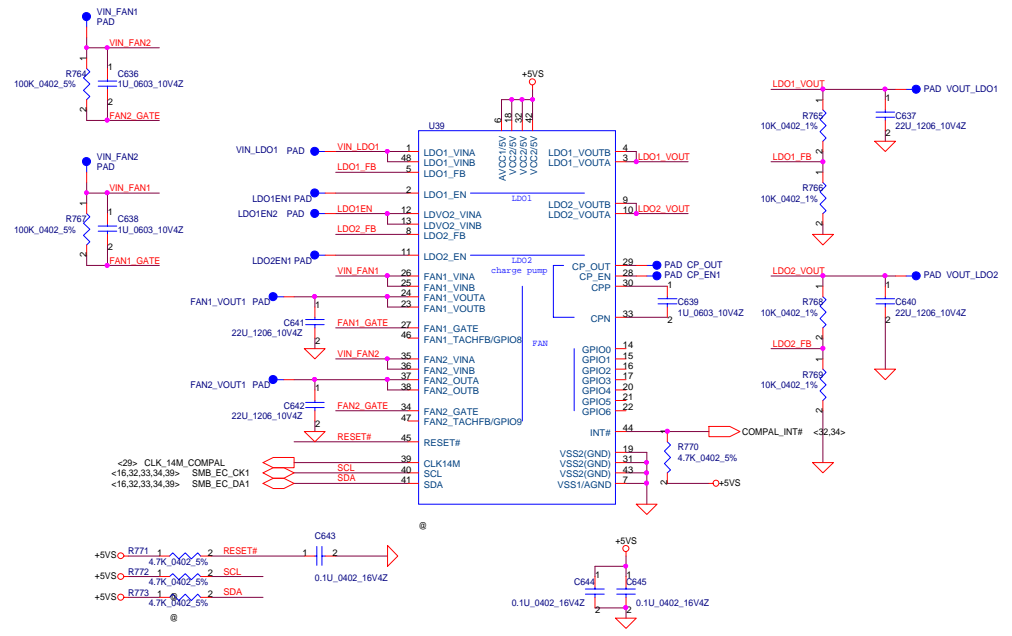
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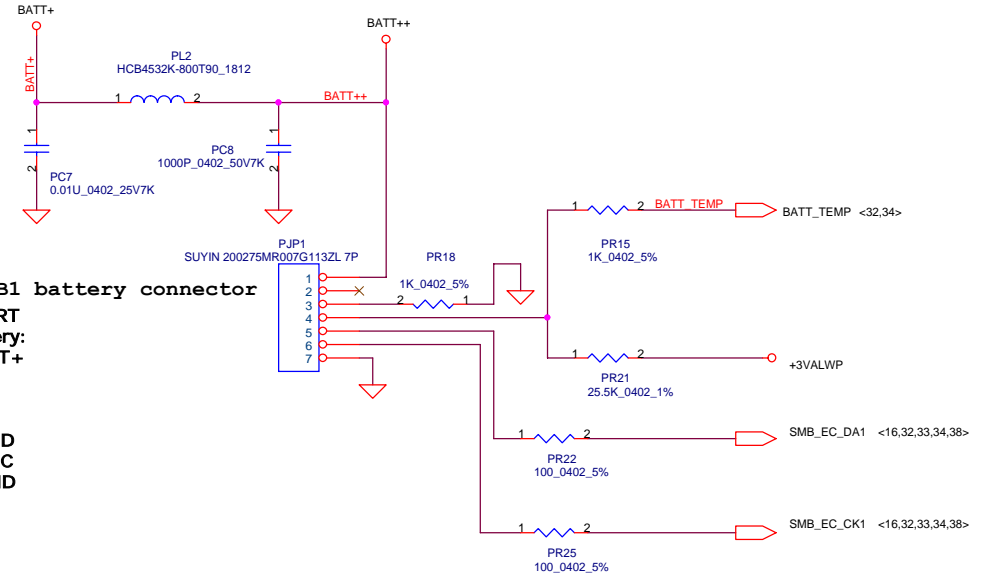
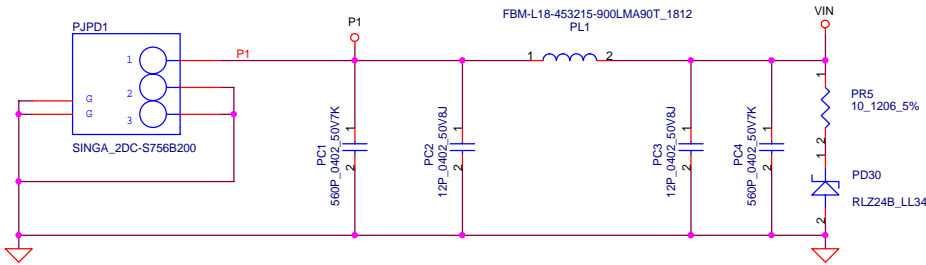
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	<b>SUBWOOFER,BT PORT and MDC</b>		
	Size	Document Number	Rev
	<b>LA-2361</b>		0.0
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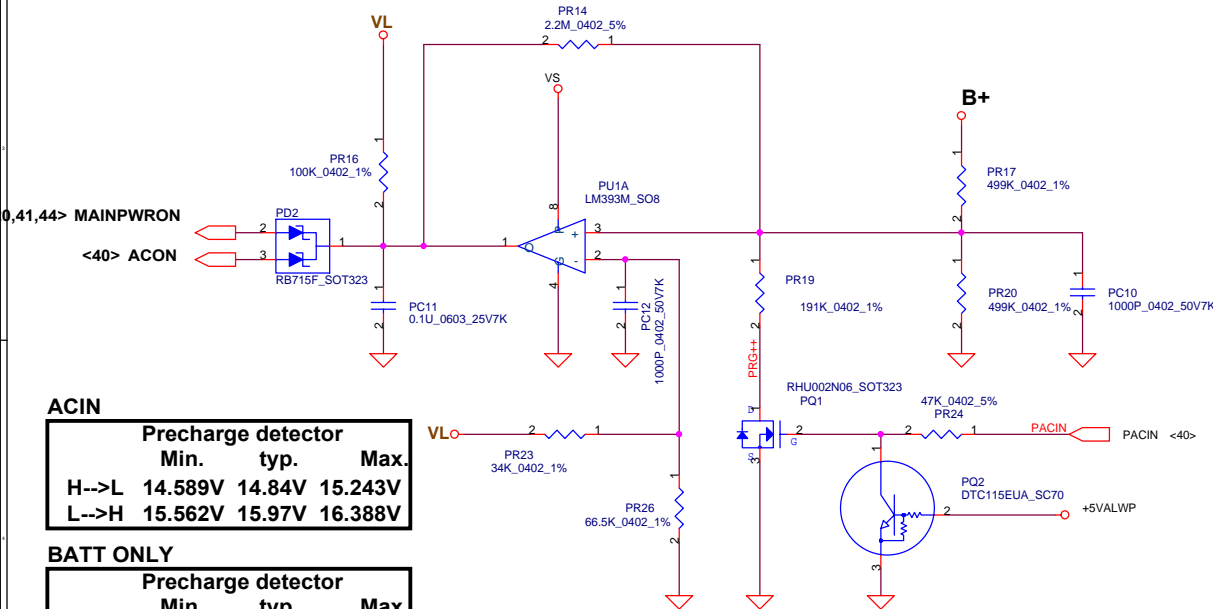
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**PJPB1 battery connector**  
**SMART Battery:**  
 1.BAT+  
 2.ID  
 3.B/I  
 4.TS  
 5.SMD  
 6.SMC  
 7.GND

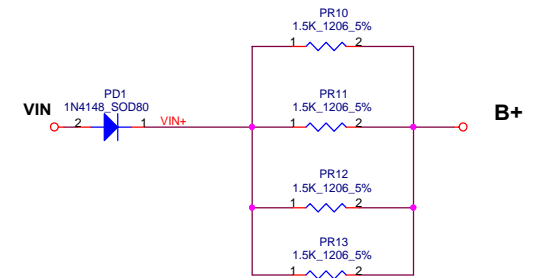


**ACIN**

Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

**BATT ONLY**

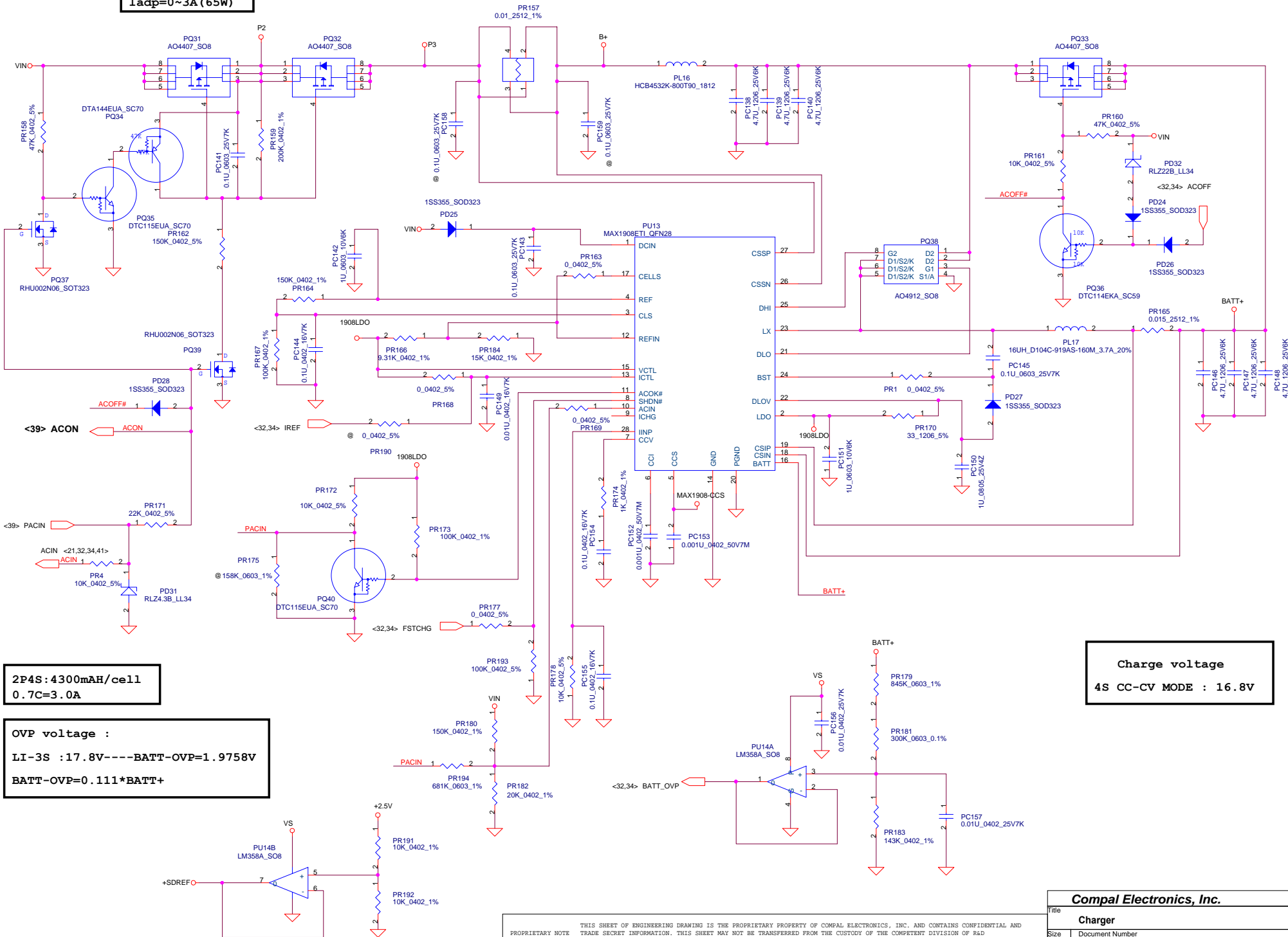
Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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<b>Compal Electronics, Inc.</b>		
Title		
<b>DCIN &amp; DETECTOR &amp; Precharge</b>		
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I<sub>adp</sub>=0~3A (65W)



2P4S: 4300mAh/cell  
0.7C=3.0A

OVP voltage :  
LI-3S : 17.8V----BATT-OVP=1.9758V  
BATT-OVP=0.111\*BATT+

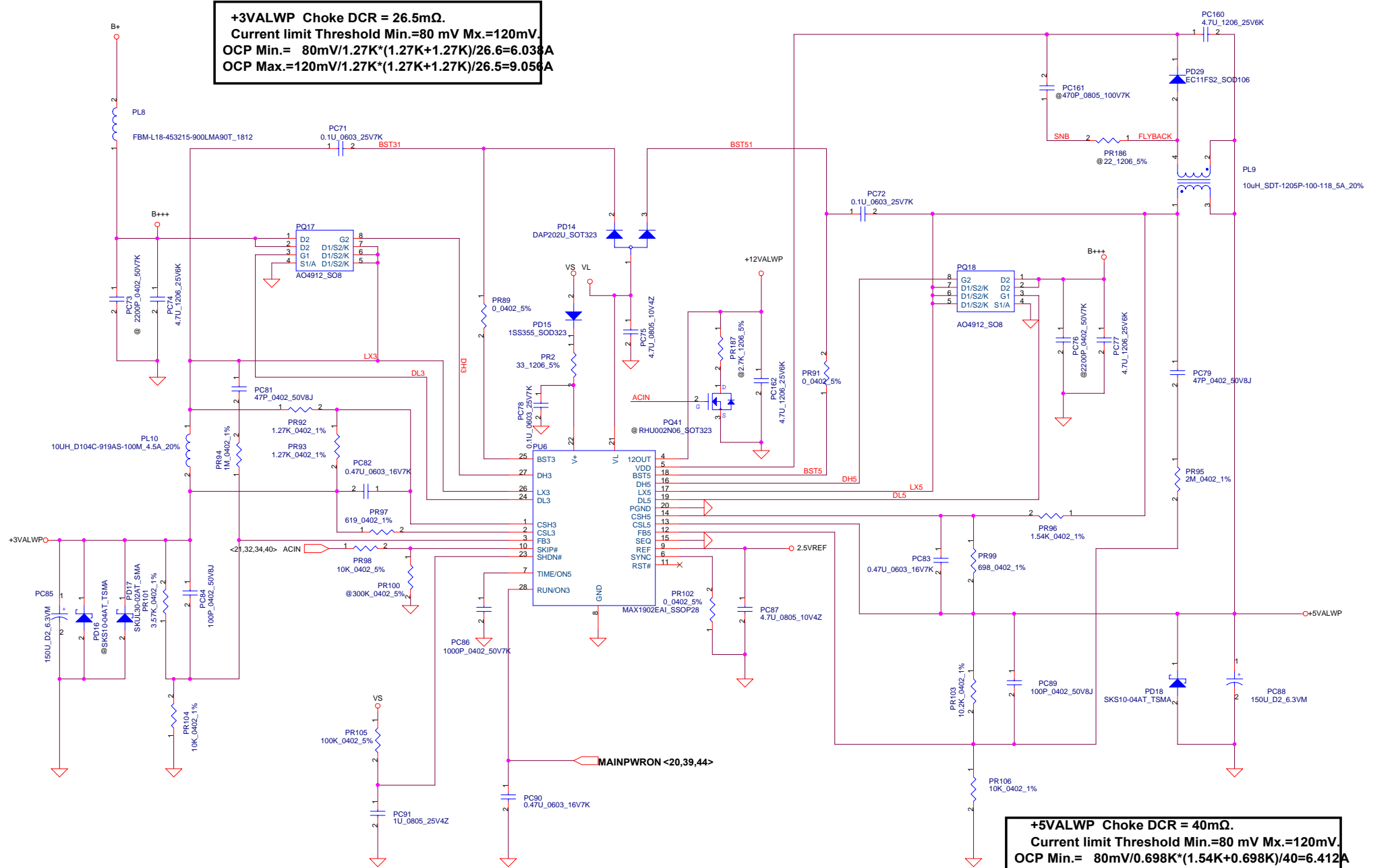
Charge voltage  
4S CC-CV MODE : 16.8V

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Compal Electronics, Inc.		
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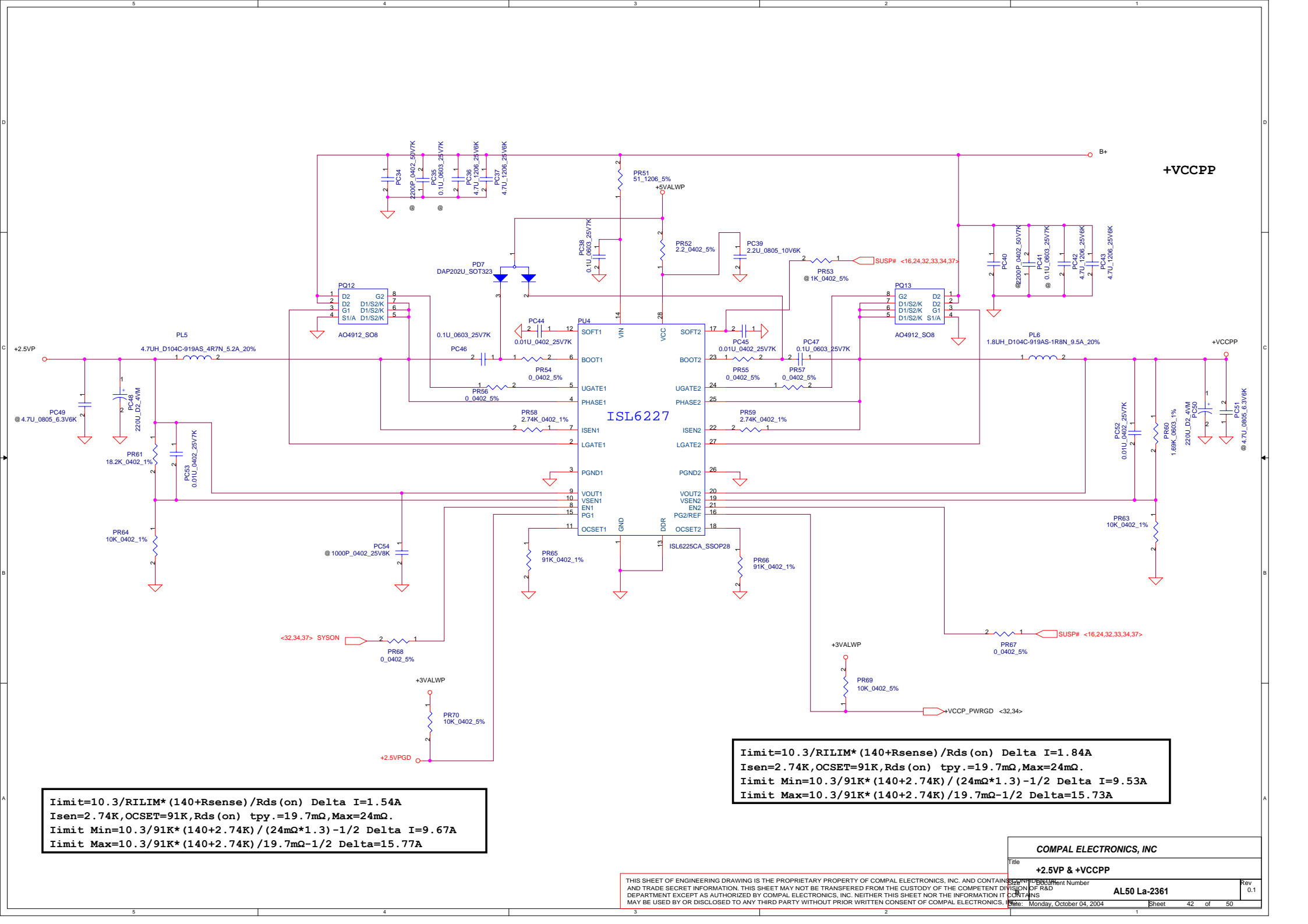
**+3VALWP Choke DCR = 26.5mΩ.  
 Current limit Threshold Min.=80 mV Mx.=120mV.  
 OCP Min.= 80mV/1.27K\*(1.27K+1.27K)/26.6=6.03A  
 OCP Max.=120mV/1.27K\*(1.27K+1.27K)/26.5=9.05A**



**+5VALWP Choke DCR = 40mΩ.  
 Current limit Threshold Min.=80 mV Mx.=120mV.  
 OCP Min.= 80mV/0.698K\*(1.54K+0.698K)/40=6.41A  
 OCP Max.=120mV/0.698K\*(0.698K+1.54K)/40=9.593A**

**RS2(PR64)=RS1(PR58)\*RS3(PR61)/(RS1+RS3)  
 L/RL(DCR)=RS1\*RS3(PR61)/(RS1+RS3)\*Cs(PC56)**

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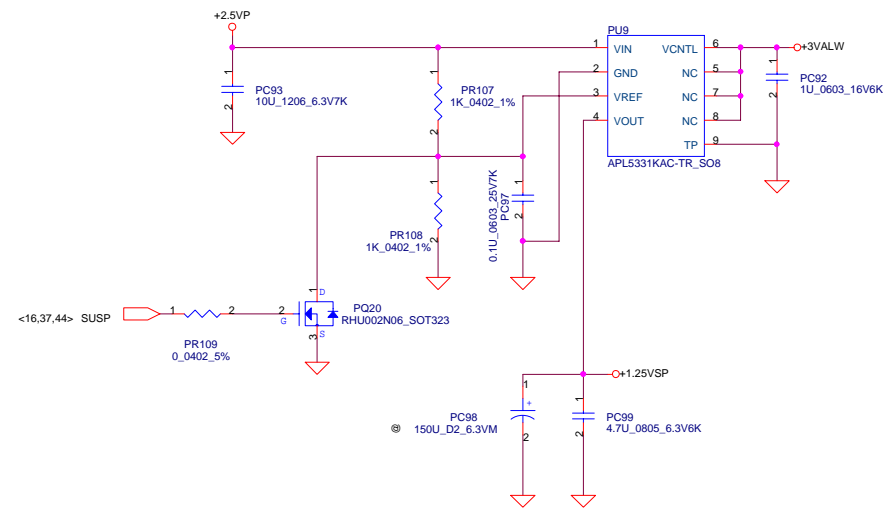
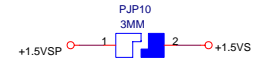
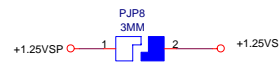
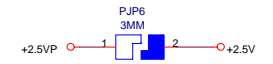
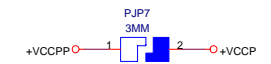
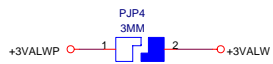
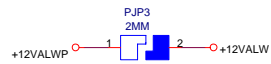
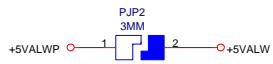


$I_{limit} = 10.3 / R_{ILIM} * (140 + R_{sense}) / R_{ds(on)}$  Delta I = 1.54A  
 $I_{sen} = 2.74K, OCSET = 91K, R_{ds(on)}$  tpy. = 19.7mΩ, Max = 24mΩ.  
 $I_{limit\ Min} = 10.3 / 91K * (140 + 2.74K) / (24mΩ * 1.3) - 1/2$  Delta I = 9.53A  
 $I_{limit\ Max} = 10.3 / 91K * (140 + 2.74K) / 19.7mΩ - 1/2$  Delta = 15.77A

$I_{limit} = 10.3 / R_{ILIM} * (140 + R_{sense}) / R_{ds(on)}$  Delta I = 1.84A  
 $I_{sen} = 2.74K, OCSET = 91K, R_{ds(on)}$  tpy. = 19.7mΩ, Max = 24mΩ.  
 $I_{limit\ Min} = 10.3 / 91K * (140 + 2.74K) / (24mΩ * 1.3) - 1/2$  Delta I = 9.53A  
 $I_{limit\ Max} = 10.3 / 91K * (140 + 2.74K) / 19.7mΩ - 1/2$  Delta = 15.73A

<b>COMPAL ELECTRONICS, INC</b>	
<b>+2.5VP &amp; +VCCPP</b>	
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**Compal Electronics, Inc.**

**+1.8VSP & +1.25VSP**

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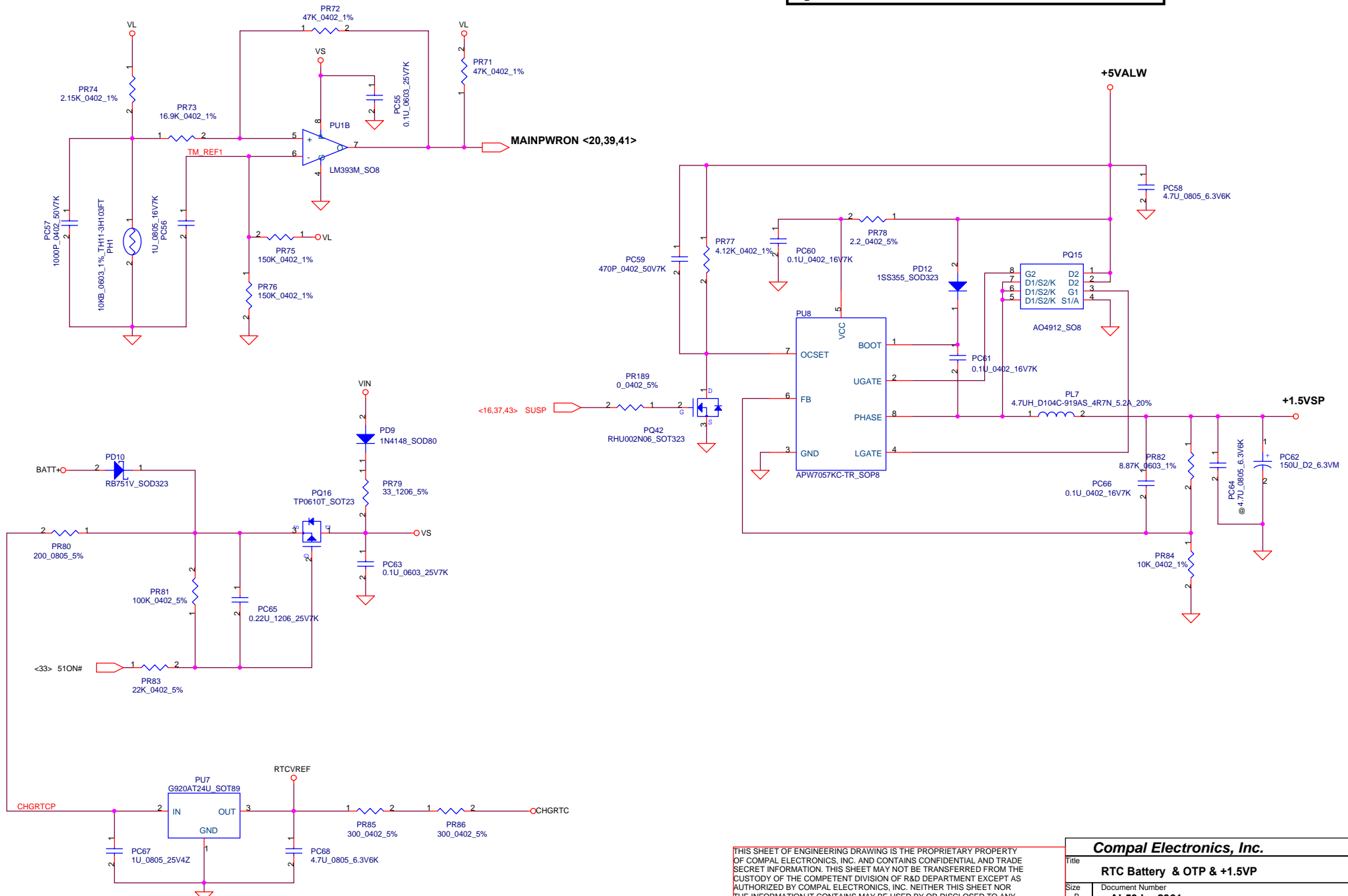
PH2 under CPU botten side :  
 CPU thermal protection at 80 degree C  
 Recovery at 44(45) degree C

$$I_{peak} = I_{ocset} * R_{ocset} / R_{DS(ON)} \text{ high side}$$

$$I_{ocset} = 40\mu A, R_{ocset} = 4.12K, R_{DS(on)} = 25.5m\Omega$$

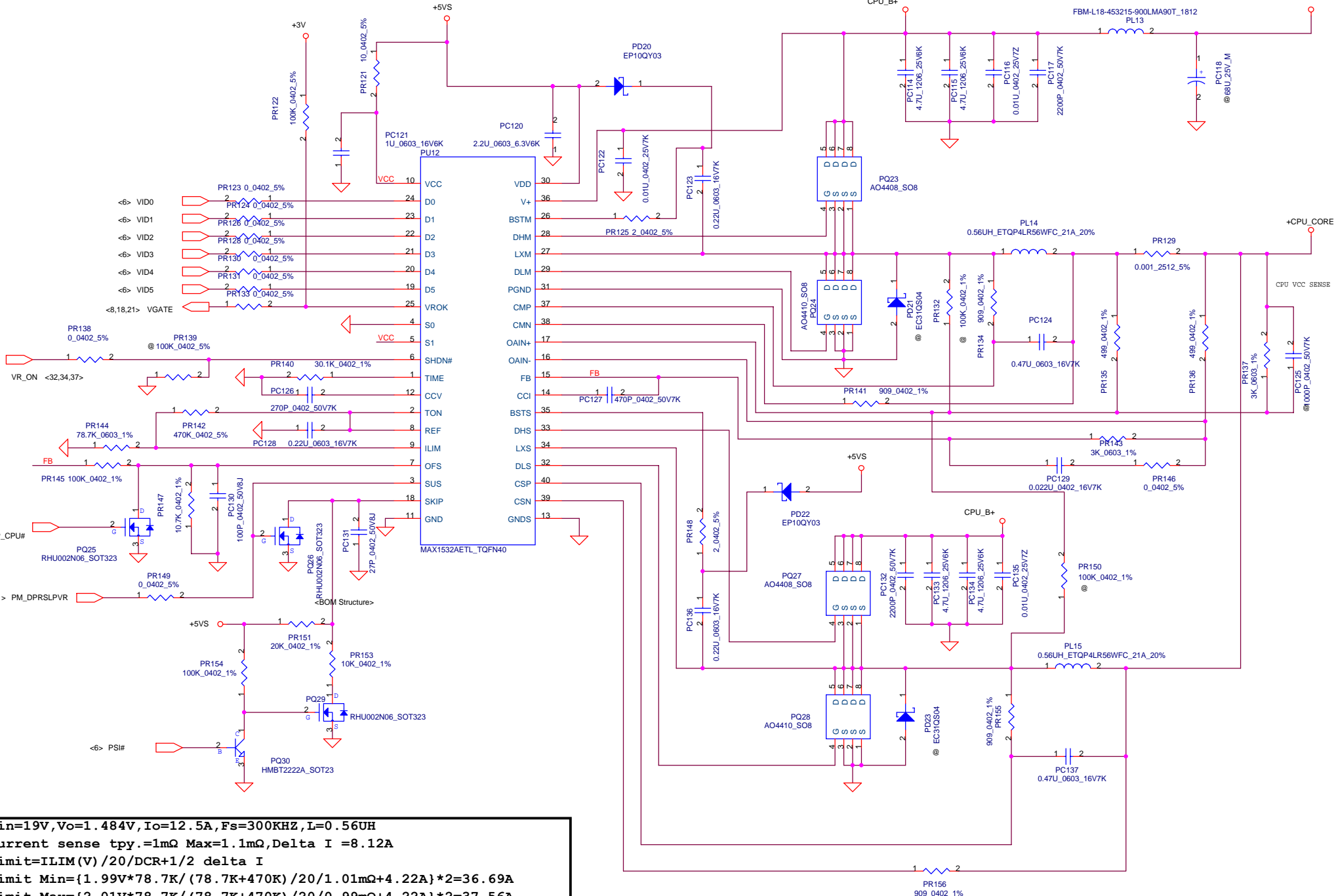
$$I_{peak \ min} = 40\mu A * 4.12 / (25.5 * 1.3) = 4.97A$$

$$I_{peak \ max} = 40\mu A * 4.12 / 25.5 = 6.46A$$



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<b>Compal Electronics, Inc.</b>		
Title <b>RTC Battery &amp; OTP &amp; +1.5VP</b>		
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$V_{in}=19V, V_o=1.484V, I_o=12.5A, F_s=300KHZ, L=0.56UH$   
 Current sense tpy.= $1m\Omega$  Max= $1.1m\Omega$ ,  $\Delta I = 8.12A$   
 $I_{limit} = I_{LIM}(V) / 20 / DCR + 1/2 \Delta I$   
 $I_{limit \text{ Min}} = \{1.99V * 78.7K / (78.7K + 470K) / 20 / 1.01m\Omega + 4.22A\} * 2 = 36.69A$   
 $I_{limit \text{ Max}} = \{2.01V * 78.7K / (78.7K + 470K) / 20 / 0.99m\Omega + 4.22A\} * 2 = 37.56A$

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1					I CH_PME# pull up +3VALW add R 10K	0.2	DVT
2					LID_SW# pull up +3VALW add R 10K		
3					SB +1.5V regulator footprint error		
4					SB +1.5V regulator footprint error U8 need to reverse		
5					R76 take off		
6					PR191 power plane 2.5vref change to +2.5V		
7					R398 remove to R401		
8					H_DPRSLP# add pull up to +vccp power plane POP R546		
9					POP U9 for lose and foot print error		
10					U3 pin6 & pin 7 need to swap		
11					Add R476/7 40.2 Ohm for memory		
12					R259 short		
13					PR122 chang power plane to +3V for EC voltage leakage		
14					Add R224/R290/R407 470ohm and Q34/9/11 2N7002		
15					ADD R 39K//220p to GND at R518 for modify SI RQ		
16					Reverse the JHP1 & JMI C1 Symble error		
17							
18							
19							
20							

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	Delete the charge circuit.	Delete the charge circuit.	0.2	38	1.Delete the PU5 IC LM393M (SM). 2.Delete PD1 S DIO 1N4148 (SM). 3.Delete PR10,PR11,PR12,PR13 S RES 1/4W 1.5K +-5% 1206.	0.2	DVT
2	Change the CPU OTP circuit from active H to active L.	Change the CPU OTP circuit from active H to active L.	0.2	43	1.Delete PQ14 S TR DTC115EUA NPN (UMT3). 2..Delete PD8 S DIO 1SS355. 3.Change PR75 and PR76 from S RES 1/16W 100K +-1% 0402 to S RES 1/16W 150K +-1% 0402. 4.Change PR73 from S RES 1/16W 15K +-1% 0402 to S RES 1/16W 16.9K +-1% 0402. 5.Change PC56 from S CER CAP .22U 16V K X7R 0603 to S CER CAP 1U 16V K X7R 0805 6.Change PR74 from S RES 1/16W 3.4K +-1% 0402 to S RES 1/16W 2.15K +-1% 0402.	0.2	DVT
3	For cost down solution.	To cost down for +1.5VP.	0.2	43	1.Change the PD12 from DIO 1N4148 (SM) to DIO 1SS355.	0.2	DVT
4	For cost down solution.	To cost down for RTC charge circuit..	0.2	43	1.Delete the PD33 S ZEN DIO RLZ4.3B (LL-34).	0.2	DVT
5	To prevent the KB-910 damag.	To prevent the KB-910 damag.	0.2	40	1.Change the PD17 from SCH DIO SKS10-04AT TSMA to SCH DIO SKUL30-02AT THIN SMA.	0.2	DVT
6	For cost down solution.	To cost down for +1.5VP for +12VALWP circuit.	0.2	40	1.Delete PR187 S RES 1/8W 2.7K +-5% 1206 S7.	0.2	DVT
7	For cost down solution.	To cost down for DDR 2.5V.	0.2	41	1.Delete PR62 S RES 1/16W 0 +-5% 0402.	0.2	DVT
8	For cost down solution.	To cost down for CPU_CORE.	0.2	44	1.Delete PR127 and PR152 S RES 1/16W 0 +-5% 0402.	0.2	DVT
9	For cost down solution.	To cost down for snubber circuit.	0.2	40	1.Deete PR127 and PR152 S RES 1/16W 0 +-5% 0402. 2.Delete the PC161 S CER CAP 470P 100V K X7R 0805.	0.2	DVT
10	For cost down solution.	To cost down for EMI capacitor.	0.2	39 40 41	1.Delete PC41,PC158 and PC159 S CER CAP .1U 25V K X7R 0603. 2.Delete PC40,PC73 and PC76 CER CAP 2200P 50V K X7R 0402.	0.2	DVT
10	Don't has pull high resister on VGATE pin.	Add pull high resister on VGATE pin.	0.2	44	1.Add the S RES 1/16W 100K +-5% 0402.	0.2	DVT
10	VCCPP output voltage has error.	Adjustment resistor divider.	0.2	41	1.Change the PR60 from S RES 1/16W 681 +-1% 0402 to S RES 1/16W 1.69K +-1% 0603.	0.2	DVT
11.	Choke Rating not enough for +1.5VP.	Choke Rating not enough for +1.5VP.	0.2	43	1.Change PL7 from 4.7UH_FDVO630-4.7UH_5.5A_20% to 4.7UH_D104C-919AS_4R7N_5.2A_20%.	0.2	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	Don't has pull down resister on SHDN# pin for charger.	Add pull down resister on SHDN# pin.	0.2	39	1.Add PR193 the S RES 1/16W 100K +-5% 0402.	0.2	DVT
2	Change the Vin Detector from LM393 to charger ACOK#.	Change the Vin Detector from LM393 to charger ACOK#.	0.2	38,39	1.Add the PQ40 S TR DTC115EUA NPN (UMT3). 2.Delete the PR3,PR4,PR8 and PR9 RES 1/16W 10K +-1% 0402. 3.Add the PR193,PR172 and PR173 RES 1/16W 100K +-5% 0402. 4.Delete PR6 the S RES 1/16W 22K +-1% 0402. 5.Delete PR1 the S RES 1/16W 1M +-1% 0402. 6.Change PR182 from S RES 1/16W 150K +-1% 0402 to S RES 1/16W 20K +-1% 0402. 7.Delete the PR7 S RES 1/16W 20K +-1% 0402. 8.Delete the PR2 S RES 1/16W 84.5K +-1% 0402. 9.Add the PR175 S RES 1/16W 158K +-1% 0402. 10.Add the PR175 S RES 1/16W 681K +-1% 0402. 11.Delete PC6 from S CER CAP .1U 25V K X7R 0603. 12..Delete PC5 from S CER CAP 1000P 50V +-10% X7R 0402.	0.2	DVT
3	For ACIN pin,	ACIN pin don't have connect to system.	0.2	39	1.Add PR4 the 10K +-5% 0402	0.2	DVT
4	+1.8VSP power rating not enough.	+1.8VSP power rating isnot enough.	0.2	42	1.Change PU10 from S IC G965-18PU SOP-8L REG to S IC APW7057KC-TR SOP-8 PWM. 2.Add PR197 S RES 1/16W 12.7K +-1% 0402. 3.Add the PQ44 S TR RHU002N06 1N SOT323 4.Delete PQ43 the S TR AO4912 2N SO8 W/D 5.Add PD33 the S DIO 1SS355. 6.Add PR195 the S RES 1/16W 2.2 +-5% 0402 7.Add PR198 the S RES 1/16W 10K +-1% 0402. 8.Add PR196 the S RES 1/16W 4.12K +-1% 0402 9.Add the PC167 the S CER CAP 4.7U 10V Z Y5V 0805. 10.Add the PC164 S CER CAP 470P 50V +-10% X7R 0402. 11.Add the PC163,PC165 and PC168 S CER CAP .1U 16V +-10% X7R 0402 12.Delete PC96 the S CER CAP 10U 6.3V K X7R 1206. 13.Add the PC166 S POLY CAP 150U 6.3V M V(D2) T520 LESR. 14.Add PL18 the S COIL 5.0UH +-20% TPRH6D38-5ROM-N 2.9A.	0.2	DVT
5	VCCP's transients cannot meet spec.	VCCP's transients cannot meet spec.	0.2	41	1.Change PC50 from S POLY CAP 150U 6.3V M V(D2) T520 LESR to S POLY C 220U 4V M V(D2) T520 LESR. 2.Change PL6 from S COIL 4.7UH +-20% D104C-919AS-4R7M 5.2A to S COIL 1.8UH +-30% D104C-919AS-1R8N 9.5A.	0.2	DVT
6	For CPU_CORE's EMI,	For CPU_CORE's EMI,	0.2	44	1.Change the PR125 and PR148 from S RES 1/16W 0 +-5% 0402S to RES 1/16W 2 +-5% 0402.	0.2	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1.	CPU's transients cannot meet spec.	Add one current sense on phase 2.	0.2	44	1.Delete PC124 and PC137 the S CER CAP 0.47U 16V +-10% X7R 0603. 2.Delete PR134,PR141,PR155 and PR156 the S RES 1/16W 909+-1% 0402. 3.Add PR134 S RES 1W 0.01 +-1%2512.	0.2	DVT
2.	PACIN pin's high level is only 2.3V.	To adjust PACIN pin's level.	0.2	39	1.Delete PR175 the S RES 1/16W 158K+-1% 0402. 2.Change the PR172 from S RES 1/16W 100K +-1% 0402 S to RES 1/16W 10K +-1% 0402.	0.2	DVT
3.	The 5VALWP rising time is faster than PACIN's.	To delay timer of 5VALWP.	0.3	40	1.Change the PR105 from S RES 1/16W 47K +-1% 0402 S to RES 1/16W 100K +-1% 0402. 2.Change the PC91 from S CER CAP .047U 25V M X7R 0603 to CAP 1U 25V Z F Y5V 0805..	0.3	DVT2
4.	The charge has error on change mode.	To adjust input and output current regulation loop compensation.	0.3	39	1.Change PC152 and PC153 from the S CER CAP 0.01U 16V +-10% X7R to CER CAP 0.001U 16V +-10% X7R.	0.3	DVT2
5.	For cost down solution.	For cost down solution.	0.3	42 43	1.Change PC58,PC68,PC95 and PC99 from the S CER CAP 4.7U 25V K X5R 1206 to CAP 4.7U 10V K X7R 0805.	0.3	DVT2
6.	The charger has EMI issue.	Add a resistor on charger's boost for EMI.	0.3	39	1.Add the PR1 S RES 1/16W 0 +-5% 0402.	0.3	DVT2
7.	Change the current limit's from sense DRC to resister.	To adjust current limit point for CPU_CORE.	0.3	44	1.Change the PR142 from S RES 1/16W 200K +-5% 0402 to S RES 1/16W 470K +-5% 0402.	0.3	DVT2
8.	To preven in-rush current for B+ of MAX1902.	To preven in-rush current for B+ of MAX1902.	0.3	40	1.Add PR2 S RES 1/8W 33 +-5% 1206.	0.3	DVT2
9.	The CPU's dual choke will shortage.	Change to single choke.	0.3	44	1.Add PQ26 SB502060000 S TR RHU002N06 1N SOT323. 2.Add PR134,PR141,PR155,PR156 S RES 1/16W 909 +-1% 0402. 3.Delete PL14 S COIL .5UH +-30% CXZT1050-R50 28A. 4.Add the PL14,PL15 S COIL .56UH +-20% ETQP4LR56 WFC 21A. 5.Add the PC124,PC137 0.47U 16V +-10% X7R 0603 S8. 4.Add the PL14,PL15 S COIL .56UH +-20% ETQP4LR56 WFC 21A.	0.3	DVT2
10.	Delete the +1.8VSP on M/B.	Delete the +1.8VSP on M/B.	0.3	42	1.Delete the PU10 S IC APW7057KC-TR SOP-8 PWM. 2.Delete the PQ43 S TR AO4912 2N SO8 W/D. 3.Delete the PR188 S RES 1/16W 0 +-5% 0402. 4.Delete the PR195 S RES 1/16W 2.2 +-5% 0402 5.Delete the PR196 S RES 1/16W 4.12K +-1% 0402 6.Delete the PR198 S RES 1/16W 10K +-1% 0402 7.Delete the PR197 S RES 1/16W 12.7K +-1% 0402. 8.Delete the PL18 S COIL 5.0UH +-20% TPRH6D38-5R0M-N 2.9A. 9.Delete the PC166 S POLY CAP 150U 6.3V M V(D2) T520 LESR. 10.Change the PC75 and PC87 from S CER CAP 4.7U 10V Z Y5V 0805 to S CER CAP 4.7U 6.3V +-10% X5R 0805 11.Delete PC95 S CER CAP 4.7U 10V Z Y5V 0805. 12.Delete PC163,PC165,PC168 .1U 16V +-10% X7R 0402. 13.Delete PC164 S CER CAP 470P 50V +-10% X7R 0402. 14.Delete PD33 S DIO 1SS355.	0.3	DVT2

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1.	Max1902 protect When power cord fast plug-out and plug-in.	Add the pre-chagre circuit.	0.3	38	1.Add PQ1 SB502060000 S TR RHU002N06 1N SOT323. 2.Add PQ2 S TR DTC115EUA NPN (UMT3). 3.Add PD2 S SCH DIO RB715F UMD3. 4.Add PD1 S DIO 1N4148 (SM) 5.Add PR10,PR11,PR12 and PR13 S RES 1/4W 1.5K +-5% 1206. 6.Add PR16 S RES 1/16W 100K +-1% 0402. 7.Add PR17 and PR20 S RES 1/16W 499K +-1% 0402. 8.Add PR19 S RES 1/16W 191K +-1% 0402. 9.Add PR23 S RES 1/16W 34K +-1% 0402. 10.Add PR26 S RES 1/16W 66.5K +-1% 0402. 11.Add PR14 S RES 1/16W 2.2M +-5% 0402. 12.Add PR24 S RES 1/16W 47K +-5% 0402. 13.Add PC10 and PC12 S CER CAP 1000P 50V +-10% X7R 0402. 14.Add PC11 S CER CAP .1U 25V K X7R 0603.	0.3	DVT2
2.	The 5VALWP choke rating is not enough.	Change the choke.	0.3	40	1.Change the PL9 from S COIL 10UH +-30% SDT-1050P-100-118 3.5A to S COIL 10uH +-20% SDT-1205P-100-118.	0.3	DVT2
3.	TP0610T will EOL.	Change the part.	0.3	43	1.Change the PQ16 S TR TP0610T 1P SOT-23 to.S TR TP0610K 1P SOT-23	0.3	DVT2

**Compal Electronics, Inc.**

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