

MODEL NAME : *NIM10*
PCB NO : *LA-5732P (DA60000EI00)*
BOM P/N : *43178431L01*

Compal Confidential

SAMOS Schematics Document

Intel Pineview-M Processor with TigerPoint

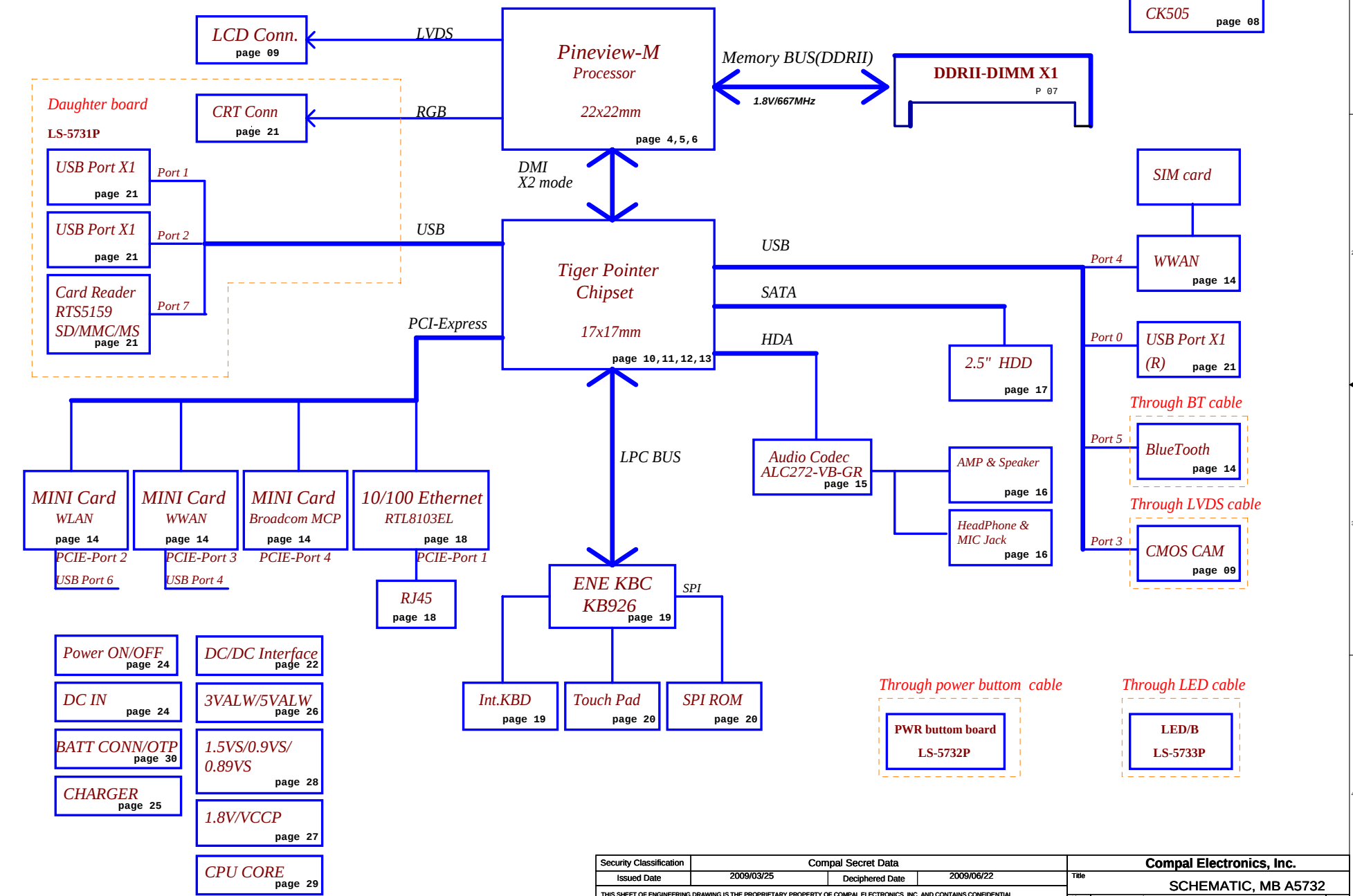
2009-8-21
REV: 0.2

@ : Nopop Component

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Model Name : NIM10
Project Code:
Project Name : LA-5732P



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+0.89VS	CORE VOLTAGE FOR CPU VGA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VS	VS always on power rail	ON	ON	ON*
+RTCBATT	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	ClOCK
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 19)

VCC	3.3V +/-5%					
ID	BRD ID	Ra	Rb	Vab (Min)	Vab (Type)	Vab (Max)
0	R01 (SSI)	NC	0	0V	0V	0.155V
1	R02 (ST)	100K +/- 5%	8.2K +/- 5%	0.168V	0.250V	0.362V
2	R10 (X build)	100K +/- 5%	18K +/- 5%	0.375V	0.503V	0.621V
3	Reserved	100K +/- 5%	33K +/- 5%	0.634V	0.819V	0.945V
4	Reserved	100K +/- 5%	56K +/- 5%	0.958V	1.185V	1.359V
5	Reserved	100K +/- 5%	100K +/- 5%	1.372V	1.650V	1.838V
6	Reserved	100K +/- 5%	200K +/- 5%	1.851V	2.200V	2.420V
7	MP	100K +/- 5%	NC	2.433V	3.300V	3.300V

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
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No PCI Device

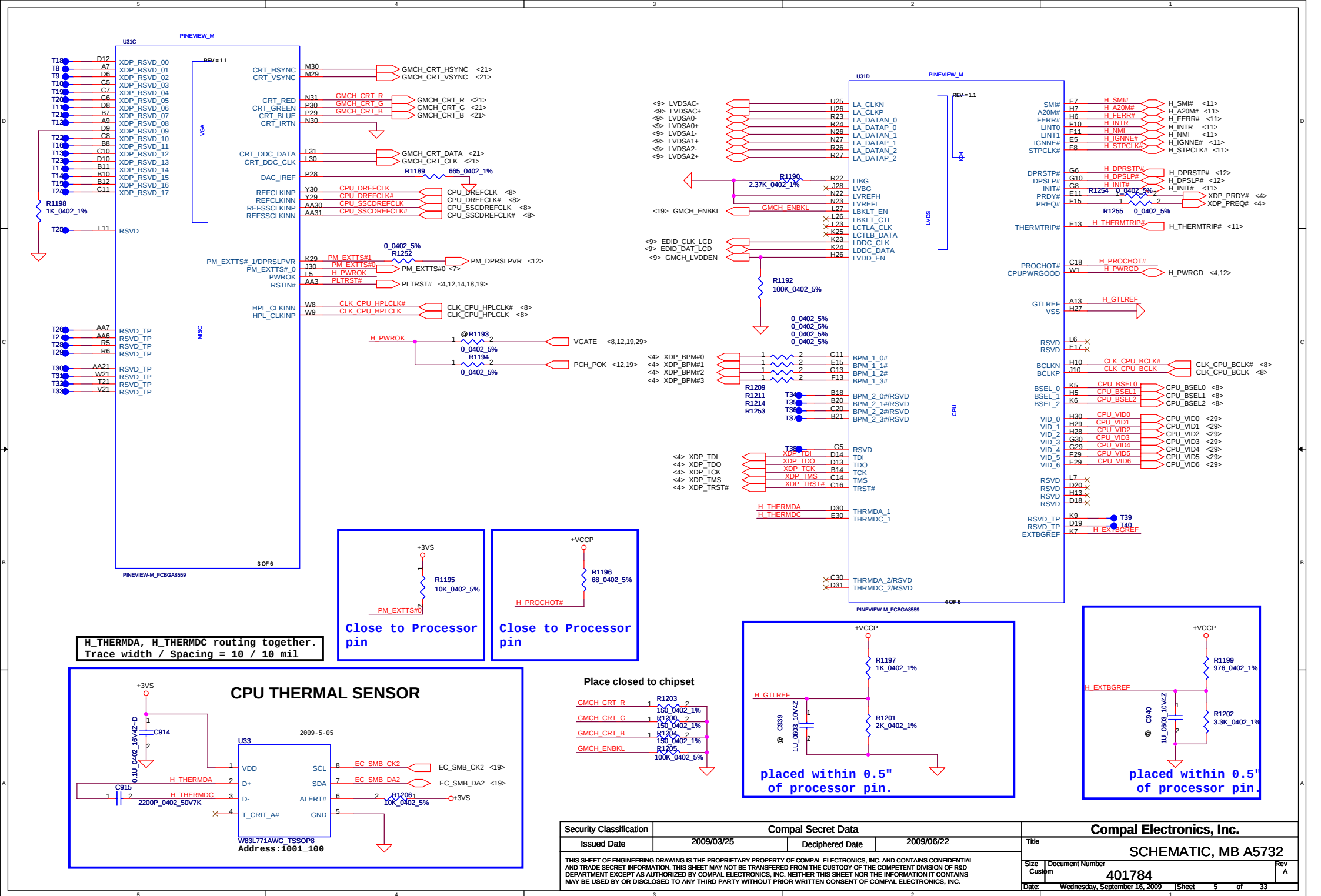
EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	W83L771AWG	1001_100X b
EEPROM(24C16/02)	1010 000X b	EMC1402	100_1100X b

Tiger Point SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb



<4> DDR_A_DQS[0..7]

<4> DDR_A_D[0..63]

<4> DDR_A_DM[0..7]

<4> DDR_A_DQS[0..7]

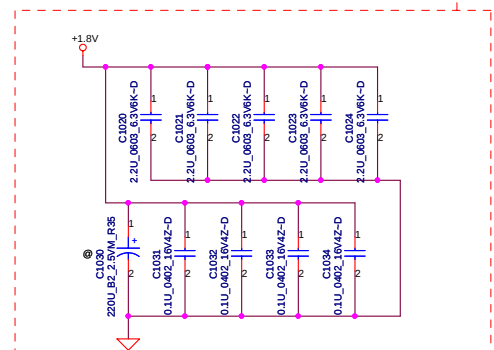
<4> DDR_A_MA[0..14]

Share +DIMM_VREF for
1.DDRII VREF
2.GMCH SM_VREF_0
SM_VREF_1

Layout Note:
Place near JDIM1

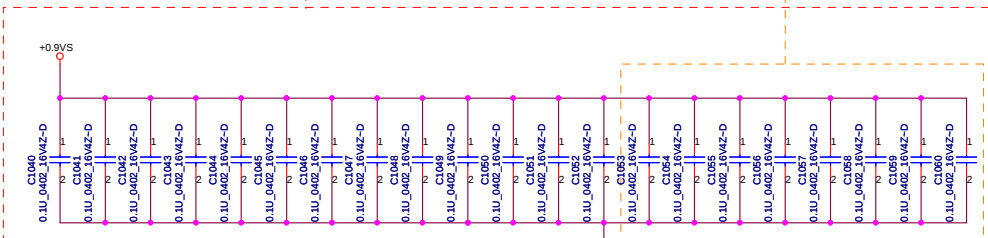
Layout Note:
Place near JDIM1

2009-5-27 modify

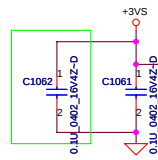


Layout Note:
Place one cap close to every 2 pull-up
resistors terminated to +0.9VS.
(check list page 18)

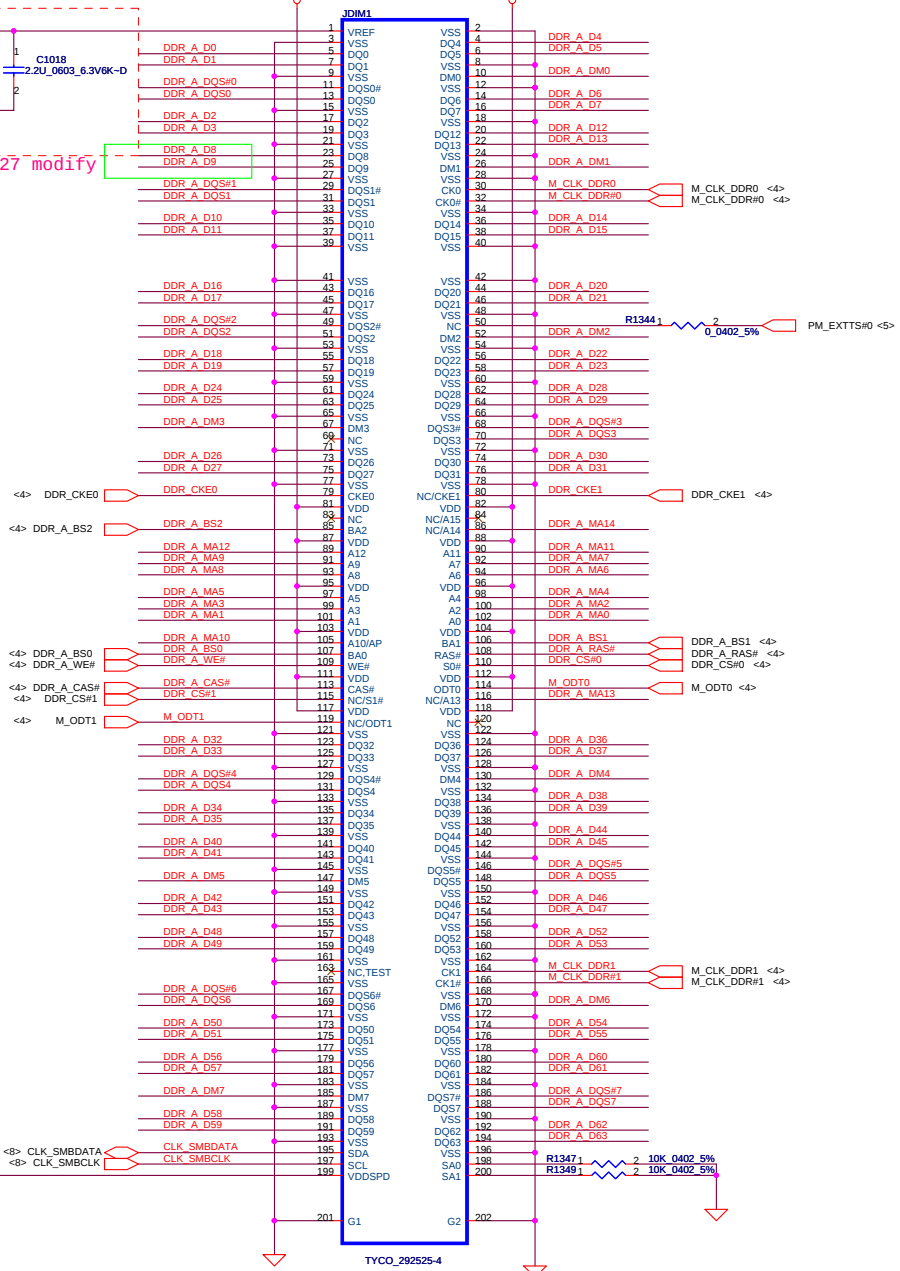
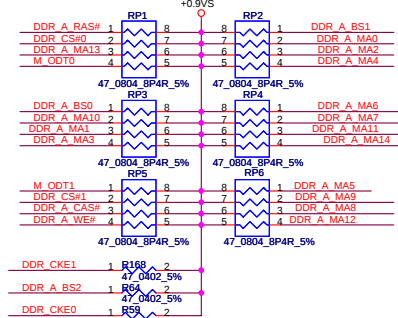
Schematic Note:
Follow Intel check list recommend, we add
8 CAP.



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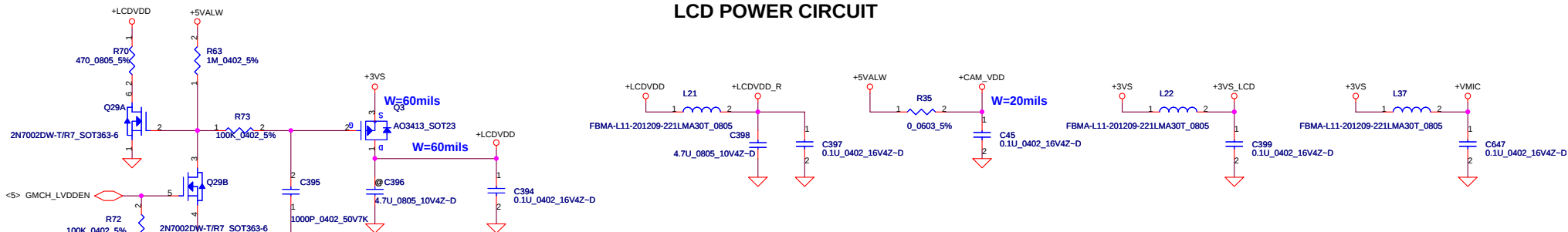
Layout Note:
Place these resistor
closely DIMM_A, all
trace length Max=1.0"



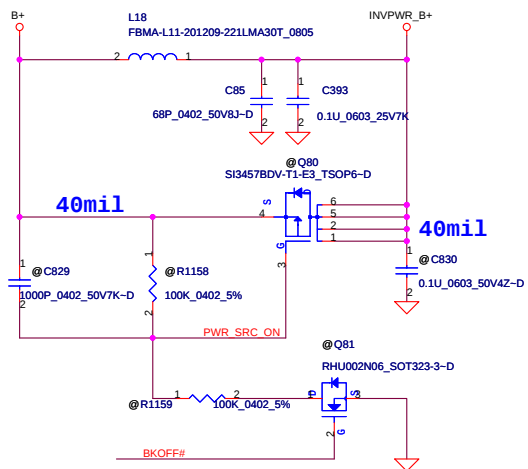
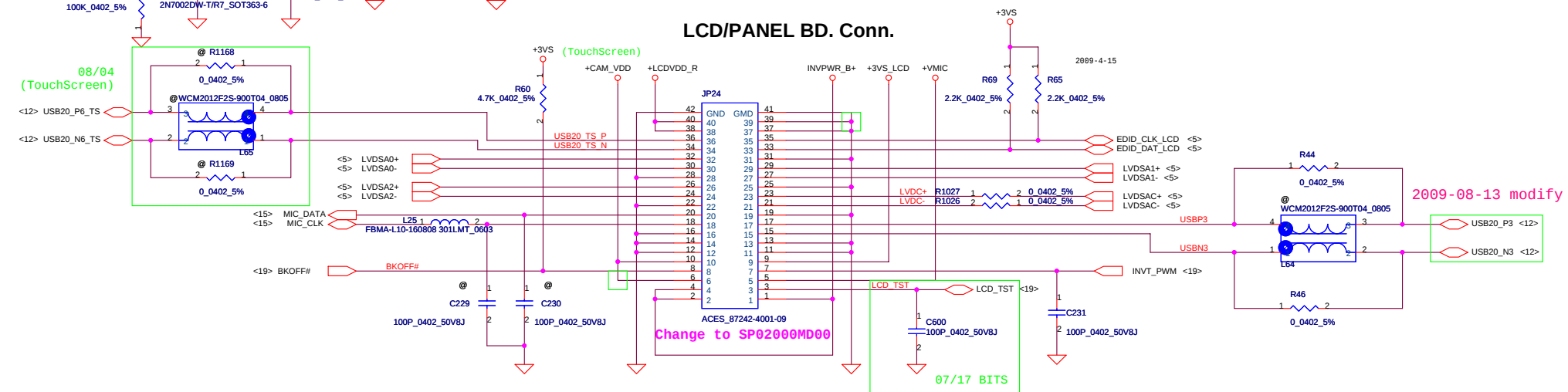
DIMM_A(REV)

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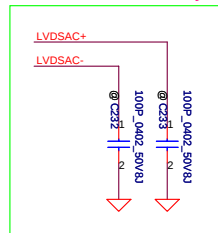
LCD POWER CIRCUIT



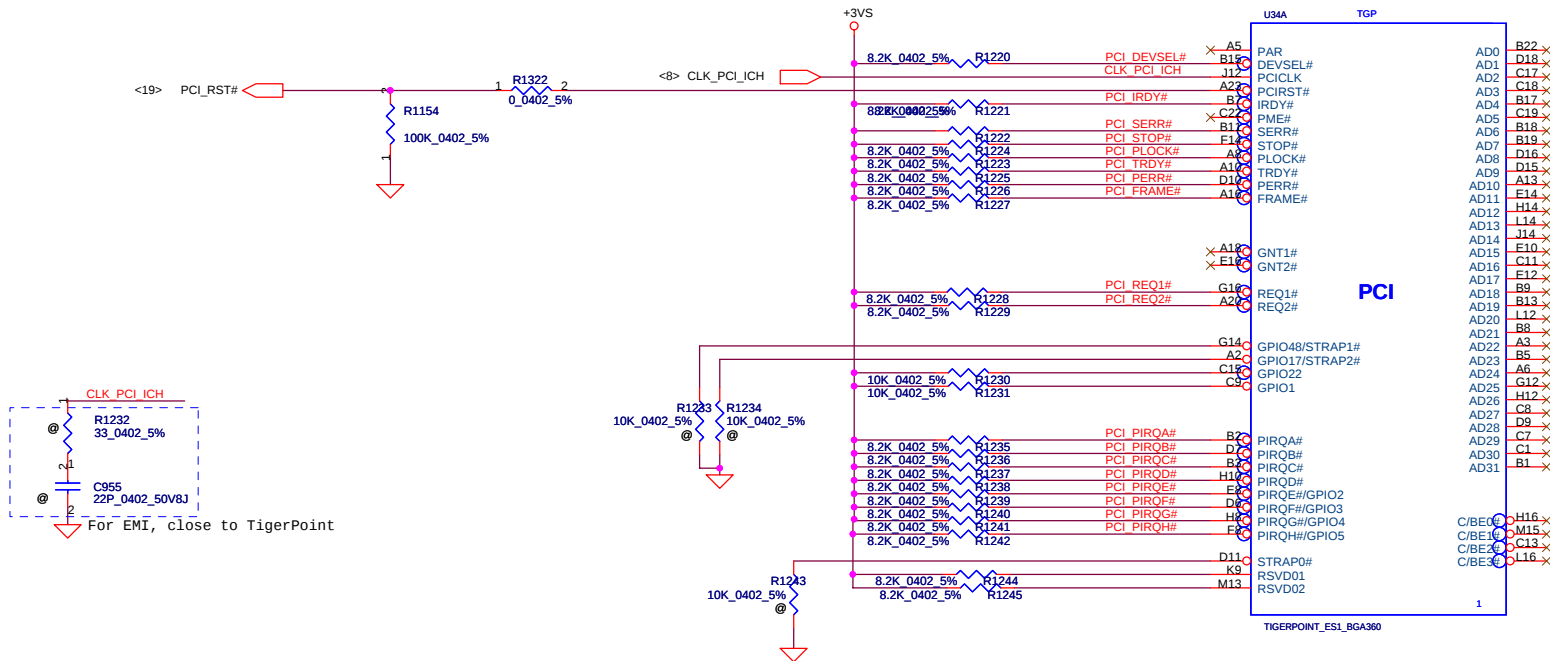
LCD/PANEL BD. Conn.

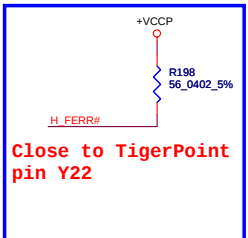
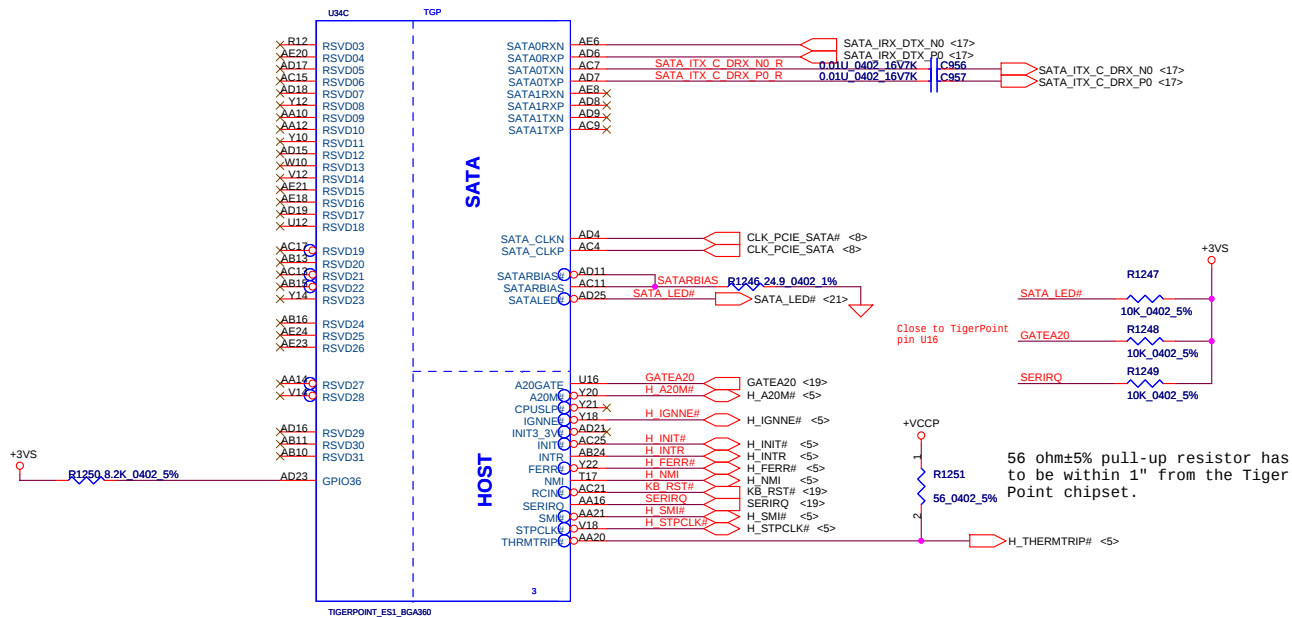


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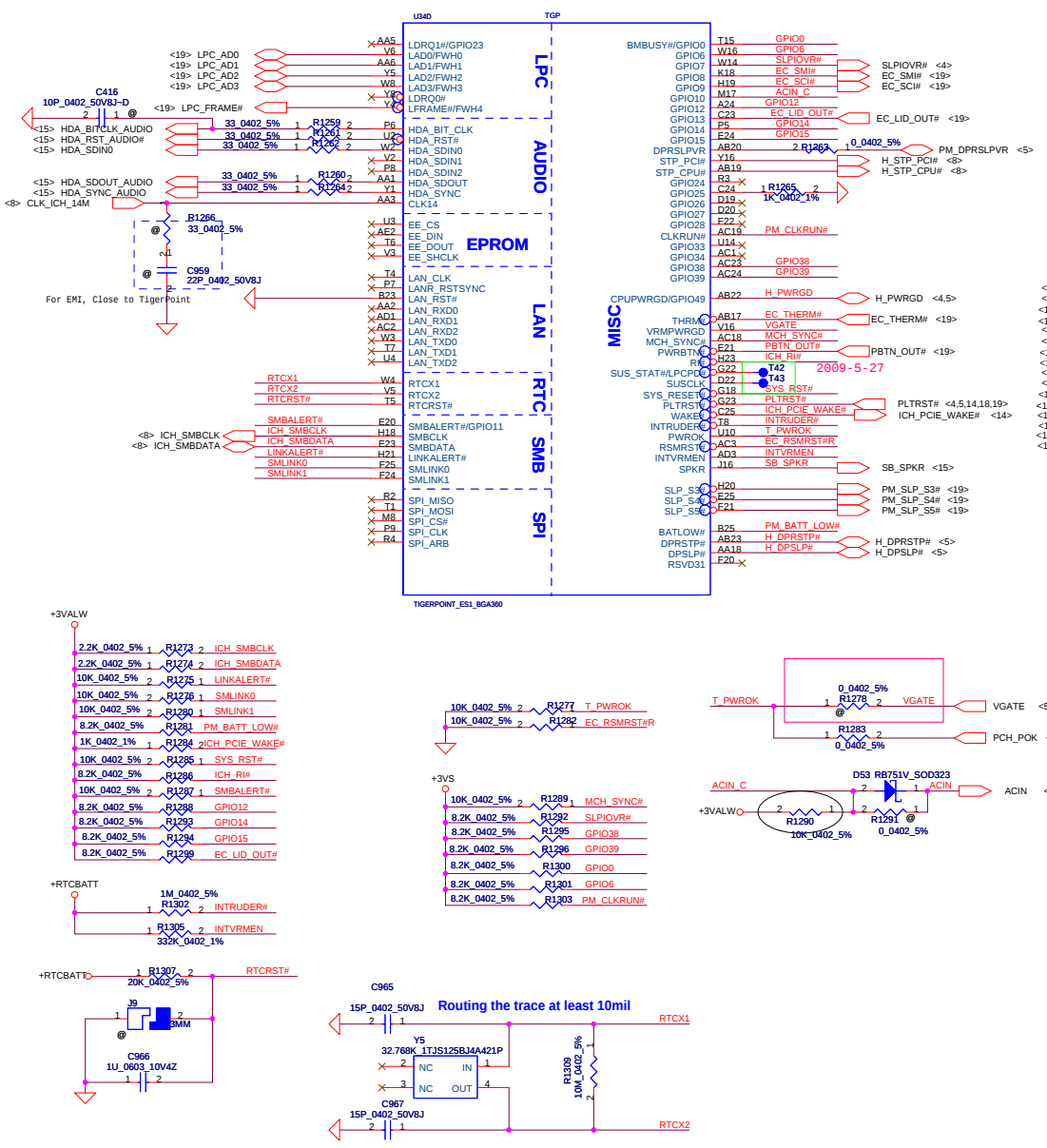


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ESD request			
H_A20M#	C450	2	100P_0402 50V8J
H_IGNNE#	C451	2	100P_0402 50V8J
H_INIT#	C452	2	100P_0402 50V8J
H_INTR	C453	2	100P_0402 50V8J
H_FERR#	C454	2	100P_0402 50V8J
H_NMI	C455	2	100P_0402 50V8J
H_SMI#	C456	2	100P_0402 50V8J
H_STPCLK#	C457	2	100P_0402 50V8J



2009-08-24 modify

2009-08-24 modify

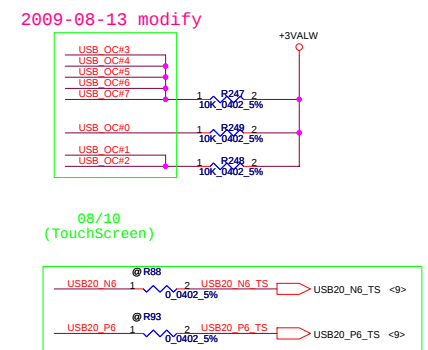
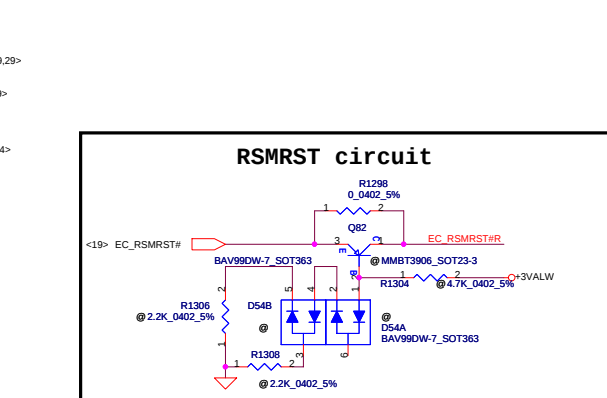
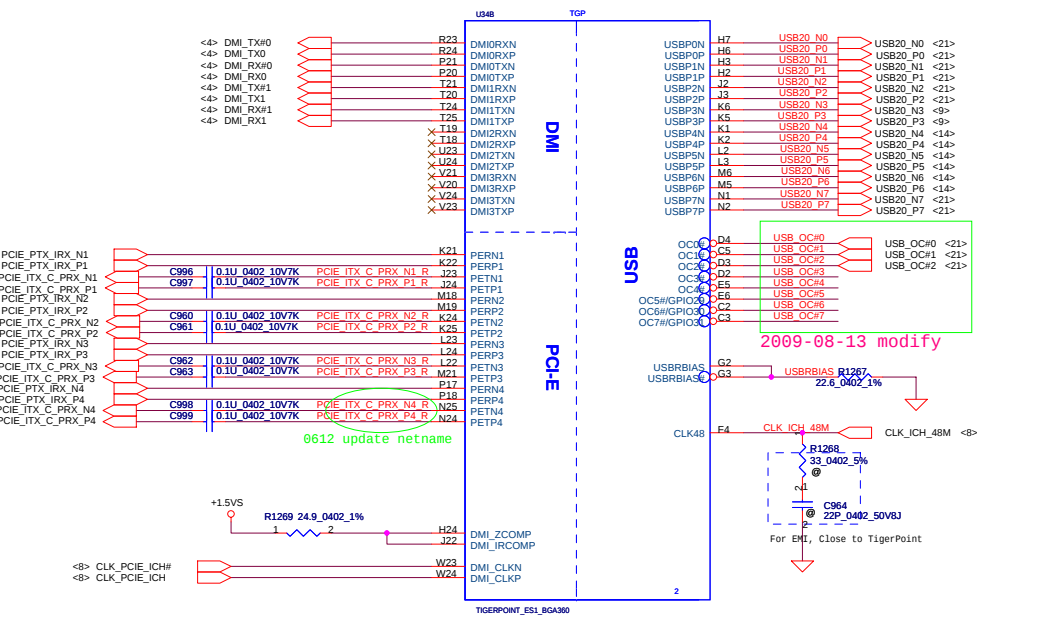
PCIE Port List	
1	LAN
2	WLAN
3	WWAN
4	Broadcom

2009-08-13 modify

2009-08-13 modify

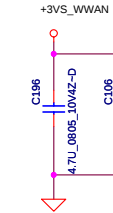
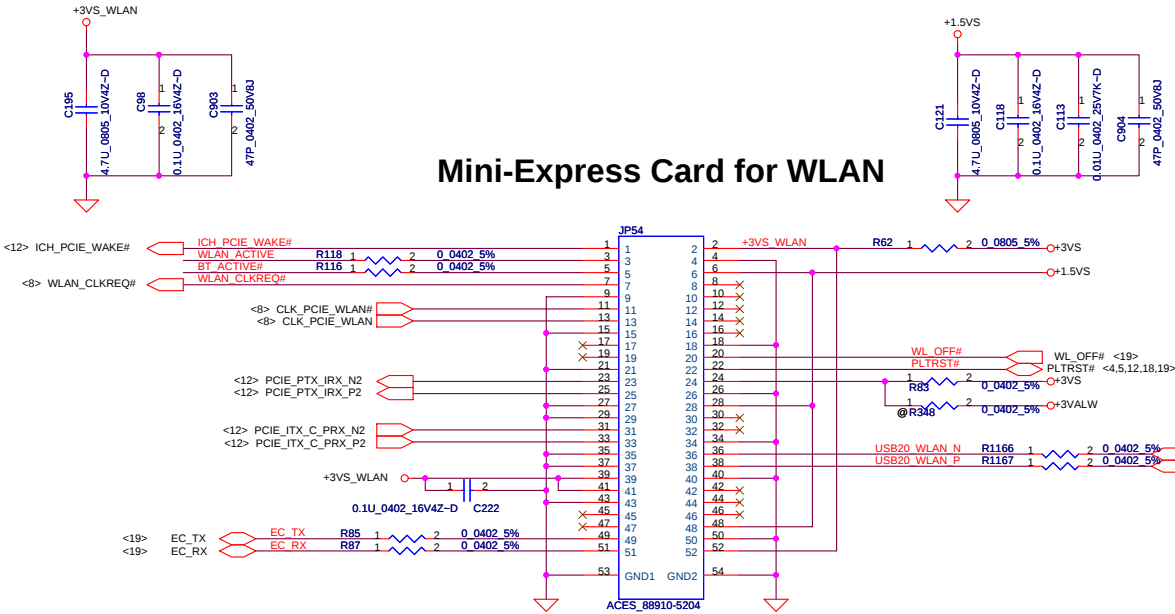
2009-08-13 modify

USB Port List	
0	USB1(Right)
1	USB2(Left)
2	USB3(Left)
3	Camera
4	WWAN
5	BT
6	WLAN
7	CardReader

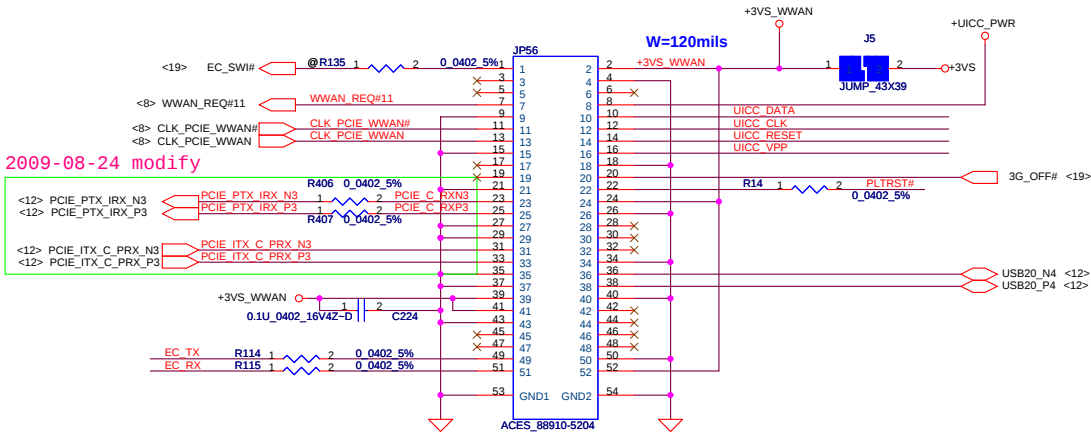


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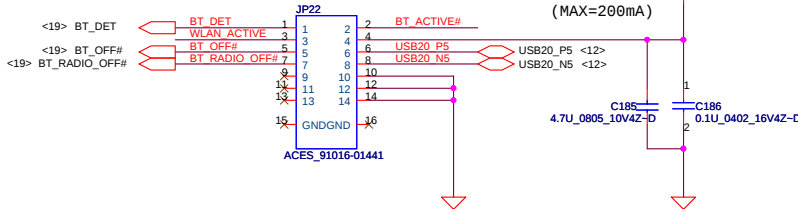
Mini-Express Card for WLAN



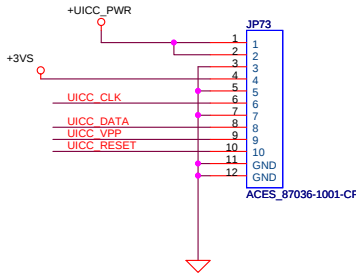
Mini-Express Card for WWAN



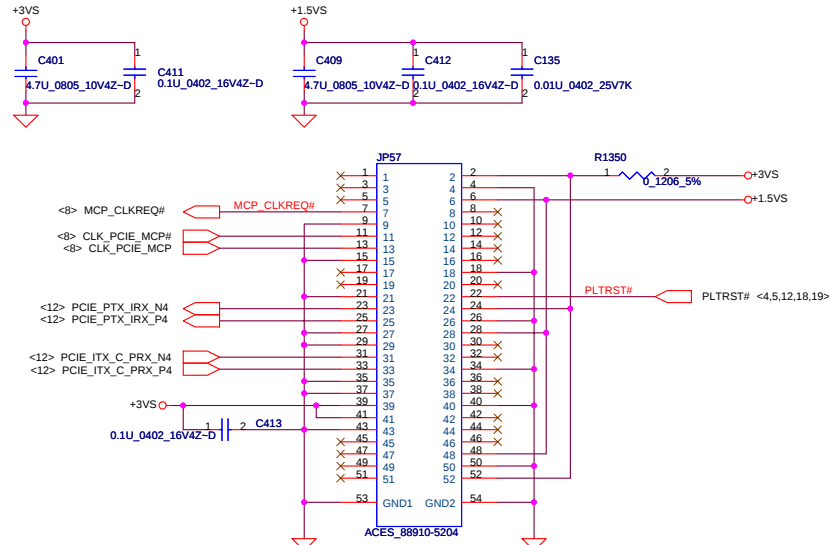
BlueTooth Interface



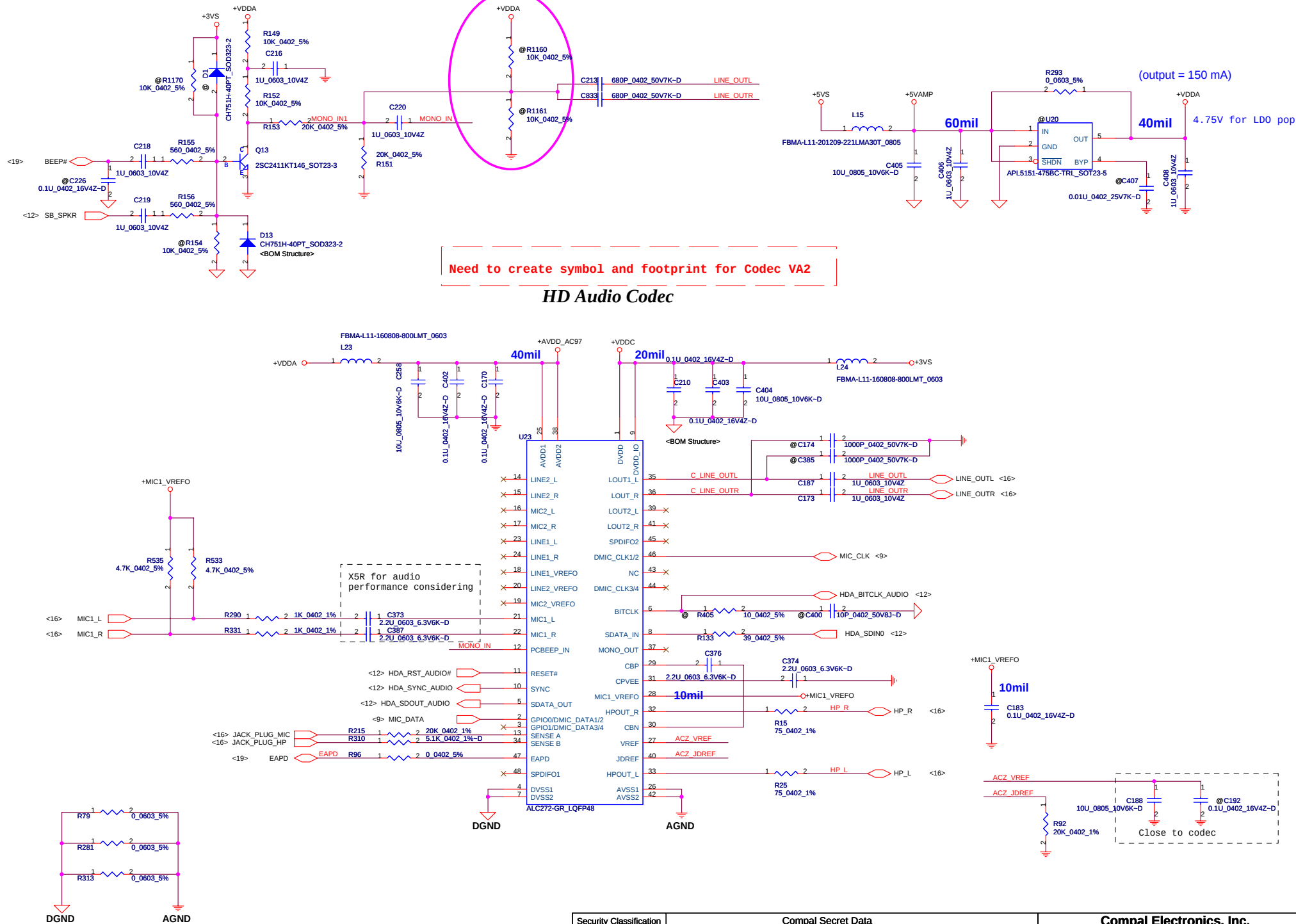
SIM Interface



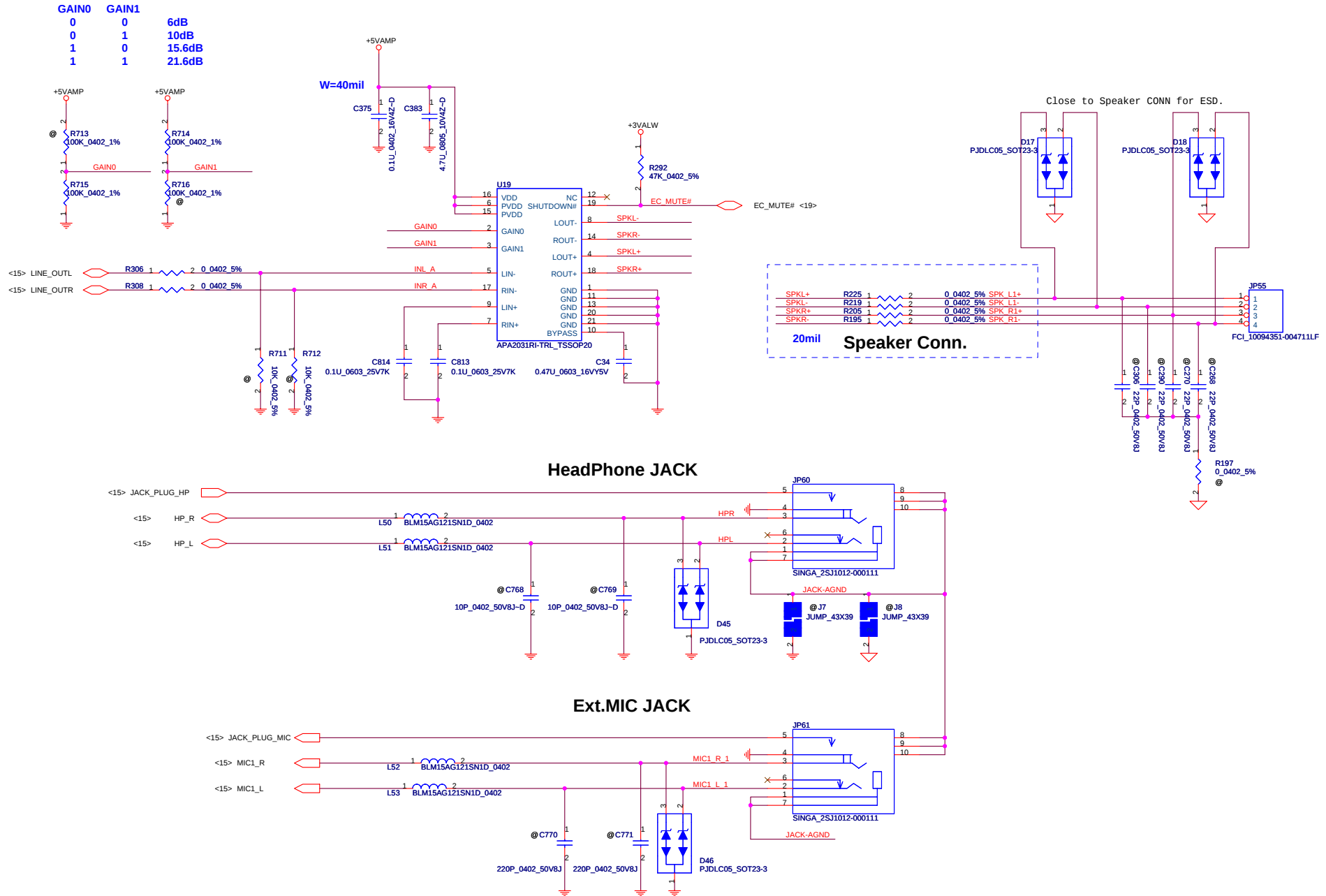
Mini-Express Card for Broadcom MCP



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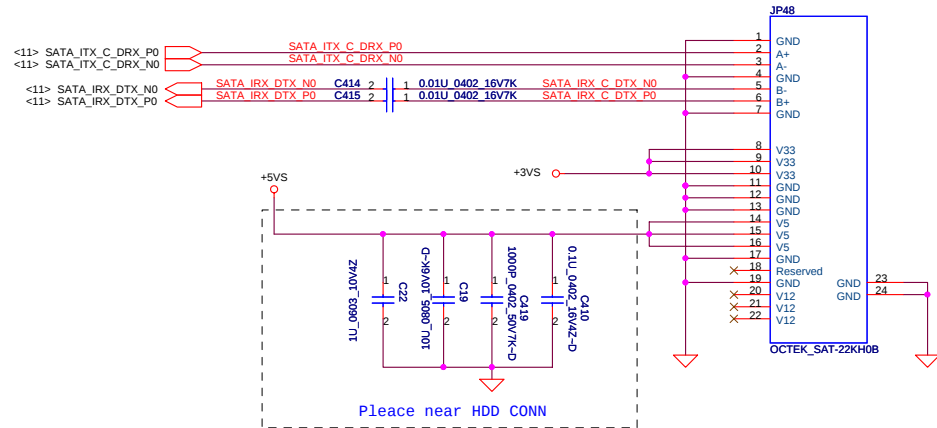


APA2031A SPK Amplifier

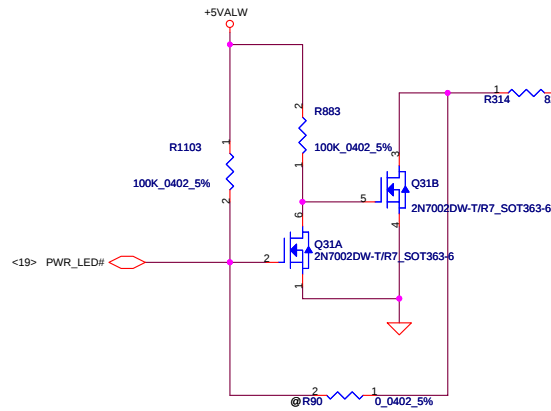


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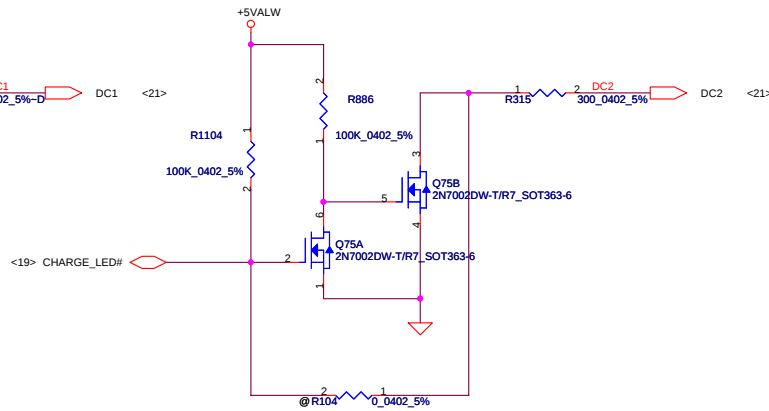
For SATA HDD



POWER LED

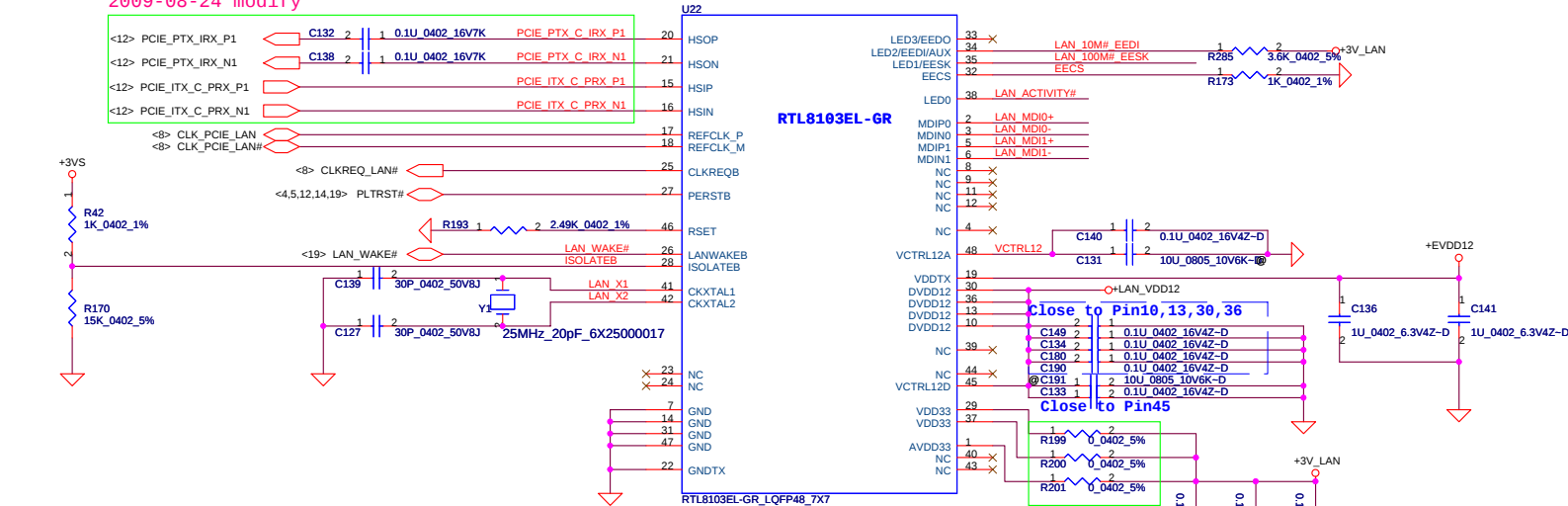


BATT CHARGE LED

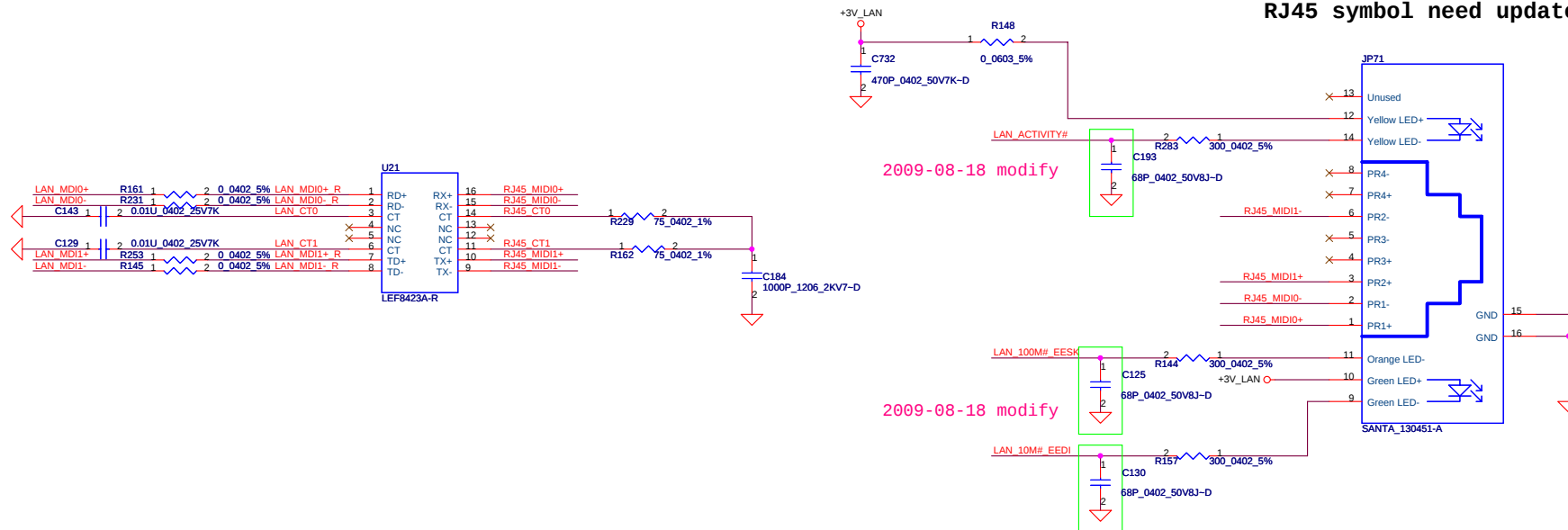


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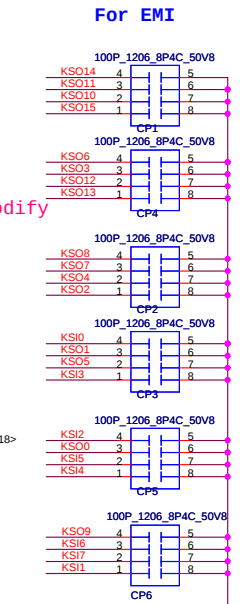
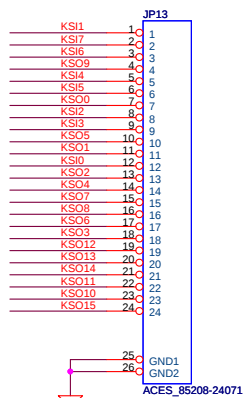
2009-08-24 modify



RJ45 symbol need update

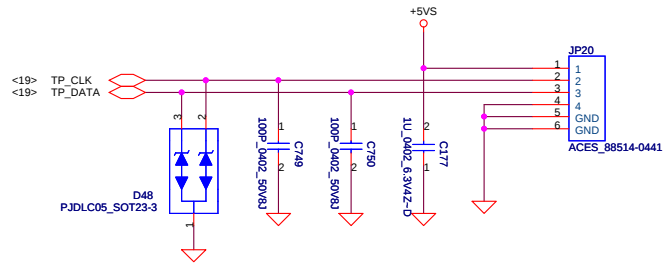


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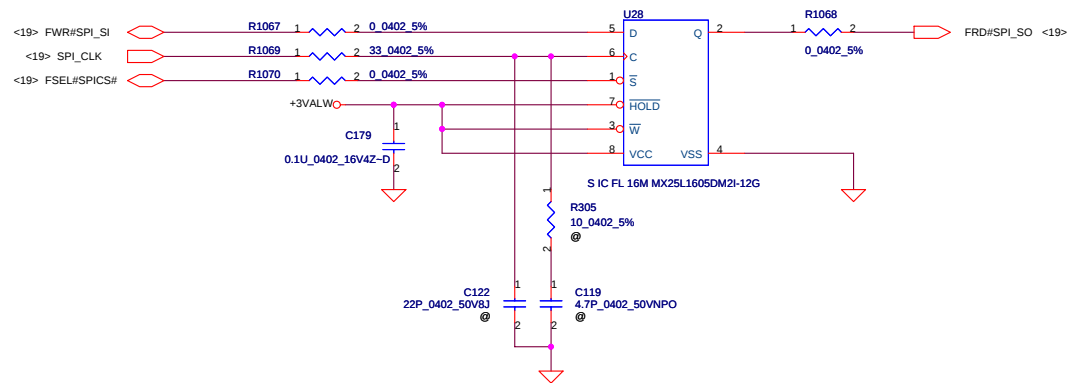
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Touch/B Connector

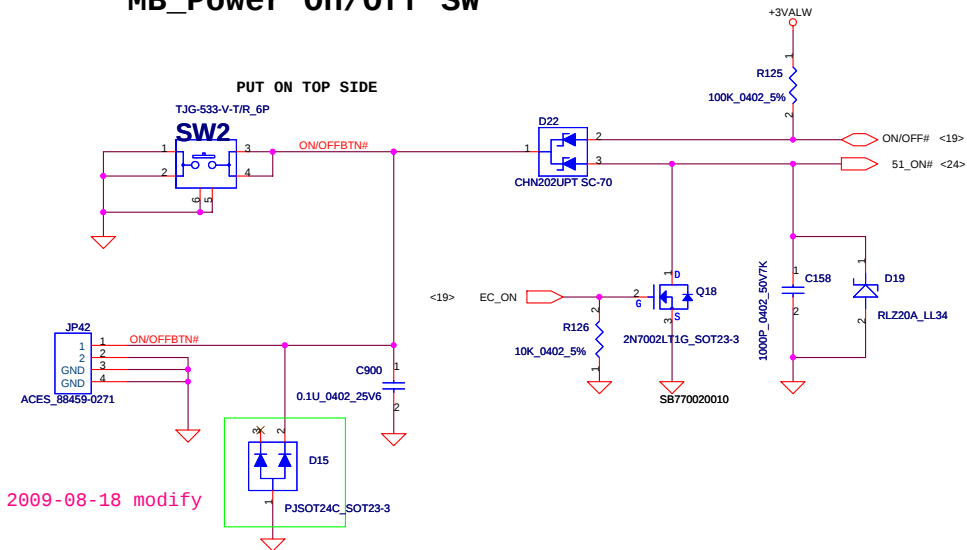


Need to create symbol and footprint for MX SPI ROM

System SPI Flash ROM (16Mb)



MB_Power On/Off SW

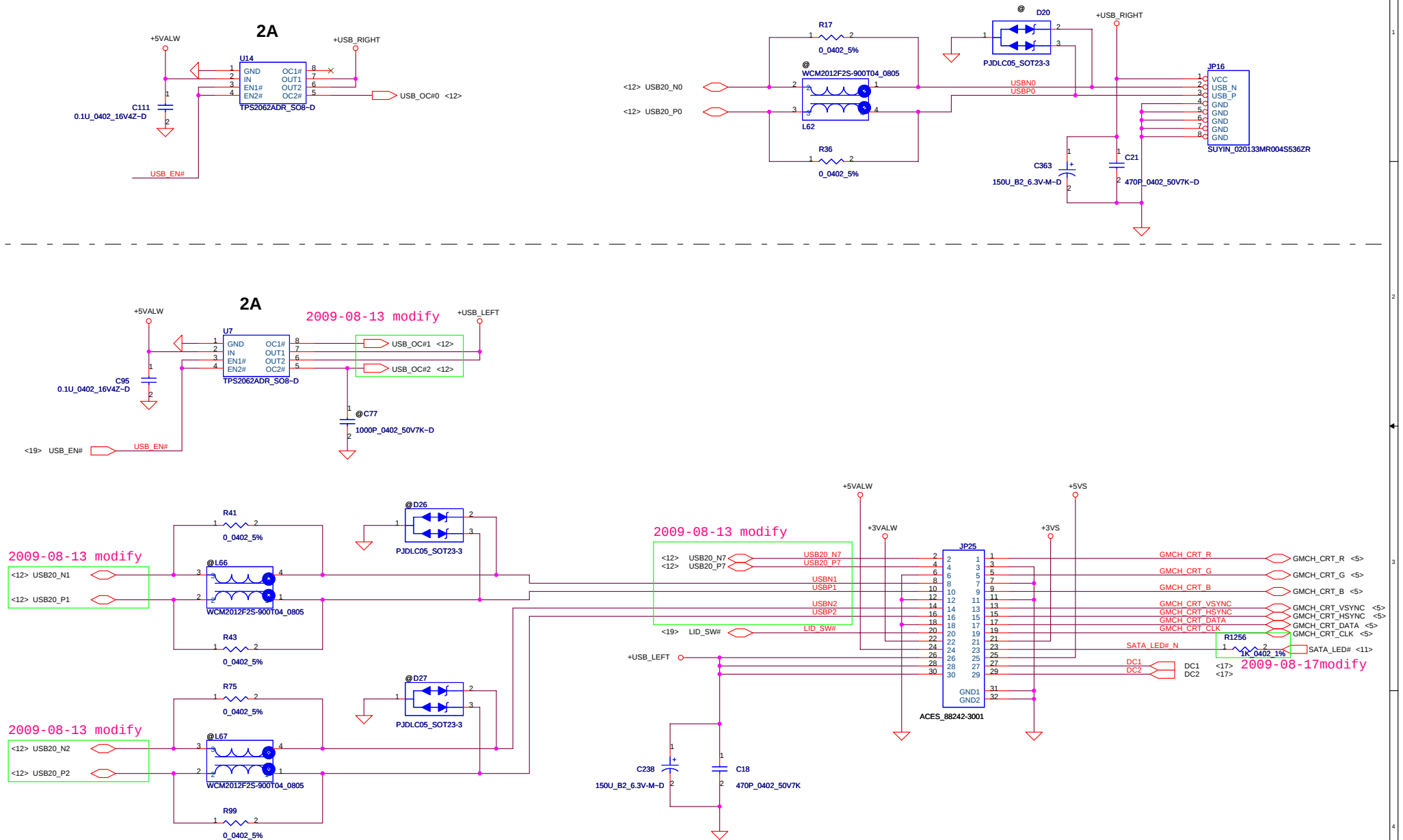


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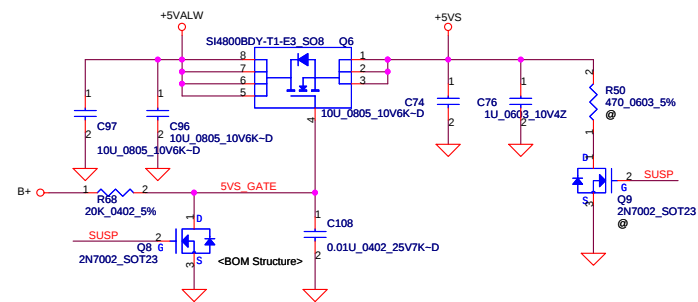
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On Board USB Connector

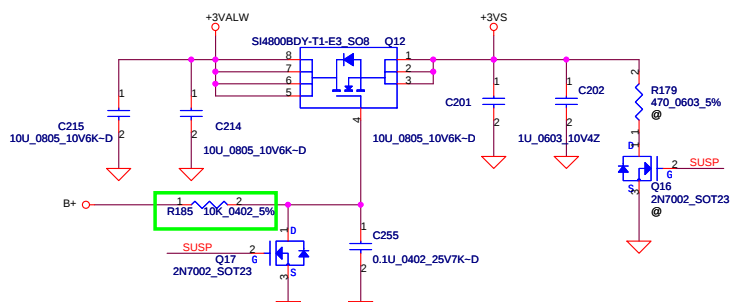


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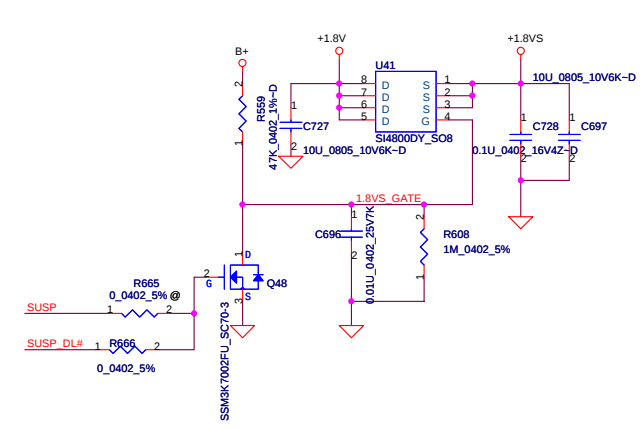
+5VALW TO +5VS



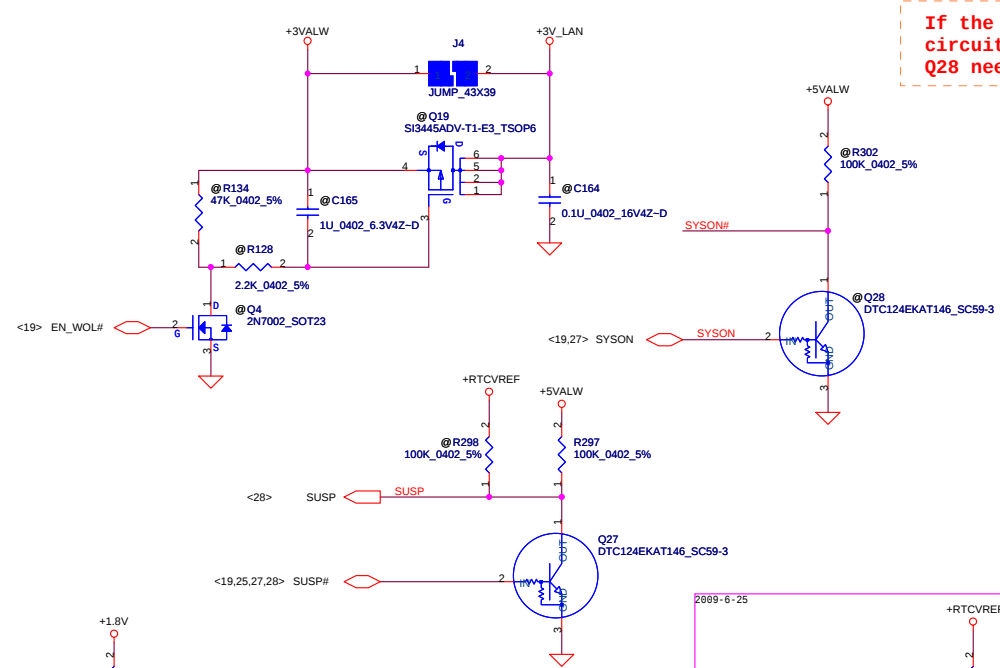
+3VALW TO +3VS



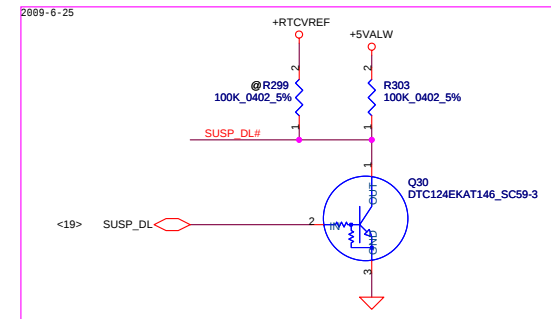
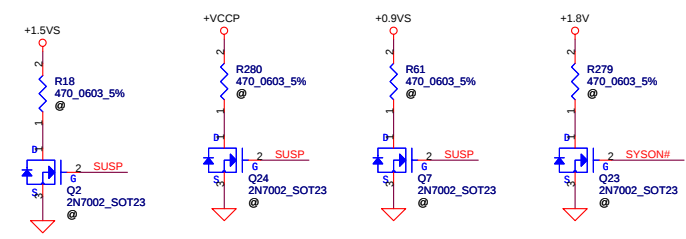
+1.8V to +1.8VS Transfer



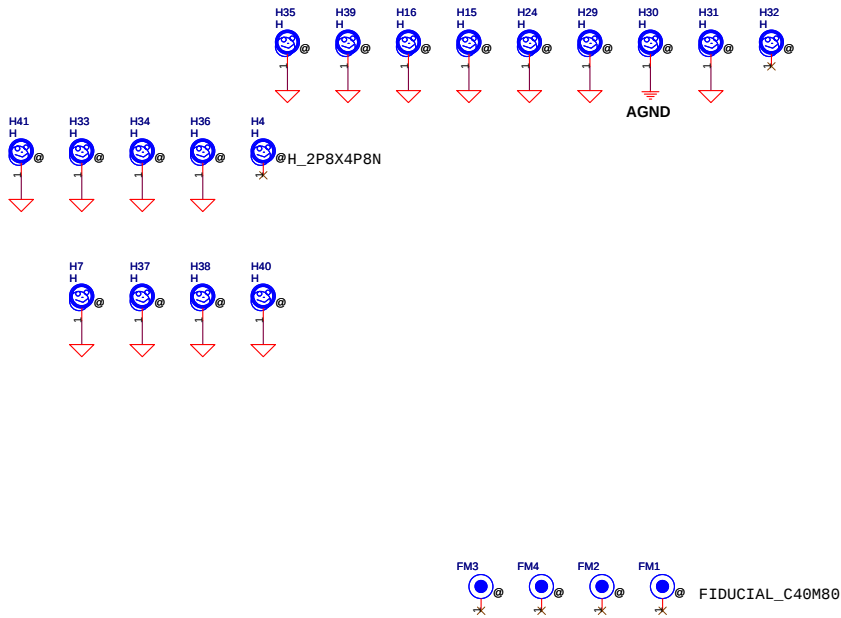
+3VALW to +3V_LAN



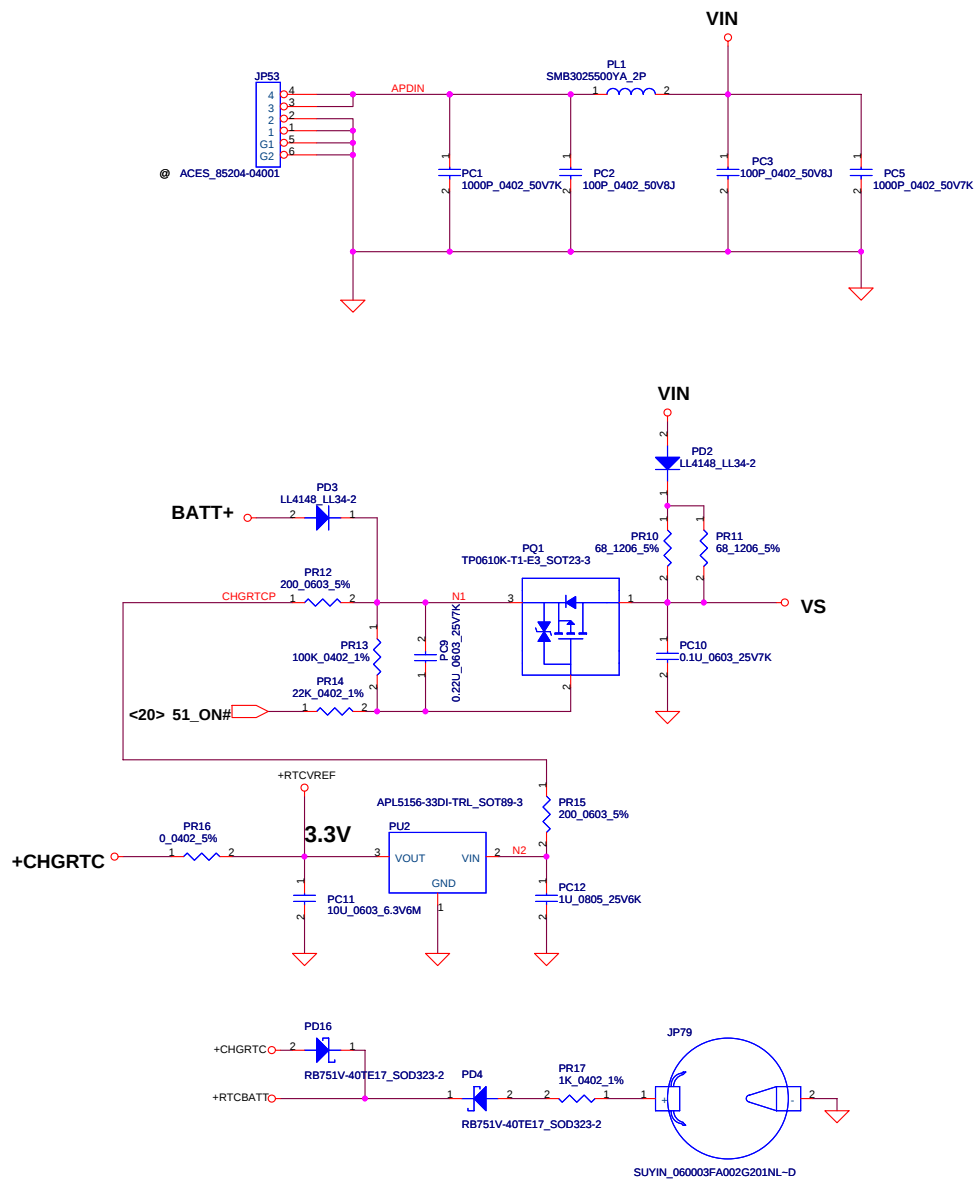
If the +1.8V discharge circuit is pop, R302, Q28 need pop.



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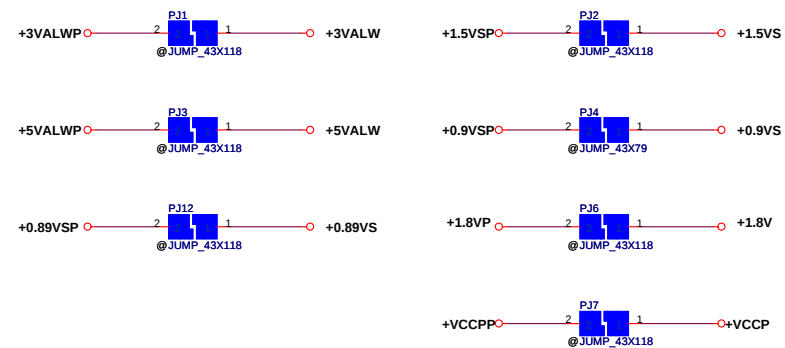
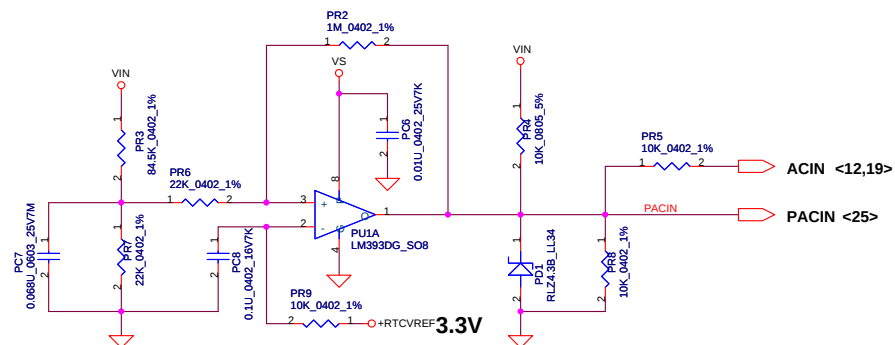


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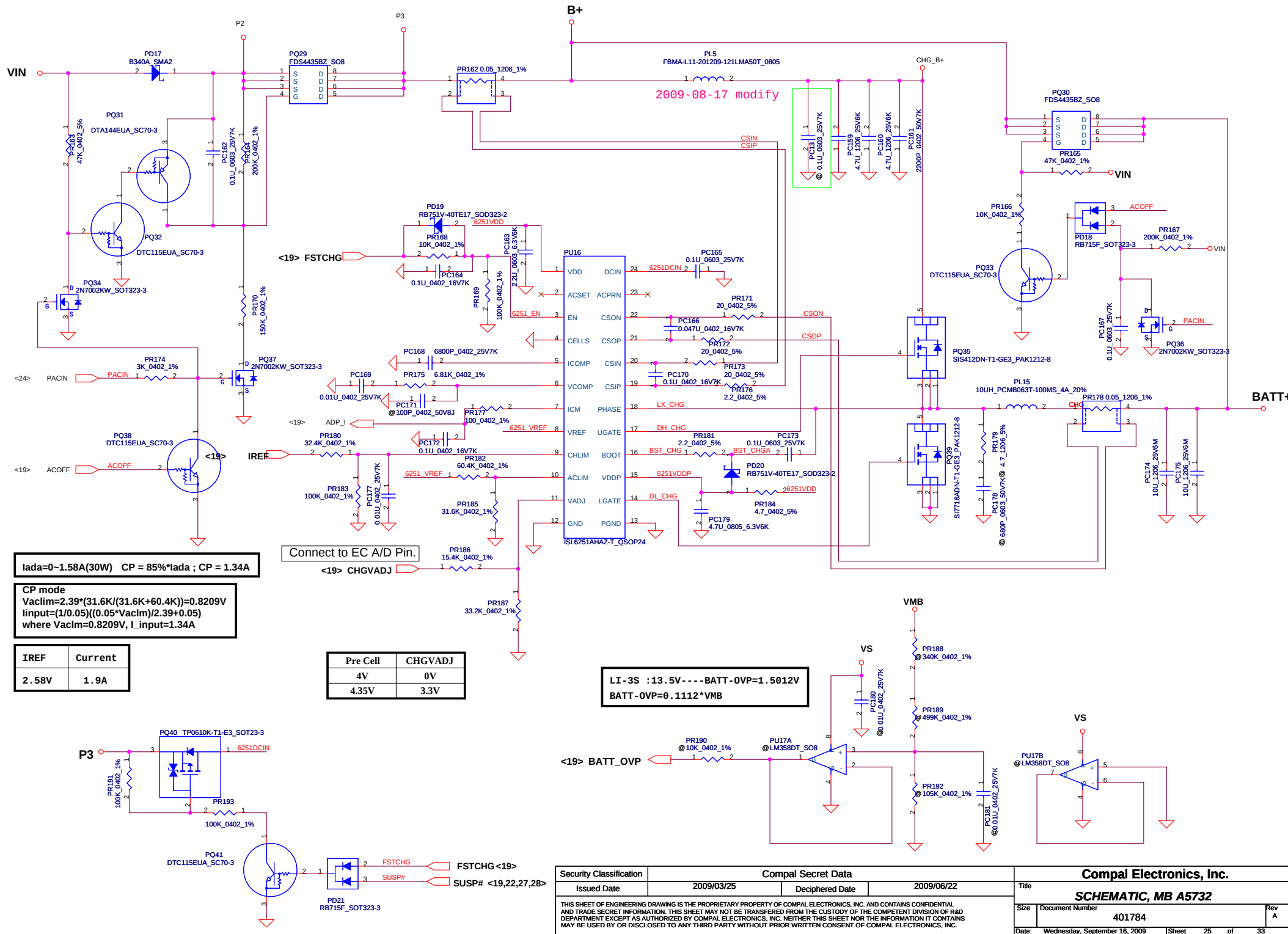


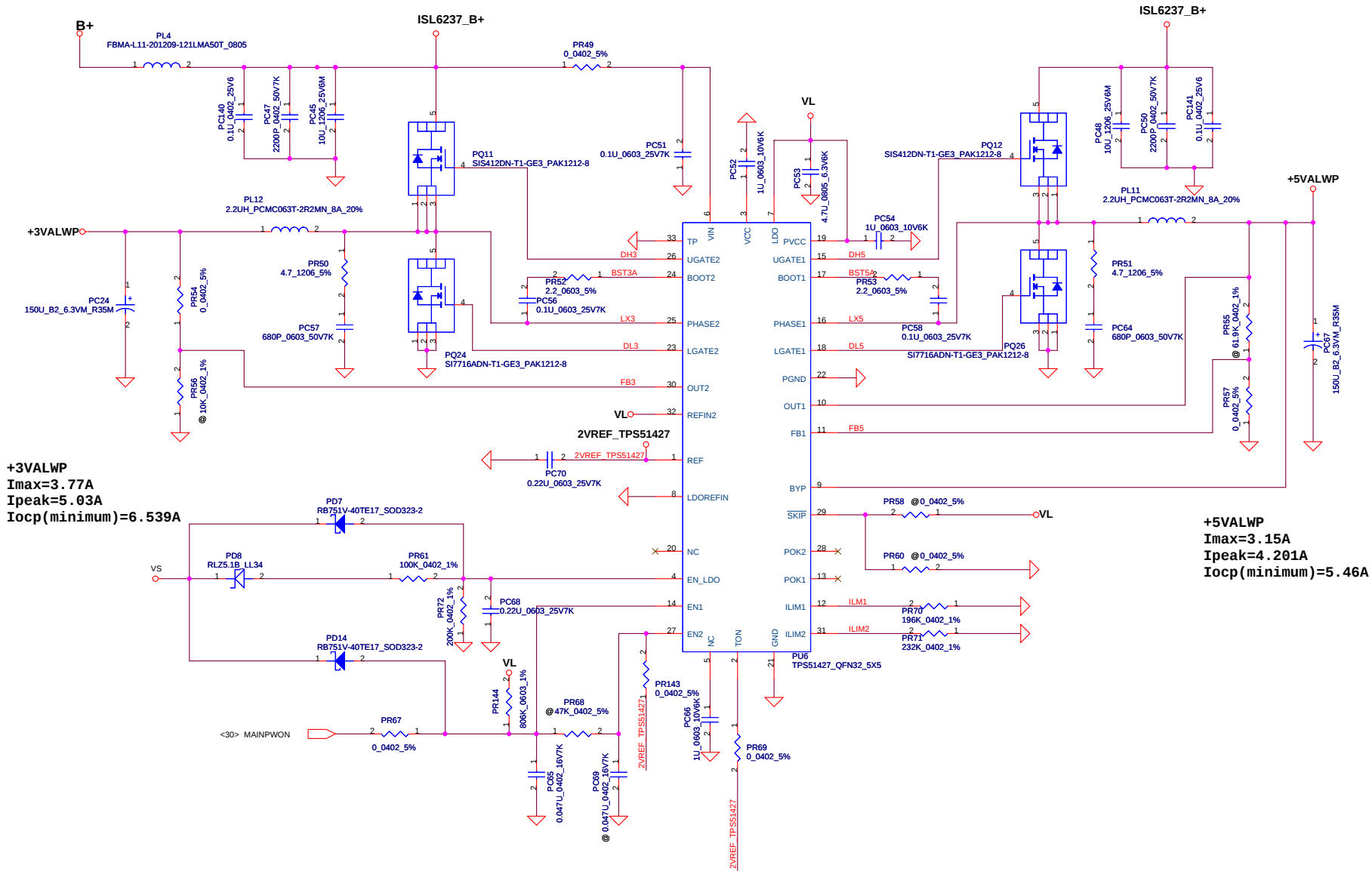
Vin Detector

High 17.944 17.706 17.470
Low 16.242 16.027 15.808

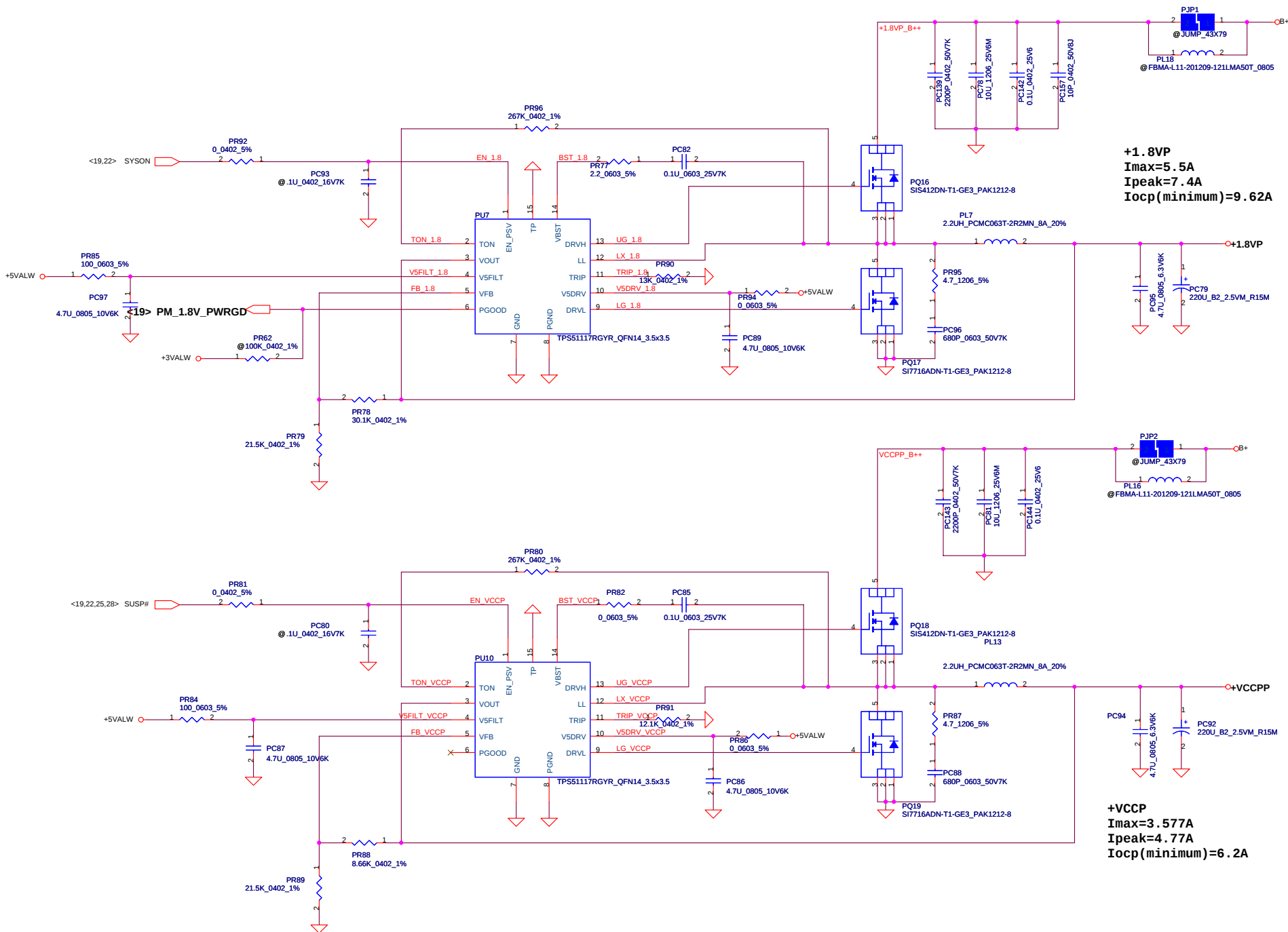


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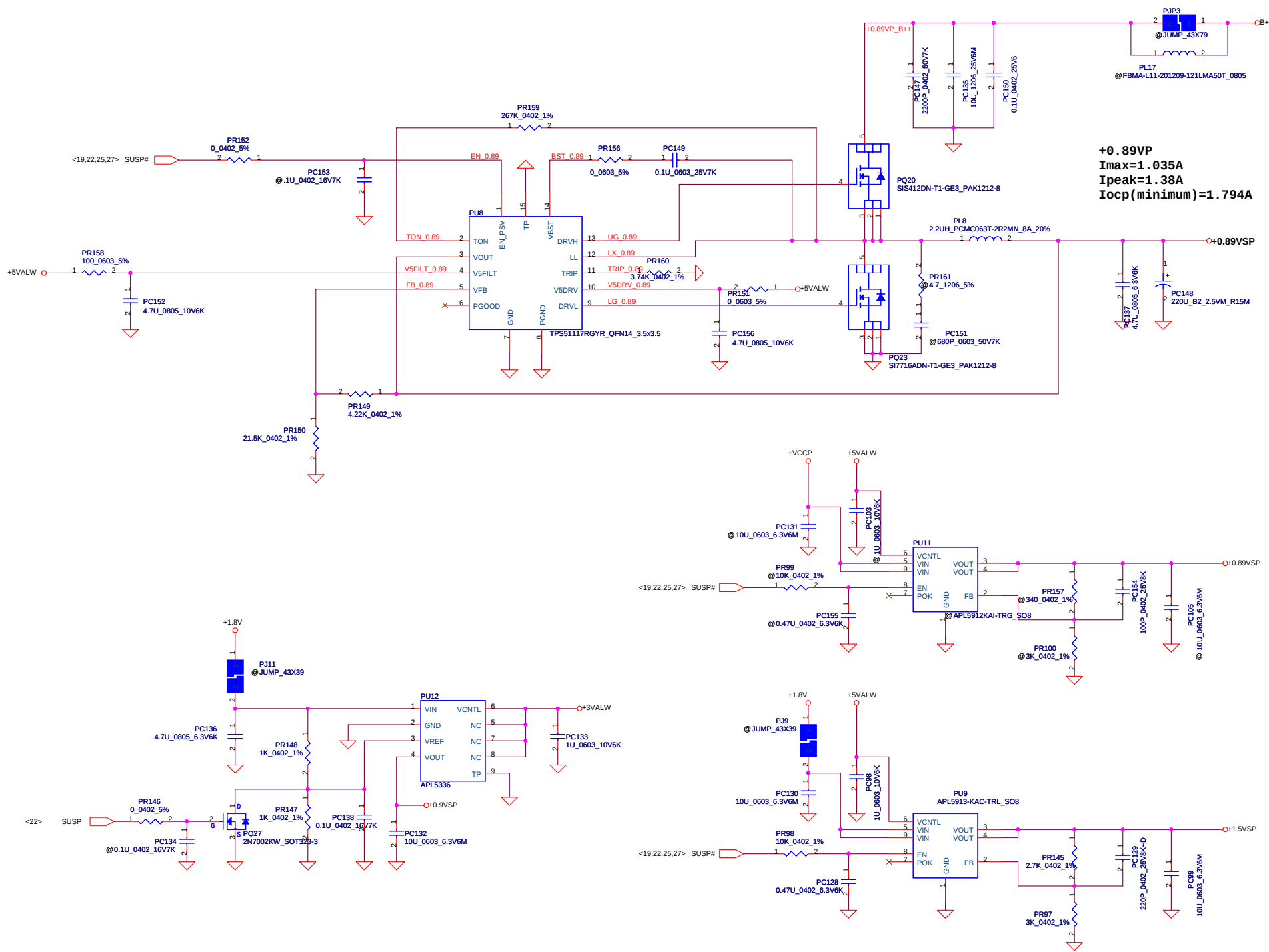




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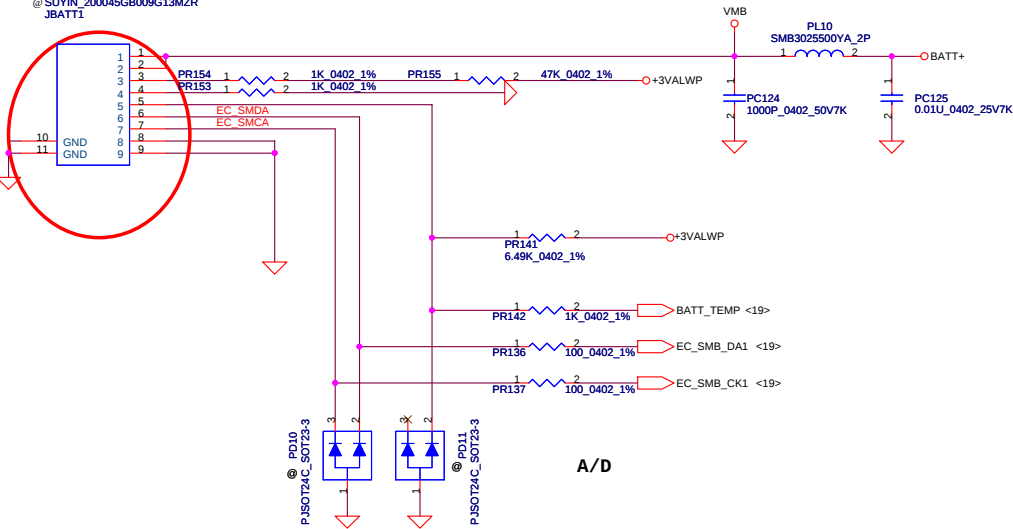


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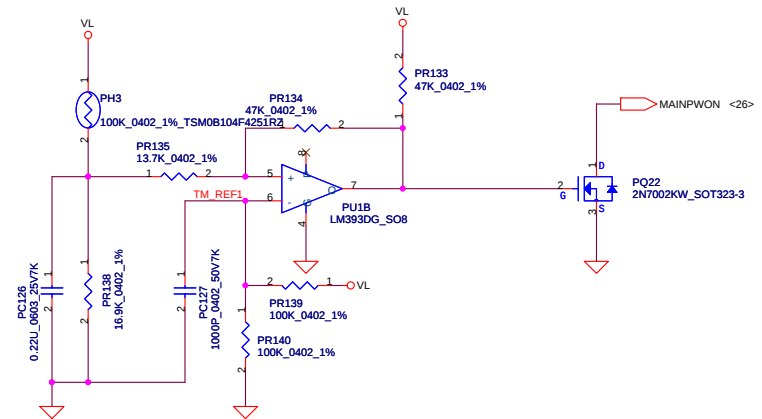


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@ SUVIN_200045GB009G13MZR
JBATT1



PH3 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C



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Version change list (P.I.R. List)

Item	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	Reserve bead to prevent noise issue happen		P27, P28	Reserve PL16, PL17, PL18	2009.07.24	PT
2	EMI request add snubber to reduce power board band.		P26, P27 P28, P29	Change PR77, PR206 to 2.2_0603_5%. Add PR87, PR95, PR50, PR51, PR115 4.7_1206_5% into BOM. Add PC88, PC96, PC57, PC64, PC109 680P_0603_50V. Add PC157 10P_0402_50V	2009.08.05	PT
3	Reserve 0.89V LDO soultion		P28	Reserve PU11, PC131, PC103, PC155, PC154, PC105 PR99, PR157, PR100	2009.08.05	PT
4	Adjust the +1.5VSP LDO feedback		P28	Change PC129 to 220P 25V K NPO 0402		
5						
6						
7						
8						
9						
10						

Version change list (P.I.R. List)

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Item	Date	Fixed Issue	Rev.	PG#	Modify List
01	2009/07/20	MEMO LIST: BOM Structure Error	0.2		Mount C170,C996,C997,C106,C196,C224,C905,R114,R115,R139,R406,R407,R185
02	2009/07/20	WWAN PLTRST#	0.2	P.14	Floating Pin17,30,32 and Mount R14 to connect PLTRST#
03	2009/07/20	Unify the quality of the capacitance	0.2	P.06	Change C56,C924,C933-22U from Y5V(SE00000868L) to X5R(SE000000I10)
04	2009/07/20	Intel MoW-WW28-glitch issue	0.2	P.08	Add R121,R124 pull-up STP_PCI# and STP_CPU# to +3.3VS
05	2009/07/20	Add LCD BIST function.	0.2	P.09/19	JP24 pin3 add LCD_TST and U27 pin16 add LCD_TST
06	2009/07/20	Add USB signal for touch screen function.	0.2	P.09	JP24-pin34,pin36 add USB signal/ pin6 connect to +5VALW and pin39 connect to GND
07	2009/07/20	Change USB connector.	0.2	P.21	Change JP16 connector.
08	2009/07/20	Change board ID to R02	0.2	P.19	Change R122 to 100K,R127 to 8.2K
09	2009/07/20	Change RJ45 LAN connector.	0.2	P.18	Change JP71 connector.
10	2009/07/20	Change BT connector.	0.2	P.14	Change JP22 connector.
11	2009/07/20	Add EC GPIO Function	0.2	P.19	Add Pin16-LCD_TST, Pin17-BT_RADIO_OFF# and Pin90-BT_DET
12	2009/07/20	For DELL Request	0.2	P.14	Pop R116, R118 for WLAN/BT co-existance control
13	2009/07/31	Change M/B to IO/B connector.	0.2	P.21	Change JP25 from 40 pin to 30 pin
14	2009/07/31	Change SIM Card connector.	0.2	P.14	Change JP73 connector.
15	2009/07/31	Add Stand off	0.2	P.23	Add H16
16	2009/08/04	Change battery connector.	0.2	P.30	Change JBATT1 connector.
17	2009/08/04	Change SATA HDD connector.	0.2	P.17	Change JP48 connector.
18	2009/08/04	Change RTC battery connector.	0.2	P.24	Change JP79 connector.
19	2009/08/04	For EMI concern circuit	0.2	P.09	Add ESD diode L65
20	2009/08/04	For EMI concern circuit	0.2	P.08	Remove RTS5159_48M; Change R137 from 22Ω to 33Ω
21	2009/08/04	Change 2P(Power board)connector.	0.2	P.20	Change JP42 connector.
22	2009/08/05	WLAN module pin define	0.2	P.14	Swap JP54.3 and JP54.5
23	2009/08/05	Change Audio Jack	0.2	P.16	Change JP60, JP61 connector.
24	2009/08/10	For TouchScreen circuit	0.2	P.12	Add R88, R93
25	2009/08/10	For Realtek Clock Generator Co-lay circuit	0.2	P.08	Add R94,R102,C182,C156; Change U3.27,U3.55,U3.72 to +1.5VM_CK505

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