Compal Confidential

QALEA/QALEB Schematics Document

AMD APU Trinity FS1r2 + FCH Hudson-M3 + GPU Seymour XTX/Thames XT

2012-01-16

REV:0.4

Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

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Title: Cover Page

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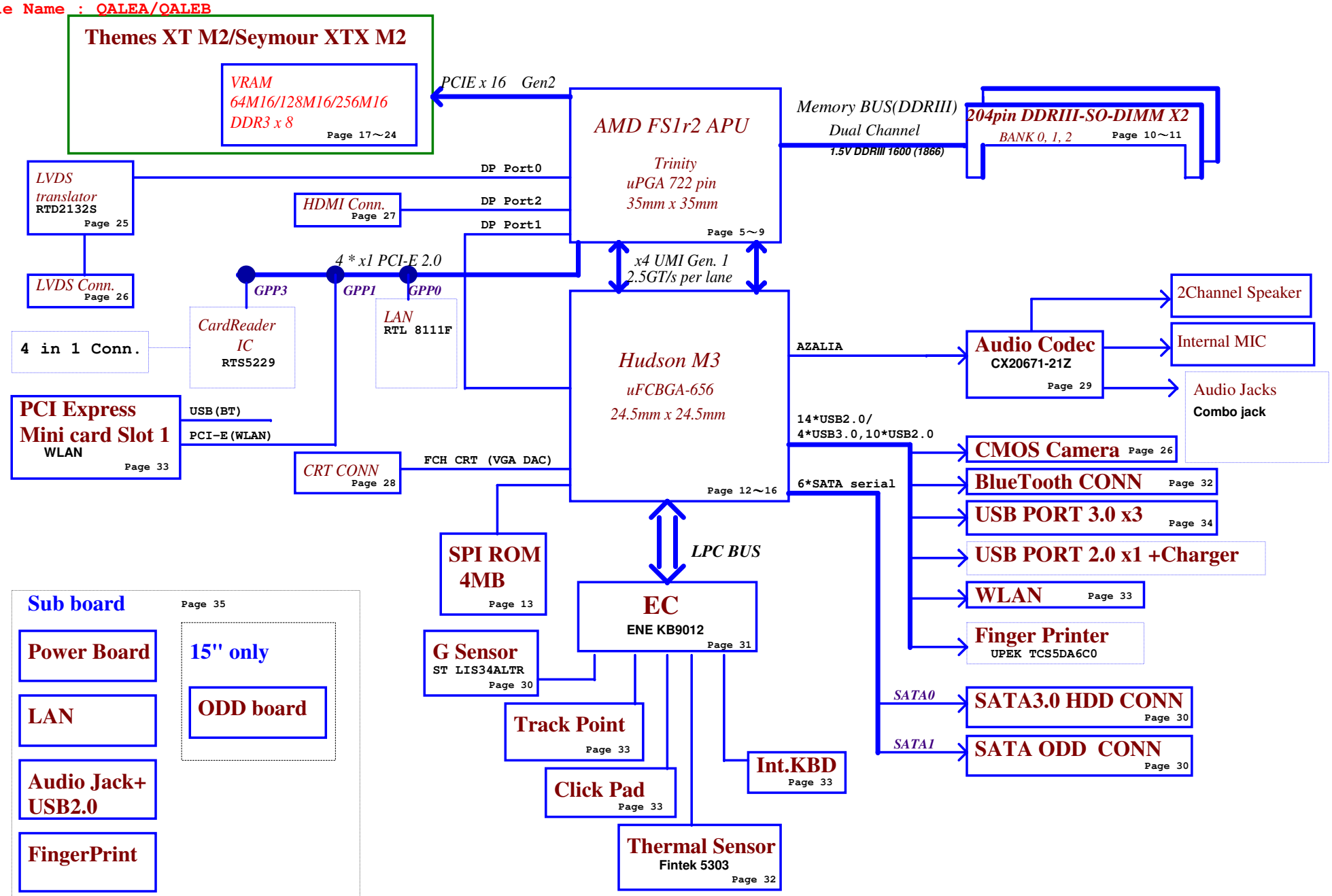
File Name : QALEA/QALEB



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Title: Block Diagrams

Size: B | Document Number: LA-8124P | Rev: 0.4

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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+1.5V	1.5V power rail for APU VDDIO and DDR	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.2VS	1.2V (VDDR, VDDP) switched power rail for APU	ON	OFF	OFF
+2.5VS	2.5V for APU VDDA	ON	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VGS	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+1.0VGS	1.0V switched power rail for VGA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS_WLAN	3.3V power rail for WLAN	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

FCH Hudson-M2/3 SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

Comal PCIE Port List

APU	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	Card Reader
FCH	PCIE0	NC
	PCIE1	NC
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M2/3 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	USB2.0 Port
Port1	NC
Port2	NC
Port3	NC
Port4	NC
Port5	WLAN
Port6	CMOS
Port7	FP
Port8	BT
Port9	NC
Port10	USB 3.0
Port11	USB 3.0
Port12	USB 3.0
Port13	NC

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001-011xb	15H

EC SM Bus2 address

Device	Address	HEX
F75303 (DDR,VRAM,CPUCORE)	1001-101xb	9AH
SB-TSI	1001-100xb	98H
Seymour XTX	1000-0010b	82H
LVDS translator		

FCH SMB0

(FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		
Security ROM		

Stencil Memo

BOM Structure

```
UMA@  : UMA only
DIS@  : DIS muxluss
PX40@ : PX4.0 Support
PX50@ : PX5.0 Support
CMOS@ : USB camera

CONN@ : ME components
X76@, H2G@, S2G@  : VRAM

Tha@:   Thames VGA
Sey@:   Seymour VGA
```

BOM option and stencil

```
SDV:
 CMOS@/DIS@/PX40@/SEY@ + X76@

PJ201,PJ401,PJ502,PJ503,PJ504,PJ601,PJ603,PJ604,
PJ701,PJ702,PJ703,PJ704,J1,J2301,J2401,J2402,J2403
PJ402,PJ403,PJ501,PJ602,PJ801,PJ802,PJ803,PJ804,PJ805
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Title: Notes List

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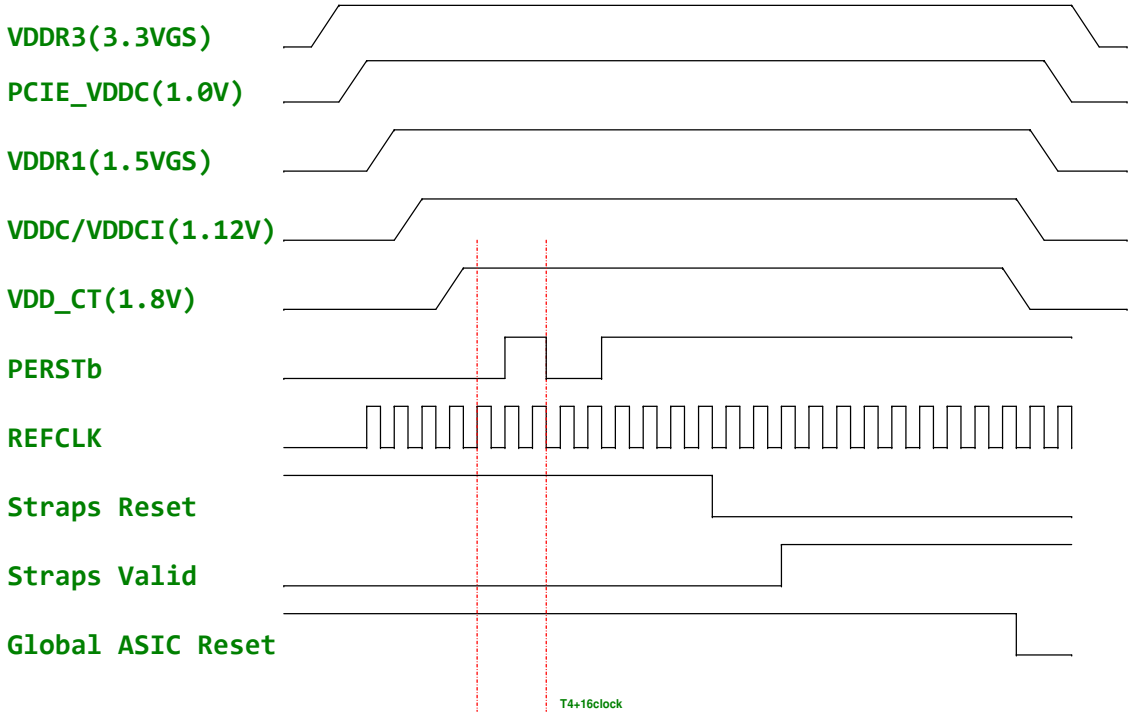
Power-Up/Down Sequence

- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



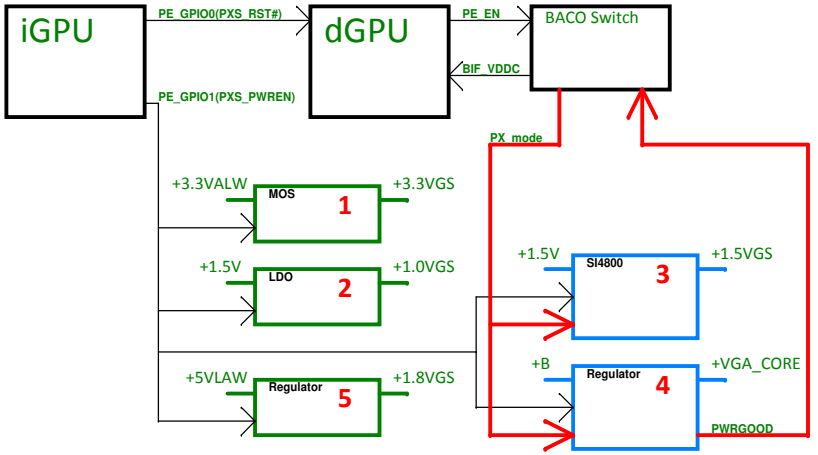
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reset on BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	775mA
PCIE_VDDC	1.0V	OFF	ON	1.1A
VDDR3	3.3V	OFF	ON	60mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	1.2A
VDDC/VDDCI	TBD	OFF	OFF	28



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Title: dGPU Block Diagram

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17 PCIE_CRX_GTX_P[0..15]
17 PCIE_CRX_GTX_N[0..15]

PCIE_CTX_GRX_P[0..15] 17
PCIE_CTX_GRX_N[0..15] 17

JCPU1A

PCI EXPRESS

GRAPHICS

PCIE_CRX_GTX_P0	AB8	P_GFX_RXP0	P_GFX_TXP0	AB2	PCIE_CTX_C_GRX_P0	C1	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P0
PCIE_CRX_GTX_N0	AB7	P_GFX_RXN0	P_GFX_TXN0	AB1	PCIE_CTX_C_GRX_N0	C2	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N0
PCIE_CRX_GTX_P1	AA9	P_GFX_RXP1	P_GFX_TXP1	AA3	PCIE_CTX_C_GRX_P1	C3	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P1
PCIE_CRX_GTX_N1	AA8	P_GFX_RXN1	P_GFX_TXN1	AA2	PCIE_CTX_C_GRX_N1	C4	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N1
PCIE_CRX_GTX_P2	AA5	P_GFX_RXP2	P_GFX_TXP2	Y5	PCIE_CTX_C_GRX_P2	C5	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P2
PCIE_CRX_GTX_N2	AA6	P_GFX_RXN2	P_GFX_TXN2	Y4	PCIE_CTX_C_GRX_N2	C6	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N2
PCIE_CRX_GTX_P3	Y8	P_GFX_RXP3	P_GFX_TXP3	Y2	PCIE_CTX_C_GRX_P3	C7	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P3
PCIE_CRX_GTX_N3	Y7	P_GFX_RXN3	P_GFX_TXN3	Y1	PCIE_CTX_C_GRX_N3	C8	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N3
PCIE_CRX_GTX_P4	W9	P_GFX_RXP4	P_GFX_TXP4	W3	PCIE_CTX_C_GRX_P4	C9	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P4
PCIE_CRX_GTX_N4	W8	P_GFX_RXN4	P_GFX_TXN4	W2	PCIE_CTX_C_GRX_N4	C10	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N4
PCIE_CRX_GTX_P5	W5	P_GFX_RXP5	P_GFX_TXP5	V5	PCIE_CTX_C_GRX_P5	C11	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P5
PCIE_CRX_GTX_N5	W6	P_GFX_RXN5	P_GFX_TXN5	V4	PCIE_CTX_C_GRX_N5	C12	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N5
PCIE_CRX_GTX_P6	V8	P_GFX_RXP6	P_GFX_TXP6	V2	PCIE_CTX_C_GRX_P6	C13	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P6
PCIE_CRX_GTX_N6	V7	P_GFX_RXN6	P_GFX_TXN6	V1	PCIE_CTX_C_GRX_N6	C14	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N6
PCIE_CRX_GTX_P7	U9	P_GFX_RXP7	P_GFX_TXP7	U3	PCIE_CTX_C_GRX_P7	C15	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P7
PCIE_CRX_GTX_N7	U8	P_GFX_RXN7	P_GFX_TXN7	U2	PCIE_CTX_C_GRX_N7	C16	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N7
PCIE_CRX_GTX_P8	U5	P_GFX_RXP8	P_GFX_TXP8	T5	PCIE_CTX_C_GRX_P8	C17	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P8
PCIE_CRX_GTX_N8	U6	P_GFX_RXN8	P_GFX_TXN8	T4	PCIE_CTX_C_GRX_N8	C18	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N8
PCIE_CRX_GTX_P9	T8	P_GFX_RXP9	P_GFX_TXP9	T2	PCIE_CTX_C_GRX_P9	C19	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P9
PCIE_CRX_GTX_N9	T7	P_GFX_RXN9	P_GFX_TXN9	T1	PCIE_CTX_C_GRX_N9	C20	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N9
PCIE_CRX_GTX_P10	R9	P_GFX_RXP10	P_GFX_TXP10	R3	PCIE_CTX_C_GRX_P10	C21	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P10
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PCIE_CRX_GTX_N11	R6	P_GFX_RXN11	P_GFX_TXN11	P4	PCIE_CTX_C_GRX_N11	C24	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N11
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PCIE_CRX_GTX_N12	P7	P_GFX_RXN12	P_GFX_TXN12	P1	PCIE_CTX_C_GRX_N12	C26	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N12
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PCIE_CRX_GTX_N14	N6	P_GFX_RXN14	P_GFX_TXN14	M4	PCIE_CTX_C_GRX_N14	C30	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N14
PCIE_CRX_GTX_P15	M8	P_GFX_RXP15	P_GFX_TXP15	M2	PCIE_CTX_C_GRX_P15	C31	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_P15
PCIE_CRX_GTX_N15	M7	P_GFX_RXN15	P_GFX_TXN15	M1	PCIE_CTX_C_GRX_N15	C32	DIS@	1	2	.1U_0402_16V7K	PCIE_CTX_GRX_N15

GPP

	AE5	P_GPP_RXP0	P_GPP_TXP0	AD5	PCIE_CTX_C_DRX_P0	C33	1		2	.1U_0402_16V7K	PCIE_CTX_DRX_P0 35
LAN 35 PCIE_CRX_DTX_P0	AE6	P_GPP_RXN0	P_GPP_TXN0	AD4	PCIE_CTX_C_DRX_N0	C34	1		2	.1U_0402_16V7K	PCIE_CTX_DRX_N0 35
WLAN 35 PCIE_CRX_DTX_N0	AD8	P_GPP_RXP1	P_GPP_TXP1	AD2	PCIE_CTX_C_DRX_P1	C123	1		2	.1U_0402_16V7K	PCIE_CTX_DRX_P1 33
33 PCIE_CRX_DTX_P1	AD7	P_GPP_RXN1	P_GPP_TXN1	AD1	PCIE_CTX_C_DRX_N1	C124	1		2	.1U_0402_16V7K	PCIE_CTX_DRX_N1 33
33 PCIE_CRX_DTX_N1	AC3										
	AC4	P_GPP_RXP2	P_GPP_TXP2	AC2							
35 PCIE_CRX_DTX_P3	AC5	P_GPP_RXN2	P_GPP_TXN2	AB5	PCIE_CTX_C_DRX_P3	C35	1		2	.1U_0402_16V7K	PCIE_CTX_DRX_P3 35
Card Reader 35 PCIE_CRX_DTX_N3	AC6	P_GPP_RXP3	P_GPP_TXP3	AB4	PCIE_CTX_C_DRX_N3	C36	1		2	.1U_0402_16V7K	PCIE_CTX_DRX_N3 35
	AG8	P_GPP_RXN3	P_GPP_TXN3	AG2	UMI_TXP0_C	C37	1		2	.1U_0402_16V7K	UMI_TXP0 12
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12 UMI_RXP1	AG5	P_UMI_RXP1	P_UMI_TXP1	AF5	UMI_TXN1_C	C40	1		2	.1U_0402_16V7K	UMI_TXN1 12
12 UMI_RXN1	AF7	P_UMI_RXN1	P_UMI_TXN1	AF1	UMI_TXP2_C	C41	1		2	.1U_0402_16V7K	UMI_TXP2 12
12 UMI_RXP2	AF8	P_UMI_RXP2	P_UMI_TXP2	AF2	UMI_TXN2_C	C42	1		2	.1U_0402_16V7K	UMI_TXN2 12
12 UMI_RXN2	AE8	P_UMI_RXN2	P_UMI_TXN2	AE2	UMI_TXP3_C	C43	1		2	.1U_0402_16V7K	UMI_TXP3 12
12 UMI_RXP3	AE9	P_UMI_RXP3	P_UMI_TXP3	AE3	UMI_TXN3_C	C44	1		2	.1U_0402_16V7K	UMI_TXN3 12
12 UMI_RXN3		P_UMI_RXN3	P_UMI_TXN3								

UMI

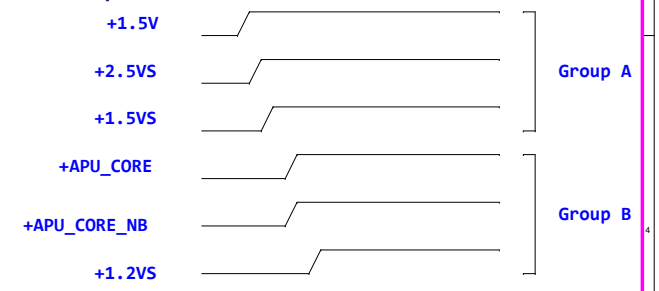
+1.2VS 1 R1 2 P_ZVDDP AG11 — 196_0402_1%

P_ZVDDP

P_ZVSS AH11 P_ZVSS 1 R2 2 — 196_0402_1%

LOTES_ACA-ZIF-109-P12-A_FS1R2
CONN@

Power Sequence of APU



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Title: FS1r2 PCIE/UMI

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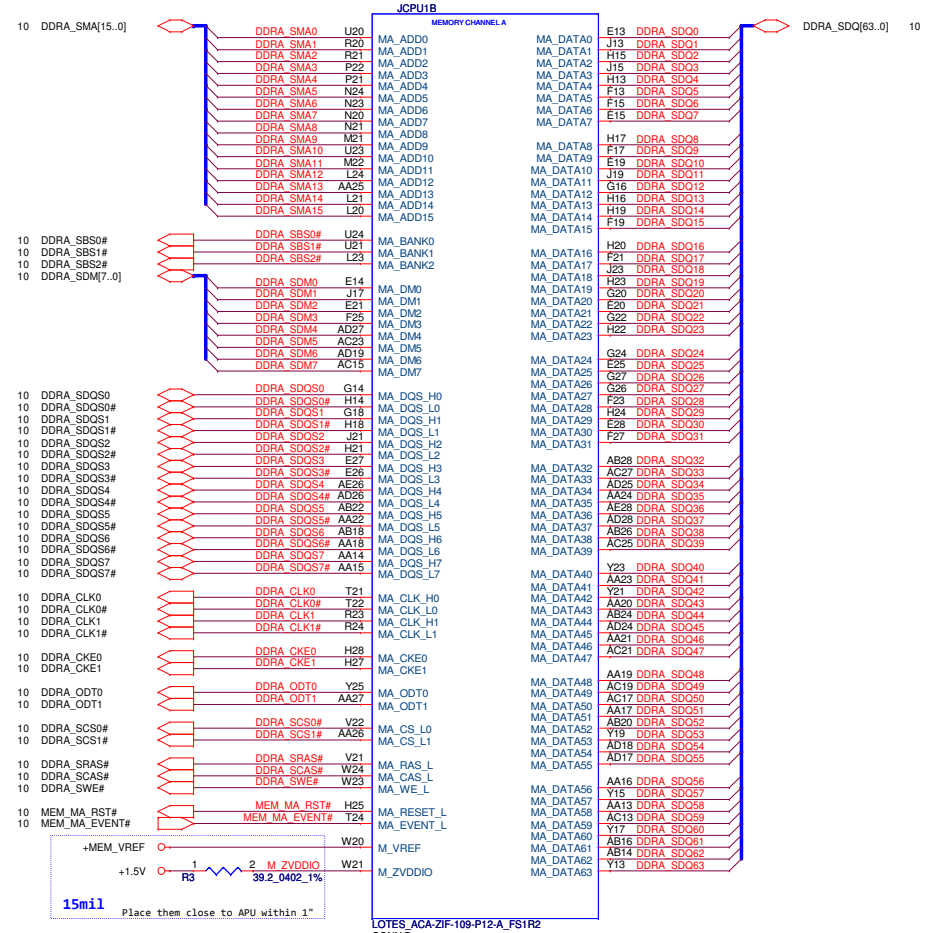
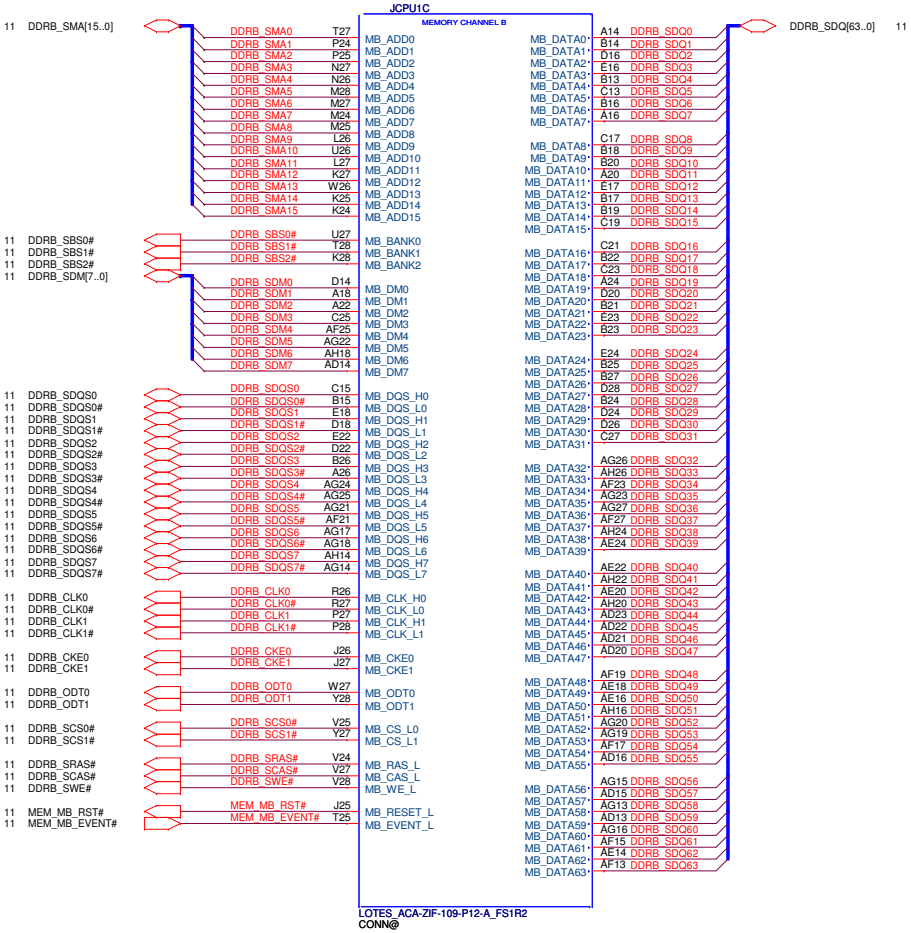
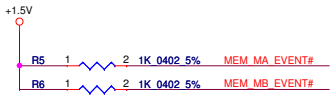
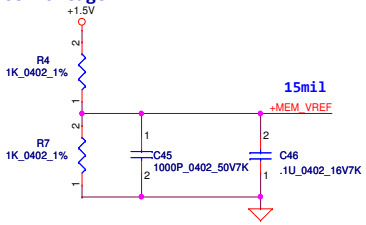




EVENT# pull high



0.75V reference voltage



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Compal Electronics, Inc.

Title: FS1r2 DDRIII Memory I/F

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Place near APU

JCPU1D

ANALOG/DISPLAY/MISC

LVDS

To FCH

HDMI

Route as differential with VSS_SENSE

LOTES_ACA-ZIF-109-P12-A_FS1R2

CONN@

SIT, NO.4

To LVDS Translater

To FCH MainLink

To HDMI

If not used, pins are left unconnected (DG ref.) 20101111

SDV2, NO.45

To FCH

Asserted as an input to force the processor into the HTC-active state

H_PROCHOT#_EC: default low/active high
APU_PROCHOT# : default high/ active low
H_PROCHOT#: default high/ active low

SIT, NO.16

THERMTRIP shutdown Temperature: 125 degree

Indicates to the FCH that a thermal trip has occurred. Its assertion will cause the FCH to transition the system to S5 immediately

MMBT3904_NL_SOT23-3

FVT, NO.37

CPU TSI interface level shift

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

SIT, NO.3

BSH111_SOT23-3

Aux signal are re-configured as I2C signals for DDC. APU AUX pin are 3.3V tolerant
Default follow PAWGX setting for pull-high resistor value

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: FS1r2 Display/MISC/HDT

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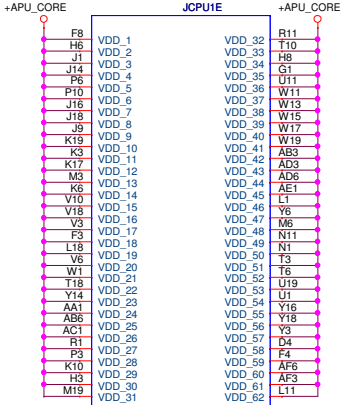
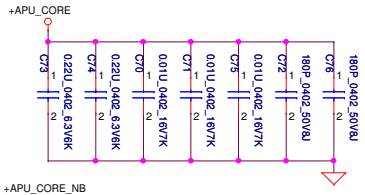
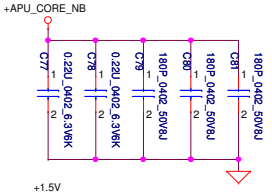
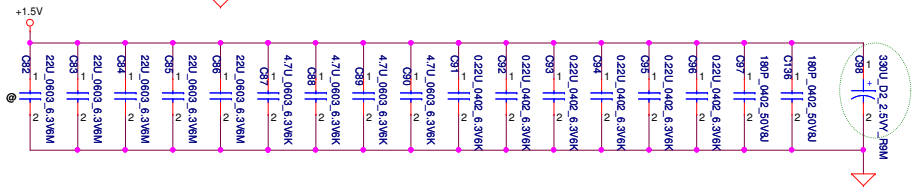
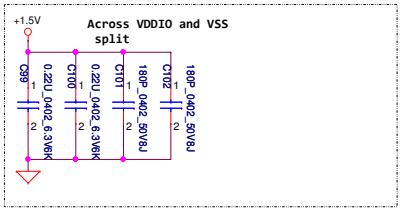
Power Name	Consumption
VDD +APU_CORE	60A
VDDNB +APU_CORE_NB	44A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A

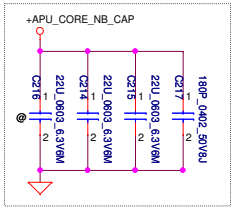


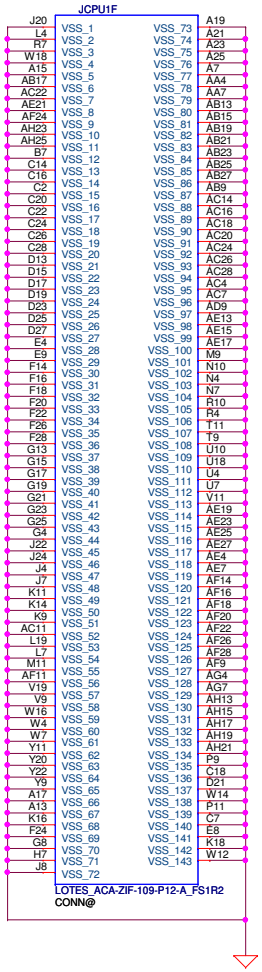


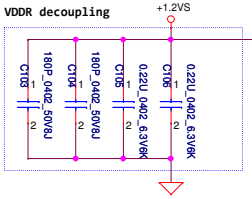


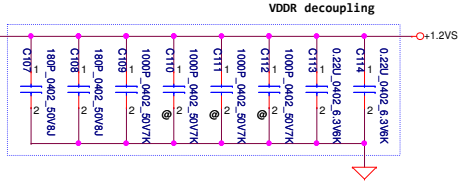


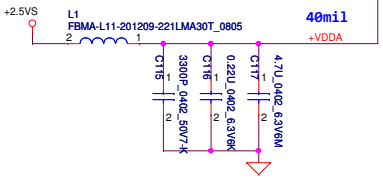












Demo Board Capacitor

APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 +2(split)
			180pF x 1 + 2(split)

VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 4	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

Security Classification	Compal Secret Data	
Issued Date	2011/04/18	Deciphered Date 2015/07/08

Compal Electronics, Inc.

Title: FS1r2 PWR/GND

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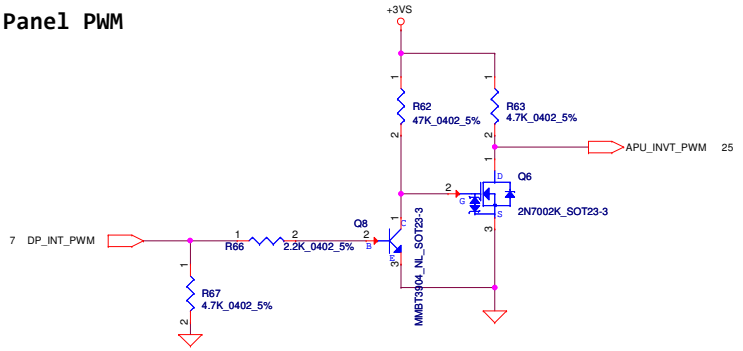
HPD

SIT, NO.4

Panel PWM



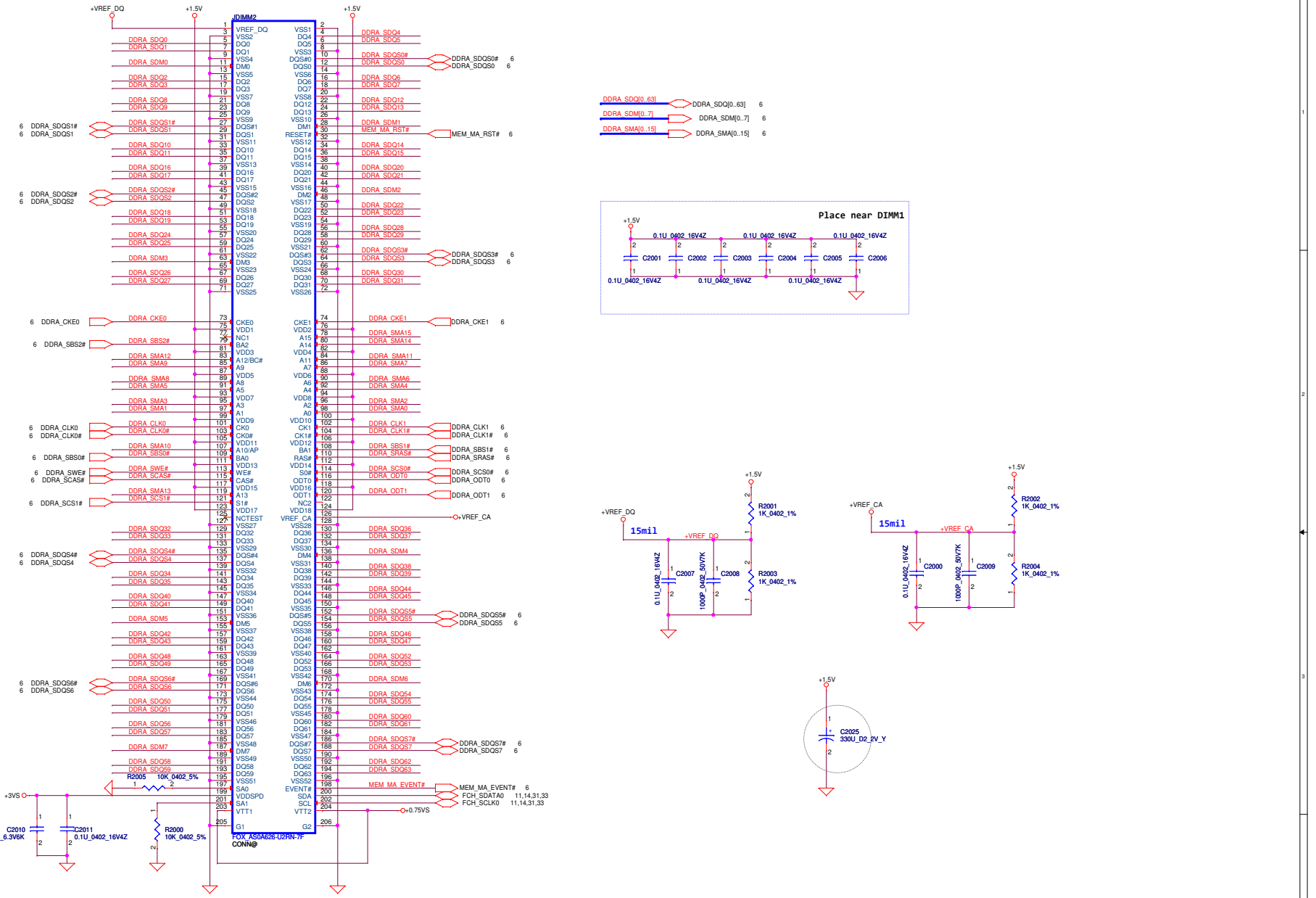
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: FS1r2 Signal Level Shifter

Size: Custom | Document Number: LA-8121P | Rev: 0.4

Date: Monday, January 16, 2012 | Sheet 9 of 50



Reverse H:5.2mm

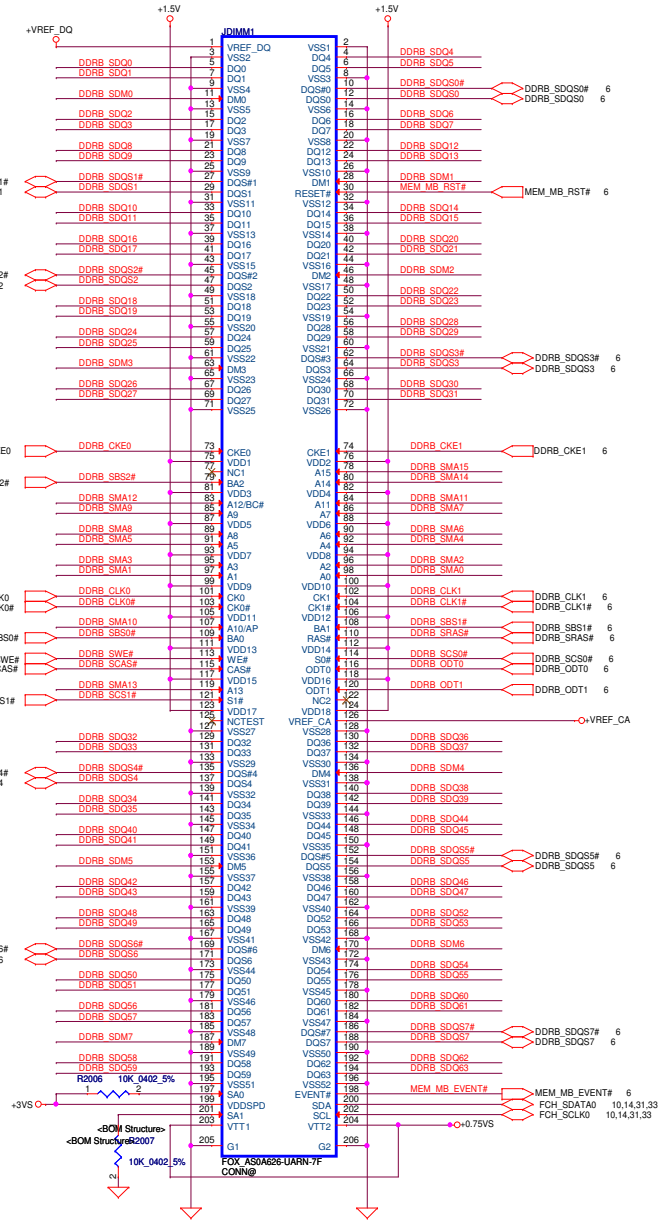
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

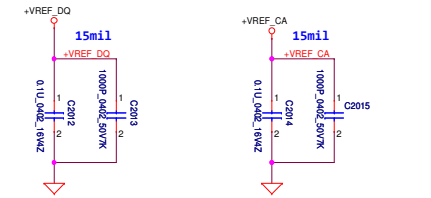
Title: DDRIII SO-DIMM 1

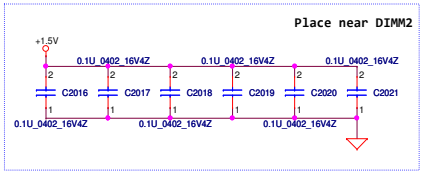
Size	Document Number	Rev
C	LA-8121P	0.4

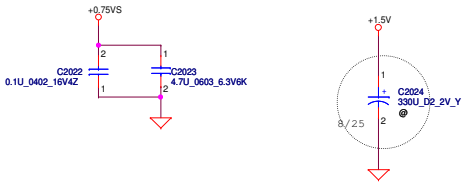
Date: Monday, January 16, 2012 Sheet 10 of 50



Reverse H:9.2mm







Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: DDRIII SO-DIMM 2

Size	Document Number	Rev
C	LA-8121P	0.4

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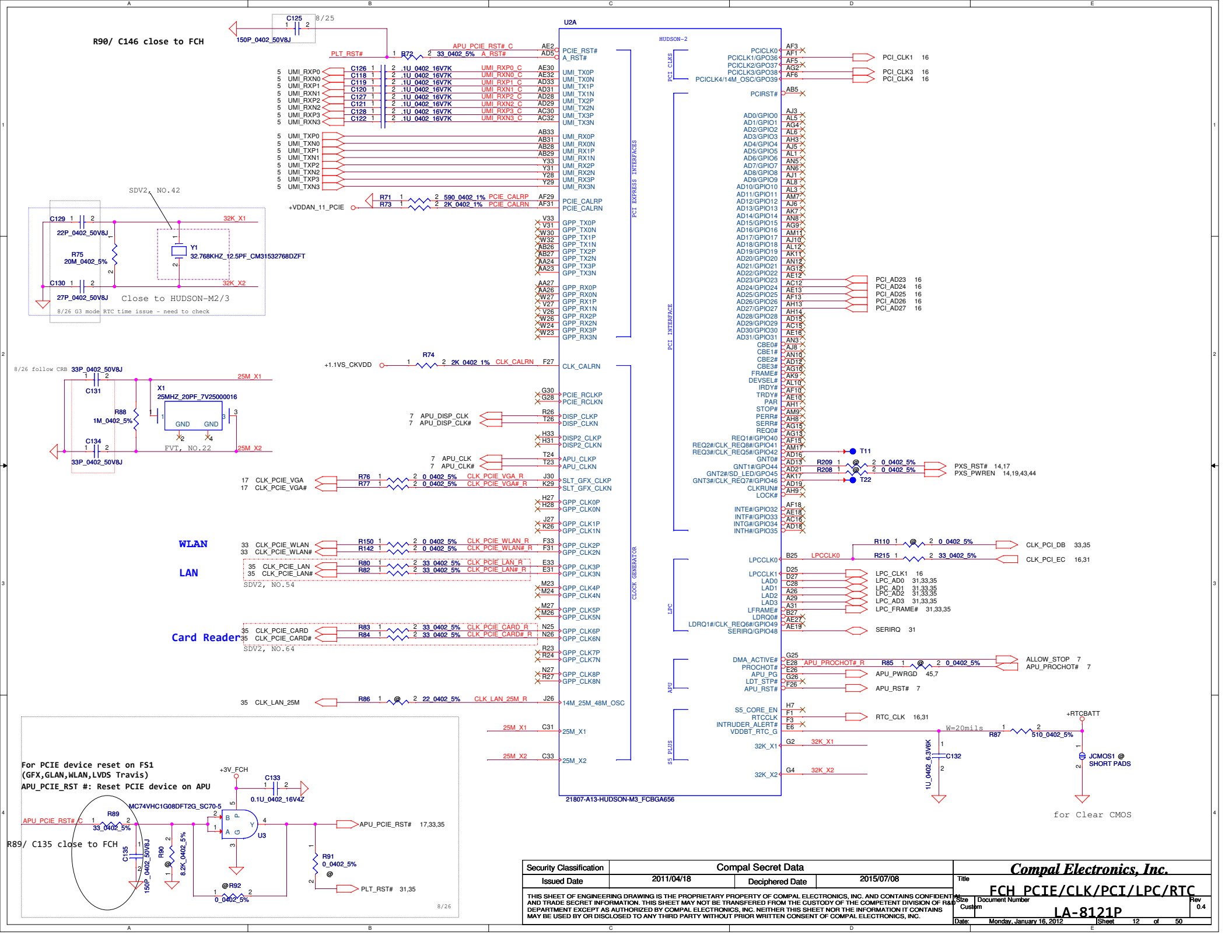
R90/ C146 close to FCH
C125
8/25
150P_0402_50V8J
PLT_RST#
R72
APU_PCIE_RST#_C
33_0402_5%
A_RST#
U2A
HUDSON-2
PCIE_RST#
A_RST#
PCI EXPRESS INTERFACES
UMI_RXP0
UMI_RXN0
UMI_RXP1
UMI_RXN1
UMI_RXP2
UMI_RXN2
UMI_RXP3
UMI_RXN3
UMI_TXP0
UMI_TXN0
UMI_TXP1
UMI_TXN1
UMI_TXP2
UMI_TXN2
UMI_TXP3
UMI_TXN3
R71
R73
590_0402_1%
2K_0402_1%
PCIE_CALRP
PCIE_CALRN
+VDDAN_11_PCIE
GPP_TX0P
GPP_TX0N
GPP_TX1P
GPP_TX1N
GPP_TX2P
GPP_TX2N
GPP_TX3P
GPP_TX3N
GPP_RX0P
GPP_RX0N
GPP_RX1P
GPP_RX1N
GPP_RX2P
GPP_RX2N
GPP_RX3P
GPP_RX3N
PCI INTERFACE
PCICLK0
PCICLK1/GPIO36
PCICLK2/GPIO37
PCICLK3/GPIO38
PCICLK4/14M_OSC/GPIO39
PCIRST#
PCI_CLK1 16
PCI_CLK3 16
PCI_CLK4 16
AD0/GPIO0
AD1/GPIO1
AD2/GPIO2
AD3/GPIO3
AD4/GPIO4
AD5/GPIO5
AD6/GPIO6
AD7/GPIO7
AD8/GPIO8
AD9/GPIO9
AD10/GPIO10
AD11/GPIO11
AD12/GPIO12
AD13/GPIO13
AD14/GPIO14
AD15/GPIO15
AD16/GPIO16
AD17/GPIO17
AD18/GPIO18
AD19/GPIO19
AD20/GPIO20
AD21/GPIO21
AD22/GPIO22
AD23/GPIO23
AD24/GPIO24
AD25/GPIO25
AD26/GPIO26
AD27/GPIO27
AD28/GPIO28
AD29/GPIO29
AD30/GPIO30
AD31/GPIO31
PCI_AD23 16
PCI_AD24 16
PCI_AD25 16
PCI_AD26 16
PCI_AD27 16
CBE0#
CBE1#
CBE2#
CBE3#
FRAME#
DEVSEL#
IRDY#
TRDY#
PAR
STOP#
PERR#
SERR#
REQ0#
REQ1#/GPIO40
REQ2#/CLK_REQ8#/GPIO41
REQ3#/CLK_REQ5#/GPIO42
GNT0#
GNT1#/GPIO44
GNT2#/SD_LED/GPO45
GNT3#/CLK_REQ7#/GPIO46
CLKRUN#
LOCK#
INTE#/GPIO32
INTF#/GPIO33
INTG#/GPIO34
INTH#/GPIO35
T11
T22
R209
R208
0_0402_5%
PXS_RST# 14,17
PXS_PWREN 14,19,43,44
SDV2, NO.42
C129
22P_0402_50V8J
32K_X1
R75
20M_0402_5%
Y1
32.768KHZ_12.5PF_CM31532768DZFT
C130
27P_0402_50V8J
32K_X2
Close to HUDSON-M2/3
8/26 G3 mode RTC time issue - need to check
8/26 follow CRB
33P_0402_50V8J
C131
25M_X1
X1
25MHZ_20PF_7V25000016
R88
1M_0402_5%
GND
C134
25M_X2
FVT, NO.22
R74
+1.1VS_CKVDD
2K_0402_1%
CLK_CALRN
CLOCK GENERATOR
PCIE_RCLKP
PCIE_RCLKN
DISP_CLKP
DISP_CLKN
DISP2_CLKP
DISP2_CLKN
APU_CLKP
APU_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
GPP_CLK4P
GPP_CLK4N
GPP_CLK5P
GPP_CLK5N
GPP_CLK6P
GPP_CLK6N
GPP_CLK7P
GPP_CLK7N
GPP_CLK8P
GPP_CLK8N
14M_25M_48M_OSC
APU_DISP_CLK
APU_DISP_CLK#
APU_CLK
APU_CLK#
CLK_PCIE_VGA
CLK_PCIE_VGA#
CLK_PCIE_VGA_R
CLK_PCIE_VGA#_R
WLAN
CLK_PCIE_WLAN
CLK_PCIE_WLAN#
CLK_PCIE_WLAN_R
CLK_PCIE_WLAN#_R
LAN
CLK_PCIE_LAN
CLK_PCIE_LAN#
CLK_PCIE_LAN_R
CLK_PCIE_LAN#_R
SDV2, NO.54
Card Reader
CLK_PCIE_CARD
CLK_PCIE_CARD#
CLK_PCIE_CARD_R
CLK_PCIE_CARD#_R
SDV2, NO.64
CLK_LAN_25M
R86
22_0402_5%
CLK_LAN_25M_R
25M_X1
25M_X2
LPC
LPCCLK0
LPCCLK1
LAD0
LAD1
LAD2
LAD3
LFRAME#
LDRQ0#
LDRQ1#/CLK_REQ6#/GPIO49
SERIRQ/GPIO48
R110
R215
33_0402_5%
CLK_PCI_DB 33,35
CLK_PCI_EC 16,31
LPC_CLK1 16
LPC_AD0 31,33,35
LPC_AD1 31,33,35
LPC_AD2 31,33,35
LPC_AD3 31,33,35
LPC_FRAME# 31,33,35
SERIRQ 31
APU
DMA_ACTIVE#
PROCHOT#
APU_PG
LDT_STP#
APU_RST#
R85
APU_PROCHOT#_R
ALLOW_STOP 7
APU_PROCHOT# 7
APU_PWRGD 45,7
APU_RST# 7
S5 PLUS
S5_CORE_EN
RTCCLK
INTRUDER_ALERT#
VDDBT_RTC_G
32K_X1
32K_X2
RTC_CLK 16,31
W=20mils
R87
510_0402_5%
+RTCBATT
C132
1U_0402_6.3V6K
JCMOS1 @
SHORT PADS
for Clear CMOS
For PCIE device reset on FS1
(GFX,GLAN,WLAN,LVDS Travis)
APU_PCIE_RST #: Reset PCIE device on APU
+3V_FCH
C133
0.1U_0402_16V4Z
MC74VHC1G08DFT2G_SC70-5
U3
R89
33_0402_5%
APU_PCIE_RST# 17,33,35
R89/ C135 close to FCH
C135
150P_0402_50V8J
R90
8.2K_0402_5%
@R92
0_0402_5%
R91
0_0402_5%
PLT_RST# 31,35
8/26
Security Classification
Compal Secret Data
Issued Date
2011/04/18
Deciphered Date
2015/07/08
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Compal Electronics, Inc.
Title
FCH_PCIE/CLK/PCI/LPC/RTC
Size
Custom
Document Number
LA-8121P
Rev
0.4
Date:
Monday, January 16, 2012
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12
of
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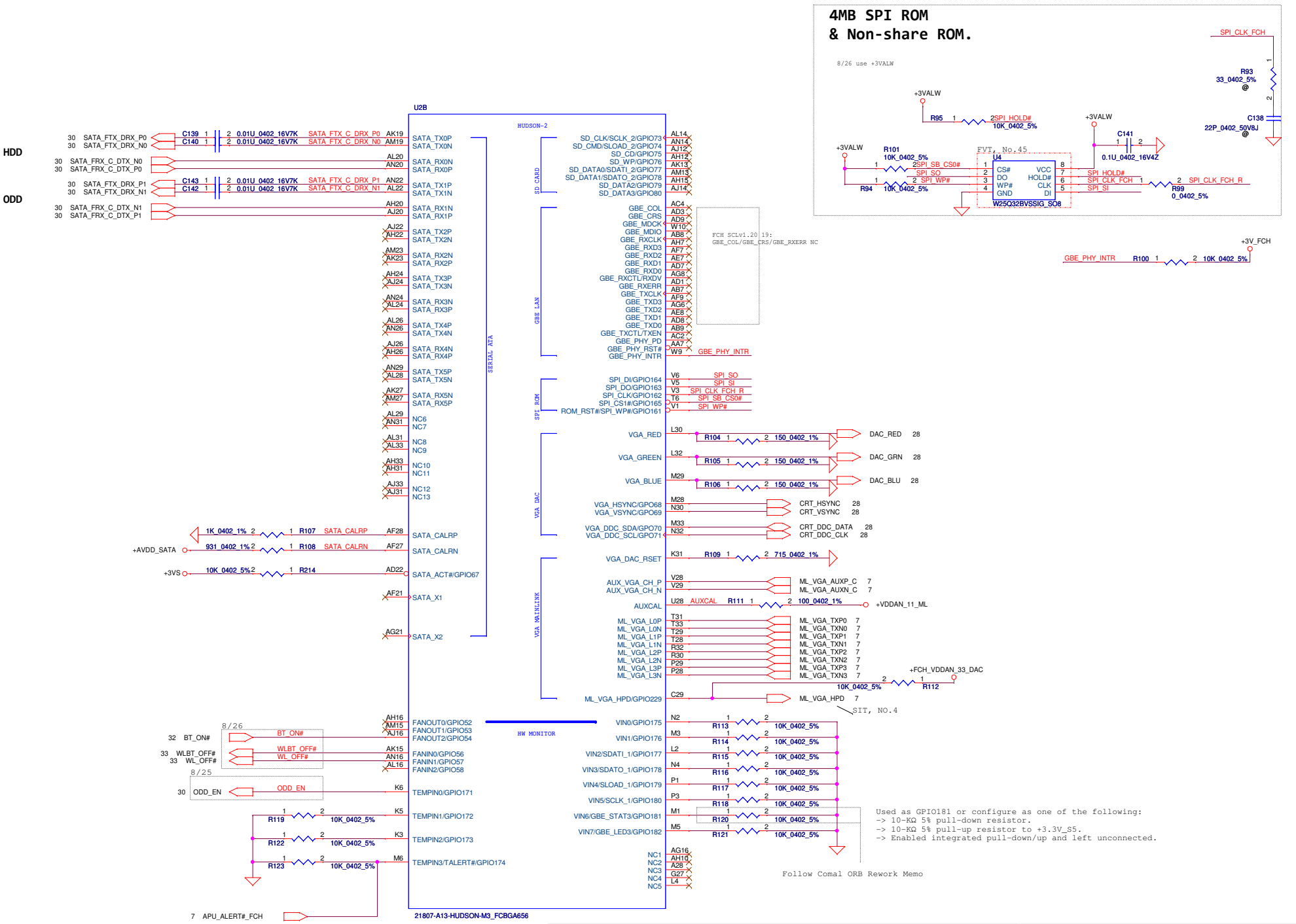


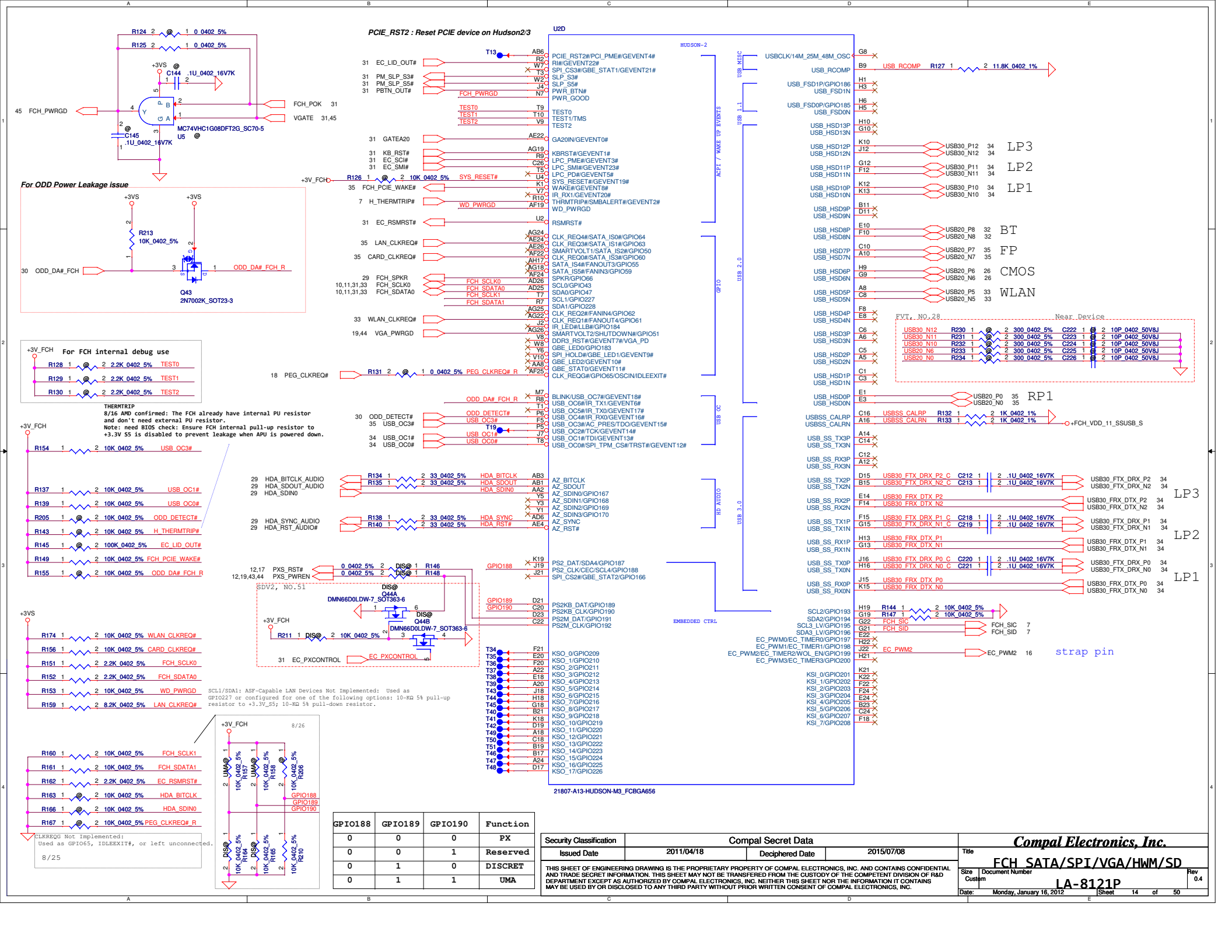
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: FCH_SATA/SPI/VGA/HWM/SD

Size: Custom | Document Number: LA-8121P | Rev: 0.4

Date: Monday, January 16, 2012 | Sheet 13 of 50



GPIO188	GPIO189	GPIO190	Function
0	0	0	PX
0	0	1	Reserved
0	1	0	DISCRET
0	1	1	UMA

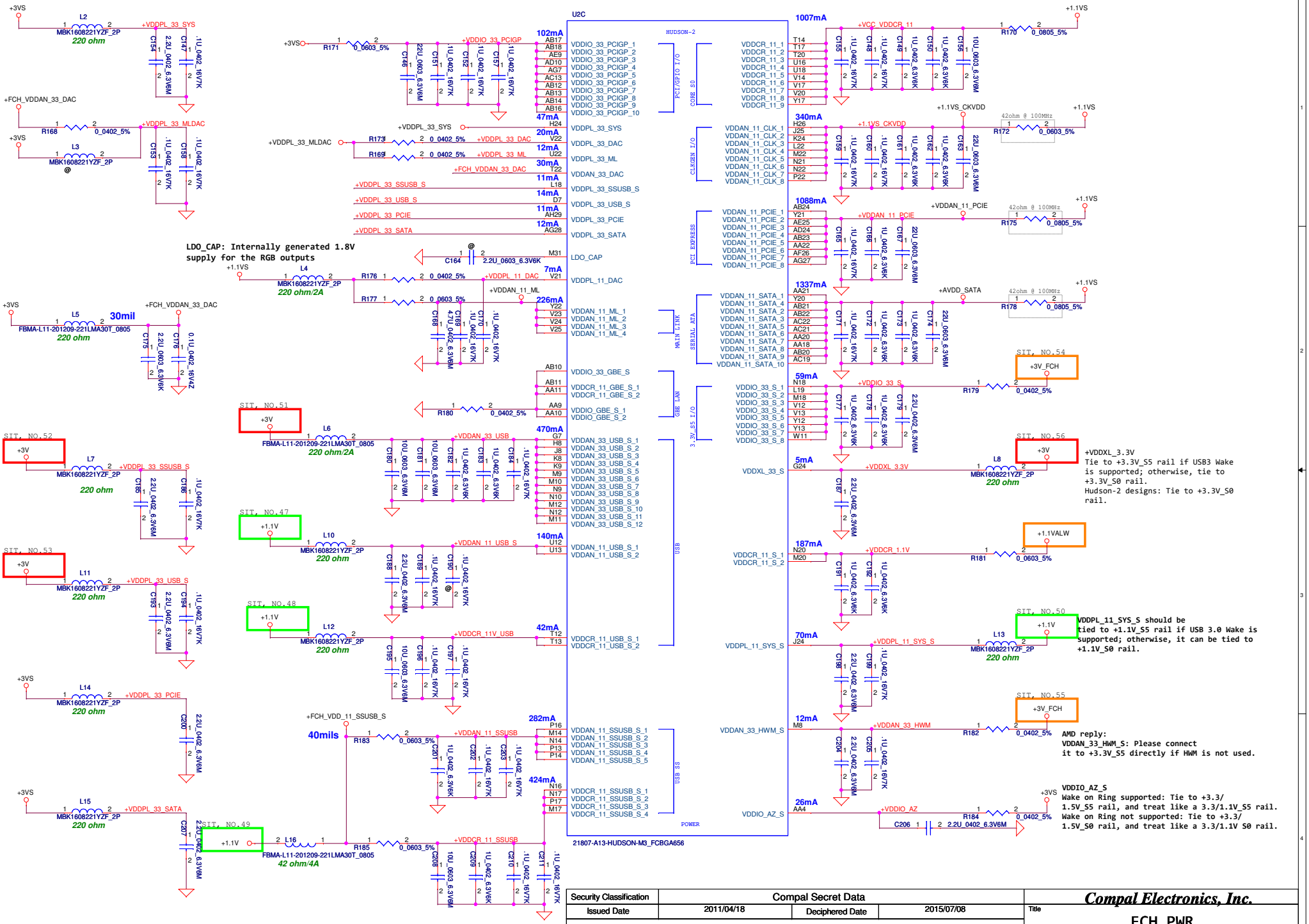
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: FCH_SATA/SPI/VGA/HWM/SD

Size: Custom | Document Number: LA-8121P | Rev: 0.4

Date: Monday, January 16, 2012 | Sheet 14 of 50



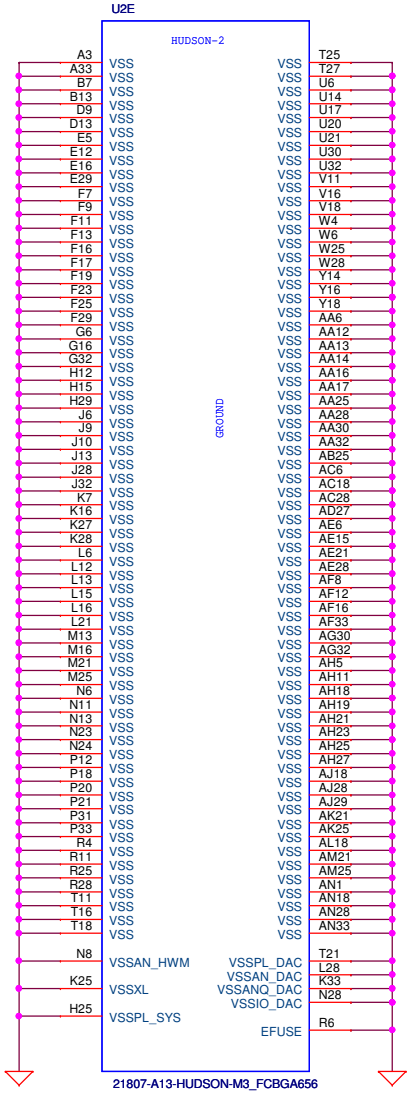
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: FCH_PWR

Size	Document Number	Rev
Custom	LA-8121P	0.4

Date: Monday, January 16, 2012 Sheet 15 of 50



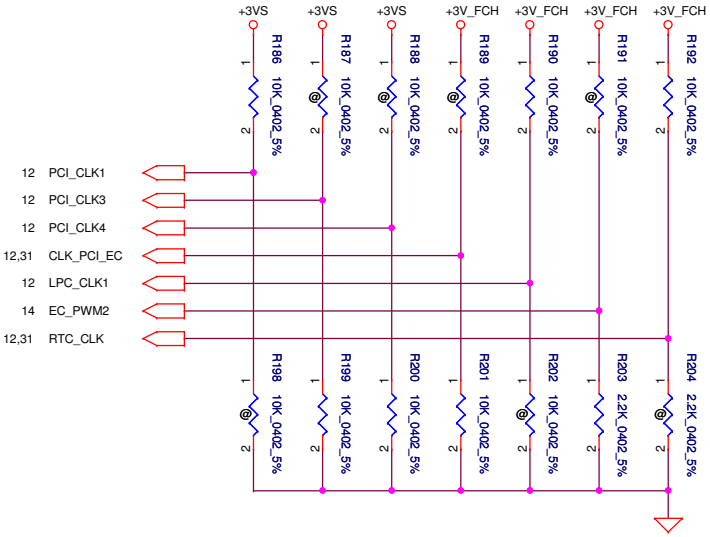
STRAP PINS

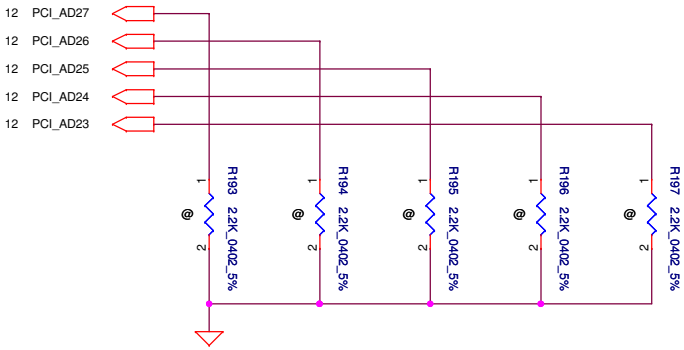
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





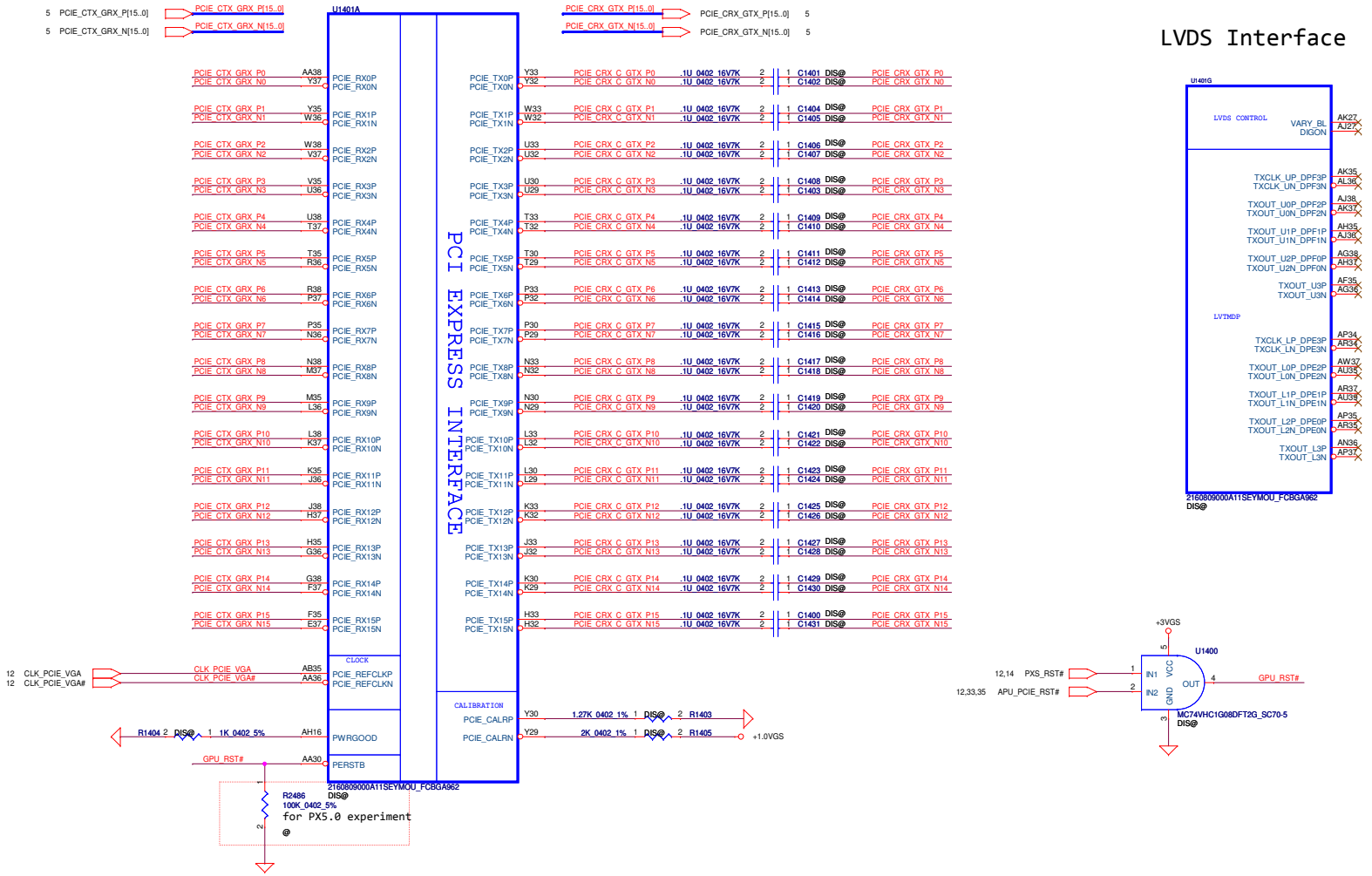
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: FCH-VSS/Strap

Size: B | Document Number: LA-8121P | Rev: 0.4

Date: Monday, January 16, 2012 | Sheet 16 of 50



Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: ATI_Themes_XT_M2_PCIE/LVDS

Size: C | Document Number: LA-8121P | Rev: 0.4

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Option for MEM ID
MEM_ID0
MEM_ID1

STRAPS

Seymour XTX / Themes XT

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
128M x 16 x 4 (1G) Hynix 1GB PN:SA00003YO00	0	1	0
128M x 16 x 4 (1G) Samsung 1GB PN:SA000047Q00	1	1	0

CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED

THEY MUST NOT CONFLICT DURING RESET

STRAPS	MLPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	Default SETTINGS
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: SAM Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable 0: GEN3 not supported at power-on 1: GEN3 supported at power-on (NOTE: RESERVED for Thames/Whistler/Seymour)	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 000 - 512bit M25P05A (ST) 001 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512bit Pm25LV512 (ChingAi) 101 - 1Mbit Pm25LV010 (ChingAi)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[6]		Reserved for future ASIC	0
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET RESERVED RESERVED RESERVED RESERVED (for Thames/Whistler/Seymour only)	
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 8 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = All usable endpoints	

Internal VGA Thermal Sensor

For GDDR5 support, or for any memory data rate above 2 Gb/s a 100-MHz reference clock is required
Clock Input Configuration -GDDR5 with Park, Madison and Broadway
a) 27MHz (3.3V) oscillator connected to XO_IN, AND
b) 100MHz (3.3V) oscillator (no spread or spreaded) connected to XO_IN2
Clock Input Configuration -GDDR5 with M97
a) 100MHz (1.8V) oscillator connected to XTALIN
Clock Input Configuration -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

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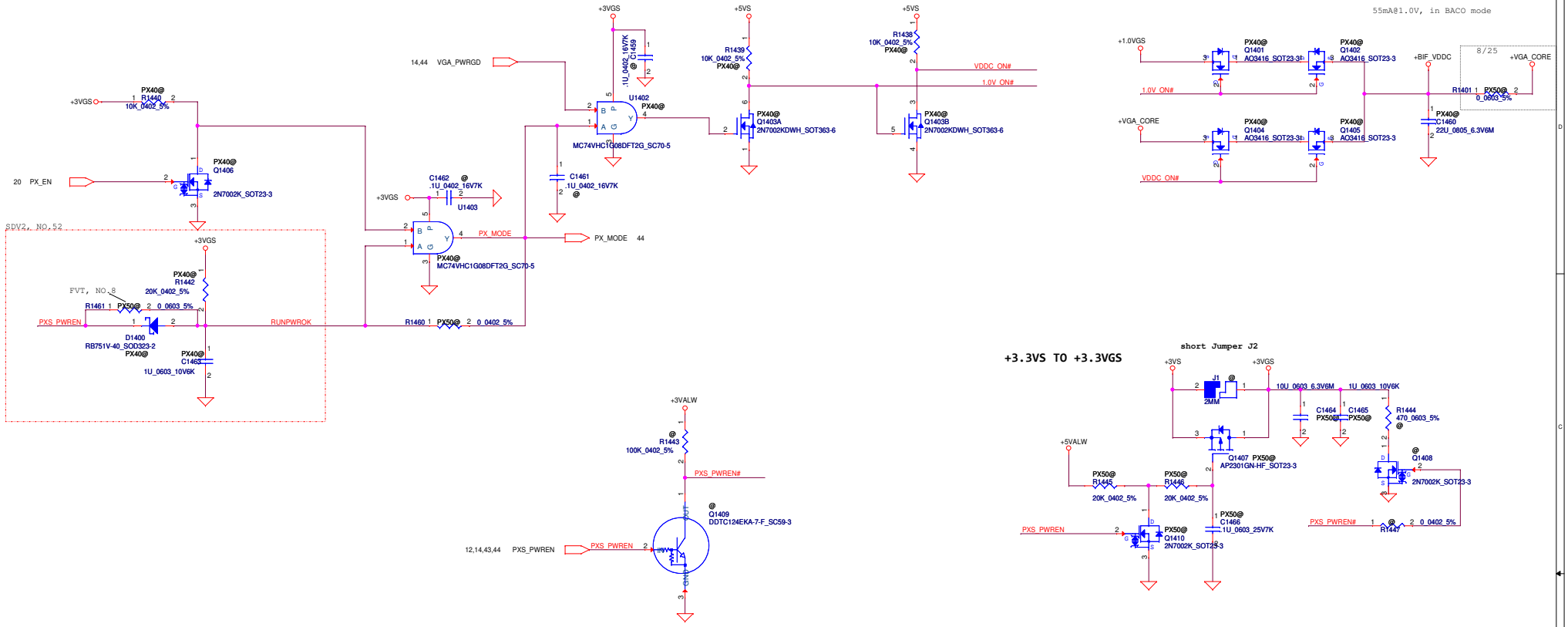
Compal Electronics, Inc.

Title: ATI Themes XT M2 Main MSIC

Size: D | Document Number: LA-8121P | Rev: 0.4

Date: Monday, January 16, 2012 | Sheet 18 of 50



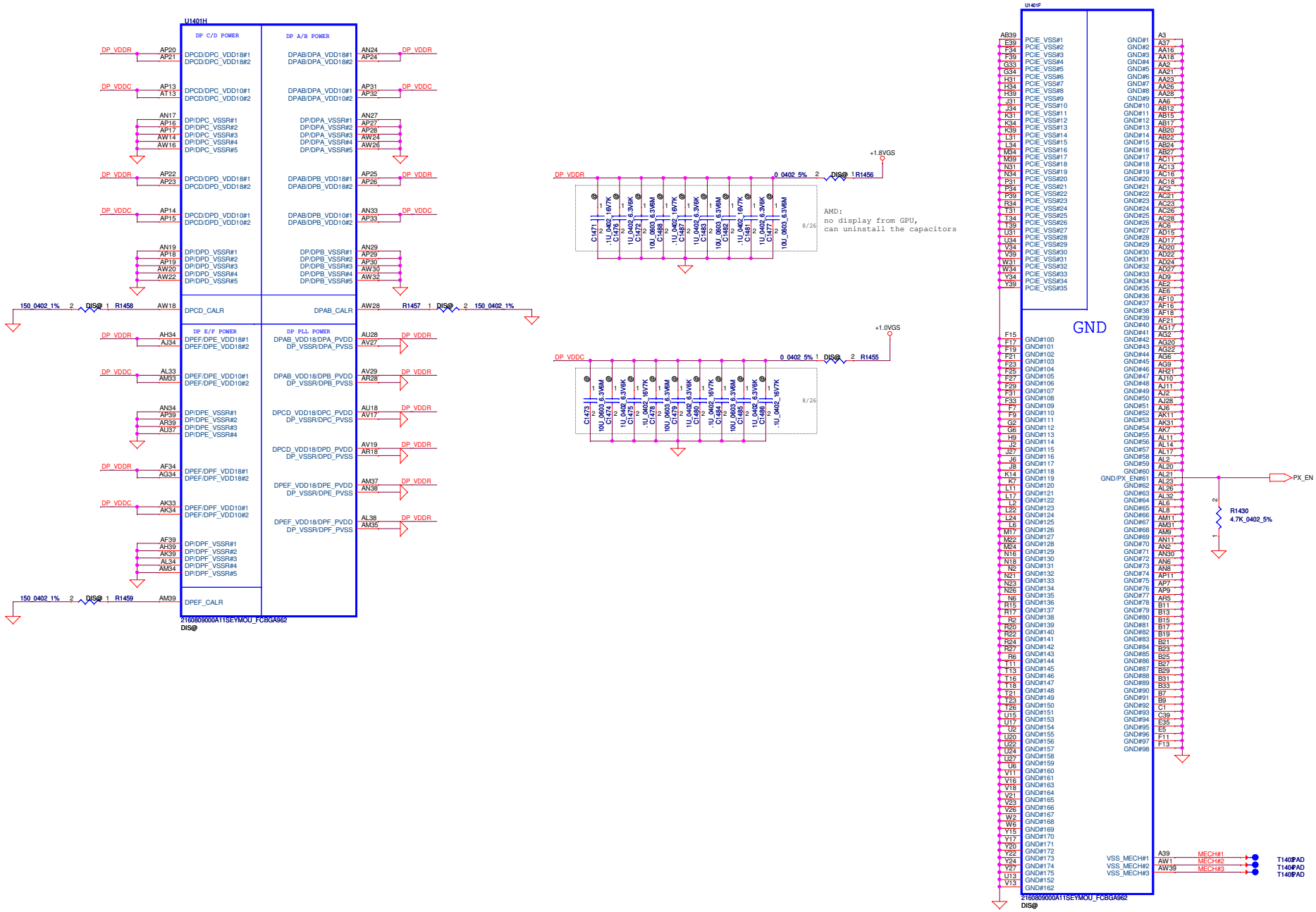
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: ATI_Themes_XT_M2_BACO

Size	Document Number	Rev
C	LA-8121P	0.4

Date: Monday, January 16, 2012 Sheet 19 of 50



Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

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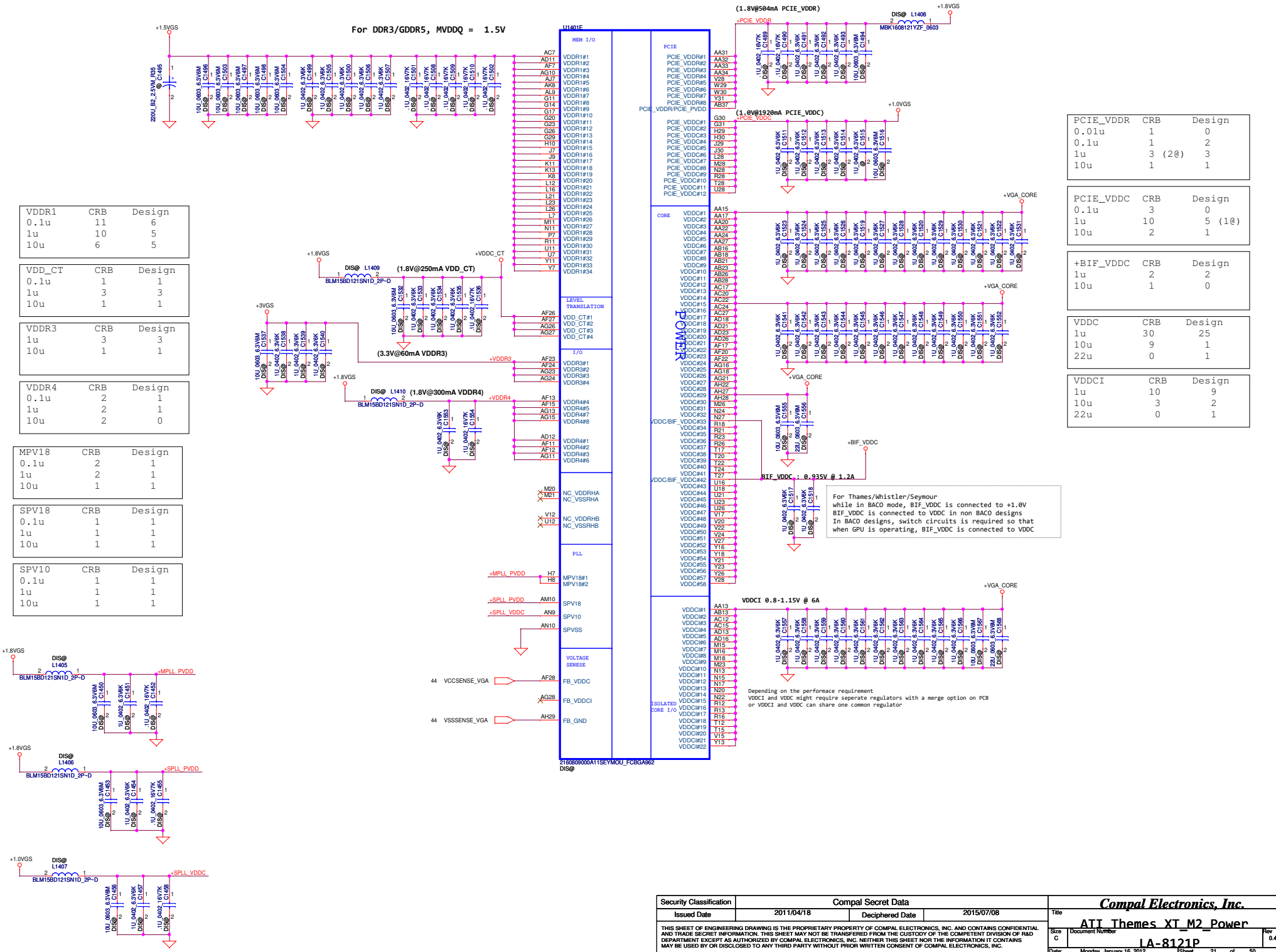
Compal Electronics, Inc.

Title: ATI_Themes_XT_M2_PWR/GND

Size: C | Document Number: LA-8121P | Rev: 0.4

Date: Monday, January 16, 2012 | Sheet 20 of 50



VDDR1	CRB	Design
0.1u	11	6
1u	10	5
10u	6	5

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

VDDR3	CRB	Design
1u	3	3
10u	1	1

VDDR4	CRB	Design
0.1u	2	1
1u	2	1
10u	2	0

MPV18	CRB	Design
0.1u	2	1
1u	2	1
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

PCIE_VDDR	CRB	Design
0.01u	1	0
0.1u	1	2
1u	3 (2@)	3
10u	1	1

PCIE_VDDC	CRB	Design
0.1u	3	0
1u	10	5 (1@)
10u	2	1

+BIF_VDDC	CRB	Design
1u	2	2
10u	1	0

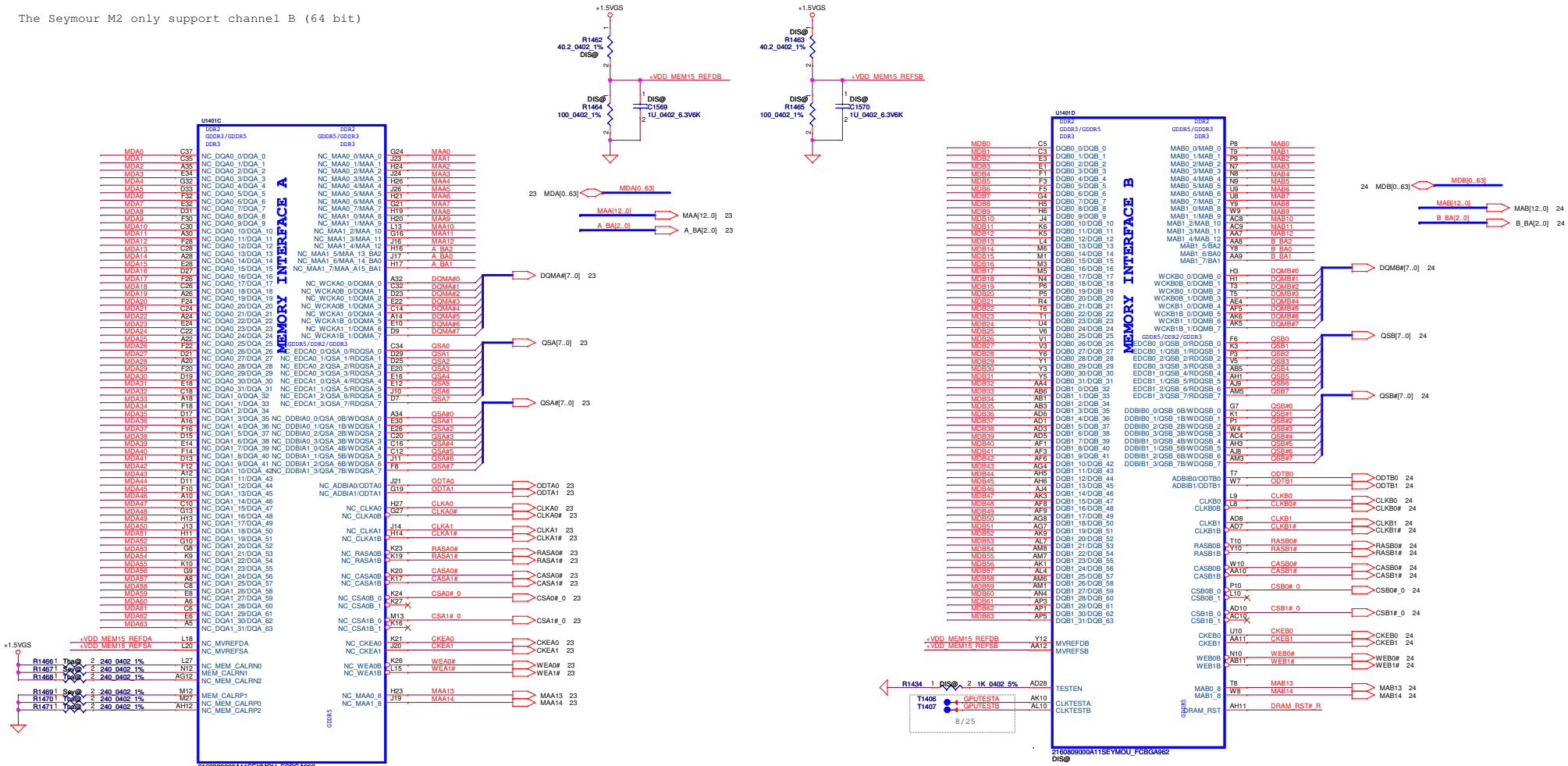
VDDC	CRB	Design
1u	30	25
10u	9	1
22u	0	1

VDDCI	CRB	Design
1u	10	9
10u	3	2
22u	0	1

Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.
Title: ATI_Themes_XT_M2_Power
Size: C
Document Number: LA-8121P
Rev: 0.4
Date: Monday, January 16, 2012
Sheet 21 of 50

The Seymour M2 only support channel B (64 bit)



	Themes XT	Seymour XTX
R1466	POP	@
R1467	@	POP
R1468	POP	@
R1469	@	POP
R1470	POP	@
R1471	POP	@

Place all these componets very close to GPU (within 25mm)
and keep all components close to each other
** This basic topology should be used for DRAM_RAT for DDR3/GDDR5

These Capacitors and Resistor values arre an example only
The series R and || cap values will depend on the DRAM loads
and will have to be calculated for different Memory,
DRAM loads and board to pass Reset Signal Spec

Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

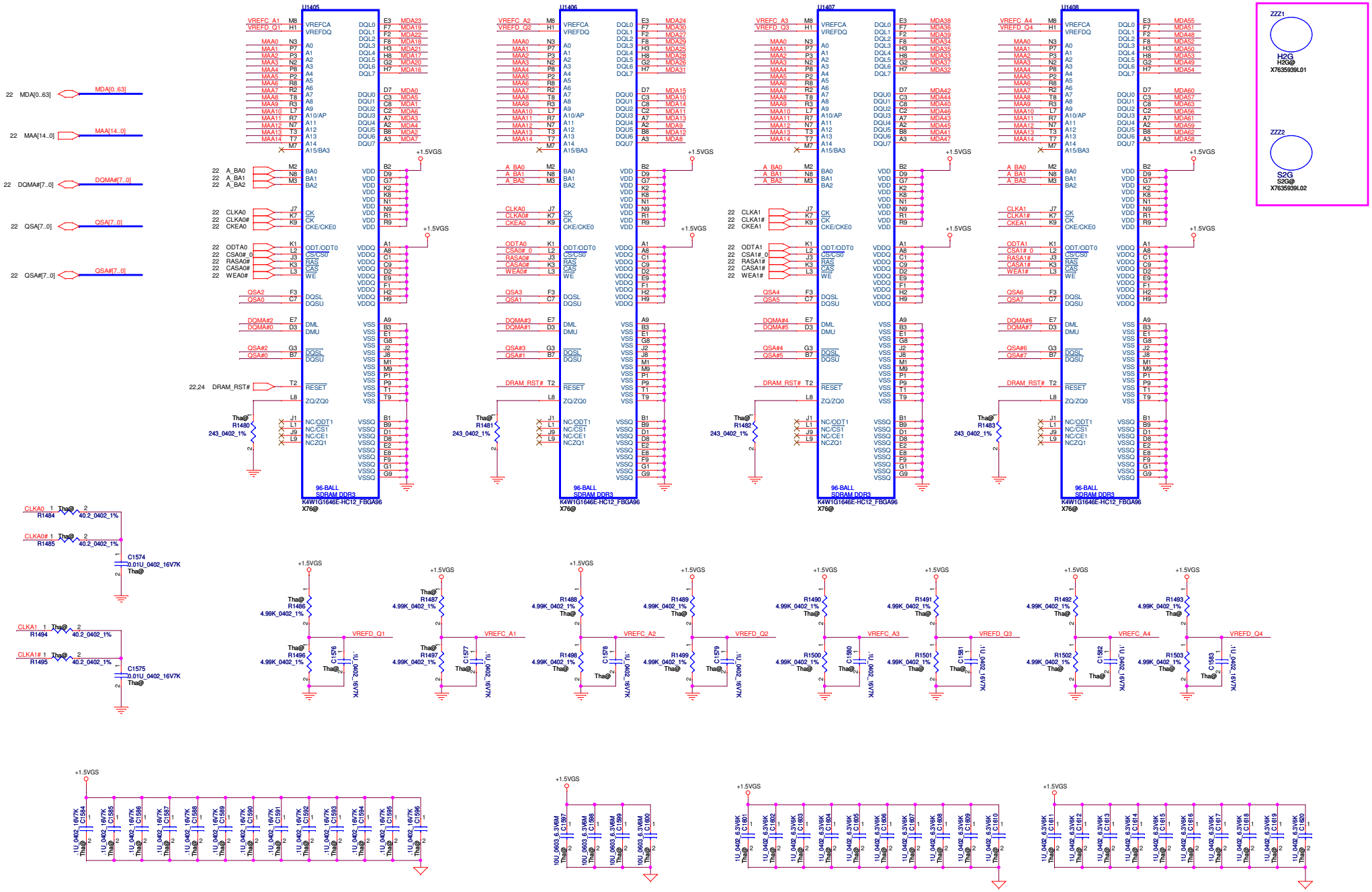
Compal Electronics, Inc.

Title: ATI Themes XT_M2_MEM IF

Size: Custom | Document Number: LA-8121P | Rev: 0.4

Date: Monday, January 16, 2012 | Sheet 22 of 50

The Seymour M2 only support channel B (64 bit),
this page unmount all parts



Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

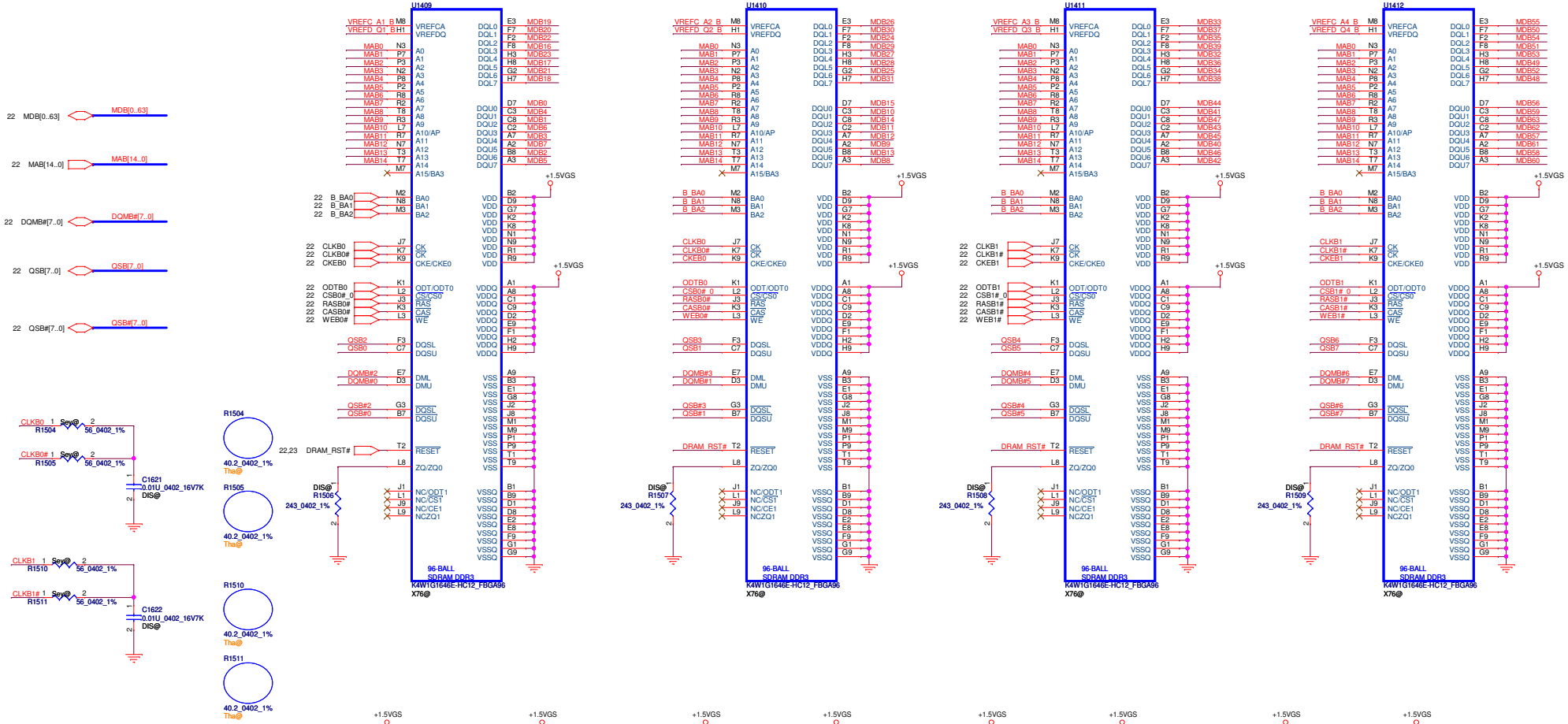
Compal Electronics, Inc.

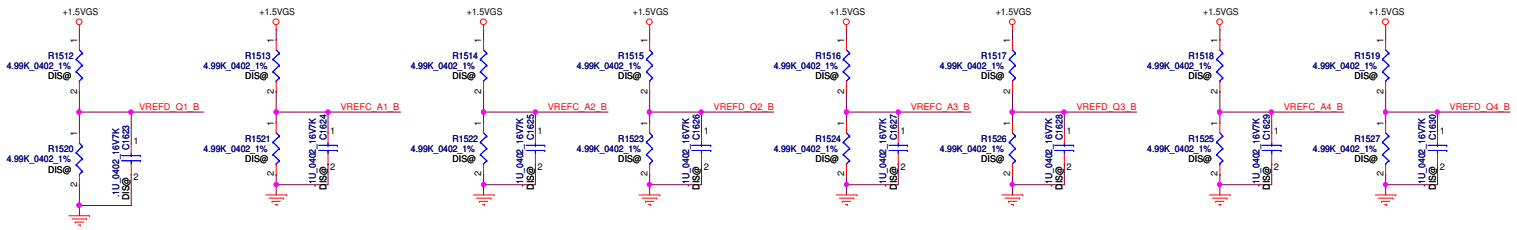
Title: ATI_Themes_XT_M2_VRAM_A

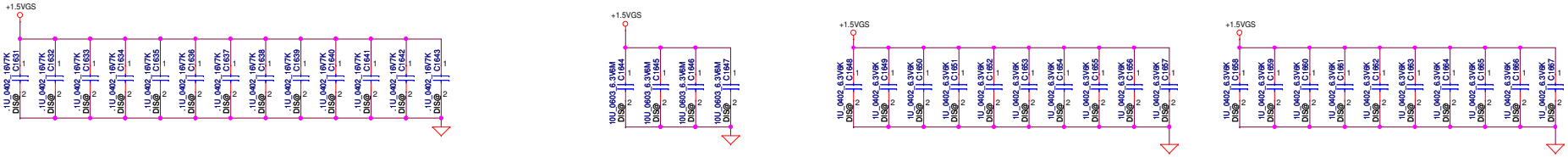
Size	Document Number	Rev
C	LA-8121P	0.4

Date: Monday, January 16, 2012 Sheet 23 of 50

The Seymour M2 only support channel B (64 bit)







Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

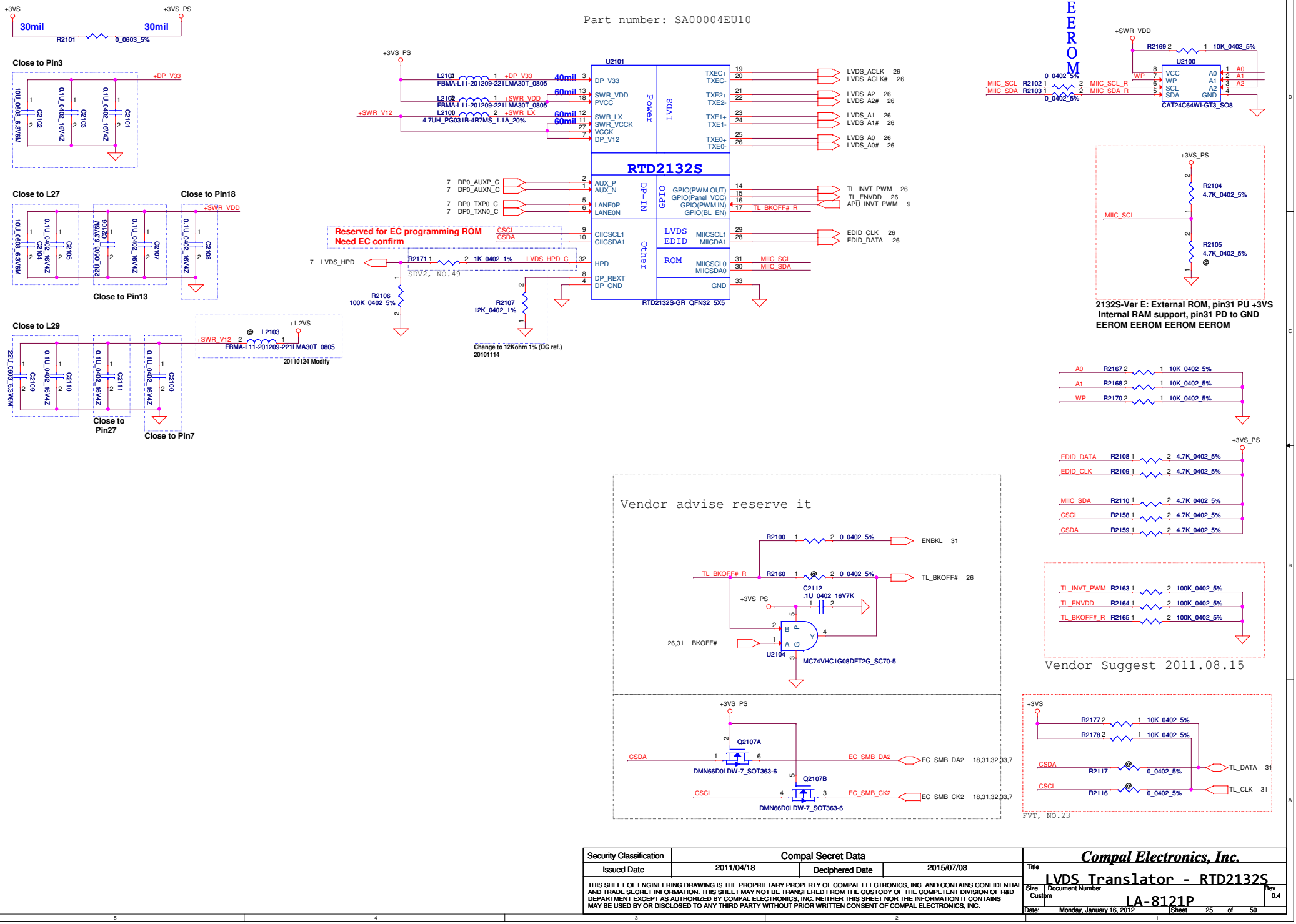
Compal Electronics, Inc.

Title: ATI_Themes_XT_M2_VRAM_B

Size	Document Number	Rev
C	LA-8121P	0.4

Date: Monday, January 16, 2012 Sheet 24 of 50

Part number: SA00004EU10



Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

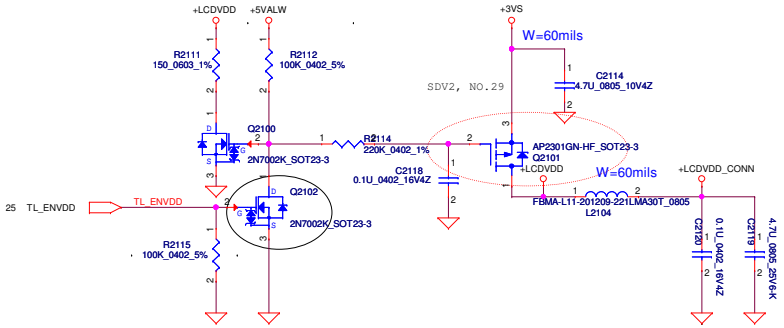
Compal Electronics, Inc.

Title: LVDS Translator - RTD2132S

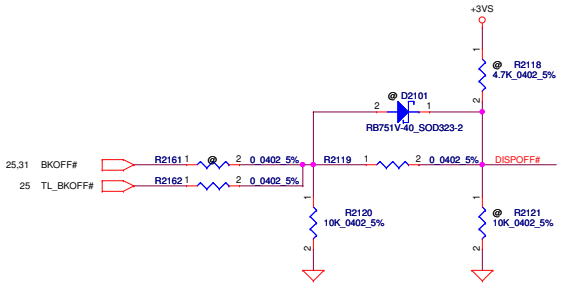
Size	Document Number	Rev
Custom	LA-8121P	0.4

Date: Monday, January 16, 2012 Sheet 25 of 50

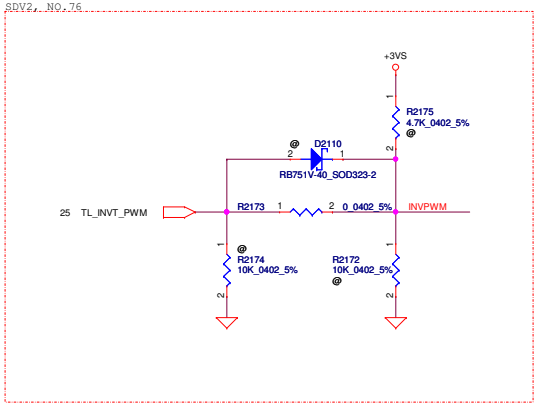
LCD POWER CIRCUIT



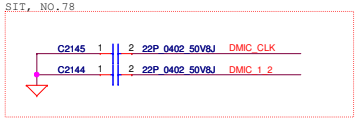
CMOS



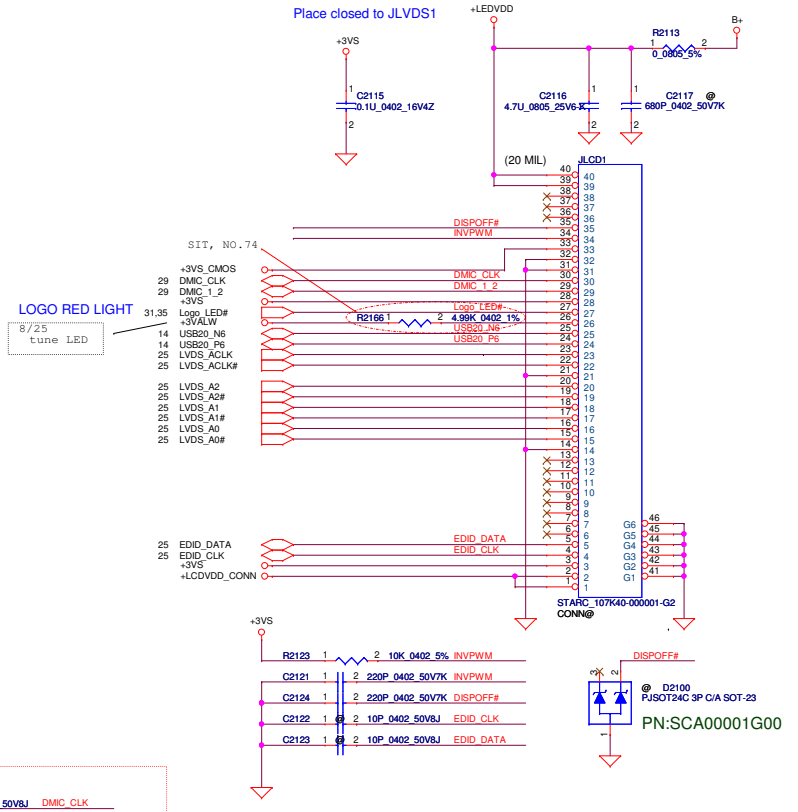
SDV2, NO.76



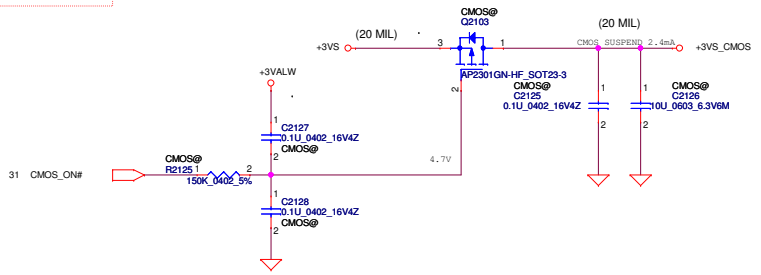
SIT, NO.78



LCD/LED PANEL Conn.



CMOS Camera Conn



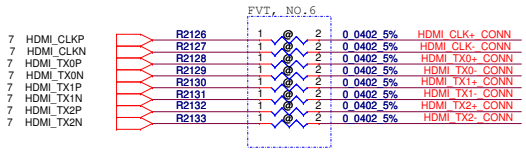
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

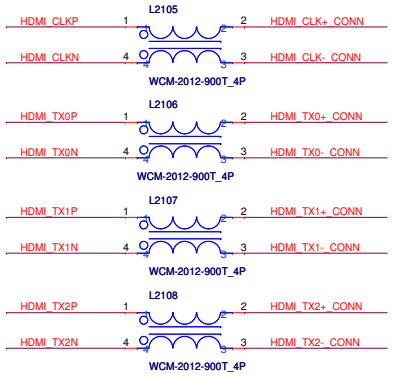
Compal Electronics, Inc.

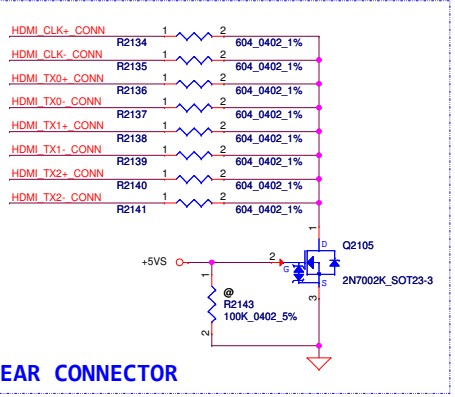
Title: LVDS CONN/CAMERA

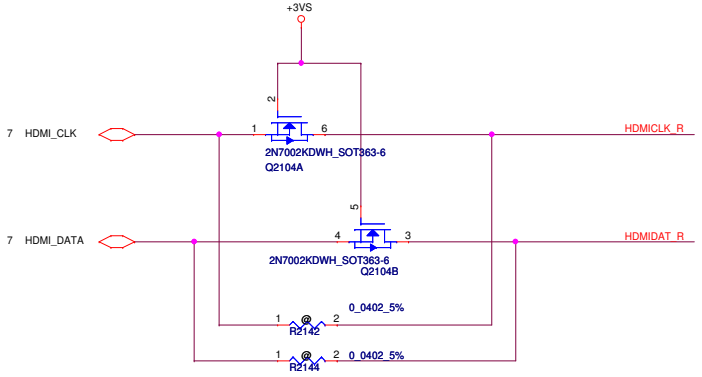
Size	Document Number	Rev
Custom	LA-8121P	0.4

Date: Monday, January 16, 2012 Sheet 26 of 50

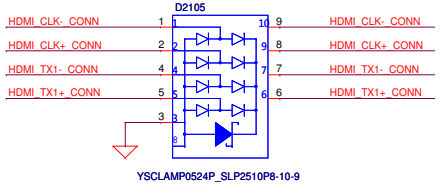


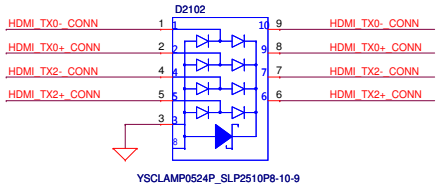


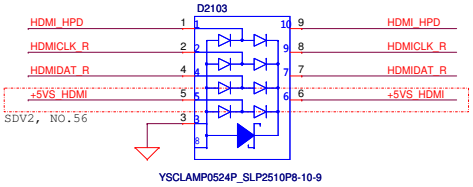


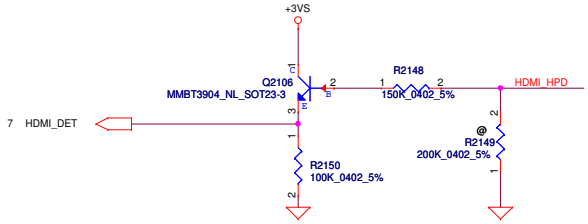


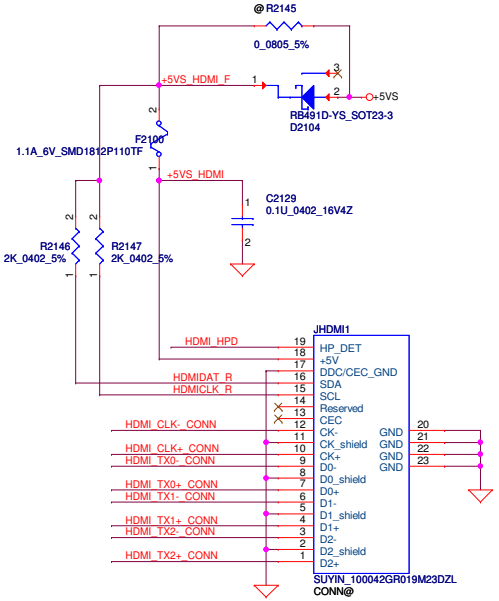
ESD Request 2011.08.13











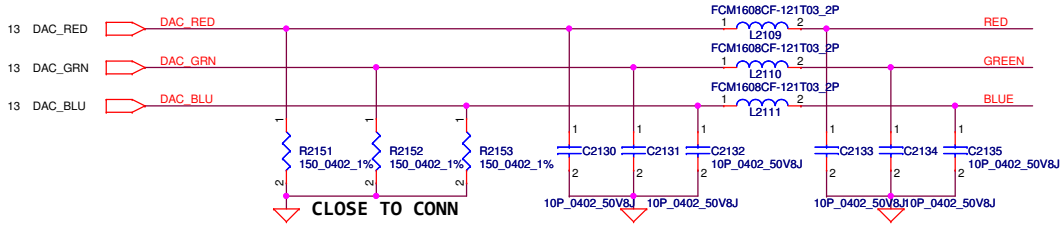
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

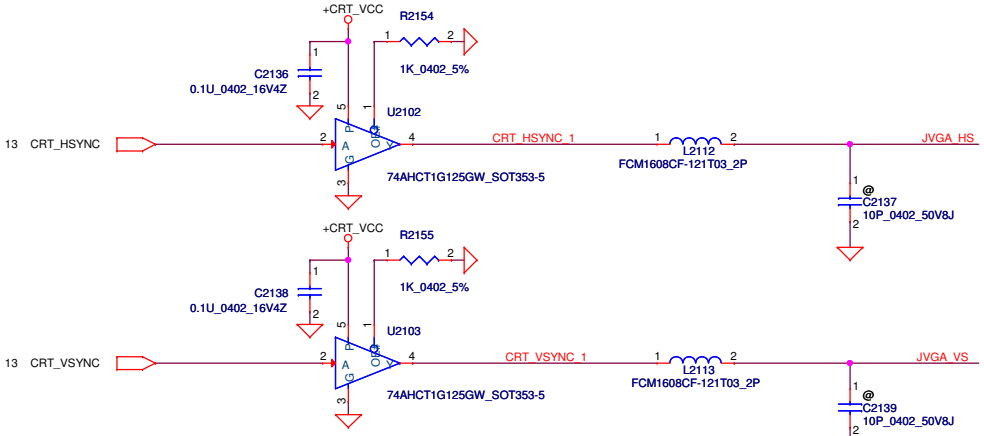
Compal Electronics, Inc.

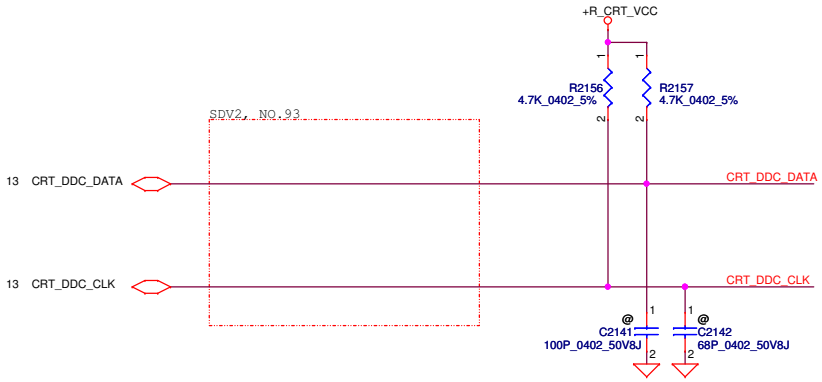
Title: HDMI Connector

Size: Custom | Document Number: LA-8121P | Rev: 0.4

Date: Monday, January 16, 2012 | Sheet 27 of 50

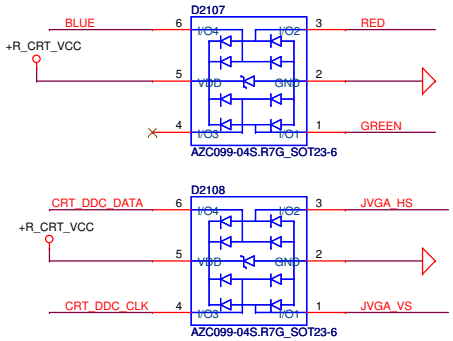




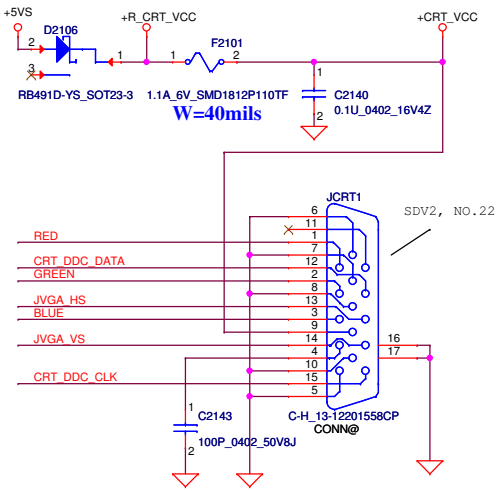


AMD check list update
20101110

ESD Request 2011.08.13



CRT Connector



Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: CRT Connector

Size: Custom | Document Number: LA-8121P | Rev: 0.4

Date: Monday, January 16, 2012 | Sheet 28 of 50

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

Layout Note:Path from +5VS to Pin12, Pin15 must be very low resistance (<0.01 ohms)

To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 & VDD_IO pins must be powerd by a rail that is not removed unless AC power is removed. *DSH page42 has more detail.

PC Beep

EC Beep 31 BEEP#

ICH Beep 14 FCH_SPKR

D1102 RB751V-40_SOD323-2 — C1111 @ 0.1U_0402_16V4Z — R1120 33_0402_5% — PC_BEEP_C — C1142 0.1U_0402_16V4Z — PC_BEEP

D1101 RB751V-40_SOD323-2

R1121 10K_0402_5%

SDV2, NO.71

SDV2, NO.35

Combo Jack detect (normal close)

MIC_JD — Q1103 LBSS138LT1G_SOT-23-3 — R1130 33K_0402_5% — EXT_MIC

C1146 1U_0402_6.3V6K

35 PLUG_IN — PLUG_IN

CX_GPIO0 — R1129 @ 33K_0402_5%

C1147 1U_0402_6.3V6K @

Internal DMIC

Internal SPEAKER

potential leakage concern

+5VS — @ Q1104 BSS138_NL_SOT23-3

14 HDA_SYNC_AUDIO — HDA_SYNC_AUDIO

R1136 0_0402_5%

Decoupling CAP

+CLASSD_5V — C1115 0.1U_0402_16V4Z — Near Pin 12

C1117 10U_0603_6.3V6M

C1118 0.1U_0402_16V4Z — Near Pin 15

C1120 10U_0603_6.3V6M @

EMI

HDA_RST#_AUDIO — C1123 @ 22P_0402_50V8J

HDA_SYNC_AUDIO — C1126 @ 22P_0402_50V8J

HDA_SDOUT_AUDIO — C1128 @ 22P_0402_50V8J

HDA_BITCLK_AUDIO R1123 @ 33_0402_5% HDA_BITCLK_AUDIO_R — C1131 @ 22P_0402_50V8J

+3VS

C1121 0.1U_0402_16V4Z — @C1119 4.7U_0603_6.3V6K — Near Pin 2

C1116 0.1U_0402_16V4Z — @C1114 1U_0402_6.3V6K — Near Pin 7

C1132 0.1U_0402_16V4Z — C1130 4.7U_0603_6.3V6K — Near Pin 3

FILT_1.65_R — C1135 1U_0402_6.3V6K — C1136 0.1U_0402_16V4Z — Near Pin 29

+LDO_OUT_3.3V — C1133 4.7U_0603_6.3V6K — C1134 0.1U_0402_16V4Z — Near Pin 27

+5VS — C1113 0.1U_0402_16V4Z — @C1112 4.7U_0603_6.3V6K — Near Pin 28

+3VS — C1124 4.7U_0603_6.3V6K — @C1129 0.1U_0402_16V4Z — Near Pin 26

FILT_1.8_R

10K only needed if supply to VAUX_3.3 is removed during system re-start.

U1101 CX20671-21Z_QFN40_6X6

FILT_1.8, VDD_IO, VAUX_3.3, DVDD_3.3, FILT_1.65, AVDD_3.3, AVDD_3.3, AVDD_HP

14 +3VS HDA_RST_AUDIO# — R1112 @ 4.7K_0402_5% — HDA_RST#_AUDIO — RESET#

14 HDA_BITCLK_AUDIO — HDA_BITCLK_AUDIO — BIT_CLK

HDA_SYNC_AUDIO — SYNC

14 HDA_SDIN0 — R1115 33_0402_5% — HDA_SDOUT_AUDIO — SDATA_IN

14 HDA_SDOUT_AUDIO — SDATA_OUT

EAPD active low
0=power down ex AMP
1=power up ex AMP

PC_BEEP — PC_BEEP

31 EAPD — R1111 0_0402_5% — CX_GPIO0 — GPIO0/EAPD#

31 EC_MUTE# — R1131 0_0402_5% — GPIO1/SPK_MUTE#

26 DMIC_CLK — R1138 FBMA-10-100505-301T_2P — DMIC_CLK_R — DMIC_CLK

26 DMIC_1_2 — R1139 0_0402_5% — DMIC_1_2_R — DMIC_1/2

SPK_L2+ — LEFT+

SPK_L1- — LEFT-

SPK_R2+ — RIGHT+

SPK_R1- — RIGHT-

GND

SDV2, NO.13

FVT, NO.13

Near Pin 17

LPWR_5.0, RPWR_5.0, CLASS-D_REF — C1107 0.1U_0402_16V4Z — +CLASSD_5V — R1137 0_0805_5% — +5VS

SENSE_A — R1113 5.11K_0402_1% — MIC_JD — +3VS

R1114 20K_0402_1%

R1116 39.2K_0402_1% — PLUG_IN

Port B
Port A

PORTB_R, PORTB_L, B_BIAS — PORTC_R — C1108 2.2U_0603_6.3V6K — R1133 100_0402_1% — EXT_MIC — External MIC — EXT_MIC 35

PORTC_L

+MICBIASB

C_BIAS, PORTC_R, PORTC_L — EXT_MIC — R1132 2K_0402_5% — R1128 4.7K_0402_5%

PORTA_R — HP_OUTR_R — R1117 15_0402_5% — HP_OUTR — HP_OUTR 35

PORTA_L — HP_OUTL_R — R1118 15_0402_5% — HP_OUTL — HP_OUTL 35

Headphone

NC, NC, NC

Changed from 5.1ohm to 15ohm for "zi zi"noise.

AVEE, FLY_P, FLY_N — C1110 1U_0603_10V4Z

Rdc < 0.05 ohms
Rated Current > 2A

C1122 0.1U_0402_16V4Z — C1125 4.7U_0603_6.3V6K — Near Pin 21

Sense resistors must be connected same power that is used for VAUX_3.3

EMI

C1102 @ 0.1U_0402_16V4Z

C1103 @ 0.1U_0402_16V4Z

C1104 @ 0.1U_0402_16V4Z

R1102 @ 0_0402_5%

R1104 @ 0_0402_5%

R1105 @ 0_0402_5%

SIT, NO.81

GND GND GNDA

Internal Speaker

Width 20 mil

31 SPK_RT_Detect#

SPK_R1- — L1102 0_0603_5% — SPK_R1-_CONN

SPK_R2+ — L1103 0_0603_5% — SPK_R2+_CONN

SPK_L1- — L1104 0_0603_5% — SPK_L1-_CONN

SPK_L2+ — L1105 0_0603_5% — SPK_L2+_CONN

SPK_RT_Detect# — R1140 0_0402_5% — SPK_RT_Detect#_R

JSPK1 E-T_4070K-G06N-00L

GND GND

EMI

@ C1137 1000P_0402_50V7K

@ C1138 1000P_0402_50V7K

@ C1139 1000P_0402_50V7K

@ C1140 1000P_0402_50V7K

Note.
QALEA 14" => JSPK1 => 4Pin
QALEB 15" => JSPK1 => 6Pin

Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

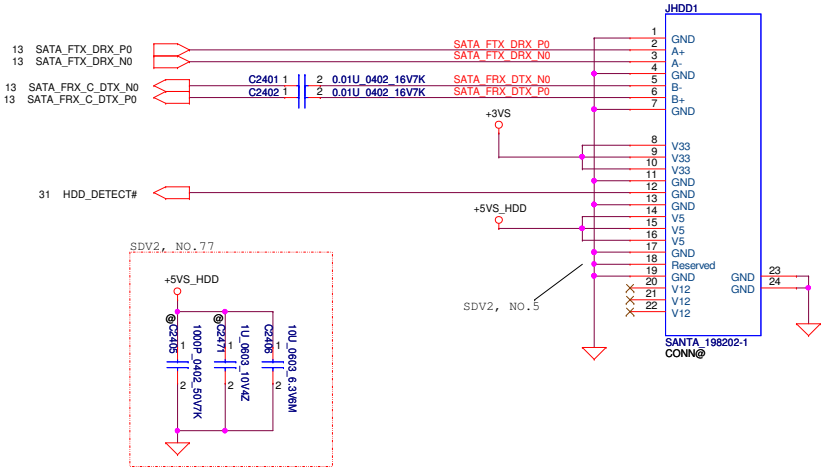
Compal Electronics, Inc.

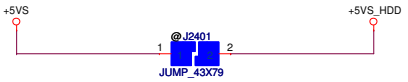
Title: HD Audio Codec CX20671

Size: Custom | Document Number: LA-8121P | Rev: 0.4

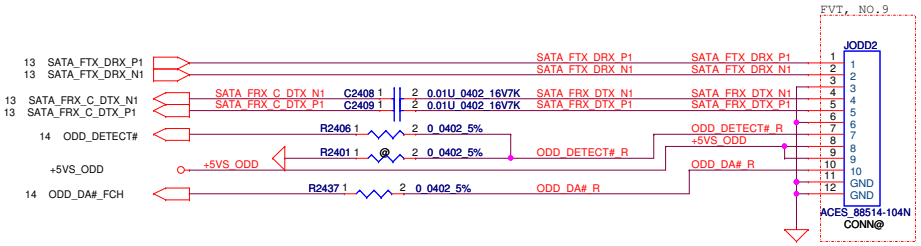
Date: Monday, January 16, 2012 | Sheet 29 of 50

SATA HDD Conn.



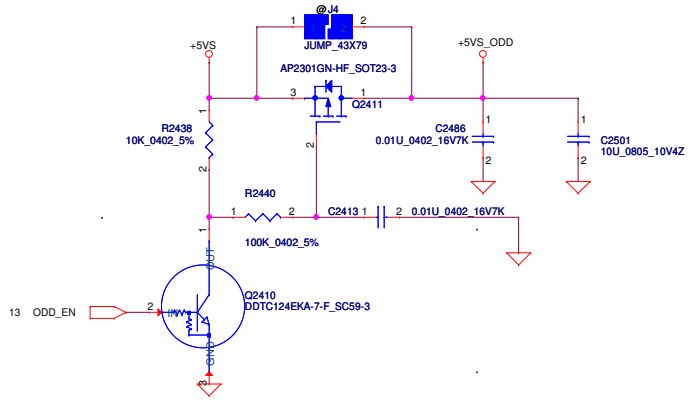


SATA ODD Conn.

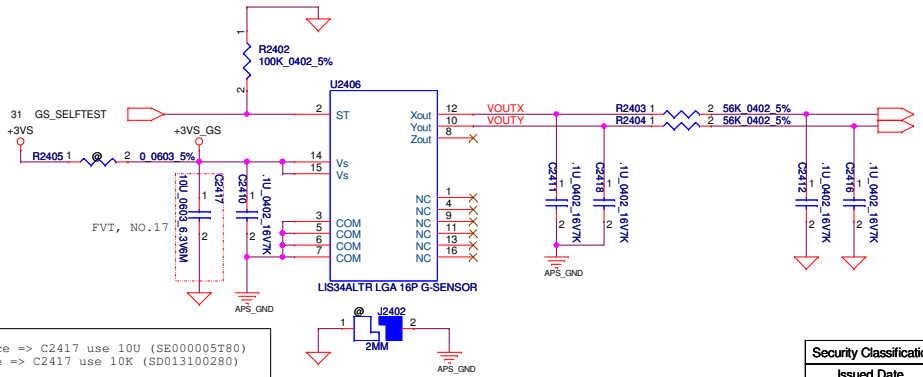


Note.
QALEA 14" => JODD1
QALEB 15" => JODD2

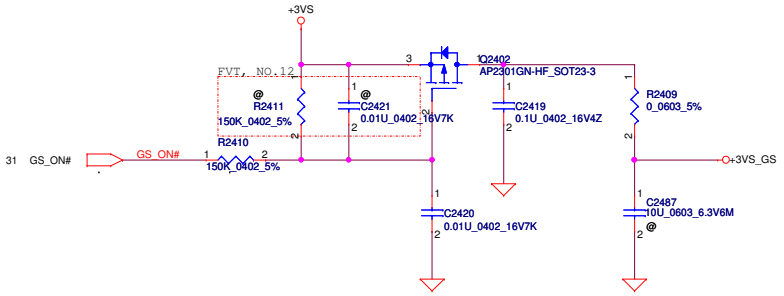
ODD Power Control



APS G-Sensor



Note.
Main Source => C2417 use 10U (SE000005T80)
2nd Source => C2417 use 10K (SD013100280)



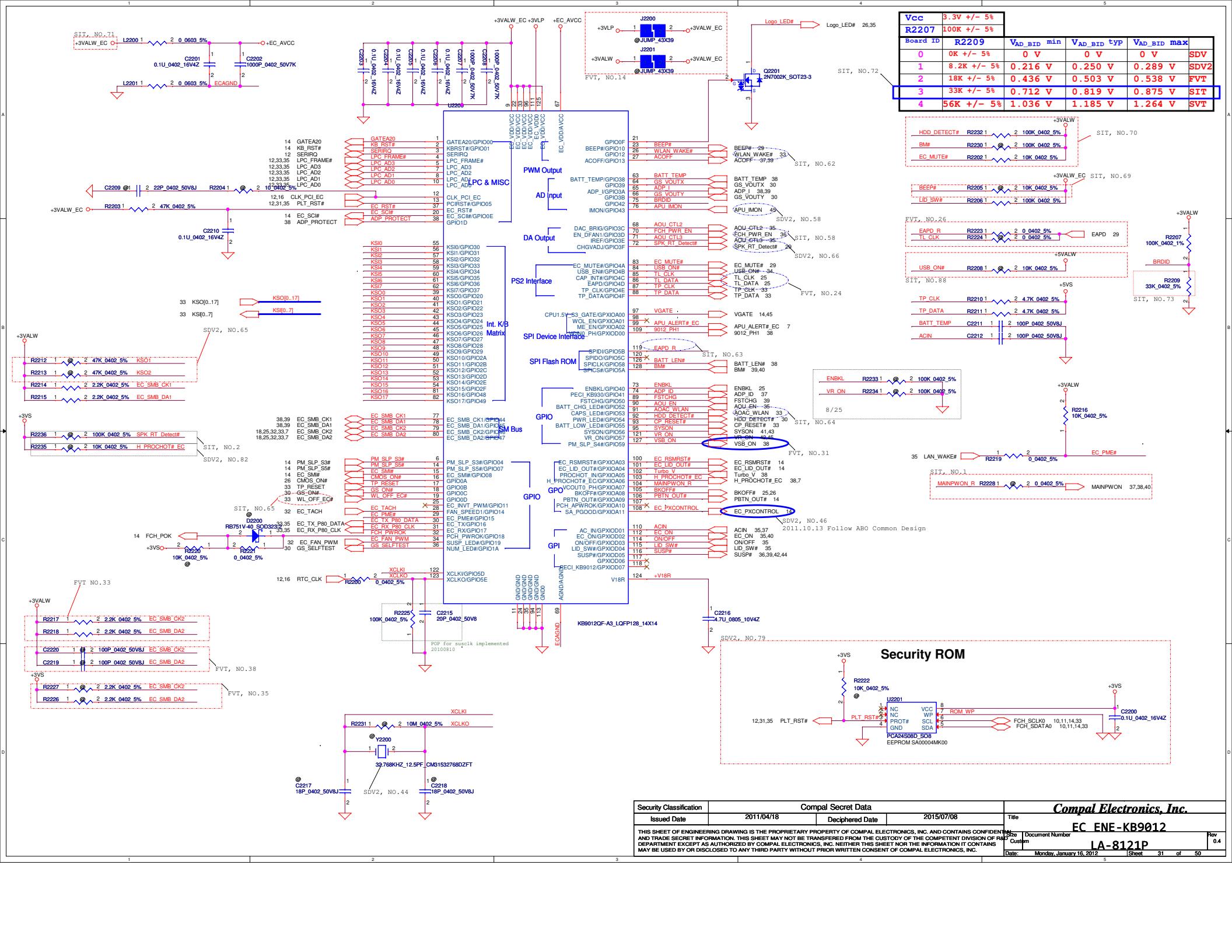
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

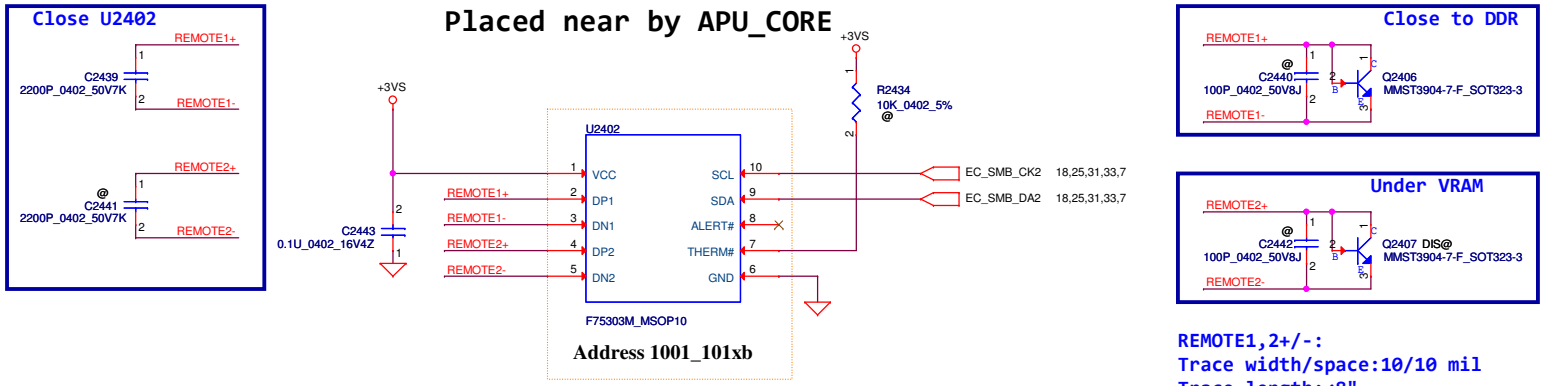
Title: HDD/ODD/G-Sensor

Size	Document Number	Rev
B	LA-8124P	0.4

Date: Monday, January 16, 2012 Sheet 30 of 50

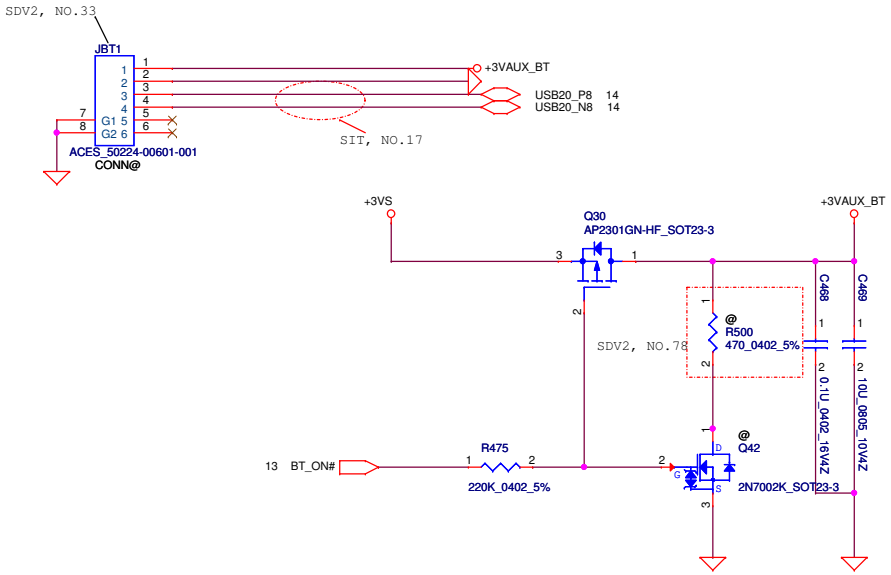

Vcc 3.3V +/- 5%
R2207 100K +/- 5%
Board ID | R2209 | VAD_BID min | VAD_BID typ | VAD_BID max
0 | 0K +/- 5% | 0 V | 0 V | 0 V | SDV
1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V | SDV2
2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V | FVT
3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V | SIT
4 | 56K +/- 5% | 1.036 V | 1.185 V | 1.264 V | SVT
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI
KB9012QF-A3_LQFP128_14X14
Security ROM
PCA24S08D_SO8
EEPROM SA00004MK00
2011.10.13 Follow ABO Common Design
Compal Secret Data
Issued Date 2011/04/18
Deciphered Date 2015/07/08
Compal Electronics, Inc.
EC ENE-KB9012
LA-8121P
Monday, January 16, 2012

Fintek Thermal sensor
Placed near by APU_CORE

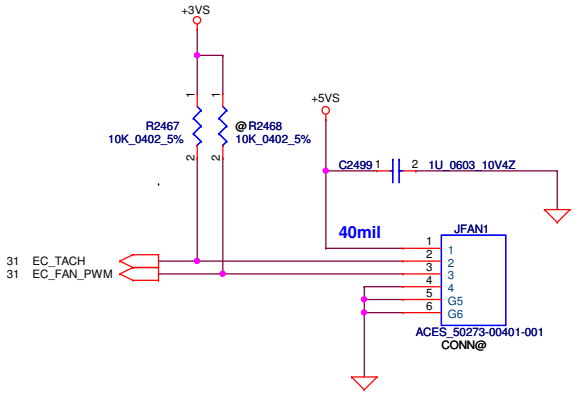


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

BT Connector



FAN1 Conn



Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: Thermal/FAN/BT

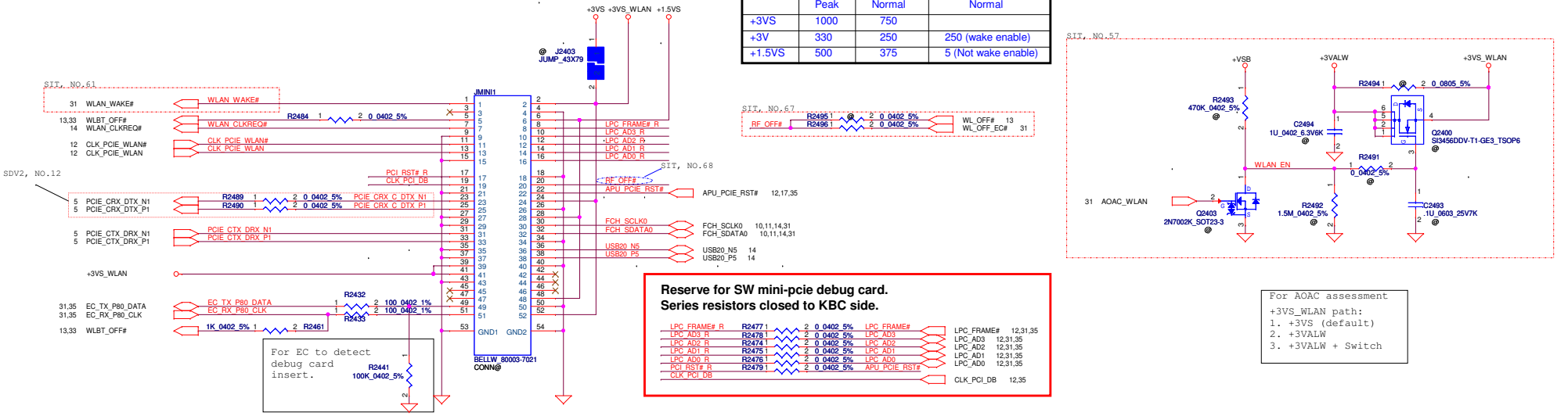
Size	Document Number	Rev
B	LA-8121P	0.4

Date: Monday, January 16, 2012 Sheet 32 of 50

WLAN Conn

Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

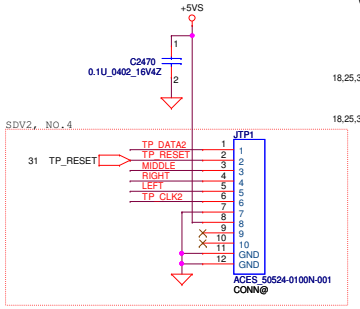


For AOAC assessment
+3VS_WLAN path:
1. +3VS (default)
2. +3VALW
3. +3VALW + Switch

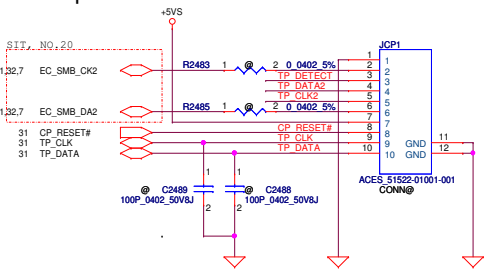
INT_KBD Conn.

CONN PIN define need double check

Track Point Conn

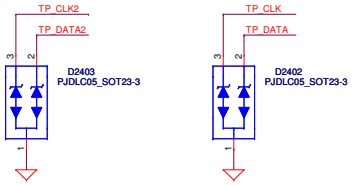


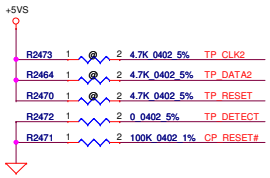
Click pad 10PIN



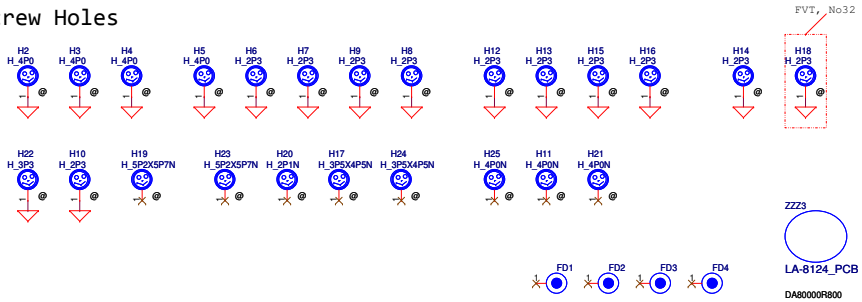
SDV2, NO.73

ESD Request 2011.08.13





Screw Holes



Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: TP/KBD/Screw Hole/Debug

Size: C | Document Number: LA-8124P | Rev: 0.4

Date: Monday, January 16, 2012 | Sheet 33 of 50

USB3.0 Conn *3

EVT, No.5

14 USB30_FTX_DRX_N0 — USB30_FTX_DRX_N0 — @R2443 0_0402_5% — USB30_FTX_DRX_N0_L
14 USB30_FTX_DRX_P0 — USB30_FTX_DRX_P0 — @R2442 0_0402_5% — USB30_FTX_DRX_P0_L
14 USB30_FRX_DTX_N0 — USB30_FRX_DTX_N0 — @R2444 0_0402_5% — USB30_FRX_DTX_N0_L
14 USB30_FRX_DTX_P0 — USB30_FRX_DTX_P0 — @R2445 0_0402_5% — USB30_FRX_DTX_P0_L
14 USB30_P10 — USB30_P10 — @R2446 0_0402_5% — USB30_P10_L
14 USB30_N10 — USB30_N10 — @R2447 0_0402_5% — USB30_N10_L

14 USB30_FTX_DRX_N1 — USB30_FTX_DRX_N1 — @R2448 0_0402_5% — USB30_FTX_DRX_N1_L
14 USB30_FTX_DRX_P1 — USB30_FTX_DRX_P1 — @R2449 0_0402_5% — USB30_FTX_DRX_P1_L
14 USB30_FRX_DTX_N1 — USB30_FRX_DTX_N1 — @R2450 0_0402_5% — USB30_FRX_DTX_N1_L
14 USB30_FRX_DTX_P1 — USB30_FRX_DTX_P1 — @R2452 0_0402_5% — USB30_FRX_DTX_P1_L
14 USB30_P11 — USB30_P11 — @R2451 0_0402_5% — USB30_P11_L
14 USB30_N11 — USB30_N11 — @R2453 0_0402_5% — USB30_N11_L

14 USB30_FTX_DRX_N2 — USB30_FTX_DRX_N2 — @R2454 0_0402_5% — USB30_FTX_DRX_N2_L
14 USB30_FTX_DRX_P2 — USB30_FTX_DRX_P2 — @R2455 0_0402_5% — USB30_FTX_DRX_P2_L
14 USB30_FRX_DTX_N2 — USB30_FRX_DTX_N2 — @R2457 0_0402_5% — USB30_FRX_DTX_N2_L
14 USB30_FRX_DTX_P2 — USB30_FRX_DTX_P2 — @R2456 0_0402_5% — USB30_FRX_DTX_P2_L
14 USB30_P12 — USB30_P12 — @R2458 0_0402_5% — USB30_P12_L
14 USB30_N12 — USB30_N12 — @R2459 0_0402_5% — USB30_N12_L

For EMI request

L2400 WCM-2012HS-900T_4P: USB30_FTX_DRX_P0 → USB30_FTX_DRX_P0_L; USB30_FTX_DRX_N0 → USB30_FTX_DRX_N0_L
L2401 WCM-2012HS-900T_4P: USB30_FRX_DTX_P0 → USB30_FRX_DTX_P0_L; USB30_FRX_DTX_N0 → USB30_FRX_DTX_N0_L
L2402 WCM-2012-670T_4P: USB30_P10 → USB30_P10_L; USB30_N10 → USB30_N10_L

For EMI request

L2403 WCM-2012HS-900T_4P: USB30_FTX_DRX_N1 → USB30_FTX_DRX_N1_L; USB30_FTX_DRX_P1 → USB30_FTX_DRX_P1_L
L2404 WCM-2012HS-900T_4P: USB30_FRX_DTX_N1 → USB30_FRX_DTX_N1_L; USB30_FRX_DTX_P1 → USB30_FRX_DTX_P1_L
L2405 WCM-2012-670T_4P: USB30_P11 → USB30_P11_L; USB30_N11 → USB30_N11_L

For EMI request

L2406 WCM-2012HS-900T_4P: USB30_FTX_DRX_N2 → USB30_FTX_DRX_N2_L; USB30_FTX_DRX_P2 → USB30_FTX_DRX_P2_L
L2407 WCM-2012HS-900T_4P: USB30_FRX_DTX_N2 → USB30_FRX_DTX_N2_L; USB30_FRX_DTX_P2 → USB30_FRX_DTX_P2_L
L2408 WCM-2012-670T_4P: USB30_P12 → USB30_P12_L; USB30_N12 → USB30_N12_L

LP1

D2404 TVWDF1004AD0_DFN9: USB30_FRX_DTX_N0_L → USB30_FRX_DTX_N0_L; USB30_FRX_DTX_P0_L → USB30_FRX_DTX_P0_L; USB30_FTX_DRX_N0_L → USB30_FTX_DRX_N0_L; USB30_FTX_DRX_P0_L → USB30_FTX_DRX_P0_L

D2405 AZC099-04S.R7G_SOT23-6: USB30_P10_L → USB30_N10_L; +5VALW

+USB3_VCCA — 150U_B2_6.3VM_R55M C2473 — 470P_0402_50V7K C2474

JUSB3 ACON_TARA4-9K1311 CONN@: USB30_FTX_DRX_P0_L, USB30_FTX_DRX_N0_L, USB30_P10_L, USB30_N10_L, USB30_FRX_DTX_P0_L, USB30_FRX_DTX_N0_L

+USB3_VCCA W=80mils

+5VALW — C2475 0.1U_0402_16V4Z — U2404 G5471P81U_MSOP8 Low Active: USB_ON# 4 ← 31 USB_ON#; +USB3_VCCA W=80mils; R2487 10K_0402_5% → USB_OC0# 14; C2476 0.1U_0402_16V4Z

LP2

D2406 TVWDF1004AD0_DFN9: USB30_FRX_DTX_N1_L → USB30_FRX_DTX_N1_L; USB30_FRX_DTX_P1_L → USB30_FRX_DTX_P1_L; USB30_FTX_DRX_N1_L → USB30_FTX_DRX_N1_L; USB30_FTX_DRX_P1_L → USB30_FTX_DRX_P1_L

D2407 AZC099-04S.R7G_SOT23-6: USB30_P11_L → USB30_N11_L; +5VALW

+USB3_VCCA W=80mils

JUSB2 ACON_TARA4-9K1311 CONN@: USB30_FTX_DRX_P1_L, USB30_FTX_DRX_N1_L, USB30_P11_L, USB30_N11_L, USB30_FRX_DTX_P1_L, USB30_FRX_DTX_N1_L

+5VALW — C2477 0.1U_0402_16V4Z — U2405 G5471P81U_MSOP8 Low Active: USB_ON# 4; +USB3_VCCB W=80mils; R2488 10K_0402_5% → USB_OC1# 14; C2480 0.1U_0402_16V4Z

+USB3_VCCA — 150U_B2_6.3VM_R55M C2478 — 470P_0402_50V7K C2479

LP3

D2408 TVWDF1004AD0_DFN9: USB30_FRX_DTX_N2_L → USB30_FRX_DTX_N2_L; USB30_FRX_DTX_P2_L → USB30_FRX_DTX_P2_L; USB30_FTX_DRX_N2_L → USB30_FTX_DRX_N2_L; USB30_FTX_DRX_P2_L → USB30_FTX_DRX_P2_L

D2409 AZC099-04S.R7G_SOT23-6: USB30_P12_L → USB30_N12_L; +5VALW

+USB3_VCCB W=80mils

JUSB1 ACON_TARA4-9K1311 CONN@: USB30_FTX_DRX_P2_L, USB30_FTX_DRX_N2_L, USB30_P12_L, USB30_N12_L, USB30_FRX_DTX_P2_L, USB30_FRX_DTX_N2_L

Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

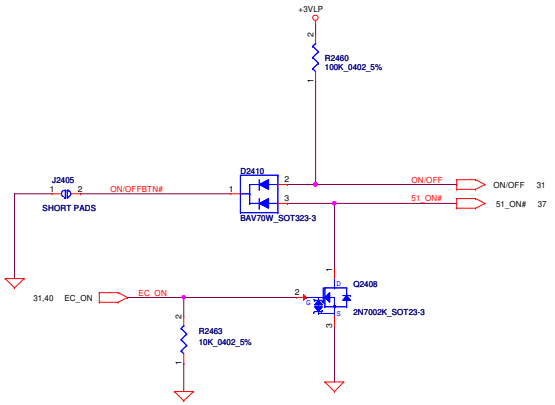
Compal Electronics, Inc.

Title: USB 3.0 Conn

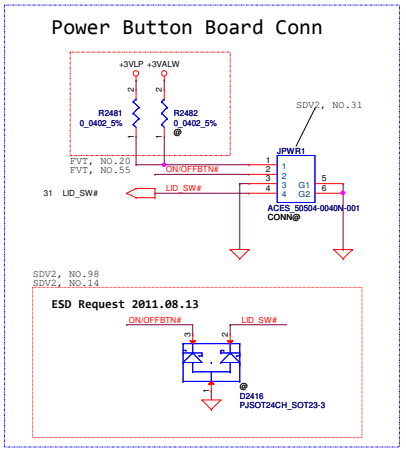
Size: C | Document Number: LA-8121P | Rev: 0.4

Date: Monday, January 16, 2012 | Sheet 34 of 50

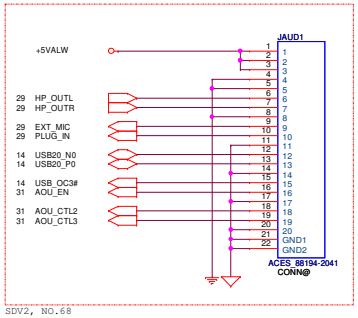
ON/OFF switch



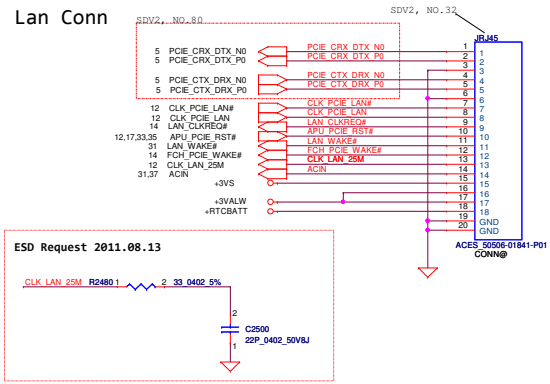
Power Button Board Conn



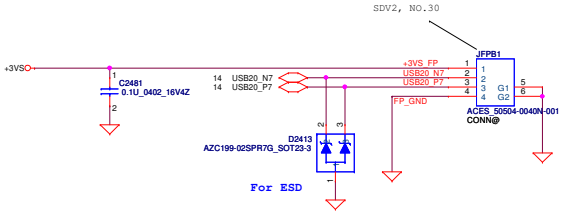
USB2.0/Audio Jack SB CONN



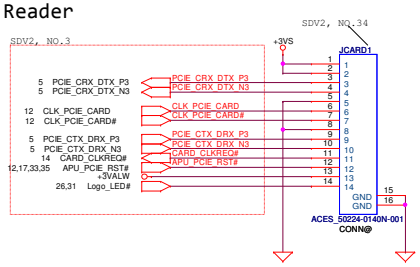
Lan Conn



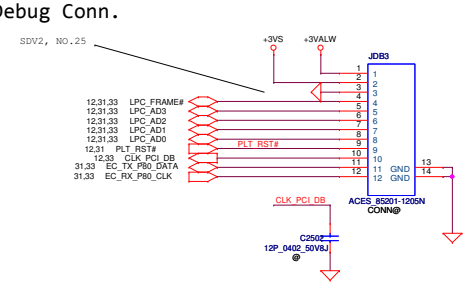
Finger Printer



Card Reader



Debug Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

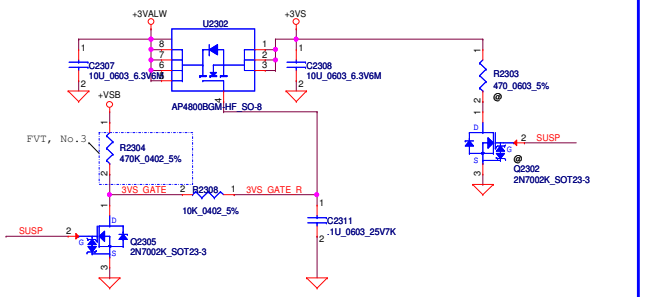
Compal Electronics, Inc.

Title: Sub Board

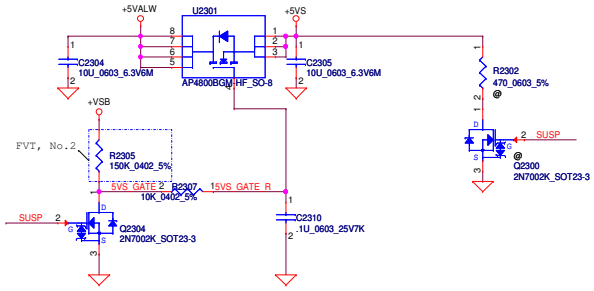
Size: Custom | Document Number: LA-8121P | Rev: 0.4

Date: Monday, January 16, 2012 | Sheet 35 of 50

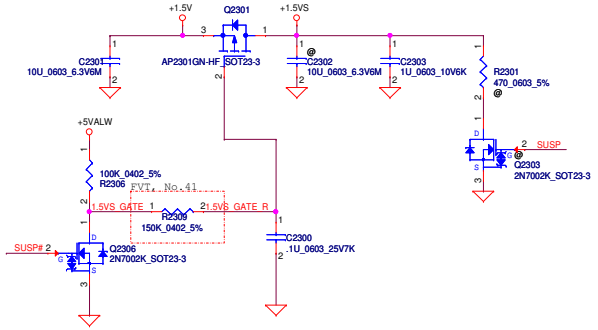
+3VALW TO +3VS



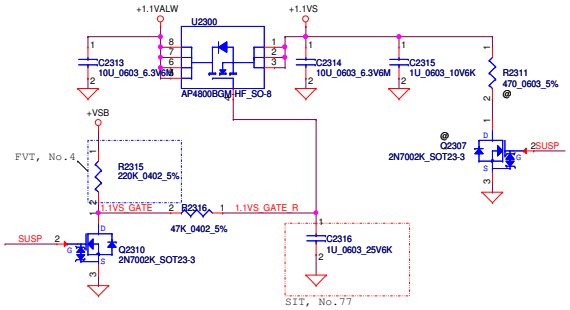
+5VALW TO +5VS



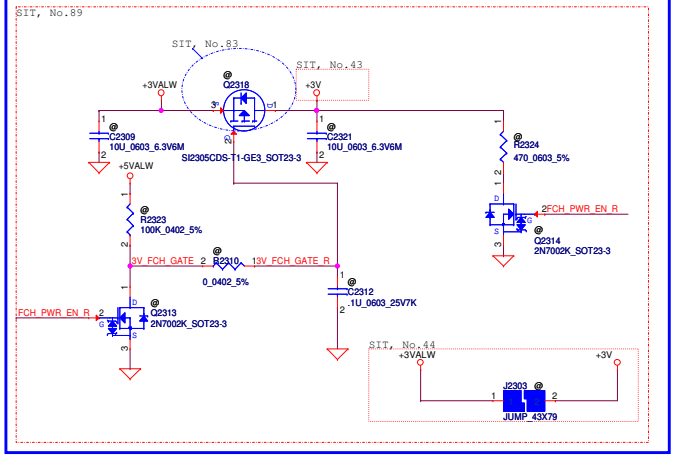
+1.5V to +1.5VS



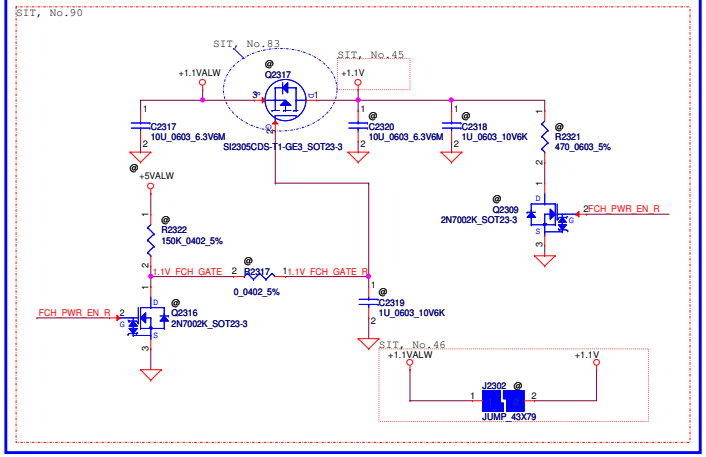
+1.1VALW to +1.1VS

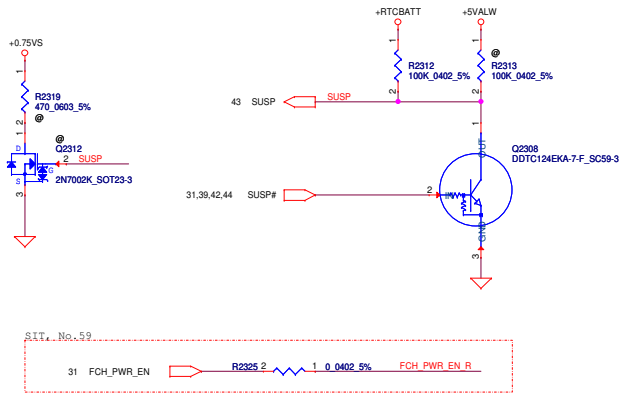


+3VALW TO +3V



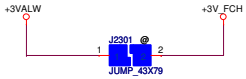
+1.1VALW to +1.1V





+3VALW TO +3V_FCH

Short J2301 for PCH VCCSUS3.3



Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: DC_V_TO_VS_INTERFACE

Size	Document Number	Rev
C	LA-8121P	0.4

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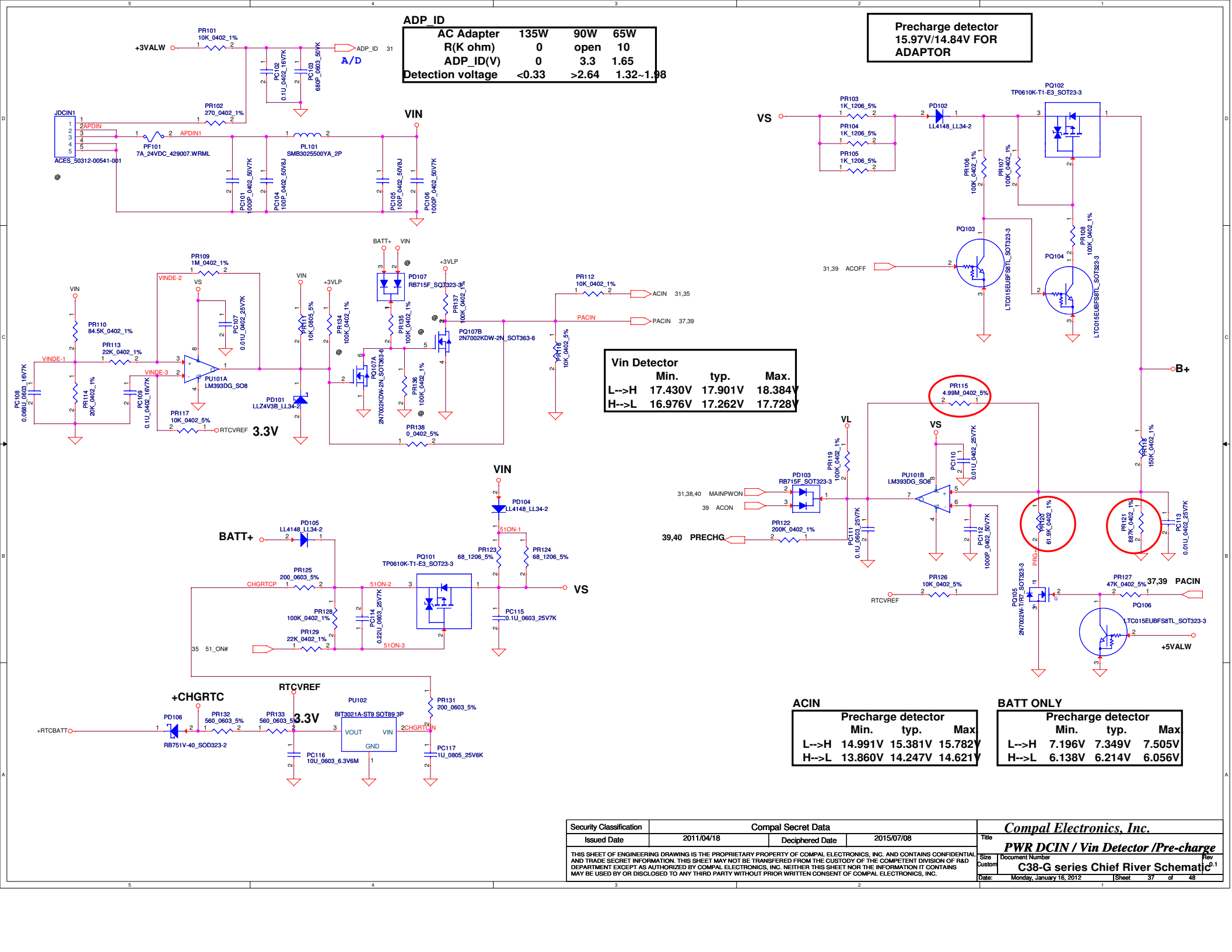
ADP_ID
AC Adapter 135W 90W 65W
R(K ohm) 0 open 10
ADP_ID(V) 0 3.3 1.65
Detection voltage <0.33 >2.64 1.32~1.98
Precharge detector
15.97V/14.84V FOR
ADAPTOR
Vin Detector
Min. typ. Max.
L-->H 17.430V 17.901V 18.384V
H-->L 16.976V 17.262V 18.728V
ACIN
Precharge detector
Min. typ. Max
L-->H 14.991V 15.381V 15.782V
H-->L 13.860V 14.247V 14.621V
BATT ONLY
Precharge detector
Min. typ. Max
L-->H 7.196V 7.349V 7.505V
H-->L 6.138V 6.214V 6.056V
+3VALW
ADP_ID
A/D
VIN
VS
VL
B+
BATT+
+3VLP
+CHGRTC
RTCVREF
3.3V
+5VALW
+RTCBATT
MAINPWON
ACON
PRECHG
ACOFF
PACIN
CHGRTCP
51_ON#
Security Classification
Compal Secret Data
Issued Date
2011/04/18
Deciphered Date
2015/07/08
Compal Electronics, Inc.
PWR DCIN / Vin Detector /Pre-charge
C38-G series Chief River Schematic
Monday, January 16, 2012
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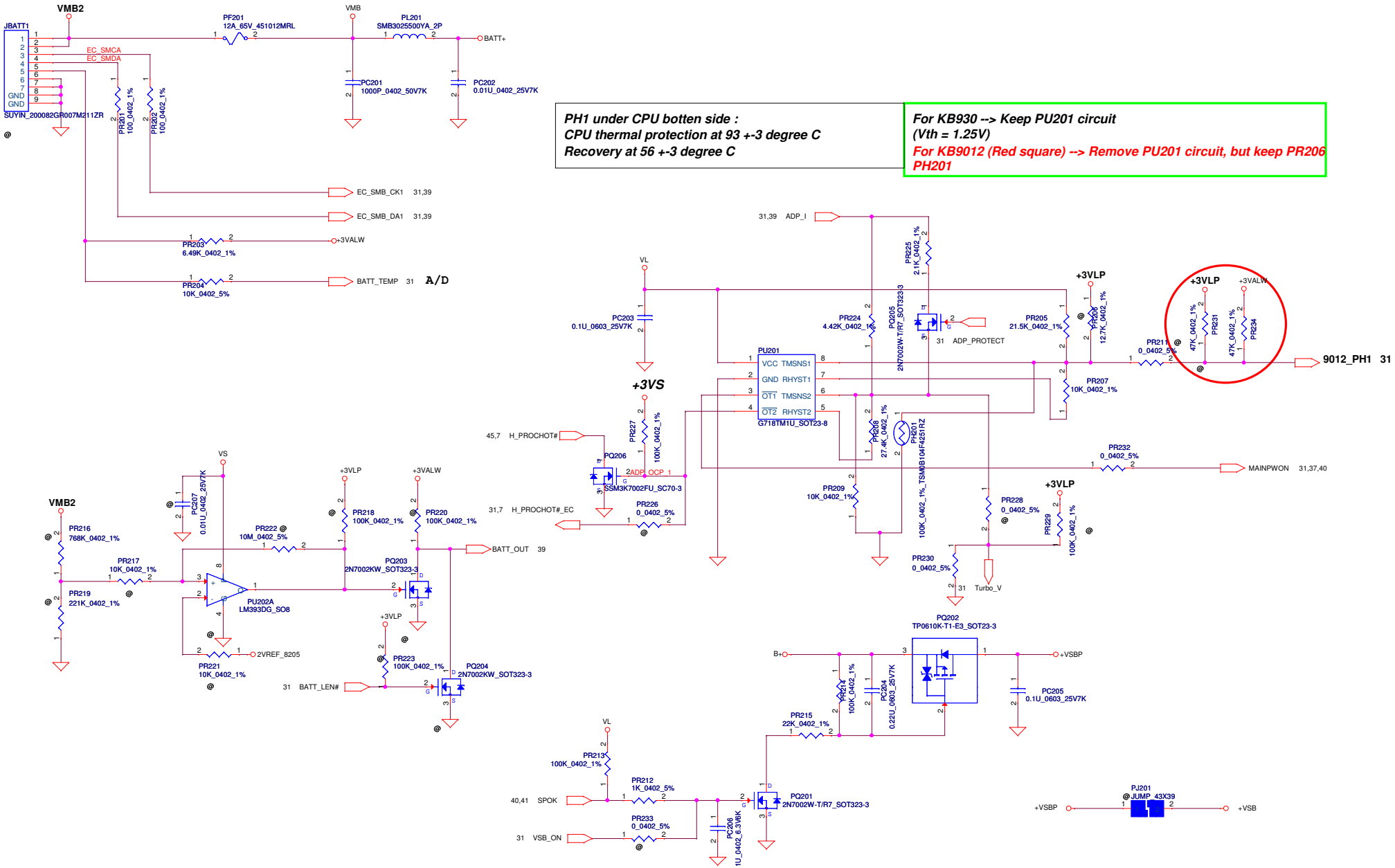


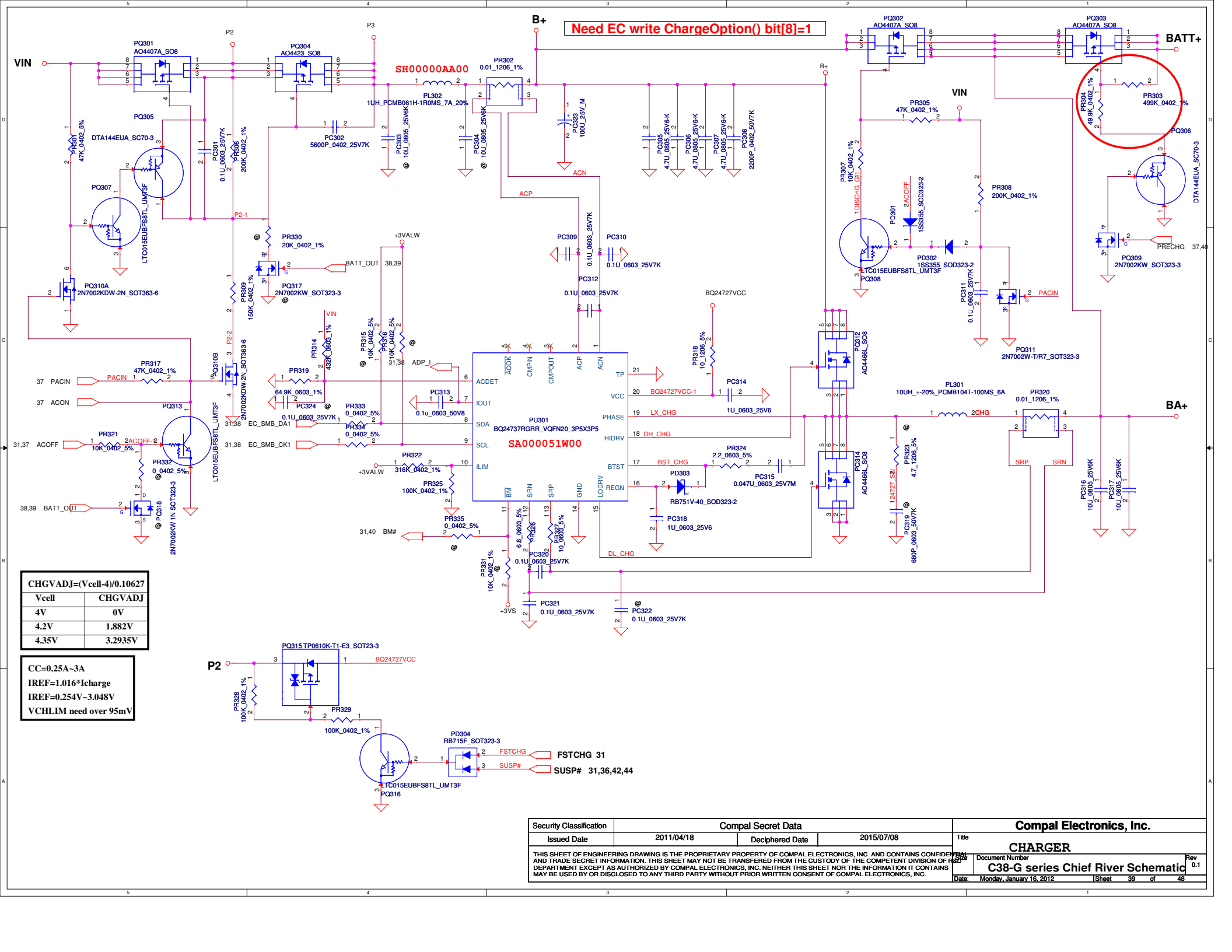
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Monday, January 16, 2012 | Sheet 38 of 48



Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

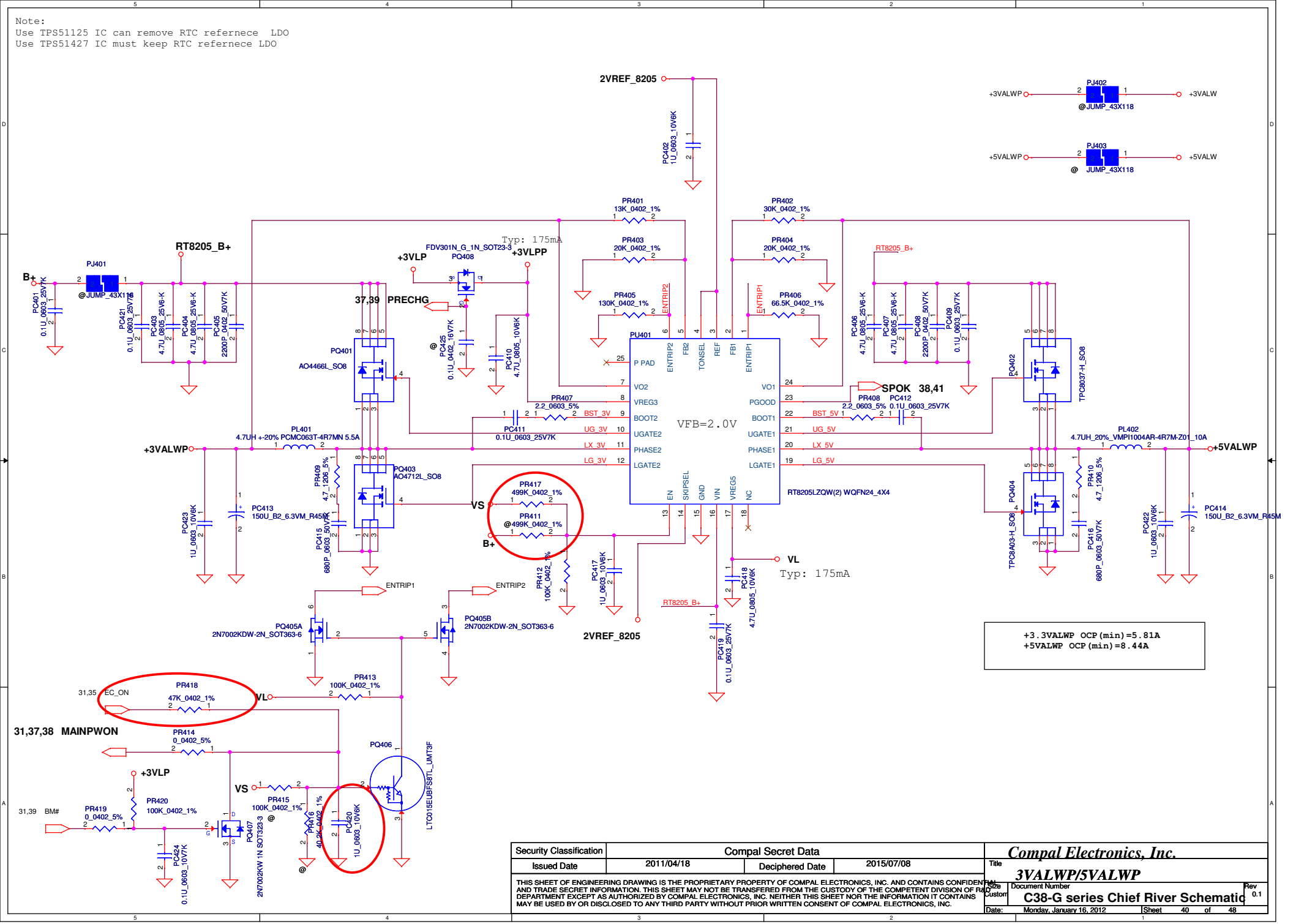
Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Monday, January 16, 2012 | Sheet 39 of 48

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



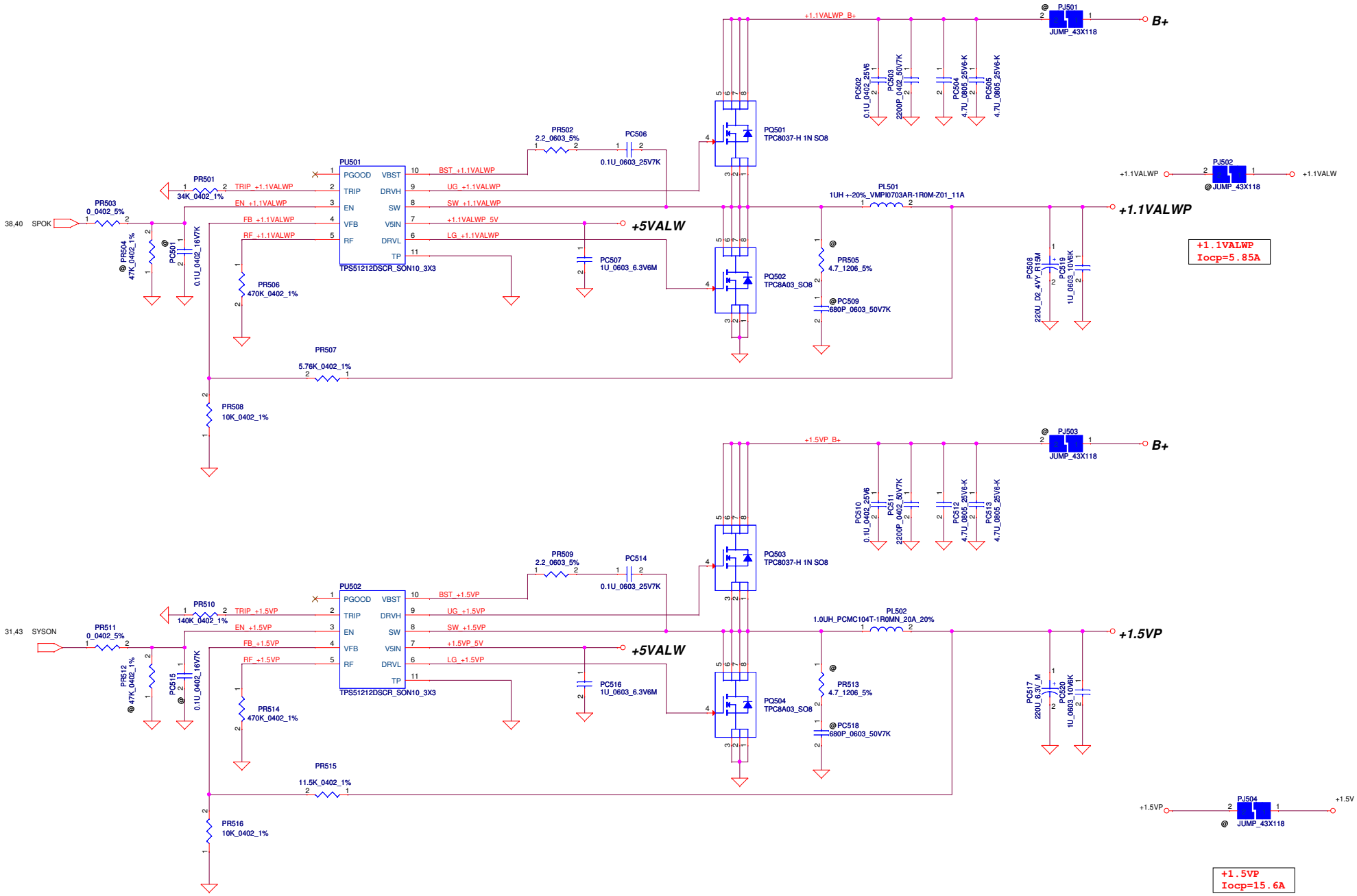
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Monday, January 16, 2012 | Sheet 40 of 48



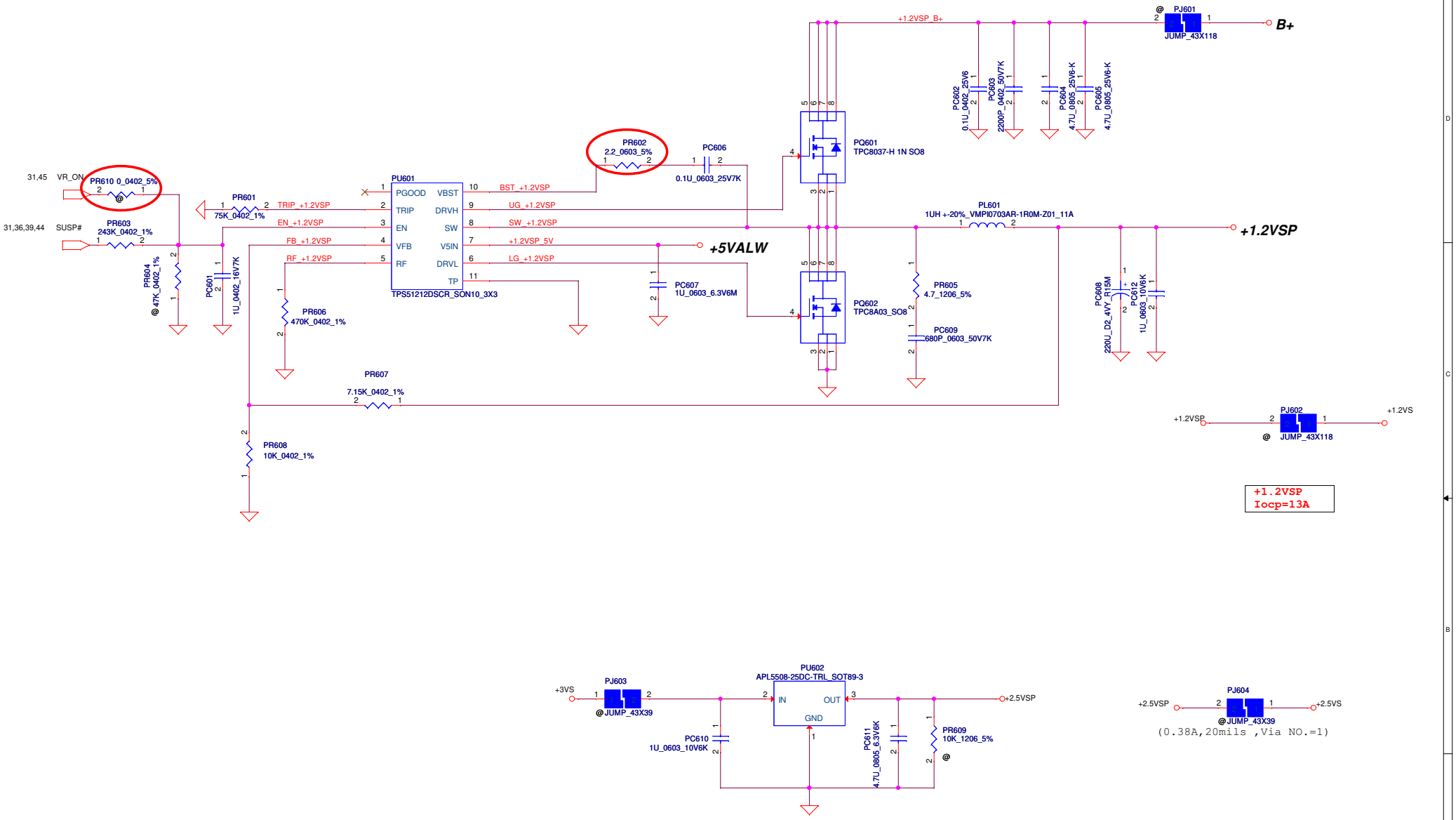
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	

Compal Electronics, Inc.

Title: **+1.1VALWP/+1.5VP**

Size	Document Number	Rev
		0.1

Date: Monday, January 16, 2012 | Sheet 41 of 48



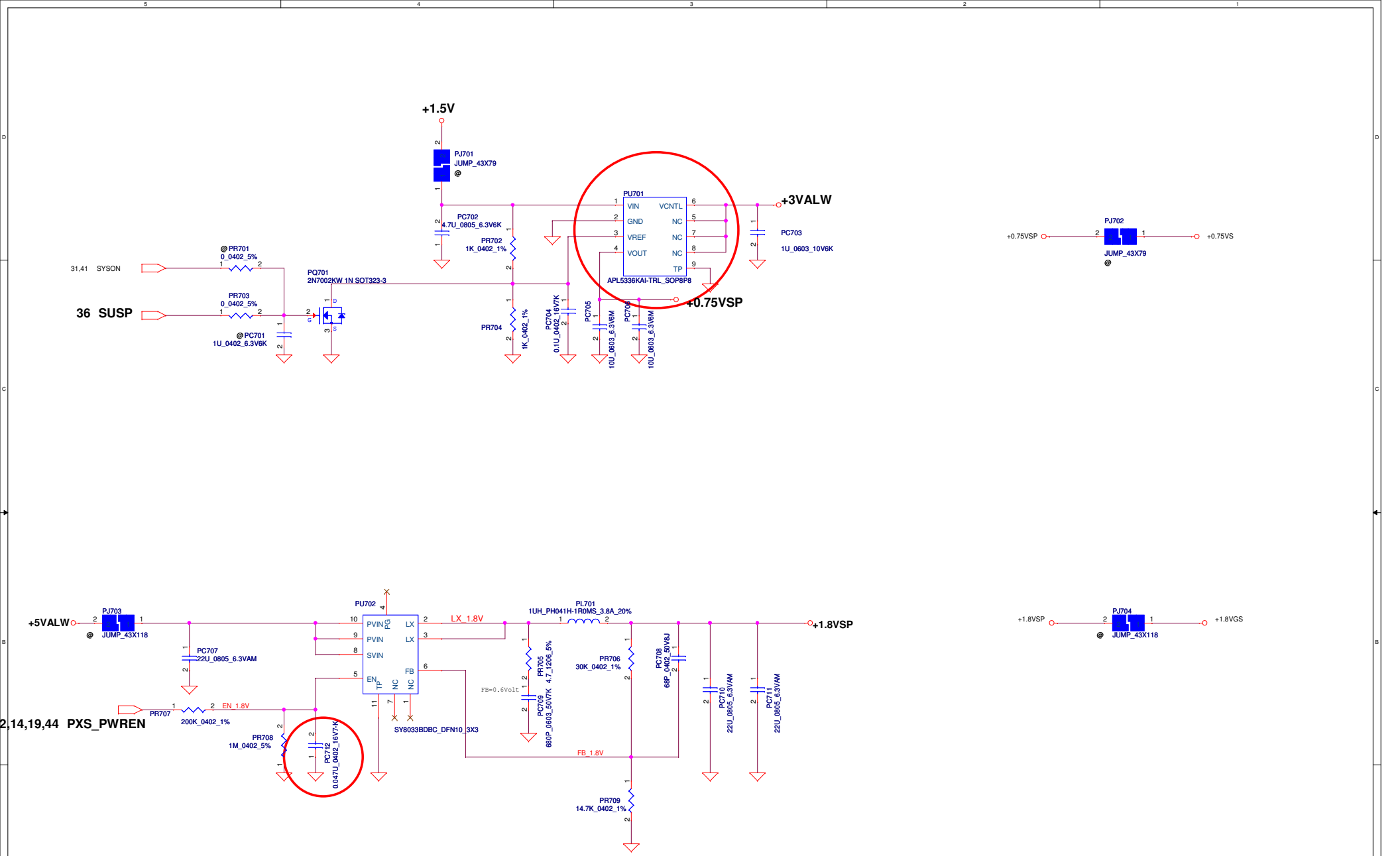
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	

Compal Electronics, Inc.

Title: **+1.2VSP/+2.5VSP**

Size	Document Number	Rev
		0.1

Date: Monday, January 16, 2012 Sheet 42 of 48



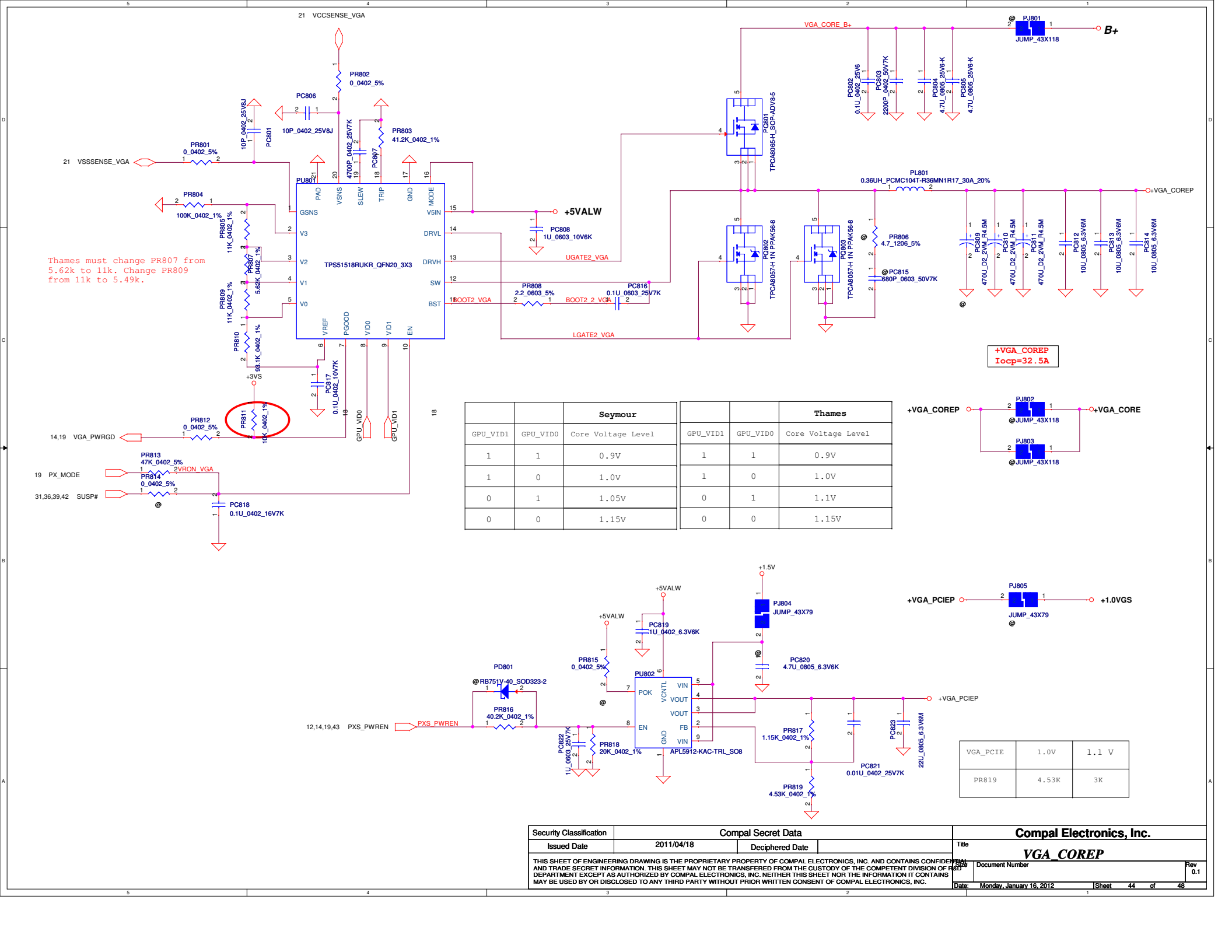
Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	

Compal Electronics, Inc.

Title: **+0.75VP/+1.8VP**

Size	Document Number	Rev
		0.1

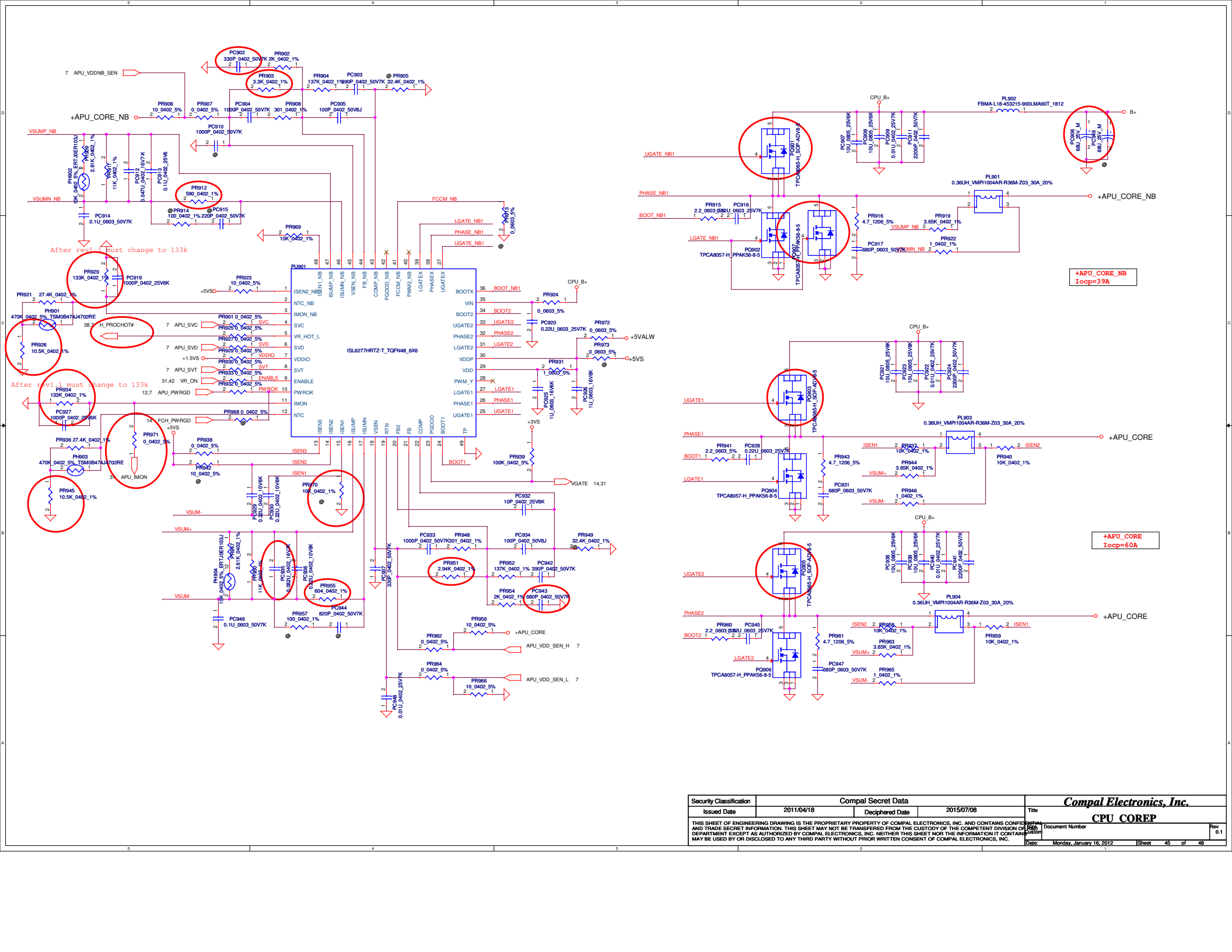
Date: Monday, January 16, 2012 | Sheet 43 of 48



		Seymour			Thames
GPU_VID1	GPU_VID0	Core Voltage Level	GPU_VID1	GPU_VID0	Core Voltage Level
1	1	0.9V	1	1	0.9V
1	0	1.0V	1	0	1.0V
0	1	1.05V	0	1	1.1V
0	0	1.15V	0	0	1.15V

VGA_PCIE	1.0V	1.1 V
PR819	4.53K	3K

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/04/18	Deciphered Date	Title: VGA_COREP
Size	Document Number		Rev: 0.1
Date: Monday, January 16, 2012	Sheet 44 of 48		

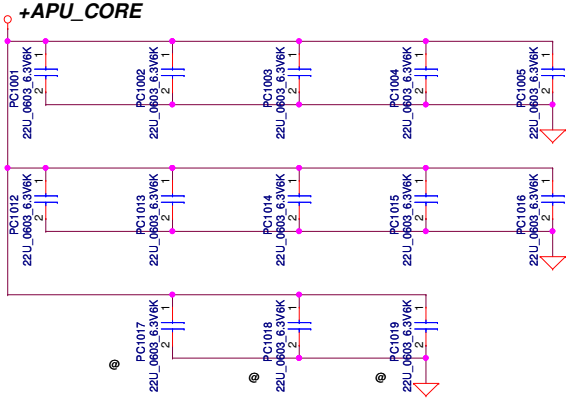


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/04/18	Deciphered Date	2015/07/08
			Title: CPU_COREP

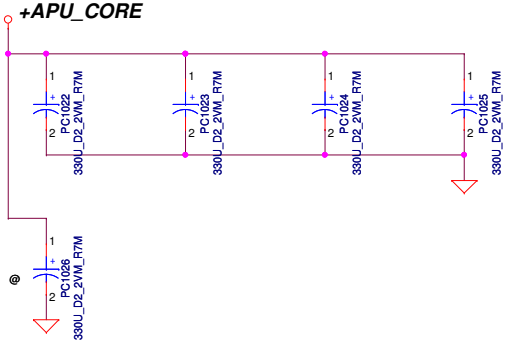
Size: Custom	Document Number		Rev: 0.1
Date: Monday, January 16, 2012	Sheet 45 of 48		

+CPU_CORE

+APU_CORE

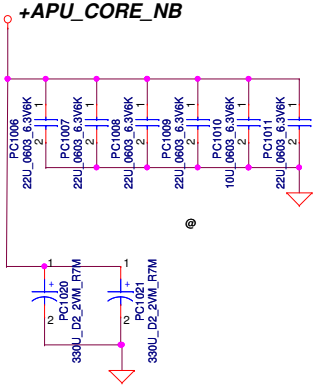


+APU_CORE

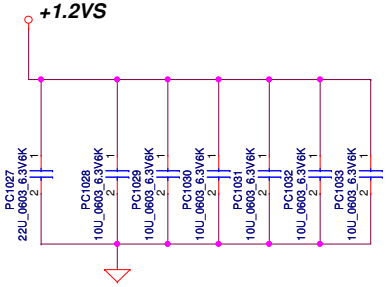


+CPU_CORE_NB

+APU_CORE_NB



+1.2VS



+1.2VS

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/04/18	Deciphered Date	Title: PROCESSOR DECOUPLING
Size: A3	Document Number		Rev: 0.1
Date: Monday, January 16, 2012	Sheet 46 of 48		

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					

Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Monday, January 16, 2012 | Sheet 47 of 48

Phase	Date	No.	BOM	Sch	Layout	Description
SDV2	2011/09/13	No.1	V			Page29, install R1102, R1104, R1105 for audio noise prevention
	2011/09/14	No.2	V			page12~16, change FCH P/N from SA000043IC0 to SA000043IG0
	2011/09/16	No.3	V	V		Page35, Swap JCARD1 Pin3,4 to Pin9,10 PCIE TX & RX for CardReader no function issue
	2011/09/16	No.4	V	V		Page33, Modify JTP1 Pin1 to TP_DATA2, JTP1 Pin6 to TP_CLK2 for Click Pad no function issue
	2011/09/17	No.5	V	V		Page30, Modify JHDD1 Pin18 connect to GND for SATA Gen2
	2011/09/17	No.6	V			Page5~9, Modify U1 to JCPU1
	2011/09/17	No.7	V			Page10~11, SWAP JDIMM1 & JDIMM2
	2011/09/17	No.8	V			Page33, Modify JFP1 to JFPB1,Modify JWLAN1 to JMINI1,Modify JLAN1 to JRJ45
	2011/09/17	No.9	V			Page12, Modify CLRP1 to JCMOS1
	2011/09/26	No.10	V			Page31, POP U2201,C2200,R2229 for Security ROM Function not work issue
	2011/09/26	No.11	V			Page14, Modify D1103,D1104 to DIS@ for DIS only
D	2011/09/28	No.12	V		V	Page33, Reserve R2489,R2490 with PCIE_CRX_C_DTX_N1,PCIE_CRX_C_DTX_P1 for PCIE WLAN RX AC Decouping
	2011/09/28	No.13		V	V	Page29, R1111.2 Connect to U1101 Pin38 add net name CX_GPIO0 for vendor request
	2011/09/28	No.14	V	V	V	Page35, Add D2416 to replace D2414 for ESD request
	2011/09/28	No.15		V	V	Page5~9, Modify JCPU1 Footprint to LOTES_ACA-ZIF-109_722P-A39 for A39 DFX Rule
	2011/09/28	No.16		V	V	Page12~16, Modify U2 Footprint to 21807-A11-HUDSON_FCBGA_656P-A39 for A39 DFX Rule
	2011/09/28	No.17		V	V	Page17~22, Modify U1401 Footprint to 2160809000A11SEY_FCBGA_962P-A39 for A39 DFX Rule
	2011/09/28	No.18		V	V	Page23~24, Modify U1405~U1412 Footprint to K4W1G1646E-HC12_FBGA_96P-A39 for A39 DFX Rule
	2011/09/28	No.19	V	V		Page31, Modify Board ID Table for AMD Build Plan Change
	2011/09/28	No.20	V	V		Page31, Modify R2209 for QALEA FVT1 Build Board IC Mapping
	2011/09/28	No.21		V	V	Page14 & 31, U2200 Pin107 add EC_PXCONTROL connect to D1103.1 , D1104.1 for PX control enable delay
	2011/09/30	No.22				Page28, update JCRT1 Footprint from SUYIN_070546FR015S200ZR_15P to C-H_13-12201558CP_15P-T for ME Conn modify
	2011/10/03	No.23	V			Page14, D1103 modify to UNPOP for VGA Sequence Tuning
	2011/10/04	No.24	V	V	V	Page14, Add C222~C237 connect to all USB2.0 port near connector for AMD request that about USB Signal Driving
	2011/10/05	No.25	V	V	V	Page35, Add JDB3 Conn for SW Debug request
	2011/10/05	No.26		V	V	Page17, Add TP57~T58 on U2 GPIO input pin for debug
	2011/10/05	No.27		V	V	Page13, Add TP59~T61, TP67~T74 on U2 GPIO input pin for debug
	2011/10/05	No.28		V	V	Page14, Add TP62~T93 on U2 GPIO input pin for debug
	2011/10/06	No.29	V	V		Page26, Q2101 P/N change to SB00007H10 for Component common
	2011/10/06	No.30		V	V	Page35, JFPB1 update P/N to SP01000Z300 for Conn List update
	2011/10/06	No.31		V	V	Page35, JPWR1 update P/N to SP01000Z300 for Conn List update
	2011/10/06	No.32		V	V	Page35, JRJ45 update Footprint to ACES_50506-01841-P01_18P-T for Conn List update
	2011/10/06	No.33		V	V	Page32, JBT1 update P/N to SP02000TF00 for Conn List update
	2011/10/06	No.34		V	V	Page35, JCARD1 update Footprint to ACES_50224-0140N-001_14P-T for Conn List update
	2011/10/07	No.35	V	V	V	Page29, reserve D1101 for Audio Noise issue
	2011/10/11	No.36		V	V	Page12, Del TP52~T58 on U2 GPIO input pin for debug
	2011/10/11	No.37		V	V	Page13, Del TP59~T61, TP67~T74 on U2 GPIO input pin for debug
	2011/10/11	No.38		V	V	Page14, Add TP62~T93 on U2 GPIO input pin for debug
	2011/10/12	No.39	V			Page22, Replace R1476 P/N From DD28100A000 to SD028100A80 for HF Part modify
	2011/10/12	No.40	V			Page19,30,36, Replace Q1409,Q2309,Q2410 P/N From SBX01240010 to SB00000J700 for HF Part modify
	2011/10/13	No.41	V		V	Page12, Replace X1 P/N From SJ100003300 to SJ10000EL00 for Sourcer request (No Footprint, Use SJ10000DJ00)
	2011/10/13	No.42	V		V	Page12, Replace Y1 P/N From SJ132P7KW10 to SJ10000BM00 for Sourcer request
	2011/10/13	No.43	V		V	Page18, Replace Y1400 P/N From SJ100006R00 to SJ10000DY00 for Sourcer request (No Footprint, Use SJ10000DJ00)
	2011/10/13	No.44	V			Page31, Replace Y2200 P/N From SJ132P7KW10 to SJ10000BM00 for Sourcer request
	2011/10/13	No.45	V	V	V	Page31, Modify U2200 Pin107 EC_PXCONTROL to U2200 Pin108 for ABO Common Design
	2011/10/14	No.46	V	V	V	Page31, Add R2215 pull up to +3VS for H_PROCHOT#_EC
	2011/10/14	No.47	V			Page19, Replace Q1401,Q1402,Q1404,Q1405 P/N from SB00000FG00 to SB00000FG10 for Sourcer request
	2011/10/17	No.48	V	V	V	Page26, Add C2144,C2145 1000P Caps connect to DMIC_CLK & DMIC_1_2 for EMI Request(Noise issue)
	2011/10/17	No.49	V	V	V	Page25, Add R2171 connect to LVDS_HPD_R for Vendor Request (Noise Filtering)
	2011/10/17	No.50	V			Page7.9,27 Replace Q2,Q3,Q8,Q2106 P/N From SB000006A00 to SB000006A10 for HF Part modify
	2011/10/17	No.51	V	V	V	Page14, Del D1103,D1104, Add Q44,R211 & use EC_Control to Control PXS_PWREN ON/OFF Timing for VGA Sequence tuning
	2011/10/17	No.52	V			Page19, Modify C1463,D1400,R1442 BOM Structure from DIS@ to PX40 & D1400 use 0_0603_5% for PX50
	2011/10/17	No.53	V			Page7, Modify R65,R69 BOM Structure to @ for Power Leakage issue
	2011/10/17	No.54	V			Page12, Modify R80,R82 value from 0 ohm to 33 ohm for EMI Noise Issue
	2011/10/18	No.55		V		Page7, 31, Modify input/output direction: H_PROCHOT#, Turbo_V
	2011/10/18	No.56		V	V	Page27, Add Net +5VS_HDMI on D2103 Pin5 & Pin6 For ESD Request
	2011/10/18	No.57	V			Page19, Modify R1454,Q1412,R1450,R1451,R1449,C1470,U1404,C1467,C1468,C1469,C1470 BOM Structure from PX40 to DIS@ for PX50 Function workable
	2011/10/19	No.58		V	V	Page31, Add Net APU_IMON on U2200 Pin76 for Power Team Request
	2011/10/19	No.59		V		Page35, Add intersheet of PLT_RST# on debug card
	2011/10/19	No.60		V	V	Page25, modify net name: LVDS_HPD_R to LVDS_HPD_C
	2011/10/20	No.61	V	V	V	Page33, Del AOAC circuit for Customer request
	2011/10/20	No.62		V	V	Page31, Del AOAC Powe Control Pin WLAN_POWER# for Customer request
	2011/10/20	No.63		V		Page14, Modify USB Signal net name from USB20_[P..N][10..12]_C to USB30_[P..N][10..12]_C for USB30 net name error
	2011/10/21	No.64	V			Page12, Modify R83,R84 value from 0 ohm to 33 ohm for EMI Noise Issue
	2011/10/21	No.65	V			Page31, Modify R2212,R2213 BOM Structure to @ for ENE Suggestion
	2011/10/21	No.66		V	V	Page31, Modify U2200 Pin 72 Net Name From AOU_ILIM to SPK_RT_Detect# for Speaker main stream & retail
	2011/10/21	No.67	V	V	V	Page31, Add R2236 pul up to +3VS for SPK_RT_Detect#
	2011/10/21	No.68		V	V	Page35, Modify JAUD1 Pin20 Net Name From AOU_ILIM to GND , Pin17 From AOU_CTL1 to GND ,Pin4 From NC to AGNDfor USB Charger Function
	2011/10/21	No.69	V	V	V	Page29, Modify JSPK1 P/N From DC030008W00 to SP02000N000 & Add JSPK1 Pin5 connect to SPK_RT_Detect#,JSPK1 Pin6 connect to GND for Speaker main stream & retail
	2011/10/21	No.70		V	V	Page31, Modify U2200 Pin120 Net Name From AOU_CTL1 to NC for USB Charger Function1
	2011/10/24	No.71	V	V	V	Page29, reserve D1102 for Audio Noise issue
	2011/10/24	No.72	V			Page35, Modify D2415 BOM Structure to POP for ESD Request
	2011/10/24	No.73	V			Page33, Modify D2402,D2403 BOM Structure to POP for ESD Request
	2011/10/24	No.74	V			Page34, Modify D2402,D2403 BOM Structure to POP for ESD Request
B	2011/10/24	No.75	V	V	V	Page28, Add Q2412 with CRT_DDC_DATA & CRT_DDC_CLK for CRT Power Leakage issue
	2011/10/24	No.76	V	V	V	Page26, Del R2116,R2117, Add R2172~R2176 & Reverse D2110 for PWM Power Leakage issue
	2011/10/24	No.77	V	V	V	Page30, Del C2404,Reserve C2471,C2405 for Intel Circuit Common
	2011/10/24	No.78	V			Page32, Modify R500 BOM Structure to @ for BOM Error
	2011/10/24	No.79	V	V	V	Page31, Del R2223~R2229 、Q2200 to update Security ROM Circuit for Intel Circuit Common
	2011/10/24	No.80		V	V	Page35, Swap JRJ45 PCIE_CRX_DTX_P0 to PCIE_CRX_DTX_N0, PCIE_CTX_DRX_P0 to PCIE_CTX_DRX_N0 For LAN Board Common
	2011/10/24	No.81	V	V	V	Page35, Del R2462 to update Power OK circuit for Intel Circuit Common
	2011/10/24	No.82	V	V	V	Page36, Del R2300, R2310, C2312, R2317 update Power OK circuit for Intel Circuit Common
	2011/10/24	No.83	V			Page31, Modify R2235 BOM Structure to @ for H_PROCHOT#_EC
	2011/10/24	No.84	V			Page34, Modify D2404,D2406,D2408 P/N from SC300001D00 to SC300002800 for ESD Request
	2011/10/24	No.85	V			Page34, Modify D2404~D2409,L2400~L2408 BOM Structure from @ to POP for EMC Request
	2011/10/24	No.86	V			Page27, Modify L2105~L2108 BOM Structure from @ to POP for EMI Request
	2011/10/24	No.87	V			Page34, Modify L2402,L2405,L2408 P/N from SC300000I00 to SM070000K00 for ESD Request (Footprint SM070000I00)
	2011/10/24	No.88	V			Page34, Modify L2403, L2404, L2400, L2401, L2406, L2407 P/N from SC300000I00 to SM070001S00 for ESD Request
	2011/10/24	No.89	V			Page27, Modify D2102,D2103,D2105 P/N from SC300001Y00 to SC300002C00 for ESD Request
	2011/10/24	No.90	V			Page35, Modify D2413 P/N from SC600001600 to SCA00001L00 for ESD Request
	2011/10/25	No.91		V	V	Page29, Modify JSPK1 P/N From SP02000N000 to DC030008W00 For LD Requirement
	2011/10/25	No.92	V	V	V	Page29, Add R1140 connect to SPK_RT_Detect# to GND for Speaker Verify
	2011/10/25	No.93	V	V	V	Page28, Del Q2412 with CRT_DDC_DATA & CRT_DDC_CLK for AMD Design Guide Require
	2011/10/26	No.94	V	V	V	Page26, Del R2122,R2124 with EDID_DATA & EDID_CLK pull up for Duplicate Pull up error
	2011/10/26	No.95	V			Page26, Modify R2174 BOM Structure to @ for BOM Error
	2011/10/26	No.96	V	V	V	Page25, Reserve R2116, R2117 to Connect from CSCL & CSCA to EC_SMB_DA2 & EC_SMB_CK2 for Power Leakage issue
	2011/10/26	No.97	V			Page29, Modify D1101, D1102 BOM Structure From @ to POP for Audio Noise issue
	2011/10/27	No.98	V	V	V	Page35, Modify D2416 P/N from SC300001G00 to SCA00001G00 for ESD Request
	2011/10/27	No.99	V			Page29, Modify C1111 ,C1141 BOM Structure From POP to @ for Audio Noise issue

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2011/03/04

Compal Electronics, Inc.

Title: EE modify list

Size	Document Number	Rev
Custom	LA-7121P	0.4

Date: Monday, January 16, 2012 | Sheet 48 of 50

Phase	Date	No.	BOM	Sch	Layout	Description
FVT	2011/11/14	No.1	V			Page17~24, Modify U1401 P/N From SA000047H00 to SA000047H50 for GPU Version update
	2011/11/14	No.2	V			Page36, Modify R2305 P/N From SD028200280 (20K_0402_5%) to SD028150380 (150K_0402_5%) for Power Consumption & Power Sequence tuning
	2011/11/14	No.3	V			Page36, Modify R2304 P/N From SD028470280 (47K_0402_5%) to SD028470380 (470K_0402_5%) for Power Consumption & Power Sequence tuning
	2011/11/14	No.4	V			Page36, Modify R2315 P/N From SD028750280 (75K_0402_5%) to SD028220380 (220K_0402_5%) for Power Consumption & Power Sequence tuning
	2011/11/14	No.5	V			Page34, Modify R2442~R2459 BOM Structure From POP to @ for EMI Request
	2011/11/14	No.6	V			Page27, Modify R2126~R2133 BOM Structure From POP to @ for EMI Request
	2011/11/14	No.7	V	V	V	Page14, Replace C222~C237 to R216~R231 on all usb port signal for AMD Design checklist update (USB no function issue)
	2011/11/14	No.8	V	V	V	Page19, Add R1461 to connect PXS_PWREN to RUNPWROK for PX50 Power Enable
	2011/11/14	No.9	V	V		Page30, Modify JODD1 Location to JODD2 for ME BOM Common
	2011/11/14	No.10	V	V	V	Page14,Remove R230~R231 on all usb port signal for AMD Design checklist update (USB no function issue)
	2011/11/15	No.11		V	V	Page35, Remove D2415 for ESD Request
	2011/11/21	No.12	V	V	V	Page30, Reserve R2411,C2421 for G Sensor Vendor Suggestion
	2011/11/21	No.13	V	V	V	Page29, Modify JSPK1 Conn From 4Pin to 6Pin & Move R1140 to connect JSPK1 Pin5 For Speaker main stream & retail
	2011/11/21	No.14	V	V	V	Page31, Add J2200,J2201 to improve EC Power Source +3VLP or +3VALW to +3VALW_EC Power Source Option and modify +3VALW Net Name to +3VALW_EC for Lenovo S4 Lid Function
	2011/11/21	No.15	V	V		Page31, Update Borad ID table for FVT Phase
	2011/11/21	No.16	V	V		Page31, Modify R2209 From 8.2K to 18K for FVT_BRDID update
	2011/11/21	No.17	V			Page30, C2417 BOM Change from 10U (SE000005T80) to 10K (SD013100280) for G Sensor Vendor Suggestion
	2011/11/21	No.18	V	V	V	Page36, Add R2321,R2322,C2317,C2318,C2319,Q2313,Q2314 for +3V_FCH Power Control
	2011/11/21	No.19		V	V	Page31, U2200 Pin70 Add FCH_PWR_EN# for +3V_FCH Power Control
	2011/11/22	No.20	V	V	V	Page35, Add R2481 Pull up to +3VLP & Reserve R2482 Pull up to +3VALW for Lenovo S4 LID Function
	2011/11/22	No.21	V			Page18, Y1400 P/N From SJ10000DY00 to SJ10000CV00 for BOM Change
	2011/11/22	No.22	V			Page12, X1 P/N From SJ10000EL00 to SJ10000CX00 for BOM Change
	2011/11/22	No.23	V	V	V	Page25, Modify R2117 connect to TL_DATA & R2116 connect to TL_CLK, Two signals connect to R2177,R2178 pull up to +3VS for LVDS Translator EEPROM Reserve
	2011/11/22	No.24	V	V	V	Page31, Modify U2200 Pin86 EAPD to TL_DATA & Add U2200 Pin85 TL_CLK for LVDS Translator EEPROM Reserve Function
	2011/11/22	No.25	V	V	V	Page31, Add U2200 Pin26 EAPD_R for LVDS Translator EEPROM Reserve Function
	2011/11/22	No.26	V	V	V	Page31, Add R2223 & R2224 to option EAPD GPIO Output singal from Pin26 (EAPD_R) or Pin86 (TL_DATA) for LVDS Translator EEPROM Reserve Function
	2011/11/23	No.27	V	V	V	Page14, Del R216~R229 for USB2.0 Signals tuneing circuit remove
	2011/11/23	No.28	V	V	V	Page14, Reserve R230~R234 & C222~C226 with USB2.0 N signals port 0,6,10,11,12 for AMD Suggestion
	2011/11/24	No.29	V	V	V	Page36, Del R2321,R2322,C2317,C2318,C2319,Q2313,Q2314 for +3V_FCH Power Control
	2011/11/24	No.30	V	V	V	Page31, U2200 Pin70 Del FCH_PWR_EN# for +3V_FCH Power Control
	2011/11/24	No.31		V	V	Page31, U2200 Pin127 Add VSB_ON & Reserve R2226 for +VSB Power Control
	2011/11/25	No.32		V	V	Page33, Add H18 for ME Drawing lose
	2011/11/25	No.33		V	V	Page31, Modify R2217, R2218 Power Source from +3VS to +3VALW for +3VGS Power Leakage issue
	2011/11/25	No.34	V	V		Page18, Install Q1400, R1427, R1428 & Remove R1433, R1435 for +3VGS Power Leakage issue
	2011/11/25	No.35	V	V	V	Page31, Del R2226 for VSB_ON resistor double reserve
	2011/11/26	No.36	V	V	V	Page31, Add R2226,R2227 Pull up to +3VS & Reserve R2217,R2218 pull up to +3VALW for SMBUS Leakage issue
	2011/11/28	No.37	V	V	V	Page7, Del R65,R69 & Reserve R45 & R45 with APU_SID & APU_SIC By Pass APU_SID_R & APU_SIC_R for SMBUS Power Leakage Issue
	2011/11/28	No.38	V	V	V	Page31, Reserve C2219,C2210 to +3VALW For SMBUS2 AC Decoulping
	2011/11/28	No.39	V	V	V	Page31, Del C2213,C2214 & Modify R2226,R2227 BOM Structure to @ & R2217,R2218 to POP For SMBUS Power Leakage issue
	2011/11/29	No.40	V			Page7, Modify R45,R48 BOM Structure to POP & Q9 to @ For SMBUS Power Leakage issue
	2011/11/29	No.41	V			Page36, Modify R2309 P/N from SD028750180(7.5K) to SD028150380(150K) for Power Sequence tuneing
	2011/11/29	No.42	V			Page36, Modify C2316 P/N from SE042104K80(0.1U) to SE080105K80(1U) for Power Sequence tuneing
	2011/11/29	No.43	V			Page19, Modify R1450 P/N from SD028150380(150K) to SD028130380(130K) for Power Sequence tuneing
	2011/11/29	No.44	V			Page19, Modify C1470 P/N from SE042104K80(0.1U) to SE080105K80(1U) for Power Sequence tuneing
	2011/11/29	No.45	V			Page13, Modify U4 P/N from SA000041P00(MXIC) to SA0003K800(Winbond) for ROM Part Issue
	2011/11/30	No.46	V			Page19, Modify C1470 P/N from SE080105K80(1U) to SE042104K80(0.1U) for Power Sequence tuneing
	2011/11/30	No.47	V			Page19, Modify R1450 P/N from SD028150380(130K) to SD028200280(20K) for Power Sequence tuneing
	2011/11/30	No.48	V			Page19, Modify R1449 P/N from SD028200280(20K) to SD028330380(330K) for Power Sequence tuneing
	2011/11/30	No.49	V			Page35, unmount R2481 and mount R2482 for LID SW function reserved
	2011/12/02	No.50	V			Page12, Modify C129 P/N from SE071150J80 (15P) to SE071220J80 (22P) For Crystal Clock Tuneing
	2011/12/02	No.51	V			Page12, Modify C130 P/N from SE071150J80 (15P) to SE071270J80 (27P) For Crystal Clock Tuneing
	2011/12/02	No.52	V			Page12, Modify C131,C134 P/N from SE071270J80 (27P) to SE071330J80 (33P) For Crystal Clock Tuneing
	2011/12/02	No.53	V			Page18, Modify C1445,C1446 P/N from SE071120J80 (12P) to SE071200JN0 (20P) For Crystal Clock Tuneing
	2011/12/05	No.54	V			Page26, Modify C2144,C2145 BOM Structure to @ for DMIC no function issue
MEMO	2011/12/09	No.55	V			Page35, unmount R2482 and mount R2481 for LID SW function implement when SMT
	2011/12/09	power				power schematics 20110208.dsn

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Phase	Date	No.	BOM	Sch	Layout	Description
SIT	2012/01/03	No.1	V	V	V	Page31, Add R2228 connect from MAINPWON_R to MAINPWON for Power Circuit update
	2012/01/03	No.2	V			Page31, Modify R2236 BOM Structure from POP to @ for +3VS Power Leakage Issue
	2012/01/04	No.3	V	V	V	Page7, delete Q9, short and remove 0 ohm: R45&R48
	2012/01/04	No.4	V	V	V	Page7,9,13, short and remove R64&R68, change Page13 net name ML_VGA_HPD, change page7 net name LVDS_HPD
	2012/01/04	No.5		V	V	Page15, Modify +VDDAN_11_USB_S power source from +1.1VALW to +1.1V_FCH for reduce power consumption
	2012/01/04	No.6		V	V	Page15, Modify +VDDCR_11V_USB power source from +1.1VALW to +1.1V_FCH for reduce power consumption
	2012/01/04	No.7		V	V	Page15, Modify +VDDAN_11_SSUSB & +VDDCR_11_SSUSB power source from +1.1VALW to +1.1V_FCH for reduce power consumption
	2012/01/04	No.8		V	V	Page15, Modify +VDDIO_33_S power source from +3V_FCH to +3VALW for reduce power consumption
	2012/01/04	No.9		V	V	Page15, Modify +VDDXL_3.3V power source from +3V_FCH to +3VALW for reduce power consumption
	2012/01/04	No.10		V	V	Page15, Modify +VDDPL_11_SYS_S power source from +1.1VALW to +1.1V_FCH for reduce power consumption
	2012/01/04	No.11		V	V	Page15, Modify +VDDAN_33_HWM power source from +3V_FCH to +3VALW for reduce power consumption
	2012/01/04	No.12	V	V		Page36, Modify R2314,R2318,R2320,Q2311 BOM Structure from @ to POP for Reduce Power Consumption
	2012/01/04	No.13	V	V	V	Page36, Add Q2313,Q2314,U2304,C2309,C2312,C2321,R2323,R2310,R2324 for +3VALW to +3V_FCH Circuit (Reduce Power Consumption)
	2012/01/04	No.14	V	V	V	Page36, Add Q2316,Q2309,U2303,C2317,C2320,C2318,C2319,R2322,R2317 for +1.1VALW to +1.1V_FCH Circuit (Reduce Power Consumption)
	2012/01/04	No.15	V	V	V	Page14, Remove R146 & R148 for component part reduce
	2012/01/04	No.16	V	V	V	Page7, Remove R207 for component part reduce
	2012/01/04	No.17	V	V	V	Page32, Remove R471 & R472 for component part reduce
	2012/01/04	No.18	V	V	V	Page29, Remove R1106,R1107,R1119,R1134,R1109 for component part reduce
	2012/01/04	No.19	V	V	V	Page35, Remove R2465,R2466 for component part reduce
	2012/01/04	No.20	V	V	V	Page33, Reserve R2483 & R2485 to connect EC_SMB_CK2 & EC_SMB_DA2 for Lenovo Multi-touch function
	2012/01/04	No.21	V	V	V	Page31, Modify EC U2200 111Pin from +3VLP to +3VALW_EC for S4 LID Function (common QILEX)
	2012/01/04	No.22	V	V	V	Page26, Del R2176 to connect to EC_INVPWM for common QILEX
	2012/01/05	No.23	V	V	V	Page14, Add R146 & R148 for component part reduce
	2012/01/05	No.24	V	V	V	Page36, Modify +3V_FCH netname to +3VS_FCH for component part reduce
	2012/01/05	No.25	V	V	V	Page36, Modify +1.1V_FCH netname to +1.1VS_FCH for component part reduce
	2012/01/05	No.26	V	V	V	Page15, Modify +VDDAN_11_USB_S power source from +1.1V_FCH to +1.1VS_FCH for reduce power consumption
	2012/01/05	No.27	V	V	V	Page15, Modify +VDDCR_11V_USB power source from +1.1V_FCH to +1.1VS_FCH for reduce power consumption
	2012/01/05	No.28	V	V	V	Page15, Modify +VDDAN_11_SSUSB & +VDDCR_11_SSUSB power source from +1.1V_FCH to +1.1VS_FCH for reduce power consumption
	2012/01/05	No.29	V	V	V	Page15, Modify +VDDIO_33_S power source from +3VALW to +3VS_FCH for reduce power consumption
	2012/01/05	No.30	V	V	V	Page15, Modify +VDDXL_3.3V power source from +3VALW to +3VS_FCH for reduce power consumption
	2012/01/05	No.31	V	V	V	Page15, Modify +VDDPL_11_SYS_S power source from +1.1V_FCH to +1.1VS_FCH for reduce power consumption
	2012/01/05	No.32	V	V	V	Page15, Modify +VDDAN_33_HWM power source from +3VALW to +3VS_FCH for reduce power consumption
	2012/01/05	No.33	V	V	V	Page29, Remove R1108,R1135,R1110,C1127 for component part reduce
	2012/01/05	No.34	V	V	V	Page31, Remove Pin25 EC_INVT_PWM for Circuit Common
	2012/01/05	No.35	V	V	V	Page31, Modify EC U2200 111Pin from +3VALW_EC to +3VLP for S4 LID Function (common QILEX)
	2012/01/05	No.36	V	V	V	Page36, Modify +3VS_FCH netname to +3V_FCH for component part reduce
	2012/01/05	No.37	V	V	V	Page15, Modify +VDDAN_33_USB power source from +3VS_FCH to +3V_FCH for reduce power consumption
	2012/01/05	No.38	V	V	V	Page15, Modify +VDDPL_33_SSUSB_S power source from +3VS_FCH to +3V_FCH for reduce power consumption
	2012/01/05	No.39	V	V	V	Page15, Modify +VDDPL_33_USB_S power source from +3VS_FCH to +3V_FCH for reduce power consumption
	2012/01/05	No.40	V	V	V	Page15, Modify +VDDIO_33_S power source from +3V_FCH to +3VALW for reduce power consumption
	2012/01/05	No.41	V	V	V	Page15, Modify +VDDAN_33_HWM power source from +3V_FCH to +3VALW for reduce power consumption
	2012/01/05	No.42	V	V	V	Page36, Add J2302 From +1.1VALW to +1.1V_FCH for reduce power consumption
	2012/01/05	No.43	V	V	V	Page36, Modify U2304 Power source from +3V_FCH to +3V for reduce power consumption
	2012/01/05	No.44	V	V	V	Page36, Add J2303 from +3VALW to +3V for reduce power consumption
	2012/01/05	No.45	V	V	V	Page36, Modify U2303 Power source from +1.1V_FCH to +1.1V for reduce power consumption
	2012/01/05	No.46	V	V	V	Page36, Modify J2302 From +1.1V_FCH to +1.1V for reduce power consumption
	2012/01/05	No.47	V	V	V	Page15, Modify +VDDAN_11_USB_S power source from +1.1V_FCH to +1.1V for reduce power consumption
	2012/01/05	No.48	V	V	V	Page15, Modify +VDDCR_11V_USB power source from +1.1V_FCH to +1.1V for reduce power consumption
	2012/01/05	No.49	V	V	V	Page15, Modify +VDDAN_11_SSUSB & +VDDCR_11_SSUSB power source from +1.1V_FCH to +1.1V for reduce power consumption
	2012/01/05	No.50	V	V	V	Page15, Modify +VDDPL_11_SYS_S power source from +1.1V_FCH to +1.1V for reduce power consumption
	2012/01/05	No.51	V	V	V	Page15, Modify +VDDAN_33_USB power source from +3V_FCH to +3V for reduce power consumption
	2012/01/05	No.52	V	V	V	Page15, Modify +VDDPL_33_SSUSB_S power source from +3V_FCH to +3V for reduce power consumption
	2012/01/05	No.53	V	V	V	Page15, Modify +VDDPL_33_USB_S power source from +3V_FCH to +3V for reduce power consumption
	2012/01/05	No.54	V	V	V	Page15, Modify +VDDIO_33_S power source from +3VALW to +3V_FCH for reduce power consumption
	2012/01/05	No.55	V	V	V	Page15, Modify +VDDAN_33_HWM power source from +3VALW to +3V_FCH for reduce power consumption
	2012/01/06	No.56	V	V	V	Page15, Modify +VDDXL_3.3V power source from +3V_FCH to +3V for reduce power consumption
	2012/01/09	No.57	V	V	V	Page33, Add R2493,R2492,R2491,R2494,Q2403,Q2400,C2494,C2493 for AOAC Power Circuit
	2012/01/09	No.58	V	V	V	Page31, U2200 add netname FCH_PWR_EN# on Pin70 for +3V & +1.1V Power Control
	2012/01/09	No.59	V	V	V	Page36, Add R2325 from FCH_PWR_EN# to FCH_PWR_EN#_R for +3V & +1.1V Power Control
	2012/01/09	No.60	V	V	V	Page36, Add FCH_PWR_EN#_R on Q2313.2,Q2314.2,Q2316.2,Q2309.2 for +3V & +1.1V Power Control Enable Option
	2012/01/09	No.61		V	V	Page33, Modify JMINI1 pin1 from FCH_PCIE_WAKE# to WLAN_WAKE# for AOAC Function
	2012/01/09	No.62		V	V	Pgae31, Modify U2200 Pin26 from EAPD_R to WLAN_WAKE# for AOAC Function
	2012/01/09	No.63		V	V	Page31, Add U2200 Pin119 from NC to EAPD_R for Audio Function
	2012/01/09	No.64		V	V	Page31, Add U2200 Pin91 from NC to AOAC_WLAN for AOAC Function
	2012/01/10	No.65		V	V	Page31, Modify U2200 Pin19 net name from ODD_DA# to WL_OFF_EC# for Circuit common with Intel
	2012/01/10	No.66	V	V	V	Page30, Del R2435 for component reduce
	2012/01/10	No.67	V	V	V	Page33, Add R2496 & reserve R2495 for RF_OFF# source option
	2012/01/10	No.68		V	V	Page33, Modify JMINI1 Pin20 net name from WL_OFF# to RF_OFF# for Circuit common with Intel
	2012/01/10	No.69	V			Page31, Modify R2205 BOM Structure to @ for Common Circuit with Intel
	2012/01/10	No.70	V	V	V	Page31, Modify R2232,R2230 from 10K to 100K & Modify R2202,R2230,R2232 pull up from +3VALW_EC to +3VALW for Common Circuit with Intel
	2012/01/11	No.71		V	V	Page31, Modify L2200.1 Power Source from +3VALW to +3VALW_EC for EC_AVCC Power Leakage Issue
	2012/01/11	No.72		V		Page31, BRDID Table update for SIT Build
	2012/01/11	No.73	V	V		Page31, Modify R2209 From 18K to 33K for FVT BRDID update
	2012/01/11	No.74	V			Page26, Modify R2166 P/N from SD028330080 (33ohm) to SD034499180 (4.99K) for logo led brightness fine tune
	2012/01/11	No.75	V	V	V	Page35, Remove R2469 for logo led brightness fine tune
MEMO	2012/01/11	No.76	V			Page18, Modify C1445,C1446 P/N from SE071200JN0 to SE071200J80 for FVT SMT Memo
	2012/01/11	No.77	V			Page36, Modify C2316 P/N from SE080105K80 to SE0000069L0 for FVT SMT Memo
	2012/01/11	No.78	V			Page26, Add C2144,C2145 P/N SE071220J80 (22P)for FVT SMT Memo
	2012/01/11	No.79	V	V	V	Page36, Add Q2317 to Replace U2303 for +1.1V Power Mos layout space not enough issue
	2012/01/11	No.80	V	V	V	Page36, Add Q2318 to Replace U2304 for +3V Power Mos layout space not enough issue
	2012/01/11	No.81	V			Page29, Modify R1102,R1104,R1105 BOM Structure to @ for Vendor suggestion
	2012/01/12	No.82		V	V	Page36, Modify R2323.1 & R2322.1 from +VSB to +5VALW for VGS over spec issue
	2012/01/12	No.83				Page36, Modify Q2317 & Q2318 P/N: from SB00000LQ00 to SB923050030 for VGS over spec issue
	2012/01/12	No.84		V	V	Page31,35 Modify U2200 Pin70 Net name from FCH_PWR_EN# to FCH_PWR_EN for +3V & +1.1V power control solution change
	2012/01/12	No.85	V			Page36, Modify R2325 to POP from FCH_PWR_EN to FCH_PWR_EN_R for +3V & +1.1V Power Control
	2012/01/12	No.86	V	V	V	Page36, Delete R2314,R2318,R2320,Q2311 for Reduce Power Consumption
	2012/01/16	No.87	V			Page31, Modify R2230 BOM Structure from POP to @ for double pull up error
	2012/01/16	No.88	V			Page31, Modify R2208 BOM Structure from POP to @ for internal pull high solution
	2012/01/16	No.89	V			Page36, Modify Q2313,Q2314,U2304,C2309,C2312,C2321,R2323,R2310,R2324 to @ for +3VALW to +3V_FCH Circuit (Reduce Power Consumption)
	2012/01/16	No.90	V			Page36, Modify Q2316,Q2309,U2303,C2317,C2320,C2318,C2319,R2322,R2317 to @ for +1.1VALW to +1.1V_FCH Circuit (Reduce Power Consumption)

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