ZZZ1

PCB

Compal Confidential

KAWG0 Schematics Document

AMD S1g1 / RS690MC / SB600

2009 / 04 / 09

Rev:1.0

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
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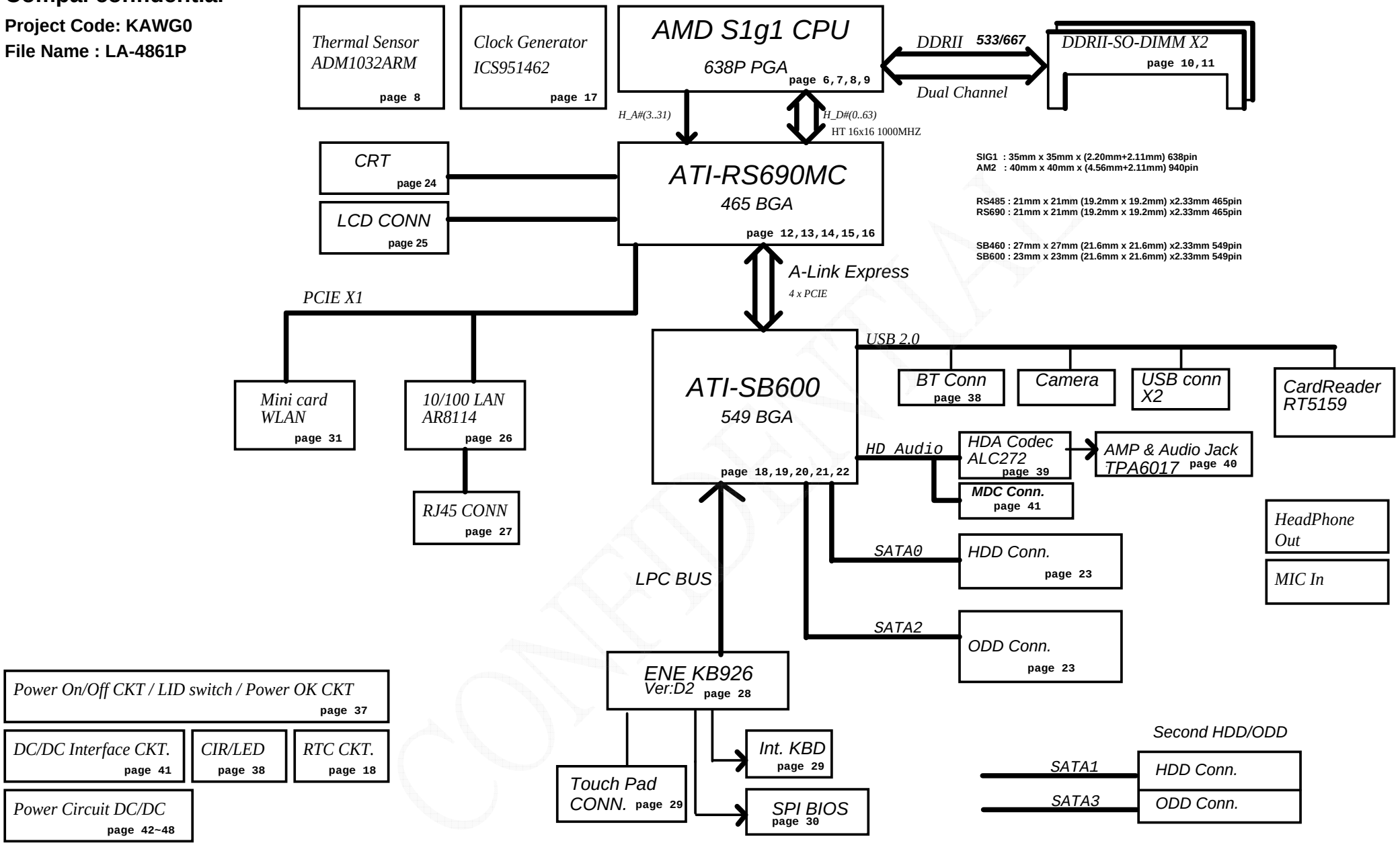
Compal confidential

Project Code: KAWG0

File Name : LA-4861P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
ADM1032	1001 100X b

SB600 SM Bus 1 address

Device	Address
Clock Generator (ICS951462)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
Wireless Lan	

SB600 SM Bus 2 address

Device	Address
New Card	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
NC Function	NC@
10/100 Lan	8114@
GIGA Lan	8132@
17" ID	17@
15" ID	15@

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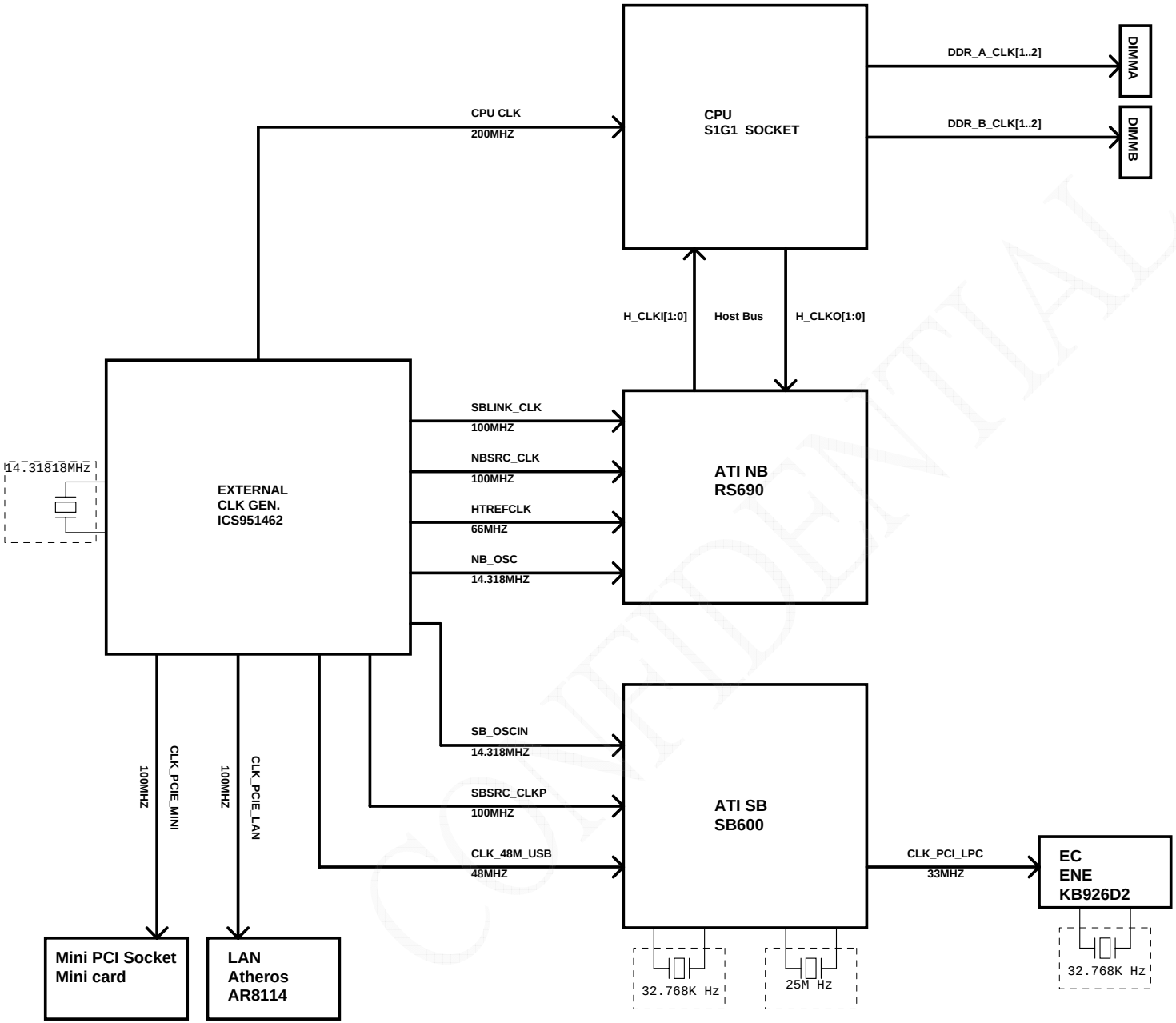

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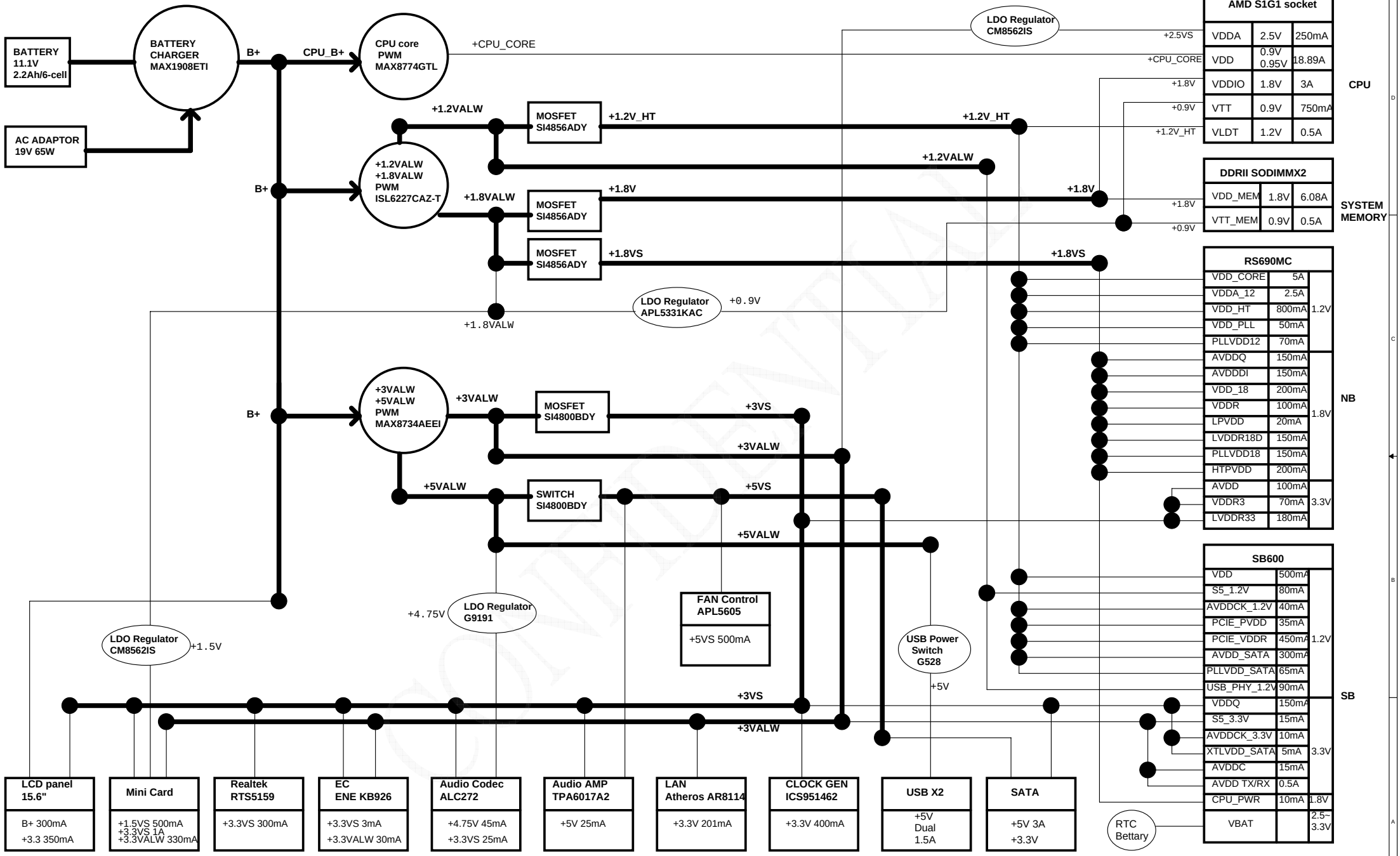

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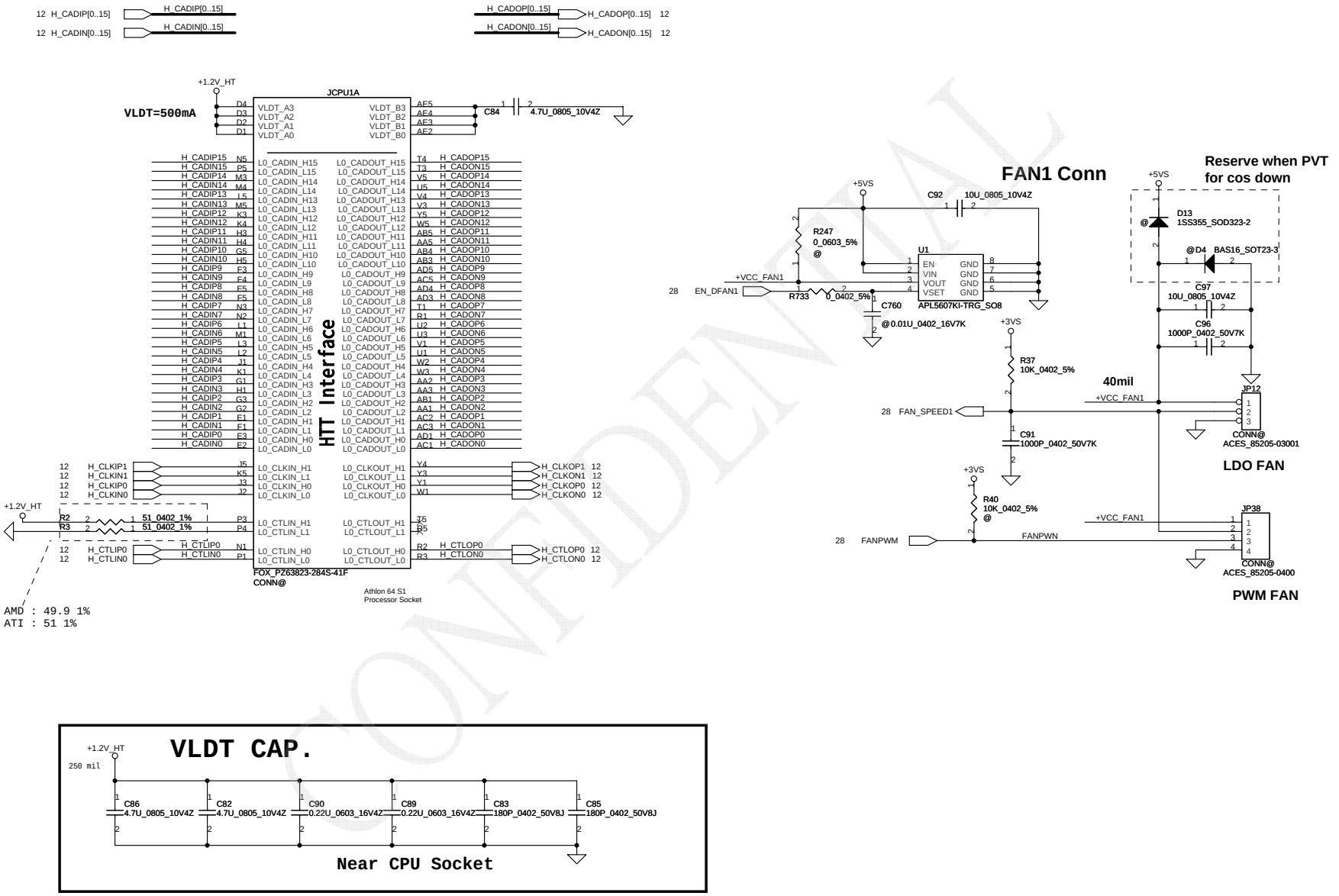

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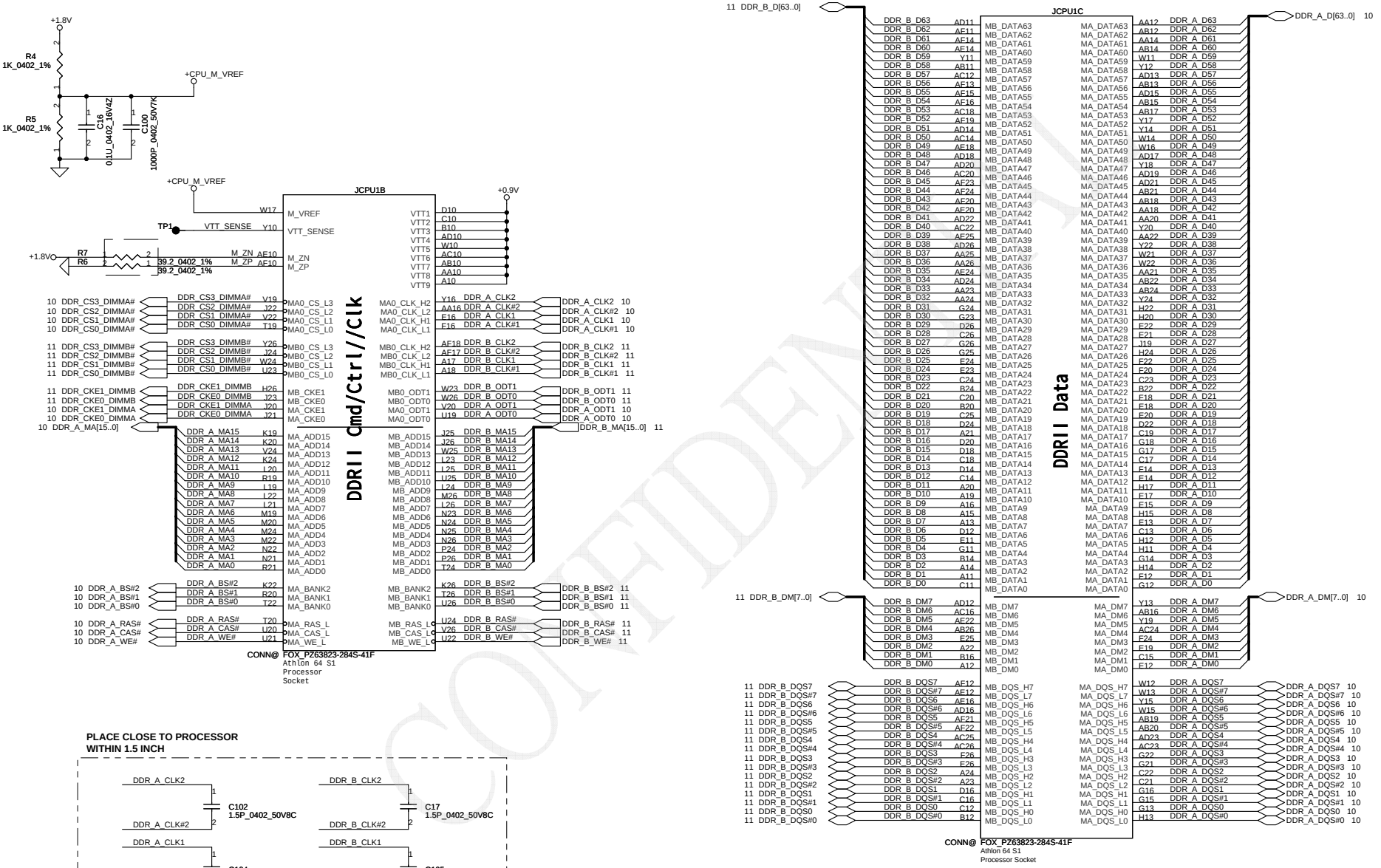
Processor DDR2 Memory Interface



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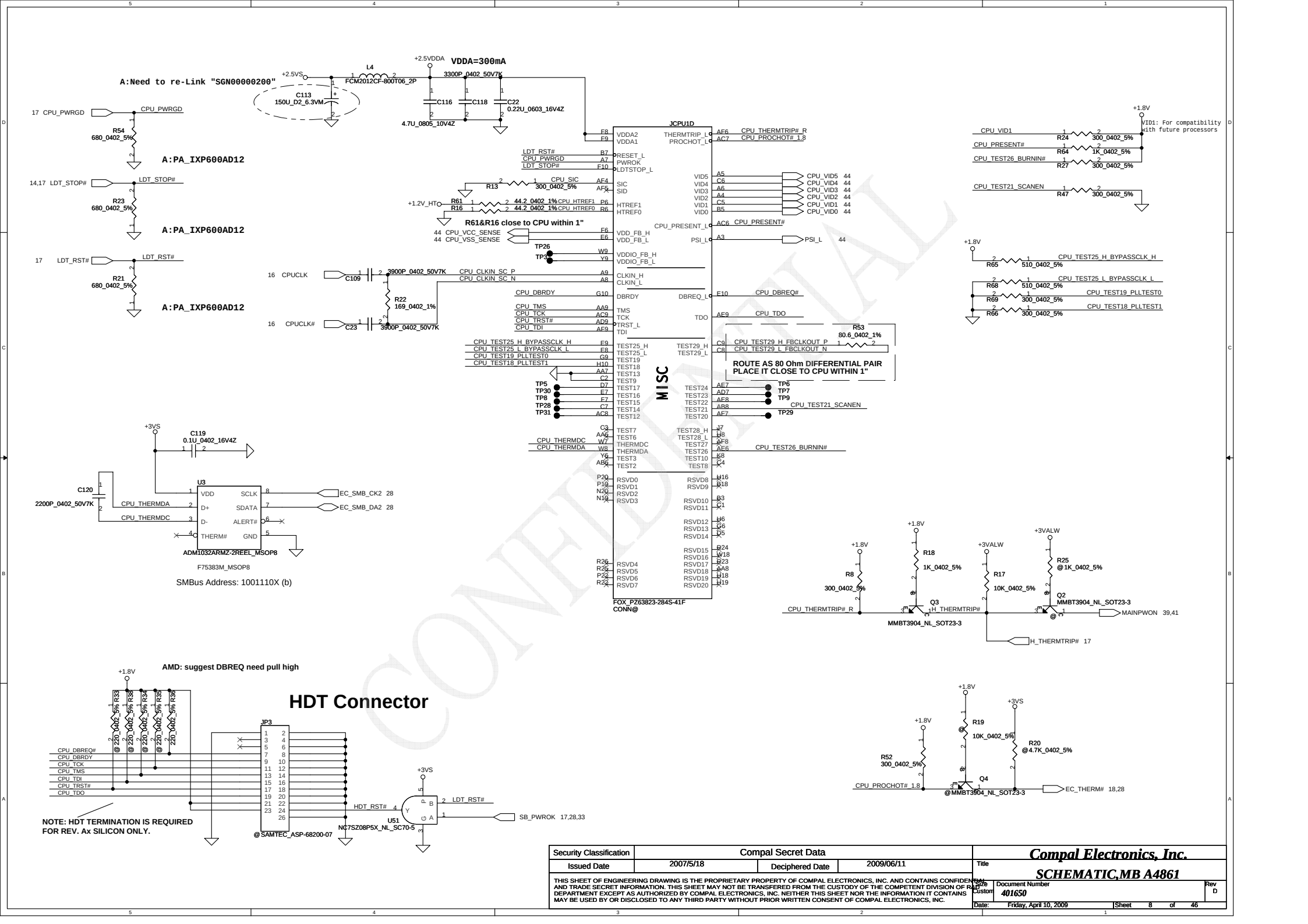

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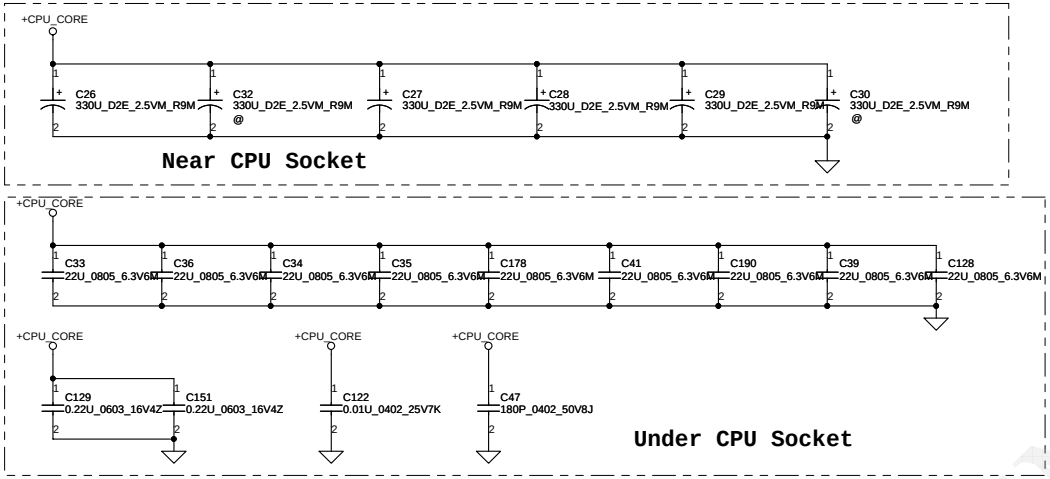
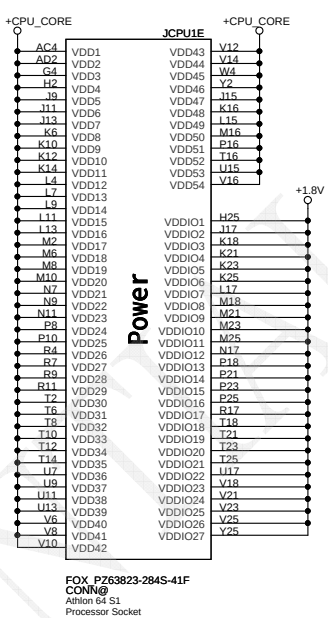
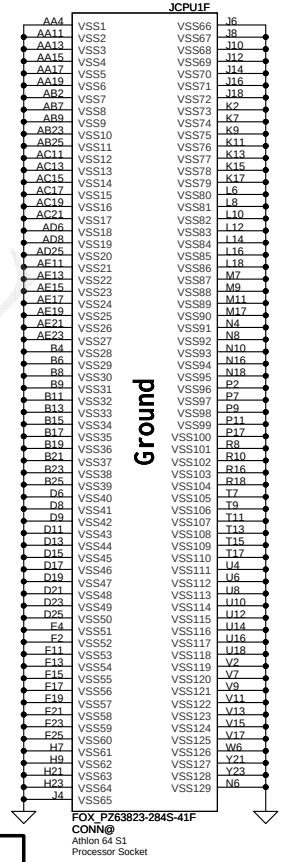
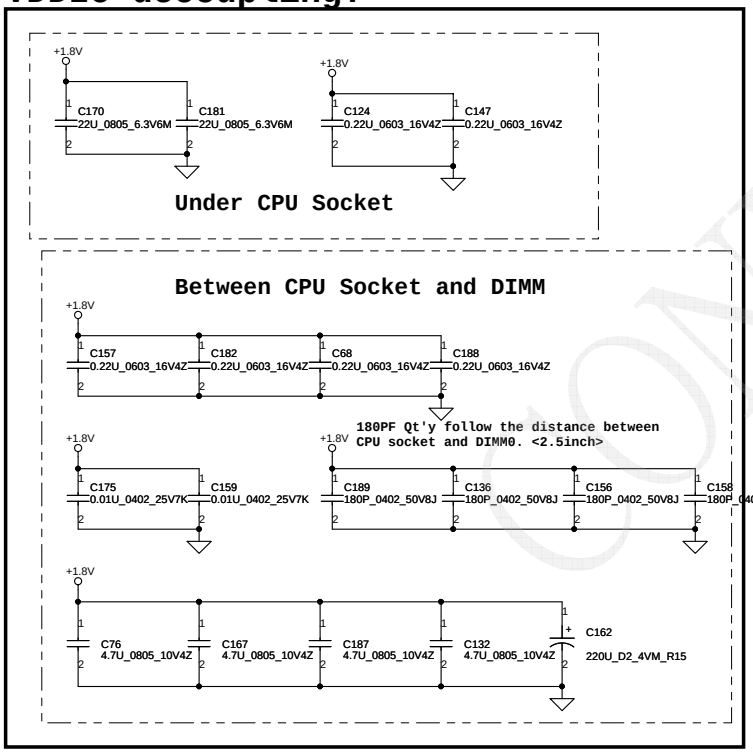
VDD(+CPU_CORE) decoupling.



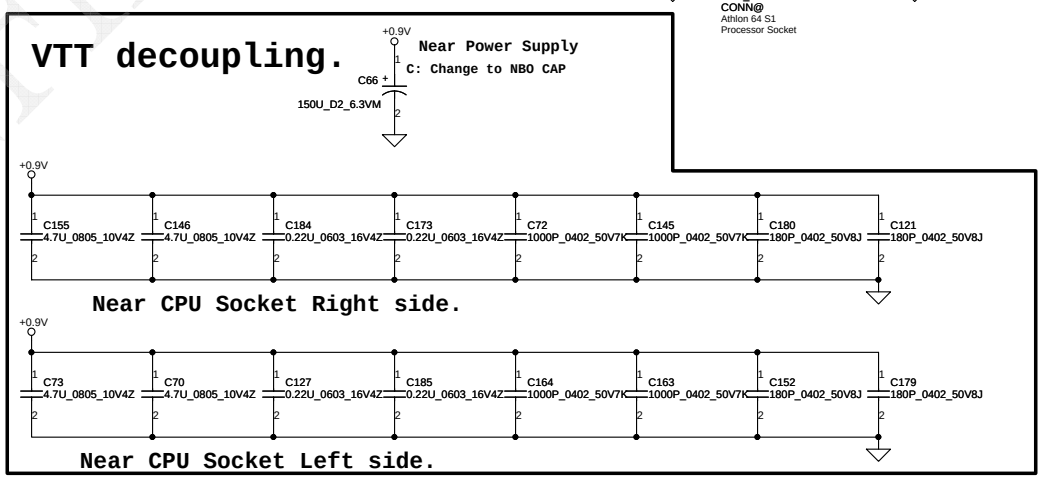




VDDIO decoupling.



VTT decoupling.



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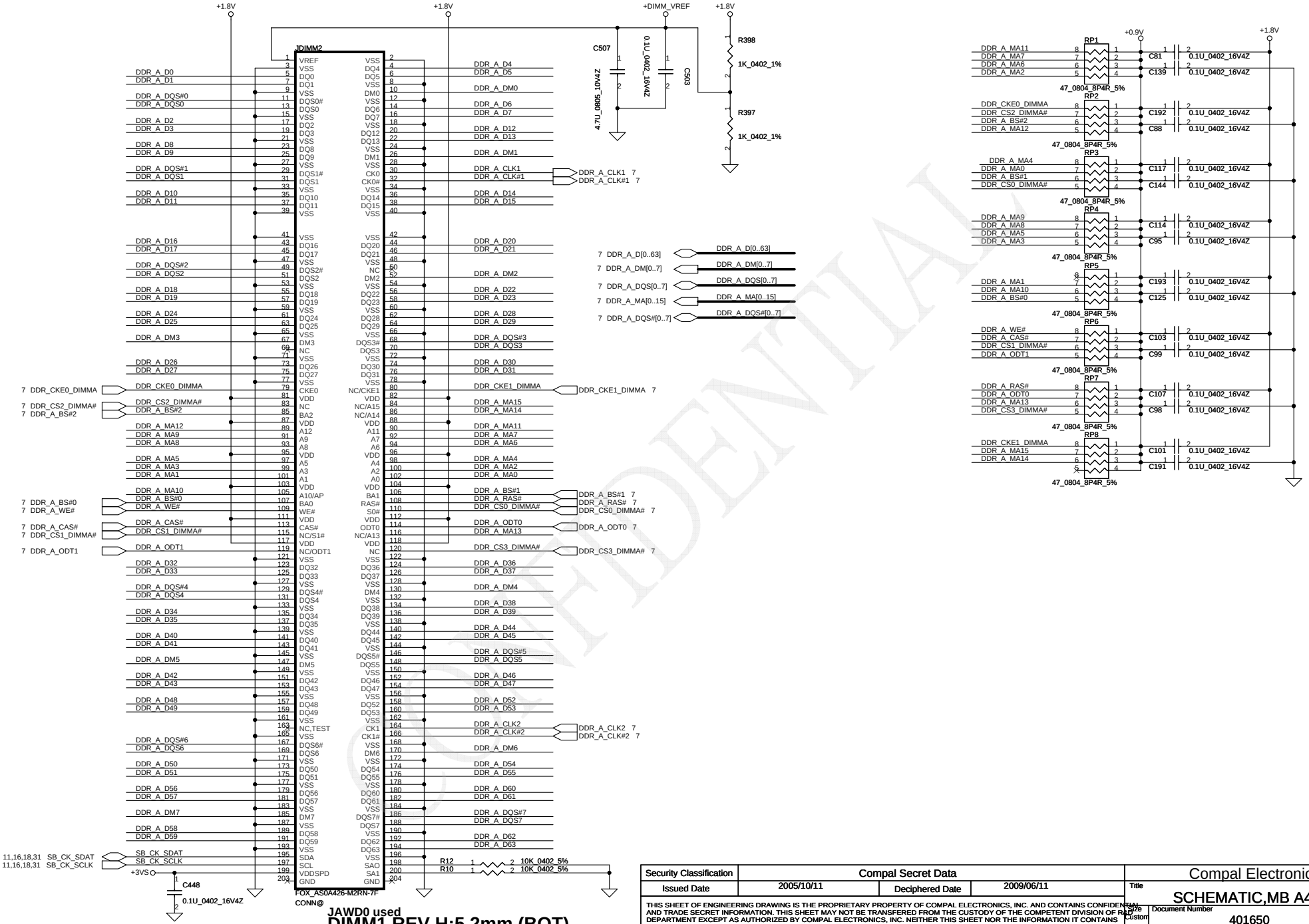

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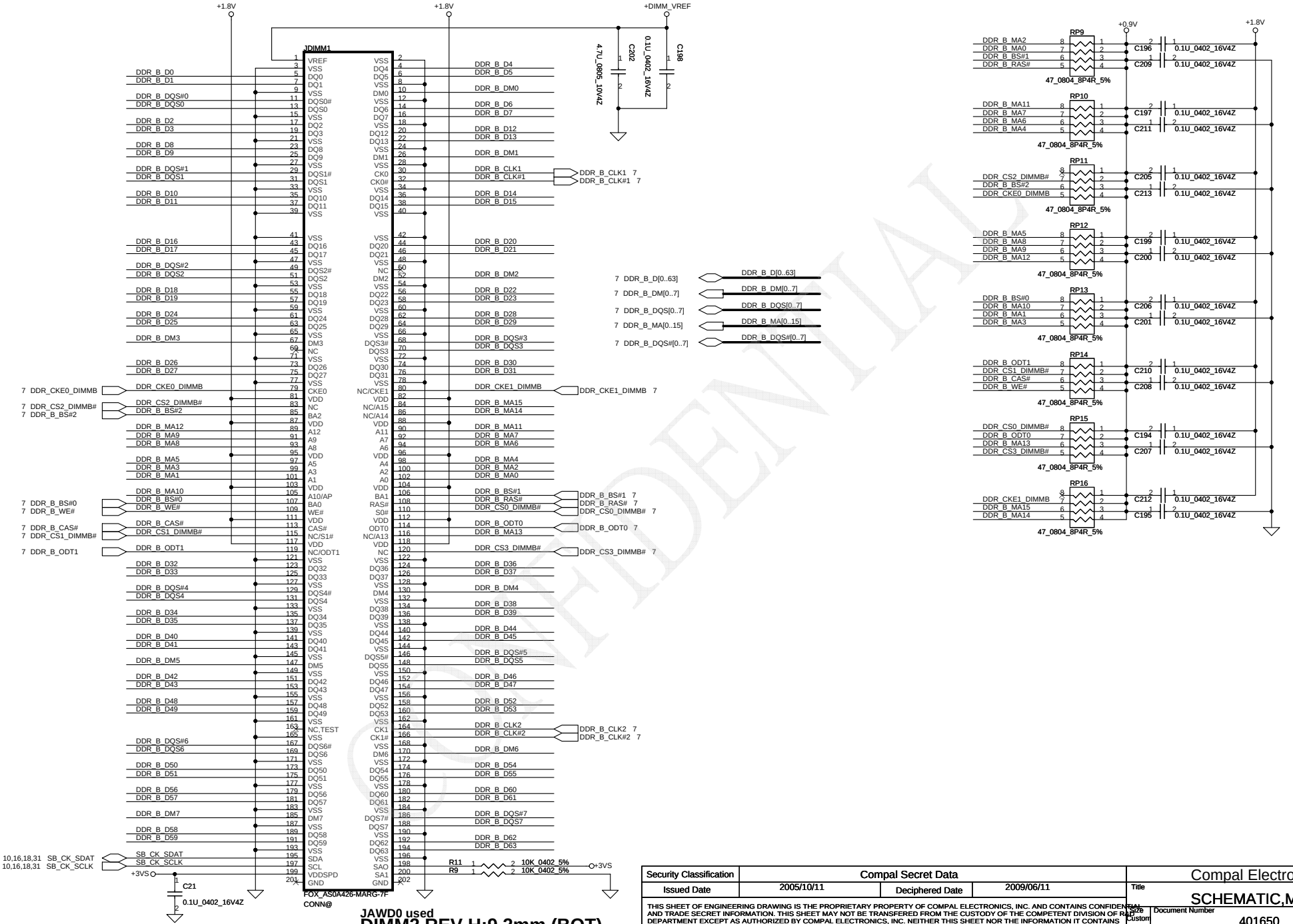

JAWD0 used

DIMM2 REV H:9.2mm (BOT)

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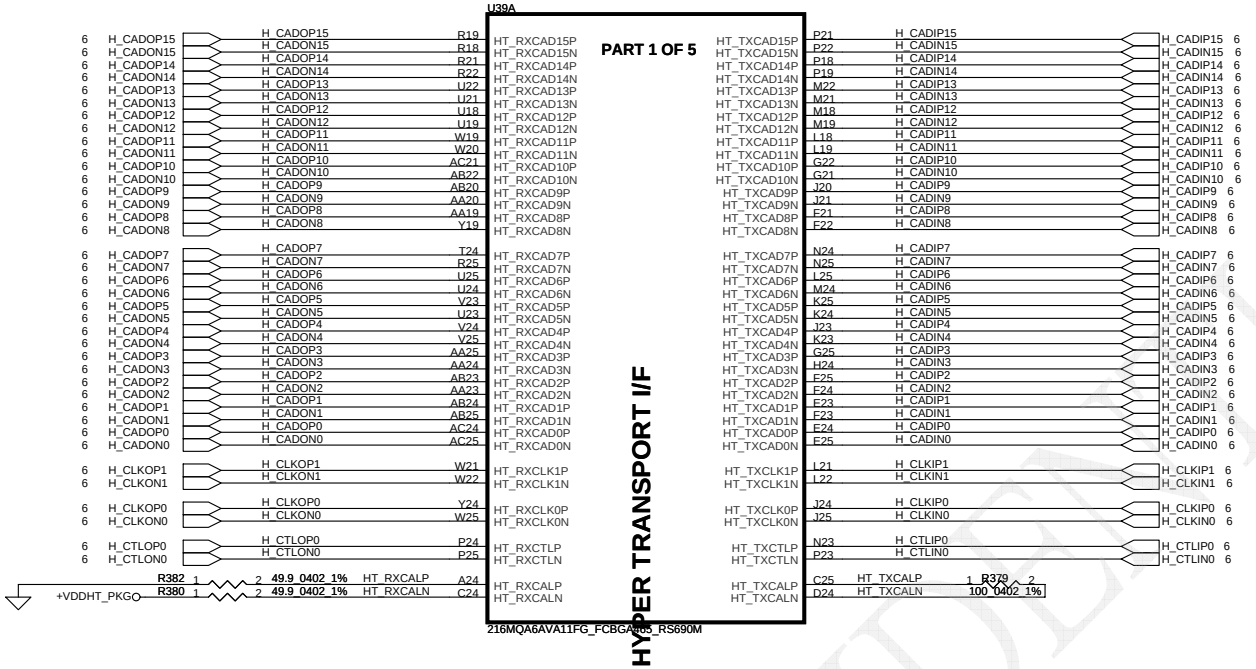

RS690MC : SA00001I480 / S IC 216LQA6AVA12FG RS690MC BGA 465P 0FA

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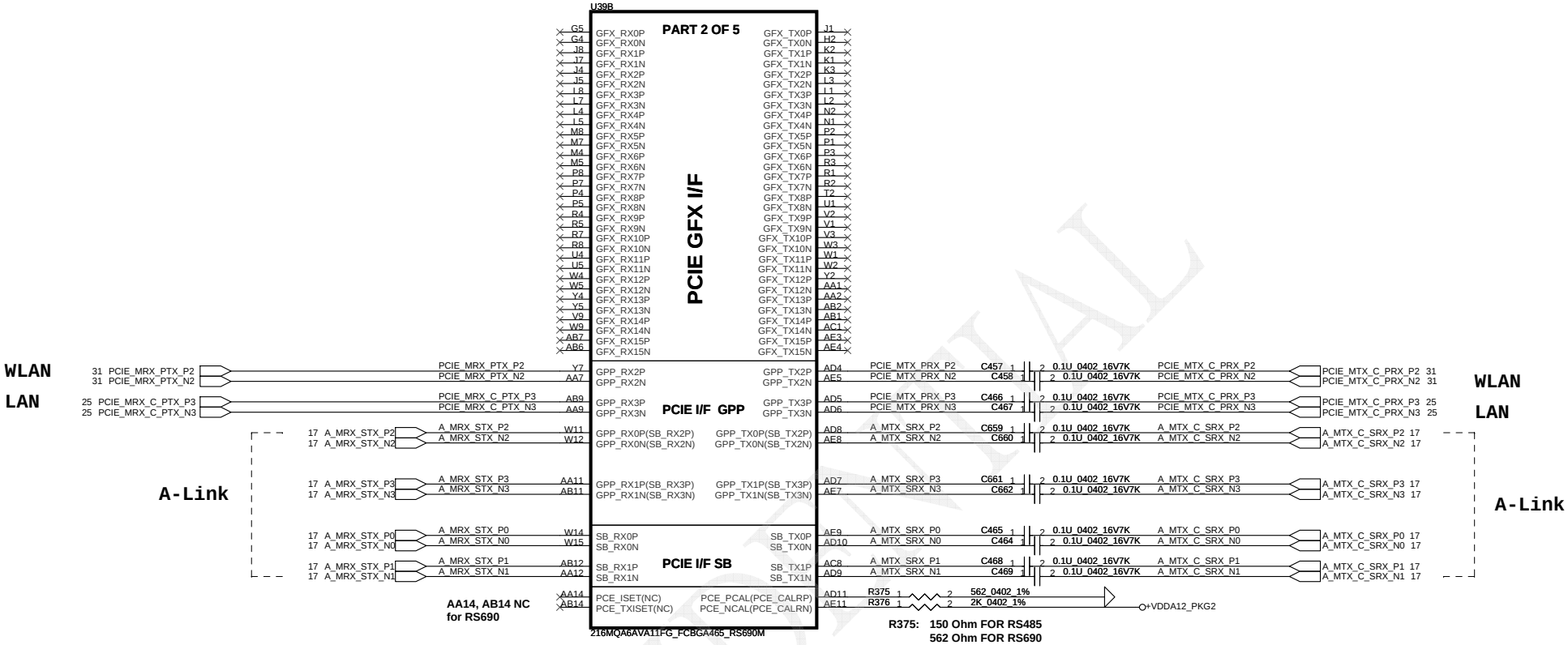

R375: 150 Ohm FOR RS485
562 Ohm FOR RS690

R376: 82.5 Ohm FOR RS485
2KOhm FOR RS690

RS690MC : SA00001I480 / S IC 216LQA6AVA12FG RS690MC BGA 465P 0FA

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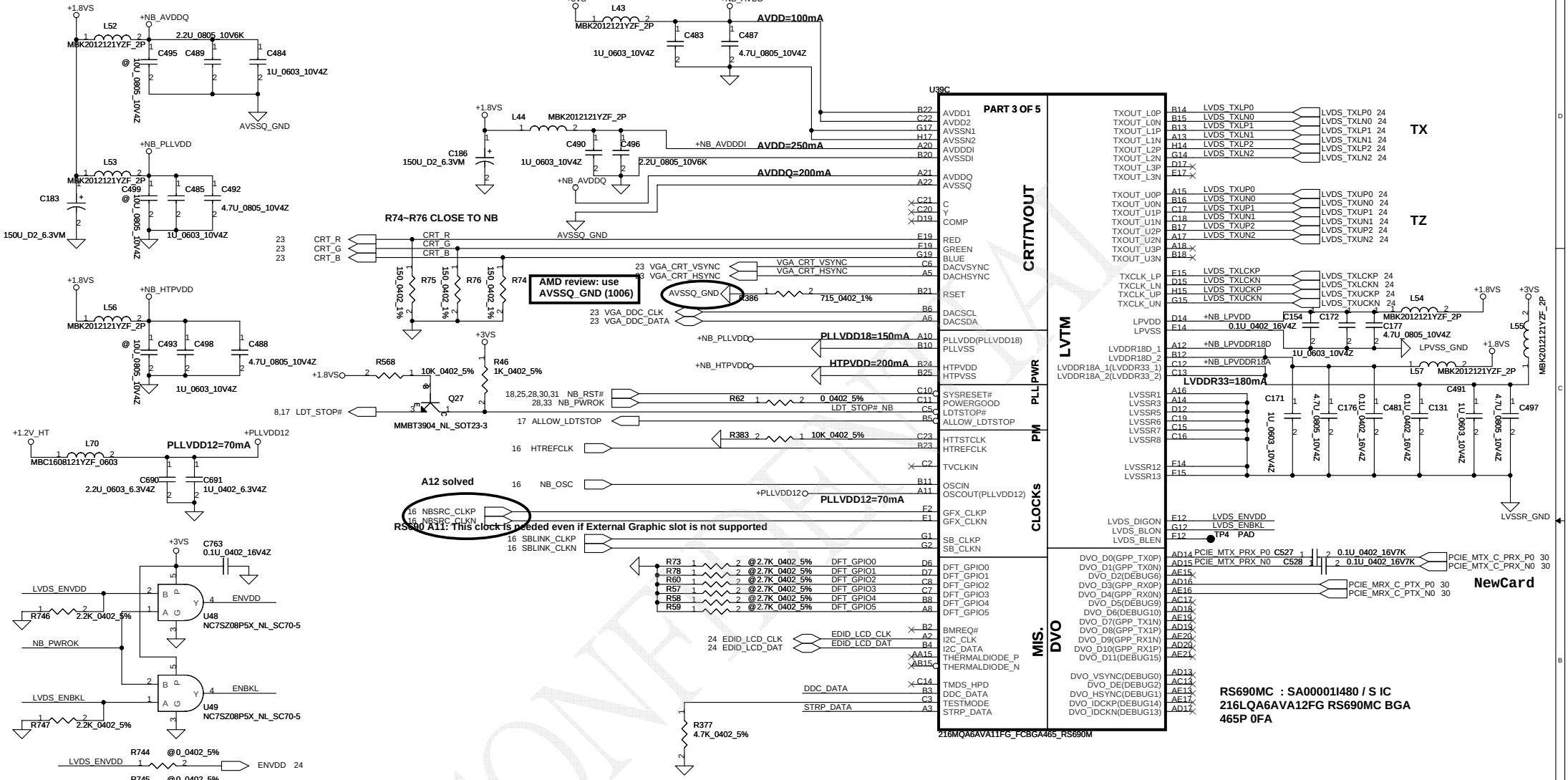

	RS690		RS690 only	
	DFT_GPIO0	DFT_GPIO1	DFT_GPIO[4:2]	DFT_GPIO5
PULL HIGH (internally pulled high)	Memory side port not available DEFAULT	Bypass the loading of EEPROM straps and use Hardware default values DEFAULT	These pin straps are used to configure PCI-E GPP mode: 111: register defined (register default to Config E) DEFAULT 110: 4-0-0-0-0 Config A 101: 4-4 Config B 100: 4-2-2 Config C 010: 4-1-1-1-1 Config E 011: 4-2-1-1 Config D others: register defined (register default to Config E)	Enable debug bus via the memory IO pads, if available in the package use default values DEFAULT
PULL LOW	Memory side port available	I2C Master can load strap values from EEPROM if connected, or use default values if not connected		use the memory data bus to output the debug bus

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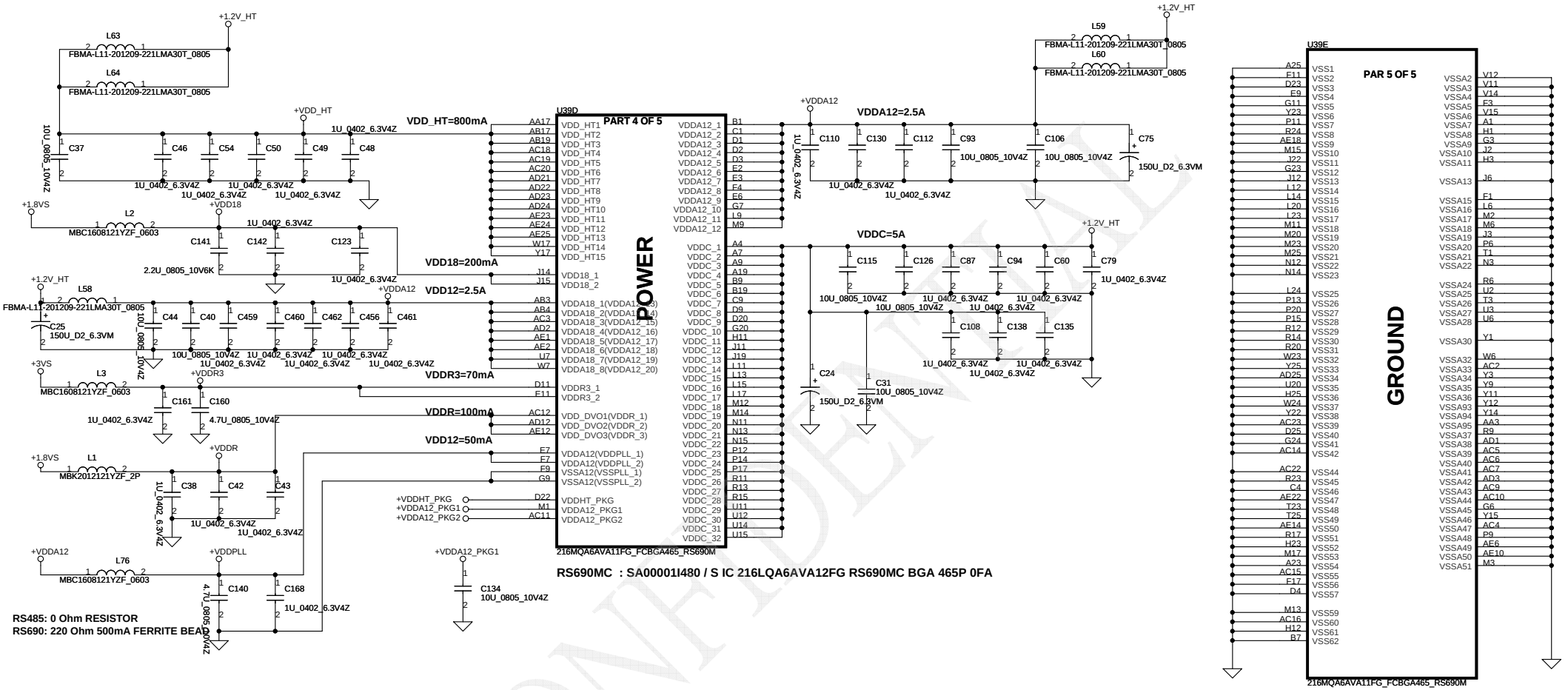

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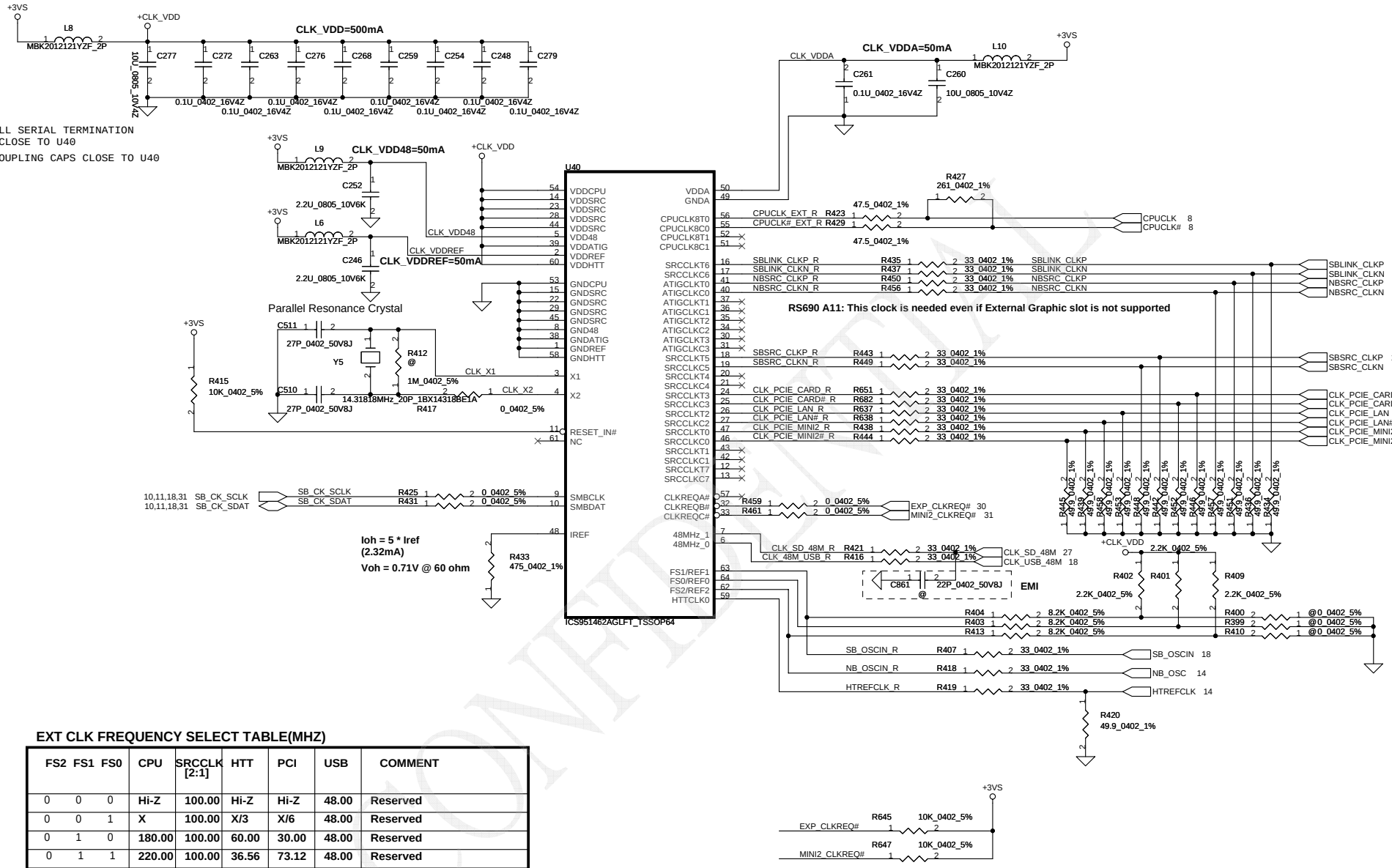

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

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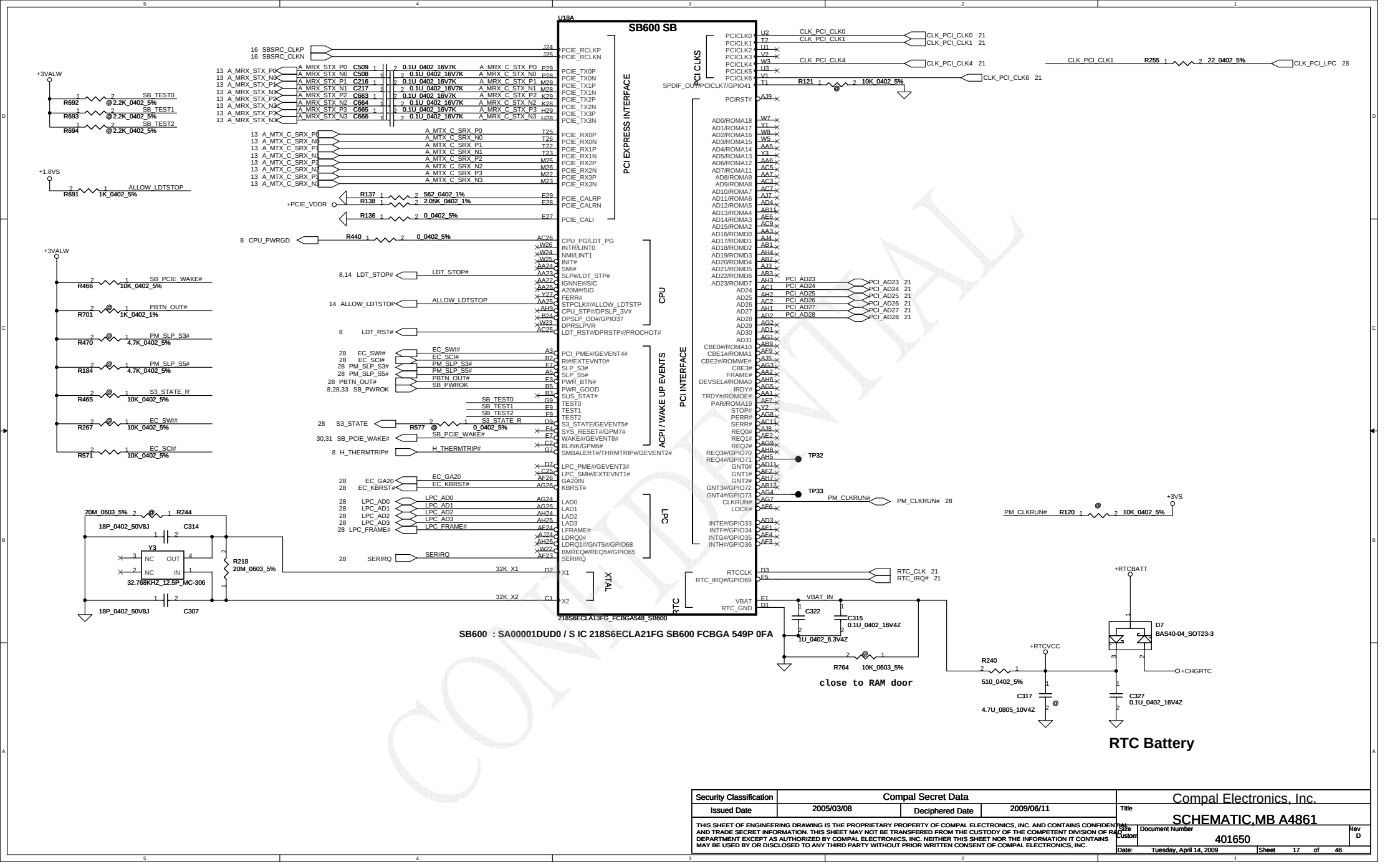

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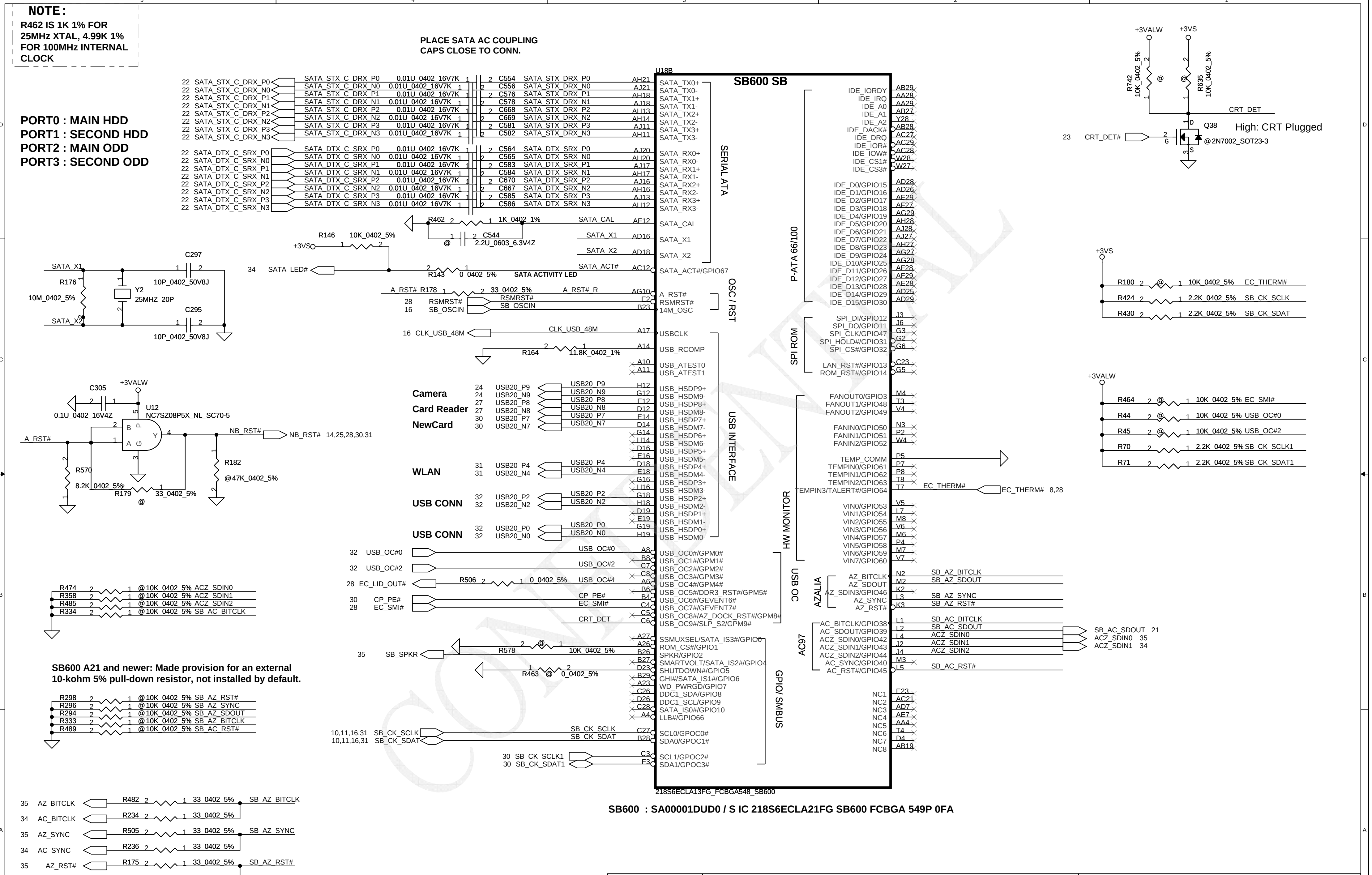

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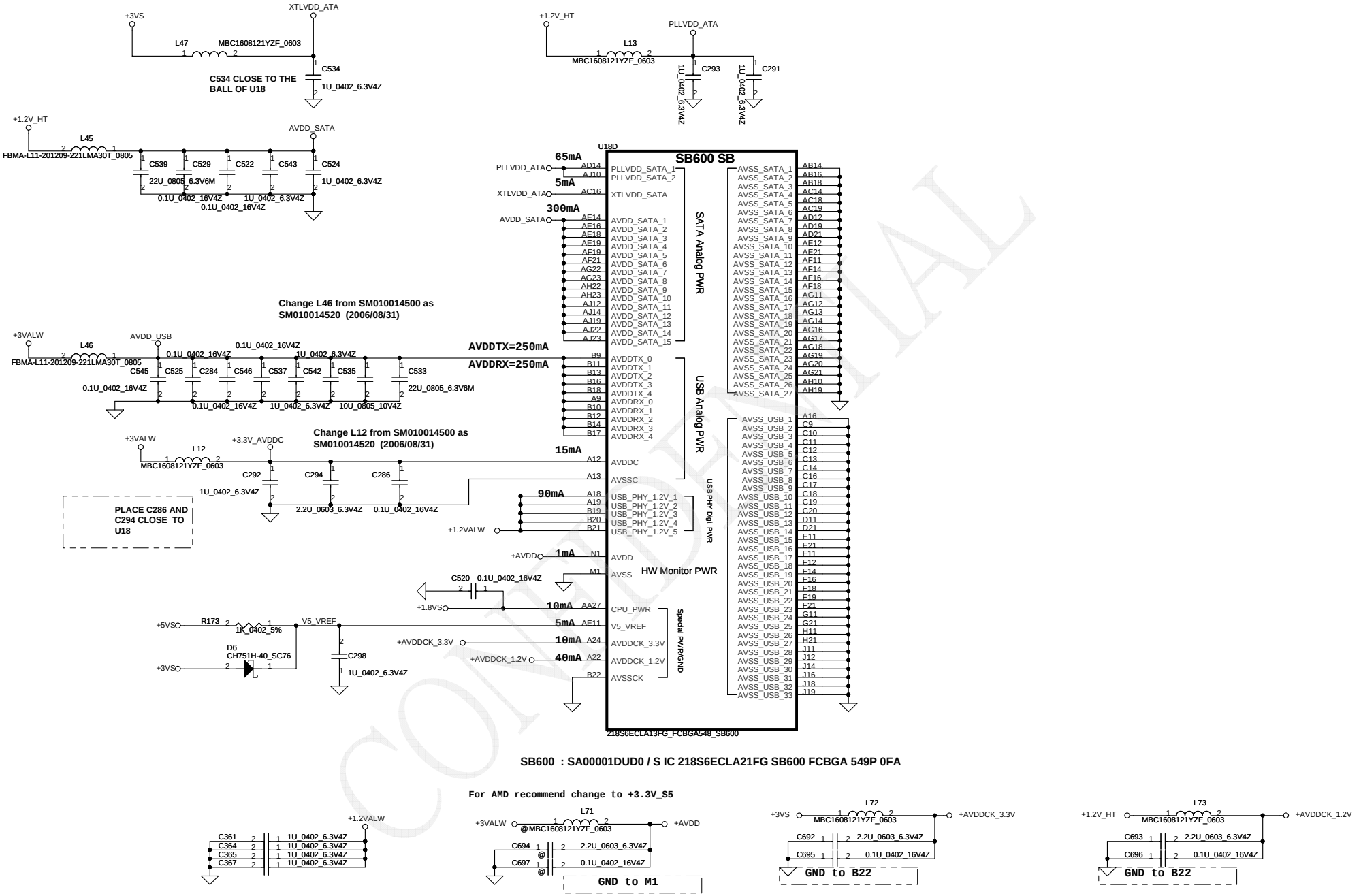

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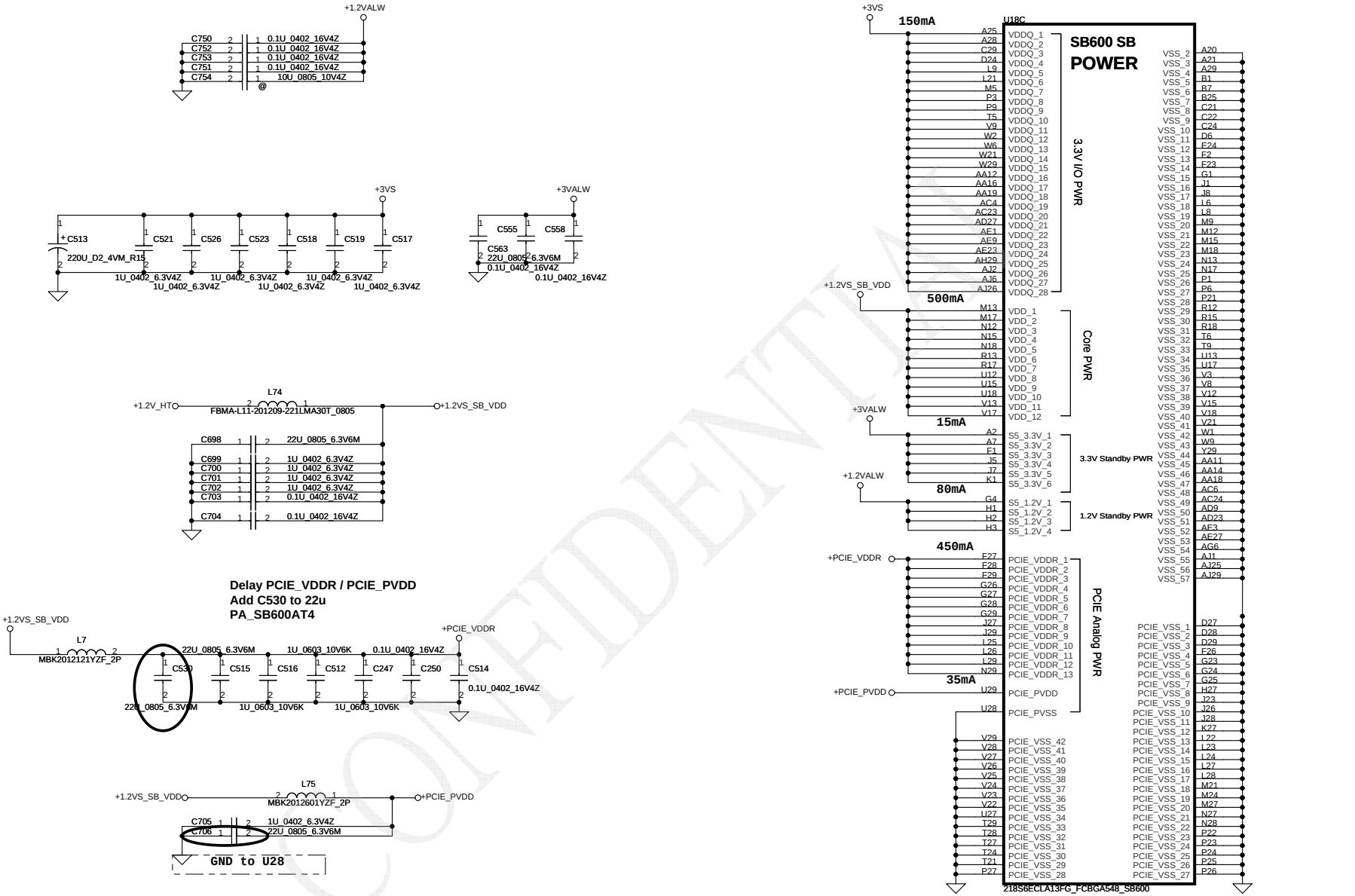

SB600 : SA00001DUD0 / S IC 218S6ECLA21FG SB600 FCBGA 549P 0FA

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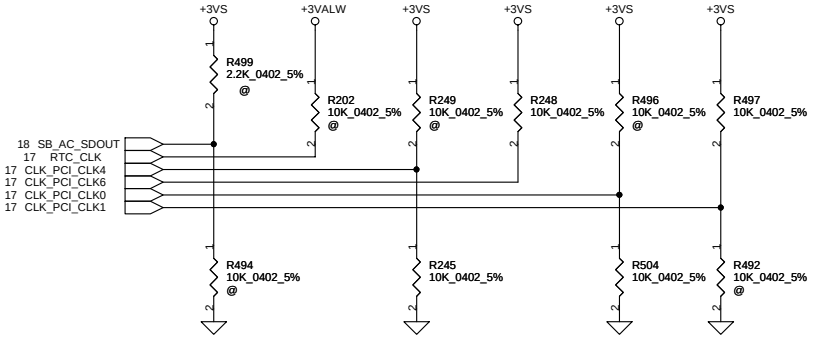
REQUIRED STRAPS

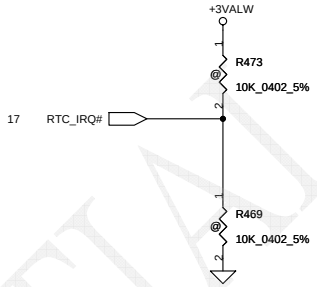
SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT, 15K PU FOR RTC_CLK, EXTERNAL PU/PD IS NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE REQUIRED



	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	

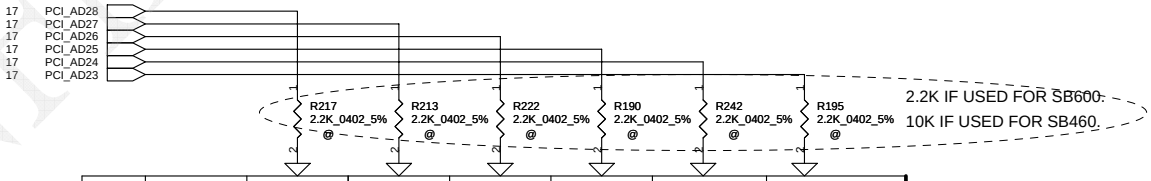
Internal RTC: Not connected. *

External RTC: Connected to IRQ# pin on external RTC. External RTC supports S5 wake capability (from S5 power rail or battery).



DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB600 ONLY

NOTE: FOR SB460, PCI_AD23 IS RESERVED

SB460 ONLY — SB600 ONLY

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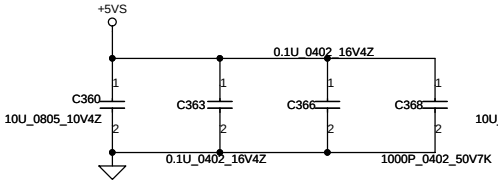
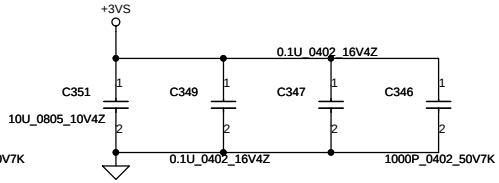
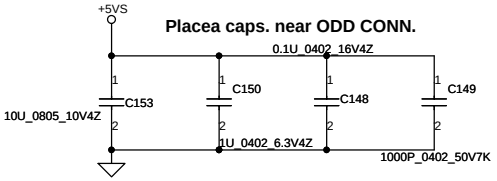
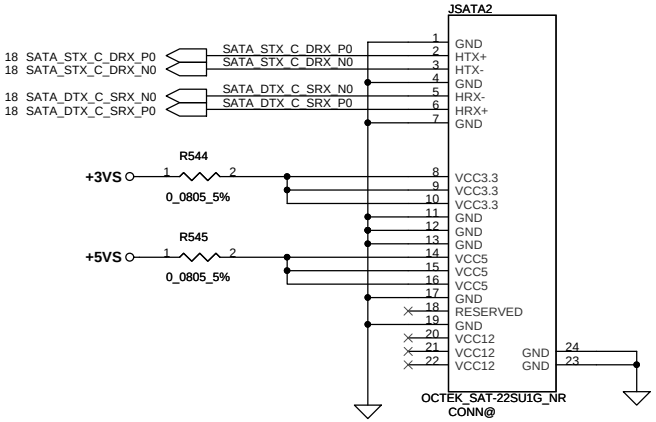




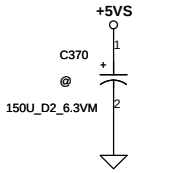


SATA HDD CONN

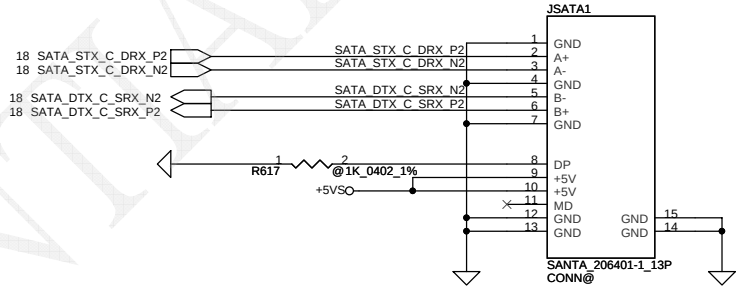
SATA ODD CONN



KALA0 used



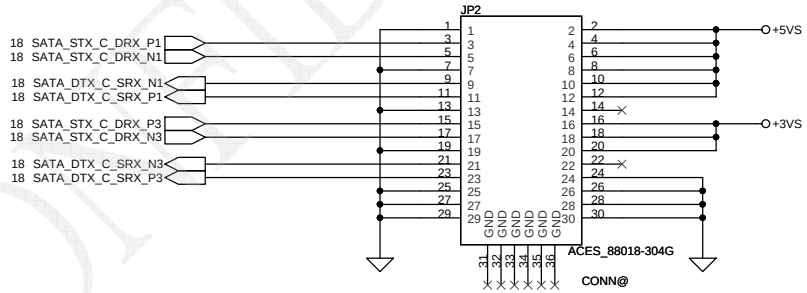
Close to SATA HDD

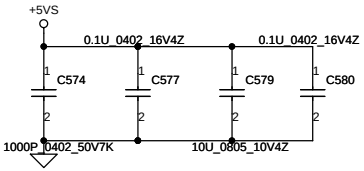


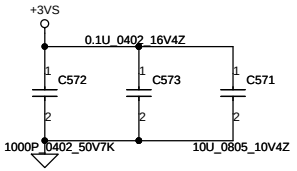
KALA0 used

Second HDD

Second ODD







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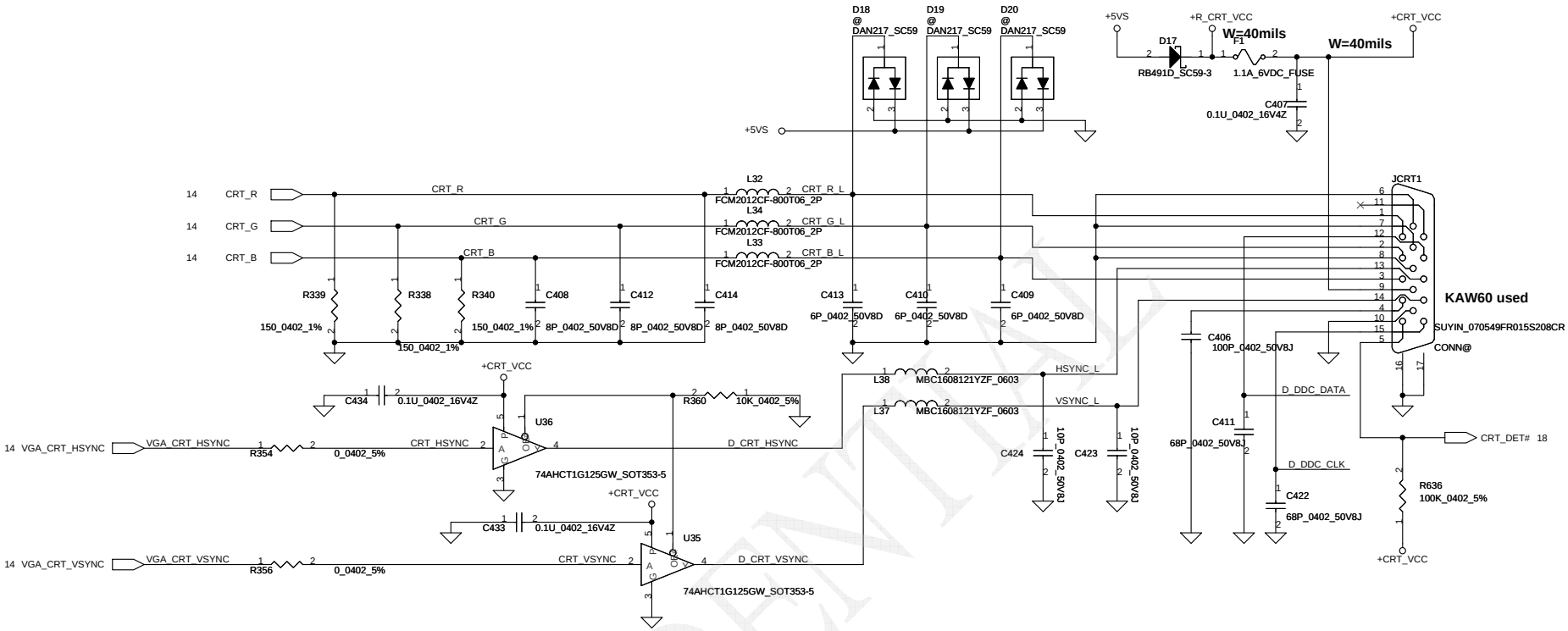
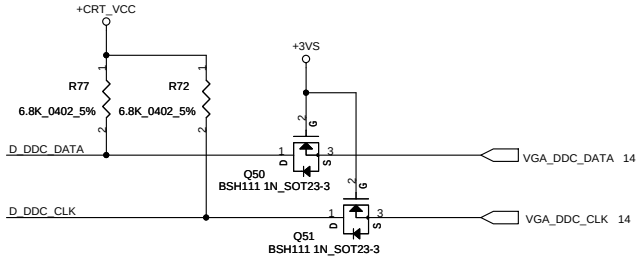
CRT Connector



Close to Conn side



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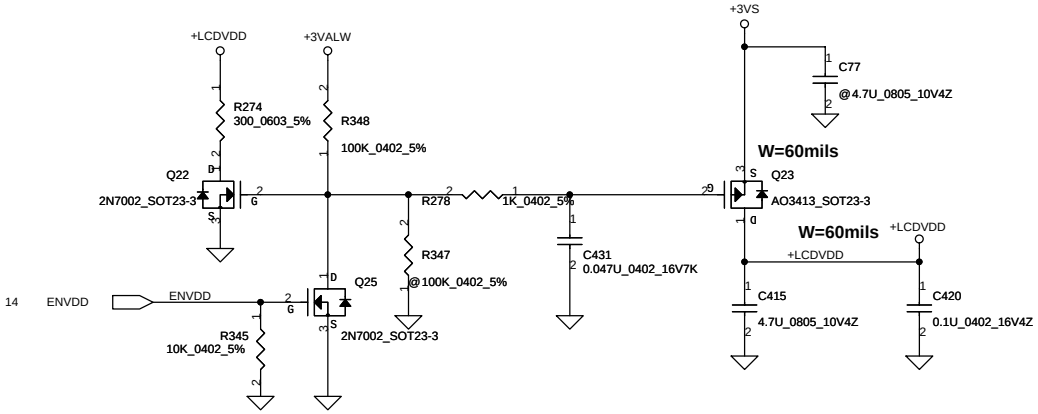
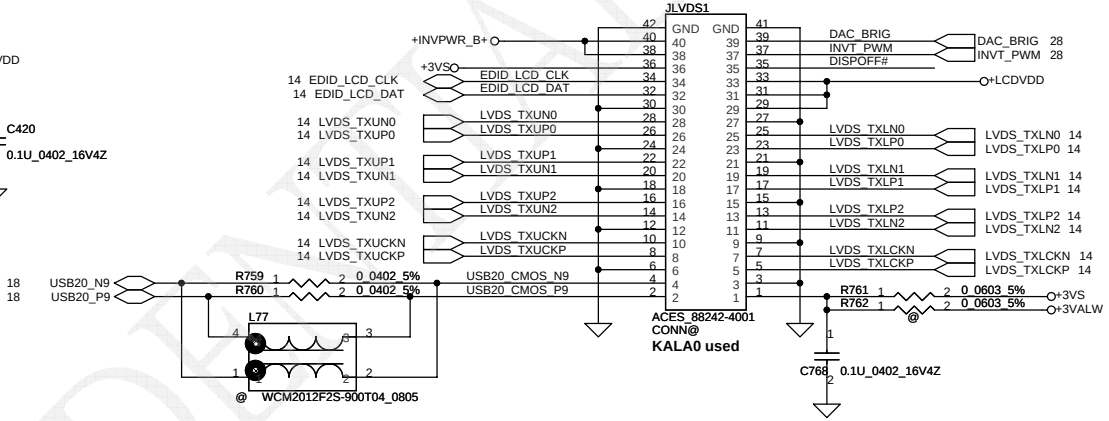
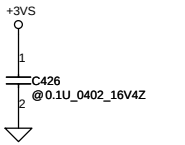
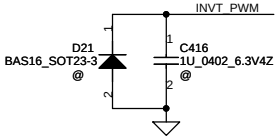
LCD POWER CIRCUIT

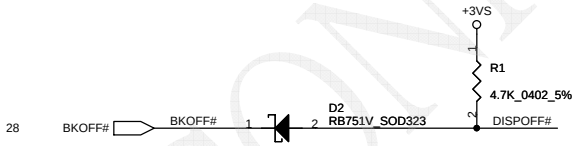


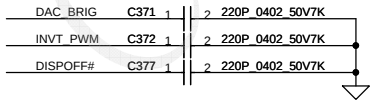
LCD/PANEL CONN.

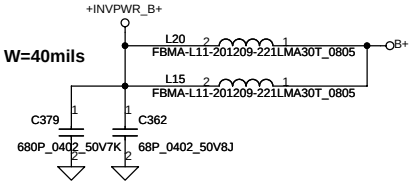


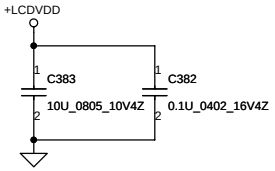












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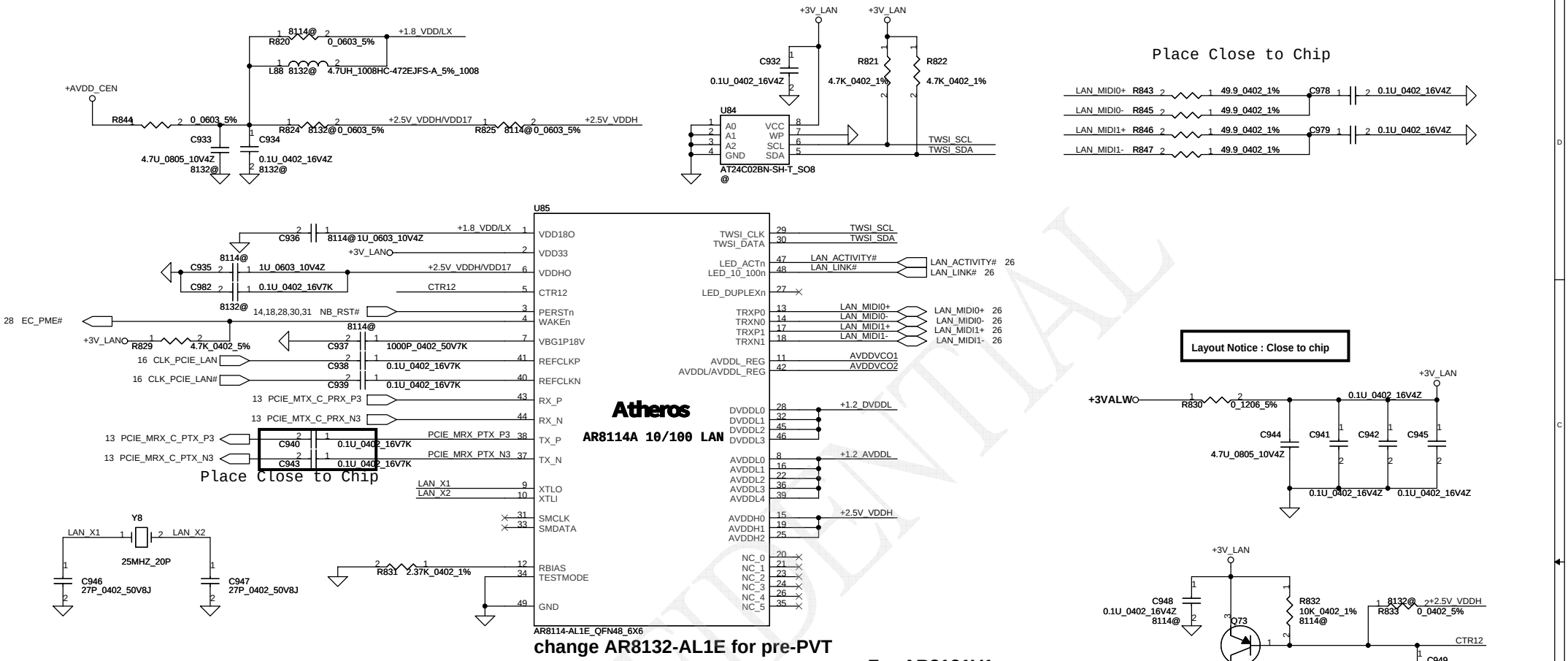

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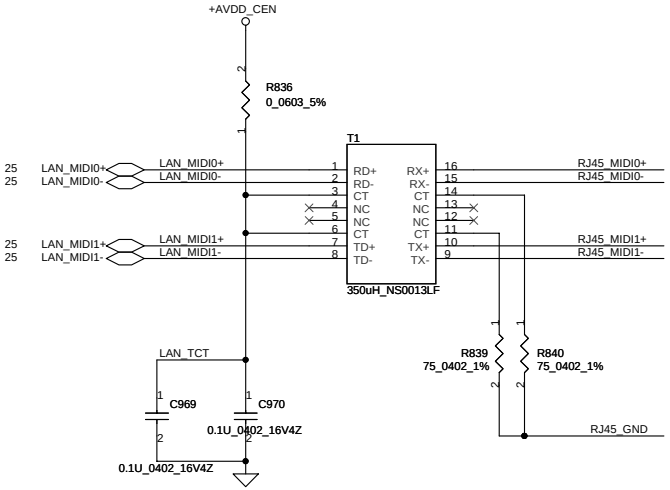

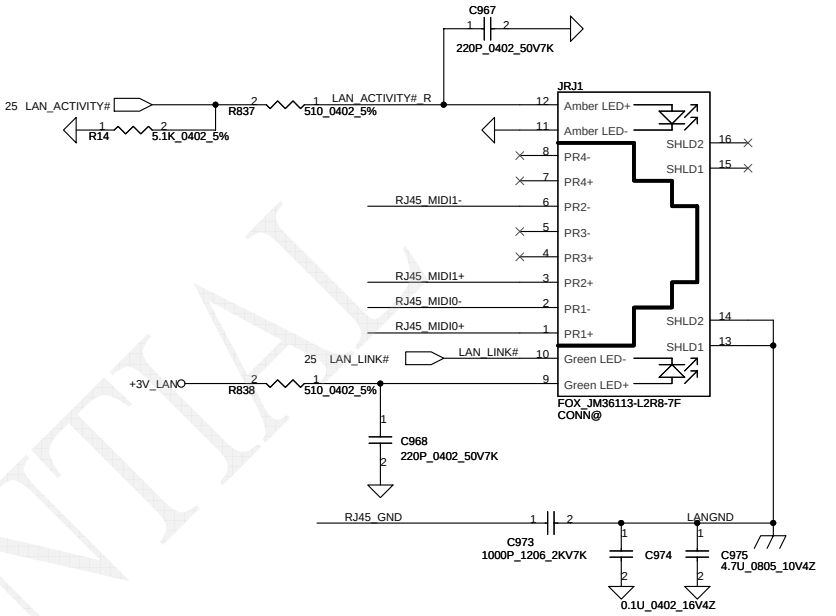

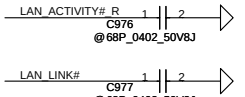

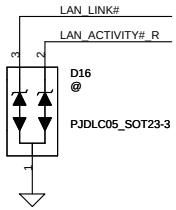

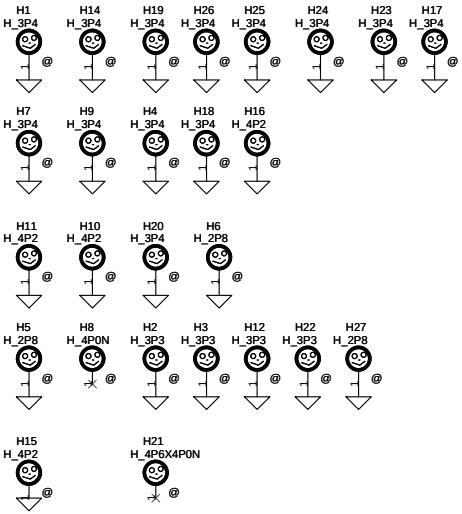

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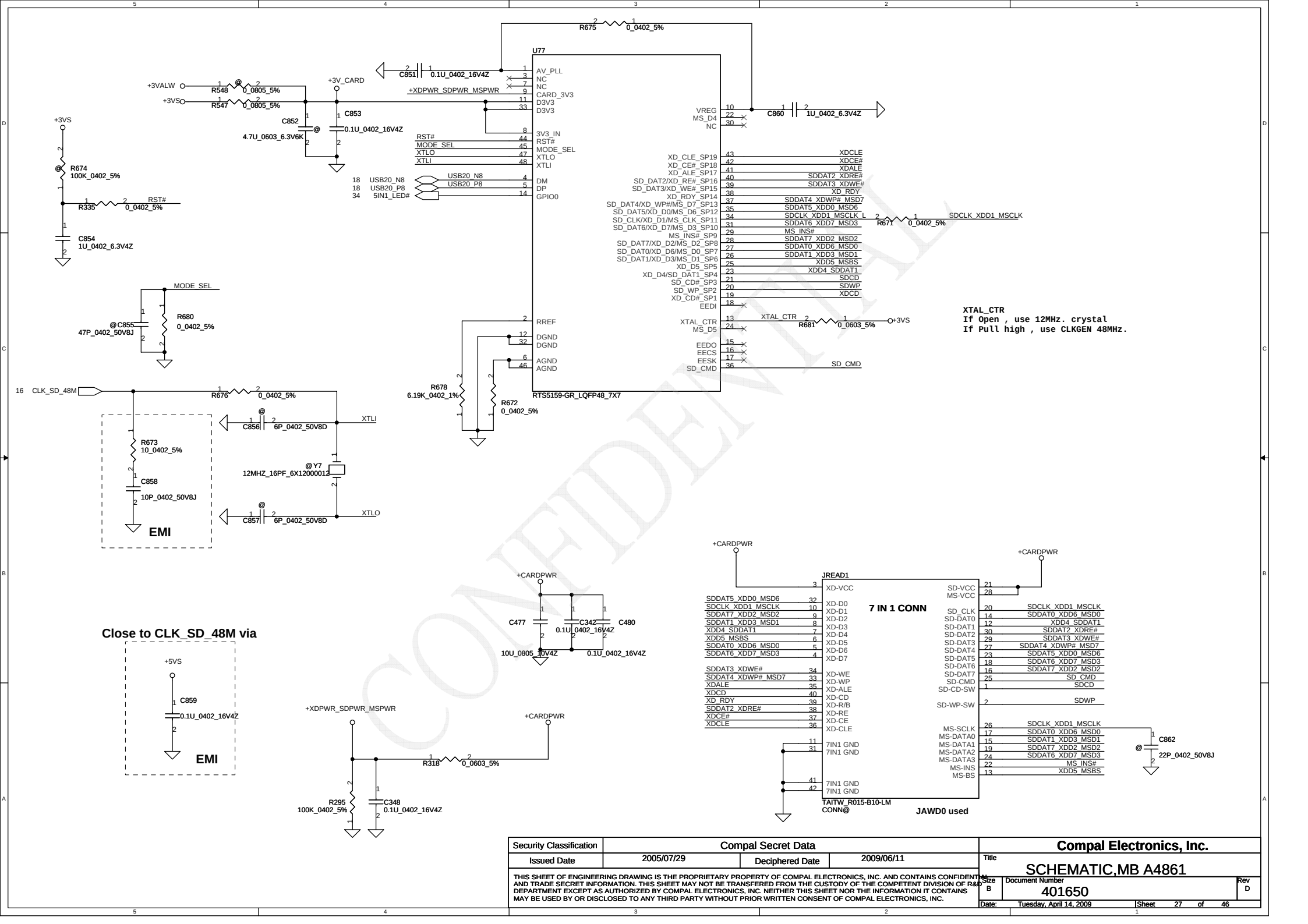

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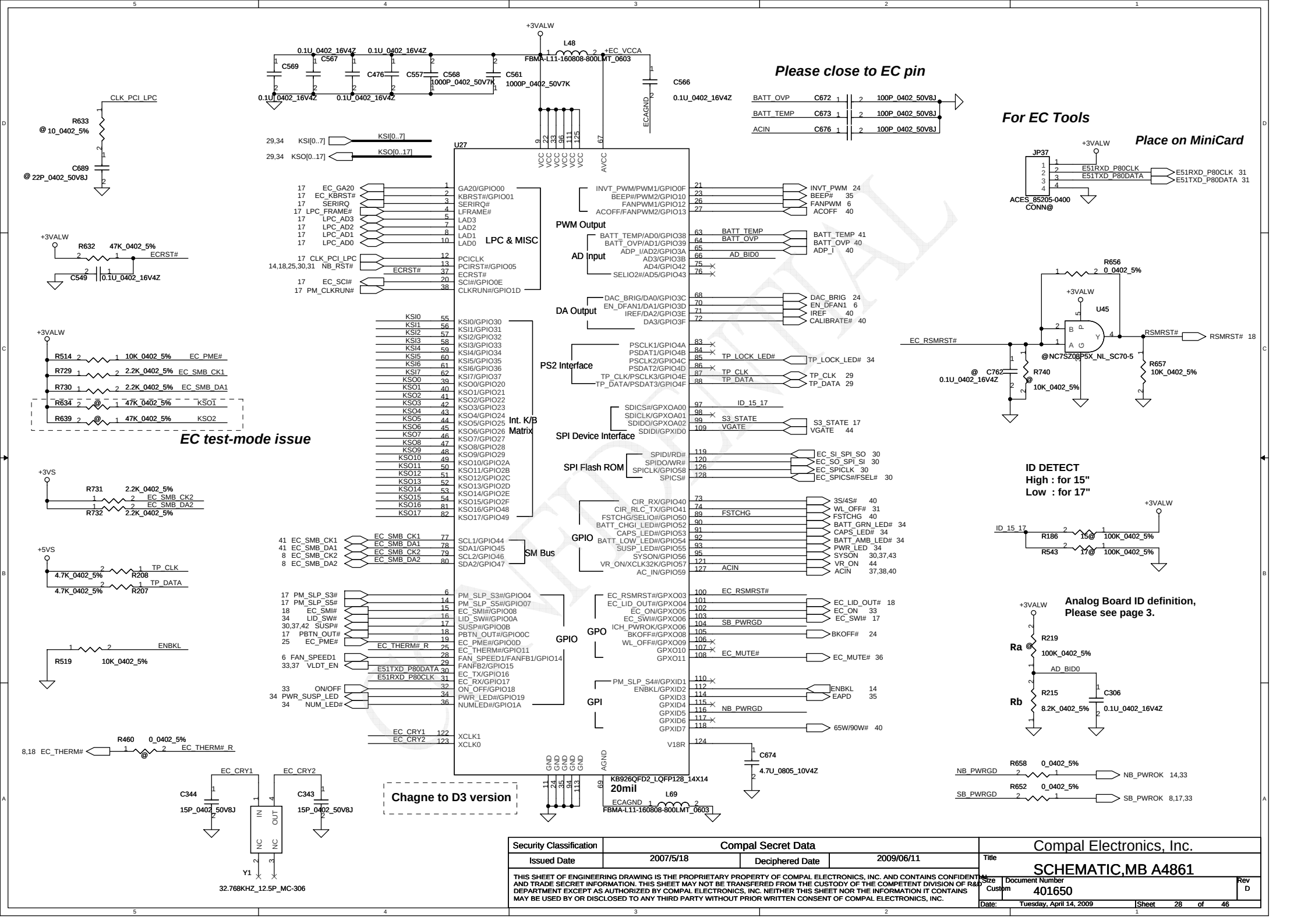

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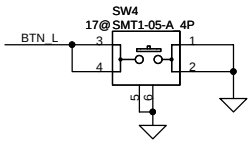
For 17"

Left



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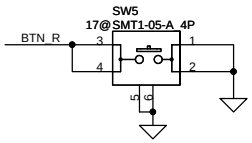
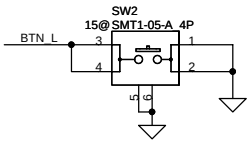


For 15"

Left



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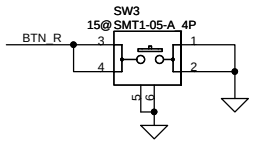
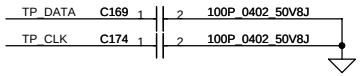
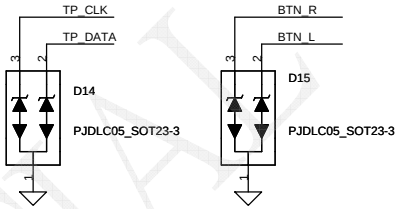
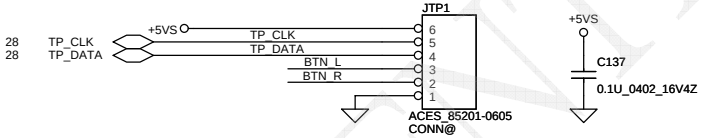






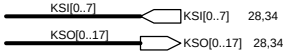
Change to SCA00000200

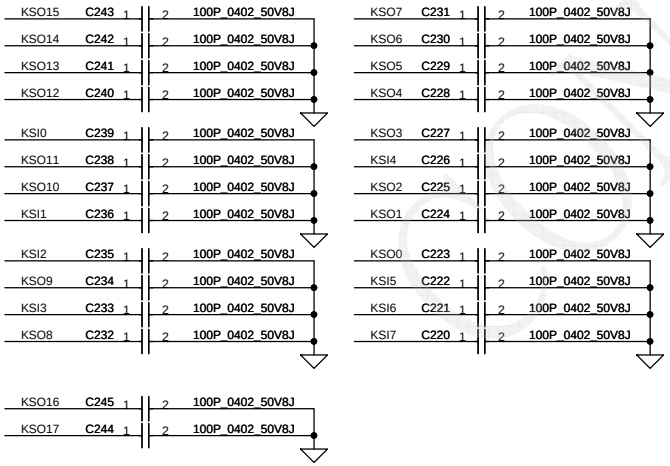
To TP/B Conn.



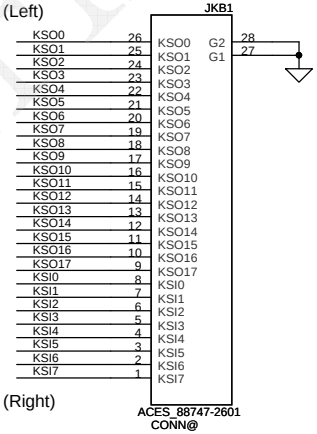
KALA0 used

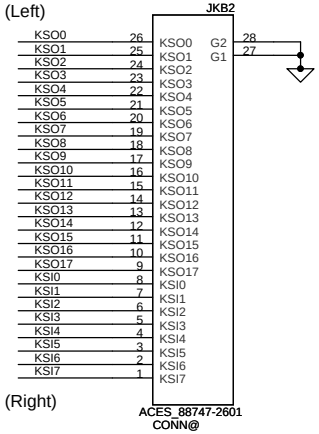
INT_KBD Conn.





KB1 for 15"
KB2 for 17"





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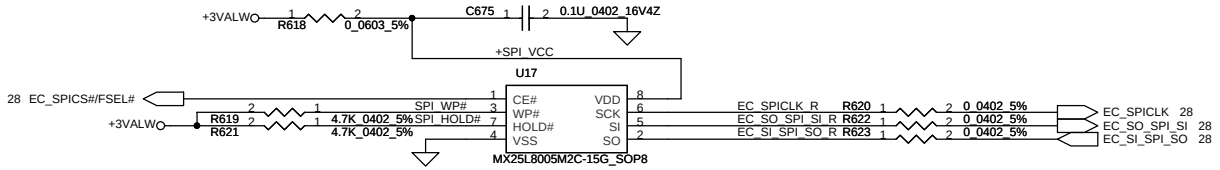
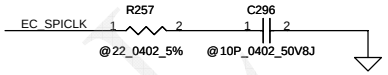
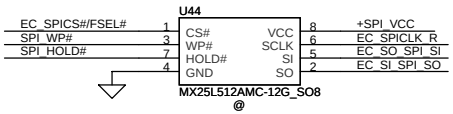


SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P
ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

ONLY MXIC used in this project (66MHz)



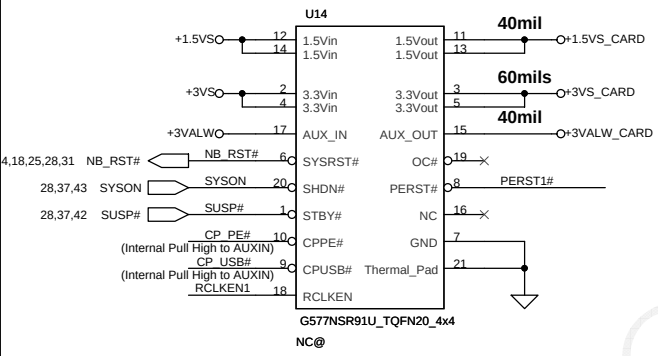


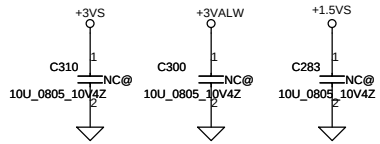
@

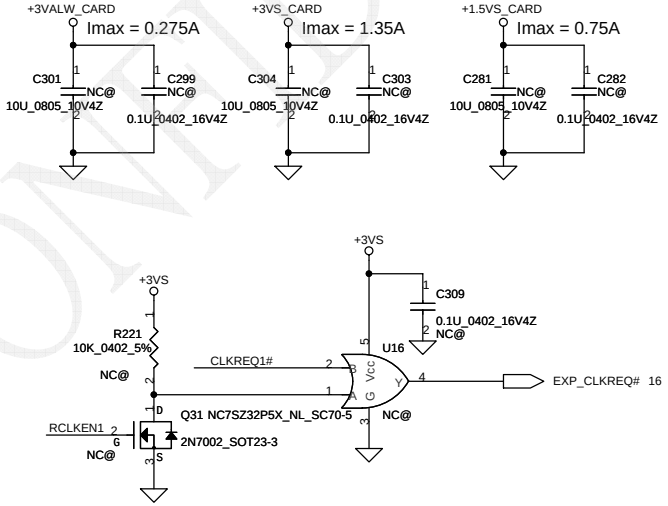
Reserved for BIOS simulator.
Footprint SO8

SPI ROM Footprint 150mil

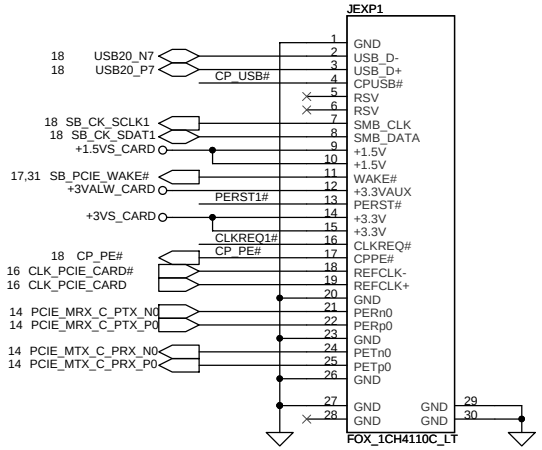
New Card Power Switch







New Card Socket (Left/TOP)



Don't Connect to GND
2008/02/22

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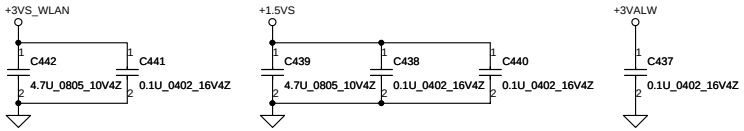
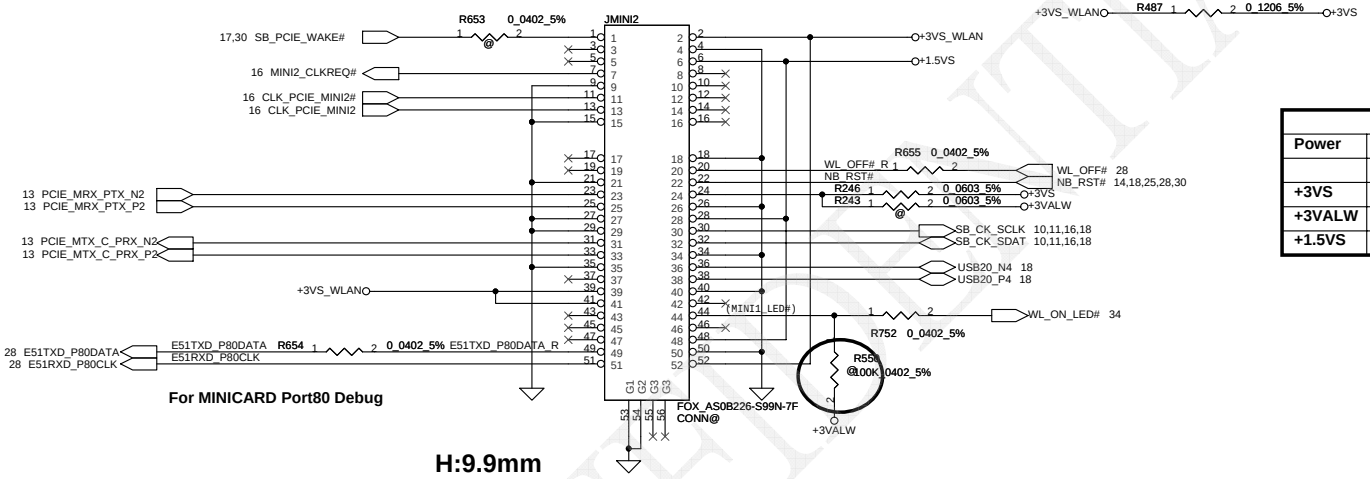


For Wireless LAN



H:9.9mm

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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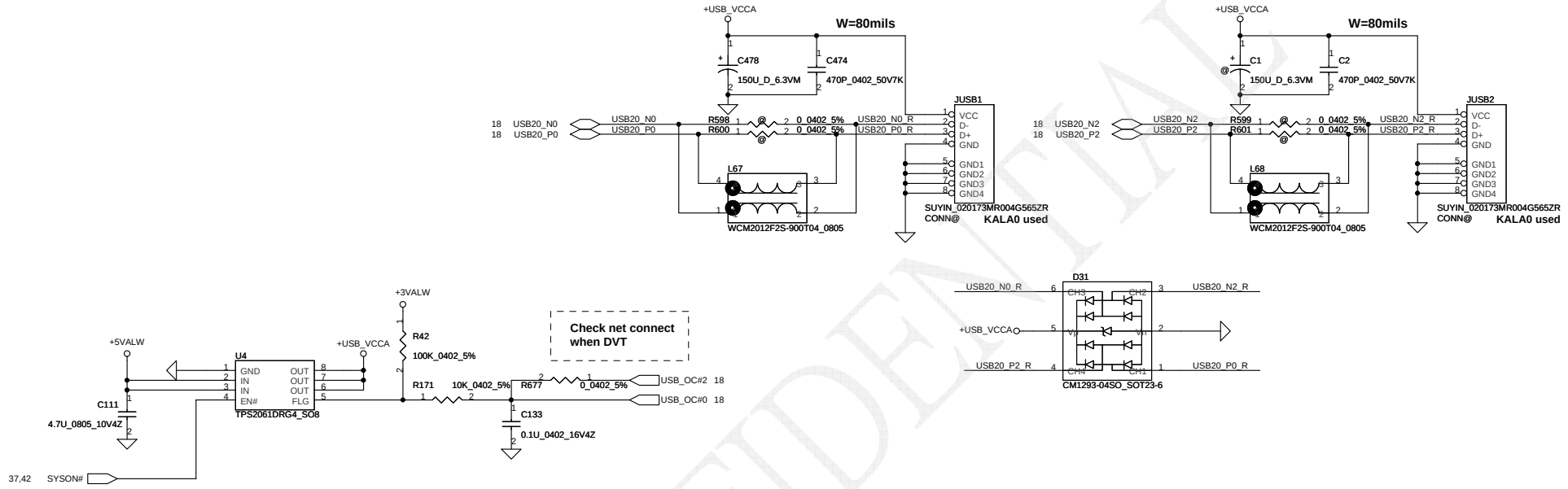
USB CONN. 1 & 2



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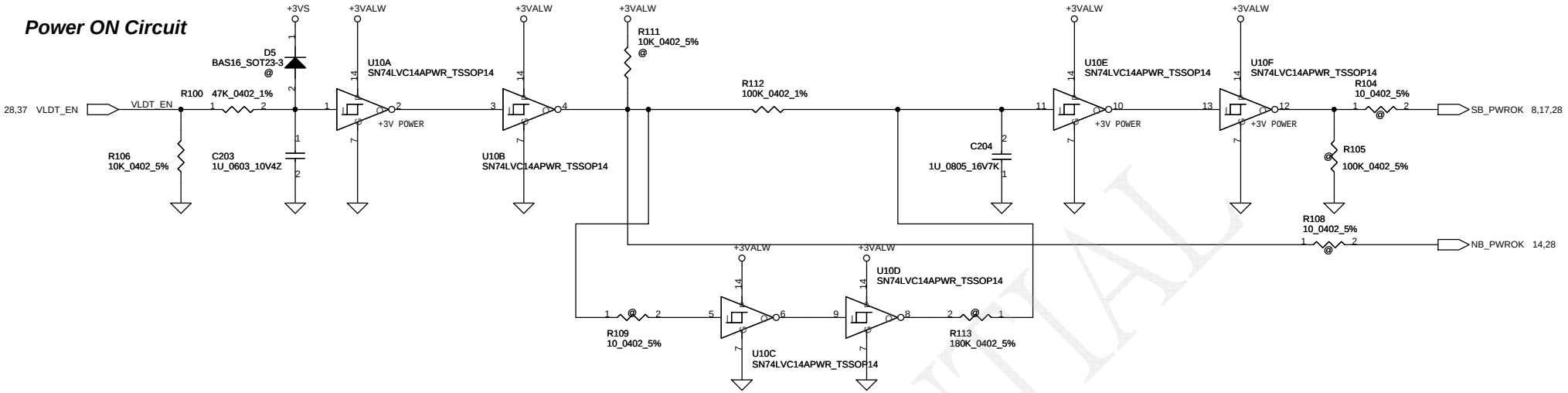
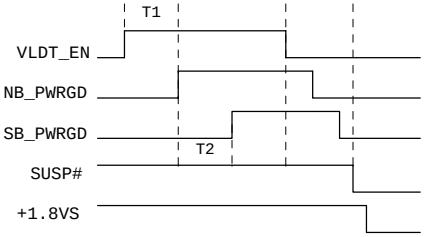
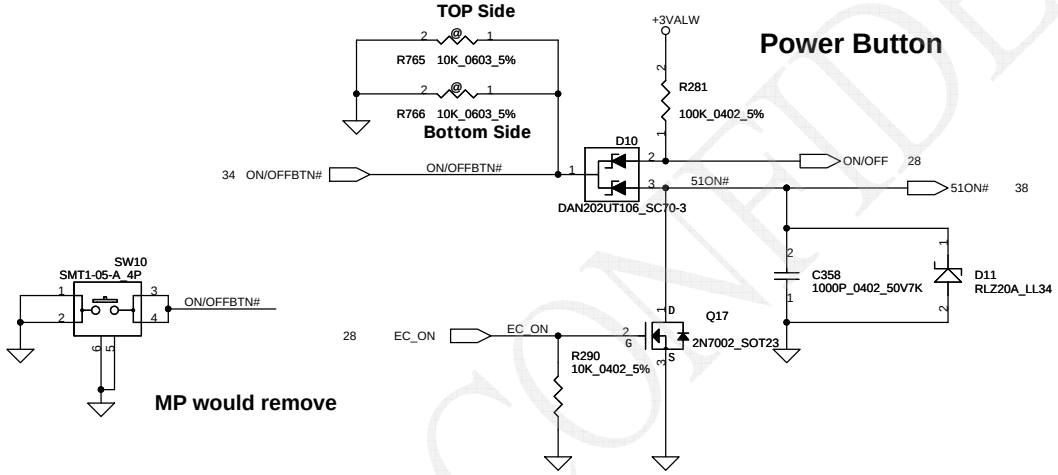
Power ON Circuit



note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



Power Button



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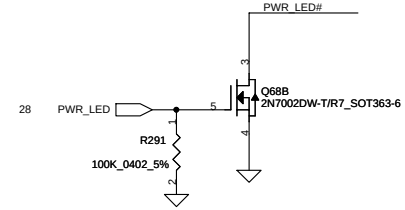
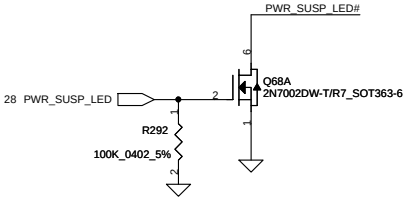
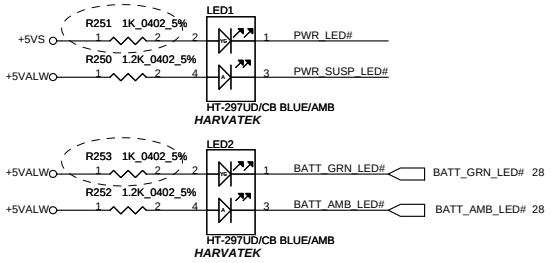
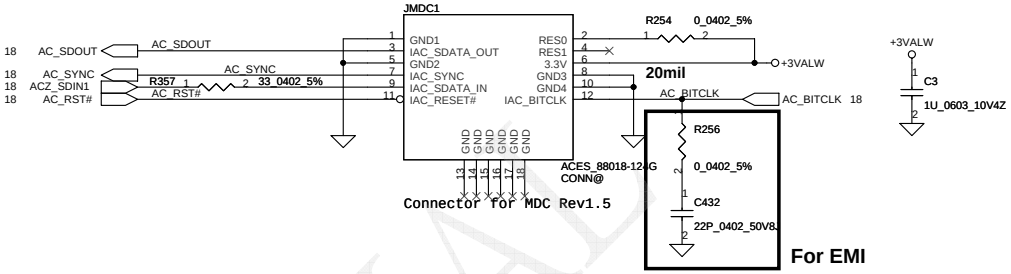




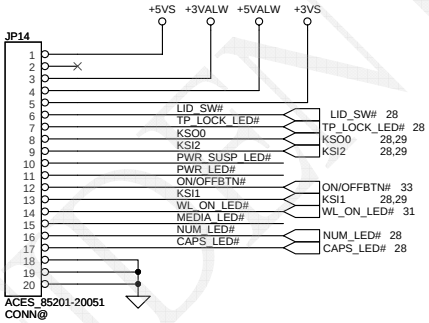


BLUE/AMB LED

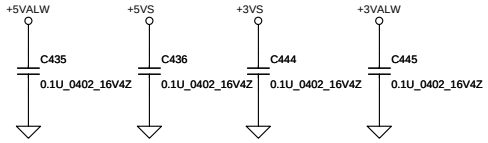
MDC Conn.

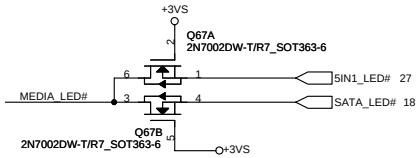


To PWR LED/B



	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	





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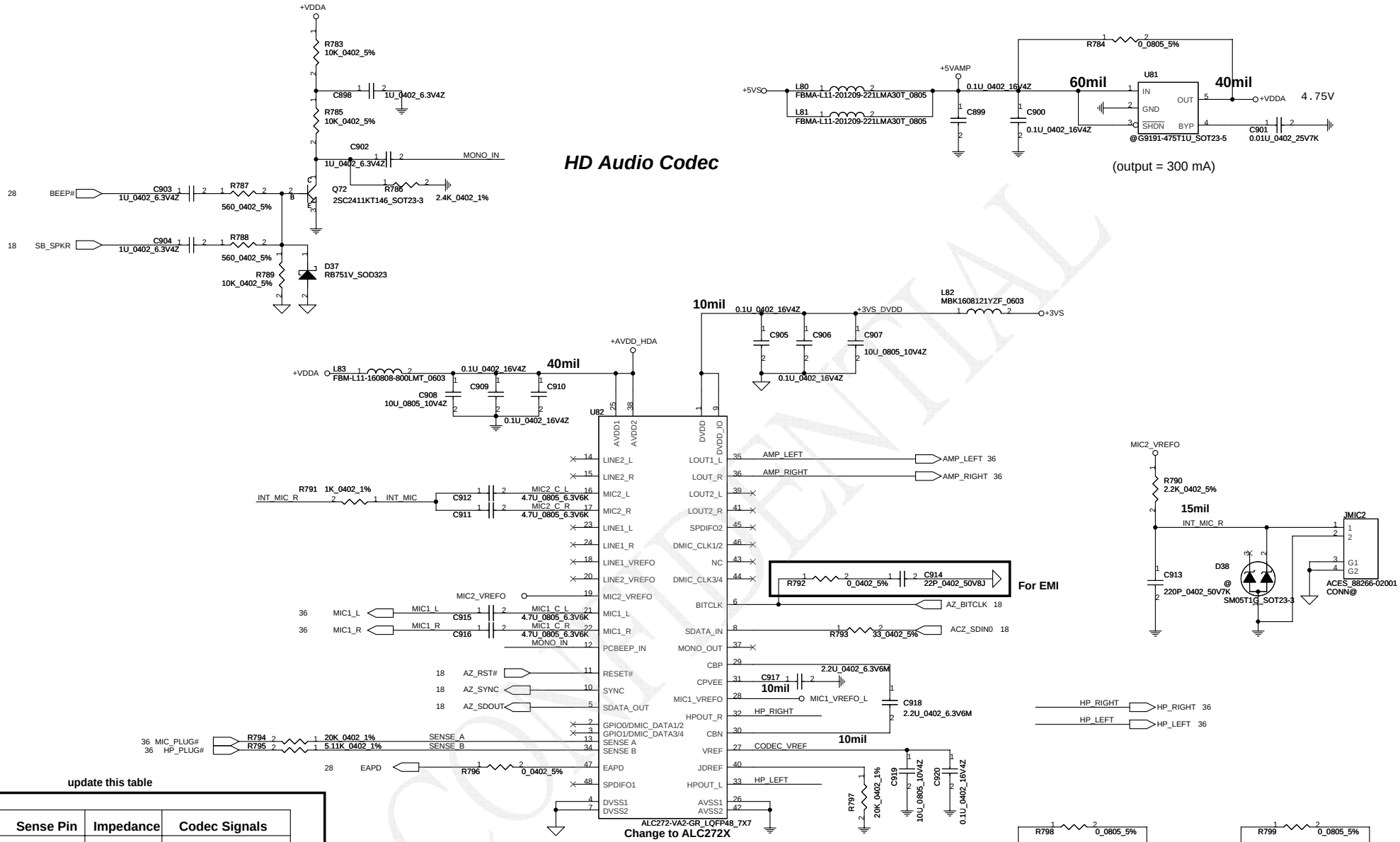

update this table

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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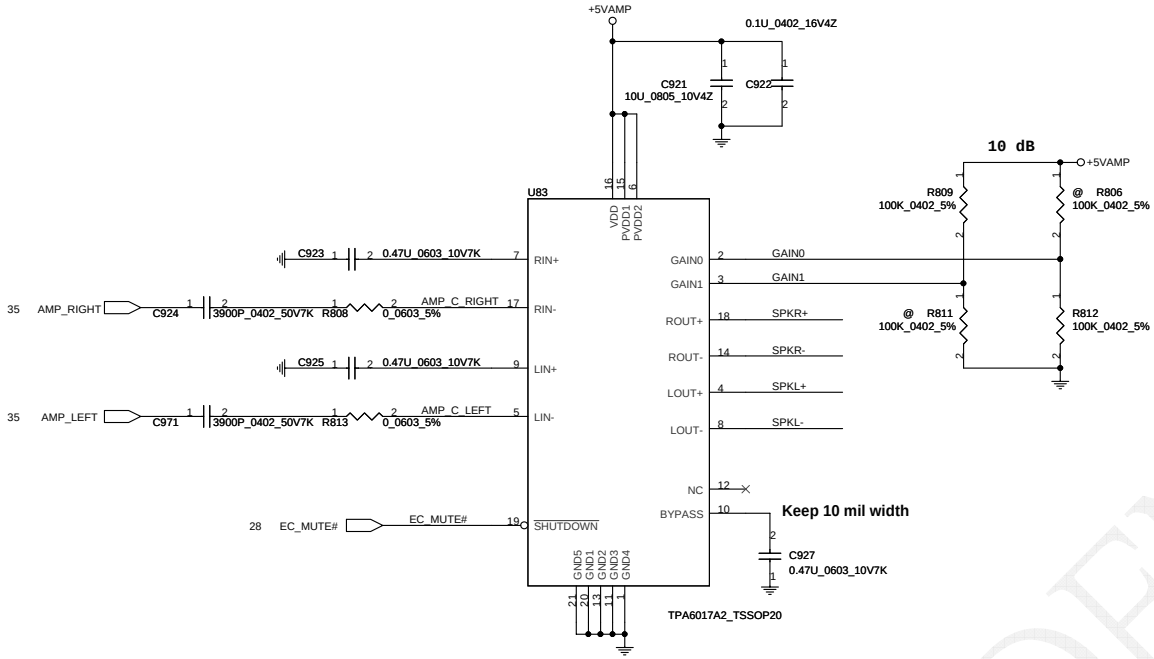
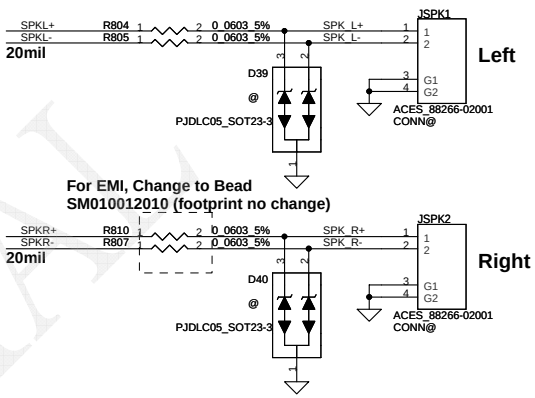
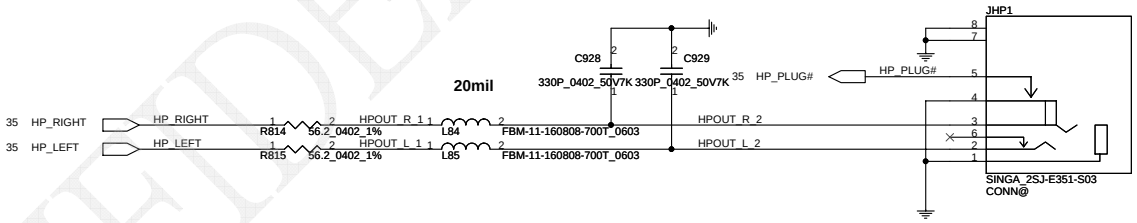


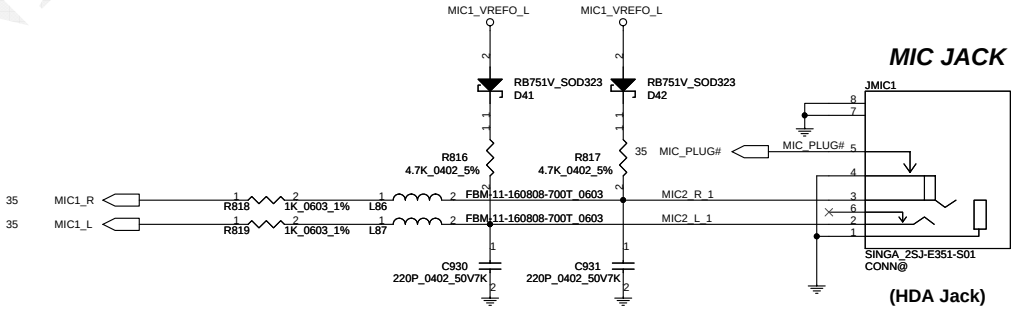
Int. Speaker Conn.



LINE Out/Headphone Out



MIC JACK



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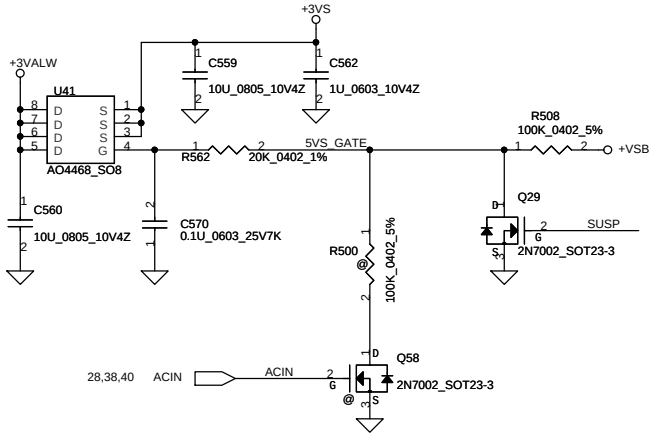
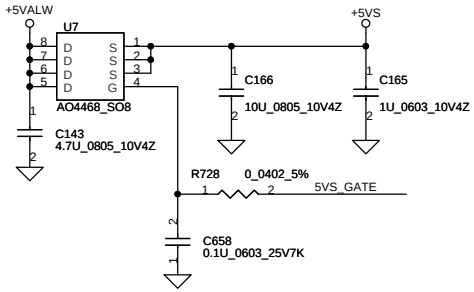
+3VALW TO +3VS

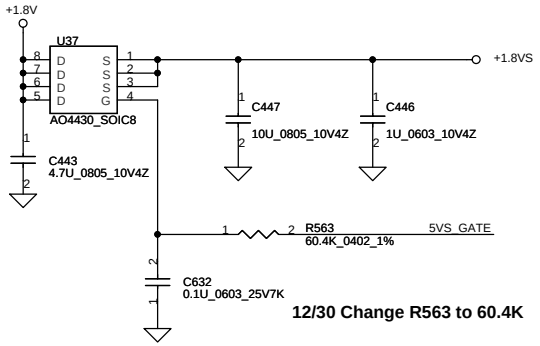


+5VALW TO +5VS



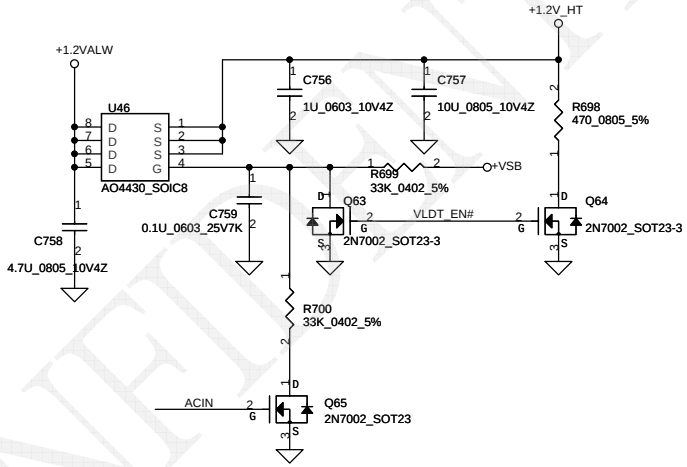
2006/2/22 Add C658 0.1uF

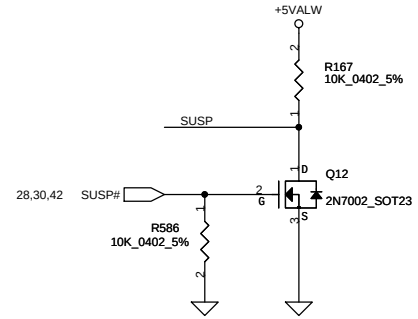
+1.8V TO +1.8VS

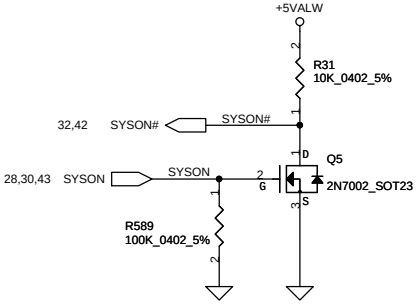


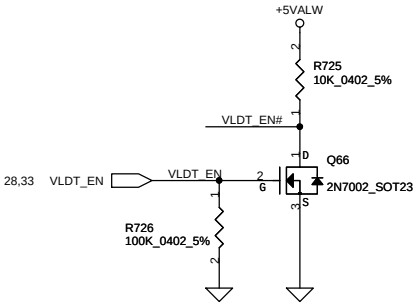
12/30 Change R563 to 60.4K

+1.2VALW TO +1.2V_HT

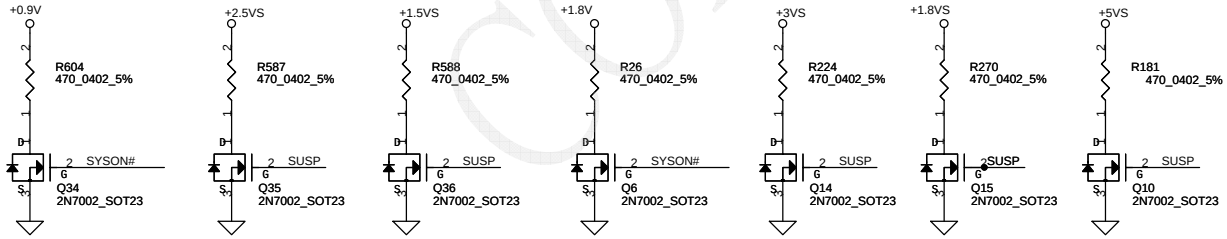








Near PU8 **Near PU12**



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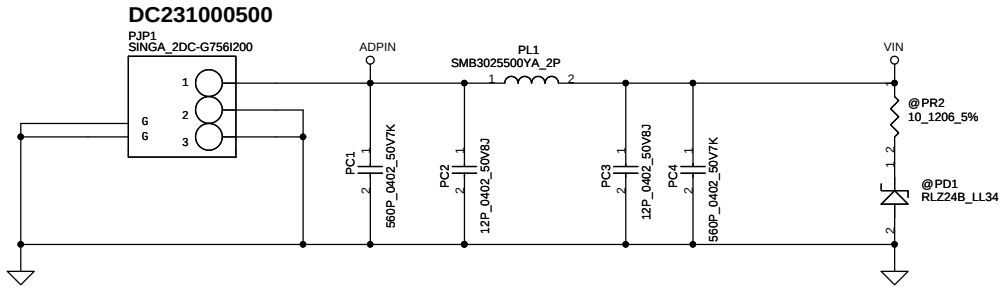
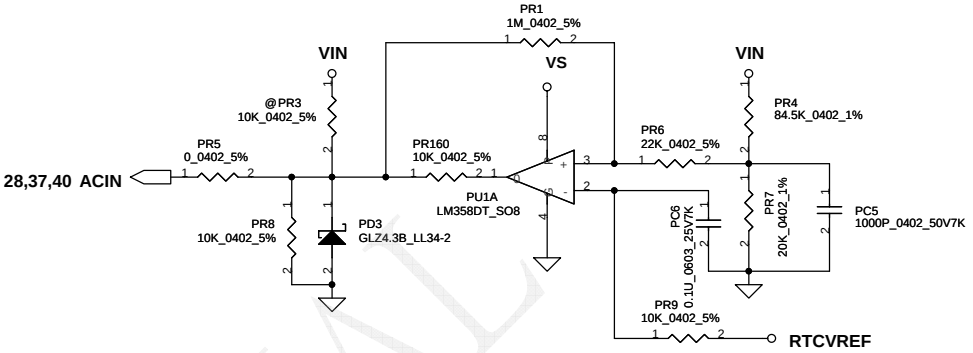
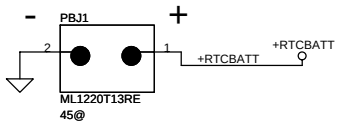
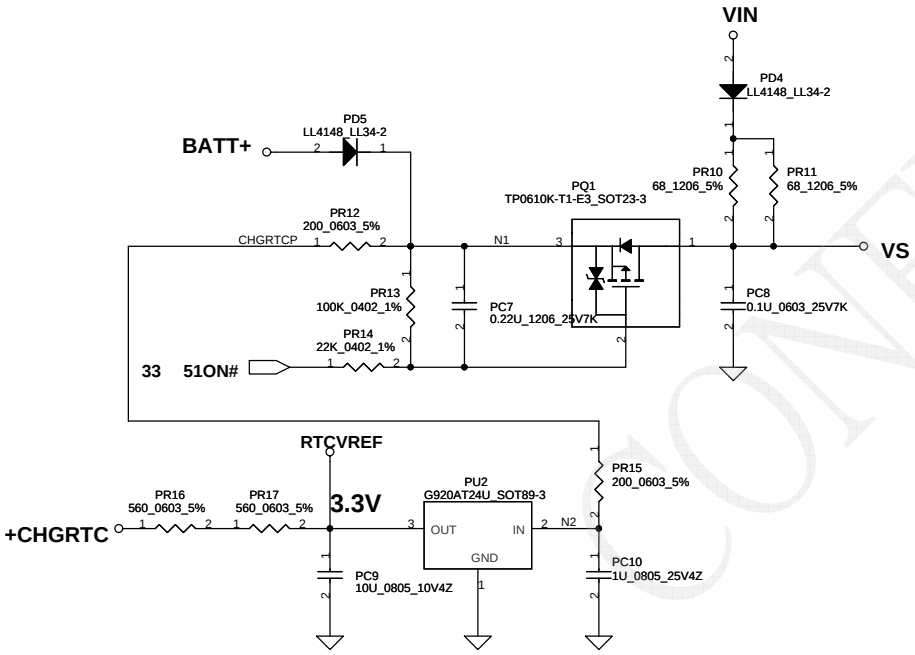


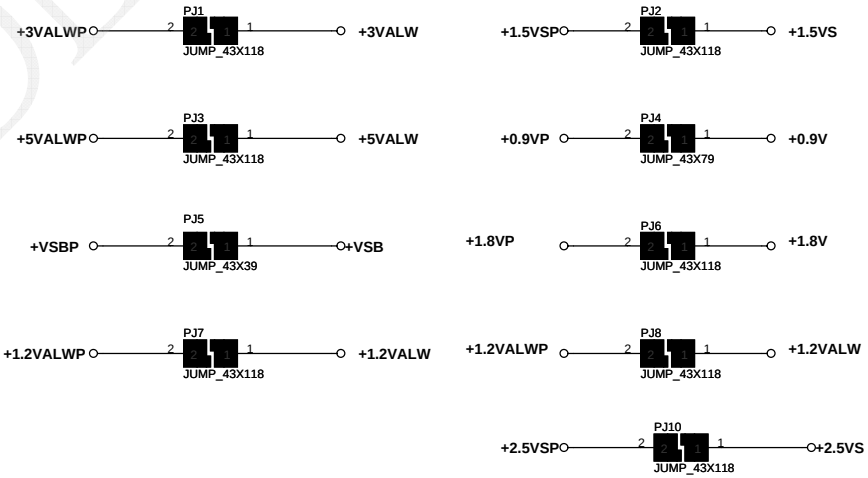




Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V





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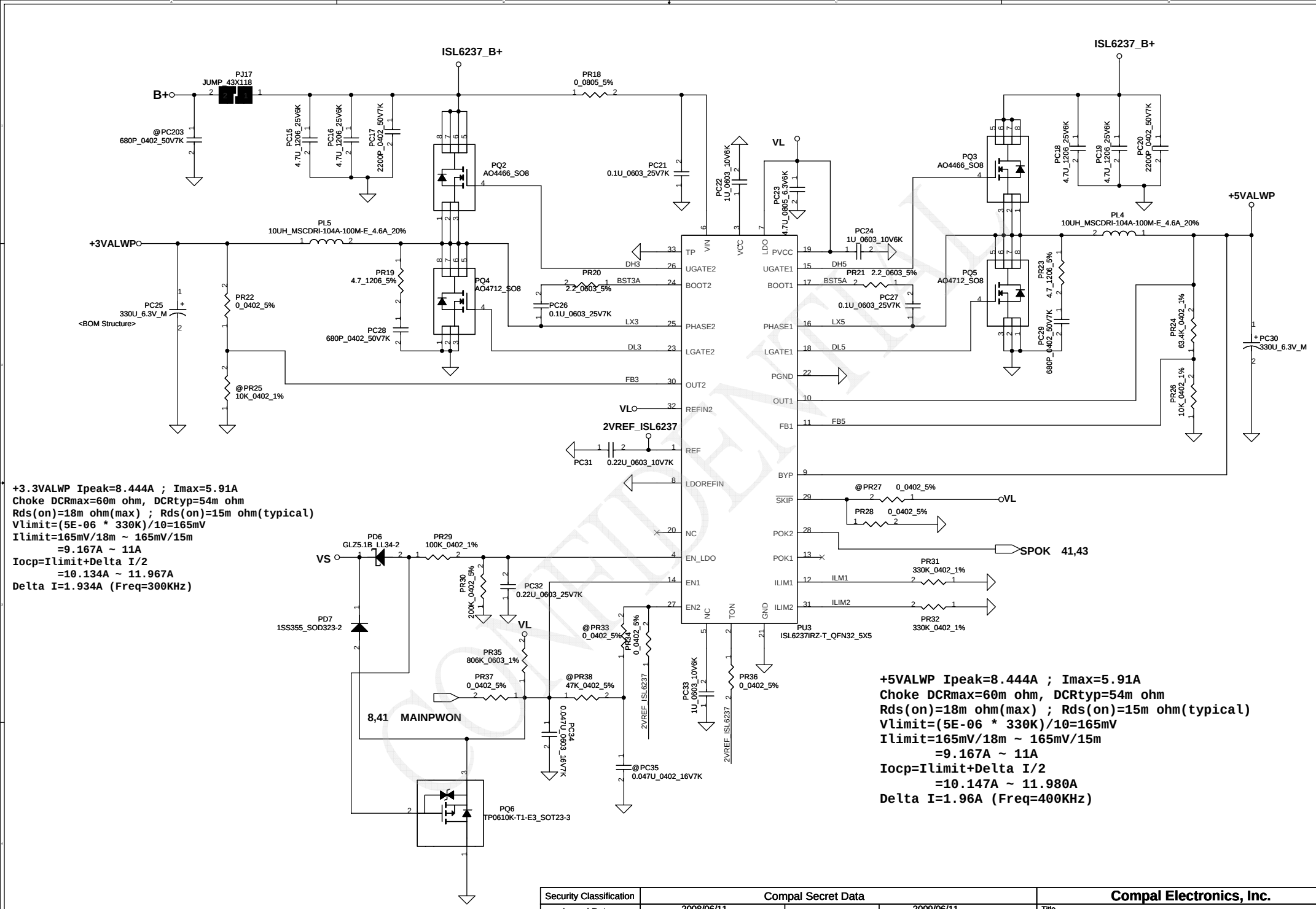

+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.134A ~ 11.967A
Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.96A (Freq=400KHz)

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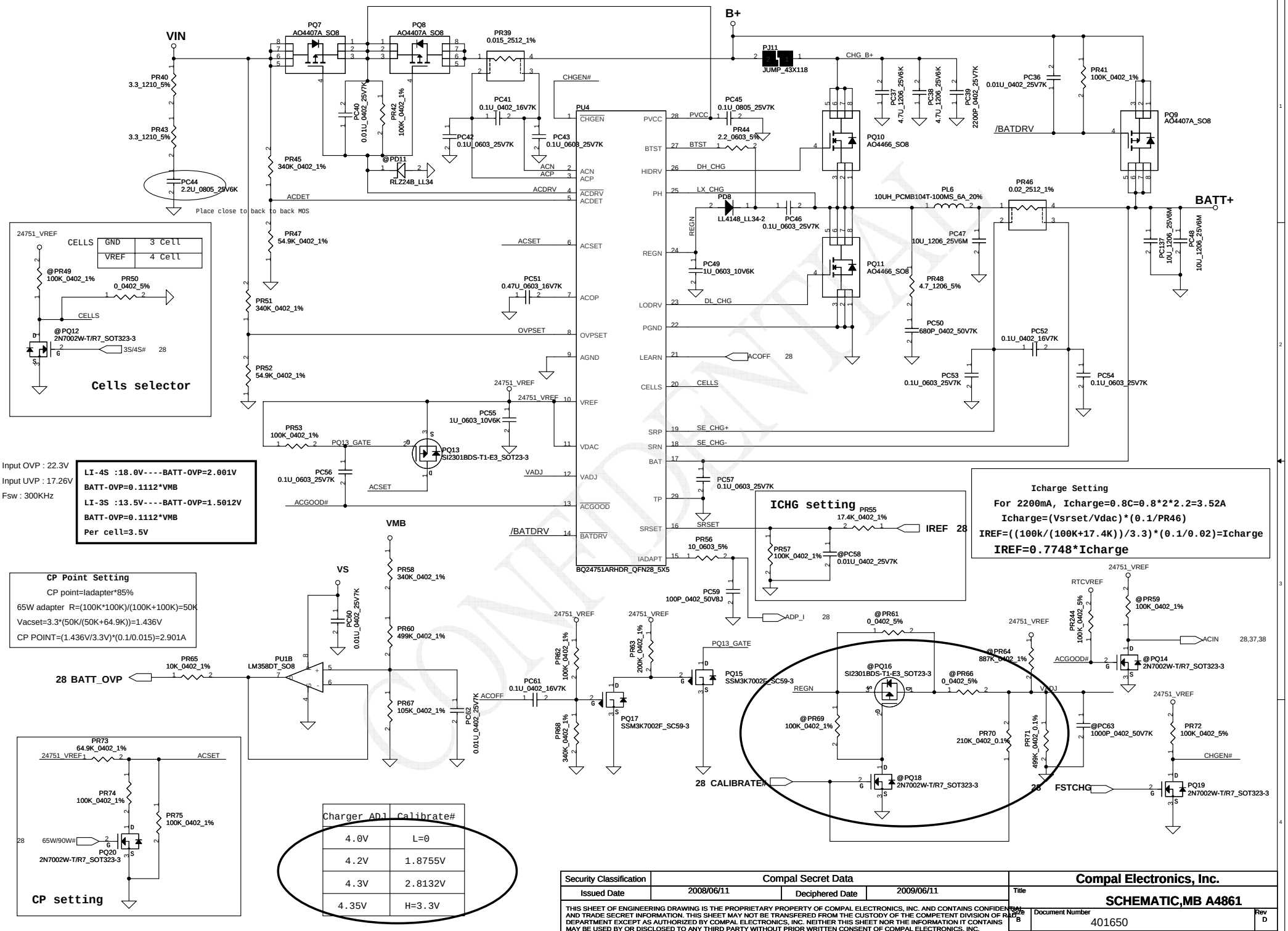
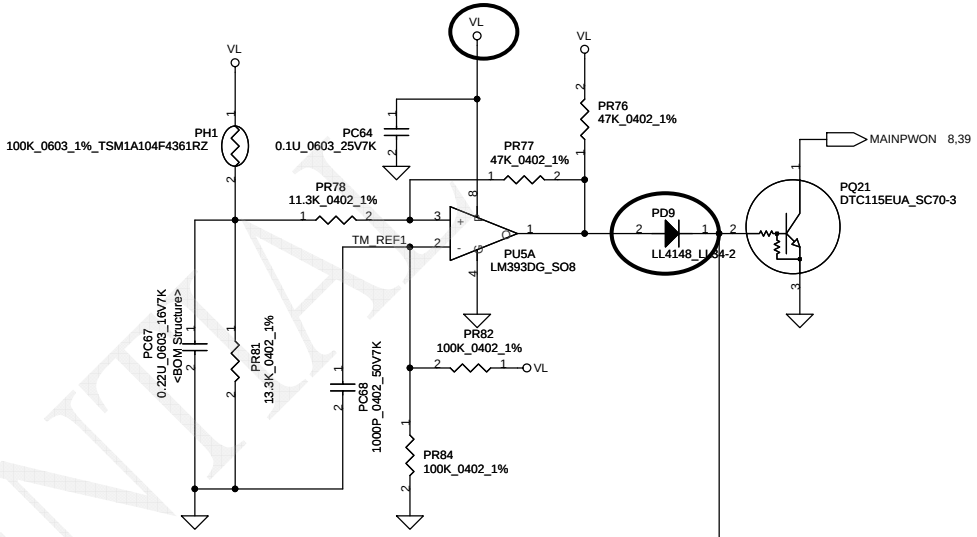
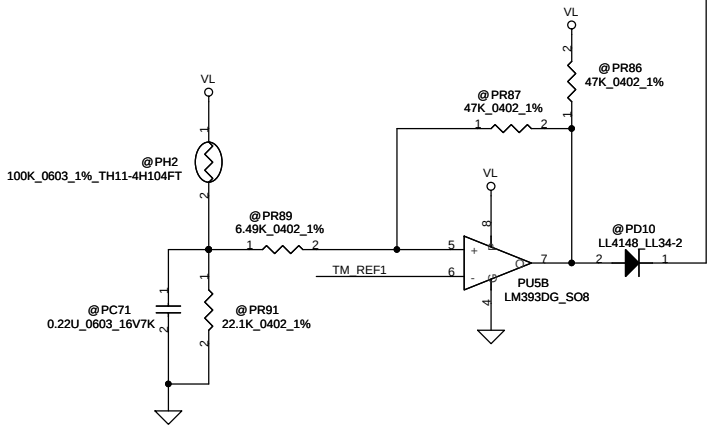
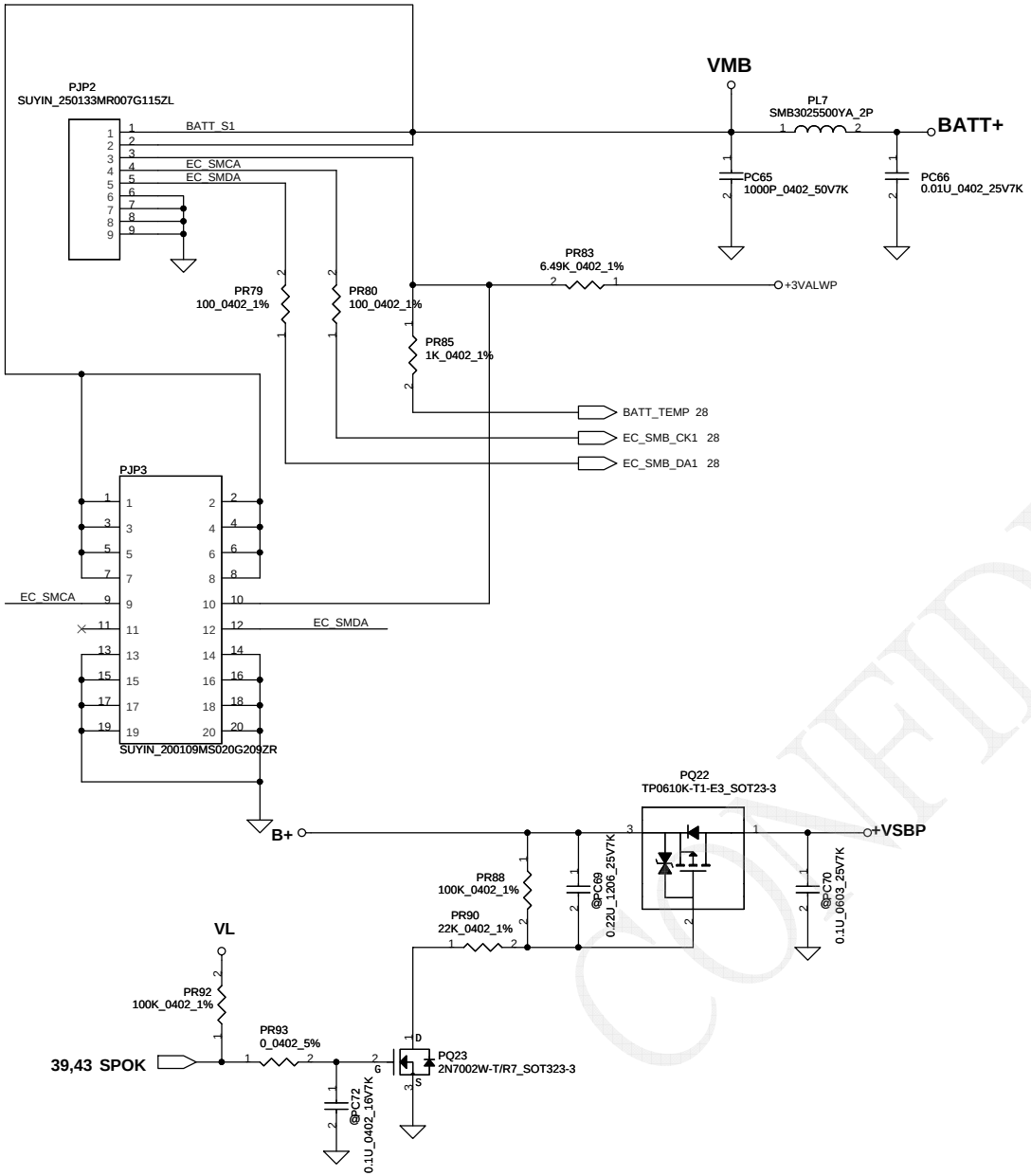


PH1 under CPU botten side :
CPU thermal protection at 92 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 75 degree C





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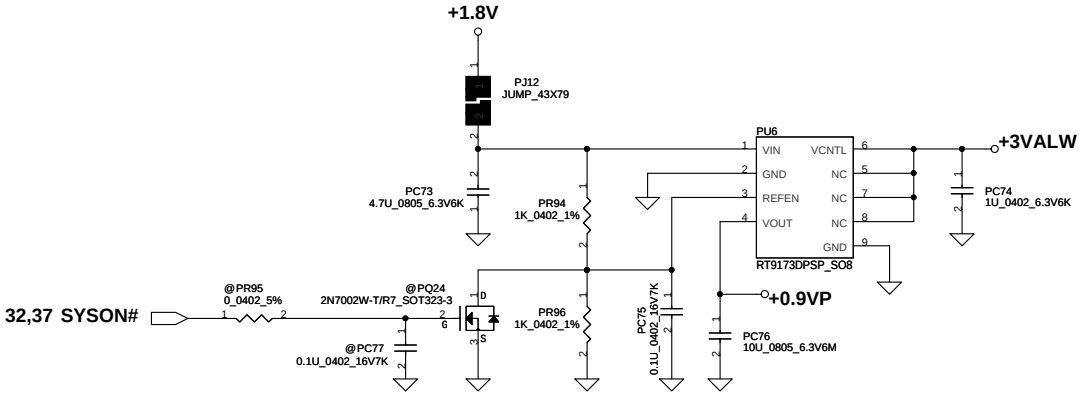

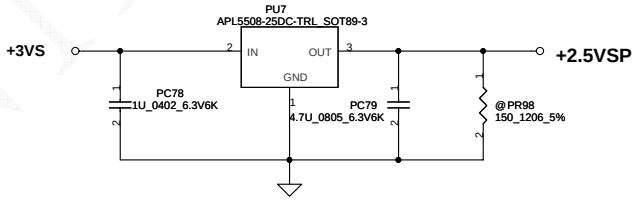

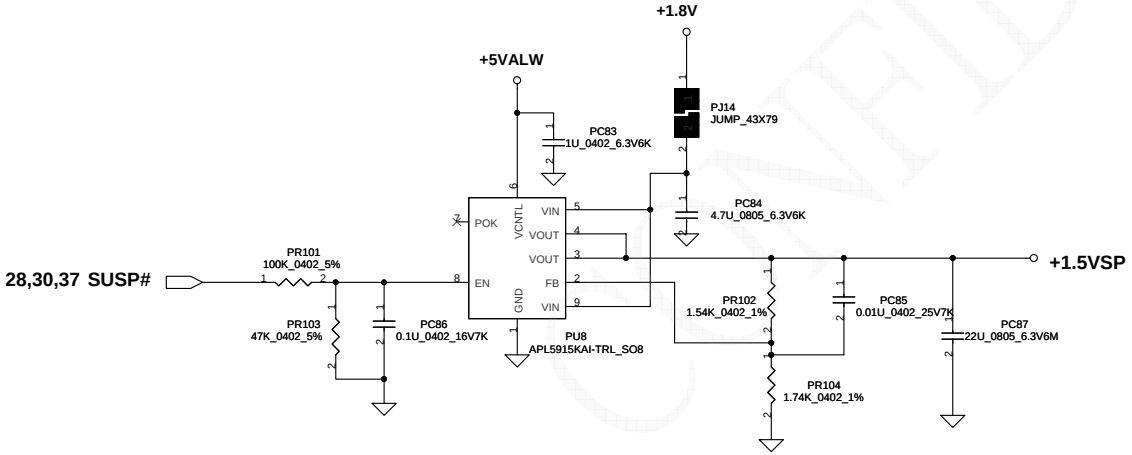

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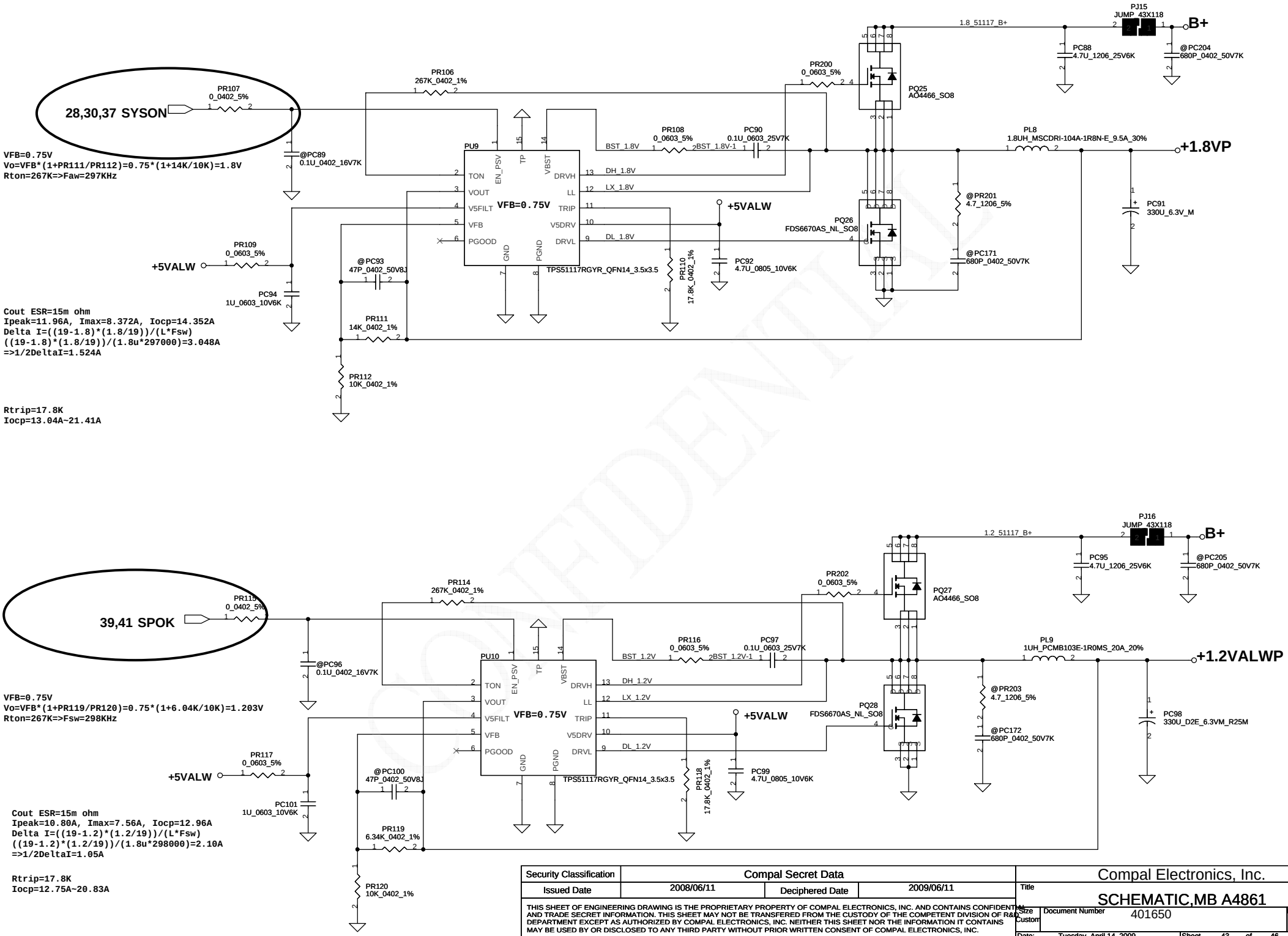

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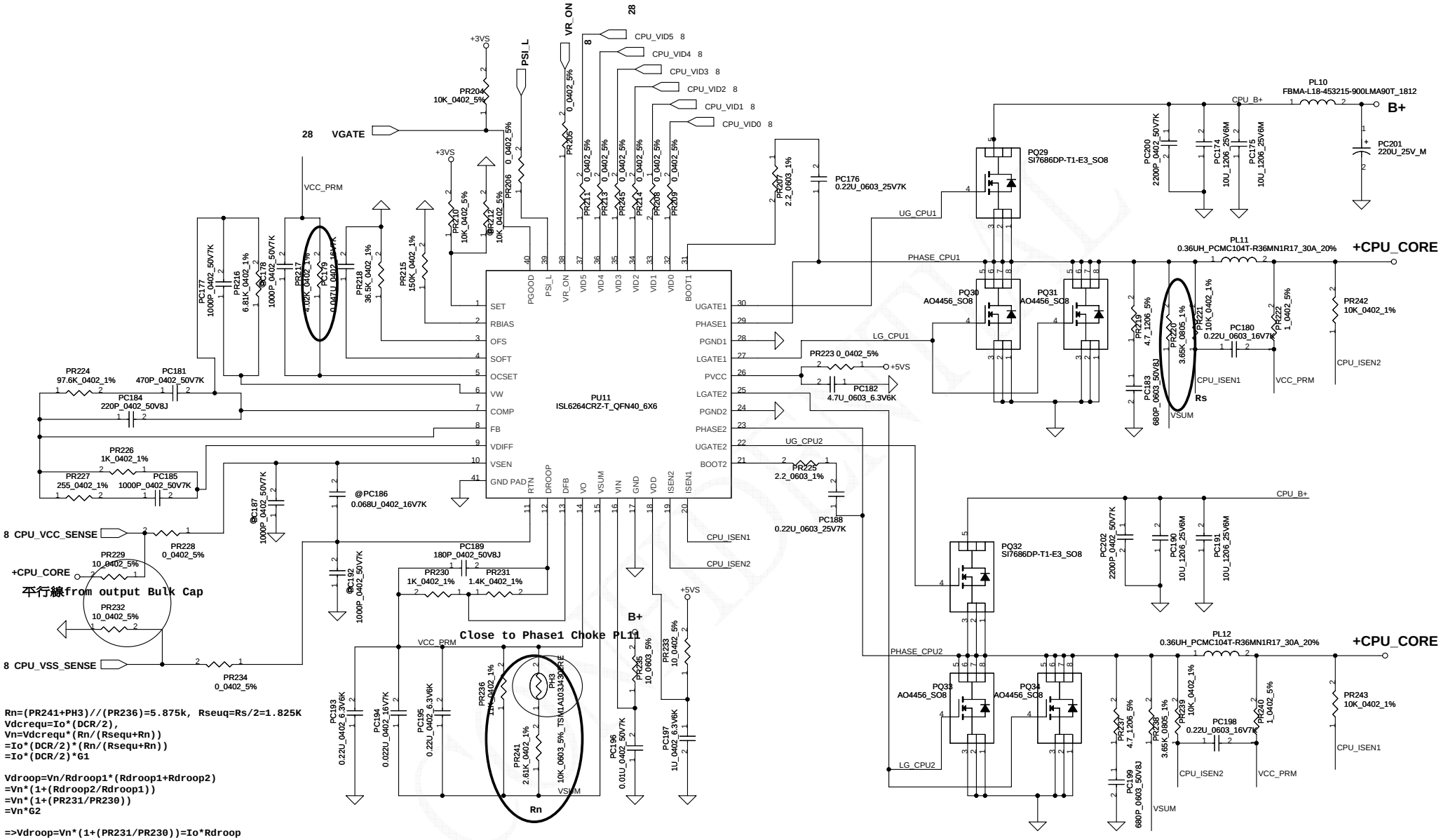


```
Rn=(PR241+PH3)//(PR236)=5.875k, Rseuq=Rs/2=1.825K
Vdcrequ=Io*(DCR/2),
Vn=Vdcrequ*(Rn/(Rsequ+Rn))
=Io*(DCR/2)*(Rn/(Rsequ+Rn))
=Io*(DCR/2)*G1

Vdroop=Vn/Rdroop1*(Rdroop1+Rdroop2)
=Vn*(1+(Rdroop2/Rdroop1))
=Vn*(1+(PR231/PR230))
=Vn*G2

=>Vdroop=Vn*(1+(PR231/PR230))=Io*Rdroop
=>Io*(DCR/2)*G1*G2=Io*Rdroop
=>Rdroop=1.007m ohm

Iocp_min*Rdroop>Rocset*10uA
=>25A*1.007m ohm>Rocset*10uA
=>choose Rocset=2.74K
=>Iocp_min*1.007m ohm>2.74K*10u
=Iocp_min>27.209A

Iocp_max*Rdroop>Rocset*10.4uA
=>Icop_max>28.297A

Iocp=~27.209A~28.297A
```

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Customer changed CPU to TF36/38.	TF36/38 is 31W CPU, must change MOS to 1H2L.	0.1	44	Add PQ31 and PQ34 SB000009F80(S TR AO4456 1N SO8)	08, 11/13	to DVT
2	Change CP OCP setting.	TF36/38 CPU OCP setting change.	0.1	44	Change PR198 to SD034402180(S RES 1/16W 4.02K 0402 1%)	08, 11/13	to DVT
3	S3 Mode issue.	Because APL5915 has 0.4V enable voltage, so add PR103 to pull down enable voltage when system in S3 mode	0.1	42	Add PR103 SD028470280(S RES 1/16W 47K 0402 5%)	08, 11/13	to DVT
4	AMD issue.	AMD request add 1.2V to 1.22V for chipset.	0.1	43	Change PR119 from SD034604180 to SD034634180.	08, 11/17	to DVT
5	EMI issue.	EMI request add charger snubber.	0.1	40	Add PR48 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC50 SE074681K80(S CER CAP 680P 50V K X7R 0402)	08, 11/17	to DVT
6	Cost issue.	Cost issue.	0.1	44	Change PC201 from SF000000G80(S ELE CAP 220U 25V M HA0 MVY) to SF22004M210(S ELE CAP 220U 25V M 8X10.2 CE-AX)	08, 11/17	to DVT
7	Support charge voltage.	Support charge voltage.	0.1	40	Delete PQ18 SB000006800(S TR 2N7002W T/R7 1N SOT-323)	08, 11/26	to DVT
8	Support charge voltage.	Support charge voltage.	0.1	40	Delete PQ16 SB923010020(S TR SI2301BDS-T1-E3 1P SOT23)	08, 11/26	to DVT
9	Support charge voltage.	Support charge voltage.	0.1	40	Delete PR66 SD028000080(S RES 1/16W 0 0402 5%)	08, 11/26	to DVT
10	Support charge voltage.	Support charge voltage.	0.1	40	Delete PR69 SD034100380(S RES 1/16W 100K 0402 1%)	08, 11/26	to DVT
11	Support charge voltage.	Support charge voltage.	0.1	40	Delete PC63 SE074102K80(S CER CAP 1000P 50V K X7R 0402)	08, 11/26	to DVT
12	Support charge voltage.	Support charge voltage.	0.1	40	Add PR70 SD034210380(S RES 1/16W 210K 0402 1%)	08, 11/26	to DVT
13	Support charge voltage.	Support charge voltage.	0.1	40	Add PR71 SD034499380(S RES 1/16W 499K 0402 1%)	08, 11/26	to DVT
14							
15							
16							
17							
18							

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Version change list (P.I.R. List) for HW

Item	Reason for change	Modify List	Rev.	PG#
1	Material Change	Change U1 to APL5607	DVT	P06
2	Material Change	Change U85 to AR8132	DVT	P25
3	8132 issue, OS black screen	Change L90 to R546 (0_0805)	DVT	P25
4	Circuit issue	Add R677	DVT	P32
5	RT5159 ID issue	Pop R680 to 0_0402_5%	DVT	P27
6	[EMI] Camera co-layout choke	Change R759,R760 to 0_0402 Reserve L77	DVT	P24
7	[Cost Down] audio LDO	Reserve U81 Pop784	DVT	P35
8	RT5159 unkow issue	Reserve R548, pop R547	DVT	P27
9	[ESD]	Pop D39,D40	DVT	P36
10	[ESD]	Pop D14,D15	DVT	P36
11	[ESD]	Pop D16	DVT	P29
12	[EMI]	Reserve C859 for EMI	DVT	P27
13	Modify PWR Sequence	Reserve R104,R108 Pop R658,R652	DVT	P34 P28
14	[EMI]	Reserve C861 for EMI	DVT	P16
15	Material Change	Change JRJ1 type	DVT	P26
16	Material Change	Change C924,C971 to 3900pF_0402	DVT	P36
17	[EMI]	Reserve C350,C352,C353,C354	DVT	P15
18	[EMI]	Pop R673 to 10ohm_0402 Pop C858 to 10pF_0402	PVT	P27
19	[EMI]	Pop C859 to 0.1uF_0402	PVT	P27
20	[EMI]	Pop C350,C352,C353,C354 to 0.1uF_0402	PVT	P15
21	Material Change	Change R251,R253 to 1.1Kohm Change R250,R252 to 1.2Kohm	PVT	P34
22	Material Change	Change Y2 footprint to correct	PVT	P18
23	Material Change	Only cChange R810,R807 P/N to SM010012010	PVT	P36
24	Circuit Change	Reserve PWN FAN function. Add R247,R40,JP38	PVT	P06
25	Material Change	Change R814,R815 to 56.2ohm_0402	PVT	P36
26	Material Change	Change U82 to ALC272X-GR (SA00002CI20)	PVT	P35
27	Material Change	Change U27 to KB926QFD3 (SA00001J580)	PVT	P28
28	Material Change	Change U85 to AR8132M-AL1E (SA000034V00)	PVT	P25
29	Material Change	Change U85 to AR8132-AL1E (SA000036Y00)	Pre-PVT	P25
30	BOM change	Del D13,D4	Pre-PVT	P06
31	ESD Cost down	Del D16,D39,D40	Pre-PVT	
32	ESD Cost down	Change D15 to SCA00000200	Pre-PVT	
33	BOM change	Change R251,R253 to 1K	Pre-PVT	

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