

Compal Confidential

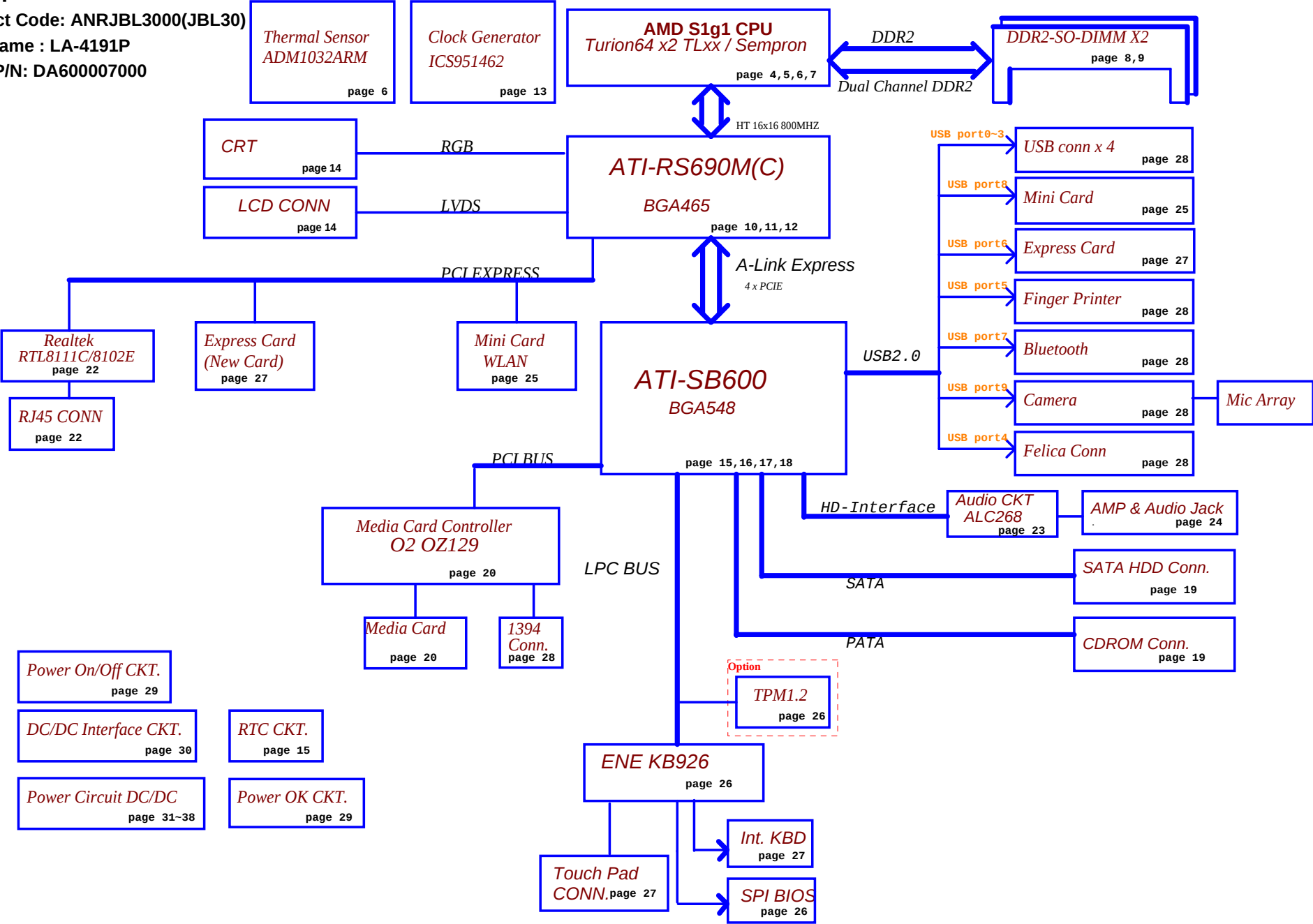
Schematics Document

AMD S1/ ATI RS690MC / SB600
2007 / 1 / 10 Rev:0.3

Security Classification	Compal Secret Data			Title	
Issued Date	2008/1/3	Deciphered Date	2009/01/3	Cover Sheet	
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				Document Number	LA-4191P
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Compal confidential

Project Code: ANRJBL3000(JBL30)
File Name : LA-4191P
PCB P/N: DA600007000



Security Classification	Compal Secret Data			Title	
Issued Date	2008/1/3	Deciphered Date	2009/01/3	Block Diagrams	
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Power Plane	Description	S1	S3	S4/ S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.2VALW	1.2V always on power rail	ON	ON	ON
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Device	IDSEL#	REQ#/GNT#	Interrupts
OZ129	AD21	0	PIRQG

Device	Address	Device	Address
Smart Battery	0001 011X b?	ADM1032	1001 110X b?
EEPROM(24C16/02)	1010 000X b?		
(24C04)	1011 000Xb?		

Device	Address
Clock Generator (ICS 951462AGT)	1101 001Xb?
DDRII DIMM0	1001 000Xb?
DDRII DIMM2	1001 010Xb?

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1 0.2
1	0.3
2	
3	
4	
5	
6	
7	

[illegible]

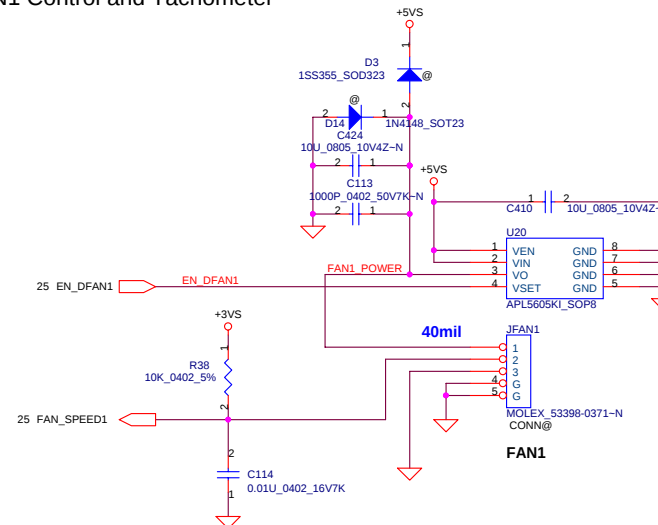
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VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



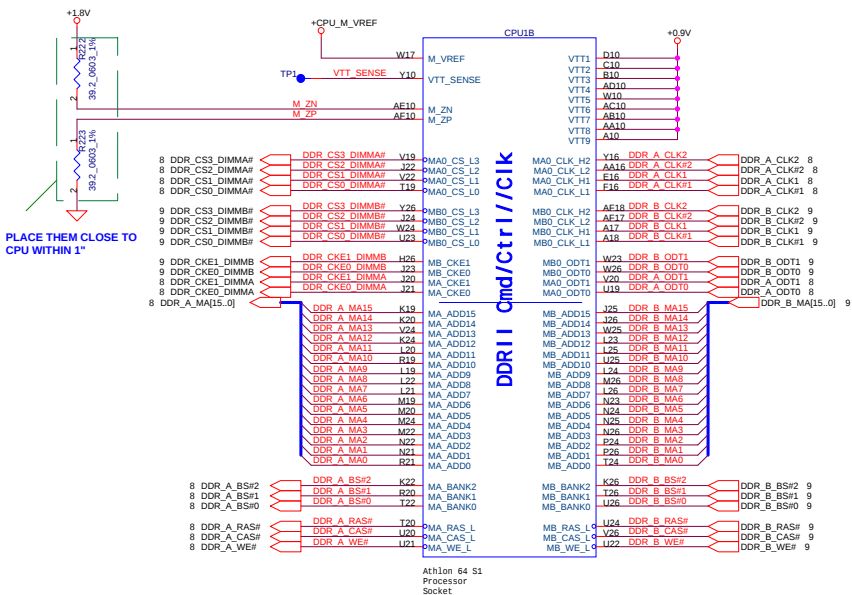
LAYOUT: Place bypass cap near CPU socket
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY
TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY
TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS



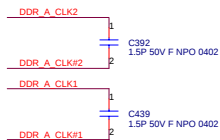
Security Classification		Compal Secret Data		Compal Electronics, Inc. TURION64 HT I/F & FAN	
Issued Date	2008/1/3	Deciphered Date	2009/01/3	Title	
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VDD VTT SUS_CPU IS CONNECTED TO THE VDD VTT SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

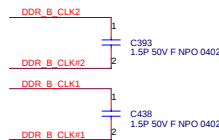
Processor DDR2 Memory Interface



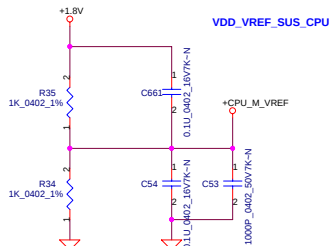
PLACE THEM CLOSE TO CPU WITHIN 1"



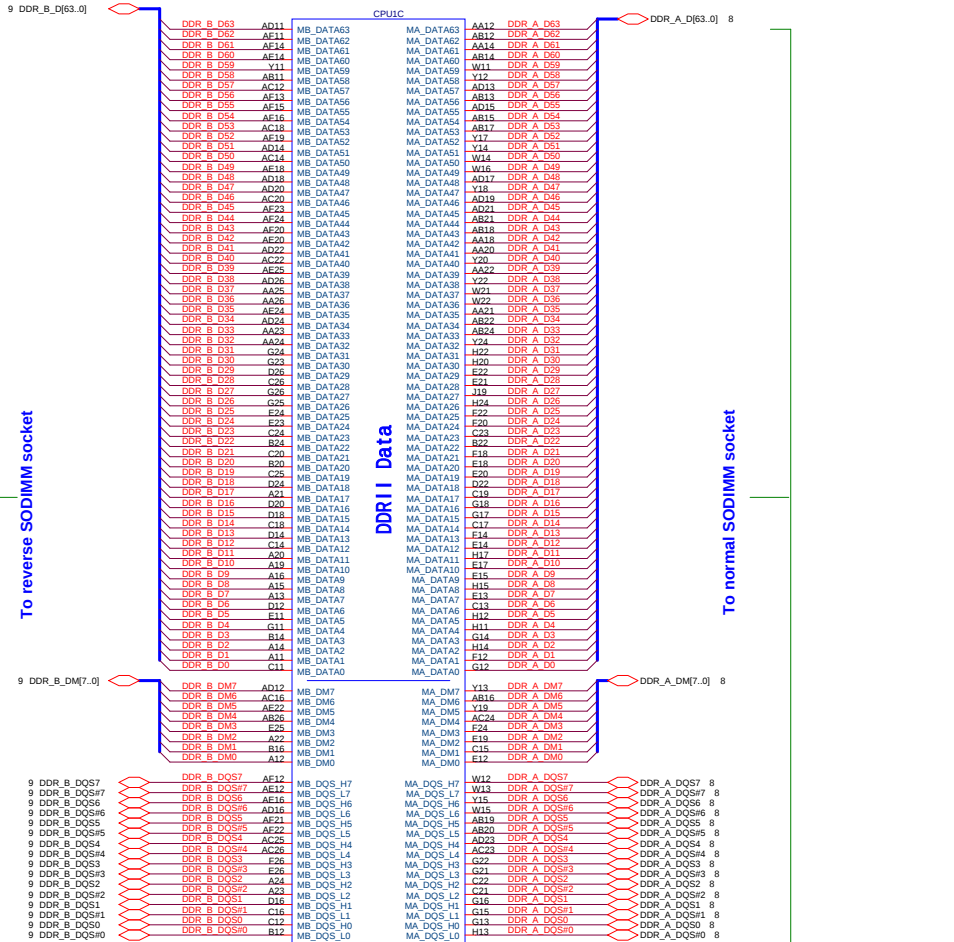
PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH



PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH



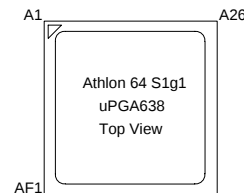
LAYOUT: PLACE CLOSE TO CPU



To reverse SODIMM socket

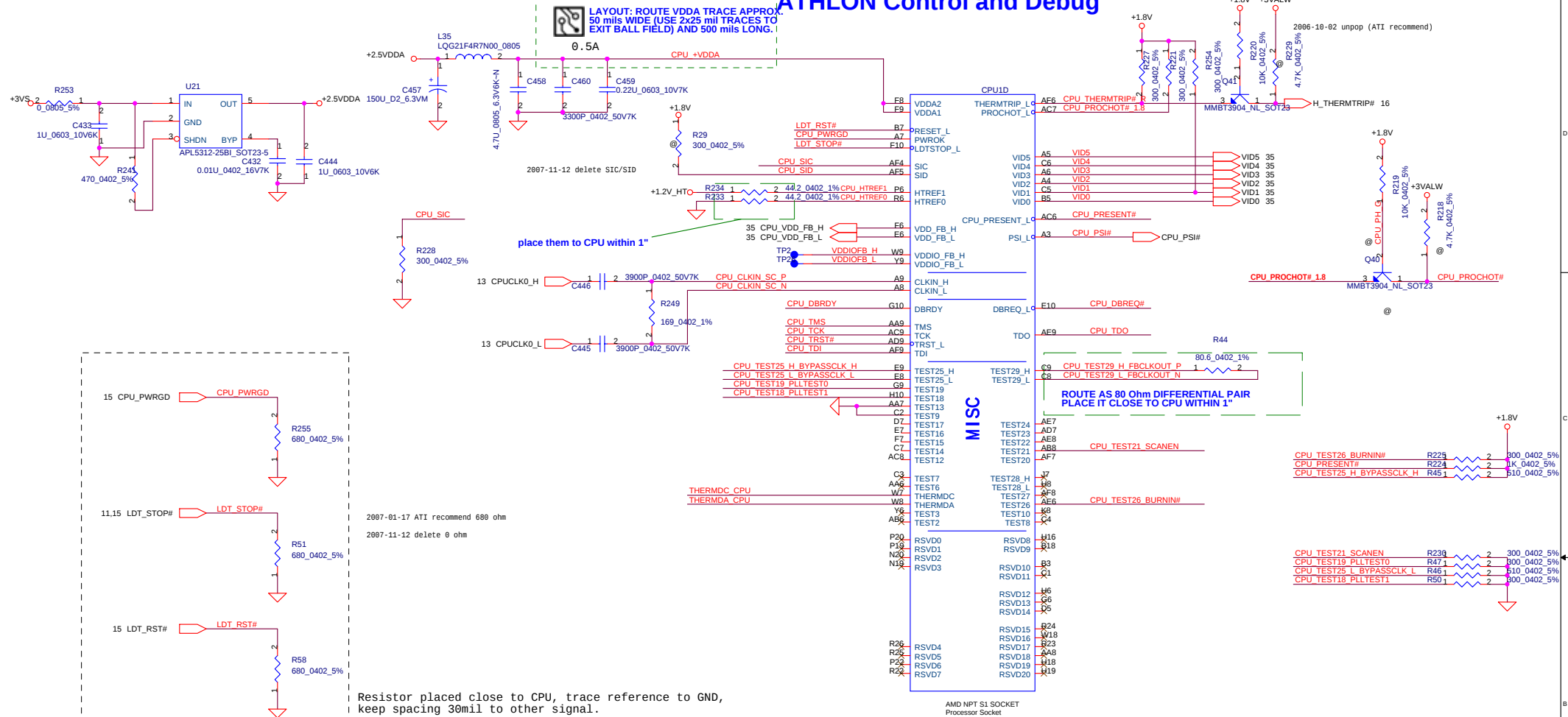
To normal SODIMM socket

Athlon 64 S1 Processor Socket

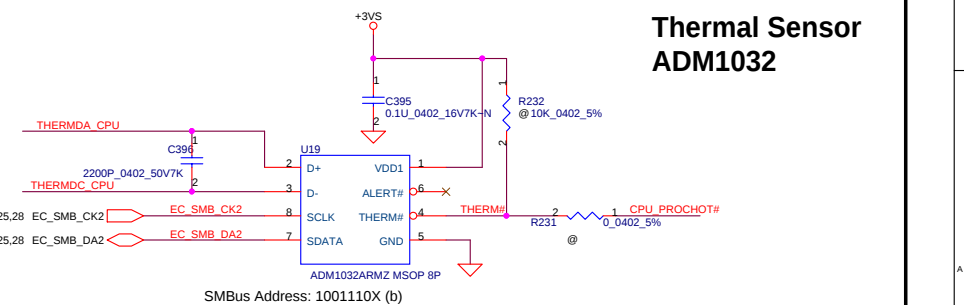
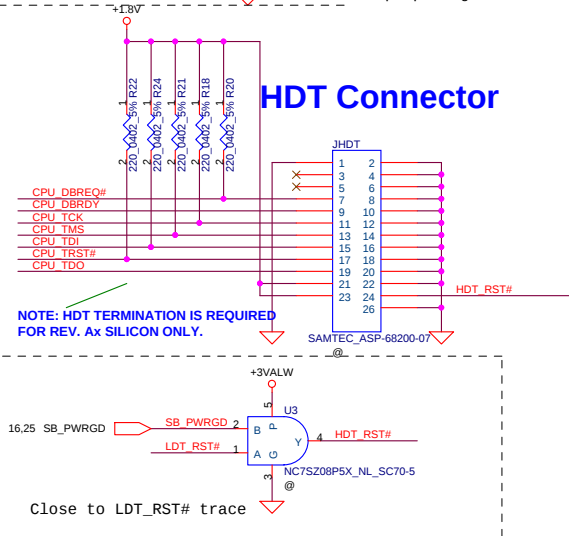


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Issued Date	2008/1/3	Deciphered Date	2009/01/3	TURION64 DDRII MEMORY I/F	
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ATHLON Control and Debug

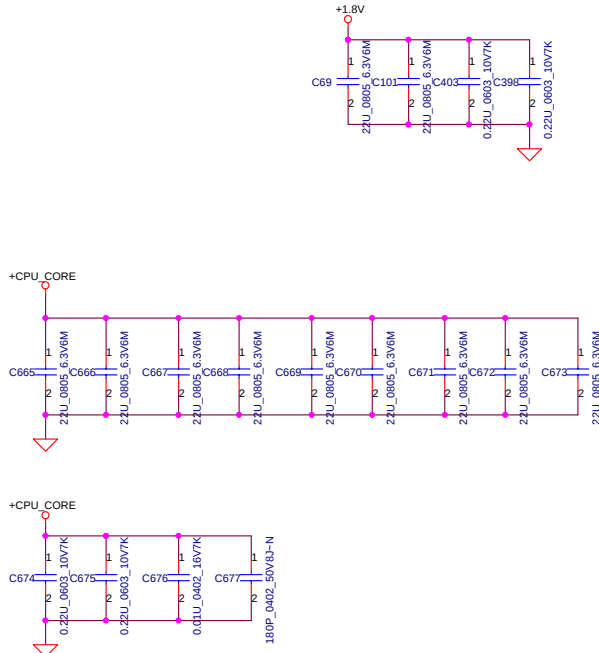


HDT Connector

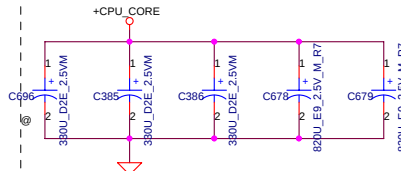
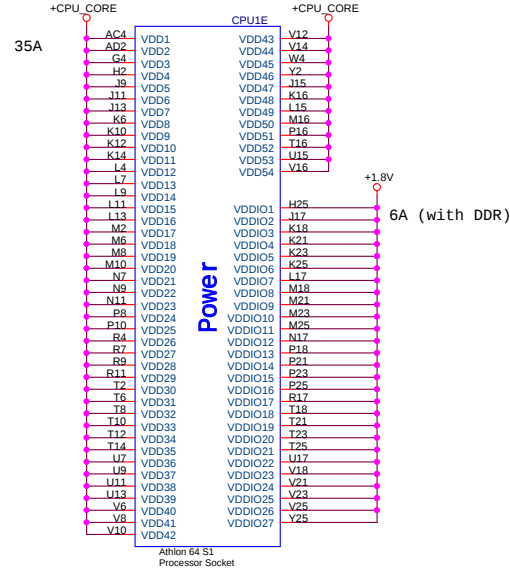
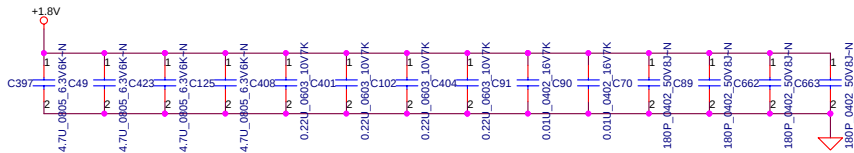


Security Classification	Compal Secret Data			Compal Electronics, Inc. TURION64 CTRL & ADM1032		
Issued Date	2008/1/3	Deciphered Date	2009/01/3	Title		
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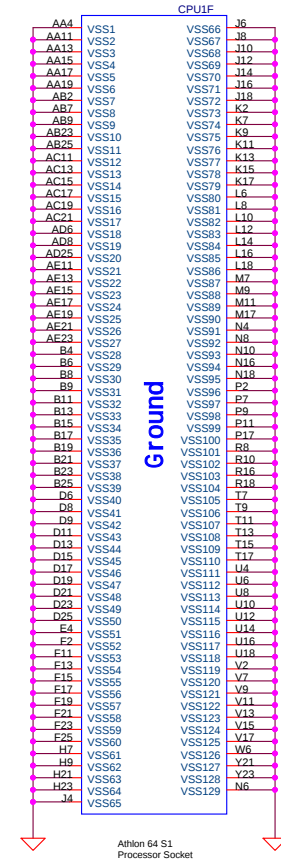
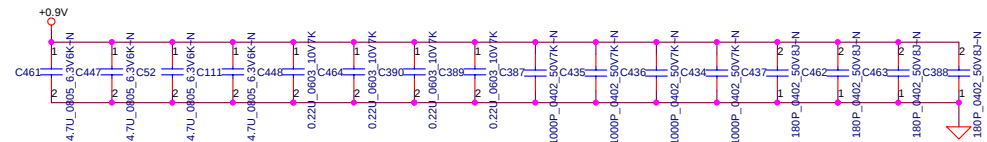
CPU BOTTOMSIDE DECOUPLING



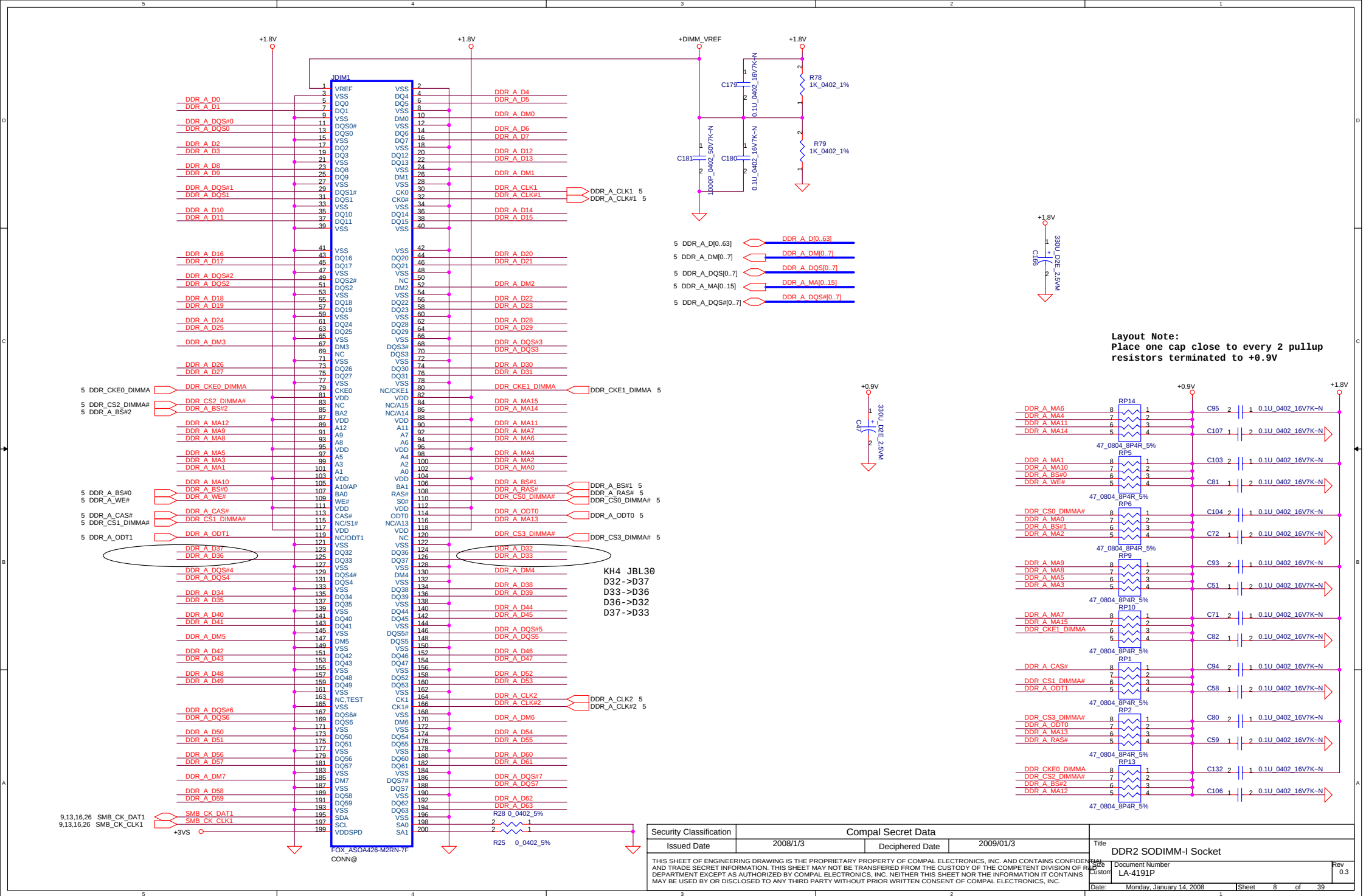
DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE

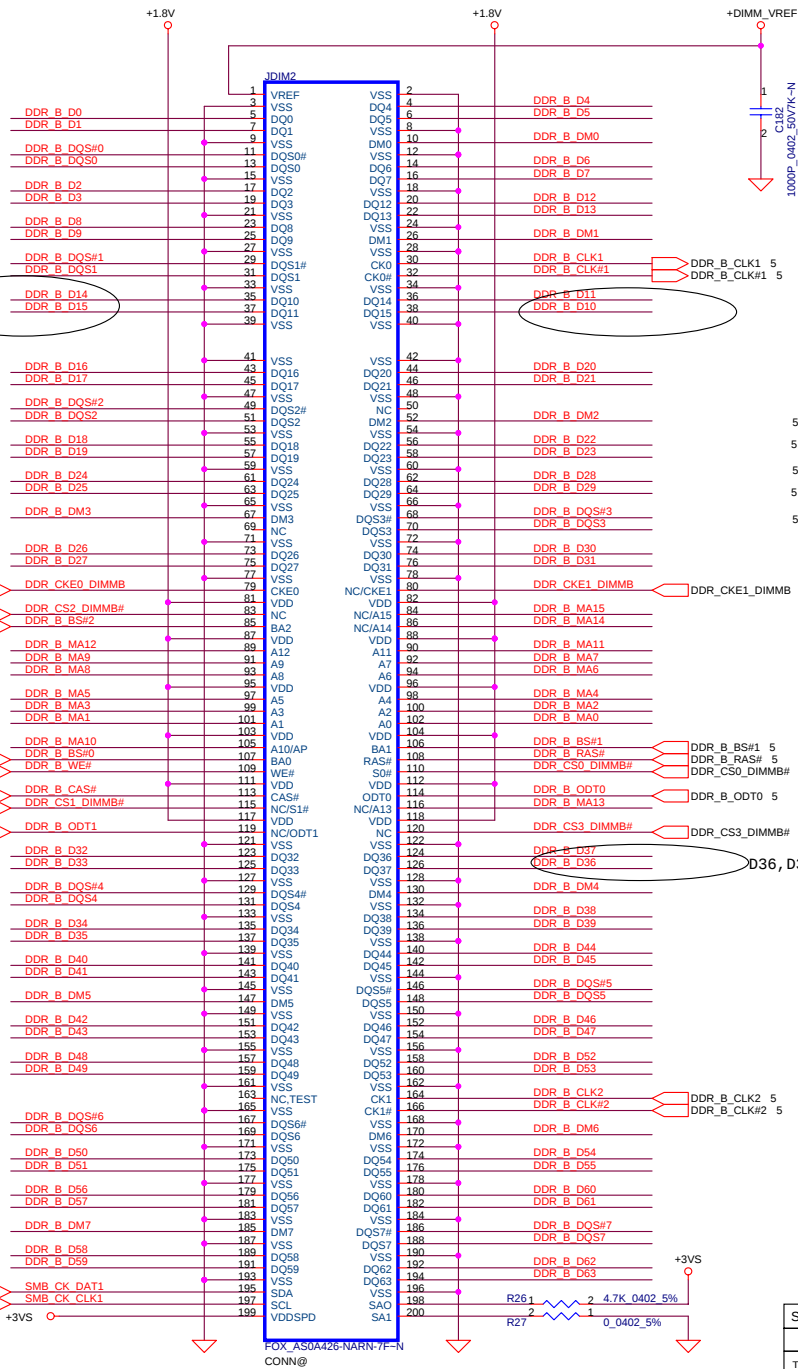


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KH4 JBL30
D10->D14
D11->D15
D14->D11
D15->D10

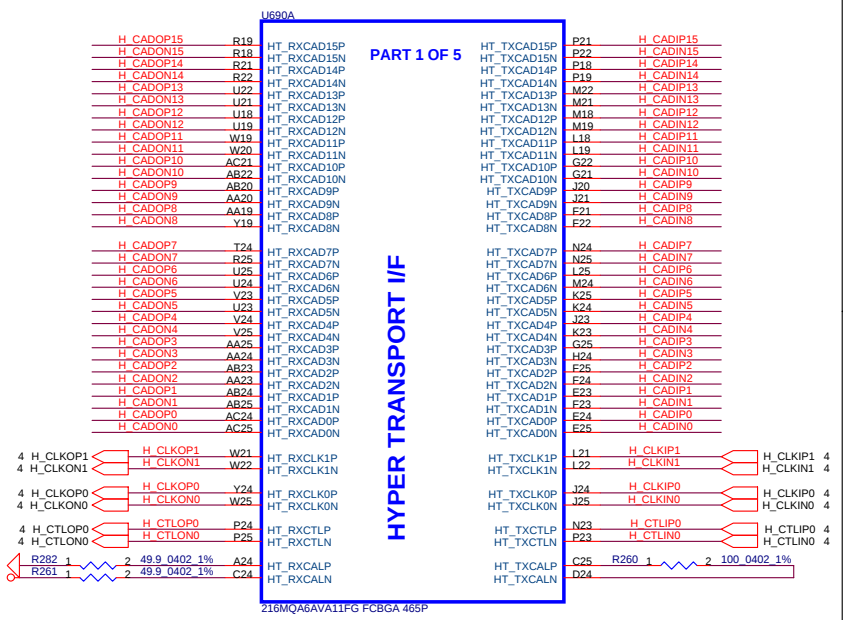
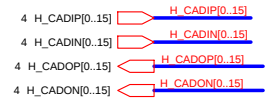
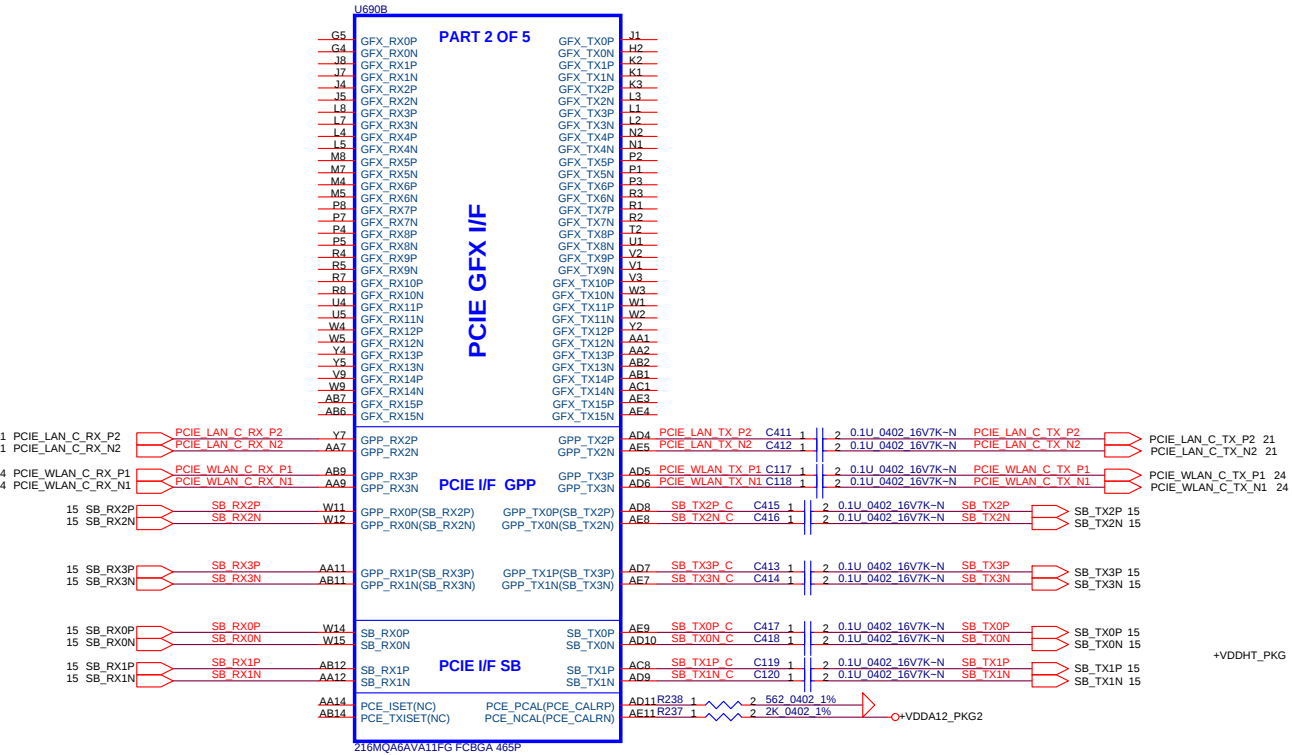
8.13.16.26 SMB_CK_DAT1
8.13.16.26 SMB_CLK1



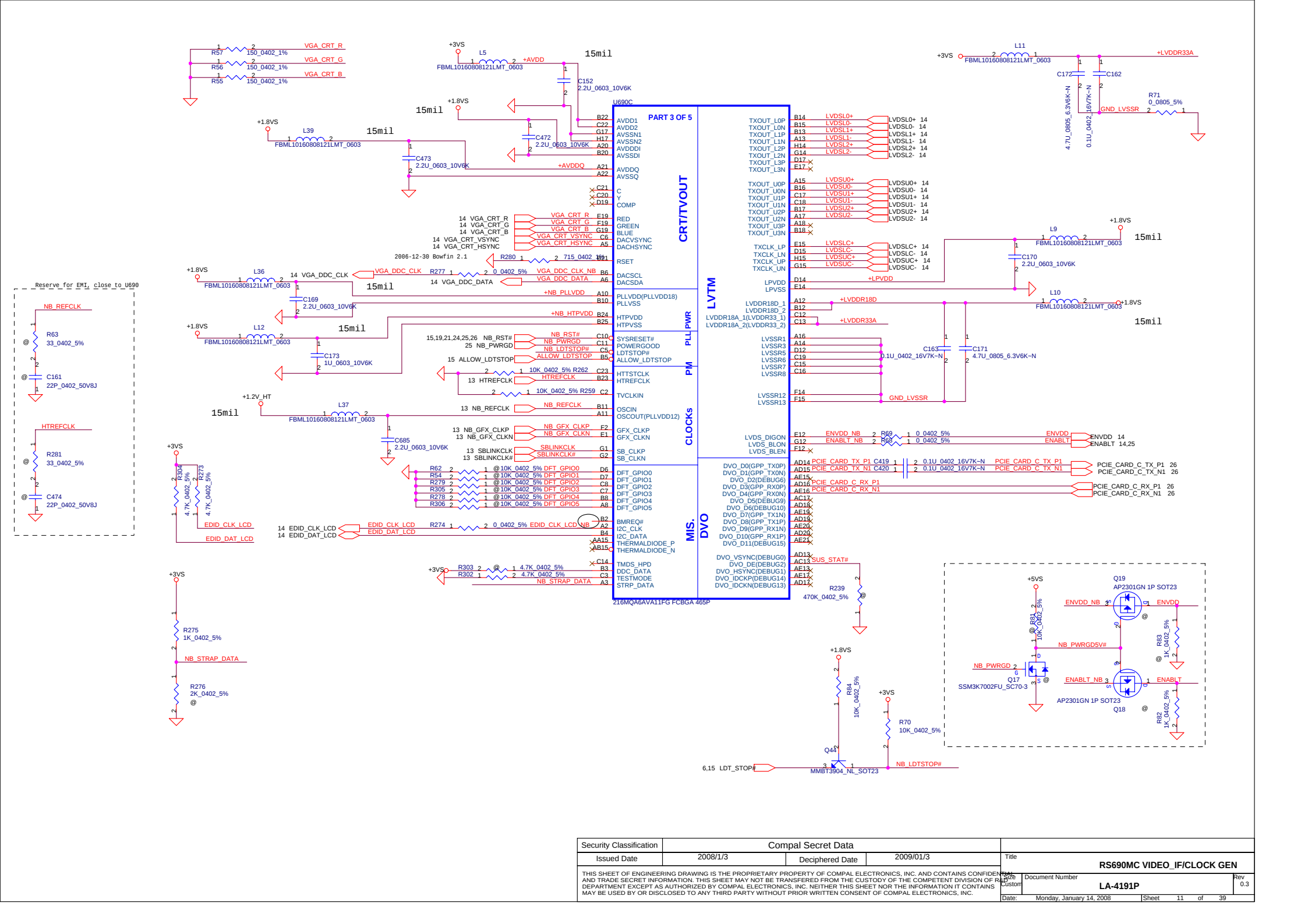
- 5 DDR_B_D[0..63] → DDR_B_D[0..63]
- 5 DDR_B_DM[0..7] → DDR_B_DM[0..7]
- 5 DDR_B_DQS[0..7] → DDR_B_DQS[0..7]
- 5 DDR_B_MA[0..15] → DDR_B_MA[0..15]
- 5 DDR_B_DQS# [0..7] → DDR_B_DQS# [0..7]

D36, D37 swap

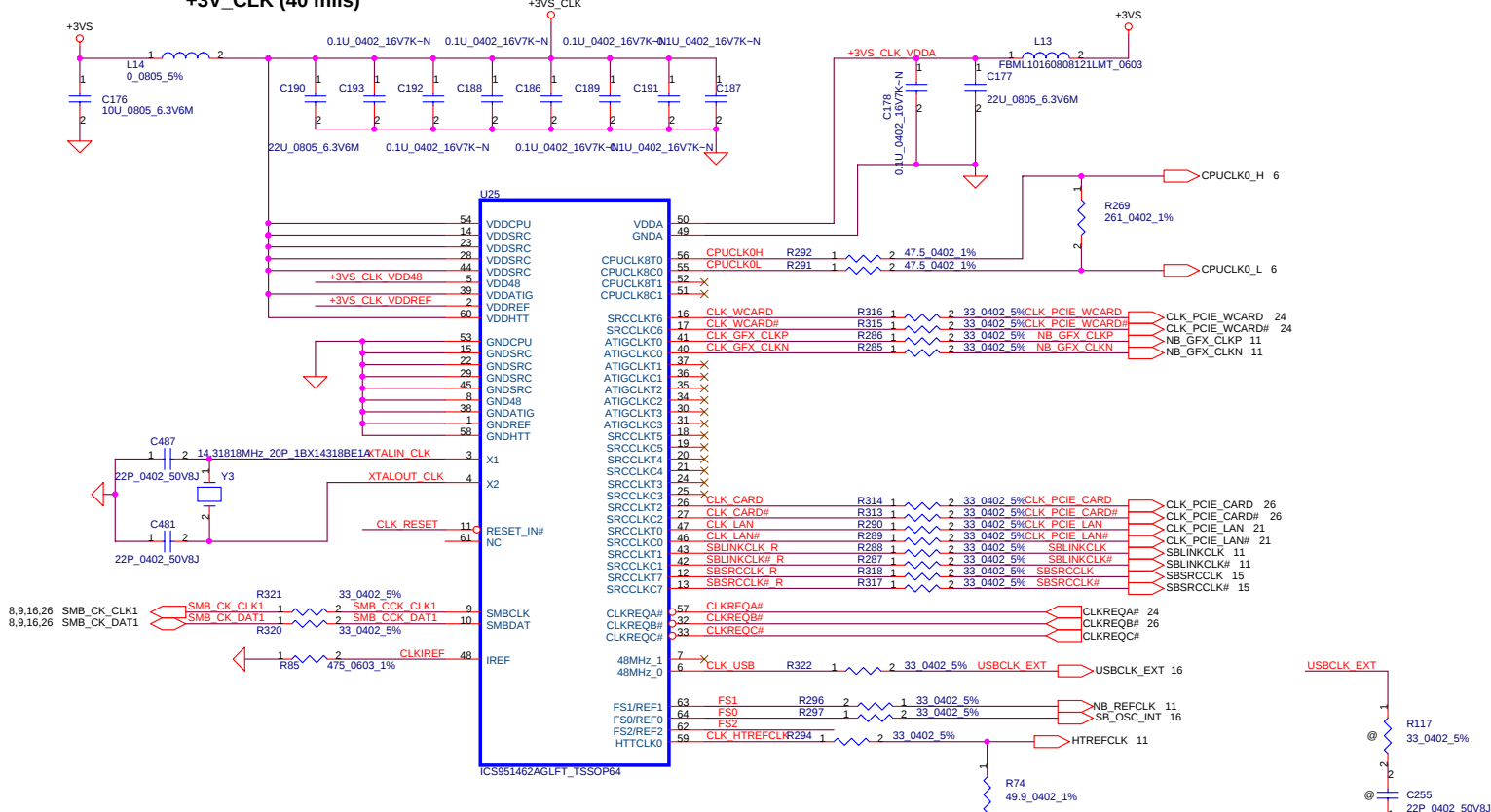
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Issued Date	2008/1/3	Deciphered Date	2009/01/3	DDR2 SODIMM-II Socket	
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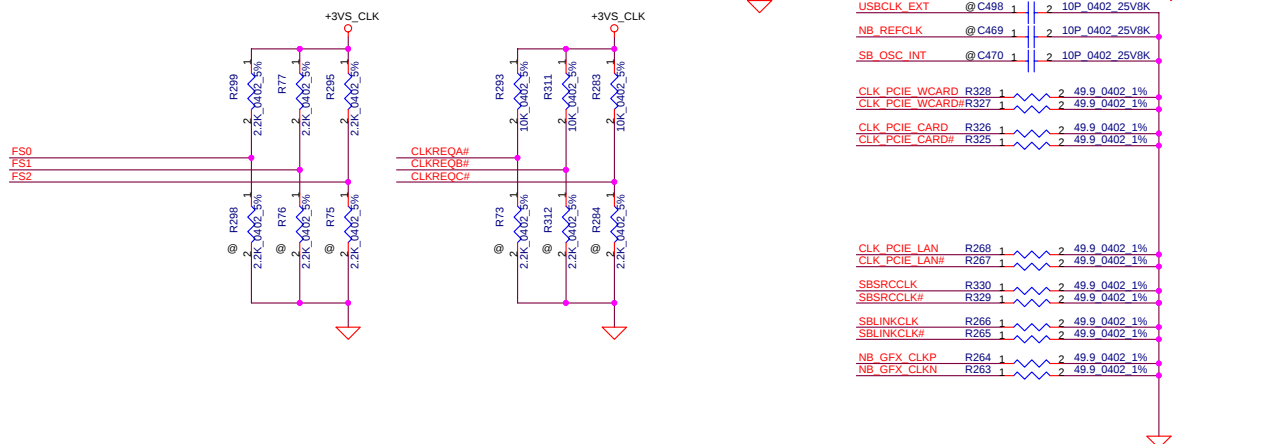


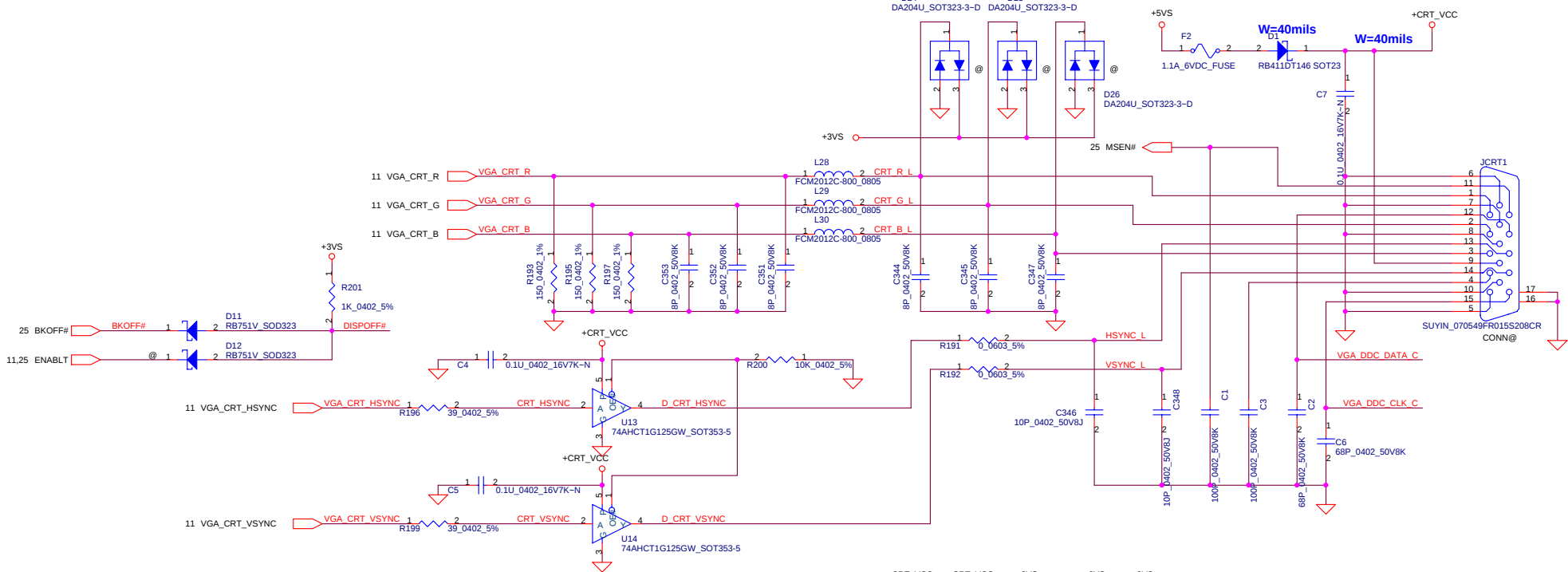
+3V_CLK (40 mils)



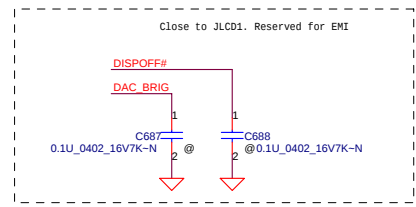
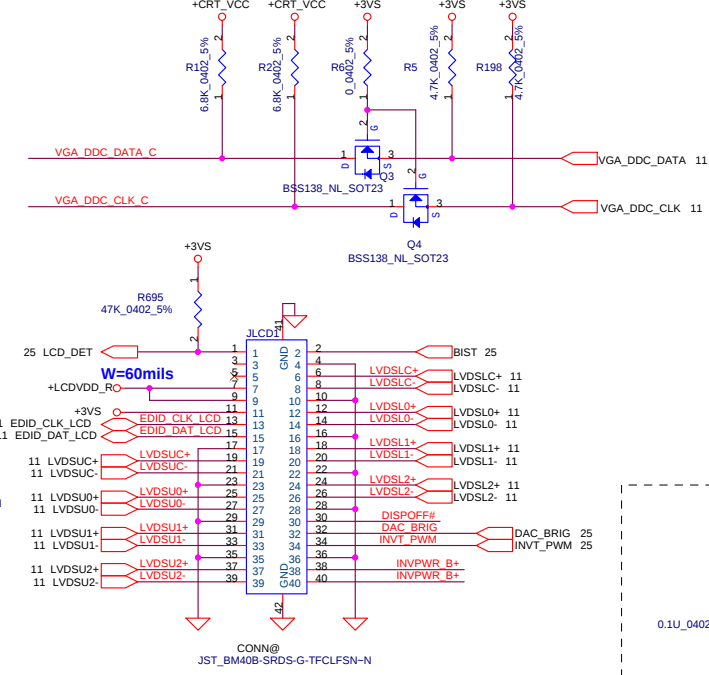
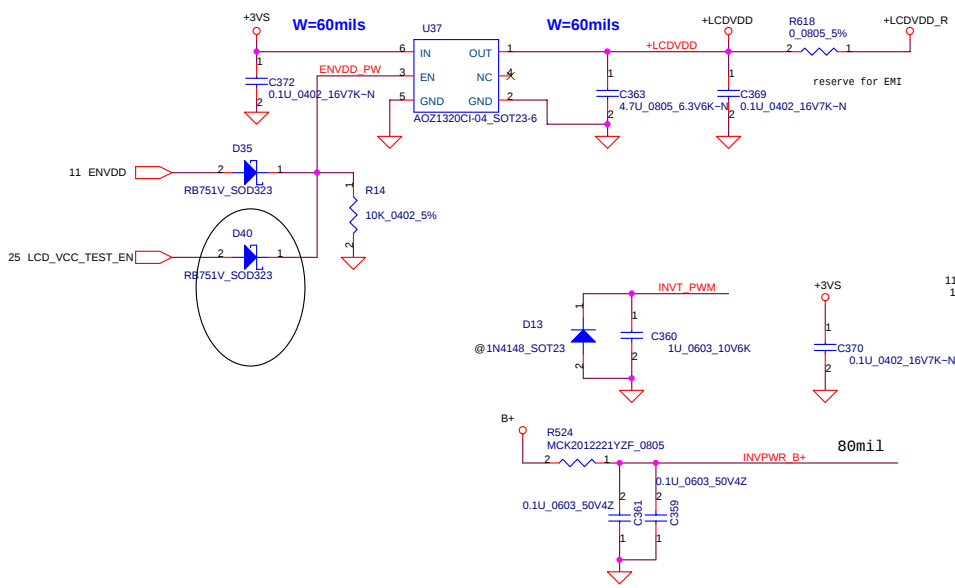
EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation





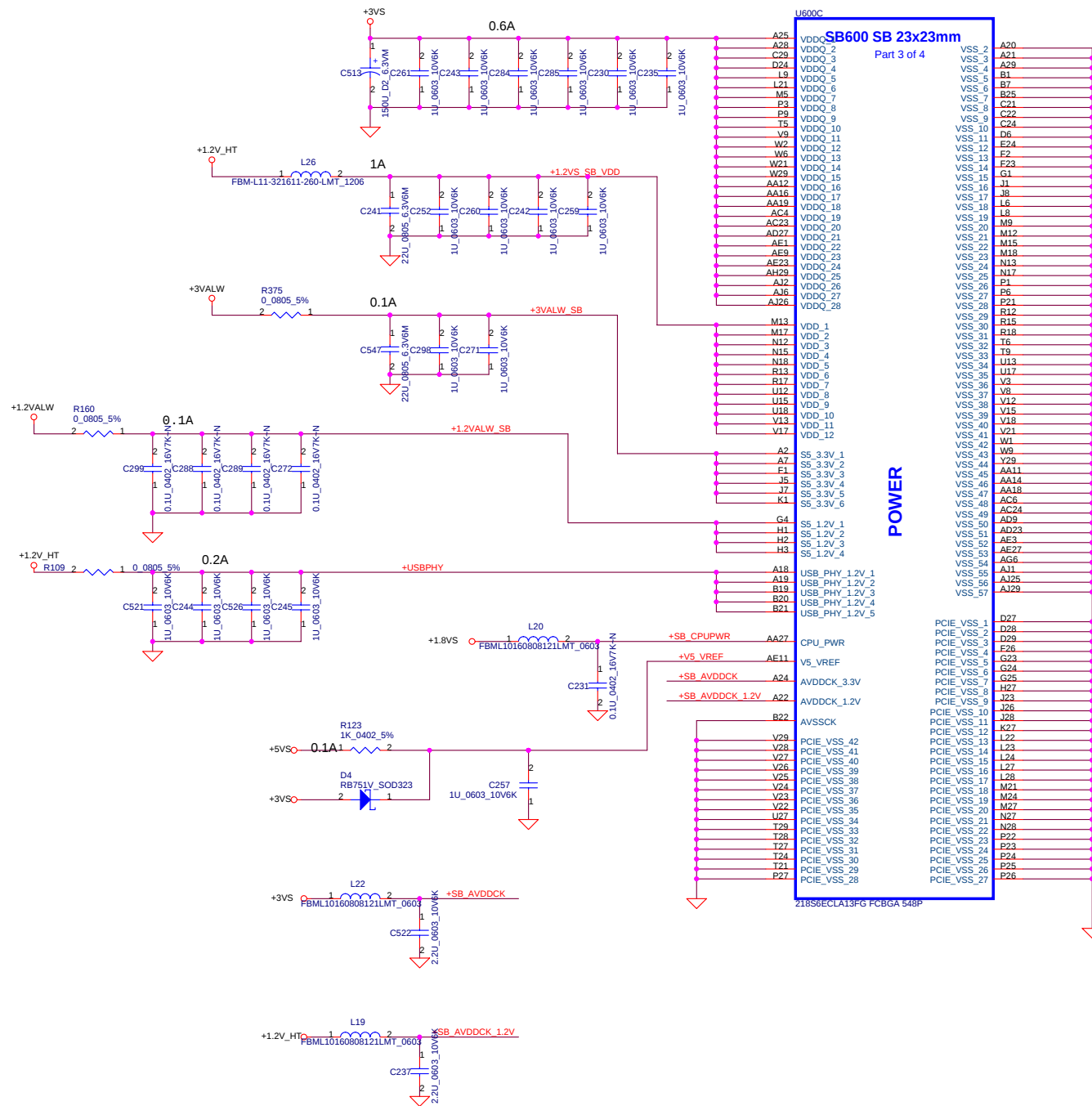
LCD POWER CIRCUIT



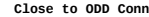
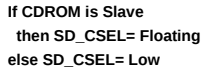
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CRT Conn.& LCD Conn.

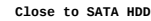
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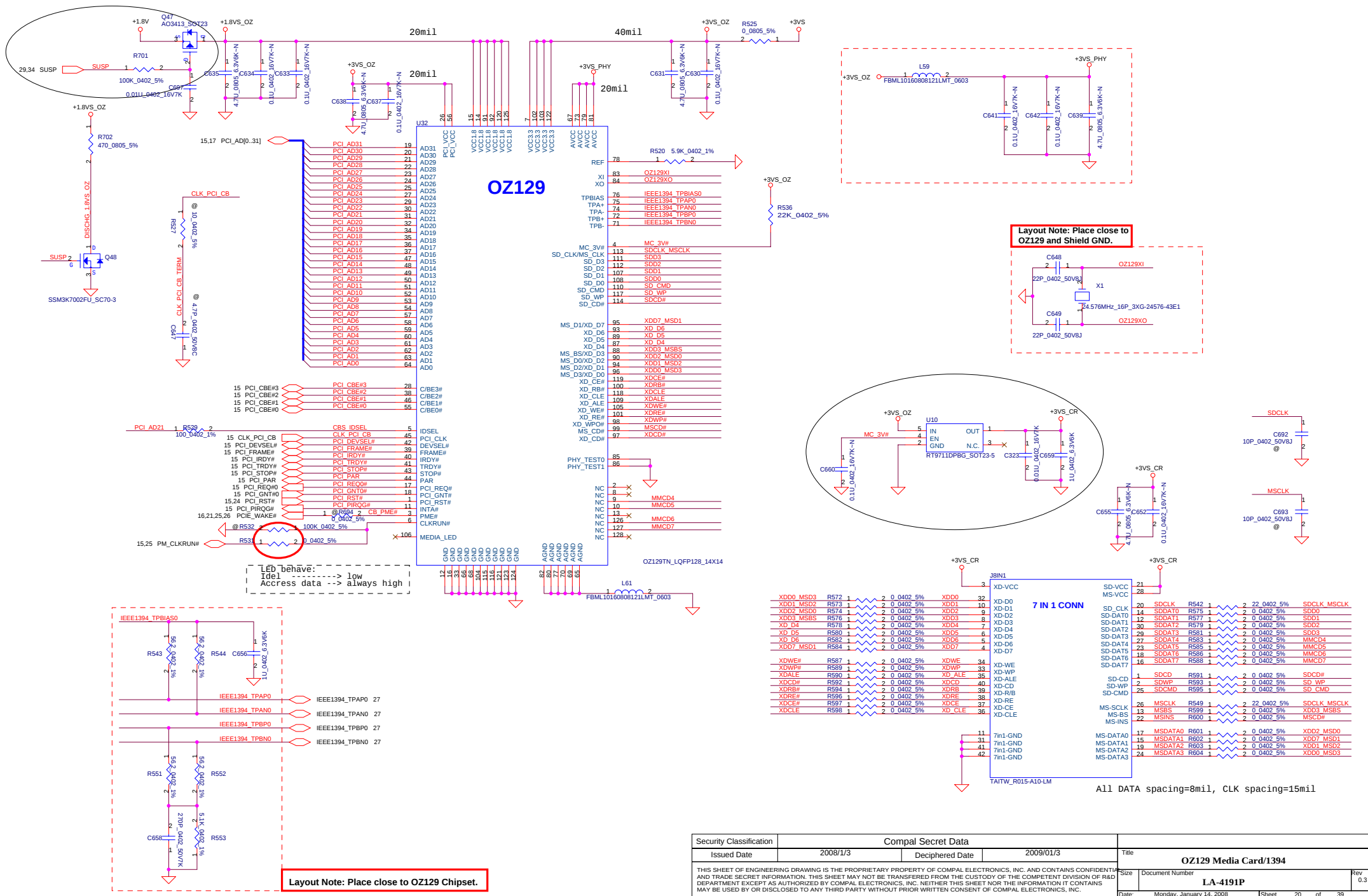
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Issued Date	2008/1/3	Deciphered Date	2009/01/3	SB600 Power/GND	
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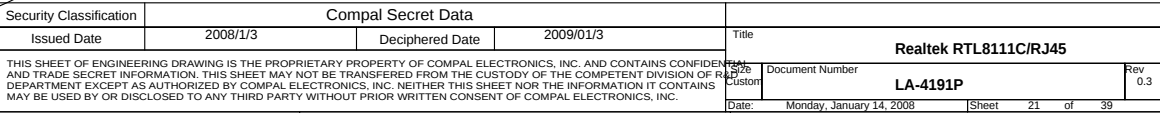


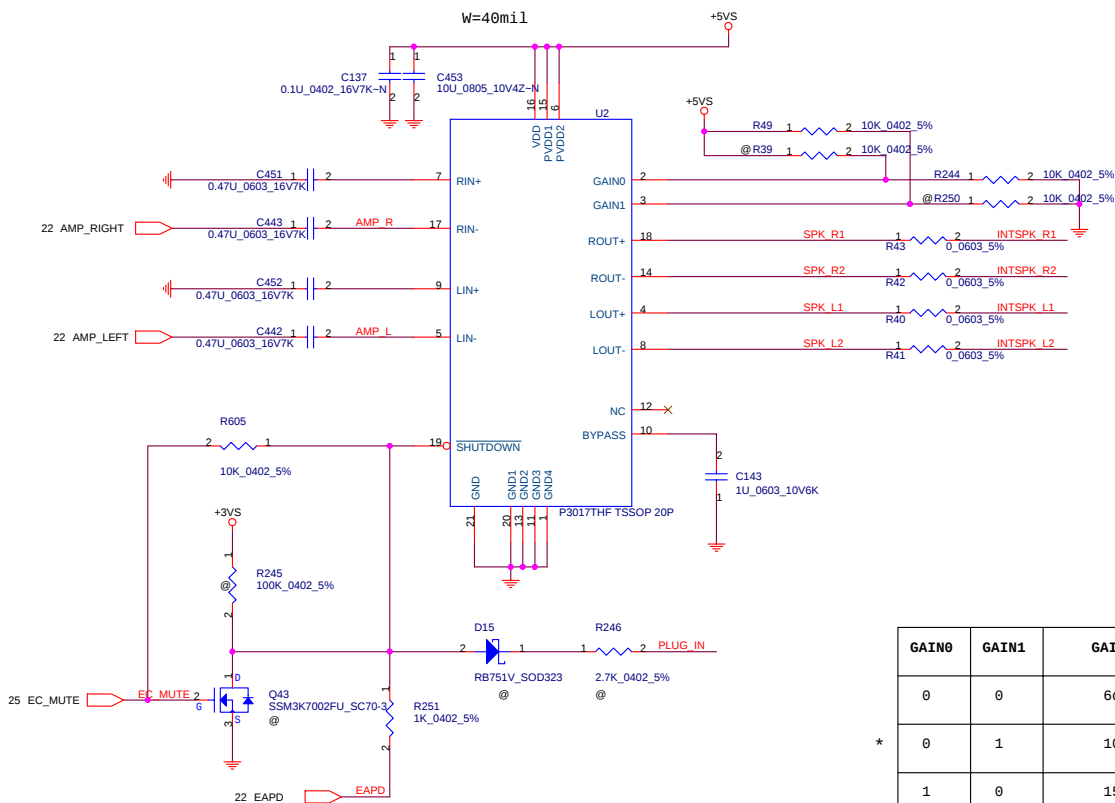
SATA HDD CONN



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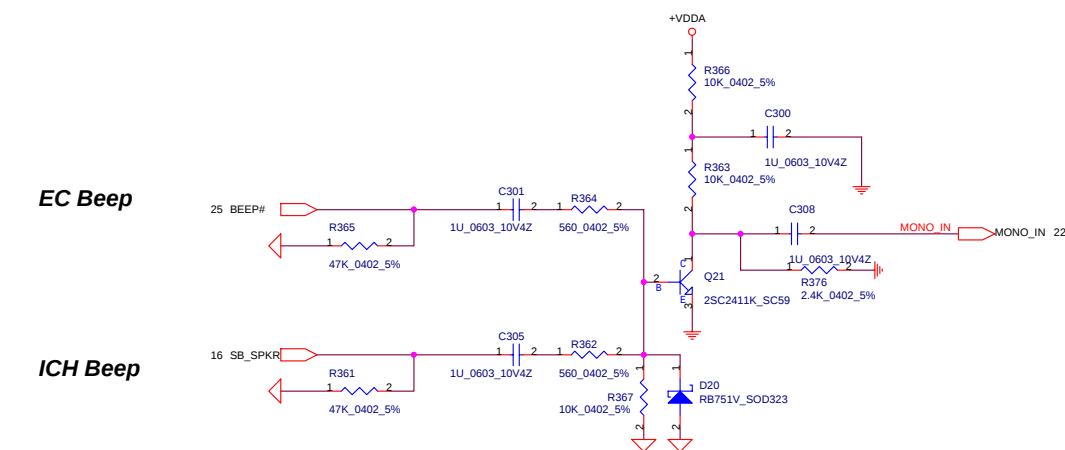




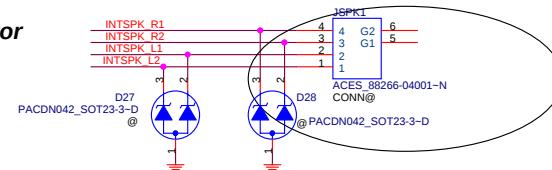


Buzzer need to support ICH/PCM_SPK/Battery_low and WL_on/off

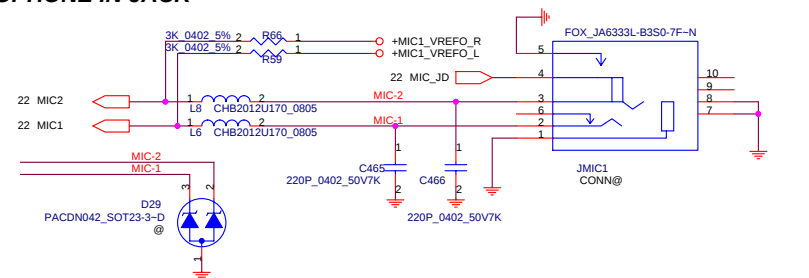
GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



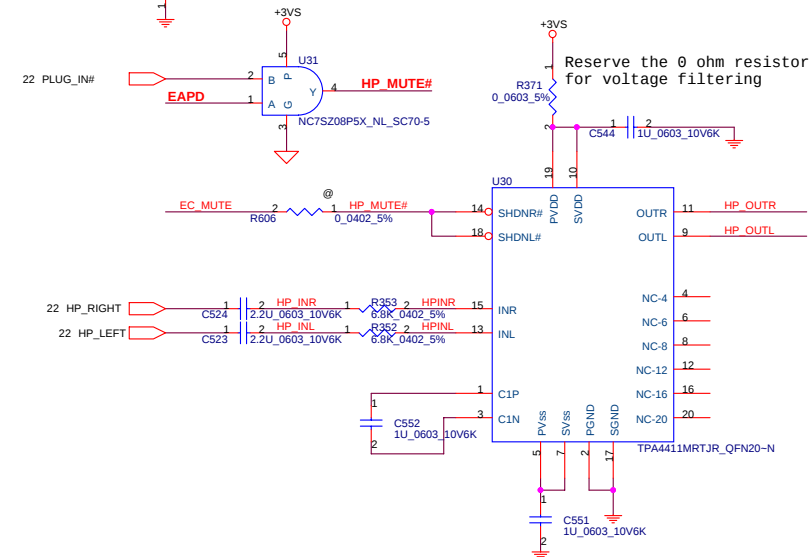
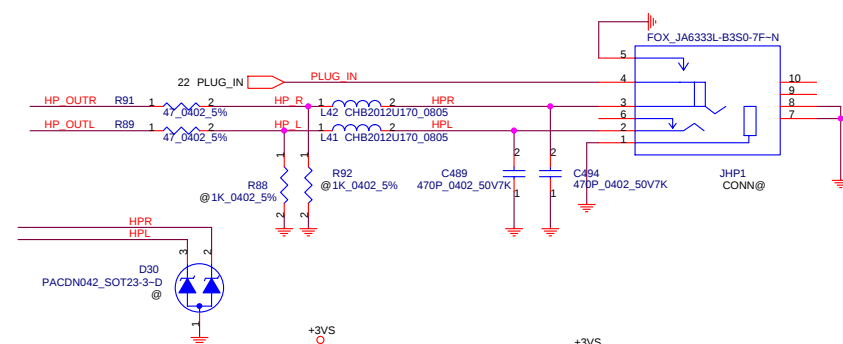
Speaker Connector

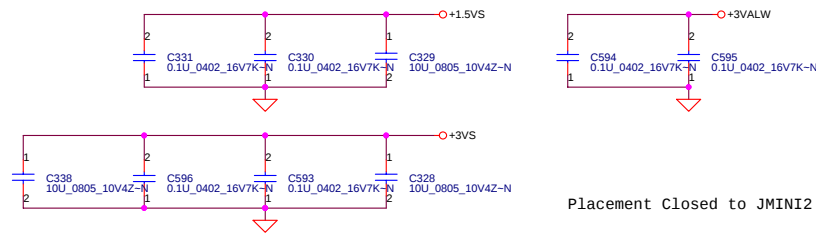


MICROPHONE IN JACK

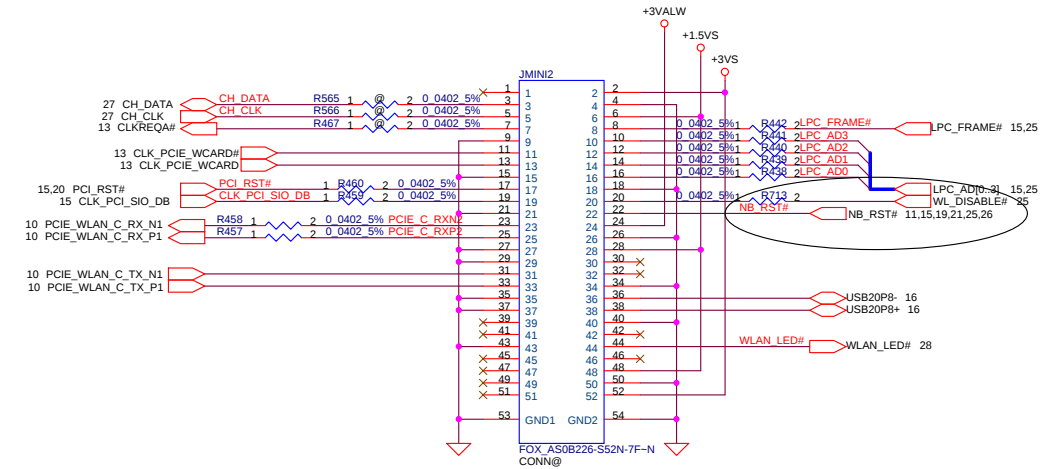


HEADPHONE OUT JACK

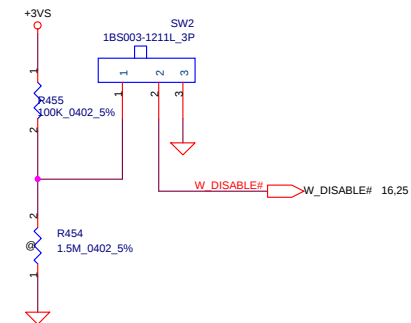




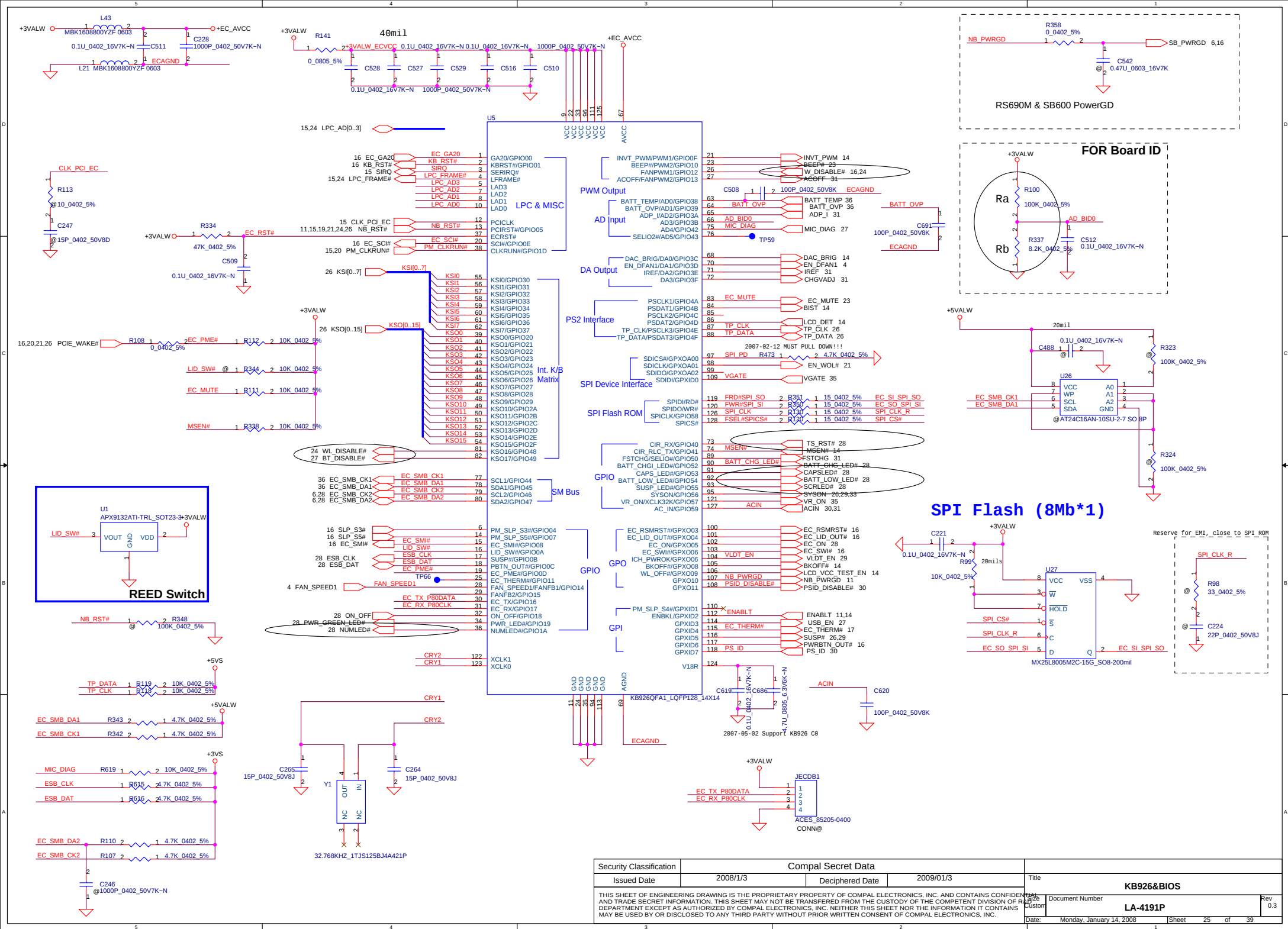
Mini-Express Card (WLAN)



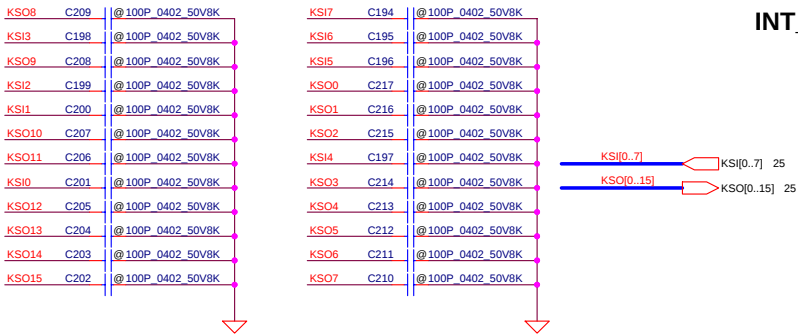
Wireless_BTN Killer switch



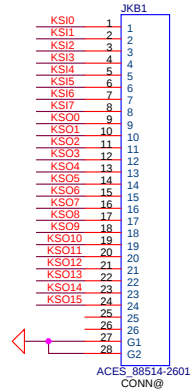
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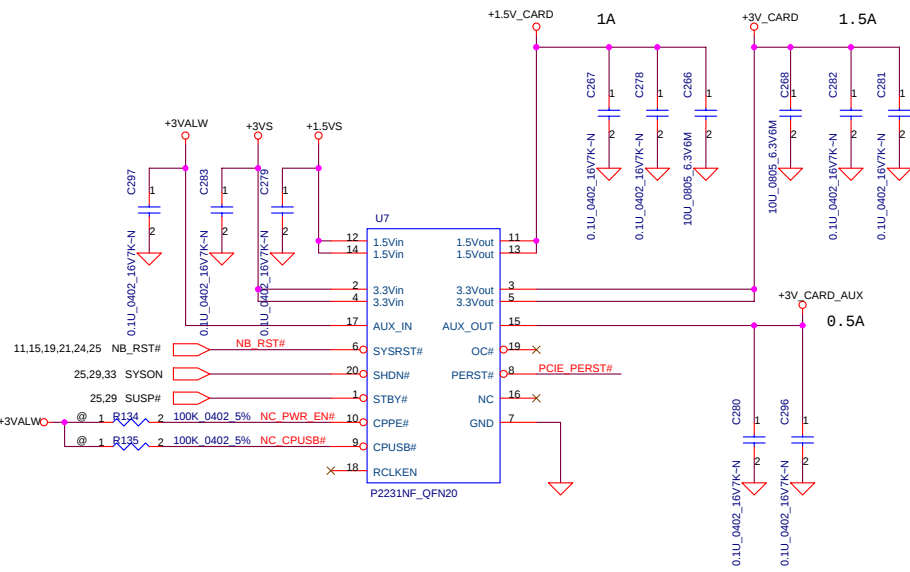
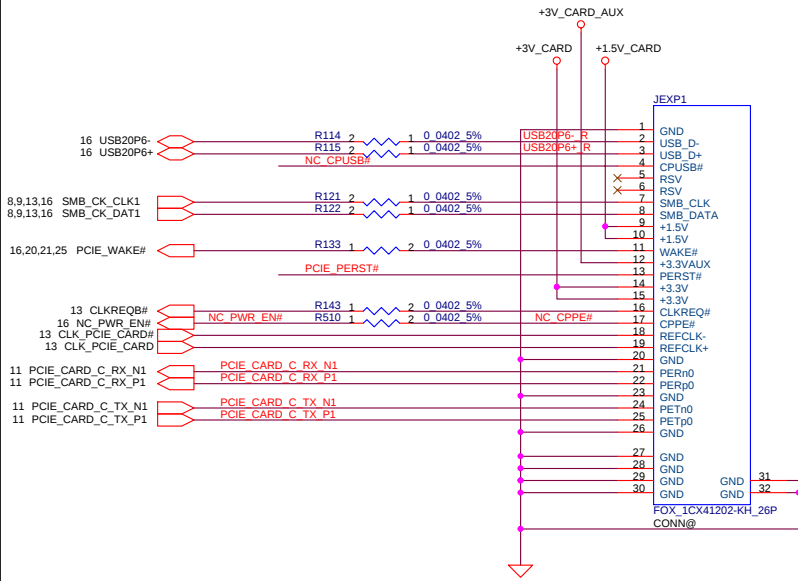
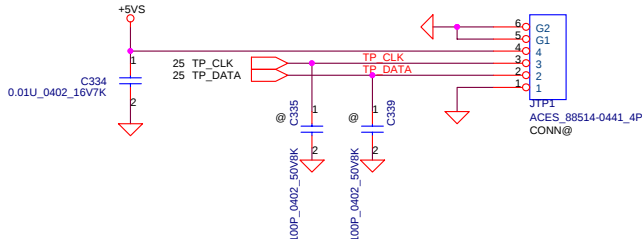
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Issued Date	2008/1/3		Deciphered Date		2009/01/3		Title	
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						Document Number		
						KB926&BIOS		
						Rev		
						0.3		
						LA-4191P		
						Date: Monday, January 14, 2008		
						Sheet 25 of 39		



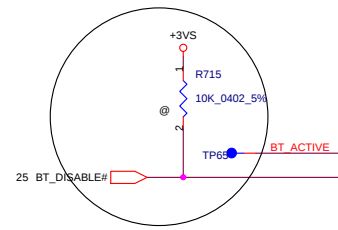
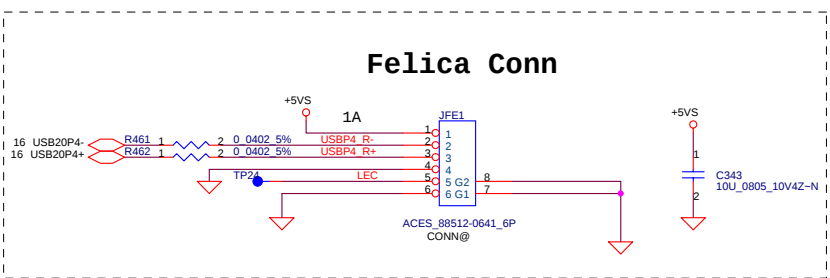
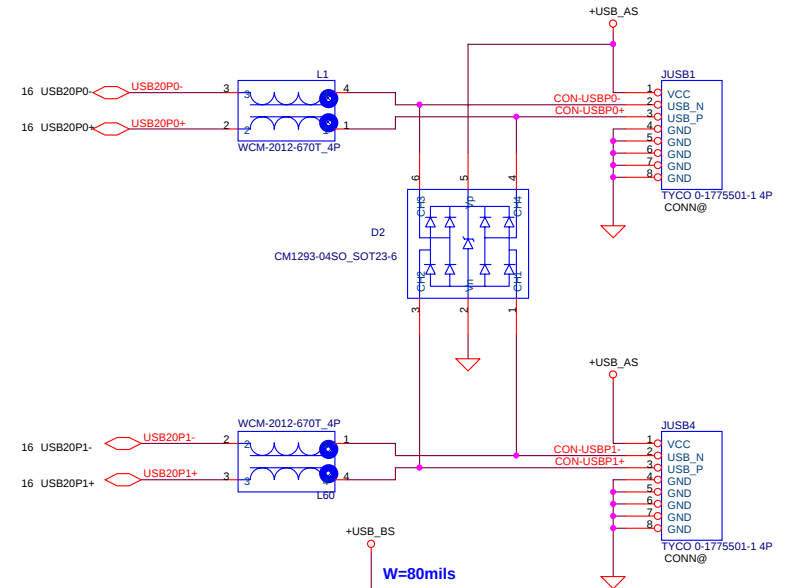
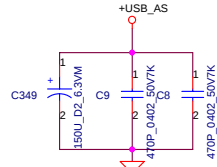
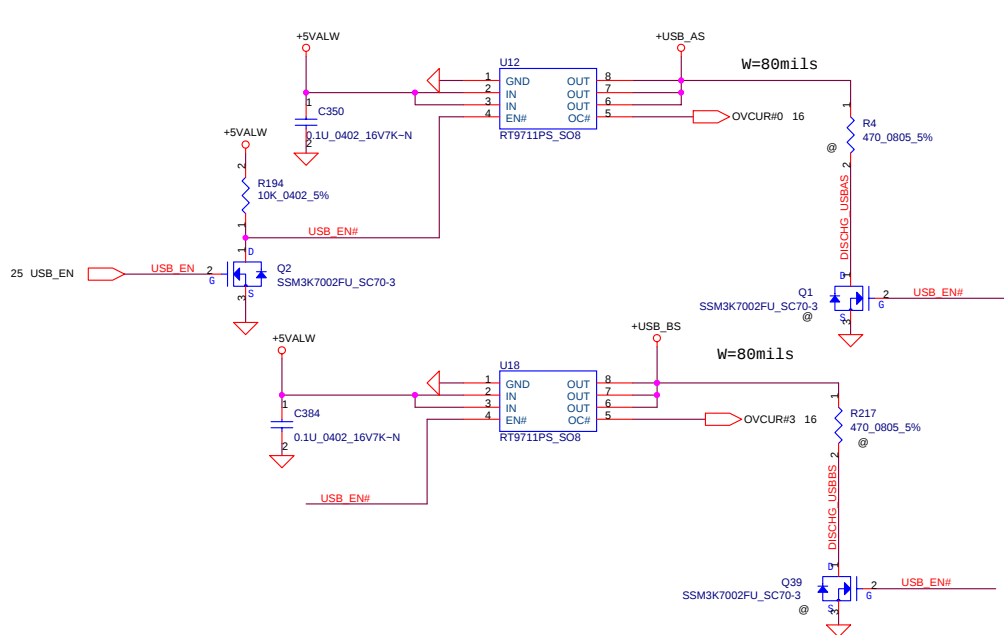
INT_KBD CONN.



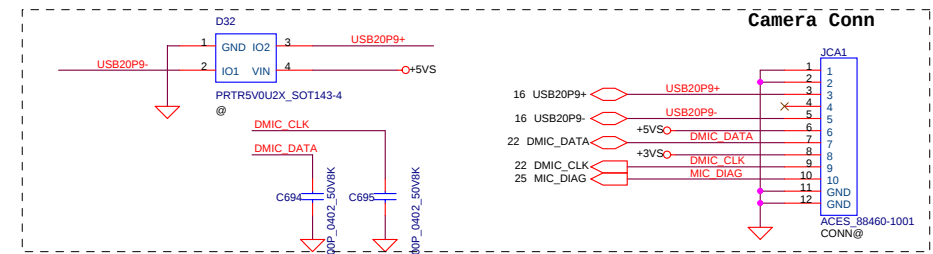
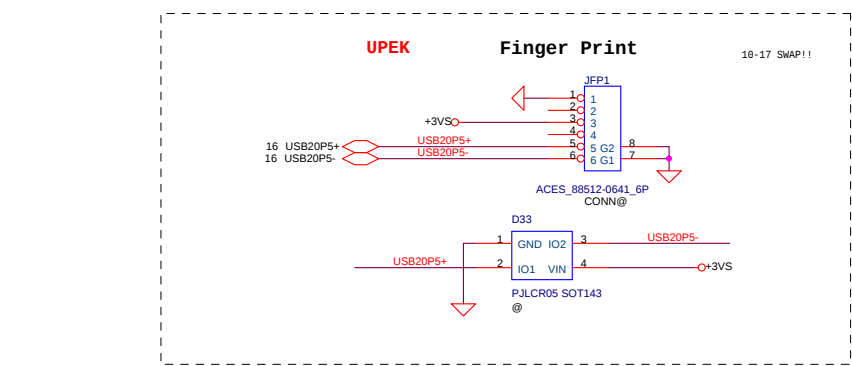
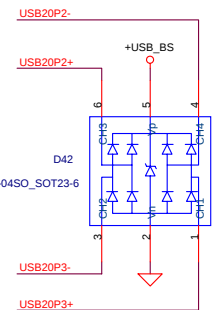
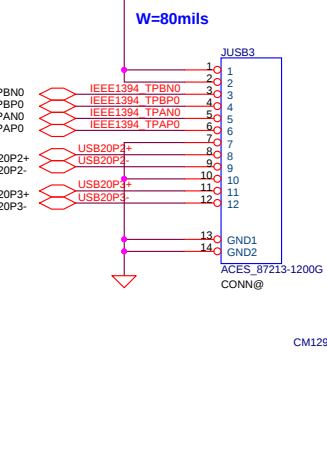
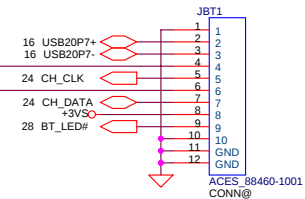
TouchPad TP/B TO M/B



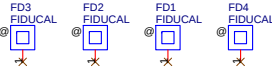
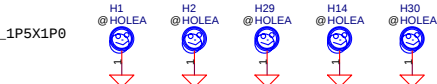
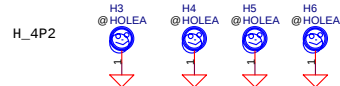
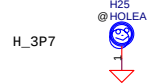
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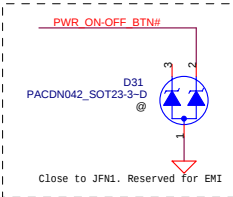
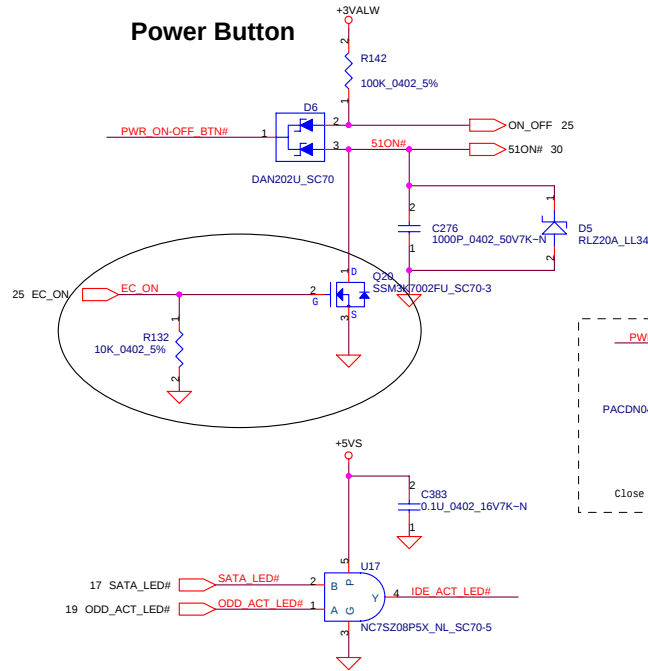
Bluetooth



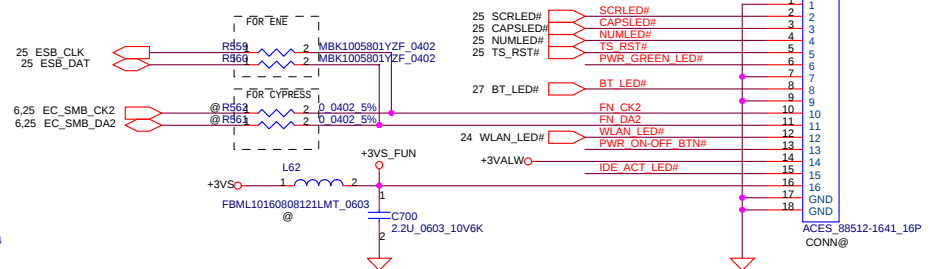
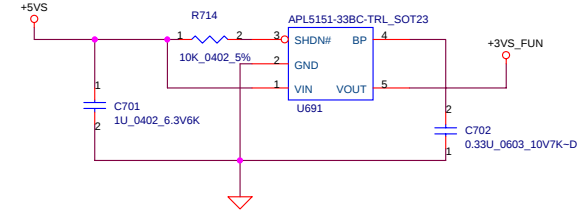
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Issued Date		2008/1/3		Deciphered Date		2009/01/3		Title			
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								Document Number		Rev	
								LA-4191P		0.3	
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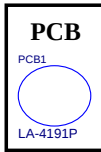
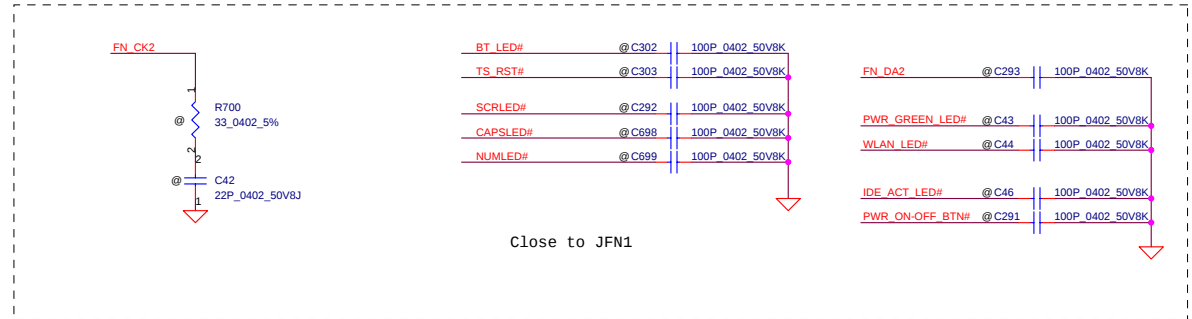
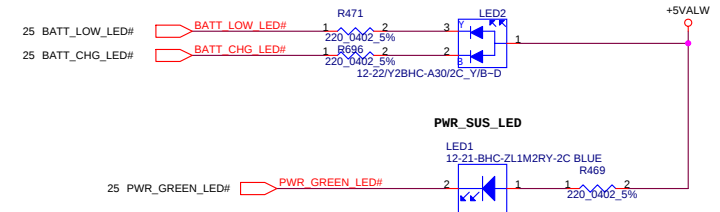
Power Button



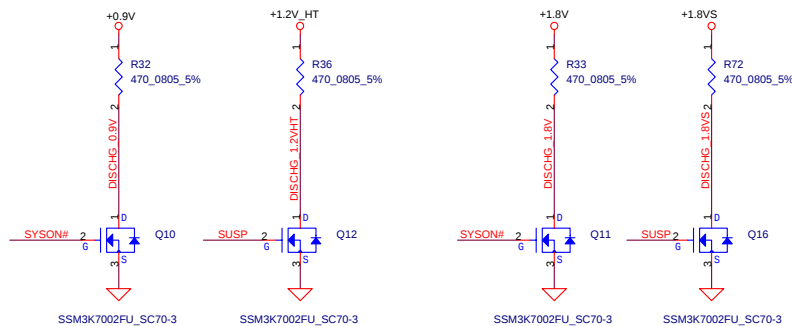
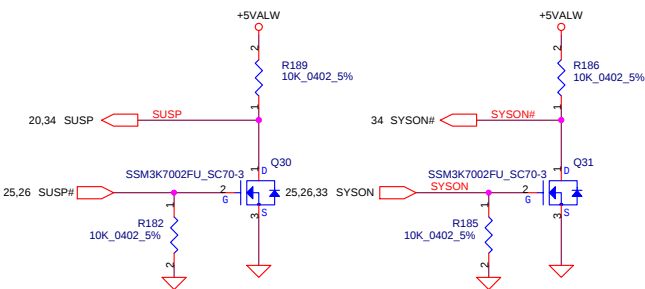
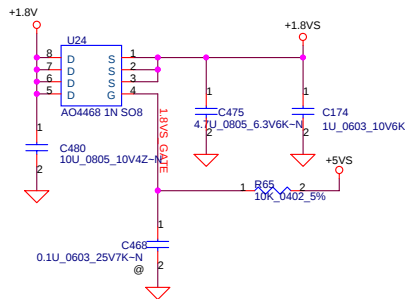
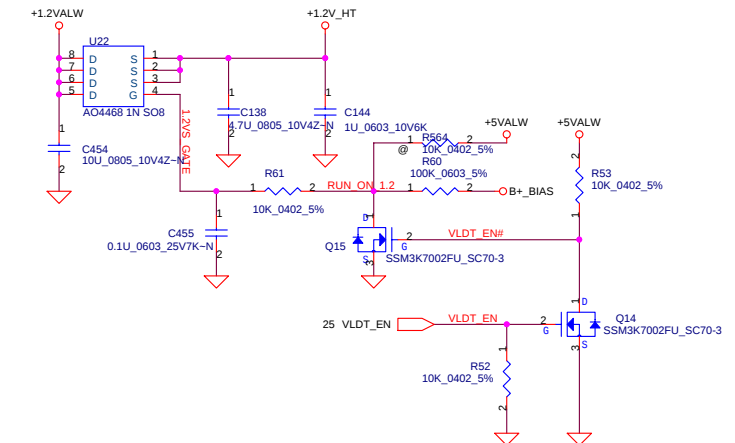
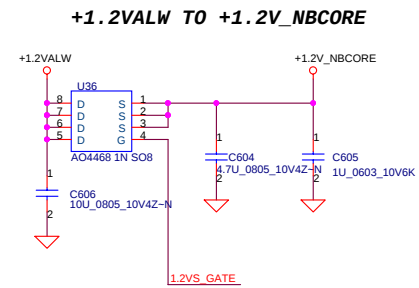
Regulator for ENE sensor



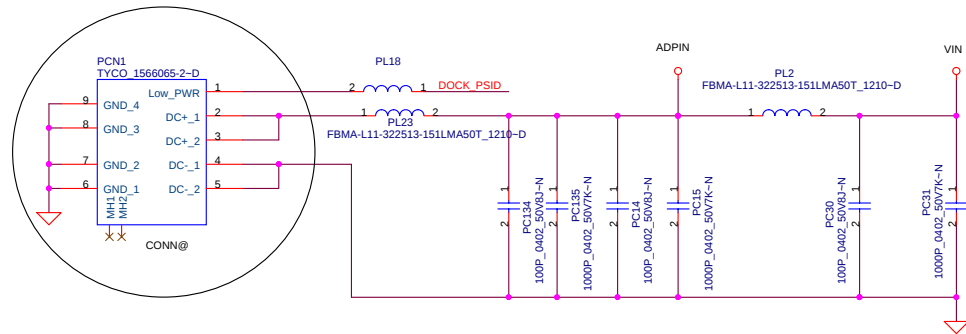
BATT_CHG_LED



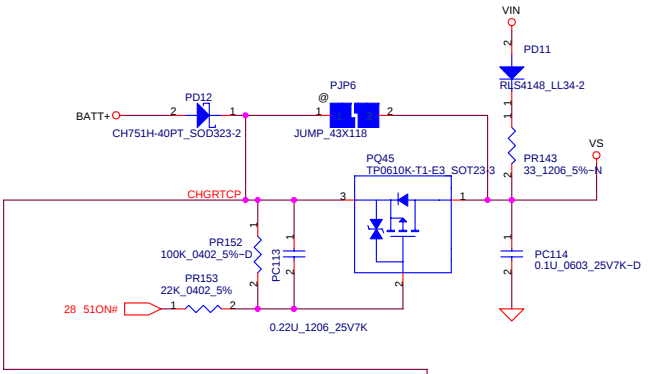
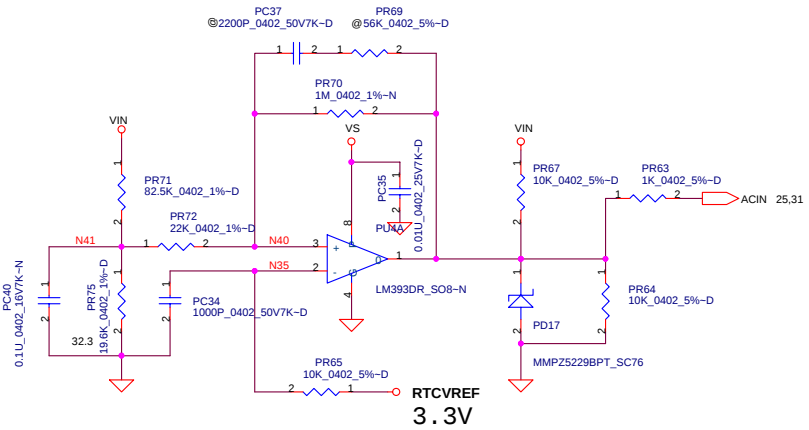
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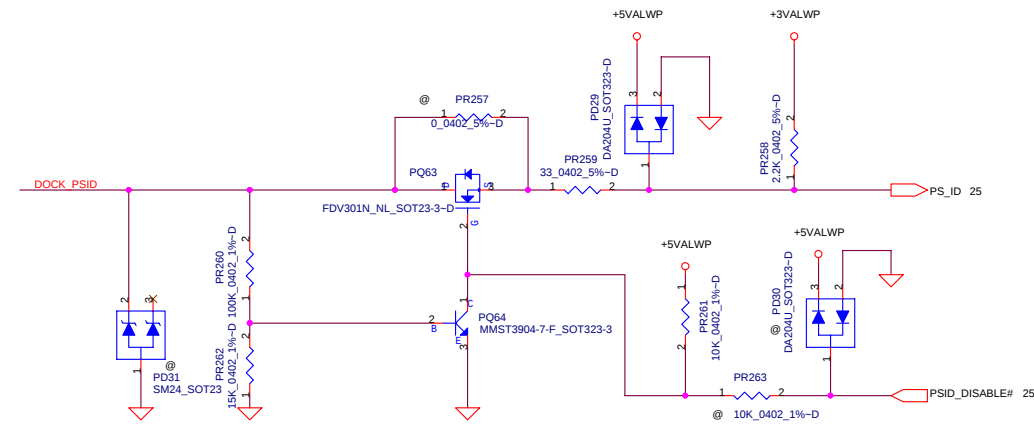
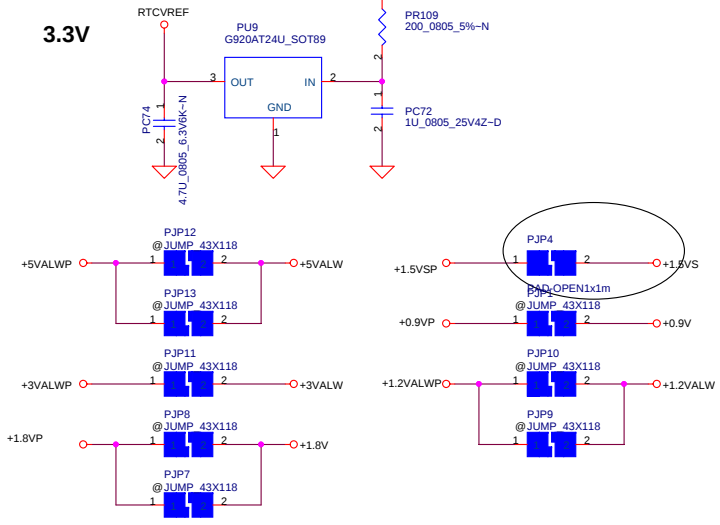
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Vin Detector			
	Max.	typ.	Min.
H-->L	18.234	17.841	17.449
L-->H	17.597	17.210	16.813

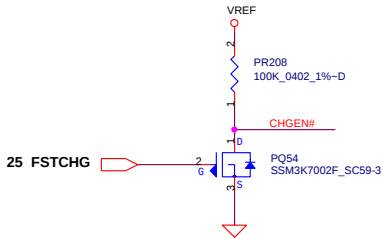
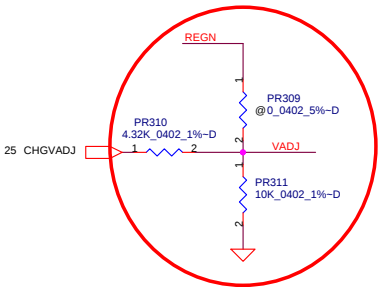
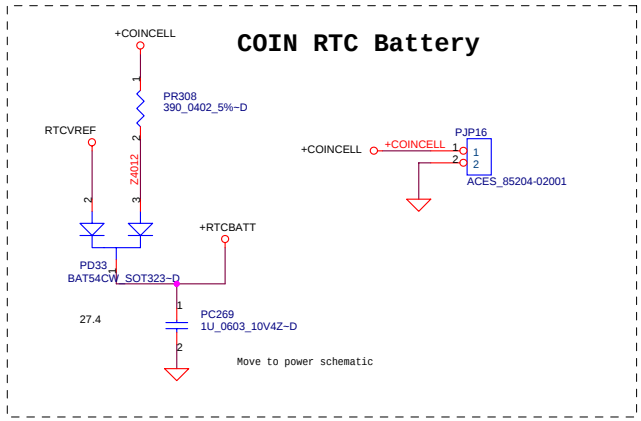
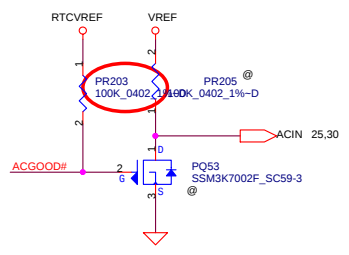
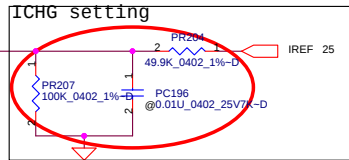
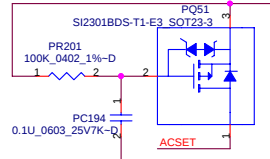
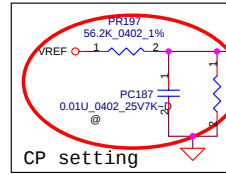
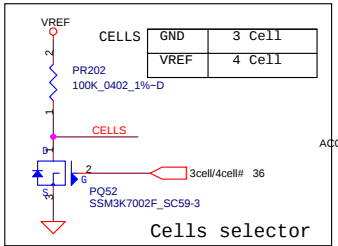


3.3V



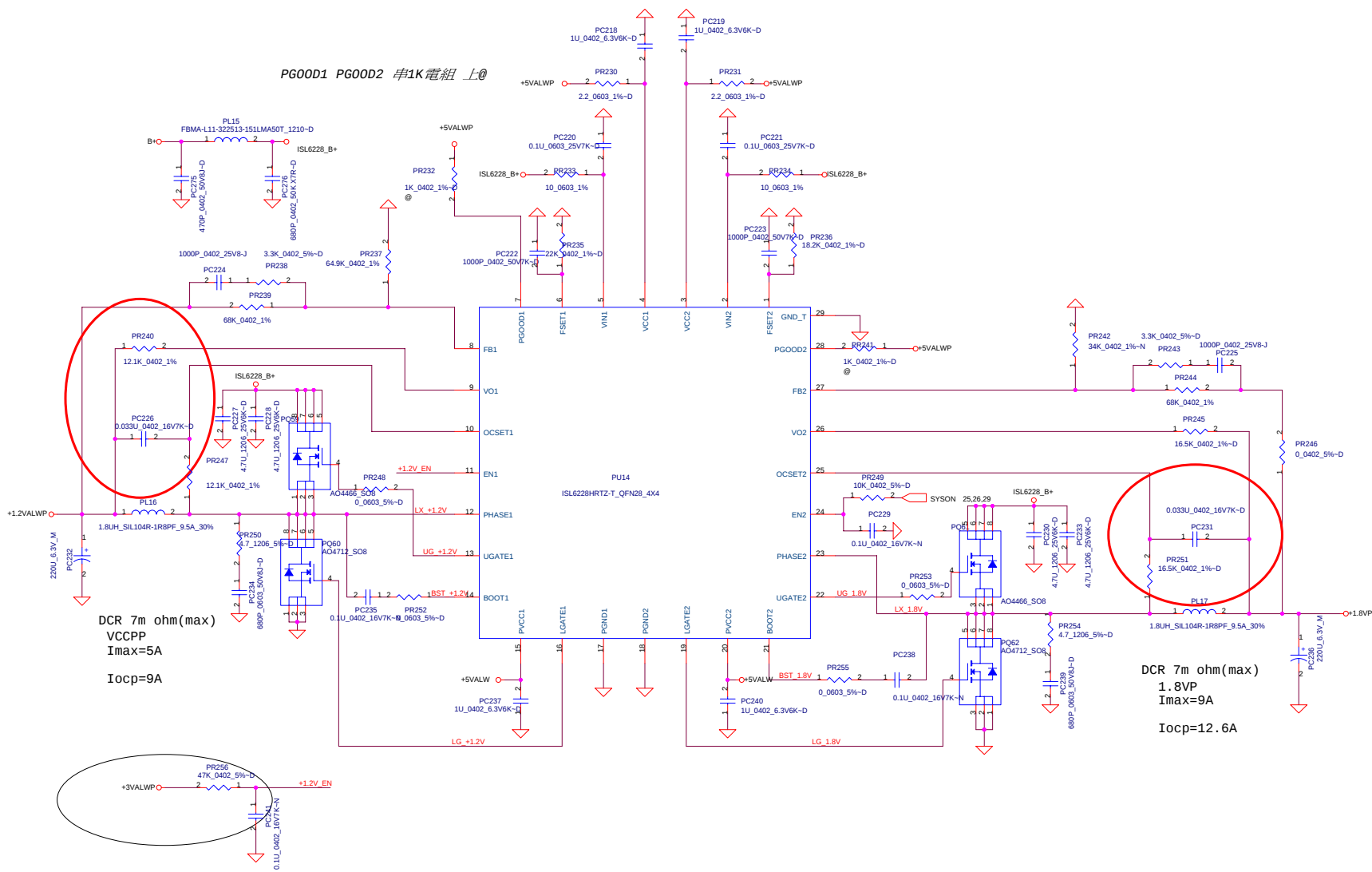
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Issued Date	2008/1/3	Deciphered Date	2009/01/3	DCIN / Precharge	
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90W adapter
 $I_{charge} = (V_{srset}/V_{vdac}) * (0.1/PR195) = 3.3A$
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR188) = 4.26A$
 Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz

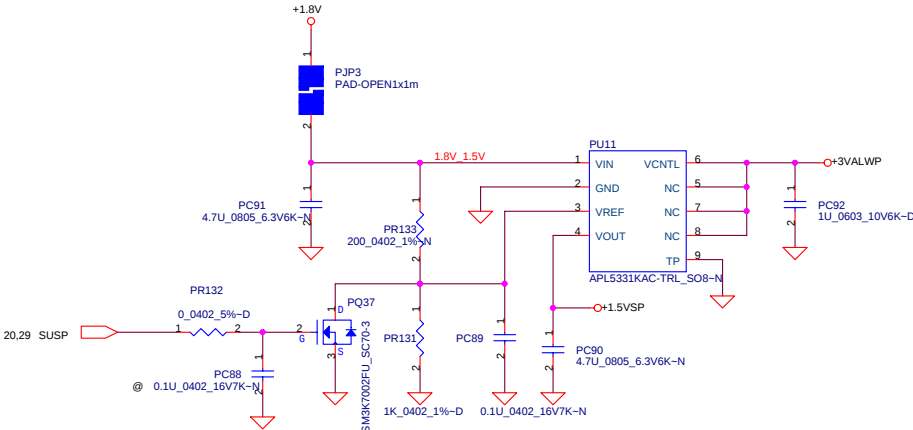
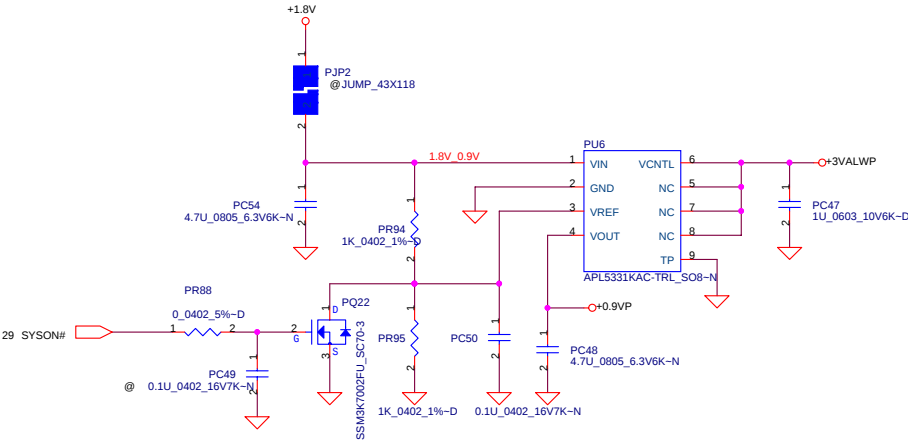


IREF	Current
3.265V	3.3A
0.49V	0.5A

PG00D1 PG00D2 串1K電組 上@

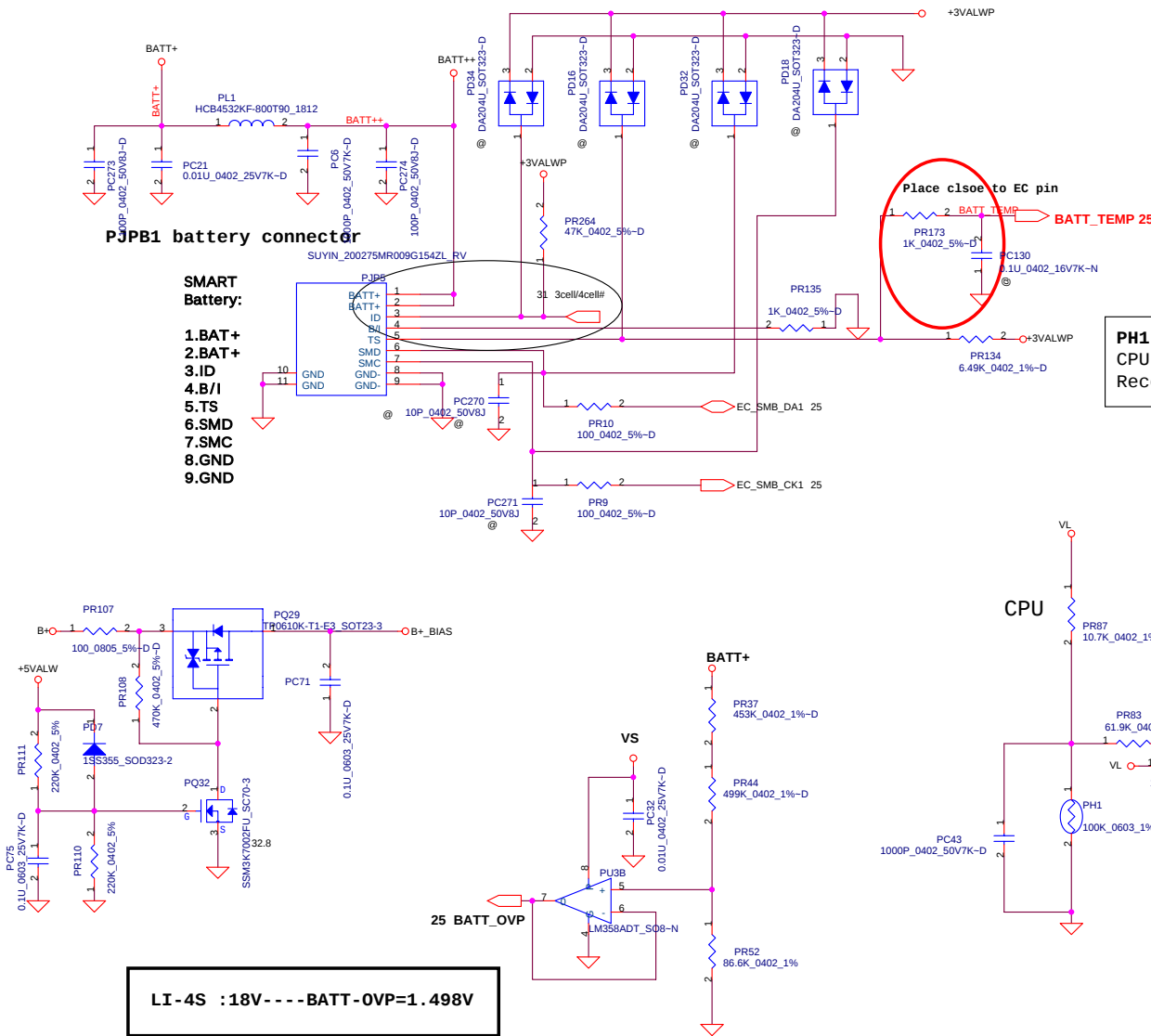


+1.5VSP/+0.9VSP



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Battery Connect/OTP



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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	31	Charge	08/01/04	COMPAL	adjust battery charge voltage set	CHANGE PR310 from 15K to 4.3K	
2	31	Charge	08/01/04	COMPAL	VIN Detector has the same function	DEL PR205 PQ53	
3	32	+3VALWP/+5VALWP	08/01/04	COMPAL	When in the DC-mode , shut down the system ,5valwp output not turn off	ADD PD35 to turn off 5VALWP wehn shut down the system in the DC-mode	

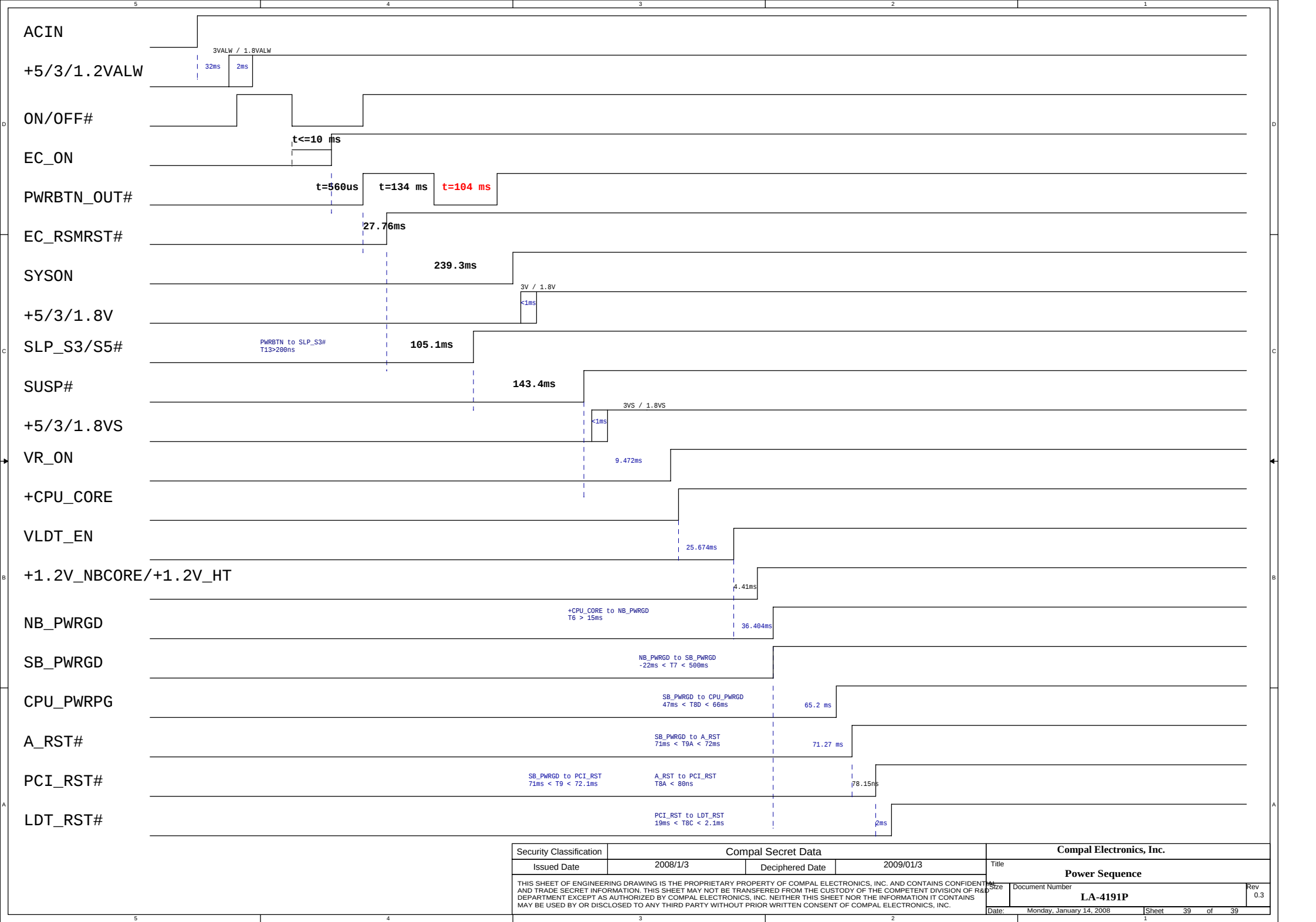
Next: PR238, PC202, PQ56, PD42, PJP21

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Compal Electronics, Inc.		
Title EE-PIR		
Drawing Number LA-4191P		Rev 0.3
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List
1	Fine-tune CPU_PWRGD, LDT_STOP#, LDT_RST#	Fine-tune CPU_PWRGD, LDT_STOP#, LDT_RST#	0.2	6	Delete CPU testpad
2		Reserve LCD enable from EC for test panel function	0.2	14	Add BIST and LCD_DET and LCD_VCC_TEST_EN from EC
3		Change RTC battery to cable type, also change to PWR portion	0.2	15	
4		Change CLK_PCI_TPM and CLK_PCI_EC to PCICLK5 and 6 (ATI recommend)	0.2	15	
5		Modify Media card circuit to 0Z129	0.2	20	Modify Media card circuit to 0Z129
6		Change Audio codec LDO to RT9198-4GPBG	0.2	22	Change Audio codec LDO to RT9198-4GPBG
7		USB port power control by EC	0.2	27	USB_EN(High=Enable)
8		CAPS, NUM, SCR LED control change from touch sensor to EC	0.3	28	
9		RTL8102E ver.B have E-fuse to flash MAC address.	0.3	21	U16 change to DNI (@)
10		Change RJ45 connector to include LED type.	0.3	21	
11					
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								Size	Document Number			Rev	
									LA-4191P			0.3	
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